COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JULY 1976

HOW COMPUTERS CAN TEST THEIR OWN MEMORIES

ASSOCIATIVE PROCESSORS: A PANACEA OR A SPECIFIC?

SYSTEM LANGUAGES FOR MICROPROCESSORS: CONSIDERATIONS AND TRENDS

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- All models are available with either 7 or 9 track, 800 NRZI, 1600 PE or 800/1600 NRZI/PE.
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The Model T-1202 is the newest member of the T-1000 Series —Tally's fine line of serial printers that offer microprocessor electronics, low acoustic noise level, digitally controlled print head advancement, dual tractor engagement and a convenient snap-in ribbon cartridge.

There's more to tell, so call your nearest Tally sales office. Tally Corporation, 8301 S. 180th Street, Kent, WA 98031, Phone (206) 251-5524.

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CIRCLE 3 ON INQUIRY CARD

THE
MAGAZINE
OF DIGITAL
ELECTRONICS

COMPUTER DESIGN

JULY 1976 • VOLUME 15 • NUMBER 7

FEATURES

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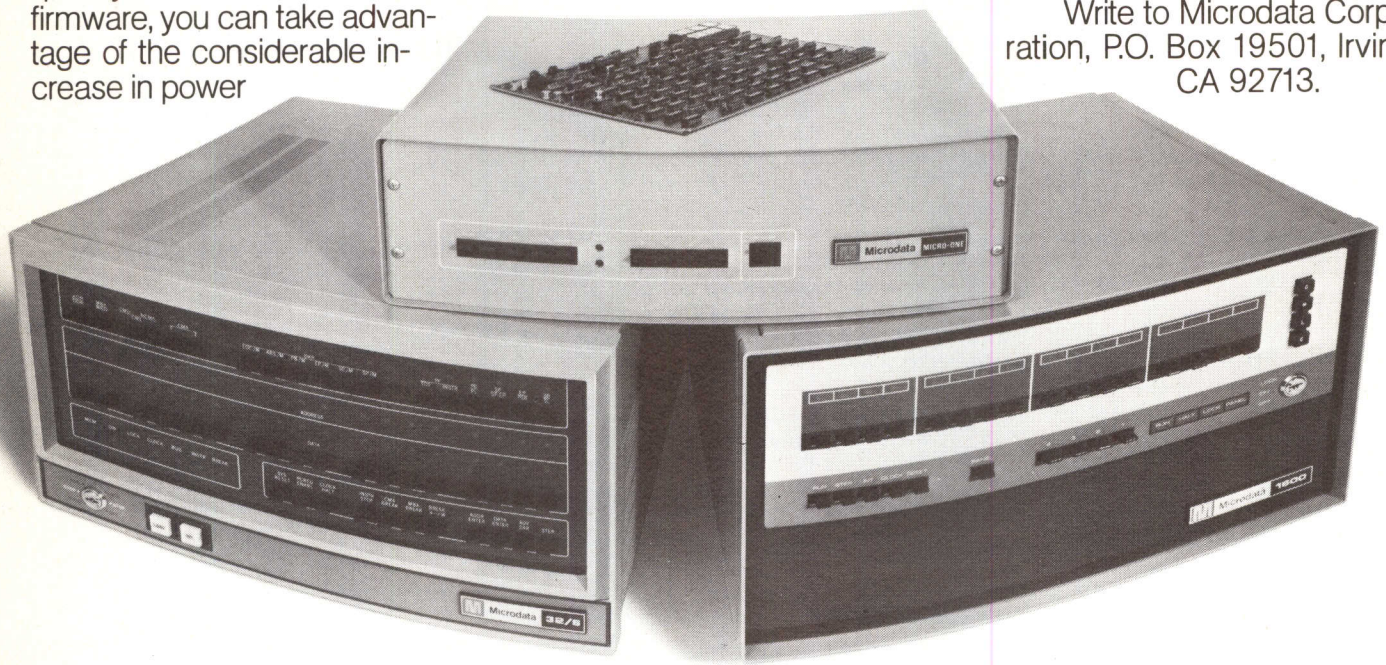

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CALENDAR

CONFERENCES

AUG 3-6—Third Internat'l Conf on Computer Communication (ICCC-76), Royal York Hotel, Toronto, Canada. INFORMATION: ICCC-76, PO Box 365, Station A, Ottawa, Canada K1N 8V3

AUG 10-12—4th Sym on the Simulation of Computer Systems, Nat'l Bureau of Stds, Boulder, Colo. INFORMATION: Arthur F. Chantker, Nat'l Bureau of Standards, Technology Bldg, Rm A247, Washington, DC 20234

AUG 24-27—1976 Internat'l Conf on Parallel Processing, Waldenwoods Resort and Conf Center, Waldenwoods, Mich. INFORMATION: Tse-yun Feng, Conf Chm, 1976 Internat'l Conf on Parallel Processing, College of Engineering, Wayne State U, Dept of Electrical and Computer Engineering, Detroit, MI 48202

AUG 31-SEPT 2—1976 Internat'l Optical Computing Conf, Capri, Italy. INFORMATION: Sam Horvitz, Gen'l Chm, Naval Underwater Systems Center, New London, CT 06320

SEPT 7-10—COMPCON 76 (13th IEEE Computer Society Internat'l Conf), Mayflower Hotel, Washington, DC. INFORMATION: Paul L. Hazan, Program Chm, The John Hopkins U, Applied Physics Lab, John Hopkins Rd, Laurel, MD 20810. Tel: (301) 953-7100, X449

SEPT 8-10—Internat'l Sym on Technology for Selective Dissemination of Information, Palazzo dei Congressi, Republic of San Marino. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEPT 13-23—UISTA Data Communication Conf, Iowa State U, Ames, Iowa. INFORMATION: Conf Director, Paul Bond, 331 Coover Hall, Iowa State U, Ames, IA 50011

SEPT 14-16—Electro-Optics/Laser '76 Conf and Exposition, New York Hilton, New York City. INFORMATION: Industrial and Scientific Conference Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

SEPT 14-17—WESCON (Western Electronic Show and Conv), Los Angeles Conv Center, Los Angeles, Calif. INFORMATION: William C. Weber, Jr, WESCON Gen'l Mgr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

SEPT 20-22—Convergence 76, Internat'l Sym on Automotive Electronics and Electric Vehicles, Hyatt Regency Hotel, Dearborn, Mich. INFORMATION: J. M. Leahy, Micro Switch Div of Honeywell Inc, 17515 W Nine Mile Rd, Southfield, MI 48075. Tel: (313) 424-3744

SEPT 21-23—Joint Conf on Data Privacy and Data Security, U of Linz, Austria. INFORMATION: Das Tagungsbüro der gemeinsamen, Fachtagung öGI und GI, "Datenschutz und Datensicherung," z.H. Herrn Dr Roland Traunmüller, Institut für Statistik und Informatik, Universität Linz, 4045 Linz/Auhof

SEPT 22-24—APL76 Conf, Ottawa, Ontario. INFORMATION: Comshare Ltd, 304-11 Adelaide St W, Toronto, Ontario M5H 1M2 Canada

SEPT 22, OCT 26, and OCT 28—1976/77 Invitational Computer Conferences, Newton, Mass; Chicago, Ill; and Minneapolis, Minn. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

SEPT 26-29—EASCON-76 (Electronics and Aerospace Systems Conf), Stouffer's Nat'l Center Inn, Washington, DC. INFORMATION: EASCON-76, Suite 636, 821 15th St, NW, Washington, DC 20005. Tel: (202) 347-7088

SEPT 28-30—Canadian Computer Show-Salon De l'Ordinateur, Place Bonaventure, Montreal. INFORMATION: Show Mgr, Derek A. Tidd, Industrial and Trade Shows of Canada, 481 University Ave, Toronto, Ontario M5W 1A7 Canada

OCT 4-5 and 19-20—Instrumentation and Computer Fair, Philadelphia Marriott, Philadelphia, Pa and Sheraton Inn/Washington-Northeast, Lanham, Md. INFORMATION: Instrumentation and Computer Fair, Marketing Ventures, Inc, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

OCT 10-14—ISA-76 (Instrument Society of America Internat'l Conf and Exhibit), Houston, Texas. INFORMATION: Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

OCT 12-14—EUROMICRO, Second Sym on Micro Architecture, Venice, Italy. INFORMATION: Jan Wilmink, Program Chm, Euromicro Symposium, Twente U of Technology, PO Box 217, Enschede 7801, Netherlands

OCT 12-15—Micro/Minicomputer Exhibit, U.S. Trade Center, Frankfurt, Germany. INFORMATION: Bureau of International Commerce, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-3748

OCT 13-15—Second Internat'l Conf on Software Engineering, San Francisco, Calif. INFORMATION: Dr C. V. Ramamoorthy, Program Chm, Dept of Electrical Engineering and Computer Sciences, U of California-Berkeley, Berkeley, CA 94720

OCT 19-21—1976 Mini/Micro Computer Conf and Exposition, Brooks Hall/Civic Auditorium, San Francisco, Calif. INFORMATION: Mini/Micro Computer Conf and Exposition, 5544 E La Palma Ave, Anaheim, CA 92807. Tel: (714) 528-2400

OCT 19-21—1976 IEEE Semiconductor Test Equipment Sym, Cherry Hill Inn, Cherry Hill, NJ. INFORMATION: Annual Test Symposium Committee, IEEE Philadelphia Section, U of Pennsylvania, Moore School of EE, Philadelphia, PA 19174

NOV 8-12—Exhibition of U.S. Computers and Peripheral Equipment, U.S. Trade Center, Sydney, Australia. INFORMATION: Irwin D. Nathanson, Office of International Marketing, DIB-233, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-4957

NOV 23-25—COMPEC'76 (Computer Peripheral, Small Computer, and Systems Exhibition), Wembley Conf Centre, Wembley, Middlesex, England. INFORMATION: Trident Conferences and Exhibitions Ltd, Abbey Mead House, 23a Plymouth Rd, Tavistock, Devon PL19 8AU England

SEMINARS

SEPT 27-29—Ninth Annual Workshop on Microprogramming (MICRO-9), New Orleans, Louisiana. INFORMATION: Prof Peter Kornerup, MICRO-9 Program Chm, Computer Science Dept, U of Southwestern Louisiana, Box 4-4330, Lafayette, LA 70504. Tel: (318) 233-3850, X538

OCT 7-8—Design and Drafting Automation, U of Wisconsin-Extension, Milwaukee. INFORMATION: John M. Leaman, Dept of Engineering, U of Wisconsin-Ext, 929 N Sixth St, Milwaukee, WI 53203. Tel: (414) 224-4189

OCT 12-14—Workshop on Design Automation, Michigan State U, East Lansing. INFORMATION: Stephen Pardee, Bell Laboratories, Rm 3B310, Whippany Rd, Whippany, NJ 07981

SHORT COURSES

AUG 2-13—Using Microcomputers; Computer Graphics, U of California, Santa Cruz. INFORMATION: Joleen Kelsey, U of California Extension, Santa Cruz, CA 95064. Tel: (408) 429-2761

Why 706,000 small businesses you couldn't sell last year may buy your data processing system this year.

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On line in its full configuration, the LC50 reads both punched and optical marks. It reads, punches and prints on either 80 or 51 column cards. It prints single line. It prints multiline on any or all of 12 lines. It verifies punched data, automatically detects and corrects most errors, stacks the cards and sorts them into one of two output stackers. Off-line, the LC50 can automatically reproduce, interpret, gang punch cards and, with the RCE feature, can selectively reproduce and gang punch data.

The LC50 offers the most cost efficient solution available for turnaround document processing and data entry. Add one LC50 to your DP system – and subtract the cost of the two or three machines it replaces. Add an LC50 and subtract some training, service and maintenance "down-time." Add one LC50 – and it can help bring the price of your entire system down to what the small business user can afford.

There's yet another way to make the modular LC50 add up to more business in the small-business market. Buy it in its minimal configuration, then add to it as your customer's DP needs grow. Start with a basic punch configuration then add individual modules for read, single-line print, multiline print and other functions. All modules, except the multiline printer, can be installed on site. And, of course, it can be configured to be an ideal I/O device in a Remote Batch Terminal System.

At Documation, we're always interested in producing the most cost effective product. That's why we push our engineers to the limit of their imaginations. Why we run a real, manufacturing plant instead of just an assembly line. Why we go on improving a particular product even though it's a best seller. We assume you're just as interested in beating your competition. That's why you should call or write Roy Ostrander, Vice President, at P.O. Box 1240, Melbourne, Florida 32901. Telephone (305) 724-1111. Place your order for the LC50 and start calling on those 706,000 new customers ...before your competitors do.

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*Based on information from the March 1975 supplement to the Datapro 70 Report by Datapro Research Corporation.

CIRCLE 41 ON INQUIRY CARD

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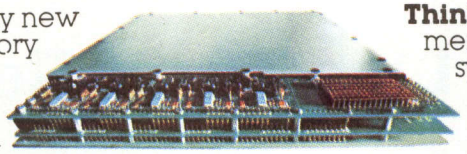
MEMORY+. It's an entirely new dimension in bulk memory for minicomputers. An add-on memory system used with MODCOMP computers to give you a whopping 4,000,000 bytes of directly accessible core storage. At far less cost than any other core memory you could ever buy. Until now.



The MODCOMP 256K-byte memory module that made it all possible.

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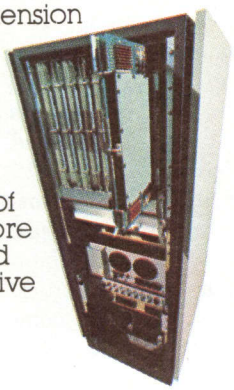
The big breakthrough came when we found a way to slash the cost-per-bit of core by condensing a massive 256K bytes of memory into a single memory plane. In a single MEMORY+ device, anywhere from one to sixteen of these memory modules go together for a total capacity of 4 megabytes.

Consider what MEMORY+ can mean to you.

Think of it as a giant extension to main memory. It's both word and block addressable, and it swaps data so fast it appears to be a part of main memory itself.



Think of it as a way to beat the sluggish speed of fixed head disc. With its core memory access time, and transfer rates as high as five megabytes per second.

Think of it as a shared memory in multi-processor systems. Two MODCOMP computers can be processing the same data at memory speeds, without tying up main memory.

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Think of it as a direct data path to main memory for external data, used as a high-speed buffer.

Any way you look at it, MEMORY+ is one giant step forward in real-time bulk storage.

And because of its modular design, you buy only the capacity you need now. As you need more, add more plug-in modules.

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Call your nearest MODCOMP sales office for full details. Or write for a comprehensive 20-page brochure that explains the whole MEMORY+ story.

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by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Private Line Tariff Revisions

On August 19, 1976, American Telephone and Telegraph Company (AT&T) will implement totally new rates for private lines. This latest change in the critical tariff is the third major restructuring of private line services in as many years. During that time, private line users have experienced three rate increases in AT&T High/Low Private Line Rates. Significance of this latest redefinition of AT&T's Tariff 260 is that every user of data communications networks must reanalyze basic financial justification of private line use, such as multipoint data networks. Most communications users tend to become immune to seasonal rate increases. This most recent change, however, can create major cost advantages or penalties to the private line user.

Prior to August 19th, a 100-mile private line between two high density cities cost $222.00 per month. As a result of this most recent revision that same line will cost $225.20 per month. The cost increase equates to only 1.4%. Major advantages to the user occur if one or both cities being interconnected are not designated as high density. Previous rate for such a line was $401.00 monthly. Under the new rates the line costs $270.55 if one terminating city has a low density designation, and $345.60 if both are classified as low density. This represents cost reductions of 32.5 and 13.8%, respectively. Under new tariff provisions, a longer distance line tends to experience even more dramatic cost reductions. A previous 1000-mile channel between a high and low density city generated $2840.00 in monthly revenue to AT&T. This same circuit now provides only $1171.23 to AT&T, with a 58.8% monthly cost reduction to the user. A private line channel between two high density cities 1000 miles apart decreases 22%, from $1050.00 to $819.20 per month.

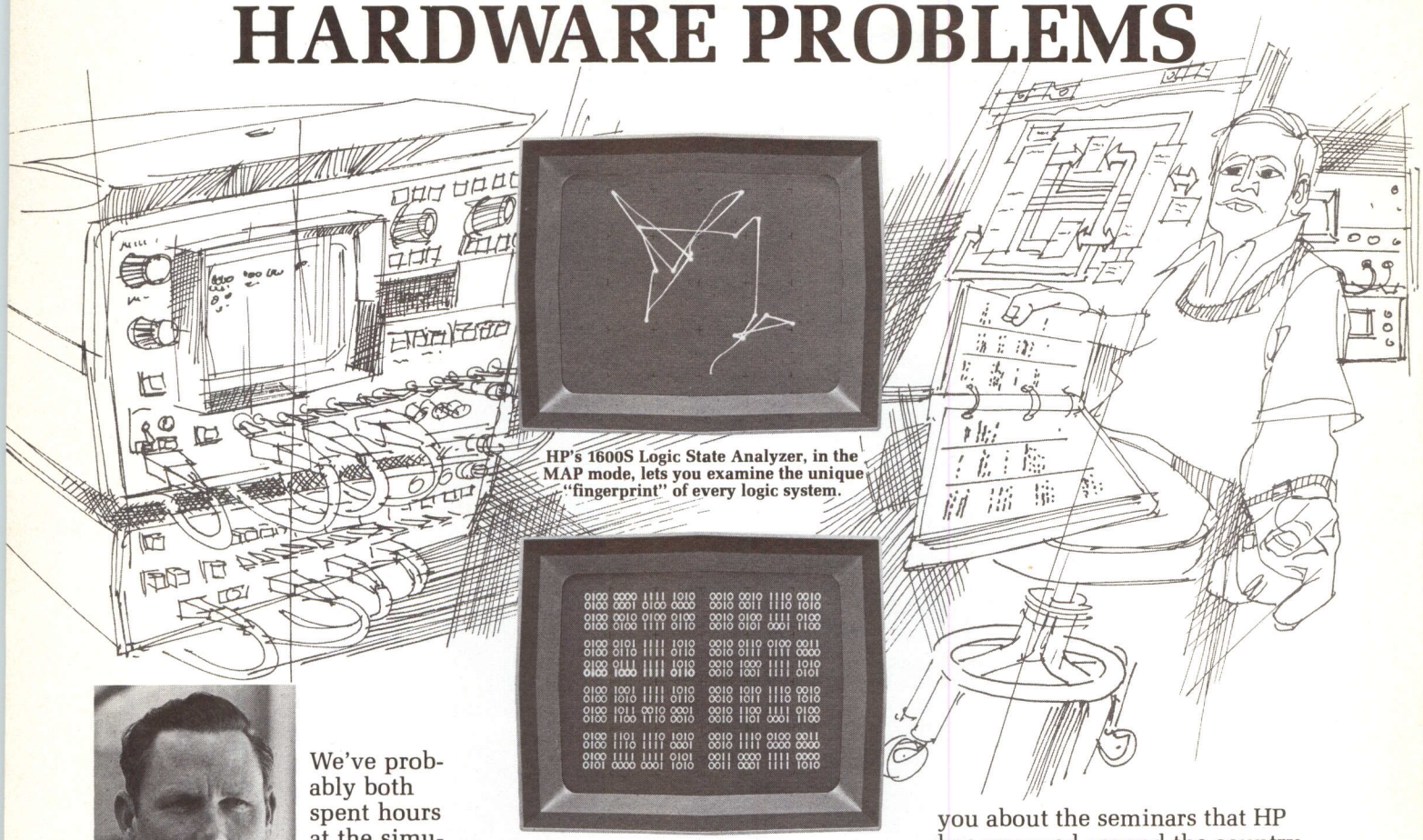
Prime motivation for this latest change was a Federal Communications Commission (FCC) ruling in January 1976. AT&T private line rates in effect at that time allowed revenue from noncompetitive regions to subsidize lower rates in competitive areas. Facility routes between major cities have been prime markets for specialized communications common carriers, such as MCI, SPCC, and USTS. In order to counteract this competition, AT&T originally filed the High/Low Private Line Tariff to provide private lines at lowest possible rates in competitive areas. Justified by higher number of channels between high density cities, past rates were intended to be compensatory; that is, to provide revenue return based on actual cost of providing the service. On this basis, AT&T has been able to justify the past 2-tier pricing concept. In January, the FCC decreed that AT&T apparently had overcompensated for competitive factors by underpricing private lines between high density cities, and unfortunately overpricing non-high density route channels. As a result, the new tariff generally provides a reduction to private line users except for slight increases to short distance channels between high density cities.

The past tariff defined 370 cities in the continental U.S. as high density locations. The intended tariff significantly revised this list, with some cities obtaining lower rates. Fifty-eight cities which were former high density locations lost that designation. Thirty-three former low density cities were elevated to high density. Most significant cost increase will be experienced by users who have leased lines between one or two cities which were downgraded to low density. Table 1 illustrates the impact on these users.

The new tariff represents a totally new pricing configuration. In order for a current or potential user of voice or data communications leased lines to properly plan future networks, complete understanding of components and their relationships is mandatory. As with the past tariff structure, certain cities are designated as high density, and are intended to represent major carrier concentrations in AT&T Long Lines network. Typically, a high density city can be expected to have a common termination of over 14,000 channel pairs among other operational qualifications. Cities which do not meet these criteria are automatically relegated to low density status. First major change in the intended

(Continued on p 14)

Let's talk about the easy way for you to spot microprocessor HARDWARE PROBLEMS



HP's 1600S Logic State Analyzer, in the MAP mode, lets you examine the unique "fingerprint" of every logic system.

In the TABLE mode, the 1600S displays up to 16 32-bit words. These words could be combinations of addresses, instructions or states of the control lines.

We've probably both spent hours at the simulator to prove we had good software and then discovered the hardware won't play—what do we do? You know the traditional answer. Dig out the scope, get out the program printout, and brace yourself for hours of grinding, point-by-point checks. But I can tell you that doesn't have to be the case. Especially now that HP has introduced some new tools that can really cut down your troubleshooting time.

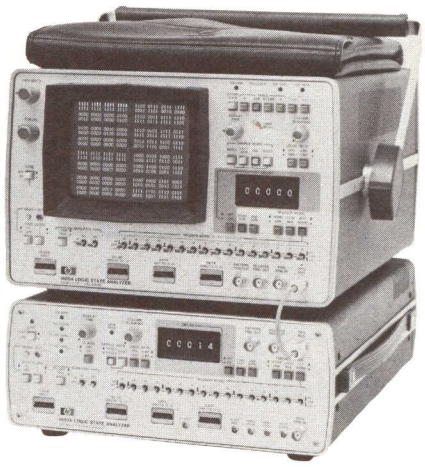
HP's Logic State Analyzers can really take a lot of pain out of your troubleshooting procedures. You'll find wiring errors, defective components, and even solder splashes; and you'll find them a lot more quickly than ever before.

Let me give you an example. We had an eight-bit microprocessor system with start-up problems. The clocks were running and phased right, and the address lines toggled, but the machine didn't function. So, we set up an HP 1600S Logic State Analyzer to look at both the Address and Data buses. It was then we noticed that only "zeros" were being fetched from memory. Knowing the ROM was good, we then added several control lines to the display and the problem showed up immediately. The "Enable" line never went high. A quick look at the "Enable" driver showed the input was ok, but no output. Obviously, the gate was defective.

I don't know how long it would have taken to find that one without HP's Logic State Analyzers, but I *know* it would have taken us a lot longer.

Call your local HP field engineer. He'll give you all the details on the 1600S (priced at $7100*) including spec sheets and application notes detailing the use of mapping for troubleshooting minicomputer and microprocessor systems. He'll tell you about the seminars that HP has arranged around the country and tell you when one will be held in your area and how you can attend. You ought to go to one, because you'll discover an exciting new concept in digital troubleshooting.

*Domestic U.S.A. price only.



086/5

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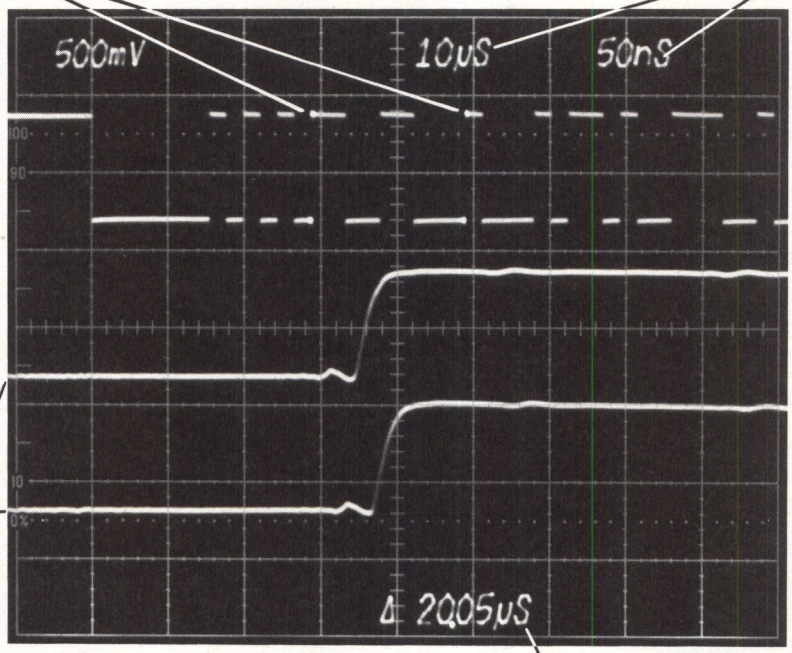
This display makes oscilloscope timing measurements easier, faster and more accurate,

Main sweep has two intensified zones.

Two intensified zones on the main sweep correspond to the two expanded, delayed sweeps shown below. They are quickly and independently positioned to provide a visual approximation of the △ time measurement.



Sweep rates displayed digitally.

Digital crt readout displays both sweep rates for measurement ease and convenient photographic documentation. To the left is the main sweep rate and to the right is the sweep rate for the two alternate (or delayed) sweeps.

Two expanded sweeps.

Both intensified zones are expanded at a faster rate for better resolution and are swept alternately with the main sweep trace for a complete, powerful measurement display. △ time accuracy is enhanced by superimposing one trace over the other, yet they can be vertically separated for independent analysis.

Time difference is computed and displayed digitally.

The time difference (△ time) between each of delayed sweeps (or intensified zones) is digitally computed and displayed directly on the crt for swift and convenient measurement. When similar points on each of the alternate delayed traces are aligned, the △ time readout gives you a highly accurate measurement of the time between the points.

CRT display, photographed on a 7904 oscilloscope, shown full size.

Fill out and mail to: Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

Please send me

- ☐ The new 7B80-Series brochure
- ☐ △ time measurement application notes.
- ☐ A catalog of 7000-Series oscilloscope mainframes and plug-ins.
- ☐ Please have a Tektronix Field Engineer contact me about a demonstration.

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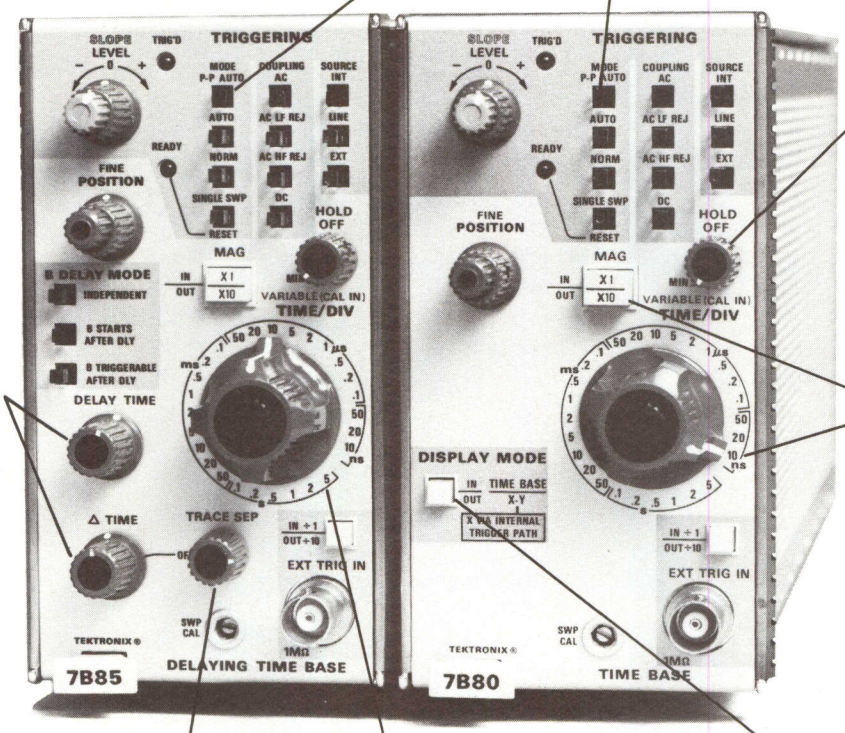
and these new plug-in time bases make it possible.

Triggering.
Peak-to-peak automatic triggering offers a continuously triggered display regardless of changes in signal amplitude or frequency. Trigger bandwidth is 400 MHz with trigger sensitivity at least 250 mV.

Trigger holdoff adjustable.
Variable trigger holdoff allows you to obtain stable displays on complex signals like digital data trains.



Controls position both intensified zones.
DELAY TIME positions the first intensified zone. △ TIME positions the second intensified zone relative to the first. The △ delay time value — the time between the two intensified zones — is presented digitally on the crt.

7B80 sweep rates.
The alternate (delayed) sweeps can be set to any rate up to 1 ns/division on the 7B80. Naturally, other 7000 Series time bases with different performance features can be used with the 7B85 to make △ time delay measurements.

Alternate traces can be separated.
TRACE SEPARATION activates the △ delay time mode and permits the two delayed traces to be vertically positioned with respect to each other for your most convenient display.

7B85 sweep rates.
Sweep rate for the main sweep can be set from 1 ns/division to 5 s/division.

Optional X-Y mode.
For phase relationship measurements, an optional X-Y mode routes the X (horizontal) signal from an oscilloscope vertical amplifier to the horizontal sweep unit without changing input probes.

Here's how to get more information

Your nearby Tektronix Field Engineer will be happy to show you how these new time bases combine with a 7000-Series oscilloscope mainframe and other 7000-Series plug-in instrumentation to fit your measurement needs. Just call your local Tektronix Field Office or send the coupon to Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

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The 7000 Series...more than an oscilloscope

For technical data, circle 9 on Inquiry Card. For a demonstration, circle 10 on Inquiry Card.

TABLE 1

Impact of Downgrading Cities
(Assume 250-mile channel)

Former Line	Downgraded City	
Cost	One	Both
$360.00	$369.55	$447.60
	2.7%	24.3%

TABLE 2

Fixed Charges

Schedule I	$49.20 per month
Schedule II	48.70 per month
Schedule III	48.60 per month

TABLE 3

IXC Mileage Charges
(per mile)

Mileage	Schedule I	Schedule II	Schedule III
First 15	$1.80	$3.30	$4.40
Next 10	1.50	3.10	3.80
Next 15	1.12	2.00	2.80
Next 20	1.12	1.35	2.10
Next 20	1.12	1.35	1.60
Next 20	1.12	1.35	1.35
Next 900	0.66	0.66	0.68
Each additional	0.40	0.40	0.40

TABLE 4

Station Terminal Charges

	Monthly	Installation
First Station in an Exchange	$25.00	$54.15
Additional Station on Same Premises	5.00	54.15
Additional Station on Different Premises	25.00	54.00

TABLE 5

Monthly Cost for 2500-Mile, 2-Point Private Line

	Schedule I	Schedule II	Schedule III
Location A			
Station Terminal	$25.00	$25.00	$25.00
IXC			
Fixed Charge	49.20	48.70	48.60
Mileage Charge			
First 15 miles	27.00	29.50	66.00
Next 10 miles	15.00	31.00	38.00
Next 15 miles	16.80	30.00	42.00
Next 20 miles	22.40	27.00	42.00
Next 20 miles	22.40	27.00	32.00
Next 20 miles	22.40	27.00	27.00
Next 900 miles	594.00	594.00	612.00
Next 1500 miles	600.00	600.00	600.00
Location B			
Station Terminal	25.00	25.00	25.00
Total Monthly Cost	$1419.20	$1484.20	$1557.60

(Continued on p 18)

They're gonna make you a star.

In just a very short while, we'll be giving static RAM users the same thing we've already given dynamic RAM users.

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Using the same super technology that gave you the world's first 150ns 4K dynamic RAM, we'll soon be giving you the μPD410 series of 4K static RAMs with speeds down to 100ns.

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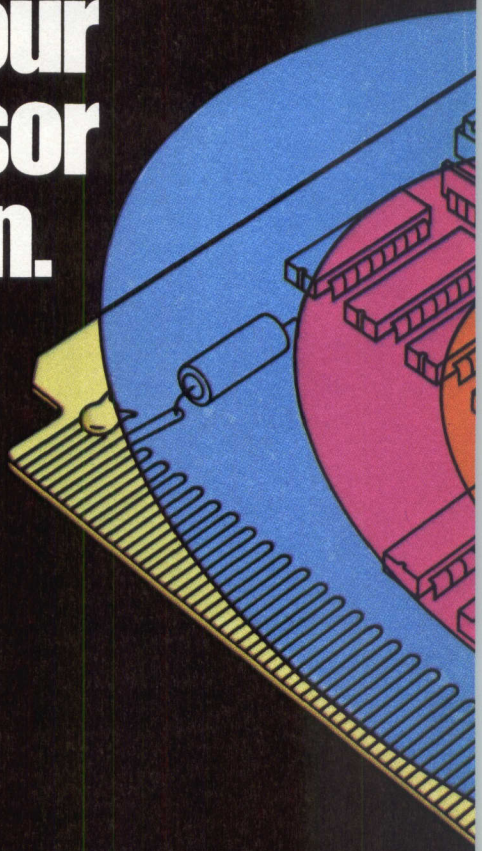
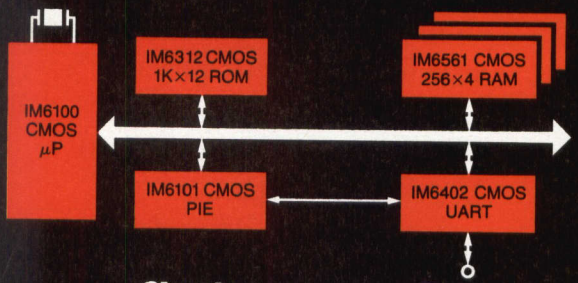
Go CMOS/LSI with your microprocessor design.



Use the CMOS microprocessor with a second source on-stream.

Here's a way to simplify design problems while gaining the system advantages of silicon gate Complementary MOS (CMOS) circuitry ... all by using Intersil's IM6100 12-bit CMOS microprocessor and its all-CMOS family of associated devices, now also available from Harris Semiconductor.



Simple power supplies.

By their very nature, CMOS circuits operate from uncomplicated, inexpensive supplies; all devices in the 6100 CMOS family use only one unregulated +4 to +11 volt supply. At 4MHz and 5V, the IM6100 dissipates only 10mW, with similar power levels for all the other members of the CMOS family. Because there's little heat, cooling problems disappear.

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CMOS is famous for its noise immunity, allowing trouble-free operation in troublesome environments.

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The IM6100 and all other members of its compatible CMOS family offer you a choice of industrial (−40 to +85°C) or full military (−55 to +125°C) temperature ranges.

Inexpensive crystal clock.

Timing for the IM6100 system operation is supplied by an on-chip clock, driven by an external crystal. No clock generators or level translators needed.

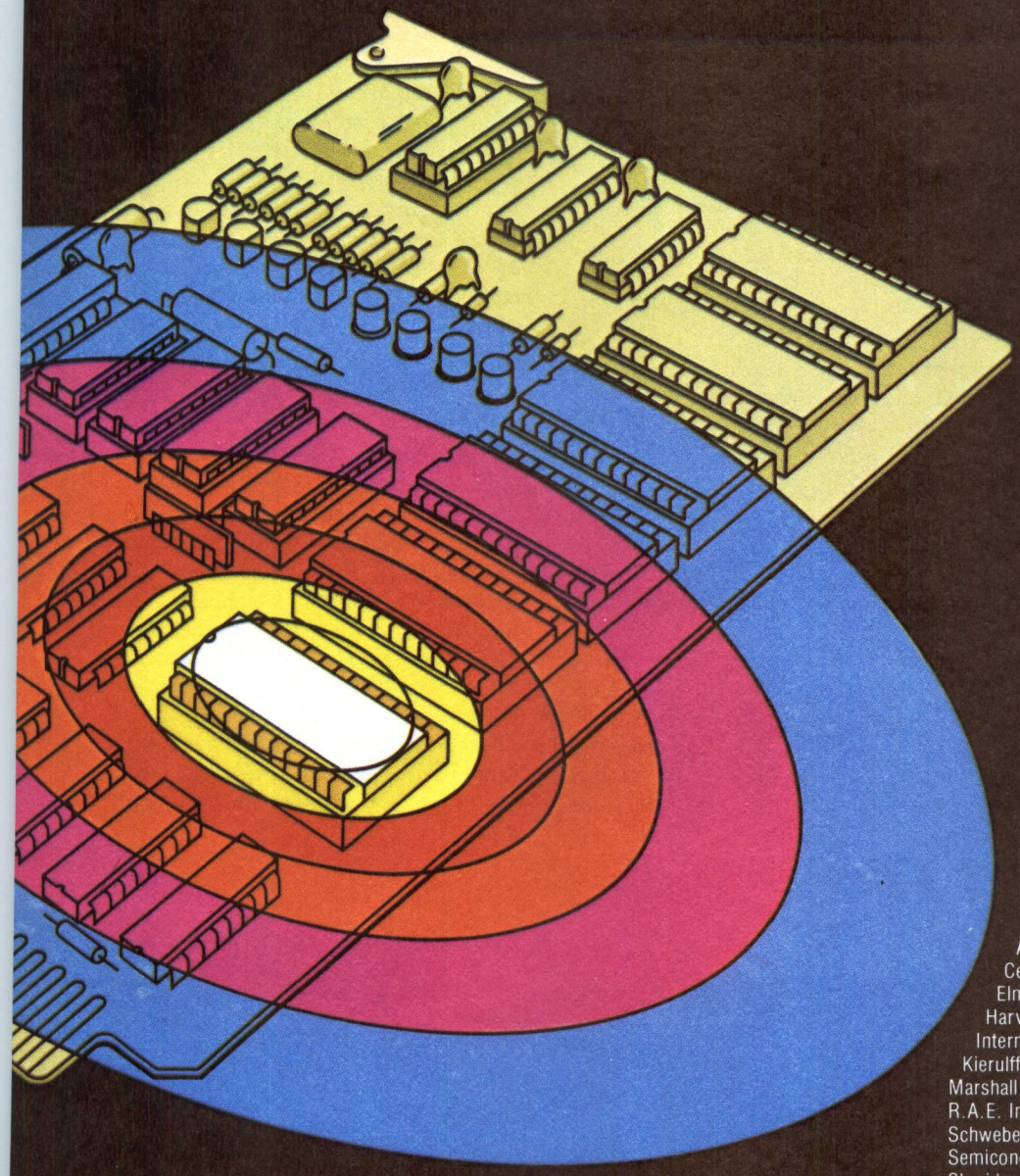
Standard interfacing.

The entire IM6100 CMOS family operates well with other technologies such as NMOS, PMOS and TTL. These Intersil devices interface directly with industry-standard RAMs, P/ROMs and LSI peripheral interfaces such as UARTs, FIFOs, keyboard encoders, analog converters, modems, etc.

Uses standard, available software.

The IM6100 executes the instruction set of the most popular minicomputer, DEC's PDP-8/E®.

INTERSIL CMOS/LSI



Getting started's easy as ABC.

Intersil has simplified your getting into microprocessor design with three easy alternatives.

A. IM6100 CMOS Family Sampler. A fully documented, complete pre-packaged kit of components for an all-CMOS IM6100 Microprocessor system. Seven-part kit includes IM6100, IM6101 PIE, IM6312 1024 x 12 ROM, IM6402 UART and three IM6561 256 x 4 RAMs. Ideal for low-cost prototyping and evaluation. Single-piece prices total $125.30. Special offer price (valid only until Oct. 31, 1976) is $55.00.

B. Intercept Jr. Tutorial System. A complete one-card battery-powered operating system, including multi-function keyboard, 8-digit LED display, 256 x 12 RAM, resident microinterpreter, provisions for modular expansion and detailed instruction manual for $281.00.

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CIRCLE 11 ON INQUIRY CARD

tariff is definition of three types of channels. Schedule I channels are defined as those which interconnect two high density cities, Schedule II channels apply to lines between a high density city and a low density city, and Schedule III channels connect two low density cities. The new tariff can properly be considered three tiered.

Actual private line pricing comprises three cost components: a fixed charge, interexchange channel mileage charge, and station terminal charge. Fixed charge is analogous to channel termination charges of the previous tariff. Major difference and a source of many typical miscalculations is that the channel termination charge had to be applied to each end of the interexchange channel. The new fixed charge is only applicable to each channel segment. If the circuit is a 2-point channel, only one fixed charge is applied. If a multipoint circuit is to be priced to four remote data terminals, four fixed charges will be incurred. Each segment will be charged one fixed charge. Table 2 shows fixed charges for each channel type.

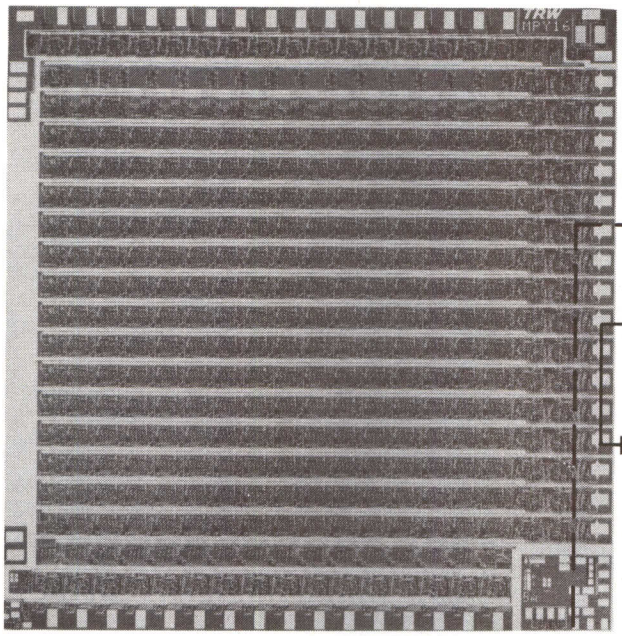
Second cost component, the interexchange channel (IXC) mileage charge, has returned to the graduated scale used by AT&T for private line rate prior to High/Low Private Line Tariff. The first 100 miles of channel distance incurs the majority of the IXC charge. A considerably lower charge per channel mile applies for channel mileage between 100 and 1000 miles. After 1000 miles, cost per mile is reduced to $0.40. Table 3 provides separate mileage rates for each rate step and for each type of channel.

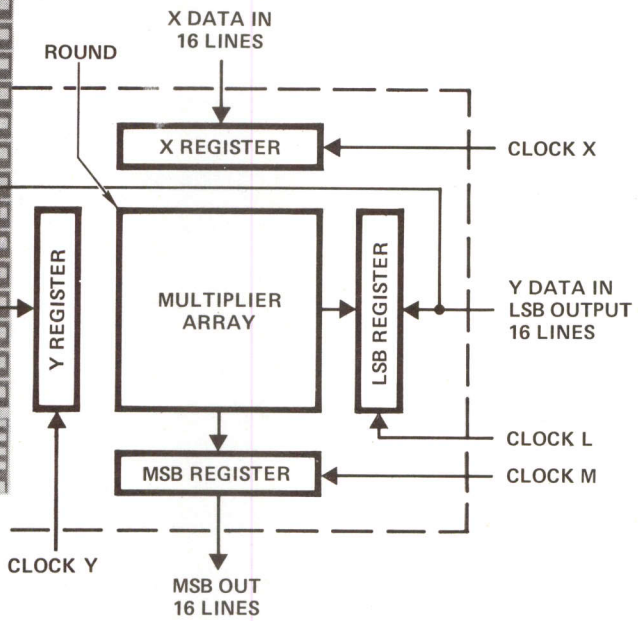
Third cost component is station terminal charge. This applies to the local loop between customer's premises and the serving central office. Station terminal charge applies to each local loop or to each "drop" provided by the telephone company to the long distance interexchange channel. It is uniform regardless of the associated channel's schedule designation. First station in a telephone central office exchange is charged $25 monthly. If a second local loop is required to the same premises as an existing station, monthly charge is only $5. A second station in the same exchange but at different premises incurs the $25 charge.

It is important to note that nonrecurring installation charges are applicable only to station terminals and not to either the fixed charge or interexchange channel mileage. Table 4 lists one-time installation charges as well as monthly station channel charges. As an example of the application of these rates, Table 5 calculates monthly cost for 2500-mile 2-point private line as Schedule I, II, and III channels.

This new tariff while offering real potential for lower cost also presents a considerably more complex structure. For those interested in past developments of private lines, the *Computer Design* Communication Channel columns which have traced these developments are "Private Line Service" (Aug 1972), "New Private Line Tariff Analysis (Part 1)" (July 1973), and "New Private Line Tariff Analysis (Part 2)" (Aug 1973). □

16-Bit Multiplier 200 Nanoseconds





The first monolithic-bipolar, 16 x 16-bit multiplier (MPY-16) is now available from TRW. It's fully TTL-compatible, too. A single MPY-16 package can replace as many as 50 MSI/TTL packages, eliminating 2 x 4 multipliers.

Applications for the MPY-16 include micro and mini computers, instruments, high-speed data processing, and wideband digital systems. If your application demands speed...the MPY-16 can meet it.

The multiplication throughput rate of 5,000,000 per second can be increased to 20,000,000 by direct parallel pipelined multiplex operation of four MPY-16 chips. In this mode, input/output ports are bussed together.

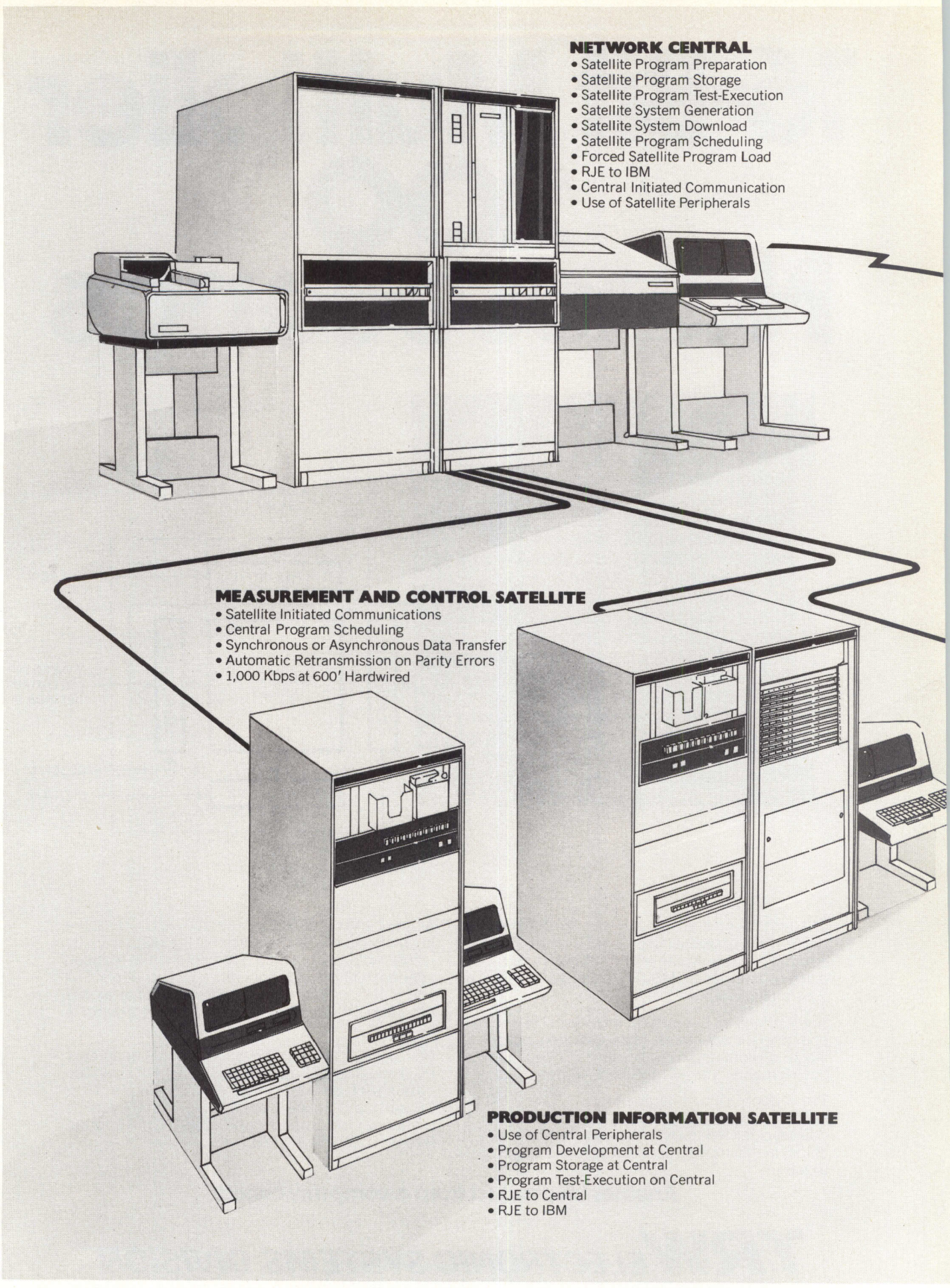
All input and output data – internally latched...three I/O ports (16 bits/port) for highest throughput speed – 200 ns typical...single port operation at reduced speed – 300 ns with separate clock controls. Full adder cells on the 16 by 16-bit multiplier array use the sequential add algorithm. A round control is available.

Delivery is less than 30 days for sample quantities. Price and delivery available on request. For a detailed data sheet, call (213) 536-1977. Or write: TRW Defense and Space Systems, Electronic Systems Division, One Space Park, E2/9043, Redondo Beach, California 90278.

Another LSI product from a company called

TRW ELECTRONIC SYSTEMS DIVISION

CIRCLE 13 ON INQUIRY CARD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• Use of Satellite Peripherals
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• Satellite Initiated Communications
• Central Program Scheduling
• Synchronous or Asynchronous Data Transfer
• Automatic Retransmission on Parity Errors
• 1,000 Kbps at 600' Hardwired
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• Use of Central Peripherals
• Program Development at Central
• Program Storage at Central
• Program Test-Execution on Central
• RJE to Central
• RJE to IBM

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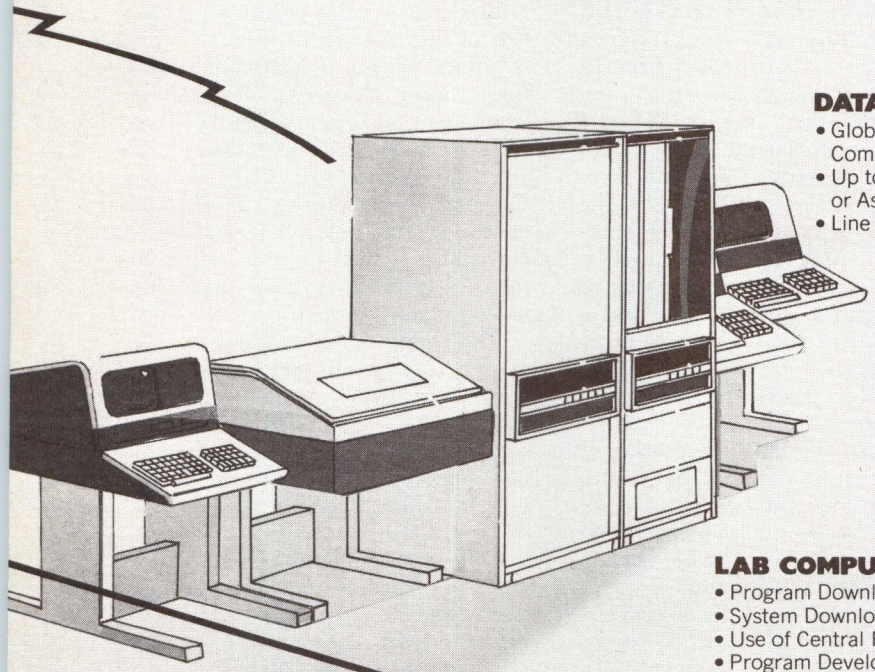

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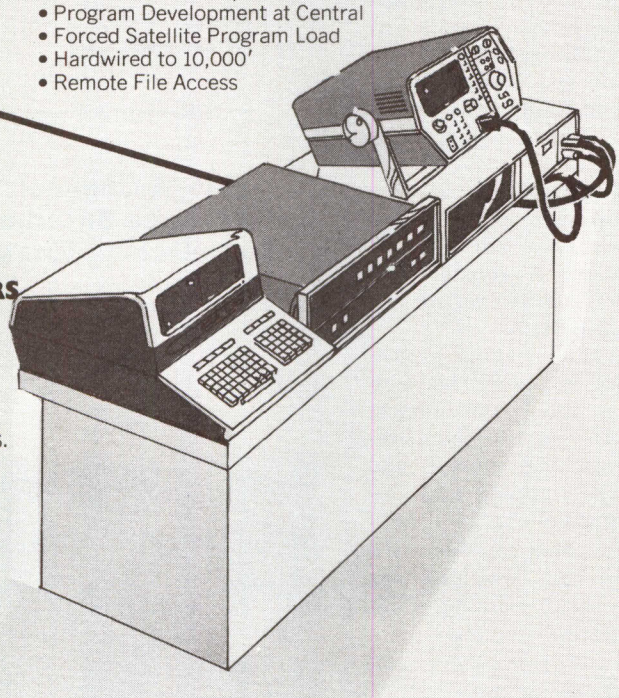

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CIRCLE 14 ON INQUIRY CARD

Data Communications Test Set Performs All Basic Tests/Simulations

A microprogrammed data communication test set for use in tech control systems, the TC-100 performs a range of troubleshooting duties to locate and define faults quickly and simply, solving many problems encountered in day-to-day operation of a data center. Testing both hardware and software functions in transmission lines, modems, terminals, and computer ports, the unit incorporates keyboard entry and a simplified front panel to allow easy operation.

Developed by Cooke Engineering Co, a div of Dynatech Laboratories, Inc, 900 Slaters Lane, Alexandria, VA 22314, to provide the buyer with a reasonable alternative to the welter of high and low priced equipment available for network testing, the set contains all necessary functions in a compact 5¼" high rackmount unit. It provides balanced, versatile, yet inexpensive testing capability by combining protocol generation, character storage, distortion measurement, bit/block error rate test, and timing measurements. Tests may be performed with asynchronous or synchronous formats at EIA RS-232 or MIL-188 signal levels, and at speeds from 50 to 9600 bits/s. The unit will accept modem clock or provide clock to a device, if required.

Nine basic test simulation routines attack line, equipment, software, and timing problems. Most tests can be used in more than one problem area, permitting several approaches for detecting and isolating faults.

The data communication system can be exercised in several ways to obtain bit-error rate performance; measurements of system behavior; remote control switching, polling, and selection; message trapping and display; and line protocol checkout. Self-explanatory front panel controls make the unit easy to use; illegal settings light a "panel check" warning. Controls are grouped into separate function units—generator, analyzer, and interface—to further ease use.

Message entry configurations may be inserted through the keyboard for polling and remote switching. Sequences may contain up to 64 characters. 2047-bit pseudo-random or incrementing binary count transmit patterns can be generated for error rate testing. Generator section of the panel also makes test points available to monitor transmit clock and data.

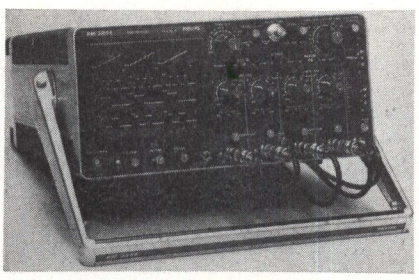
The analyzer section of the panel provides a 3-digit LED numeric display with floating decimal point with HOLD/RUN/CLEAR control. Programmable analysis modes provide for automatic testing with results shown on the display. These modes provide bit and selectable block error rate, measurements of request-to-send/clear-to-send turnaround delay in the 1-ms to 999-s range, and measurements of total data path delay in the same range. User-selected trap character may be programmed via a front-panel DIP switch with continuous or stop-on-character display. An increment/decrement switch permits scanning and display of the stored data characters that precede or follow the stop character.

Controls on the interface section of the panel permit standard data rates from 50 to 9600 bits/s plus external clocking to be programmed; external modem timing is also provided. Data format is either synchronous or asynchronous with 5- to 8-bit characters, one or two stop bits, and odd, even, or no parity.

Circle 140 on Inquiry Card

Portable, 4-Channel Oscilloscope Based on Cold-Switching Concept

Providing 4-channel operation in a portable lightweight unit, the PM 3244 has four identical 50-MHz channels with 5-mV sensitivity, permitting users to see the actual behavior of the device at one glance. The completely portable device, developed by Philips Test & Measuring Instruments, Inc, 400 Crossways Park Dr, Woodbury, NY 11797, can be used in the laboratory or in mobile service; it can even be operated from batteries.



Showing six signals simultaneously on an 8 x 10-cm display, Philips' PM 3244 oscilloscope provides four identical 50-MHz channels in a compact portable unit that weighs 21 lb and operates 5 hours from a battery pack

Key concept that permitted realization of this instrument, cold switching—remote control of instrument operation—allows complete freedom in component and front panel layout, resulting in electronically-ideal layout and ergonometrically-ideal control. Compact packaging is possible because of the highly efficient direct conversion power supply, which reduces power dissipation and eliminates the need for ventilation.

The scope has a bright clear 8- x 10-cm display on which six signals can be shown simultaneously—the four input signals and two differential signals. Triggering for the main timebase may come from any of the signals, the incoming line supply, or an external source.

Cold-switching not only allowed complete freedom in locating components and front panel controls, but permitted the equipment to be contained in a compact case. Instead of front panel controls being connected directly and mechanically to the instrument functions, they switch low power dc command voltages which derive solid-state and reed-relay switches mounted on the instrument boards. Cable bunches provide the only relation between controls and circuitry. This allows the controls to be placed logically for operator convenience, without sacrificing electrical performance. Cold-switching also permits high frequency input signals to be confined to the boards, eliminating problems of crosstalk on front panel controls and nonlinearities—ringing, overshoot—from self-inductive long scope leads.

Because the electronics are not necessarily grouped around the controls, they can be laid out for optimum performance. Vertical input modules—integrating reed-relay attenuators and first amplification stages—deliver their signals to one central vertical amplifier board over 50-Ω lines. This board has 4-quadrant symmetry, with channel selection gate circuitry along the central axes; position control, display-mode selection, and inverting take place on this board.

(Continued on p 26)

Point by point, line by line:

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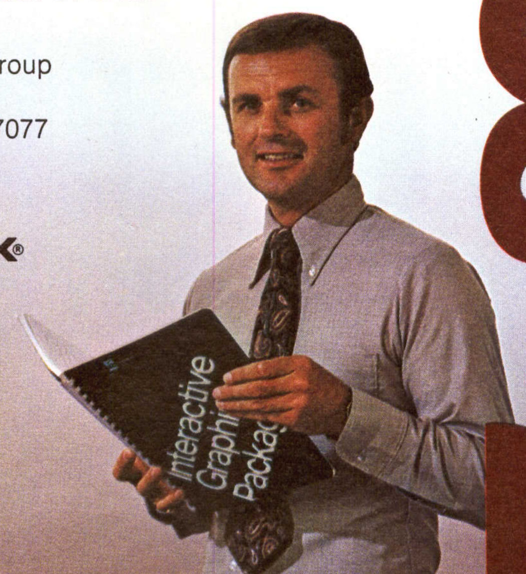
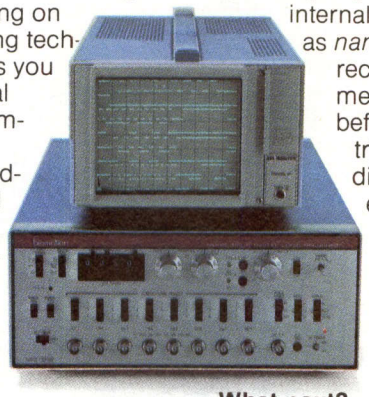
Graphics $2995



Your next digital logic analyzer.

Biomation's new 851-D 8-channel, 50 MHz logic analyzer.

Digital logic analyzers are revolutionizing the solutions of design and trouble-shooting problems. Biomation, building on our early waveform recording technology, has created the tools you need for your fast new digital world. We offer the most complete line of logic analyzers anywhere. And our thousand-plus customers have helped us develop the most useful features for real-world problems of digital system design and test. Our new 851-D catches, records and displays 8 channels of high speed logic. It is the slickest handling, most cost-effective logic analyzer we've seen yet. But don't take our word for it. Check over the features for yourself.



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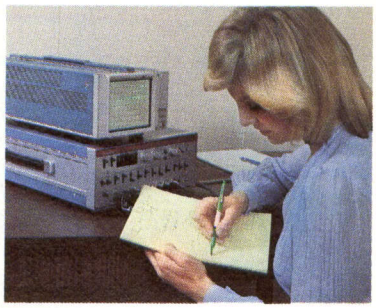

What next?

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(851-D shown actual size.)

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☐ Sounds great, but I don't know what all of the features actually do. Please send more information.

☐ Send information on your complete digital logic analyzer line.

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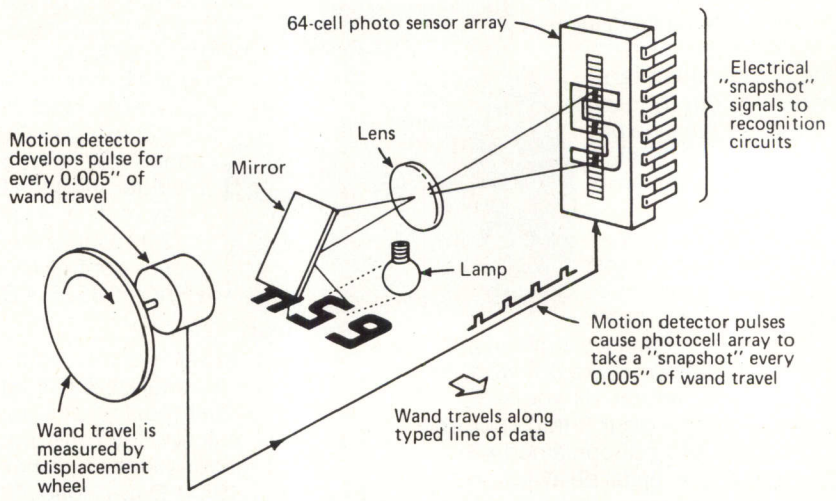
CIRCLE 16 ON INQUIRY CARD

Remote control concept also allows the low power Schottky-TTL switching logic that drives the channel-switching gates to be mounted on a separate board. Only four output lines control the gates, one for each channel. Operator control input comes from the front panel pushbuttons through one cable bunch. Complex measurements can be set up simply, from a choice of triggering sources, as a result of the compact scope design.

The unit is powered by a direct-conversion power supply which immediately rectifies the incoming line supply, and stabilizes the resulting raw dc using a highly efficient switching regulator. The stabilized dc supplies all instrument power rails through a 20-kHz dc-dc converter. This arrangement has very little dissipation or heat generation, and avoids the need for a heavy, bulky 50- or 60-Hz power transformer. Overall power dissipation of the instrument is 29 W. The supply runs on any ac supply between 90 and 270 V at 46 to 440 Hz or any dc voltage between 100 and 200 V without switching. The device will operate continuously for five hours on a PM 8901 battery pack.

Magnesium-alloy castings are used for front and rear panels; side profiles are extruded aluminum, resulting in low weight and leaving interior space for electronics and controls. Because of low power consumption, ventilation holes and forced cooling are not necessary. Lack of cooling holes protects the electronics from sudden temperature changes and thermal instability.

Circle 141 on Inquiry Card



Key Tronics' OCR wand consists of a 64-cell photosensor array, which feeds a fresh set of character signals to recognition circuitry each time the motion detector measures 1/200" of wand travel, and recognition circuitry capable of sensing which character has been read

Hand-Operated OCR Wand Reads Typed or Handprint Data at 100 Char/s

Permitting data entry operations to be automated, the KT3 OCR wand can speed the entry process by a factor of five, and is sufficiently inexpensive to be used with a large proportion of present CRT terminals, thereby permitting a mixture of OCR and keyboard entry operations. Developed by Key Tronic Corp, Bldg 14, Spokane Industrial Pk, Spokane, WA 99216, the wand system consists of a small character reading electronic camera or wand, linked by flexible cable to a "black box" containing recognition circuits.

The wand uses a 64-cell linear photodiode array to develop electrical output signals. As it is moved across the character line, a displacement wheel emits control pulses that cause the cells to take a fresh set of electrical identification signals for every $\frac{1}{200}$ in. that it travels. This is equivalent to a resolution of 4000 points/in.^{2} Recognition circuitry compares the incoming wand signals with stored signal patterns that represent known characters; when a character is recognized, the circuits feed out a digital signal in ASCII or other computer-compatible code. If a character cannot be identified because of poor print quality, the circuit emits a "beep" to notify the operator. Since the wand is usually used with a CRT terminal, the unreadable character can then be entered by the operator through the terminal's keyboard.

In normal use, the wand is first placed in contact with paper or other surface on which data are printed. Its optical reading section is aligned with character line, and the wand is moved by hand across the line of characters, enabling the displacement wheel to step off wand travel.

The wand and its recognition logic are capable of handling the numerals 0 through 9 in the OCR-A font. Where data sources include letters of the alphabet as well as numerals, the model KT9 can be used. This unit handles OCR-A alpha characters as well as eight numeric fonts and handprint. Recognition rate is less than 1 "can't read" for every 10,000 characters scanned, if copy is cleanly typed.

The KT9 can also read degraded copy and even carbon copies. It may be moved across the typed line at speeds to 10 in./s—equivalent to 100 char/s for conventional 10-char/in. type. Capability to read data with either a backward or a forward motion can provide excellent data verification. In addition, the microprocessor used in the recognition process can provide parity check and check-digit computation for data verification, permitting errors to be caught during data entry.

Five pushbuttons on the back of the KT9 allow the user to select the specific font reading capability needed for the document being read. The buttons can also generate custom codes such as tab, back space, new line, clear, or transmit.

Circle 142 on Inquiry Card

THE LOGICAL CHOICE—First in a series

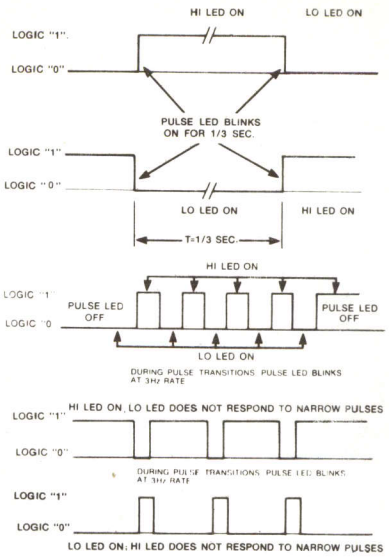
Logic Probe 1 is a compact, enormously versatile design, test and troubleshooting tool for all types of digital applications. By simply connecting the clip leads to the circuit's power supply, setting a switch to the proper logic family and touching the probe tip to the node under test, you get an instant picture of circuit conditions.

LP-1's unique circuitry—which combines the functions of level detector, pulse detector, pulse stretcher and memory—makes one-shot, low-rep-rate, narrow pulses—nearly impossible to see, even with a fast scope—easily detectable and visible. HI LED indicates logic "1", LO LED, logic "0", and all pulse transitions—positive *and* negative as narrow as 50 nanoseconds—are stretched to ⅓ second and displayed on the PULSE LED.

By setting the PULSE/MEMORY switch to MEMORY, single-shot events as well as low- rep-rate events can be stored indefinitely.

While high-frequency (5-10MHz) signals cause the "pulse" LED to blink at a 3Hz rate, there is an additional indication with unsymmetrical pulses: with duty cycles of less than 30%, the LO LED will light, while duty cycles over 70% will light the HI LED.

In all modes, high input impedance (100K) virtually eliminates loading problems, and impedance is constant for all states. LP-1 also features over-voltage and reverse-polarity protection. Housed in a rugged, high-impact plastic case with strain-relieved power cables, it's built to provide reliable day-in, day-out service for years to come.



CSC'S MULTI-FAMILY LOGIC PROBE 1. AT $44.95, IT DIGS UP A LOT OF INFORMATION WITHOUT BURYING YOUR BUDGET.

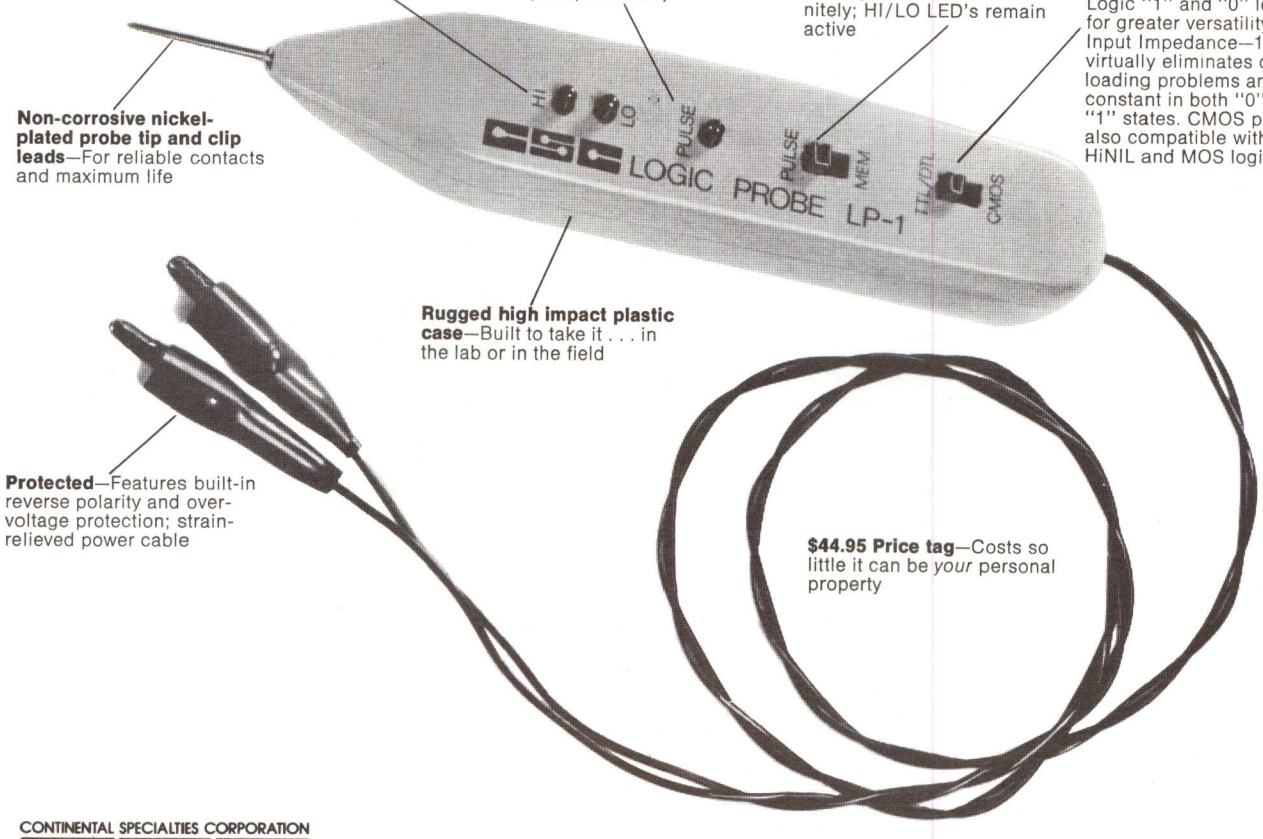
HI/LO LED's—Display level (HI-logic "1", LO-logic "0") of signal activity at node under test

PULSE LED—Lets you know what's going on—and off. Indicates positive *and* negative pulse and level transitions. LP-1 stretches pulses as narrow as 50 nanoseconds to full ⅓ sec. (3Hz pulse rate)

PULSE/MEMORY Switch—PULSE position detects and stretches pulses as narrow as 50 nanoseconds to ⅓ sec. Switch to MEMORY and it stores single shot and low-rep-rate events indefinitely; HI/LO LED's remain active

Logic Family Switch—TTL/DTL or CMOS matches Logic "1" and "0" levels, for greater versatility. High Input Impedance—100K virtually eliminates circuit loading problems and is constant in both "0" and "1" states. CMOS position also compatible with HTL, HiNIL and MOS logic

Non-corrosive nickel-plated probe tip and clip leads—For reliable contacts and maximum life



Rugged high impact plastic case—Built to take it . . . in the lab or in the field

Protected—Features built-in reverse polarity and over-voltage protection; strain-relieved power cable

$44.95 Price tag—Costs so little it can be *your* personal property

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CIRCLE 17 ON INQUIRY CARD

Microcode Kit Allows Users to Develop Non-Standard Interfaces

A User-Microcode Kit intended to enable those who need interfaces for non-standard peripheral devices to fulfill their special requirements has been introduced by The Naked Mini Div of Computer Automation, 18651 Von Karman, Irvine, CA 92664. The kit is intended for use with the general-purpose intelligent cable. A small I/O processor—a PicoProcessor—in the cable can be programmed to interface a system's peripherals with any LSI family minicomputer. Using the kit, this programming can be accomplished by the user at a fraction of the cost normally associated with developing special purpose interfaces.

For systems manufacturers with specialized interfacing requirements, the kit allows existing devices to be used with a system, rather than redesigning the device to fit an existing interface, or developing a new interface.

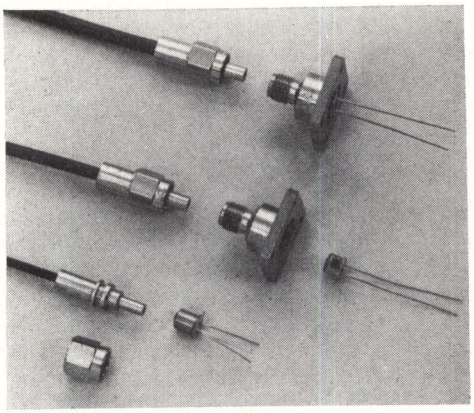
The Distributed Input/Output System is based on an I/O distributor half-card that controls up to eight intelligent cables (see *Computer Design*, Feb 1975, p 18). Cables are available as positive- or negative-true (model 14361-11 or -12).

User-Microcode Kit (model 20631-00) consists of user-microcode manual, ROM-p/ROM generator program manual, macro definitions on paper tape, and ROM-p/ROM generator on paper tape. It provides all necessary documentation and software to code and assemble any microprogram easily and to generate input patterns for the user's ROMs or p/ROMs which are exchanged for ROMs in the cables. User-coded ROM controls cable sequencing to produce the special purpose interface needed. Price of the kit is $1000.

Circle 143 on Inquiry Card

Bundle Connectors Fit Most Currently Available Fiber Optic Cables

Specifically designed to minimize signal loss, maintain mechanical integrity, and provide ease of assembly, Amphenol® fiber optic connectors will join all optical bundles currently available from the leading manufacturers. Introduced by the RF Div of Bunker Ramo Corp, 33 E Franklin St, Danbury, CT 06810, the optical device receptacles are designed to accept phototransistors in large TO-5 cases, although they can handle LEDs and other semiconductor devices through the use of inserts.



Subminiature connectors designed to terminate a wide variety of fiber optic bundle cables, Amphenol series 905 from Bunker Ramo's RF Div accepts phototransistors, but can handle LEDs and other semiconductor devices with the use of inserts

The series includes straight cable plugs, device receptacles, and inline splices as well as other flange-mounted and panel-type receptacles. Costs are kept low by taking the basic design from SMA coaxial cable connectors, and by using brass for the body of the connector rather than more expensive stainless steel or beryllium copper. In addition, the connectors use the same coupling nut and snap ring as SMA connectors.

Principal design change was in configuration of the connector body. Outer geometry was changed to accommodate the maximum cable size—currently a cable with 900 individual fibers. The connector body has a 0.250-in. outside diameter with a possible maximum cable opening of 0.156 in. in its solid brass backend. The mating probe end is then drilled to optimize the packing fraction of the specific bundle.

Designed with the objective of minimizing loss across the connector interface and maintaining the integrity of the mating faces, optic fiber connectors provide acceptable loss, in the area of 3 dB per connection, necessary to make long runs of cable possible. In addition, they provide the small size relative to the cable, positive coupling, and ease of assembly stated as desirable characteristics by the cable manufacturers.

According to Allen B. Kasiewicz, products manager for Bunker Ramo's RF Div, without low-loss bundle connectors, there could be no fiber optic technology. In early fiber optic systems there was as much loss at the connectors as through the entire cable; only through improved connectors have long runs of cable been made possible. While the 3-dB loss is acceptable for optical bundle interface, the advent of single fiber technology will demand optical connectors having a loss of less than 1 dB to make long haul voice communications a reality. Connector loss measurement techniques must also be improved and standardized to provide accurate and repeatable loss measurements.

Circle 144 on Inquiry Card

Network Control System Circumvents Problems in Distributed Data Nets

Claimed to answer the acute downtime problems that plague online users of distributed intelligence data networks, the NCS4000 Network Control System combines network-level diagnostic testing with specific commands that automatically switch in spare modems or dial network lines when a malfunction interrupts data traffic. Designed for very large networks, the system handles up to 4000 remote sites and works with any network configuration at any speed, including mixed-speed systems from 1200 baud to 9600 bits/s. It does its testing in multipoint or point-to-point networks, unhindered by remote processors, multiplexers, or concentrators.

The system, developed by Intertel, Inc, 6 Vine Brook Park, Burlington, MA 01803, is capable of passing test signals around hub sites, allowing in-depth tests to be carried out online

3M got there first. Again.

We put the features of our ¼" DC300A cartridge into a shirt-pocket size. Then we designed a drive—small in size, small in price, for applications where high data reliability must be combined with compact size.

The new DCD-1 system will fit in a 5 inch cube—the cartridge alone measures just 2.4 x 3.2 x .5 inches. Enough about size, let's talk performance.

The drive records *full width* across the entire tape, which virtually eliminates errors. It has an encoding method virtually independent of tape speed, and control logic that prevents the drive from accepting any command that might harm the cartridge.

The electronics are designed to give the system engineer the greatest application flexibility—has byte oriented data input and output and 100,000 byte storage capacity. It's also designed to permit battery operation.

This new system will change the industry much like our ¼" cartridge. So it's time for our competitors to play follow the leader again—if they can. That's the story in a nutshell. Just send the coupon for more details.

All our competitors can do is follow us.

Mail to: 3M Company
Data Products, Dept. 125
Mincom Division, Bldg. 223-5E
3M Center, St. Paul, Mn. 55101

I'm interested in receiving information on your DCD-1 Drive.

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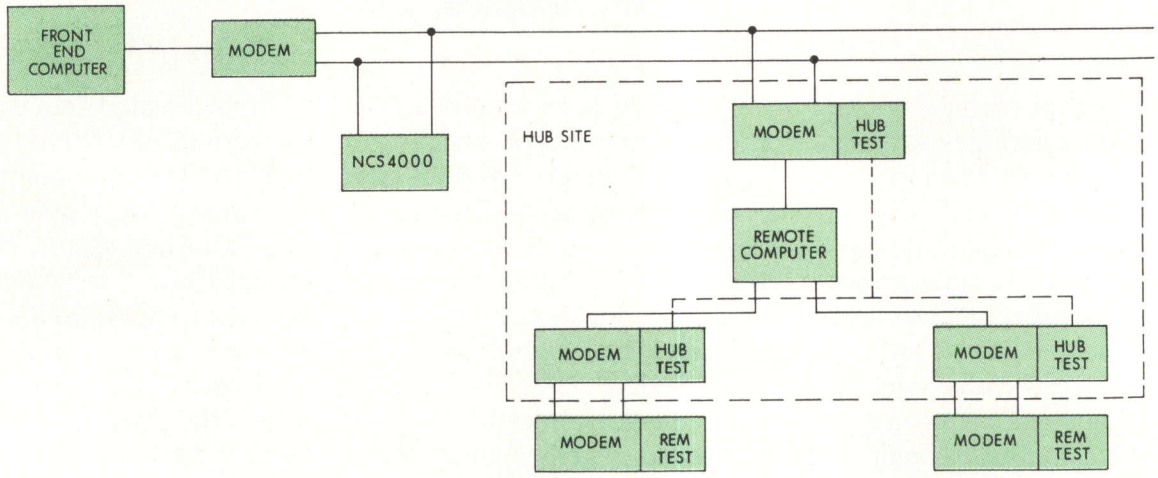
Title_____
Firm_____
Address_____
City_____ State_____ Zip_____
Phone_____

DATA PRODUCTS
Mincom Division 3M COMPANY
3M CENTER · SAINT PAUL, MINNESOTA 55101

CIRCLE 18 ON INQUIRY CARD



Incorporated in a remote processor network, Intertel's NCS4000 Network Control System provides the central site operator with ability to monitor, test, and control remote sites and transmission lines deeply embedded in the network

anywhere in the network. It also provides central site control of testing and restoral functions, serving as a "command post" to solve problems and isolate malfunctions to a transmission line, modem, or data terminal. Test results are displayed in plain English phrases, allowing the system to be run by regular computer personnel; and all diagnostics and restoral functions are performed without operator intervention at remote sites.

Made up of high performance modems and diagnostic and backup hardware, the system accurately transmits and receives data; tests remote modems, transmission lines, and data terminals; and performs remote switching for backup. Online tests can be run while the network is operating to isolate modem, line, or terminal problems without shutting down the line. No hardware or software changes are required to make full use of the comprehensive diagnostics. The system is completely hardware and software transparent, meaning that the system can be installed in a network without the network being aware of its existence.

In many situations, users can take corrective action after locating a problem, without waiting for a service organization to respond to a call. Among the remedial commands available are (1) switch from private lines to backup lines for testing and return, (2) switch in spare modem at remote site, and (3) locate and stop a streaming terminal. Initiated from the central site, these commands allow the user to keep the network up and running until faulty equipment is fixed.

Offline system diagnostics are especially useful in day-to-day preventive maintenance. Running tests each day can detect developing performance degradation and increasing error patterns before they become major problems. Online tests can be run one at a time or automatically; automatically, the entire sequence runs in less than 1 min., indicating pass and fail messages on the status display to alert the operator.

Using offline tests, the operator can count and display bit-error rates without external test equipment; transmit/receive line quality can be judged from the test results displayed on the control console.

Circle 145 on Inquiry Card

Design and Architecture Combined to Form Virtual Computer

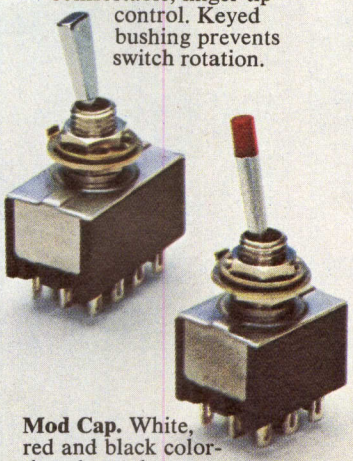
Making extensive use of flexible firmware to provide multiple virtual machine capability, Criterion series computers combine extensive use of emitter-coupled logic, 4K MOS memory chips with error correction (expandable up to 1M byte in the mainframe), pipelined processor which cycles at speeds to 56 ns, and multiple virtual storage which provides up to 16M bytes of virtual memory for each program. Primary architectural feature is use of an internal transfer bus, which uses distributed-intelligence techniques to eliminate much of the processing bottleneck in traditional computer architectures. This combination of features is claimed to provide 35% more processing power at less cost than competing systems such as the IBM 370/115 through 370/135.

Additional features of Criterion models 8550 and 8570, introduced by NCR Corp, Dayton, OH 45479, are a dedicated service processor which manages operating control and acts as the diagnostic control center; direct memory access by high speed peripherals to reduce the workload on the CPU; three levels of diagnostics, which check components and isolate

New "Cricket" sub-miniatures: Interchangeability plus full 6 amp rating.

Cutler-Hammer introduces a broad new line of quality sub-miniature switches whose specifications meet industry standards for size, terminal spacing and bushing height. They're rated 6 amps. They're fully interchangeable. They feature high torque bushings. They're competitively priced. And they're available right now. For more information on new, interchangeable sub-miniature switches, call your Cutler-Hammer sales office or Stocking Distributor. Just ask for "Cricket."

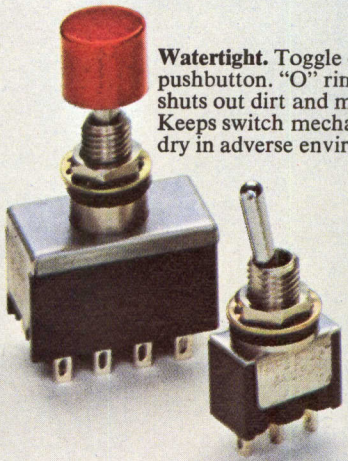
Flat Lever. Designed for comfortable, finger-tip control. Keyed bushing prevents switch rotation.

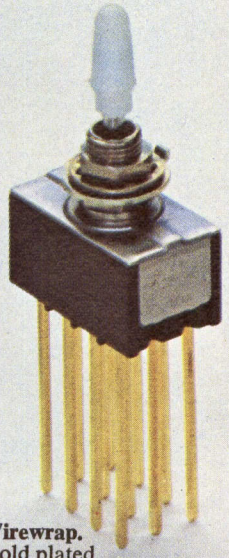


Lever Lock. Locks in position to assure precise control of vital or sensitive functions and equipment. No accidental operation.

Mod Cap. White, red and black color-tipped caps let you choose and vary your operational coding.

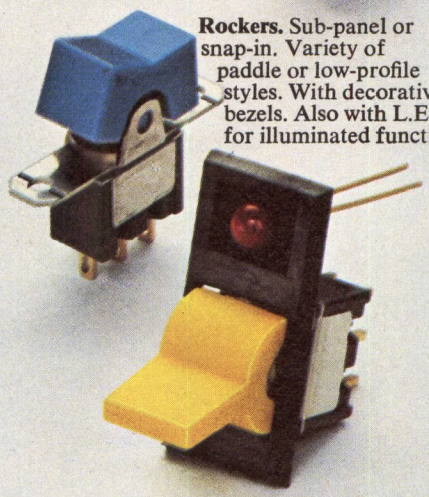
Watertight. Toggle or pushbutton. "O" ring seal shuts out dirt and moisture. Keeps switch mechanism dry in adverse environments.



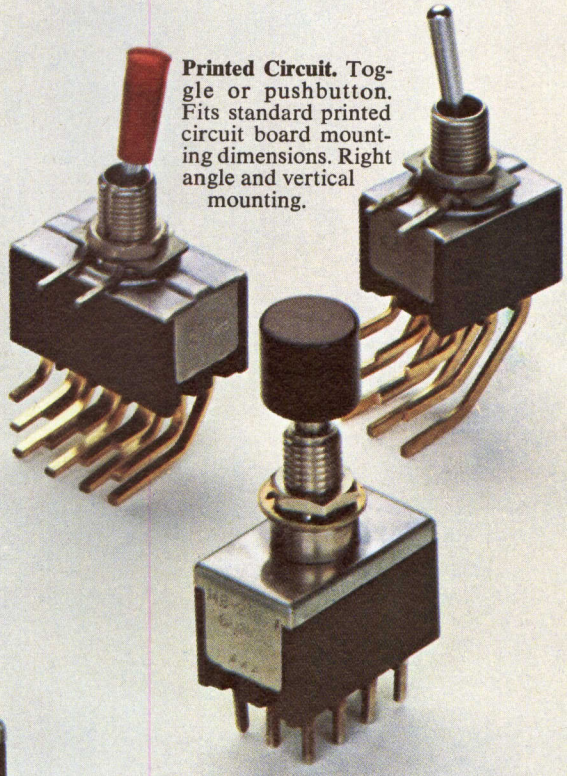


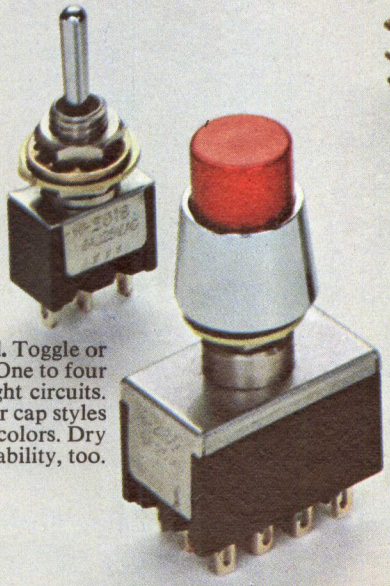
Wirewrap. Gold plated terminals in .750 and .964" lengths to satisfy power or dry circuit requirements.

Rockers. Sub-panel or snap-in. Variety of paddle or low-profile styles. With decorative bezels. Also with L.E.D. for illuminated functions.



Printed Circuit. Toggle or pushbutton. Fits standard printed circuit board mounting dimensions. Right angle and vertical mounting.





Standard. Toggle or pushbutton. One to four poles. Eight circuits. Two decorator cap styles in a variety of colors. Dry circuit capability, too.

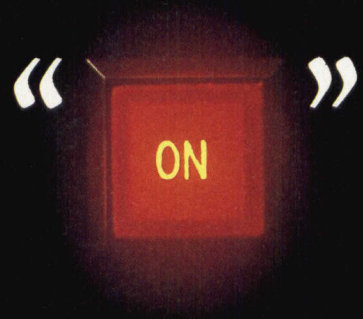
Switch to No.1

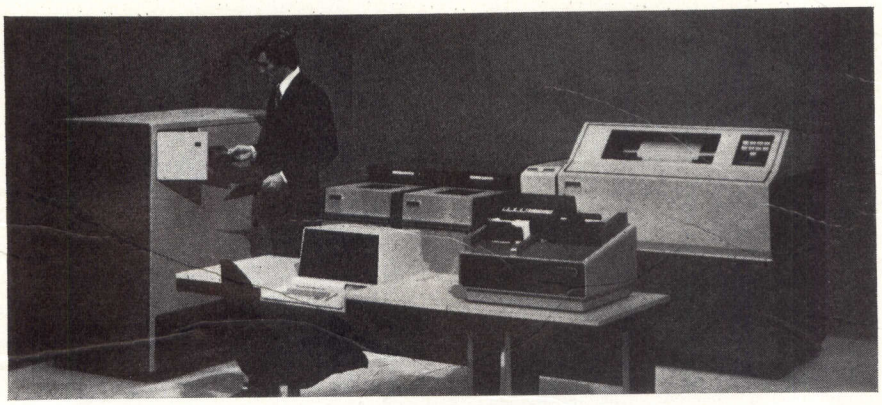
CUTLER-HAMMER
SPECIALTY PRODUCTS DIVISION, Milwaukee, Wis. 53201

CONTROL

CIRCLE 19 ON INQUIRY CARD

A Statement of Our Objectives:





Occupying only 10 sq ft of floor space, NCR's Criterion 8550 mainframe (left) combines MSI and LSI circuits with up to 1M bytes of MOS memory in the same cabinet. The processor's internal transfer bus uses distributed-intelligence techniques to eliminate processing bottlenecks; flexible firmware provides multiple-virtual machine capabilities

malfunctions; online program development; and an additional miniprocessor for intelligent disc interface plus multiple microprocessors for low cost communications interface.

Multiple-virtual machine capability is provided through the use of "tailorable" firmware, which permits the system to duplicate processing capabilities of Century computers. A specially developed set of microinstructions allows the system to function as a COBOL virtual machine. The COBOL compiler can then generate an intermediate language which is interpreted directly and efficiently by the firmware, permitting faster compilation and execution of COBOL programs than on larger conventional computer systems. Comparisons made on object-code compilation, storage, and execution of COBOL programs indicate that object programs compiled for execution on the Criterion contain 25 to 30% fewer instructions than those processed on traditional compilers from the same source code. These studies also show that the high level object programs were executed with 70 to 75% fewer memory access functions.

Among the technological and design concepts incorporated in the system is integrated processor design which interconnects all hardware elements which process or retain data on a single, internal transfer bus using an etched-circuit backpanel to replace most conventional wirewrap panels. Use of miniaturized components on the circuit cards enables medium and large scale processors to have far fewer cards than before. For example, the input/output interface of a Century computer might have 10 or 15 circuit boards; the Criterion has two.

Driving the system with firmware makes for considerable flexibility in structuring commands to be executed by the machine. Firmware is stored on magnetic media, rather than requiring hardwiring; loaded into memory from flexible discs, it resides in and is executed from a dedicated segment of high speed memory. A flexible disc with capacity for 300K bytes resides in a miniature drive housed within the system's single cabinet processor.

Processing subsystem within the computer's mainframe is divided into three segments, each performing instruction fetch, interpret, or execute. System is designed to pass an instruction along from one segment to the next, through use of "live" registers, until execution is complete. Segmentation of the subsystem makes it possible to perform all three functions simultaneously, effectively completing one instruction during each processor cycle. Efficiency of the pipeline technique is further enhanced by the firmware which presents instructions to the subsystem in machine-level microprogramming format. The ability to overlap memory fetch operations with compute functions further speeds processing.

Operating software for the system includes Real Storage Software, comprising batch, online, and multiprogramming executives; and the Virtual Resources Executive (scheduled for release in mid-1977), higher level software featuring virtual storage, file-access method, and the COBOL virtual machine. Other compilers include FORTRAN, NEAT 3, RPG, and BASIC.

Basic model 8550 system consists of minimum 128K-byte memory, 112-ns processor, 600-card/min. reader, 1200-line/min. printer, and 200M-byte disc drive. It has a price of $258,950. The more powerful 8570 with 256K memory, expandable to 1M byte, card reader, line printer, and 300M-byte disc sells for $458,-250. Deliveries are scheduled to begin in the third quarter of this year.

Circle 146 on Inquiry Card

Fiber Optic Cables Available in Production Quantities

Offering distinct advantages over copper wire and eliminating most of copper's limitations, five GALITE™ optical communications fibers, each produced via a different process for optimum efficiency within determined lengths, have been developed by Galileo Electro-Optics Corp, Galileo Park, Sturbridge, MA 01518. The extremely strong, hair-thin glass fibers, which combine the wide bandwidth of waveguide systems with the small size and flexibility of wire, are impervious to organic solvents and retain their optical properties at temperatures above those at which plastic materials begin to deteriorate.

Recommended for use in applications from 1 to 150 ft, Galite 1000 has one of the highest numerical apertures offered for data communication —0.66—as well as the thinnest cladding; the combination minimizes typical coupling losses in optical data links and permits the use of LED light sources.

Designed to reduce attenuation levels to maintain the Radiation Transfer Index (defined as the 10th root of the overall transmission efficiency) at a high level for long distances, 2000 fiber is recommended for applications ranging from 150 to 250 ft. A step-index fiber, the 3000's cladding glass is deposited by a patented process to minimize scattering losses at the core/clad interface. Range is 250 to 1100 ft. A plastic-clad fused silica optical fiber, the 4000 features superior nuclear radiation hardness. Although transmission properties extend from the ultraviolet to the infra-

Pick a signal and any mini...Using RTP

Let's say you have some relay contacts to monitor, 115 VAC control signals to sense, 4 to 20 mA analog process signals to measure, and you need to provide relay output contact closures and 4 to 20 mA set-point signals.

This application can be handled by a few standard RTP analog and digital input/output cards, a Universal Controller, and an RTP Bus Converter.

First, you select the cards. Our family of process I/O interface cards provides the versatility to match almost all industrial sensors and actuators.

The Universal Controller provides the logic, power and space for up to 16 of these cards, in any combination.

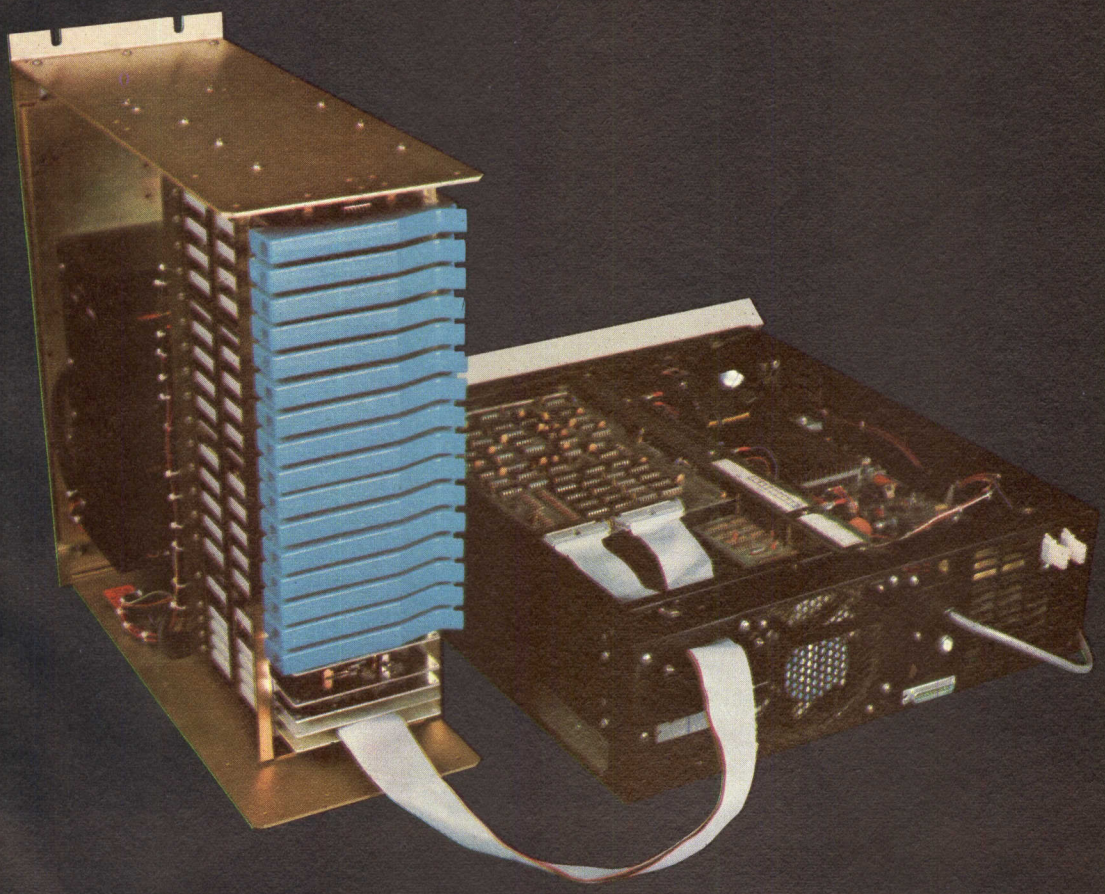
The RTP Bus Converter interfaces the Universal Controller to your mini by converting your mini's parallel I/O bus to the standard RTP parallel bus. Appearing transparent to your computer, it allows the Universal Controller to be directly programmed, as if it were one of the computer's peripherals. Best of all, RTP Bus Converters are available for all popular minicomputers.

Those are the essentials! But it's kind of tough to design a measurement and control system from an ad.

So, we'd like to send you "Using RTP." This booklet will provide you with a concise RTP subsystem design overview. Just circle our number on the Reader Service Card.

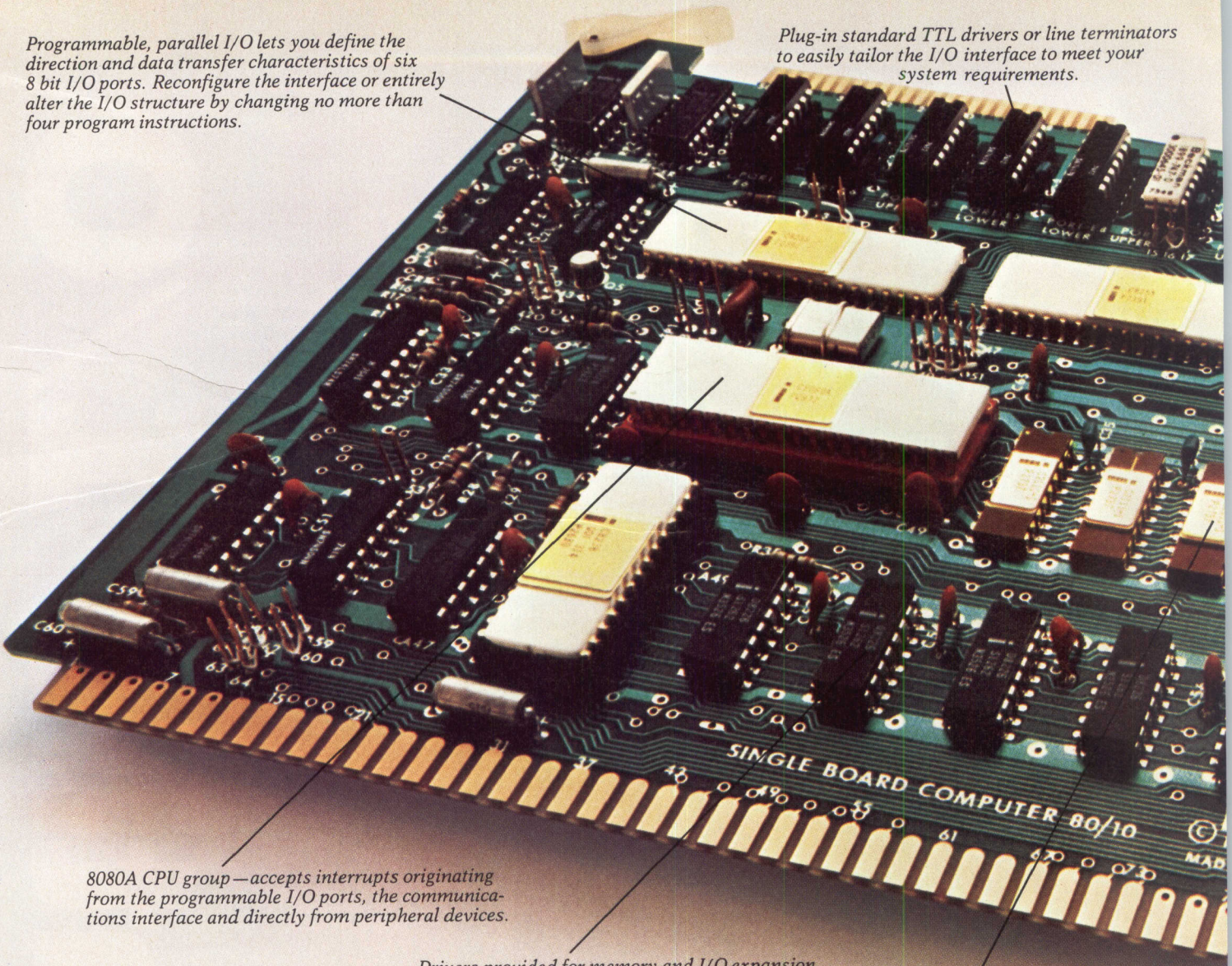
Computer Products, inc.

Versatile I/O



1400 N.W. 70th Street, Fort Lauderdale, Florida 33309 • (305) 974-5500, TWX (510) 956-9895
Japanese Distributor: Tamagawa Seiki Co., Ltd. 3-19-9 Shin-Kamata, Ohta-Ku, Tokyo, Japan 144. Phone: 03-731-2131.

CIRCLE 21 ON INQUIRY CARD



Programmable, parallel I/O lets you define the direction and data transfer characteristics of six 8 bit I/O ports. Reconfigure the interface or entirely alter the I/O structure by changing no more than four program instructions.

Plug-in standard TTL drivers or line terminators to easily tailor the I/O interface to meet your system requirements.

8080A CPU group—accepts interrupts originating from the programmable I/O ports, the communications interface and directly from peripheral devices.

Drivers provided for memory and I/O expansion. Simply plug any of the SBC 80 RAM, EPROM/ROM, I/O or Combination expansion boards into the standard SBC 80 card cage.

1K bytes of high speed, low power static RAM.

The first complete single

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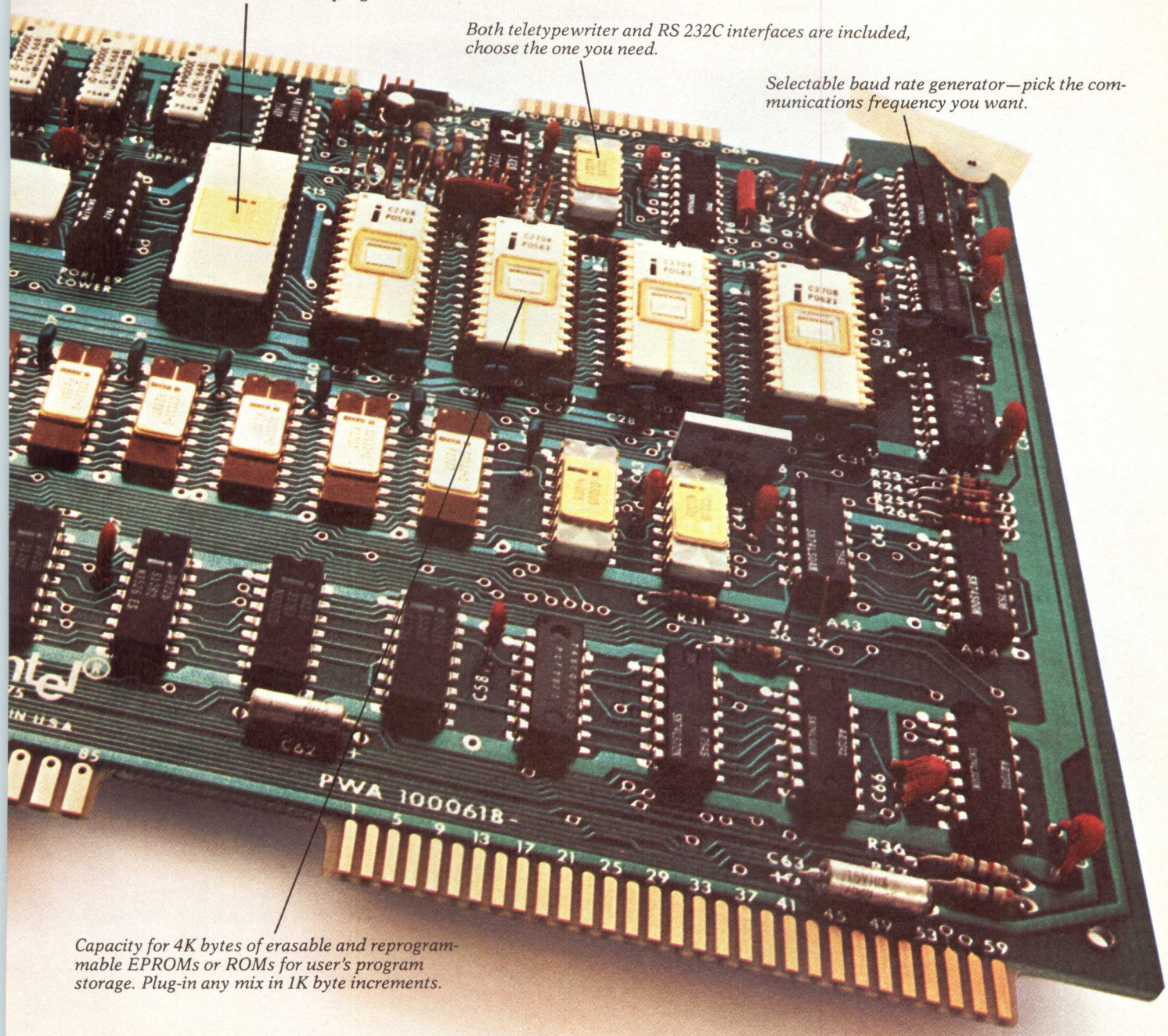

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The five fibers may be sheathed in different jackets depending on the intended use of the finished cable. All come jacketed in PVC or TEFZEL™; Galite 3000, 4000, and 5000 are also available in a strengthened jacket—a combination of TEFZEL and KEVLAR™. Users may select from standard cables containing one to two fibers or those containing bundles of 7 or 19 strands.

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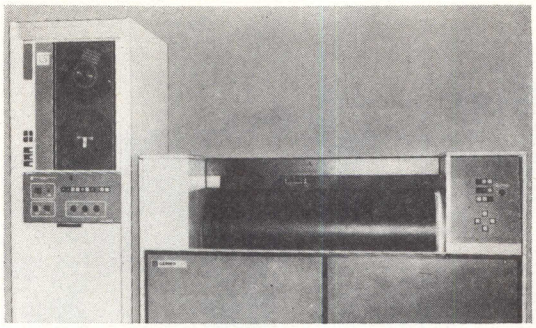

Prepackaged offline plotting system from Gerber Scientific incorporates model 42 "flat-bed drum plotter" with 36 x 48" plotting surface and uses series 6200 microprocessor-based control unit to provide plotting system control. Controller permits significant cost reduction without consequent reduction in performance characteristics

Prepackaged Offline Plotting System Provides High Quality at Low Cost

A completely prepackaged offline plotting system, the self-contained 6242 Data Superplotter System is claimed to provide users with high quality performance and reliability characteristics of higher priced systems at a significantly lower cost. Developed by Gerber Scientific Instrument Co, 83 Gerber Rd, South Windsor, CT 06087, the system incorporates the model 42 Superplotter and series 6200 plotting system control. The control uses microprocessor technology to provide input data handling and high speed contouring capabilities, permitting cost reduction without sacrificing performance or features.

The model 42—called a "flat-bed drum plotter", because of its plot quality, accuracy, acceleration, and speed and space-saving advantages—features stationary motors and minimum inertia, and is capable of 2.5-G acceleration. This is coupled with a plotting speed of 42 in./s, accuracy of ±0.004 in., and repeatability of ±0.002 in. to guarantee high quality performance and reliability. The drum offers an ideal writing surface while affording full visibility and easy access to the 36 x 48" plotting area. Fast paper loading is provided by a vacuum system which smooths the wrinkles from any plotting material on the curved writing surface and holds it there without clamps, tape, or masking material.

The microprocessor-based control unit provides input data handling and high speed contouring capabilities, and enables the unit to handle English or metric data units. Input is standard ½-in. magnetic tape with 800- or 1600-bit/in. density. Programs for the control reside in ROM modules, eliminating the need for program loading.

Circle 148 on Inquiry Card

Magnetic Tape Units Use Group Coded Recording For High Performance

High performance magnetic tape units featuring high density Group Coded Recoding, Uniservo® 30 series transfer at from 320K bytes/s at 1600 bits/in., to 1250 bytes/s at 6250 bits/in. Introduced by Sperry Univac, a div of Sperry Rand Corp, PO Box 500, Blue Bell, PA 19422 for use with 1100 series computers and 90/60 and 90/70 systems, models include the 7- and 9-track model 30, and the 9-track 32, 34, and 36.

Group coded recording (GCR) techniques provide fast throughput, and extensive capability for "on the fly" error correction while recording at 6250 bits/in. on ½-in. magnetic tape. High transfer rate substantially reduces I/O portion of the time usually necessary to perform tape-oriented serial file processing. GCR provides data storage 3.9 times more dense than phase-encoded recording, and 7.8 times more dense than NRZI techniques. Error correction unique to GCR enables an infinite burst of 2-track errors to be corrected on the fly; in addition, a high percentage of errors involving more than two tracks can be corrected, assuring a high level of data integrity.

Basic tape subsystem consists of a 5042 control unit and from one to eight tape units in any combination. Tape units are designed to provide completely automatic tape loading using industry standard wraparound cartridges. Also incorporated are automatic tape threading; power windows; and a radial tape interface, which permits each unit to be attached directly into the control unit for data transfer, ac (power) and dc (signal control) primary power.

Models in the series include the model 30 (type 0872-00/01) a 9-track PE and NRZI unit with transfer rate of 320K bytes/s at 1600 bits/in., 160K bytes/s at 800 bits/in., with tape speed of 200 in./s; type -02/03 is a 7-track NRZI unit that transfers at 160K bytes/s (800 bits/in.), 111.2K bytes/s (556 bits/in.), and 40K bytes/s (200 bits/in.).

Model 32 is a 9-track unit designed for GCR and PE recording. It transfers at 470K bytes/s at 6250 bits/in., and 120K bytes/s at 1600 bits/in. Tape speed is 75 in./s. With tape speed of 125 in./s, the model 34 records nine tracks (PE and GCR) and transfers 780K bytes/s at 6250 bits/in. and 200K bytes/s at 1600 bits/in.

Designed only for use with 1100 series computers, the model 36 provides GCR and PE recording on 9-track tapes and transfers at 1250K bytes/s (6250 bits/in.) and 320K bytes/s (1600 bits/in.) with tape speeds of 200 in./s.

Tape units range in price from $34,800 to $38,880; a basic control unit for 90/60 and 90/70 computer systems has a purchase price of $55,392; a buffered control unit for use with 1100 series computers costs $72,336. □

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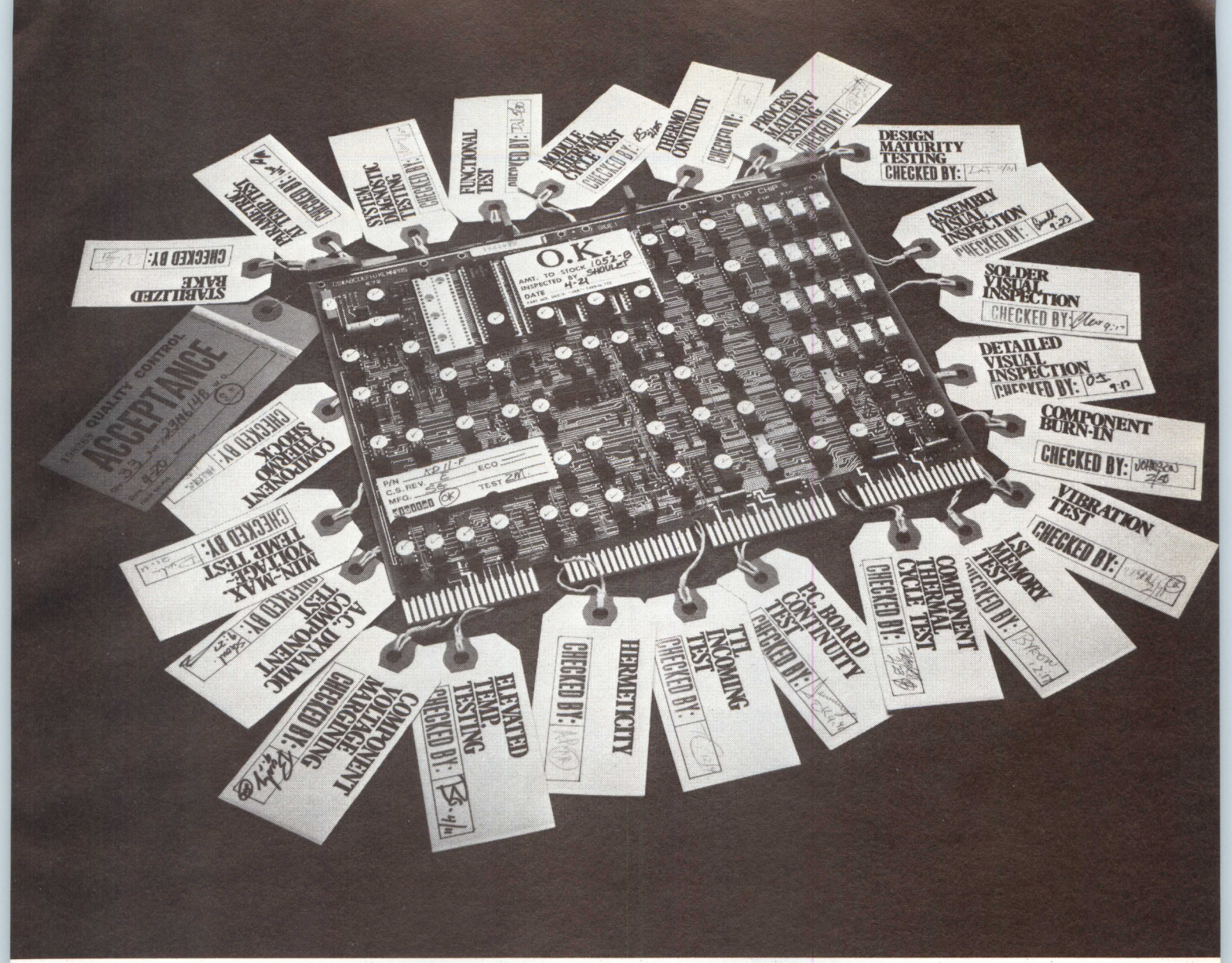

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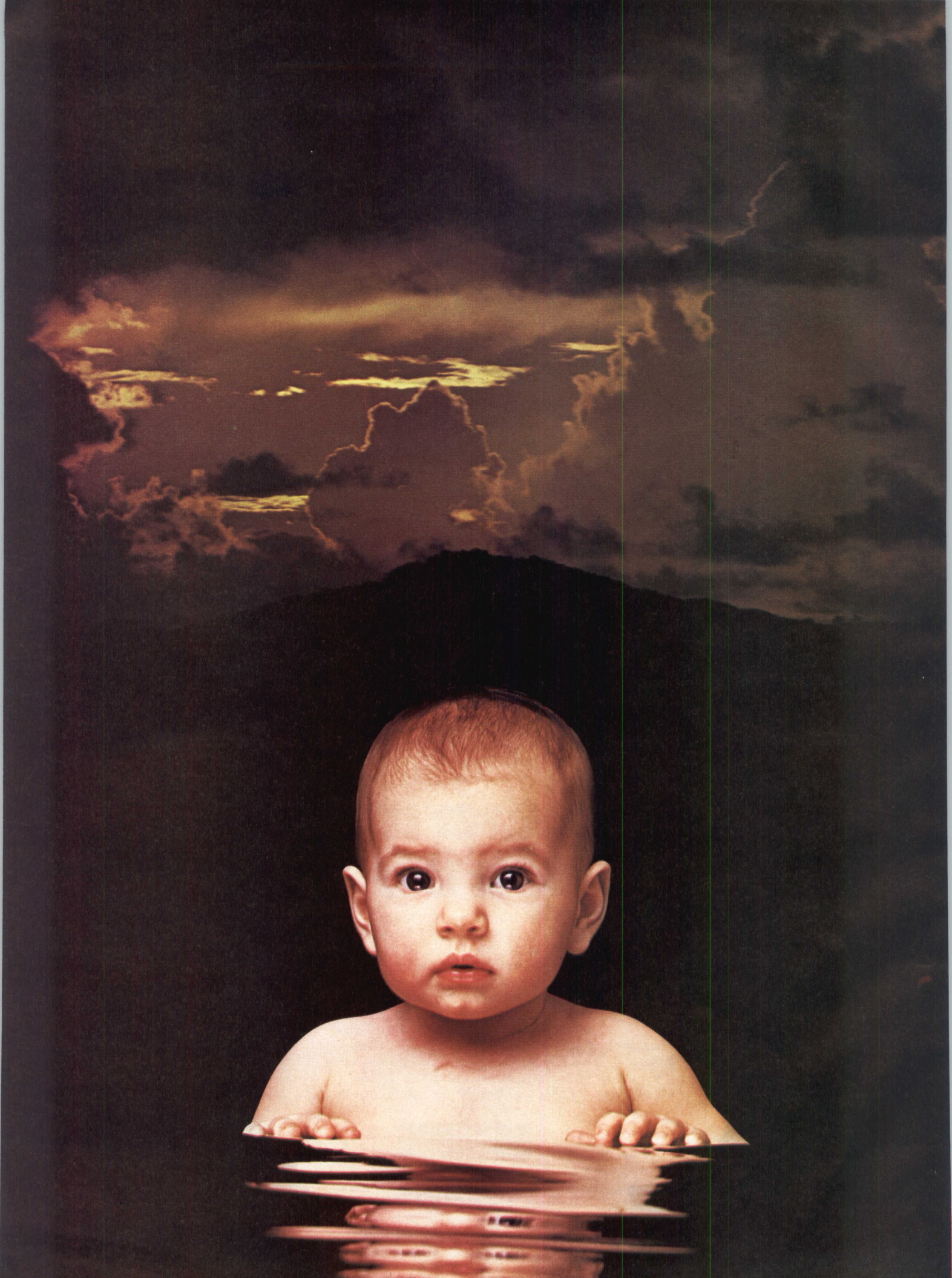

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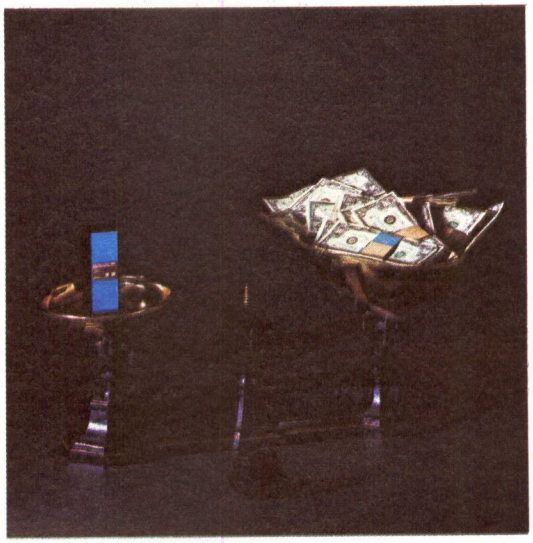

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DEVELOPMENTS

IIL Device May Simplify Use of Existing Lines For Data Transmission

Conversion of analog data transmission circuits for digital use involves many problems. Among these are the difficulties resulting from adding large numbers of logical switching elements which operate at high clock frequencies.

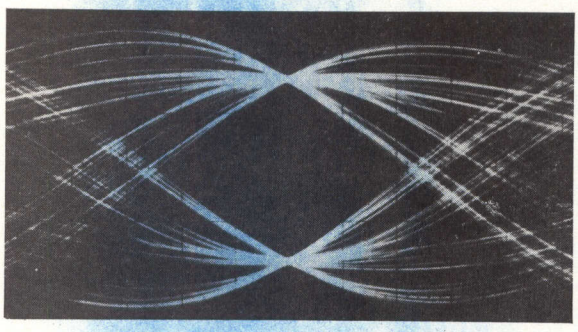
Reportedly, such difficulties have been overcome by a digital transmitter developed by Philips Research Laboratories in Eindhoven, The Netherlands. This transmitter is made up of a digital signal filtering and modulating circuit, a read only memory (ROM), a digital-to-analog converter (DAC), and an analog filter. All but the ROM are contained on a single silicon chip produced by integrated injection logic (IIL) technique. This transmitter was developed in laboratory experiments and will not necessarily be produced for marketing.

Digital input signal is a binary pulse train whose frequency spectrum contains many "harmonics" and which has a periodicity equal to the fundamental frequency (ie, the repetition frequency of the pulses). The digital filter passes only a frequency band centered on a sufficiently high harmonic of the fundamental, easing separation of upper and lower sidebands which are formed by the modulation process. Frequency band of the signals passing through the filter is then transferred to the desired frequency region in the telephony band by modulation of a carrier of suitable frequency.

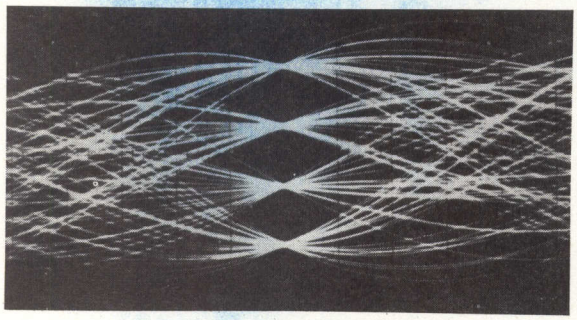
Undesired bands left in the signal (originating from the modulation process and from periodicity of the digital output signal) are of such high frequencies that they can easily be suppressed afterwards by a simple low pass RC network rather than an expensive, complicated digital post-modulation filter. Because the digital band filter is an interpolating filter, fewer circuit elements are required and a low clock frequency can be used. The modulation process is simplified by suitable choice of system parameters.

Output spectra of various shapes and positions and various types of modulation (single, vestigial, and double sideband) are obtainable from the IIL chip by changing content of the ROM.

A combination of two such transmitters, each with a corresponding ROM, allows various types of phase modulation, eg, 8-phase modulation with 4800 bits/s at a carrier frequency of 1800 Hz. Vestigial sideband transmitters for signals of 2400 and 4800 bits/s have also been built.



(a)



(b)

Eye patterns of signals produced by the vestigial sideband transmitter. Frequency band of both signals covers the 600- to 2700-Hz region; carrier frequency is 2100 Hz. (a) 2-level eye pattern for 2400 bits/s; (b) 4-level eye pattern for 4800 bits/s

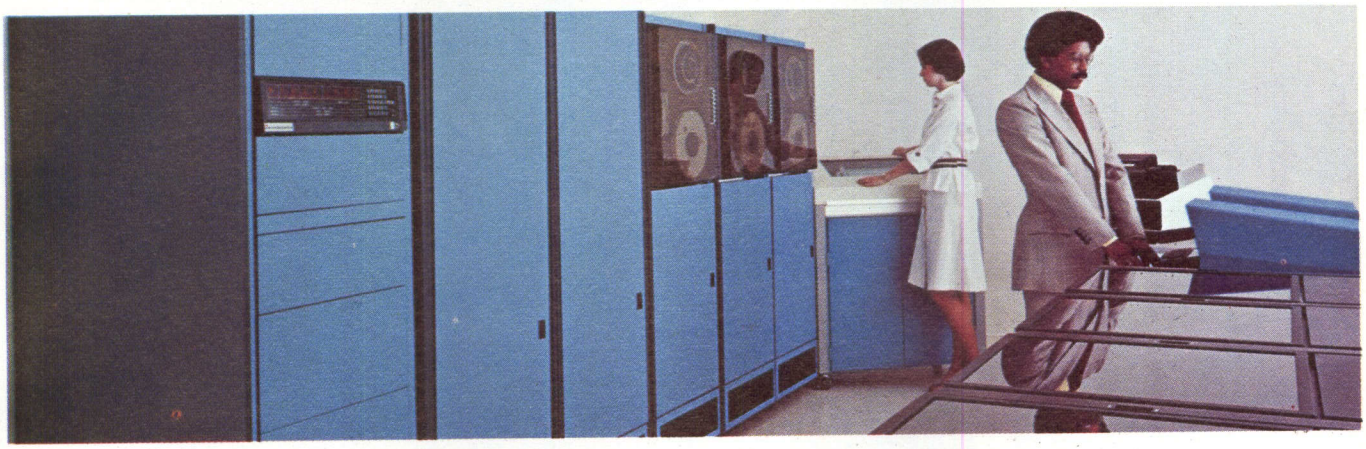
Megabit CCD Chip Arrays Predicted for Late 1977

Parallel development programs, one under contract to the U.S. Naval Research Laboratory and the other company-funded, are expected to result in CCD IC memory arrays of 100K bits by late this year—and over 1M bits by late 1977. TRW Inc's Defense and Space Systems Group, Redondo Beach, Calif, developer of the devices, states that charge coupled device (CCD) semiconductor technology will produce bulk storage memory units capable of storing several million bits of digital information on a monolithic integrated circuit (IC). Such devices would help large data networks provide faster information flow with simpler equipment.

Among the company's CCD work to date are development and operation of logic devices and arithmetic devices, including a 3- x 3-bit multiplier and a 4- x 4-bit adder. Success in producing these devices is expected to lead to development of a single-chip fast Fourier transform (FFT) analyzer computer by early 1977. A second chip will contain memory for the analyzer. Comparable bipolar FFT analyzers require more chips, yet the CCDs are expected to offer equal performance at a fraction of the power.

The company claims that the very high circuit density possible with CCDs offers many advantages over conventional technologies. For example, "the density and the speed/power product of a typical digital CCD is about 10 times better than present n-channel MOS devices. When compared to IIL devices, the TRW digital logic CCDs appear similar in performance at low operating speeds; at speeds over several megahertz, CCDs offer a marked speed/power performance improvement over IIL devices. Block-oriented

INTERDATA 8/32 MEGAMINI LIFE SUPPORT



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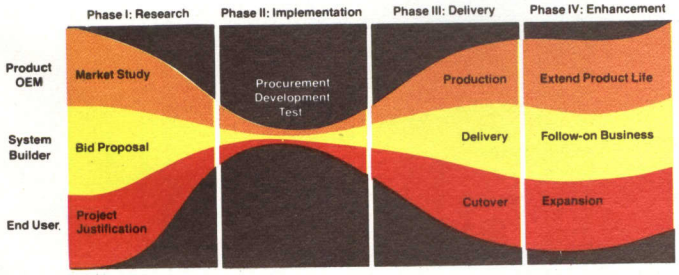

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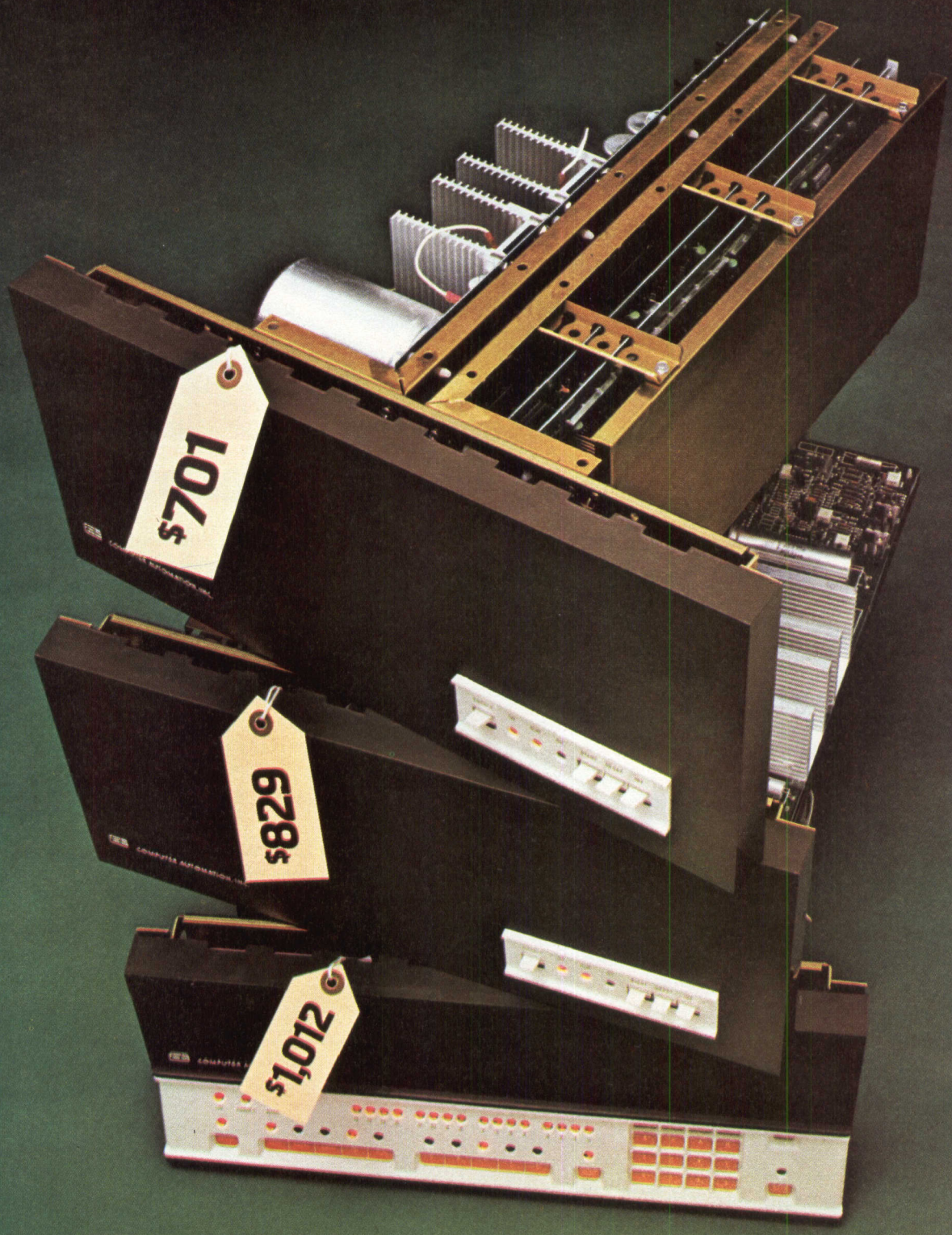

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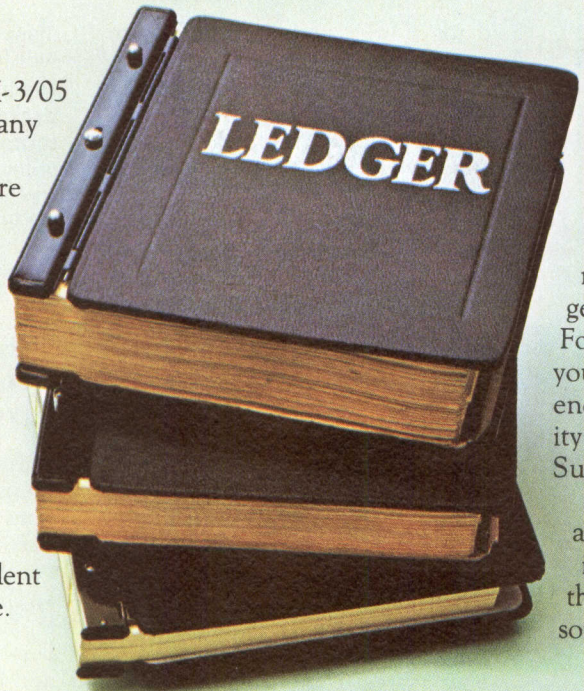

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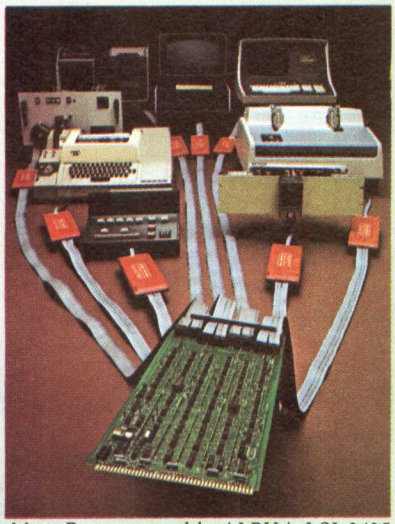

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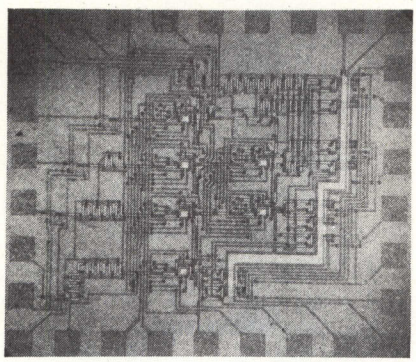
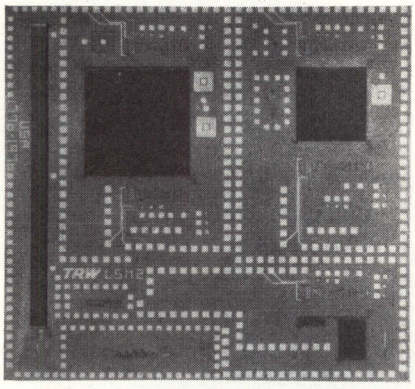


Digital 3 x 3-bit multiplier, one of several CCDs under development by TRW, has far greater density than multipliers built with conventional MOS and bipolar technologies

memories capable of storing several million bits of data can be produced in extremely small sizes. These could eventually replace video storage discs and many other temporary storage memories where a block of data must be retrieved instead of an individual bit or data word."

Among the operating advantages of CCDs are that memory array power requirements are only on the order of a few microwatts per bit, and shifting speeds can be attained that are equal to those of many bipolar memories (but in chip densities that cannot be approached by bipolar devices). Also, other common delays such as transistor turn-on time are absent.

Applications of CCD bulk memories include first-in, first-out computer memories where data must be held for a brief period, digital voice processing systems where digital voice signals must be held for additional signal processing, and photocopy machines which could store a page of information for use in making multiple copies.



Comparison of two 16K-bit CCD memories built by TRW on test chip at different packaging densities. 100K-bit arrays are planned for this year and arrays of over 1M bits are expected by late 1977

Basic operation of a CCD depends on the transfer of an electrical charge from one circuit element to the next. Operation results from the movement of carriers caused by a voltage difference between circuit elements that transfer or couple the charge to the next element.

A piece of crystalline silicon coated with a very thin layer of SiO_2 (about 1000 Å thick) forms the basic CCD structure. Gates are then deposited on top of the SiO_2 layer. Basic silicon and gate layers form the two circuit elements separated by the SiO_2 insulating layer in a capacitor-like structure.

The charge is actually contained in a well that forms under the electrode in the silicon. In surface channel devices, carriers are transferred on the surface of the silicon. As a voltage is applied to the gates, the charges are forced to move to the next charge well.

CCD memories are sequential in operation with the elements of one circuit physically coupled to the next circuit in a chain. The charge or the data bit is transferred from one storage cell to the next by transferring the charge from device to device through basic silicon substrate. The extremely close spacing possible for the storage cells on a CCD array makes it ideal for large scale volatile bulk storage memories.

CCD sizes are dependent on the size of the electrodes. The company states that, using conventional semiconductor processing techniques, it should become feasible to build a single IC CCD memory capable of storing a million bits of data by the end of 1977, and that more advanced photolithographic techniques could easily expand this type of memory to 10 million bits within the next two years.

Development of sequential high density CCD memory is continuing. Read-only memories of extremely high density can also be produced from the same structure. Digital arithmetic and logic devices are being developed, and early in 1977 complete CCD digital logic and arithmetic functions capable of duplicating many functions of a minicomputer will be possible on a silicon chip. The company believes that "high circuit packaging density and low manufacturing costs should make CCD technology very cost-effective with performance improvements over popular MOS and bipolar technologies."

"Talking Board" Offers Speech Synthesis for Diverse Applications

Currently performing the speech synthesis, audio, and power supply functions of a talking calculator, the S16001-A module contains a 24-word vocabulary specifically useful for that application. However, Prof Forrest S. Mozer of Berkeley, Calif—a member of the Univ of California faculty and inventor of the speech synthesizer —says that another 64-word vocabulary is in preparation. This expanded vocabulary will include basic electrical English and metric measurement units, some mathematical terms, and sufficient numerals to allow generation of any number from zero to 1 million.

Application areas for the "expanded" unit include the machine tool industry where an operator might be instructed step-by-step via synthesized voice. Another might be providing vocal landing instructions to an aircraft pilot.

"Talking boards" are fabricated as 4 x 7" printed circuit cards weighing 3 oz. The power supply provides —5 V ±10% at 150 mA max, and battery operation is possible. Vocabulary is synthesized from a male voice.

As shown in the diagram, V_{CC} (—5 V) is applied to a voltage converter which generates the —15 V required by the speech synthesis microcontroller (CRC). When the synthesizer is idling (not speaking), the CRC generates a logic signal that turns off power to the read-only memory (ROM) and the "busy" signal is low. When the "start" input goes high, the CRC detects it and turns on power to the ROM. At the same time it raises the "busy" output to a logic 1 to indicate that speech processing is in operation.

When the start signal returns to a logic 0, the CRC reads the information on the "data" input lines. These signals are used to fetch control in-

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The dependable iCOM controller is already used in hundreds of different systems. It takes the load off your software, letting your microprocessor do its job without getting bogged down. Auto track/sector seek and verify, full sector I/O buffers, auto CRC generation and checking, are just a few of the controller features. Handles from 1 to 4 drives with no changes in software or hardware. IBM compatible, too.

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iCOM's Frugal Floppy™ sells for only $995 in small OEM quantities. If you need just one it's still only $1195.

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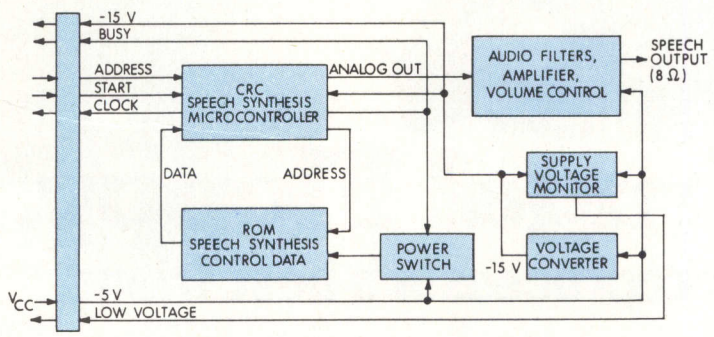
CIRCLE 27 ON INQUIRY CARD



A 24-word calculator vocabulary is now being expanded to a 64-word capability that will contain units of measurement, math terms, and numeral combinations to permit synthesis of any number up to 1 million

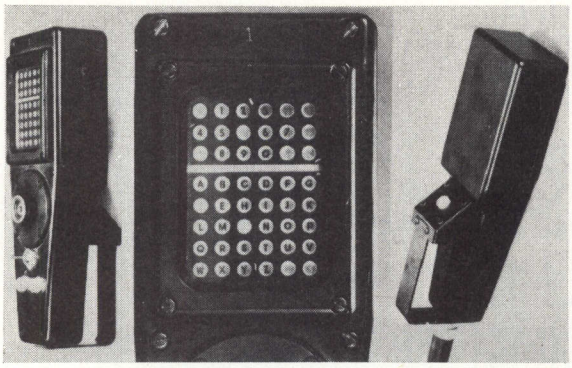
formation stored in the ROM. The CRC also determines the addresses needed to access data stored in the ROM. From ROM information, the control chip determines how to say the word, the pronunciation, how long to say the word, and when to stop saying the word. The start signal can interrupt the speech synthesizer at any time to initiate spoken output of another word.

Sound is produced from data stored in the ROM. The microcontrol chip selects the ROM addresses to be read and speech is produced from the data stored in a given location. A sound is made up of many digital bits, each one making up an increment of the analog audio signal. The control chip also converts the digital information produced in conjunction with the ROM to an analog audio signal via an on-chip D-A converter.

The audio signal is filtered and amplified. A volume control adjusts audio level, and final speech output is obtainable at an earphone jack near the volume control.

Data Entry Device Will Require Only One Hand For Full Operation

A small data entry device that functions on commands from one switch and two pushbuttons—all of which can be controlled by one hand—has been developed by Britain's Defence Ministry's Signals and Development Establishment. Although originally intended for military use where the operator might need to have one hand free, the National Research Development Corp, London, England believes the device is applicable to stocktaking and other computer peripheral operations.



Data entry device developed in England requires only limited manual dexterity of one hand for operation. User moves a switch with thumb to choose upper or lower section of keyboard, presses a button—also by thumb—step-by-step to position a light to the required character, and then presses a button with a finger to enter that character

In use, the operator moves a thumb-operated switch to select either an alphabetical or a numerical section on the keyboard. Then a button, also worked by thumb, is pressed to move a light one step at a time, horizontally, vertically, or diagonally from a central position to a required character. Direction of movement is determined by the angle at which the button is pressed. A button on the back of the device is then pressed with a finger to enter the character. This action also returns the light to the central position. A space is entered by pressing the character entry button while the light is in a clear spot.

Letters are arranged alphabetically, except for E—the most widely used letter—which is out of sequence in order to place it diagonally next to the center position. Average rate of input is 1 char/s. For special applications, number-only or letter-only arrays or other configurations could be designed.

Digital Techniques May Solve High Frequency Radio Relay Problems

With the growing capacity requirements for data transmission, radio relay systems have become more and more important. However, the expansion into higher frequencies to alleviate traffic jams has brought in new problems. For instance, at the higher frequency range, signal attenuation increases drastically, especially during periods of rain.

That problem is solved by organizing the networks such that there are shorter radio paths and, therefore, more repeater stations. This, in turn, necessitates that transmission quality be maintained at a high level, such as by a digital transmission system in which, by means of regeneration, the wanted signal can always be freed completely from noise, distortion, and adjacent-channel interference.

Digital radio relay system PSK 120-240/15000, developed by Sie-

Power on or power off, reliable core holds the data. That's why system engineers are taking a new look at Ampex MCM, the Microcomputer Core Memory.

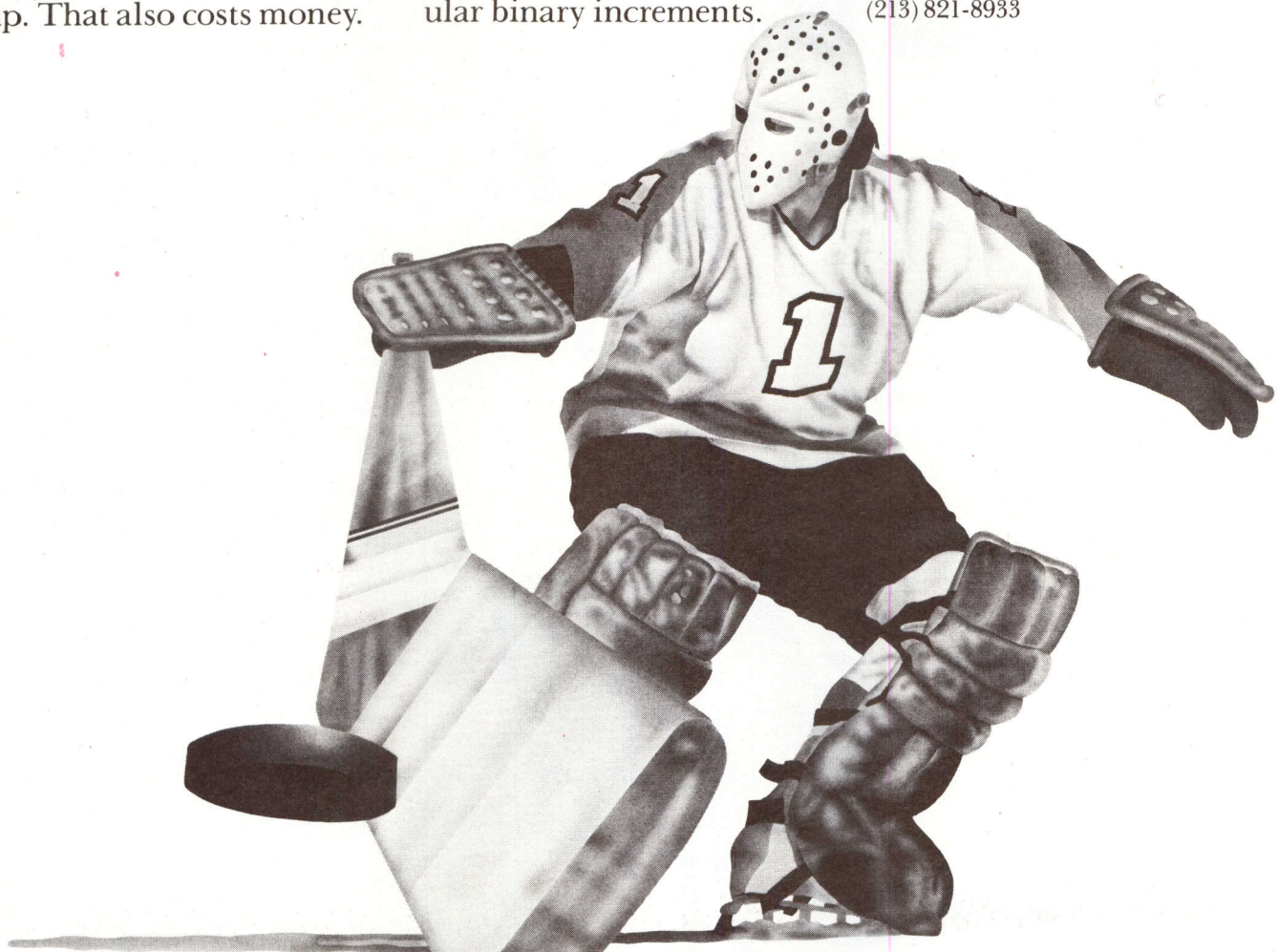
Sure, you can use semiconductor memory. Maybe smaller and cheaper at first glance. Then, the first time somebody plays with the power, you lose data. So you reload. That costs money. Or you design battery back-up. That also costs money. Matter of fact, *every* system provision for data preservation costs money. In the end, core costs less than semiconductor memory.

Get Ampex MCM. Ready to plug in and operate. No fussy assembly of components on boards. No support circuitry. Nothing but the steady reliability of core. Word lengths from 4 to 18 bits, storage capacity from 256 to 4096 words. In all popular binary increments.

Build Ampex MCM into your system, and you won't squander time and personnel bringing programs back up after the power goes down. Block the power play. Get Ampex MCM.

AMPEX

Ampex Memory Products Division
13031 W. Jefferson Blvd.
Marina del Rey, California 90291
(213) 821-8933



MICROPROCESSOR CORE MEMORY BLOCKS POWER PLAY

CIRCLE 28 ON INQUIRY CARD

mens AG of the Federal Republic of Germany, operates with differential direct 4-phase shift keying of the carrier (4DPSK). Information is contained in phase shifts at 0, 90, 180 and 270 deg. Such modulation permits a compromise among immunity to interference, bandwidth requirements, and technical complexity.

One system can transmit two bit streams at a rate of 8.448M bits/s, corresponding to 2 x 120 voice channels. Transmitters and receivers operate in the 15-GHz range. In accordance with CCIR recommendations, two 120-MHz wide bands are used, each with eight channels separated by 14 MHz. A total of eight transmitters and eight receivers can be operated with one antenna; four of each polarized vertical and the other four polarized horizontal. Parallel to these systems, another eight systems can be operated via a second antenna, with the rf channel arrangement shifted by 14 MHz. A total capacity of 3840 (2 x 8 x 240) voice circuits can therefore be achieved on a radio path in this frequency range. Transmit power is 100 or 500 mW, according to choice. On the basis of rainfall figures for Germany, radio path lengths of 22 to 28 km are advisable.

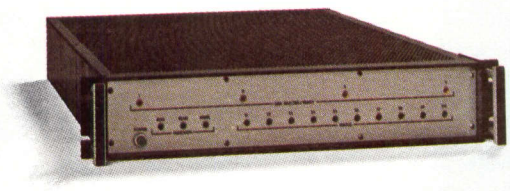
Equipment can be installed close to the antenna, resulting in lower transmit power requirements and less expensive overall construction. A weatherproof case measuring 700 x 700 x 370 mm, the front serving simultaneously as a parabolic reflector, accommodates four system units. One transmitter section, one receiver section, and one power supply section can be combined to form an equipment inset which fits into style 7R narrow racks.

This system is said to be particularly suitable for tightly meshed radio relay networks whose nodes have several links radiating from them and which have relatively short transmission paths of between 25 and 50 km. Such network structures and corresponding transmission capacities can be found, for instance, at the short-haul level of the Federal German communication networks. This is where the radio relay system will probably be used first, when it becomes necessary to transmit large numbers of digital signals, such as PCM speech bands, data for communication between EDP systems, or coded videotelephone signals. □

When you choose DATUM mag tape or disc systems You get performance... but We get system responsibility!

Choose a DATUM peripheral-device-controller system knowing that you will be free of any problems when the system is installed! No matter what the problem, or where, DATUM will get you up and running . . . because DATUM assumes system responsibility in every system installation.

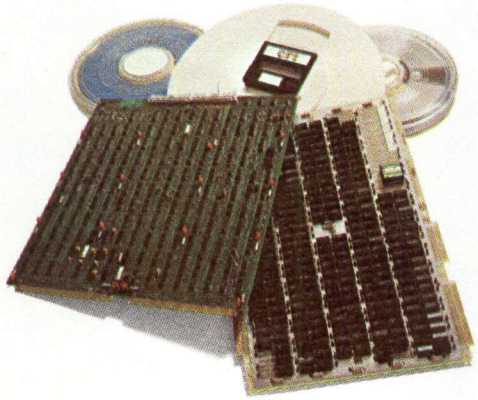
Only DATUM has designed, built and installed over 6000 controllers and systems for so many different minicomputers to interface with so many different peripheral devices. And, of all device-controller manufacturers, only DATUM/Peripheral Products Division has the advantages and expertise given by cooperating in-house divisions that design and build custom data acquisition systems and sophisticated micro-programmed minicomputers.



Series 4091 Disk Controller

Check these features!

• Triple-Density NRZI Formatting • Dual-Density PE/NRZI Formatting • 200 IPS for all Existing Interfaces • Single-Source Responsibility for all Major Tape-Drive Manufacturers



Off-the-shelf controllers for these computers:

Computer Automation Alpha LSI • **Data General** Nova and Eclipse • **DCC** 112, 116 • **DEC** PDP-8, -8e, -8i, -8l, -9, -9l, 11, 12, 15 • **Harris Communications** Slash 4, Slash 7 (Datacraft) • **HP** 21MX, 2100, 2114, 2116 • **Honeywell** 316, 416, 516 • **IBM** 1130 • **Interdata** 716, 832 • **Lockheed** SUE • **Micro Systems** 810 • **Rolm** 1602, 1603 • **Varian** 620i, 620l, 620f, V73, V74, V75, V76.

DATUM Tape Controllers are available with the following Formatters:

NRZ: 9-track, 800 BPI and 7-track, 800, 556, 200 BPI • **PE:** 9-track, 1600 BPI • **QUAD:** 9 track 1600, 800 BPI and 7-track 800, 556, 200 BPI.

Each formatter controls as many as four drives with individually-driven ports for each tape unit. All drives with industry-compatible interfaces can be accommodated.

DATUM formatters provide all timing for IBM-compatible inter-block gaps and correct head-positioning between records.

Advanced MSI/LSI hybrid technology gives optimum cost/performance ratio • Systems and controllers are compatible with your computer software • Components plug together and into the computer for uncomplicated installation • Complete with controls, power supply, all necessary cables, diagnostic software and instruction manual.

Write for specifications and prices and for a copy of, "How To Buy Computer Peripherals."

Series 5091
Magnetic Tape Controller

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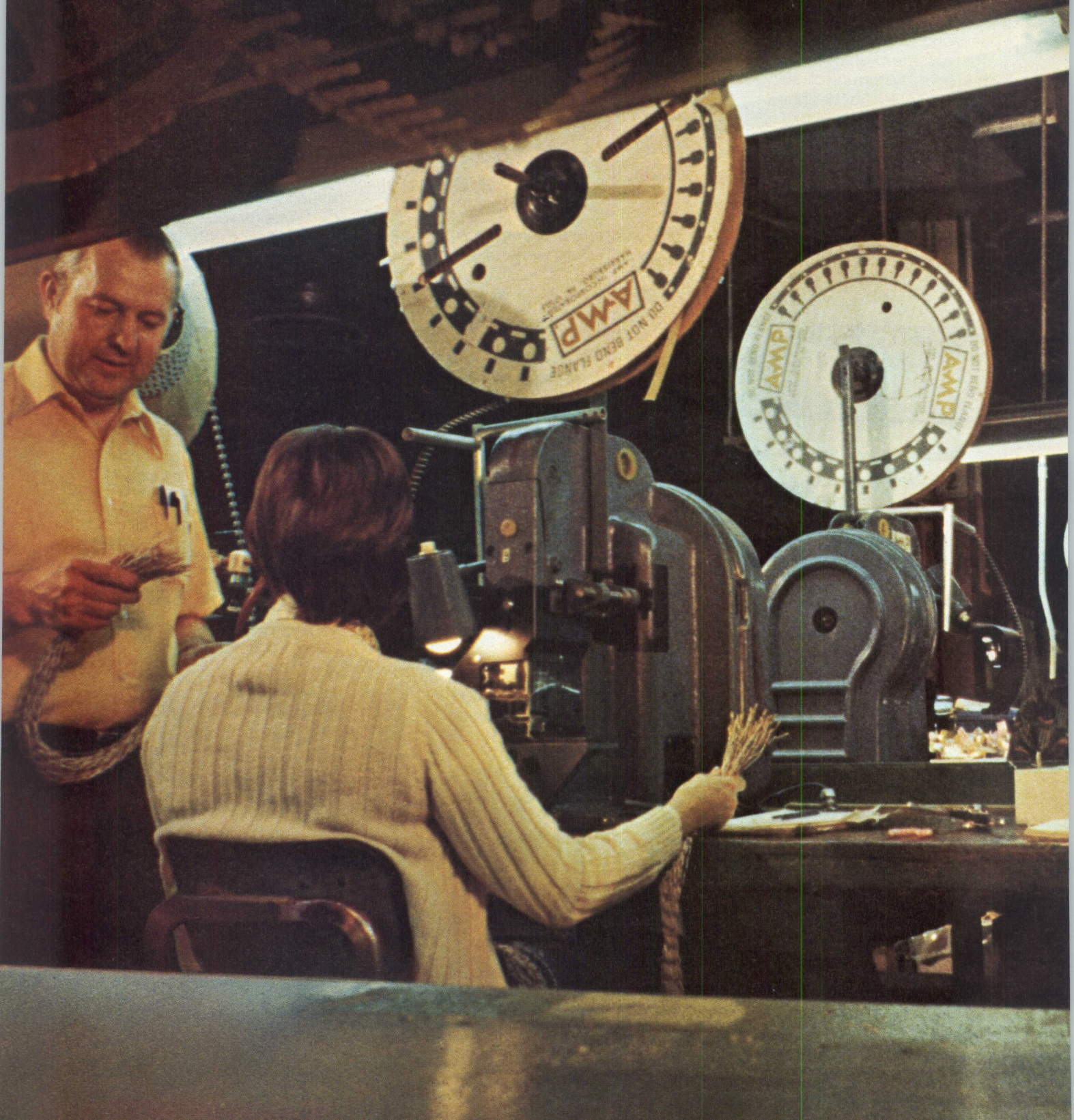
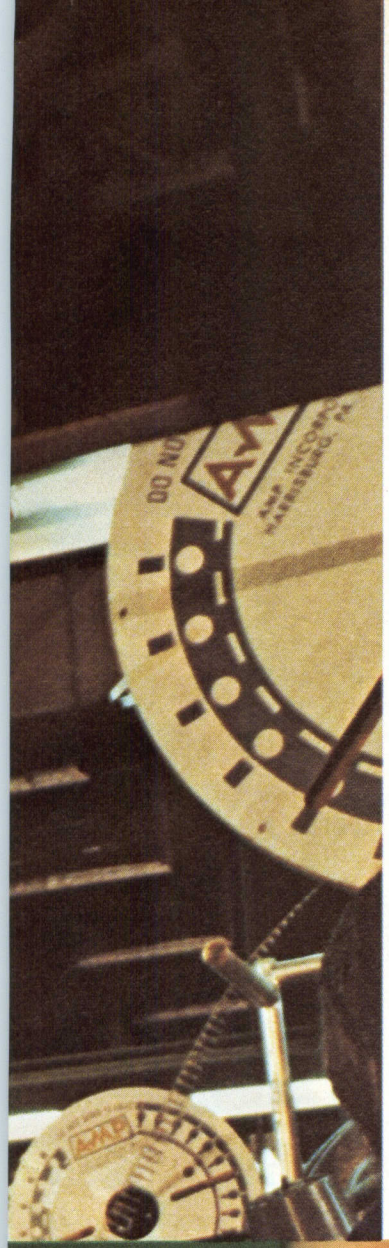
Series 5191 Quad Formatter

Must you always obtain new application tooling when you develop a new design?

Not always. You can use AMP Multimate.





You asked for a way to produce new I/O cable or internal harness designs without always having to obtain new connector application tooling.

AMP answers with the Multimate concept.

For example.

A choice of three, size 16 contacts. A screw machine contact, and 1 or 2-piece precision formed contacts. All interchangeable and intermateable plus AMP Subminiature Coaxial contacts fit in the same cavities when needed.

Then specify AMP Connector housings from many proven styles and sizes.

The rugged, economical Circular Plastic Connector, or those versatile M Series connectors widely used for commercial and military applications; or the AMP MI Connectors, designed to international standards. Additionally there is a cast shell rack and panel range as well as metal-shelled modular connectors.

If you have AMP application tooling for the Multimate contacts, you can produce these connector assemblies. And that can save inventory and allows for larger piece part volume purchases. Further savings can be made in the field because fewer service tools are needed.

Here at AMP, answering your problems is our business.

So when you work with Multimate, you can expect the kind of service and backup for which AMP is famous.

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With Multimate, you not only get real contact-connector flexibility, you have AMP behind your design innovations. For information on Multimate, write or call AMP Incorporated, Harrisburg, PA 17105. (717) 564-0100.

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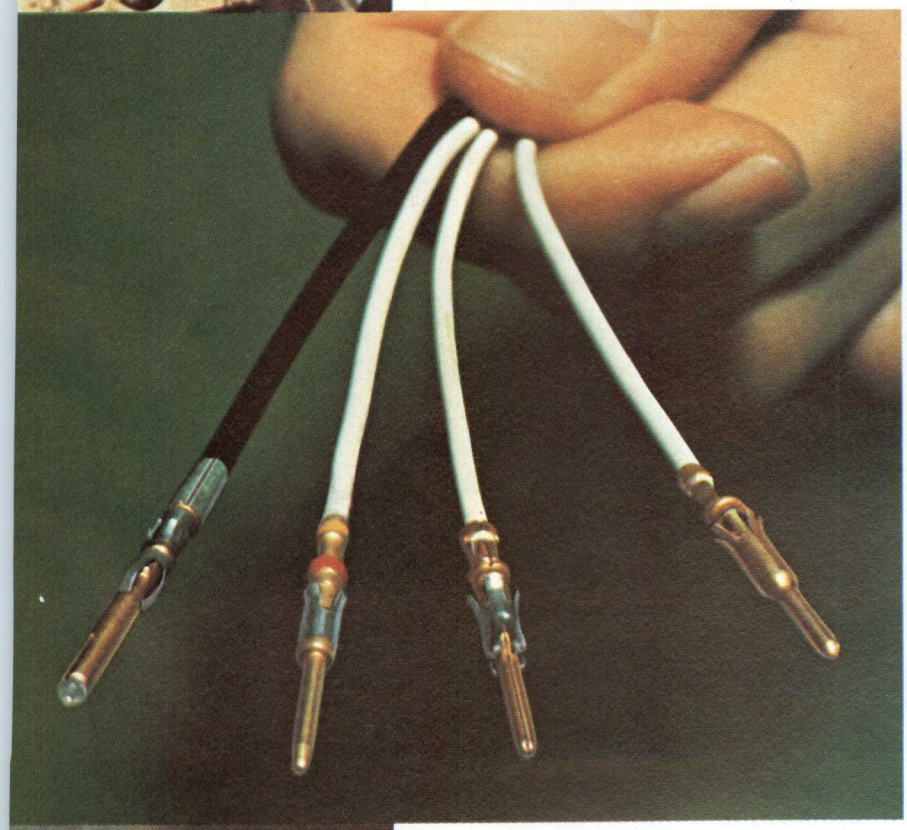
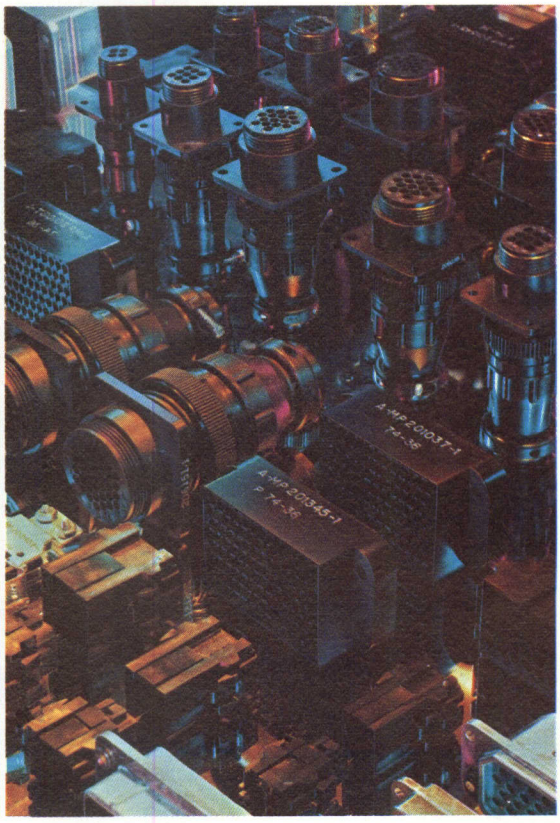
CIRCLE 31 ON INQUIRY CARD





Dual-Computer System Provides Continuous Control of Cement Plant

Control of cement manufacturing processes, unlike most other process control systems, does not require fast response times. Lags and time delays in the process can be as long as several minutes. Therefore direct digital control of the functions involved can be terminated and manual control substituted without hindering operation or product quality.

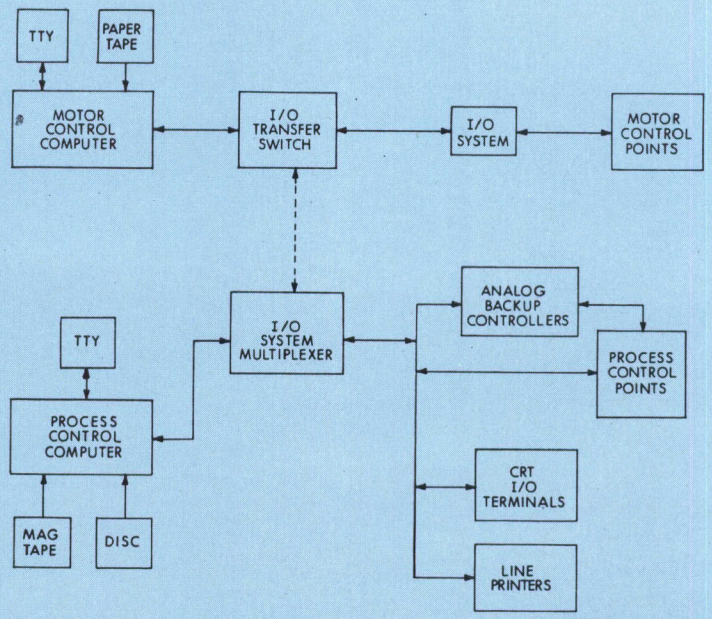
Plant motor control in the same facility, however, *is* critical to the overall operation. Response times must be rapid and failure of the computer in the motor control system could be costly. Therefore, this computer must be constantly backed up by a second computer that can immediately assume control if a serious failure occurs in the primary computer.

At the St. Constant, Quebec plant of Canada Cement Lafarge Ltd, after studies to compare capabilities of computers and programmable controllers, the requirements were reconciled by installation of a dual-computer control configuration. One computer controls the motor system, the other controls the process—but if the motor control computer fails, the process control computer assumes motor control duties. Control of manufacturing processes is then performed manually, with no loss in production.

Leeds and Northrup Co, Sumneytown Pike, North Wales, Penn developed and formed this dual control organization based on two identical LN5000 digital computers. The motor control computer regulates operation of approximately 560 motors and solenoids; the process control computer directs 58 loops by direct digital control (DDC). Video display terminals (4-color CRTs) portray symbolic diagrams and permit graphic changes to be made.

Control Hardware

Motor control and DDC process control are separate functions and, therefore, separate problems. However, they operate together, with the process control com-



Combined computer control system at manufacturing plant of Canada Cement Lafarge Ltd. Twin computers provide both motor system control and DDC process control. Motor control computer is constantly backed up by process control computer, which assumes motor control duties if first computer fails. Since processing steps are slow, the second computer has only manual backup in the event it fails or has to become motor controller

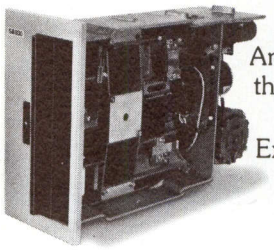
3 years, 12 patents, and 30,000 installations back every Shugart floppy disk.

No wonder two out of three OEM's specify Shugart floppy disks. They get more exclusive features, more product support, and more responsive delivery schedules. So can you.

A SA800/801 diskette storage drive gives your system more salable features: □ Single density, or double density for the same price. □ A patented diskette clamping/registration design that prevents diskette damage from misregistration over 30,000 interchanges. □ A proprietary ceramic read/write head that extends media life to over 3.5 million passes per track with a head life exceeding 15,000 hours. □ Extras like patented pop-out diskette retrieval, drive activity indicator light, and die cast cartridge guide and base plate.

If your system needs more data storage, you can easily convert from single to double density on the same drive. And you have a wide selection of product configurations—standard or compact "skinny" drive options, controller kits, and complete storage sub-systems.

Shugart gives you more daily support—systems design, technical service, documentation and applications help.



And Shugart is responsive. We will give you the delivery schedule you want, and we'll meet that schedule. Ask our customers.

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YOU MUST HAVE A CONTEST ENTRY KIT FOR FULL PARTICULARS. The kit must be ordered no later than August 9, 1976 . . . to get yours, circle No. 125 on the Inquiry Card in the back of this magazine right now!

WINNERS will be announced in the January 1977 issue of COMPUTER DESIGN.

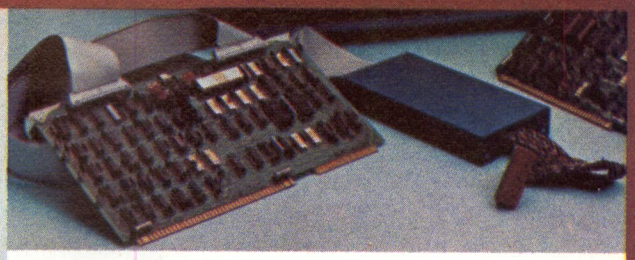
CONTEST RULES

1. Contest closes SEPTEMBER 30, 1976. All entries must be postmarked no later than midnight of that date.
2. All entries must be submitted on official forms contained in the CONTEST ENTRY KIT.
3. MICROPROCESSOR/MICROCOMPUTER APPLICATION IDEAS must be free of restrictions on their use. They may not contain any proprietary, confidential, or patentable information.
4. Ideas submitted must be original with the entrant(s) and must not have been previously published.
5. All materials included with, or as part of, the entry become the property of COMPUTER DESIGN Magazine and will not be
6. Exclusive publishing rights will be held by COMPUTER DESIGN Magazine.
7. The contest is open to everyone except contest judges; their relatives or business associates; or employees, relatives, or agents of Computer Design Publishing Corp. and Intel Corp. or its subsidiaries.
8. Contest is void in locations where prohibited by law.
9. Decisions of the judges will be final.

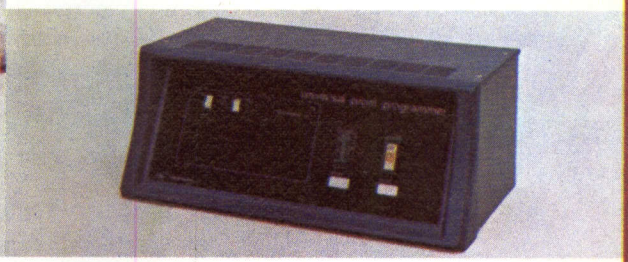
Circle No. 125 on Inquiry Card to receive your official

FIRST PRIZE (Valued at $6,150.)

An IN-CIRCUIT MICROCOMPUTER DESIGN CENTER!



Intellec MDS-ICE-80 IN-CIRCUIT EMULATOR MODULE that interfaces to any user configured 8080 system and allows the designer to emulate the user 8080 in real-time, single step the user system's 8080, substitute Intellec MDS memory and I/O for user system equivalents, and extend powerful debug functions into the user system.



Intellec® MDS-800 MICROCOMPUTER DEVELOPMENT SYSTEM is a modular system containing all necessary hardware and software to develop and implement an intel® MCS 80™ Microcomputer System.

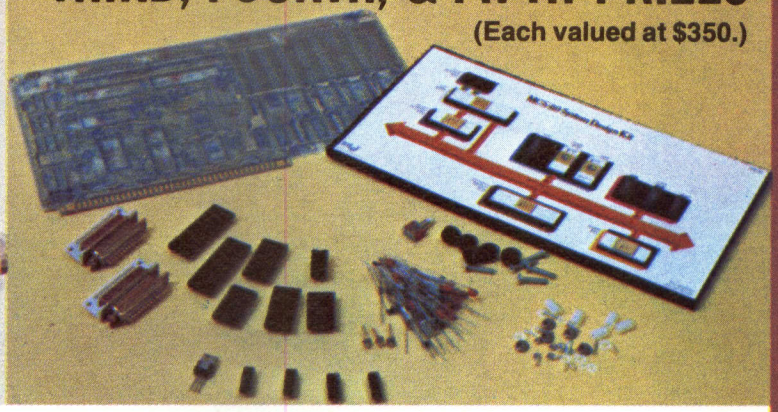
Intellec MDS UPP 101 UNIVERSAL PROM PROGRAMMER which allows you to program and verify all intel p/ROMs by initiating p/ROM programming commands from your system console.

MICROPROCESSOR / MICROCOMPUTER
. . APPLICATIONS CONTEST

SECOND PRIZE (Valued at $3,950.)

THIRD, FOURTH, & FIFTH PRIZES

(Each valued at $350.)



Intellec MDS-800 MICROCOMPUTER DEVELOPMENT SYSTEM as described above. In this advanced development system you will receive an 8080 CPU, 16K bytes of RAM, 2K bytes of ROM, power supplies, front panel, and system software.

intel 8080 SYSTEM DESIGN KIT (SDK-80)
The SDK-80 is a complete 8080 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful functional system.

JUDGES

Edwin E. Klingman, President, Applied Cybernetics

Dr. A. J. Nichols, Mgr., Microcomputer Applications, Intel Corp.

Jerry L. Ogdin, President, Microcomputer Technique, Inc.

Dr. Hoo-Min-Toong, Systems Professor, Dept. of EE & Computer Science, M.I.T.

John A. Camuso, Editor, COMPUTER DESIGN Magazine

COMPUTER DESIGN

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puter constantly ready to replace a malfunctioning motor control computer.

Motor control operations include interlocking, sequencing, gate positioning, and time delay functions. The computer's 40K words of core memory are adequate not only for the present but for planned future expansion of control levels. Programs are loaded through a high speed paper tape reader, and a teletypewriter permits the programmer to enter changes. Changes in motor control status are entered through a manual input console directly to the motor control computer. However, a data bus connection permits concurrent update of these changes in the memory of the process control computer. If the process control computer is called on at any time to assume motor control duties, its memory is fully updated.

Motor control will continue to be handled by the process control computer as long as necessary, with duties of the DDC computer conducted manually by an operator. When the malfunction in the motor control computer has been corrected, the entire dual system returns to normal operation.

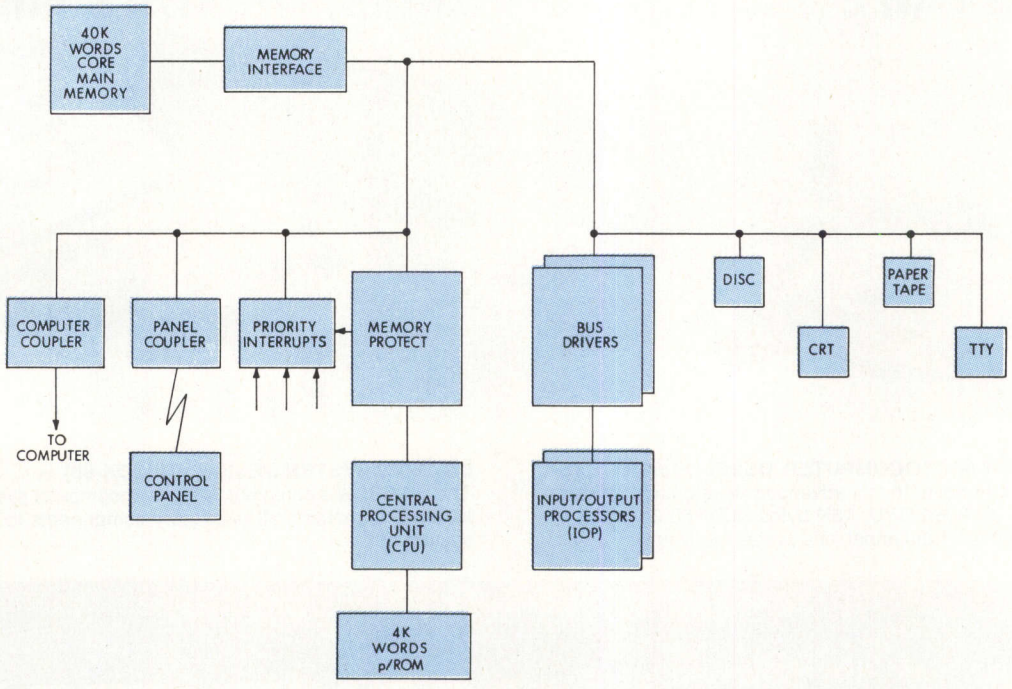
This switch of duties occurs only in the event of a serious malfunction within the circuitry of the motor control computer. Failure of only a single input merely causes display of the fault on one of the CRTs; there would be no switchover of computer duties.

Each control loop has either a manual or supervisory controller for backup, permitting an operator to bypass the computers for direct access to the control point. Backup stations contain pushbuttons for control input, a meter for viewing the action that is being ordered, and a set of lights to indicate control mode: manual, computer, or alarm. Most of the backup stations at the cement plant are of the manual type.

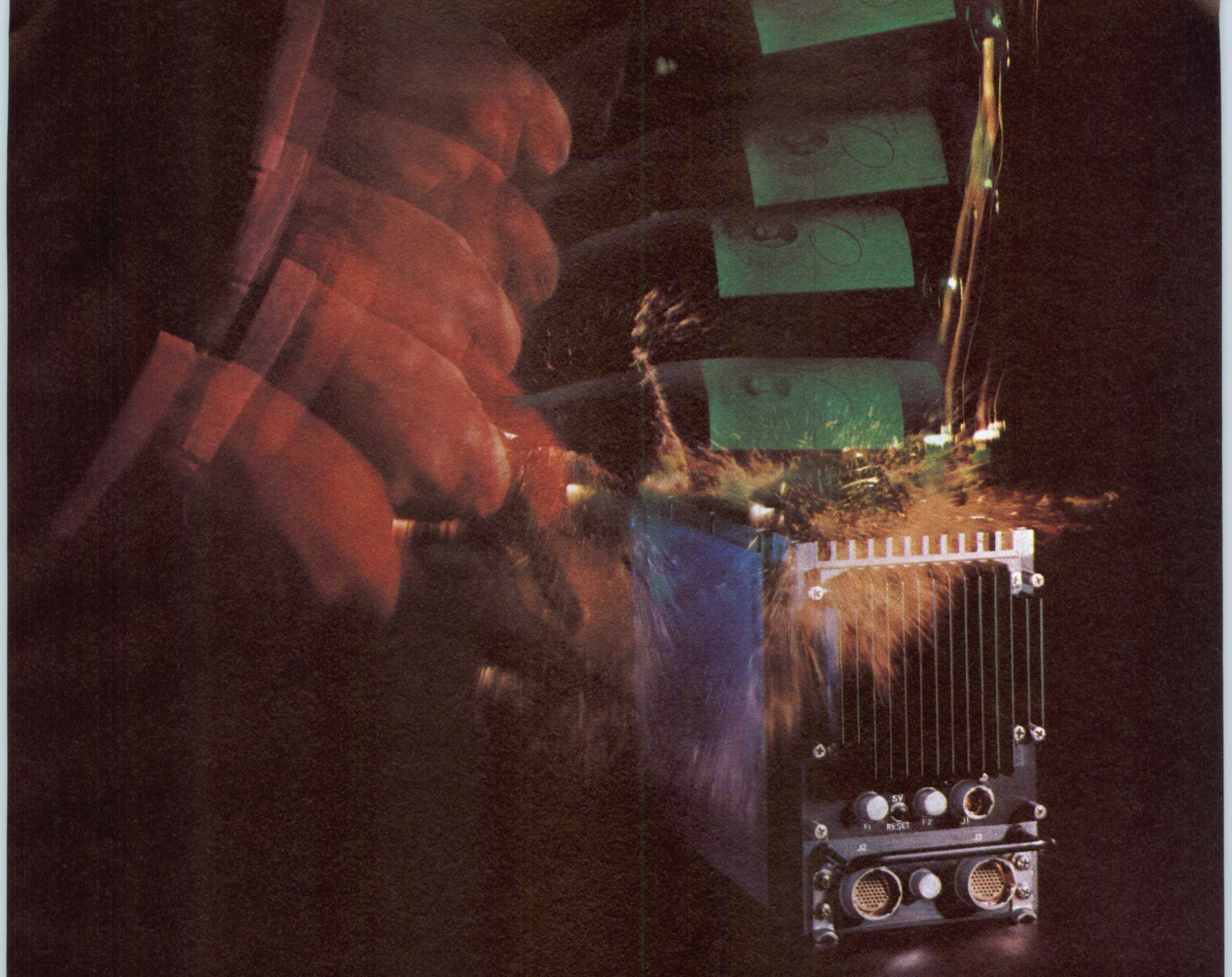
Mark II 4-color CRT terminals permit the operator to communicate with the computers and to order changes in setpoints or variables such as material composition or level, flow, pressure, and temperature. Symbolic diagrams can be called up on the displays for study, and changes can be made via keyboard, joystick, or lightpen. Digital values of setpoints may be superimposed on the analog presentations to aid in the interpretation.

Rather than turning dials or pressing pushbuttons as would be the case in an analog system, the operator of this cement plant makes adjustments through the CRT display on the console. Touch of a lightpen to the CRT screen will call up graphic, trend, systems function, or loop displays. The plant section display acts as plant communicator and alerts the operator to changes in status throughout the plant. Operator can then request step down to a lower branch to locate the problem. Loop modules are the lowest levels attainable. They display the control diagram language modules in each loop as well as rate, reset, alarm limit, and other parameters.

Separate 40K-word main memories for the two computers are organized in five units, each containing 8K



Block diagram of single unit of LN5000 twin computer system. Main memory in each unit is made up of 40K words in 18-bit format (2 bits are parity). CPU is controlling element for most system functions; IOP operates concurrently to supervise peripheral controller when transferring data



Rolm launches its most compact computer

The 1650: rugged, lightweight, ½ ATR size

The 1650 (AN/UYK-34) smashes the size barrier . . . especially in critical applications that have to meet Mil-E-5400 and Mil-E-16400 Environmental Specs.

It's about one-third the physical size of the Rolm 1602, yet has equivalent computing power through the use of the latest bipolar LSI technology. A microprogrammed 1650 CPU with an instruction set identical to the 1602 is packaged as a single folded-board module. The ½ ATR chassis also holds two 16K core memory modules (1 μsec cycle time) and a +28 Vdc power supply. Total weight — less than 30 pounds.

You can choose from a variety of cooling configurations including natural convection, external forced air or a Rolm-supplied blower. Single-sided access makes maintenance and service easy. Cap it off with optional floating point firmware, extensive I/O capabilities and complete software support . . . and you've got a compact computer system that can't be beat. Call (408) 257-6440, TWX 910-338-0247 or write ROLM Corp., 18922 Forge Drive, Cupertino, CA 95014. In Europe: 06181 15011, TWX 841-418-4170, 645 Hanau, Muehlstrasse 19, Germany.

ROLM CORPORATION

The Rugged Computer Company

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MOSTEK'S MK 4027-2. HIGH PERFORMANCE STARTS WITH ACCESS TIME.

150ns

With MOSTEK's new 4K RAM your system performance can match data sheet specs.

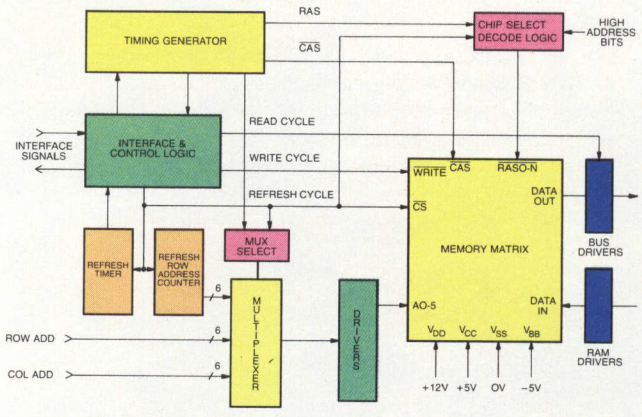
At 150 ns access time (worst case), the MK 4027-2 is the fastest 16-pin 4K RAM in the industry. It appears even faster when compared to 18 or 22-pin 4Ks that require high-level clocks and differential outputs. In this comparison, our 150ns is actually better than their 120ns.

But fast MOS memory can't be used efficiently unless you can surround it with high performance logic. You can with the MK 4027 because it's completely Schottky-TTL compatible with a max V_{IL} spec of .8 volts. And a wide ±10% tolerance on all power supplies is a standard feature from MOSTEK.

Gated $\overline{CAS}$, another new MK 4027 feature, provides an expanded timing window to compensate for timing skews encountered in the multiplexing operation. This window is a full 25% of overall access time.

The MK 4027 can further upgrade system performance with an improved output drive capability. It sources 5mA and sinks 3.2 mA while driving a 100 pF load. Other 4Ks drive only one TTL load and 50 pF.

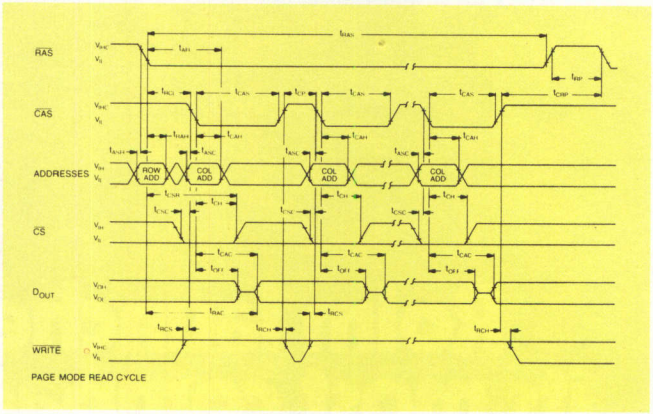
By employing essentially all dynamic internal circuitry, the MK 4027 dissipates very little DC power. This allows the device to remain much cooler in operation than competitive products and is one reason for its outstanding reliability.



TYPICAL HIGH PERFORMANCE MEMORY SYSTEM

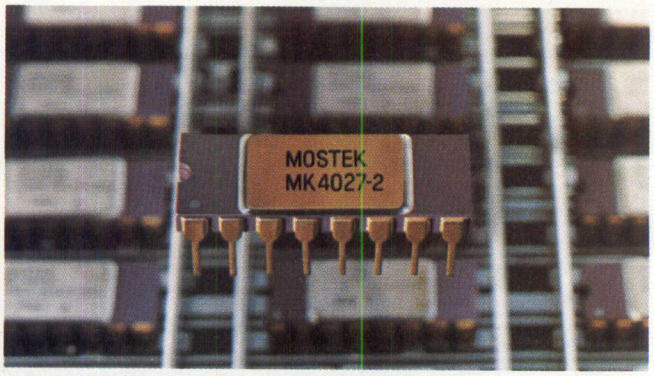
A new operating mode improves access time to 100ns.

It's called "page mode," an addition to the normal cycles of read, write, read-write, and read-modify-write. In a nutshell, page mode allows for successive memory operations at multiple column locations at the same row address with increased speed — 100ns — and decreased power.



PAGE MODE READ CYCLE

Page mode is not limited to any single chip. Since the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of "page" cycles, the page boundary can be extended to multiple 4K memory blocks.

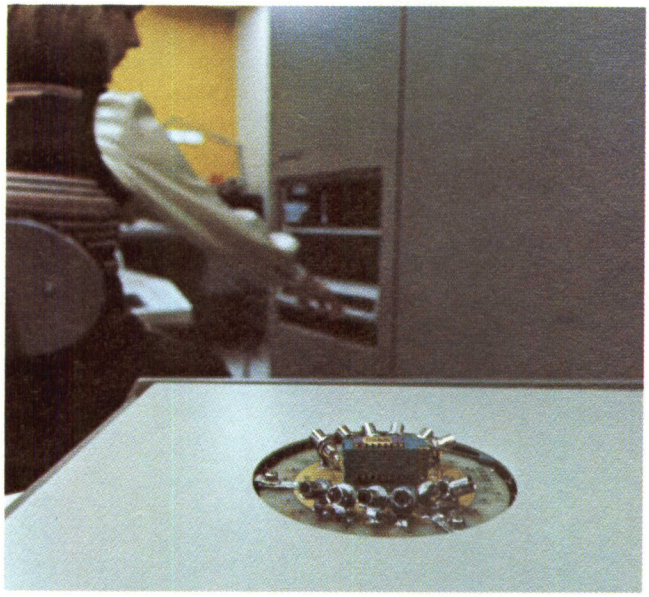


MOSTEK's 16-pin package reduces memory board size 50% over 22-pin packages.

How about density — yours and ours?

As you might expect the MK 4027 is in the industry standard 16-pin package allowing the greatest possible density for your high performance memory system.

We've been working on our own density, too. At 104 mils x 140 mils the MK 4027-2 is the smallest 4K RAM in the industry.



Reliability? MOSTEK sets the standard.

The fastest, the smallest, the most versatile is not automatically the best. Not without MOSTEK quality. Every 4K RAM MOSTEK ships is subjected to these screens and stresses: pre-burn at high temperature, temperature cycling, centrifuge, dynamic burn-in at 125° C, and final test with wide guardbands.

High Performance 4K RAMs . . . Here's your choice.

	16-pin MK 4027-2	18-pin TI 4050-2	22-pin 2107B
FEATURES			
Access Time	150ns	200ns	200ns
Cycle Time	320ns	400ns	400ns
Read/Modify/Write	350ns	600ns	520ns
Worst Case Power Dissipation	462mw	478mw	680mw
V_{IL} (all inputs)	0.8v	0.6v	0.6v
V_{IH} (data, address)	2.2v	2.2v	2.4v
V_{IHC} (clocks)	2.4v	12.0v	12.0v
Clock Cap.	7pF (max)	33pF (max)	25pF
Power Supply Tol.	±10%	±5%	±5%
Page Mode	YES	NO	NO

MOSTEK's 16K RAM is coming soon.

In addition to an unlatched output, MOSTEK's 16K RAM will include all the features found in our high performance 4K. This means Schottky-TTL compatibility, ±10% tolerance on power supplies, page-mode, gated $\overline{CAS}$ and low power. Designing and testing with MOSTEK's MK 4027's in your production systems now is a logical "first step" toward an efficient 16K system.

Want more information? There's an application note and data sheet package that tells the complete MK 4027 story. Write on your letterhead to MS 402 for quick response. Or pick up the literature package and a sample at your local MOSTEK distributor.

MOSTEK

1215 West Crosby Road, Carrollton, Texas 75006
(214) 242-0444
In Europe, Contact:
MOSTEK Gmbh, TALSTR, 172, 7024 Filderstadt-1,
West Germany
Telephone: (0711) 701096

CIRCLE 35 ON INQUIRY CARD

18-bit words (16 instruction bits and two parity). Each memory unit feeds into the system via a memory interface unit.

Controlling element for most system functions is the central processing unit (CPU). It executes instructions, controls the direct I/O system including interrupts and control panel, and activates the input/output processor (IOP). The latter processor operates concurrently with the CPU to supervise peripheral controllers when transferring data into or out of main memory.

In a system of this type, process I/O equipment serves as interface between computer and process; ie, it directs analog and digital variables read by the computer or sent by the computer to points in the process. Analog input parameters include pressures, flows, temperatures, levels, analysis measurements, and valve positions. Digital inputs are supplied from on-off or pulse-type devices; digital outputs operate annunciators, relays, printers, and, through DDC interface circuitry, process control end-elements.

Four types of digital signals—status, counter, events, and priority interrupt—are input to the system. These signals are applied to digital input cards via signal conditioning and isolation circuits appropriate to the type of input signal, process noise, and electrical transients present or expected. Input density per card ranges from one input for a 16-bit counter card to 32 inputs for a status type card.

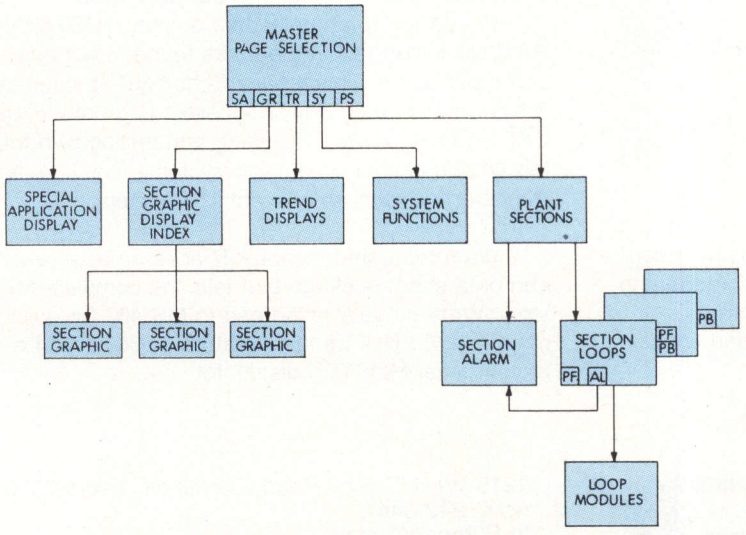
The computer can output up to 256 16-bit words to two basic types of output cards that provide either output levels or pulses. These outputs are used to drive relays or solid-state switches used for operating such devices as solenoid switches, circuit breakers, stepping motors, latching relays, signal lamps, and alarms.

Control Software

All programs for the LN5000 system at this cement manufacturing plant operate under and are scheduled by a system executive program. Immediate tasks—those involving real-time process monitoring and control—are handled as foreground functions, while less critical items are background program functions. Foreground functions include data acquisition programs, process oriented system applications programs, and motor control and man/machine interface programs. New program development, testing and integration of potential programs, special CRT display generation, and data base updates are treated as background functions and are performed in free time without interference to the foreground or real-time system.

A COntrol DIagram Language (CODIL), specifically designed for use by a process engineer rather than a programmer, handles LN5000 control functions. This language is made up of a series of modules or functional blocks which represent functions such as multiply, divide, control, gate, and interlock. These functions can be interconnected in diagrammable fashion to execute a chosen control strategy. A completed CODIL diagram graphically documents the control scheme for the computer. Functional blocks symbolize control operations and are designed to be similar to those used in an instrumentation diagram.

The manner in which the diagram is drawn defines the way the program should be structured. Interconnections of diagrammable symbols define control functions to be performed, and the logical order of symbols on the diagram is the order in which they are to be executed by the operation system. This diagram, however, describes only what control functions will be performed; it does not describe how to perform them.



Hierarchical structure of display system. Master page selection branches off into subsections which in turn may branch off into lower display levels. Loop modules are lowest level available

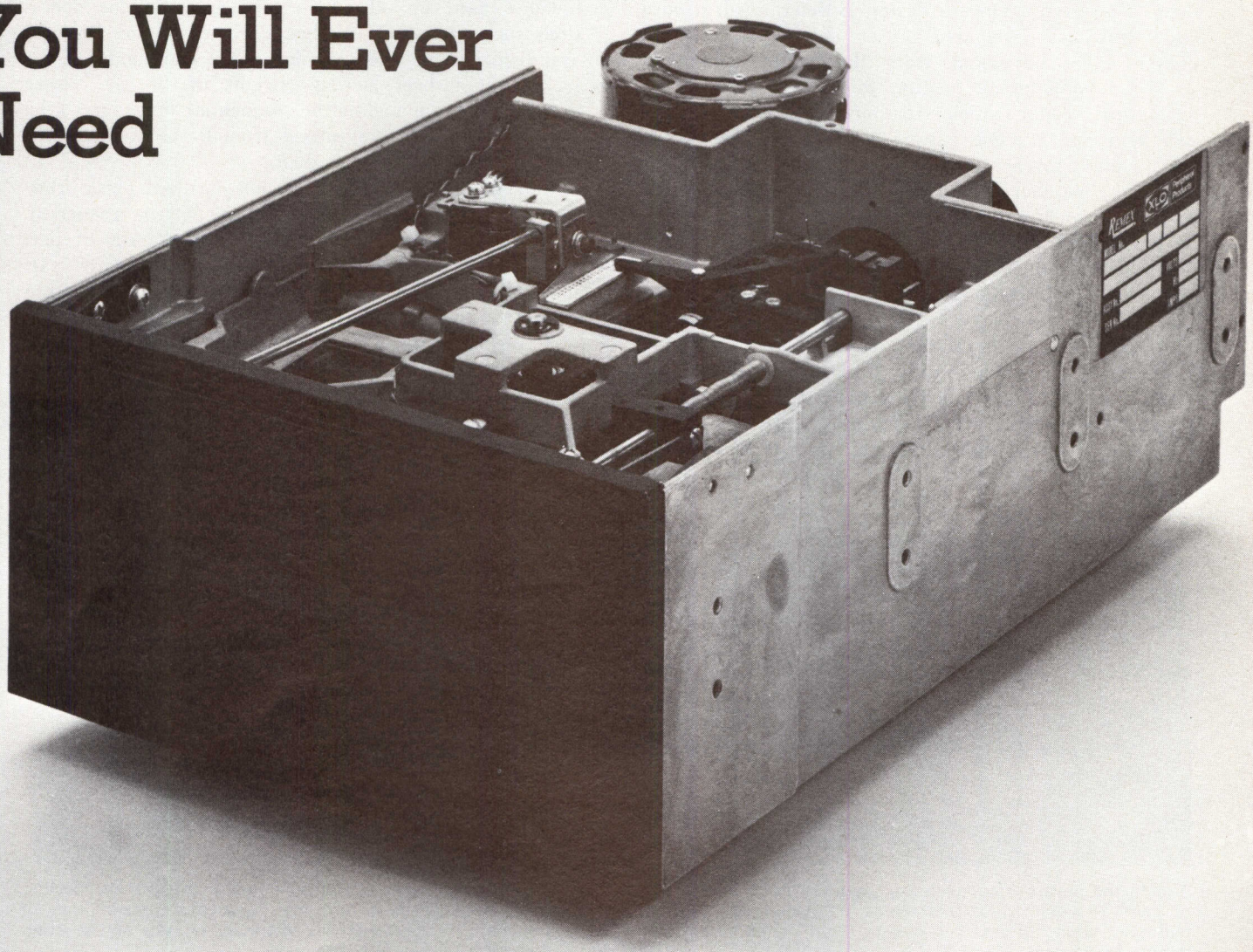
Circle 160 on Inquiry Card

The REMEX RFD 1000—Because It's Versatile. Double or single density with capacity up to 6.4 Mbits...IBM standard or 32 hole hard sectored media without drive modification...IBM compatible or expanded hard and soft sectored formats for application flexibility...Unit select daisy chain capability for maximum controller efficiency...Selectable DC negative voltage for system compatibility...Individual drive housing or two drives horizontally side by side in a 19 inch rack configuration.

The REMEX RFD 1000—Because It's Reliable. Ceramic head for extended life...Precision machined, die-cast construction...Operator interlock and expandable clutch for media protection...Front panel "head in contact" indicator and optional "head in contact" door lock...Optical write protect to assure data security...Stylus ball lead screw positioning system for long-lived accuracy...Optical track 00 sensing for drive carriage protection.

The Remex RFD 1000 is the RIGHT peripheral from Remex.

This Is The Only Flexible Disk Drive You Will Ever Need



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CIRCLE 36 ON INQUIRY CARD

Computerized Graphic Display System Aids in Automatic Design of Tractor Parts

An automated design/production facility now in use at International Harvester's Engineering Center for Agricultural Equipment not only saves stock but also drastically reduces the man-hours required to design tubing. Whereas before the system was installed only one part could be produced from a single stock plate, many parts can now be nested, increasing stock utilization by 20%. In addition, the 50 man-hours of drawing board time previously required to design hydraulic tubing has now been reduced so drastically that one designer can perform the steps in one hour.

A computerized graphic display system made by Sanders Associates, Inc, Nashua, NH is a key portion of the overall facility. This system enables the designer to either create new designs on a 21″ CRT display or retrieve and display any of 10,000 drawings—and alter them if necessary. Once a design is determined, a hard copy drawing is prepared on an automated precision plotter under command from the central computer. At the manufacturing facility, this print is traced by an optical reader which simultaneously produces signals to order a flame cutting machine to move from two to eight torches to cut the required parts.

A large number of the same item can be displayed and moved or flipped about—or different order parts can be mixed on the screen for maximum utilization of a plate. This both cuts waste of portions of the steel plate and optimizes cutting time. Numerical control tapes of the drawings can be made for use by other company divisions for automated parts production.

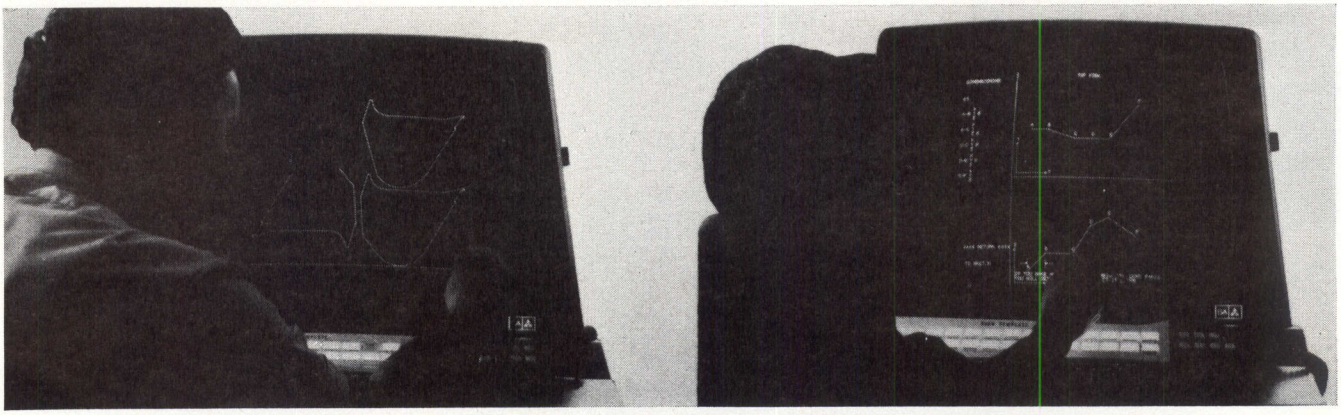
When designing hydraulic tubing, a mathematical representation of the tube is displayed on the console screen. The designer can perform calculations involving stretch, spring back, length, and type of tube, and each will be depicted on the screen. From this information a number of drawings are generated including a full scale shop template which is used to fabricate a prototype tube part. The system enables engineers to change scales merely by touching a light pen to the screen. Drawings can be produced in either English or metric scale. Vendor and tooling information is automatically generated.

In addition, structural analysis on tractor and loader chassis can be performed by displaying a 3-dimensional image on the screen for analysis. As the computer simulates increased loads on the protective frames and chassis, the system depicts the deformation of each element. Designers can continue increasing the load until an actual break occurs. By touching the light pen to sections of the displayed image, users can select individual chassis sections to be enlarged on the screen for independent study.

The graphic display system is also used for a steering geometry program which analyzes four types of linkages used on off-road equipment built for operations such as copper mining. Various steering linkages are displayed on the console screen and analyzed for jackknifing, wheel locking, height of tie rod above ground, king pin inclination, sequential turns, and king pin offset. Wheels are turned from 0- to 50-deg turns in 5-deg increments and studied.

Currently, approximately 10,000 digitized parts drawings are stored on discs. When a part is requested, a catalog appears on the screen in the form of part numbers. By touching the light pen to the desired part number, users can call up and display the part within seconds.

A displayed drawing can be altered if necessary, or sent directly to the computer for printout on the plotter. In most cases, a number of different parts making up one order or a number of different orders are nested for efficient flame cutting.



Among the several capabilities of Sanders Associates' graphic display system as used by International Harvester are nesting of parts to obtain maximum usage of steel stock from which the parts are cut (left) and mathematical representation of hydraulic tubing to assist in design (right). Other uses include 3-dimensional structural analysis of tractor chassis and steering geometry studies

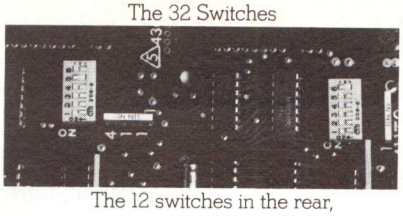
Circle 161 on Inquiry Card

All the people who bought our DUMB TERMINAL (the ADM-3) because of its low $995* unit price didn't really expect a lot. But they hadn't counted on the 32 switches. Switches that let you turn the DUMB TERMINAL into a pretty clever animal.

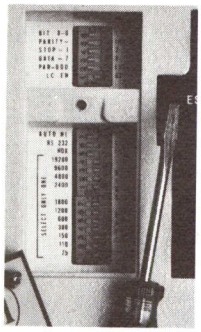
Take the 20 switches under the LSI name plate, for example. Among them, 11 communication rate positive action switches that let you select bauds from 19200 to 75. Also an RS232 interface extension port switch. It allows you to connect the DUMB TERMINAL to all kinds of clever devices — to recorders, printers and smarter terminals. And switches for odd-even parity. Optional upper and lower case (the complete set of 128 USASCII characters) — plus a lot more.

Inside on the PC board, 12 more switches. More positive action types that instruct the DUMB TERMINAL how to behave. And for all those who bought the 24-line optional display, there's a switch to change over from the standard 12-line format. So instead of showing 960 standard characters in 12 rows, you have the option of displaying 1920 characters in 24 rows of 80 letters. And there are still more switches that make your terminal a cinch to operate.

The 32 Switches



The 12 switches in the rear, on the PC board.



The 20 switches under the front name plate.

Now people aren't sure what turns them on: the low price, the 32 switches, or the DUMB TERMINAL's standard features. Features like a full 12" diagonal screen. 59 data entry keys, arranged like on a typewriter. Compatibility with all popular computers. Simple, quiet operation. An optional numeric key pad. And fast data throughput. All features that make this terminal a perfect video replacement for the old teletypewriter.

The fact is, people keep finding more and more jobs for our DUMB TERMINAL. Because they can do anything within reason — with just a little switching and training. And that's why the DUMB TERMINAL really turns out to be a smart buy. Which may be the biggest switch of them all.

For full information, write: Lear Siegler, Inc., E. I. D./ Data Products, 714 N. Brookhurst St., Anaheim, CA 92803; Tel. (714) 774-1010.

DUMB TERMINAL. SMART BUY.

*U.S. domestic price

THE $995 DUMB TERMINAL CAN BE TRAINED TO DO PRACTICALLY ANYTHING.

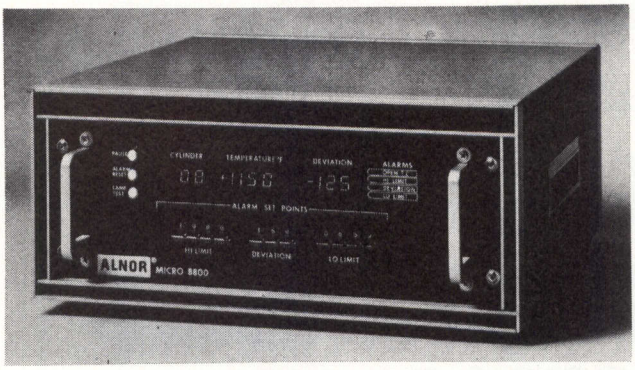
Microprocessor-Controlled Instrument Monitors Exhaust Gas Temperatures

Cylinder exhaust temperatures in large diesel engines typically vary with engine speeds, loading, and other normal conditions. By comparing the exhaust temperature of individual cylinders with the average of all cylinders and with preset high and low limits, abnormal functioning can be located in time to make adjustments before serious damage occurs.

Designed primarily for monitoring diesel engine cylinder exhaust gas temperature (EGT) in marine applications and for industrial use with compressor, pumping, or power generating diesels, the Micro-8800 combines all functions under control of a microprocessor. It continually scans up to 32 engine cylinders at a rate of 1 zone/s. A 0.43″ high red LED display shows the number of each cylinder as it is scanned, the actual temperature of that cylinder (°F), and the number of degrees by which this temperature deviates from the average cylinder temperature.

If the temperature of a cylinder approaches 10% of preset high or low limits, an indicator flashes on the display panel; if the temperature of a cylinder exceeds preset high/low limits, or goes beyond the preset maximum allowable deviation-from-average, a panel indicator lights and an external alarm output is activated. A separate panel indicator and alarm output are activated if a thermocouple breaks or becomes disconnected.

Two 4- and one 3-digit thumbwheel switches are used to fix high and low alarm and deviation-from-average alarm setpoints, respectively. A "pause" pushbutton inhibits the scan advance to permit temperature fluctuations of one cylinder to be observed. An "alarm reset" pushbutton clears any alarm condition to resume normal operation, and a "lamp test" pushbutton checks the LED display segments by forcing all digits to 8.



Setpoints entered via thumbwheel switches determine high and low limits and acceptable deviation-from-average in microprocessor-controlled system for monitoring exhaust gas temperatures of individual cylinders in diesel engine. LED readouts identify each cylinder as it is scanned, its temperature, and its deviation. External alarms can also be added

The system also can be used to balance cylinder performance for maximum power output with minimum fuel consumption. This is done by setting deviation-from-average alarm setpoints at around 25° F, and making fine adjustments in fuel flow until all individual cylinder deviations stay within that preset limit. With optional modification, the 32-channel capacity can be split to permit the same instrument to monitor two engines of up to 16 cylinders each.

In cases where the total 32-channel capacity is more than required, the additional channels can be used to monitor water or oil, inlet-at-turbine, or engine bearing temperature, or any other thermocouple checkpoint using the same TC alloy as in the EGT thermocouples. An optional printer can be added to log EGT upon command or once every 10, 20, or 60 min., and an optional remote display unit allows monitoring at a separate station. A variety of optional BCD outputs accommodates interface with computerized systems.

System circuitry is on four PC boards mounted on a motherboard to minimize internal wiring. Only the power supply connections and I/O terminal connections are hardwired. Boards include a digitizer that converts analog thermocouple inputs into digital form, an FET thermocouple scanner, a controls-and-display board, and a microprocessor set built around an Intel CPU.

Four separate alarm outputs, each capable of up to 240 Vac at 0.75 A, permit the addition of individual external alarms for high limit, low limit, and deviation-from-average, plus a master alarm that is activated when any of the other alarms are triggered. All input and output connections are opto-isolated to help minimize the effects of common mode noise.

Noise rejection is >90 dB in the normal mode and 170 dB with 100-Ω unbalance in the common mode. Special double-loop front-end design has less drift than conventional closed-loop systems. A 32-segment digital linearizing circuit provides highly stable, unblinking readout displays, accurate to within ±0.25° F or C in conformity with NBS specifications.

Operation is rated for ambient temperatures from 40 to 120° F (4 to 49° C) with storage temperatures of −20 to 130° F (−29 to 54° C) at 0 to 95% RH. Vibration and shock tolerance complies with MIL-STD-167. Input power requirement is 115 or 230 Vac rms ±10%, at 49 to 36 Hz. The unit draws no more than 25 VA in normal operation.

Three package formats available from Alnor Instrument Co, Niles, Ill include a desk-type enclosure that can be installed in a standard 19″ rack or panel using an optional mounting kit, a dust- and oil-tight NEMA-12 housing, and an explosion-proof housing. The standard rack and panel model measures 7 x 17 x 15″ (18 x 43 x 38 cm) and weighs 24 lb (11 kg).

Circle 162 on Inquiry Card

DC&AS BRIEFS

Computer-Based Gas Chromatograph System Reduces Lab Analysis Costs

A computer-based process chromatograph data acquisition and control system being implemented by Dow Corning Corp at its Carrollton, Ky plant will handle up to 32 gas chromatographs with as many as 64 streams. ProPace™ 1000, manufactured by Electronic Associates, Inc, West Long Branch, NJ, is based on a Pacer™ 100 digital computer and an all solid-state data acquisition front-end. Chromatograph detector output signals are automatically processed to calculate and report stream compositions based on linear-with-concentration peak areas. Component response factors are applied to each peak area, and results normalized to compensate for any variance in sample volume or detector sensitivity. Analysis reports, containing stream names, time, date, component names, and concentrations are typed out after each analysis on teletypewriters.

Through a status and control panel, the system handles all time-coded control functions for chromatograph analyzers interfaced with the system, and processes all data reduction, compositional calculations, and reporting of results. All stream switching, sample injection, and other functions previously handled by a programmer/control module are handled by this system. Need for timer, logic switching, attenuator circuits, and strip chart recorders used to present composition data in bar-graph form is eliminated.

Compositional data from the instruments are claimed to be as accurate as that from laboratory-derived analyses, with the added advantage of being online for immediate display to process operators. Program and hardware diagnostics routinely check chromatograph performance as well as the integrity of the concentration calculations, with periodic checks and updates, if necessary, of the computational parameters. Laboratory analysis costs as well as maintenance and calibration expenses are reportedly reduced significantly. In addition, the system increases analysis speed, accuracy, and flexibility.

Optical Comparator Functions As Computer-Controlled Inspection System

A self-contained, computer-controlled inspection system developed by EMR Photoelectric, Princeton, NJ is claimed to permit nearly any machined, molded, or stamped part requiring inspection of linear or diametrical dimensions to be accurately measured. The company says that parts inspection for both long-term, single-piece manufacturing operations or short-run, multiple-part production can be accomplished by its Comp-Gage electronic optical comparator. The system utilizes an electronic camera and a computer to measure, analyze, and record the dimensions of a given part during inspection procedures.

A complete industrial inspection system that converts optical dimensional data into digital language for computer analysis, the comparator is designed to improve the efficiency and accuracy of routine industrial inspections. It can be operated completely automatically, inline, and by inexperienced plant or laboratory personnel who have no prior quality control or computer programming experience. During quality control inspection procedures, the comparator can automatically calculate the dimensions of a product to 1 part in 2000 in <1 s and either display them on a large screen for operator communication or store the information within the computer.

All functional components are incorporated into a desk-type console with the camera head and inspection table separately mounted on a single adjacent pedestal for remote stationing. Systems expansion is possible for additional equipment such as telephone and teleprinter communications, mass storage of product information, and line printers for labels, tags, or permanent records.

Preprogrammed System Complements Total Distributed Control Architecture

A process monitor and control (PM/C) system, a preprogrammed system for medium-to-large industrial process applications which supports and complements the company's total distributed control (TDC) architecture, is being offered by Honeywell Process Control Div, Phoenix, Ariz. The system provides computing power, supervisory and direct digital control, historical data collection, and additional display and online program development capabilities. It supports any combination of HS4450 analog I/O subsystem, HS7024 telecontrol system, and TDC 2000 process interface equipment.

When used as a component for the TDC 2000 process control system (see *Computer Design*, Jan 1976, pp 44-48), it combines central processing advantages with the security of distributed control. In addition, it can be used as a centralized, dedicated computer-based system (with the HS4400 process computer as the central processing unit), without the use of TDC 2000 controllers. Used alone, PM/C interfaces with the process through local, remote, or telemetry I/O hardware; variable output controller; VutroniK miniature electronic equipment; or other control stations.

The system is programmed to provide process measurement, signal conditioning, limit checking, alarming, video display, hardcopy log, historical data collection, direct digital, and regulatory control functions. It has video-based, human-engineered operator interfaces and online program development and testing facilities as well as optimization aids.

Displays are constructed or modified by the operator as needed for optimum reporting of events. Through CRT operation stations, the operator has access to all process variables and control loop parameters, including those in the distributed controllers connected to the computer by the use of single or redundant coax-cable data highways. □

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because it costs less!

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CIRCLE 38 ON INQUIRY CARD

A semiconductor memory, after it has been installed in a computer, is subject to testing in addition to its manufacturer's tests. This testing must encompass architecture and accessing mechanisms yet is limited because the memory must store its own test program

How Computers Can Test Their Own Memories

Robert C. Goldblatt

Sperry Univac
Blue Bell, Pennsylvania

After a semiconductor memory subsystem has been installed as part of a computer system, it must remain accessible to testing by the customer engineer—testing as part of preventive maintenance, and testing for diagnosis in the event of malfunction. This remains true even though memory components have been tested by the semiconductor manufacturer before shipment, again by the subsystem builder upon receipt, and yet again at the subsystem level before installation in the computer. What kind of testing is done at the system level depends on whether the subsystem includes simple error detection (parity) or a higher level of error correction, and is complicated by the fact that the program executing the test must be stored in the same memory that it is to test.

Individual memory chips usually accept and produce one bit at a time; at the subsystem level, memories are ganged to work with bytes, words, or double words. Only when it has become part of a computer system is the chip in the environment for which it was built. Now the connections that drive it are no longer a test mechanism; they are a central processor, its control unit, and various input/output (I/O) drivers, all controlled in their access by a priority network. With test mechanisms, memory timing factors were measurable to within a nanosecond; now, with a number of different system connections, memory accesses may vary by as much as 50 ns. Variations are found because a nanosecond represents a difference of a few inches of wire, and because of the physical positioning of the various components within the system. Access time tolerances must be wide enough to allow for these variations, and recovery must be fast enough to allow an early access after a late one (Fig. 1). These conditions impose the need for the computer to test its own memory, with a test program that is stored in that memory.

Three different stages of computer program tests must be considered. In the development stage, every area of a subsystem must be thoroughly tested to verify the design, to detect any logic or timing errors, and to insure that the device actually functions as intended. In the manufacturing stage, tests assure that subsystems are being built exactly as specified by the developers. Finally, in the customer usage stage, diagnostic and prognostic tests assist the customer engineer in locating causes of malfunctions.

Addressing Tests

An important part of development tests are addressing tests, which insure that accesses to one set of chips are not also inadvertent accesses to another chip set, on the same board, on a different board, or in a different cabinet. If partial word accesses are allowed in the system, all such partial accesses must be tested. All boundary conditions between different memory segments must be tested. If the system's address format can refer to more words than are physically present, unused high order address bits or other "illegal" addresses must be checked to see that they either indicate errors or wraparound to low addresses, depending on the addressing logic. These and other error conditions, which are supposed to set

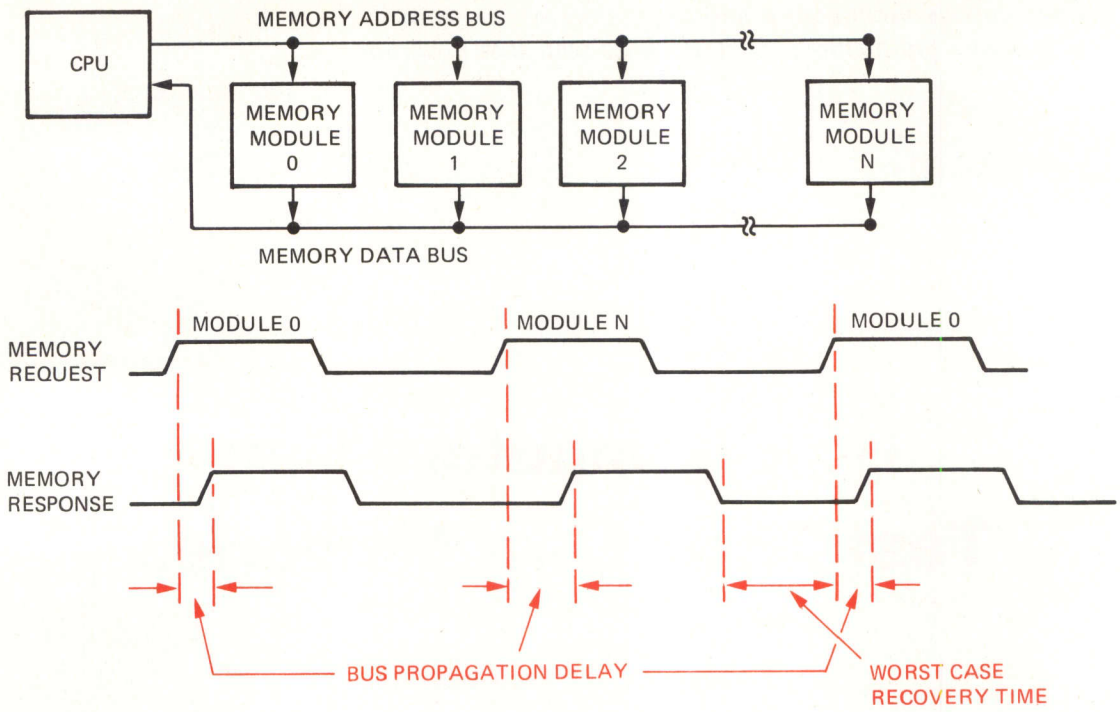


Fig. 1 Access time tolerances. Modules at different distances from CPU respond to signals at different times, all of which must be within system specifications, even though broader than module specifications. However, different response times must not set up insufficient recovery time between cycles

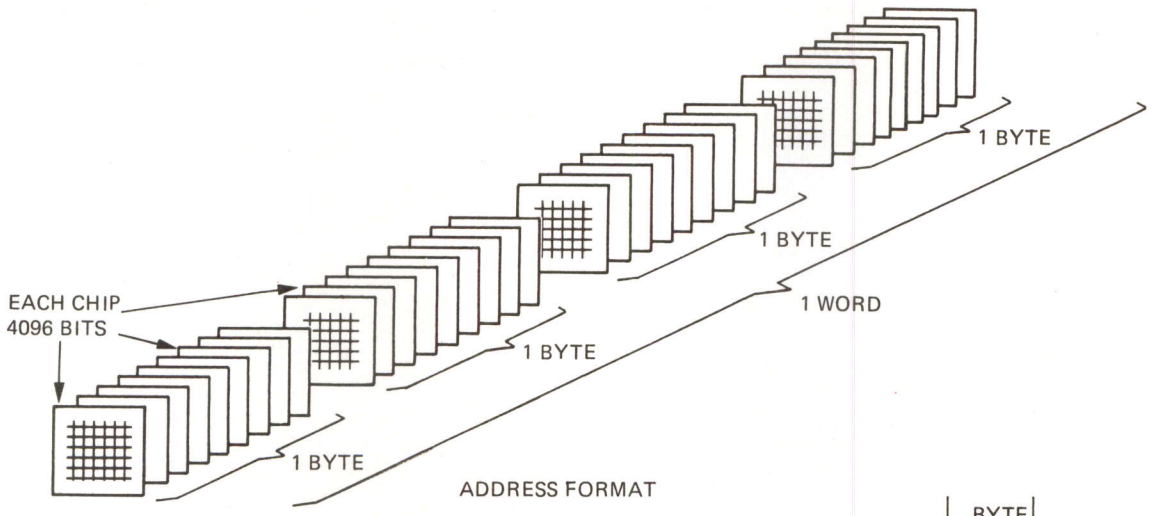
error indicators, must be tested for proper operation—which requires creation of the errors, sometimes with special switches or jumper wires.

All these tests can be executed by computer programs, which are subject to certain requirements. First, the program should occupy no more than half of the smallest available memory module, from which it can test the other half, then move itself to the second half and test the first half. All additional memory can be tested from one of these two areas.

How much memory to test as a unit can be determined by multiplying the number of bits per chip (a chip-design parameter) by the number of bytes per cycle (a system-design parameter). This rule comes about because memories are generally made up of a number of chips in parallel. A memory cycle thus addresses one bit from each chip in a parallel set, as specified by a memory address register (MAR), which addresses the same location on each chip. Thus, for example, with 4K chips and 4-byte access, a block is 16K bytes (Fig. 2).

For this case, assuming that a parity bit is appended to each 8-bit byte, 12 bits within an instruction address point to one word of 36 bits or four bytes. They select one bit on each of 36 chips. In a purely byte-oriented machine, two more address bits point to one of the four bytes. If partial-word accesses are permitted, these two bits can be expanded to four—one for each byte—allowing any combination of one to four bytes to be addressed. In most applications only combinations of contiguous bytes will be useful. These 12, 14, or 16 address bits, placed in the MAR, must fan out to 36 chips for each 4-byte access. Larger memory subsystems with more than 16K bytes have longer addresses; higher-order address bits choose other sets of chips, on the same or a different circuit board, or in different cabinets.

Within the memory chip, the 12 word-oriented address bits are divided into two groups and are separately decoded to identify a particular bit cell at the intersection of two lines in the x and y directions. One of several possible such divisions is two groups of six bits each. Outside the chip, MAR bits 1 through 6 can be connected to address inputs 1 through 6; however, if connected 1, 5, 3, 6, 2, 4 or in any other order, the only internal difference would be the physical location of the bit cell addressed. It is important to recognize that such a crossing over of address bit identities can also occur within the chip, often without the user's knowledge, even if a one-to-one external connection is made. Test programs that depend on bit adjacencies should take such addressing schemes into account. (Some manufacturers of 4K memory chips use 12 address lines on 12 inputs; others multiplex 12 lines onto six inputs. In the generation of 16K memories that are now beginning to appear, all devices announced to date multiplex the address lines. The 14-bit addresses required would necessitate large unwieldy packages if pin-for-pin address inputs were used. Multiplexing must be taken into account in subsystem design and in testing.)



ADDRESS FORMAT

S-SELECT	Y-SELECT	X-SELECT	BYTE SEL.
---SS	YYYYYY	XXXXXX	BB

Fig. 2 Testing unit. Convenient block for one test cycle is product of bits per chip and bytes per cycle. Address format must contain enough bits to locate one bit cell on every chip; it may have additional bits to identify specific bytes or other memory blocks

Bit Pattern Tests

Assuming for the purposes of this article that the address connections from MAR are one-to-one, that they remain one-to-one internally, and that the bit-cell array within the chip is 64 by 64, the problem of setting up desired bit patterns within the chips arises. For example, to store a pattern of alternating 1s and 0s in a set of chips (a checkerboard pattern), it is necessary to store a word of 0s followed by a word of 1s. This is repeated to the end of one row (all values of x for a fixed value of y). The next row (y incremented by one) must start with a word of 1s followed by a word of 0s (Fig. 3). If addressing is not one-to-one as assumed, considerable address juggling is required in the program to produce this same pattern.

However, both all-0 and all-1 words have the same parity bit; a 1 if parity is odd. Thus different patterns must be used to produce the checkerboard pattern in parity bit chips. Similarly, any test that involves data patterns must be repeated with other patterns to test the parity bits.

Initial testing should store, then check, all-0s, all-1s, alternate 1s and 0s, and its complement. Then, since all patterns could have gone to one or a few locations, the next test should load each location with its own address, then read it back and verify it. Next the complement of the address should be stored and checked in each location. These tests show that addressing within a set of chips is unique.

After initial testing, difficult or so-called worst-case patterns should be tested. Various patterns known as walking 1s and 0s, marching 1s and 0s, galloping 1s and 0s, ping-pong, Rowpat, Criss Cross, Ranpat, and others are used for this purpose. They test unique addressability, data-disturb patterns, and high speed address-line switching, and look for pattern dependency.

A major difficulty with many test programs is their execution time. However, a program that takes many hours to execute can be replaced by two others that operate in seconds. Both types determine whether storing data in any given cell affects data in any other cell, and exercise the most extreme changes in addressing as a measurement of access time. Short programs can do a better job of testing these parameters than one long program can.

With either approach, the memory must first be filled with a background pattern. A fast processor that can move 256 bytes with one instruction in 100 μs would require about 7 ms to store the background pattern in a module of 16K bytes (4K words). Then various fetching, comparing, and storing operations must take place.

Worst Case Testing

Galloping 1s and 0s test compares every word with every other word, looking for interaction between words as fetching and storing take place. The test can be

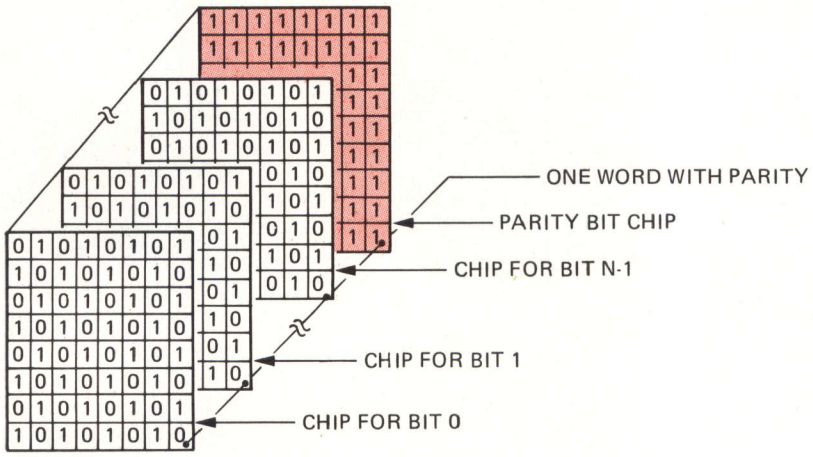


Fig. 3 Word-bit relationship. Each word comprises one bit from each chip. Words with data bits chosen to set up prescribed patterns in their chips are likely to set up different, undesired, patterns in chips that store parity bits (color)

(a)	(b)	(c)
0000	0000	0000
0001	0001	1111
0010	0011	0001
0011	0010	1110
0100	0110	0011
0101	0111	1100
0110	0101	0010
0111	0100	1101
1000	1100	0110
1001	1101	1001
1010	1111	0111
1011	1110	1000
1100	1010	0101
1101	1011	1010
1110	1001	0100
1111	1000	1011

Fig. 4 Address switching pattern. Conventional binary sequence (a) frequently changes more than one bit at a time, as shown in color. Gray code (b) includes all binary combinations but in an order that always changes only one bit at a step. Modified Gray code (c) also includes all combinations but changes maximum number of bits per step; it is useful in testing for delayed address-bit switching

implemented with a relatively short program containing an inner loop that is executed $(4096)^2$ times and a somewhat longer outer loop executed once for each word, a total of 4096 times. Total execution time for this routine on a 4K-word block is less than 3.5 min. for a single pattern. It should be repeated for that pattern's complement, a corresponding pattern that tests the parity bits, and its complement. This increases the execution time to nearly 14 min. for the same size block. If the block is part of a megabyte memory, total testing time—given the assumed cycle and execution times—is nearly 15 h. Some machines will take three times that long, for this relatively uncomplicated pattern; other tests will have execution times an order of magnitude longer.

Although galloping 1s and 0s tests both crosstalk and address switching, crosstalk can be tested just as well with marching 1s and 0s and address switching with a modified Gray-code address sequence. The marching test reads and writes both 1s and 0s against the next location in the direction of the march. It makes eight passes. Four begin with background data patterns of all 0s and all 1s and march both forward and backward through the memory block; the other four do the same, but test parity bits instead of the words themselves. This takes about half a second for a 4K-word block and half a minute for a megabyte memory. As a test for crosstalk, the march pattern depends on adjacency of consecutive addresses.

Gray code, or reflected binary code, is a straightforward method of obtaining all 2^n combinations of an n-bit quantity in which every adjacent pair in the sequence differs in exactly one bit. It is most useful when converting an analog quantity to digital form, especially when the analog quantity is mechanical, because it is not subject to uncertainty caused when two bits that should change simultaneously are slightly mistimed.

In checking address switching, a sort of inverse Gray code is useful. Such a code changes the maximum pos-

sible number of bits from step to step, instead of just one. A binary number representing an address is complemented, so that all bits change, and then almost recomplemented, changing all bits except one. The one bit that does not change is chosen so that the addresses after each double complement form a Gray-code sequence (Fig. 4).

When applied to memory testing, the technique divides each address into three parts: column-select bits X, row-select bits Y, and chip-set select S. To test a given set of chips, S remains constant; then within the set, Y alternates between one value and its complement while X undergoes the double-complement sequence. This addresses all bit cells in two rows of each chip, corresponding to Y and complemented Y values. Y is given successive values, and their complements, beginning with the two rows at the ends and progressing toward the center. Each time Y changes, X goes through the whole routine. After both X and Y have gone through the entire sequence, checking every word in a module with a given S-address, S-bits are put through the same sequence, this time with X and Y held constant. Their values must be judiciously chosen, and held constant while only one pass is taken through all the possibilities for S, because otherwise this sequence may stray outside the limits of the memory system being tested or wipe out the test program.

While this sequence of addresses is being generated, data being placed in the memory consist in each case of an initial background of all 0s, read word by word, checked, and replaced with their own addresses. Afterward all locations are checked against a straight binary count. This sequence takes 75 ms for a 4K-word block, and less than 10 s for 1M byte.

If any of these tests detect an improperly functioning bit cell, the bit's identity is not important. The chip, or the board containing the chip, must be replaced.

These tests assume a 36-bit memory consisting of four 8-bit bytes (32 bits) and a parity bit for each byte. With the advent of 4K chips, memories have become cheap enough that adding a few more bits for automatic single-bit error correction is feasible and reasonable. In place of the four parity bits, an 8-bit field is established, containing an error-correcting code (ECC). Part of the execution of a write command generates error-correcting check bits for the word, which are stored along with the word. When this word is read, the extra bits check its validity, and if an error has occurred, correct it if possible, and signal its presence if not.

Well over 90% of memory problems that occur in the field involve single bits. Multiple-bit errors, with each bit coming from a different chip, usually denote a problem elsewhere than on the chip. Therefore only single-bit correction is necessary.

Testing ECC fields involves storing, then reading, patterns of all 0s, all 1s, alternating 1s and 0s, and so on, just as in a parity-checked memory. Particular data patterns are necessary to produce the required patterns in the extra check bits.

Error Detection Tests

Beyond checking the bits themselves, with crosstalk and address switching, the ability to detect and correct errors must be tested. This requires a way to store a known difference between data and related ECC pattern—perhaps with a manual or programmable switch that inhibits the ECC. Known data are stored in a large segment of memory, setting the check bits. Then the ECC inhibit switch is set, and modified data are stored. Finally the switch is reset and data are read. If the modification was a single bit inversion, it should be "corrected"; uncorrectable modifications should be flagged as such.

This procedure should be carried out several times, beginning with the known data as a pattern of all 0s and continuing with all 1s. In these cases, modifications should be an opposite bit in a single position in the word, testing every bit position in successive words. Similarly, the test should begin with patterns of words with one odd bit modified to invert the odd bit. Finally, if the system permits partial word accesses, they should be tested similarly, with manufactured errors both in the accessed part of the word and in the unaccessed part. A complication arises with partial accesses, namely, every partial write requires complete regeneration of the check bits. This capability should also be tested.

Other patterns can be applied if the user deems them useful, but since testing every possible bit pattern with every possible error is not feasible, a judicious selection is necessary.

Summary

Memory testing within a computer involves considerably more than testing individual chips. All aspects of the memory's architecture and its interfaces with various accessing mechanisms must be tested. These tests are performed by computer programs, which must operate in very short periods of time, because tests that run hours or days are not a reasonable way to locate simple hardware malfunctions.

Tests described in this article are not meant to be all-inclusive. Complete memory tests can be developed only after obtaining a thorough knowledge of the memory's construction and its entire usage within a computer system.

Bibliography

K. Jackson and B. E. Sear, "Measurement Techniques for Testing High Speed Memories," *Computer Design*, May 1975, pp 127-132

E. R. Hnatek, "4-Kilobit Memories Present a Challenge to Testing," *Computer Design*, May 1975, pp 117-125

IEEE Computer Society, *Digest of Papers*, 1972 Symposium on Semiconductor Memory Testing, Oct 1972, pp 51-53

IEEE Computer Society, *Digest of Papers*, 1973 Symposium on Semiconductor Memory Testing, Oct 1973, pp 27-44, 83-85

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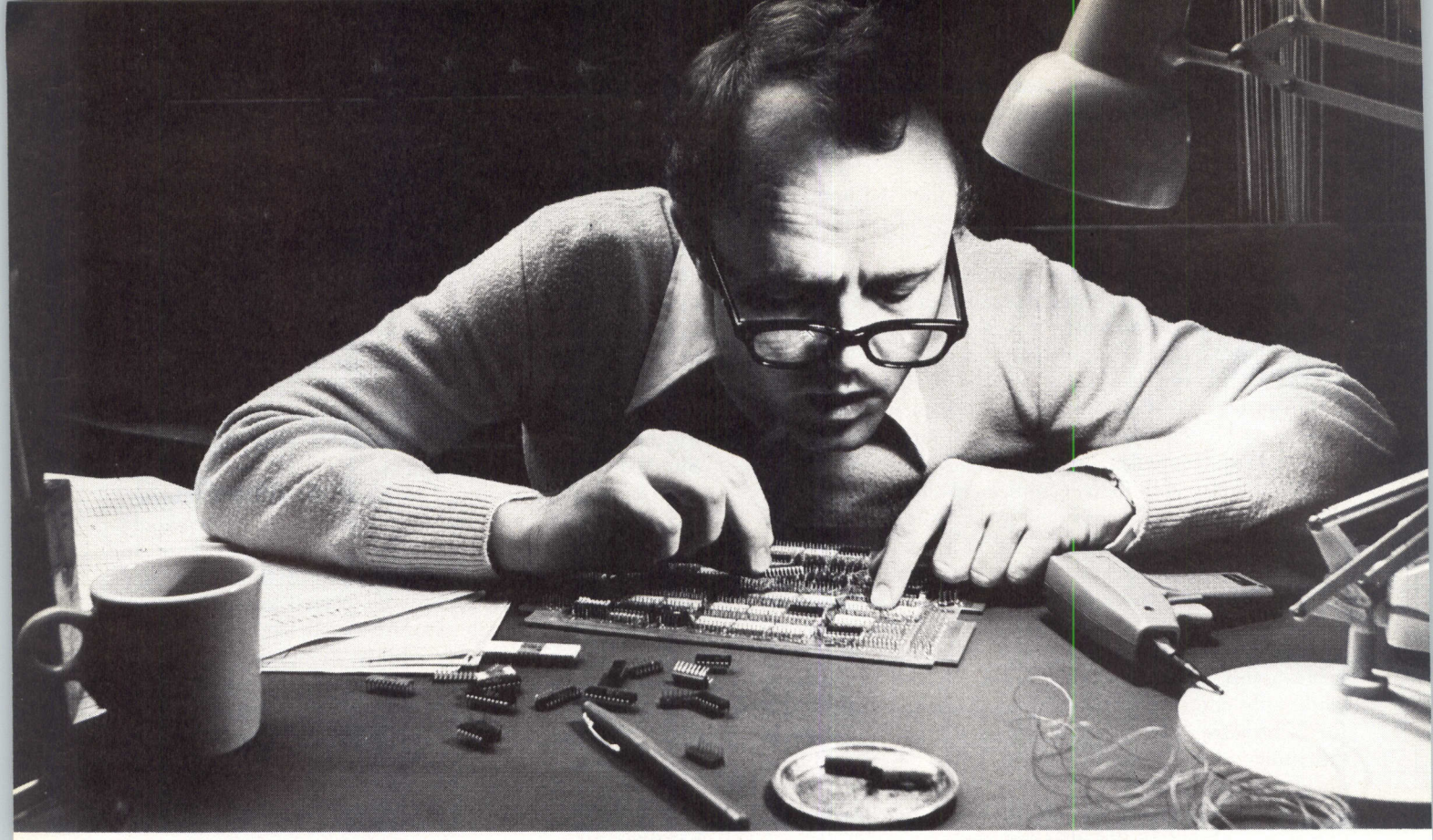

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CIRCLE 39 ON INQUIRY CARD

Often promoted as applicable to a wide variety of problems, associative array processors, in fact, are very useful in some applications but are not suitable at all in others

Associative Processors: A Panacea or a Specific?

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In the recent past, associative array processors have been touted as having great power and applicability in such diverse problem areas as signal processing, text processing, photo interpretation, air traffic control, weather forecasting, signature analysis, and missile tracking. Apparently their promoters consider them the ultimate computer design, a panacea of sorts. However, although there is a niche in which they can serve very well, they are not suitable as general-purpose computer systems.

A small number of associative array processors (AAPs) have been built, eg, the Sanders Orthogonal computer (c 1966), Goodyear Staran (c 1971), and Raytheon RAP (c 1974). It seems that every computer architect has also designed one, so that a virtually unlimited number of AAPs exist on paper. Some of these designs have been carried almost to hardware, such as the Sanders Omen and the Honeywell ECAM. No doubt more will be built as the marketplace is demonstrated by the few entrants in the field.

Architecture

An AAP is a bit- or byte-slice processor (Fig. 1); ie, it processes much data in parallel or simultaneously, but along separate paths, or slices, on a bit-by-bit or byte-by-byte basis. Each processor slice consists of one 1-byte processor, or processing element (PE), or several PEs in series, operating on a fixed byte position of a set of words in any of several configurations (Fig. 2). All PEs in the slices operate in lockstep on the data. AAPs with precision from 1 to 16 bits per byte are frequently proposed; an extreme example of precision is the Illiac IV, which can be thought of as an AAP with the precision of a 64-bit byte.

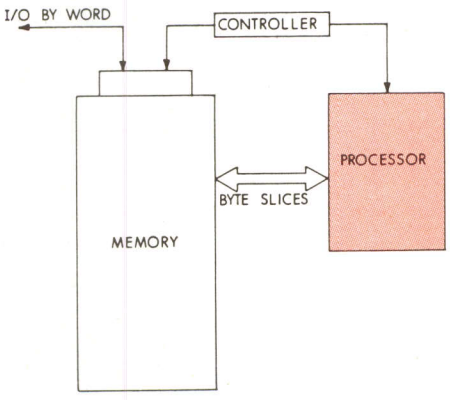


Fig. 1 Associative array processor. The processor itself (color) is actually a large number of processing elements, each working serially on bytes that may be only one bit each. All elements execute the same instructions at the same time, but on different data

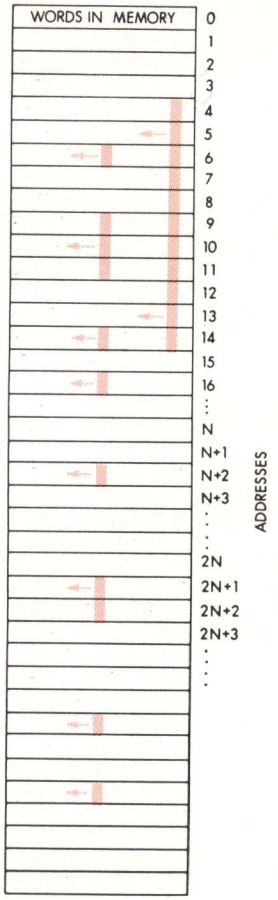


Fig. 2 Slices for processing. AAP may work with one bit from each of a set of contiguous words extending part or all the way through memory, or with one bit from each of a distributed set of words. Successive cycles process these words bit by bit (colored arrows)

A slice requires two parameters: its length, which equals the number of processors, and its width or precision, which equals the number of bits processed simultaneously within the slice. Normally the length of the slice is obvious from the context, so only the width need be specified. Because the width is usually one bit, this article frequently uses the term "bit" when a byte of an unspecified number of bits more than one is possible.

In concept, all data are processed in respective slices either identically or not at all, and all operations are carried out in synchrony on many data streams. In practice, some AAP designs have allowed different operations by different slices. For example, the Omen allowed add/subtract to be under PE control so that any set of additions and subtractions could be performed simultaneously.

All slices share a common main memory. In the simplest case, the PE in the slice processor is an extremely simple 1-bit full arithmetic and logic unit with a few bits of storage for carry bits during addition and masks for control functions (Fig. 3). X is a flip-flop used for storing the carry, Z is the memory mask flip-flop, and Y is a register. The memory mask register, comprising memory mask bits from all PEs, acts like a sieve during store operations, which modify the reference memory location only for those PEs with memory mask bits equal to 1 (Fig. 4). For PEs with 0 in the memory mask, the corresponding memory location is not altered.

Memory Layout

One major problem with using any sort of highly parallel computer system is the organization of data in memory. Several different organizations are possible; each facilitates certain applications. One such organization is that of Fig. 2, with data laid out one character, byte, or word after another. For some algorithms, there are very few comparisons of one datum to its neighbors, in which case each PE's data can be processed separately from the others, and stored as a separate block of words or bytes. A layout suitable for numeric processing is shown in Fig. 5(a); another, for bit-by-bit algorithms or associative work, is in Fig. 5(b).

Because of the complexity of the data organization problem, numerous devices have been invented to pro-

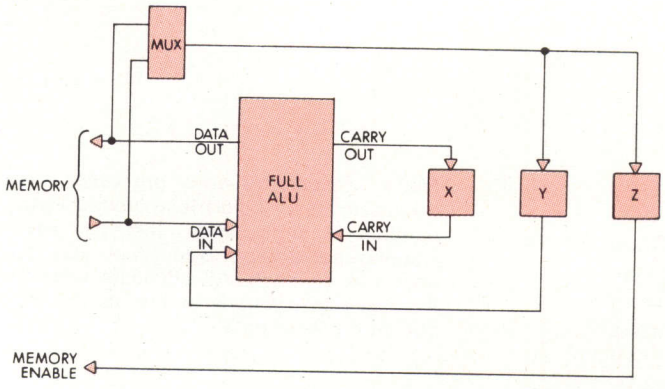


Fig. 3 Processing element. Although relatively simple, element gives the AAP great computational power because it is replicated many times through the system. X, Y, and Z are registers; when the PE is one bit wide, they are single flip-flops

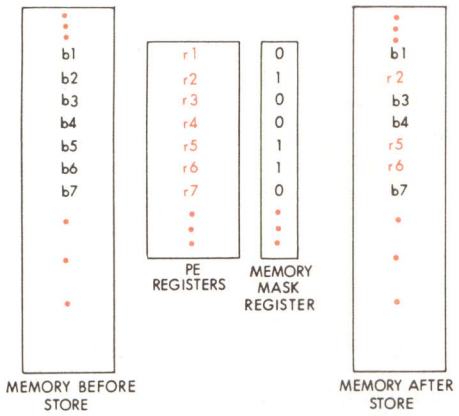


Fig. 4 Memory mask. Mask controls whether data from a PE register actually go to memory during a store operation. All PEs execute the store, but an individual PE whose mask is 0 merely goes through the motions without actually storing anything

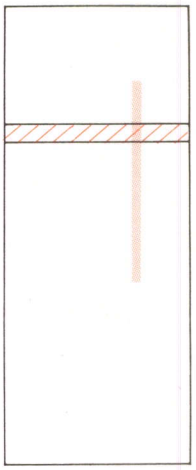


Fig. 6 Orthogonal structure. Cross-hatched area is word slice, accessible by I/O channel (parallel by bit, serial by word). Solid color is a bit slice, accessible by PEs (serial by bit, parallel by word)

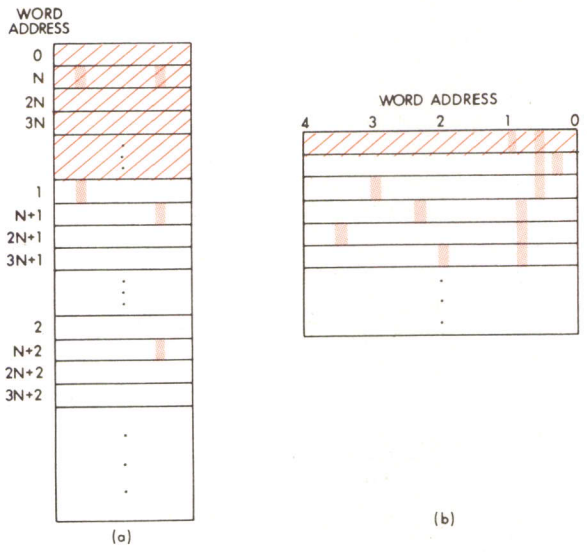


Fig. 5 AAP memory organization. Color cross-hatching shows the part of total memory assigned to the first PE in the array. Organization (a) is suitable for numeric work; consecutive addresses are in different modules. Organization (b) is suitable for associative processing. A third organization, that of Fig. 2, is the usual arrangement for I/O-oriented tasks. All three show the same two sets of bits arranged two different ways

vide alternative paths to memory, such as orthogonal memory, indexed memory, multidimensional access, and sliding window. Virtually every AAP has an orthogonal memory, which allows access to either a slice (serial by bit, parallel by word) or a word (serial by word, parallel by bit) (Fig. 6). Word access is necessary for ordinary input/output (I/O) operations, but slice memory reference is required for associative processing.

Indexed access is the capability of each PE to specify an independent offset from its normal access. It facilitates the storage of arrays with dimensions that do not quite fit the most easily used blocks of memory. For example, if a matrix of $(N + 1) \times (N + 1)$ elements is stored row by row in memory organized in blocks N-elements wide, an indexed fetch operation brings out the elements of a column (Fig. 7).

With multidimensional access, used in Goodyear Aerospace Corp's Staran, memory can be organized into words of any bit-length that is a power of 2. A system, for example, may contain 256 PEs and a single main memory that can conveniently be divided into 256 individual PE memory blocks (PEMs). Multidimensional access hardware permits each of these PEMs to consist of one 256-bit word, two 128-bit words, four 64-bit words, and so on, down to the opposite extreme of 256 1-bit words. Fig. 5(b) is an example of the first of these organizations; Fig. 5(a) might be viewed as an intermediate layout of 16 16-bit words; and Fig. 2 shows the 1-bit word organization. Any AAP has one or perhaps a few layouts available; multidimensional access makes the full range available when a system is installed and permits the organization to be changed quickly.

Sliding-window access is the controller's ability to specify, from among N memories labeled 0 to $N - 1$,

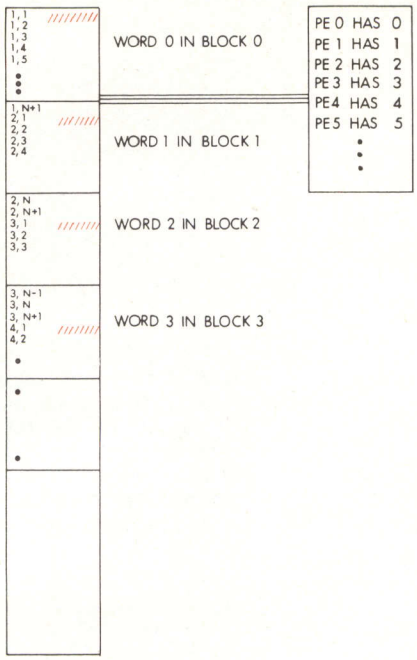


Fig. 7 Memory indexing. Each PE has an index that modifies the memory address from which it fetches data. By this means, a column of a matrix that does not quite fit the memory modules can be fetched easily. A slightly different indexing pattern would fetch the rows

which memory is number 0. Remaining modules are in a fixed sequence. The capability requires a programmable shifter in the memory access path (Fig. 8).

Routing and Skewing

Sliding-window access is a special case of data routing and skewing, or moving data from one PE to another or from one PEM to a PE other than its own. It requires a routing and skewing switch, the sophistication of which is a major factor affecting the flexibility of the computer system. Types of data movements required for an algorithm largely determine the programmer's difficulties in efficiently fitting his algorithm to the hardware for which he is coding. Both skewing (PEM to PE) and routing (PE to PE) are necessary for machines with multiple registers in each PE.

There are many typical skewing patterns, each with a similar corresponding routing pattern. For example, a simple binary shift transfers data from each PEM to the PE some number of positions to the left or right, the number being 1, 2, 4, 8, ... In a linear array, the two PEs at the end are considered "next" to one another for purposes of the binary shift—ie, the linear array is in fact a ring array. If the number of positions shifted is not restricted to a power of 2, the skewing pattern is a barrel shift.

The perfect shuffle and its inverse are important skewing patterns; the perfect shuffle sends the data from PEMs 0, 1, 2, 3, . . . , to PEs 0, 2, 4, 6, . . . , in much the same way that cards move when a deck is cut and shuffled; ideally the cards of half the deck pass between the cards of the other half. The inverse of the perfect shuffle is simply the undoing of this operation.

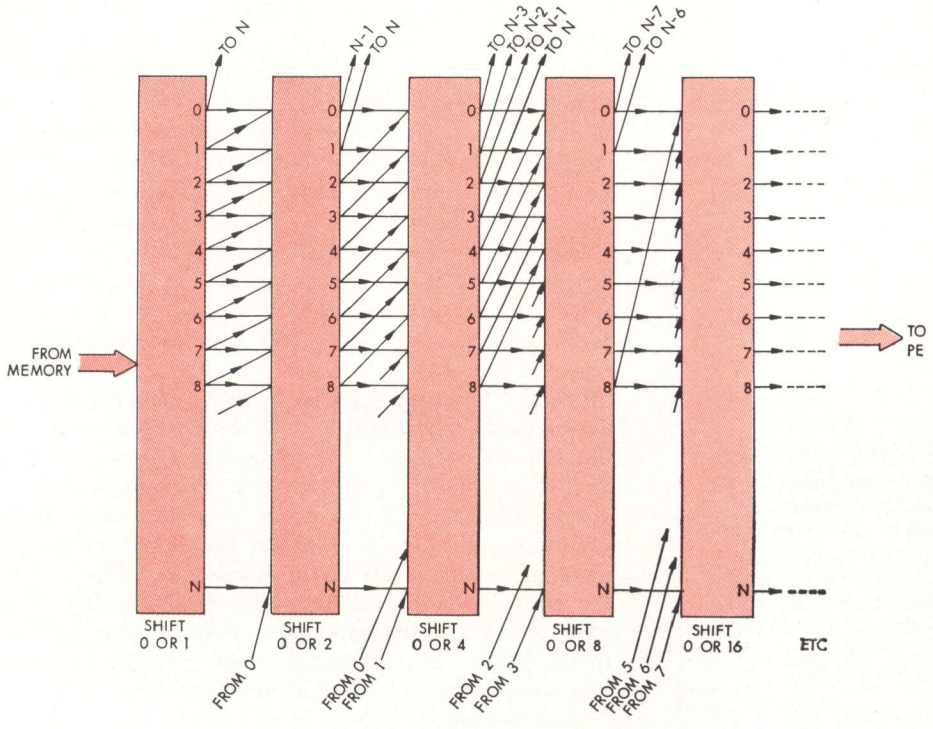


Fig. 8 Skewing switch. Two alternatives at each level can be set to alter block structure of memory, providing sliding window access. Strategem is transparent to programmer. Similar switches aid generalized skewing patterns, of value in various algorithms

If the number of PEs is a perfect square, PEs can form a matrix, in which a skewing pattern transfers data from a PEM in that matrix to a PE at the corresponding position in the transpose, in which rows and columns of the original matrix have been interchanged. In addition, broadcast operations are required when a datum must be loaded into all PEs or some major subsets of them, including a single row, a single column, or the first k or last N − k PEs.

Many routing and skewing operations are economical in an AAP because only a 1-bit slice is being skewed. Thus a full crossbar switch for 64 PEs can be built with 1-of-16 multiplexers using only 256 ICs yet providing far more capability than the few skewing patterns mentioned would indicate. However, since the switch size increases in proportion to the square of the number of PEs, a crossbar switch is not practical for machines having many PEs. A machine providing most of the useful operations would require many fewer ICs to implement than a full crossbar switch.

Arithmetic Instruction Times

Some typical arithmetic operations form an example of AAP microinstruction control. Each PE has a full adder which accepts two data inputs and a carry input, and generates one result and a carry output; the carry output automatically replaces the carry input from the previous operation. To add two 32-bit integers then requires 32 micro-operations, assuming that the carry register is initialized to 0 as the fetch for the first bit is performed. The bits are fetched in order from right to left. Although this is a fairly lengthy operation, the advantage of doing it this way is in the assumption that many more than 32 PEs are simultaneously adding pairs of 32-bit numbers, completing all of them in the same time required for one.

Similarly, multiplication of a pair of 32-bit integers requires 31 additions of 32 bits each, for a total of 992 micro-operations. Table 1 lists how many micro-operations are required for some typical AAP arithmetic operations. For all these operations, timing is independent of the number of PEs, and 4-bit slice processing is four times as fast as 1-bit slice processing. In contrast, among several typically associative operations (Table 2), although timing is still independent of the number of PEs, speed increase for 4-bit processing is generally less than a factor of four. This leads to a significant conclusion about AAPs—that multibit precision processors and array processors such as Illiac IV are relatively better suited to numeric processing than to associative work.

Bit-slice processors are best suited for non-numeric work, because speed increases slowly as slice precision increases and because there are fewer liabilities from a large number of PEs for non-numeric work. Non-numeric processing requires few skew patterns, and if done on a bit-by-bit basis, pipelining the switch is a natural way to increase the efficiency of switch hardware. On the other hand, numeric processing requires many skew patterns, for efficiently implementing matrix algebra, fast Fourier transforms, interpolation, and the like. Because skew switch size increases as the square of the number of PEs, it is not economic to have more than a few skew patterns in an AAP with a large number of PEs; however, many patterns can easily be built into a machine with 16 or so PEs.

One design tradeoff compared a 1024-PE machine having 1-bit slices with a 64-PE design having 16-bit precision operation in the PEs but bit-slice PEMs. The comparison showed that both machines had approximately equal numeric speed, as might be expected, but that the 1024-PE system was 16 times faster on typical associative operations. For any problem set, the optimal machine will probably not have a unique slice precision; eg, PEs may operate on 16-bit slices but skewing and routing may take place on 1-bit slices.

Partial Differential Equations

Many important physics problems require solving partial differential equations (PDE). These include weather forecasting; cloud or storm, bomb-blast, geotectonic, and earthquake modeling; and aerodynamics. The problems are so large that few computers today can handle them. Typical method of solution is to set up a grid on the area or volume to be studied and numerically integrate the equations at each grid point. Since there are usually thousands of grid points, the problem is highly parallel and apparently well suited to associative array processors.

Such is not the case, however. Algorithms for solving these problems require many arithmetic operations, generally with floating-point operands to cope with the wide range of data magnitudes. Furthermore, because of the subtractions used for computing the approximations to

TABLE 1

AAP Instruction Times For Arithmetic Instructions

	Bit Slice		4-Bit Byte Slice	
	Add	Multiply	Add	Multiply
16-bit integer	16	240	4	60
32-bit integer	32	992	8	248
32-bit floating*	184	584	46	146
48-bit integer	48	2256	12	564
48-bit floating*	312	1608	78	402

*Floating-point data are assumed as 8-bit exponent and 24- or 40-bit mantissa

TABLE 2

AAP Instruction Times For Non-Arithmetic Instructions

	Bit Slice	4-Bit Byte Slice
Search for greatest 32-bit integer*	97	97
Match 20 6-bit characters	120	30
Find best fit, 50-bit field	60	23

*Timing assumes entire 32-bit or 20-character field is checked

derivatives, high accuracy is needed. Minimum word length for problems of this size is about 40 bits. To use Table 1, assume a 48-bit word length; each micro-operation is executed in one clock cycle at 10 MHz. The algorithm consists of a ratio of two additions to one multiplication and negligible proportions of other steps. According to the table, two floating-point additions on 48-bit words require 624 clock cycles, and the multiplication requires 1608 cycles. Total is 2232 cycles, which at 10 MHz requires 223.2 μs for each loop of three instructions. At this rate, one PE can execute 4480 3-instruction loops/s, and an AAP having 1024 PEs can execute 4.59 million loops/s—or about 13 million instructions/s (MIPS). A similar calculation yields the same figure for 256 PEs with a 4-bit slice.

This rate might be just acceptable for, say, weather forecasting, over a usefully large area with enough grid points to give reasonably dependable results. However, boundary conditions, heterogeneity of the air (or the modeled substance), and nonparallel operations in sufficient quantity as to be non-negligible, contrary to the stated assumption, all combine to make any AAP highly unlikely to approach this rate. Maintaining 10 to 20% of this rate on any real problem would probably be good. On the other hand, Control Data Corp's 7600, which is not an AAP, can execute about 10 MIPS on these problems.

Difficulty of keeping all PEs busy continuously is illustrated by a hypothetical global weather circulation model. This model requires a grid of points covering the globe, and can conveniently be evaluated by an AAP having one PE for each grid point which lies along the equator. If the grid includes 256 such points, they are spaced approximately 1.4 degrees of longitude, or 97 miles, apart. After the PEs process meteorological data along the equator, they start on grid points immediately north of the equator, working their way step by step toward the North Pole to evaluate the entire northern hemisphere. (The southern hemisphere would be a separate process beginning at the equator and proceeding toward the South Pole.) As latitude increases, grid-point separations (in miles) decrease, even though x-separation in degrees of longitude remains constant; thus at sufficiently high latitudes adjacent PEs become largely redundant. At such latitudes, therefore, for the model to continue to work efficiently, longitudinal spacing of grid points must increase, which means that some PEs in the AAP must stop working. This is an economic disadvantage, because all PEs that become inactive at high latitudes are nevertheless necessary, and must be paid for, to process data at low latitudes.

However, changing the grid-point spacing in this way introduces difficulty in implementing interpolation between points, required because complete evaluation at any given point requires data from nearby points as well as local data. The difficulty is minor if the number of points always decreases by a factor of two; it can also be traded off against an even further reduction in the number of grid points, and thus of the total amount of computation, by increasing grid-point spacing in smaller steps.

Most general equation for this weather model includes terms for various kinds of terrain, to the extent that terrain influences the weather. If the model were evaluated by a serial processor, terms referring, for example, to mountains and oceans could be skipped when evaluating grid points in plains and deserts. However, an array processor must compute all terms for all points, even when some are meaningless, because all elements of the array must remain in step at all times.

Another major area of difficulty for current AAPs is performance limitations that are imposed by their memories. Although large disc storage units with parallel read/write heads can supposedly give AAPs arbitrarily large I/O bandwidths, main memory bandwidth remains about the same as that of a serial processor. Furthermore, latency problems are more critical than transfer rates for most applications. The only bulk memory technology that would favor AAPs over serial computers would be one suited to both very long words and very high word data rates. Few serial processors can take advantage of, say, 1024-bit words at a 10-MHz rate.

Text Processing

At first glance, AAPs seem well suited for text processing, but investigation shows some serious disadvantages, eg, the problem of dictionary lookup. Given a fixed dictionary of some kind with, say, 10^5 words, lookup is simply matching one datum to a large set—a classic associative problem. However, if dictionary entries are in alphabetical or other prescribed order, a serial processor, using a binary search, will require no more than 17 compare operations; using a clever hash code—derived from logic operations on the dictionary entries—this could probably be improved by a factor of five or so, although the comparisons might be more time-consuming. These same techniques can be used in an AAP with N PEs, so that it does one compare on no more than N dictionary words—a simple hash code could easily achieve this. However, because words in the dictionary already have their hash codes, only the one word being looked up requires a new hash code, which one PE can generate.

If, instead of merely looking up words in a dictionary, the problem involves a thesaurus, in which a search is made for a "path" of ten or fewer synonyms connecting two words, memory conflicts (Fig. 9) make the problem just about impossible to implement efficiently on any array processor. Although this is not a very common problem, it illustrates a task that can probably run faster on a PDP-11 than on an AAP.

Air Traffic Control

Another area often cited as requiring an associative processor is air traffic control. The problem is complex because the number of possible conflicts between aircraft is proportional to the square of the number of aircraft. However, analyses generally overlook the fact that conflicts need be checked only for nearby aircraft.

A hypothetical algorithm checks on all possible conflicts during the next 60 s, within 4 s—sweep rate for a typical air traffic control (ATC) radar—of the illumination of a given aircraft. During that 60-s period, subsonic aircraft will travel no more than 10 mi in a generally forward direction (Fig. 10). This means that

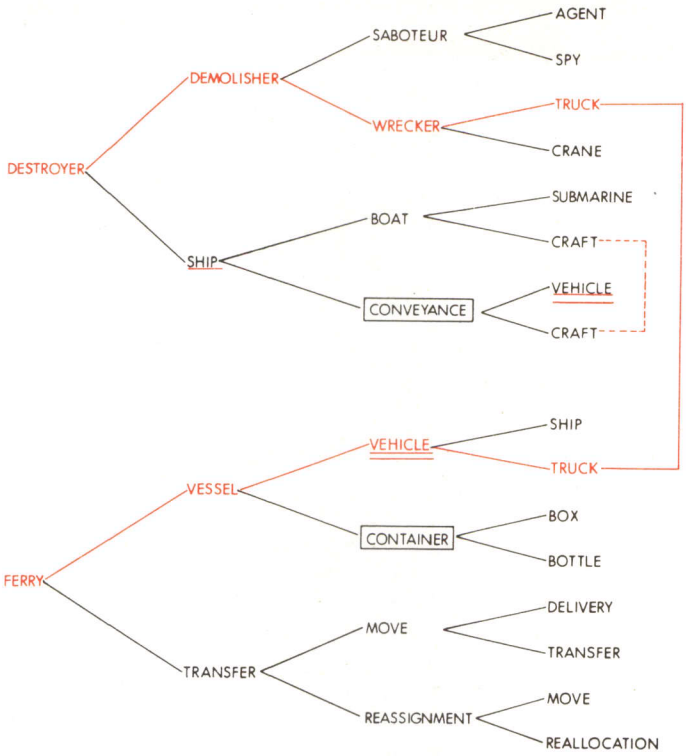


Fig. 9 Thesaurus problem. Path of synonyms links the terms "destroyer" and "ferry" (color); a second shorter path that skips two levels is indicated by color underscore. Dashed color line indicates a path that loops back on itself. If search is performed in an AAP with each PE memory containing only words beginning with the same letter of the alphabet, conflict would occur when two similar but not necessarily synonymous words are found at the same search level (shown in boxes). Such conflicts double memory access time; they are likely to be numerous, and so render synonym searches unsuitable for AAPs

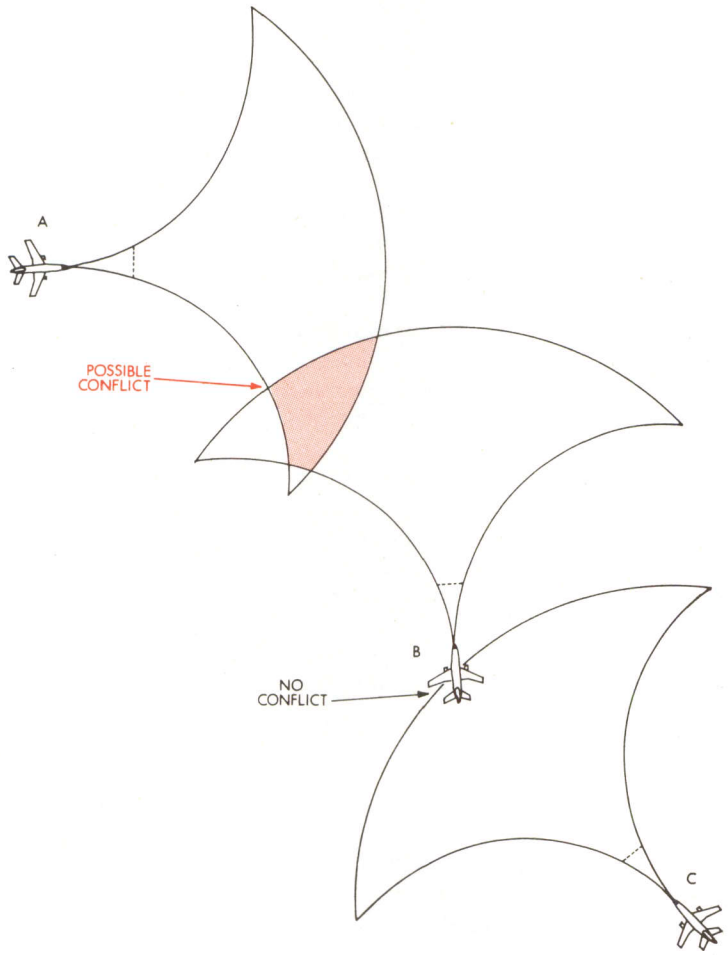


Fig. 10 Conflicts in air traffic control. Conflicts occur only ahead of aircraft involved, taking into account possible turns during a period of maneuvering. Color shows possible conflict between aircraft A and B; B and C do not conflict, because if and when C gets to where B is now, B will be somewhere else

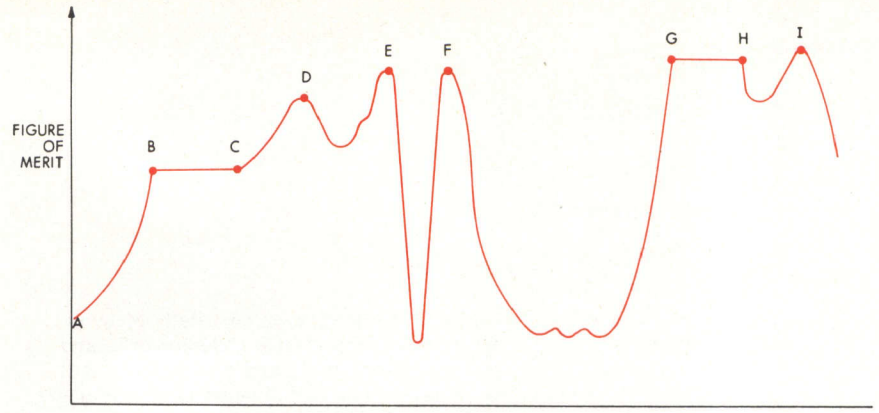


Fig. 11 Best-match search. Successive comparisons of data points with a reference, when done serially, are time-consuming. However, an AAP can compare all points against the reference at once, locating the best match (point I) in a few microseconds

possible trajectories of each aircraft need be compared only to those within 20 mi of it. Altitude bracketing further reduces the number of aircraft to be considered. In the vicinity of a terminal, aircraft are moving much more slowly, so that the 20-mi clearance distance can be reduced. This problem hardly appears to justify introducing exotic computer architectures. Reliability is, or should be, the primary concern when choosing ATC systems, not exoticness.

Correlation and Comparison

The particular applications cited above, for which AAPs are ill suited, show that they are not panaceas. However, in one major application area, they appear to have a decided edge over the competition.

When a best-match search is made serially on a data set that cannot be linearly ordered, much time elapses. For example, suppose a data set with the quality curve shown in Fig. 11 is being analyzed serially from left to right. It is assumed to contain 1000 points, each with 50-bit precision, and each compared with a 50-bit reference; measure of goodness is the number of equal bits, whether 1s or 0s. This is not a wholly hypothetical problem; the task occurs, for example, in interpreting "noisy" photos, speech recognition, adaptive pattern recognition, and dictionary look-up where errors are suspected in the original message.

In the example, a succession of points with varying degrees of goodness are found. Sometimes, as between A and B, each new high is almost immediately surpassed; sometimes a series of equally good values comes in succession, as between B and C or between G and H; and sometimes one value reigns supreme for a long or short period before a better datum appears. In the example, the very best turns out finally to be point I.

If the 1000-point set is analyzed by a 1024-PE AAP that runs at 10 MHz, point I can be located in about 6 μs. Few serial processors can solve the problem as quickly. However, even here, for large data sets, better serial algorithms may reduce the AAP's advantage.

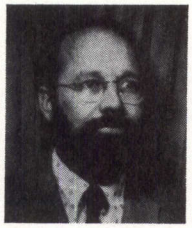
An earlier example showing that dictionary searching is best done by serial computers assumed error-free text. Looking up "Camputer" with hash codes, for example, is likely to hash the program. Here the AAP will break through to the right answer quickly. Furthermore, the 1-bit PE, which requires only a few dozen gates, can easily be put on a custom MSI chip or fabricated out of a few off-the-shelf MSI chips, in either case operating at 10 MHz without difficulty.

In other words, the 1024-PE AAP is not necessarily a monster machine. In fact, using LSI, 16 to 64 PEs can conceivably be put on a chip today.

Conclusion

The associative array processor is well suited to some problems which to date have not been satisfactorily solved. It is not a general-purpose computer, but has a niche of its own. It is well suited to applications such as photo interpretation, signature analysis, speech or handwriting analysis, or text processing for noisy texts. It is ill suited for highly numeric tasks such as weather forecasting and signal processing. Serial processors can do very well in still other areas such as air traffic control and dictionary look-up. However, as the precision of an AAP's slice is increased, its numeric capability becomes ever more cost-effective.

If both AAPs and serial processors were being produced in quantity, the AAP could search disordered tables more cost-effectively than the serial processor, because its 1-bit arithmetic logic unit is faster and simpler. This table searching would also be efficient in cases where the entire table must be checked, regardless of how quickly a first match is found, as where many keys are involved. However, in most table searching the AAP is not significantly better than a serial processor.



Lee Higbie, an assistant professor at the Massachusetts Maritime Academy, is currently on leave to the University of Massachusetts where he is doing research in array processor architecture. He is an active consultant on computer and system design and on operations research.

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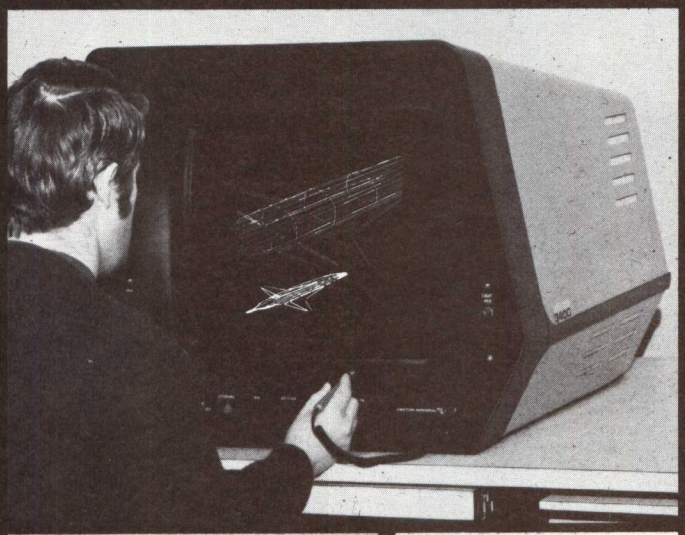

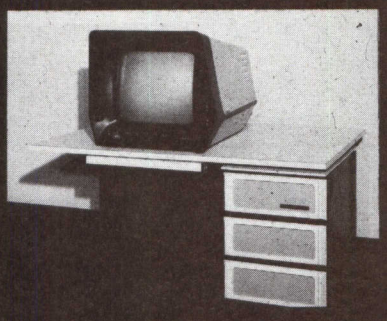

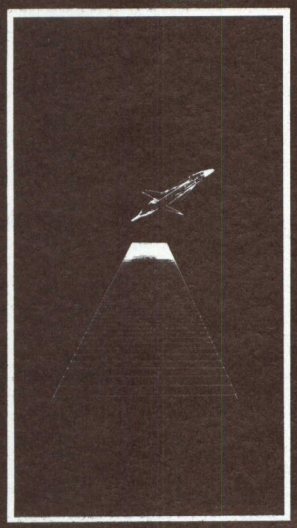

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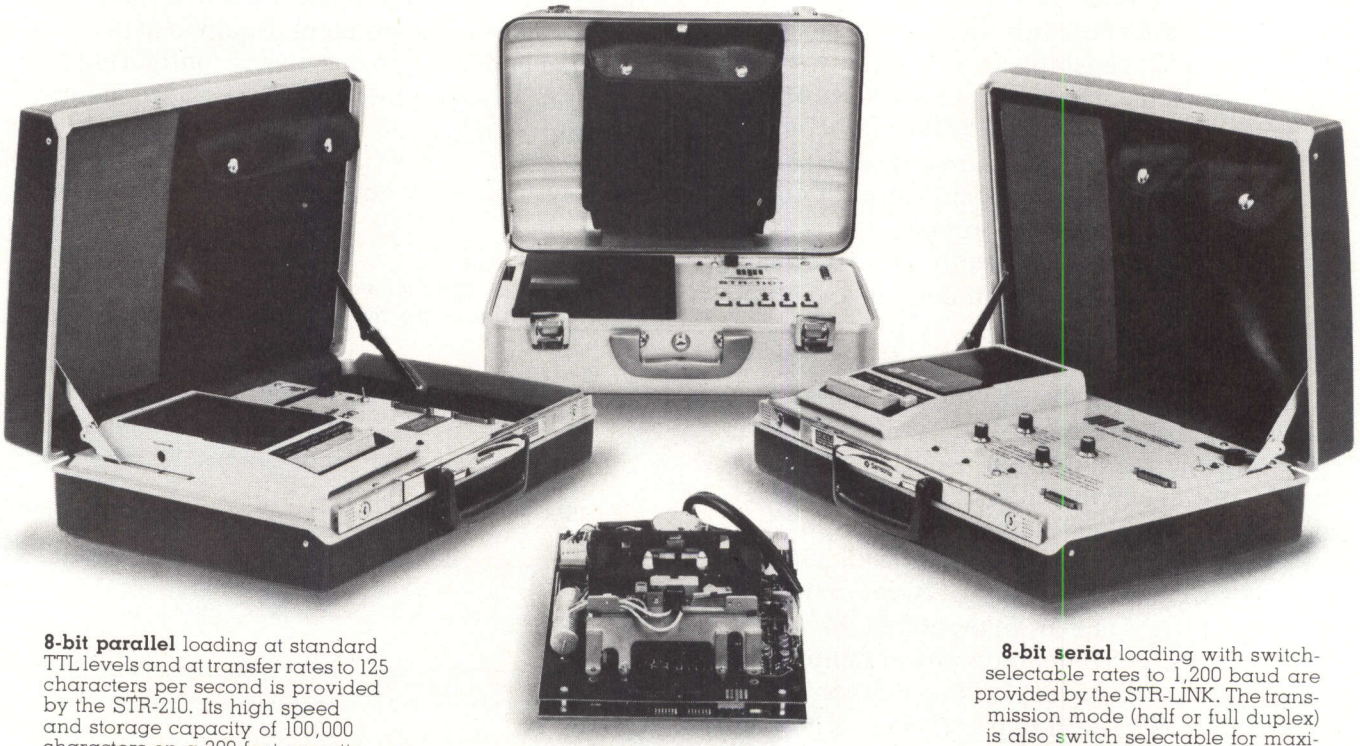


8-bit parallel loading at standard TTL levels and at transfer rates to 125 characters per second is provided by the STR-210. Its high speed and storage capacity of 100,000 characters on a 300-foot cassette makes it ideal for memory dumps as well as program loading. Priced at just $700.

OEM systems recorder, the STR-100, is a complete tape-drive unit that provides full remote signal or character control of all transport functions. It includes read-write electronics, control and timing logic, and motor-control logic. All you need to supply is a mounting location, power supply, and an interface with the controlling I/O device and you have a reliable unit for program storage and retrieval.

8-bit serial loading with switch-selectable rates to 1,200 baud are provided by the STR-LINK. The transmission mode (half or full duplex) is also switch selectable for maximum flexibility. Data capacity is 100,000 characters on a 300-foot cassette. Priced at $1,190.

CIRCLE 42 ON INQUIRY CARD

Addressing the question of whether mini and micro system languages will become marketable and find wide use, panel sheds light on economic and philosophical stumbling blocks encountered in implementing these programming tools

System Languages for Microprocessors: Considerations and Trends

Computer Design
Editorial Staff

Will system languages be successfully developed for microprocessors? If they won't, users of these proliferating devices face a bleak future of programming at the symbolic level or even in machine language. If they will, the future in some respects is almost as desolate, as languages that supposedly run equally well on several manufacturers' machines turn out to require tweaking or trimming of some sort when moved from one to another. This has come to be the grim truth with system languages for large computers; whether it will continue to be true for small systems remains to be seen.

The question was addressed by a panel of experts at the IEEE Computer Society Conference (COMPCON 76 Spring) last February in San Francisco, and again by seven speakers participating in three sessions at ELECTRO 76 in Boston in May. Although their different viewpoints cast some light on the subject, unfortunately they reached no definitive conclusion—and could hardly have been expected to, on a question as broad and as important as this. They expressed divergent points of view on the effect the mini and micro industry has had on system languages and vice versa, on how the languages might be used, on cost-effectiveness, on compilation versus interpretation, on the profile of the customer base, and on the languages and the vendors who provide them.

Terry Opdendyk, manager of software development for Intel Corp, moderator of the Compcon panel, pointed out that activity in system languages at a low level has been extant since the late 1960s, but no results have reached the market in the form of tools offered by manufacturers and used extensively by customers for their system programming. The question is whether mini and micro system languages will be marketable and widely used, or will remain in the academic background like their older cousins.

The past three years have been tremendously active. Microprocessor system languages were produced by Intel in 1973; a year later one observer estimated that 35% of all microprocessors shipped were coded in a high-level system language—a very large percentage at such an early stage in the life of a product line. Although that figure may be imagined, or may be based on a statistically indeterminate number of microprocessors, such that it is both correct and meaningless, either way, a number of minicomputer and microprocessor manufacturers have announced system languages—including Hewlett-Packard, Digital Equipment, Signetics, Motorola, and National Semiconductor. Similarly, a number of independents have products of this nature for the marketplace.

Is this a "bandwagon" effect, or merely a bump in a process that repeats history? Is it related to the extremely low hardware cost of microprocessors, the rise of programming costs, the emergence of structured programming, software engineering, and maturing computer science education—or are they merely coincidental?

The Compcon panel attempted to project its members' personal viewpoints—not necessarily representing those of their employers—regarding the future of

system languages. Besides Opdendyk, the panel comprised

- Gary Kildall, an active consultant in the microprocessor and language field for several years, and the inventor and implementor of PL/M, a system language for Intel microprocessors
- Wes Patterson, manager of microsystem software development for Motorola Semiconductor Products Div, Phoenix, Ariz
- Jerry Ogdin, president of Microcomputer Techniques, Reston, Va, an applications-oriented consulting firm, who claims to have done work in 36 high-level languages
- Bill Barrett, who is responsible for system programming at Hewlett-Packard's Data Systems Div, Cupertino, Calif. Formerly a professor of electrical engineering at Lehigh University, Barrett has worked in computer and software engineering for 18 years
- Colin Gobel, manager of high-level language development for Intel, Santa Clara, Calif
- Peter Christy, staff consultant and staff assistant to the vice president of software development, Digital Equipment Corp, Maynard, Mass. Christy describes himself as a "corporate gadfly," whose job is to influence hardware people with software ideas and to force changes in the company

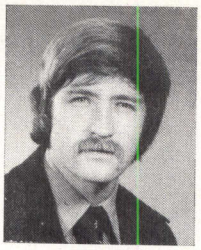
Individual's points of view have been summarized here. Because some speakers returned several times to a particular subject, their remarks have been presented in a revised order if necessary to conjoin discussion on each subject. In many places the speakers' words have been retained, in others they have been edited to provide cohesiveness and order to the discussion. Each speaker has been identified wherever possible, although some identifications may be omitted or uncertain because the speaker was not clearly identified or because the remark came from the audience. (This summary was made from a tape recording of the session.)

What is a Microcomputer?

Any discussion of system programming languages for microcomputers must either define what is meant by the terms "microcomputer" and "minicomputer," or, by relying on unstated assumptions, run the risk of getting bogged down. A definition is particularly important because it seems to change often as technology advances. However, Peter Christy observed that one very dramatic difference does not depend directly on technology; it is that microcomputers are really components.

Minicomputers continue to be sold over the years at a more or less constant price; however, what the buyer gets for that constant price changes rather dramatically. Current market figures and projections from various sources lead to the conclusion that in 1980 a complete minicomputer system with a half-million bytes in the central memory, and a couple hundred million bytes on a disc, with 20 terminals connected to it will represent a cost of $50,000 to

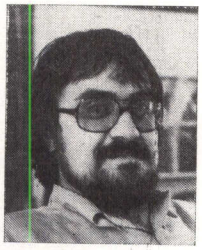
Gary A. Kildall



G. Wesley Patterson

Jerry L. Ogdin

William A. Barrett



Peter Christy

the customer. However, the annual salaries of 20 terminal operators on one shift add up to a good fraction of a million dollars. If those people are amortized unmercifully for five years, they cost a capital equivalent of $2 million. When the hardware cost is only $50,000, how the hardware is used is irrelevant. The payoff comes when people are effective in getting their jobs done. At that point, if there is something wrong with the way the system programming language runs on the hardware, the problem can be easily solved by engineers.

Meanwhile, the $50,000 price identifies the system as a minicomputer, although it will not be used the way a 4K-word PDP-8 or an Intel Intellec™ is used today. On the contrary, large segments of traditional minicomputer business will have slid into small silicon packages; the makers will bid them fond farewell and develop new $50,000 systems. Microcomputers will undergo the same kind of metamorphosis.

Ultimately, there will be a "who cares" attitude. In the good old days, processor efficiency people said a bit saved was a bit gained, and that was really important. Today everyone has a pocket calculator, which is in frequent but certainly not continuous use. Technology forecasters never thought of the pocket calculator, because all they could see was a pocket PDP-8. Nevertheless, calculators represent the dominating use of logic today.

Definition of SPL

Opdendyk defined a system programming language (SPL) as any language in which one implements a system. He felt that the definition is broad enough for almost any kind of panel discussion, because it includes assembly language and absolute coding, and goes all the way to FORTRAN and COBOL—in each

of which individuals have claimed that at least one system has been written. He also admitted that the definition might be too broad.

Kildall liked the definition, especially from the system viewpoint, but rather than argue relative advantages of assembly and high-level system language, he essentially came down on the side of the latter. "System languages are with us; they exist; they prove themselves to be useful," he said, "and it's only a question of how they will evolve and what sort of direction we can give them."

Colin Gobel, on the other hand, preferred a somewhat narrower definition. He said that the key concept of a system programming language is to provide a cost-effective means by which its users can develop complete microcomputer-based systems. SPLs are a key tool of microcomputer software designers and developers, and are unquestionably destined to achieve much more widespread usage in the future.

Microprocessor systems have particular aspects that may not be evident in large mainframes, Gobel said. For example, they usually operate in real-time, and are tightly linked to a particular application—a traffic light controller, small business system, or whatever. The system language must provide the right tools for that initial software development. These tools must permit that software to be modified and enhanced and to utilize the hardware resources efficiently. Usually these objectives cannot all be realized at once. System programming languages must attempt to strike the right tradeoff between those objectives.

System Vs Application Programming

Whether system programming and application programming are significantly different became a point of issue between Jerry Ogdin and Peter Christy. Ogdin felt that they are essentially alike, their only difference being the user's identity—the programming methods are the same. What traditionally has been called system programming is primarily to allocate the machine's resources, to control real-time input/output, and so on, and that is precisely what many microprocessor applications are. Instead of dividing the power of a large machine to run several external tasks or devices, each of several micros is dedicated to one such external application.

Christy, on the other hand, insisted that application and system programming are extremely different, especially in minicomputers. Over a period of time, application programming will disappear from computers. For instance, everyone at DEC would like to have a $2000 desktop PDP-10 at home. There would be a tremendous initial market for it if the price were right because everyone in the engineering organization would buy one immediately—but would your mother buy one? Would she really want to learn how to program? The vast majority of the world wants nothing to do with programming. On the other hand, system programming can be an invaluable aid to professional people who design and build the computer your mother can and will use.

The vast majority of the world wants nothing to do with programming

With such disagreement on the definition of a system program language, the panel considered some general qualifications of such a language. Jerry Ogdin led off by observing that while few users write system programs or care about system programming languages, system software, operating systems, or translators, most users, when faced with writing a program for a traffic light controller, would rather not do it in absolute hexadecimal code. They need a suitable language.

The ideal language, to Ogdin, is very rich, with procedural ability and a lot of flexibility in its data structure, and also the ability to descend into something similar to assembly language, to allow the user to allocate the machine's resources. Languages approaching this ideal would pay off primarily in small-volume applications. In high-volume applications, the advantage of saving a few bytes of code warrants the additional expense required to save them. Ogdin later returned to this advantage in a discussion of economics.

With a good language definition, Ogdin said, standard cross-compilers or even standard native compilers could be built. Present system programming languages are partway solutions. They favor procedures instead of data structures, which is a fundamental flaw in the way most people look at language design. People jump on the structured programming bandwagon without understanding what the bandwagon carries. Furthermore, existing languages are much too machine de-

People jump on the structured bandwagon without understanding what it carries

pendent. They generate unportable programs, and do not insulate the user from the machine in any way. Not only must he know the machine that the language translator works on, but he must know the bowdlerized version of that machine for which the translator generates code.

Ogdin's conclusion: "I know what I want. I want a language that's rich in procedural ability, and rich in data description ability. I'd like it to be highly portable, I'd like it to be highly optimizing, and I'd like to pay about 20 bucks. But I'm willing to compromise." Barrett and Gobel assured Ogdin that attaining all these goals would be impossible.

Other Characteristics

Simplicity is a major factor, in Kildall's view. System languages have to be simple, if they are to be implemented on several different processors. Simplicity leads to fairly easy and reliable translators, and eventually to self-hosted translators, which run on the microprocessors themselves. One manufacturer already does this. Simplicity also considerably reduces the learning barrier for users of the language. With a simple system language, various application languages can be implemented, which are transportable between machines without much difficulty.

Real advantages of system languages, as Gobel sees them, are to get lower software development costs by giving programmers a tool specifically tailored for their needs and not for the needs of the machine; and lower maintenance costs by writing programs in a modular structured fashion, perhaps in easily readable fashion. Ensuring this is a software management problem, but having the right tool available will ease that problem. System languages also provide enhanced product reliability, because humans are best suited to algorithm development, while machines and compilers are best suited to generating the details of particular machine code sequences; system languages let each one do that task to which it is best suited.

Opdendyk asked if there were a reason for the apparent derivation of many minicomputer languages from ALGOL, while micro languages seem to be derived from PL/1. He suggested that this conformity might mean that existing system languages do not represent the user's needs. To this implication Christy replied that the actual languages are almost irrelevant. A lot of possible languages like FORTRAN are clearly wrong, in a number of ways, but equally obvious is that any system language must have a number of characteristics. Certain other characteristics are important to some people and unimportant to others. People have very strong feelings, but that is not the relevant issue. The conflict is not whether one is the right language or one is the wrong language, within bounds; it's between having a language or not having a language.

The conflict is not whether a language is right or wrong; it's between having or not having a language

Computers in the Open

A member of the audience claimed that any language tends either to obscure the computer or to obscure what one is trying to do with the computer; it's mostly the latter. The best language would be a non-compilable descriptive language that carries the application as deep in the design as possible so that simple tests need not involve bit manipulations or fooling with the processor, but which could be divided into small chunks mentally translatable without a compiler. Ogdin asked, "If you have that kind of notation, and everybody agrees that it's a nice notation, then why not formalize it a little and build a translator for it?" The auditor agreed that this might be desirable "as long as the syntax doesn't obscure what you're trying to do."

When asked by another member of the audience, "What is the potential in making the machines themselves a little less difficult, so that the system programming language isn't as bad?", Christy replied, "When there is a large existing customer base, all the known difficulties in changing architecture are really horrifying; but where the machines are microprogrammed, the microprogram emulates the main instruction set that the user sees. In this case, making changes to the instruction set is technologically very simple, because they aren't cast in silicon."

Barrett made an additional reply at length: "An evolutionary process also takes place." In the early days machines had the very simplest architecture that could be put into logic. Now as system programming languages are evolving, the machines will have to satisfy some features of the language. Result will be a reasonable mix of simplicity and language adaption.

One of the biggest problems in language design is resource allocation. For example, in a 16-register machine, how are resources allocated to those 16 registers to minimize the number of memory references? Another problem is the special instructions found in every machine. A system programming language is usually designed from a user's point of view, and has no way of incorporating those special instructions. So either such an instruction is never used, or somebody discovers it and uses it in assembly mode. If special features are designed into the language to take advantage of that instruction, the designer has strayed far from some of the objectives of a general-purpose language.

What good is a special instruction if people don't have straightforward access to it?

Other problems are posed by clever algorithmic methods. For example, a cute trick on a stack machine is to build a data structure by exercising an algorithm that leaves words on the stack. Suppose one cycle of the algorithm leaves three words behind. The programmer doesn't really realize this until he studies the code. A series of cycles build up an extensive array, which works as a data structure. When the engineers put a pointer on it, they've added something potentially very useful. But Barrett said he doesn't know how to simulate that in a system programming language. There are also interrupts, and real-time processing, and gauging the time required for a program to go through one cycle, and various other problems involving indexing and loop structure optimization.

Standards

Standard system languages have not previously been successful. They start out well, but then individuals start "improving" them for particular machines. Apparently for a system language to be successfully adopted, it needs an economic or a political reason to survive. Opdendyk asked if anyone on the panel believes there is such a reason today for the adoption of system languages for micros and minis.

. . . for a system language to be successfully adopted, it needs an economic or political reason to survive

Because the PL/M language has been implemented on four different microprocessors, Kildall's opinion is that standards can exist for system programming languages. He admitted, however, that assembly and machine language would still be used in critical applications and critical parts of large programs where compactness or speed were especially important.

Ogdin's opinion is that no common language is likely to emerge within 10 years, for the simple reason that no potential source—semiconductor vendors, users, universities, or software houses—has both the interest and the capability. Self-interest of semiconductor vendors and minicomputer makers dominates structure of the languages and the way compilers and translators are produced, Ogdin said, and those interests are directly at odds with the end user's requirements. An example of that conflict is portability versus efficiency. Semiconductor makers who put out PL/M and its variants are interested in highly portable compilers.

Self-interests of semiconductor vendors and minicomputer makers . . . are directly at odds with users' requirements

For portability, compilers are written in FORTRAN, which takes so much space that the result is inefficient. Efficient code must be tailored to specific kinds of machines or even to specific individual machines.

Users are smart enough to develop a common language; in fact, semiconductor vendors and, to a lesser degree, minicomputer makers, have a gross disdain for their customers' abilities and needs. They tend to design for the lowest common denominator, and do not recognize that most users are pretty savvy if given the tools to work with. Unfortunately users as a group are too fragmented to collectively arrive at a new language unless it's nationally funded—an idea that Ogdin finds intrinsically objectionable.

Very few good languages that have come out of academic institutions have been adopted; a few that might have been commercially practical usually met a fate similar to that of a BASIC compiler for the 8008, written about 1973 by a couple of graduate students at the University of Illinois. When they finished, they wrote their master's thesis and then threw away the associated code.

Software houses can't afford to develop new languages for system programming, because the cost of selling a new language concept is simply too high. Cost of marketing the language makes its construction prohibitive.

Economics of System Languages

Economic considerations ranked high among the obstacles to be surmounted in developing a system programming language, in the opinion of most members of the panel. One such consideration was cited by Patterson, who pointed out that customers of semiconductor manufacturers almost invariably demand second sources, whereas hardly any minicomputer or large mainframe manufacturer has a second source. When their customers require a second source, they choose a similar but not identical machine and write software for both versions. System software isn't a problem for these users because it is provided by every manufacturer from the smallest vendor all the way through IBM. System software has been considered a necessary adjunct to the hardware, and apparently has never been assessed on an economic basis. To Patterson, this raised the question of whether system software can pay its own way, or, in other words, who would pay for system software development in the presence of second sources for hardware.

Semiconductor customers invariably demand second sources, while hardly any mini or mainframe manufacturer has a second source

Software development must clearly and demonstrably pay for itself

In his opinion, software development must clearly and demonstrably pay for itself. However, he noted that money invested in system development languages has a very long return time, and in the recent past the semiconductor industry has not been a popular area of investment.

A further problem is deciding whether microprocessors are components or systems, and whether they should be priced on their declining cost as components or at a stable level over a period of time, as systems. If the semiconductor industry continues to market microprocessors as components, and if the danger continues that customers can take all a manufacturer can offer in the way of support but buy components in volume from a second source, justifying the development of these kinds of systems will become very difficult.

Another panel member agreed that easy portability between identical processors from independent sources implies that software development must be self-supporting. However, investing in that kind of software support is perhaps a little short-sighted. After all, the interest of everybody, both suppliers and users, is to make the right tools available, with which people can effectively utilize microprocessor products, develop better systems, sell those systems to their end users, and benefit everybody.

At Digital Equipment Corp, according to Christy, software development has to pay its own way, because otherwise the developers' budgets are cut off.

Ogdin had a somewhat different view on the cost of system software. "Compiler writers and language designers, for the most part, have experience on large machines," he said, "with perhaps some exposure to minis. With this background, although they are experts in the techniques of building software, which is the same for micros as for large systems, they are often unaware of the significantly different economic equations that describe the cost of software for microcomputers." Thus, where Patterson thinks the economics of software has never been properly worked out, Ogdin says that it has for large computers, that

Language designers . . . are often unaware of the economic equations that describe the cost of software for microcomputers

many of the same people who perfected system software for large computers are trying for an encore with micros, but that these people haven't yet discovered that a new set of economic rules is called for.

Ogdin cited two basic reasons why a particular language might be used—to reduce development costs or to minimize the exposure to risk on high-volume products. In his opinion, reducing cost isn't very important. True, system programming languages will help generate correct code more quickly within certain bounds, and in that way save a little time and money—but the savings are not great. In good system design, cost of coding and translation, from design to object code to test, is perhaps 10% of the job's total cost. Therefore, even wiping it out to zero reduces the total cost of the system by only 10%.

System programming languages can be much more valuable in risk protection. In an application calling for 100,000 masked read-only memories (ROMs) for microprocessors, each storing a microprocessor program, a bug may be discovered after the ROMs are fabricated and delivered, leaving the user with 100,000 pieces of worthless sand. However, if he can apply certain established program-proof methods over a well-defined structured language, he may be able to salvage them. This is not going to happen at the binary bit level; but it will happen at a level where the information content of the source program isn't lost.

Christy thought this view was very optimistic. A lot of people have put energy into proving programs, but the results are always the same, he said. If they had spent the same energy desk-checking the program, they would have come to a better conclusion. Testing is vital, and the people using micros at DEC are being burned by software errors a lot more than the software people ever were. They're still learning what the software people got down pat long ago—that the cost of rigorous design and masochistic testing to be sure that the product is perfect, and then ten times more testing, is easily justified by the consequences of having a bug go out when the product is shipped.

On the other hand, remarked another panel member, when people make hardware/software tradeoffs, they have a strong tendency to reduce hardware costs to an absolute minimum, right up to the boundary of what the processor can handle, either within a given memory space or with given processor execution time constraints. That tendency must change; customers must begin to respect software development costs a little more, and become less sensitive to these tradeoffs.

Customers must begin to respect software development costs

Ogdin gave an example of the economics of microprocessor design in terms of his own company, which works with virtually every commercially available microprocessor, in one form or another. Since the technical staff is very small, it can't afford the luxury of having each person be an expert in a particular processor. Similarly, the company can't afford a home-made system programming language transportable among these various microprocessors. However, although the staff is small, its clients have high-volume applications. Thus, for example, suppose the client plans to build 1000 units of a design worked out by Ogdin's people, at a fee of $20 per production unit. Suppose further that the first pass at the design produces a program of 2100 bytes. Ogdin can easily afford to spend another $5000 to reduce the program by 52 bytes, so that it will fit into a 2048-byte memory and save the client one integrated circuit per production unit.

Transportability

No one claims that a particular system programming language for a machine is necessarily transportable to some other machine. At the very least, someone must write compilers for it. Transportability between successive models in a line is also important, because computer systems evolve. A system programming language highly tailored to one product, and difficult to refit to a new machine architecture, ties up all of a company's software money in one product, and recouping that investment for the next generation is difficult. Therefore an important characteristic of a system programming language is that it should be transportable over at least two product lines, if not three or four.

Barrett pointed out two aspects of portability: portability of language product to a totally different machine, and portability in the sense of changing the machine base under an established compiler written in a system programming language. Larger vendors are in the second situation. Hewlett-Packard, for example, sells many products in the OEM market to customers who write their own software. If these customers were told to write in assembly language, H-P would have no freedom to change the users' machines except at the cost of telling customers to change their software. However, a system programming language permits new machine architectures to be developed in different machines, which will run with existing software. That is a very important consideration. Semiconductor manufacturers do not have that kind of control over the software base.

Patterson considered that point of view to be naive. "You can't force your customers to program in high-level language," he said. "You can perhaps suggest it, but you don't make any hardware changes that cause problems for users." In fact, he went on, the mainframe industry has gone to great pains to maintain hardware compatibility; and although carrying along an outmoded architecture is bad, causing changes at the user level is worse. "So we'll continue to make

hardware structures that are more complex and less efficient than they could be if we were free to change them. That's the price we have to pay to benefit the user whose software continues to run and run and run. The microprocessor will probably prove no exception."

Ogdin had a differing point of view here as elsewhere. He said that transportability does not mean moving a program from machine to machine, where microprocessors are involved. The issue is a transportability of skills. If a company making widgets decides to change from a right-hand to a left-hand thread, it may use an entirely different microprocessor on absolutely firm economic grounds, but its people should not have to learn new language skills. That kind of transportability will come only from the user base. Getting vendors together to agree on a common language is absurd, because standards are not for the seller's benefit; they are for the benefit of the customer.

Kildall felt that such a language would not really be a system language. A system language is a base for implementation of application languages which would have to be changed to make a left-handed widget. For example, a company that does a lot of controller work might implement its own language for handling controllers, based on a system language that would permit transportability among various processors. Simple system languages with uncomplicated data structures will permit some cross-manufacturer standardization. For example, one program compiled with the Signetics PL/M equivalent made the Signetics 2650 microprocessor directly compatible with the Intel 8080 with no alterations of the source text.

Applications

In considering the real application for system software in the microprocessor business, Patterson identified three kinds of applications for microprocessors, only one of which could utilize system software in its usual form. The three applications were the microprocessor as the logic element replacement; microprocessor systems, or microcomputers, as resident software development equipment; and microcomputers masquerading as minicomputers.

As a logic element replacement, a microprocessor in a simple job such as controlling a traffic light does not require much system software. Its peripherals are very specific, and since it is not a multi-user application, its operating system is probably either nonexistent, or is so simple it shouldn't be called system software. At most, it has a bootstrap loader or some diagnostic capability, stored in a read-only memory. In Patterson's view, a lot of systems are cost-optimized to such an extent that even such simple software would not be pertinent.

Examples of the second kind of application, microcomputers for software development, are Intel's MDS, Motorola's EXORciser, and others of a similar nature. They include a certain amount of system software, such as language processors—assemblers are available now, and resident compilers and interpreters are clearly just around the corner. Such machines also have a form of operating system, particularly for flexible disc configurations. However, probably very little if any part of that operating system could be resident in the usual sense, because if a user is building a prototype, he can't employ any part of a resident operating system without requiring that part to be included in the production version. For example, if he is building a traffic light control, he has to write a standalone program; if he uses an operating system, for software development, it must eventually disappear, or provide no more than a very basic file structure.

In the third category, minicomputer-like micros, there is a large market for very inexpensive inventory control, small business accounting, and similar systems which meet some of the requirements for an operating system. For example, the hardware configuration is reasonably fixed, with enough memory to hold resident software plus transient data and a complement of peripherals to move data and nonresident software in and out. Some of the software might include application languages, so that users don't have to program these systems in the traditional languages. These application-dependent languages might fall into the category of system software. This requirement identifies a need for some new system software.

Barrett agreed, in general. He said the principal application of system programming languages is in larger programming projects—not the small in-house maker of traffic controllers, cash registers, and that sort of thing. However, the problem of finding a suitable median among all the diverse objectives of language is almost superhuman, so that compromise is unavoidable.

The average computer designer has enough intelligence to outperform the best compiler . . . because he can come up with tricks it just can't match

The average computer design engineer has enough intelligence to outperform the best compiler in any language in certain areas, because he can come up with tricks that the compiler just can't match.

Patterson went on to say that system languages probably would have to be forced on the vendor by the customers. Certainly Motorola would not be particularly interested in providing the language with which a disenchanted customer could easily move all his software over to Intel products. That certainly happened in the large-machine business, because customers more or less insisted that they wouldn't buy systems without FORTRAN or COBOL.

System languages as they exist today are subject to a number of legitimate objections. In particular, Kildall cited their deficiency in macro processing capabilities and conditional compilation, which are very useful in assembly languages. He felt that loaders do not handle address constants and address arithmetic properly, if at all; but he believes the objections will wither as the languages evolve and acquire some characteristics of assembly language coding.

What Companies Do

Employers of the various panel members were all involved in system language implementation to some extent. For example, Digital Equipment Corp, according to Christy, is very interested in system programming languages because it spends an enormous amount of money on software, and then charges its customers for software. To develop this software, DEC has an internal organization which fights against dogmatic ideas; thus things like structured programming and the uniform use of high level languages have never caught on. However, the company offers a number of successful software products in higher level languages.

At Hewlett-Packard, Barrett said the SPL concept has been sold and will work out very well. Most of H-P's people are using it. The HP-3000 line has a system programming language with escape hatches into assembly mode. These were used almost to abuse in the previous version, but today at least 95% of the average 3000 program is in high level.

Motorola writes two kinds of software. One is cross-computer software—cross assemblers, simulators, and compilers which for reasons of portability must be written in FORTRAN. The rest is developed initially in an internal language called P-notation, which is then hand-compiled into assembly language. If hand-compilation is considered as a use of a system design language, then perhaps 80 to 90% of the programming at Motorola is high level.

At Intel, all software development for 8-bit micros is done using a high level system language; results have been outstanding. Semiconductor manufacturers are faced with a number of problems. For example, they have to deliver products on exceptionally tight time schedules to be competitive in the market. Users demand increasingly sophisticated products with increased capability. Certainly, quality is of paramount importance. Finally, reliability is very important; maintenance costs on a released software product can get out of control in a very short period of time. System programming languages are a very effective means for tightly controlling all of these problems.

Cost of programming is exceptionally important at Microcomputer Techniques. Ogdin wants to minimize that cost, because all of his work is on a fixed-price basis. Therefore the company doesn't use any system implementation languages unless the hand-assembled kind is counted.

Future Trends

In the future, many more complete systems will be built. Every microcomputer application is integrated with a system, thus requiring microcomputer programmers to be fluent with both applications and systems. Systems will also become steadily more complex. As they become more complex, Gobel points out, having the right tool available for their development will become more and more important. Obviously programming costs, which are human costs, will continue to rise; hardware costs, as has been said many times, will continue to fall. Thus it's essential that programmers have the right tools for their task.

Christy quoted a recent article in the trade press which discussed the 8- versus 16-bit argument now going on in the semiconductor industry. The article brought peals of laughter within DEC, Christy said, because it was reminiscent of the company's transformation from the PDP-8 to the PDP-11. That argument raged for three years and spun off Data General. Christy feels that the 8-bit micro will go the way of the 12-bit mini.

Another panel member asserted that the disproportion between hardware and software costs will separate microprocessors from many potential applications. Building a direct high level language implementation on a chip, while not within today's state-of-the-art, is in sight. Efforts over 20 years or more of trying to beat down software costs have been remarkably unsuccessful; so it's just a matter of doing something that we know how to do.

Patterson had a lot of hope for such direct execution of higher level languages. The technology is improving by leaps and bounds. "What are you going to do with a million bytes on a chip if you don't implement a high level language directly?" he said. Ogdin didn't think that was likely, certainly not in the next five years and probably not in the next decade, as long as machine architecture is controlled by the marketing force.

Christy seemed to be frightened by such a prospect, remarking that the rate of change of technology is

terrifying, and quoting Gordon Bell, vice president of engineering at DEC, as saying that "the number of bits on a chip is easily computable as 2 to the T minus 1962." That turns out to be quite accurate. We are approaching the bounds of optical lithography,

In three or four years the microcomputer people will be as lavish in not using every bit as the minicomputer people are now

and we go to electron lithography, and then to X-ray lithography. While this is going on, prices are also decreasing. So anything that's possible now becomes ludicrously cheap in a few years. Christy believes that in three or four years the microcomputer people will be as lavish in not using every bit as the minicomputer people are now. The same arguments applied to the buyer of the 4K PDP-8, to whom that next 4K of memory was the world's biggest increment; today it costs more to make a 4K memory than it does to make an 8K memory.

System languages should become more widespread and people should get upset with them, because only in that way will we see progress

Other viewpoints on future trends: "System languages should become more widespread and people should get upset with them, because only in that way will we see progress."

"A language can be devised for such things as traffic control and carburetion control. Initially it will be a standard high level language. On the other hand, if and when microprocessors are applied to carburetion control, a special processor will definitely be more economical than a programmed function with or without a language. Any industry that uses 10 million units a year can have whatever it wants."

"A high level language for that application would be essentially a description of the carburetion problem. Microcomputer input would be a small array defining the exact parameters of a particular carburetor. This approach to design would tend to reduce proliferation of procedural languages. Instead, the trend will be toward non-procedural statements of the problem intent, with everything needed to solve the problem manifest in the machine. That trend is present in the commercial world now, in transaction processing and interactive programming, where there's much more tabular definition in the process and much less writing of extensive procedural solutions.

Summary

The industry apparently will not end up with a single language. It has been tried repeatedly over the years, and every trial has failed. On the other hand, little is known about the fundamentals of languages, what properties they should have, and what qualities the user can get along without, or add for himself. In other words, an information theory of languages and language translators is needed. We must try to understand the nature of the goal in building these languages and adopt some general rules of thumb. Then, if we decide to build a carburetor class of languages, at the start somebody knows the carburetion problem and knows the basic rules that he must follow.

Christy aptly concluded the session (except for remarks by Opdendyk) with the words: "Natural languages in humans do very poorly what computers do very well. Computers follow rote procedures of very detailed descriptions, and humans use language to wander through rounds of abstraction and vagueness and imprecision. System programmers are apparently trying to eliminate application programmers, because dealing with the latter is a pain. The desire is to replace an application programmer with an artificial intelligence of equivalent capability. Artificial intelligence people are getting fairly good at simulating cockroaches, but that's about all. If an application programmer and a cockroach are comparable logical engines, there is some hope for optimism; but anything that might replace a human application programmer is probably more than 1000 years off." □

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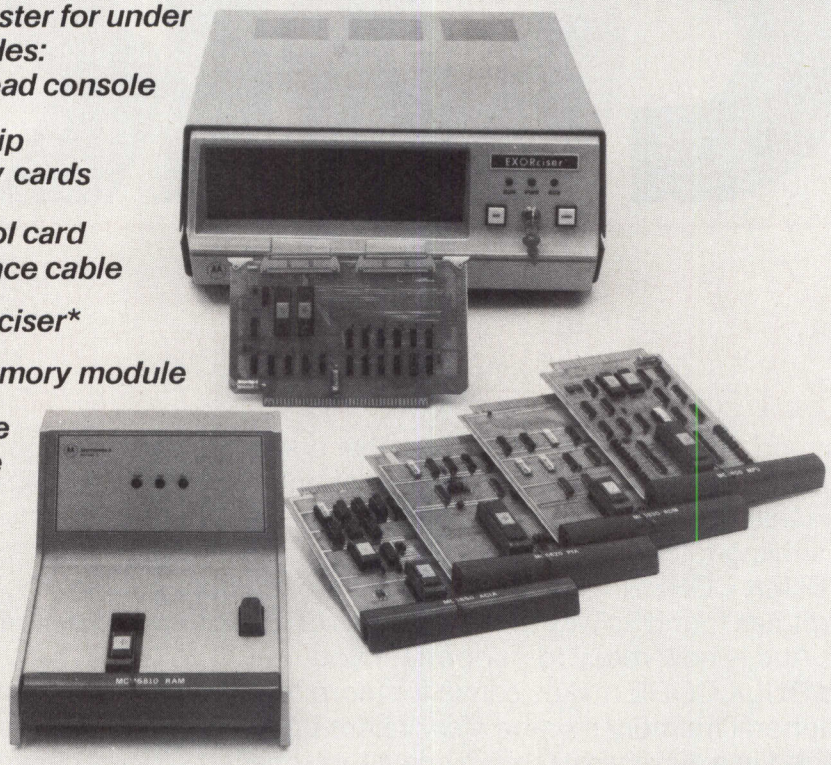

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You can expand your MOTEST-I to test other MOS and bipolar LSI by obtaining additional personality cards, available at costs ranging from approx. $175 to $260.

With MOTEST-I, board test failure and repair becomes significantly reduced. For the latest available data, write Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036, or circle the reader service number. All Motorola data sheets are also available from your in-plant VSMF Data Center, authorized Motorola distributors and Motorola sales offices.

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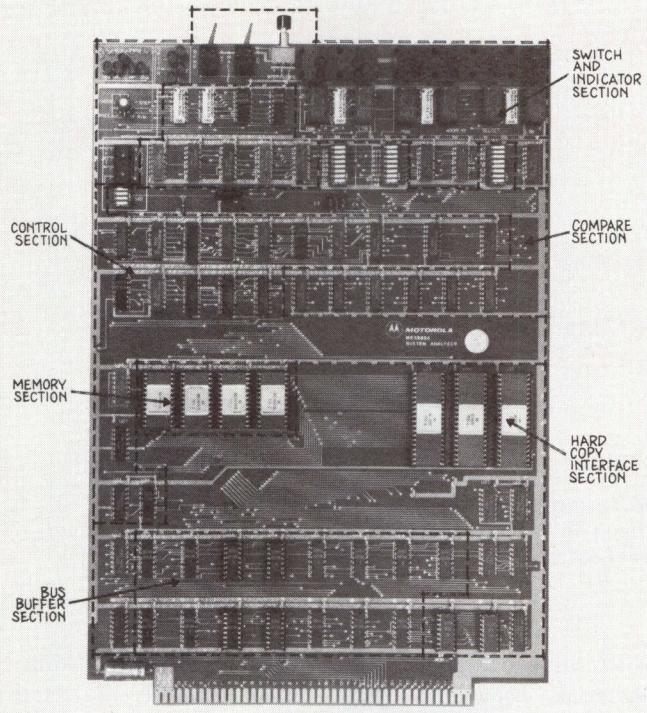
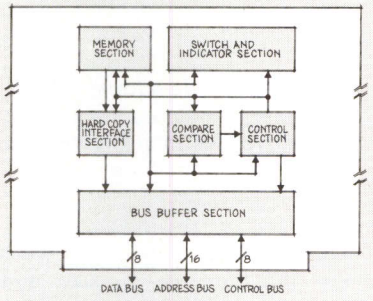
CIRCLE 44 ON INQUIRY CARD

Motorola introduces the low cost analyzer for M6800 systems.



- *Window Mode for real time capture of 128 consecutive MPU cycles*
- *on-board hardware display*
- *monitors, analyzes, and troubleshoots M6800 systems*
- *use as stand-alone unit, or with EXORciser**
- *priced under $1,300*



It's the latest evolutionary development in Motorola's M6800 total product approach to microcomputer systems.

The MEX68SA Systems Analyzer is a highly efficient tool for monitoring, analyzing, and troubleshooting M6800 systems.

And its low cost? Under $1,300.

Each of the Systems Analyzer's operation modes has its individual purpose, of course, but the Window Mode can be the most useful. While the MPU runs at full speed in real time, the analyzer can capture 128 consecutive 32-bit bus cycles and store them, display them... all while the MPU continues to run, uninterrupted. The captured data can be accessed for a hardcopy printout. The other modes are Step Mode, Read/Write Mode, Trace Mode, and Standby Mode.

The Systems Analyzer is hardware oriented because it requires no software for operation, except the firmware for hard copy printing. The on-board hardware display is actually wider than existing logic analyzers, able to indicate 32 bits of address, data, and control information.

For copies of the latest data write Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036, or circle the reader number. All Motorola data sheets are also available from your in-plant VSMF Data Center, authorized Motorola distributors and Motorola sales offices.

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CIRCLE 45 ON INQUIRY CARD

TECH NOTE

New Magnetic Materials Help Core Memories Stay Alive

Rodger D. Thuras

Control Data Corporation
St. Louis Park, Minnesota

Continuing developments in ferrite materials will extend the long history of magnetic memory technology, even in the presence of the challenge offered by advances in semiconductor technology

Core memory technology is not stagnant—despite the publicity describing advancements in semiconductor memory. On the contrary, recent changes in memory design and in core materials have extended the potential of core memories for small-, medium-, and large-scale systems.

Since the early days of computers, ferrite core technology has evolved rapidly enough to overcome competition from contending technologies, such as rods, thin films, and plated wire. Today, however, many observers feel that core is finally yielding its preeminence in main memory to semiconductor storage, primarily to metal-oxide semiconductor (MOS) memories. In this area, however, transition continues to be gradual because core memories have been improved. Improvements are continuing, in manufacturing techniques, support electronics, and the designs that optimize these advances. Notable is the technological evolution of the memory core itself, in two main areas: size and material. Today's current standard core size is 18 mils outside diameter; some memories under development use 14-mil cores.

Reduction in core size has made possible greater performance, higher density, and reduced power. Smaller core diameters mean higher switching fields and hence faster switching, since core switching time is inversely proportional to switching fields. Smaller cores can be nested more densely, shortening drive lines and sense loops, which also reduces delays and improves memory performance.

Standard materials for cores over the past decade have been mixtures of magnesium-manganese (MgMn) and lithium (Li) ferrites; every manufacturer has its confidential formulation. These mixtures benefit from the low cost of the original MgMn material, developed in the 1950's, and from the wider temperature range of the later Li material, which is expensive, difficult to manufacture, and still requires temperature-compensated drive currents. With similar but somewhat increased compensation, MgMn-Li mixtures operate in systems satisfactorily over a temperature range of 0 to 50°C —better than that achieved with MgMn alone, but still not up to the 0 to 75°C range within which semiconductor drive circuits work.

The wider temperature range is needed in newer memory systems that lay out an entire array in one plane instead of in multiple stacked planes. One-plane layout, double-herringbone alignment of individual cores, use of smaller cores, and other factors all contribute to high core densities, that now exceed 3000 cores per square inch. Furthermore, as densities increased, capacity of individual "mats" also increased step-by-step over several years, from 4000 to 8000, 16,000, and even 32,000 cores. (These counts, more precisely, are all powers of 2,

rounded off here to the nearest thousand.) In the newest mats a single inhibit-sense wire in the 3-wire 3D organization threads all 32,000 cores and is connected to one driver-amplifier. (Eight such circuits would be necessary for the same capacity in 4000-core planes, which clearly demonstrates the economics of large planes.)

However, in use, systems tend to repeatedly address small clumps of locations within the array during a short span of time. Repeated switching of a single core generates heat, the energy represented by the area of the hysteresis loop; repeated switching of several cores near one another produces "hot spots" in the array. A more important contributor to hot spots is localized heating on adjacent electronic boards (eg, current drivers, etc). High component density on the boards and tight packing of boards make uniform cooling difficult. Current compensation is not very satisfactory in attaining reliable performance in such arrays, because compensation changes all drive currents even though temperature variation occurs in only a portion of a large array.

Thus, still newer materials became necessary—materials which would be more stable over a considerable operating range, would fit in the majority of design applications, and would not compromise performance. Such a material has been under development at Control Data Corp for several years; it is a refinement of the previous MgMn-Li mixture with certain proprietary additives. Criteria established for cores made from this material include

Compatibility—they should be compatible with the single 18-mil core type previously used in most designs

Ease of Assembly—their physical dimensions should allow stringing no more difficult than current 18-mil products

Quality—they should show no degradation of parameters, primary or secondary, compared with standard 18-mil cores

Performance—they should operate in a system over the 0 to 75°C temperature range without current compensation

Cost—they must be economically manufacturable, so that users do not have to pay a high premium for the improved performance

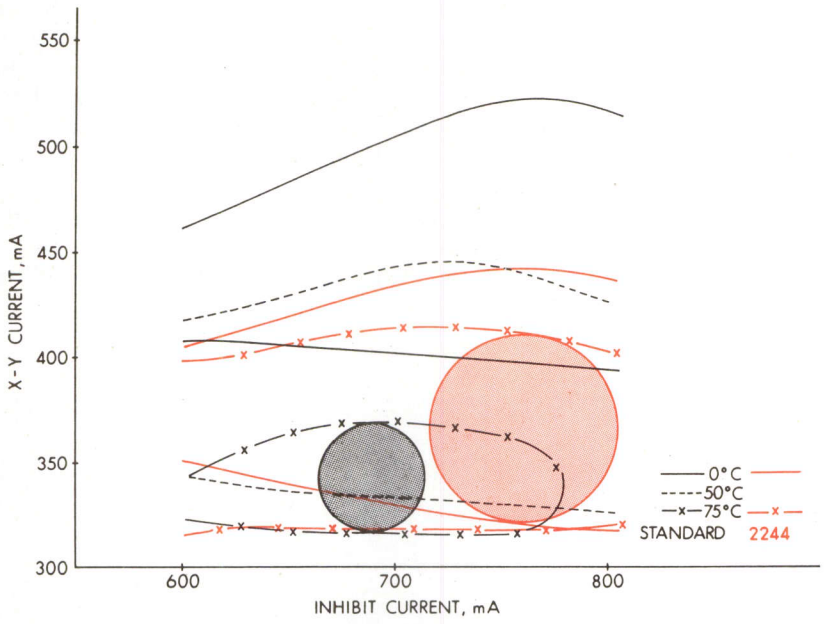
Unitemp 2244 memory cores meet these requirements with uniform drive currents under varying temperatures, and are equivalent to older formulations in all other respects (see Table 1). Secondary parameters are at least as good and in some instances better than those of the

TABLE 1

Comparison of Primary Parameters of Standard and Unitemp Memory Cores

		Standard Medium-Temp Cores			Unitemp 2244		
	Parameter	0°C	25°C	75°C	0°C	25°C	75°C
Drive Current	I_{r7} I_w (mA)	800	750	660	750	750	750
	I_{pr7} I_{pw} (mA)	500	485	400	460	485	450
	t_{r7} t_p (ns)	50	50	50	50	50	50
	t_d (ns)	300	300	300	300	300	300
Core Response	uV_1 max (mV)	58	58	58	60	60	60
	dV_1 min (mV)	39	39	39	39	39	42
	dV_s max (mV)	9	9	9	9	9	9
	t_p ±15 (ns)	115	115	115	115	115	105
	t_s max* (ns)	200	200	200	200	200	190
Dimensions	O.D.(in.)	0.0182 ±0.0005			0.0182 ±0.0005		
	I.D. (in.)	0.0118 ±0.0005			0.0118 ±0.0005		
	Height (in.)	0.0046 +0.0002 −0.0003			0.0046 +0.0002 −0.0003		

*Measured at 10-mV level on dV_1



Schmoo diagrams. System performance at 0 to 75°C for 32K x 18 systems with 8K sense lines is much improved with Unitemp 2244 (color), attained without current compensation, over standard cores (black) with current compensation. Of particular interest are the increased margins at 75°C

previous standard. For example, magnetostrictive characteristics (sensitivity to stress or force) are an order of magnitude better.

System current schmoo diagrams illustrate the desired system performance goal (see illustration); both are for a 32K x 18 system with an 8K sense line. Even with compensated drive currents for the old standard, performance at 75°C is much improved for the uncompensated 2244. Normal operating point for the system is the pair of currents represented by the center of the largest possible circle that can fit inside the schmoo diagram; the radius of this circle is the margin that the memory can tolerate in those currents without failing. When temperature variation causes the schmoo to migrate across the plot, or to change its shape, the margin for uncompensated currents is represented by the largest fixed circle that stays within the schmoo no matter where it goes; compensation for currents moves the center of the circle (the operating point) across the diagram in a line that ideally is straight and practically is as nearly straight as possible. Clearly the uncompensated margin for the 2244 is 60% larger than the compensated margins for the standard core.

Manufacturing processes for the 2244 are identical to those for standard magnetic technology products and initial production indicates no large differences in yield. Thus, cost will not prohibit wide usage.

The cores' uniform response under varying temperature conditions also characterizes the Unitemp 2230, which requires drive currents about 25% less. Other similar cores are also under development—one with parameters optimized for longer sense lines and one requiring a small drive current to meet low power system requirements.

In addition to performance-related core advancements, costs of manufacturing processes historically have been halved every three years. Furthermore, defects have been reduced from one bad core in 4000 five years ago to one in 20,000, so that average stringing time per bit has dropped; fewer repairs mean fewer solder connections and hence better reliability.

Today's cores are so uniform that test yields of 95% and up are common, and at least one manufacturer has proposed eliminating the 100% test of cores. Improved uniformity is also a key element in achieving longer sense lines. The number of cores which can be served by a single sense wire is determined by the delta noise (partially cancelled half-select noise) which precedes the strobing of the selected bit. The more cores per line, the higher this noise tends to be. Because the total noise is the sum of cancellations between pairs of cores, more uniform cores result in better cancellation and less noise.

Core improvements such as these have led to significant systems improvement. For example, both systems described in Table 2 employ 18-mil cores and represent typical available OEM systems, not speculations.

For special applications, particular parameters may be improved. For example, in a 16K x 18 system, 250-ns access can be achieved or, with a 32K x 36 system, even greater economy and density can be attained; a cost of 0.2 cent/bit is not unreasonable.

In the future, further increases in memory size and reductions in cost will be forthcoming in systems with 32K sense lines. Additional density increases of 25%, performance improvement, and power reduction will be attained with successful designs using 14-mil cores. Temperature-stable cores will be even more important for competitive performance.

The temperature-stable material may overcome one barrier facing designers who use 14-mil cores—ie, resistance heating in the smaller wire that is necessary to fit the reduced hole size. This heating can lead to temperature variations in addition to those caused by localized switching. Temperature-stable materials may help solve this problem.

Continued evolution of core may well extend the viability of core memory for a considerable period of time, depending on the relative progress of core memories and competitive technologies. The most prevalent competitor seems to be semiconductor memory; to achieve complete dominance of random access storage techniques, however, it must achieve these goals:

Standardization—stability and standardization of chip design to allow reliable second sourcing

Reliability—reliability of the devices within systems must be adequately demonstrated

Adequate testing—effective test procedures must be developed at all levels, derived from system performance data and field experience

Cost—reductions in cost must continue until it falls below that of competitive core systems

Nonvolatility—an economic solution to the problem of volatility must be found

Attaining these goals will require time; until then memory systems designers must consider the continually evolving core memory as a viable alternative. □

TABLE 2

Systems Improvement Achieved With Core Memory Technology

System Parameters	Specification 1974	1976
Configuration	8K x 18	32K x 18
Dimensions (in.)	11 x 14 x 1	15 x 17 x 1
Power	100 W	120 W
Cycle time	750 ns	750 ns
Access time	325 ns	325 ns
Operating range	0 to 55°C	0 to 75°C
Cost (in OEM quantity 100)	0.6 cent/bit	0.3 cent/bit
MTBF	20,000 h	20,000 h

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CIRCLE 47 ON INQUIRY CARD

APPLICATION NOTE

Programmable Interface Drivers Simplify Logic Testing

David T. Kan

Pulse Instruments Company
San Pedro, California

Testing complex logic components and systems need not require expensive and voluminous equipment; but simple signal drivers may not be adequate either. Proper drivers are neither complex nor expensive

In testing digital circuits and systems, high speed random logic signals with variable amplitude and level offset are required for simulating optimum and worst case drive conditions. Many of these signals must travel along transmission lines because only a few signal sources and receiving circuits can be located close together. For example, when measuring propagation delay of a multiple input integrated circuit, such as an 8-input multiplexer, 9-bit parity generator/checker, or 6-bit identity comparator, a large number of inputs are involved, so that it is physically impossible to connect all inputs to test signal sources with short leads. Another example is testing a high speed logic card inside an environmental chamber where temperature and other conditions are controlled. Test signal sources must be outside the chamber. In both cases, properly terminated transmission line connections are necessary to preserve high frequency characteristics of test signals which have variable amplitude and level offset to evaluate the circuits' behavior under different drive conditions.

Many dedicated interface drivers on the market are slow and cannot work through transmission lines. Only a few drivers for metal-oxide semiconductor (MOS) circuits have any level offset. Pulse generators are not suitable for random logic interface applications unless their timing control functions, such as period, delay, and width, can be bypassed—and in any case, in multichannel drive applications they would be uneconomical and cumbersome. Dedicated logic circuit testers are too expensive to use.

In spite of these problems, equipment manufacturers should have adequate test equipment for evaluating high speed digital circuits and systems. Without such equipment, large scale integration (LSI) and medium scale integration (MSI) circuits are tested either inadequately or not at all for dynamic characteristics before they are installed in systems. Consequently, defective or marginal components must be located in systems—a painfully time-consuming and costly task. Thus, high speed test equipment is necessary; and it can be built at reasonable cost using the proper interface drivers.

Rudimentary Test Circuit

A simple test system (Fig. 1) consists of a programmable 100-mA current source, an output switching network, and an input differential amplifier. Output current I_O is controlled by current I_P in the emitter of Q_1, and is approximately equal to $20I_P$. The switching network, controlled by the input differential amplifier, steers current either through resistors R_S and R_L or directly to offset return.

When V+ terminal of the amplifier is at least 400 mV more positive than V− terminal, the switching network directs I_O into R_S and R_L. Out-

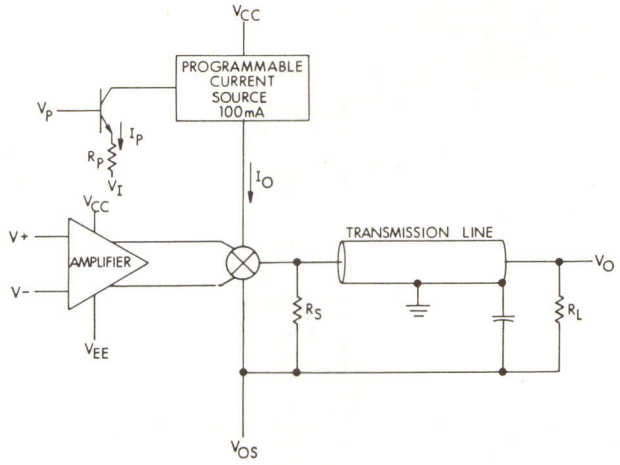

Fig. 1 Simple test system. Multiple connections like this can test high speed random logic, even though not all drivers can be close enough to the logic to obviate need for transmission lines

put is on, and output voltage is the sum of voltage drop across R_S in parallel with R_L plus offset voltage. It delivers maximum output current of 100 mA into a load biased between $V_{CC} - 20$ and $V_{CC} - 5$. Maximum attainable output high levels are $V_{CC} - 5$ at 100 mA and $V_{CC} - 1$ at 10 mA. With a 20-V supply, therefore, output swings of 15 V at 100 mA and 19 V at 10 mA are obtainable. Within this range, output impedance of the current source is equivalent to 5 kΩ in parallel with 10 pF.

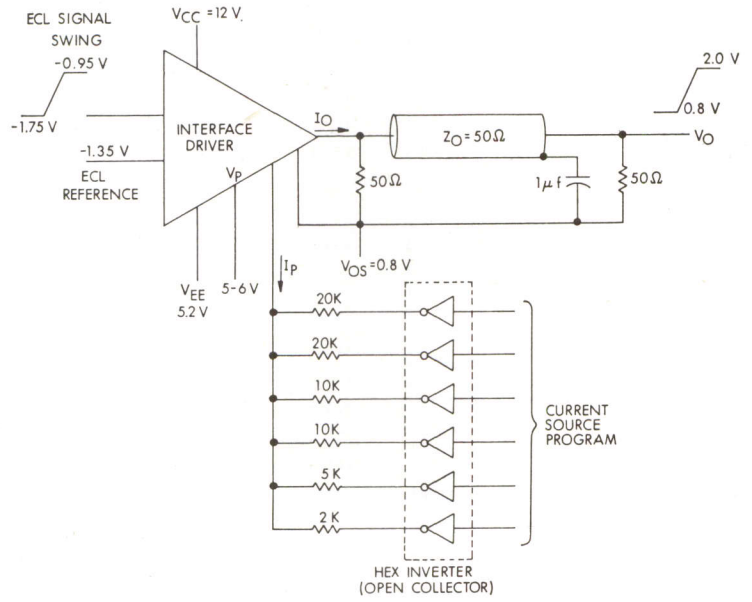

Fig. 2 ECL to TTL translator. Appropriate choice of levels and connections simplify testing of many other combinations—including choice of output amplitude through binary signals to hex inverter driving resistor network

With the more positive voltage applied to V−, no current is in the load, output is off, and output voltage is the same as offset voltage. Output is virtually an open circuit shunted by about 3 pF, and output leakage current is approximately 50 nA.

For optimum pulse response, input signal excursion should be limited at some point beyond the threshold level, but not too far beyond. For transistor-transistor logic (TTL) input signals, optimum response is obtained from the interface driver when the input high level is limited between 2.0 and 2.5 V.

In either on or off state, the offset voltage supply must sink a current equal to I_O plus approximately 35 mA. Other power supplies are conventional: V_{CC} is the usual positive voltage, between 10 and 20 V, while V_{EE} can be ground for TTL, negative voltage for emitter-coupled logic (ECL), or negative whenever the input threshold bias voltage is less than 1.5 V. For example, if the input signal varies from −0.5 to 0.5 V, the nondriven input pin should be biased at ground. This in turn requires V_{EE} to be −1.5 V or lower.

Adding a Cable

Unavoidable physical separation between test circuit and load requires a transmission line between the switching network and load, plus terminating resistors at one or both ends and possibly a bypass capacitor at the load end. Three common configurations of this type are ECL to TTL translator with matched terminations, TTL to MOS translator with source termination, and interstage dc amplifier with load termination.

High speed digital test signals are often generated by ECL devices such as counters, shift registers, and memories. The previously described test circuit can be applied to such signals as an ECL to TTL translator (Fig. 2). Resistance programming of output amplitude is possible by providing six different resistances for R_P in Fig. 1, connecting them to outputs of an open-collector hex inverter, and selecting one or more of the six by binary input to the inverter. Typical ECL input swing is −1.75 to −0.95

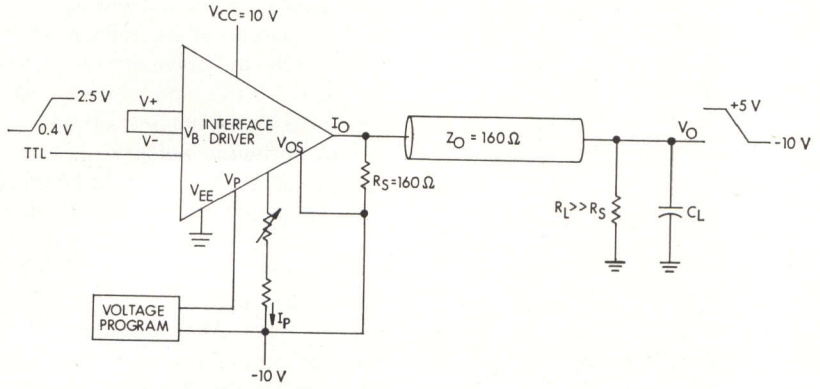

Fig. 3 TTL to MOS translator. No ill effects arise from terminating transmission line only at source; advantage is compact connectability of many cables at load end

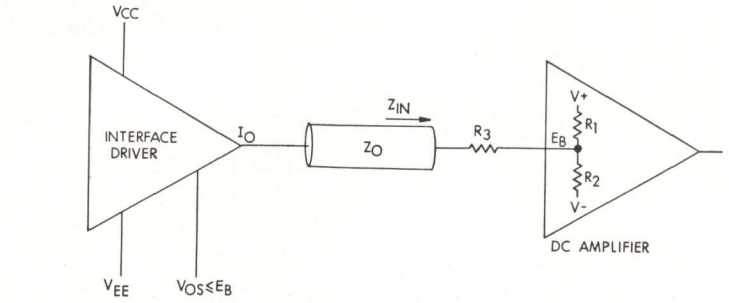

Fig. 4 Load termination. Series resistor R_3 often can nearly match line to load closely enough to minimize reflections in the line

V, symmetrical about a reference of −1.35 V with required threshold of 400 mV. Output swing of 0.8 to 2.0 V simulates worst-case drive conditions of a very small TTL swing with large offset. The transmission line has a characteristic impedance of 50 Ω, matched by 50-Ω resistances at both ends. Returning these to the same voltage reduces standby dissipation to zero, so that the resistors can have small power rating even when offset voltage is large. This is the most desirable configuration for the driver when fast, clean pulses are required. With this circuit, Schottky TTL J-K flip-flops have been tested at clock frequencies of over 80 MHz.

TTL to MOS translator with output swing from −10 to 5 V drives an n-channel silicon-gate shift register (Fig. 3). Since input impedance of the MOS device is capacitive with a very large parasitic resistive component, any fast signal will be reflected toward the source. However, if a resistive termination that matches cable impedance (160 Ω) is placed at the source, no multiple reflection will occur. This configuration offers the simplest interconnection between load and driver, since the connection from load end to offset voltage is unnecessary. With no discrete resistor at load end, it also enables compact connection of many cables in a small area, such as 22-pin socket; therefore, it is useful for probing integrated circuit wafers and hybrid circuit assemblies, where load end termination is seldom possible. By changing the values of V_{CC} from 10 to 20 V and of V_{OS} from −10 V to ground, the same circuit can drive CMOS devices.

In other applications, source terminated configuration is not desirable—as when testing an interstage dc amplifier (Fig. 4) with integral input bias network. Source termination would load the bias network, which together with the amplifier becomes the load termination. If this does not match the characteristic impedance of the cable, the absence of source termination will cause multiple reflections. However, matching often can be improved with a series resistor between the bias network and cable, modifying input impedance of the amplifier to be almost equal to the characteristic impedance of the cable.

Switching Time Measurements

To evaluate switching characteristics of current controlled devices such as diodes and bipolar transistors requires well-defined high speed current pulses. Since such pulses in general cannot be transmitted through coaxial cables or twisted pairs without changing their characteristics, an alternative approach is to transmit voltage pulses through the cable and to convert them to current pulses with a series resistor at the termination.

This approach is inefficient, especially in medium to high current applications. The requirement of high current pulse at low voltage often becomes much more difficult, as high power pulse is generated for the con-

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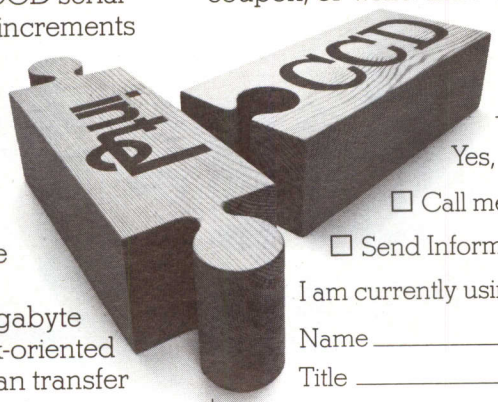

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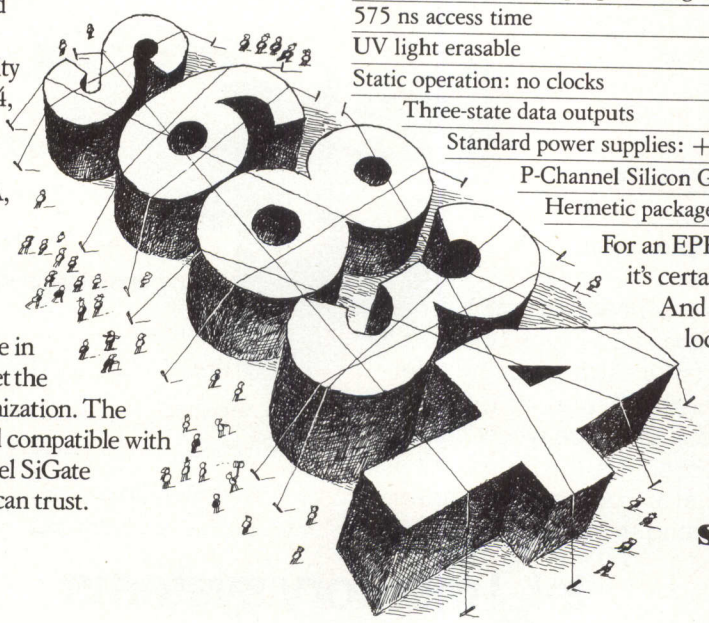

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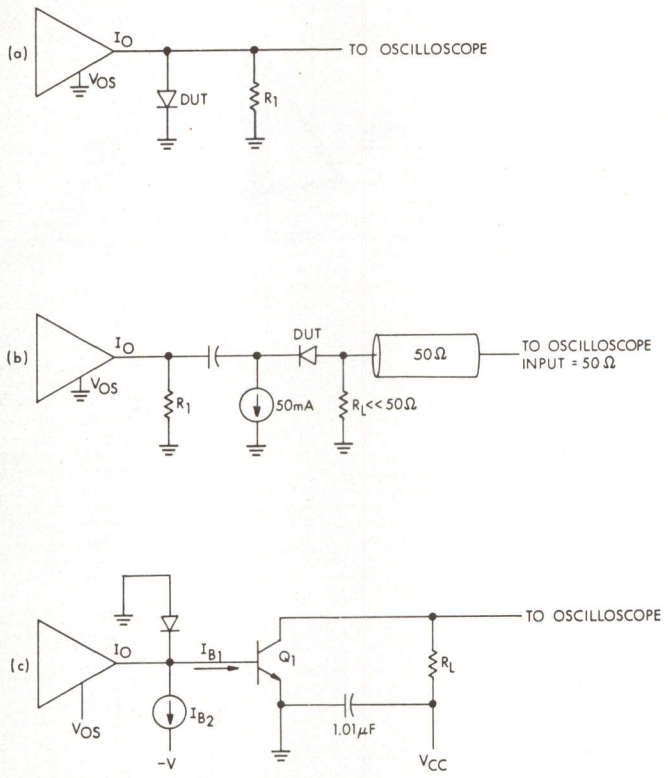

Fig. 5 Switching time measurements. Interface driver is useful in generating fast current pulses to measure (a) diode forward recovery time, as stored charge dissipates through R_1; (b) diode reverse recovery time (low value of R_L means less power dissipation and lower reverse voltage); or (c) turn on and turn off times of transistor. For pnp transistor the same configuration would work, except diode would be reversed

version. Furthermore, when the device under test (DUT) is nonlinear, such as a diode, impedance matching and hence generating an accurate current pulse are difficult.

In these applications, a physically small high speed current source can be placed close to the device under test as a transmission line receiver. Low voltage pulse is transmitted through a terminated coaxial cable to the input of the current source, turning it on, and injecting current pulse into the DUT. Neither high amplitude voltage pulses nor impedance matching at the current-source output is required. Rise time of short circuit current is about 1.5 ns. Some practical examples appear in Fig. 5.

Conclusion

Since most commercially available digital signal and pulse generators are not suitable to drive both bipolar and MOS devices or to use in random logic interface applications, the interface driver fills an important gap in these testing applications. Furthermore, it offers drive capabilities of a high performance pulse generator at the cost and size of a component; it therefore provides a low-cost alternative for building high speed test equipment. □

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MM5281* (22-pin)	250 ns	400 ns	510 ns

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TECH BRIEF

Generation Of Key In Cryptographic System For Secure Communications

A number of general-purpose digital computers are used for gathering, categorizing, and storing confidential data. When these data are transmitted to a remotely located terminal, unauthorized access to it may be prohibited by using cryptographic encipherment. Encipherment with a particular key is illustrated as

```
Sequence: 0 1 1 0 1 0 1 1 1 1 0 1 1 0 0
     Key: 1 1 1 1 0 1 0 1 1 0 0 1 0 0 0
  Cipher: 1 0 0 1 1 1 1 0 0 1 0 0 1 0 0
```

Transformation consists of a bit-by-bit modulo-2 sum (ie, exclusive-OR) of the data sequence with the key.

An authorized user would have *a priori* knowledge of the key and of the corresponding inverse transformation. Thus deciphering proceeds as

```
  Cipher: 1 0 0 1 1 1 1 0 0 1 0 0 1 0 0
     Key: 1 1 1 1 0 1 0 1 1 0 0 1 0 0 0
Sequence: 0 1 1 0 1 0 1 1 1 1 0 1 1 0 0
```

Decipherment involves an inverse transformation whereby the key is subtracted bit-by-bit modulo 2 from the cipher, yielding the data sequence.

The cipher described is known as the Vigenère cipher. A Vigenère cipher with a key of unlimited length (ie, nonrepeating) is called a Vernam system.

A report has been published which discusses key generation for the Vigenère, the compound Vigenère (where two or more combined sequences comprise the key), and the Vernam systems, using feedback shift registers (FSRs). The report discusses theoretical considerations necessary for key generation. One major topic includes binary FSRs, particularly nonsingular FSRs. Key sequences are generated using nonsingular FSRs, which are determined from factors of de Bruijn graphs of order r. A section of the report is devoted to linear feedback shift registers (LFSRs) and their role in generating binary sequences. These are compared with nonlinear FSRs.

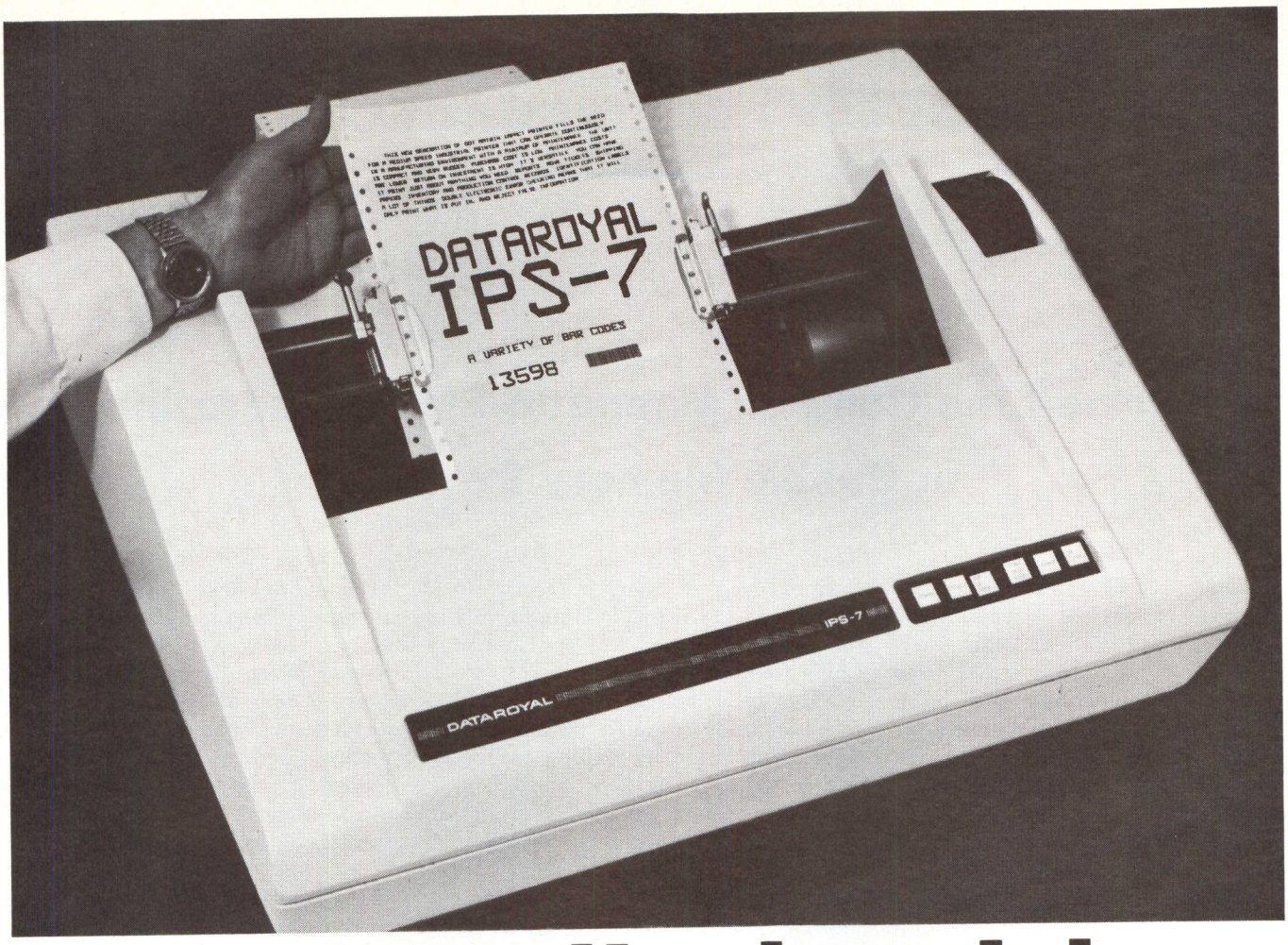
A number of feedback functions are discussed for generation of long key sequences, which can be split and then rejoined to create additional nonrepetitive sequences. The report includes a number of examples. Projections for future work are also discussed.

Note

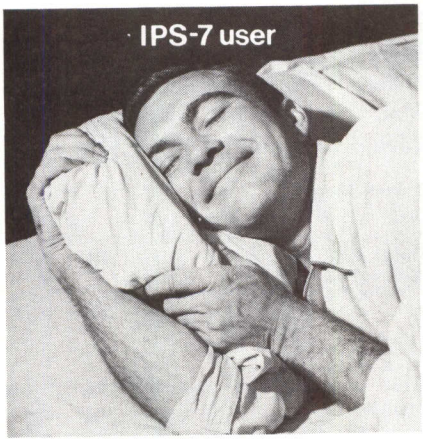
Requests for further information may be directed to Technology Utilization Officer, NASA Pasadena Office, 4800 Oak Grove Dr, Pasadena, CA 91103. Reference: TSP75-10278.

Patent Status

This invention has been patented by NASA (U.S. Patent No. 3,911,330). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to Patent Counsel, NASA Pasadena Office, 4800 Oak Grove Dr. Pasadena, CA 91103. Source: Marvin Perlman of Caltech/JPL (NPO-13451).



the alternative to printers that break down in the middle of the night!



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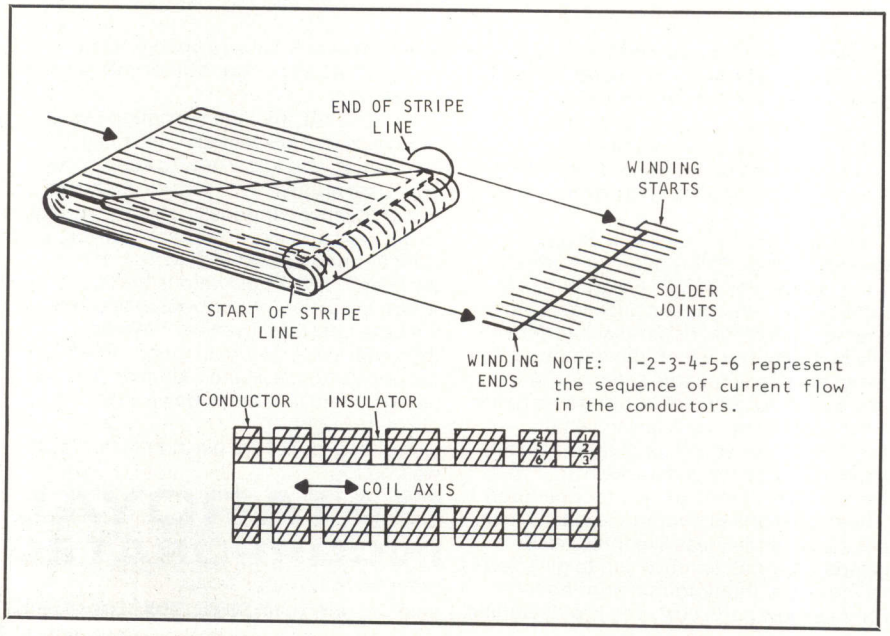
TECH BRIEF

Stripe-Line Coil For Magnetic-Field Generation In Bubble Memory Devices

An improved coil for magnetic bubble memory devices consists of a stripe-line coil pattern with varying widths of conductor etched from a conductive film supported on a polyamide film. The multiple-layer stripe-line coil has conductors in series along the layer direction, rather than in the axial direction, which minimizes potential differences. The stripe-line layer is wrapped around a fixed coil form, and the outer ends of the conductors are connected electrically as a single loop to form a field coil (see illustration). Conductor length, width, and spacing are controlled by the etched pattern, resulting in coil parameters, such as size, shape, and the like, with less variation from run to run than in wire-wound coils. The stripe-line coil arrangement is simpler, easier to wind, and has better field uniformity inside the coil and less coil loss at high frequency operation.

The printed-circuit magnetic-field coil is produced on a flexible conductor substrate by etching the desired stripe-line pattern on a conductor foil supported on an insulating film. Preferably, this consists of cold-rolled copper on a polyamide film. Photolithographic techniques provide one method of forming the stripe-line pattern of the conductor layer. The copper surface is coated with a thin layer of light-sensitive photoresist, which is exposed to light through a photomaster with the desired stripe-line design. The conductor material is then developed and etched to produce the pattern.

The multiple-layer stripe-line coil structure substantially reduces the high frequency loss in two ways. First, sufficient spacing between layers or columns of conductors can be provided to reduce the interwire coupling, and secondly, with the winding in the coil connected in series, the current will flow through adjacent vertical arrays or columns of conductors. This winding arrangement minimizes potential differences between neighboring turns, thereby minimizing high frequency loss due to interwire coupling. The arrangement also helps to minimize unequal current distribution at high frequencies which occurs in coils with parallel-wound layers. Effective turns in this winding scheme can be controlled by varying the conductor width. (Increasing the width decreases the number of turns.)



Note

Requests for further information may be directed to Technology Utilization Officer, Langley Research Center, Mail Stop 139-A, Hampton, VA 23665. Reference: B75-10195.

Patent Status

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the Rockwell International Corp, Anaheim, CA 92803. Source: Thomas T. Chen and John E. Ypma of Rockwell International Corp (LAR-11705).

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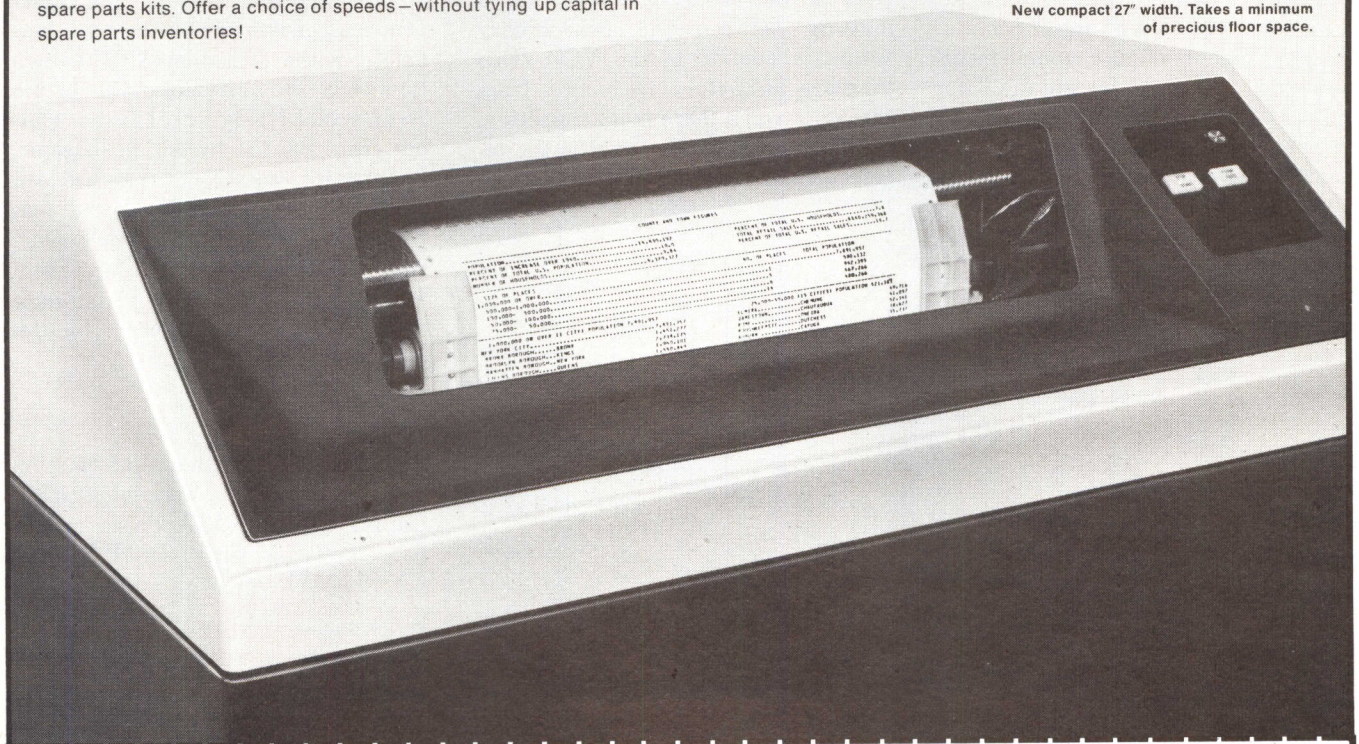

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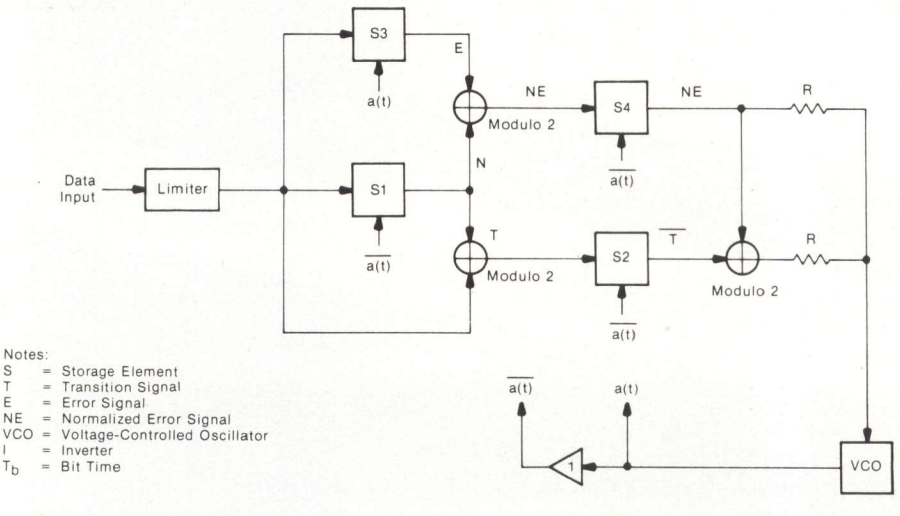
TECH BRIEF

Synchronizer For Random Binary Data

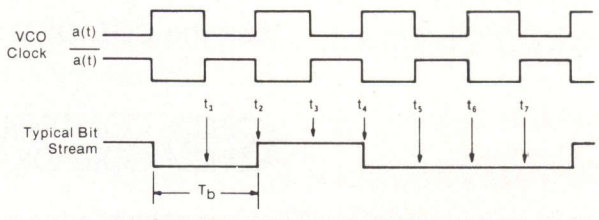
A simplified binary-data transition detector, for synchronization of relatively noise-free signals, can be used with radio or cable data-control links. It permits reception of binary data in the absence of a clock signal or a self-clocking coder. The detector includes a phase-locked loop (PLL) and a voltage-controlled oscillator (VCO) to reconstruct the data clock rate at the receiver.

The detector loop, shown in the diagram, incorporates a VCO which generates a squarewave output at twice the frequency of the incoming bit rate. The true and complement outputs at $a(t)$ and $\overline{a(t)}$ are the data transition sample pulse and the mid-bit sample pulse, respectively. When the PLL is in lock, the leading edge of timing signal $a(t)$ occurs at the bit transition, and the leading edge of timing signal $\overline{a(t)}$ occurs mid-bit.

The leading edge of timing signal $a(t)$ is used to sample input data to determine the sign of the present phase error and to derive the error signal. The leading edge of timing signal $\overline{a(t)}$ is used to sample input data to determine whether or not a transition occurred. If a transition occurred, a binary-valued error voltage is applied to the VCO. If a transition did not occur, a voltage that is midway between the two binary values is applied to the VCO. This provides an output frequency from the VCO, when there is no transition, that is approximately equal to the received data rate.



Notes:
S = Storage Element
T = Transition Signal
E = Error Signal
NE = Normalized Error Signal
VCO = Voltage-Controlled Oscillator
I = Inverter
T_b = Bit Time



System Block Diagram and Sample Timing

Storage is required as follows (see sample timing under diagram): Time t_1 is the point in time where data is first sampled and then stored in storage element S1. At time t_3 data stored is added modulo-2 to present data and is stored in S2. Output from S2 then indicates whether a data transition occurred at time t_2. At time t_2 data is sampled and stored in S3. Output from S3 is added modulo-2 to output from S1 which serves as the normalizing term N.

This addition assures the independence of the sign of the error signal from the direction of the transition. At t_3 the normalized sign of the error signal NE is stored in S4. Output from S2, the transition detector, remains for one full bit time between t_3 and t_5. Output from S4, the sign of the error signal, remains for the same length of time. Data are eventually clocked into a serial-input shift register (not shown) for receiver processing.

Note

Requests for further information may be directed to Technology Utilization Officer, NASA Pasadena Office, 4800 Oak Grove Dr, Pasadena, CA 91103. Reference: TSP75-10325.

Patent Status

NASA has decided not to apply for a patent. Source: Tage O. Anderson, Jack K. Holmes, and William J. Hurd of Caltech/JPL (NPO-13286).

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Microcomputer Interfacing: The Substitution of Software for Hardware

Peter R. Rony
Virginia Polytechnic Institute & State University

David G. Larsen
Virginia Polytechnic Institute & State University

Jonathan A. Titus
Tychon, Inc

Readers who follow the current literature on microcomputers frequently encounter phrases such as "hardware/software tradeoffs" or "substitution of software for hardware," which are indicative of anticipated microcomputer applications in the near future, and which do much to explain why industry is so excited about them. In this month's column, we will discuss how to "substitute" microcomputer software for hardware.

First let us recall the definitions:

Hardware—mechanical, magnetic, electronic, electromechanical, and electrical devices from which a system is fabricated

Software—totality of programs and routines used to extend capabilities of computers, such as compilers, assemblers, narrators, routines, and subroutines[1]

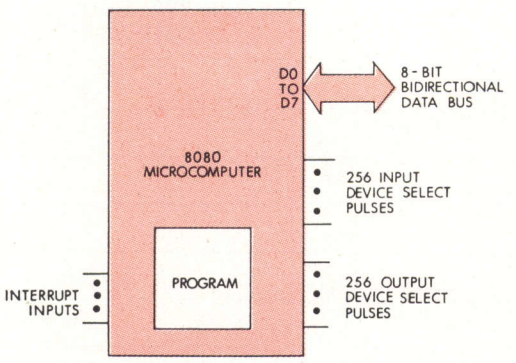
In this case, software represents the machine-language program stored within the memory of a microcomputer, and hardware represents specific devices that store, manipulate, receive, or transmit digital information. Included in the definition of hardware is the microcomputer itself. The basic point can be simply stated:

Through skillful programming, it is possible to substitute machine-level routines and subroutines for specific hardware devices that store, manipulate, transmit, or receive digital information. This activity is called "the substitution of software for hardware."

Typical hardware that is replaced includes knobs, buttons, pulsers, switches, logic switches, clocks, and small memories. Still others are TTL IC chips that perform digital functions such as debouncing, sequencing, shifting, adding, subtracting comparing, and logic operations on multibit digital words. Hardware that is usually not replaced includes simple TTL chips such as inverters, flip-flops, gates, latches, 3-state buffers, and counters.

Basic "tools" used in substitution of software for hardware (Figure) are

(1) Programming



Basic microcomputer "tools" required for substitution of hardware by software

(2) Use of synchronized data appearing on bidirectional 8-bit data bus, D0 through D7

(3) Input and output synchronizing pulses called device-select pulses

(4) Interrupts to the microcomputer

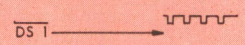
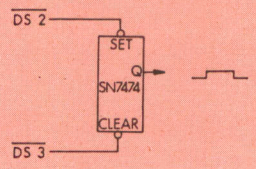
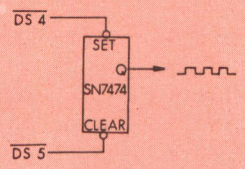
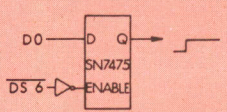
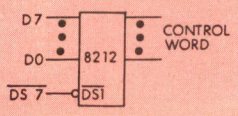
In an 8080-based microcomputer, 256 input and 256 output synchronizing pulses can be generated. If more pulses are needed, memory I/O techniques can always be used, as discussed in last month's column. An unlimited number of synchronizing pulses are therefore available to coordinate behavior of almost any type of digital electronic circuit. As software is substituted for hardware, the main tradeoff will be speed of operation. It is useful to remember that in substitution of software for hardware, the key tradeoff is speed of operation. Execution of any computer instruction takes time; therefore, the more instructions that are used, the longer it takes to execute them. This tradeoff is not as serious as it may seem. Present 8-bit microcomputers are very fast, and future microcomputers will be at least ten times faster. By digital electronic standards, the majority of existing electromechanical machines are slow. Human senses cannot participate in activities that require millisecond time resolutions, ie, in an I/O sense, humans are very slow machines.

The Table summarizes some commonly encountered situations in which hardware items such as debounced pulsers, switches, logic switches, and clocks are replaced by simple wire connections, latches, flip-flops, and inverters. Abbreviated versions of the required software are given. Ref. 2 or previous columns provide details on generation of OUT n pulses, where n is an octal number ranging between 000_8 and 377_8. "Timing loop" is a short microcomputer subroutine that generates precise time delay, typically >100 μs. As seen in the Table, replacement can be accomplished in most cases by use of one or two different device-select pulses. A pair of OUT n instructions that bracket a timing loop are sufficient, when applied to SN7474 flip-flop, to produce monostable pulse of precise time duration. Addition of a second timing loop and jump instruction, JMP, changes output of the flip-flop to that of a variable duty-cycle clock; duty cycle is controlled by relative time delays of two timing loops.

Of particular interest is entry f in the Table, in which an 8-position mechanical switch or eight individual mechanical switches are replaced by an 8-bit control word that is strobed into an 8212 chip from the accumulator with the aid of a device-select pulse. This control word is latched by such an action, and subsequently can influence behavior of a rather sophisticated digital circuit. The chip therefore functions as control register for the circuit. This principle is being widely used in a group of interface chips that reduce number of wire connections needed between a microcomputer and external device. The 8255 programmable peripheral interface chip described in last month's column is included in this category.

Only a few examples of how hardware can be replaced by simple software with aid of device-select pulses are provided in the Table. Omitted are more obvious hardware substitutions: arithmetic logic units (SN74181), digital comparators (SN7485), and shift registers (SN74194, SN74198, SN74199). Such chips are replaced by microcomputer instructions that add, subtract, compare, and shift 8-bit contents of the accumulator register.

Some Uses for Device-Select Pulses In Substitution of Hardware by Software

SUBSTITUTED HARDWARE FUNCTION	NEW HARDWARE CIRCUIT	SOFTWARE EMPLOYED
(a) PULSER, 500 ns MONOSTABLE		OUT 0
(b) LOW DUTY-CYCLE CLOCK (500 ns PULSES)		OUT 1 TIMING LOOP JMP
(c) DEBOUNCED PULSER, MONOSTABLE, LOGIC SWITCH		OUT 2 TIMING LOOP OUT 3
(d) VARIABLE DUTY-CYCLE CLOCK		OUT 4 TIMING LOOP OUT 5 TIMING LOOP JMP
(e) ONE BIT OF CONTROL INFORMATION FROM MECHANICAL SWITCH		MVI A CTRL OUT 6
(f) EIGHT BITS OF CONTROL INFORMATION FROM SET OF EIGHT MECHANICAL SWITCHES		MVI A CTRL OUT 7

References

1. *Microprogramming Handbook*, Microdata Corp, Santa Ana, Calif, 1971
2. *Bugbook III. Microcomputer Interfacing Experiments Using the Mark 80® Microcomputer, an 8080 System*, E & L Instruments, Inc, Derby, Conn, 1975

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

CPU and Support Products Expand μComputer Line

Nineteen products, providing improved cost/performance microprocessors as well as I/O devices and memories that enhance total system capabilities at low cost, are available from NEC Microcomputers, Inc, 5 Militia Dr, Lexington, MA 02173. These include two 8080A central processing units, eight support chips, seven memory products, and two controllers. Some are available from inventory; all will be available in production quantities by the end of the third quarter this year.

Full support through documentation, a time-sharing service for software development, and a self-contained microcomputer system for program development which includes programming capability for EEPROM are also provided. Products are pin and software compatible with other companies' products.

8080A Microprocessors

Two high-performance microprocessors, the uPD8080A-2 and the uPD8080A-1 are, respectively, 25 and 50% faster than the company's standard 8080A processor. The -2 has a clock frequency of 2.5 MHz, while the -1 has a 3.0-MHz frequency. Main features are BCD subtraction as well as addition capability, and register-to-register move instruction time of four clock periods, 20% faster than other 8080A processors. Both processors are n-channel, 8-bit parallel units with TTL compatibility. Standard features include 78-instruction repertoire, software and pin compatibility with other processors, multibyte interrupt handling, and automatic stack operation with 16-bit stack pointer.

Upon interrupt, an instruction of three bytes can be accepted; a call instruction can be inserted so that any address in memory can be a starting location for an interrupt handling routine. Each interrupt operation has a separate location; as a result, no polling is required to determine the kind of interrupt. Decimal adjust accumulator instruction operates correctly after subtraction, as well as after addition, so that BCD subtraction can be performed at the same speed as BCD addition, without a special subroutine.

Peripheral Chips and UART

Three support circuits for use in 8080A microprocessor applications are the uPD8212D, an 8-bit I/O port; the uPD8216D, a bidirectional 4-bit bus driver; and the uPD369D/C, a fast programmable universal asynchronous receiver/transmitter (UART). Compatible with Intel products, the two chips provide users with an alternative source for these products.

The 8-bit I/O port is a versatile device with multi-mode operational characteristics for implementing latches, gated buffers, and multiplexers, the principal peripheral and I/O functions of a microcomputer system. I/O port features fully parallel 8-bit data register and buffer, 3-state outputs, service request flip-flop for interrupt generation, asynchronous register clear, and low input load current of 0.25 mA max. Operating from 5-V supply, it is housed in a 24-pin package.

Designed to buffer microcomputer system components, the 4-bit bidirectional bus driver features two separate 3-state buffers on each of four lines, with TTL compatibility on one side for interfacing to system components, and high voltage output drive (3.65 V) on the other side for direct interfacing to the CPU. Device operates from single 5-V supply, and comes in ceramic 16-pin DIP.

Functionally identical to the 1602, the UART has the advantage of operating at transmission speeds up to 50K baud; receiver margins are 43% at that range. The unit uses n-channel aluminum gate MOS technology. It is externally programmable to control word length, odd/even parity generation/verification, parity inhibition, and data word format. I/O is DTL/TTL compatible. Operating from standard n-MOS power supplies of 12, 5, and −5 V, UART is packaged in either a 42-pin ceramic or plastic DIP.

Additional support chips include uPB8224D, 16-pin single chip clock generator and driver; uPB8228D/38D, 24-pin system controller and bus driver; uPD8251C, 28-pin universal synchronous/asynchronous receiver-transmitter; uPD8255C, 40-pin programmable parallel I/O port; and uPB8214D, 24-pin priority interrupt control unit.

Large Capacity EEPROM

Capable of being erased electrically, the 1K-word x 8-bit EEPROM (uPD458D) is four times larger than its companion 256-word x 8-bit EEPROM (uPD454D). With high reliability and long life, the EEPROM is functionally compatible and similar in size to other p/ROMs. Less power for programming and erasing operations is required. Maximum access time of the n-channel, silicon gate device is 450 ns.

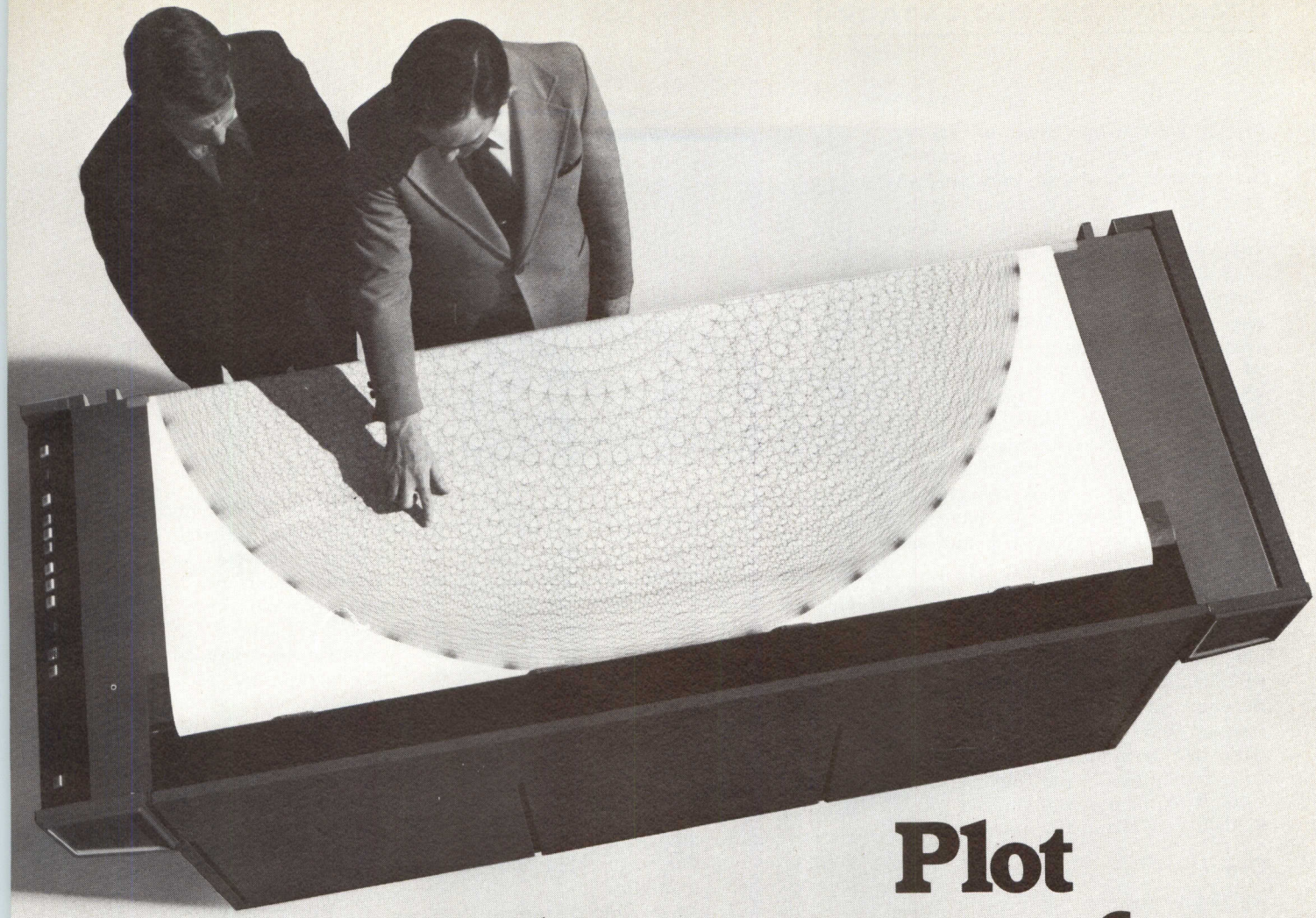
Compatible with 2708 type ultraviolet erasable 8K p/ROMs, EEPROM has four extra pins on one end for erasure voltages; 24 pins used for addressing and data are the same for both types, permitting use of either without board modification or program changes. Electrical erasability allows the device to remain in the system while data are erased, or written. More programming changes are accommodated with this unit than with others.

Applications include developing microcomputer systems, checking and debugging software for later use in masked ROM, and use in systems requiring standby memory for emergency storage of data in case of power failure. Typical program write time is 30 s and requires 26 V. Erase time is 60 s and requires 36 and −40 V. Power requirements are approximately 0.25 W. Other features include nonvolatile storage, TTL-compatible I/O for read and program operations; 3-state outputs; and power supply voltages of 12 and 5 in ROM mode. Device is contained in 28-pin ceramic DIP.

Other available ROMs are uPD2308D, a 1024 x 8 n-MOS, and uPD2316AD, a 2048 x 8 n-MOS, both with 450-ns access times.

RAM Chip Families

Three families of high speed, low cost R/W memories (uPD2101ALC, uPD2102ALC, and uPD2111ALC) are fabricated using n-channel MOS silicon gate process for contamination protection. They require 5-V supply only and use depletion mode loads. Also available is a complementary MOS R/W memory (uPD5101C-E) which is a 22-pin ultra low power static CMOS device organized 256 x 4 with access time of 1 μs. I/O is directly TTL compatible. Data are read out nondestructively and have the same polarity as the input data. With separate I/O data terminals, device is suited for low power applications in



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which battery operation, or battery backup for nonvolatility, is required. In standby, it draws only 10 μA from single 2- to 3-V power supply.

The uPD2101ALC family of 22-pin fully decoded static RAMs is organized 256 x 4, has separate data I/O terminals, and is pin compatible with the CMOS device. With full TTL compatibility, it features access times of 250, 350, and 450 ns. A single chip-enable ($\overline{CE}$) pin is provided for selection of an individual device in systems with bused outputs. In standby mode, with power lowered to 1.5 V, power dissipation is reduced to 42 mW max. Output data have the same polarity as input data, and are read out nondestructively.

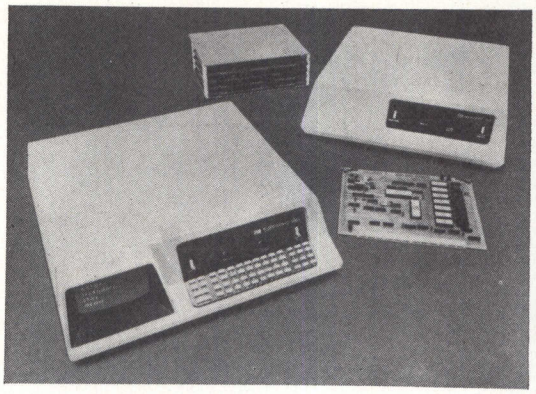
Available with the same access times, chip-enable pin, I/O polarity, and power supply characteristics are the other two families. The uPD2102ALC family of 16-pin fully decoded static R/W memories is organized 1024 x 1, and has separate data I/O terminals. The uPD2111-ALC family has 18-pin fully decoded static R/W memories, organized 256 x 4; data I/O terminals are common.

Controllers

An 8-bit bus compatible magnetic tape cassette controller of n-channel MOS technology, uPD371D controls up to two cassette tape drives in an 8080A microcomputer system; uPD372D, a flexible disc controller of n-MOS technology, is compatible with IBM 3740 flexible disc drives, and can control up to four drive units in an 8080A system.

Modular μComputer Line Developed to Meet Industrial Control Needs

PCS 180 family, a line of industrial microcomputers, is designed using CMOS and other low power logic technologies to keep power dissipation to a minimum. An additional advantage is that CMOS provides noise immunity for industrial applications. To ensure that high and low speed peripherals can be interfaced with a high degree of bus efficiency, the 180 systems use 3-state bus logic. Expandable to meet changing industrial requirements, the series can be altered or added to without rewiring or shutdown.



Family of microcomputers designed for systems use in noisy, corrosive, industrial environments contains SuperPac 180, MicroPac 180, and the 1810 and 1806 single board microcomputers, also available with 4-slot chassis

The developer, Process Computer Systems, Inc, 5467 Hill 23 Dr, Flint, MI 48507, feels that SuperPac 180, the advanced component of the line, may be the first packaged, general-purpose microcomputer system offered to the industrial market. Containing full ASCII keyboard and CRT display capability in a single low-cost package, it includes the PCS 1806 microcomputer. Unit has display memory, character generation, timing, and video electronics; it provides 16 lines of 16 or 64 characters, 1024 directly addressable character locations, programmable cursor, blink, and reverse video capabilities.

A low-cost, rack-mountable industrial microcomputer system, MicroPac 180 includes an 1806 microcomputer, plus 4-slot chassis, power supply, and industrial front panel with on/off switch and status indicators. Also included in the 180 family is the 1810, a single-board microcomputer which includes power fail/auto restart and battery backup that can support 256 bytes of CMOS RAM (expandable to 1K bytes) for up to 10 days. Based on the 8080A microprocessor, the 1810 also includes crystal-controlled clock; 16 3- to 30-V digital inputs; 16 30-V, 500-mA digital outputs; RS-232/20-mA current loop serial port; external interrupt; five interval timers; provisions for 3K bytes of EROM/ROM; and DMA capability. System can be expanded by addition of memory and I/O, as well as peripheral and communications options. It also may be used in the SuperPac 180 or the MicroPac 180 configuration.

Available for applications where battery backup is not important and where more memory is required on a single board is the 1806 microcomputer. With 1K-byte RAM, provision for 7K EROM/ROM, eight TTL inputs and eight outputs, it is otherwise similar to the 1810. Both the 1806 and 1810 will be offered with a basic 4-slot chassis and power supply for low-end, low-cost applications. Easily mounted in an OEM system, it will be a basic microcomputer system with I/O modules to be added by the user as needed. Eight- and 20-slot chassis versions also are available.

Circle 170 on Inquiry Card

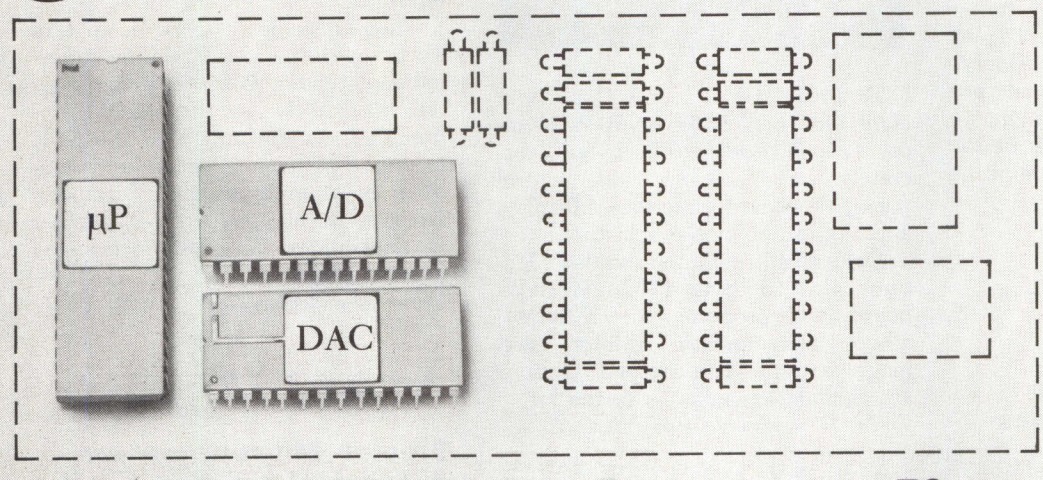
Microcomputer Based on F8 Microprocessor Is Small, Complete Unit

Claimed by Pronetics Corp, Div of Electronic Packaging, Inc, 6431 Preston Crest, Dallas, TX 75230 to be the smallest, complete 8-bit microcomputer, PS-810 comes fully assembled and tested with instruction cycle time of 2 μs. Unit contains F8 microprocessor, 1K-byte R/W memory, 1K-byte firmware, and 32 bidirectional latched and TTL-compatible I/O ports.

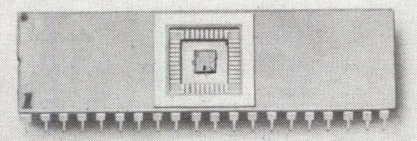
Two independent external interrupt inputs enable response to external asynchronous events, while two independently programmable interval timers provide real-time capacity. Clock frequency is controlled by a 2-MHz crystal. Other features include over 76 instructions, 64 R/W memory scratchpad registers on CPU, indirect addressing modes, automatic power-on reset, and standard 4½ x 6½" board. A 1K-byte resident monitor-debug program provides I/O utility subroutines, memory loading, dumping, and debug capability to aid in program development.

(Continued on p 126)

A lot of microprocessor users wish their analog interface problems would go away.



We made them disappear.



With our monolithic CMOS converters.

10- and 13-bit A/D converters with tri-state output logic that gets you directly onto the microprocessor data bus. And our 10-bit D/A converter with double-buffered inputs direct from the microprocessor. And each communicates in two bytes: the 8 LSB's, and the remaining MSB's.

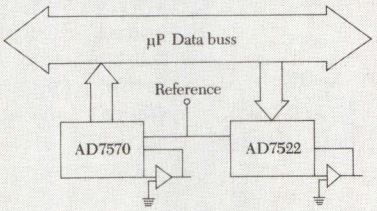
Our AD7550, industry's newest and most accurate monolithic CMOS A/D converter, uses a patented (Analog Devices U.S. Patent No. 3872466) "quad slope" conversion technique to provide 13-bit accuracy, 1 ppm/°C offset and gain drifts, and has its own amplifier, comparator, clock and digital logic.

Our AD7570 is a monolithic CMOS 10-bit successive approximation A/D converter with ratiometric operation and only 20mW of dissipation. Parallel and serial outputs with 20μs conversion time provide excellent application flexibility.

Our AD7522 is a monolithic CMOS multiplying, 10-bit DAC. It's the only such device available with double buffered inputs that can be loaded in parallel or serial mode. Low dissipation, very low feedthrough and drifts of only 1 ppm/°C complement the interface handshaking routine for maximum flexibility and optimum performance.

These I/O peripherals, the AD7550, AD7570 and AD7522 data converters are your only real solutions for interfacing a microprocessor to the analog world.

And these are just three of a complete line of more than 20 IC converters that make a lot of your conversion problems disappear. For more information, write Analog Devices, the real company in precision measurement and control.



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CIRCLE 53 ON INQUIRY CARD

Four 8-bit I/O ports are available on two 16-pin DIP sockets for connection through flexible flat cable to peripherals, displays, and relays. Onboard flexible data terminal interface connects to any terminal; when data terminal interface connector is removed, full use of all 32 I/O lines is obtained.

All necessary microprocessor functions are available on a dual 22-pin edge connector to permit memory expansion. A 4K-byte universal p/ROM board, 4K-byte R/W memory board, and cassette mag tape interface board are offered to accomplish this expansion.

Circle 171 on Inquiry Card

Arithmetic Software Package Designed for μComputer Applications

Designed for use with the Intel 4040 microcomputer, program requires only 512 memory locations of 8 bits, and performs algebraic addition, subtraction, multiplication, and division of a decimal number of up to 16 digits. Simple subroutine addressing instruction enables each arithmetic function. Program is intended for numerical controllers, process controllers, and other microcomputer applications involving arithmetic calculations. Available from Leuven Research & Development—M.I.D., Groot Begijnhof, Benedenstraat 59, B-3000 Leuven, Belgium, the package contains a set of two programmed 1702 p/ROMs.

Circle 172 on Inquiry Card

Keyboard System Can Enter Languages Without Extra Interface Equipment

Designed by Diversified Technology, PO Box 213, Ridgeland, MI 39157, Cosmos microcomputer features KeyTop programming keyboard which allows ASCII and assembly language to be entered without additional interface equipment. Other features include bus-oriented design, and low power CMOS technology which facilitates battery operation.

Unit is available either complete or in a kit which contains an RCA

CDP 1801C CPU, four I/O ports of eight bits each, 256-byte R/W memory (expandable to 64K bytes), discretely variable clock with control panel, keyboard interface, display, and 11-position motherboard.

Deluxe unit contains standard features plus 256-byte 1702A EPROM board (with provisions for 1K bytes), 20-col alphanumeric printer, and magnetic tape data storage. Options are available as add-ons to the kit.

Circle 173 on Inquiry Card

Resident Assembler Provides Complete Programming Facility

Developed for Intel's 8080-based system design kit (SDK) microcomputer, assembler is self-hosted rather than cross-assembler; it runs directly on the microcomputer for which source code is written. Source language is fully compatible with existing assemblers, but without macros. Source statements additionally can contain complex expressions, including nested parentheses, and arithmetic and logical operators. Conditional assembly enables easy control when a variety of software versions is required. Relocatable object code and self-contained relocatable loader permit programs to be loaded anywhere (all address references are corrected).

One-pass operation, in addition to the normal two or three, permits final object program to be created in a single reading of source code. In 2-pass assemblies, all statements in error are printed separately during pass one, allowing the user to determine the extent of any errors without obtaining a complete listing. Object code may optionally be assembled directly in memory, enabling assembled program to be executed immediately. Other output options include side-by-side source and object listing, and object code stored on magnetic or paper tape.

Another feature is full range of error diagnostics, which includes capability to detect symbol table overflow. It occupies less than 4K bytes of storage, and the object code produced can be run on any 8080-based microcomputer. Printed output also includes the symbol table listing, a sorted list of all labels, and their values. Any undefined or unreferenced symbols are flagged for easy reference.

The developer, Microcomputer Technique, Inc, 1120 Reston International Center, Office Building, Reston, VA 22091, says the p/ROM programmer can be added to the SDK to create permanent copies of assembled programs, providing complete facilities at minimal cost. Assembler is available on four preprogrammed p/ROM chips.

Circle 174 on Inquiry Card

Bipolar Microprocessor Features Improved Processing Speed

Improved model 300 central processing unit now provides minimum system cycle time of 250 ns, which is the total time required to fetch, decode, and execute any instruction. As a result, unit can execute 4M instructions/s. The manufacturer, Scientific Micro Systems, Inc, 520 Clyde Ave, Mountain View, CA 94043, states that this faster cycle time permits direct control of double-density floppy discs.

Processing power allows firmware control of such functions as calculation of CRC and disc formatting, normally requiring additional ICs. Unit provides advantage of added economy. CPU treats I/O registers like internal registers and can directly manipulate and test groups of bits within 8-bit bytes in a single cycle, enabling it to replace random logic in areas such as communications, control, and I/O interfacing.

Two I/O units, 362 and 363 IV (interface vector) bytes, feature external clocking and input latches which operate asynchronously with CPU timing, eliminating need for additional edge-triggered latch when capturing transient data. 362 has 3-state outputs; 363 is an open collector. These components enable the CPU to be interfaced directly with up to 4096 I/O lines.

Circle 175 on Inquiry Card

TERADYNE'S J401: THE FULL CAPABILITY IC TEST SYSTEM EVERY ENGINEER CAN USE.

Until now, the complexities of test programming have kept all but a few specialists from using IC test systems. Everyone else had to queue up at the programmer's desk or do without the kind of information that was really needed.

Now there's a J401. A fully programmable test system for T^2L ICs with up to 24 pins, complete with built-in CRT, printer, and mag tape unit, that any engineer can learn to use in minutes.

For IC producers this means immediate access to vital process control information. For IC users it means the data necessary to choose components and vendors intelligently. And the ability to extract from field returns the information needed to improve product quality and yield.

The performance and flexibility of a large, computer-operated test system.

The J401 delivers the flexibility ordinarily associated only with larger, more expensive systems. It can datalog any forced or measured function and it can generate an x-y plot of any two parameters. The system also operates as a high throughput go/no-go tester for the production line or incoming inspection.

Product data fast. Higher product yield.

For the semiconductor manufacturer, the easy-to-use J401 allows errors to be spotted before they can begin to multiply. QC engineers can use it to evaluate devices, determine test margins, and check device lots.

The electronic equipment manufacturer will find the J401 useful in monitoring vendor-to-vendor and lot-to-lot variations. It enables him to spot device characteristics that could be contributing to problems. And QC personnel can use the system to analyze failures and reduce service costs.

A system for meeting the real objectives of incoming inspection.

The J401 gives you fast go/no-go testing with an important difference. It gives control over the *way* devices are tested. By pushing a few keys you can change test conditions, bin out top-quality ICs, or have datalogging to support returns. All in seconds. This is incoming inspection as it should be.

It's a Teradyne.

Each J401 is built for hard use on the factory floor. Each is supported by Teradyne's ten-year circuit module warranty, a 24-hour telephone trouble-shooting service, and a world-wide field service backed up by local parts stocking centers.

For complete information on the J401, write:
Teradyne, 183 Essex Street, Boston, Massachusetts. In Europe: Teradyne, Ltd., Clive House, Weybridge, Surrey, England.

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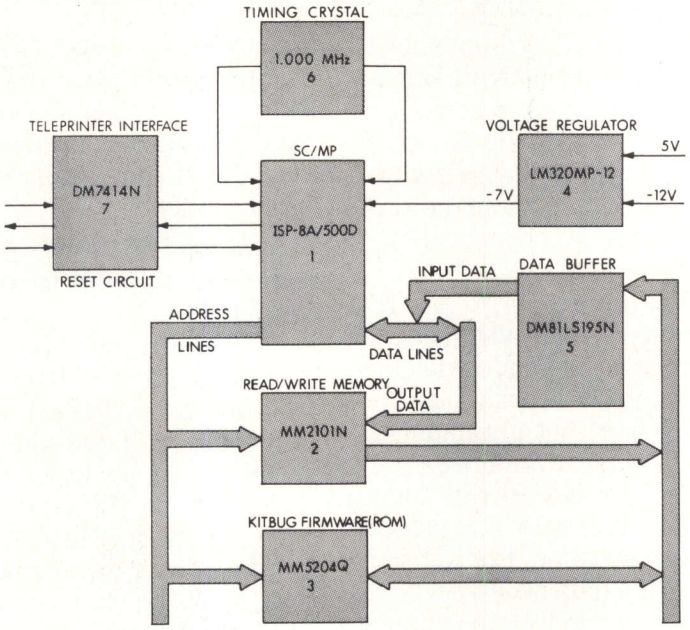
FPU Improves Microcomputer Power, Saving Time and Cost

Plug-in compatible with Intel MDS and SBC (single board) computers, microcomputer floating point unit (FPU) extends the 8080 instruction set to include binary-to-floating point decimal conversion; all trigonometric functions (inverse and hyperbolic); logarithms and powers (natural, common, X-power-Y); multiplication, division, addition, and subtraction (12 digits, $10^{\pm 99}$ range); coordinate transformation (rect-polar-rect); and mean and standard deviation. Hardware FPU module appears as a set of macro-instructions or as a set of subroutines which may be called by assembly language programs. Less than 64 bytes of user-supplied R/W memory are required. Unit is nonvolatile, operates when power is turned on, and offers more computational power than any other that has been available for the 8080.

Primary feature of the FPU, made by Applied Cybernetics, 960 N San Antonio Rd, Suite 281, Los Altos, CA 94022, is its ability to use symbolic parameters for arguments and results. Module requires no user "driver" software and is called from user program like an assembly language subroutine.

Circle 176 on Inquiry Card



Low cost SC/MP kit is based on SC/MP microprocessor chip which generates all control signals needed for operation of the system. When −12 V is applied to system through regulator, SC/MP reads the first instruction in ROM. Communication between user and SC/MP is via interface. User programs can be entered into R/W memory; SC/MP then operates under the direction of the new program

8-Bit Microcomputer Kit Provides Various Capabilities at Low Cost

A completely functional 8-bit microcomputer system based on the "SC/MP" microprocessor, SC/MP kit includes all the firmware and components necessary to build a working system. It can be assembled in less than 50 min. Priced at $99 each in quantities up to 10, the kit is offered by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. The SC/MP microprocessor is an 8-bit single-chip CPU housed in a 40-pin DIL ceramic package. It features static operation, 46 instruction types, single- and double-byte operation, software controlled interrupt structure, built-in serial I/O ports, bidirectional 8-bit tri-state[R] parallel data port, and latched 12-bit tri-state address port.

Memory is 4096-bit ROM organized into 512 bytes, with 8 bits/byte. It is preprogrammed to contain "Kitbug," a monitor and debugging program that assists in application program development, provides teletypewriter I/O routines, and allows examination, modification, and controlled execution of user's programs. Two 1K R/W memories are organized into 256 4-bit words. Together, they provide 256 8-bit bytes of static memory for application program storage. The microprocessor and Kitbug program control the transfer of data to and from the R/W memory section.

Voltage regulator provides stable −7 V for the chip, eliminating need for extra power supply. Interface between memory and microprocessor's data lines is provided by 8-bit data buffer. Timing crystal provides a 1-MHz timing signal for the clock circuit on the chip, which is the only external timing component needed by the clock. Teletypewriter interface IC has buffer and drive capabilities to implement 20-mA current loop interface for a teletypewriter.

A 72-pin edge-connector simplifies interconnection between the kit board and external hardware. The 24-pin IC socket is for easy mounting of the ROM, while the 40-pin IC socket allows quick mounting of the microprocessor onto the PC board, which measures 4 x 5". The board simplifies kit assembly and reduces possibility of assembly errors. Eight capacitors and seven resistors are also included in the kit.

While the ROM contains the Kitbug monitor program, other ROMs or p/ROMs with different programs can be added. Kitbug firmware allows programs to be entered directly into R/W memory from a teletypewriter keyboard. The user can execute the program while examining

(Continued on p 137)

advance program

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fall COMPCON 76

a choice of two pre-conference tutorials for the practicing professional

COMPCON's first hands on microprocessor tutorial

DESIGNING WITH MICROPROCESSORS: A "HANDS-ON" WORKSHOP

Don't miss this unique workshop on the principles and practice of microprocessor design. An extensive laboratory session will permit attendees to solve design problems on a variety of microprocessors using actual hardware.

Tilak Agerwala
Electrical Engineering Department, University of Texas

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Also . . . the most topical field in software today:

STRUCTURED PROGRAMMING

Victor R. Basili
University of Maryland at College Park

Terry Baker
IBM Federal Systems Center

COMPCON 76 Fall is celebrating the 25th Anniversary of the IEEE Computer Society by presenting an exceptionally comprehensive technical program. The Conference combines a state-of-art roundup by acknowledged technical leaders with "hands on" Engineering oriented sessions.

Designing with Microprocessors has been given particular attention, including Advanced Architectures, Microprocessor Software, Development Aids, and Applications. Software is also given special emphasis, but with a practical, result-oriented flavor. Real Time computing, Advanced Semiconductor technology, Computer System Architecture and Distributed Intelligence are combined to make this bicentennial COMPCON *THE* technical event of the year.

Don't miss this informative and stimulating International Conference. Participate in the Great Debate series, and interact with the leaders in your own and related technical fields.

See you at the Mayflower!

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DESIGNING WITH MICROPROCESSORS: A "HANDS-ON" WORKSHOP

COURSE OUTLINE:

- BASIC CONCEPTS AND RECENT ADVANCES IN MICROPROCESSORS
  - – Chip Architecture
  - – Microprocessor Selection Criteria
  - – Software Aids
  - – Development Systems
  - – Microprocessor Applications
    - o Input/Output - Peripheral Control
    - o Programmable Interfaces
    - o Solution to Typical Case Studies
- MICROPROCESSOR INTERCONNECTION – A DESIGNER'S PERSPECTIVE
  - – Microprocessor Networks
    - o Interconnection Concepts
    - o Information Transfer and Control
    - o Path Structures
  - – Bussing Strategies
    - o Design Tradeoffs
    - o Cost Measures
  - – Distributed Intelligence
    - o Problem Partitioning
- MICROPROCESSOR WORKSHOP

  A variety of microprocessor facilities ranging from evaluation kits to developmental systems will be available for tutorial participants to demonstrate the concepts introduced in the lecture sessions.

INSTRUCTORS

Tilak Agerwala is on the electrical engineering faculty at the University of Texas in Austin. He lectures on microprocessors at the graduate level and heads the microprocessor laboratory. Dr. Agerwala received his Ph. D from Johns Hopkins University in 1972.

Gerald Mason is a lecturer in the Electrical Engineering Department of Johns Hopkins University. His areas of specialization and interest include computer networking and fault-tolerant computing. He received his Ph. D in electrical engineering from Northwestern University.

Microprocessor Tutorial Chairman

Roger Westgate is professor of electrical engineering at The Johns Hopkins University. He is chairman of the COMPCON 76 microprocessor tutorial/workshop. Dr. Westgate received his Ph. D from Princeton University.

STRUCTURED PROGRAMMING

COURSE OUTLINE:

- Introduction to the major ideas of structured programming, their theoretical and practical foundations.
- Detailed presentation of the development of a single program, stressing the top-down evolutionary character of the process.
- Development of a major application program system, together with the quality and productivity results experienced.
- Case studies involving SP incuding NASA's Manned Space Flight Program. (SKYLAB)
- Concluding summary: the advantages and disadvantages of SP ideas as observed through their installation use by a large programming organization.

INSTRUCTORS

Terry Baker is responsible for the development of a software system for newspaper production for a consortium of eight major newspapers. With IBM since 1956, he most recently was manager of the Development Tools Department, responsible for the guidelines, tools, and support necessary for the introduction of programming support libraries, structured programming, top-down programming, and chief programmer teams at the center. He received his BS in mathematics from Yale University and his MS in applied mathematics from Harvard University.

Victor Basili has been on the computer science faculty at the University of Maryland at College Park since 1970; his major interests are the design, modeling, and implementation of programming languages. His major language development efforts have been the graph algorithmic language GRAAL and the SIMPL family of programming languages and compilers. He received a Ph. D in computer science from the University of Texas at Austin in 1970.

BOTH TUTORIALS START
9:00 AM, TUESDAY, SEPTEMBER 7, 1976

REGISTRATION FOR TUTORIALS AND CONFERENCES ON LAST PAGE

COMPCON 76 fall preliminary program

WEDNESDAY September 8, 1976

9:30 PLENARY SESSION

Opening Ceremony

Walter Beam, COMPCON 76 FALL General Chairman
Paul L. Hazan, COMPCON 76 FALL Program Chairman
Dick B. Simmons, President, IEEE Computer Society

Plenary Address

11:00 TECHNICAL KEYNOTE SESSIONS (Parallel)

MICROPROCESSORS: TRENDS IN MICROCOMPUTERS
Frederico Faggin, President, Zilog Corporation

SOFTWARE: NEW MANAGEMENT AND TECHNOLOGY HORIZONS
Elaine Bond, Manager of Programming, Systems Products Division, IBM

11:30 TECHNICAL KEYNOTE SESSIONS (Parallel)

COMPONENTS & MEMORY TECHNOLOGY: SEMICONDUCTORS AND MEMORIES . . . THE PACE IS ACCELERATING
H. Dean Toombs, Technical Director, Texas Instruments

COMPUTER SYSTEM TECHNOLOGY: INNOVATIONS IN SYSTEM ARCHITECTURE
Richard J. Clayton, Vice President for Computer Systems Development, DEC

12:00 TECHNICAL KEYNOTE SESSIONS (Parallel)

REAL-TIME SYSTEMS . . . UNDEFINED BUT UNDERSTOOD
Daniel G. O'Connor, Technical Director, The Singer Company

COMPUTER APPLICATIONS: THE APPLICATIONS PROGRAMMER OF THE FUTURE
Frederick B. Thompson, California Institute of Technology, Pasadena

WEDNESDAY AFTERNOON (Parallel Sessions)

2:30 SESSION 1 (COMPUTER APPLICATIONS)

CHARTING THE NATIONS ENERGY FUTURE

Chairperson: Richard H. Williamson, Energy Research & Development Administration
"ECONOMETRIC SYSTEMS ANALYSIS – ENERGY VS. GROWTH," David J. Behling, Brookhaven National Laboratory
"MODELING ENERGY FLOW THROUGH LARGE LINEAR SYSTEMS," Clark Bullard, University of Illinois

SESSION 2 (MICROPROCESSORS)

INNOVATIONS IN MICROPROCESSOR ARCHITECTURE

Chairperson: (To be selected)
"DESIGN OF THE Z80 MICROPROCESSOR SYSTEM," Zilog Corporation
"SINGLE CHIP PROCESSOR DESIGN," H. Blume, Intel Corporation

SESSION 3 (COMPUTER SYSTEM TECHNOLOGY)

SECURITY, PROTECTION, & RELIABILITY

Chairperson: Robert Courtney, IBM
"RELIABILITY MODELING OF VARIOUS MULTI-PROCESSOR STRUCTURES," A. Ingle & D. Siewiorek, Carnegie-Mellon University
"A CRYPTOGRAPHIC STANDARD," Theodore Linden, National Bureau of Standards

4:00 SESSION 4 (SOFTWARE)

SOFTWARE REQUIREMENTS SPECIFICATION ANALYSIS AND VALIDATION "PREVIEW: BLUEPRINT FOR SOFTWARE SUCCESS," J.H. Manley, JHU/APL

Chairperson: E. Goldberg, TRW
"SOFTWARE SPECIFICATION TECHNIQUES: A TUTORIAL," Donald J. Riefer, University of Southern California
"SOFTWARE REQUIREMENTS VALIDATION FROM THE PRIME CONTRACTOR VIEWPOINT," Gale Schluter, McDonnell Douglas Astronautics
"SOFTWARE REQUIREMENTS VALIDATION – THE SUB-CONTRACTOR VIEWPOINT," Joseph D. Mason, TRW

SESSION 5 (COMPONENTS TECHNOLOGY AND MEMORIES)

ADVANCED BIPOLAR COMPONENT TECHNOLOGY

Chairperson: Turner Hasty, Texas Instruments
"OVERVIEW OF SEMICONDUCTOR TECHNOLOGY TRENDS," Jerry Luecke, Texas Instruments
"ADVANCES IN I^2L TECHNOLOGY," R. Stehlin, T. I.
"ADVANCED ANALOG-TO-DIGITAL CONVERTER DEVELOPMENT," National Semiconductor Corp.

SESSION 6 (GREAT DEBATES SERIES)

CENTRALIZED VS DISTRIBUTED PROCESSING

Chairperson: J. Robert Wood, IBM Federal Systems Division

WEDNESDAY EVENING

5:30 COMPCON Cocktail Party

THURSDAY September 9, 1976

THURSDAY MORNING (Parallel Sessions)

9:00 SESSION 7 (COMPUTER SYSTEM TECHNOLOGY)

INNOVATIONS IN SYSTEM ARCHITECTURE

Chairperson: Robert Goldberg, BGS Systems
"ANALYSIS OF SEVERAL QUEUEING MODELS FOR MULTIPROCESSOR SYSTEMS," Yuan-Chieh Chow and Walter H. Kohler, University of Massachusetts
"VIRTUAL MACHINES FOR A TACTICAL ENVIRONMENT," John G. Perry Jr. and Robert R. Hein, Navy Surface Weapons Center
"VIRTUAL MACHINE RESEARCH ON THE HONEYWELL 6000," R. McGee, R. Goldberg and H.S. Schwenck

SESSION 8 (MICROPROCESSORS)

MICROPROCESSOR SYSTEMS

Chairperson: (To be selected)
"FEDERATED MICROPROCESSOR SYSTEMS," S.S. Roy, International Computer Limited, England
"MEDIUM SIZED COMPUTING SYSTEMS CONSTRUCTED FROM MULTIPLE MICRO COMPUTERS – THE GALAXY 5," Robert Laughlin, Digital Systems Corporation
"CENTRALIZED MICROCOMPUTING," Xerox Corporation

SESSION 9 (SOFTWARE)

SOFTWARE DESIGN METHODOLOGY

Chairperson: Robert Brown, Hughes Aircraft
"SOFTWARE DESIGN FOR HARDWARE INTERACTION OF REAL TIME SYSTEMS," H.M. Breneman and L. Danielian, Hughes Aircraft
"DATA STATE DESIGN," Jon Petersen, IBM

11:00 SESSION 10 (REAL-TIME SYSTEMS)

PROCESS CONTROL AND INTERACTIVE SYSTEMS

Chairperson: George Fath, General Electric

"ON-LINE TESTING AND SECURITY OF A DISTRIBUTED SYSTEM FOR PROCESS CONTROL," Geffroy Courvoisier, Centre National de la Recherche Scientifique, Toulouse, France
"A MODULAR SOFTWARE ARCHITECTURE FOR ROM RESIDENT PROGRAM," R. Lowe, W. Edwards, and J. Hudson, Northrop Corporation
"INTERACTIVE CURVE AND SURFACE DESIGN," R. Riesenfeld, University of Utah

SESSION 11 (COMPUTER APPLICATIONS)

COMPUTERS – SAVING ENERGY FOR THE NATION

Chairperson: Robert D. Williams, TRW
"POWER MANAGEMENT WITH THE IBM ENERGY CONSERVATION SYSTEM," Jack Breyer, IBM
"A MICROPROCESSOR BASED SYSTEM FOR ENERGY MANAGEMENT SYSTEM," Gideon Chavit, Honeywell
"THE USE OF COMPUTERS IN ENERGY MANAGEMENT SYSTEMS," Bryan Travis, DATRIX

SESSION 12 (SOFTWARE)

SOFTWARE COST ESTIMATING AND SIZING

Chairperson: Judy Clapp, The Mitre Corporation
"ADP RESOURCE ESTIMATING: A MACRO-ESTIMATING METHODOLOGY FOR SOFTWARE DEVELOPMENT," L.H. Putnam, Department of the Army/OAS – Washington, D.C.
"DEVELOPING A SOFTWARE COST METHOLOGY," Eldred Nelson, TRW Systems

SESSION 13 (SHORT NOTES)

UP TO THE MINUTE TECHNOLOGY ROUNDUP

THURSDAY AFTERNOON (Parallel Sessions)

2:00 SESSION 14 (COMPUTER SYSTEM TECHNOLOGY)

PRACTICAL APPLICATIONS OF PERFORMANCE EVALUATION

Chairperson: J. Buzen, BGS Systems
"HIERARCHIES OF MODELS," T. Giammo, Social Security Administration
"PREDICTING TIME SHARING PERFORMANCE," R. Salas, Brandeis University
"THE NEW GENERATION OF PERFORMANCE PREDICTION TOOLS," J. Buzen, BGS Systems

SESSION 15 (COMPONENTS TECHNOLOGY AND MEMORIES)

ADVANCED MOS COMPONENT TECHNOLOGY

Chairperson: James Heenan, IBM
"STATE-OF-ART HIGH SPEED N-CHANNEL MOS TECHNOLOGY," David Hause, Intel
"NON VOLATILE MNOS MEMORY DEVELOPMENT," NITRON Corp.

SESSION 16 (MICROPROCESSORS)

MICRO-COMPUTERS DESIGN AIDS

Chairperson: Jeanette Loustounom, Intel
Panel discussion, "THE MICROPROCESSOR DEVELOPMENT PROCESS: 3 DIVERGENT VIEWPOINTS, The Manufacturer – The Designer – The User."

4:00 SESSION 17 (REAL-TIME SYSTEMS)

REAL TIME DESIGN AND SIMULATION

Chairperson: R.L. Taylor, Singer
"DESIGN CONSIDERATIONS FOR REAL-TIME ARCHITECTURE," Kenneth J. Thurber and R.C. Deward, Sperry Univac
"REAL TIME NUCLEAR AND FOSSIL POWER PLANT SIMULATION FOR OPERATOR TRAINING," Enian Hay, Electronics Associates, Inc.
"REAL TIME 'REAL WORLD' SIMULATION FOR TRAINING," Redifon, Ltd.

SESSION 18 (COMPONENTS TECHNOLOGY AND MEMORIES)

STATE-OF-ART SEMICONDUCTOR MEMORY TECHNOLOGY

Chairperson: Jan Hofland, Hewlett Packard
"HIGH PERFORMANCE SEMI-CONDUCTOR MEMORY APPLICATIONS FOR ADD-ON MEMORY," Advanced Memory Systems
"SEMI-CONDUCTOR MEMORIES FOR HIGH PERFORMANCE COMPUTER APPLICATIONS," AMDAHL Corporation
"16k DYNAMIC RAM APPLICATIONS – MICROS TO MAIN FRAMES," K. Davis, MOSTEK

SESSION 19 (COMPUTER APPLICATIONS)

COMMAND AND CONTROL IN MILITARY AND LAW ENFORCEMENT SYSTEMS

Chairperson: Jack Munsen, Systems Development Corporation
"FOURTH GENERATION MILITARY COMPUTER FAMILY," Aaron Coleman, U.S. Army Electronics Command
"A MULTI-MINICOMPUTER NETWORK FOR OPTICAL MOVING TARGET INDICATION," H.E.T. Connell, Mitre
"LOS ANGELES COUNTY SHERIFFS DEPARTMENT COMMAND AND CONTROL SYSTEM," Sgt. Randy Matwood (LASO) and David Scully, Systems Development Corporation

THURSDAY EVENING

SESSION 20 (GREAT DEBATES SERIES)

THE LIMITS OF SOFTWARE RELIABILITY

FRIDAY September 10, 1976

FRIDAY MORNING (Parallel Sessions)

9:00 SESSION 21 (COMPUTER SYSTEM TECHNOLOGY)

DISTRIBUTED SYSTEMS AND NETWORKS

Chairperson: Sam Fuller, Carnegie-Mellon University
"TOWARD MODULAR HIERARCHICAL STRUCTURES FOR PROTOCOLS," M.G. Gouda and E.G. Manning, University of Waterloo, Canada
"DESIGN REQUIREMENTS FOR PRACTICAL GENERAL PURPOSE MULTIPROCESSORS," L.C. Widows
"ANALYSIS OF A MULTICOMPUTER SYSTEM: A CASE STUDY OF DFMP," R. Glorioso, F. Colon, W. Kohler, and Dominick Li, University of Massachusetts and DEC

SESSION 22 (MICROPROCESSORS)

MICROPROCESSOR APPLICATIONS

Chairperson: (To be selected)
"MICROPROCESSOR BASED CORRELATOR REFERENCE SYSTEM," R.C. Scott, III, and H.P. Erich, Martin Marietta
"MICROPROCESSOR IMPLEMENTATION IN PROCESS CONTROL," D. Tabak, E. Maymon, M. Janowitz, S. Greenberg, Ben-Gurion Univ., Israel
"MICROCOMPUTERS IN COMMUNICATIONS," CODEX Corporation

SESSION 23 (SOFTWARE)

SOFTWARE VISIBILITY & CONTROL

Chairperson: Richard Sylvester, Martin Marietta
"CONTROL OF SOFTWARE DEVELOPMENT ON THE VIKING MARS PROGRAM," G. Heylinger, Martin Marietta
"A SOFTWARE DEVELOPMENT FACILITY FOR MINI & MICROCOMPUTERS," T. Sleight and W. Sederowitz, Johns Hopkins University Applied Physics Laboratory
"ROBOT: THE HIGHEST LEVEL HUMAN/MACHINE INTERFACE LANGUAGE PROCESSOR FOR INTERACTIVE INFORMATION RETRIEVAL," R.M. Landau, Science Information Association

11:00 SESSION 24 (COMPUTER APPLICATIONS)
COMPUTERS: THE HEALTH OF THE NATION
Chairperson: Melville Hodge, TECHNICON
"COMPUTED TOMOGRAPHY – THE FIRST REQUIRED USE OF A COMPUTER IN DIAGNOSTIC MEDICINE," Robert Wake, Ohio Nuclear
"THE QRS, THE PVC AND ME," Charles S. Goetowsky, TELEMED
"ASPECTS OF INSTALLING A COMPUTERIZED MEDICAL INFORMATION SYSTEM AT THE NIH," Thomas Lewis, National Institutes of Health

SESSION 25 (COMPONENTS TECHNOLOGY AND MEMORIES)
ADVANCED SOLID STATE MEMORY TECHNOLOGY
Chairperson: James Daughton, Honeywell
"OVERVIEW – ADVANCED MEMORY TECHNOLOGY TRENDS," J. Daughton, Honeywell
"MAGNETIC BUBBLE TECHNOLOGY – STATUS AND PROSPECTS," Hsu Chang, IBM
"DIRECTIONS IN CCD DIGITAL MEMORY," M. Guidry, Fairchild Semiconductor
"EBAM – ELECTRON BEAM ADDRESSABLE MEMORIES," D. Speliotis, Microbit Corporation

SESSION 26 (SOFTWARE)
SOFTWARE RELIABILITY AND QUALITY ASSURANCE
Chairperson: J. Musa, Bell Laboratories
"RECENT DEVELOPMENTS IN SOFTWARE RELIABILITY – THE STATE OF THE ART," Martin Shooman, Polytechnic Institute of New York
"ATLAS – AN AUTOMATED SOFTWARE TESTING SYSTEM," W.H. Jessup, J.R. Kane, S. Roy, J.M. Scanlon, Bell Laboratories
"TECHNIQUES USED FOR TESTING MVS," A. Mondello, IBM

FRIDAY AFTERNOON (Parallel Sessions)

2:00 SESSION 27 (COMPUTER SYSTEM TECHNOLOGY)
PROBLEM PARTITIONING FOR DISTRIBUTED SYSTEMS
Chairperson: E. Douglas Jensen, Honeywell
"PROBLEM PARTITIONING IN TIME & SPACE," Douglas Jensen, Earl Boebert, Honeywell
"OPTIMAL PARTITIONING OF WORKLOADS FOR DISTRIBUTED SYSTEMS," V.B. Gylsys and J.A. Edwards
"MEASUREMENT OF PARALLEL PROGRAMS ON A MULTI-MINI SYSTEM," S. Fuller and P. Oleinick, Carnegie-Mellon University

SESSION 28 (MICROPROCESSORS)
MICROPROCESSOR SOFTWARE
Chairperson: (To be selected)
"MICROPROCESSOR SOFTWARE – A MANUFACTURER'S PERSPECTIVE," Wes Patterson, Motorola Semiconductor
"AN INDEPENDENT SOFTWARE HOUSE LOOKS AT MICROCOMPUTERS," J. Gibbons, Ryan McFarland, Inc.
"MICROPROCESSOR SOFTWARE – A USER'S EXPERIENCE,"

SESSION 29 (COMPUTER APPLICATIONS)
COMPUTERS FOR EDUCATION
Chairperson: John Carr, University of Pennsylvania
"CONTROVERSIES IN COMPUTER SCIENCE AND ENGINEERING EDUCATION AND THEIR IMPACT ON YOU AND FUTURE COMPUTER APPLICATIONS," Martha Sloan, Michigan Institute of Technology
"INVESTIGATION OF A FACILITATING NETWORK FOR HIGHER EDUCATION," James C. Emery, EDUCOM-Princeton, N.J.
"DATA PROCESSOR TECHNOLOGY IN EDUCATION – CYBERNETICS LEARNING ENVIRONMENTS," Alberto F. Tassinari, Universidad Industrial De Santander – Columbia

SITE OF compcon 76 fall

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The IEEE Computer Society membership desk will be open Monday evening, September 6,1976 through Friday afternoon, September 10,1976. Membership fees will be reduced by $15 for those non-member registrants who join the IEEE Computer Society at the conference.

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☐ TUTORIAL 2 + COMPCON	110	125	120	135

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*** Limited attendance. Register early — avoid disappointment.**

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compcon 76 fall

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the contents of memory and SC/MP registers to monitor performance. TTL-compatible I/O interface simplifies connection of application hardware so that practical test and demonstration circuits can be implemented. Hardware is controlled by the user's application programs.

Microprogram Sequencer for Pipelined Systems or Controllers

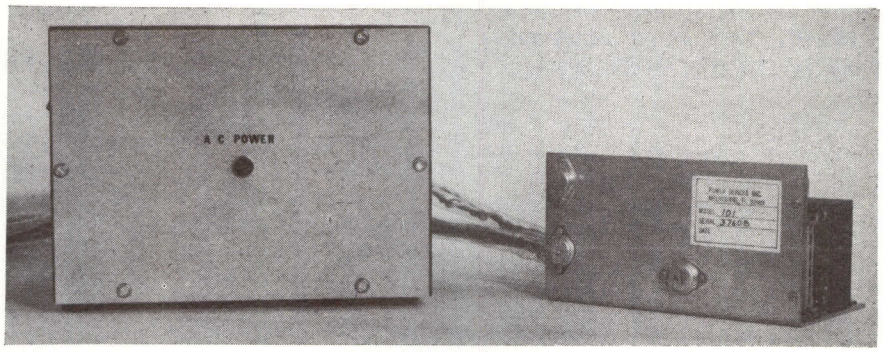
Am2911, a 4-bit element that can generate, increment, or store addresses, is designed as a second microprogram sequencer for use in bipolar microprocessor or for computer control systems. This LSI device has undergone 100% internal visual inspection, post-seal stabilization bake, temperature cycling, centrifuge stressing, and gross leak hermeticity testing, all requirements of MIL-STD-883. Sequencers come in 20-pin molded DIP with 0 to 70°C temperature range, and in 20-pin hermetic DIP with either 0 to 70°C or −55 to 125°C range.

A 45-ns circuit, the sequencer is designed for high speed and pipelined microprogrammed systems, especially those built with the Am2901 bipolar microprocessor, also from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. As a microprogrammable slice containing an 8-function arithmetic logic unit, 2-port 16-word scratchpad memory, additional accumulator register, and shifting and control logic, microprocessor circuit can execute read-modify-write cycle in 100 ns. Included in the family are a carry-look generator, 2-port register, pair of 256-bit high speed bipolar R/W memories, and 4-bit sequencer in 28-pin package.

Circle 177 on Inquiry Card

System Automatically Provides Uninterruptible Power During Failures

Able to keep up data processing systems for 20 min. to more than an hour during power failures, OEM



type power supply (model 101) provides 5 Vdc to loads of 3 to 8 A, and 12 Vdc at 0.6 A. Very little heat is generated by switched regulation system, which measures 4½ x 5 x 8¾". Announced by Power Devices, Inc, PO Box 333, Melbourne, FL 32901, system can be used with or without standalone uninterruptible conversion unit (model 201) which contains sealed batteries, chargers, controls, and inverter for supplying 20 W of ac for fan operation.

Switchover to battery and back to prime power operation is completely automatic without transients in output voltage. Batteries are recharged within 10 h after complete discharge cycle. Dc outputs are regulated to within 1% of nominal value for load change and for input variation from 105 to 130 Vac. Overvoltage and overcurrent protection on each dc output are included as standard features.

Circle 178 on Inquiry Card

Extended Temperature Components Available for µComputer Systems

MCS-40 microcomputer system components have performance guarantees over the −40 to 85°C temperature range, enabling their use in hostile, as well as normal commercial, temperature environments. Guarantees, such as central processor unit speed, are similar to those of MCS-40 components specified for 0 to 70°C operation. Claimed by Intel Corp's Microcomputer Systems Div, 3065 Bowers Ave, Santa Clara, CA 95051, to be the industry's most widely used, low-cost microcomputer system, it is expected to broaden the applications range by allowing equipment manufacturers to use it in hostile environments without making special provisions for temperature control in the equipment design.

The system consists of the 4040 (60 instructions, interrupt mechanism) and 4004 (46 instructions) central processor units and a family of components for use with either CPU. Components available for extended temperature range include: system clock generator, read-only memories (256 x 8 with 4-bit I/O port, 1024 x 8 with four 4-bit I/O ports, 2048 x 8, and 256 x 4 erasable p/ROM), random-access memories (80 x 4 with 4-bit output, and 256 x 4 static CMOS, 15 nA/bit), and I/O units (general-purpose programmable with 16 I/O lines, programmable keyboard/display, standard memory interface, and 10-bit serial/parallel register and output expander).

Performance guarantees allow the extended temperature range components to be used interchangeably with commercial range MCS-40 components in essentially all applications. System's key specification, CPU clock period range, has not been changed. It is guaranteed over −40 to 85°C range at 1.35 µs min to 2.0 µs max with power supply tolerances of ±5%, for both CPUs. Other component guarantees, such as for the max access times of memory units, are compatible with those of the CPUs. Minor modifications have been made in speed and drive currents of certain components.

Circle 179 on Inquiry Card

Functionally Mechanized Microprocessor Controls Applications With Ease

ACS-4040 MPU, a parallel 4-bit general-purpose PCB, is mechanized around Intel's 4040 CPU IC to provide cost-effective maximum microprocessor power for system applications such as process and dedicated control systems, data acquisition and storage systems, and smart stand-alone terminal systems. Functional sections include 4-bit CPU; crystal clock timing; 8-bank R/W memory and 2-bank p/ROM addressing; 8-bit program instruction, 13-bit p/ROM I/O address, R/W memory bidirectional memory data, and I/O bidirectional buffered expansion buses; run/single-step mode control; and single step, photo-isolated local/remote power and master resets. On-board bus control logic is provided to interface with optional program development control and display panel module.

Hardware capabilities include 10.8-μs single instruction cycle time, polled interrupt handling capability, and up to seven levels of subroutine nesting. On-board logic provides direct addressing of 8K bytes of p/ROM/RAM R/W program instructions, 2560 4-bit RAM data words, 32 4-bit I/O ports, and 32 4-bit RAM buffered output ports. Sixty basic processor instructions are compatible with 4004 CPU source code software. Twenty-four 4-bit single index registers (or 12 8-bit register pairs) are provided by the MPU for enhanced programming.

Measuring 8.75 x 5.9 x 1/16" with an MIB connector interface via a single pin connector with PCB fingers spaced on 0.125" centers, MPU PCB from Automated Computer Systems, 2361 E Foothill Blvd, Pasadena, CA 91107 requires 5 V at 0.9 A and −10 V at 0.1 A. Combination 2K-byte p/ROM/1280-word data RAM/16 buffer output port; 4K-byte R/W program memory; 8-port 3-state universal I/O with handshaking capabilities; combination ASR-33 TTY and RS-232-C modem interface; 64 x 4-bit input channel MUX; 1702A p/ROM programmer; universal wire-wrap for mechanizing user custom logic; full computer control/HEX display panel for checkout and program development; plug-in switching regulated power supply module; and MIB multi-slot with connectors for custom system mechanizations are all standard supporting PC board modules.

Program development tools include an assembler/simulator p/ROM programmer software development microcomputer system with supporting operating system software which includes a chip based utility system and a chip based assembler system.

Circle 180 on Inquiry Card

µProcessor-Compatible Converters Feature 16-Bit Resolution

Designed to interface with advanced digital circuitry and microprocessors, the 500 series of 100-kHz voltage-to-frequency converters delivers exceptional linearity and temperature stability over wide input signal dynamic range. Converters from SGR Corp, Neponset Valley Industrial Pk, PO Box 391, Canton, MA 02021 are available in six modules and offer better than 16-bit resolution, with low nonlinearity error. Overall accuracy is from 11 to 13 bits. Full scale error range is from ±150 ppm/°C (economy grade) to ±15 ppm/°C max (high performance model).

Series is engineered to accommodate 2-wire data transmission over long distances for remote data acquisition and process control systems; it can also serve as inexpensive method of transmitting data through high noise environments. Compatible with 3½ digit DVMs, units provide monotonic 13-bit performance with no missing codes.

Circle 181 on Inquiry Card

µProcessor and 8K RAM Designed for Difficult OEM Applications

With standard 4½"-wide boards and 22-pin double-sided edge connectors, the 6800 microprocessor-based central processing unit and 8K memory board can operate by itself with up to 384 bytes of on-board R/W memory or with up to seven 8K memory boards. Introduced by M&R Enterprises, PO Box 61011, Sunnyvale, CA 94088, the CPU serial I/O port offers both RS-232 and 20-mA current loop. On-board cycle-stealing DMA does not idle the processor. Disc drives and tape units directly address memory; provisions for addressing slow memory add flexibility. CPU recognizes 72 instructions; greater number of address modes make 6800 software easier to write. I/O is addressed like memory, permitting data in interface registers to be handled like data in memory. Interrupt structure saves registers in stack when interrupted. An external stack in memory allows unlimited subroutine nesting. Oscillator has 1-MHz crystal. Unit comes with a Mikbug ROM in optional ROM socket, which also accepts a custom programmed ROM.

8K static memory board can plug into any location in backplane. Low power static R/W memories cycle in 500 ns and entire memory draws 1.5 A from single 5-V supply. On-board location selectors address the memory to any slot in the CPU's 64K memory map.

Circle 182 on Inquiry Card

16K RAM Module Designed for Microcomputer Development Aids

Compatible with M6800 development instrumentation, MEX 6816-1 provides 16,384 bytes of dynamic R/W memory. Thirty-two 4096 x 1-bit RAMs are organized into a 16K-word x 8-bit array. Module contains refresh circuit, address multiplexer, address decoder, array row/column select circuit, module control logic, bus interface buffers, and switches that allow the base memory address to be relocated in the system memory space. Circuitry to test parity of data byte is also offered as an option.

Memory refresh, initiated every 32 μs, is accomplished on a clock "cycle-stealing" basis. Power requirements of module, offered by Motorola Semiconductor Products, Inc, PO Box 20294, Phoenix, AZ 85036, are 5.0 V at 1.5 A, 12 V at 1.6 A, with operating temperature range of 0 to 70°C.

Circle 183 on Inquiry Card

FIND OUT WHERE THE PARADE IS GOING AND GET IN FRONT OF IT.

That's leadership.
You know where the parade is going. So do we: Distributed Processing. Putting the power where you need it means you get information when you need it. No fumbling. No bumbling. That's why we built the Zentec 9003 user programmable intelligent terminal. Not just intelligent . . . programmable.

Do it your way.
The 9003 is designed to solve a wide range of problems. That's why we provide comprehensive sets of microcomputer firmware programs in either PROM or ROM . . . plus a RAM option that provides true programmability. What's more, you can add the peripherals you need, when and where you need them.

Keep it simple and dependable.
As often as not, your operator isn't a programmer. Thus, simple and understandable operation is vital. That's why we build the 9003 to be easily understood and operated. And, easily maintained.

Test it yourself.
We do. Every single 9003 goes through exhaustive tests before we deliver it to you. That means you get a nice surprise . . . no surprises. You just put the 9003 to work and watch it perform. But that's not surprising. At Zentec, we know where the parade is going.

Distributed Processing From

ZENTEC

CIRCLE 55 ON INQUIRY CARD

Call us for information:

- Santa Clara (408) 246-7662 • TWX 910-338-0572
- Southern Calif. (714) 998-9680 • TWX 910-593-1339
- Midwest (312) 297-8550
- Boston (617) 879-7530 • TWX 710-380-0105
- New York (914) 949-6476 • TWX 710-568-1335
- Philadelphia (215) 688-7325 • TWX 510-668-2995
- Washington (301) 656-3061 • TWX 710-824-0093
- United Kingdom (0442) 61266 • TLX 851-825629
- West Germany 0611-634037 • TLX 841-416608
- Austria 425451 or 421675 • TLX 847-74737
- Switzerland 041-831043 • TLX 845-72231
- Netherlands 01720-94044 • TLX 844-34111

Memory Modules With Various Configurations Available for MPU Kits

Measuring 9.75 x 9.75", the series of memory modules is the same width as, and is pin for pin pluggable with, Motorola EXORciser™. Modules can be configured to 4K, 8K, 12K, and 16K bytes. In the 4K-byte module, top four bits are address selectable, and can shift to any space in memory. This module contains a write protect switch; memory can be used as read-only, or can be written in—in which case it is protected from overwrite. Memory chips are low power static RAM.

Other features of series include interface bus signal with 16 address lines and eight data lines, phase 2 clock signal, read-write select line, and valid memory address signal to indicate that lines are stable. Modules also read R/W specifications for M6800 microcomputer. Busing for power is from separate pins in memory; power supply inputs can be jumpered from normal supply, or from auxiliary battery, if desired. Capacity for 1K bytes of UV erasable p/ROM is included on board for restart or bootstrap programs. Memory is standalone for use with the M6800, and also has interrupt and restart vectors. Modules are available from Revenue Control Sciences, 137 Richmond St, PO Box 868, El Segundo, CA 90245.

Circle 184 on Inquiry Card

Assembler and Simulator Are Combined in Software Development System

The 8080 microprocessor program development software is a complete system that runs on any 4K PDP-8 series minicomputer equipped with an ASR-33 terminal, or equivalent. Available from FBE Research Co, PO Box 68234, Seattle, WA 98168, CAL-80/SIM-80 combines an efficient assembler and powerful simulator, providing all that is necessary to write and test 8080 software. A conventional 3-pass paper tape symbolic assembler that accepts Intel instruction mnemonics, assembler (CAL-80) outputs a BNPF format p/ROM image tape and formatted, paged program listing. Input is an ASCII paper tape. Assembly language source format is free-field, line oriented and assembler operation is controlled by familiar punctuation and order of occurrence. Facilities for symbol assignment, automatic symbol definition, and constant generation are provided. Up to 400 symbols may be defined.

The interactive simulator (SIM-80) makes the PDP-8 look like an Intel 8080 system running an invisible debugger/monitor program and having 2K of core memory. Programs are input as BNPF format p/ROM image tapes; these tapes can also be generated from contiguous sections of simulated memory. Numbers and single character self-terminating commands are used to control the simulator from the minicomputer terminal. Commands are provided to examine single or successive memory location contents, alter memory contents, list register contents, print status bits as words, set the breakpoint, continue from breakpoint, simulate vectored interrupt, print program counter and stack pointer, and simulate input data. Both programs can use high speed paper tape equipment, if available.

Circle 185 on Inquiry Card

DAPL Is High Level Programming Language For 4-Bit Microprocessor

A programming language called DAPL, and a compiler for the language are available to program Advanced Micro Devices 2900 family of 4-bit bipolar microprocessors, and soon will be offered for other microprocessors, including Monolithic Memories 6700 and Texas Instruments SBP-0400. DAPL provides four levels of programming capability, covering range from simple bit patterns through register transfer notation. Extensive error checking facilities as well as the ability to handle device-dependent considerations such as p/ROMs and PLAs are provided.

Announced by Zeno Systems, Inc, 2210 3rd St, Suite 110, Santa Monica, CA 90405, DAPL features up to 8192-word x 256-bit microprograms; free-form syntax, flexible commenting formats, and commands for formatting the source program listing; paper tape output in format acceptable to most p/ROM writers; commands for conveniently locating program segments at specific word or R/W memory boundaries; symbolic macro substitution facility; complete variable cross-reference listing; and support of PLAs. DAPL can also serve as an assembler for an arbitrary machine implemented using bipolar slice architecture.

Circle 186 on Inquiry Card

Single Board μProcessor Memory System

Based on the National Semiconductor Pace microprocessor, AED/Pace/Memory system is packaged on one 6 x 9" card. Features of the card developed by Advanced Electronics Development, 880 Boston Post Rd, Old Saybrook, CT 06475 include: 16-bit instruction word, 8- or 16-bit data words, 45 instructions, common memory and peripheral addressing, four general-purpose accumulators, and 10-word stack. Card has six vectored priority interrupt levels and programmer accessible status register. Instruction execution time is 10 ms. Containing single phase true and complement crystal clock, card operates with a 5- to 12-V supply. Memory is 256 x 16 R/W, with sockets for 3K x 16 p/ROM/ROM. Also included are start-up circuitry, split busing for data I/O/addresses, socket for CPU, address latches, and card edge connectors. There is a 165-h burn, with a 1-year warranty on the system.

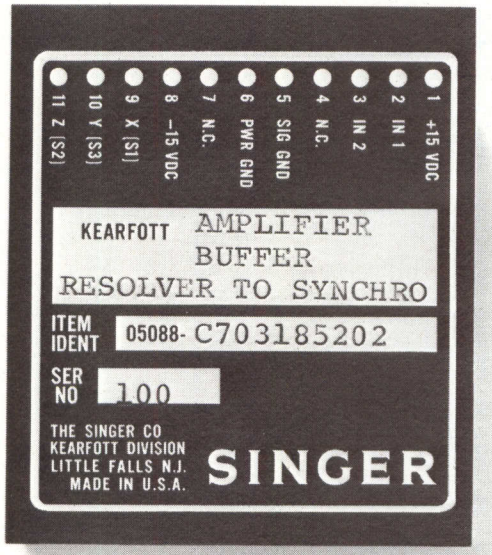
Card is available with such options as a soldered in p/ROM, an I/O port, 16-bit parallel and serial, and free library of software. □

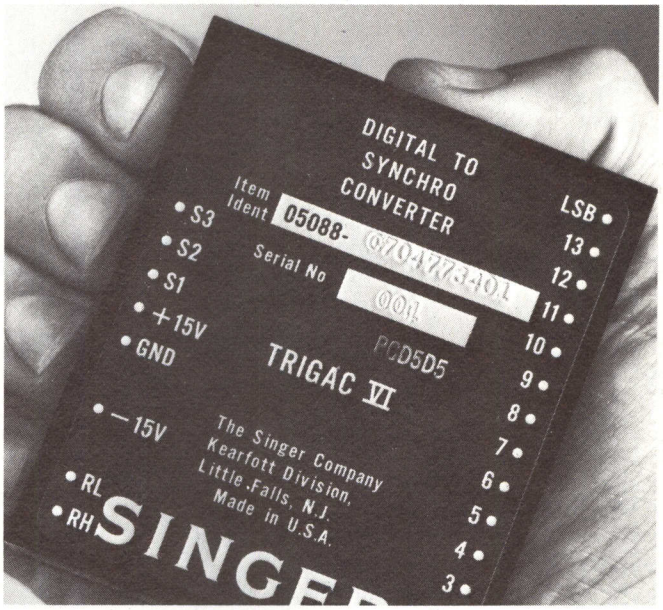
Circle 187 on Inquiry Card

Trigac VI digital-to-synchro converter gives you accuracy and power without raising your temperature.

The closest thing yet to a Solid State Synchro, Kearfott's Trigac VI Modular Digital-to-Synchro/Resolver Converters provide the accuracy and power you need, with a bonus. In addition to standard 4 arc minutes of accuracy at 1 volt ampere, the transformation ratio remains constant within ±.25%. We also have units constant within ±0.1%. That can make the difference between delivering power or just throwing it away.

Let us help you be cost effective. Standard options range from industrial grades thru hi-reliability units, from accuracies of ±20 arc minutes to ±1 arc minute and, in addition, special designs and packaging as you require.





Need more power? Try our line of compatible synchro amplifiers.

Our 3185 Series is designed to perform the synchro power buffering or resolver to synchro (Scott-T) function. They provide matched power amplifier channels and transformer coupled outputs capable of driving torque repeaters or multiple control transformers up to 5 va. These fully potted units feature overload protection, low-quiescent currents and transformer-isolated outputs. Models available range from industrial to full MIL-SPEC high-reliability grades.

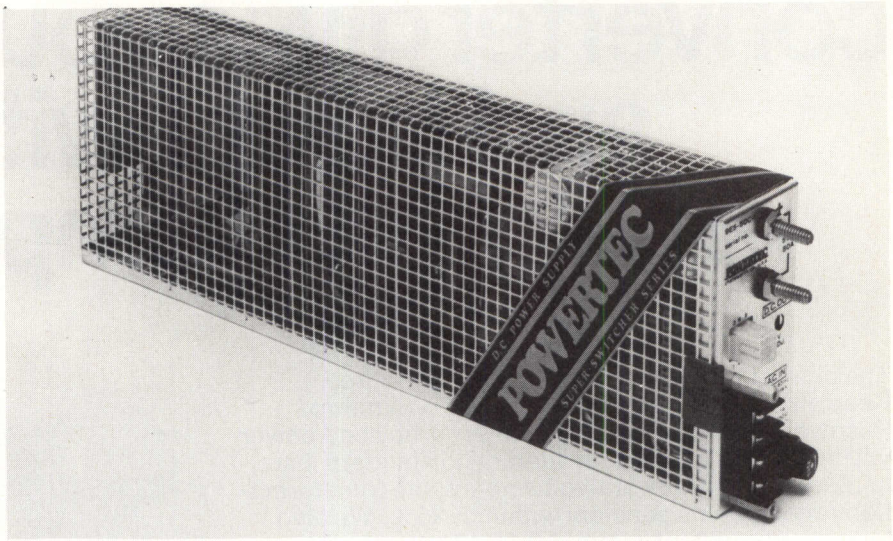
NEED ADDITIONAL POWER? We have units available with power outputs to 50 va, 60 or 400 Hz operation, and options of built in digital converters and/or power supplies.

For details on our converters and amplifiers, contact The Singer Company, Kearfott Division, 1150 McBride Avenue, Little Falls, New Jersey 07424.

SINGER
AEROSPACE & MARINE SYSTEMS

CIRCLE 56 ON INQUIRY CARD

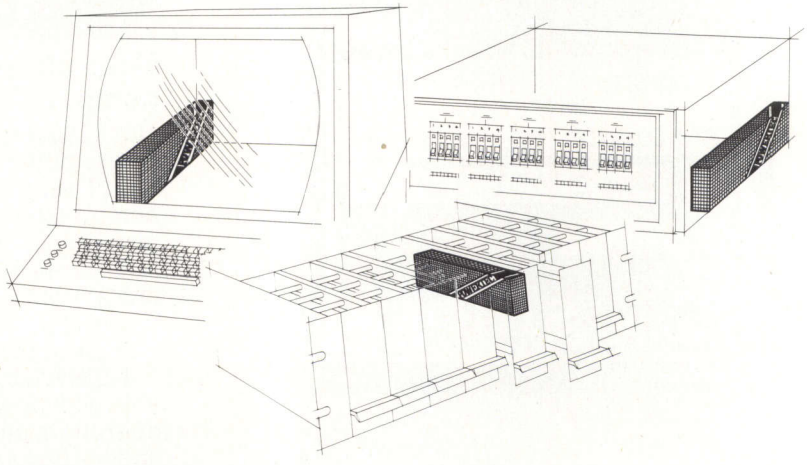
PRODUCT FEATURE



Form Factor of Switching Power Supply Meets User Requirements for Diverse Designs

Utilization of a 40-kHz switching rate for the first time and a specially designed mechanical configuration permit the 9E5-50C-17 SuperSwitcher™ to attain what is claimed to be the highest packaging density of any off-the-shelf, convection cooled, 250-W power supply. Powertec's 5-V ±10%, 50-A switching power supply yields 1.4 W/in.^{3} from a 7-lb package that measures only 4.94″ high x 2.25″ wide x 15.5″ long (16.38″ including front connectors and terminals).

This low profile packaging permits installation of the unit in many different locations and attitudes. It may be mounted vertically, horizontally, or crosswise in a standard RETMA rack; alongside, above, below, or behind rack drawers in a cabinet; or within terminals, consoles, or other equipment. Because the unit is convection cooled, there is no fan noise to bother office personnel.



Packaging of SuperSwitcher evolved from survey to determine most practical configuration. Only 2.25″ of rack depth is used if fit into a standard 5.25″ RETMA rack. It also can be mounted alongside the CRT in a video display terminal (left), in the side panel of a computer or other console (right), in a card cage (center), or in a variety of other equipment

Operating Characteristics

Under nominal conditions—input voltage of 115/230 Vac +10/−20% and 25°C ambient operating temperature—and with the chassis mounted such that its 4.94″ dimension is vertical, the unit will provide 250 W, 5 V, 50 A. Mounted with the 4.94″ dimension horizontal and with the screen side up, the unit derates load current 10%.

The supply will operate from inputs of 92 to 126 or 184 to 253 Vac, 0 to 40°C ambient temperature, and supply 4.75 to 5.25 Vdc. Under normal ±10% line conditions, the unit will operate from 110-, 115-, 208-, 220-, or 230-Vac nominal line potentials. A 20-ms min voltage hold

up allows it to function under abnormal line conditions. Input frequency range is 47 to 63 Hz. Shutdown occurs if input voltage drops below the proper limit or if internal temperatures become excessive. Automatic recovery takes place when voltage and temperature return to the acceptable ranges.

Output voltage regulation is 2 mV over the rated input voltage range and 0.2% for the full output current range. Voltage ripple and noise is 40 mV pk-pk typ, 50 mV pk-pk max with measurements made on a 50-MHz oscilloscope.

Voltage transient deviation with step load change is ±5% for 50% change of full load rating occurring between 20 and 100% of full load. Recovery to 0.1% requires ≤400 μs. No ringing or instability will occur.

Standard features include remote sensing and voltage programming as well as logic inhibit. Options include power-fail logic output and factory installed master/slaving paralleling which permits interchanging of units as master and slave.

Five proprietary internal features guard against operating conditions that might be destructive to many other switchers. In addition to standard protection against over-voltage, over-current, and over-temperature and inadequate line voltage, unique control circuitry keeps transistor collector currents and transformer flux densities balanced and within design limits under all normal and abnormal operating conditions.

A front panel connector provides access for remote sensing to compensate for load cable drops and for connection of a potentiometer to adjust remote voltage. A logic inhibit signal is provided through this connector to shut down the unit when a low logic signal is applied. Removal of the signal allows the unit to resume operation.

Price and Delivery

Single unit price for the 9E5-50C-17 SuperSwitcher is $395. OEM quantity discounts are available. Prototype units are now available. Delivery on production quantities is eight weeks ARO. Powertec Inc, 9168 DeSoto Ave, Chatsworth, CA 91311. Tel: (213) 882-0004.

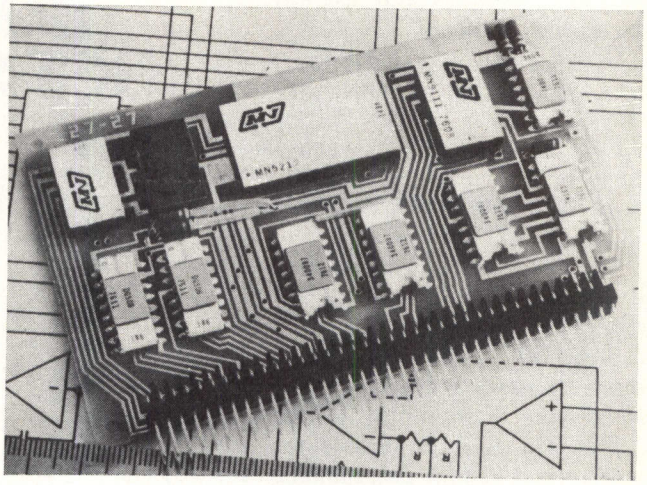
For additional information circle 199 on inquiry card.

PRODUCTS

Miniature Data Acquisition System Interfaces Directly with Microcomputers

Direct interface with microprocessors and microcomputers by the MN7002 miniature data acquisition system is accommodated through buffering of selected outputs with 3-state gates. The 16-channel, 12-bit system retains its capability to operate in either single-ended or true differential modes even when expanded to 256 channels. A right-angle connector allows the device to be mounted parallel to a motherboard. The 2.9 x 4.5 x 0.35″ device is available in standard and military temperature ranges, operates without external adjustments, and is fully specified over its full temperature range. Linearity over the entire range is +1 LSB max; crosstalk is −80 dB or more for operation in either 16-channel, single-ended or 8-channel, true-differential operating modes. Max throughput rate of 40 kHz is achieved in a multiplex overlap mode. Input impedance is 100 MΩ or better under all conditions. **Micro Networks Corp,** 324 Clark St, Worcester, MA 01606.

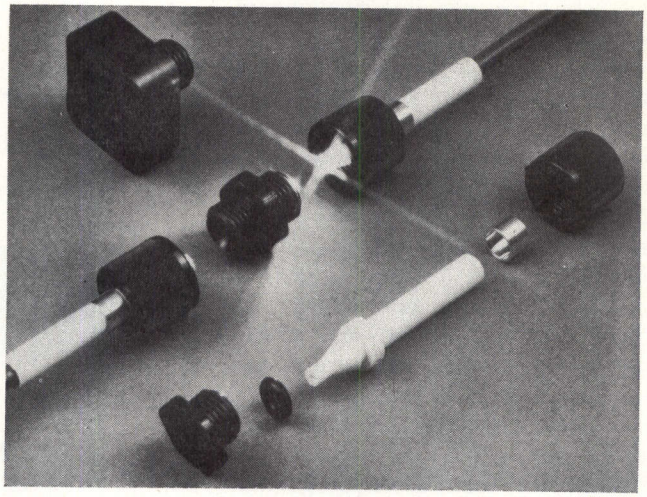
Circle 200 on Inquiry Card



Fiber Optic Connector Eases Termination Problems For Both Dry Splice and Fluid Coupling Insertions

A wide variety of fiber optic bundles can be accommodated by a universal end termination that provides optimum packing fraction and simplifies end polishing. The termination can be used in multiposition connectors and mates with a splice bushing or with a bushing that houses either light source or photodetector. Insertion loss varies from about 2 dB (depending on type of bundle terminated) with index matching fluid as a coupling medium, to approximately 3 dB for a dry splice (two terminations face-to-face in a splice bushing). During termination (and when connected) the resilient nose of the thermoplastic ferrule is compressed radially, compacting the fibers into a minimum diameter bundle on the centerline of the termination. This permits the termination to absorb the tolerances normally associated with the number and diameter of fibers in a bundle to provide a superior packing fraction. Terminations are supplied with a polishing bushing and complete installation instructions. **AMP Inc,** Harrisburg, PA 17105.

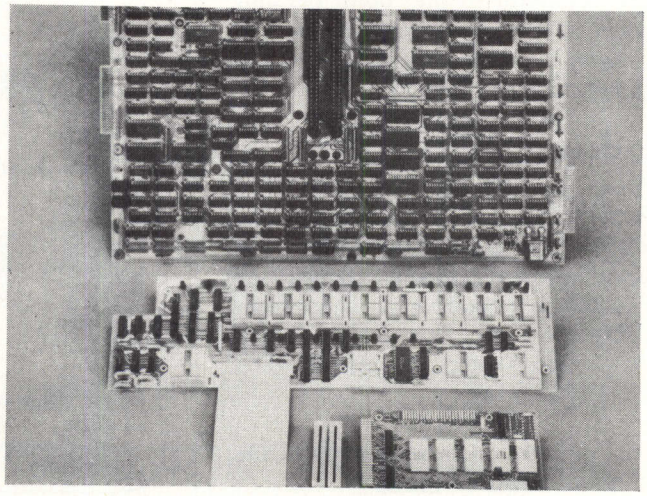
Circle 201 on Inquiry Card



Full Minicomputer Performance and Capabilities Provided by Single Board Processor

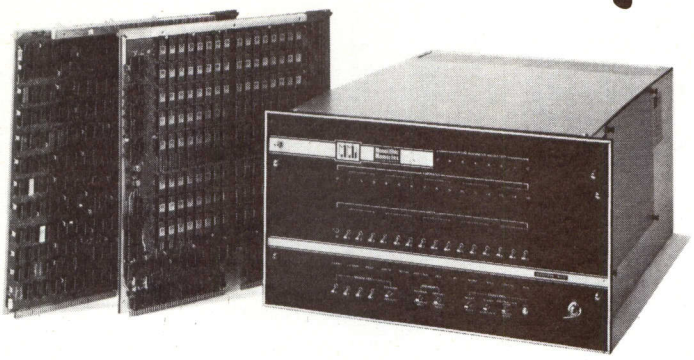
Requirements for a processor having power, speed, and flexibility of a high level minicomputer but packaged as a component for OEM systems are met by the 2108K miniprocessor. Up to five times faster than microprocessors and LSI-based microcomputers, this minicomputer-on-a-board at its basic level is a high performance 24-bit microprocessor capable of a register-to-register add in one 325-ns machine cycle. With the optional 21MX instruction set ROM, the processor becomes a full minicomputer that is completely compatible with 21MX computers, software, and peripherals. Available instruction set includes floating point, data communication, and integer arithmetic instruction. User programs may be dynamically loaded into p/ROM and plugged into control store or placed into main memory. Available accessories include 8- and 18-slot card cages, front panel control assembly, engineering and reference documentation, and base set instruction ROMs. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

Circle 202 on Inquiry Card



Stop waiting for a better NOVA*.

The μMini 3™ is here now.



Look at the features. See if we can't enhance performance, and reduce your cost, all at the same time.

Available as boards or a complete system.

High speed 300ns micro cycle cpu.

Maximum flexibility through user microprogrammable PROMs.

Complete 32K words system with paper tape I.O. and multiply/divide on only two boards.

Upward and downward compatible.

High speed, bipolar, LSI, microprocessor from the leading bipolar manufacturer.

High density, solid state MOS memory with up to 32K words on one board.

Low power consumption.

If your OEM system is tied to NOVA* software and peripherals but you need a mini with more performance and less price, stop waiting and give us a call. The Monolithic Memories μMINI 3 is here and deliverable right now.

And the price is right. Compare for yourself:

CONFIGURATION	NOVA 2/10	μMINI 3/09	NOVA 3/12
CPU, Chassis, P.S., Front Panel	✓	✓	
32K words memory	✓	✓	
Auto Program load	✓	✓	
PM/AR	✓	✓	
MPY/Div	✓	✓	NOVA 3 WHERE ARE YOU?
Real Time Clock	✓	✓	
TTY Control	✓	✓	
PTR Control	✓	✓	
PTP Control	✓	✓	
Slots used	5	2	
List Price	**$13,800**	**$9,450**	

Above pricing derived from Data General April 1, 1975 price list and MMI May 15, 1976 price list. Single unit prices.

For more information, or to arrange a hands-on demo, call TWX, write Al Trejo, or contact your local representative.

United States
Monolithic Memories, Inc.
1165 E. Arques Avenue
Sunnyvale, CA 94086
Phone: 408/739-3535
TWX: 910-339-9229

Europe
Monolithic Memories,GmbH
8000 Munich 80
Mauerkircherstr. 4
West Germany
Phone: (089) 982601
Telex: (841) 524385

Far East
MMI Far East Ltd.
Parkside-Flat Building
4-2-2 Sendagaya
Shibuya-Ku
Tokyo 151, Japan
Phone: (3) 403-9061

* Nova is a trademark of the Data General Corporation

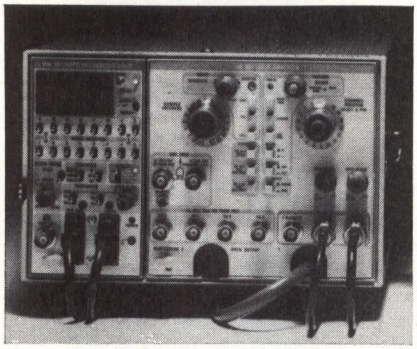
Monolithic Memories

PRODUCTS

AUTO LOADER FOR FLOPPY DISC TESTERS

Designed for a Memorex 652, but adaptable to most floppy disc drives, loader handles up to 20 discs at a time, eliminating hand insertion and removal of each disc. When used on the FD-33 tester, 50 discs can be tested in an hour, including 6 s for loading and unloading. After a 20-disc test sequence is completed, discs are stacked in a receiving bin. A dual stacking mechanism offsets rejected discs ½" from good discs, allowing easy separation when testing is complete. **Three Phoenix Co,** 10632 N 21st Ave, Phoenix, AZ 85029.
Circle 203 on Inquiry Card

WORD RECOGNIZER/ DIGITAL DELAY PLUG-IN

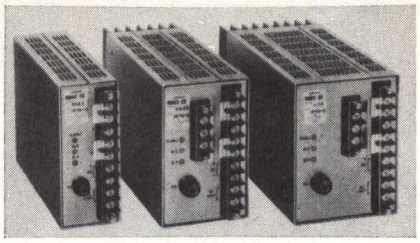


WR501 adds 16-bit word trigger and digital trigger delay to the 16-channel LA501 logic analyzer. A 17th qualifier bit provides selection of the time or condition under which the recognizer searches for the chosen pattern. Inputs are divided into two easily attached, 9-channel active probes. Probe input impedance is 1-MΩ paralleled 5 pF (at probe head) for min loading on all logic families. Separate threshold controls for each probe allow the unit to accept inputs from two different logic families simultaneously. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.
Circle 204 on Inquiry Card

16-PIN IC PACKAGING PANEL

Consisting of 108 16-pin IC patterns, with additional committed voltage and ground sockets at every IC position, and six 108-pin I/O connectors, series 6PS108 panels offer a max I/O capability of 648 I/O pins/panel with six I/O channels. Panels are available with or without connectors in any or all of the six perimeter locations, for max wire-routing flexibility. Connectors are glass-filled nylon with gold-over-nickel plated contacts. **Garry Manufacturing Co,** 1010 Jersey Ave, New Brunswick, NJ 08902.
Circle 205 on Inquiry Card

SWITCHING POWER SUPPLIES

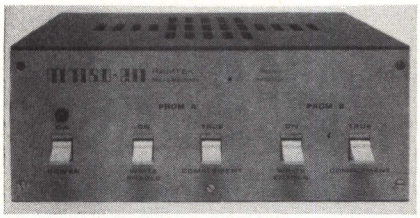


Modular style stabilizers rated 50, 100, and 150 W provide voltage levels of 5, 9, 12, 15, and 24 V. Output current for 50-W models ranges from 0 to 10 A at 5 V to 0 to 2 A at 24 V; 100-W models, from 0 to 20 A to 0 to 4 A; and 150-W models, from 0 to 30 A to 0 to 6 A. Other specs include 105 to 125 Vac, 47- to 420-Hz source voltage; 20-ms holding time; 65% efficiency; ±2% overall stabilization; 5 mV rms, 300-mV pk-pk ripple and noise; 5-ms recovery time, step load current, and 0.05%/°C tempco. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.
Circle 206 on Inquiry Card

EIA STANDARD CABINET BLOWERS

CB series computer/electronics cabinet blowers for racks 19" wide and 7, 8¾, and 10½" high has air flow rates at 115 V, 60 Hz, and typ static pressure of 0.1-in. H_2O range from 155 to 480 cfm. Consisting of dual single-inlet centrifugal units driven by single motor in welded box cabinet, it features split and expanded aluminum filters, exhaust outlet guards, and stainless steel grills in two optional designs. Blower motors are permanent split capacitor or shaded pole. **Torin Corp,** Torrington, CT 06790.
Circle 207 on Inquiry Card

p/ROM SIMULATOR

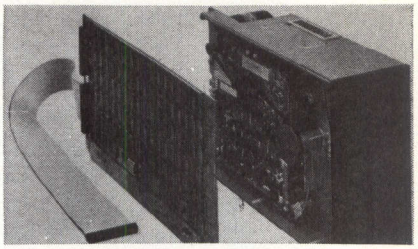


Providing high speed static RAMs to replace MOS p/ROMs or ROMs, as an option to the MM80 microprocessor in-circuit emulator, p/ROM simulator acts as a memory extension to the emulator, permitting multiple units to be daisy chained. Each unit will simulate two p/ROMs of up to 1K x 8 bits. The device being simulated is replaced by a p/ROM simulator connector cable and plug. Front panel controls select true/complement data and write protection. Self-contained power supply retains memory contents when emulator is off. **Ramtek Corp,** 585 N Mary Ave, Sunnyvale, CA 94086.
Circle 208 on Inquiry Card

1200M-BYTE DISC FORMATTER

Model XDF-76 operates with 3340-type disc storage modules, providing for 40M- to 1200M-byte capacity; 1200M-byte storage is accomplished with four storage modules and one formatter. Design provides ECC (error correction codes), rotational position sensing, and interleaving for consecutive sector transfers. Other features include 128K-byte transfer in one operation, overlapped seek of up to four drives simultaneously, 512-byte buffer for computer/drive synchronization, and multiport capability. **Xebec Systems Inc,** 2985 Kifer Rd, Santa Clara, CA 95051.
Circle 209 on Inquiry Card

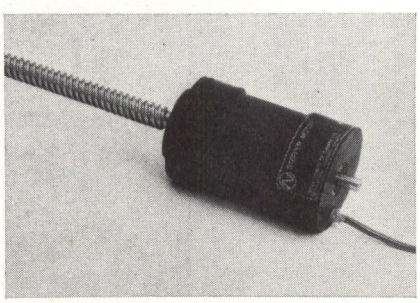
FLOPPY DISC SYSTEM KIT



Consisting of a smart controller; one to four drives; interconnecting cable from controller to drives; and hardware interface for connecting the system to microcomputers, the microprocessor-based disc controller is packaged on a single PC board that pancakes directly to one disc drive, and requires less than 1" of space. Additional drives are daisy chained from the first. Dual-density version writes 630K bytes/diskette; IBM-compatible unit writes 256K bytes/diskette. **Sykes Datatronics Inc,** 375 Orchard St, Rochester, NY 14606.
Circle 210 on Inquiry Card

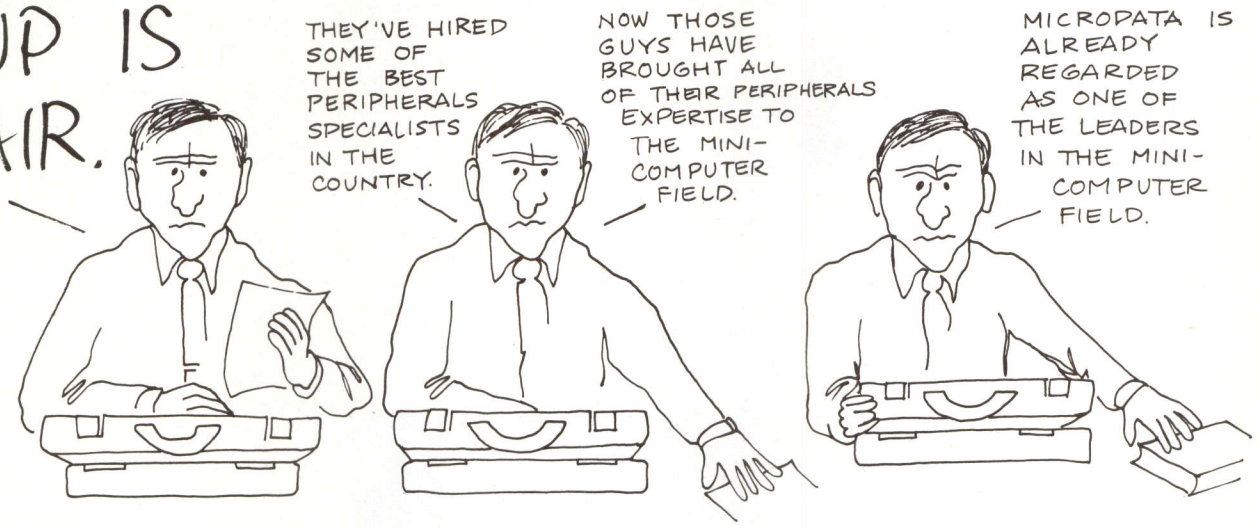
STEPPER MOTOR

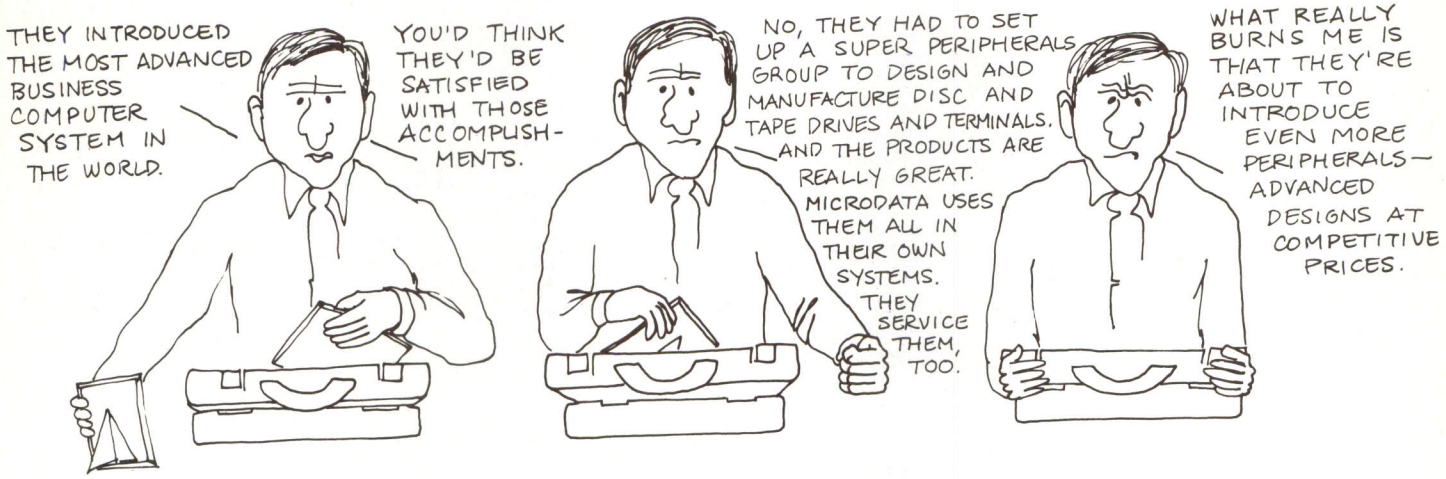
Extended shaft version of std size 20, 15-deg, 3-phase voltage regulated motor is intended for use in floppy disc drives. Three shaft sizes with two, three, and four start ground or rolled threads are available. Model 20M33 series uses precision instrument ball-bearings, preloaded to ensure min end play of extended shaft. Features include holding torque of 40 to 50 oz-in.; ±3% step error; and 28 Vdc. **Novatronics of Canada Ltd,** PO Box 610, Stratford, Ontario, Canada N5A 6V6.



Circle 211 on Inquiry Card

MICRODATA'S PERIPHERALS GROUP IS UNFAIR.





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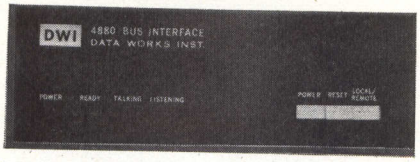
17481 RED HILL AVENUE,
IRVINE, CA 92714
P.O. BOX 19501, IRVINE, CA 92713
PHONE 714/540-6730
TWX: 910-595-1764

Microdata

For immediate need, circle 60 on Inquiry Card.
For information only, circle 61 on Inquiry Card.

PRODUCTS

IEEE BUS INTERFACE COUPLER

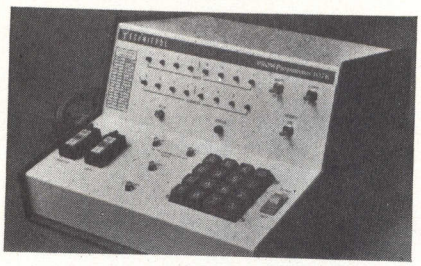


Model 4880 IEEE Std bus coupler is designed to make any electronic instrument compatible with IEEE 488 bus. Three configurations are: as talker, where coupler takes output of measuring instrument (such as DVM) and outputs readings onto 488 bus; as listener, where coupler takes commands from bus, using them to operate stimuli or output devices from the 488 bus; and for connecting and controlling devices in bidirectional manner (talker/listener). **Data Works Instrumentation,** 9748 Cozycroft Ave, Chatsworth, CA 91311.
Circle 212 on Inquiry Card

ALPHANUMERIC LED DISPLAY

DL-416 display has four 0.16" alphanumeric characters preassembled for multiplex operation on PCB with pins on 0.075" centers. Boards can be stacked end to end to create a display with any number of characters, spaced on 0.260" centers. High-contrast characters are readable in daylight at up to 5 ft, within 20-deg half angle. Characters are formed using 16-segment starburst pattern. Luminous intensity is 0.5 mcd/digit at 5-mA current/segment. **Litronix, Inc,** 19000 Homestead Rd, Cupertino, CA 95014.
Circle 213 on Inquiry Card

p/ROM PROGRAMMER

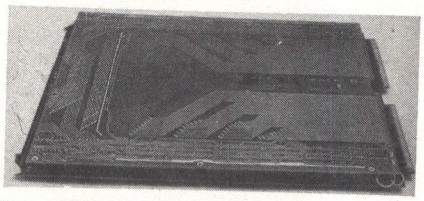


Model 107K incorporates a circuit that permits a complete copy of any 1702 p/ROM to be made in 20 s or less with reduced chip heating; up to 2 min. are required to make copies with conventional programmers. Features include hex keyboard entry of data and address, autocopy between selectable min and max addresses, verify while reading or writing, and stop-on-error detect. General purpose interface is offered as an option. **Technitrol, Inc,** 1952 E Allegheny Ave, Philadelphia, PA 19134.
Circle 214 on Inquiry Card

HUFFMAN CODER/DECODER

Coder/decoder pair increases efficiency of word-oriented digital transmission systems by assigning short (1- or 2-bit) Huffman codes to commonly occurring input words, and long (10- or 12-bit) codes to infrequently occurring words. Max efficiency is obtained when codes are generated from statistics produced from actual data being transmitted. Data-sampling device is available for producing word-frequency histograms. Each pair is available on two matching 4½ x 6" PCBs, and is equipped with sockets for installing up to two sets of p/ROMs. **Tyton, Inc,** 395 North Rd, Sudbury, MA 01776.
Circle 215 on Inquiry Card

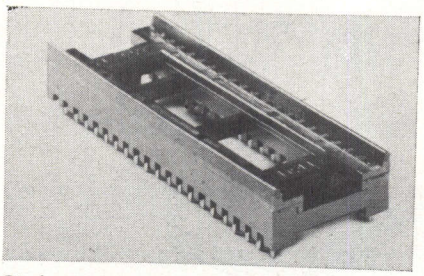
32K-WORD CORE MEMORY SYSTEM



The ECOM^{R} R, a single-board core memory system with storage capacity of 32,768 x 18-bit words, is compatible with H models (16K). Standalone MM-124 memory module has complete timing and control, memory bus interface, and core array drive circuits on a single PC board, measuring 11.5 x 16 x 0.75". With byte control it can be operated as a 65,536-word x 9-bit memory. A max of 16 modules can be paralleled to form a 9.4M-bit memory system. Access time is 300 ns max; memory cycle time is 750 ns. **Standard Memories,** 4120 Birch St, Suite 105, Newport Beach, CA 92660.
Circle 216 on Inquiry Card

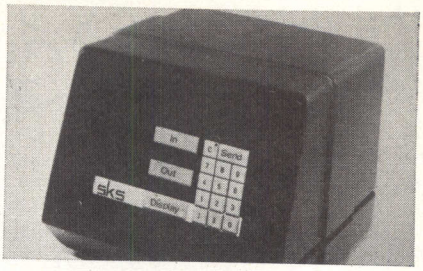
CLOSED ENTRY LSI SOCKET

Allowing insertion and withdrawal of fragile LSIs without damage, while maintaining sufficient normal force for a reliable low level electrical contact, the 6097 combines Soldercon™ 1938 dual beam contact with 94 V-O flame retardant polyester housing. Housing design incorporates a closed entry cap and a closed socket base to prevent solder wicking during wave soldering. The device is available in 24, 28, and 40 positions on 0.100 x 0.600" spacing. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.



Circle 217 on Inquiry Card

MPU-BASED MAGNETIC CARD TERMINAL

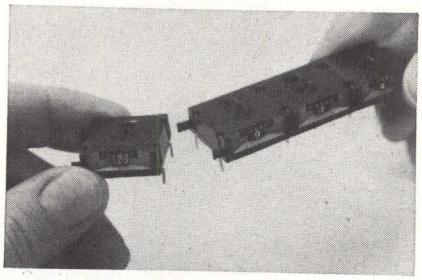


Small, lightweight magnetic card terminals for use in synchronous or asynchronous entry or receipt of data are available in five configurations ranging from a basic read-only model to a unit that offers five function keys, a 10-digit numeric keyboard, an 8-digit LED display, and a 16-digit numerical impact printer. Units measure 10.4 x 12 x 12.2", and weigh from 16 to 20 lb. **Quatro, Inc,** 3 Great Meadow Lane, East Hanover, NJ 07936.
Circle 218 on Inquiry Card

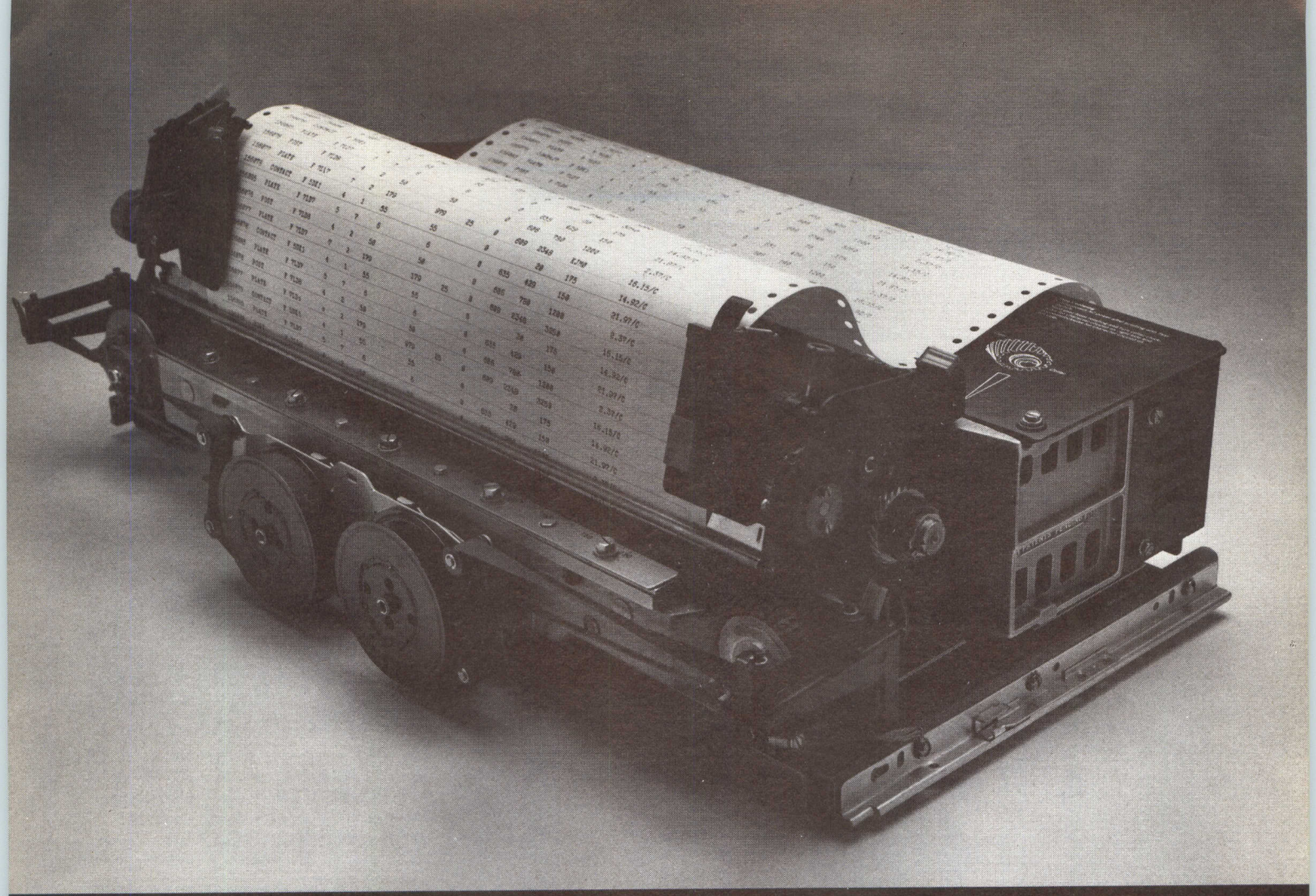
ULTRA-HIGH SPEED DACs

Totally self-contained units for converting ultra-high speed digital input signals, three DAC 1100 models provide 5-, 6-, or 7-bit resolution at conversion rates ranging from 100 to 60 MHz, respectively. Every unit contains an ECL-compatible input holding register, solid-state analog switches, precision ladder network, temp-compensated internal voltage reference generator, and low impedance output driver circuit. All units are fully-tested and calibrated "system-ready" modules. **Phoenix Data, Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017.
Circle 219 on Inquiry Card

LOW PROFILE STRIPSWITCH



Featuring 0.300" high design enabling mounting on PC cards racked at 0.5" intervals, switch mounts directly to PCB by hand, wave, or flow soldering, vertically or horizontally on both sides of board. No mounting hardware is required. Single modules can be snapped together to form multi-station switch assembly, allowing mix and match of different codes within one unit. Snaps can be cut off in single station applications. Models offer thumbwheel or screwdriver setting. **EECO,** 1441 E Chestnut Ave, Santa Ana, CA 92701.
Circle 220 on Inquiry Card



132 columns. Over 300 lines per minute. Under $2000.*

In printers, it's not just a question of how much they cost, but one of how much you get for your money. And on a price/performance basis, nothing even comes close to the Teletype® model 40 OEM printer.

Besides getting a 132-column, heavy-duty impact printer that delivers over 300 lpm for less than $2000, you also get a printer with outstanding flexibility and reliability.

The big reason behind the model 40's price/performance advantage over the competition is our unique design. Even though it operates at speeds over 300 lpm, wear and tear is less than you'd find in a conventional printer operating at a much slower speed. Fewer moving parts and solid-state components add up to increased reliability and reduced maintenance.

We'd be ahead if we just stopped there, but the model 40 also offers you a number of other features. Like a choice of character sets, operator-adjustable form width and form length, parity error indication, and a built-in self-test feature, just to name a few.

For complete information, please contact our Sales Headquarters at: 5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.

TELETYPE

The Teletype model 40 OEM printer. Nothing even comes close.

Teletype is a trademark and service mark registered in the United States Patent and Trademark Office.
*80-column-version available for under $1400.

CIRCLE 62 ON INQUIRY CARD

PRODUCTS

AUTORANGING PORTABLE DMM

A field-grade multimeter with performance characteristics of a bench-type instrument, model 6000 provides automatic ranging for ac and dc volts, ac and dc amps, and resistance measurement functions. Twenty-six ranges cover voltage measurements from 200 mV to 1 kV, current from 2 mA to 10 A, and resistance from 200 Ω to 20 MΩ. A "hold" input jack provides memory retention capability for remote measurements. Auto-zero and auto-polarity are built-in. Accuracy is 0.35%. **Weston Instruments Div, Weston Instruments, Inc,** 614 Frelinghuysen Ave, Newark, NJ 07114.
Circle 221 on Inquiry Card

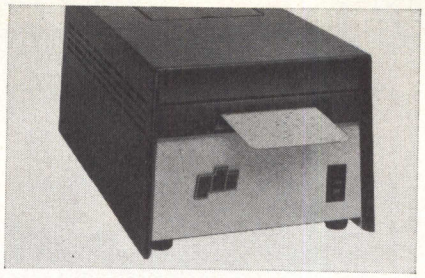
MULTIPLE-OUTPUT POWER SUPPLIES

Model 601.5 has all voltages necessary to operate small CRT, and features 1.5 kV for anode, 6.3 V for heater, −1.5 kV for cathode, and −1.5-kV floating supply for blanking. Input power is unregulated 24 Vdc. Line and load regulation is 1% on each output, with voltage choice of 10, 12, and 15 kV ±5%. Supply provides max power of 5 W. Short circuit, arc, and overload protection; and full-load transient of 0.5 to 1% peak, with recovery in 3 ms typ are provided. **Keltron Corp,** 225 Crescent St, Waltham, MA 02154.
Circle 222 on Inquiry Card

MIL-R-28803/1 READOUT ASSEMBLY

Model 905H has been qualified to MIL-R-28803/1, a severe environment spec that covers high impact shock, RFI shielding, and moisture-sealing requirements. Each readout component in assembly uses fiber optic light tubes to transmit light from solid-state LED light sources in the back of unit to display face with min light intensity loss. Displays are created by lighting various combinations of dot-pattern segments. Digits are 0.43″ high. **Master Specialties Co,** 1640 Monrovia Ave, Costa Mesa, CA 92627.
Circle 223 on Inquiry Card

SINGLE BADGE/CARD READERS

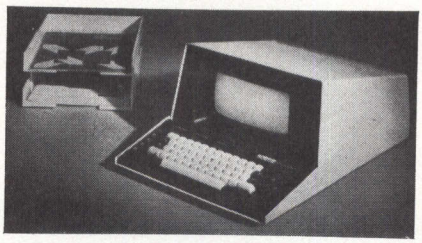


Line of word/data collection stations have one-at-a-time readers designed to handle identification badges as well as punched or mark sense cards as small as 22 col. Std features include ability to automatically process cards of any length and a variable speed transport control. Models are available in 80-col std tab hole cards, 40- and 80-col hole/optical mark or mark sense cards, and 40- and 80-col std tab hole cards and optical mark cards. **Peripheral Dynamics, Inc,** 1850 Gravers Rd, Plymouth Township, Norristown, PA 19401.
Circle 224 on Inquiry Card

INTELLIGENT MULTIPLEXER

Timeline 780 Supermux, a microprocessor-controlled time division multiplexer, eliminates data transmission errors generated on the high speed link between multiplexers. The device uses an ARQ technique to eliminate errors, and has sufficient buffer storage to assure data integrity even with outages lasting 10 s on a fully loaded 9600-bit/s line. Unit will intermix speeds, data rates, and protocols, and allows synchronous and asynchronous channels to contend for the same bandwidth. **Infotron Systems Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.
Circle 225 on Inquiry Card

MINIATURE CRT DATA ENTRY TERMINAL



The 278 mini-display terminal, a CRT device, is compatible with IBM 3270 and can be intermixed with any 270 system display and printing devices. With min of electronic components to insure reliability and ease of maintenance, design includes non-glare/tilt screen, flicker-free display, and separate low-profile keyboard. Comparable in size to std electric typewriter, unit can be connected to company's controllers, including local, remote, and virtual terminal line controller. **Courier Terminal Systems, Inc,** 2202 E University Dr, Phoenix, AZ 85034.
Circle 226 on Inquiry Card

RIBBON EDGE SENSOR

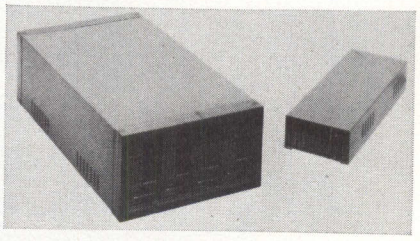
Using hybrid circuitry to provide TTL, CMOS, and DTL compatibility, the 126-1 is a solid-state optoelectronic assembly containing infrared LEDs which are spectrally matched and precisely aligned to silicon phototransistors. Designed for ribbon-edge sensing in printers, the unit is suitable for any sensing application where a logic high output is required for an obstruction of ≤2% transmissivity or a logic low output if the transmissivity is ≥75%. **HEI, Inc,** Jonathan Industrial Ctr, Chaska, MN 55318.
Circle 227 on Inquiry Card

ABSOLUTE ENCODER

The RA___/158S offers resolution to 22 bits (4,194,304 counts/turn) in 8-in. through-hole, 15-in. dia configurations. Features include chrome slit and disc assembly, redundant optical system, rotary seals, and IC electronics. Other specs include non-operating slew speed of 100 rpm max, op temp range of −40 to 50°C, breakaway torque of 35 oz-in. max, and running torque of 25 oz-in. max. **Measurement Systems Div, Itek Corp,** 27 Christian St, Newton, MA 02161.
Circle 228 on Inquiry Card

FREQUENCY DIVISION MULTIPLEXERS

M series devices enable several terminals to utilize a single leased line. Designed to operate over std 3002 voice-grade lines, carrying data at from 75 to 1200 bits/s, the units can multiplex up to 25, 75-bit/s terminals or combinations of data and voice over the same conditioned voice-grade lines. Operating over either 2- or 4-wire lines, the multiplexers perform equally well in half- or full-duplex modes, as well as in polled environments. Modules consist of two PC boards: channel receiver, and channel transmitter and control. **Prentice Electronics,** 795 San Antonio Rd, Palo Alto, CA 94303.

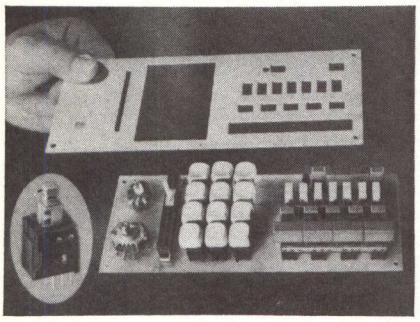


Circle 229 on Inquiry Card

LOW LEVEL A-D CONVERSION SYSTEM

Providing a direct-coupled amplifier-filter module on each channel, GMD-10 through -1000 act as low level signal enhancement devices for GM series A-D conversion systems. Amp provides configurations with single fixed gains from 1 to 1000; fixed 2-pole output filter offers full power bandwidths from 1 Hz to 60 kHz (−3 dB points) and full scale output of ±10 V at 5 mA in addition to the normal high level multiplexer output of the converter. Features include 120-dB common mode rejection (at gain 1000X), <2-μV noise RTI, and drift as low as 1.0 μV/°C RTI. **Preston Scientific Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.
Circle 230 on Inquiry Card

STANDARDIZED PUSHBUTTON SWITCHES



IMPS (integrated modular pushbutton switch) has standardized mounting and device heights to simplify the front panel PC board interface. Switch requires only 0.6″ from switch side of the board to inside surface of the front panel. Modular design permits close stacking (10-mm center-to-center spacing) for momentary function keyboard applications and for push-push and interlocked assemblies. Other features are 2M-cycle min load life; 2.5- to 3.5-oz actuation force; spst, spdt, dpst, and dpdt switch contacts; and 10-, 15-, 20-, or 25-mm center-to-center spacing. **Centralab Electronics Div, Globe-Union Inc,** PO Box 858 Hwy 20 W, Fort Dodge, IA 50501.
Circle 231 on Inquiry Card

INTELLIGENT TERMINALS

Series 30 and 40 provide cartridge disc storage up to 40M bytes, with up to 32 CRT operator positions and 32 printers/"cluster". Software support consists of Data Entry Software Level I and II, high level BASIC programming language, and file management software system. Cartridge disc storage of the 40 is operated under Program Development and File Management System software; it requires 32K, 48K, or 64K bytes of core memory. The 30 features 16K, 32K, 48K, or 64K bytes of programmable memory. **Incoterm Corp,** 6 Strathmore Rd, Natick, MA 01760.
Circle 232 on Inquiry Card

MICA PAPER CAPACITORS

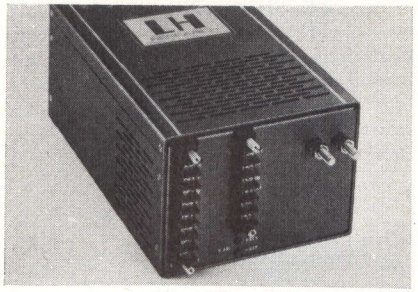
Developed for high reliability applications, K series is manufactured with mica paper dielectric impregnated with epoxy formulation. Ac corona inception and dc breakdown levels are increased two to four times with possible 30 to 50% volume and weight reductions. Wrap and fill unit has 0.1 μF capacity and 4200 dc working voltage; fiberglass housed unit has 1.0 μF capacity, 12K dc working voltage; and epoxy molded unit has 4.0 μF capacity, with 8K dc working voltage. Units are available in solder type, threaded stud, or wire lead terminations. **Custom Electronics, Inc,** Browne St, Oneonta, NY 13820.
Circle 233 on Inquiry Card

8-BIT MONOLITHIC D-A CONVERTER

Fully processed to MIL-STD 883 level B or C and designed for −55 to 125°C temp range, unit is pin-for-pin equivalent of MC1408/1508. Packaged in 16-pin hermetically sealed DIP, it includes bias circuit, reference amplifier, and switch and resistor network chip. Output is fast settling (300 ns), and is in 0 to 2 mA or ±1 mA range, depending on pin interconnections and input coding. Input is TTL/DTL compatible and has binary and offset binary coding. Required power supply is ±5 Vdc. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.
Circle 234 on Inquiry Card

PRODUCTS

4-OUTPUT SWITCHING POWER SUPPLY



Supply offers up to four outputs totaling 750 W from package measuring 5.1 x 7 x 12.75". Primary output of model MM-440 is 5 V at 150 A. Second output can be 2 V at 12 A, 5 V at 12 A, 12 V at 10 A, 15 V at 10 A, 18 V at 8 A, or 24 V at 5 A. Third and fourth voltage outputs can be any combination of 5 V at 5 A, 12 V at 5 A, 15 V at 5 A, 18 V at 4 A, and 24 V at 3 A. Up to 80% efficient, unit features 1% pk-pk or 50-mV pk-pk ripple and noise on output, and line and load regulation of 0.4%. **LH Research, Inc,** 1821 Langley Ave, Irvine, CA 92714.
Circle 235 on Inquiry Card

FOCUS DISTORTION CORRECTION MODULE

FC101 module accurately corrects for focus errors in CRTs which employ magnetic or electrostatic focus. Module synthesizes output function required and features 800-kHz full power output frequency with 1% full scale accuracy typ. Slew rates are 55 V/μs; settling time to 1% for 10-V step input is 1 μs. Operation is from −25 to 85°C with 0.06% FS/°C total error vs temp. Packaged in 1.5 x 1.5 x 0.4" epoxy package, module is suitable for socket or PCB mounting. **Intronics, Inc,** 57 Chapel St, Newton, MA 02158.
Circle 236 on Inquiry Card

COMPUTER OUTPUT MICROFILMER

Fully integrated into graphic processing system, AP75 micrographic plotter presents readable digital data on high resolution CRT, which has 16K x 16K positions, 4096 x 4096 resolvable elements, and eight intensity levels. Plotted image is photographed simultaneously by precision camera onto microfilm. Basic film recording capability is 35 mm, with 80 line-pairs/mm at 24X resolution. Options include 105 mm (170 line-pairs/mm at 48X) and 16 mm (170 line-pairs/mm at 24X) capabilities. **Applicon Inc,** 154 Middlesex Tpk, Burlington, MA 01803.
Circle 237 on Inquiry Card

7-SEGMENT LED DISPLAY

Line of decode displays have memory units featuring all logic functions on plug-in cards with readout on 0.6" LED display. Unit draws 23 mA/segment at 5 V for both logic and display functions. Readouts provide brightness level of 6K ft-L; display provides clear readable numeral up to 30 ft. Optional power supply can be mounted within IDI bezel housing, providing a self-contained unit which can be sealed. Displays are available with from two to eight decades. **Instrument Displays, Inc, Div of Keltron Corp,** 225 Crescent St, Waltham, MA 02154.
Circle 238 on Inquiry Card

INTEGRATING A-D CONVERTER

Microprocessor-compatible converter modules feature 3-state output and 13-bit resolution with up to 13-bit accuracy. TTL-compatible outputs allow both high and low data bytes as well as status lines to be connected to same 8-bit microprocessor bus. Units use precision multi-slope integration technique to deliver accuracy and resolution. Other features are automatic zero correction, internal reference, and overrange flag. Units accept bipolar input and provide 2's-complement binary output. **SGR Corp,** Neponset Valley Industrial Pk, PO Box 391, Canton, MA 02021.
Circle 239 on Inquiry Card

MULTIFUNCTION COMPUTER-BASED MULTIPLEX SYSTEMS

Based on the DEC LSI-11 microcomputer, combined with communications, control options, and software, series 600 provides specific user requirements. Communications options include SSM-600 signal stream multiplexing system, which links computer with dispersed sensors and output controls; CPM-602 command polling multiplex system, which allows central terminal to transmit data transfer commands; and RRM-603 random response multiplexing system. Display options include CRTs with or without graphics, teleprinters, annunciator panels, individual indicators, and special map displays. **Receptors, Inc,** 4203 Spencer St, Torrance, CA 90503.

Circle 240 on Inquiry Card

QUAD 256-BIT MOS RAMs

Offering access speeds of 150, 175, and 200 ns, family of quad 256-bit (256 x 4) static RAMs are directly TTL-compatible and use a 5-V power supply. They have common I/O and output disable, and 400-mV noise immunity. Each basic part type is available in 16-, 18-, or 22-pin DIP versions and is fabricated with ion-implanted silicon-gate MOS technology. Three-state outputs provide OR-tie capability. **Synertek,** 3050 Coronado Dr, Santa Clara, CA 95051.

Circle 241 on Inquiry Card

A-D CMOS SWITCHES

Four units are all controlled with binary input, and have on/off output voltage ratio, crosstalk between switches, and operate to 65 MHz at 10 V. Operating supply range is 3 to 18 V. MC14051 is 8-channel analog multiplexer, MC14052 is dual 4-channel analog multiplexer, MC14053 is triple 2-channel analog multiplexer, and MC14066 is quad bilateral switch. MC14051, 2, and 3 are 16-pin DIPs, with 80 dB at 1 MHz; MC14066 is 14-pin package, with 50 dB at 8 MHz. **Motorola Inc, Integrated Circuits Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721.

Circle 242 on Inquiry Card

LOW PROFILE SUBMINIATURE RELAY

Specifically designed for high density packaging and demanding operating requirements, series 1475 DC flat-pack low profile relays feature multiple convoluted contacting surfaces rated from dry circuit up to 10 A ac resistive depending on voltage. Greater capacity enables device to switch higher lamp or capacitance inrush current loads. Unit has terminals on std 0.1" grid spacing for use on PC board or card with 0.6" spacing between boards, and is available in spdt or dpdt versions. **Guardian Electric Manufacturing Co,** 1550 W Carroll Ave, Chicago, IL 60607.

Circle 243 on Inquiry Card

DC-DC CONVERTER FOR MICROPROCESSORS

Designed to power 8080-type microprocessors, model UD5722 operates from regulated 5-Vdc input and produces short-circuit protected outputs of 12 Vdc at 300 mA and −5 Vdc at −100 mA. Overvoltage protected, outputs respond smoothly to both power turn-on/off and abrupt changes of loading, without chip-destroying overshoots. Unit has 65 to 75% efficiency under nom line, full load conditions. Operating temp range is −25 to 71°C. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.

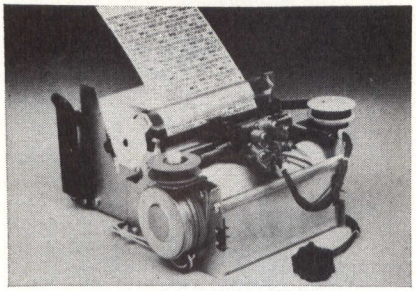
Circle 244 on Inquiry Card

INTERACTIVE GRAPHICS EMULATOR

Plug-to-plug replacement or addition to IBM interactive graphics configurations, 2250/3 is based on GP/400 graphics peripheral, which has 200-ns microprogrammed processor implementing graphics orders in firmware. GP/400 firmware package interprets and executes orders faster than the IBM does. Increased processing and vector drawing speeds permit display at 40 frames/s. The 2840/2, replacing IBM display control unit, provides local or remote attachment to 360/370 multiplexer or selector channel. **Adage, Inc,** 1079 Commonwealth Ave, Boston, MA 02215.

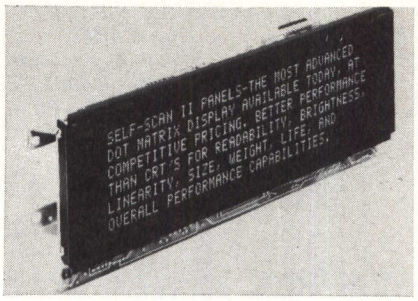
Circle 245 on Inquiry Card

DOT MATRIX ALPHANUMERIC PRINTER



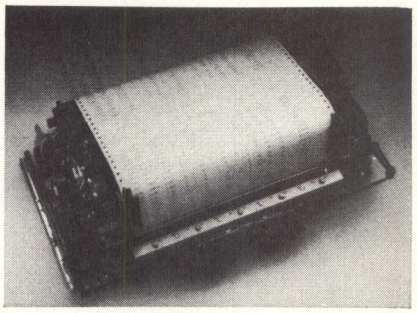
Model 7040L employs dot matrix techniques with 7-wire dots, and has 40-col capacity, multi-copy capability, 0.112″ char height, and 1.25 line/s printing speed. External electronics "clock" the print pulses to solenoids to form char of variable density and font configuration. Print wires are arranged vertically with printing element driven from right to left. Options include second motor for 5-line/s paper speed rate; and left to right printing. **C. Itoh Electronics, Inc, Systems and Components Div,** 5301 Beethoven St, Los Angeles, CA 90066.
Circle 246 on Inquiry Card

240-CHAR GAS PLASMA DISPLAY



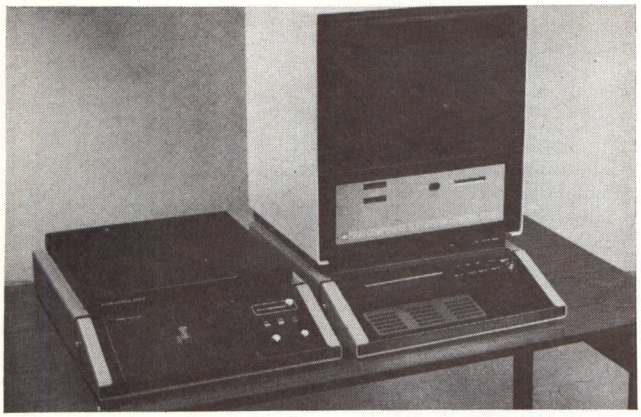
Designed for use in data terminals, flat-panel gas plasma display is arrayed in six rows of 40 char each. Panel/driver assemblies measure 11 x 4″ and are <1¼″ thick, including drive electronics, have no danger of implosion, and require no high voltage which may produce X-ray radiation hazards. 5 x 7 dot matrix char are 0.26 x 0.14″, and are readable from up to 18 ft at horizontal viewing angles up to 120 deg. Char are uniform in size, with high brightness and contrast. **Burroughs Corp, Electronic Components Div,** PO Box 1226, Plainfield, NJ 07061.
Circle 247 on Inquiry Card

132-COL TRACTOR-FEED IMPACT PRINTER



Designed especially for the OEM market, the 300-line/min. printer accommodates std fanfold forms from 4⅛ to 15″ wide, 2½ to 22″ long, and up to 6-ply. An addition to the model 40 line, the unit is available with ASCII monocase set as well as the full 96-char set for u/lc printout. An extended font feature permits sets to be increased up to 190 char. Other features include foldover, optional even or odd parity recognition, automatic new line, 2-line buffer, paper-out alarm, and built-in diagnostics. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60076.
Circle 248 on Inquiry Card

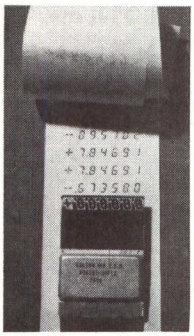
AUTOMATIC MODULE-TESTING SYSTEM



A fully automated, user programmable, bench-top system for high volume testing of multileaded devices, the 2230 evaluates, tests, and provides hardcopy data for both discrete and hybrid networks. Versatility, provided through an LSI-11 microcomputer, permits rapid mixed measurements on circuits containing resistors, capacitors, inductors, and diodes or transistors. Performance of each circuit component is measured against individually specified limits. Programs are written via the system keyboard and are automatically stored on magnetic cards. Complete I/O capabilities permit interfacing the system to automatic handlers and peripheral instrumentation. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.

Circle 249 on Inquiry Card

THERMAL PRINTHEAD



PS-015 family of non-impact 7-segment thermal printheads intended for general-purpose numeric data logging applications print a 0.155″ slanted character onto thermographic paper of various sensitivities and image color. Six configurations print from four to seven digits with the ± sign in a variety of column positions. Char printing time can be as low as 8 ms with speeds up to 3 lines/s. Nom segment resistance is 260 Ω with 5 W of pulse printing power required at 20 ms on 3M 161 paper. Char are placed along the edge of the printhead for immediate visibility of the last printed line. **Gulton Industries, Inc, Electronic Component Div,** Metuchen, NJ 08840.

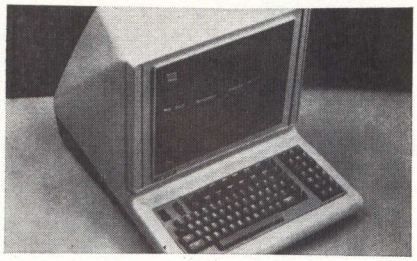
Circle 250 on Inquiry Card

800-LINE/MIN. COMMUNICATION PRINTER

A memory management capability provides for a short line throughput in excess of 800 lines/min. on the model COM printer, which interfaces to communications lines with RS-232-C, CCITT, or current loop at speeds from 75 to 9600 baud. Asynchronous reception of ASCII, EBCDIC, or Baudot codes is available with memory sizes from 512 to 1024 char. Short lines can be printed continuously at 1200 baud without requiring transmission of pad or fill characters to accomplish carriage return and line feed. A single block of 1400 char of 10-col width lines can be transmitted to the printer at 1200 baud. Line lengths can be as short as 30 char. **Hydra Corp,** 2218 Old Middlefield Way, Mountain View, CA 94043.

Circle 251 on Inquiry Card

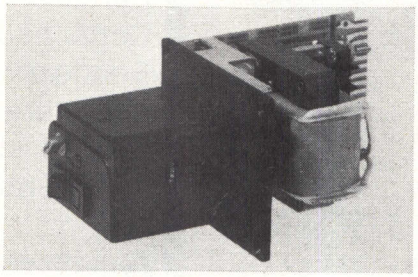
CRT COMMUNICATIONS TERMINAL



A firmware programmed, microprocessor-controlled CRT for standalone or online data entry, the 8025C operates in both normal and protected field mode, in which protected areas of form cannot be altered when variable data are inserted in unprotected blanks. Protected field capability has been extended by means of "literals transmission" which permits beginning and end of data fields to be identified by transmission control char imbedded in the field. **Omron Corp of America, Information Products Div,** 440 E Middlefield Rd, Mountain View, CA 94043.
Circle 252 on Inquiry Card

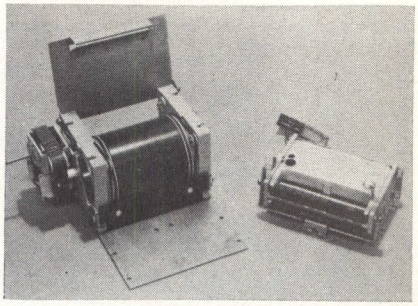
350-CHAR/s PAPER TAPE READER

Reading all std 5-, 6-, 7-, or 8-level tapes with no adjustments at 350 char/s, model 640 "Data Loader" series employs LED light sources and hermetically sealed phototransistors. Power requirement for LEDs is 12 Vdc; motor requires 115 Vac, 10 W. Available outputs are Schmitt-triggered CMOS amps and TTL-compatible drivers for 640-1; Schmitt-triggered CMOS data amps for 640-2; and phototransistors only (includes selected emitter resistors) for 640-3. **Addmaster Corp,** 416 Junipero Serra Dr, San Gabriel, CA 91776.



Circle 253 on Inquiry Card

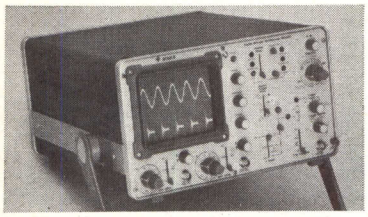
MODULAR PRINTER SYSTEM



Offering a series of rotary drum impact printers ranging from 15- to 40-col, numeric and alphanumeric, with journal and multi-slip validation capabilities, MARK II systems provide over 300 std printer mechanism combinations. Printers use a multi-column spanning hammer; each hammer prints three or four col (depending on model). Units can be mounted horizontally or vertically and have complete flexibility in use of forms including multicopy capability. Slip insertion can be either right- or left-handed. **Sheldon Printer Corp,** 1173A Grove St, Anaheim, CA 92806.
Circle 254 on Inquiry Card

DIGITAL STORAGE OSCILLOSCOPE

OS-4000 combines performance of a dual-trace, wide-band, 10-MHz triggered oscilloscope with a digital storage capability that permits the retention and flicker-free display of signals from extremely low frequency up to 450 kHz. Digital storage provides ability to view pre-trigger as well as post-trigger portions of waveforms; simultaneous viewing of stored and real-time signal; no deterioration of the stored signal display with time; flicker-free performance at low frequencies (sweep times as long as 200 s); and unattended monitoring to capture and display a transient that exceeds a preset trigger level. **Gould Inc, Instrument Systems Div,** 3631 Perkins Ave, Cleveland OH 44114.



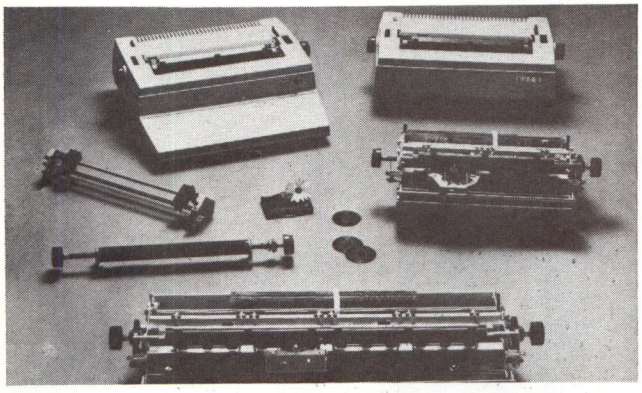
Circle 255 on Inquiry Card

MICROPROCESSOR-CONTROLLED TELEPRINTERS

PACT 200 for Telex and telegraph use over private or leased circuits and PACT 500 for data communications have operator-oriented features such as angled keyboard, optimally arranged keys and control buttons, and 50-dBA noise level. Smaller than conventional machines—16-cm (6.3") high profile—units comply fully with standards such as relevant CCITT recommendations. Features include call selection for frequently needed numbers, 1-key call repeat, tape punch while printer is online, 50-char/s print speed, electronically formed print char, electronic tabulation, and local visual and aural alarms. **Philips Telecommunicatie Industrie BV,** PO Box 32, Hilversum 1301, The Netherlands.

Circle 256 on Inquiry Card

HIGH SPEED IMPACT CHARACTER PRINTERS



A 26.4" wide print area, twice the standard size, is key feature of the WideTrack™ model in the Sprint Micro 3 series of daisywheel printers. A MOS microcomputer eliminates need for many standard electronic components and connections, providing improved performance and reliability. Unit prints 264 col at 10 char/in. and 316 col at 12 char/in. with 40-char/s speed. It also can print with proportional spacing. Other models and basic specs are 3/35—35 char/s, avg English text, std printwheel; 3/45—45 char/s, std printwheel; 3/55—55 char/s, std printwheel; 3/X30—30 char/s, metallized printwheel; and 3/X40—40 char/s, metallized printwheel. **Qume Corp,** 2323 Industrial Pkwy W, Hayward, CA 94545.

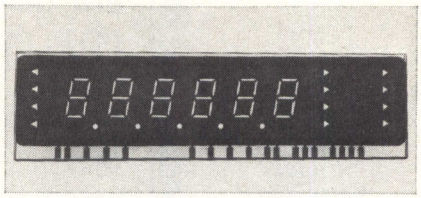
Circle 257 on Inquiry Card

MICROCIRCUIT PACKAGE

Approximately one-third smaller than conventional DIL package, Mini-Pak is a square configuration, approx ½" on a side and ⅛" thick. Microcircuit chip is mounted on top of substrate and wire-bonded to conductors which carry signals from chip to array of solder bumps formed on underside of package. A special coating protects top of chip. Package is attached to PCB by heating its perimeter and allowing solder bumps to reflow onto PCB connections. **General Instrument Corp, Microelectronics,** 600 W John St, Hicksville, NY 11802.
Circle 259 on Inquiry Card

6-DIGIT GAS-DISCHARGE DISPLAY

A 7-segment, ½" high, 6-digit display for point of sale terminals, W06-0002 also has

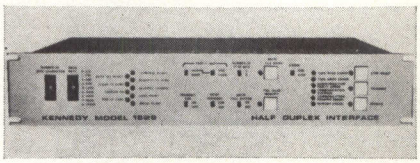


five decimal points plus 12 annuciator points which can indicate the appropriate function (sale, tax, change). Overall size is 5.2 x 1.4 x 0.25". Displays have a "halo" effect backlight, achieved through precise control of segment to segment over surface gap, to give a more continuous line for greater visibility, clarity, and contrast. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.
Circle 260 on Inquiry Card

12 X 80-COL CARD READER

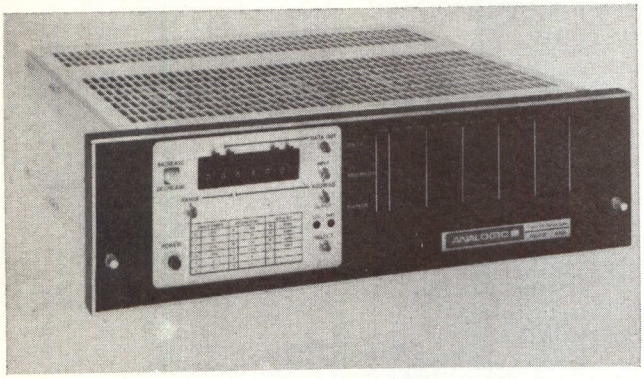
Discrete I/O terminations provide isolated circuits for test and process control for model 1280 reader. Field of 960 female spade receptacles are located at top of unit, one terminal for each switch point. Inputs and outputs can be bused in groups of 12 or 80 (horizontally or vertically) by comb-type bars which plug into desired rows or columns. Unit reads 960 bits of information from std 80 x 12 IBM punched card. **Sealectro Corp, Programming Devices Div,** 225 Hoyt St, Mamaroneck, NY 10543.
Circle 261 on Inquiry Card

HALF-DUPLEX RS-232 INTERFACE



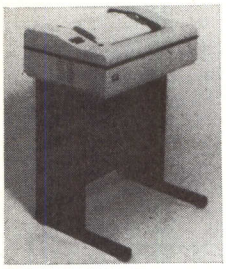
Providing complete operational control between buffered tape systems or RS-232-C compatible terminals and buffered transports without mainframe processing, model 1629 allows offline key-to-tape or tape-to-tape conversions via hardwires or telephone lines, with modems, at rates from 110 baud to 19,200 bits/s. Three transport/controller configurations accommodate varying remote data collection requirements. Tape speeds range from 10 to 125 in./s. **Kennedy Co,** 540 W Woodbury Rd, Altadena, CA 91001.
Circle 262 on Inquiry Card

DATA ACQUISITION/CONTROL SYSTEM



Both multi-channel and digital I/Os with up to 512 analog channels in a single chassis can be converted and processed by the AN5400. Based on a master chassis which holds 16 user-modules, the system can be expanded to a total of eight chassis accommodating up to 128 user-modules for a total of over 4000 high level single-ended, or over 2000 differential multiplexer channels. Low level inputs can be expanded to greater than 1000 channels. Modularity permits expansion or change from standalone data logging to complex computer-based A-D, D-A, I/O data processing, or control systems. A microprocessor with its own I/O bus executes ROM resident subroutines, and also executes programs from its own RAM or a host computer memory. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 263 on Inquiry Card

INTELLIGENT PRINTER



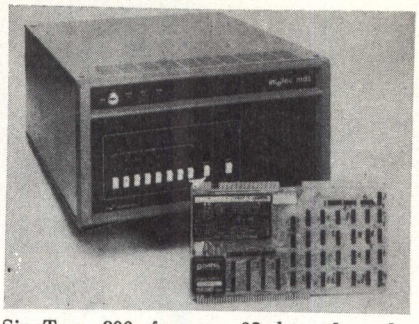
A high speed impact printer with speeds ranging from 450 char/min. for 2-col listings to 66 char/min. at 132 col, the Design 2400 uses a plug-in printhead in which a vertical column of seven pins strike the ink ribbon five times for a 5 x 7 dot matrix for each char or symbol. An Intel 8008 microprocessor provides system control. Features include buffered line for up to 180 char/s max.; tabulating capability (non-print function) at 300 char/s; black reel-to-reel ribbon with reversing mechanism (red and black is optional); matrix format 5 x 7 u/lc, 96-char, ASCII code; capability to make original plus four copies, std char set of 96 char, 10-pt type equivalent, ASCII, u/lc, with 27 ASCII graphics, and parallel I/O interface. **MI² Corp,** 1212 Kinnear Rd, Columbus, OH 43212.
Circle 264 on Inquiry Card

256K-BYTE SEMICONDUCTOR RANDOM-ACCESS MEMORY

Four modular memory cards, a timing and control card, and optional special features and custom interface cards make up model NS3, a self-contained solid-state bulk data memory system that stores 128K 22-bit words in a 5.25" (13.33 cm) high package. Card size is 11.75 x 15.4" (29.85 x 39.12 cm). Each memory card has 64K-byte max capacity. Basic storage element is the company's MM5270 4K dynamic RAM 18-pin package IC which permits all levels to be compatible with those of bipolar TTL devices. Access time is 280 ns, and cycle time for either the read or write mode is 430 ns. Read-modify-write cycle takes 610 ns plus the time needed by the user's equipment to modify the data. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

PRODUCTS

ANALOG INTERFACE CARD



SineTrac 800 features 32-channel analog input card which slides into Intel's MDS-800 or SBC-80/10 microcomputer. Card is controlled by 8080 CPU assembly language program. Three methods of programming are program-controlled mode, program-interrupt mode, and direct memory access. With one peripheral base address, on-card channel address counter automatically sequences after each conversion; stored-address first and last channel registers provide automatic recycling of channel scans. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
Circle 265 on Inquiry Card

RACK AND PANEL CONNECTOR SYSTEM

Amphenol® 17 series system, a family of miniature D-shaped connector housings, choice of contacts, accessories, and termination equipment and tools, enables selection of proper combination to meet most needs. Miniature Min Rac® plug and receptacle connectors feature rear-insertion crimp Poke-Home® pin and socket contacts. Contact/connector design permits fingertip contact insertion without aid of an insertion tool. Connectors are available in 9, 15, 25, 37, and 50 contact configurations. **Bunker Ramo Corp, Industrial Div,** 1830 S 54th Ave, Chicago, IL 60650.
Circle 266 on Inquiry Card

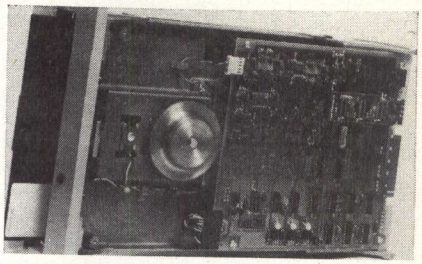
MULTI-FUNCTION CONTROLLER BOARD

For users of Data General computers, the 2804 asynchronous multiplexer board contains four asynchronous communications channels, 100-Hz real-time clock, and parallel line printer interface to Centronics, Data Products, Tally, or Printronix line printer. Board can also contain optional I/O channel for a Teletype® terminal. Switches in each channel allow baud rate selection in seven steps from 110 to 9600 baud. Cabling from backplane to DB25 connectors mounted on connector panel is std. **Media III,** 2259 Via Burton, Anaheim, CA 92806.
Circle 267 on Inquiry Card

COMPUTER DRIVE CONTROL

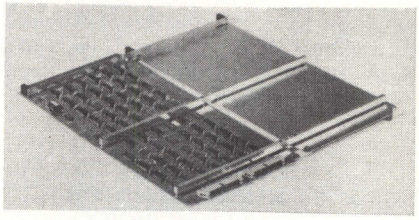
Consisting of a dc motor, digital controller, and serial interface, the control operates as a high speed stepping servo commanded by a process control computer. Modes of operation include run forward, run reverse, and computer control. A dual-speed control allows the run at high or low speed. Features include 100-Hz stepping rates, >1-hp output power, tolerance to a wide range of load inertias and frictions, selectable 800- to 8000-parts/rev motor resolutions, 200-rpm and 3-lb-ft motor speed and torque, and high positioning accuracy. **Unico, Inc,** 3725 Nicholson Rd, Franksville, WI 53126.
Circle 268 on Inquiry Card

DOUBLE DENSITY FLEXIBLE DISC DRIVE



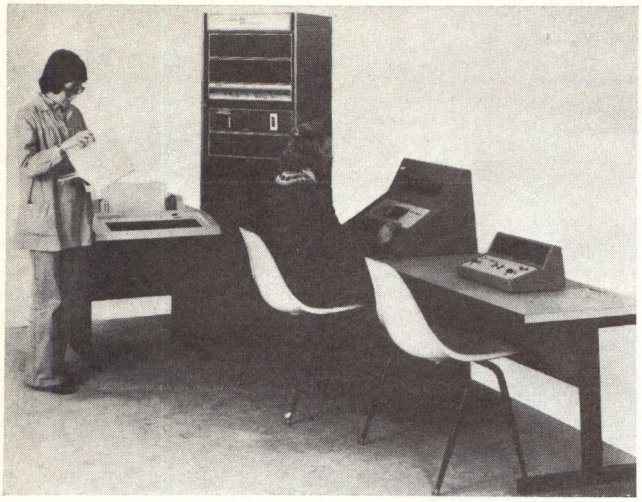
Adaptable to MFM and M²FM encoding techniques, -110 disc drive accommodates up to 6.4M bits of data on one side of std media, for double density applications. Single density storage in variable formats provides up to 3.2M bits of data. Fully IBM compatible, unit reads and writes 3740-formatted diskettes for up to 1.9M bits. Drive offers one to four drive daisy-chain capability, parallel ready lines plus unit select, separation of clock and data, and track 00 sensing. **General Systems International, Inc,** 1440 Allec St, Anaheim, CA 92805.
Circle 269 on Inquiry Card

I/O BUS CONVERTER



RTP7410/63 is contained on a single PC board that plugs into a half controller slot in Interdata model 70, 74, 80, 7/16, 7/32, or 8/32 computers. Converter allows the company's complete RTP family of analog and digital I/O measurement and control equipment to be operated under the control of the computer involved using std I/O instructions. Up to eight controllers can be connected to one converter in chain fashion using RTP I/O cables. **Computer Products,** 1400 NW 70th St, PO Box 23849, Fort Lauderdale, FL 33307.
Circle 270 on Inquiry Card

SEMICONDUCTOR TEST SYSTEM



Controlled by PDP-11 central processors, Impact II systems test all popular discrete semiconductors and linear ICs. Each system is custom assembled to fit requirements, but can be reconfigured later if the user's needs change. Depending upon options chosen, the system can be assembled for wafer testing, engineering evaluation, production testing, incoming inspection, or high reliability testing and sorting. Options are available for devices such as power FETs, 4-layer diodes, DIACs, PUTs, and opto-isolators. Software uses simple, English-language programming of configurations and tests. **Lorlin Industries, Inc,** Precision Rd, Danbury, CT 06810.

Circle 271 on Inquiry Card

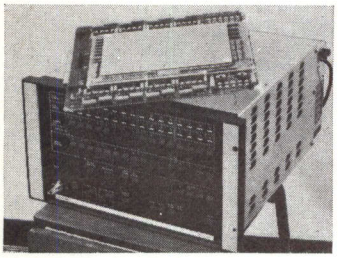
MICROPROCESSOR-BASED TELECOMMUNICATIONS TERMINAL

Control of Micro Net™, an ASR terminal that can simultaneously access TWX, Telex, Timeshare, DDD satellite, private lines, and computers through simple instructions entered from its 4-row typewriter keyboard, is maintained by microprocessor. An operator does not need to learn complicated operating procedures to use the standard format keyboard. Message preparation is standardized on one network tape and printed automatically on the terminal. Automatic features include time/date stamp, keyboard dialing and redialing, and mini-buffer mode that allows the user to create a short message in the buffer memory and send it automatically without using tape. **Sidereal Corp,** PO Box 1042, Portland, OR 92707.

Circle 272 on Inquiry Card

SECOND SOURCE MINICOMPUTER SYSTEMS

Nucleus Packages, intended as alternates for GA SPC-16 minicomputers, are based on the Enhancer I. EI/16-RT, designed for real-time, disc-based applications, includes 32K of 16-bit memory, controller for up to four cartridge discs, and serial I/O for teleprinter or CRT; -DB also has controller for line printer, card reader, and card punch, and permits speeds of 300, 600, and 1200 lines/min.; -D3 has 32K words of main memory, controllers for fixed or removable discs, and up to four CRT terminals, and line speeds program-selectable from 100 to 9600 baud; and -D4, an augmented version of the -D3 with 48K of core, has controllers for 25.6-byte disc. **Datum Inc,** 1363 S State College Blvd, Anaheim, CA 92806.



Circle 273 on Inquiry Card

SURVEY OF MICROPROCESSOR/ MICROCOMPUTER BUYERS

The publishers of COMPUTER DESIGN and the leading industrial market research company INTERNATIONAL DATA CORPORATION announce a significant new market research report entitled:

Survey of Microprocessor/ Microcomputer Buyers

7000 COMPUTER DESIGN readers were surveyed to determine:

- the type of equipment using μPs/μCs they are currently designing.
- the μP/μC models selected and the criteria for the selection
- the memories selected and the criteria for the selection.
- peripherals used with the equipment.
- various aspects of software and test.
- opinions on current μPs/μCs and peripherals.
- recommendations for their improvement.
- future plans for using μPs/μCs

and much more.

The 150 page report contains more than 50 tabulations of data from the survey, many of them correlating use factors and selection criteria with type of equipment. Each table is accompanied by an explanation of its meaning and an interpretation of its significance.

For a more detailed description of the report, circle 120 on the Reader Inquiry Card,

or write

Survey of Microprocessor/
Microcomputer Buyers

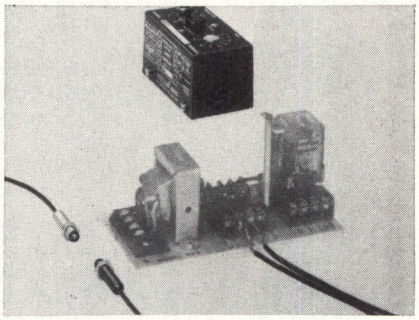
Computer Design
Market Research Group
143 Swanton St.
Winchester, MA 01890

PRODUCTS

LOW PROFILE RELAY

Type RU115 has one changeover (form C) contact, with continuous contact rating of 6 A at 120 Vac general purpose resistive, or 1/10 hp at 120 Vac. Rated breaking capacity is 10 A at 2200 VA. PC mountings are on 0.1" grid pattern. Rated coil voltages range from 5 to 110 Vdc. Measuring 1⅛ x ¾ x ½", relay comes in clear plastic dust cover. Std contact material is silver-cadmiumoxide to withstand high currents and reduce wear. Relay can be mounted and will operate in any position. **Schrack Electrical Sales Corp,** 1140 Broadway, New York, NY 10001.
Circle 274 on Inquiry Card

PHOTOELECTRIC SYSTEM



Modularized MB-3 system offers modulated LED scanning with high sensitivity amplification, and interfaces directly with the company's logic modules. System can be used in new applications or can be added to current systems through a simple plug-in replacement of existing amps. The system can be used in dirty air (smoke, dust, oil, or fog) at distances up to 6 ft. By modulating the current to the miniature hermetically sealed LED scanner, ambient light does not influence performance. **Banner Engineering Corp,** 9714 10th Ave N, Minneapolis, MN 55441.
Circle 275 on Inquiry Card

12- AND 16-STATION KEYBOARDS

Low profile, short stroke keyboards have plastic bezels and 2-shot ⅜" keys. Both 12- and 16-station models are furnished with 0.025" sq pins either top or bottom mounted, and are available in either binary or single contacts. Keyboards having single contact switches use two std switching matrices: 1-col, all keys out, and row/col. For binary switching, std matrix is row/col with 1-common to all switches. Other features include tactile/audible feedback and gold or silver epoxy screened PC boards. **Bowmar Instrument Corp,** 8000 Bluffton Rd, Fort Wayne, IN 46809.
Circle 276 on Inquiry Card

SURFACE TEMPERATURE SENSORS

Dual bimetal design of VE sensors produces a large force and contact motion; intimate coupling between mounting base and actuating elements provides fast response time. Contact chatter is eliminated and the unit has no resonant points below 2000 Hz. Sensors can be either factory set (0 to 150°C, 32 to 300°F) or unsealed for field adjustment. Setting tolerance is ±5°F (±3°C), sensitivity is 60°F (33°C) per setting-screw turn. Contact can be open on rise or close on rise. **Warren G-V Communications, div of Sola Basic,** 101 Okner Pkwy, Livingston, NJ 07039.
Circle 277 on Inquiry Card

100-LED LINEAR ARRAY

Featuring dense packaging of individual LED chips, and internal wiring of LEDs to minimize the number of external connections needed for multiplex operations, the array provides 100 LEDs on 0.020" centers, requires only 20 external connections, and has a 0.125" thick profile. The unit consumes 3.2 W, is compatible with ICs, and is end-to-end stackable to form arrays 4, 6, 8, or 10" long. The long life unit is available in red, green, yellow, and infrared. **Digital Components Corp,** 1111 E Elizabeth Ave, Linden, NJ 07036.
Circle 278 on Inquiry Card

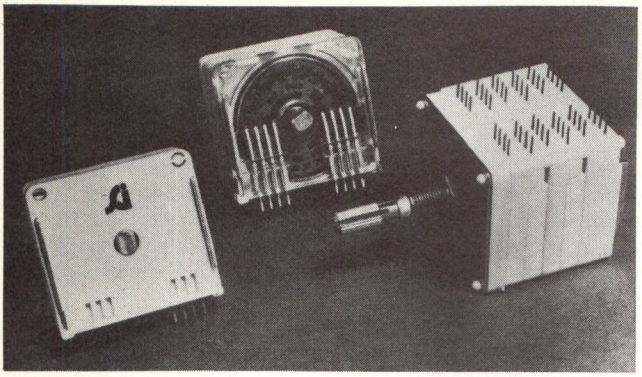
DIGITAL ANALYZER

Model 80-M records and displays up to eight channels of digital signals on any conventional oscilloscope, operating at speeds to 12-MHz input frequency. Variable threshold makes the unit suitable for a range of logic families; spike detection and word recognition are std features. Memory function stores a 1024-bit record for each channel. Record function triggers the device on preselected word, trace, or external trigger source. An illuminated indicator shuts off when the predetermined event occurs. **Digital Broadcast Systems, Inc,** Brentwood Lane, PO Box 381, Madison, AL 35758.
Circle 279 on Inquiry Card

SINGLE-OUTPUT POWER SUPPLIES

QPS series incorporates features such as barrier block interface and socketed IC regulator. Specs include line and load regulation of 0.10%, ripple and noise of 1-mV rms. All units are protected against overloads and short circuits and have an overvoltage crowbar as an accessory. QPS-1 is rated at 5 Vdc at 3.0 A or 6 Vdc at 2.5 A; -2 at 12 Vdc at 1.5 A or 15 Vdc at 1.2 A; and model -3 is rated at 24 Vdc at 1 A. **Deltron, Inc,** Wissahickon Ave, North Wales, PA 19454.
Circle 280 on Inquiry Card

PROGRAMMABLE ROTARY ENCODED LOGIC SWITCH

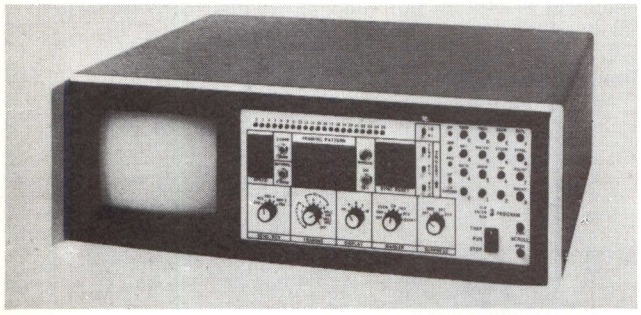


An alternative to conventional rotaries for manual switching of complex binary codes, the P/rel™ switch is fully programmable up to 60 detent positions. A specially processed PC disc provides full programming to the user's truth table and allows for the use of any code. Features include modular stacking for multi-layer operation; snap together, enclosed housing which resists contact contamination due to solder flux; 1⅝ x 1½" detent with a dual ball starwheel design to provide positive indexing and longer life; up to 20 PC or solder terminals on 0.100" centers; and front-plated metal plate and shaft. **Standard Grigsby, Inc,** 920 Rathbone Ave, Aurora, IL 60507.
Circle 281 on Inquiry Card

150-ns 4K RAM

In addition to 150-ns access time, the MK 4027-2 offers "gated-CAS," which provides a timing window at a full 25% of overall access time to compensate for timing skews that may be encountered in the multiplexing operation. Output of the RAM will source 5 mA and sink 3.2 mA in addition to driving 100-pF capacitance load. Inputs to the 16-pin device are TTL-compatible (<5 pF capacitance), permitting use with high performance ECL or Schottky TTL memory systems. Std power supply tolerance is ±10%. The device is capable of page-mode timing and RAS-only refresh cycles as well as the usual read, write, and read-modify-write cycles. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 282 on Inquiry Card

COMMUNICATIONS CHANNEL DIAGNOSTIC UNIT



Features of the model D-501 member of the Datascope family include some not usually found on a portable test instrument. A programming language designed specifically for dealing with data communications problems permits recognition of extremely complex information patterns in a full-duplex data stream; 2000-char buffer allows data surrounding events of interest to be captured and scrolled backward and forward on the 5", 375-char screen; programmed event counter allows complex occurrences to be counted up to 9999; and an external control feature allows capture of a buffer-full of data on command from an external electrical signal. **Spectron Corp,** Church Rd & Roland Ave, Mt Laurel, NJ 08057.
Circle 283 on Inquiry Card

LITERATURE

Spike Characteristics

Describing test equipment and setups, bulletin, complete with diagrams and chart, helps to determine spike and transient susceptibility characteristics of computers and peripheral equipment. **Solar Electronics Co, div of A. T. Parker, Inc,** Hollywood, Calif.
Circle 300 on Inquiry Card

Subminiature Switches

Electrical and mechanical specs of pushbutton, toggle, and rocker DIP switches for PCB applications are detailed in brochure including photos, schematics, and diagrams. **Control Switch, a Cutler-Hammer Co,** Folcroft, Pa.
Circle 301 on Inquiry Card

Readout Devices

Details of LED, incandescent, and neon modules available as components, systems, or packages are described and illustrated in selector guide. **Dialight, a North American Philips Co,** Brooklyn, NY.
Circle 302 on Inquiry Card

Network Measurement System

National Bureau of Standards report describes interpretation and statistical treatment of data acquired by network measurement machine component of network measurement system. Send $1.15 (plus 25% if foreign) for C13.46:897 to Superintendent of Documents, **US Government Printing Office,** Washington, DC 20402.

IEEE/ASTM Standard on Metric System

Serving as basic guide, U.S. source book on metric system measurement lists units, scientific and technical applications, selection, and conversion, plus section on style and usage. IEEE Std 268-1976 is available from **IEEE,** 345 E 47th St, New York, NY 10017; or ASTM E380-76, from **ASTM,** 1916 Race St, Philadelphia, PA 19103. Price is $4.

Microcomputer and Memory Products

Containing 12 sections, data catalog covers RAMs, ROMs, serial memories, memory support circuits, software, and time keeping circuits, in addition to memory, development, and microcomputer systems. Send $2 check or money order to Marketing Services, **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95050.

Paper Tape Punch

Specs, timing chart, and diagrams of mechanism, connector pin assignments, and dimensions of 6110 punch are presented in leaflet. **Epson America, Inc,** Torrance, Calif.
Circle 303 on Inquiry Card

Optical Character Recognition System

Discussions of features, applications, and product specs of Laser OCR-ONE are furnished in illustrated brochure. **Optical Business Machines, Inc,** Melbourne, Fla.
Circle 304 on Inquiry Card

Speed/Torque Systems

Containing illustrations, graphs, and tables, detailed, expanded catalog features application and selection information on permanent magnet systems, drives, and accessories. **Bodine Electric Co,** Chicago, Ill.
Circle 305 on Inquiry Card

Power Supplies

Tables and drawings in bulletin on model HE237, and catalog on encapsulated supplies provide features and detailed tech specs. **Computer Products, Inc,** Fort Lauderdale, Fla.
Circle 306 on Inquiry Card

Magnet and Resistance Wire

Technical booklet covers range of magnet wire film insulations, and physical and electrical properties of resistance and heating element alloys. **Magnet Wire Supply Co,** Chatsworth, Calif.
Circle 307 on Inquiry Card

IC Packaging Panels

Fold-out short form pamphlet consists of dimensions, descriptions, and photos of available types of panels, pins, sockets, connectors, racks, and boards. **Excel Products Co Inc,** New Brunswick, NJ.
Circle 308 on Inquiry Card

Data Communication Switches

Arranged as pictorial indexes, two compact catalogs help to select series 5000 and 5700 switches, which are pushbutton and toggle actuated, respectively. **T-Bar Inc,** Wilton, Conn.
Circle 309 on Inquiry Card

Power Supplies and Systems

Illustrated brochure offers descriptions, specs, and options of series PT rack-mounting supplies, and multiple and redundant output systems. **Acopian Corp,** Easton, Pa.
Circle 310 on Inquiry Card

Protection Systems Tapes

Describing applications, specs, and features, pocket guide outlines in chart form the properties of 12 types of resilient tapes. **3M Co, Industrial Specialties Div,** St. Paul, Minn.
Circle 311 on Inquiry Card

Optical Page Readers

Three pamphlets outline features, specs, and typing and editing information for models 101, 102, and 103. **Context Corp,** Burlington, Mass.
Circle 312 on Inquiry Card

Digital Control Valve

Specs, descriptions, and programming information for smart valve package are discussed in 8-page foldout bulletin which provides diagrams, photos, and charts. **Digital Dynamics, Inc,** Sunnyvale, Calif.
Circle 313 on Inquiry Card

DC Power Supplies

Flyer supplies general specs and features of Slim Line supplies, with dimensional drawings of 32 and 42 series. **Standard Power, Inc,** Santa Ana, Calif.
Circle 314 on Inquiry Card

PCB Connectors

Organized by contact centers, illustrated catalog containing cross-referenced index specifies characteristics, materials, contact terminations, and mounting styles of connectors. **Viking Industries, Inc,** Chatsworth, Calif.
Circle 315 on Inquiry Card

Rotary Motion Control Elements

Drawings and charts are used in engineering catalog, which provides technical specs, plus selection and installation information for preassembled modules, controls, and power supplies. **Electroid Co,** Union, NJ.
Circle 316 on Inquiry Card

Switching Regulator

Specs, dimensional drawings, and features are included in bulletin describing 673 series of three output power supplies for computer systems. **Trio Laboratories, Inc,** Plainview, NY.
Circle 317 on Inquiry Card

High Voltage Power Supplies

Illustrated data sheet gives general, typ operating, and mechanical specs, and application data on 4000 series multiple output supplies. **CPS, Inc,** Sunnyvale, Calif.
Circle 318 on Inquiry Card

Ceramic Capacitors

Contained in short form catalog are rating tables, typ performance curves, and mechanical and electrical characteristics of various types of Monolythic[R] capacitors. **Sprague Electric Co,** North Adams, Mass.
Circle 319 on Inquiry Card

Microcircuits and Modules

Presented in data sheet format with diagrams, tables, and drawings, products guide details specs, hook-up packaging, and applications information and instructions. **Teledyne Philbrick,** Dedham, Mass.
Circle 320 on Inquiry Card

Data Acquisition Systems

Specs on modular AN5400 series are available in 22-page technical data brochure with sections covering microprocessor, cards and modules, typ configurations, and applications. **Analogic International,** Wakefield, Mass.
Circle 321 on Inquiry Card

PC Card Cages, Guides, Retainers, Extractors

Brochure offers design and application data, as well as features, dimensional information, and specs on electronic packaging products. **Calmark Corp,** San Gabriel, Calif.
Circle 322 on Inquiry Card

Resistors

Technical information on precision/power wire-wound resistors, networks, and special products is furnished in catalog which features Mil-style cross reference chart. **RCL Electronic Div, AMF Inc,** Manchester, NH.
Circle 323 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

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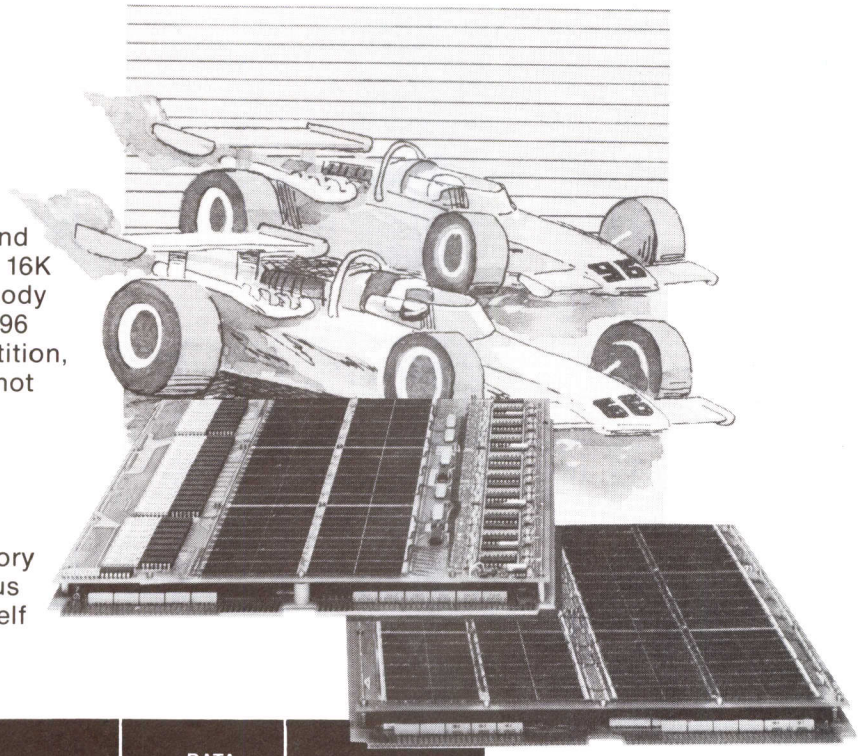
Who's the performance winner in 16k and 32k memory systems?

Check the specs.



Fabri-Tek has packed more speed and total performance into single-board 16K and 32K memory systems than anybody else in the business. Compare our 696 and 698 systems against the competition, and you'll see what we mean. We'll not only beat them in specifications—we're the only company that offers you total upward compatibility to 32K. At competitive prices, too. It's what you'd expect from a company with years of leadership in the memory business. Go with the winner—call us today for the best in both off-the-shelf and custom memory systems.

	FABRI-TEK		EMM		DATA PRODUCTS		DATARAM	
MODEL	696	698	Micro 3000 D.D.	Micro 3000 Q.D.	Store 1680		DR-103	DR-103
MEMORY SIZE	16K	32K	16K	32K	16K	32K	16K	32K
CYCLE TIME	650	650	650	850	650		650	750
ACCESS TIME	250	250	270	300	280		265	300
PHYSICAL SIZE	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0	11.75x15.4 x1.0		11.5x13.7 x1.0	11.5x13.7 x1.0
COMPATIBILITY 16K TO 32K	YES		NO		NO		NO	

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Fine print quality, graphics versatility and high speed tabbing.

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Diablo

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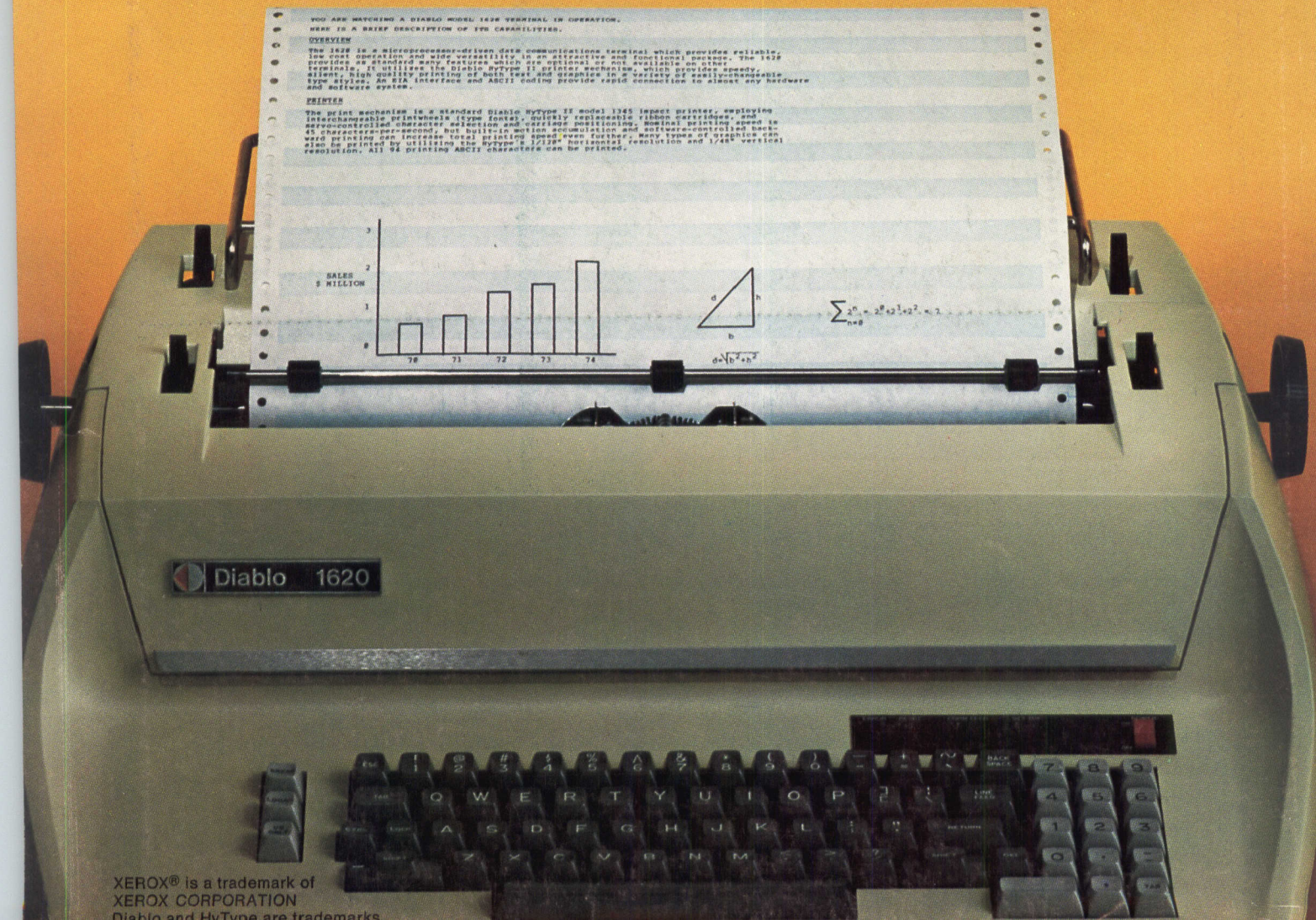
CIRCLE 78 ON INQUIRY CARD



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