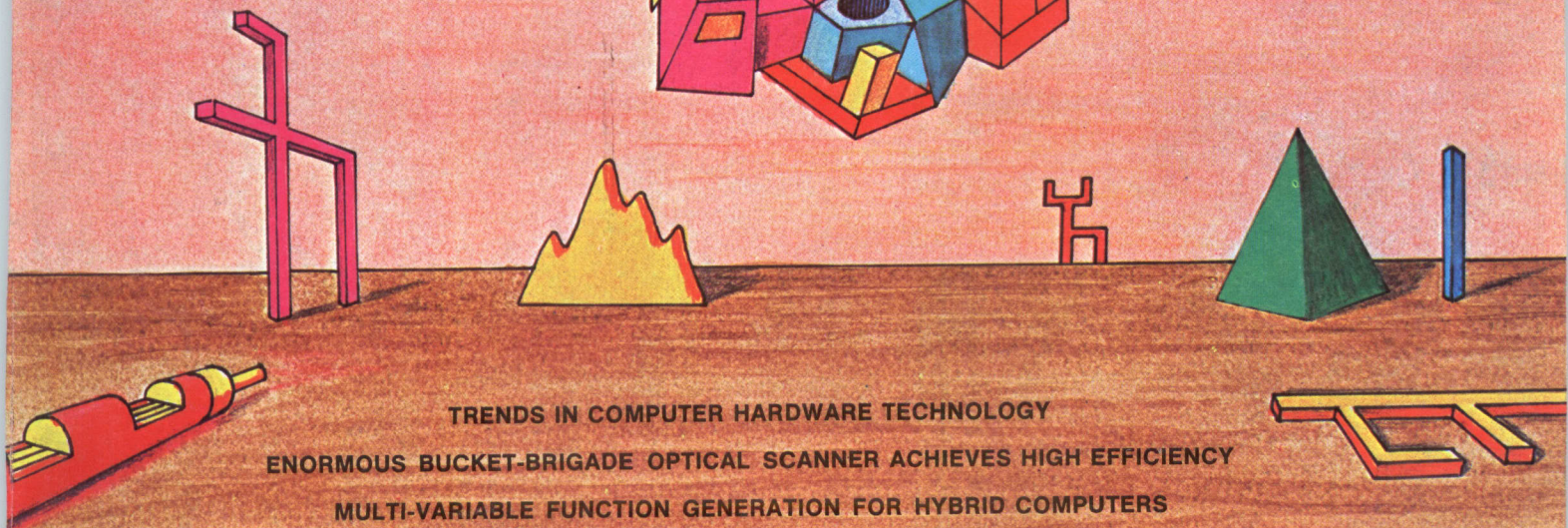


COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

FEBRUARY 1976

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TRENDS IN COMPUTER HARDWARE TECHNOLOGY

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MULTI-VARIABLE FUNCTION GENERATION FOR HYBRID COMPUTERS

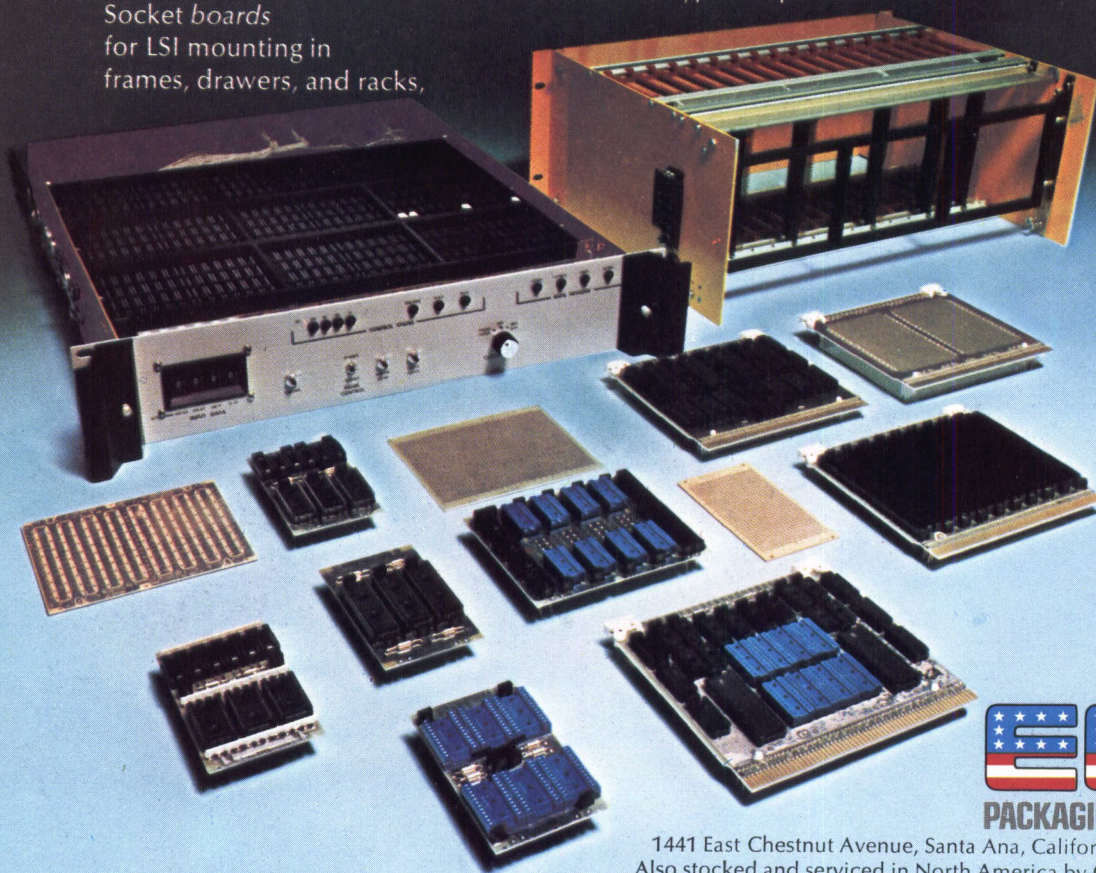
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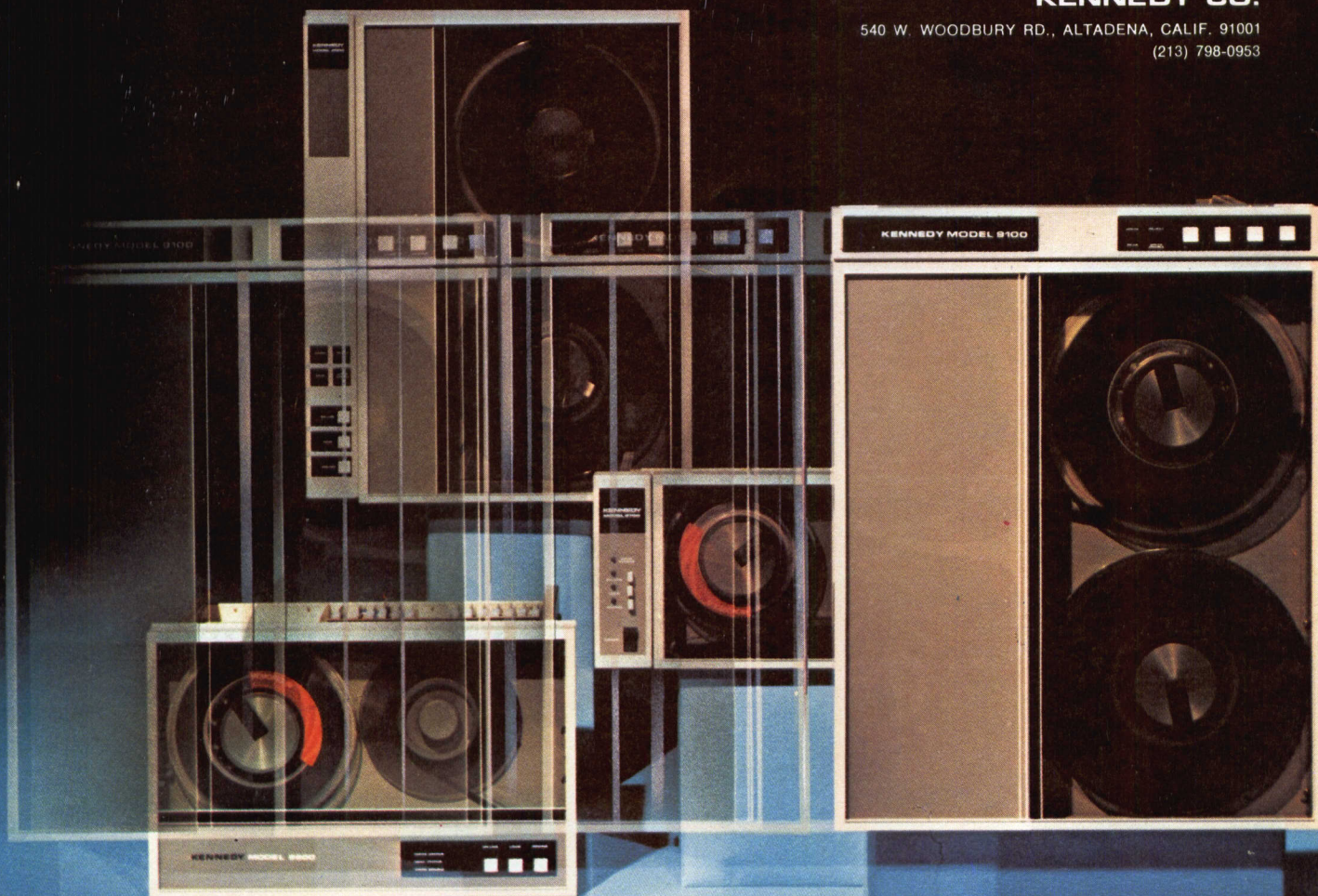
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CIRCLE 3 ON INQUIRY CARD

THE
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COMPUTER
DESIGN

FEBRUARY 1976 • VOLUME 15 • NUMBER 2

FEATURES

67 COMPCON 76 SPRING

This year's IEEE Computer Society International Conference will explore recent advances in circuit technology as well as ideas still on the drawing boards in trying to predict their effect on the computer industry during the next five years

77 TRENDS IN COMPUTER HARDWARE TECHNOLOGY

by David A. Hodges

Rapidly evolving technologies have resulted in greatly increased reliability, and significantly lower costs. Future technological advances should have an even greater impact when applied to overcome existing limitations of I/O and communications hardware

**89 ENORMOUS BUCKET-BRIGADE OPTICAL SCANNER
ACHIEVES HIGH EFFICIENCY**

by Barry J. Deliduka

Probing its way into existing and new applications, the solid-state sensor consumes little power, can capture an entire picture, needs no mechanical scanning, and operates at low cost. Here, it is applied in the form of a very large-area optical scanner

**99 MULTIVARIABLE FUNCTION GENERATION
FOR HYBRID COMPUTERS**

by Arthur I. Rubin

Permitting faster than real-time simulation of functions of four or more variables for design studies, a truly analog multivariable function generator frees both hybrid computer programmer and end-user analyst from concerns over phase-error-induced instabilities introduced by inadequate program performance

108 TOOLS FOR LOGIC ANALYSIS

by Jim Wagner

Although development of powerful logic analyzers has led to predictions of its demise, the oscilloscope still serves as a significant tool in troubleshooting logic problems

**118 MULTI-LEVEL NESTING OF SUBROUTINES
IN A ONE-LEVEL MICROPROCESSOR**

by Philippe de Marchin

Nested subroutines can be handled with the aid of a microprocessor's scratchpad memory, which is used as an automatically expandable stack register

**138 SINGLE UNIT CARD READER/PRINTER
SERVES AS LOW PRICE I/O DEVICE**

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DEPARTMENTS

6 CALENDAR

10 LETTERS TO THE EDITOR

**12 COMMUNICATION
CHANNEL**

**18 DIGITAL TECHNOLOGY
REVIEW**

38 DEVELOPMENTS

**50 DIGITAL CONTROL AND
AUTOMATION SYSTEMS**

**128 MICRO PROCESSOR/
COMPUTER DATA STACK**

142 PRODUCTS

168 LITERATURE

**169 GUIDE TO PRODUCT
INFORMATION**

172 ADVERTISERS' INDEX

Reader Service Cards
pages 173-176



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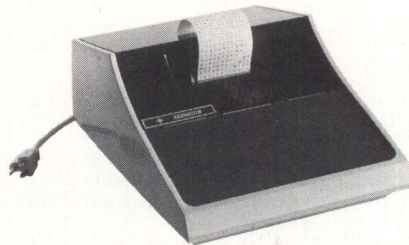
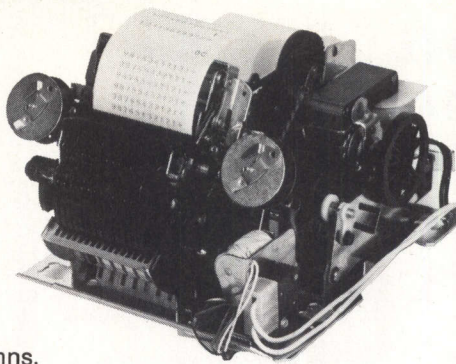
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CONFERENCES

Mar 2-3—Federal DP Expo '76, Sheraton Park Hotel, Washington, DC. **Information:** Robert E. Harar, Instrumentation Fair, Inc, 5012 Herzel Pl, Beltsville, MD 20705. Tel: (301) 937-7177

Mar 2-4 (Boston), **Mar 9-11** (New York City), **Apr 13-15** (Chicago), **May 4-6** (Los Angeles), **May 11-13** (San Francisco)—CompDesign/76 Tour. **Information:** Jack Edmonston, The Conference Co, 797 Washington St, Newton, MA 02160. Tel: (617) 965-5800

Mar 4-6—ACM Conf on Programming Micro/Minicomputers, Delta Towers Hotel, New Orleans, La. **Information:** Assoc for Computing Machinery, 1133 Ave of the Americas, New York, NY 10036. Tel: (212) 265-6300

Mar 8-10—IEEE Conf on Industrial Electronics & Control Instrumentation (IECI '76), Sheraton Hotel, Philadelphia, Pa. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 644-7500

Mar 9-11—Electro-Optics/Laser Internat'l Exhibition, Brighton, England. **Information:** British Information Services, 845 Third Ave, New York, NY 10022. Tel: (212) 752-8400

Mar 10-12—1st Nat'l IEEE Control of Power Systems Conf and Exp, Oklahoma City. **Information:** Randolph Frost, 7824 Northwest 28th Terrace, Bethany, OK 73008. Tel: (405) 236-7339

Mar 17-19—9th Annual Simulation Sym, Tampa. **Information:** Ira M. Kay, Southern Simulation Service, Inc, PO Box 22573, Tampa, FL 33622. Tel: (813) 839-5201

Mar 25 (Orange County, Calif), **Apr 13** (Cleveland, Ohio)—Invitational Computer Conf. **Information:** B. J. Johnson & Assoc, 300 Otero, Newport Beach, CA 92660. Tel: (714) 644-6037

Apr 5-7—IEEE Region 3 Conf & Exhibit (SOUTHEASTCON), Clemson House, Clemson U. **Information:** Dr J. T. Long, Gen'l Chm, E & CE Dept, Clemson U, Clemson, SC 29631. Tel: (803) 656-3376

Apr 5-8—Design Engineering Show/Amer Soc of Mechanical Engineers Conf, McCormick Pl, Chicago, Ill. **Information:** Clapp & Poliak, Inc, Management, 245 Park Ave, New York, NY 10017. Tel: (212) 661-8410

Apr 7-9—IEEE Reg 6 Conf on Energy for the Future, Braniff Place Hotel, Tucson, Ariz. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 644-7500

Apr 12-14—IEEE Internat'l Conf on Acoustics, Speech, and Signal Processing, Marriott Hotel, Philadelphia, Pa. **Information:** Institute of Electrical & Electronics Engineers, 345 E 47th St, New York, NY 10017. Tel: (212) 644-7500

Apr 20-22—Sym on Computer Software Engineering, Barbizon Plaza Hotel, New York City. **Information:** Jerome Fox, Exec Sec'y, MRI Sym Comm, Polytechnic Institute of New York, 333 Jay St, Brooklyn, NY 11201. Tel: (212) 643-2393

Apr 20-22—Internat'l Reliability Physics Sym, Caesar's Palace, Las Vegas, Nev. **Information:** C. H. Zierdt, Jr, IRPS Publ Chm, Bell Laboratories, 555 Union Blvd, Allentown, PA 18103. Tel: (215) 439-7500

Apr 22-24—Milwaukee Sym on Automatic Computation & Control, U of Wisconsin-Milwaukee. **Information:** MSACC-76, U of Wisconsin, College of Eng & Applied Sci, Milwaukee, WI 53201

Apr 26-27—7th Annual Pittsburgh Conf on Modeling and Simulation, University of Pittsburgh. **Information:** William G. Vogt or Martin H. Michle, Modeling and Simulation Conf, 231 Benedum Engineering Hall, U of Pittsburgh, Pittsburgh, PA 15261

Apr 26-27—8th Annual Southeastern Sym on System Theory, U of Tennessee, Knoxville. **Information:** Dr Peyton Z. Peebles, Electrical Engineering Dept, The University of Tennessee, Knoxville, TN 37916

Apr 26-28—Electronic Components Conf, Jack Tar Hotel, San Francisco, Calif. **Information:** Tyler Nourse, Electronic Industries Assoc, 2001 Eye St NW, Washington, DC 20006

Apr 27-28—24th Annual Nat'l Relay Conf, Oklahoma State U, Stillwater. **Information:** School of Electrical Engineering, Engineering Ext 301 EN, Oklahoma State University, Stillwater, OK 74074

Apr 27-29—Internat'l Sym on Circuits and Systems, Technical U of Munich, Fed Rep of Germany. **Information:** Institute of Electrical & Electronics En-

gineers, 345 E 47th St, New York, NY 10017. Tel: (212) 644-7500

Apr 27-29—Internat'l Optical Computing Conf, Capri, Italy. **Information:** IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

May 11-15—Exhibit of Computers, Related Equipment, and Systems, U.S. Trade Center, Milan, Italy. **Information:** Donald T. Mathes, Project Officer, Office of International Marketing, DIBA, Rm 1012, US Dept of Commerce, Washington, DC 20230. Tel: (202) 967-3957

May 18-20—COMPEC Europe '76, Centre International Rogier, Brussels. **Information:** Trident Confs & Exhibs Ltd, Abbey Mead House, 23a Plymouth Rd, Tavistock, Devon PL19 8AU, England

May 25-28—6th Internat'l Sym on Multiple-Valued Logic, Utah State U, Logan. **Information:** Dr Stephen Y. H. Su, Electrical Engineering Dept, Utah State University, Logan, UT 84322. Tel: (801) 752-4100, X7806

SEMINARS

Mar 11-12—Uninterruptible Power Systems, U of Wisconsin, Milwaukee. **Information:** Univ of Wisconsin-Ext, Dept of Engineering, 929 N Sixth St, Milwaukee, WI 53203. Tel: (414) 224-4181

Mar 28-Apr 2—System Design Using Micro/Minicomputers, Minicomputers—Principles and Applications, Microcomputers—Principles and Applications, Pheasant Run Lodge, St. Charles, Ill. **Information:** National Engineering Consortium, Inc, 1301 W 22nd St, Oak Brook, IL 60521. Tel: (312) 325-5700

SHORT COURSES

Feb 25-26 (New York City), **Mar 2-3** (Chicago), **Mar 31-Apr 1** (Washington, DC), **Apr 6-7** (Dallas, Tex), **Apr 13-14** (San Francisco)—Microprocessors and LSI in Telecommunications Applications; **Feb 27** (New York City), **Mar 4** (Chicago), **Apr 2** (Washington, DC), **Apr 8** (Dallas), **Apr 15** (San Francisco)—Software Development Techniques for Microcomputers. **Information:** Julie Schneider, Integrated Computer Systems, PO Box 2368, Culver City, CA 90230. Tel: (213) 559-9265

Feb 25-27—Microcomputers/Microprocessors in Instrumentation Systems, Louisiana State University. **Information:** Dr J. L. Hilburn or Dr P. M. Julich, Electrical Engineering Dept, Louisiana State U, Baton Rouge, LA 70803. Tel: (504) 388-5241

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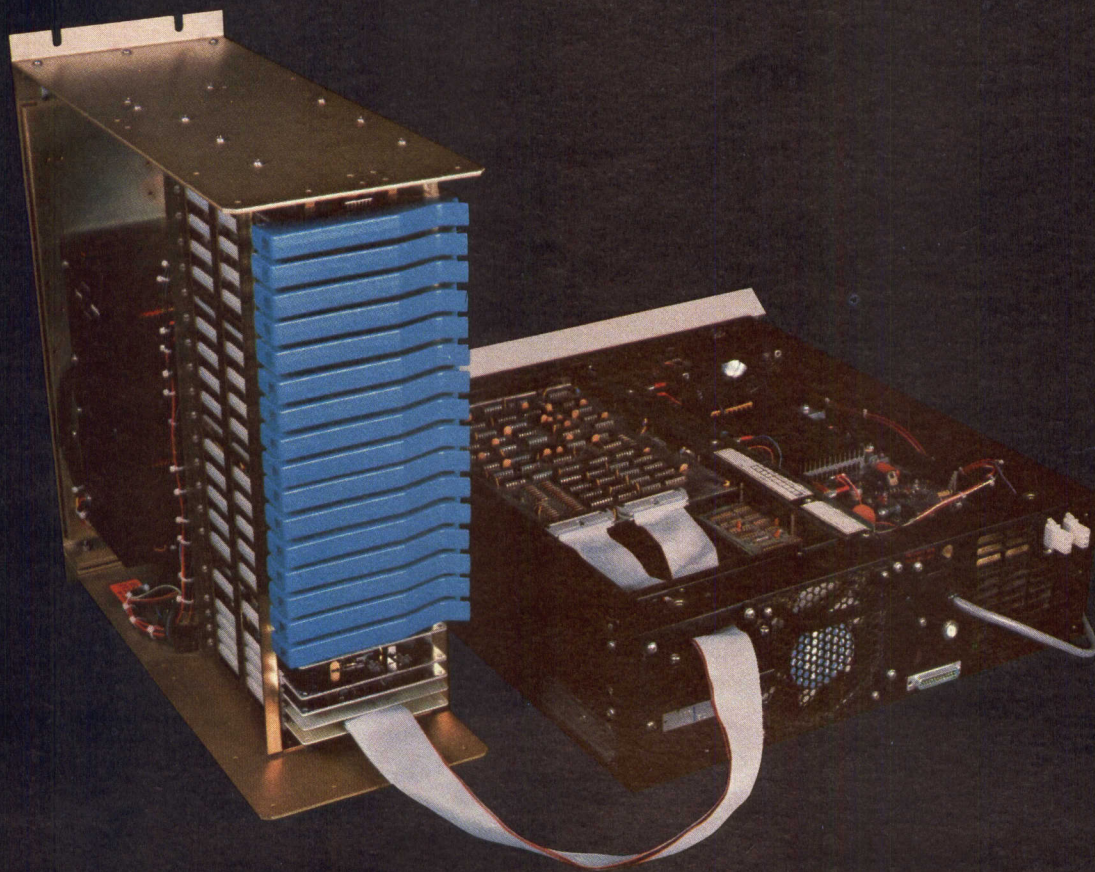
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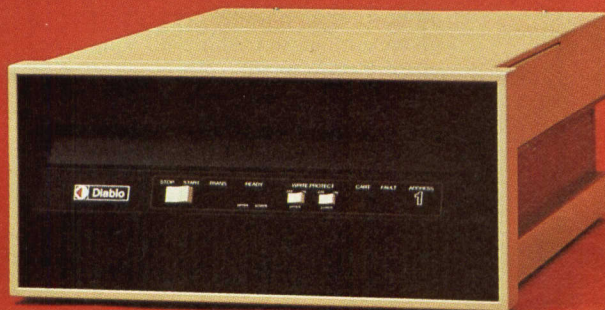
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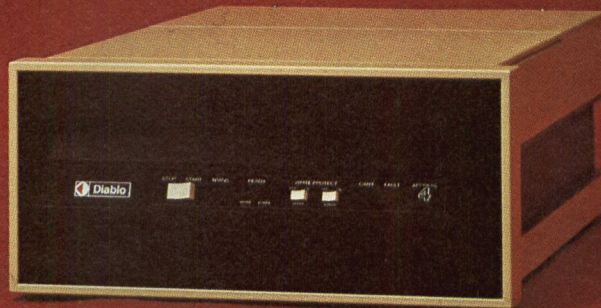
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LETTERS TO THE EDITOR

To the Editor:

I was interested to read the article by Pandeya and Cassa ("Parallel CRC Lets Many Lines Use One Circuit," Sept 1975) concerning a parallel method of accumulating cyclic redundancy codes (CRCs). The main reason for my interest was that I was in the process of preparing an article myself on the same topic, but based on a design of mine which is currently implemented in the ICL 7950/2 and /3 multiplexers of the 7950 series equipment.

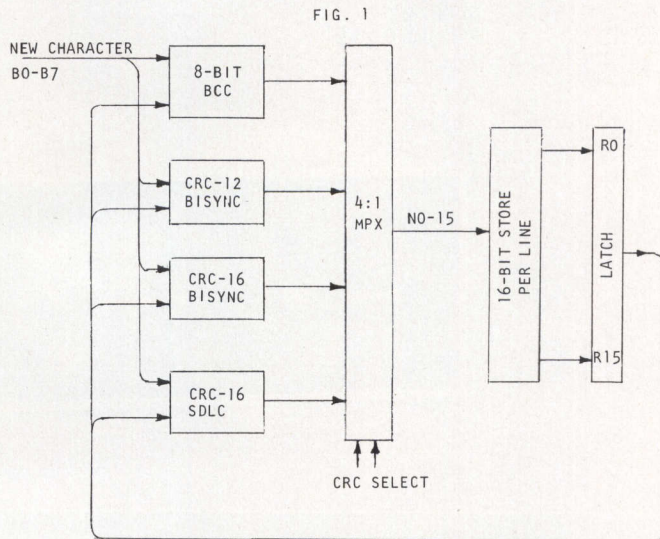
Since my design is now about four years old, the method proposed by Pandeya and Cassa can hardly be described as "new," although I have not come across any other documents describing the "parallel" approach. While their article described the basic principles and hinted at certain ad-

vantages, it did not extend the concept far enough.

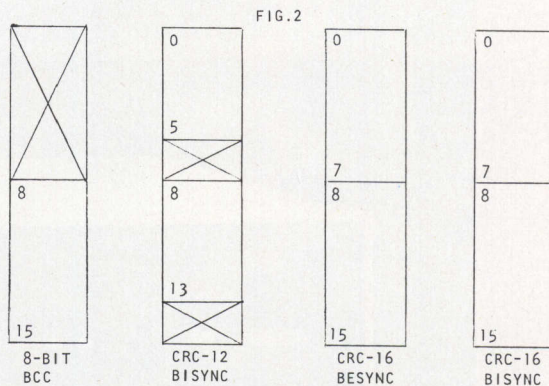
As they suggest, the parallel method is ideally suited to multiplexers where a common circuit can be time-shared between several channels, but multiplexers are also suited to having a mix of different types of line. With the ICL 7950/2 and /3, each channel can be separately configured under software control, and, hence, circuits for all three CRCs are provided, together with circuits for the more conventional Block Parity Check (BCC) accumulation. [The BCC method for 8-bit data is also a CRC of the form $(x^8 + 1)$.]

Fig. 1 shows how the generator circuits and store are configured.

By allocating the storage register bits as shown in Fig. 2, the generator functions for the four different CRCs can be formed by a series of



Note: The CRC referred to as SDLC is also used as the CCITT polynomial for character-oriented systems.



Note: 16-bit store usage for each type of CRC.

cascaded exclusive-ORs similar to those listed by Pandeya and Cassa. [Space does not permit these functions to be listed here.—Ed.] These functions show a high degree of commonality in sub-terms, considerably reducing the total logic for generating all four functions. In fact, the logic uses approximately 30 exclusive-OR elements (apart from 4:1 multiplexers.)

Thus, by more carefully considering a typical application of the parallel method of accumulation, a very efficient, fast, and reasonably flexible design can be achieved.

A further extension of this design allows the use of 5-, 6-, 7-, and 8-bit codes with BCC, which would use only the required number of terms of each function, and inhibit the others.

D. R. Whitby
6 Horsham Rd
Bedfont, Middlesex
TW14 8LW England

The Author Replies:

I thank Mr Whitby for extending our work on parallel CRC to software-selectable CRC. The scope of our article was 'parallelism of CRC' and did not include rather trivial hardware of multiplexers and registers around the parallel circuit. For a given application where all four types of CRCs are needed, the multiplexing is indeed a good idea.

As to Mr Whitby's comments on "new" approach, I maintain that our work was authentic, original, and independent. In case Mr Whitby's claims of originality and date of conception are valid, it is not the first time in history that two parties have independently conceived the same idea. Incidentally, in the particular case of SDLC, the specific CRC polynomial (and the unique techniques of its implementation) which is an IBM protocol was not universally known four years ago.

Arun K. Pandeya
Data General Corp
Southboro, Mass

To the Editor:

I would like to let anyone who is experimenting with building his own computer system, or microprocessor, know that I would like to communicate with him, and swap ideas, software, and hardware.

I am currently building two microprocessors using Intel 8080 and Moto-

rola 6800 chips. I would also like to swap or sell (for storage and shipping cost) an IBM line printer, card reader, and tape drive that came off the famous S.A.G.E. Air Defense computers that the Air Force operates. I bought the machines when the Air Force closed its S.A.G.E. Air Base in New York.

I also have a large scale Univac Series 70 computer up and running. It has six tape drives, 140K memory, 1000-line/min. printer, and a 600-card/minute reader. I would like to make it available to experimenters and novices for \$10 per run. I am putting together a guide for the Univac for \$5 and a complete programming course, including audio cassettes, for \$25. The programming courses will cover COBOL RPG, FORTRAN, and BASIC—the major computer languages. I am also planning an Intel 8080 and Motorola assembly language course kit. I am developing an interpreter for my Univac so that 8080 and 6800 assembly programs can be developed, for convenience of the novice, on a large-scale computer. If anyone is interested in helping with the simulator or other compilers/translators, please let me know.

Milton Goodman
President
Techno cadimum Data Corp
101 Park Ave
New York, NY 10017

To the Editor:

[Regarding Jack Dennon's "Letter to the Editor" (Oct 1975, p 8) with respect to his difficulty in obtaining universal asynchronous receiver/transmitters (UARTs)], I recently ordered three UARTs from Diplomat Electro-Com, a Minneapolis, Minn distributor representing Western Digital. They arrived by mail three *days* later. Can't beat that! Mr Dennon should change suppliers!

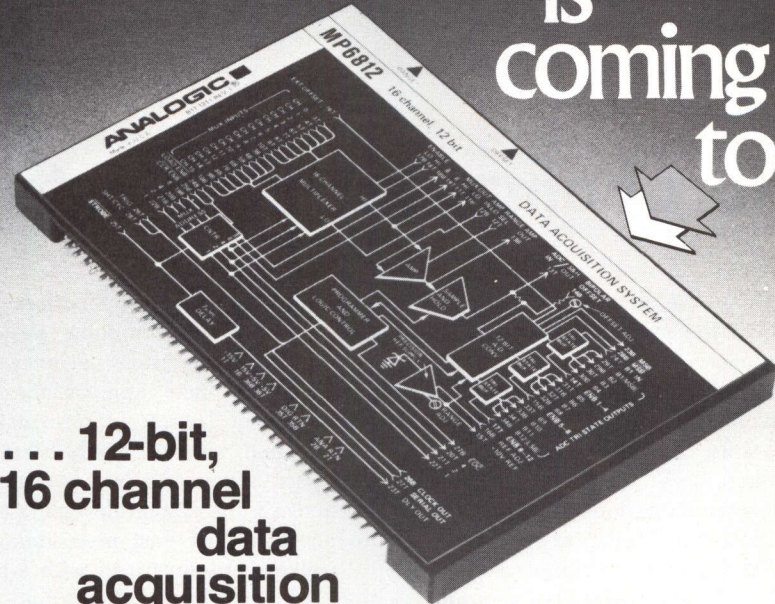
Myron A. Calhoun
Computer Science Dept
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by **John E. Buckley**
Telecommunications Management Corp
Cornwells Heights, Pa.

Microcomputer Converter

Throughout the short yet significant history of the microcomputer—from an engineering novelty to a viable information system component, this column has discussed its potential applications, the most valuable of which has been said to be within the telecommunications environment. As a peripheral adjunct to otherwise static remote terminal devices, the microcomputer provides, economically, a major degree of logic flexibility. Remote terminal manufacturers are rapidly adopting the microprocessor to provide basic control logic. Rather than offering totally programmable terminals, the initial application of the microcomputer in a terminal environment has been primarily to provide fixed, programmed logical devices.

Recently, microcomputer-based "subcompact" computer systems have been introduced by various manufacturers. These systems have typically taken the form of small business-application processors with limited storage and input/output peripheral capabilities. They are intended to function as free-standing business computing systems with minimal communications capability. Typically, their processing logic is configured with parallel microprocessors, thereby compensating for the relatively slow execution time of the microprocessor, yet creating the illusion of a comparable overall-task execution time.

To many observers, these domains are the only envisioned applications of the microcomputer. This replacement of discrete logic designs with fixed-program microcomputers in remote terminal devices is presently

considered its major application. The design of small computer systems with a communications peripheral is currently the new applications implementation. Design of information systems and associated subsystems is heavily influenced by traditional methods. Some system designers tend to merely repeat past methodologies or system configurations with which they are familiar, rather than re-examine them in light of current technological developments. There are a number of long-time requirements within an information system that could not be resolved with past technologies, and therefore compensating techniques had to be implemented. Unfortunately, today's system designers tend to forget these original compromises and accept the compromise technique of methodology as absolute.

Such has been the assumption that the centralized host computer system must provide compatibility with the various codes, protocols, and data rates of its connected remote terminals. Supposedly, the remote terminal is permitted to transmit to the host computer interface the code, protocol, and data rate native to the remote terminal; and, since the host computer is the citadel of "unlimited" processing capability, the host will adapt to the remote terminal's uniqueness and perform the necessary conversion to its native environment.

This myopic perspective results in the user's data processing management issuing decrees that only a certain type of terminal can be connected so that only one code, protocol, and, hopefully, one data rate

need be supported by the host computer system. This unfortunate decision limits the available remote terminal devices that may be employed for particular applications. When major computer and terminal manufacturers announce new protocols for their future terminal product lines, the system user can only reluctantly prepare for another round of replacements and conversion to an updated system.

Ideally, maximum efficiency of a centralized computer center would be achieved if a single code, protocol, and data rate could be assured without the need to limit selection of remote terminal equipment. In a multi-application environment, the use of different types of terminals is mandatory in order to realize a totally effective information system. This fact of data processing unfortunately requires that the central computer devote a significant portion of its resources to provide operational compatibility to a number of codes, protocols, and data rates.

Through use of microcomputer technology, development of a microcomputer converter has recently been announced by DBS, Inc of Nashua, NH as a new information-system component. Located between the digital equipment and its modem, it performs the required code, protocol, or data rate conversion. It is intended to permit existing data centers to maintain support of a common data code, protocol, and data rate, yet utilize newer and more diversified remote terminal equipment. In addition, present data centers that are burdened with multiple terminal support can reduce this requirement to a minimal support program resident within the computer center.

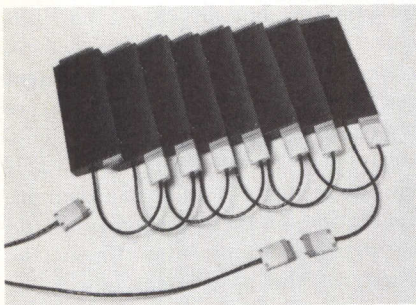
The satisfaction of this application requirement is unique to microprocessor technology. While the requirement has always been present, earlier semiconductor technologies prohibited, for economical reasons, any practical solution. The microcomputer converter is based on a microprocessor-controlled metal-oxide semiconductor (MOS) memory array. Controlled by programmed instructions resident in programmable read-only memories, the converter controls a minimum of two Electronic Industries Association (EIA) interface controllers. These interfaces provide serial connections between the remote terminal and its

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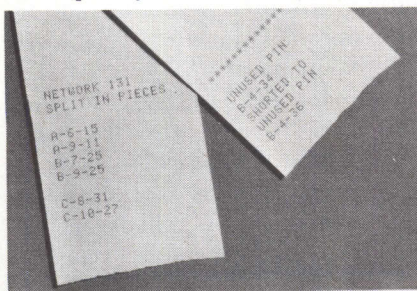


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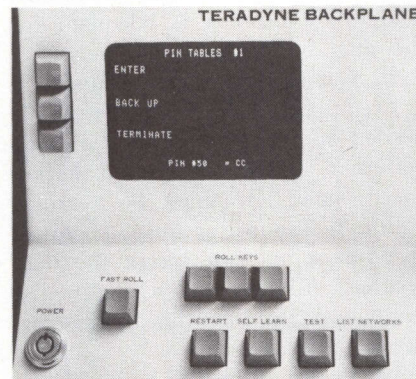
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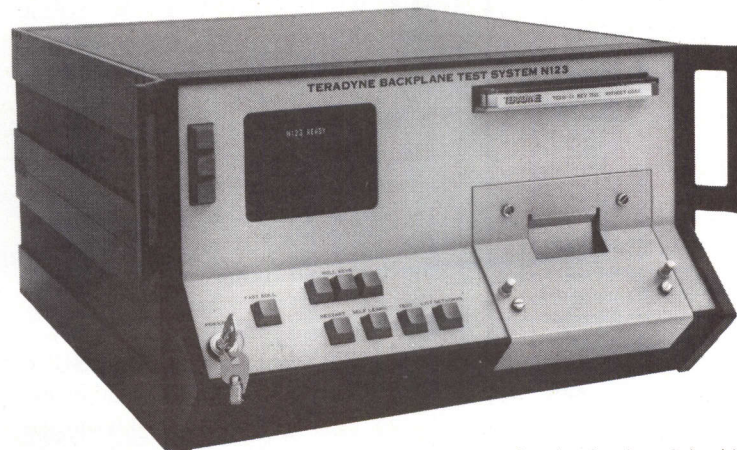
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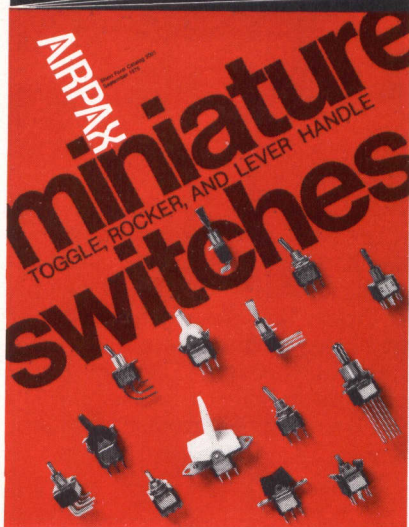
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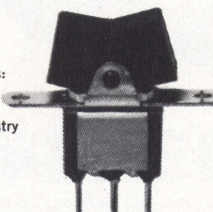
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associated modem if the converter is to be located at the remote terminal site. An alternate location for the converter is to permit the communications channel to operate under the native characteristics of the remote terminal and interface between the communications channel's computer center modem and the computer's communications peripheral interface; this appears to be more desirable from physical control and support aspects.

The basic converter is, in effect, two operating microprocessor systems, each programmed for a specific data code and protocol. A 4K to 8K MOS memory provides the program execution environment as well as the necessary transient data storage. Assuming that data terminal and central processor data rates are equivalent, the need for extensive storage capacity can be avoided. The MOS memory is adequate for the dual buffering requirements.

If a major data rate conversion is required, auxiliary storage is needed for the data rate reduction activity. The incoming and higher speed data flow must be retained within the converter until the lower speed terminal can accept the data volume. Addition of a floppy-disc peripheral provides this storage capacity.

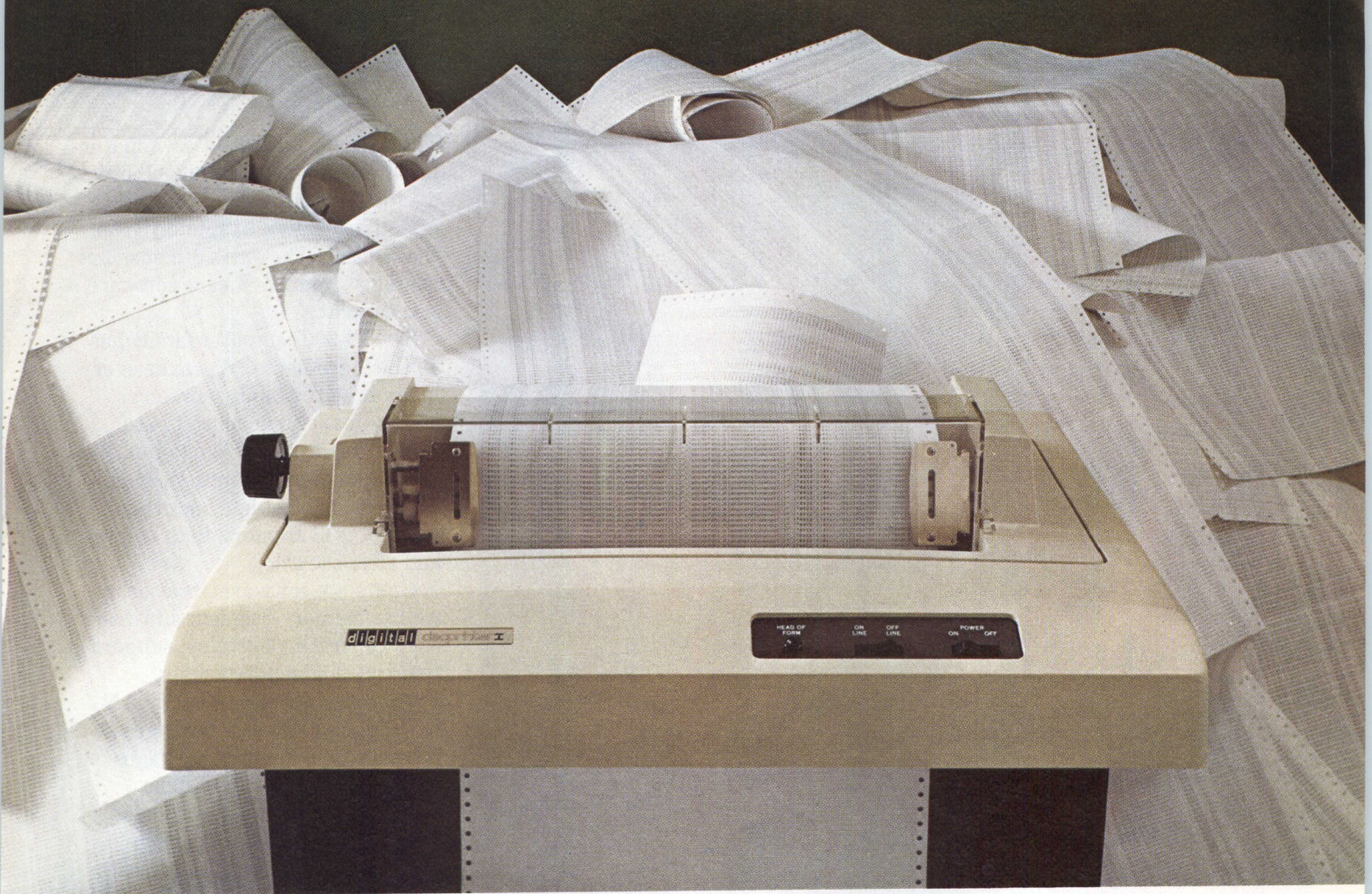
Use of multiple EIA interfaces, which can be added to the converter, permits expansion to include a concentrator function. A number of low speed remote terminals can be interconnected or connected via the converter which will operate with the appearance of a single terminal using a standard protocol and data rate. Within the data block content, individual low speed terminal identification and addressing can be recognized and routed by the converter.

The initial application area envisioned for such a converter is Synchronous Data Link Communication to Binary Synchronous Communication (SDLC-BSC) conversion. Many medium and large scale data processing systems have been programmed to support BSC procedures. With IBM's announcement of SDLC procedures, it can be reasonably anticipated that future remote terminals from that company, as well as devices from independent terminal manufacturers, will reflect these new protocol requirements. If present

BSC data processing systems are to be expanded with new SDLC terminals, without the need to replace their existing remote BSC terminals, the only choice is to install SDLC support within the data processing system. Considering a microcomputer converter of the type described here, BSC support uniformity can be maintained within the data processing center while the remote terminal population comprises both BSC and SDLC terminals.

It is reasonable to expect that the use of microcomputer converters will become even more common as future applications develop. An additional use is with respect to packet-switching systems provided by either a value-added carrier, such as Telenet, or a private intelligent network. Primary obstacle in the development and implementation of such networks is the degree of protocol sensitivity resident within each node of the network. One approach in packet-switching network design has been to attempt to make the node protocol-transparent; but this is not possible, since any protocol requires control responses as well as data content responses. The control responses are typically established with time constraints at the remote terminal. If the node were totally transparent, generation of these responses would be dependent upon the timely delivery of the associated data block to the destination computer center. The ensuing network transmission time would therefore impact these timing requirements. To design the node to full protocol processing significantly limits the acceptable remote terminal types. Through use of a microcomputer converter, however, the node can be implemented with full support of a native protocol. A variety of remote terminal types can be utilized if each terminal has a properly programmed converter associated with its communications channel.

The range of applications for such a converter is limited only by diversification of the information system environment. As long as new data codes and protocols are being developed, coupled with the desire to minimize the multiple support requirements of the central processor, such converters will be mandatory for any expanding computer communications system. □



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These packaged systems provide a flexible method of implementing early project development. These include the low-priced 990/4 Program Development System and the powerful 990/10 Program Development System. The 990/10 system combines the power of



the 990/10 minicomputer with the disc-based DX10 operating system and an extensive set of software development tools. The standard package includes the 990/10 minicomputer with 64K bytes of error-correcting memory, ROM loader and diagnostics, 3.1-million byte removable disc kit with accompanying peripherals, and a complete software development package. And, at \$24,500, this system costs at least 20% less than comparable equipment from other manufacturers.

For developing firmware modules, there is a \$5950 prototyping system which includes a 990/4 computer with 16K bytes of memory and programmer's front panel, and a "Silent 700*" twin-cassette ASR data terminal. Also, an optional PROM programming kit is available for developing read-only memory.

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CIRCLE 11 ON INQUIRY CARD

17

Disc Drive Innovations Provide Flexibility for System Designers

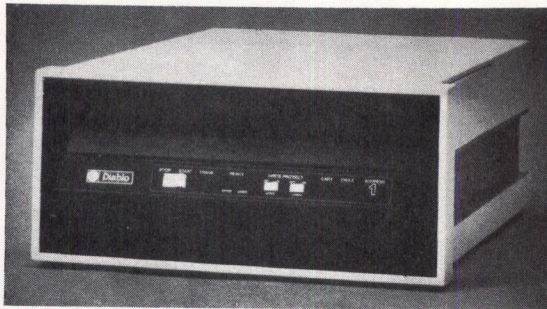
Significant design advances incorporated in a family of disc drives are claimed to result in a price/performance "breakthrough" for small- to medium-scale computer systems. Among the innovative features are a dual head-positioning mechanism based on an inertial actuator, a motor-generator set that replaces the usual internal power supply, a servo-following technique that eliminates the need for special alignment packs, and use of a microprocessor to control logic functions.

Initially, eight Series 400 disc drives—front- and top-loading models each of 13.3-, 26.6-, 40-, and 53.3-megabyte/drive capacities—are being offered by Diablo Systems Inc, 24500 Industrial Blvd, Hayward, CA 94545. Prices range from under \$2500 to just under \$3600 in OEM quantities; single unit prices would be about 60% higher.

Although traditionally any one disc drive has met the requirements of only a particular application, the flexibility of this series suits nearly all applications. System designers are provided with a broad range of storage capacities with total compatibility of interface, media, technology, and transfer rate. Upgrading to higher capacity drives can be accomplished quickly without the need to write new software, change to a different technology, or redesign cabinets, interfaces, or controllers.

Both sides of the disc are used; the dual head-positioning mechanism permits independent movement of two head positioners per disc drive, effectively placing two disc drives in a single machine since this doubles the throughput. One can be seeking at the same time that the other is reading or writing. The drive on the fixed disc can operate with or without the removable disc in place.

Design of the dual inertial actuators eliminates conventional large magnetic fields. Operating power consumption (10 W) is about 2% of that associated with traditional voice-coil positioners, and weight of the dual system is about 40% of that of a single voice-coil actuator. In addition, inertial actuators are far more precise in positioning than a voice-



Compact Series 400 disc drives announced by Diablo Systems are 8.75" in height and fit a standard 19" rack. Both front- and top-loading models will be available in four capacities from 13.3 to 53.3 megabytes. Total power consumption of 1/5 to 1/2 that of other common drives will reduce heat stress and result in increased overall reliability

coil system. There is no need for periodic preventive maintenance, realignment, or replacement.

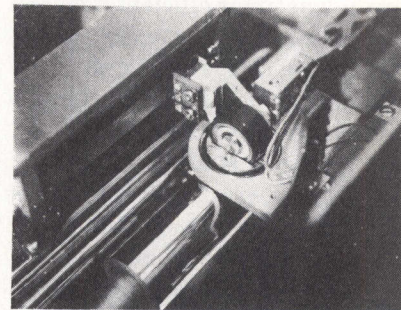
Power source is a single motor-generator set which converts ac to dc and requires virtually no filtering. Low power consumption of the inertial actuator and high efficiency of the power supply (about 80%) reduce heat generation to a small fraction of that produced by internal power supplies in conventional disc drives.

Since there is no electrical connection between generator and ac source, the possibility of electrical noise transients affecting disc drive operation is eliminated. Protection against brownouts or short power fluctuations is also provided by the inherent inertia of the motor-generator. The drives will continue to operate unaffected for 150 ms after a complete loss of power—long enough for programs or volatile memory to be unloaded on the disc drive.

Total power consumption is 200 W, versus 400 to 1000 W for drives now in common use. This not only minimizes component failure due to heat, but also permits operation over a broader temperature range (50 to 104° F, 10 to 40°C). Overall drive reliability is therefore increased.

Use of a servo track-following positioning system eliminates the need for special head alignment packs. Servo data are prerecorded on each data track and interspersed in the unused sector area between data fields. The recording head aligns itself with the servo data and, therefore, with the data to be recorded by the user. Since each data head is self-aligning on each data track, the drive will operate under tolerance and environmental ranges nearly twice those of comparable disc drives.

A microprocessor is included as an integral part of disc drive logic, and



Dual head-positioning mechanism in Series 400 disc drives, based on an inertial actuator, allows independent movement of two head positioners per drive. One positioner can be used for seeking while the other is reading or writing

is shared between the two actuators. Diagnostic programs can be run on a plug-in memory to locate any problem down to the functional block in the circuit board. As a further advantage, the microprocessor provides the flexibility to change the interface and to add drive functions.

Initial prototypes of Series 400 disc drives are scheduled for the first quarter of 1976. Large quantity production is expected in the third quarter.

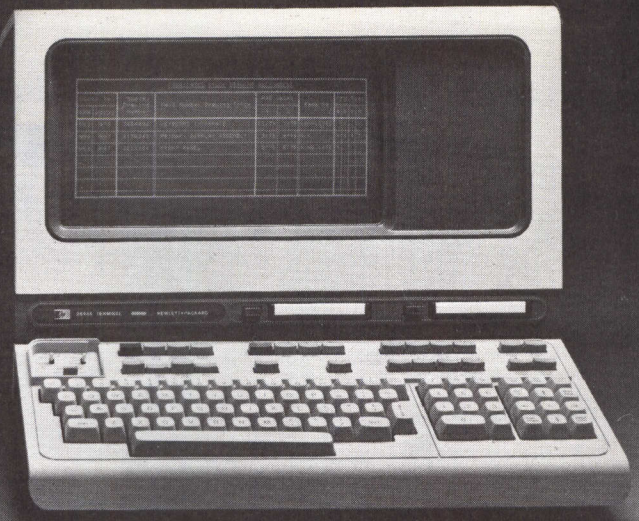
Circle 140 on Inquiry Card

Full Redundancy Assures Non-Stop Operation of Transaction-Type System

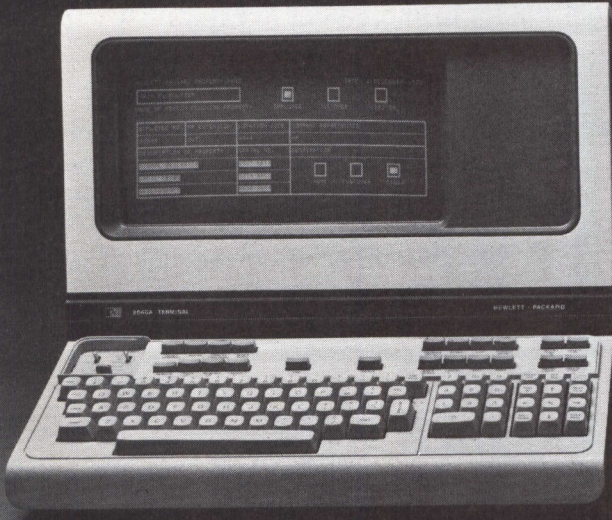
Until now the privilege of fail-safe computer operation has been available only to very large facilities or those in which a subsystem failure might endanger life or property. For such users, the added cost and, some-



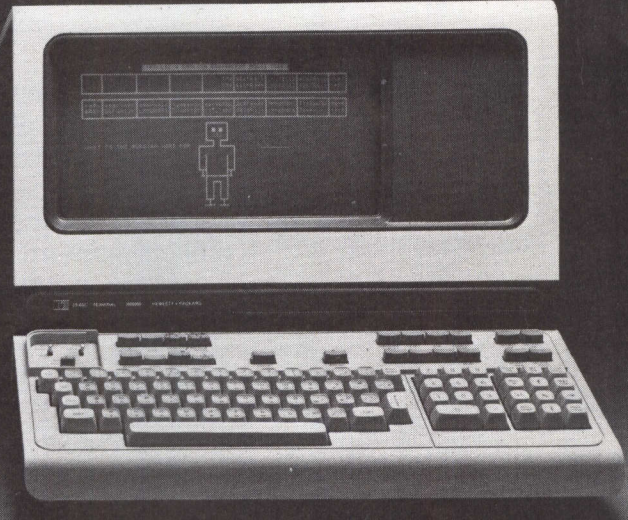
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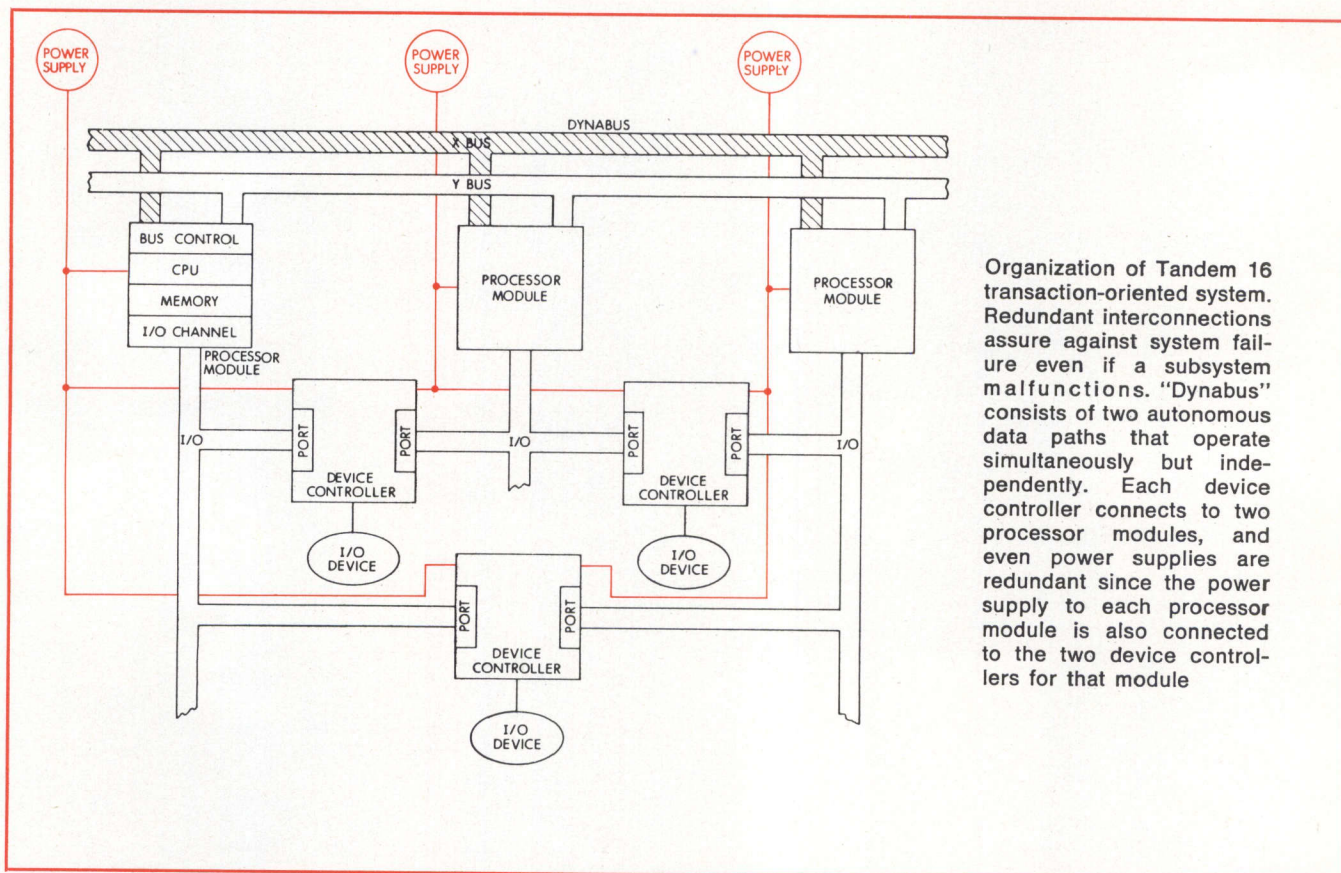
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Organization of Tandem 16 transaction-oriented system. Redundant interconnections assure against system failure even if a subsystem malfunctions. "Dynabus" consists of two autonomous data paths that operate simultaneously but independently. Each device controller connects to two processor modules, and even power supplies are redundant since the power supply to each processor module is also connected to the two device controllers for that module

times, reduced speed were accepted because of the intolerable alternatives that might result, for instance from failure of the computer in a single-processor system. Other users, however, were expected to put up with occasional failures since such failures would not likely result in disastrous situations.

This dilemma need no longer exist, according to the manufacturers of a "NonStop" computer system recently announced. James G. Treybig, president of Tandem Computers, Inc, 2909 Stender Way, Santa Clara, CA 95051, says that this "marks the first time multiple processors have been both hardware and software designed to act as a team, virtually as one processor." Tandem 16 provides both multiple processors and totally redundant interconnections among all processors, controllers, power supplies, and peripheral equipment without sacrificing speed or economy.

The modular configuration is such that whenever one essential module fails, a redundant module takes over automatically and the system works around the failed module. Even though the take-over may require

postponement of a low priority task, important work continues and the system as a whole suffers only "graceful degradation" or a temporary lowering of performance. Repair of the failed module can be accomplished without interrupting operation of the system.

Claimed to extend the concept of economical redundancy to all transaction-oriented users, this system is configured about processor modules linked by two fully redundant buses called the "Dynabus." Either bus can handle all interprocessor communication so that programs in one processor module communicate with programs running in other processor modules. Each bus is fully autonomous and operates independently but simultaneously with the other. Transfer rate on the buses is 20 megabytes/s. Packet-multiplexed transfers can be made among any number of processor modules. Block transfers of 1 to 32,767 bytes can be made to a designated processor module by one hardware instruction.

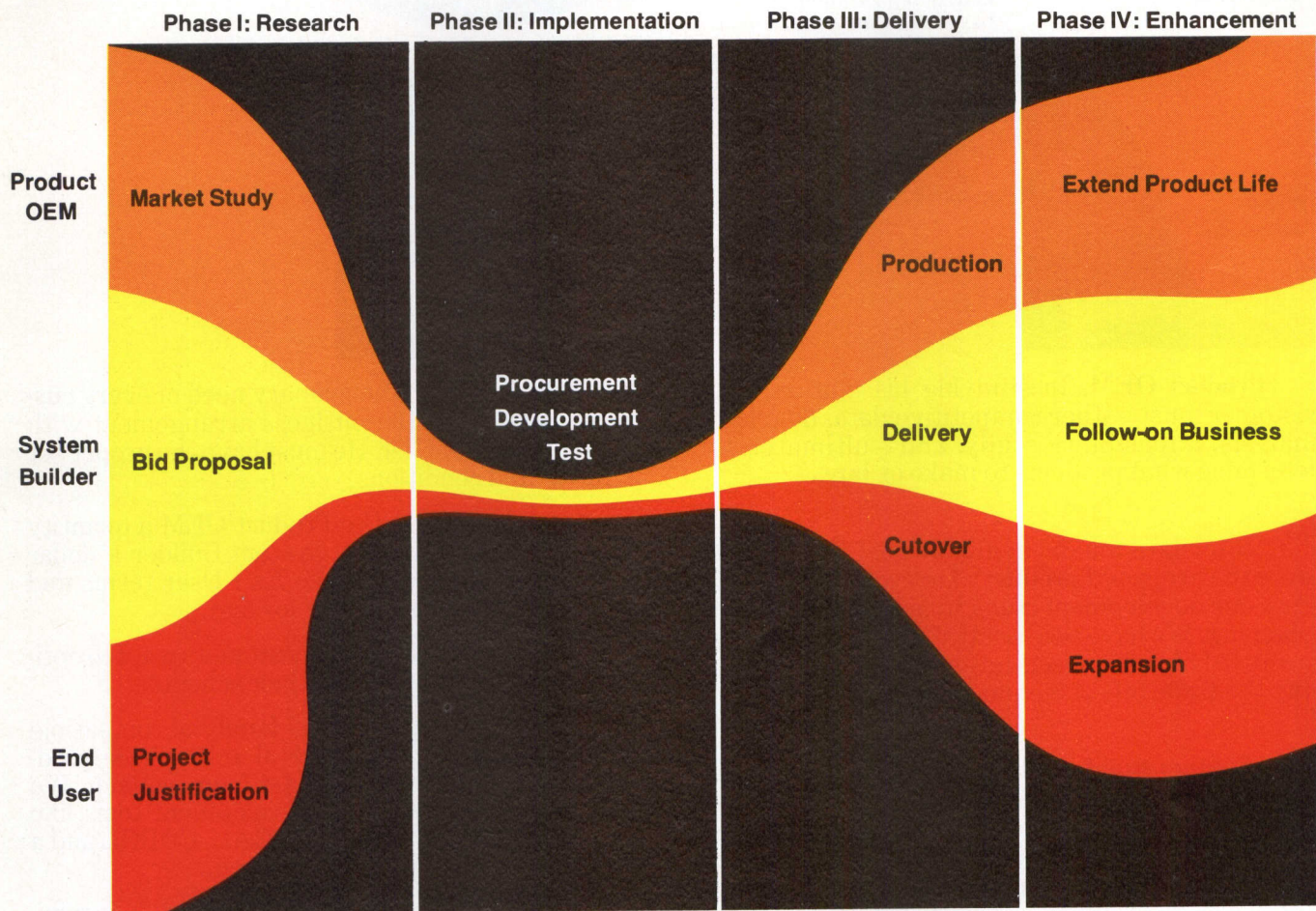
A minimum system, the NonStop 204, is made up of two T16 processor modules, each containing 32 thousand

words of memory; 10-megabyte disc drive; magnetic tape unit; operator console; and 16 terminal lines. Expansion is possible up to 16 processor modules with 512 kilobytes of memory each, and up to 32 dual-port peripheral device controllers per module. As many as 1000 terminals or 2048 input/output (I/O) devices can be supported by a fully expanded system.

Each processor module contains a Dynabus control unit for automatic switchover or disconnect in the event of processor or bus failure, a micro-programmed central processor unit (CPU) with six general-purpose registers, semiconductor or core memory, and a separate processor for control of I/O functions. CPU micro-instruction cycle time is 100 ns; micro-instructions are 32 bits in length. I/O transfers are performed at 4 megabytes/s through a burst-multiplexed direct memory access (DMA) port.

Each I/O controller is connected to the I/O channels of two processor modules through dual ports, thereby providing two communication paths to each I/O device. Although

INTERDATA INTRODUCES COMPUTER LIFE SUPPORT.



YOUR COMPUTER'S LIFE CYCLE.

Interdata's computer products and services exist for one reason — to satisfy our customers. The key to our business is understanding our customers' business needs.

There are three types of computer buyers:

The Product OEM buys large quantities of identical computers, adds special software and hardware, and sells a resulting product.

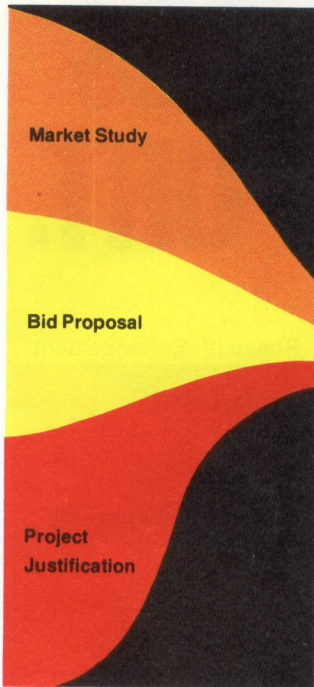
The System Builder buys computers and peripherals, packages them into a system, adds proprietary software and delivers them to fulfill a specific customer need.

The End User buys a computer system to solve his problem.

Each of these buyers goes through a Computer Life Cycle consisting of four specific Phases—Research, Implementation, Delivery and Enhancement. Interdata responds to the specific needs of the computer buyer during all four Phases of his Computer's Life Cycle.

If you are a Product OEM, System Builder or End User, you might be interested in reading the next two pages to find out how Interdata can make your job easier.

The following description is the essence of the Interdata concept called Computer Life Support.



Phase I: Research

Computer Life Support begins here. The Product OEM studies his market to determine just what his product should be, where it fits and how much it should cost. The System Builder produces a bid proposal aimed at solving his customer's specific problem. The End User is interested in defining a computer-based solution to a problem and justifying this project to management.

Interdata recognizes that each kind of customer has specific needs during this Phase. Here's how we respond to them.

Product OEM. In studying his market, this customer must gather competitive data, do a ROI analysis, a feasibility study, and—ultimately—determine what products to make or buy.

Interdata makes available cost information over the projected product's life cycle. We will discuss our development plans to help you with your planning. We have field analysts and systems engineers to help with specifications. And we help identify the trade-offs of any make-or-buy decision.

System Builder. This customer needs responsive project and proposal support. He demands a professional relationship with his computer vendors. And he must identify what equipment meets his performance specifications.

At Interdata we format our proposals to your requirements. We offer technical support plus special products and services to fill your needs. And we back this all up with our policy of not competing with our customers.

End User. This customer needs an easy-to-understand computer system. He's interested in near term solutions yielding long term profits. And he must know that his computer can do the job.

Interdata computers have familiar IBM-like architecture supported by thorough documentation. We show you similar applications and provide local benchmark and demonstration facilities.

And, as a subsidiary of Perkin-Elmer, we bring you the resources and financial stability of a multi-million dollar corporation.



Phase II: Implementation

In the Implementation Phase, very similar tasks must be performed by each Interdata customer—be he a Product OEM, System Builder or End User. Each customer must take his computer through procurement, development and testing.

Procurement. The primary need of every customer is an equitable business arrangement with his computer supplier. He must have the proper set of terms and conditions.

Interdata offers the Product OEM a quantity discount agreement; the System Builder a dollar volume agreement; and the End User terms and support tailored specifically for him.

Development. Here all customers want to optimize their design and meet their schedule.

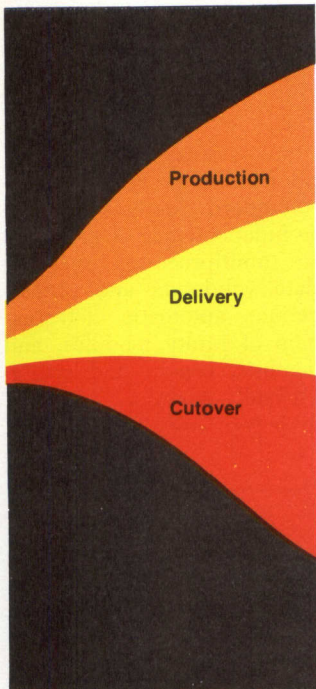
Interdata provides a full family of compatible hardware, software, peripheral and service products so you don't have to start from scratch. We have easy-to-use program development tools like BASIC, FORTRAN, MACRO CAL, COBOL and a multi-terminal development system.

Test. At this point the customer needs to minimize the possibility of system failure.

Interdata provides system debugging and integration aids such as hardware memory protect and privileged instructions.

Net Results. You can benefit from Interdata support during Implementation in three critical areas: Lowest overall price. Optimum computer performance. And on-time systems completion.





Phase III: Delivery

At this Phase of a computer's life cycle, our customers again have distinct tasks: The Product OEM must produce as efficiently and economically as possible. For the System Builder, on-time delivery is critical. And, the End User wants to cutover his system as soon as possible.

Product OEM. This customer wants to minimize recurring product costs. He wants his computer equipment to be reliable and delivered on time. He also wants to increase the value he adds to his product.

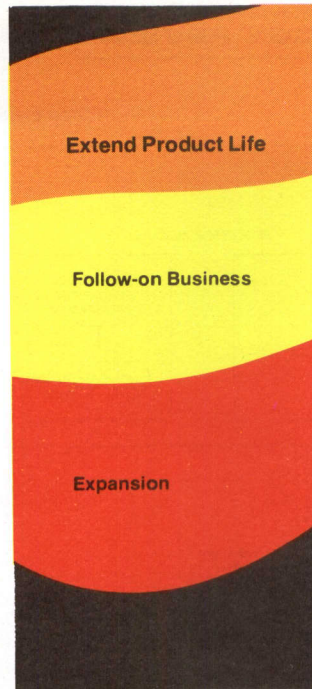
Interdata reduces your recurring costs with unbundled hardware and software modules. Our products are reliable because of our conservative design and stringent quality control procedures.

For vertical integration, Interdata sells computer board sets to allow you to increase your value added.

System Builder. To meet delivery commitments, he must have reliable computer equipment backed up by responsive field service.

Interdata's quality control assures you of no on-site surprises. We 100% test all our incoming parts. We put our computers through a unique "shake and bake" process. We solve product problems in the factory — rather than in the field.

End User. When cutting over to production, the End User needs service. Accordingly, Interdata provides four field service programs: resident service; contract service with fixed price on parts and labor; on-call service for which we charge for parts and hourly labor; and depot parts maintenance service.



Phase IV: Enhancement

In the final Phase of the computer life cycle, the Product OEM is working to extend his product's life. The System Builder is looking for follow-on business. And the End User wants to expand his system.

Product OEM. This customer's concern is to avoid product obsolescence.

Interdata offers you improved product performance through upward compatibility. Or, you can lower your product's price by taking advantage of the next generation of Interdata computers.

System Builder. To capture follow-on business, the System Builder needs to transfer his experience, training and software from one system to the next.

Interdata makes transferability easy because of our familiar, large-machine architecture and complete family compatibility.

End User. For this customer, system enhancement means system expansion.

Interdata's computer architecture allows you to expand all the way from a single board 16-bit processor to a \$300,000 32-bit MEGAMINI™ computer system.

Find out more. Interdata's responsiveness to your needs during every Phase of your Computer's Life Cycle adds up to Computer Life Support. If you are a Product OEM, System Builder or End User, we have a lot more to tell you. Just send in the coupon. Or call us.

Gentlemen:

I'm a (check one) Product OEM
 System Builder End User who wants to know more about Computer Life Support.

Send information. Have an Interdata representative call.



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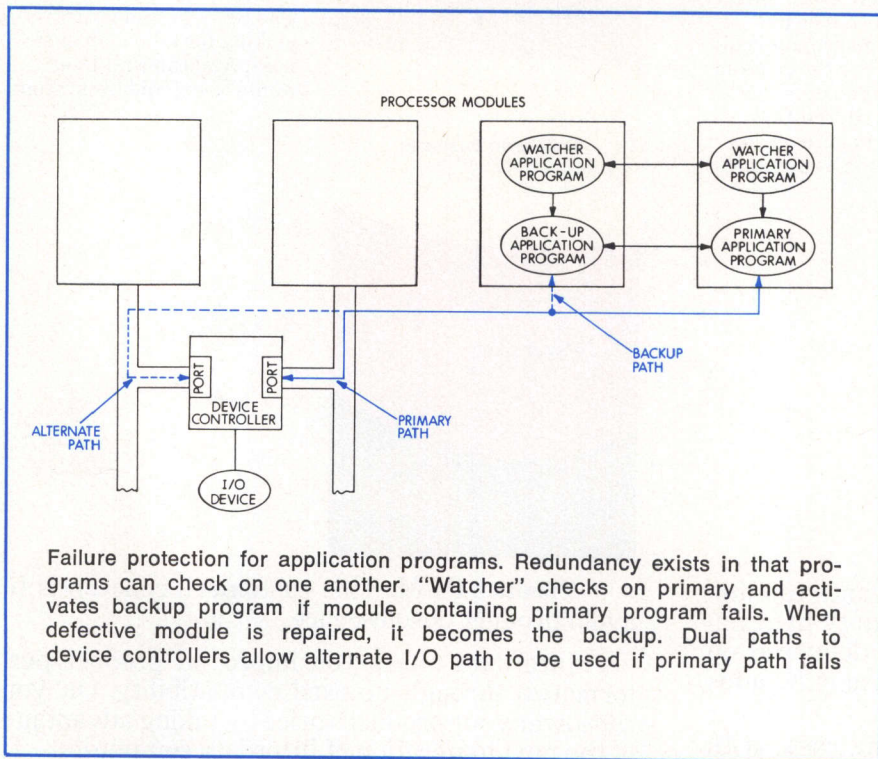
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allocates buffer space and control blocks, and handles process synchronization. Standard features include geographic independence of programs and data; multiprocessor message system; data validation and processor protection; automatic detection and isolation of faulty modules; and online diagnosis, repair, and reintegration of a faulty module.
 Circle 141 on Inquiry Card

Process-Control-Oriented Programmable Calculator Has Dual Capabilities

More powerful and versatile than a programmable controller or a microcomputer, the HP 9825A programmable calculator includes many features usually found only on minicomputers. Yet the desktop unit is easier to use than a minicomputer and can be operated as a calculator at the same time that control programs are running.

Although intended as a controller for an instrument system or a pilot process application, for remote data collection, or for production control, the calculator can also be used as a standalone computer. Hewlett-Packard's Calculator Products Div, Loveland, CO 80537, has designed the medium-priced unit primarily for use

a controller will accept commands from only one processor, if a controller's master processor module fails, the other processor module takes over control. Only a few components are common to both of the 16-bit data paths.

Data transfers on the I/O channels occur directly between memory and I/O devices at memory speed. Burst-multiplexed transfers can be made from any number of devices. Data transfers can be made in blocks of from 1 to 4094 bytes. Up to 256 devices can be handled simultaneously on each I/O channel. Peripherals are connected in a star pattern, assuring that failure of one device will not cause failure of any others.

Memory may be either semiconductor or core. Cycle time is 500 ns for accessing a 16-bit word in semiconductor memory, including accessing the map registers and error correction (if necessary); for core it is 800 ns including mapping and parity checking. The next instruction to be executed is prefetched while the current instruction is being executed.

An instruction set contains 122, 16-bit instructions. Twelve memory reference instructions can directly address any of five data areas in memory: global, local, system global, parameters, and sublocal. Two instructions are provided for reading

constant information from a program's code area. Data and code memory reference instructions can use the contents of a direct memory location as an indirect reference to another location.

Main memory is mapped for protection and relocation in four separate maps: system data, system code, user data, and user code. Up to 128 kilobytes are addressable through each map. Memory mapping automatically reallocates user code or non-critical operating system code to alternate physical memory pages upon detection of a parity or uncorrectable memory error.

Distribution of power is also organized such that failure of a power supply does not shut down the system. Each processor module has its individual power supply, but if that supply fails, making the module inoperative, the alternate module assumes control. Since each dual-port device controller is connected to two processor modules, the controller receives power from two sources.

Software, designated as T/TOS (Tandem/Transaction Operating System), is a multiprogramming, multiprocessing, virtual operating system. A copy resides in each processor for the necessary redundancy. The software allocates execution time to multiple programs on a priority basis,



Live keyboard on Hewlett-Packard's 9825A desktop programmable calculator permits calculations to be made at the same time that the calculator is running control programs. At top front of unit, from left to right, are tape drive (for minicartridges), 32-character LED display, and 190-line/min. thermal printer

Who is the largest supplier of OEM semiconductor memory systems?

If you're in the computer or systems business you probably already know that it's Intel. You also know the importance of getting your systems out of engineering and into the marketplace. Nothing happens until you get an order.

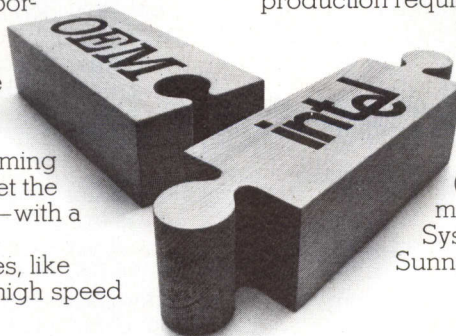
If the semiconductor memory part of your system is delaying things or if you have two important memory projects but only one design team, then you should talk to us. Chances are we may already have just the memory system you need. That's why more and more computer companies and system houses are coming to Intel for help. We're helping them get the competitive jump in the marketplace — with a memory as good as their own.

We're talking about big memories, like 8 megabytes in a single frame. And high speed

memories as fast as 150 ns access time, 300 ns cycle time. And memories to interface with your TTL or ECL logic, with or without error correction.

We're already shipping over 50 multi-megabit systems, plus thousands of single board memories every month. That means we'll be able to support your volume production requirements. And because we're the world's largest manufacturer of both semiconductor memory systems and components you get the best possible price/performance package.

It's easy to get started. Call Gary Andersen, OEM Marketing Manager, (408) 734-8102 Ext. 451, or send your memory specifications to Intel Memory Systems, 1302 N. Mathilda Avenue, Sunnyvale, California 94086.



intel[®] memory systems
A DIVISION OF INTEL CORPORATION



Plant Tours: 8:0

The next time you're planning to visit Los Angeles, schedule a Pertec Plant Tour. Sure, Southern California has many tourist attractions, but Pertec's Plant Tours are getting more and more popular.

Our guests have come from all over the world.

Our plant tours have been enjoyed by countless domestic and foreign guests. Including customers from Thailand, Africa, India, Germany, England, Japan — literally, almost every country in the world. Businessmen (and women) from every nook, cranny and capital city in the United States have inspected the Pertec plant. (Changing many from a curious, interested guest to a solid customer.)

First, one tape drive. Then 50,000 more.

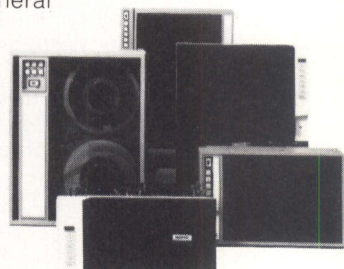
We had no idea our manufacturing techniques — and

products — would become so popular. And, as our popularity increased, so did OEM customer interest in our plant.

Today, at Pertec, you'll see the most advanced electro-mechanical technology (the art of reducing manufacturing costs on prosaic tape drives, disk drives, floppy disk drives, and other related peripheral equipment). You'll see how Pertec customers select tape drives from more than 400 model variations.

And you'll see how Pertec cartridge disk drives can be top- or front-loading and interface compatible.

You'll see the Pertec family of *fixed-disk* drives.





0am to 5:00pm.

And, you'll see how we are able to manufacture low-cost, high-volume flexible disk drives.

In short, you'll see tape transports, disk drives and flexible disk drives *all* in one location.

All produced by Pertec.

You'll see how Pertec's product-testing and worldwide service operations assure you the best combination of product quality, reliability and price of any computer peripherals in the world.

You'll understand how Pertec's 8 years of successful product design, manufacturing and product support have created a financially sound and attractive entity: Pertec.

And, you'll see this *right before your very eyes!*

Interested? Call Pertec or your travel agent.

The Pertec Plant Tour is a must for anyone seriously

involved in the buying decisions of peripheral equipment.

Call the Pertec regional office nearest you: Boston (617) 890-6230; Chicago (312) 696-2460; Los Angeles (213) 996-1333; London (Reading) 582-115. Or, write us at Plant Tours, 9600 Irondale Avenue, Chatsworth, California 91311.

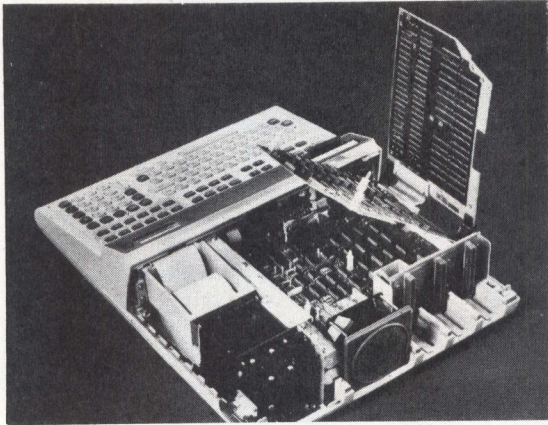
Or call your travel agent. If he hasn't heard about the Pertec Plant Tours, it's about time somebody told him about the great new show going on outside of Hollywood.

At Pertec.

The world's leading computer peripheral equipment showplace.

PERTEC

Drop by and see us sometime.



Easy access to interior of HP 9825A calculator is provided by hinged printed circuit boards. Complete unit weighs only 26 lb and is about half the size of earlier calculators

in engineering, research, and statistics. Some of its features are interrupt capability, input speeds of up to 400,000 words/s and output speeds of up to 200,000 words/s (16-bit words), live keyboard, direct memory access, bidirectional tape drive using mini-cartridges, multidimensional arrays, automatic memory record and load, internal calculation range of $\pm 10^{511}$ to $\pm 10^{-511}$, and optional plug-in read-only memories.

A live keyboard, claimed to be a "first" for desktop calculators, permits a user to perform simple calculations, examine and change program variables, and list programs while the calculator is performing other operations. Actually, an interrupt capability apportioned operations on a priority basis, but the process is so fast that everything appears to happen at once. The live keyboard can be turned on or off under program control.

Available in an extended I/O ROM (input/output read-only memory), this interrupt capability allows the calculator to control instruments or peripherals, print, plot, and run programs at the same time on an operator-determined priority schedule. On the calculator this is accomplished by simple keyboard commands; on a minicomputer the operator would have to write a program in assembly language.

HPL, a high level, formula-oriented programming language, handles subroutine nesting and 16 flags. It allows up to 26 simple variables and 26 multidimensional array variables, limited only by the size of the calculator memory. Claimed to contain the power and efficiency of FORTRAN for handling complex formulas and equations, but as easy to

learn as BASIC, HPL is suited for both controller and data processing applications. The structural unit is a line composed of one or more statements separated by semicolons. Errors are indicated by error messages and line numbers in the display and are identified by a flashing cursor. Math errors can be overridden by the programmer.

Programs can be debugged by commands inserted from the keyboard. Tracing can be made on the entire program, a section, or a single line. Both fixed- and floating-point formats can be set by the user. Entire lines or individual characters can be inserted, deleted, or changed. When line insertions or deletions are made, addresses are automatically renumbered.

In addition to a typewriter-like section, a calculator-key section, and command keys, the keyboard contains 12 special function keys. Using a shift function, 24 different operations can be handled. These keys also aid in program writing and in peripheral and instrument control, and can be used as immediate execute keys, as call keys for subroutines, and as typing aids.

Memory load and record operations are performed via a mini-cartridge of the same type as used on the company's 9815 calculator. The 2-track tape holds up to 250 kilobytes of data and has a 2.7-kilobyte/s transfer rate. If power should fail, an autostart feature permits information to be reloaded into calculator memory from the cartridge after power has been restored. Tape cartridge commands permit the user to load and record data, programs, or the entire memory. After tape files are recorded, they are automatically

verified against the calculator memory.

Cartridge drive bidirectional search and rewind speeds are 90 in./s (2286 mm/s) and read/write speed is 22 in./s (559 mm/s). Average access time is, therefore, 6 s. Transfer rate is 2750 bytes/s, typical access rate is 14,300 bytes/s, typ rewind time is 19 s end-to-end, and typ erase time is 40 s for one entire track. Since the calculator always knows the location on the tape, it is able to search in either direction for the next bit of information, thereby saving time. Also, an operator can interrupt a long program, load the data onto the cartridge, run a short program, and then restart the first program.

A built-in, 16-character, 5 x 7 dot matrix, 190-line/min. thermal printer and a 32-character LED display provide upper and lower case alphanumeric readout in a full ASCII character set. Some European and Greek character sets are ROM-addressable.

The standard calculator includes 8 kilobytes of internal read/write memory, which is expandable in 8-kilobyte increments to 32 kilobytes. Optional ROMs can be added in four plug-in slots in the front of the calculator: STRINGS, which provides string arrays; 32,767 characters; functions like length, position, value, and capitalization; and concatenation; ADVANCED PROGRAMMING: MATRIX, which provides standard operators like invert (40 x 40 in 70 s), transpose and multiplication, multi-dimensional array operators, and scalar multiply; PLOTTER; GENERAL I/O; and EXTENDED I/O.

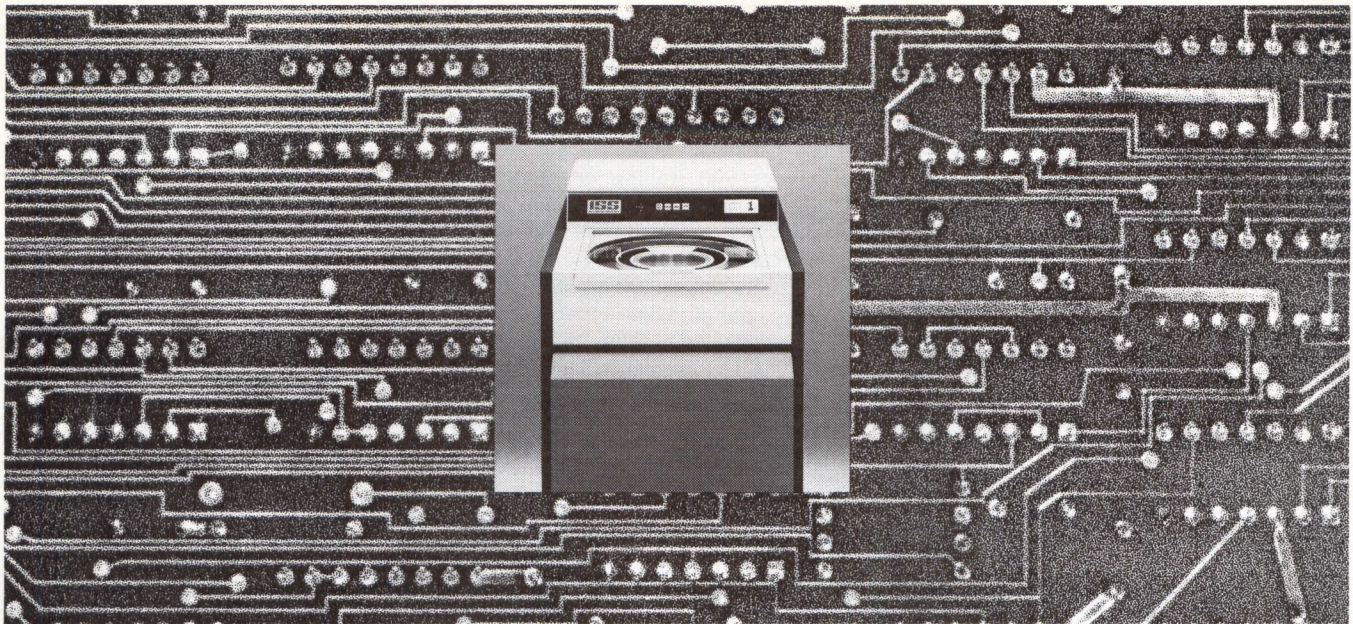
Three optional interface cards can be accommodated simultaneously in I/O slots. These are a 16-bit parallel card that may be used for general-purpose interfacing, a BCD card for use with BCD devices, and an HP-IB card for instruments that conform to IEEE Standard 488-1975.

High speed internal calculation is provided by N-MOS II (LSI) circuitry designed by Hewlett-Packard. In addition to four bipolar display chips, BPC processor, I/O, and extended math chips are included. ROM is based on a 16 x 1024 format.

Rear panel switches permit user selection to match power sources of 100, 120, 220, or 240 V (+5%, -10%), at 48 to 66 Hz. Power consumption is 1.7, 1.5, 0.8, or 0.75 A, respectively, for these voltages.

A number of peripherals can be attached to the calculator. These include printer/plotter, plotter, paper tape punch and reader, digitizer, and the recently announced 9866B line printer.

Circle 142 on Inquiry Card



Introducing the industry's most advanced 100/200-megabyte OEM disk drives.

ISS 733-10/11 — benefits for all.

The new ISS 733-10/11 disk drives are, by far, the most advanced random access mass storage devices ever designed for the OEM market. Their numerous features are designed to benefit both you and your customer. For example, the 733-10/11 offer exceptional speed in both head positioning and start/stop times. Compactness, advanced sound insulating, and waist-high pack loading are just a few of the additional design considerations. The big news, however, is the 733-10/11's field-upgrade capabilities. ISS 733-10, with a 100-megabyte capacity, can be easily field-upgraded to 200 megabytes. Or the 200-megabyte capacity is available immediately with ISS 733-11. In addition, either unit can be ordered with, or field-expanded to, dual port capability.

Advanced interface design for extended compatibility.

The advanced design of the ISS OEM interface permits functional compatibility between ISS 733-10/11 and most current model 40, 80, 100 and 200-megabyte drives. As a result, controller modifications are minimal.

ISS designed-in performance features:

Standard power supply — The integral power supply is designed to tolerate

wider variations of AC power, greatly reducing susceptibility to powerline brownouts.

Module select plug — Permits added flexibility in disk address assignments in multi-drive systems.

Data separation and write data precompensation — All read/write data encoding and decoding is performed in the drive.

Absolute cylinder addressing — Simplifies programming by performing disk addressing functions in the drive which are normally performed in the controller

Industry standard media — 3336 and 3336-11 or equivalent disk packs.

Programmable sector mark — Allows user to pre-select sector size to suit his specific application.

Important extra-performance options:

Dual port — ISS 733-10/11 can be upgraded from single to dual port in the field. Or, if you prefer, dual port can be factory installed prior to delivery.

Sector counter — Permits system to interrogate which data sector is approaching the read/write heads.

Rotational position sensing — Increases system throughput by signaling to the using system when the desired sector is approaching the read/write heads.

Address mark format — Specifically for those who require variable record lengths on their systems.

Daisy chaining — Dramatically reduces cabling requirements.

Capacity upgrading — 100 megabyte to 200 megabyte.

Round-the-clock ISS support.

ISS maintains a complete support facility for all its customers. Spare parts and technical assistance are available round-the-clock and are as near as your phone.

Write or call today.

We would like to give you more information about the ISS 733-10/11 and their many advantages. Just write or call ISS marketing, 10435 N. Tantau Avenue, Cupertino, CA 95014, (408) 257-6220. ISS is an operating unit of Sperry Univac.



ISS

Technological leadership
for the generations ahead.

Sperry Univac is a division of Sperry Rand Corporation

G-P System Performs Batch and Time-Sharing Operations Concurrently

Described by its manufacturers as a medium scale computer with large computer features but a small computer price, DECsystem-20 is intended for organizations that require batch and time-sharing facilities but until now could not afford the systems that have been available. The general-purpose system, announced by Digital Equipment Corp, 200 Forest St, Marlborough, MA 01752, can handle up to 64 time-sharing users and permit batch operation at the same time.

Primary markets are expected to be in educational and engineering facilities where users tend to be self-sufficient and technically oriented, but where the number of applications will not be large enough to require or warrant the cost of a very large system. The first DECsystem-20 is scheduled to be delivered this month.

Needs of most users will be met by a configuration of 96 thousand 37-bit words (36 data bits plus parity) of core memory, 16 asynchronous ports, two RP04 disc drives, two TU16 tape drives, one 300-card/min. reader, and one 300-line/min. printer. However, full capacity of 256 thousand words of memory, 64 ports, eight

disc drives (800 million characters), eight tape drives, one 300- or 1200-card/min. reader, and one 300- or 1200-line/min. printer can be attained later by users who want to start with a basic configuration that meets present needs but then update to meet growth requirements. Only 28 ft² are required for processor, memory, and I/O controllers.

The central processor unit (CPU) is built of high density multilayer circuit boards and emitter-coupled logic. It contains a microcoded instruction set, 16 integrated circuit general-purpose registers, two accounting meters, three performance and monitoring meters (interval timer, time base, and performance analysis counter), and interrupt and trap facilities.

383 logically grouped instructions enable programs to use far fewer instructions to perform a given function. This not only allows programs to be shorter than on other computers but also simplifies the monitor, language processors, and utility programs. (Compiled programs, for example, can be 30 to 50% shorter and therefore require less memory and shorter execution time than on other comparable computers.)

Some of the key functions provided by hardware include 70-bit double precision fixed- and floating-

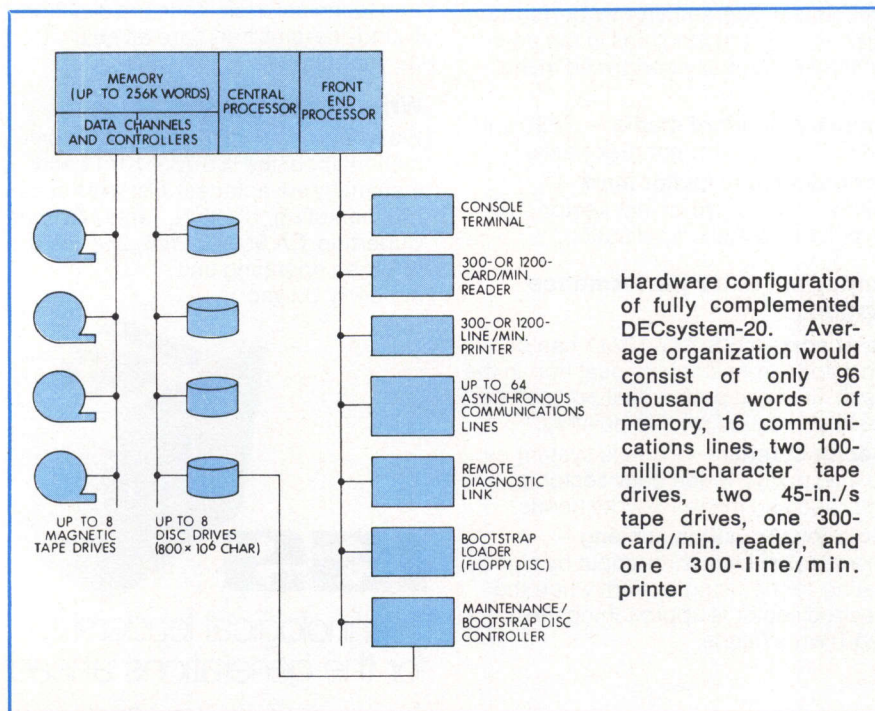
point arithmetic; hardware stack instructions which ease shareable programs and fully recursive subroutines; and a flexible business instruction set with sophisticated editing and character handling capabilities. Such capabilities include check protection through floating currency signs, leading zero suppression, EBCDIC-to-ASCII character set translation, and binary-to-decimal, decimal-to-binary conversion.

The instruction set is logically grouped into families of instructions, and mnemonic codes have a consistent format. All instructions are capable of directly addressing a full 256 thousand words of virtual memory without resorting to base registers, displacement addressing, or indirect addressing. However, instructions may use indexing with indirect addressing at any level. Most instruction classes, including floating-point, allow immediate mode addressing. Also, the instruction set includes a large number of operation codes which trap to either the monitor or the user area, permitting a full range of programmable monitor and subsystem calls.

General-purpose registers can be used as accumulators, index registers, or the first 16 locations in memory (thereby eliminating a reference to main memory). By providing eight sets of registers (with 500-ns register switching time), the need for saving user-register contents during context switching is eliminated. Since the registers can be addressed as memory, no special instructions are required for register-to-register operations.

Instructions are executed in either Exec or User mode. In Exec mode, all implemented instructions are legal; the monitor runs in this mode and is able to control all system resources and the processor's state. In User mode, instructions such as direct I/O are illegal and cause a trap to the monitor. (Users must issue monitor calls for such system services.)

The interrupt facility does not require devices to be hard-wired to a particular level. Instead, devices are assigned under program control to any one of seven priority levels through the dynamic loading of device registers. Therefore, the monitor can change the priority level of any device or disconnect the device from the system and later reinstate it at another level. Priority level 0 is above the seven programmable levels and is reserved for the front-end processor which, therefore, is able to interrupt the system at any time for console or diagnostic operations.



Announcing Honeywell's Series 60, Level 6.



**Our new minicomputer -
it's small and quick
and very smart.**

Now Honeywell has a whole new family of minicomputers.

Level 6 means high-reliability hardware that's easy to program, easy to configure, easy to service.
For only \$2634.*

Powerful central system architecture: Level 6 architecture is designed to support the most demanding minicomputer applications, and provide a full range of compatible systems from which the user will be able to select the one best suited to his requirements. Initial models include many of the following architectural features:

- Microprogrammed instruction set with writeable control store available to the user.
- Direct addressing up to 8 million words of memory.
- Minimum of 18 programmable hardware registers.
- Bit, byte, word and multi-word addressing.
- Hardware stack and queue management.

- Proven N-channel MOS memory in 8K by 16-bit modules, with byte parity and up to 32K words on a single board. Cycle time is 650 nanoseconds.

- Error detection and correction (Corrects single bit, detects two-bit errors).
- Memory management hardware.
- Over 100 basic instructions, with more than 600 variations.
- High-performance scientific and commercial instruction set extensions.
- Common asynchronous Megabus™ operating in an interleaved mode, with a bandwidth of 6 million bytes per second.
- Vectored interrupt capability with up to 64 interrupt priority levels.
- Separate trap structure with more

than 20 unique entry points.

- Microprogrammed input-output controllers.
- Multiprocessor and networking capabilities.

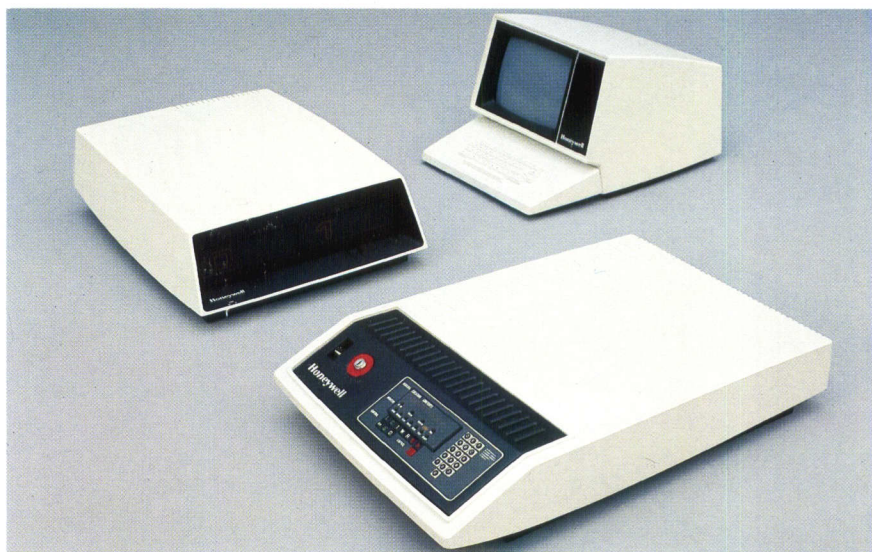
The benefits include the ability to write compact and efficient programs, increased processing speed, reduced memory utilization and memory management overhead, reduced software overhead, increased throughput, and the capacity to handle large and versatile configurations.

Models 6/34 and 6/36 incorporate subsets of the above features and are immediately available. These models are well suited for OEM and system-builder applications. Maximum memory for the 6/34 is 32K words, and for the 6/36, 64K words.

Advanced modularity:

Level 6 combines TTL logic, LSI and MSI circuitry, firmware-driven microprocessors, MOS memory, and etched wire connections in a new way to achieve plug-in modularity with optimum configurability and replaceability. Specifically:

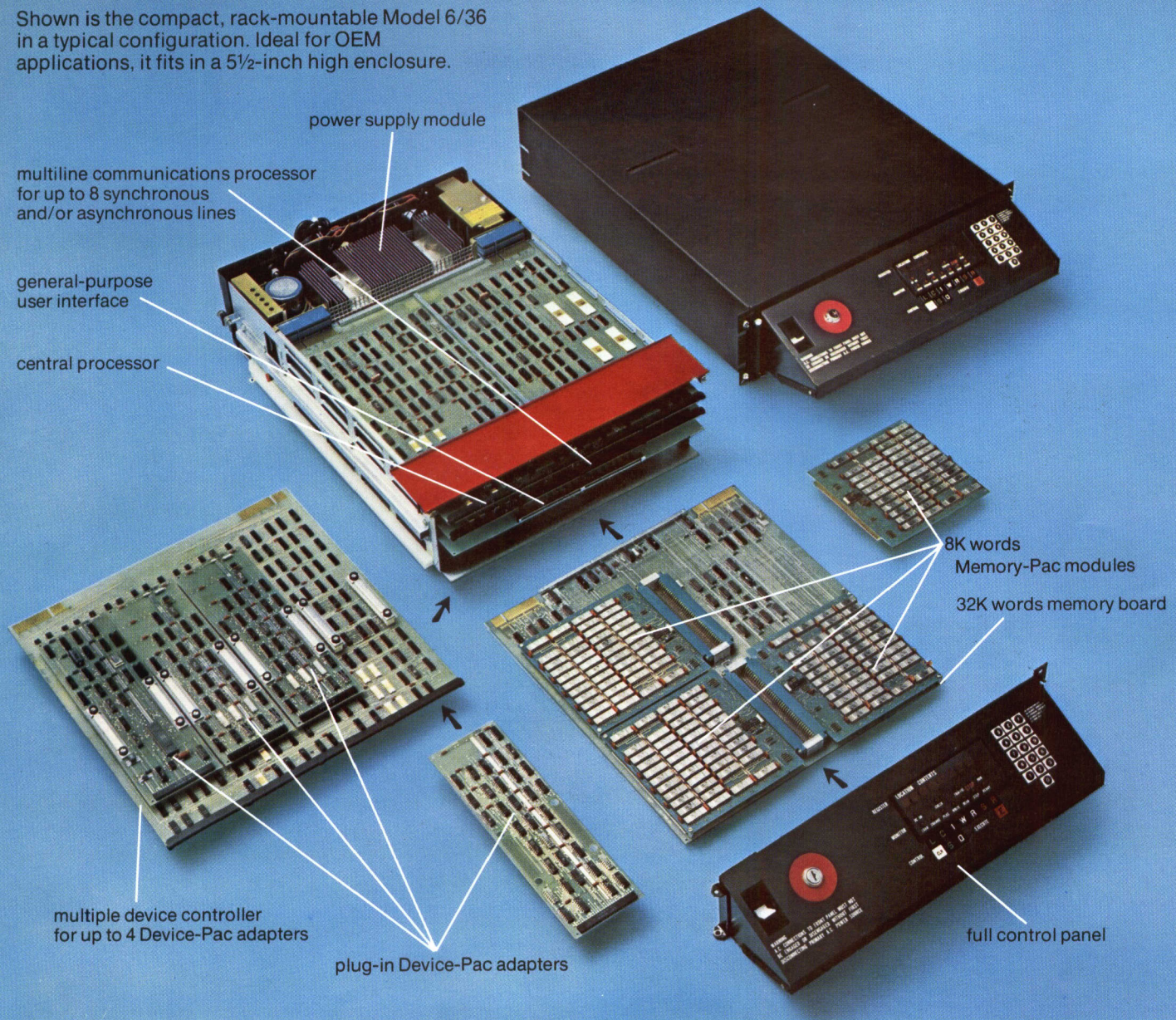
- The entire central processor is contained on a single board 15" x 16".
- Other 15" x 16" boards are devoted to the memory, communications processor, peripheral controller, and user interface.
- Functional modules (i.e. device adapters and memory modules) plug into the 15" x 16" boards.
- Boards fit into the bus without backplane wiring.



Level 6 offers a choice of rack-mountable, cabinet and tabletop models. Level 6 also includes a new full line of low-cost peripherals in both tabletop and rack-mounted versions. Shown are the tabletop minicomputer, diskette and CRT.

*U.S. price in quantities of 50 for rack-mountable Model 6/34. Includes 8K words of MOS memory, with parity, multiply/divide, realtime clock, and bootstrap loader.

Shown is the compact, rack-mountable Model 6/36 in a typical configuration. Ideal for OEM applications, it fits in a 5½-inch high enclosure.



These features offer the following benefits: The sharing of costly logic elements such as controller microprocessors and memory error correction lowers the system cost. A system can be easily configured through the selection of a minimum number of appropriate boards and modules. Fewer components and connections mean increased system reliability. And serviceability is improved by having fewer — as well as more easily replaceable — components.

Microprogrammed communications processor: Honeywell's multiline communications board functions as a true front-end processor. It offers unusually powerful

communications capability at moderate cost.

- Separately programmable memory allows tailoring to individual requirements.
- Usable memory of 4096 bytes enables execution of complex line-handling procedures with no central processor involvement.
- Each board handles up to eight full-duplex lines.
- A variety of modules adapt the communications processor for different line types and speeds (up to four modules per board, line types and speeds may be mixed on the same board).

As a result, the central processor is relieved of most of the data com-

munications overhead, and the user has maximum application flexibility.

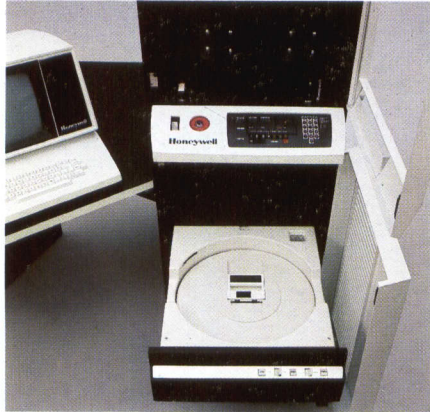
Built-in test and verification:

The Level 6 system provides an automatic configuration integrity check and self-diagnosis:

- Light-emitting diodes on the central processor and each controller board verify logic quality.
- A console indicator verifies that boards, terminators, and bus cabling are properly connected at time of system initialization.

By means of these features, together with the simple replaceability of boards and plug-in modules, the Honeywell Level 6 system is designed to be the most serviceable minicomputer ever built.

Efficient system-building software: Honeywell has gained considerable system building experience through the application of minicomputers within the general purpose computer and control system segments of its business. This experience, together with the expertise gathered in ten years of



building minicomputers, has been applied to Level 6 hardware and software design to produce integrated system products particularly well-suited to a wide variety of jobs. The initial software includes:

- Stand-alone program development system.
- Stand-alone multitasking real-time executive.

- Disk-based multitasking realtime operating system.
- Assembler, FORTRAN and utilities.

These are the first results of a comprehensive software development program. Scheduled for future release are additional higher level languages, communications software enhancements, and operating system extensions.

System 700 compatibility: Level 6 offers System 700 com-

patibility via the Model 6/06. The 6/06 incorporates the packaging and technology advances of Level 6 and supports the full range of System 700 software and peripherals. Memory is available in 8K word increments up to 64K. Systems are available for immediate shipment.

For more information, please mail us the coupon or circle number 125 on reader card. We'd like to show you why Honeywell's Level 6 is the biggest news in minicomputers today.



The Model 6/06 is offered with a variety of peripherals. The configurations shown include disk drive, CRT, tape cassette unit, card reader, printer, and paper tape reader/punch.

The Other Computer Company: **Honeywell**

Honeywell Information Systems, 200 Smith Street, MS 440, Waltham, Massachusetts 02154

- Please send me more information about Level 6 minicomputers.
 Please have a salesman call.

Name _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Phone _____

To help you answer my request more effectively, here's some basic information:

I'm an OEM End-user I have a need for _____ minicomputers during 1976.

My intended application(s) is _____

I am interested in Model(s) 6/34 and 6/36 6/06

F G



A trapping mechanism handles certain conditions which affect a single job. Such conditions include address violation, arithmetic overflow, pushdown overflow, illegal instruction, monitor calls, and page faults.

Memory modules are integral to the CPU, thereby allowing faster memory accessing than with comparable external memories. Single access memory cycle time is 1.28 μ s. However, effective accessing rates are greatly enhanced through several features. For instance, software-settable switches provide 2- and 4-way interleaving which is initialized at system start-up time. Up to four data words may be accessed by a single memory reference. This provides a memory bandwidth of more than 7 megabytes/s (1.8 million 36-bit words/s) when 4-way interleaved.

Because memory-address mapping hardware has been developed in conjunction with software, memory management is totally transparent to the user. Physical core memory is divided into 512-word segments or pages. All addresses (both monitor and user) are translated from virtual address to the physical memory address space. Only a portion of the monitor therefore need be permanently core resident.

Page maps—one for the monitor and one for each user—exist in core. These contain storage address pointers which identify either a page in core or one on disc of three basic types: private (belongs to only one user), shared (used by more than one user), or indirect (points to another map page where the pointer may again be one of three types). Control bits are also present to serve various functions, such as to indicate that the page is read only, or that currently no physical page corresponds to this address slot.

High speed mass storage controllers, called integrated Massbus controllers, interface disc and tape drives to the integrated data channels in the memory controller. Since each controller is connected to the memory system with its own built-in channel, all controllers can transfer data simultaneously. Parallel data and control paths in the Massbus permit simultaneous operations.

Front-end processor for the system is a PDP-11. It is used for control of low speed peripherals, console operations for the CPU, online and remote diagnostic analysis, and micro-

code loading and system startup. Interface with the CPU permits 2-way data transfers.

Even if the CPU is inoperative, the front-end processor can examine the data paths and control its logic. Failure of system power is sensed by a detection circuit that causes an interrupt. All three phases of ac power are monitored and low voltage on any phase will initiate a power-down sequence.

Fully compatible with the interactive time-sharing mode, the batch system enables both types of jobs to be executed concurrently. Batch jobs can be entered either through punched cards or through a user's terminal. Batch programs consist of input spooler, batch controller, centralized queue manager and task scheduler, and output spoolers. Multiple batch jobs may be run concurrently.

The programmer may choose from among several languages—COBOL, FORTRAN, BASIC, APL, ALGOL, CPL, and MACRO—depending on which is best suited to his application and experience. ANS-68 COBOL supports ISAM, for high performance sorting and simultaneous updating, and DBMS, a data base management system. The other languages are valuable either to solve scientific problems or to aid beginning programmers.

Circle 143 on Inquiry Card

Remote Intelligent MUX Preprocesses Data Before Transmitting to Host CPU

For distributed data acquisition and control in the processing industries, General Automation Inc, 1055 South East St, Anaheim, CA 92805, has introduced a Remote Intelligent Multiplexer (RIM) with an integral 16-bit microcomputer, which provides computational power, field-expandable I/O, communications back-up, host-independent control and data logging, and local display. The unit provides substantial savings in cabling costs alone by accommodating all communications from a process to a computer over four twisted-pair telephone grade cables at \$1/ft instead of 32-conductor refinery-grade cables at \$6/ft. In addition, provision of data acquisition and processing power and interrupt servicing at the pro-

cess significantly reduces the communications load on the supervisory computer.

A basic unit consists of GA-16/220 microcomputer with 8K words of semiconductor memory, high speed synchronous data link control (SDLC) communications controller for point-to-point or multidrop networks, 5½" CRT/keyboard operator's console, and a ROM loader for exchanging programs and data with a remotely located host computer. Provision is made within the standard 72" cabinet for addition of 10 standard I/O interface cards to allow signals such as wide-range or low-level analog input, current or voltage analog outputs, and isolated digital ac or dc inputs and outputs. Using additional enclosures, the multiplexer can accommodate up to 256 analog inputs, 128 analog outputs, and any combination of 512 digital inputs and outputs.

In cases where the RIM unit is located more than 2000 ft from the host computer, conventional data modems or other analog communications links may be used to effect communication between RIM and host computer. Data rates may range from 9600 baud to several hundred kilobaud. The controller is capable of multidrop operation with up to 255 stations attached to a master computer, permitting users to tie essentially all remote data acquisition into one host via a single data pathway. SDLC discipline provides data security and high speed for the multiplexer.

Since the RIM is based on a conventional programmable microcomputer, it can be programmed to perform numerous data acquisition and processing tasks. Software modularity permits custom tailoring through simple table changes. The unit's monitor functions to control scanning and coordinate communications with the host computer. It is also responsible for bootstrapping the RIM memory from the host on power-up, and for coordination of communications to and from the optional operator CRT.

RIM is specified for two scan rates: one covers analog outputs and digital inputs and outputs; the second specifies a per-point basis for analog inputs and consists of a scan interval and time slot in which to sample the variable. Analog input points are filtered with a single stage, low-pass digital filter and are processed by a second-order linearizing and conversion routine; values can then be compared against high and low setpoint limits with hysteresis.

Circle 144 on Inquiry Card

DEVELOPMENTS

Manufacturing Process Improves Characteristics of Plated Wire Memories

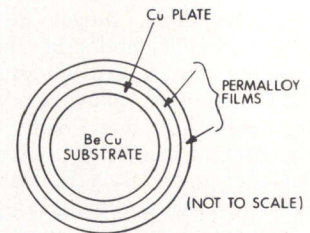
A process for the manufacture of plated memory wire, based on a patent recently issued to Raytheon Co, Lexington, Mass, is said to result in a memory device with improved storage and readout characteristics as well as increased manufacturing yield. The method, invented by Emil Toledo, chief metallurgist at the company's Equipment Development Laboratories in Sudbury, Mass, involves adding one copper and two Permalloy™ plates to raw beryllium copper wire in a carefully controlled process. Although initially intended for the manufacture of 5-mil diameter wire, a similar but more complex process has also been developed for the manufacture of 2.5-mil wire.

Routinely, the manufacture of an acceptable plated-wire element for critical military applications involves inherent problems at several stages: raw wire and surface preparation, copper plating, Permalloy plating, magnetic heat treating, and online testing. In addition, there is a limitation imposed by nondestructive readout (NDRO) wire requirements.

Because of the lack of control over the raw beryllium copper

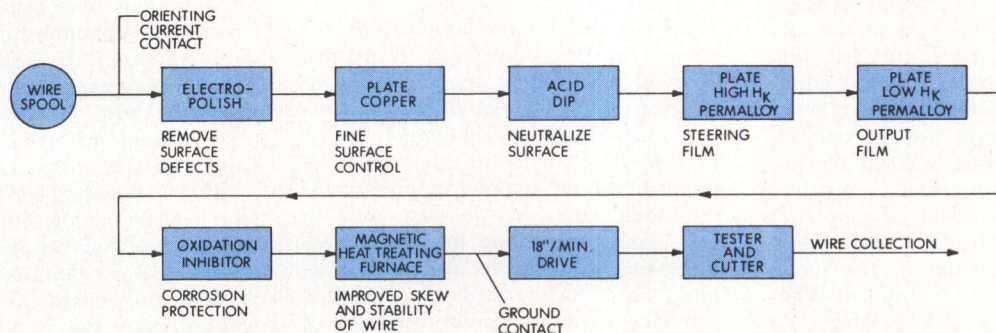
(BeCu) wire—tensile strength, electrical conductivity, surface topography, and oxidation—it was necessary to develop an electro-polishing (EP) bath capable of improving the worst available wire to a point where end product yields with that material could exceed 20%. However, this EP bath had to provide fast operation (remove 0.5 mil/dia of 5-mil wire at 20"/min. line speed); remove or level both horizontal (die marks) and vertical defects; possess wide operating ranges chemically, electrically (current density), and thermally; solve the problems of selective etching of cobalt beryl, copper, copper corrosion products, and beryl oxides; and yield readily reproducible results.

The standard phosphoric acid EP bath for copper is too slow and selectively etches cobalt, beryls, and copper. Also, the standard EP bath for beryllium (phosphoric, sulfuric, and chromic acids) has a narrow operating range and selectively etches cobalt beryl areas. Adding 1% fluoroboric acid to this bath eliminated the selective etching of cobalt beryl. Finally, a patented bath that produced a much wider operating range than the standard beryllium bath was developed by balancing with 3% sulfuric acid, 5% chromic acid, 80% phosphoric acid, and 11% water.



Cross-section of a plated memory wire using two "mated" magnetic films. A fabrication process, invented by a Raytheon metallurgist, results in good reproducibility, consistent properties, higher yields of acceptable lengths of plated wire, and ability of the plated wire to store closely spaced magnetic bits of information

Preparation of a chemically pure substrate by copper plating the BeCu wire overcomes a major problem. In order to produce a suitable substrate the surface must be rough to provide good adjacent bit resistance and homogenous for good dispersion



Process flow for Raytheon's "mated" film plated wire. Keys to the success of this process are the ability to treat raw wire of inconsistent quality such that it will accept a control plate of copper, and then to add two plates of Permalloy film, one at high H_K (anisotropy field parameter of ≥ 6 oersteds) and one at low H_K (≤ 4 oersteds)

You asked for it... the Skinny Floppy from Shugart!!

**Introducing the SA800/801R...the new member
of the most popular Floppy Disk Drive family,
now available for mounting two
units horizontally in a
standard 19-inch
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The SA800/801R, custom designed with the user in mind, is identical to its 20,000 predecessors in the field today except for a new slim line base casting. Just one more example of Shugart's response to requirements in the Floppy Disk marketplace.

The SA800/801R features single or double density recording capabilities, IBM compatibility, a ceramic read/write recording head, a superior die cast base plate and cartridge guide that guarantees positive diskette registration on every insertion increasing overall performance and reliability... all of the outstanding features you receive with our standard SA800/801.

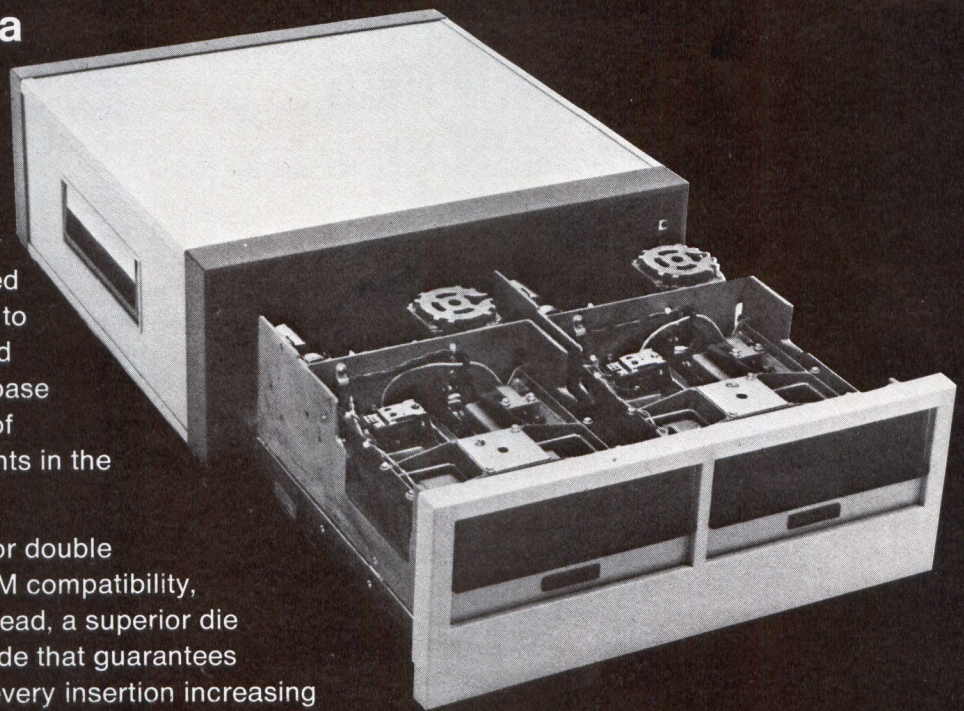
Take a good look at the unique design of the SA800/801R when you plan your next Floppy Disk System. The SA800/801R can be packaged either horizontally or vertically and offers numerous features that our competitors do not have.

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Why more engineers than all other microcom

The 8080 system comes with four CPU options, twenty-five performance matched peripheral, I/O and memory components, and the industry's most useful software and hardware development systems. We've had the 8080 in volume production since April 1974 and there are now major second sources. These are just a few of the reasons why more engineers use the Intel 8080 system than all other microcomputers combined. Join them and you'll eliminate complex random logic, save design time, and get your products to market faster and at lower cost.

Start by replacing hundreds of TTL packages with the three LSI circuits in the MCS-80™ CPU Group—the 8080A CPU, 8224 Clock Generator and 8228 System Controller. Built into the Intel 8224 and 8228 are many of the extra functions that most designs require, such as TTL & MOS clocks, auxiliary timing functions and current

sinking capability that keeps memory and I/O interfaces simple.

A dozen I/O and peripheral circuits that attach directly to the system bus make it easy to add on peripheral subsystems. Five are programmable LSI devices. These operate under software control in numerous modes and can often replace up to 75—or more—TTL packages each. For example, the Intel 8251 Programmable Communication Interface provides virtually all serial data transmission protocols in use today, including IBM Bi-Sync. Or, for easy interface to printers, keyboards, displays and motor drives, use the 8255 Programmable Peripheral Interface. You can reorganize its 24 I/O lines with software as your needs change.

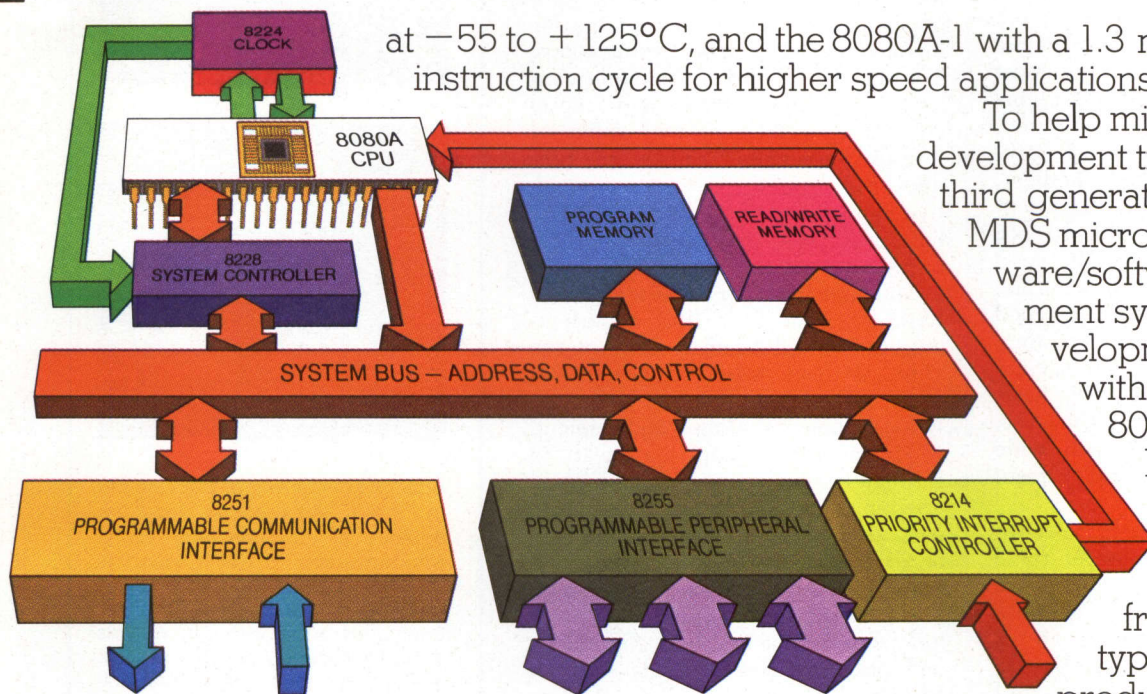
You have thirteen options in performance matched standard memory circuits, such as 16K ROMs, 8K erasable PROMs and 4K RAMs for high density at low cost, plus CMOS RAMs for lowest power.

You also get four CPU choices, including the M8080A for operation

MCS-80™ SYSTEM COMPONENTS		
	Part No.	Description
CPU GROUP	8080A	8-bit Central Processor Unit, 2 μ s cycle
	8224	Clock Generator
	8228	System Controller
CPU OPTIONS	8080A-1	1.3 μ s cycle
	8080A-2	1.5 μ s cycle
	M8080A	2 μ sec cycle (-55 to +125°C)
I/O	8212	8-bit I/O Port (15 mA drive)
	8251	Programmable Communication Interface
	8255	Programmable Peripheral Interface
PERIPHERALS	8205	1 out of 8 Binary Decoder
	8210	Dynamic RAM Driver (8107B)
	8214	Priority Interrupt Control Unit
	8216	Bidirectional Bus Driver, Non-Inverting (50 mA)
	8226	Bidirectional Bus Driver, Inverting (50 mA)
	8222	Dynamic RAM Refresh Controller (8107B)
	8253*	Programmable Interval Timer
	8257*	Programmable DMA Controller
8259*	Programmable Interrupt Controller	
PROMs	8604	512 x 8, 100 ns
	8702A	256 x 8 Erasable, 1.3 μ s
	8704	512 x 8 Erasable, 450 ns
	8708	1K x 8 Erasable, 450 ns
ROMs	8302	256 x 8, 1 μ s
	8308	1K x 8, 450 ns
	8316A	2K x 8, 850 ns
RAMs	5101	256 x 4 Static CMOS, 650 ns
	8101A-4	256 x 4 Static, 450 ns
	8102A-6	1K x 1 Static, 650 ns
	8102A-4	1K x 1 Static, 450 ns
	8107B	4K x 1 Dynamic, 420 ns
	8111A-4	256 x 4 Static Common I/O, 450 ns

*Available 1st quarter 1976.

use the Intel 8080 system puters combined.



at -55 to $+125^{\circ}\text{C}$, and the 8080A-1 with a 1.3 microsecond instruction cycle for higher speed applications.

To help minimize system development time use the third generation Intel[®] MDS microcomputer hardware/software development system. This development system with its unique ICE-80 in-circuit emulator lets you simultaneously debug software and hardware, from initial prototyping right through production. The Intel

MDS is supported by six comprehensive software packages including a macro-assembler, ICE-80 interactive software driver and a diskette operating system.

In addition to the software packages in the development system, three cross product software packages are available on magnetic tape and on several time share networks. The Intel 8080 system is also supported by the industry's largest user's library, training courses and field applications assistance.

Start now with the new MCS-80 System Design Kit. It's a complete system for only \$350 and includes: An 8080A CPU, Clock Generator, System Controller, Programmable Communications Interface and a Programmable Peripheral Interface. You also get two 1 of 8 binary decoders, 256 bytes of static RAM, two kilobytes of erasable PROM (with the system monitor supplied in one kilobyte), a PC board, clock crystal, connectors, other assembly parts, plus a user's manual and programming manuals.

To order the MCS-80 kit, contact our franchised distributors: Almac/Stroum, Component Specialties, Cramer, Elmar, Hamilton-Avnet, Industrial Components, Liberty, Pioneer, Sheridan or L.A. Varah.

For your free copy of the new 8080 system brochure and our Intel[®] MDS brochure, write: Intel Corporation, 3065 Bowers Ave., Santa Clara, Calif. 95051. For \$5.00 we'll send you a copy of our new 236 page 8080 Microcomputer Systems User's Manual that includes complete hardware, software and interfacing data for all 8080 systems.

intel[®] Microcomputers. First from the beginning.

DEVELOPMENTS

and high output. There must be low plating stresses and absorbed hydrogen levels for good environmental stability, and the copper plating must be of constant thickness with an equi-axed grain structure to assure a consistent subsequent magnetic plating. Both solution and cell must be capable of plating at high current densities to produce a sound, thick copper; must consistently produce a fine, controllable, nodular, homogenous substrate for consistent memory properties from bit to bit; and must provide consistently good adhesion onto a BeCu wire substrate. The copper bath must have good throwing power for even plating, be able to level out defects not completely removed by the EP bath, be safe for nonprofessionals to use, and be easy to control, with wide chemistry, temperature, and current density tolerance levels.

Although several copper electroplating methods meet some of these requirements, no single procedure solves all of the problems; each has inherent undesired effects such as poor surface, narrow tolerance levels, and failure to produce equi-axed grain structure. Best results occurred with a modified potassium cyanide bath which overcomes all processing problems but which is not safe for use by untrained personnel.

For the copper electroplating stage finally decided upon, a copper cyanide solution is used rather than acid solutions. Hot solution from a reservoir tank (which keeps the solution at 50°C) is pumped into an overhead tank to provide a constant head for flow of solution into the copper plating cell. The copper cyanide plating bath consists of 30 g/l potassium carbonate, 15 g/l potassium hydroxide, 60 g/l potassium cyanide, and 60 g/l copper cyanide and has a free cyanide concentration maintained at 16 to 24 g/l. The bath surface is monitored continuously, microscopically and magnetically, to assure fabrication of a good quality wire surface. Adding trace amounts of cobalt optimizes topography of the substrate.

Most Permalloy films are prepared from metal sulfate electrolytes containing saccharine or other agents to control grain size. Such film can be plated by the mono-film process (which defines a single homogeneous film) or the mated-film process (which involves plating one high-

anisotropy film of nickel-cobalt followed by a low-anisotropy film of nickel-iron).

Key feature of this invention is a magnetic plating stage consisting of two magnetic plating cells and a stage similar in construction and design to the copper plating stage. Internal construction of the plating cell design, when used with the correct magnetic plating solution, produces an NDRO wire acceptable for missile system memory applications. The magnetic plating solution consists of nickel sulfate and nickel chloride in a 3:1 ratio with sufficient ferrous ammonium sulfate to produce the desired zero magnetostrictive film. The bath also contains boric acid, saccharine, and a wetting agent.

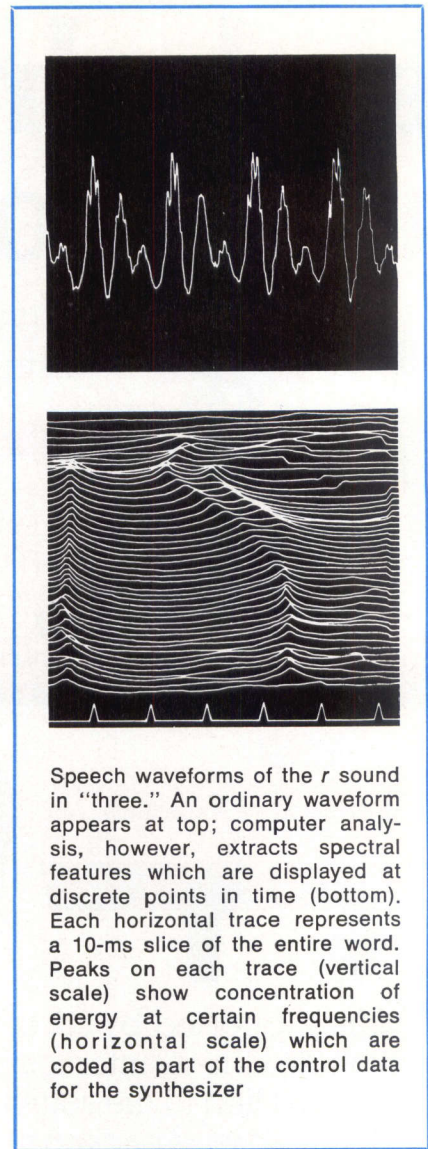
Magnetic heat treatment improves basic magnetic properties to acceptable levels and controls skew of the wire. Without magnetic heat treatment, plated wire becomes completely unsuitable as a memory element. It is done by applying heat in through-furnace coils and passing orienting current through the wire in a ceramic tube. A magnetic field of 25 oersteds is produced by passing current through coils located around the ceramic furnace tubes. Furnace temperature reaches 350 to 360°C, and orienting current heats wire an additional 10 to 20°C.

Continuous online testing insures the high quality of the product. Each bit length (55 mils) undergoes 10 tests to a severe pulse pattern. Defect-free wires, 256 bits long, are cut to a prescribed length automatically; defective pieces are cut and discarded.

According to Joseph P. McNamara, manager of the Laboratories' memory design section, typical applications of the 2.5-mil plated memory wire are in systems requiring fast, reliable, nondestructive readout, non-volatile, electrically alterable memory. Usage through the early 1980s is foreseen in aircraft, missile, and spacecraft guidance systems, as well as in high reliability controllers such as those used for large automated machine tools.

Computer Speech Analysis May Be Key to Low Cost Voice Response Systems

A small, solid-state voice synthesizer combined with highly compressed digital vocabularies which may be stored in the memory of any



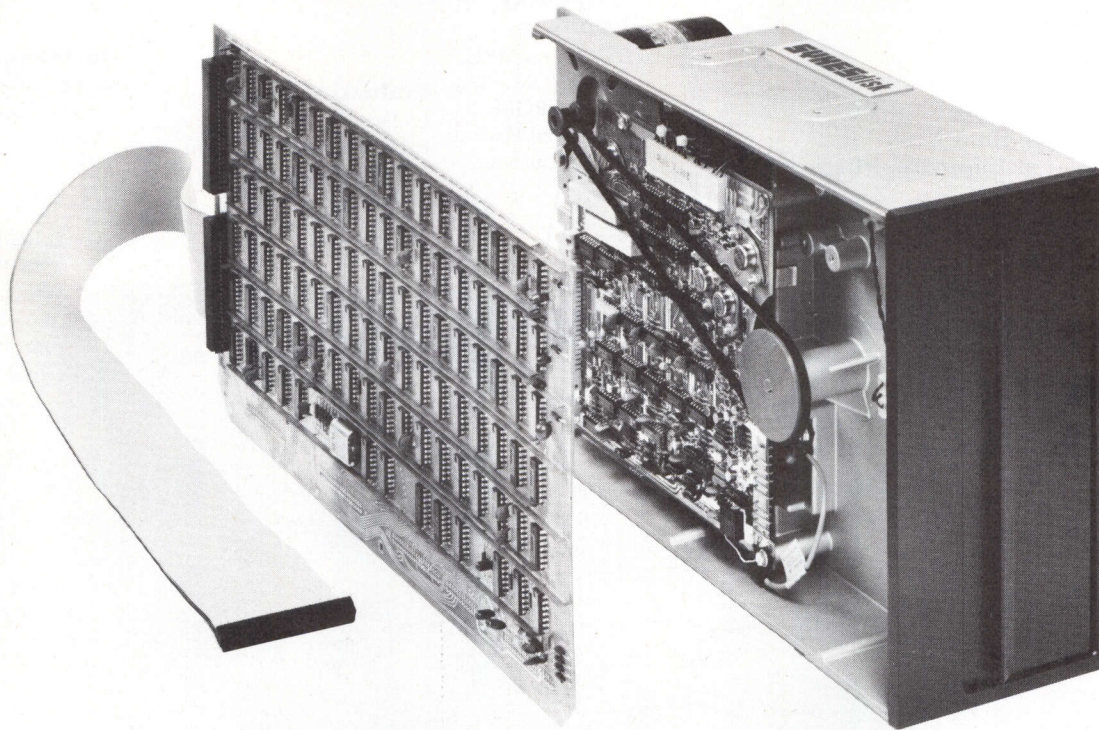
Speech waveforms of the *r* sound in "three." An ordinary waveform appears at top; computer analysis, however, extracts spectral features which are displayed at discrete points in time (bottom). Each horizontal trace represents a 10-ms slice of the entire word. Peaks on each trace (vertical scale) show concentration of energy at certain frequencies (horizontal scale) which are coded as part of the control data for the synthesizer

digital processor, such as a minicomputer or microprocessor, form the basis of a voice generator developed by Speech Technology Corp, Santa Monica, Calif. According to John E. Stork, the company's president, this development permits voice response to be applied in areas where it was previously impractical because of the high cost of conventional voice-response methods.

Key element is the software technique developed by the company. While electronic speech synthesis is not new, it has progressed from early means which duplicated the energy spectrum of speech sounds, to modern methods in which the synthesizer is a model of the human vocal tract—either in terms of the acoustic features of speech or the physiological functions of speech generation.

A difficult problem has been the derivation of control functions which will make the synthesizer produce natural speech. The method used by

Announcing the Sykes OEM Floppy System Kit. An idea whose time has come.



With our \$1,398 kit and your imagination, nothing can stop you now.

Sooner or later someone was bound to offer all the pieces—a smart controller, disk drives, interface cables—everything you need to build the machine of your dreams. Everything you need to talk to your microprocessor.

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THE KIT. The Sykes OEM Floppy System Kit gives you either an IBM compatible or Dual Density controller; one, two, three or four floppy disk drives per controller; interface cables from controller to disk drive; hardware interface for microprocessors.

PERFORMANCE. The heart of the kit, of course, is our controller. It provides hardware for what you ordinarily do in software. It saves time and money in developing, documenting and maintaining your system. You get the following hardware features with either the IBM compatible (256K Bytes/diskette) or the Dual Density (630K Bytes/diskette) controller:

- Hardware address search
- Automatic sector and track sequencing
- FIFO buffer for asynchronous operation
- Automatic CRC generation and detection

PACKAGING. *The packaging is unique; the total controller is contained on a single PC board and pancakes directly to one disk drive giving you minimum volume requirements for your overall system.*

INTERFACES ONLY AN OEM COULD

LOVE. When your microprocessor interfaces with our OEM Floppy Kit you'll use only 13 I/O lines. That's right, just 13: 1 Reset line, 3 Control lines, 1 Flag line and 8 Bi-directional data lines.

Our unique 8-bit Bi-directional bus is configured to transmit disk commands, status and data. Its simplicity drastically reduces the number of I/O lines, and connector requirements normally required in disk interfaces.

If you are using a standard mini, we've probably got a plug compatible interface and software for that too.

PRICE. Just \$1,398 buys you a single drive kit at quantity one. Obviously, attractive OEM quantity discounts are available.

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Sykes manufactures *all* the elements of our OEM Floppy Kit. Our disk drive has been extensively field tested, with several thousand of them in use right now throughout the world.

YOUR LETTERHEAD IS WORTH

\$100. Drop us a brief note on your company stationery asking for more information on the OEM Floppy Kit. Or call our marketing department at (716) 458-8000. If your inquiry results in an order for a complete kit, we'll apply a \$100 discount to your order. Offer expires April 1, 1976.

AMI 6800: The whole Kit.

Smart Terminal.

Complete program editing through CRT and keyboard. Also includes Modem communication to remote computers.

Magnetic Tape.

Cross product software— assembler, loader, simulator.

AMI 6800 Family.

It's all here: MPU, RAM, ROM, PIA, ACIA, PROM, USRT and Modem. By test, the best.

Evaluation Board.

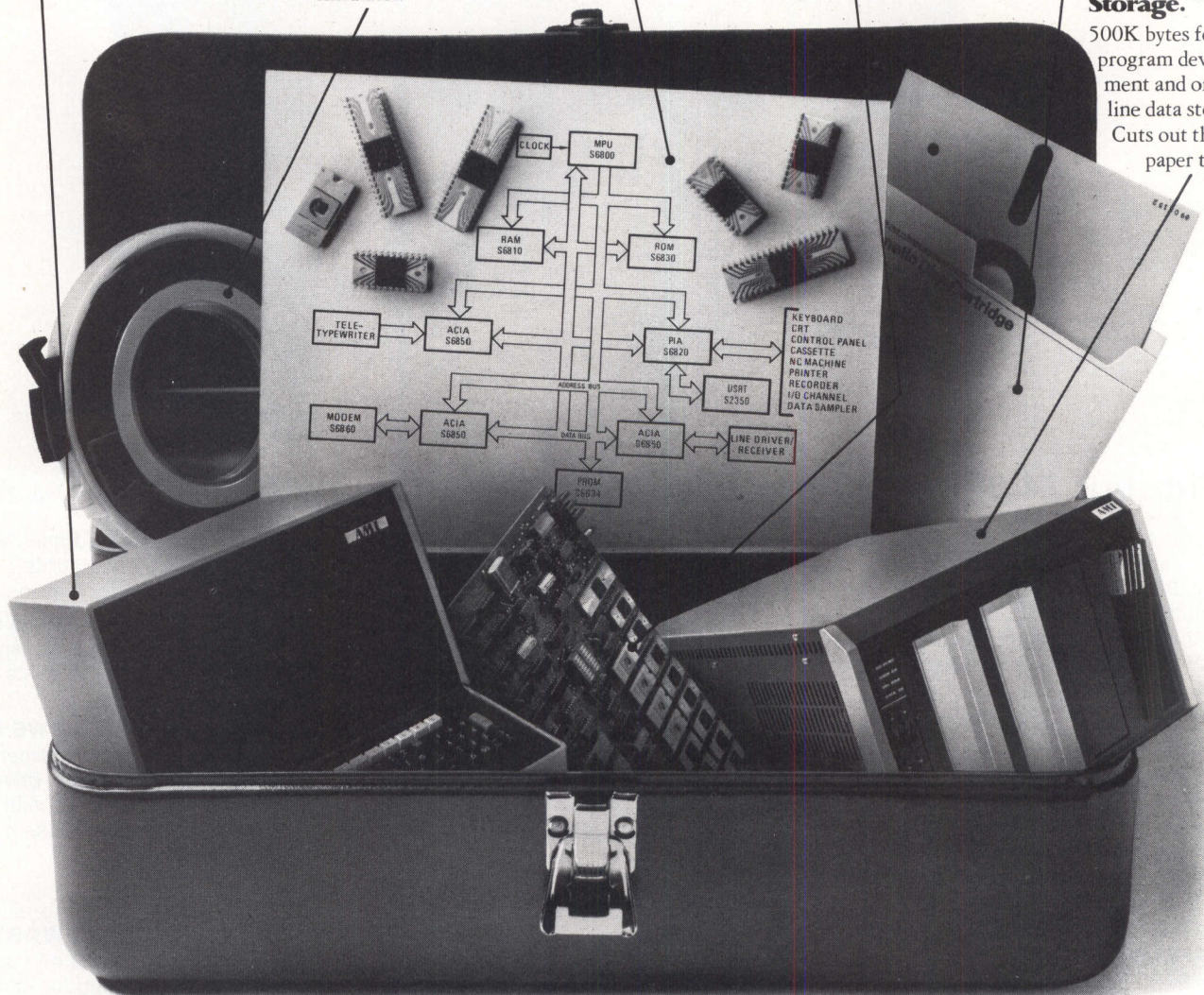
Includes everything you need to evaluate parts, program PROMs and, connected with a peripheral, run programs.

Dual Floppy Disk.

Storage for resident software— assembler, editor, etc.

Disk Program Storage.

500K bytes for program development and on-line data storage. Cuts out the paper tape!



Our AMI 6800 Kit is a big step forward in simplifying your design, evaluation and test programs. For example, our intelligent CRT is simple to operate with either resident or remote software. It really is smart, because it contains an S6800! And it's planned to have an in-circuit emulator added later.

Our dual disk is extremely useful for developing programs, and saves you hours of paper tape shuffling. And our Evaluation Board is loaded with

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this company starts with recordings of speech typified by the waveform in the top display of the Figure. Samples of the speech waveform are subjected to highly involved, offline computer analyses which reduce the information in the waveform to short codes that set up variable operating parameters in the synthesizer to duplicate the waveform. One step in the process is illustrated by the lower display in the Figure, where speech has been reduced to spectral features from which some of the synthesizer parameters can be derived.

This process provides an analog of the human vocal tract. When highly compressed digital codes stored in read-only memory are supplied to the synthesizer, human speech is recreated—retaining regional accents and usually allowing speaker identification. The method is so efficient that it stores voice messages in only 2% of the memory space used by conventional digitizing techniques.

Compressed digital codes used in the voice generators are prepared offline by highly automated computer analysis of real speech. Stored vocabularies may include separate words as well as continuous phrases in either male or female voice. Since codes are transmitted from memory to the synthesizer in short bursts, many synthesizers can be operated independently from a single vocabulary memory. The development is claimed to lead to a dramatic reduction in storage requirements for the speech data while retaining natural speaker intonation, regional accents, and usually speaker identity. Control data rates for the synthesizer are typically 1000 bits/s (4 or 5 syllables), allowing economical memory storage of substantial vocabularies. Words, phrases, or sentences are individually addressable, and a common vocabulary can be simultaneously shared among a large number of independent voice channels, each with its own synthesizer.

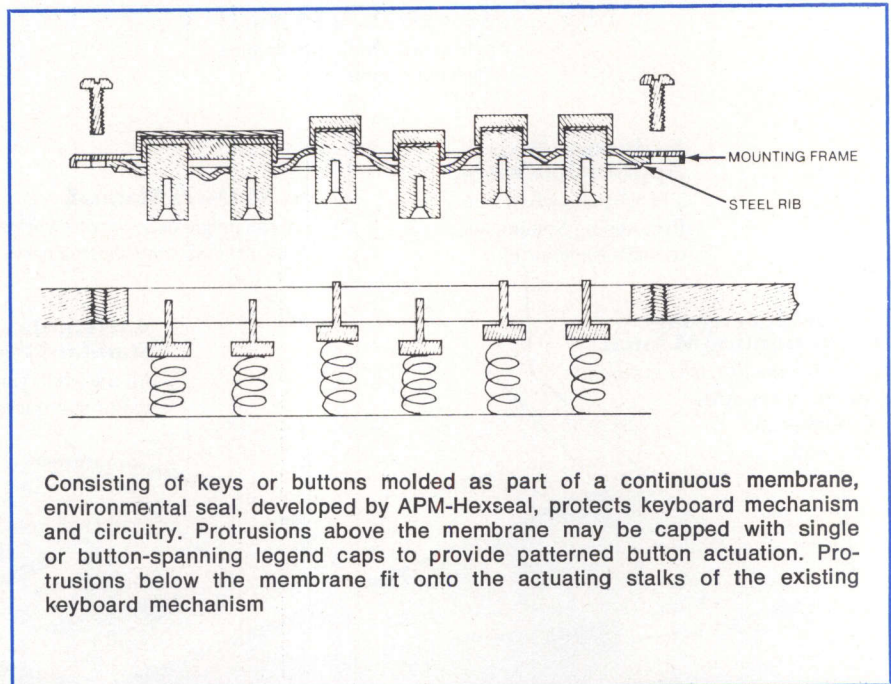
Evaluation units of a Model 200 voice generator, the first product to incorporate this development, are available with a standard 48-word vocabulary. They are entirely self-contained, solid-state voice response units including vocabularies and logic circuits to select prestored messages via a simple parallel digital interface or from a serial data input accepting ASCII codes at various standard baud rates. They can accept,

without significant modification, additional plug-in message storage up to two minutes of continuous speech.

Applications for the voice generator might be in digital communications systems for police cars and taxicabs, patient monitors in hospitals, wake-up systems for hotels, radio

interrogation to determine landing conditions at unattended runways, and talking calculators for the blind. They could also be used in process or control areas to eliminate distractions that occur when operators have to look away from their work to obtain instructions.

Environmental Seal Protects Keyboard Mechanism and Circuitry



Consisting of keys or buttons molded as part of a continuous membrane, environmental seal, developed by APM-Hexseal, protects keyboard mechanism and circuitry. Protrusions above the membrane may be capped with single or button-spanning legend caps to provide patterned button actuation. Protrusions below the membrane fit onto the actuating stalks of the existing keyboard mechanism

Permitting keyboards to be used in environments previously too hazardous, an environmental seal has been developed to protect both keyboard mechanisms and circuitry. Keyboards sealed with the device can be flushed with soap and water or with solvents.

Disclosed by the APM-Hexseal Corp of Englewood, NJ, which has applied for patents, the device replaces all buttons on any existing keyboard with its own keys or buttons, which are molded as part of a continuous silicone rubber membrane. When designed into new equipment, the unitized design eliminates the need for standard actuator buttons.

Molded-in keys protrude above and below the membrane. Protrusions above the membrane are capped with

appropriate legends; those below the membrane fit onto the actuating stalks of the existing keyboard mechanism. A convoluted web between each molded-in key permits full actuation without imparting any motion to adjacent keys. The molded key-and-membrane combination may be removed as a unit, allowing work to be performed on the underlying switching mechanism.

Covers have either a fixed or modular design. Modular units have changeable legend caps and multiple (button-spanning) legend caps for patterned button actuations. In the fixed design, pattern actuations are molded permanently into the sheet and cannot be altered. Combination units can be made for special requirements.

Amplifier-per-channel or differential multiplexing. System 620 now gives you a choice.



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In just 4 short years, our Series 100 has become the industry standard. With features such as low pass active filters having selectable cutoff frequency, computer programmable input sensitivity, and continuous analog outputs. And four versatile differential input amplifier configurations: low level, high level, simultaneous sample and hold, and ± 300 volt common mode.

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For high performance at a low price, you can't find a better differential multiplexer than our Series 400. It has programmable input sensitivities from 5 millivolts to 10 volts, 10 kHz channel sampling rate, and 120 dB crosstalk rejection.

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Signal Conditioning Series 300

You asked for it. Now here it is. A companion 620 unit which provides transducer excitation and signal conditioning. Series 300 has constant voltage and constant current excitation. Plug-in mode cards make it easy to configure a channel for a particular bridge, thermocouple, resistance

temperature device (RTD) or other types of transducers. Programmable calibration is standard and shares computer interface with either the amplifier-per-channel or differential multiplexed System 620.

The Essential Computer Interface

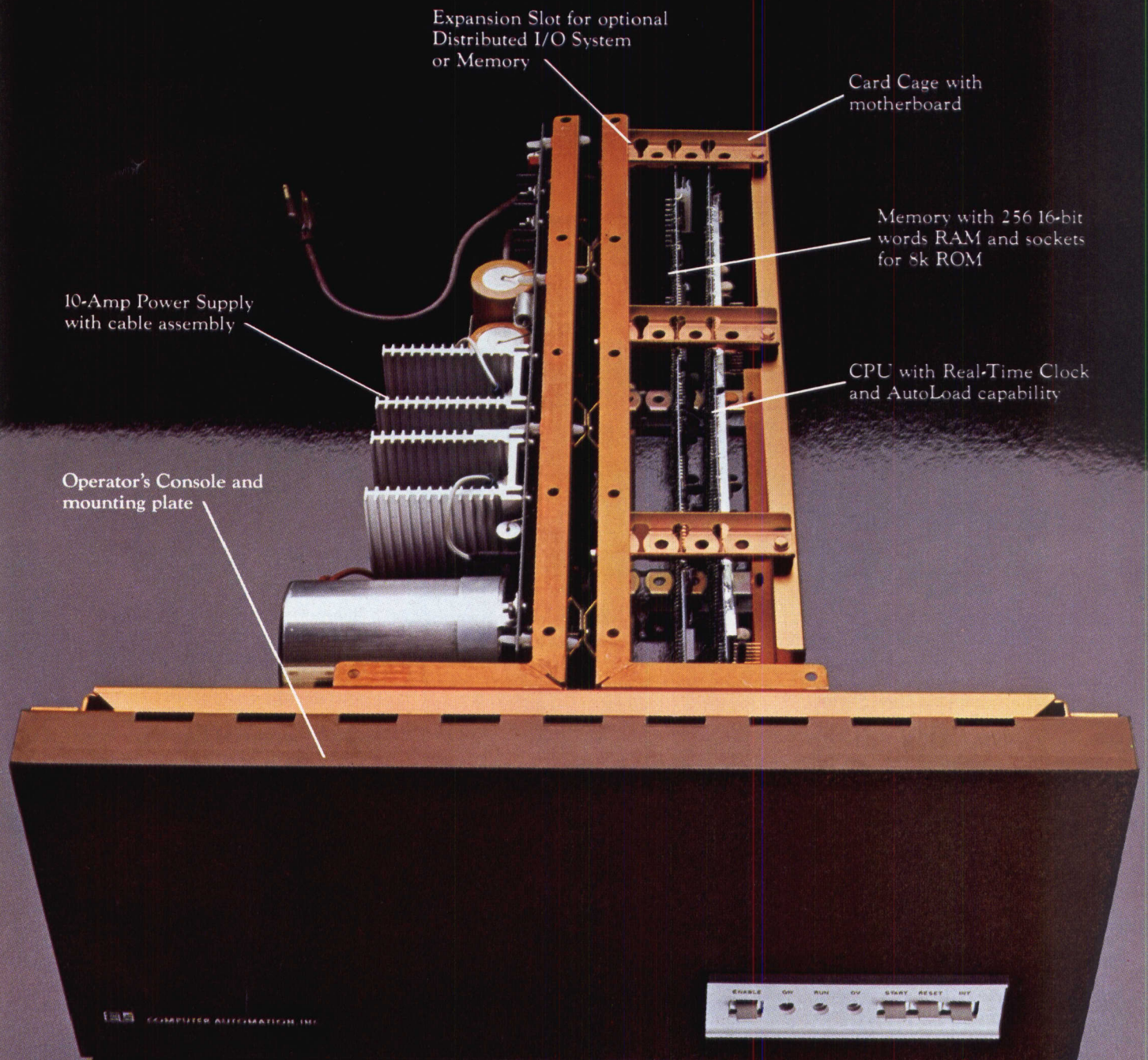
Today, a high speed data acquisition system is only as good as its computer interface. System 620 offers standard interfaces to most computers, some with Direct Memory Access, for high speed data transfer. Or, if you choose to design your own, our TTL logic simplifies the task by including most necessary interface functions right in the system.

For the whole 620 story — amplifier-per-channel, differential multiplexer and signal conditioning — contact Neff today. If you have an immediate requirement, request our System 620 Users' Manual — 30 pages of down-to-earth facts and figures.

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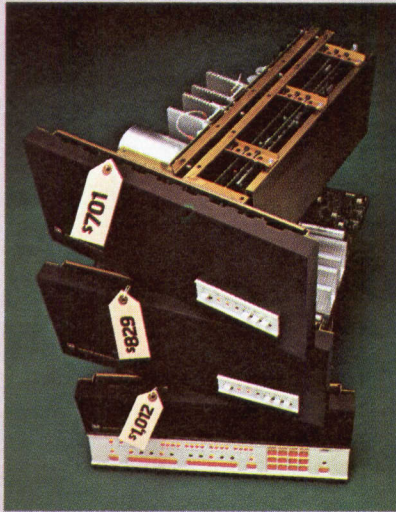
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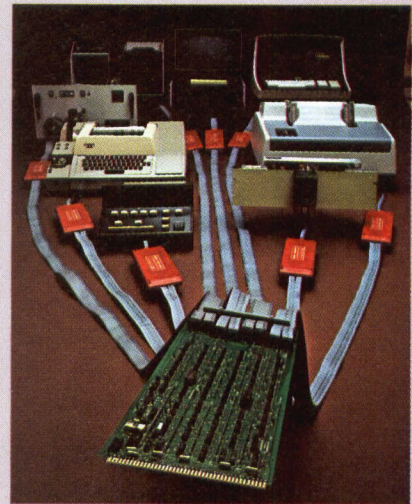
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Digital Measurement of Shaft Position: Synchros and Resolvers or Encoders

Sidney Davis

Associate Editor

Recently developed synchro/resolver-to-digital converters compare favorably with more familiar shaft angle encoders, providing the digital control engineer with a whole new set of design options

Output-shaft control is the ultimate objective in many systems, whether or not the systems are computer controlled. In digital computer-based systems, however, the control aspects become even more significant because of the inherent need for a suitable means of converting an analog angle to a corresponding digital word, which may then interface with a digital computer.

Such systems range across the industry: numerical control of machine tools, automation of factory and processing-plant operations, military and industrial electromechanical control and measurement equipment, shaft position and speed control, and hybrid computation. With the recent introduction of microprocessors for control use, the importance of digital control of shaft position, velocity, and acceleration in systems yet to be designed is likely to be enhanced even more.

Two approaches that have received wide acceptance for their performance and versatility are the shaft angle encoder, and the analog synchro or resolver plus a suitable converter. Principal objective of this article is to discuss and compare these approaches such that the system designer can then choose the one that is better for his requirements.

Encoder vs Synchro/Resolver

Until a few years ago, there was no really suitable alternative to the shaft angle encoder as a means for converting shaft angle to binary data. After all, what could be simpler in concept or more direct in application than an encoder whose internal sensors provide the required digital output with no additional conversion (although signal conditioning of the output lines may be required)? In contrast, a synchro or resolver requires a separate converter to encode analog voltages to the desired digital measure of angle.

It is only recently that the synchro- or resolver-to-digital (S/R-D) converter has become sufficiently compact, reliable, and low in price to effectively compete with the encoder. Now, the designer of computer-based electromechanical systems must become familiar with the comparative characteristics of the encoder and the S/R-D converter approaches.

Comparing Encoding Techniques

Two basic approaches in a simple positioning servomechanism are compared in the two parts of Fig. 1. Depending on system requirements, the encoder of Fig. 1(a) may be incremental or absolute. The incremental encoder—simpler and less expensive, and frequently used in stepping motor systems—usually includes direction sensing; the absolute-value type, though more complex, provides a more reliable indication of position in noisy environments. The arrangement of Fig. 1(b), using a synchro or resolver for angular sensing, requires a converter to change the analog output of these devices to digital form.

For simplicity and ruggedness, the synchro and resolver have the edge over the encoder. They are inherently low impedance, high voltage-level devices, not requiring signal-conditioning electronics. Input and output are transformer-coupled, with dielectric isolation and optimum output voltage levels.

A key feature of the resolver or synchro is that angular information is determined by voltage *ratios* rather than absolute values. Since output impedances are uniform and independent of shaft position, accuracy is not affected by loading (such as by stray capacitance), common mode voltages, or input line harmonics and noise. Accuracy is almost unaffected by lines which are hundreds of feet long.

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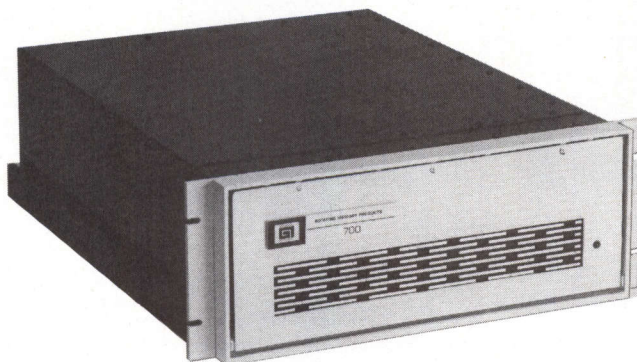
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In contrast, encoder output as generated at the sensors is relatively low level, with impedance dependent on the output state. Sensor output may include a significant noise component, as with brush-type encoders. The digital output lines are particularly sensitive to ambient noise. Encoding errors result directly from common mode voltages. The most common optical encoders develop (at the sensors) an output waveform more like a distorted sine wave than a square wave.

For these reasons, shaft angle encoders incorporate considerable signal-conditioning electronics. Such electronics are located within or very near the encoder, and perform the functions of amplification, isolation, noise rejection, and filtering. Low output impedance amplifiers on the data lines minimize the effects of line noise. It is a significant disadvantage that an out-

put lead is required per data line, usually requiring bulky cabling between encoder and computer. Where it is important to reduce the number of data lines, parallel-serial conversion may be incorporated in the encoder electronics.

Comparing Application Factors

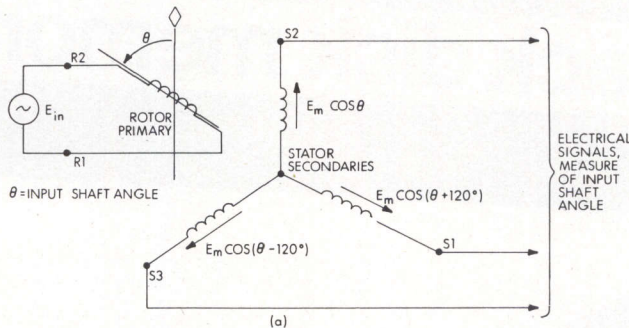
In many applications where noise is either low or can be controlled, excellent performance can be achieved at very low cost with an incremental encoder together with a high acceleration dc motor or a stepper. Typically, the encoder disc and sensor may cost about \$20. The principal disadvantage of incremental encoding is the counting error which may be caused by electrical noise. Some users are rejecting incremental encoder systems because of the increasing frequency of occurrence of power line disturbances causing system inaccuracies.

From the point of view of reliability and service life, especially in severe environments, the advantage appears to lie with synchros and resolvers. These devices were originally developed for military applications, to operate reliably under shock and vibration,

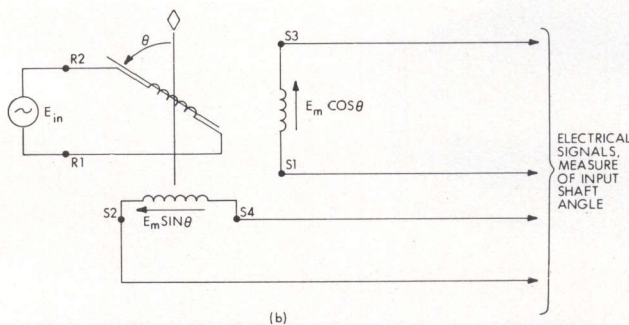
**Synchros and Resolvers for Converting
Shaft Angles to Electrical Signals**

Synchros and resolvers are small motor-like devices which are used to convert mechanical shaft angles to corresponding electrical signals for transmission and processing. Typically, they operate as rotary transformers, with primary winding on the rotor and an arrangement of secondary windings on the stator. In a synchro, secondary windings are connected in a 3-phase configuration; in a resolver, they are 2-phase. When the primary is energized from the reference line

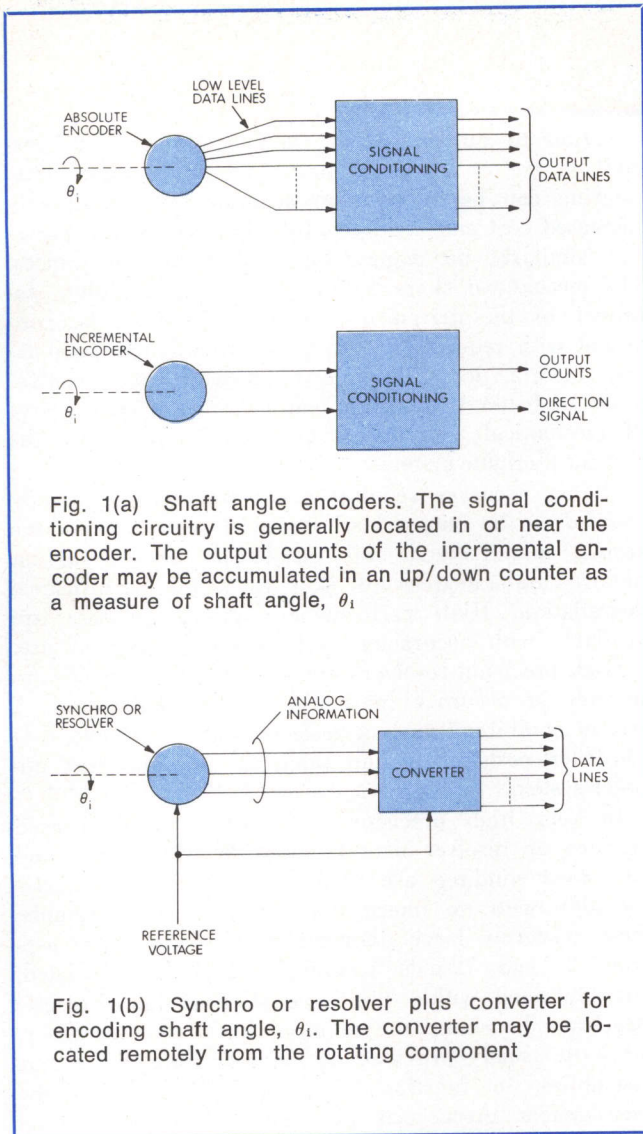
(typically 60 or 400 Hz), voltages appearing across the secondary terminals depend on the rotor shaft angle. Although the absolute values of the secondary voltages will vary with changes in reference voltage, shifts in line frequency, temperature changes, and loading, the ratios of the secondary voltages depend only on shaft position. S/R-D conversion devices operate on these ratios to generate a digital measure of the input shaft angle.



The synchro as an electromechanical rotating transformer. E_{in} is a reference carrier applied to the rotor through slip rings. Accuracies of the most common synchro types are between 5 and 10 arc min.



The resolver as an electromechanical rotating transformer. Although similar to the synchro, the resolver has 2-phase output winding rather than 3-phase. Resolver accuracies are typically about 3.5 min., or 0.001 rad



over wide temperature ranges, and in high humidity and salt spray environments. Even when design compromises are made to reduce manufacturing costs, the parameters are adequate for most industrial applications.

Comparatively speaking, the encoder is less rugged and more sensitive to non-standard conditions. Humidity, for example, can distort a plastic encoder disc, or interfere with the light path between source and sensor. In addition, environmental dirt can be a hazard.

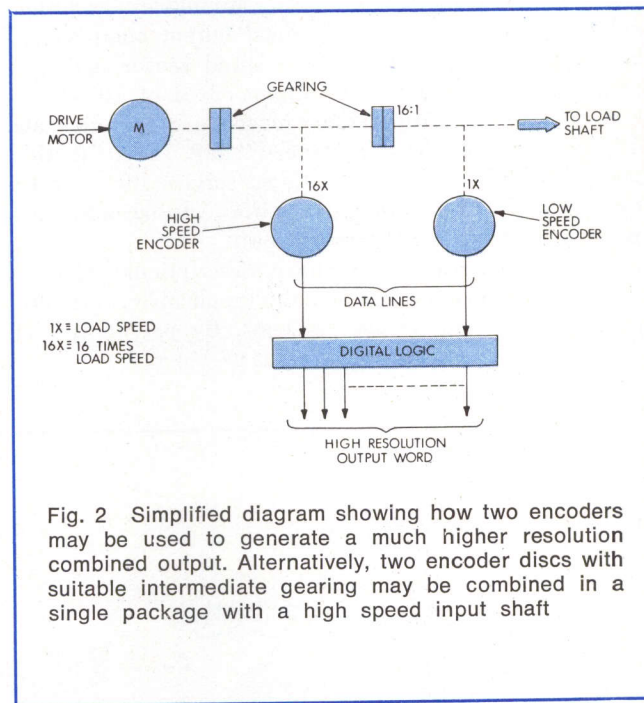
Lamp failure, one of the earlier reliability limitations of the optical encoder, has been substantially eliminated in many models through substitution of light-emitting-diodes (LEDs). Their lower light levels in comparison with incandescent lamps, however, place an added burden on the output electronics in amplifying and shaping the output data. Also, allowance must be made for the temperature sensitivity of LEDs and their decline in output over several years of operation. On the other hand, the absence of optical encoder brushes means long service life within specified environmental limits, and permits high speed operation, consistent with the speed limitations of the signal-conditioning electronics. However, although synchros

and resolvers do have brushes, their service life and speed capabilities are ample for almost all applications. Typically, brush life is at least 10^8 revolutions at speeds to 1200 to 1500 rpm, as borne out by several decades of test and field experience. A scanning radar operating at 100 deg/s requires over 10 years of 24-hr/day operation to accumulate 10^8 revolutions.

Higher Accuracy Applications

The most common means of achieving high accuracy and high resolution is to use a multi-speed system (Fig. 2) in which the angle-measuring device (or at least a portion of it) rotates at a substantially higher rate than the shaft being measured. When more than one rotation of the angle-measuring device is required to attain full scale, an additional sensing device may be necessary on a slower shaft—usually the output drive shaft—to avoid ambiguity. When using encoders in a multi-speed system, circuitry may be required to synchronize high and low speed transitions, to avoid “glitches.”

Fig. 2 shows a substantial gain in accuracy and resolution in a multi-speed system as compared with the characteristics of the individual high and low speed components. For example, 10-bit encoders in a 16-speed system exhibit, in effect, 14-bit performance. Combining high and low speed data becomes almost trivially simple when the multi-speed ratio is an in-



tegral power of 2, ie, 2, 4, 8, 16, 32, Otherwise it is much more difficult, such as for the commonly used 36:1 ratio of older angle-measuring systems.

Unfortunately, there are definite limits to the benefits of multi-speeding, determined primarily by the accuracy of gearing and coupling at the load. The high speed angle sensor, generating the less significant data bits, provides the critical data on output

DIGITAL CONTROL AND AUTOMATION SYSTEMS

angle. Logic circuitry synchronizes the low speed data, regardless of gearing and coupling errors. However, these same errors represent uncertainties in output shaft angle. For maximum encoding accuracy, precision gears in a minimum backlash configuration and high precision couplings are essential.

In typical moderate cost assemblies using standard, readily available mechanical components, output accuracy is of the order of two arc minutes, corresponding to one part in 10,800—equivalent to the resolution step of a 13-bit encoder. Note that this resolution can be achieved only when the high speed gearing from motor to output shaft is accessible. It cannot be achieved by gearing up from the output shaft and driving backward through the gear train, since gearing errors at the output shaft are multiplied by the gear train step-up ratio. For this reason, a 2-disc encoder incorporating an internal gear train is always driven at high speed by its drive shaft.

While the principal limit to attainable resolution and accuracy is in the mechanical output components, the rotational speed of the high speed sensor can also set a limit. For example, an output speed of 100 deg/s in a 64:1 multi-speed system means a rotational rate of 1067 rpm at the high speed shaft. Even if this speed is within component ratings, service life may be compromised. For this reason, life calculations must be carried out for the high speed shaft.

Note that although the above descriptions refer to encoders, conclusions are equally applicable to multi-speed synchro and resolver systems. By paying special

attention to output gearing and coupling, it is possible to get an extra bit or so of valid output data. Gearing can be made more accurate, at considerably increased cost and in larger diameters. Output couplings can similarly be manufactured to tighter tolerances. The mechanical characteristics (precision, rigidity, stability) of the driven load must, of course, be consistent with required accuracy. By attention to mechanical factors, it is feasible to measure and control angle to better than 0.5 arc minute. However, the cost of mechanical components may be several times the cost for 2-minute systems.

Higher accuracy requires a superior sensor, directly coupled to the output load shaft. In such systems, the design, manufacture, and installation of a coupling require high degrees of skill to avoid performance degradation. High performance optical encoders are available with accuracies to a second or two of arc.

High precision resolvers are available to about 20 arc seconds of accuracy in a 2¼-in. diameter frame. A system combining such a resolver with a suitable R-D converter costs about the same as an equivalent encoder system.

In very high precision applications, a multi-speed synchro or resolver may be used in which high and low speed windings are combined in a single magnetic assembly with no intermediate gearing. For example, these relatively large diameter devices may have separate 2- and 72-pole windings individually isolated, but contained within the same slots of the magnetic structure. To assure the required installation accuracy, they are usually provided as separate rotor and stator assemblies, to function as integral elements of the user system. Accuracies are available to better than 3 to 5 arc seconds. Alternatively, proprietary synchro-like devices, typically operating at 10 kHz, electrically equivalent to gearless, high ratio 2-speed systems with a second or two of accuracy, are also available.

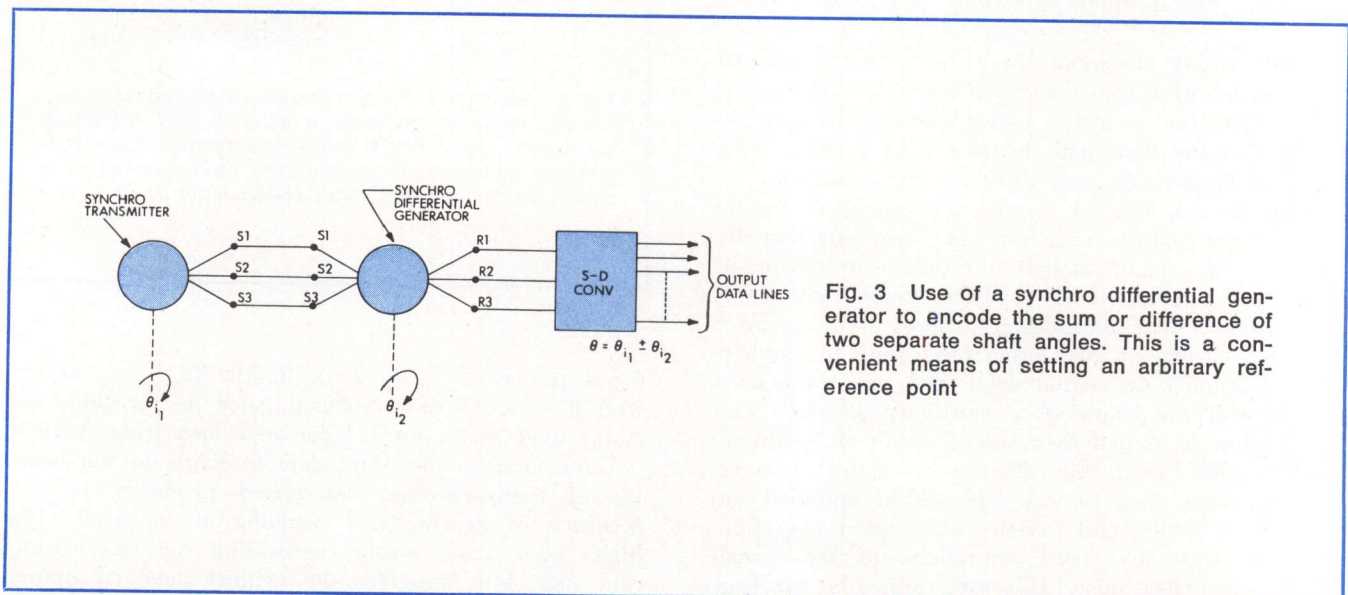
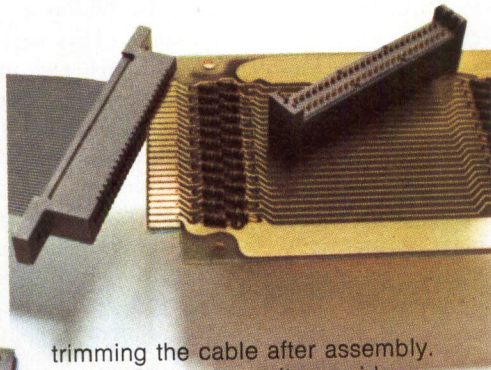


Fig. 3 Use of a synchro differential generator to encode the sum or difference of two separate shaft angles. This is a convenient means of setting an arbitrary reference point

Design with the complete flat cable/connector system.

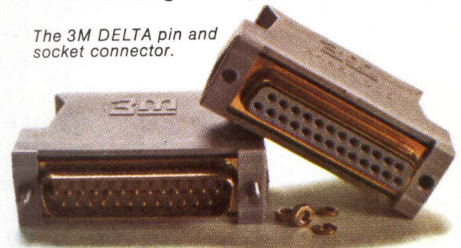


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The fast, simple "Scotchflex" assembly sequence makes as many as 50 simultaneous multiple connections in seconds, without stripping, soldering or

100 connectors to interface with standard DIP sockets, wrap posts on standard grid patterns, printed circuit boards, or headers for de-pluggable applications. 3M's DELTA "D" type pin and socket connectors are now also available. For full information, write Dept. EAH-1, 3M Center, St. Paul, MN 55101.



3M's "Scotchflex" line.

"Scotchflex" is a registered trademark of 3M Co.

Additional Application Factors

Aside from the features described, synchros exhibit an unusual flexibility. The synchro differential generator, when interposed between transmitter and S-D converter, permits addition or subtraction of its shaft angle to that of the transmitter (Fig. 3). This provides an especially simple means of setting in zero, or any arbitrary reference point.

Many S/R-D converters, with some additional circuitry, can generate output logic levels as a function of shaft position similar to that obtained from an incremental encoder. This can often be a convenient addition to the normal absolute output data.

According to some manufacturers, the most common user error is failure to distinguish between accuracy and resolution requirements. Errors occur in synchros and resolvers and encoders which may substantially exceed the resolution step, most noticeable in larger, high resolution devices. These errors generally vary slowly with shaft angle—typically one and/or two cycles per revolution. For relatively small angular displacement from a reference point, errors tend to more closely approximate the resolution step. This extra precision is a common reason for specifying resolution to closer tolerances than for accuracy.

A difficulty in some high performance S/R-D conversion systems is sensitivity to the electrical phase shift of the rotating component(s). As with electrical transformers, phase shift is greatest in small, low frequency components (50 to 60 Hz) and least in larger, higher frequency components (≥ 400 Hz). For this reason, 400-Hz resolvers and synchros are preferred even when 60 Hz is available. This requires a 400-Hz supply to be used as system reference—an

extra package and an added expense. However, the separate supply may also be used to filter out line noise. In addition, it permits a smaller synchro where required for convenient packaging.

Errors due to phase shift can be trimmed out at any given temperature. However, since phase shift depends on the electrical resistance of a copper winding, it will vary with temperature, introducing error. Where required, this error can be eliminated by well understood and highly effective compensation means developed for electrical resolvers. Compensated resolvers are generally required for best accuracy.

A frequently overlooked error component, characteristic of synchro and resolver systems, results from velocity voltages generated by rotation of the components. This error depends on the ratio of operating revolutions per minute to cycles per minute of line frequency, and becomes significant when this ratio exceeds perhaps 0.25. Since it is a relatively small error component, it need be considered only when 12- to 13-bit output precision at high rotational rates is required. It may usually be ignored in 400-Hz systems.

A special and increasingly useful type of synchro or resolver substitutes a unique rotatable transformer for brushes, thus completely eliminating a major limitation to component service life and maximum application speed.

Solid-state synchros are available to enhance the versatility of S-D conversion systems (Fig. 4). Although these are not widely known or well understood among potential users, their all-solid-state operation, computer system compatibility, and flexibility should lead to increasing application in the future.

Packaging

Factors related to packaging tend to favor synchros and resolvers over optical encoders. The critical packaging problem is placement of the angle-sensing device in relation to the shaft whose angle is being measured or controlled. A 1 $\frac{1}{16}$ -in. diameter electrical resolver coupled to the shaft can provide absolute accuracies of one part in 2^{12} to 2^{13} . Its small size is in itself a contribution to its ruggedness and reliability. Relatively few leads are used in comparison with an encoder, and no electronic circuitry is required in its immediate vicinity (which is frequently the least accessible part of the system).

In some applications, where leads are brought out through slip rings, minimizing the number of leads is a major design goal. Similarly, packaging the electronics remote from the measured shaft, in a generally more protected environment, often adds to system simplicity, reliability, and maintainability.

Summary

Until recently, the most practical means of encoding shaft angle was the digital encoder. Alternative means based on the electrical synchro or resolver were overly complex and not at all cost-competitive.

Compact S/R-D converter packages are now available, however, which are reliable, easy to use, and low in cost, giving the engineer a wide range of options for optimizing his system design. In most applications, S/R-D systems compare favorably in performance and price with encoder systems. □

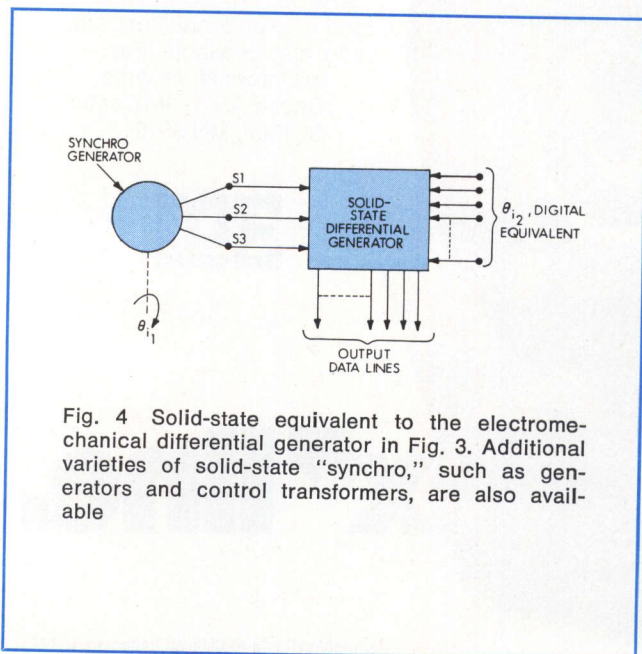
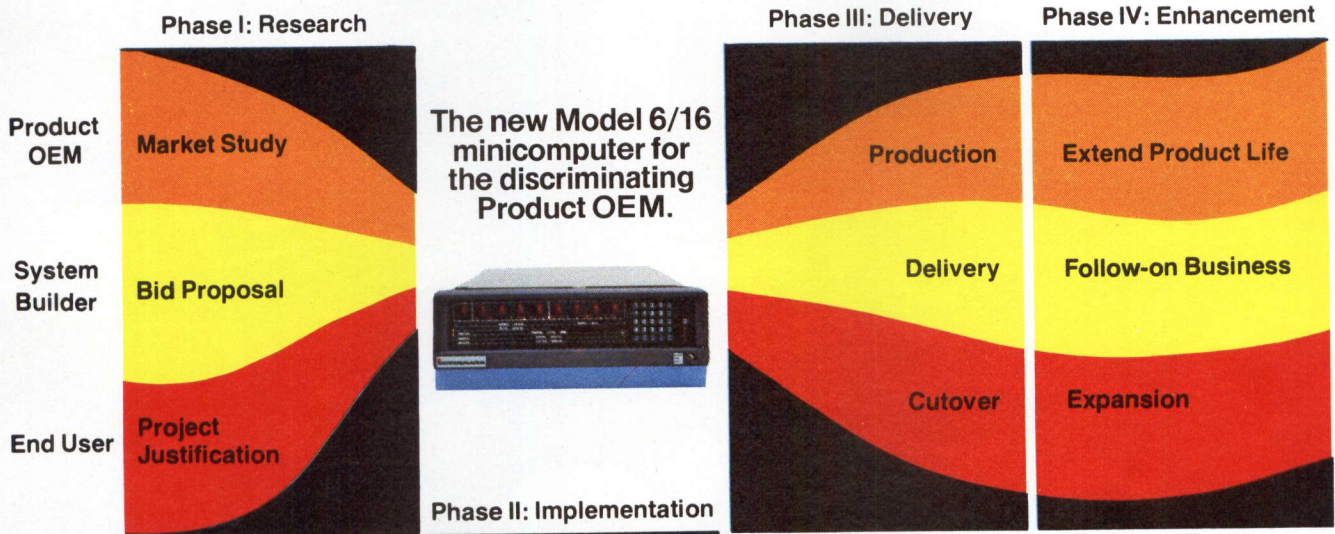


Fig. 4 Solid-state equivalent to the electromechanical differential generator in Fig. 3. Additional varieties of solid-state "synchro," such as generators and control transformers, are also available

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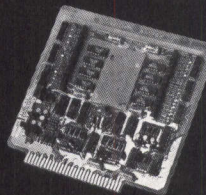
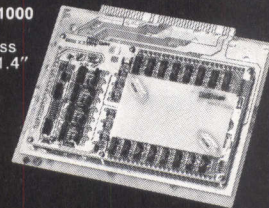
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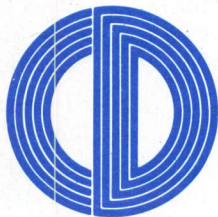
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Systems Problems...
Application Problems...
Business Problems...

CompDesign/76 provides digital electronics engineers the most comprehensive forum for understanding their problems and the state-of-the-art capability for solving them.

Workshop forums, product seminars and exhibits are all part of one event, and are all aimed at bringing these problems into focus . . . how they inter-relate . . . how to solve them.

Computer Design Magazine has assembled a group of professionals in each of these areas to present the most current information, listen to your problems and ideas and work out the best avenues to solutions.



COMPDESIGN/76

**Three days of Forums, Seminars and Exhibits directed at you,
the Computer Design reader**

BOSTON NEW YORK CHICAGO LOS ANGELES SAN FRANCISCO

The most complete concentration of technical sessions and product exhibits in the computer industry is scheduled for three days each in Boston, New York, Chicago, Los Angeles and San Francisco in 1976.

Tailored for multiple-unit buyers, including traditional OEM's, systems houses and in-house systems people, CompDesign/76 will provide the most-up-to-date practical information on microprocessors, peripheral devices and business topics relating to the design and implementation of computer systems.

The touring conference is sponsored by Computer Design Magazine and the three days of sessions will be geared to all levels of digital electronics engineers with special emphasis for computer-based systems designers and technical management. The meetings will be held in conjunction with the Computer Caravan in these cities and in addition to forums on the above topics, attendees will be eligible to attend exhibitor seminars and the Computer Caravan exhibits with no additional charge.

The co-appearance of CompDesign/76 and the Computer Caravan in the above cities, comprised of forums, product seminars and exhibits, will provide attendees with the most complete and integrated overview of the computer industry to date.

Forum sessions will be set up and administered by personnel with years of experience in presenting technical information, and the material will be presented by established, knowledgeable people in the engineering and technical management fields.

During each of the three days in each city, forum sessions will take place during the morning, exhibitor seminars during the afternoon, and the exhibits will be open from 10 a.m. to 5 p.m.

The forum sessions will be keyed to practical, state-of-the-art information to help OEM suppliers and designer-users put together more efficient and reliable products and systems. These will not be tutorial sessions but give and take meetings that will put the problems on the table for thorough discussions.

Tuesday (Day 1)

CONCURRENT WORKSHOPS UNDER THE THEME OF BUSINESS TOPICS FOR THE COMPUTER PRODUCT MANAGER.

a) "Specmanship": How to cope with it.

Specmanship is the art of distorting a specification without actually making a false statement. This session covers subtle variations in parameter definition and test methods, omission of qualifying statements, use of "typical" rather than properly toleranced values, and many other misleading techniques which add to the difficulty and cost of choosing the right components and equipment.

The session will cover the many forms which "specmanship" can take, with topical examples, how to cope with it, and inter-action between users and vendors on the more controversial aspects.

b) Standardization — status, future directions.

Standardization, a valuable tool in dealing with "specmanship", is also a means for simplifying the application and interfacing of electronic equipment. However, standardization is especially difficult to implement in the rapidly growing and highly competitive computer industry. The workshop will review the nature and role of standardization procedures, with pertinent illustrative examples. It will explore possibilities for accelerating the standardization process while still encouraging creativity in product development and application. Vendor-user interaction will be a prime element of this forum.

c) Buying from new or very small companies.

New small companies are frequently structured (at least initially) around technologically advanced products which extend the state-of-the-art. However, there is an element of risk to the user who must be assured that the advanced product supplier will remain in business and continue to provide necessary customer support for the life of the application.

The session will consider appropriate criteria for small company evaluation, including decision-making trade-offs. Specific experiences will be used as illustrations.

d) Testing and quality of purchased products, economic factors.

As part of the effort to cut costs in the highly competitive digital electronics industry, many companies are spending less on quality control. The consequences are costly production line rejections as well as field failures. Frequently, the only practical user alternative is to set up a comprehensive incoming inspection system.

The workshop will consider the problems of testing and quality, with emphasis on economic trade-offs. Strong interaction between vendors and users will assure airing of all pertinent factors.

Wednesday (Day 2)

CONCURRENT WORKSHOPS UNDER THE THEME OF PERIPHERALS FOR MINI- AND MICRO-COMPUTERS.

a) Defining characteristics of mini- and micro-peripherals.

The development of mini- and micro-computers has made substantial computing power available at low cost, with a forecast for more of the same. As a result, computer applications are expanding phenomenally. However, since the cost of peripherals can easily exceed the computer cost, the development of mini- and micro-peripherals with computer-compatible performance and price, is a major requisite for continued growth.

The sessions will estimate the desired nature, performance and price of peripherals for micro-computer applications. Some guidance will be provided by comparison with the evolution of peripherals for mini-computers.

b) Interfacing and standards.

Important simplifications in system design and application may be achieved by the establishment of comprehensive interface standards for mini- and micro-peripherals.

The workshop will review the status of current standards and standardization programs, and will emphasize desirable future trends. The role of the microprocessor and associated LSI devices in the interface function will be illustrated by specific examples.

c) Micro-peripherals — current status vs. users' needs.

The defining characteristics of micro-peripherals are examined in another forum session. This session reviews the state-of-the-art of micro-peripherals with regard to type, availability, general characteristics, and price. Special attention will be given to specific user needs, including performance and price goals. Vendors are expected to comment on the practicality of user expectations.

d) Future trends.

In view of the emphasis on new peripheral development, some effort will be made to anticipate future trends. For example, the impact of solid-state alternatives (such as CCDs, bubble memories) to electromechanical mass storage means. The session will seek out the latest vendor opinions on the impact and timing of new products arising from today's laboratory models.

Thursday (Day 3)

CONCURRENT WORKSHOPS UNDER THE THEME OF MICROPROCESSORS

a) The State of the art; availability.

The state-of-the-art in the microprocessor design is changing so rapidly, that "keeping up" is a continuing and time-consuming process. This session will examine the current state-of-the-art, with particular attention to performance and availability of the newer types.

b) Application factors; user needs.

The typical system design engineer using microprocessors for the first time, will usually require considerable application assistance. The nature and adequacy of this assistance, as provided by microprocessor suppliers, will be explored. Users will be given ample opportunity to discuss their experiences, both good and bad, in getting started with microprocessors, and to describe the kinds of support they would like to have. Interaction between users and vendors should be particularly illuminating.

c) Applications — variety of examples.

The versatility and benefits of the microprocessor will be illustrated by a variety of application examples presented by users. The principal areas of microprocessor usage will be covered. Discussion will be moderately technical, emphasizing application requirements, the benefits expected from the microprocessor, microprocessor performance requirements, reasons for the specific microprocessor choice, and problems encountered in application. Users at this session will have ample opportunity to ask questions and to describe their own application needs.

d) Future trends.

Because of the impact of the microprocessor on the entire digital electronics industry, estimating future trends is critically important for long-term product development and marketing planning. Estimates must consider the timing of new products, improvements as well as breakthroughs in technology, ultimate technological limits, and price trends. The forum session will cover these topics, as well as their impact on microprocessor usage and on new applications.

Three reasons why you should attend **COMPDESIGN/76**

1. Keep Abreast of Your Industry.

Techniques, technology and applications in the computer industry change faster than in any other industry.

Basic technology developments have given us new products — especially in the mini and microcomputer areas. These have led to new applications which means new interfaces, new customers, new business problems, specification changes, re-design, and testing problems. The impact can be seen by looking at the growing market for microprocessors and microprocessor-based equipment, just as one example.

The forums and seminars at CompDesign/76 will bring together knowledgeable people in problem areas such as those cited above to give you an update on developments and how to deal with them.

You will attend shirt-sleeve sessions with plenty of opportunity for two-way communication. You will be exposed to problems concerned with your particular discipline or function. And you will better understand how you affect and are affected by other areas of the industry.

"The Computer Designers' Forum, the name given to the technical program of CompDesign/76, is an extension of the editorial objective of Computer Design Magazine. You can expect the same approach as we follow in our pages: no vendor pitches, but an important dialogue on digital equipment and systems technology by designers who have solved very specific problems.

John Camuso
Editor, Computer Design Magazine

When returning the registration form make sure you designate which days you would like to attend and check the city.

Boston, March 2-4	Showcase 1-2-3 & 4 Movie Theater, Woburn, Mass.
New York, March 9-11	Mariott's Essex House
Chicago, April 13-15	McCormick Place On-The-Lake
Los Angeles, May 4-6	Los Angeles Convention Center
San Francisco, May 11-13	Civic Auditorium

2. Exchange Ideas With People Responsible for Progress in the Industry

You will be meeting and exchanging ideas with people from all levels and all areas of the industry who are responsible for making things happen. OEM suppliers and designer-users will be interacting in all aspects of the forums and exhibitor seminars. You will get first hand knowledge of problems from people who have experienced them, and who will describe their solutions. You will have an opportunity in a face-to-face environment to state your views, question speakers and generally work out problems that affect your job and your industry.

3. "Backyard" Availability

These forums and seminars will be held in five regional cities. The cities were selected because they are centrally located in the largest "computer markets" in the U.S. and have the accommodations required to make the meetings a success.

For most industry people it will be a relatively short trip to one of the sites, which is a positive cost factor in a cost-conscious economy.

In addition to the morning forums you will have the advantage of attending, free-of-charge, the Computer Caravan exhibits (which will be held in conjunction with CompDesign/76) and exhibitor seminars for either conference.

DAILY SCHEDULE OF EVENTS

9 am to 1 pm — COMPDESIGN FORUM
9:00-9:40—Welcome, Orientation and Introduction to theme of the day presented by Sid Davis, Associate Editor, *Computer Design Magazine*.
9:45-11:00—Four Concurrent Workshops (First presentation)
11:00-11:10—Coffee Break
11:10-12:25—Workshops (Repeated)
12:30-1:00—Wrap-up Panel
1:00 to 2:00—Dutch Treat Lunch
2:00 to 5:00—Product Seminars

Exhibits: Open 10:00 to 5:00 each day

WHAT IS YOUR PRINCIPLE ENGINEERING FUNCTION OR MANAGEMENT RESPONSIBILITY?

- E1 Computer-Based Systems Design
- E2 Digital Systems Design
- E3 Digital Equipment Design
- E4 Digital Circuit Design
- E5 Interface Engineering
- E6 Data Communications Engineering
- E7 Test/Inspection/Reliability Engineering of Digital Equipment
- E8 Consulting/Educating on Digital Electronics

WHAT IS YOUR ORGANIZATIONAL CLASSIFICATION:

- C1 Executive Management
- C2 Engineering Management
- C3 Senior Personnel
- C4 Staff Personnel
- C5 Consultant/Educator

WHAT IS THE NATURE OF YOUR ORGANIZATION?

Use code for best description.

- Manufacturer of:
- 02 Large Computers
 - 04 Minis/Medium Computers
 - 06 Micros (excl. ICs)
 - 08 Memory/Storage Equip (excl. ICs)
 - 10 I/O Equip (incl. Data Terminals)
 - 12 Data Comm Equipment
 - 14 Computer-Based Systems
 - 16 Office/Business Machines
 - 18 Industrial Control Equip
 - 20 Test/Masurement Equip; Instruments
 - 22 Comm Equip (other than Data Comm)
 - 24 Navigation/Guidance Equip
 - 26 Undersea/Aircraft/Missile/Space/Ground Support Equip
 - 28 ICs/Circuit Modules
 - 30 Consumer Electronic Products
 - 32 Medical Electronic Products
 - 34 Other Products Incorporating Digital Electronics:
- Other organizations:**
- 36 Systems House
 - 38 Industrial Company Using/Incorporating Digital Electronic Equipment (incl. Computers) in Manufacturing/ Research/ Development Activities
 - 40 Commercial User of Digital Electronic Equipment
 - 42 Government/Military Agency or Installation
 - 44 Independent Research/Test/Design Laboratory (i.e., one not connected with a manufacturing company)
 - 46 Independent Consulting Company
 - 48 Educational Institution
 - 50 Other



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TOTAL NUMBER OF DAYS FOR ALL PEOPLE BEING REGISTERED WITH THIS ORDER

First Day is \$50, additional days are \$35 each (for example, if you have three people registering for a total of eight days, fee will be \$50 plus 7 times \$35 (\$245), or \$295 for all people).

Calculate *total fee due* and enter here

Remember that any single-day Forum registration also entitles you to attend all three days of exhibits.

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REGISTRATION FORM

Use this form to register up to two different people for any number of days. Please fill out completely and mail to:

THE CONFERENCE COMPANY
COMPDESIGN 76 Registration
 797 Washington Street
 Newton MA 02160

(If form below has been removed fill out reverse side.)

You may charge registration to your American Express Credit Card. See Check Box below.

Register me for: All three days, or: 1st Day 2nd Day 3rd Day

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Telephone (____) _____

Please enter proper codes from box with listing:

Function (E) _____ Organizational Classifications (C) _____ Nature of Organization _____

CHECK CITY IN WHICH YOU PLAN TO ATTEND

- Boston March 2-4
- Los Angeles May 4-6
- New York March 9-11
- San Francisco May 11-14
- Chicago April 13-15
- Charge my American Express Card

Your Card number _____ Expiration Date _____

Your Signature _____

Check Enclosed Purchase Order Enclosed

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- 10 I/O Equip (incl. Data Terminals)
- 12 Data Comm Equipment
- 14 Computer-Based Systems
- 16 Office/Business Machines
- 18 Industrial Control Equip
- 20 Test/Measurement Equip; Instruments
- 22 Comm Equip (other than Data Comm)
- 24 Navigation/Guidance Equip
- 26 Undersea/Aircraft/Missile/Space/Ground Support Equip
- 28 ICs/Circuit Modules
- 30 Consumer Electronic Products
- 32 Medical Electronic Products
- 34 Other Products Incorporating Digital Electronics:

Other organizations:

- 36 Systems House
- 38 Industrial Company Using/Incorporating Digital Electronic Equipment (incl. Computers) in Manufacturing/ Research/ Development Activities
- 40 Commercial User of Digital Electronic Equipment
- 42 Government/Military Agency or Installation
- 44 Independent Research/Test/Design Laboratory (i.e., one not connected with a manufacturing company)
- 46 Independent Consulting Company
- 48 Educational Institution
- 50 Other



COMPDESIGN/76

IEEE Computer Society International Conference

Jack Tar Hotel

San Francisco, California
February 24-26

Revealing products, services, and ideas now on the drawing boards, but expected to appear in the field within the next five years, COMPCON 76 Spring will explore recent advances in circuit technology and attempt to determine what effect they will have on the computer industry. Under the direction of general chairman Dr Sidney Fernbach of Lawrence Livermore Laboratory's Computation Dept, and program chairman Dr Herschel H. Loomis, Jr, University of California, Davis, 23 sessions will cover hardware, software, firmware, technology, and applications under the general theme "Computers: The Next Five Years—Evolution or Revolution."

A full-day tutorial, "Unique Aspects of Microcomputer Applications," will be given on Monday, Feb 23, immediately preceding the Conference. Chaired by Robert H. Wyman, Jr, Lawrence Livermore Laboratory, and with Fred F. Coury, an independent consultant in digital designs, as instructor, the tutorial will attempt to define microprocessors, deal with their architectures and process technologies, and analyze hardware and software support necessary for them. As an application example, one complete microprocessor-based system will be analyzed and described in detail.

Among the events of special interest to attendees are the Keynote Session on Tuesday morning, during which Dr Edward E. David, Jr, Executive Vice President of Gould, Inc will set the tone for the Conference in his Keynote Address. To provide further perspective on sessions to follow, Dr J. Presper Eckert, Vice President and Scientific Advisor for Sperry Univac will review the history of computing. In addition, Conference Kick-Off Talks, planned for Tuesday afternoon, divide the broad subject of computers into hardware, software, firmware, technology, and applications. These subjects are taken on by Dr Michael Flynn, Stanford University; Dr Robert McClure, Palyn Associates; Michael J. Galey, IBM; Dr Jack S. Kilby, consultant; and Andy Knowles, Digital Equipment Corp, respectively. Short Note sessions, cocktail parties on Tuesday and Wednesday evenings, and a Conference Panel discussion should also prove of special interest.

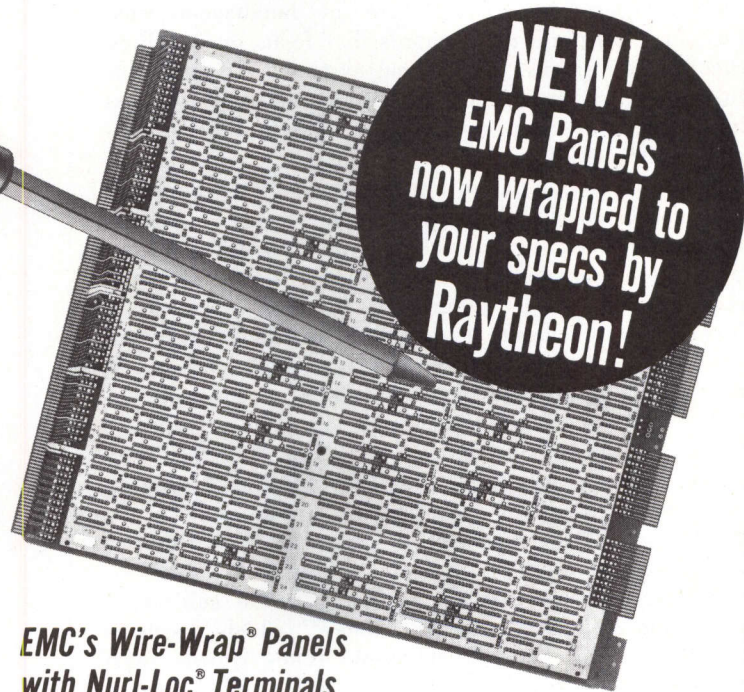
(Continued on p 68)

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On the regular program, hardware-oriented sessions take up the topic of "What Will Microprocessor Hardware Evolve Into?" which covers software issues in LSI microprocessor design, and reliability which can be attained with triple modular redundancy. "What Can We Expect in Hardware Design Techniques" illustrates uses of programmed logic as a hardware design tool and attempts to define when and where to use programmed logic arrays; "The Personal Computer" discusses home and hobby computers.

Also under consideration are "What's Going On In the Rest of the World?" with details on computers in Japan, Western Europe, and China, Russia, and Eastern Europe, and how computers are being used in crime, which scrutinizes the topic from aspects of computer security, legal ramifications of computer abuse, and computers and data abuse.

Among the "crystal-ball" sessions are one devoted to upcoming microprocessor software, with a panel considering differences between mini and micro software; an examination of mass storage systems, focusing on effectiveness and practical applications; and expected data communication techniques, discussing packet switching and network interfaces. Computer networks are also examined in a "what will happen?" session, looking at the common carrier as a catalyst, some trends in network architecture, and user-service quality in a distributed network. The reality of distributed computer systems is discussed by a panel composed of Philip Ware, Servaro Ornstein, and T. C. Chen.

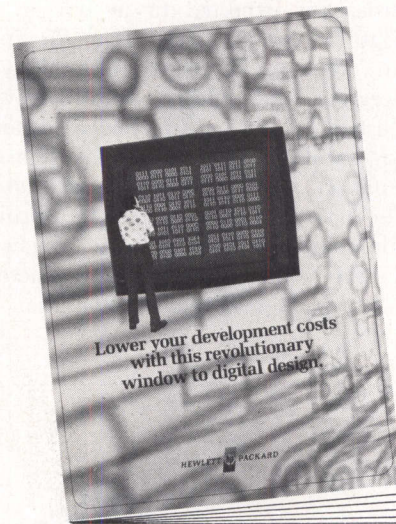
Solid-state memories—CCDs vs RAMs for bulk use and IIL vs NMOS for main memories—are highlighted in an attempt to determine what will become the prevailing technology. The future of language-directed machines is examined in papers that focus on graphics, theory and practice of personal systems, and problems in push-down stack implementation of such systems as well as on language-directed representation of machine instructions.

The impact that microprocessors may have on super computers, and whether supers and minis will squeeze out mainframes are considered in a session that attempts to determine what the future will be for super computers. "Design Automation in 1980" presents a 5-year view of design systems and predicts what will be forthcoming in testing and modeling. Automated production of discrete parts, its effect on productivity, and the use of real-time industrial process control are topics under consideration in "How Will the Computer Advance Automation?" Two additional sessions are devoted to data base systems, pointing out the directions which management systems, architectures, and storage hierarchies are likely to take.

How computers will affect society is the subject of "Will the Computer Replace Money," which discusses the relationship between electronic funds transfer systems and the financial community and whether or not it is liable to be a permanent one. Another session evaluates the relationship of computer science curricula to computing, with speakers examining "Computer Science and Education Programs—Today and Tomorrow," "IEEE Computer Society Curriculum Recommendations," and "IEEE Regional HELP Activities," as well as a "Bachelor of Arts in Computer Programming." □

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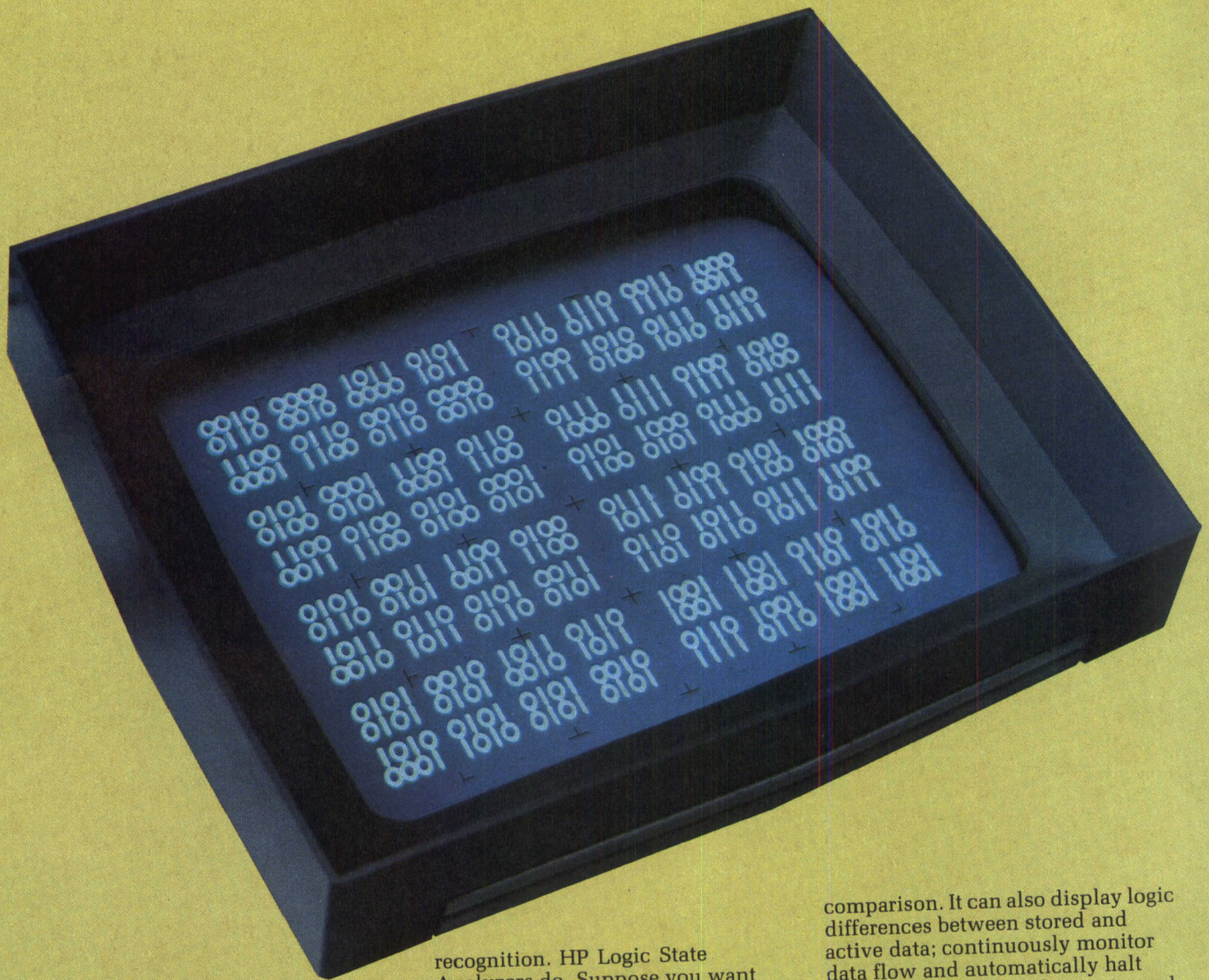
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If you rely primarily on we think you're



Now we're not advocating that you stop using your scope. You've always needed one and you always will. But if a scope is all you're using, you're probably wasting a lot of time. A couple of years of field experience with logic state analyzers has shown us that about 85% of digital troubleshooting problems can be solved faster with a logic state analyzer than with a scope.

Think about it. When you want to observe action on address or data buses, or on control lines, which instruments give you more meaningful data—a scope with four input channels or a logic state analyzer with 12, 16, or 32 channels?

You need a trigger that's related to program steps. Scopes by themselves simply don't have the capability of triggering on pattern

recognition. HP Logic State Analyzers do. Suppose you want to delay the data display to a specific point after the trigger word. The scope's analog time delay system has the inherent problem of display jitter. This is completely eliminated by the stable clock-pulse delay of a logic state analyzer. And when you're viewing data, would you rather mentally convert waveforms to digital words (1's and 0's) or have the instrument do the conversion for you?

Obviously, the scope is the logical choice for electrical measurements such as voltage level, rise time, and timing measurements. But when you're viewing state flow, there's no substitute for a logic state analyzer.

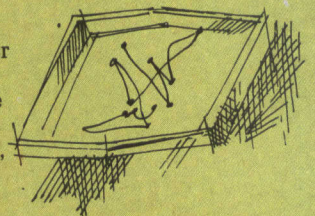
For example, one of HP's Logic State Analyzers can store one table of digital words and display it next to your active word display for

comparison. It can also display logic differences between stored and active data; continuously monitor data flow and automatically halt when the active data does not equal the stored data.

A new technique called mapping gives you an entirely new view of operating logic circuits—over 65,000 data words can be displayed as discrete dots, each representing one input word.

You can easily recognize these dot patterns after some familiarization, thus providing a rapid way to spot system irregularities. And for locating "lost programs," the map provides unequalled speed.

But these aren't just interesting measurement techniques, HP Logic State Analyzers provide more



a scope for digital design. making a mistake.



capability than any other digital troubleshooting instrument can deliver.

The Logic State Analyzer is the only economic alternative when it comes to digital system design.

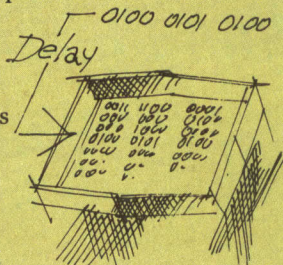
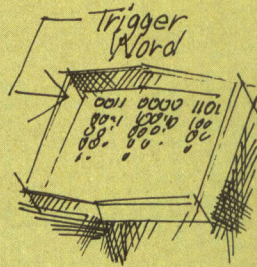
Your digital system operates in the data domain. You know all about time domain and frequency domain measurements, but how do you define data domain measurements? Basically they are measurements of logic state as a function of discrete intervals of time — clock cycles, for example. The emphasis is on word parameters. While the scope gives you an analog display of amplitude vs. time (time-domain dimensions), the logic state analyzer gives you a display of digital words vs. clock cycles.

But what are the other requirements of a data domain instrument? Obviously you need sufficient channels to see what's happening

on address and data buses. With today's systems, that means 16 channels or more. You need data registration — the ability to trigger on a specific bit pattern and the ability to position the display window as a function of clock cycles (pattern recognition triggering and digital delay). Because you often encounter events that occur only once in a program, you need a method of internal storage. Obviously, you want the ability to look at bit patterns after the trigger point, but you also want to see what happens before that point... in other words, you want negative time display; and even the ability to look on both sides of the trigger word at

the same time. It's essential that you be able to qualify both the trigger point and the display so you won't trigger on, or display, unwanted data. You'll still need to observe time-domain waveforms on your scope for detailed electrical measurements such as rise times, logic levels, and for locating glitch-generating race conditions. Your data domain instrument should therefore be able to drive a time-domain instrument — providing a trigger upon pattern recognition. Finally, you want data displayed in a functional format (a display of states) to simplify analysis.

From the previous comparison with a scope, you can see that these are the requirements we've used at HP in developing our family of Logic State Analyzers. Obviously, some members of the family have more capability than others, and prices vary accordingly. But the point is, all have been designed specifically to help speed digital design and debugging by giving you a better view of your system's operation. A view in the data domain... where your program flow is happening.

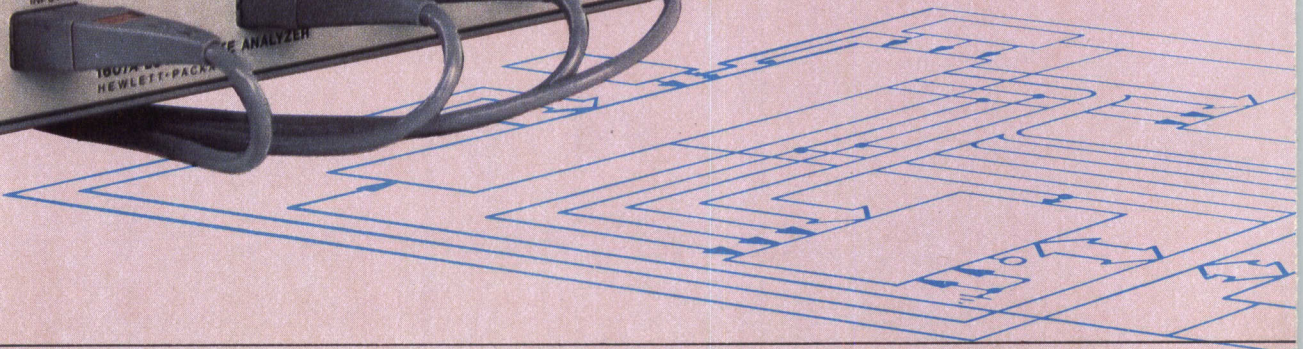
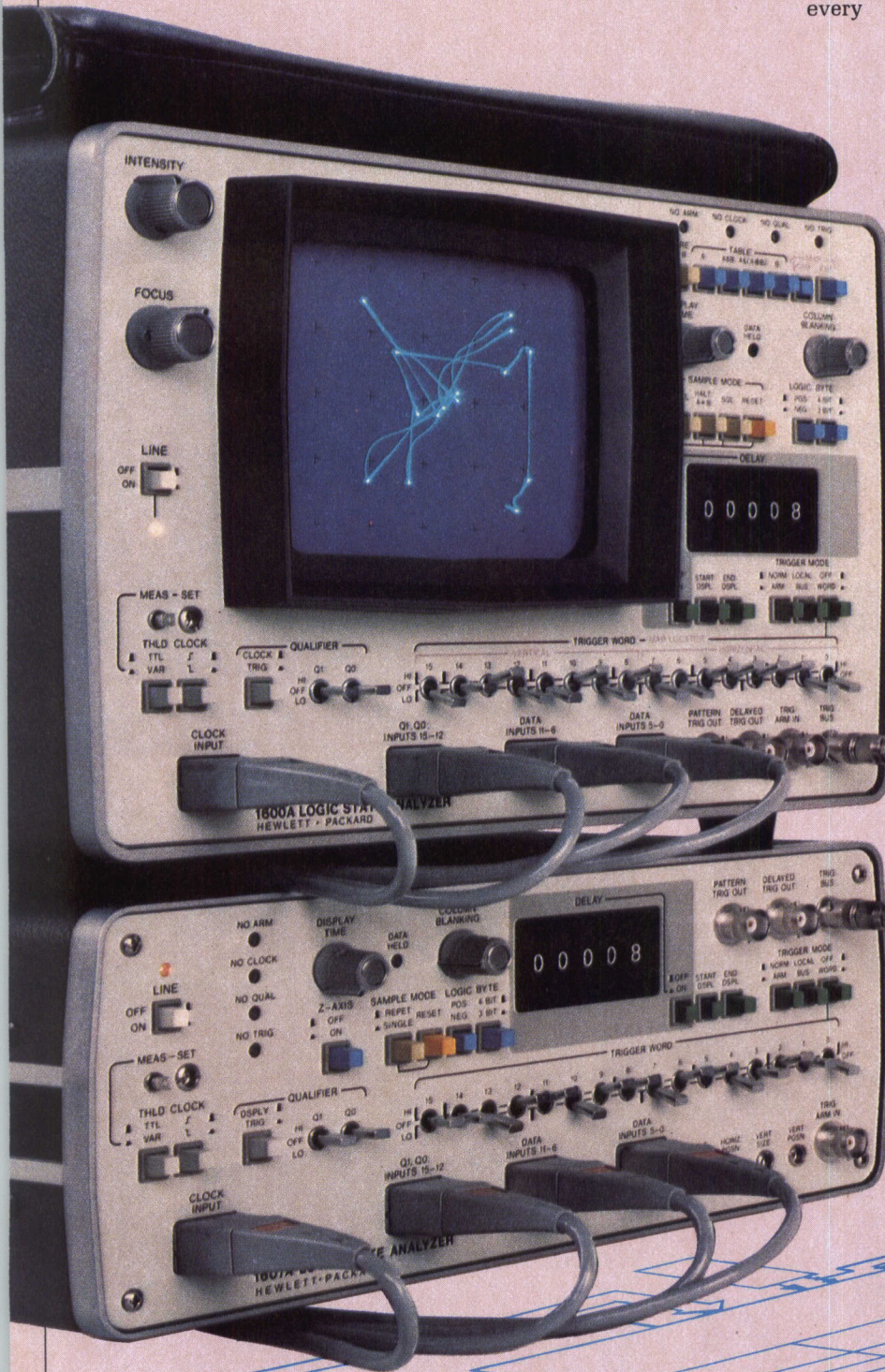
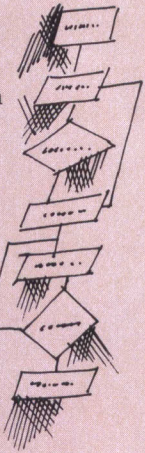


HP's Logic State Analyzers

Software debugging. It's great if you write a program that works right the first time it's implemented in hardware. But you know that it doesn't happen every

time. And when you get into program debugging, it's usually a time consuming task. How can an HP Logic State Analyzer help? By putting a window right on the data and address buses and giving you a real-time view of your program in operation... so you can see the exact word flow while it's happening. What's more, HP Logic State Analyzers let you move the window around at will by triggering on any word you want, or delaying the display a specific number of words beyond the trigger word.

This lets you compare the actual addresses and data on the buses with the program instructions you entered. It becomes much easier to spot an erroneous data word, an erroneous jump in the program, or an unending loop. With the mapping capability of the HP Model 1600A Logic State Analyzer, it's a simple matter to compare an executing program pattern to a known good pattern, or spot unique points in the pattern that indicate problems in an executing program. The 1600A also gives you the ability to locate any word on the map and trigger on that word so you can pinpoint a potential error source quickly. Then you can zero in by



Pioneers in the data domain are convinced.

Our customers have been using HP Logic State Analyzers since 1973. And we've talked to quite a number of users to find out what designers need in data-domain instrumentation. We've also found out how these data-domain pioneers feel about the HP Logic State Analyzers.

Here's a sampling:

"With the 1600A analyzer, I can do in an hour what I couldn't do in 3 months otherwise, and that's a fact."

"I designed a buffer interface that allows us to make real time tests using a slower tester. With my \$20,000 interface, the \$100,000 tester and your \$4,000 logic analyzer, we can do the job of a \$400,000 real time tester."

Don Glancy,
Principal Engineer

"We encountered some severe software problems on a real time 4K system where we were at a loss as to how to approach the problem. Because it was a real time system we were unable to stop it to use the standard software debug techniques. By coincidence your salesman called on the same day to demonstrate the 1601 Logic Analyzer. We hooked the analyzer to the system under test and wound up solving the problem that same afternoon. We were so thoroughly convinced of the potential power of the 1601 as it applied to software debug that we ended up buying two of them."

"Even though we had limited experience with microprocessor design, there's no question the logic analyzer saved us valuable design time."

Ken Fiske,
Senior Design Engineer



"When a parity error does occur, our equipment re-reads the data block fifteen times. In order to initiate that search routine, many sequential logic events must occur. Problems occasionally arise in that logic flow and it's been very difficult to analyze using just a scope. The logic analyzer allows us to troubleshoot logic flow in parity error problems about twenty times faster than the scope does. In addition to being faster, it's also easier to interpret the 1's and 0's than it is to interpret waveforms."

Don Stewart
*Coordinator of
Service Planning*

You've just read actual testimonials from users who have achieved significant time savings with an HP Logic State Analyzer — savings ranging from a factor of 20 to well over 400 compared to other methods, (Don Glancy's comment, "I can do in an hour what I couldn't do in three months otherwise.") And equipment savings of a factor of 3 or more.

If you or your people spend significant numbers of hours in the development of bus-structured systems such as computers and microprocessor-based systems, consider what those time savings could mean to you:

speed digital design.

using the table display (1's and 0's), and digital delay to examine the program sequence in detail.

Watching your software in action ... it gives you a big edge in problem solving.

Hardware/software marriage.

In digital design, you often discover incompatibilities between hardware and software — particularly when separate design teams have responsibility for these two aspects of the system.

It's not uncommon for the software to command the hardware to look for a signal (such as a request for interrupt) that apparently never occurs. Failure to get the signal may be a timing problem — the signal may occur too early or too late. The signal may exist at the right time, but at the wrong place — on the wrong data line for example. Or perhaps the signal was omitted altogether in hardware implementation. With microprocessors, the

problem may be due to lack of understanding of CPU peculiarities.

Whatever the case, you could spend an inordinate amount of time looking for the answer with the channel and triggering limitations of time-domain instrumentation.

However, with an HP Logic State Analyzer, you can tie into both the address and data buses at the same time, plus flag or qualifiers (up to 32 channels can be displayed on one screen). You can then run a short test program, trigger on a specific word at the beginning of the program, and view the program implementation leading up to the problem.

With this detailed picture of software in action, it's a simple matter to observe the displayed program sequence and see what's happening to that signal at a specific point in time. Then it's usually easy to spot the problem and apply a software or hardware solution — whichever is more appropriate.

System interaction. Additional problems frequently show up when you start transferring information across an I/O port. And your troubleshooting problems are compounded because you have two sources of data to monitor at the same time. They may have independent clocks ... be asynchronous ... but require a common trigger signal.

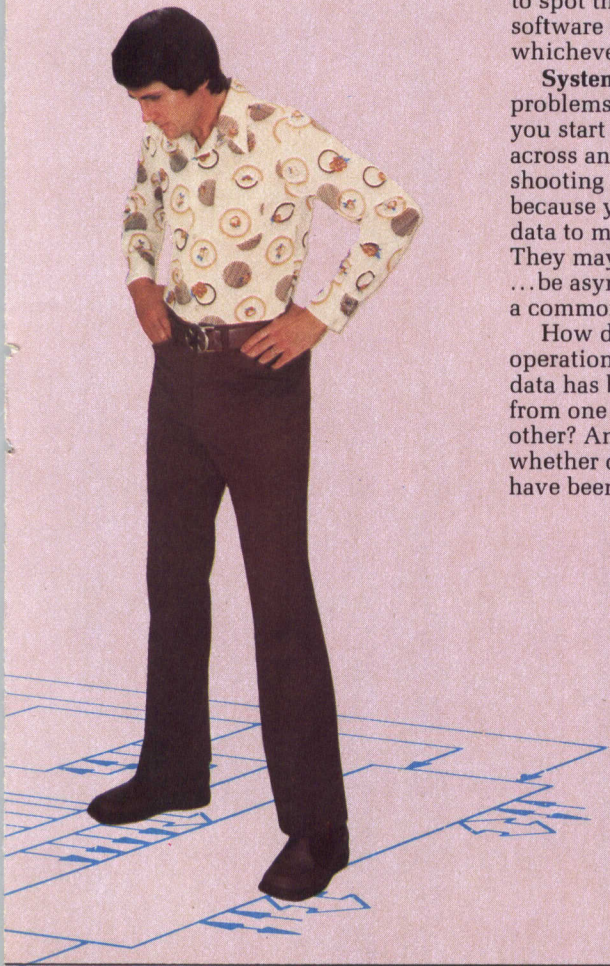
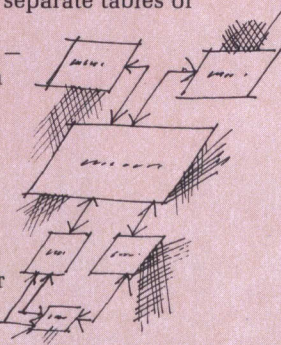
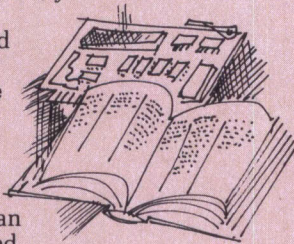
How do you verify overall system operation? How do you find out if data has been properly transferred from one part of the system to the other? And how do you determine whether or not the instructions have been executed properly?

Suppose, for example, you've designed a microcomputer-controlled test system for production. How do you know that the software is giving proper instructions to the instruments under test? Or that the instruments are inputting data correctly to the microcomputer? Unless you can verify the states in your program flow and look at digital inputs and outputs during the test cycle, your test could be meaningless. But with your microcomputer operating at one clock rate and the monitoring instrumentation at some other rate, how do you observe both and relate microcomputer software to hardware output.

The answer is HP's 1600S Logic State Analyzer. It lets you display two separate tables of data on the same screen — even though clock rates are different or one system is asynchronous. One table can display your microcomputer software

sequence while the other displays the hardware output and input resulting from that software. With program flow displayed alongside the input and output states of the instruments being controlled, there's no doubt about a correct testing sequence ... or about the information being fed back to the microcomputer. Furthermore, if there is a fault, you have adequate information to diagnose problems for correction.

In all of these phases of digital design — from the time you input software right through system checkout — an HP Logic State Analyzer can give you a clear view of program flow and hardware logic states to simplify design and debugging.



Convince yourself.

Over and over again, the reports from the field say: time saving... greater productivity... reduced development time... products into production faster. Whether you're a digital designer or an engineering manager, this message is important to you.

As a circuit designer, you know the importance of sticking to development schedules and budgets. And that always means

solving the problems the fastest way you know how. Take a look and see what kind of savings you might realize with an HP Logic State Analyzer.

If you're an engineering manager, concerned with the productivity of your engineering department, consider how much further your engineering budget could go if your people had HP Logic State Analyzers.

(A) — Estimated man hours spent in evaluating and debugging hardware and software using conventional techniques.

÷ — Your estimated time-saving factor — using a logic state analyzer — based on these testimonials.

= (B) — Estimated time spent in evaluating and debugging hardware and software with a logic state analyzer.

(A)÷(B) = — Potential time savings during the project.

× — Your hourly rate including overhead.

= — Potential direct cost savings.

Make your own analysis of what the time savings can mean in terms of getting products into production faster. The figures you come up with might easily exceed the cost of one of our Logic State Analyzers.

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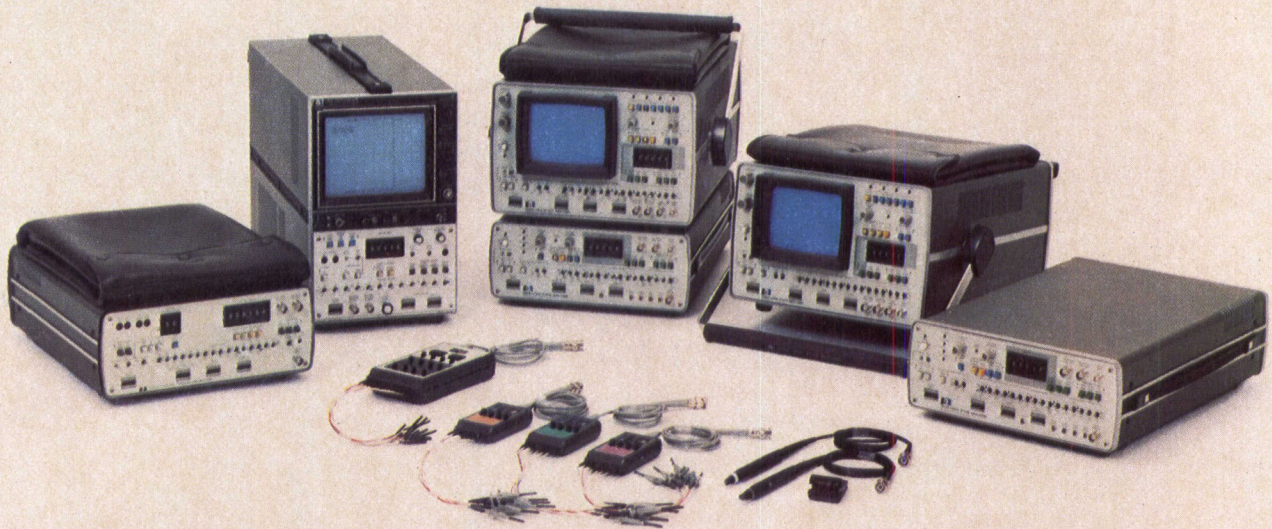
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Your choice in data domain instrumentation is growing steadily. It extends from simple 4-bit AND gate trigger probes, to an optional Logic State Switch on HP scopes for selecting either time or data domain, to the 1600S—the system with up to 32 channels plus qualifier inputs, storage, delay, and two modes of display (table or map). There's an instrument or accessory in this family to put you in the data domain and give you a much better view of your digital designs.

We've just scratched the surface.

There's a lot more to know about the data domain and about HP's family of instruments. And there are several sources for more information.

Seminars. HP instructors are now conducting one-day seminars on logic state analyzers and their application, and will continue in 1976.

Technical Data Sheets. These publications give you details of operation and instrument specifications on each of the family members.

Application Notes. A number of notes cover the use of mapping, using logic state analyzers to troubleshoot mini computer systems, microprocessor systems, etc.

For more technical data, simply mail the attached reply card, indicating the data sheets you want. Or, for even faster action, contact your local HP field engineer and ask him for more details about the instruments or seminars. Give him a call today and join the data domain revolution.

086/4

I'd like more technical information about HP's family of data-domain instruments. Please send data sheets on:

- Logic State Analyzers
- Pattern Trigger Accessories
- Clips and Probes

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Developments continue to improve performance, cost, and reliability of computer hardware. Technology for CPUs, main and file memories, and input/output continues its rapid evolution. Forthcoming technology will likely have its greatest impact on small computer systems for dedicated and real-time applications

Trends in Computer Hardware Technology

David A. Hodges

Department of Electrical Engineering and Computer Sciences
University of California
Berkeley, California

Changing computer system architecture and the increasingly broad scope of computer applications result from developments in hardware technology that have occurred during the past 15 years. A three orders of magnitude increase in the maximum feasible number of components in a single silicon integrated circuit chip has led to proportionate decreases in the cost per gate of computer central processing unit hardware and in the cost per bit of main and secondary data and program storage. Simultaneously, reliability of central processor and memory hardware has increased by about three orders of magnitude on a per-gate or per-bit basis. However, while central processor and memory hardware have benefited greatly from advances in solid-state technology, computer input/output and communications hardware have improved at a much slower rate. Growing efforts are now focusing on application of new technology and system concepts to overcome the limitations of existing input/output and communications hardware.

Further major improvements in cost and reliability of computer hardware are possible through evolutionary enhancement of established technologies. However, improvement rates may differ widely in different application areas. Revolutionary advances, where they appear, may have an even greater impact. Expected technological advances for large and small computer systems have important implications. In fact, small, dedicated computer systems may well provide a growing percentage of society's computing capability.

Central Processing Unit

Maximum feasible number of gates per single-chip integrated circuit (IC) has increased dramatically since 1960 (Fig. 1), and improvement at the same rate is likely to continue until 1980. During the past 15 years, the price of maximum-complexity ICs has remained roughly constant, while complexity has increased by three orders of magnitude, with still further increases likely beyond 1980. Even if only evolutionary development of present IC fabrication processes is assumed, at least 100,000 gates/chip may ultimately be achieved. Potential memory densities are an order of magnitude greater.

A variety of circuit technologies are in use or are proposed for use in central processing units (CPUs) built with large-scale integrated (LSI) circuit technology—circuits having more than 100 gates. Each of these alternative technologies^{1,2} is already well advanced (Table 1); much has been written about each.

The three highest density approaches are favored for LSI applications. Complementary metal-oxide semiconductor/silicon-on-sapphire (CMOS/SOS) devices are significantly more costly to manufacture than n-channel MOS (NMOS) or integrated injection logic (IIL). The latter two are directly competitive in all but a few specialized applications, and will likely coexist over the next decade. Speed and density of each will be improved by reducing their minimum dimensions and otherwise improving the fabrication processes. Both can

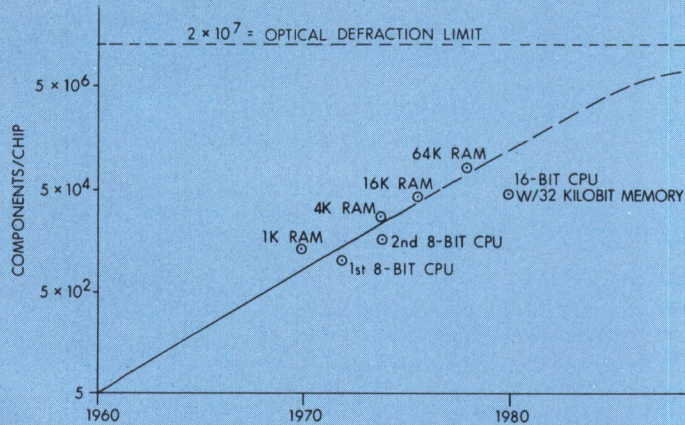


Fig. 1 Maximum components per chip. The number of circuit elements (eg, transistors, resistors, diodes) per IC chip has been increasing exponentially. The optical diffraction limit assumes 0.1-mil minimum features over a 2-in. diameter wafer; such resolution has been demonstrated in the laboratory. Still smaller dimensions can be formed using emerging electron beam and X-ray lithographic techniques

TABLE 1
Comparison of LSI Logic Families

Family	Density Gates/mm ²	Power-Delay Product, pJ			Smallest Delay, ns
		15 V	5 V	1 V	
ECL bipolar	30 to 40	—	5	—	0.5
Schottky bipolar	30 to 40	—	5	—	2
CMOS	30 to 40	50	5	—	10
NMOS	80 to 120	50	5	—	20
CMOS/SOS	80 to 120	25	3	—	3
IIL bipolar	100 to 200	—	5	1	10

Design rules: Approximately 7- μ m metal lines and spaces

profit, for instance, from selective oxidation techniques. Propagation delays of 1 ns or less appear ultimately possible with each. Emitter-coupled logic (ECL) and Schottky transistor-transistor logic (TTL) may eventually provide slightly shorter delays, but at a large cost because of lower density and higher power dissipation.

Anticipated increases in LSI circuit density will not benefit all applications areas equally. Concerning performance, further reductions in minimum logic delay are likely to be relatively slight. While delays of a few tenths of a nanosecond have already been achieved, and appear to be near the fundamental limitations of silicon technology,³ these high speeds cannot be

fully exploited in LSI circuits because heat removal is difficult. High speed circuits in silicon technology are likely to have a minimum power-delay product on the order of 1 pJ, meaning that gates with 1-ns propagation delay will dissipate 1 mW. Since, at most, about 3 W can be dissipated into a stream of air from an IC package, a maximum of about 3000 gates could be incorporated in one such high speed circuit. (Attempting to dissipate more than 3 W in one package would cost more and yield lower reliability than a multi-package approach.) This level of complexity would be adequate for a 16-bit CPU capable of executing at least 10 million instructions per second (MIPS)—approximately three times the state-of-the-art in 1975

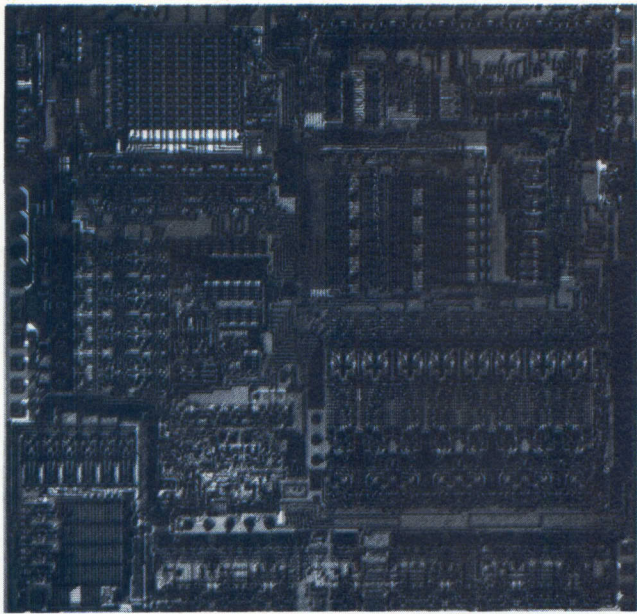


Fig. 2 8-bit microprocessor. This Schottky TTL, bipolar LSI microprocessor, fabricated commercially on a 250 x 250-mil die, is capable of executing 3 million instructions per second in control applications (Courtesy Scientific Micro Systems Inc)

(Fig. 2). A large computer exploiting high speed LSI has been reported recently.⁴

Pin Limitations

Another severe limitation on high speed LSI circuit complexity is off-chip connection density, as represented by LSI package pin count. This count, like the gates per chip, has increased since 1960 (Fig. 3), but at a much lower rate, so that the maximum feasible pin count has increased by less than one order of magnitude during this period. The state-of-the-art today is about 64 pins (Fig. 4). No breakthroughs are in sight on this problem. Consequently, full parallelism in memory addressing and data paths and uncoded control paths (desirable for highest speed CPU operation) are not feasible in LSI microprocessors. Multiplexed data and memory address paths and highly encoded control information must be used to reduce interconnection count. These reduce operating speed.

Power dissipation and interconnection count problems are much less troublesome with moderate to low speed circuits designed for low cost per function. Gates designed for delays of 10 ns and more achieve lower power-delay products than high speed gates. Power-delay products for such gates may well decline to 0.1 pJ. This means that 10-ns gates would dissipate 10 μ W, permitting more than 100,000 gates on a chip from the power dissipation standpoint. Multiplexed data paths and encoded control information are acceptable in moderate speed applications. By the early 1980s, it is possible to visualize the existence of a complete minicomputer system chip, including a 16-bit CPU, 32 kilobits of read-only and/or read/write memory, and simple input/output (I/O) interfaces. Speed, as limited

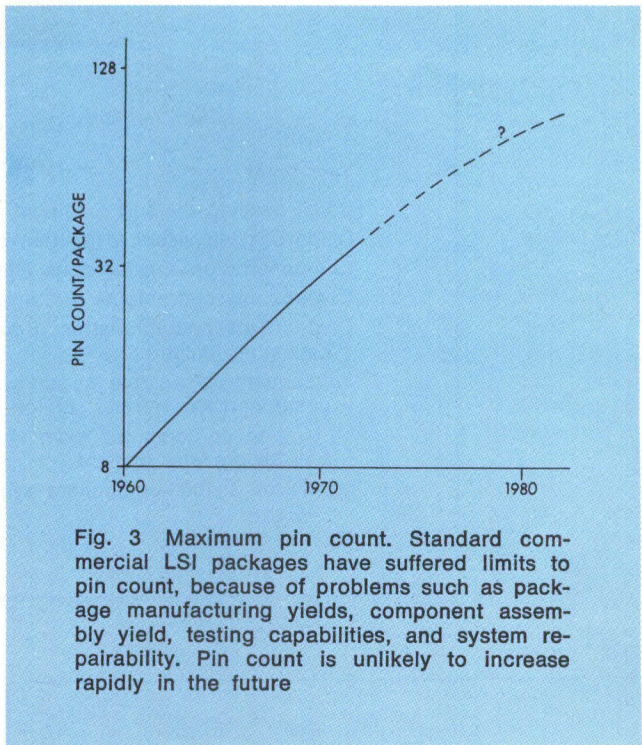


Fig. 3 Maximum pin count. Standard commercial LSI packages have suffered limits to pin count, because of problems such as package manufacturing yields, component assembly yield, testing capabilities, and system repairability. Pin count is unlikely to increase rapidly in the future

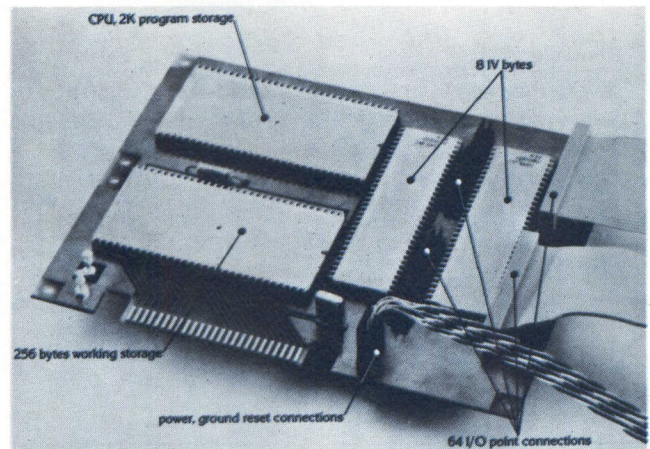


Fig. 4 Microcomputer system packaging. This is an advanced commercial LSI device. Power dissipation and repairability problems may limit further advances (Courtesy Scientific Micro Systems Inc)

by power consumption and serialized I/O, might be in the range of 100,000 to 1 million instructions/s; manufacturing cost should be \$10 or less.

Primary motivation for increasing LSI circuit complexity continues to be lower cost per function and improved reliability. Chip-count continues to be the best first-order measure for electronic hardware cost and reliability. Any LSI circuit which can be manufactured in volume will cost less than \$10 at the factory. After the design and process have been debugged, reliability will be determined by interconnections and packaging. Mean time between failures (MTBF) of about 10 million hours per packaged chip is easily obtained by simple means; 100 million hours is achiev-

TABLE 2
LSI Component Reliability

Test Point	Number
Chips passing die-sort electrical test	100
Chips passing visual inspection of lead bonds	98
Components passing all tests after packaging	80
Components operable at first system test	78
Components operable after 18-hr burn at maximum temperature	76
Subsequent failure rate of surviving components in normal service	
Lab or computer room	0.001 to 0.01%/1000 hr
Severe environment	0.010 to 0.10%/1000 hr
MTBF for a 1000-component system	10^3 to 10^5 hr

TABLE 3
Possible Trends in Dynamic MOS RAM
(With 500-ns Cycle Time)

Characteristic	1K	4K	16K	64K
Storage capacity	1K	4K	16K	64K
Date introduced	1972	1974	1976	1979?
Cell area, mil ²	6	2	1	0.5
Chip area, in. ²	0.02	0.03	0.04	0.06
Power/bit, μ W				
Active	300	100	20	4
MTBF/bit, hr	10^{10}	—	—	$>10^{11}$?
Component manufacturing cost/bit (Note 1)	0.3¢	0.1¢	0.03¢	0.01¢
Memory system price/bit (Note 2)	1.2¢	0.4¢	0.12¢	0.04¢

Note 1: Two years after introduction
Note 2: To OEM market

able with special care.⁵ Table 2 summarizes the testing and screening strategy needed to achieve these levels of LSI component reliability.

Memory

Semiconductor main memory costs have declined rapidly over the past decade, primarily because of the increasing density of LSI memory chips. Further large increases in memory density are expected (Table 3), with 64-kilobit chips feasible before 1980;⁶ 16-kilobit random-access, read/write memory (RAM) chips (see Fig. 5) will be announced in 1976.⁷ Read-only memory

(ROM) chips will probably have about twice the density of read/write chips. Price per bit of read/write memory systems should fall well below 0.1¢/bit before 1980. These numbers apply to moderate performance systems; high speed cache memories having cycle times of about 50 ns are likely to cost two to five times as much per bit, and to dissipate substantially more power.

Characteristics of moving-surface memories (drums and discs) have improved drastically over the past two decades,⁸ but further improvements in large-capacity moving-surface storage devices are probable (Table 4). Costs of fast-access storage should fall to one millicent per bit or lower by 1980.

New devices such as the floppy disc provide file storage at moderate system price—about \$2000 for a system storing 2 megabits/surface, or 0.1¢/bit at present. As much as an order of magnitude reduction in the price of floppy disc systems seems feasible if high volume usage develops. The main problem with these and other low cost electromechanical systems will probably be reliability. If maintenance costs for floppy discs are high, users will choose all-electronic storage devices, even if first cost is somewhat higher (Fig. 6).

Charge-coupled device (CCD) memories⁹ and magnetic domain (bubble) memories¹⁰ are being widely discussed as potential successors to one or more of today's storage technologies. To achieve wide acceptance, the price per bit of a new storage technology must be significantly lower than alternatives. Special characteristics such as nonvolatility or ease of application may be decisive factors in specialized applications, but will not overcome cost as the key consideration in most cases.

Comparable cost data on RAM, CCD, and bubble memories are not yet available. However, a crude comparison may be drawn, based on fundamental factors limiting the cell density of each technology and on the relative complexity of the fabrication process for each. In such a comparison (Fig. 7), where a number of simplifications have been made for clarity, assume

that pattern definition techniques allow a certain minimum feature size (Δ). Then the minimum area required for each cell using each technology can be estimated as shown in the figure. Actual cells are two to five times larger than the areas indicated here, because of alignment tolerances, crossovers, and other factors. A newer form of bubble cell¹¹ requires about half the area indicated here. (Even more refined comparisons, when data are available, should not mask the fundamental distinction that most semiconductor memories are random-access devices, whereas CCD and bubble memories are serial. They should properly be compared with long semiconductor shift registers.)

The conclusion emerging from this crude comparison is that RAM and CCD have comparable maximum densities, while the CCD fabrication process is slightly more complex. Bubble cells require two to four times the area, but the number of precision pattern definition steps is two to four times fewer. Overall, it is hard to construct an argument that CCD or bubble memories will be significantly cheaper than RAM in the long run. In fact, RAM may always have a cost advantage simply because its development is already well advanced.

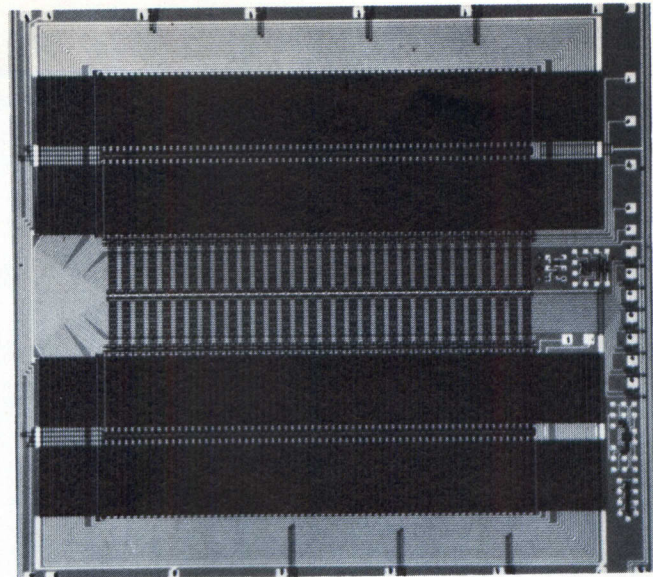


Fig. 5 Photomicrograph of a 16-kilobit, n-silicon gate exploratory RAM. 128 single-transistor cells, each occupying a 1-mil² area, share one sense-refresh amplifier. Using external clocks, the chip can be operated at a cycle time of about 1 μ s (Courtesy Siemens AG)

TABLE 4
Disc File Storage Density

Year	Linear Density (bits/in.)	Track Density (traces/in.)	Storage Density (bits/in. ²)
1960	200	40	8000
1965	2200	100	220,000
1970	4000	200	800,000
.			
.			
.			
1985	160,000	2000	320 x 10 ⁶

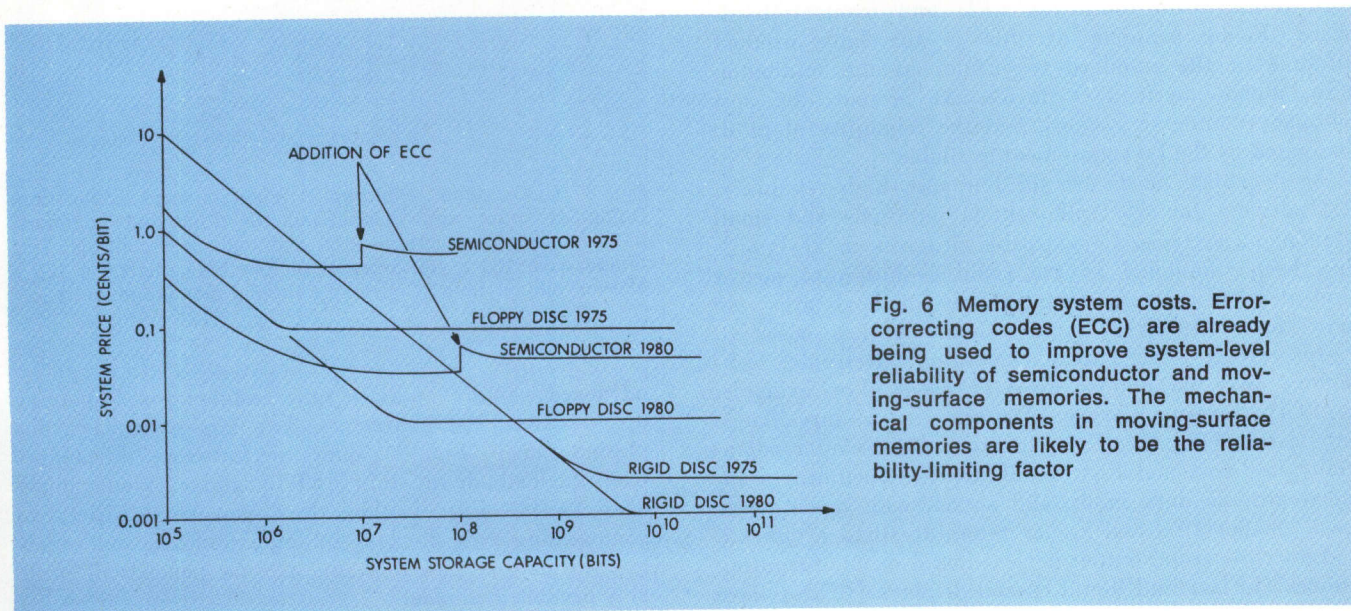
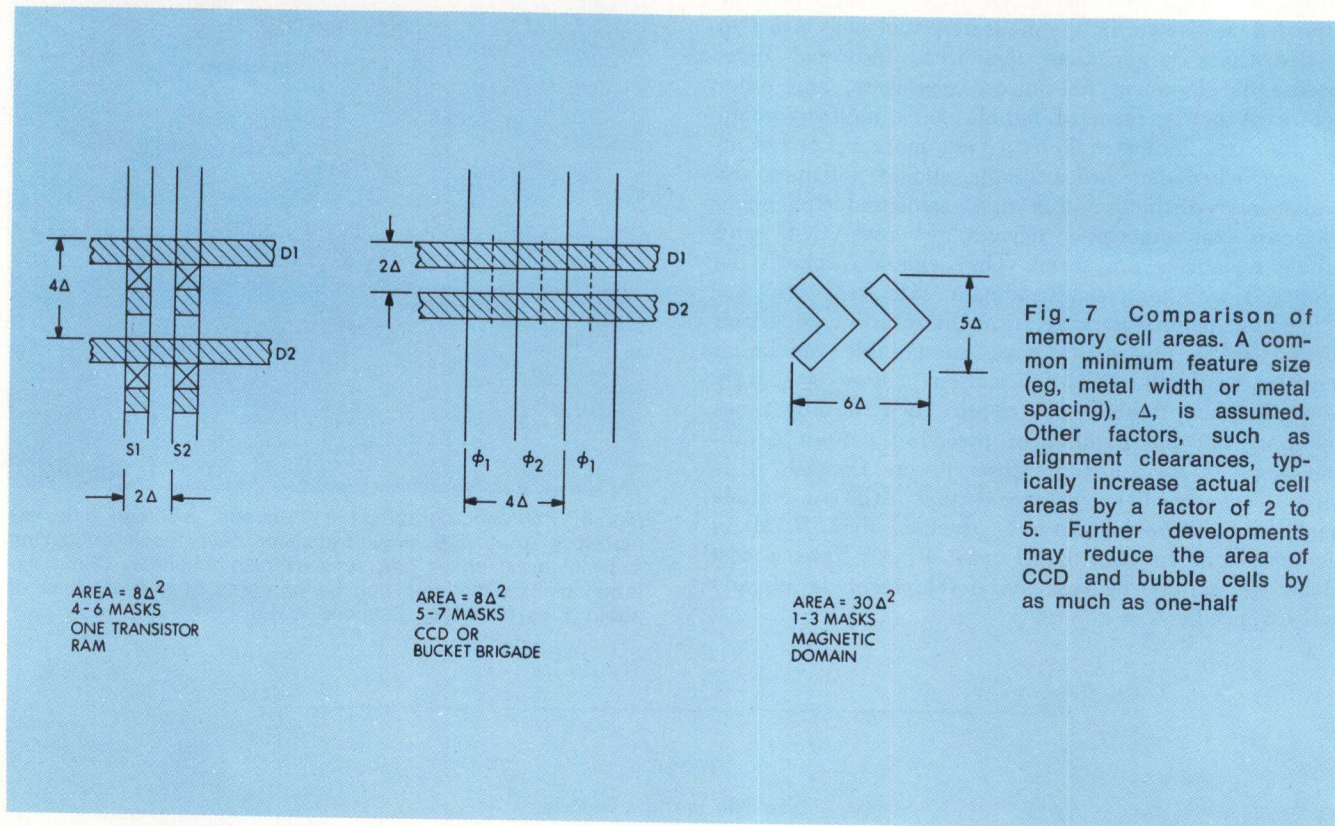


Fig. 6 Memory system costs. Error-correcting codes (ECC) are already being used to improve system-level reliability of semiconductor and moving-surface memories. The mechanical components in moving-surface memories are likely to be the reliability-limiting factor



Factors which might modify this conclusion include developments such as multilevel CCDs, capable of storing two or three bits per cell, and the so-called "bubble lattice," in which the storage array does not require defined patterns for each bit.

Input/Output

Improvements in cost, performance, and reliability of computer I/O equipment have taken place at a far slower rate than those for CPU and memory hardware. Prime example of this is the long product lifetime of the standard teleprinter as the minimum-cost, alphanumeric I/O device. At present, the cost of many computer systems, and the reliability of most, is limited by the I/O equipment available.

Most critical needs are for low cost, high reliability, I/O devices for use with remote terminals and small standalone systems. Considerable progress in keyboards has been stimulated by the rapid evolution of pocket and desk calculators; many types of keyboards are now manufactured in large volumes at low costs.

In several other areas, emerging electronic technology may be applied to I/O needs. For example, a CCD imaging device is useful in a surveillance application (Fig. 8). These imaging devices offer potentially low cost and high reliability for document scanners, graphic data input, and so on, with much lower cost, smaller size, and higher reliability than a vidicon.

Low cost, visual output devices based on light-emitting diodes (LEDs) and liquid crystal displays (LCDs) have

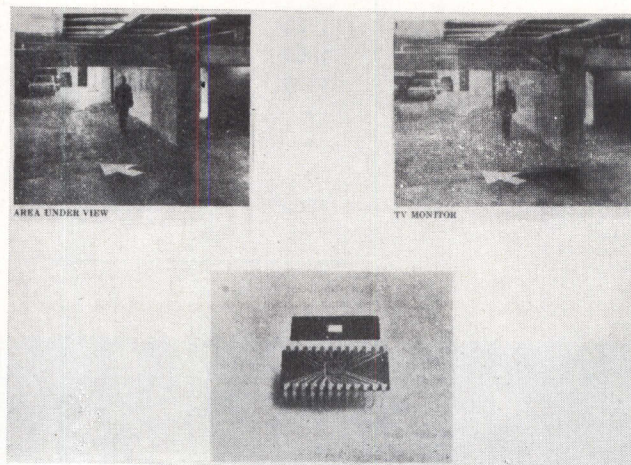


Fig. 8 CCD imager. Pictured is a surveillance application. Computer input applications include document scanners, pattern recognition processors, and industrial controls. This imager is a 100×100 array of picture elements on a 120×180 -mil silicon chip (Courtesy Fairchild Semiconductor)

advanced rapidly and are now suitable for displaying up to about 100 characters. For larger displays, the plasma panel (Fig. 9) offers performance advantages over the cathode-ray tube (CRT) and cost advantages over LEDs. With further development, a variety of compact low cost displays for alphanumeric and graphic information, based on the plasma panel, will probably become available.

For hardcopy output, thermal printers based on silicon technology are already available. A single-character printhead (Fig. 10) is potentially manufacturable in quantity for a \$1 to \$2 cost. In present applications,

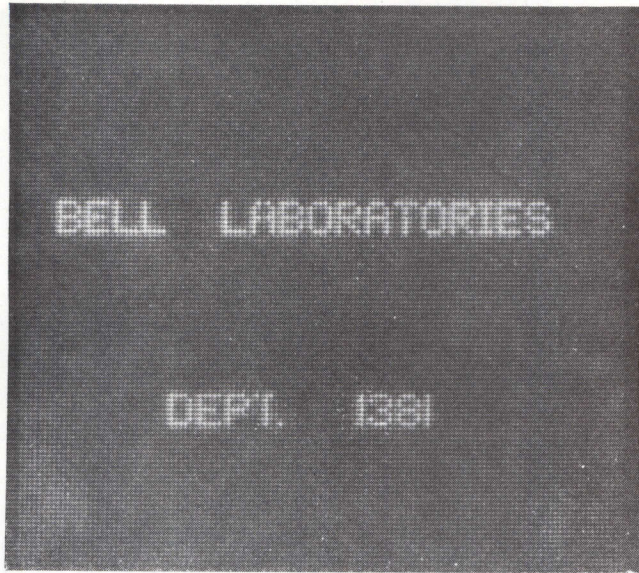


Fig. 9 Plasma panel display device. Features include high resolution, high legibility, freedom from geometric distortion, and the flat device structure. Present drawbacks include high cost and relatively high complexity of the necessary driver circuits (Courtesy Bell Laboratories)

such a device moves horizontally across a sheet of sensitized paper, while the paper moves upward, driven by a typewriter-like roller. A low cost line printer could be built with 80 thermal printheads in a horizontal line, thus easily printing the content of one standard punched card per line. This would eliminate the relatively slow and troublesome mechanical scan across each line.

Efforts in I/O technology are sorely needed for control-oriented applications as well as the data processing applications suggested already. Now that computing capability is available for as little as \$20 in the form of a microprocessor, computer applications in automobiles, point-of-sale terminals, toys, and many other areas become economically feasible. Sensors and actuators (transducers) are a limiting factor at present, although extensive efforts are underway to reduce the cost of electronic transducers for all common physical variables. For example, silicon technology is being applied to transducers for temperature, pressure, flow rate, and acceleration, while other solid-state technologies are being examined for uses such as automobile exhaust gas sensors. Objectives in each case are low cost and high reliability.

Communications

It can no longer be assumed that the cost per unit time of a CPU is far greater than the cost per unit time of a local telephone connection. For many years, this assumption has been the basis for developmental

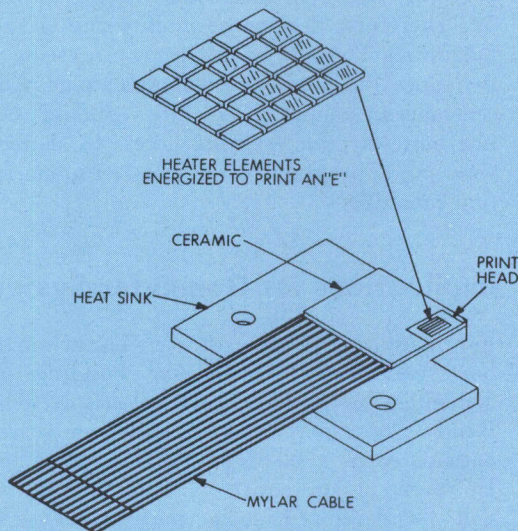


Fig. 10 Thermal printhead. This silicon integrated circuit is now used in several computer terminals with hardcopy output. The printhead is an array of individually heated elements. Some costs and mechanical limitations associated with common impact printers are overcome with this approach (Courtesy Texas Instruments)

TABLE 5
Data Transmission vs
Local Processing and Storage

Item	Purchase Price	Rental Price/Hr
Local voice-grade switched telephone line	—	\$0.60 to 1.20
Microcomputer	\$500	\$0.50
10 ⁶ -bit RAM	\$2500	
Floppy disc system	\$2000	

Note: Assume 200 hr/mo; 50-mo amortization of rental equipment

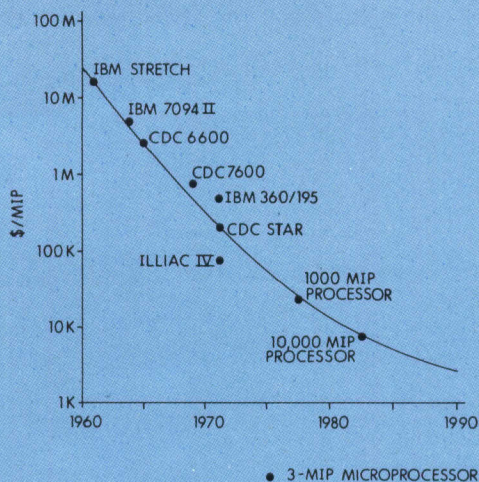


Fig. 11 System cost per MIPS. Until recently, cost per instruction executed was best reduced by building larger, faster, shared general-purpose systems. Recent developments in microcomputer technology seem to be changing this pattern in selected application areas, though not in the area of computer center EDP applications (Chart taken from Ref. 12)

efforts on time-sharing and other multi-terminal computer systems. As pointed out previously, advances in hardware technology have reduced the cost of CPU and memory per unit capability by three orders of magnitude. Meanwhile, over the same period of time, the actual cost of providing a local telephone connection has risen, based as it is on the costs of cable, rights of way, labor for installation and maintenance, and interest on investment. Furthermore, political and consumer interests are forcing a trend toward usage-sensitive billing. As a result of this, local calls, which for years have cost a fixed charge for unlimited duration, may soon be charged for on a time basis.

At these rates, communication is likely to cost more per unit time than local computing and storage (Table 5). Therefore, designs of multi-terminal systems should maximize internal information processing and storage to reduce the need for communications. Links to large, centralized computing facilities should be used only intermittently, for essential access to shared data bases, very large programs, and massive numerical computation capability.

Implications for Computer Systems

For many years, the cost per instruction executed has been continually reduced by building larger, faster computers (Fig. 11). This pattern is evident from a Rand Corp report¹² issued only two years ago, which anticipated a 1000-MIPS CPU by this year or next. However, at present it is unlikely that such a CPU will be developed soon, partly because fundamental limitations on the speed of silicon logic circuits have already been approached.

Another obvious approach to higher speed computers is through parallelism, as exemplified by the ILLIAC IV.¹³ Unfortunately, parallel architectures are most efficient

TABLE 6
Comparison of Microcomputer System
Execution of Control-Oriented Benchmark Programs

Microcomputer System	Total Benchmark Execution Time
SMS-300	39 μ s
Intel 8080	195 μ s
DEC PDP-8/A	246 μ s
National IMP-8	873 μ s
DEC MPS (Intel 8008)	3560 μ s

Source: Scientific Micro Systems

when used on specialized problems such as matrix arithmetic. Another troublesome drawback is that a highly parallel computer would require a complete redesign of existing systems and applications software.

These considerations make revolutionary changes unlikely in the design of large general-application computer system hardware. Instead, computers of conventional architectures will be gradually improved. For commercial reasons, new machines are virtually assured to be software compatible with previous systems from the same manufacturer. Meanwhile, the potential cost-effectiveness of a 1000- or 10,000-MIPS processor, or of a higher speed processor based on non-silicon technology (at least 10 years away), is not at all clear at this time.

Drastic decline in computer hardware costs, especially those for moderate speed operation, improves the economics of small, dedicated and special-purpose computer systems. One dramatic example is the 3-MIPS microcomputer (Fig. 2). With a basic system price of \$600 in 1975 (\$200 per MIPS), this unit would fall a factor of 100 below the curve in Fig. 11. Of course, such a microcomputer has a very limited instruction set and memory capacity, and includes no I/O devices. Nevertheless, if it can do the job in a dedicated application, such a microcomputer is likely to be a far more attractive solution than a large remote, time-shared computer system would be, especially in real-time control applications.

Furthermore, the speed of a dedicated processor is not always a limitation, if system performance is related to the characteristics of I/O hardware and/or storage devices. As pointed out previously, another important motivation for maximizing the amount of local computation is the high and growing cost of communications relative to other computer system costs.

Some dedicated processors are likely to be in use only a small fraction of the time, if they are associ-

ated, for example, with point-of-sale terminals, machine controls, or communication controllers. However, they are still likely to be more cost-effective than a larger, shared system that is kept busy most of the time.

Some patterns that appear to be developing in microcomputers deserve mention. First, performance already has a broad range (Table 6). Second, specialized designs have begun to appear; more are sure to be forthcoming. Applications for specialized processors include automobiles, appliances, games, point-of-sale terminals, and others. Third, upward compatibility of new designs is likely, as the Intel microprocessor families have already demonstrated. Finally, two nearly direct microprocessor replacements for existing mini-computers have been announced.

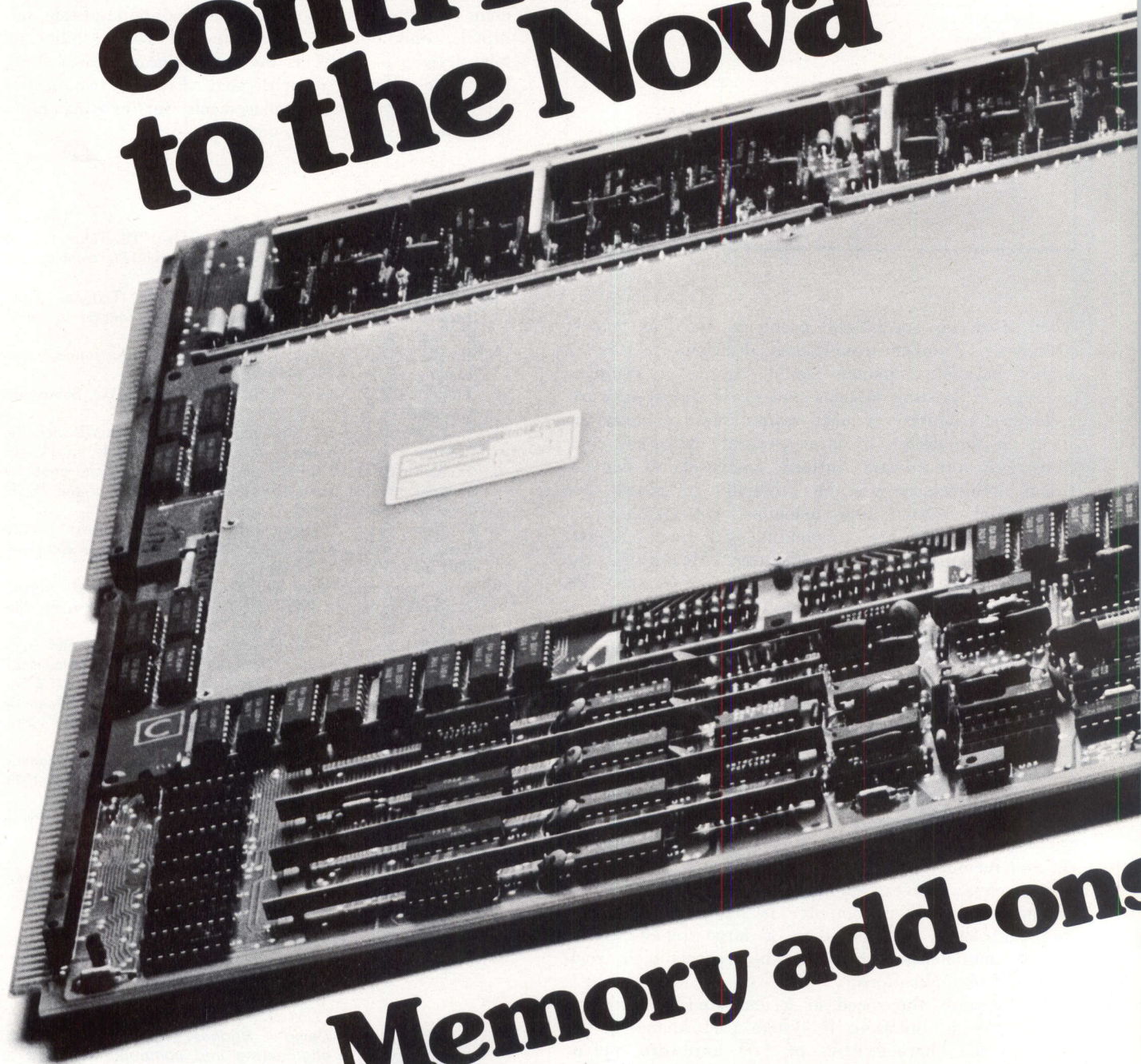
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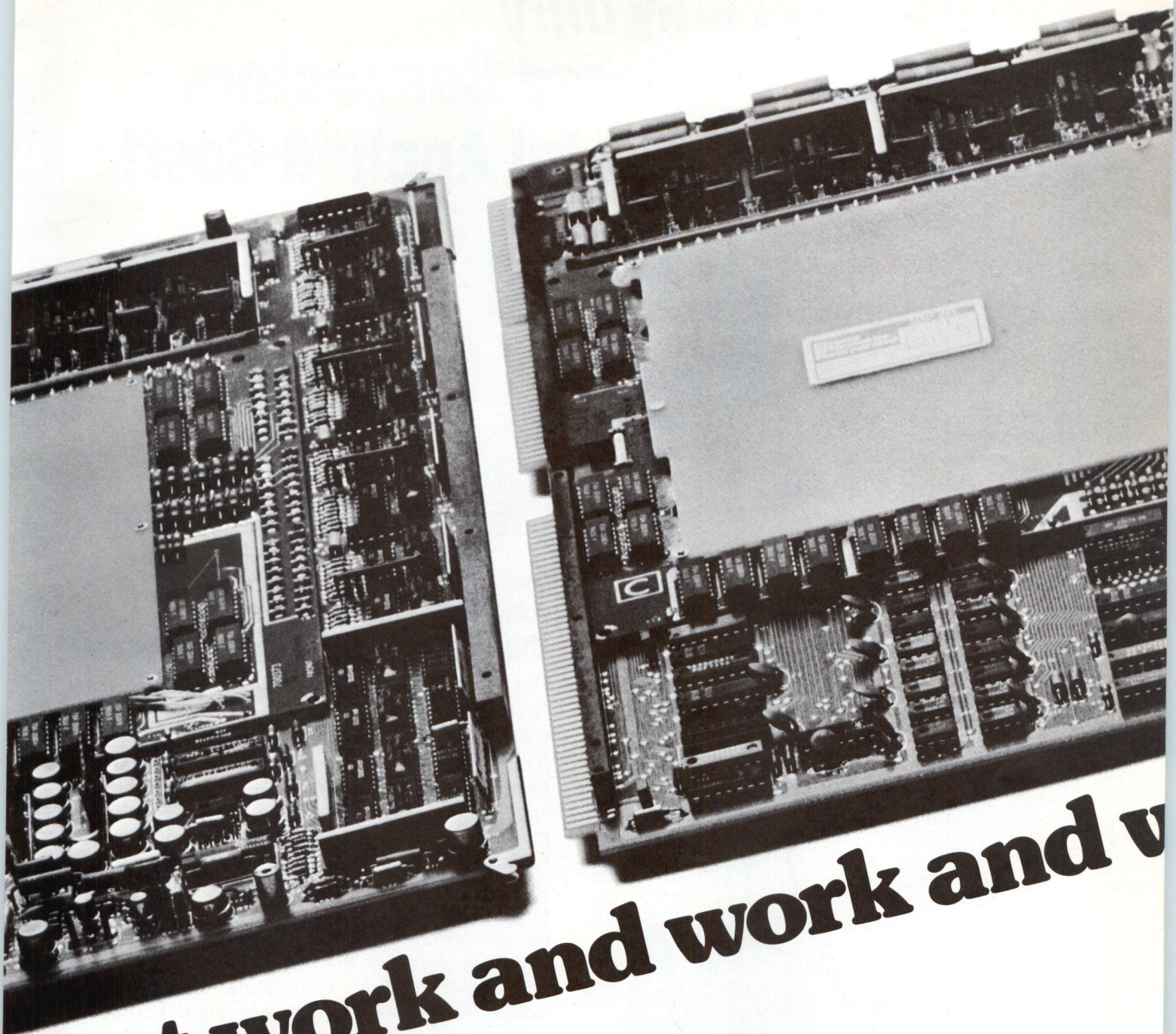


David A. Hodges, professor of electrical engineering and computer sciences at the University of California, Berkeley, has experience in component technology and in system research. He holds a BEE degree from Cornell University, and MS and PhD degrees in electrical engineering from the University of California, Berkeley.

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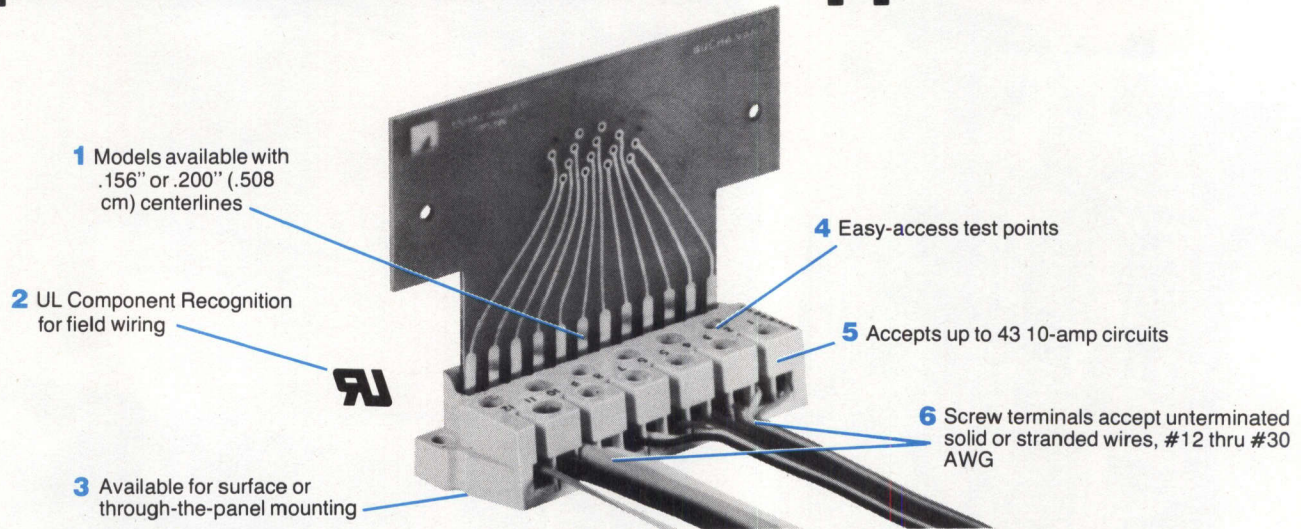
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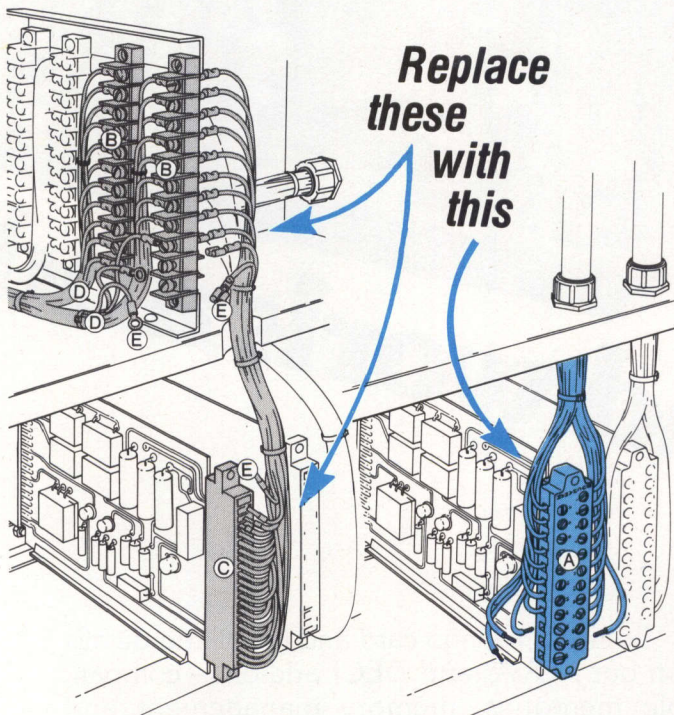


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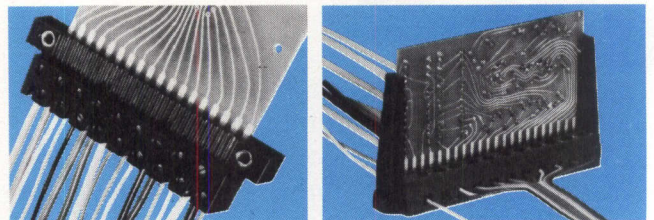
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Employing long channels for efficiency, plus numerous circuit design innovations, giant-size area scanners using bucket-brigade shift registers have been built and tested. They can also be used as memories in series-parallel-series mode, shifting in and out serially at high speed, and propagating internally in parallel at a much lower speed

Enormous Bucket-Brigade Optical Scanner Achieves High Efficiency

Barry J. Deliduka

International Business Machines Corporation
System Products Division
Essex Junction, Vermont

Charge transfer devices are being developed, not only for shift-register memory and analog delay line applications, but also for photosensors and memories. To provide further insight into the future of large photo-sensitive arrays, one recent effort is studying the feasibility of building very large area sensors. An area scanner chip, believed to be the world's largest solid-state image array, has been developed, using processes similar to those used in constructing computer memories,¹ and built around bucket-brigade shift registers.²

In any application of shift registers, transfer efficiency or transfer loss is the most important concern. Study and modeling of bucket-brigade structures have verified that when channel length is increased, transfer loss decreases. This improvement in transfer efficiency makes feasible shift registers as long as 512 bits, with uncompensated measured efficiencies of 99.95%/transfer. Even this high efficiency has been improved with a clock noise suppression amplifier on the chip, permitting an apparent efficiency of more than 100% under certain conditions.

The imaging array comprises 1024 of these long shift registers, and thus contains 524,288 photo elements (PELs) on one extremely large chip—approximately 2.54 by 4.06 cm—about the size of a standard razor blade. Several of these chips have been fabri-

cated using standard n-channel metal-oxide semiconductor field-effect-transistor (MOSFET) technology. When the devices are fully operational, their resolution exceeds that of conventional vidicon tubes used in TV cameras. They are fast enough to scan an 8½-by 11-in. page and reproduce the information on an oscilloscope screen in 4 ms.

The project was basically a feasibility study: Was it possible to construct an extremely large chip, the physical, electrical, and image-sensing performance of which could be evaluated, and for which the fabrication problems involved could be realistically estimated? With this overall viewpoint in mind, the design was chosen.

The bucket-brigade shift registers (BBSRs) consist of aluminum-gate FETs connected to form series circuits (Fig. 1). In each FET, the overlap between the gate and drain produces a larger capacitance than that between the gate and source of the device [Figs. 1 (a) and 1 (b)]. This difference in capacitances provides directionality for the flow of charge in the circuit. Alternate transistors are turned on and off by two clock pulses connected to their gates, so that information is propagated through the register.

The optical windows of the register are those portions of the silicon that are not covered by the metal

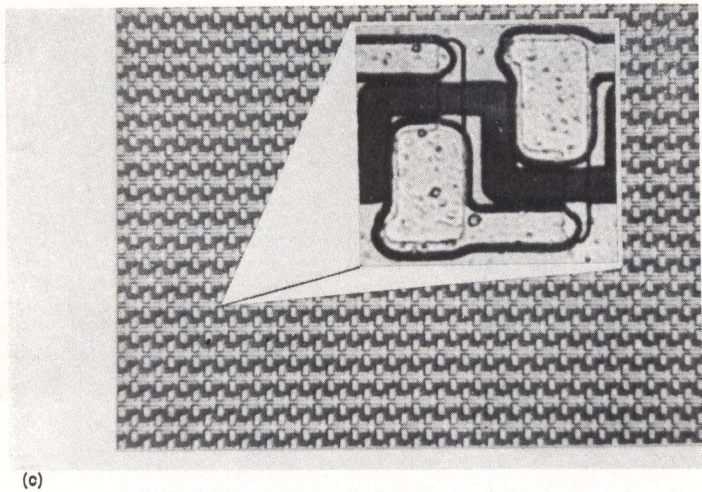
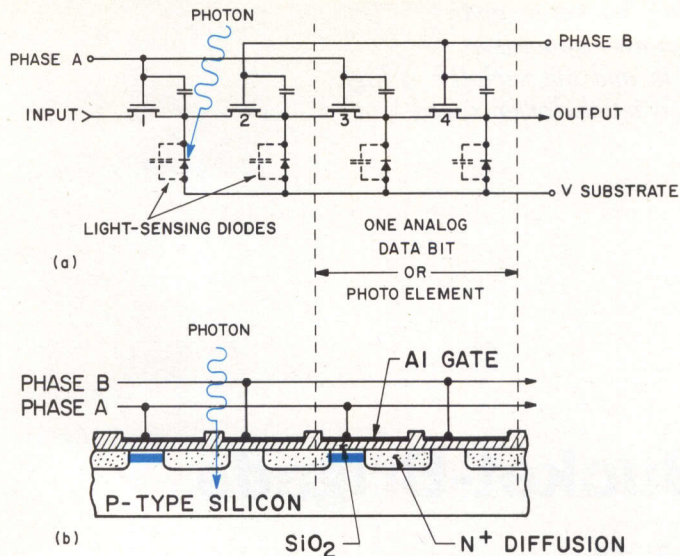


Fig. 1 Two-phase bucket-brigade shift register. Two FET devices are required for one analog data bit or photo element (PEL). Associated with each device is a photo diode and a large gate-to-drain capacitance, shown in schematic form in (a) and by the asymmetrical gate position shown in the cross-section (b). Source of one FET is connected to the drain of the next FET by a common diffusion, which produces the series circuit without contact holes. Channel conduction established between diffusions by clock phase A appears in color, as does incident light; during clock phase B, channel conduction occurs at alternate areas. The photo diodes are formed by the diffusion-to-substrate junction. Microphotograph (c) of a single PEL shows the serpentine layout, by which adjacent shift registers share metal phase lines that run parallel to the flow of data. This layout also preserves the unity aspect ratio

gate lines. Light energy enters the silicon through these windows and generates electron-hole pairs. The electrons collect in the diffused "buckets," which in turn change the voltage on the diffusion-to-substrate capacitor.

Two transistors form a single PEL. To preserve an aspect ratio of unity, the transistors were arranged in a serpentine fashion [Fig. 1(c)], so that PELs would be equally spaced, 0.0381 mm apart, in both the horizontal and vertical direction of the array.

Ordinarily, bucket-brigade devices require only three mask levels: diffusion, thin oxide, and metallization. In this case, however, one additional mask level is used between the thin oxide and metallization steps, to provide contact holes necessary for construction of the on-chip amplifier and output circuits. Nevertheless, the process is very simple, and is subject to few defects, thus providing potential yield improvement.

In the use of bucket-brigade or any other transfer device, the fraction of charge that is actually transferred from one FET to the next in the shift register—called transfer efficiency per stage—is a matter of

importance. If all of the charge is transferred, the transfer efficiency would be unity. In practice, however, this is not the case; a portion of the signal charge is always left behind during each transfer operation. Thus practical transfer efficiency is always less than unity, and its complement—transfer loss—is always greater than zero. One mechanism that affects transfer loss and dominates at low frequency is the modulation of threshold voltage by the drain voltage. This problem can be reduced by using a longer channel.^{3,4} In the half-million-PEL device, to minimize modulation, a channel of about 12 μm in length is used in the FETs that make up the array registers.

The phase lines that drive the array registers run parallel to the flow of data instead of in the conventional perpendicular fashion. This parallel phase line pattern provides a number of important advantages. For example, it enables the electrical subdivision of the array registers that make up the entire array. This, in turn, permits partial operation of the chip should any localized process defects occur that could cause short circuits. Also, if there is a break in a

phase line, the parallel pattern minimizes the number of shift registers affected. However, the probability of such breaks is small, because the parallel phase lines can be shared by two adjacent registers. Therefore, they can be wider for a given density of PELs per unit area, and wider lines are less subject to damage.

Basic Chip Organization

The chip is organized as an array of 512 by 1024 PELs. Its basic building block is a subsection of 16 shift registers each 512 bits long, and consisting of 1024 transistors. (Each register actually contains 1025 transistors, as a result of a miscalculation in drawing up the masks; however, the extra transistor, aside from adding one step to the propagation of data through the register, does not affect its operation.) Associated with the subsection are a 16-bit input shift register, 16-bit output shift register, transfer circuits connecting these to the long registers, and sense amplifier and output circuits following the output shift register (Fig. 2). Four subsections, consisting of 64 long shift registers, four sets of input/output (I/O) circuits, and 24 contact pads (12 at each end) make up a section (Fig. 3), which is the smallest portion of the array that can be probed for testing. The entire chip comprises 16 sections, electrically isolated from one another except for the sharing of phase lines between the 64th register of one section and the first register of the next.

The optical window of each PEL is formed by the gap between the phase lines. In this system, the circuit was arranged to provide uniform photo response across the array, permitting the use of a step-and-repeat process to make the different masks necessary for fabricating the large chip.

Attached at the end of each of the 64-output shift registers is a source-follower clock suppression network⁵ driving an output device (Fig. 4). The input

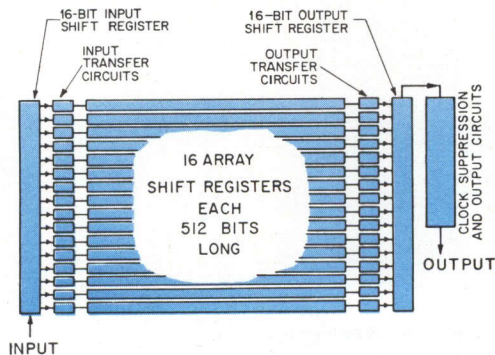


Fig. 2 Basic building block. Called a subsection, each block has its own input and output high speed registers, array registers, and output circuitry

Why Build Giant Chips?

From the system point of view, a huge array such as that described here by Barry Deliduka would permit better resolution than would smaller arrays, because individual elements of a given area would respond to a smaller fraction of a whole picture focused onto the array. IBM's array may well be the largest ever fabricated, but other, experimental devices of respectable size have been built elsewhere, and a few designs are in commercial production.

Fairchild Semiconductor, for example, makes several scanners of both linear and area formats. Its linear scanners, which come in lengths of up to 1728 elements, each 13 μm across—for a maximum total length of just under 1 in.—have a scan rate of 10 MHz, while area scanners of up to 244 x 190 elements are compatible with standard TV but can be operated more than 10 times as fast.

Other commercial scanners are made by General Electric and Reticon. GE uses charge-injection device (CID) technology; in its simplest form, CID senses the stored charge through the substrate instead of moving it from element to element, as CCD technology does. GE is now marketing a TV-compatible scanner, or imager, with a 244- x 188-element array, and is expected to introduce a larger unit (244 x 248) soon. These devices measure in the neighborhood of 10 x 12.5 mm.

Among large experimental scanners is one at Bell Laboratories on a 16- x 20-mm chip carrying 496 x 475 elements, and a 488- x 380-element array at Fairchild; elements on both devices measure about 18 x 30 μm , compared with IBM's 38 μm sq. However, a chip of the IBM size, according to a Bell researcher, seems too large to have a practical yield.

Utility of such large arrays, of course, depends on their speed—how quickly they can pick up an image and scan that image for transmission or other processing. Speed, in turn, depends on the technology with which the array is fabricated. The maximum rate at which IBM's array was tested was 3 MHz—respectable but still well below the standard TV channel width of 6 MHz and below Fairchild's linear scanning rate of 10 MHz.

Yield has always been a problem in large-scale integration, because of the vulnerability of large chips to small defects in the wafer or in a process mask. Yet yield is not necessarily an obstacle to the economical production of large solid-state scanners.

The author describes methods by which bad sections could be bypassed or recovered, thus substantially improving the yield of his laboratory process. Yet, as he points out, the best individual scanner had only 13 good sections, out of a possible 16. Nevertheless, these methods might be developed to apply to a production process—although doing so would be a task that could not be completed this year or next.

Even at a low percentage yield, the process might be economical. One semiconductor expert, whose company manufactures a processor chip of nearly 70,000 sq mils—one of the largest in commercial use today—observes that yield for such a device is not very important, because they are not used in large quantities. Yield is more important, for example, in semiconductor memories, he points out, because they are sold in very large quantities and require a high-yield process to obtain the necessary production rates.—Ed.

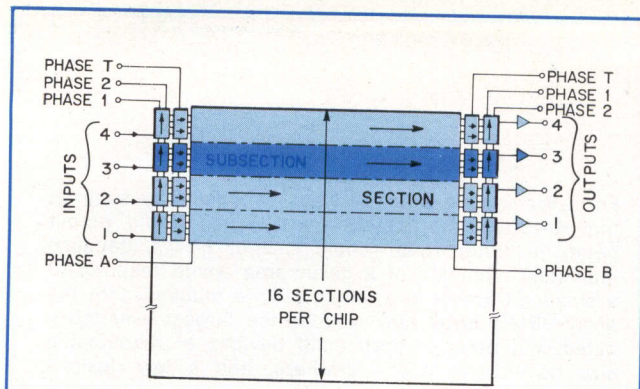


Fig. 3 Four subsections per section. Sections are electrically independent; 16 sections form the giant (512- x 1024-PEL) scanner chip. Arrows show direction of data flow

shift registers contain similar sense and output devices, providing a test print and permitting the input and output registers to be identical.

Memory

When the chip is used as a memory, it operates in a series-parallel-series mode, in which a line of data (16 bits) is read into the input shift register serially, and shifted in parallel into the first bit positions of the 16 array registers through the input transfer devices. All charge transfers between BBSRs are made in the bucket-brigade mode through the transfer devices. Then, another line of data is read into the input register, followed by another parallel transfer into the array registers. While the second line of data is being shifted in parallel into the array registers, the previous line is shifted from the first into the second bit

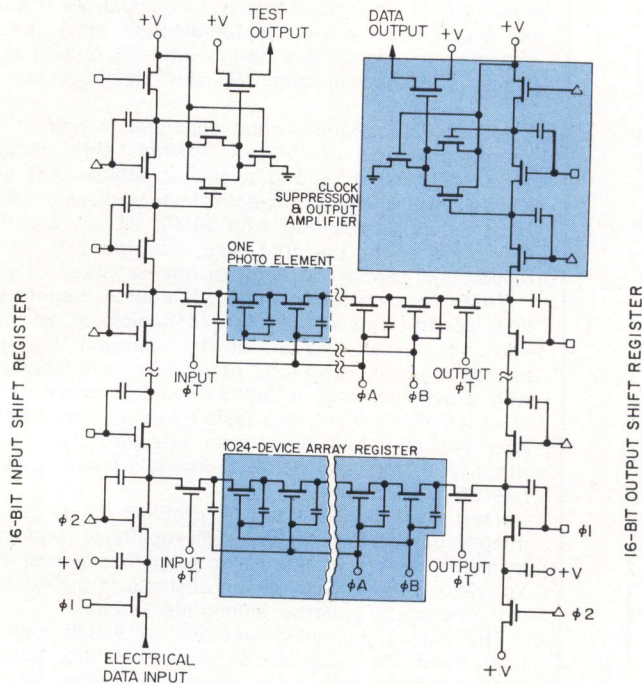


Fig. 4 Subsection. Input, array, and output shift register are included, as is the clock suppression output circuit. The array actually contains 1025 devices (see text); therefore, ϕB is connected to both the first and last in the series, instead of ϕA to the first and ϕB to the last, as would be the case if the number of devices were even

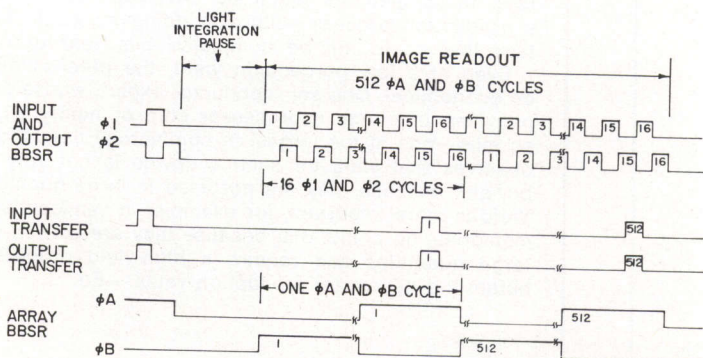


Fig. 5 Timing for both image sensing and memory testing. Input and output shift registers (2 MHz) operate 16 times as fast as the array registers and transfer gates (125 kHz)

positions. In this way, 512 lines are read into the main array. Then, with the next step, the first line of data is transferred to the output shift register and read out while a new line enters the input register.

The input and output registers cycle at a rate of 16 times that of the array registers. In this experimental chip, the rates are 2 MHz and 125 kHz, respectively. Of several possible timing schemes, for performance evaluation, a relatively unsophisticated one that was easy to work with was chosen (Fig. 5). The BBSR drive pulses are complementary and thus nominally 180 deg out of phase, except for the light integration pauses.

Evaluation of the Processed Chips

Each of the 16 sections of the processed chips was probed and evaluated in both dc and ac tests. Even

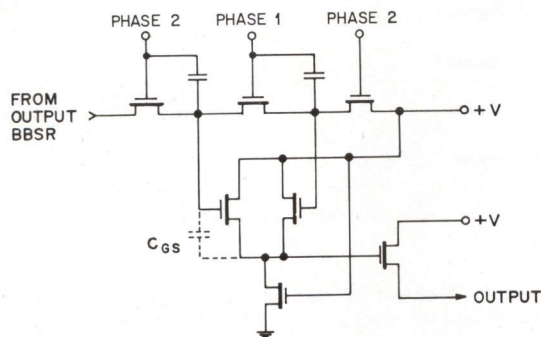


Fig. 6 Source-follower clock suppression sense amplifier. This circuit includes an output driver. Gate-to-source capacitance, which is responsible for transfer loss compensation at low frequencies, is shown with dashed lines

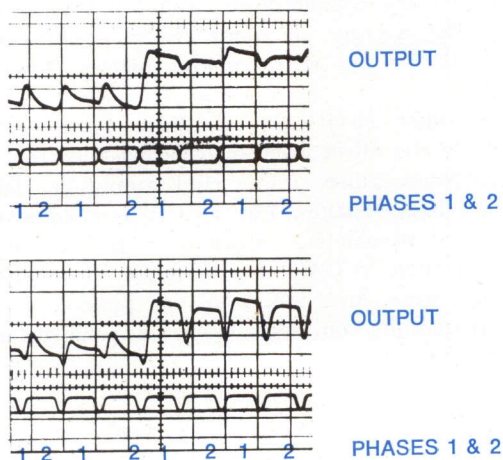


Fig. 7 Clock noise. Overlapped phase pulses at 2 MHz produce less noise on the output (top two traces) than non-overlapped pulses do (bottom traces)

though in no chips did all sections pass the testing criteria, several chips were found to have nine or more sections operational, and in these most of the sections were adjacent. One of these chips had a series of eight working sections, followed by a shorted section and four more working sections. With a laser beam, an aluminum short-circuit between two array phase lines was cut away in the shorted section, thus providing a total of 13 adjacent operational sections, or a working array of more than 425,000 PELs.

The output sense amplifier (Fig. 6) of each output shift register consists of a source-follower clock-suppression circuit driving a source-follower output device. The output signal (Fig. 7) contains a pair of data pulses for each bit stored in the BBSR. Phase 2 is connected to the gate of the first source follower via a capacitor. When phase 2 is positive, the first source follower turns on while the low gate voltage of the second source follower keeps this device turned off. At this time the sensed data are transferred to the output device through the first source follower. Then, when phase 1 is turned on and phase 2 is off, the data are transferred to the next node in the shift register, where they are again sensed by the second source follower. Thus the output device sees the signal first at a phase-2 node, then at a phase-1 node, providing a pair of data pulses for each bit sensed. If the bit is a 1, the signal is relatively high, with a small dip between the phase-2 and phase-1 portions; but if the bit is a 0, both phases produce a peak about one-third the 1 and 0 signal difference that decays exponentially.

The amount of clock noise appearing at the output depends on the extent to which the phase pulses overlap. Using only square-wave clock pulses, minimum clock noise was achieved with phase pulses having 20-ns rise and fall times overlapped at their 40 and 60% points, respectively. Under these conditions, clock noise was reduced to less than 10% of the voltage difference between a 0 and 1 signal level. However, the circuit does not eliminate the predominant resistance-capacitance time constant slope in a 0 signal.

Although the two pulses are theoretically of equal amplitude, they may be unequal, or unbalanced, as the result of unequal node capacitances. Also, because of transfer loss, the second sense node does not receive all of the charge contained on the first. Experiments have shown that the unequal amplitudes can be equalized by unbalancing the amplitudes of the two clock phases.

The clock suppression network also acts as a compensator⁶ for transfer loss. As with all FETs, the first source follower has a gate-to-source capacitance. When this device is cut off and the second source follower is on, the gate-side of the capacitance is held to the reference voltage on the sense node, while the source-side is maintained at a voltage only slightly different from the drain voltage of the second source follower. When phase 1 turns off, the charge on the capacitance is trapped; when phase 2 turns on, this trapped charge is altered by adding or removing some charge from the new signal that was shifted into the sense node of the first source follower.

When a step input is applied to the compensator (Fig. 8), it appears as a string of 1's following a string

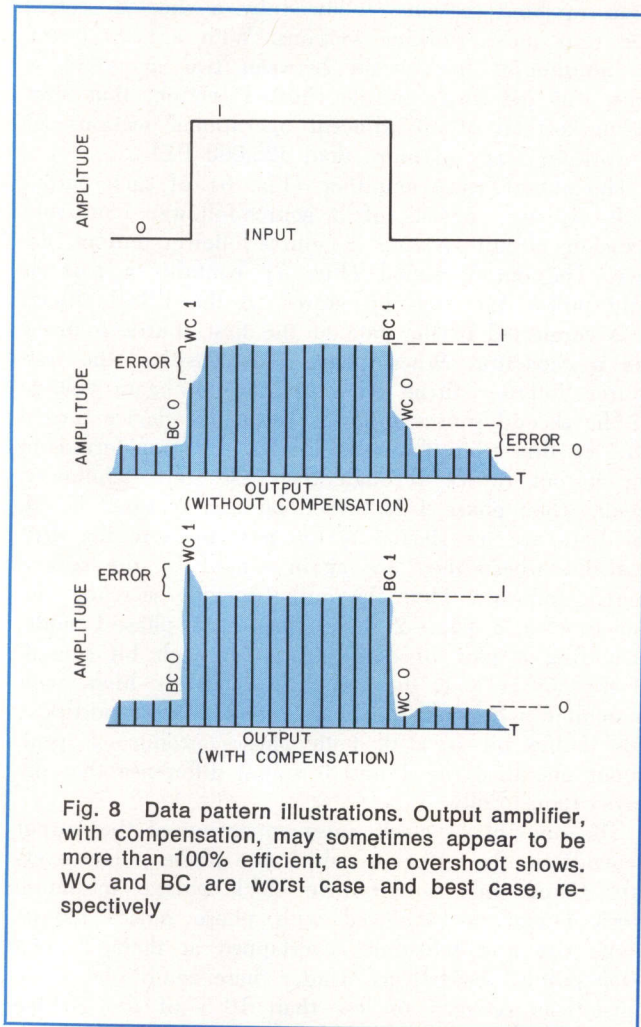


Fig. 8 Data pattern illustrations. Output amplifier, with compensation, may sometimes appear to be more than 100% efficient, as the overshoot shows. WC and BC are worst case and best case, respectively

of 0's. Normally, the first, or worst-case, 1 of such a string would have a lower amplitude than the last, or best-case, 1. However, the compensator boosts the amplitude of the worst-case 1; it also negatively enhances the amplitude of the worst-case 0, as the diagram shows for low frequency. (At higher frequencies, the compensation merely brings the worst-case amplitude closer to the best-case amplitude without exceeding it.)

This compensation capability introduces difficulties in measuring transfer efficiencies of the array and output registers. When the output shift register is operating at frequencies below 1.5 MHz, the amplitude of the worst-case 1 exceeds that of the best-case 1. Thus the calculated transfer efficiency appears to exceed unity, although, obviously, this is not possible. Therefore, to measure the true transfer efficiency of the output shift register, the gate connection to the second source follower was removed with a laser. Transfer efficiency was then found to lie between 0.996 and 0.998 per transfer [Fig. 9 (a)].

The transfer efficiency of the array shift registers [Fig. 9(b)] was measured with the clock suppression

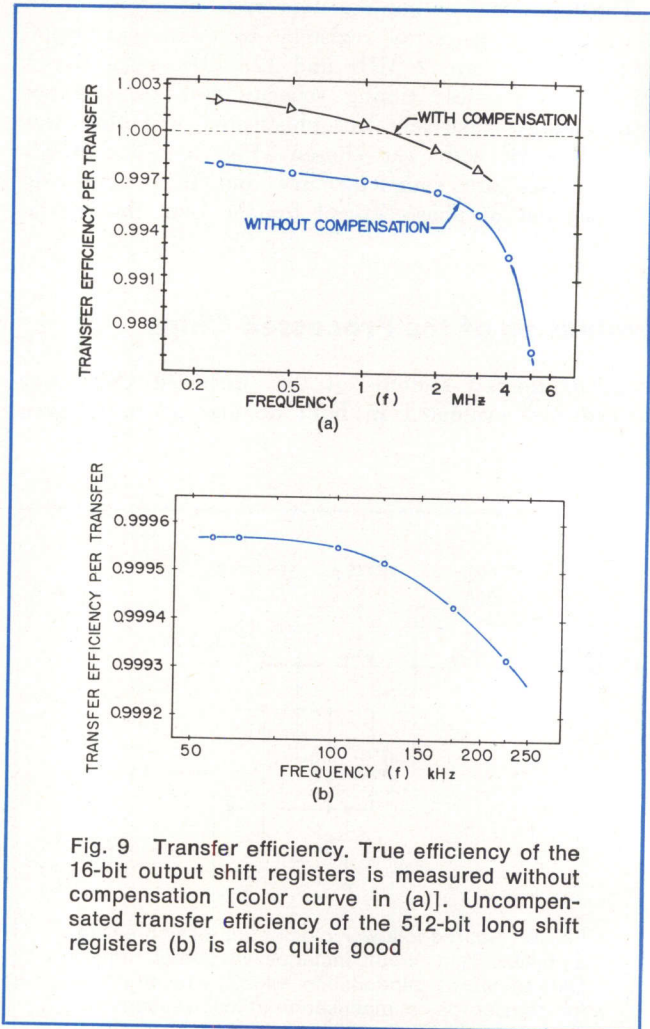


Fig. 9 Transfer efficiency. True efficiency of the 16-bit output shift registers is measured without compensation [color curve in (a)]. Uncompensated transfer efficiency of the 512-bit long shift registers (b) is also quite good

network intact, and with a data pattern of 1's and 0's, so that the compensation would not influence the results. The average of many different chips at 125 kHz was 0.9995 per shift (ranging between 0.9993 and 0.9996).

Many other electrical tests have been performed to evaluate the effect on transfer efficiency from variation in phase pulse timing and amplitude, temperature, and bias voltages. For a $\pm 10\%$ change allowed in any one parameter, variation in transfer loss has been less than $\pm 12\%$. Furthermore, from the time the chips were first tested to the present—a period of many months, no degradation in performance has been observed.

Imaging

There is a striking comparison between the area scanner and the human eye. Just as the discrete rods and cones found in the human eye convert light into electrical signals, so do the tiny sensors (PELs) which make up the scanner. Signals from the scanner can be trans-

mitted to a display system that reconstructs the picture.

When the chip is functioning as an image sensor, it operates in frame transfer mode, whereby an image is projected and focused onto the array. Light entering the silicon through the spaces between the metal phase lines generates electron-hole pairs; the electrons accumulate in the diffusion "buckets" and change the potential on the diffusion-to-substrate capacitances of each bucket by an amount proportional to the num-

Image-sensing evaluation of the chip was largely devoted to a demonstration of its performance (Fig. 10). The bench setup used to evaluate the chip electrically was also used for the optical evaluation, along with a display incorporating very simple signal processing. An image obtained from an object illuminated with a 12-V, 60-W tungsten lamp was projected onto an image splitter incorporated in the microscope and focused onto the surface of the chip. Only one section of the array (64 x 512 PELs) could be used at a time,



Fig. 10 Results. Author displays sketch that was illuminated and focused on a section of the 1- x 1.6-in. area scanner chip (left). The chip produced the picture on the oscilloscope (right)

ber of photons of the incident light. This corresponds to both the brightness of the light and the length of time for which it shines. Therefore, as long as the accumulated charge does not overflow (saturate) the individual buckets, the charge pattern will correspond to the image focused onto the chip. After a period of time has elapsed, to allow sufficient light integration, the phase lines are turned on and the array is rapidly read out in the same manner as in the memory application described earlier. While data are being read out, the charge on the capacitors is being reinitialized in order to be ready for the next frame of optical data. After the entire array is read out, the phase lines are turned off and the next frame of optical data begins to accumulate in the buckets.

Since the stopping of phase lines during light integration is used in place of an optical or mechanical shutter, the image is incident on the array while the frame is being read out, and introduces additional, unwanted charge, or noise, that distorts the properly gathered data. To reduce this distortion, total readout time—in relation to integration time—should be very short.

limited by the probe station and optics. Consequently, only four output analog signals from the four subsections were multiplexed and digitized by a single-level comparator, which controlled the blanking pulse of a standard laboratory oscilloscope. This approach reversed the image, displaying the light areas as black and the black areas as white. External logic generated the x-y raster on the scope to match this aspect of the array segment.

The array registers were operated at between 100 and 187.5 kHz (output data rate of 1.6 to 3 MHz) with no significant change on the displayed image. Integration time was varied from less than 2 to more than 16 ms, while the light intensity was decreased accordingly. Again, no degradation showed up in the final display. Sensitivity of the array registers was measured, with the infrared light filtered out. An energy density of approximately $0.23 \mu\text{J}/\text{cm}^2$ was required to produce a 1-V change at the output circuit.

A number of different images were used, including white letters on a black background, black letters on a white background, and photographs of faces; in the last, the faces were recognizable on the black/

white display. The most impressive demonstration was a typewritten message which moved across the segment at 3 in./s and could be read on the display with no smearing of letters.

Several types of defects were observed and identified from visual and electrical tests, such as missing or bridged patterns, shorts between metallization patterns, and shorts to substrate. Also, a variety of black and white bar and point defects were observed on the display. The black defects were caused by dark current sources and areas extremely sensitive to light; the white defects were traced to a blockage in the shift register or transfer circuits caused by missing or distorted patterns and possible pinholes⁷ in the oxide. Blooming, which is caused by charge spreading through the register from an intense spot of light, was present and produced black bands across the display. By either reducing the light intensity or decreasing light integration time, blooming was eliminated from the normal field of view of the optics without any loss of information; but even when blooming was present, it was not severe, because the analog data signal, having been digitized into either a black or white level, tended to reduce the extent of the bloom.

Other, more satisfactory displays are possible, either by filtering the analog signal or by digitizing it into various levels of gray. The important point to remember when analyzing the results is that the display's resolution and performance should not be assumed to be those of the imaging device itself.

Numerous other modes of memory and image operation are possible, since the chip is divided into 16 electrically independent and addressable sections, each with serial input registers. These would make the device useful as a buffer, with information entering through the serial input of one section while other information is read out of another section.

Conclusion

Solid-state sensors of many sizes, with high or low resolution, will probe their way into existing and future markets. Whatever the application—research to manufacturing, monitoring to measuring—or as an input reading device for a computer system (Fig. 11), they can function in areas where the human eye cannot, such as in hostile environments or very small places. Solid-state image sensing is a fast-growing technology that should be looked at with new, vigorous ideas to assure its development and growth.

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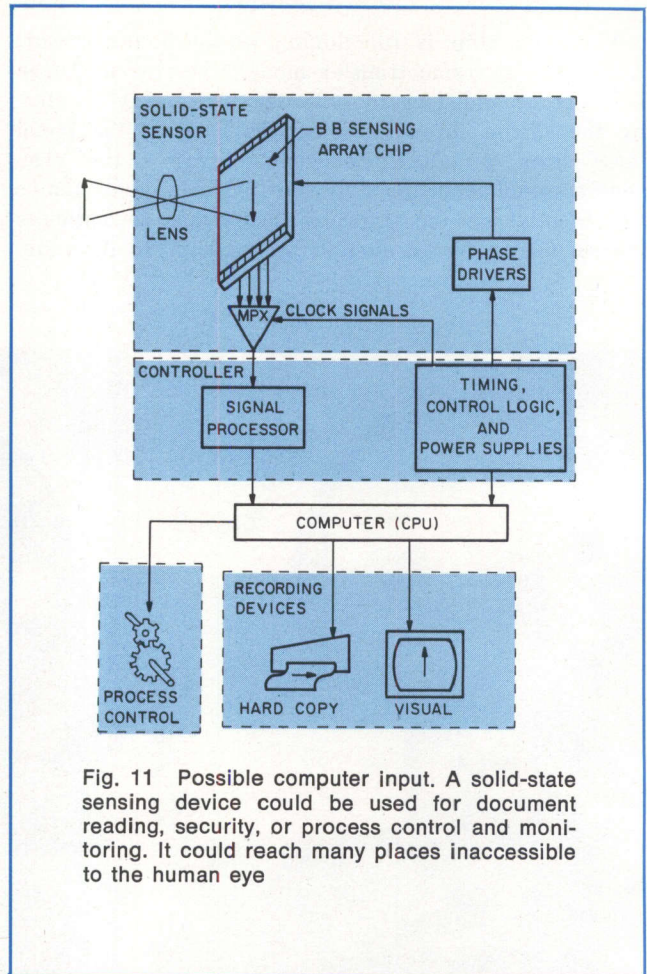


Fig. 11 Possible computer input. A solid-state sensing device could be used for document reading, security, or process control and monitoring. It could reach many places inaccessible to the human eye

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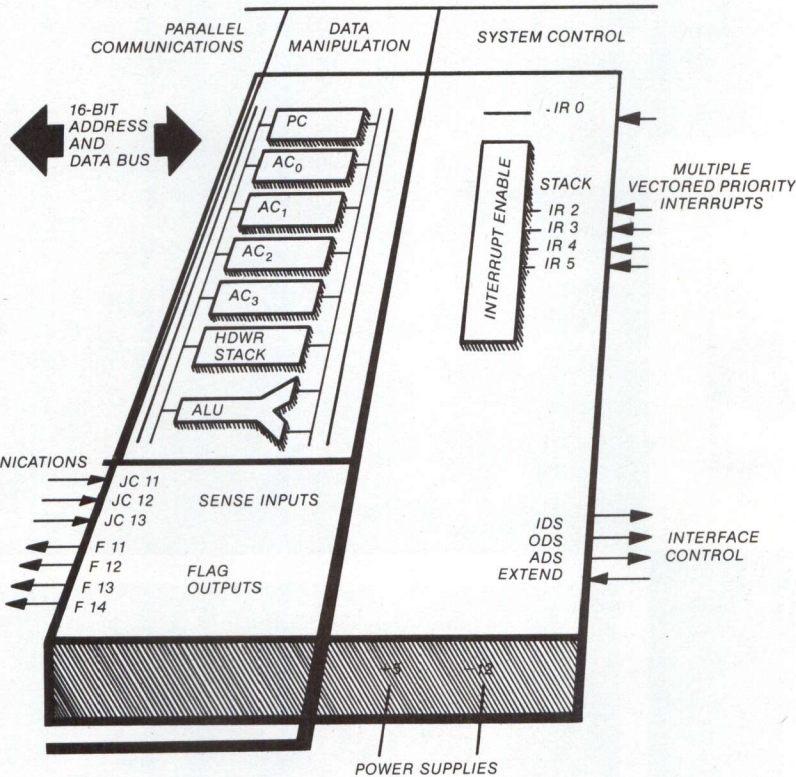
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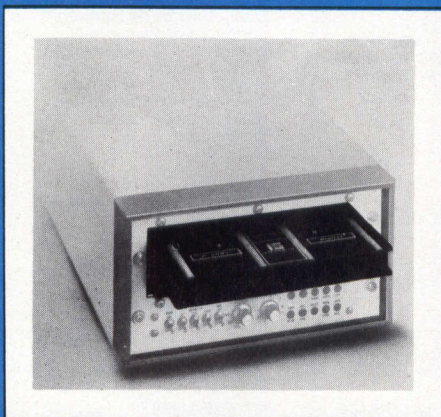
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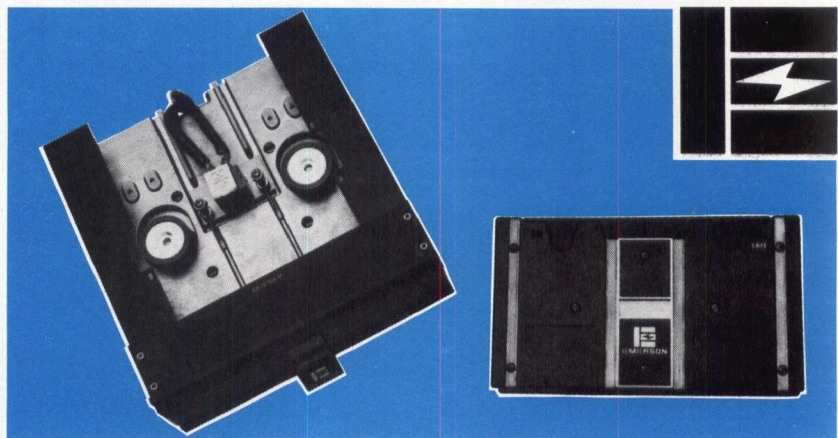
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Complex functions of many variables, difficult to handle conventionally in analog computers, are often generated in digital form by hybrid computers, at substantial penalty in time and accuracy; under a new approach to simulation they need not be

Multivariable Function Generation For Hybrid Computers

Arthur I. Rubin

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Multivariable function generation has been a problem with analog computers from the very beginning. Even hybrid computation has not satisfactorily solved it, because hybrid computers tend to run at digital, not analog, speeds in this application. Digital processes, which are intrinsically sequential, tend to be slower than analog processes which work simultaneously with many inputs in parallel, but are limited primarily in precision.

Now, however, a truly analog multivariable function generator (MVFG) allows faster than real-time simulation of functions of four or more variables for tradeoff or design studies, and frees both the hybrid computer programmer and the end-user analyst from constant concern over whether the phase-error-induced instabilities, sometimes observed in computer solutions, are real or appear only as a result of inadequate performance of the computer program.

Various analog techniques, all more or less inadequate, have been used in the past. For example, *Bivar*, which was limited to two variables, consisted of a semiconducting sheet on which equipotential lines were drawn. When the sheet was placed on a plotting board, and the board's pen replaced with a pick-up probe, it would produce a function $f(x, y)$. Limitations of accuracy, speed, and long set-up time for this device severely restricted its use.

Another 2-variable generator was assembled from 1-variable diode-function generators (DFGs), which approximate smooth, continuously varying nonlinear

functions by placing a series of linear functions end-to-end (Fig. 1). In this device, the breakpoints between linear segments in one function could vary as a function of another variable. Sixteen DFGs were required to produce one 2-variable function. Aside from tying up so much hardware, the approach required a lengthy set-up time, and, in addition, restricted the user to a narrow range of types of functions.

A much slower, but less costly, method was based on a tapped-servo potentiometer. With this component, interpolation among up to 17 functions of 1-variable (generated either by another tapped-pot servo driven by x , or by DFGs) was performed by a "y" servo. Again long set-up times were necessary, and the approach tied up lots of hardware.

Because of hardware limitations such as these, functions of two variables have often been generated by breaking them down into simpler entities, such as the sum or product of two functions having one variable each. More exotic variations of these techniques include quadratic interpolation among a limited number of 1-variable functions. Notably, none of these techniques attempts to generate 3-variable functions. This simply could not be attempted, since a single 2-variable function requires most of the nonlinear gear available on "old" analog computers.

Nevertheless, multivariable functions are often necessary in modern simulation of complex systems such as aerospace vehicles. Generating such functions requires from 40 to 60% of available digital processor

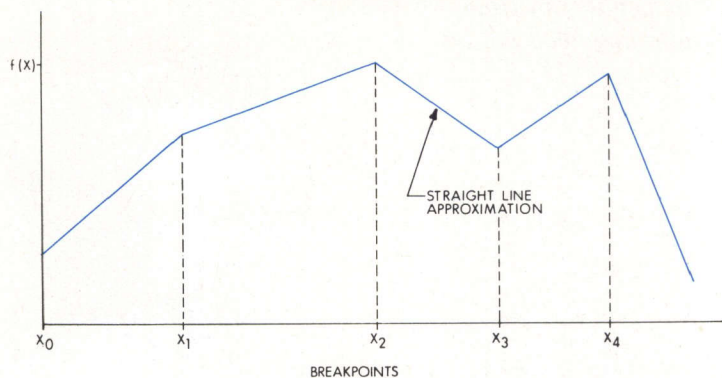


Fig. 1 Simple function generation. A diode plus a resistance has a linear voltage-current characteristic. Several such combinations, properly interconnected, can approximate almost any single-variable function

time in hybrid simulations, and similar proportions of time in all-digital simulations (which have the added burden of 1-variable functions). Multivariable function generation is also a significant factor in simulation of nuclear reactors, jet engines and turbines, and underwater sound propagation, as well as in ionospheric ray tracing. In these applications, functions take the

form of steam tables, curves relating pressure and flow to speed, velocity of sound as a function of distance in three spatial dimensions, and spatial variation of electron density. Multivariable functions also describe empirically determined basic characteristics of man-made devices or interaction of man-made devices with the environment. Common examples of the latter

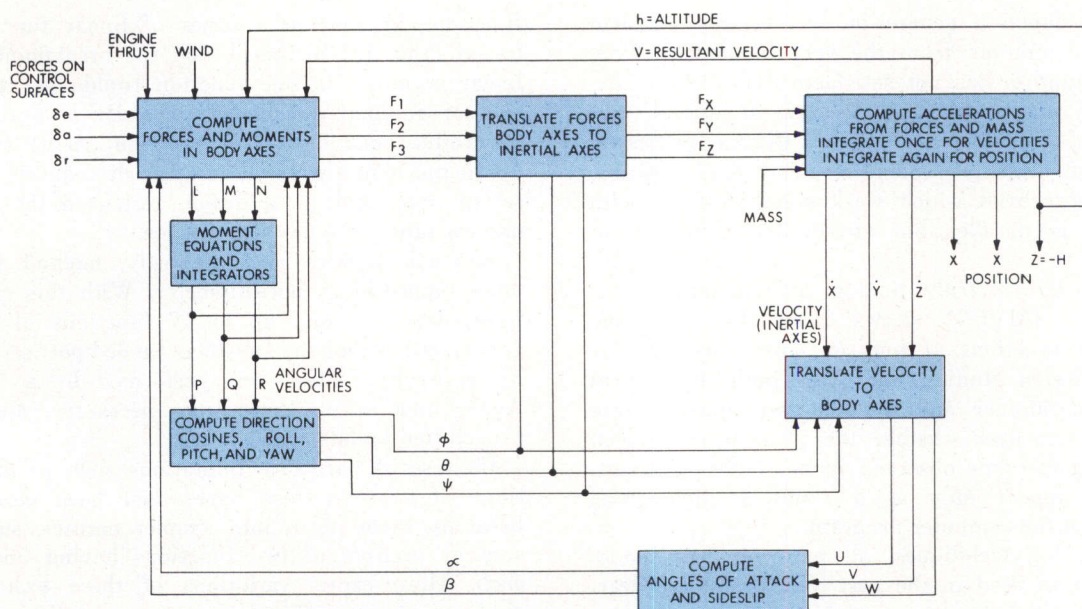


Fig. 2 Aircraft trajectory simulation. Several feedback loops are represented. For example, moments exerted on aircraft by external forces determine its angular velocity which can affect the moments. Similarly, these same forces determine accelerations and velocities of translation, which in turn determine the angle of attack and the angle of sideslip—or the relationship between the direction the airplane is pointing and the direction it is moving

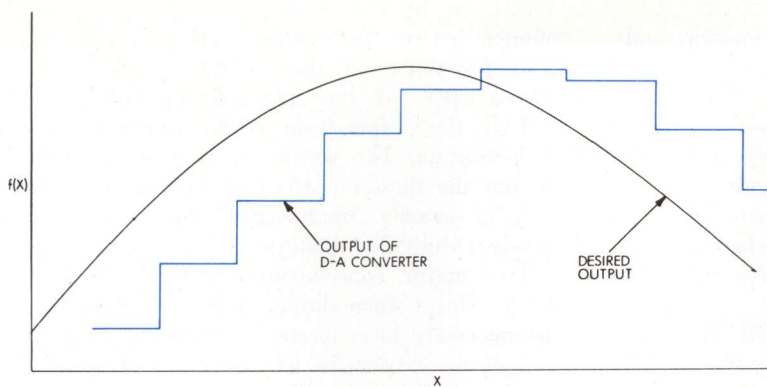


Fig. 3 Phase error. Because the output of a digital-to-analog converter can never perfectly match the desired waveform, an error arises that can significantly affect digital simulations of analog phenomena

are the aerodynamic forces and moments resulting from the interaction of an aerospace vehicle and its control surfaces with the air mass.

For example, the trajectory of an airborne vehicle can be computed from the forces (F_1 , F_2 , and F_3) and moments (L , M , N) in body axes (Fig. 2). Several kinds of variables affect the forces and moments. Some examples are external variables such as wind or wind gusts, which are obviously not under pilot control; control surface deflections δ_e , δ_a , and δ_r (elevator, aileron, and rudder), under pilot control, which produce forces through their interaction with the air; and, of course, engine thrust. All of these are examples of forcing variables, or forcing functions, which cause the airplane or missile to change its path. Other variables, which affect the aerodynamic forces, are altitude (h), vehicle translational velocity (V), angular velocity rates P , Q , and R , and angles of attack (α) and sideslip (β).

These variables are the most important from the aerodynamic viewpoint, since they affect the stability and response of the unpiloted airframe. Furthermore, important feedback terms are usually generated by an autopilot from α , β , P , Q , R signals and, sometimes, depending upon the sophistication of the control system, other velocity signals, which improve handling qualities and stability.

Thus, trajectory computation involves several important feedback loops. One is the "moment loop," in which, from moments L , M , N (the tendency of forces to produce rotation), angular acceleration terms \dot{P} , \dot{Q} , and \dot{R} are calculated. These are integrated once to produce angular velocities P , Q , and R , which in turn are immediately fed back to the moment loop to affect possible changes in moments L , M , and N . Another important feedback loop is the α , β loop, which is essentially a nonlinear "translational velocity" feedback. This feedback begins with the forces along the body axes, which are translated into inertial forces and then into accelerations and velocities in the three inertial directions. These, in turn, affect both the body forces, F_1 , F_2 , and F_3 , and the moments, L , M , and N .

The other two principal feedback terms are V (total translational velocity), and h , altitude. Of these, V

is more significant, since it affects all of the aerodynamic forces and moments. The effect of the altitude, h , is to vary the air density, which is a multiplying factor, or a gain effect, on the aero functions.

In simulating modern aircraft and missiles, all these variables must be taken into account. Fidelity of the simulation is crucially dependent upon the proper phasing of the angular and translational velocity contributions to the aerodynamic force and moment terms, as well as their equivalent contributions through external forces on the control surfaces. Only a few degrees of phase error in these contributions may be sufficient to degrade simulation of a stable airframe to appear unstable.

Phase error in an all-analog simulation is typically measured in tenths of a degree at frequencies of 1 kHz or more. The usual range of frequencies for modern aircraft is from 1 to 8 Hz, and for missiles from 2 to 250 Hz or more. At these frequencies, systems are well within the acceptable phase-error range of the analog components, even if the simulations are speeded up by factors of 10 or 100, as is sometimes the case for statistical and other design studies.

Phase errors of several degrees, at the frequencies required by aerospace simulations, are introduced when the essentially continuous aerodynamic forces and moments are represented as discrete quantities. When these are reconverted to analog form, there is inevitably a difference between the converter output and the original signal (Fig. 3). Discrete representation, in turn, has been necessary because of the absence of analog components that could generate multivariable functions conveniently or at reasonable cost—thus, the need to perform the simulation digitally and, therefore, sequentially, and to store the large number of data points (ranging from 10,000 to over 100,000) necessary to represent the multivariable aerodynamic functions during the sequential simulation.

Modern Methods for MVFG

Two methods for generating multivariable functions are in common use. Most widely known is a method

which uses a digital processor in a table look-up and interpolate routine; for speed of response, a hybrid approach is used.

In the hybrid method, the digital computer fetches data only when the variables are crossing a breakpoint; analog and interface hardware do all computing and interpolating while the variables are between breakpoints. This computation, like all-analog computation, is very fast, but requires less hardware than an all-analog simulation.

Both methods suffer from the same restriction, i.e., the execution of many functions by a single digital processor. Consequently, the effective frequency response ranges from a few hertz for the digital method to 20 to 50 Hz for the hybrid approach.

Two side effects result from the use of a digital computer in the "hot loop" for aerodynamic force and

moment calculations. One is that computation of the aero functions on this digital computer takes from 40 to 60% of the available central processor unit (CPU) time, and from 40 to 100% of the available core storage. The second, a consequence of the first, is that the digital portion of hybrid aerospace simulators is usually implemented on powerful (and expensive) digital computers.

Two major consequences result from these side effects. One, since large, powerful digital computers are necessary to generate aerodynamic functions, enough computing power is left over to perform increasing portions of the simulation that were previously allotted to the analog part of the hybrid system. Second consequence is that virtually all aerospace simulations in six degrees of freedom—both translation and rotation in each of the three spatial axes—have been

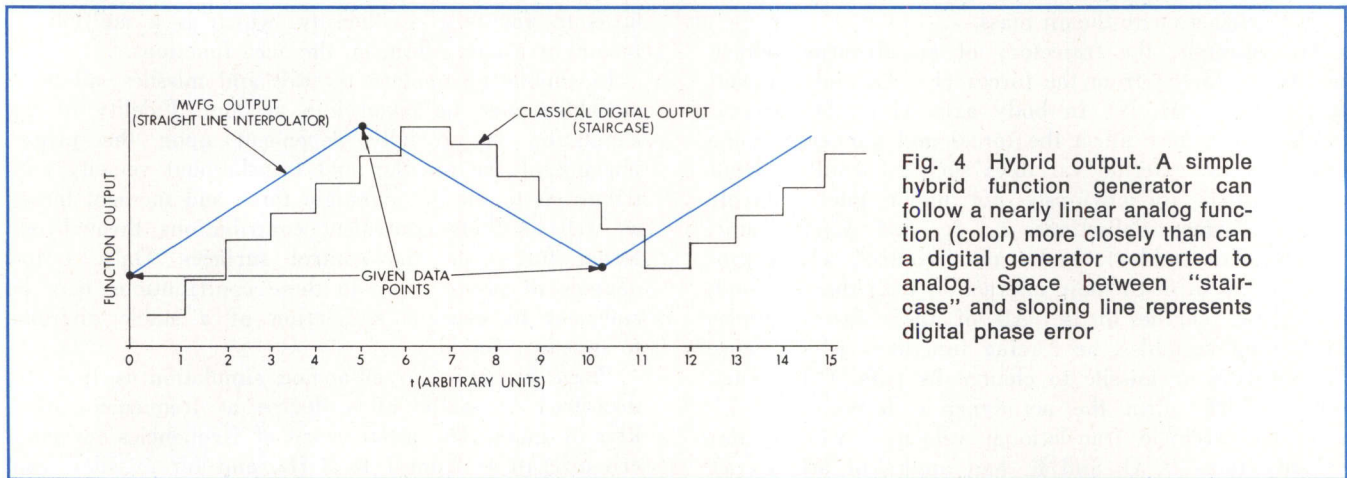


Fig. 4 Hybrid output. A simple hybrid function generator can follow a nearly linear analog function (color) more closely than can a digital generator converted to analog. Space between "staircase" and sloping line represents digital phase error

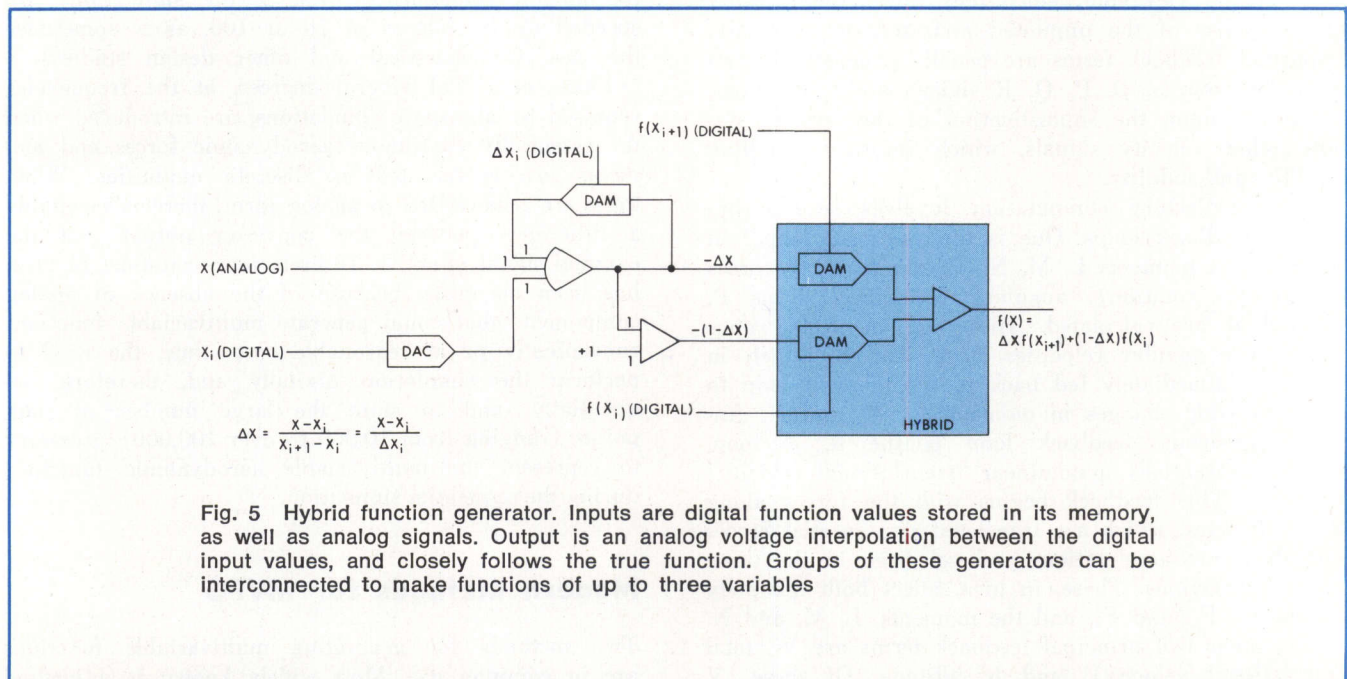


Fig. 5 Hybrid function generator. Inputs are digital function values stored in its memory, as well as analog signals. Output is an analog voltage interpolation between the digital input values, and closely follows the true function. Groups of these generators can be interconnected to make functions of up to three variables

restricted to execution in real-time speed. This precludes the advantages that system analysts would gain from generating families of solutions, quickly and inexpensively, which would allow them to make more meaningful tradeoffs among controllable system parameters, manufacturing tolerances, sensitivity to random (noise) inputs, and so forth, as well as a more thorough study of alternative designs.

Need for an Analog MVFG

Examination of Fig. 2 shows that the aerodynamic function computing block in the upper left corner is at the heart of the fastest, most critical feedback loops. If any of these variables must be generated on the analog computer because of speed requirements, it is

negate the gains realized by providing analog inputs to the aero computation—eg, reduction or elimination of phase shift in the high speed, critically important variables.

Consequently, from a phase-error or frequency-content viewpoint, if justification for computing these variables in analog form exists, many of the aerodynamic functions affected by them should also be computed analogically by components whose bandwidth and phase-error characteristics are compatible with the basic variable components. Ideally, such an analog MVFG would have error characteristics and bandwidth similar to those for other nonlinear analog devices, such as multipliers, resolvers, and 1-variable function generators.

Furthermore, availability of such a device and of analog consoles equipped with true MVFGs would

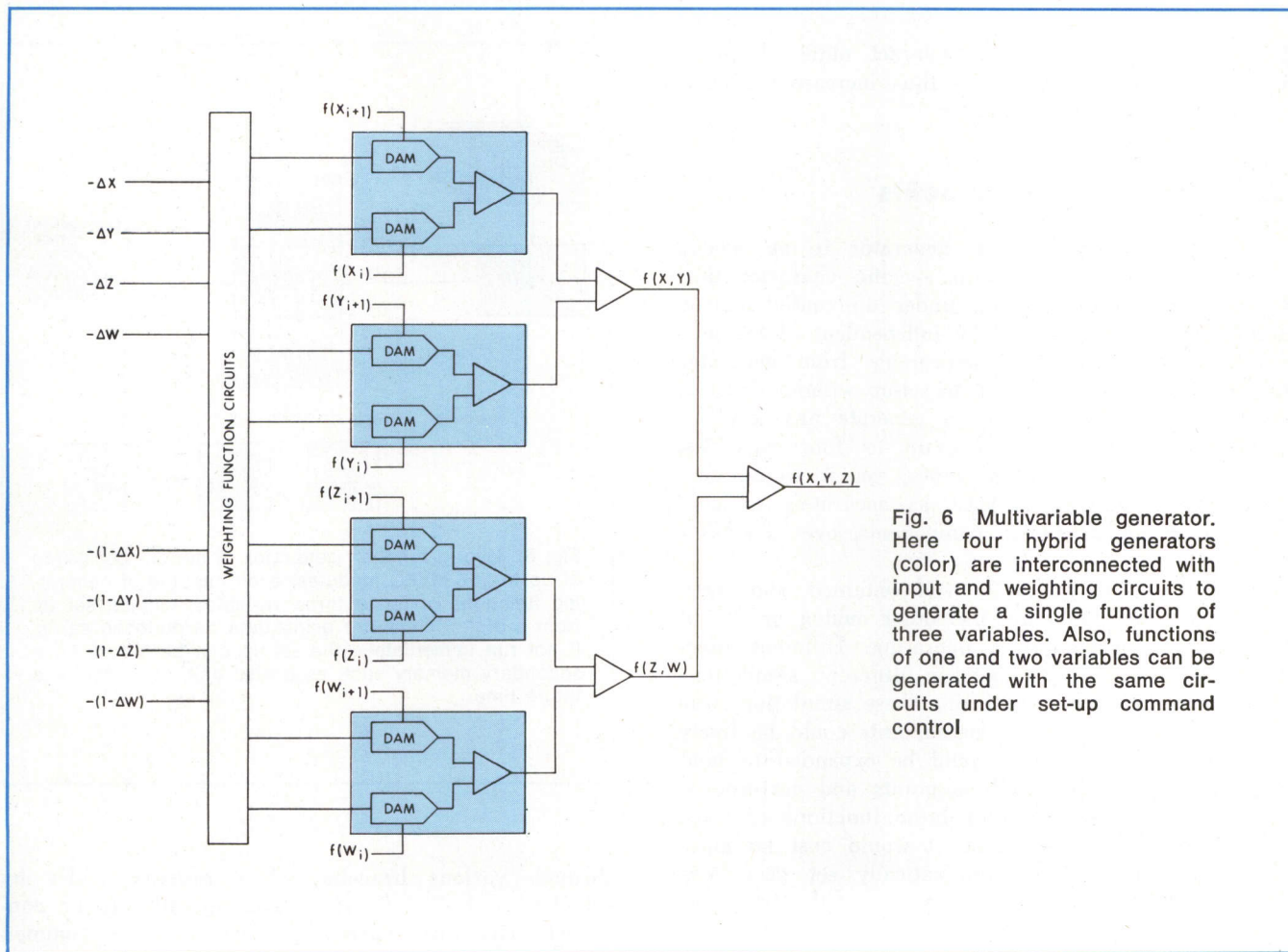


Fig. 6 Multivariable generator. Here four hybrid generators (color) are interconnected with input and weighting circuits to generate a single function of three variables. Also, functions of one and two variables can be generated with the same circuits under set-up command control

pointless to digitize the variables, do a table look-up and interpolation on a sequential digital computer, and then use the resulting aero functions either digitally or converted back to analog. The large phase errors which would be introduced by performing all of these steps in the heart of the hot loop would

free the digital portions of hybrid systems from the laborious and time-consuming task of generating such functions. The digital equipment could then be put to better use performing those parts of the computation that require great accuracy, or in analyzing, processing, and displaying the results of the simulation online.

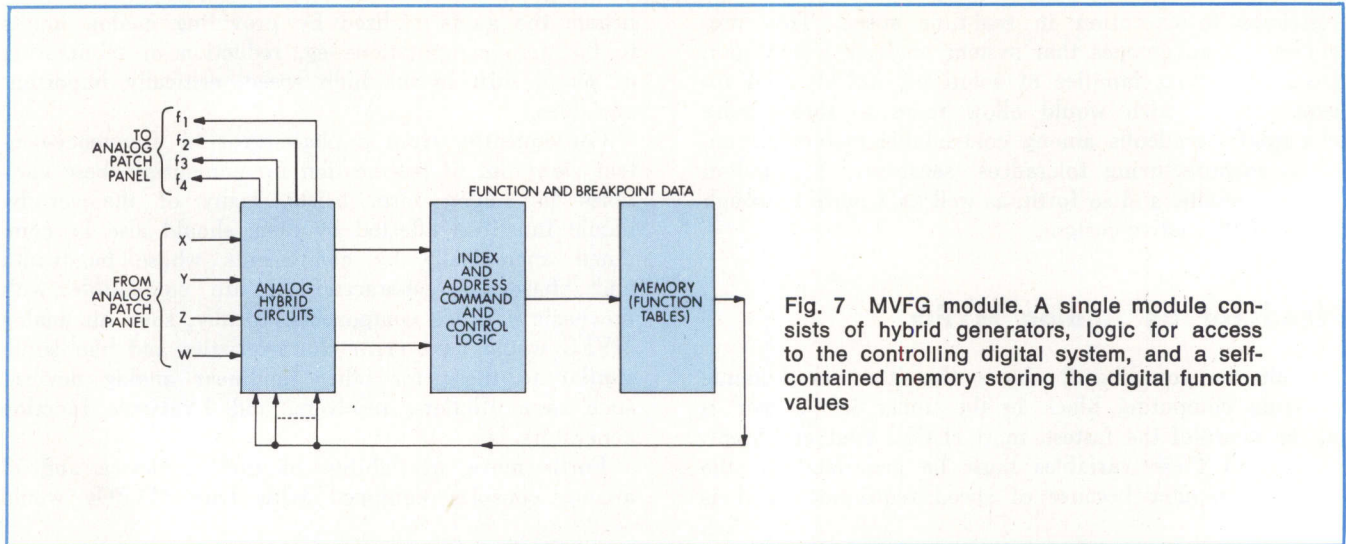


Fig. 7 MVFG module. A single module consists of hybrid generators, logic for access to the controlling digital system, and a self-contained memory storing the digital function values

By this means, they would interact more effectively with the systems analyst, and thus increase the effectiveness of the hybrid system.

User Features and Benefits

An ideal arbitrary function generator in an analog computer would have several specific characteristics: It could be instantly set-up under automatic control, and its performance would be independent of the generator used—it would be repeatable from generator to generator and from set-up to set-up without drifting. It would be programmable to generate any kind of multivariable function having up to four variables, including those with steep slopes, yet it would generate these functions at least as accurately as conventional nonlinear analog components, over a similar bandwidth.

In addition, it would be self-contained and independent—eg, it would not use other analog or digital computing resources while operating. Different function modules could be used in different simulations at the same time. In performing these simulations, the number and spacing of its breakpoints could be freely assigned, and its memory could be expanded to hold any practical number of breakpoints and corresponding function values, even for large functions of three variables. Last, but not least, it would cost no more than currently available automatically set generators of 1-variable functions, when operating at the 1-variable level.

An MVFG module has been developed which meets all of these requirements. It combines large digital data storage and continuous high speed analog interpolation. Its output (Fig. 4) is produced from a basic hybrid function generator circuit (see Ref.). This circuit (Fig. 5) utilizes multiplying digital-to-analog converters (DACs), often called digital-to-analog multipliers (DAMs). Like conventional DACs, DAMs may have a reference voltage from which current is routed

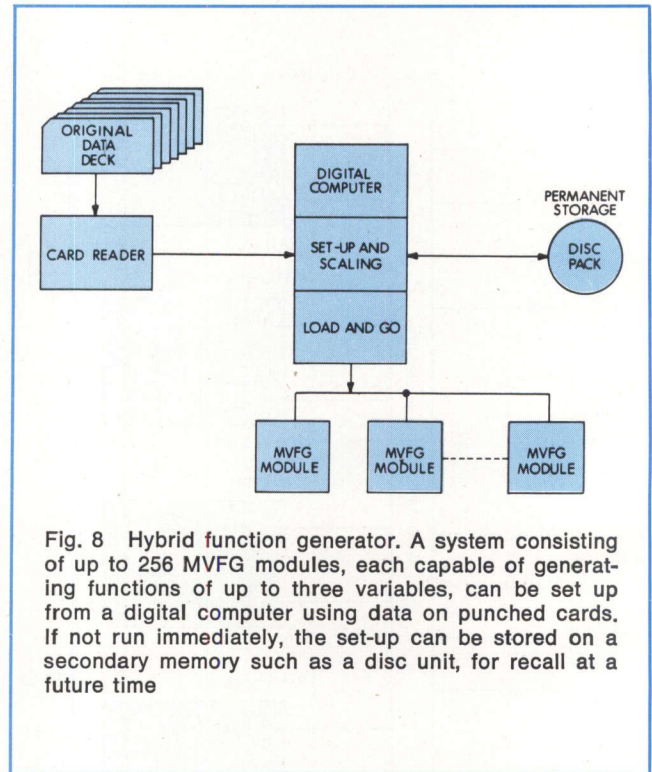


Fig. 8 Hybrid function generator. A system consisting of up to 256 MVFG modules, each capable of generating functions of up to three variables, can be set up from a digital computer using data on punched cards. If not run immediately, the set-up can be stored on a secondary memory such as a disc unit, for recall at a future time

through various branches of a resistive adder by switches controlled by the digital quantity to be converted. The total current at the resistor's common node, or a voltage derived from it, is an analog quantity proportional to the digital input quantity. However, in the DAM, the reference voltage is not fixed; it can vary, and the circuit's output is proportional to the product of this "reference" or variable and the digital input.

Analog variables are converted to normalized scaled analog variables, such as ΔX , $1 - \Delta X$, by the input detector circuits, shown in Fig. 5.

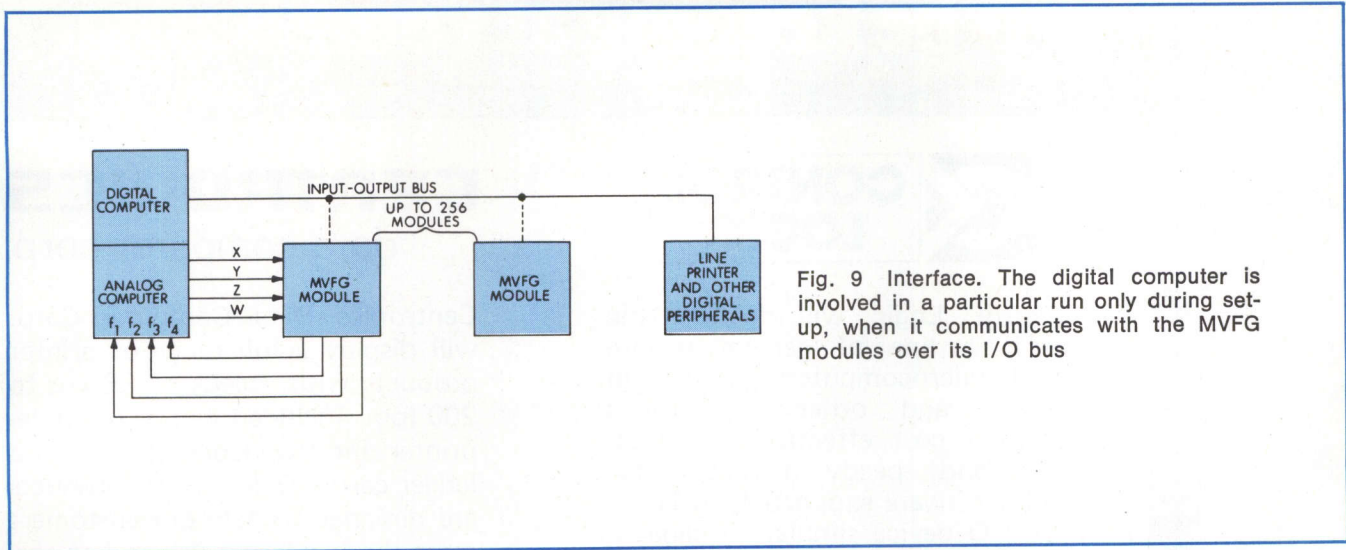


Fig. 9 Interface. The digital computer is involved in a particular run only during set-up, when it communicates with the MVFG modules over its I/O bus

The normalized analog variables, ΔX , ΔY , ΔZ , $1 - \Delta X$, $1 - \Delta Y$, $1 - \Delta Z$, are transformed through weighting function circuits, which then are multiplied by the function values, f_i , contained in the output DAMs, which represent the stored data points of the corners of the functions in the local region defined by ΔX_i , ΔY_i , and ΔZ_i . The circuit for a function of three variables is shown in Fig. 6. Analog comparator circuits sense when the input variable crosses a breakpoint, and signal the module to fetch new data from its own memory (Fig. 7).

The MVFG is a modular unit housed in a single chassis containing all components necessary to form one function of three input variables, plus electronic switches for reconfiguring the generator. Up to eight modules can be housed in one standard single-bay rack along with a power supply.

The MVFG module may be functionally divided into two major subgroups. The first includes high speed digital logic and control, 4000 words of high speed memory, and an interface to a master digital computer. The second subgroup, the hybrid interpolator, includes four analog input units, four quad multiplying DACs, several analog multipliers, and output buffer amplifiers. Under control of the master digital computer, the module can be configured in one of three modes of operation, generating one function of three variables $f(x, y, z)$, two functions of two variables, or four functions of one variable. One function of four variables can be generated with two such modules, requiring only a small internal change to the standard module.

Software for access to the module is included in the standard FORTRAN Run Time Library. Arguments for this routine indicate the desired configuration of the MVFG module, its address, and breakpoint and function value data. The module, after it is configured by the system digital computer, produces continuous analog function values corresponding to the applied analog inputs.

The MVFG is loaded by the system digital computer (Fig. 8) from a card deck. This permits the system

digital computer to perform all of the set-up, configuration, and module assignment (Fig. 9). The digital computer then generates the run-time "load and go" file, which can be loaded immediately into the MVFG modules or stored away for later use on a digital mass-storage device.

An initial use for MVFG modules will be at the U.S. Army's MICOM Advanced Simulation Center, Redstone Arsenal, Alabama. The units will be an expanded version of the basic modules, wherein each of the four MVFGs installed will produce up to eight output functions from four input variables, relieving the hybrid system's digital computer from time-consuming function generation, trigonometric resolution, and certain algebraic tasks. The four modules, contained within a standard 21-in. rack, will be addressable to any of six analog variables, such as ΔX , $1 - \Delta X$, by the input that is used along with a multiple-OR (MOR) switching network to provide for analog computer control and computation of three simulation cells for any of several digital computers.

Reference

A. I. Rubin, "Hybrid Techniques for Generation of Arbitrary Functions," *Simulation*, Dec 1966, pp 293-308



Presently manager of the scientific computation department at Electronic Associates, Arthur I. Rubin's background includes responsibility for analog/hybrid computer study projects, analytical studies of aerospace vehicle systems, and implementation of a large independent hybrid computing system.

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Tools for Logic Analysis

Jim Wagner

Tektronix, Incorporated
Beaverton, Oregon

Although logic analyzers have increased in variety and capability, useful perspective can be gained by stepping back and comparing them with oscilloscopes—the most familiar tool for analysis and detection in engineering laboratories

For several years, the imminent demise of the oscilloscope as a tool for logic analysis has been predicted. These predictions would seem to be borne out by the recent development of sophisticated and powerful logic analyzers. However, aside from the fact that many logic analyzers use oscilloscope displays, oscilloscopes still offer significant power and utility to users with logic problems.

Problems encountered include open- and short-circuit conditions in networks, faulty components, improper impedance levels, intermediate voltage levels, and excessive propagation delays. Instruments used to track these problems down include logic probes, logic clips, word recognizers, and digital delay generators. When used in conjunction or in competition with these tools, oscilloscopes have both undeniable strengths and unconcealable weaknesses.

Logic problems are conveniently separated into two groups (see Table); these characterizations are not absolute, of course, and the classifications overlap somewhat.

"Simple" Logic Problems

Characterized as "simple" or "low

frequency" or "gate-functional," the first group of logic problems relates to the logic network's basic integrity, and includes open and short circuits, and nonfunctional gates and flip-flops. Symptoms can usually be detected by dc or low frequency testing, which checks input and output logic levels, and impedance levels. The basic question here is simply whether the network's dc parameters are correct.

Instrumentation used to troubleshoot this first group of problems is diverse, ranging from the venerable voltohmmeter (VOM) to the latest

in simultaneous voltage- and impedance-sensing logic probes. Virtually any voltage-sensing device, whether VOM, vacuum-tube voltmeter (VTVM), digital voltmeter (DVM), or oscilloscope, will perform some of the measurements.

Logic probes, however, have several advantages, including detection of specific logic levels and display at the point of measurement (Fig. 1). Logic probes do not divert the user's attention from the measurement point to a display, which he must first look at and then inter-

Characterization of Logic Problems

	<u>"Simple" Problem</u>	<u>"Complex" Problem</u>
System description	Network integrity	Network timing
Common faults	Shorts, opens, non-functional logic	Induced transients, propagation delays
Time scale	Long	Short
Common tests	Logic levels, impedance levels	Logic sequence testing

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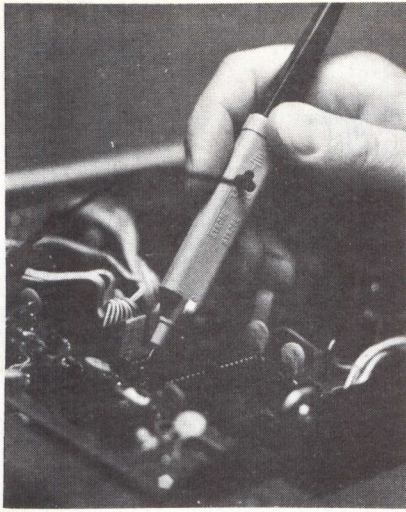


Fig. 1 Logic probe. These simple devices can detect logic levels, pulse trains, and some abnormal conditions (Tektronix, Inc)

pret. Most logic probes indicate a HIGH logic level by lighting one indicator, and a LOW by lighting another. When both are on, a pulse train is cycling between a high and a low level; when neither is on, the level is usually somewhere between the two logic states.

However, logic probes offer mixed blessings. A single probe can seldom be used on more than one logic family, and may add enough loading to alter circuit operation. In addition, some probes require power connections to the circuit.

The *logic clip* (Fig. 2) is like several logic probes in one package: it displays all the static states of an entire device clearly and concisely. However, one major difference from the logic probe is that it has only one indicator showing the logic state at each terminal, and thus does not readily detect in-between levels. Loading problems are usually similar to those of the logic probe.

One unique logic clip is really a logic comparator. When a known-good integrated circuit (IC) of the type being tested is placed in the clip, indicators show when the good IC differs in output from the test IC.

With input impedance of at least 1 M Ω —much higher than a logic probe or clip—oscilloscopes present minimal circuit loading. Their wide range of sensitivities presents no compatibility problem with various logic families. Logic levels which are neither strictly 0 nor 1 are readily

detected. Display interpretation is eased by marking logic levels on the oscilloscope's CRT faceplate with a grease pencil. Special overlays are also available which prevent scratching of the faceplate. Among the oscilloscope's many other capabilities are transient observations and power supply ripple measurement.

Some disadvantages of using an oscilloscope are that attention must be diverted from the measurement point, and that the instrument does not provide the logic clip's simultaneous display. Since oscilloscopes also cost more than simple logic probes, cost and special-purpose functions have to be balanced against their versatility.

Complex Logic Problems

The second group of logic problems might be characterized as "dy-

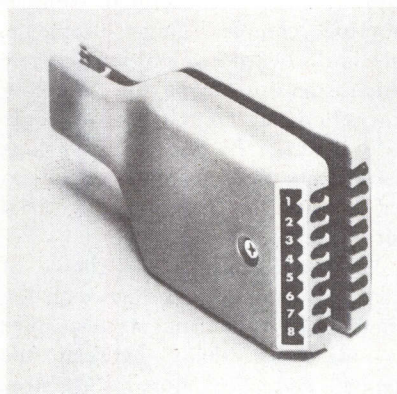


Fig. 2 Logic clip. Concise information about logic levels at various pins of an IC is provided simultaneously by these units (Continental Specialties Corp)

namic," "high speed," "system functional," or "glitch hunting." Having to do with time relationships within the logic network, these problems include measurement of propagation delays, pulse coincidence, improper rise and fall times, and induced transients. They can be particularly frustrating, as they frequently occur at random or in conjunction with a specific system state.

A significant portion of the fault-finding procedure for these problems often consists of determining the system state or the state of pertinent logic variables associated with the fault. This determination may be difficult, because the fault may be hidden in a sequence of

normal and correct logic changes, or it may occur very infrequently. To be useful for detecting logic problems in this group, an instrument must be able to surmount such difficulties.

Several recent innovations have appeared among the instruments available for use in solving complex logic problems. One type of instrument has been called the "super logic probe"; another is the logic analyzer. Yet another, an old friend with new helpers, is the oscilloscope.

The *super logic probe*, or hand-held logic analyzer (Fig. 3), provides more time-related information than the simple logic probe. A simple logic probe can often detect narrow pulses; a logic probe with strobe inputs can detect pulse coincidence. In contrast, one type of hand-held logic analyzer samples, stores, and displays several parallel inputs at an adjustable time delay after an input trigger. Other hand-held logic probes load a single serial input into a shift register under control of an adjustable-rate clock or external trigger and stop the shifting operation at a selectable number of clock pulses after another trigger. This is, effectively, a pre-trigger; it allows observation of a logic sequence leading up to a specific state. The display on these probes is an array of light-emitting diodes (LEDs) indicating the contents of the storage register.

Offsetting the considerable capability of these probes is their inability to sense a unique combination of states which may denote a fault. They also suffer from a lack



Fig. 3 "Super Logic Probe." This hand tool displays status of system in a 32-stage shift register shifted by an external clock trigger (CPSR, Inc)

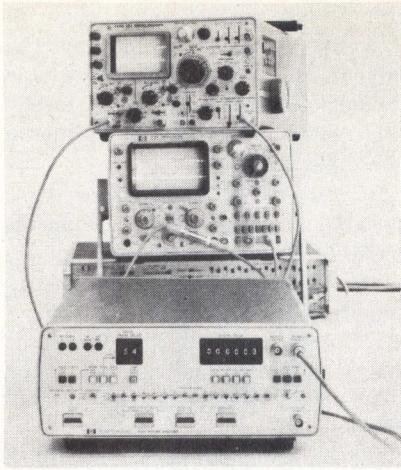


Fig. 4 Logic analyzer. This particular unit (foreground) uses a separate oscilloscope to display its data. It has 16 parallel inputs and can sense any specified combination of them as a trigger. It also has digital delay between the trigger and the storage control (Hewlett-Packard Co)

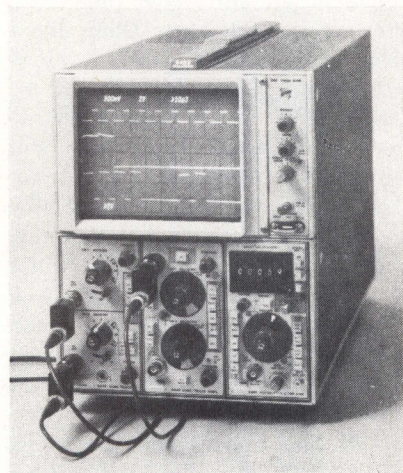


Fig. 5 Plug-in oscilloscope. Two dual-trace plug-in modules permit this oscilloscope to display up to four traces apparently simultaneously. A digitally delayed sweep provides either delay by time or delay slaved to a system clock (Tektronix, Inc)

of resolution; data are stored only on clock command. Glitches or transients occurring at other times are often missed.

The full *logic analyzer* (Fig. 4) has been implemented in several forms. All offer parallel inputs ranging from 2 to 16 channels, and sample and store input data in memories, varying from 16 bits or samples per channel to three or four times that in capacity. Some set the time interval between samples with an internal sampling clock,

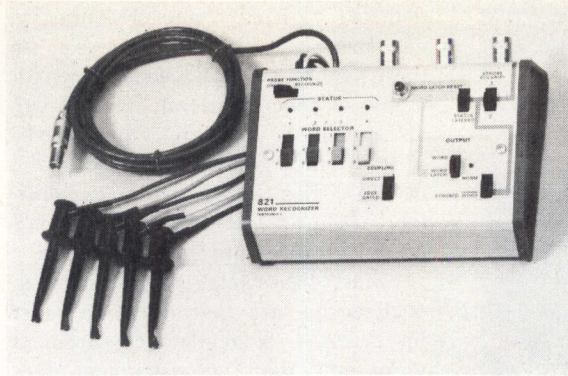


Fig. 6 Word recognizer. Any oscilloscope can have combinational triggering with this accessory. It senses four bits and can be expanded in increments of four bits (Tektronix, Inc)

while some sample only on command of an external signal; a few offer both capabilities. Displays also vary considerably, and include CRT displays of data as "pseudo-waveforms," CRT displays of sequential truth tables as logical 1 and 0 notations, and LED displays of stored data.

Many logic analyzers offer several significant features useful in troubleshooting complex logic problems. One is the word recognition trigger, which starts or stops the sampling process on any combination of logic states selected by the user. Various instruments offer capabilities for triggering on parallel words, serial words, or both.

Another feature is the choice of starting or stopping storage with the trigger. Many instruments also offer an adjustable delay between the trigger and the store start/stop. These two features provide an effective pre-trigger (in conventional oscilloscope terminology) which stores and displays system states that occur before the main trigger. For example, if storage in a 64-sample storage register is stopped 16 clock intervals following word trigger (on a fault, perhaps), the register contains the 48 samples that precede the trigger and the 16 samples that follow.

Together, these three features allow selective storage, so that, for example, only events leading up to a fault are stored. Detecting the occurrence of a specific fault and recording the logical process that leads to it can be a great help in fault tracing.

Oscilloscopes

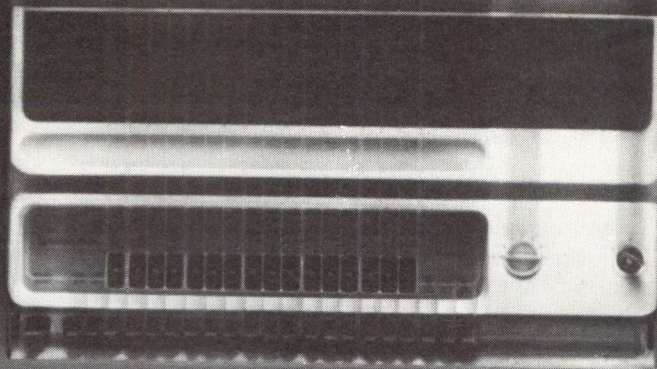
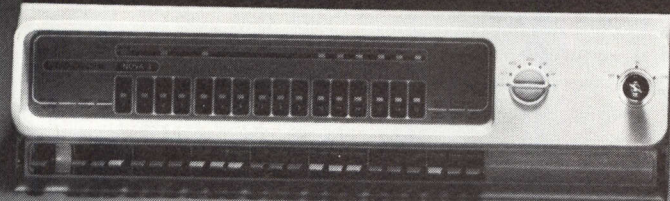
Conventional oscilloscopes (Fig. 5) have several difficulties in handling complex logic problems. One difficul-

ty is combinational or word triggering; however, accessories are available to perform this function (Fig. 6). In addition, word recognizers can be fabricated with comparators or combinations of exclusive-OR and AND gates. Such fabrication is often the only option when non-TTL logic is being analyzed.

Lack of a pre-trigger is a somewhat more difficult problem for oscilloscopes. With the built-in delay line that is included in most high-speed oscilloscopes of 10 to 15 MHz and up, the leading edge of a trigger is observable, along with the preceding logic level, at any point in the logic network. It is not possible, however, with current conventional oscilloscope technology, to observe signals earlier than that. Random-sampling oscilloscopes can provide a significant pre-trigger capability in high speed logic systems, but they have limited utility in low speed systems.

There are situations, however, where a pre-trigger effect can be obtained. If the fault is nonfatal and can be made to recur, the oscilloscope can be triggered at a unique point in the system cycle (using a word recognizer, for example). Then, using digital delay, the sweep starting point can be stepped incrementally toward the fault, while the technician observes the logic state. If the digital delay is controlled by a system-related signal such as the system clock, very long delays, with little or no jitter, can be used. Digital delays are available as a combination delay and sweep, as a standalone package, or as an oscilloscope plug-in delay unit.

Another problem oscilloscopes have is simultaneous display of several input channels. Although



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CIRCLE 39 ON INQUIRY CARD

many oscilloscopes offer up to four input channels, these are displayed simultaneously only in the chopped mode. In this mode, the display switches from channel to channel several times during a single sweep, thus "chopping" each display into discontinuous pieces. If the chopping frequency is not high enough, all parts of the signal from each channel are displayed only after several sweeps. Persistence of the phosphor and of vision make the displays seem continuous and simultaneous.

However, since typical chopping frequencies are usually less than 1 MHz, the chopped operation is suitable only for slow-speed logic.

Alternate channel switching, in which successive sweeps are dedicated to individual channels, does not provide simultaneous display, but can be used effectively if the system is cyclic and the fault is not fatal. Again, a trigger unique within the system cycle is required—another application for a word recognizer.

Storage and variable persistence oscilloscopes help capture and retain information about transients or faults when faults occur randomly or infrequently. Most storage scopes, when used with a digital delay unit and a word recognizer, form a package with significant capability for logic analysis.

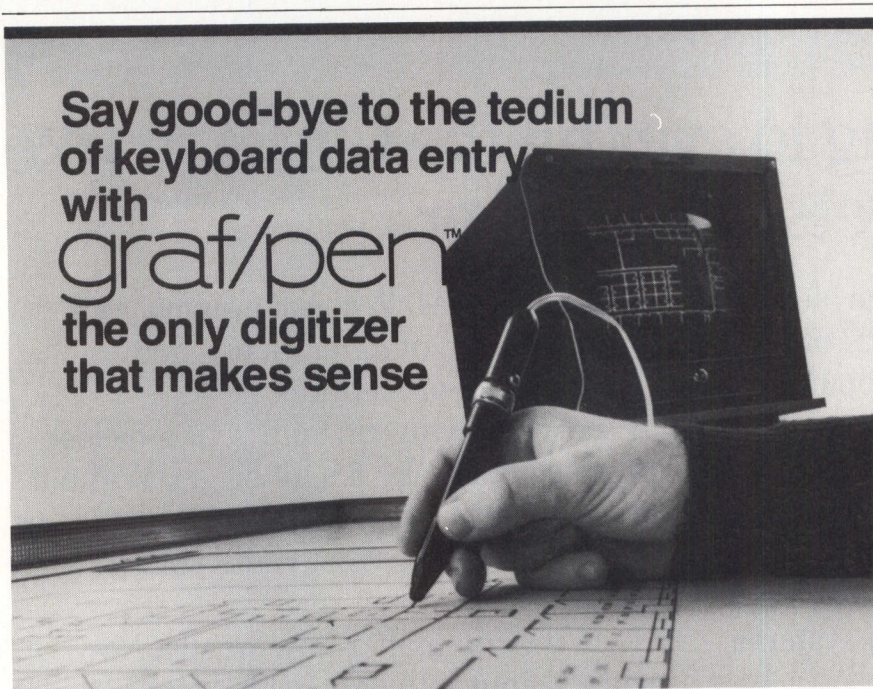
What capability does an oscilloscope have that logic analyzers do not? In brief, it has versatility and continuous—not sampled— analog display. Logic analyzers cannot accurately display slow rise and fall times, in-between logic levels, and the like, because most of them use single-level comparators set near the midpoint of the logic swing. Thus, a signal above the comparison level is sensed and displayed as a logic HIGH while a signal below that level is sensed as a logic LOW. However, logic does not sense the same thing that the analyzers sense. For example, if the analyzer threshold for TTL is 1.45 V, it will recognize 1.6 V as HIGH; however, if low and high logic levels are 0.8 and 2 V, respectively, the logic response to a 1.6-V signal would be unpredictable.

The oscilloscope's full analog display makes problems like this readily apparent. It can accurately show slow rise times and indeterminate levels; or, without sampling, precisely where anomalous signals occur. Versatility has been, and still is, one of the oscilloscope's major strengths. With an oscilloscope, ground bus or power supply noise and core memory signals are directly observable, and troubleshooting power supplies, tape drives, or paper tape readers is possible.

In conclusion, the oscilloscope is hardly in a state of imminent demise for logic analysis, even though logic analyzers can do the job more simply in some situations. The perfect logic analysis tool has not yet been devised, and the oscilloscope continues to be improved; its logic analysis capability will continue to provide a major and significant solution to troubleshooting logic problems.

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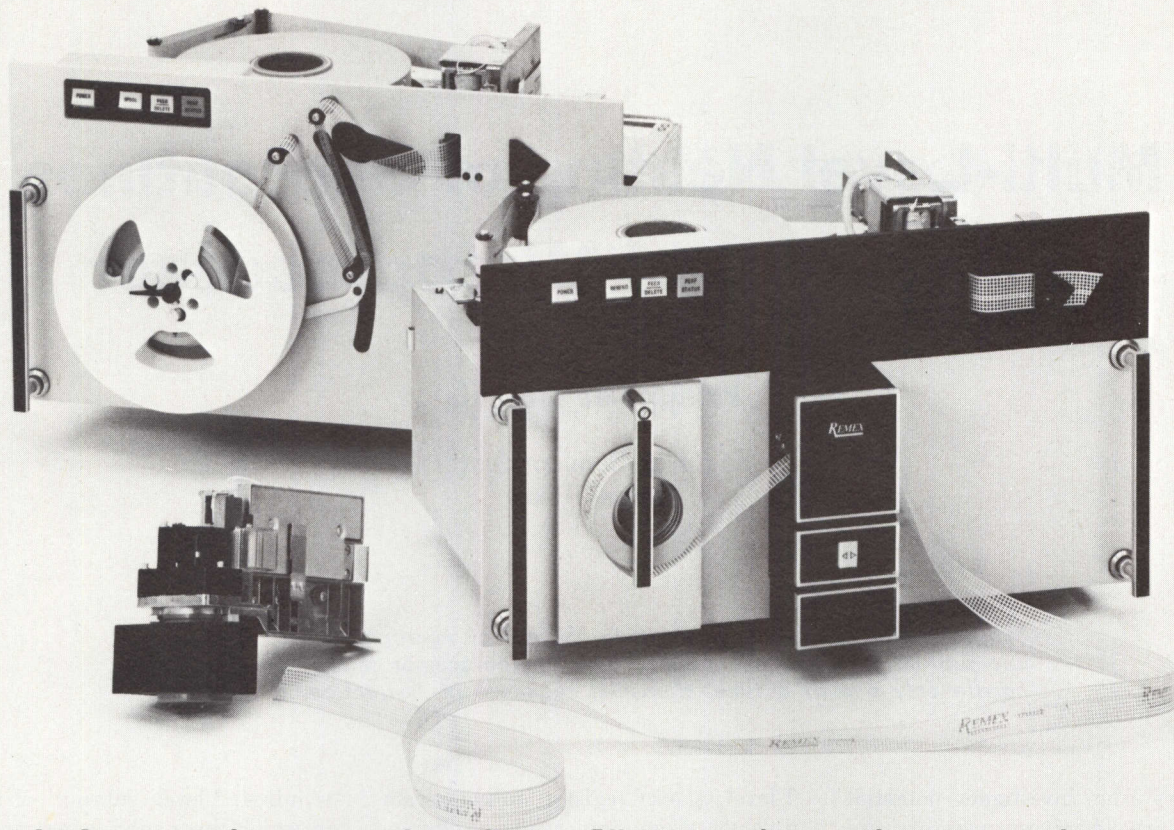
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CIRCLE 41 ON INQUIRY CARD

Multi-Level Nesting of Subroutines in a One-Level Microprocessor

Philippe de Marchin

Fairchild Semiconductor
Dallas, Texas

Subroutines are valuable adjuncts to the use of microprocessors; but when one subroutine must call another, in a microprocessor that is designed to handle only one at a time, a special sequence of instructions is necessary

Engineers who investigate potential applications of microprocessors are often obliged to execute in software familiar functions they are accustomed to implementing in hardware. Although the logical process of design is essentially the same, they sometimes find the details baffling. One such detail is the use of subroutines, which can perform the same task at different points in a program with a single, short sequence of instructions, and of nested subroutines, in which one subroutine calls for another, and perhaps another, and still another.

Each subroutine requires temporary storage of the contents of the program counter, so that at the conclusion of the subroutine, the processor "remembers" where to resume the main routine. In general, multiple-nested subroutines require as many temporary storage locations as there are levels of nesting.

Thus multiple-nested subroutines in a microprocessor having only a

1-level stack register might seem difficult, if not impossible, to implement; such is not the case, however. On the contrary, under software control, nesting is quite simple.

Such a stack register is contained in the new Fairchild F-8 microprocessor (Fig. 1). It readily handles nested subroutines with the aid of the microprocessor's 64-byte scratchpad memory, which is used as an automatically expandable stack register.

Where To Use Nesting

Nested subroutines are useful, for example, in square root computation and in transferring data to a serial printer such as a teletypewriter. A square root subroutine requires, as part of its execution, a division process, which is executed by another subroutine. This, in turn, requires a subtraction process which may be performed by yet another subroutine. Thus, computing a square root

requires 3-level subroutine nesting, in which three subroutines are called in sequence from the main program.

In serial printing, a line of 8-bit characters is printed, one at a time. The task requires the main program to call one subroutine, SEND. As the microprocessor leaves the main program and begins executing this subroutine, its first step is to locate the beginning of the data to be printed. It loads the first character in a preassigned scratchpad register and calls a second-level subroutine, designated PRINT. At this level, two calls are made to two third-level subroutines, PARC and TTYO. PARC is a parity check routine that verifies the validity of the character, or, if it detects an error, replaces it with a special character, such as @. TTYO, which stands for Teletype[®] Output, transmits the bits of the character, one at a time, preceding and following them with start and stop bits, according to the standard code for such printers. After the

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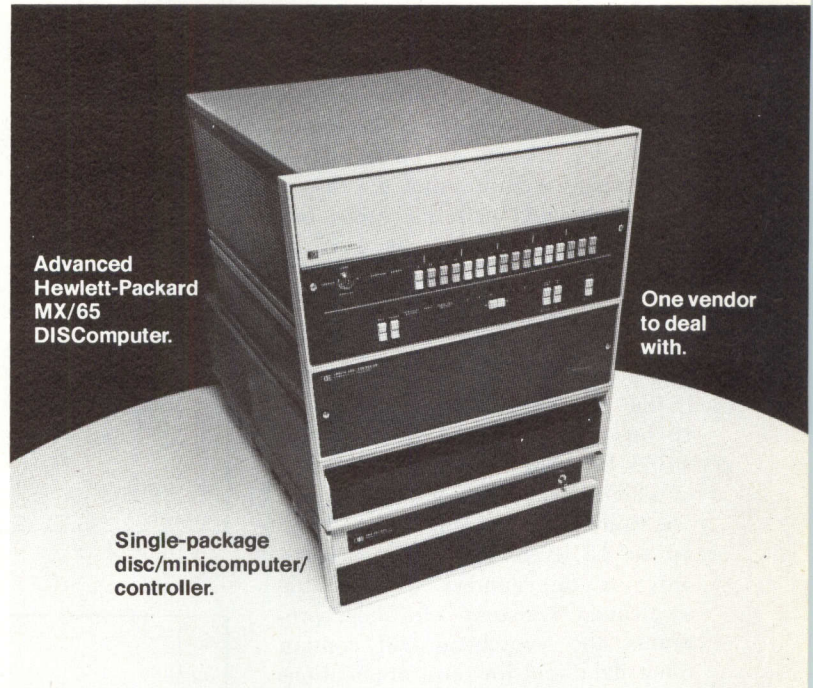
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character is transmitted, TTYO returns to PRINT, which then returns to SEND, which fetches the next character if the last one in the line has not already been printed.

Under different circumstances the same routines can be called for use in other ways. For example, PARC can be used independently of any printing operation—perhaps in connection with another type of output or input, or where an error following an internal operation is suspected. This independence of operation is what makes a subroutine a subroutine, as opposed to inline code; but executing a subroutine as part of another subroutine is nesting.

Multiple Nesting with One Pointer

In the F-8, the program counter is 16 bits wide; each address thus requires two scratchpad registers, each of which holds one byte (eight bits). The coding shown here is good for up to 31 levels of nesting, limited only by the number of available scratchpad registers. (In most programs, the scratchpad will contain other data, and for most applications only a few levels of nesting are sufficient.)

To execute a subroutine, certain preparatory instructions in the main routine are required, together with a special 11-byte sequence of 10 instructions, called Service (SERV), which stores the previous contents of the program counter in the scratchpad (Fig. 2). Following the subroutine, another sequence of 1-byte instructions, called Go Back (GOBA), reloads this stored address in the program counter. Each subroutine must begin and end with the two specific instructions that call these two sequences—which are themselves, in fact, short subroutines.

At the moment a jump to a subroutine occurs, whether from the main routine or a higher-level subroutine, scratchpad location 0 must contain an address one higher than the highest available scratchpad locations, into which the stack register contents will be moved after the jump. Location 0 is a working register for use with the indirect scratchpad address register (ISAR)—a 6-bit register that points to one of the 64 locations in the scratchpad.

The two preparatory instructions in the main program establish the

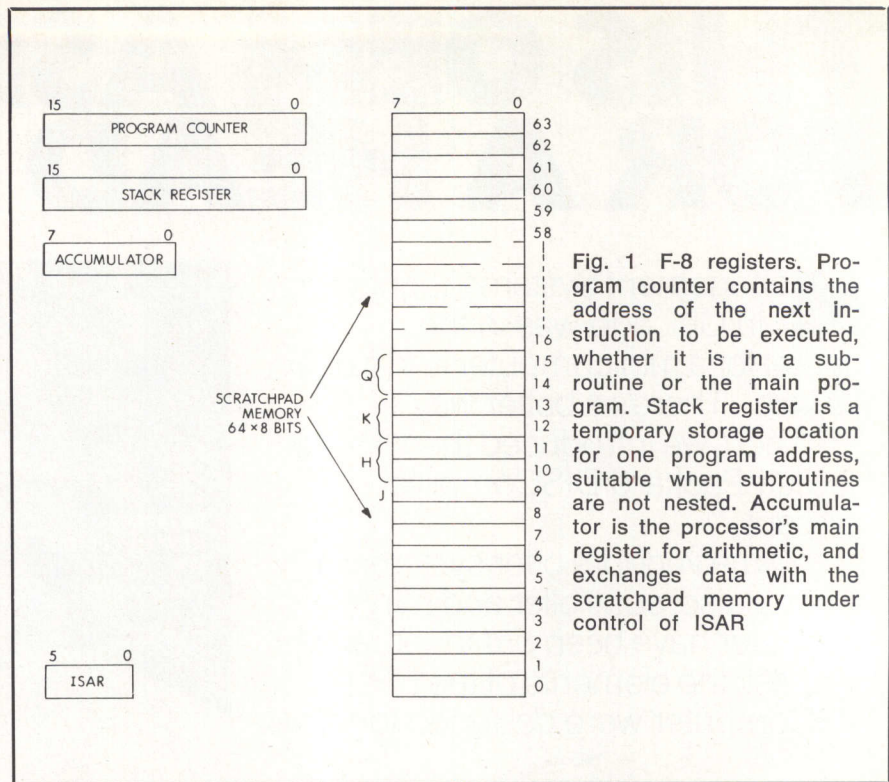


Fig. 1 F-8 registers. Program counter contains the address of the next instruction to be executed, whether it is in a subroutine or the main program. Stack register is a temporary storage location for one program address, suitable when subroutines are not nested. Accumulator is the processor's main register for arithmetic, and exchanges data with the scratchpad memory under control of ISAR

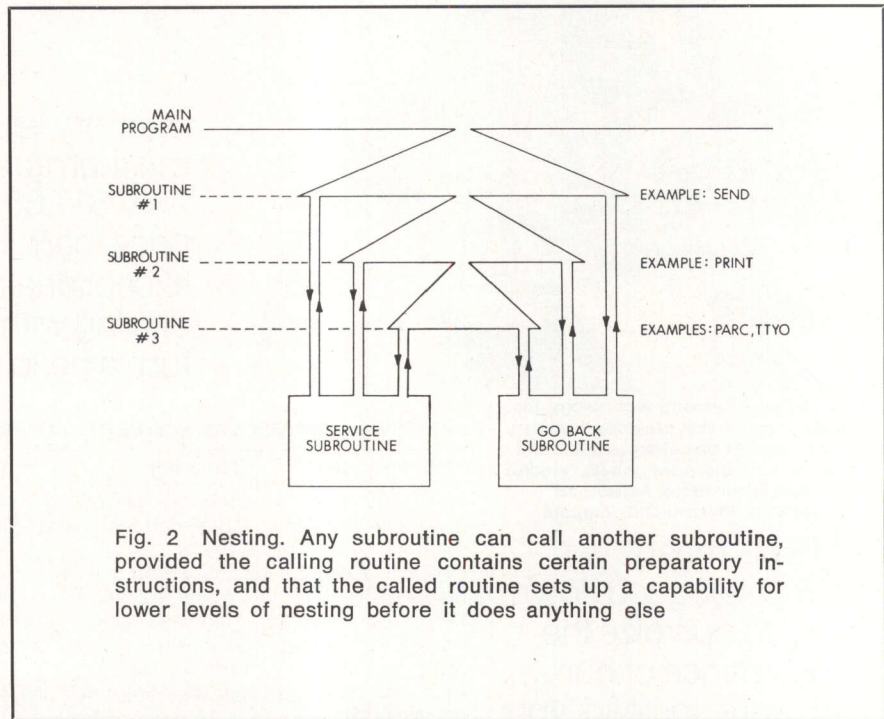


Fig. 2 Nesting. Any subroutine can call another subroutine, provided the calling routine contains certain preparatory instructions, and that the called routine sets up a capability for lower levels of nesting before it does anything else

address for the stack register contents. Load Immediate Hex (LI H'40') (see Table) places the hexadecimal number 40 in the accumulator, and Load Register 0 from Accumulator (LR 0,A) transfer it to scratchpad location 0. Then, the jump itself, which is the execution of a Push Immediate (PI) instruction,

automatically moves the contents of the program counter into the stack register and puts the address of the start of the subroutine—operand SUBN—into the program counter. SUBN, of course, will be a number assigned when this symbolic-language program is assembled into machine code.

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Two-Level Nesting

MAIN	SERV	GOBA	SUB1	SUB2
INSTR	LR A,0	LR A,0	LR K,P	LR K,P
INSTR	AI H'FF'	LR IS,A	PI SERV	PI SERV
LI H'40'	LR IS,A	LR A,13		
LR 0,A	LR A,KL	LR KU,A	INSTR	INSTR
PI SUB1	LR 14,A	LR A,12	INSTR	INSTR
	LR A,KU	LR KL,A	INSTR	INSTR
INSTR	LR 12,A	LR A,IS	PI SUB2	PI GOBA
INSTR	LR A,IS	INC		
INSTR	LR 0,A	LR 0,A	INSTR	LR P,K
	POP	POP	INSTR	POP
			INSTR	
			PI GOBA	
			LR P,K	
			POP	

Gaps in listing indicate where each routine stops to wait for a subroutine execution; actual instructions at these points are consecutive

What the Subroutine Must Do

To permit nesting, the first instruction in the subroutine must save the contents of the stack register. It does this with a Load Register instruction (LR K,P), which moves the stack register contents to the K register (actually scratchpad locations 11 and 12). This number, which is the return address in the main program once the subroutine is completed, cannot stay in K, because if a lower-level subroutine is called in, it will also clear the stack register in the same way. Therefore, the second instruction in the subroutine calls on the special sequence SERV, which transfers this number to the high end of the scratchpad, in a location defined by the contents of scratchpad 0—the number placed there by the main routine or by SERV itself at the start of the previous-level subroutine.

This sequence first loads the accumulator with the contents of scratchpad location 0, decrements it by 1, and moves the result to ISAR (LR IS,A). If the jump to the sub-

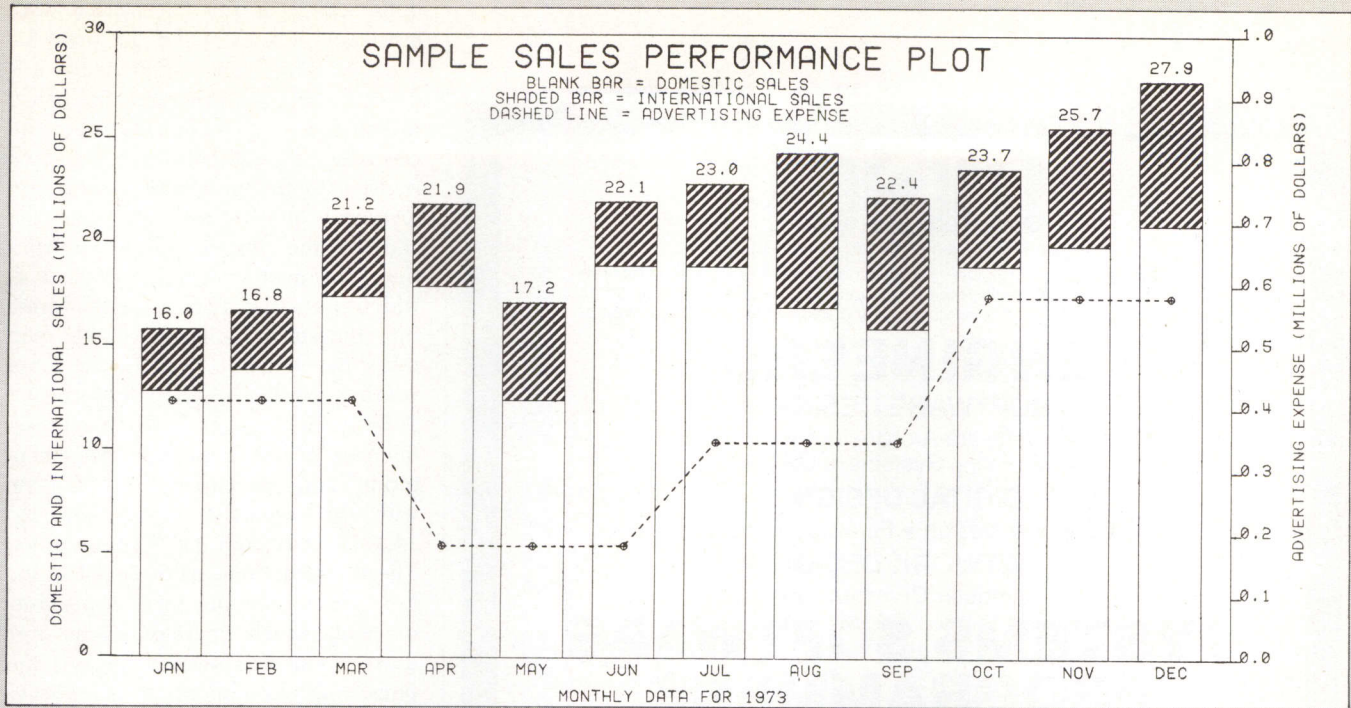
routine is from the main routine, location 0 will contain the hex number 40. The decrementing instruction is Add Immediate Hex FF (AI H'FF'), which adds the binary number 1111 1111 to the contents of the accumulator—equivalent to subtracting 1. Thus, at the first level, ISAR contains the hex number 3F, which is the address of the last scratchpad register. Now, with a series of four Load Register instructions, the original contents of the stack register, which were temporarily moved into scratchpad registers 12 and 13, are moved again via the accumulator into scratchpad registers 63 and 62, steered by ISAR. In these instructions, KU and KL refer to the high- and low-order bytes of K, while designations 14 and 12 are codes that, respectively, cause ISAR to be decremented and remain unchanged. They look like scratchpad locations but are not; locations are specified by the contents of ISAR. Thus instruction LR-14,A transfers a byte from the accumulator to the scratchpad location specified by ISAR, and then decrements the contents of ISAR; two steps

later, instruction LR 12,A again transfers a byte in the same way, but leaves ISAR unchanged. Thus, after the transfer, ISAR contains hexadecimal digits 3E, having been decremented twice. Two more Load Register instructions restore the address to location 0, again via the accumulator. Finally, the POP instruction restores the contents of the stack register to the program counter, so that the subroutine can begin in earnest.

This subroutine, executing its assigned task, can jump to a lower subroutine if necessary, without taking the preliminary steps required of the main routine, because the Service sequence has already modified the contents of scratchpad register 0. However, every lower-order subroutine must begin with the same two instructions—LR K,P and PI SERV. Again, these temporarily store the stack register in scratchpad locations 11 and 12, and again, the Service sequence first decrements the contents of location 0 and puts the result in ISAR. However, because this is a lower-level routine, the decrementing changes 3E to 3D and moves the stack register contents into scratchpad registers 61 and 60.

Going Back to the Main Routine

Every subroutine, at whatever level, ends with three specific instructions: PI GOBA; LR P,K; and POP. GOBA is essentially the reverse of the Service sequence. It obtains the most recent program address from the high end of the scratchpad, places it in register K, and increments the pointer in scratchpad 0. Two Load Register instructions transfer the contents of scratchpad location 0 into ISAR via the accumulator. This identifies the location of the address, which, in turn, is the point in the main routine or the higher-level subroutine to which the machine is now returning. Four more LR instructions make the transfer into K; one of them—LR A,13—automatically increments ISAR. Then ISAR is moved into the accumulator and incremented. (The F-8 instruction set includes an Increment Accumulator but not a Decrement Accumulator; that is why



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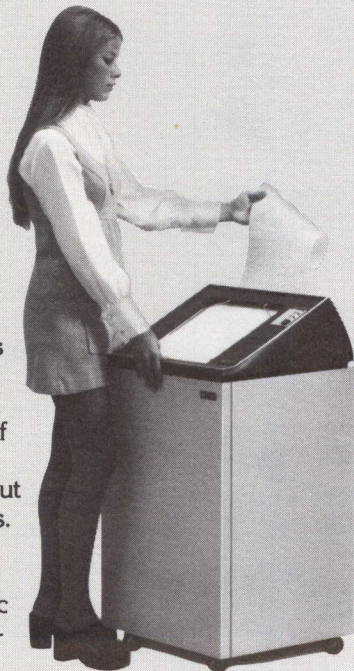
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GOBA can use the instruction INC, but SERV has to make do with AI'H'FF'.) This new scratchpad address, having been incremented twice, is returned to location 0, and POP restores the contents of the stack register to the program counter, returning GOBA to a point near the end of the just-completed subroutine. The next instruction is LR P,K, which puts the real return address into the stack register. Another POP takes the machine back to the main routine or the higher subroutine.

Both Service and Go Back sequences utilize automatic decrementation and incrementation of ISAR, with the respective instructions LR 14,A in SERV and LR A,13 in GOBA. These instructions, as designed in the F-8, affect only the three lower bits of ISAR, which operates as an up/down counter. However, in this application, the updating is always even-to-odd when incrementing and odd-to-even when decrementing, which means that these instructions affect only the least significant bit of ISAR. The real updating, which can include carries through all six bits of ISAR, is executed by instructions AI'FF' and INC. These actually update the accumulator, but at the moment they are being executed, the contents of ISAR are passing through the accumulator en route to or from temporary storage.

For example, suppose a fourth-level subroutine is being executed and a call is made to a fifth level. At the beginning of SERV, register 0 contains H'38', which is binary 0011 1000. This is decremented by AI'FF' to H'37', or binary 0011 0111; part way through SERV, it is decremented again by LR 14,A to H'36', or binary 0011 0110. The second change affects only the last bits; the first one affects the last four bits. A similar process applies in GOBA.

Regardless of the number of nested levels, the amount of added software is minimal. Service and Go Back sequences are executed in 38 and 35 μ s, respectively, when the clock frequency is 2 MHz, including call and return. The same technique can be applied to store in the scratchpad, along with the return address, any additional information, such as the contents of the status register, special counters, or other processor data. □



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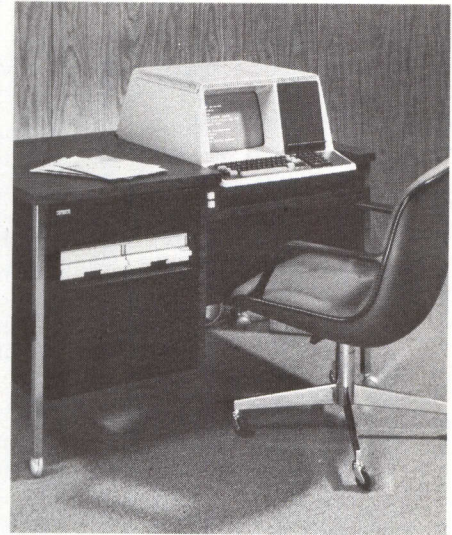
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Computer Interfacing¹: Anatomy of a Microcomputer

David G. Larsen

Virginia Polytechnic Institute
& State University

Jonathan A. Titus

Tychon, Inc

Peter R. Rony

Virginia Polytechnic Institute
& State University

A typical microcomputer system, such as that illustrated in the Figure (based on the Intel 40-pin 8080 microprocessor chip), possesses all of the minimum requirements for a computer. That is, it can input and output data; it contains an arithmetic/logic unit, located within the chip, that performs arithmetic and logical operations; it contains "fast" memory (speed is an important requirement for a functional computer); it is programmable, with the data and program instructions capable of being arranged in any sequence desired; and it is digital. The Figure shows the important data paths within the microcomputer.

Memory

Let us first consider the data communication between central processing unit (CPU) (also known as an MPU) and memory. Some definitions^{2,3} will be useful in the ensuing discussion:

Memory—Any device that can store logic 0 and logic 1 bits in such a manner that a single bit or group of bits can be accessed and retrieved

Memory Cell—A single storage element of memory

Memory Word—A group of bits occupying one storage location in a computer. This group is treated by the

computer circuits as an entity, by the control unit as an instruction, and by the arithmetic unit as a quantity. Each bit is stored in a single memory cell

Memory Address—Storage location of a memory word

Memory Data—Memory word occupying a specific storage location in memory, or the memory words collectively located in memory

Random-Access Memory (RAM)—A semiconductor memory into which logic 0 and logic 1 states can be written (stored) and then read out again (retrieved)

Read-Only Memory (ROM)—A semiconductor memory from which digital data can be repeatedly read out, but cannot be written into, as is the case for random-access

Programmable Read-Only Memory (p/ROM)—A read-only memory that is field programmable by the user

Volatile Memory—In computers, any memory that can retain information only as long as power is applied to that memory; opposite of nonvolatile memory

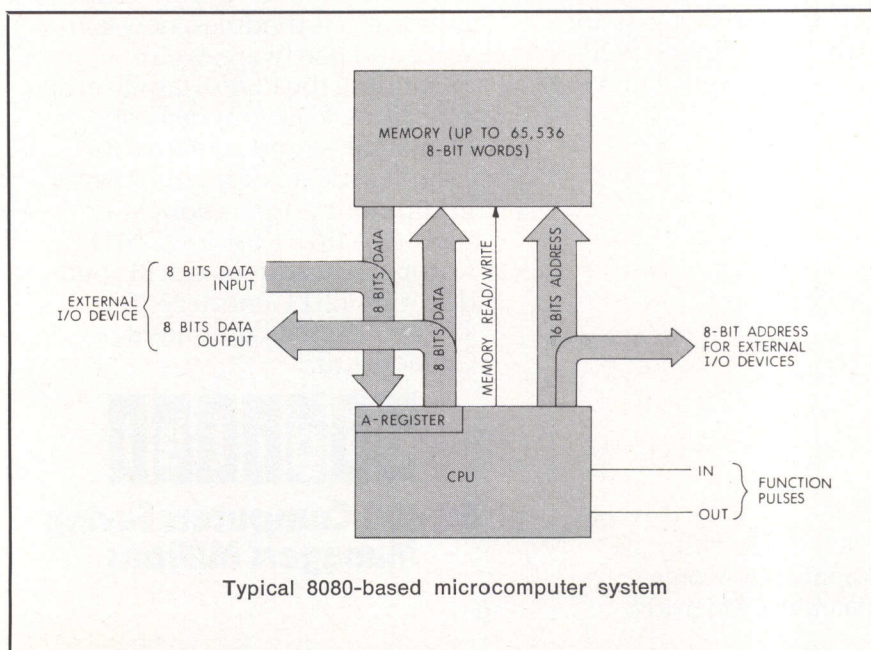
Read—To transmit data from a semiconductor memory to some other digital electronic device; this term also applies to computers and other types of memory devices

Write—To transmit data into a semiconductor memory from some other digital electronic device; this term also applies to computers and other types of memory devices. A synonym is *store*

The 8080 microprocessor employs 8-bit words that are stored in memory with the aid of a 16-bit memory address bus. By quick calculation, we can conclude that there exist 2^{16} , or 65,536 different memory locations that can be accessed by the microprocessor. This access to memory is direct, which means that no digital electronic gimmicks need be applied to access any given memory location within the 65,536 possibilities. Forty-pin integrated circuit (IC) chips do have their advantages, and this is one of them. Total memory capacity of the microprocessor is 64K—far more than required for most applications, but in reserve if needed.

Data are transferred between CPU and memory over 8-bit input and output buses, both of which are depicted in the Figure. By "input," we mean "input into the CPU"; "output" is defined in a similar fashion. The point of reference is always the CPU; data

This article is based, with permission, on a column appearing in *American Laboratory* magazine.



Now you can "see" inside your 8080 with the Ramtek MM 80

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RAMTEK's new MM 80 In Circuit Emulator plugs directly into a 8080 microprocessor socket with its own 8080, giving you complete system access through a full complement of console commands, front panel controls, probe points and displays. With the MM 80, you actually "see" what's going on inside the system you're working on.

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The programmer can step, trace and breakpoint the software in the real system, and display and alter the 8080 registers, memory and I/O ports . . . all without special programs in the user system or special user hardware. In fact, the user programs can all be in ROM and the MM 80 will still let you see inside.

Real-time debugging is a cinch. The MM 80 holds the addresses of your last 255 instructions on tap for you, and real-time halts can occur on both memory and I/O references.

For those really heavy software efforts, the MM 80 options include a ROM resident one pass assembler, so you never have to load the assembler—and the source is only loaded once. The editor is ROM resident, so it never needs loading. And the PROM emulator and PROM programmer mean that

error correction is a breeze.

The MM 80 provides a complete control and test center for any system under test. Five scope probe points let you trigger on M1, sync, $\phi 1$ and $\phi 2$ signals, and specific address references. RAM diagnostic programs and ROM checksum computation is provided. And the LED display provides complete processor status information, so problems can be detected the moment they arise.

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The RAMTEK MM 80 is available now from Texas Instruments Supply.

leaving it are always output data, while data entering it are always input data.

Note in the Figure that the input and output data are transferred between *accumulator* and memory. Although this is frequently the case, a more detailed look at the chip will reveal that data stored in memory are transferred to other internal *registers* within the chip as well. The most obvious is the *instruction register*, from which decoding of the instruction occurs. Other registers, known as *general-purpose registers*, are classified by the letters B, C, D, E, H, and L. The accumulator register is the heart of the entire microcomputer. Arithmetic and logic operations are always performed to or on the eight bits of data present in the accumulator. All input and output data pass through it with the aid of two computer instructions, called *IN* and *OUT*.

Between CPU and memory there exists a single output line called memory *READ/WRITE*. When this line is at logic 1, you can *READ* data into the CPU either from memory or an external device. When the line is at logic 0, you can *WRITE* data from the CPU into memory or external output device.

Any type of "fast" digital electronic memory device can be employed (RAM, ROM, or p/ROM). What do we mean by fast memory? Simply that it can perform a read or write operation during a single microcomputer instruction. A typical 8080 microcomputer system operates at a clock rate of 2 MHz, and a read or write operation takes 3.5 μ s. Thus RAM, ROM, and p/ROM each need an access time of about 1 μ s to allow full advantage to be taken of the maximum clock speed. Slower semiconductor memories can be used, but the microcomputer has to "wait" while a read or write operation takes place.

Data Output

The 8-bit output bus between CPU and memory also serves as the output data bus to an external output device. If output to an external device is to be provided, several important points should be remembered: the specific output device that will receive eight bits of data from the CPU must be selected, availability of output data on the output data bus must be indicated to this device, and the device must capture the output data within a very short period of time, typically 0.5 μ s.

The third point is perhaps the most important. Keep in mind that the microcomputer is operating at a 2-MHz clock rate, and each computer instruction is executed in 2 to 9 μ s. Thus accumulator data designed as output data to an external device are not available for very long, and must be captured while available.

Data Input

The basic considerations that apply to data output apply to data input into the CPU from an external input device. That is, the specific input device that will transmit eight bits of data to the CPU must be selected, it must be indicated to this device when the CPU is ready to acquire the input data, and care must be taken that the CPU acquires these data within a very short period of time, typically 0.5 μ s.

Input/Output Device Addressing

The 16-bit memory address bus is time-shared so that it can provide, at certain times, an 8-bit device identification number called a *device code*. Eight bits of information allow decoding of 2^8 , or 256 different devices. When used in conjunction with two output function pulses (*IN*, *OUT*), the microcomputer system can address 256 different input and 256 different output devices. (A "device" can be a complex machine such as a teletypewriter or cathode-ray tube display, or a simple, single IC chip.)

Microcomputer Interrupt

Not included in the Figure is a single input line to the microcomputer that generates a program *interrupt* during microcomputer operation. This would be generated by an external device that is instructed to transfer data to or from the computer.

Summary

Microcomputers are fascinating machines. They are small and relatively inexpensive, so that a user is less likely to be intimidated by them. They are far simpler than their mini-computer and computer counterparts and can be readily repaired by the simple process of chip substitution.

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3. J. Blukis and M. Baker, *Practical Digital Electronics*, Hewlett-Packard Co, Santa Clara, Calif, 1974

Microprocessor Software

Intel 8080/8008 • Intel 4040/4004 • Motorola 6800 • Fairchild F8 • Signetics 2650

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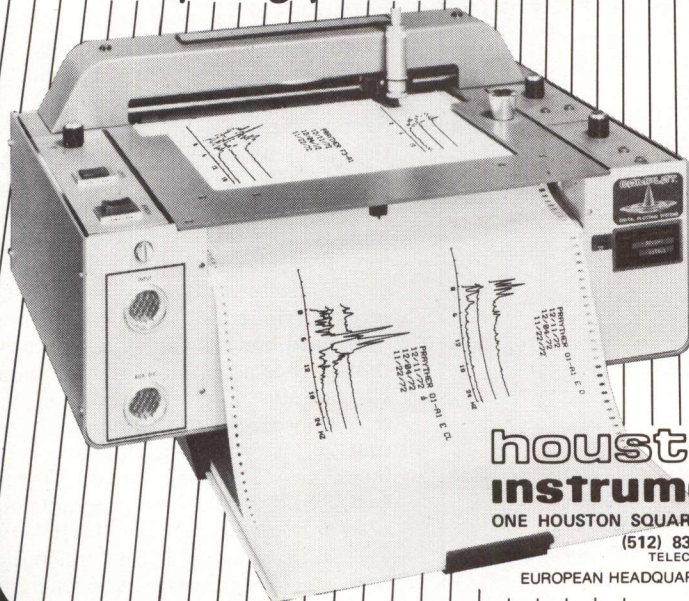
These programs are well commented, modular and fully documented. A manual and source listing accompany each program. The Assemblers are priced at \$800 and the Simulators are priced at \$650.

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1-Chip Microcomputer Offers Many Powerful Features at Low Cost

Claiming to have solved the random-logic testing problem at the chip and board levels, Zilog, 170 State St, Suite 260A, Los Altos, CA 94022 has introduced as its first product the Z-80 microcomputer. The component set includes all logic circuits necessary for building high performance microcomputer systems with virtually no external logic, and a minimum of inexpensive, static or dynamic memory components.

Heart of the microcomputer is a single-chip, n-channel processor. It is a 40-pin metal-oxide semiconductor (MOS) device, with 158 instructions, including those of the Intel 8080A plus software compatibility with it; 17 internal registers; direct indexing; relocatable software; and three fast interrupts. All of this is available on the one chip for approximately the price of the Intel 3-chip set (8080A, 8224 clock, 8228 control).

Also featured are built-in refresh for dynamic memory, 1.6- μ s machine cycle time, and a single 5-V power supply and single-phase TTL clock.

TTL-compatible data and address buses are driven by 3-state circuits. In addition, 25 to 100% better throughput and 25 to 50% less memory than the 8080A provide considerable bottom-line savings.

The chip, though slightly larger in size, contains twice the number of transistors that others do. This is achieved through use of depletion-rather than enhancement-mode n-MOS, which requires only 5 V.

Interface and Control Circuits

Parallel and serial input/output (PIO, SIO) programmable controllers allow for direct interface to a wide range of parallel/serial interface peripherals, without other external logic. Real-time events are controlled by four independent, programmable timer circuits—all contained in a single circuit.

A programmable, direct memory access controller can directly transfer data between the SIO or PIO and memory on a central processing unit (CPU) cycle-steal basis. All controllers have built-in nested priority interrupt control and fast interrupt response capability (up to six times faster than the 8080A). In addition,

the controllers monitor peripheral status to eliminate any type of CPU polling.

Hardware/Software Development System

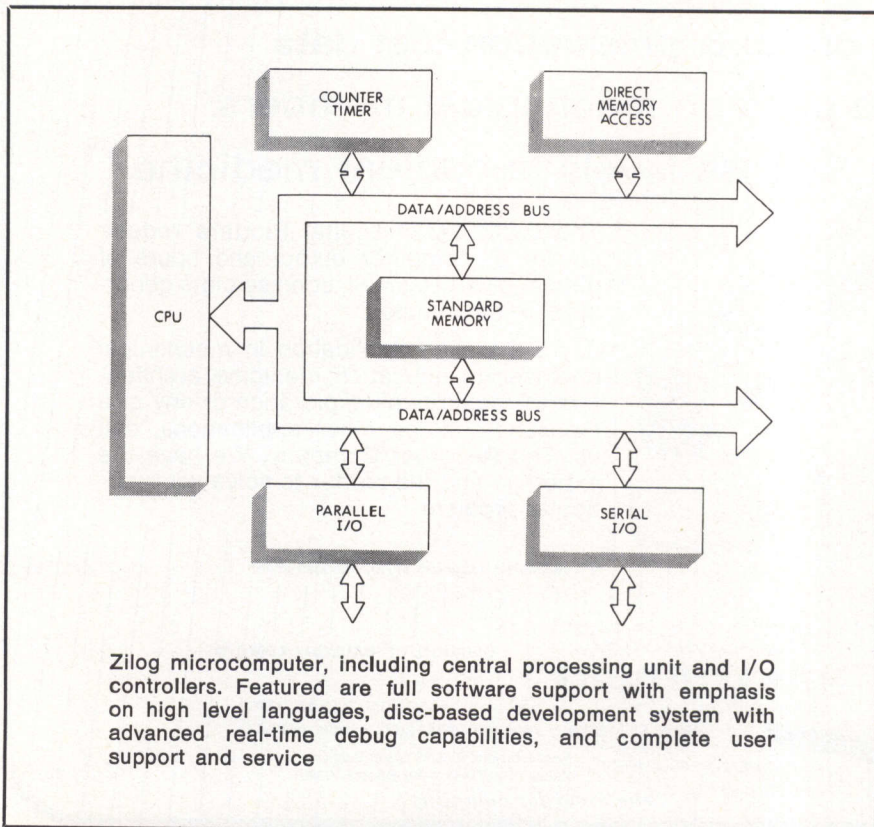
A standalone, floppy-disc-based system, which features advanced, real-time debug capability, is based on random-access memory (RAM) rather than on programmable read-only memory (p/ROM), for fast program development. Constant memory diagnostics are performed in background mode; system diagnostic software is provided for rapid fault isolation. Full resident software includes ROM-based Executive, RAM-based assembler and text editor; disc operating system with file maintenance; real-time debug software; and resident Basic compiler. Offline software support includes assembler, simulator, compiler, and test pattern generation.

External ROM, RAM, or p/ROM can be substituted for system RAM at any time. Flexible structure permits interchangeability of the user's prototype elements with Z-80 elements to simplify user hardware debug. Complete hardware/software interface support is provided for a wide range of high speed peripherals.

Availability

Samples are being made available this month; by April, components may be obtained off the shelf.

Circle 170 on Inquiry Card



Microcomputer Kit Developed for System Design and Prototyping

Claimed to be the "most versatile microcomputer system design kit available to date," the MCS-80, offered by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, is based on the company's 8080A central processing unit (CPU) group and programmable large-scale integration (LSI) input/output (I/O) blocks. The latter allow the system to control and communicate with a number of different peripherals.

In addition to the microprocessor, the ready-to-assemble, preprogrammed kit contains a clock generator, system controller, programmable communications and peripheral interfaces, two 1-out-of-8 binary devices, two 8K erasable programmable read-only memories (p/ROMs), two 1K static random-access memories, and a clock crystal. Also included are a printed-circuit (PC) board, connectors, all necessary discrete com-



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Intel Corp's MCS-80 micro-computer system design kit. All necessary components are included to build a complete 8080A-based system. The board also provides area for system expansion and for custom interfacing

ponents, system monitor program, 8080 system user's and programming manuals, and PL/M programming manual.

Although developed primarily for system prototyping by equipment designers, the kit is also suitable for other users. Its PC board contains pre-drilled areas for system expansion; eg, one area provides 12 in.² for wirewrapped connectors, which may be used to customize interconnections to devices such as analog-to-digital converters and modems. Space also is provided for further memory and I/O expansion with standard components.

The CPU group, consisting of CPU, clock generator, and system controller, defines the system bus and makes all CPU inputs asynchronous in nature, in addition to providing all central logic and interface functions. Features built into the group include crystal-controlled transistor-transistor logic and metal-oxide semiconductor (MOS) clocks, auxiliary timing functions, power-on reset, system bus control, single-level interrupt control, and bidirectional bus drive. The CPU is an n-channel silicon-gate MOS, 8-bit parallel processor with an instruction cycle time of 2 μ s. Clock generator and system controller are Schottky bipolar LSI devices.

Virtually any types of peripherals and serial data communications links can be operated though the two programmable LSI blocks. The programmable communications interface operates as a receiver/transmitter and implements all presently used serial communications protocols, including synchronous, asynchronous, and IBM Bi-Sync. The programmable peripheral interface has 24 I/O lines, which operate in over 40 software-selectable configurations. It is used to interface display, printers, read-

ers, keyboards, motor drives, and other peripherals.

System monitor "firmware" in one p/ROM provides a general-purpose system operating program to facilitate design evaluations and tests. The second p/ROM can be used to develop specialized applications programs, operating either in conjunction with the system monitor or independently. An extensive collection of applications programs is available to members of the company's users' library.

The three manuals contain about 600 pages of information on system design methods, programming, applications, and MCS-80 system components. The two programming manuals cover both MCS-80 system programming approaches: macro assembly, and high level software design with Intel PL/M, a high level programming language for microcomputers.

Circle 171 on Inquiry Card

μ Computer Bus Structure Permits Easy Addition of Options, Peripherals

Although presently configured about an Intel 8080A 8-bit microprocessor, the MM1 microcomputer includes provision for future use of a 16-bit central processing unit (CPU). Capable of operating totally independent of other computers or time-sharing ties, this system contains a microprocessor unit, programmer's console, utility software, and peripheral options. Full program development can be performed on the plug-in console.

Included in the system, made by Control Logic, Inc, 9 Tech Circle, Natick, MA 01760, are UV-erasable

programmable read-only memory (p/ROM) in 1K increments up to 4K; optional 1K random-access memory (RAM) with provision for RAM battery backup power; optional 8-level, vectored priority interrupt; and program-controllable systems reset. Option boards provide real-time clock with crystal-controlled interval times (256 possible intervals selectable by software control); choice of current loop or EIA RS-232-C compatible serial interfaces; and parallel transistor-transistor logic input/output (TTL I/O) up to 32 bits.

Intel 2708 p/ROMs are used in 1K increments up to 16K on each memory board. Access time is 450 ns. By pairing boards, the memory system can be 16 bits wide. The RAM is expandable in 1K increments to 4K on each board and can also be paired. Cycle time is also 450 ns.

The programmer's console provides direct memory and register examine/modify, octal numeric format display of both address and data, automatic address relocation, indirect addressing for data displays, and I/O simulator with 16 ports. An optional maintenance memory module includes add-on memory with four ZIF sockets for diagnostic p/ROMs.

A single Poly-BussTM printed-circuit board is used for all interprocessor, memory, and I/O interface wiring. Standard versions contain space for either five or ten boards. Specially packaged systems can mount the bus board on any suitable surface, such as in a NEMA enclosure. Addition of bus boards, extension of the bus board, or ribbon cable connection to peripherals is accomplished via board sockets.

A system monitor/debugging program has examine/modify memory locations, processor flags, and registers. Contents of memory are listed in octal format. Direct input/output is provided to specified I/O device number. A general-purpose text edit-



Programmer's console for MM1 micro-computer. The desktop unit plugs into the computer's "Poly-Buss." Controls include reset, run, halt, cycle step, instruction step, and interrupt enable/disable

ing program allows insertion, deletion, or changing of lines of text or characters within a line; locating lines containing key words; and list or punch of text on high or low speed punch.

Three-pass type assemblers are in absolute and relocating versions. Included are data statements for single- and double-precision fixed point constants and text, external symbols and entry lines, and user-modifiable symbol table.

The software package also includes cross-assemblers, loaders, disc operating systems, and a FORTRAN IV compiler. Multiple peripherals such as printers, floppy discs, magnetic and paper-tape units, and CRT display/keyboards are available.

Circle 172 on Inquiry Card

User-Oriented μ Computer Also Functions as Assembler/Simulator

Configuration of the ASC-4040MC can be as either a conventional microcomputer or an assembler/simulator software development system. The basic microcomputer, made by Automated Computer Systems, 2361 E Foothill Blvd, Pasadena, CA 91107, contains five functional plug-in modules that are interconnected through a 15-slot motherboard card rack assembly housed in an air-cooled cabinet. Module boards include a 4040 central processing unit; combination 2-kilobyte programmable read-only memory (p/ROM)/1280-word data random-access memory (RAM)/16 buffer output port; 8-port, 3-state universal input/output (I/O) with handshaking capabilities; and full computer control/hex display panel. There is also a plug-in switching regulated power supply module. Spare connectors for user custom expansion by either additional basic functional modules or standard module options are included on the motherboard.

Standard module options include a 4-kilobyte read/write (R/W) program memory, combination ASR-33 TTY and RS-232-C modem interface, a 64 x 4-bit input channel multiplexer, 1702A p/ROM programmer, and universal wirewrap boards for mechanizing user custom logic. RAM options include storage expansion in 80-word and/or 1280-word increments, to a maximum of 2560 words. p/ROM-ROM program options include storage expansion in 256-byte, preprogrammed integrated-circuit increments and/or 2- or 4-kilobyte p/ROM-ROM printed-circuit board in-



crements to a maximum of 16 kilobytes. RAM R/W program options include storage expansion by 4-kilobyte increments to a maximum of 16 kilobytes. I/O options allow up to 32 I/O ports configured by the user, either as 32 unidirectional input or output ports in any combination or as 32 bidirectional time-share I/O ports.

Circle 173 on Inquiry Card

μ Processor Development Aid Offers Mini Flexibility

The μ Pro-80 microcomputer, made to support the Intel 8080 microprocessor, is designed to provide all of the flexibility of a minicomputer. Announced by μ Pro Associates, 10340 Bubb Rd, Cupertino, CA 95014, it is totally self-contained, requiring only the addition of a terminal to become operational. Also, it includes its own software package.

A removable console permits machine control and status monitoring; this function uses no memory space, input/output device assignment, interrupt, or special software. All features of the 8080 are available to the user's system.

The front-panel console offers, in addition to all common control functions, both breakpoint and program trace capabilities. Register and memory contents are displayed in hexadecimal form on the front panel itself, eliminating the need for a peripheral device. Small size (4.6 x 6.6 x 3"), modularity (simply unplugs from the main system), and transparency (does not utilize user



memory space, device addresses, or interrupts) make the console a convenient debugging and field service tool. An option to the basic system converts it into an in-circuit emulator.

A powerful Assembly language, available in both resident and FORTRAN cross-assembler versions, features block structure, relocatability, and macro definitions. During assembly, it provides comprehensive syntax error messages and symbol cross-reference tables.

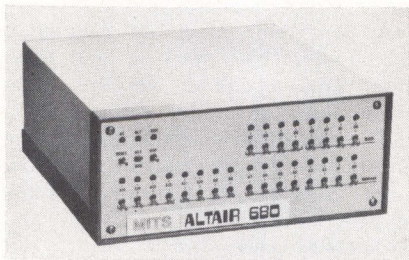
Circle 174 on Inquiry Card

Lower-Power μ Computer Maintains Reliability While Reducing Cost

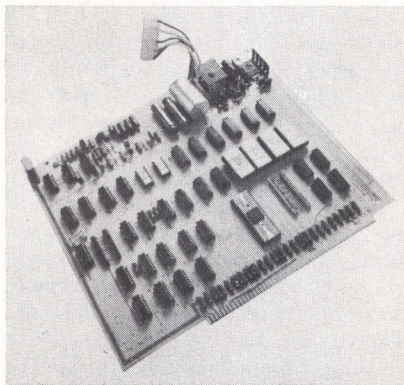
Not quite as powerful as the earlier 8800 but selling at "less than half the price of a similar system," the Altair 680 microcomputer—based on the M6800 microprocessor available from Motorola and American Microsystems—has been introduced by MITS, Inc, 6328 Linn, NE, PO Box 8636, Albuquerque, NM 87108. The package measures 11 $\frac{1}{16}$ x 11 $\frac{1}{16}$ x 4 $\frac{11}{16}$ "—less than one-third the size of the earlier unit. Three configurations are available: a fully user-programmable system with complete front-panel controls, and two versions for dedicated program applications.

Almost all of the circuitry, including memory and a built-in input/output (I/O) port, is on a single printed-circuit (PC) board. Power transformer and control switches (depending on the configuration) are the only other components in the case. A full front-panel model contains all controls necessary for addressing and entering data besides those for controlling the processor itself; it also contains an additional PC board with all of the logic circuitry necessary to reset, halt, or start the processor, as well as switches and LED indicator lights for each of the 16 address lines and eight data lines. There is no need for a wiring harness since the second PC board mounts on the main board via a 100-contact edge connector. A power switch is contained on the unit's back panel. Two turnkey models have no front-panel controls, except one for restarting the processor. A fourth configuration, for use inside another machine or for the experimenter, consists of only the main PC board and its components, with no power supply or controls.

The 8-bit parallel microprocessor uses a bidirectional data bus and a



Fully user-programmable version of the MITS Altair 680 microcomputer. Front-panel assembly contains switches for 16 address lines and eight data lines, and an indicator light for each switch. In addition, it includes a run/halt switch with an LED indicator for each position of that switch, reset and deposit switches with no indicators, and an indicator for the ac power switch which is located on the back panel of the unit. Dedicated-program versions, in which most functions are handled by ROM or p/ROM, contain only ac power and reset switches



Altair 680 main PC board. M6800 micro-processor, memory, and I/O port plus associated circuitry are on this one card. Power and control must be supplied by system with which the micro-computer is associated

16-bit address bus that provides the capability to directly address 65 kilobytes of memory. Its instruction set consists of 72 basic instructions out of a possible 256 codes. (The remaining 59 possible codes are unassigned.) Cycle time is 4 μ s.

There are seven different addressing modes, with the particular mode being a function of both the type of instruction and the actual coding within the instruction. These modes are 1-byte instruction accumulator addressing, specifying either of two accumulators; 2- or 3-byte immediate addressing; 2-byte direct addressing;

3-byte extended addressing; 2-byte indexed addressing; 1-byte implied addressing; and 2-byte relative addressing.

Basic memory for the unit is on the main PC board. Included are 1024 bytes of random-access memory (RAM) and provisions for another 1024 bytes of read-only memory (ROM) or programmable ROM (p/ROM). RAMs are 2102-type 1024 x 1 bit, ROMs are custom ordered, and p/ROMs are 1702-type UV-erasable 256 x 8-bit units. Additional memory, available at a future date, may add as much as 12 kilobytes.

An I/O port and appropriate interface circuitry, on the main PC board, may be configured for RS-232 or for 20- or 60-mA current loop Teletype[®] (TTY) levels. Since the microprocessor uses address to refer to I/O as well as memory, a large number of separate devices can be operated. (Additional I/O interfaces are now in development.)

Necessary 5-V power is supplied from a power transformer through a conventional bridge rectifier, filter capacitors, and voltage regulator integrated circuit. A 32-V winding on the transformer generates unregulated ± 16 V required for a TTY interface, and a -16-V line feeds to four zener-diode-regulated outputs to provide four -9-V lines for the p/ROMs. If required, a cooling fan can be installed.

Optional software includes p/ROM monitor, assembler, debug, and editor.

Prices for the full front-panel model are \$345 for a kit, \$420 for an assembled unit. The microprocessor board alone sells for \$195 in kit form, \$275 assembled.

Circle 175 on Inquiry Card

Time-Sharing Service Helps Develop Microcomputer Programs

NEC Microcomputers, Inc, 5 Militia Dr, Lexington, MA 02173 has made available a worldwide time-sharing network for developing and simulating programs for any Intel 8080A microcomputer system. The service provides four programs, including a macro library, to aid in writing, assembling, debugging, simulating, and generating paper-tape output of programs that run on NEC's μ COM-8

microprocessors and memories, and on compatible products of other companies.

Key feature of the programs, which are stored on and accessed through the General Electric Co Mark III time-sharing network, is the Macro Maintenance Program. It includes a library of basic macro routines in addition to allowing developers to build, store, and maintain their own 8080A macroinstructions; each macro consists of several symbolic instructions.

The remaining programs include μ COM*8A Assembler—a macro assembler that translates 8080A symbolic source code instructions into binary machine code; μ COM*80 Output Program, which reformats the binary machine code object program into hex, BNPF, or NROM paper-tape format so that the code can be punched into a paper tape on the user's terminal; and μ COM*8S Simulator, which allows interactive debugging of the object-level program, giving developers a second opportunity to test the program before it is made part of a microcomputer system. Circle 176 on Inquiry Card

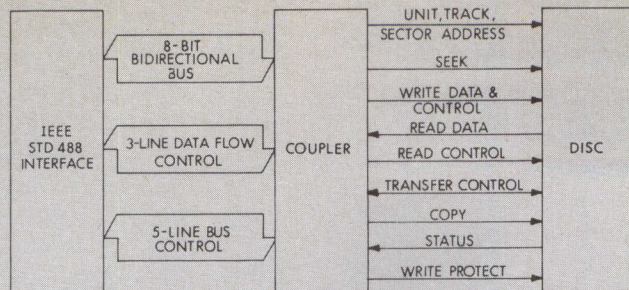
High-Level Language, Compiler Developed for M6800 Applications

Suited for constructing programs that contain mathematical computations and data manipulations, MPL[™] has been introduced by Motorola Semiconductor Products, Inc, PO Box 20294, Phoenix, AZ 85036. Source programs written in the language—a subset of PL/I—are translated by a compiler (available through the General Electric Co Mark III Information Services International Network) into M6800 assembly language (rather than machine code). Additionally, the compiler checks for source program errors and produces appropriate diagnostic error messages. Optimization of memory space and execution speed for program segments that involve input/output hardware elements may be accomplished with assembly-level subroutines embedded in the program.

Circle 177 on Inquiry Card

Flexible Cartridge Disc for Use with IEEE Standard Interface

Model 488, from Process Dynamics Inc, 2517 Hiway 35, Manasquan, NJ 08736, provides low cost mass stor-



Model 488 flexible cartridge disc system developed by Process Dynamics is fully compatible with IEEE standard interface for Programmable Instrumentation Standard 488

age for systems using the Institute of Electrical and Electronics Engineers (IEEE) Standard 488 digital interface for programmable instrumentation. Switch-selectable talk and listen addresses permit easy connection into any system.

The controller, which mounts above the first drive, accommodates up to eight drives, each with a capacity of 270 kilobytes/cartridge. The flying head, non-contact drive and fully enclosed cartridge provide maximum reliability and life for the device and media.

The only commands used in control of the disc are Read, Write,

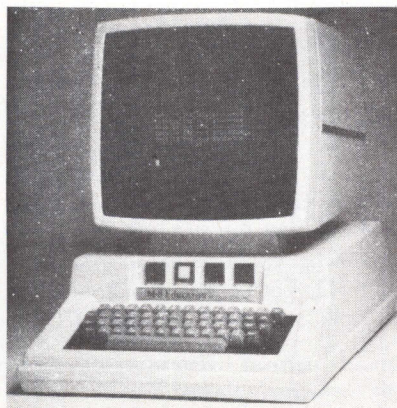
Finished, Copy, Protect, and Enable. Copy allows one sector to be copied to another without going through the controller or processor. Sequential sectors may be accessed without re-addressing, permitting up to a full platter to be transferred. A sector-sized buffer enables the disc to be connected directly to other devices or instruments on the bus whose transfer rates may vary from 1 to 300,000 bytes/s.

The unit may be desktop style or rack-mounted. Write protect and CRC are standard options.

Circle 178 on Inquiry Card

Single-Unit System Provides All Functions for Program Development

Comprising a communications terminal and a Fairchild F-8 microprocessor module in one unit, the M-8 Educator from Technical Communications, Inc, PO Box 306, Olathe, KS 66061 is capable of performing all functions essential for program development. Standard on all units are a 53-key, solid-state (Hall-effect) keyboard terminal, 64-character/31-line CRT display, 110-baud Teletype™.



compatible serial input/output (I/O), 300- or 600-baud TTL-compatible serial I/O, and composite video output for use with an optional remote monitor.

The microprocessor module features a debug monitor with user-callable I/O subroutines, 2K random-access memory expandable to 32K, 2- to 8-bit TTL-compatible output ports (open-collector, 50-mA sink), 2- to 8-bit TTL-compatible input ports, parallel-entry port for high speed peripherals (150- μ s minimum character spacing), and rear-panel access to all bus structures and control lines. Firmware-resident assembler, cassette tape storage module, and programmable read-only memory programmer are available as options.

Circle 179 on Inquiry Card

Programming Language for M6800 Aids Software Development

Availability of PL/M6800™, a high level programming language for the Motorola M6800 microprocessor, has been announced by Intermetrics, Inc, 701 Concord Ave, Cambridge, MA

02138. According to a company spokesman, the language "is an effective aid to microprocessor software development, . . . brings the well-known benefits of high-level language programming to the field of microprocessor programming, . . . (and) cuts programming time and effort to a fraction of that required for assembly language, while allowing access to hardware features and assembly language procedures." He also claimed that by reducing the time and cost associated with microprocessor software development, PL/M6800 can give a "significant competitive edge" to companies developing products for the rapidly evolving microprocessor-based system market. The language encourages the use of structured programming techniques, and is self-documenting.

PL/M6800 has a 1-pass compiler which produces optimized object code in a format directly usable by the Motorola MINIBUG/MIKBUG and EXBUG Loader Function. The compiler includes a number of user-controlled features to enhance its utility, such as source program listing, object code listing, assembler code listing, and symbol table dumps.

The compiler is compatible with the PL/M language developed by Intel to program its line of microprocessors, and PL/M programs can be compiled with few, if any, changes, thus allowing a "significant degree of software portability."

Circle 180 on Inquiry Card

Macro Cross-Assembler Features Economy Over FORTRAN Packages

An assembler for the MOS Technology 6500 microprocessor which operates on both IBM S360/370 and DEC PDP-10 computers is written in assembly language in both cases and is claimed to be more cost-effective than competing packages written in FORTRAN. Developed by Zeno Systems, Inc, 2210 3rd St, Suite 110, Santa Monica, CA 90405, the assembler is functionally equivalent to manufacturer-provided software, with the additions of normal arithmetic expressions and a macro and conditional assembly capability. Other available enhancements include clear and extensive error diagnostics within the assembly listing and summarized in a separate file or at the user's terminal, optional variable cross-reference listing, and improved assembly listing format.

Circle 181 on Inquiry Card

PRODUCT FEATURE

Use of a microprocessor in the model 60 Microperipheral™ card reader/printer is said to eliminate much of the standard logic and therefore enable manufacture of a versatile but low cost unit. A Motorola M6800 microprocessor controls reading and printing functions to allow either local offline verification—just printing information already punched or coded on the card—or full duplex operation with a local or remote computer.

iCOM, Inc's combination punched/mark-sense card reader and printer is believed to be the first single unit produced that is capable of performing both functions, and is designed for use with virtually any 8- or 16-bit microcomputer or most minicomputers. It operates as both an input and an output device and will interface with standard I/O logic cards.

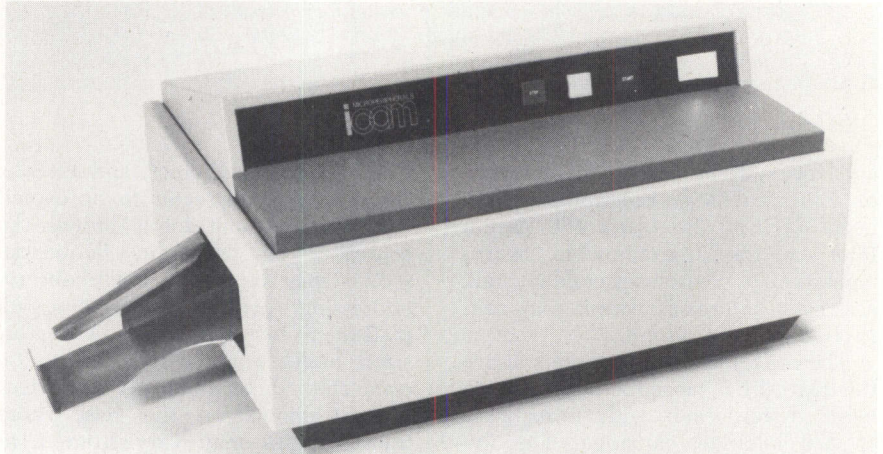
Operation

Standard 80-column cards can be hand-fed into the unit at a rate of 10/min. Cards may be punched or marked or both. For example, part of a card could be pre-punched and the balance formatted for hand marking.

Both input and output data formats can be either ASCII or EBCDIC. Input and output buffers are each 80 characters.

After a card passes through the read station, the upper edge of the card can be printed with up to 80 characters. Full duplex mode allows any one of 64 characters to be printed in each column regardless of the character punched or marked in that column. In offline verify mode the character punched or marked is printed at the top of each column.

When the card to be read is inserted by hand into the input slot, it is automatically positioned, under direction of the microprocessor, through the read station until all columns have been read. Then the card is passed laterally to the print



Single Unit Card Reader/Printer Serves as Low Price I/O Device

station where it waits momentarily for information that either was read from the card or is sent from the computer (if the unit is online). Once the card is printed, it passes through the exit gates into a 45-card hopper.

The time period required to read the card and pass it to the print station is 400 ms; a full read/print cycle requires 6 s max. An interlock prevents an operator from entering a new card while another card is being processed.

General Details

Design of the card track is such that a card passes from insertion completely through the unit in a straight line motion. This minimizes the possibility of a card jam or of errors in card processing if a damaged card is accidentally fed into the unit. Access to the card track is attained by tipping up the front panel; lifting the back panel allows complete access to the two printed circuit boards containing all the electronics.

The printer functions without a ribbon. As a card moves through the printer station, a hammer strikes it from behind and impresses it against a permanently inked roller that is in front of the card.

A general-purpose interface is provided in the form of 3-state, 8-bit parallel ports. Connection to individual 8-, 12-, 16-, or 32-bit computers will differ, but signal levels and timing are compatible with all popular minicomputers.

Size of the unit is 14 x 6 x 7"; weight is 20 lb. Power requirement is 115 Vac, 60 Hz.

Price and Delivery

Unit price for the model 60 in OEM quantities (100 or more units) will be between \$500 and \$600. Single units will sell for under \$1000. Delivery of small quantities is scheduled for March and full production quantities will be available by June. iCOM, Inc, 6741 Variel Ave, Canoga Park, CA 91303. Tel: (213) 348-1391.

For additional information circle 199 on inquiry card.

Brownoutproof:

Often the Difference Between Up and Running or Down and Out.

To smooth out the Ups and Downs of today's utility power, digital design engineers are turning to The Dependables - the family of brownout-proof, switching power supplies that virtually eliminates the effects of utility power variations on equipment reliability.

The Dependables can supply their specified outputs at full load over input voltage ranges of 92 to 138 or 184 to 250 VAC; and, in fact, they'll operate for several minutes at inputs as low as 70 or 140 VAC. If AC input fails completely, the supplies will hold up for 30 milliseconds, allowing orderly system shutdown.

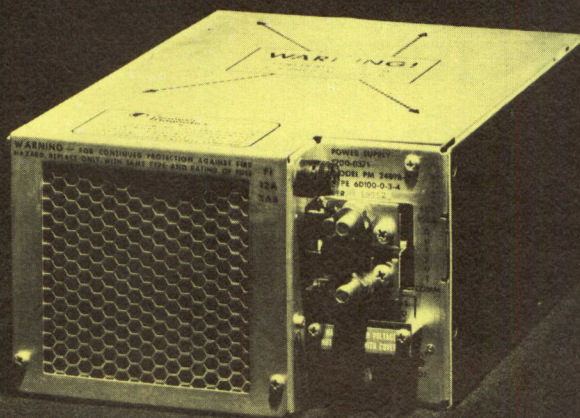
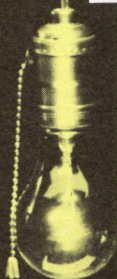
In addition to brownout protection, the Dependables feature:

- 0.1% Combined Line and Load Regulation
- 40,000+ MTBF, field proven
- 0 to 50°C Operating Range at Full Load with 80% Output at 70°C
- U.L. Recognition

For over 17 years, Pioneer Magnetics has been designing, building and delivering switching power supplies. Today, more engineers are considering them. Because tomorrow, utility power isn't going to be any better.

For complete information on our standard and customized switching power supplies, contact: Pioneer Magnetics, Inc. • 1745 Berkeley St. • Santa Monica, CA. 90404 • Tel. (213) 829-3305 • TWX 910-343-6249.

SINGLE OUTPUT SUPPLIES				CONFIGURATIONS
MODEL	PM2496	PM2497	PM2498	
Output Volts	Output Amps	Output Amps	Output Amps	
2	100	200	400	
3	60	100	300	
5	50	100/150	300	
12	23	60	120	
15	20	50	100	
18	17	45	90	
21	14	38	76	
24	13	33	66	



Pioneers in Switching Power Supplies.

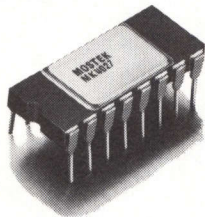
Announcing a in 4K RAM

Mostek packs all of this:

1. 200 nsec access time
2. $\pm 10\%$ tolerance on all supplies
3. low capacitance (< 5 pF),
TTL-compatible inputs
4. three-state TTL-compatible output
5. output data latched and valid
into next cycle
6. gated $\overline{\text{CAS}}$
7. $\overline{\text{RAS}}$ only refresh
8. page mode operation with page
access of 135 nsec.
9. read modify write operation

new standard performance.

Into this 16-pin package!



Mostek's new MK 4027 makes 4K RAM performance as revolutionary as the 16-pin package was two years ago. Now, every MK 4027 we ship has $\pm 10\%$ tolerance on all power supplies. And fast access time of 200 nsec. There are no high level clocks and the MK 4027 is Schottky TTL-compatible. That means your system performance can now match data sheet specifications.

Quality is another high standard at Mostek. This quality is inherent in the MK 4027. Mostek 4Ks work . . . and keep working.

Availability? *We've got them stocked on distributor's shelves for immediate delivery.* There's also a complete package of specification data and application information. Call or write Mostek. Or contact any Mostek sales representative or distributor.

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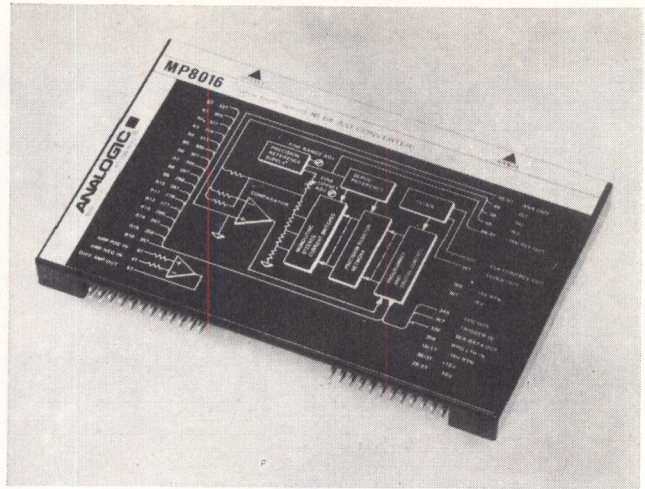
1215 W. Crosby Rd., Carrollton, Texas 75006
214/242-0444

In Europe, Contact:
MOSTEK GmbH, TALSTR. 172, 7024 Bernhausen, West Germany
Telephone: (0711) 701096

PRODUCTS

Fully Buffered 16-Bit A-D Converters Feature External Calibration Adjustments

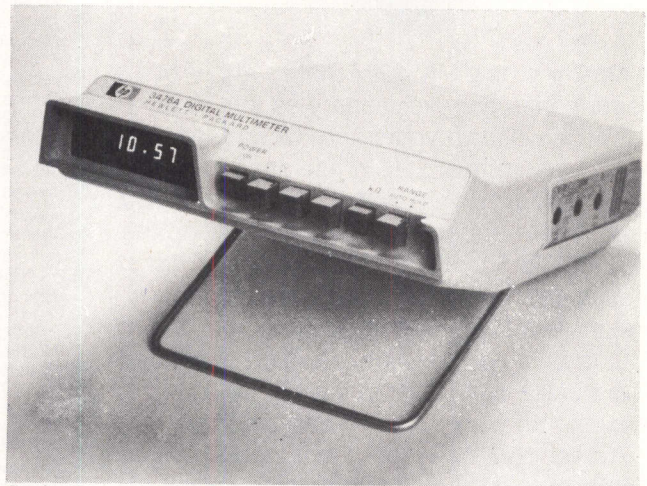
Series 8000, 14-, 15-, and 16-bit converters use built-in externally accessible calibration adjustments to guarantee accuracy traceable to the National Bureau of Standards. Conversion time is externally adjustable to $0.6 \mu\text{s/bit}$, relative accuracy is $\pm 0.0015\%$ FSR, differential linearity tempco is $1 \text{ ppm}/^\circ\text{C}$, gain tempco is $< 2 \text{ ppm}/^\circ\text{C}$, and offset tempco is $< 1.5 \text{ ppm}/^\circ\text{C}$. Packaged in a $4 \times 3 \times 0.375$ " metal case, the unit has fully buffered inputs/outputs, and is shielded against rfi and emi to make the modules virtually noise-free ($300 \mu\text{V pk-pk}$) in high interference environments. The design contains a true differential input amp with high input impedance; a current-switching ladder network with critical tracking stability; a high gain, low noise comparator designed to ensure rated resolution and wide temp stability; a temp-compensated, current-controlled zero reference for accuracy; and a digital programmer for adjusting word length. Devices are fully compatible with DTL/TTL input and output, as well as positive-true logic levels and furnish parallel output data and NRZ serial output data with synchronizing clock pulses. **Analogic Corp.**, Audubon Rd, Wakefield, MA 01880.



Circle 200 on Inquiry Card

Low Cost, Autoranging Digital Multimeter Measures Voltage, Resistance, Current

Low cost, $3\frac{1}{2}$ -digit, 5-function, fully autoranging 3476 DMM measures dc and ac voltages from $\pm 100 \text{ mV}$ to $\pm 1 \text{ kV}$ and $300 \mu\text{V}$ to 700 V , respectively; resistances from 1 to $11 \text{ M}\Omega$; and current from $100 \mu\text{A}$ to 1.1 A dc and $300 \mu\text{A}$ to 1.1 A ac. Auto-zero, autopolarity, and autoranging are built in. Low price is achieved through use of fine-line, tantalum nitride resistors which enable more costly discrete precision resistors to be eliminated. Typ accuracy for dc voltage measurements is 0.5% ; dc current accuracy is 1% . On ac voltage ranges, frequency is specified to 10 kHz , while ac current measurement is to 5 kHz . Resistance measurements on the three highest ranges are accurate to 0.6% ; 0.4% on the two lowest ranges. Open circuit voltage is $< 4 \text{ V}$. Input resistance on all voltage ranges is $10 \text{ M}\Omega$ with input capacitances of $< 30 \text{ pF}$. Model 3476A is ac line-powered only; -B also includes rechargeable nickel cadmium batteries, which when fully charged provide 8-hr typ operating time. **Hewlett-Packard Co., Instrument Group**, 1501 Page Mill Rd, Palo Alto, CA 94304.



Circle 201 on Inquiry Card

Compact Data Cartridge System Records 100 Kilobytes at 30 in./s

Utilizing the DCD-1 data cartridge drive (containable within a 5 " cube) and the Scotch brand DC100A data cartridge, which is approximately one-third the size of previous cartridges, this data cartridge system offers the same reliability, and operates at the same speed as the larger DC300A/DCD-3 cartridge system. As many as four cartridge drives may be incorporated into one system, selectable by control circuitry. The TTL system uses two 5×12 " PC boards which may be mounted at a convenient location within the device or its cabinet. Average data capacity of one $2\frac{1}{2} \times 3\frac{1}{4}$ " DC100A cartridge is $100,000$ 8-bit bytes, with an avg transfer rate of 2530 bytes/s . Tape speed is 30 in./s (76.2 cm/s) forward and reverse [60 in./s (152.3 cm/s) reverse speed can be ordered]. The mechanism has 27-ms start delay and 5-ms stop delay. Recording is in serial mode across the full 0.15 " tape width, virtually eliminating soft errors; encoding technique is independent of tape speed; and control logic prevents the drive from accepting any command that might harm the cartridge. **3M Co., Mincom Div**, Bldg 223-5E, 3M Center, St. Paul, MN 55101.



Circle 202 on Inquiry Card

Tektronix TM 500

a line
of 29 test
instruments

that go
six-in-a-rack
including
custom circuits.

- digital multimeters
- counters
- generators
- amplifiers
- power supplies
- oscilloscopes
- a blank plug-in for your own circuitry
- and more

TEKTRONIX modular instrumentation offers your QC, production test, or built-in test equipment a highly compact, extensive line of test instruments . . . TM 500. They are designed to work totally independently or as a system with each other. Blank plug-in kits make it easier for you to build in your own testing circuits compatible with TM 500. The RTM 506 rackmounting power module/mainframe (only 5¼" high) provides six compartments to accommodate TM 500 plug-in modular instruments and the plug-in kits. It is available for benchtop or portable use (TM 506), as well as for rackmounting (RTM 506).

A common interface circuit board within the mainframe permits the intercommunication of inputs, output, and various parameters among the plug-ins. Tektronix will supply you with data on voltages, currents, and pin connection diagrams, so you can determine the feasibility of assembling your special circuits in blank TM 500 plug-in kits.

The TM 500 family of instruments is designed to fulfill your test and system needs in such widely divergent areas as high-speed logic; dc, power line frequency, audio, and rf to 550 MHz; oscilloscope and other instrumentation calibration; and even medical instrumentation calibration. They represent Tektronix standards of quality in design, performance, and ease of opera-

tion. Included are pulse generators with features such as independent pulse top and bottom controls and repetition rate to 250 MHz. And the DC 505A Universal Counter/Timer features direct counting to 225 MHz and time interval averaging with resolution to 100 ps.

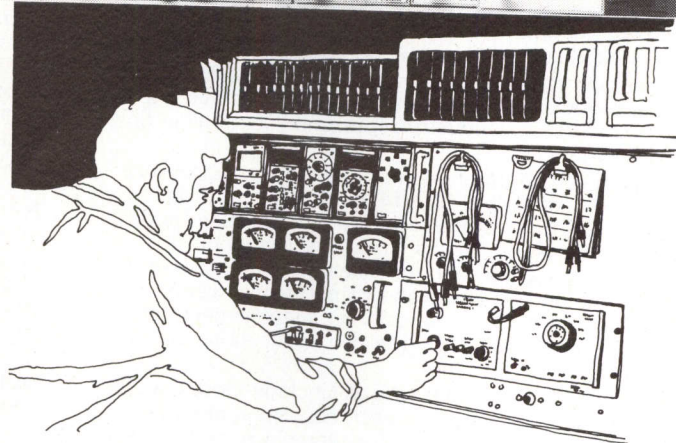
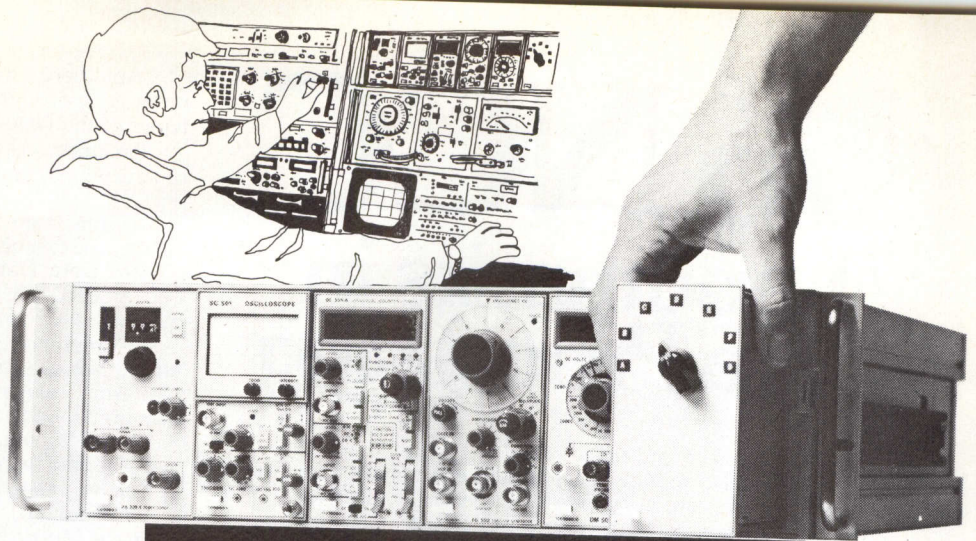
Here is a growing, compatible family of 29 plug-in modular instruments, accessories, and one, three, four, and six-compartment mainframes providing the common power supply. All mainframe/power modules may be hand-carried, all go on the bench, and there are SCOPE-MOBILE® configurations as well. Some instruments are general purpose, such as DMMs, some are highly specialized, such as those for oscilloscope calibration. They comprise test and measurement systems that are difficult to duplicate with monolithic instruments.

Send for the 56-page TM 500 catalog A-3072 with full specifications and suggested selections of instruments for typical applications. Or contact your local Tektronix Field Engineer for a demonstration of how TM 500 instruments can solve your needs. Write to Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97077. In Europe write Tektronix Limited, P.O. Box 36, St. Peter Port Guernsey, Channel Islands.



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technical excellence



For technical data, circle 22 on Inquiry Card.
For a demonstration, circle 33 on Inquiry Card.

'76 NCC

Landmarks in Data Processing

Mark the place and time... New York City, June 7-10... for the National Computer Conference, a landmark event for computer professionals, applications specialists, users, business managers, administrators, educators, and others concerned with data processing.

The '76 NCC will be your one opportunity during the Bicentennial Year to hear leading experts, to see and evaluate the latest in products and services, and to confer with colleagues, customers, and industry representatives... all in one place at one time.

More than 100 information-packed sessions will analyze the latest trends and issues affecting performance, productivity, and profit. The program sessions will be organized into 10 or more major areas, or "tracks," running throughout the Conference and covering such topics as complex systems, hardware technology, software and components, system architecture, computer communications, management concerns, education and training, advanced applications, and societal issues.

In addition, the program tracks will include more than 20 special one-day "mini-symposia," each consisting of four sessions. In advanced applications, for example, mini-symposia will cover medicine and health care, banking and electronic funds transfer, and business systems. Other symposia will include such key topics as government policy, control instrumentation, performance measurement, standards, networking, privacy, legal considerations, and word processing systems.

And there's much more. The world's largest lineup of data processing products and services will be displayed on three floors of the New York Coliseum.

Included will be the latest offerings from more than 275 organizations, ranging from mainframes, minicomputers, peripherals, packaged programs, and publications, to micro-processors, memories, terminals, systems, and services. Among the exhibitors will be such leading companies as Ampex, Control Data, Data General, The Harris Corporation, Hewlett-Packard, IBM, ICC/Milgo, Lear Siegler, Modular Computer Systems, NCR, Pertec, and Xerox.

Conference registrants will also have the opportunity to attend five special Plenary Sessions featuring leading spokesmen from industry, the computing profession, and major user areas. And, for an additional fee, they will be able to choose among a number of in-depth Professional Development Seminars dealing with advanced techniques for cost-effective computer usage.

In addition, a Pioneer Day Program will honor individuals from the Moore School of Electrical Engineering, University of Pennsylvania, who developed ENIAC—the world's first electronic digital computer. All this plus a Computer Art and Graphics Display, a National Student Computer Fair, the annual Conference Reception, and many other high-interest events promise to make '76 NCC a landmark event for the entire computer industry.

Advance full-conference registration brings you the *NCC Bicentennial Card*, providing complete access to all four days of the Conference program, including exhibits. Benefits include a \$15 saving over the on-site full-conference registration fee, advance housing information and forms, and a copy of the '76 NCC Proceedings. Post-conference price of the Proceedings alone is \$50.

Fill in and mail the coupon below for advance registration or to get all the facts; or contact AFIPS, 210 Summit Avenue, Montvale, New Jersey 07645, telephone 201/391-9810.

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in Data Processing**

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- My company is interested in exhibiting at '76 NCC.

Name _____

Title _____

Company _____

Street _____

City _____

State _____ Zip _____

CD

MM1 from the OEM Microcomputer

You've seen the hardware. Now we'd like to tell you about the software and **MDS 1 . . . A Family of 12 Microcomputer Development Systems. The first digit beyond the / refers to software (i.e. MDS 1/21 is supplied with Level 2 software); the second digit after the / is the console (in the example, it refers to a monitor start system.**

The software levels are:

Level 1 Absolute assembler, loader and system monitor with paper tape reader/punch TTY drivers, 5K bytes memory.

Level 2 Level 1 plus relocatable assembler and loader, 8K bytes memory.

Level 3 Level 2 plus disk operating system, 12K bytes memory.

Level 4 Level 3 plus Fortran IV compiler, 24K bytes memory.

The console levels are:

Level 1 Monitor Start

Level 2 Operator

Level 3 Programmer



MDS 1/11 Level 1 software with 5K byte memory, Monitor Start

System Prices:

MDS 1/11	MDS 1/21	MDS 1/31	MDS 1/41
\$2350.	\$2950.	\$3950.	\$6450.
MDS 1/12	MDS 1/22	MDS 1/32	MDS 1/42
\$3150.	\$3750.	\$4750.	\$7250.
MDS 1/13	MDS 1/23	MDS 1/33	MDS 1/43
\$3800.	\$4400.	\$5400.	\$7900.

Enclosures:

Desk Top \$220.00

Desk Side \$500.00

Cabinet \$800.00

Peripheral Options: (Pricing to be announced)

High speed paper tape reader/punch.

Printer.

Single or dual floppy disk.

CRT/Keyboard.

PROM Programmer.

Disk Operating System (MIDOS)

Supports both Single and Dual Floppy Disks.

Memory Resident — requires 4K of memory.

MIDOS is relocatable — Bootstrappable via System Monitor.

Provides user with disk file support, keyboard commands and program calls.

COMMANDS:

CRT Create a file.
DEL Delete a file.
CHG Rename a file.
CAP Change file attributes.
SAV Save memory image in absolute binary file.



MDS 1/32 Level 3 software with 12K byte memory, operator's console.

LOD Load absolute binary file into memory.

PCK Create a file on same track as an existing file (binary only).

INI Initialize diskette by clearing directory and writing copy of MIDOS on diskette for bootstrap.

DUP Duplicate a file or diskette.

MAP List diskette directory.

GOT Go to starting address of file loaded.

ODT Go to system monitor.

Direct program calls provide the user with the following functions (all program calls via I/O control program):

- Open a source (input) file (close any currently open source file).
- Open a destination (output) file (close any currently open destination file).
- Close source and destination file.
- Read N bytes from source file.
- Write N bytes on destination file.
- Reset source file to start of file.
- Terminate disk operation.
- Update directory.
- Print error code.

Extensive error messages are provided.

NF No such file name.

NU File name in use.

DK Disk error.

Tφ File directory format error.

DA Disk not ready / protected.

NA Attribute does not allow operation.

DS Disk space exhausted.

HS Maximum number of files exceeded (26).

TE File type does not allow operation.

HI Directory information overwritten in memory.

FE Binary checksum error.

SO Packing error.

System Generator (SYSGEN)

The System Generator allows the user to configure his system to his I/O requirements, and, with the use of I/O control, to add new device drivers to his system as required.

The System Generator:

- Reads device drivers, support routines, and main programs in relocatable binary format and provides the same load features as the linking loader.
- Creates in absolute binary formatted data, the programs loaded, the system parameters and the I/O device table.

Absolute Assembler — (MIABS)

- Runs in 3.5K memory plus symbol table.
- Allows ~ 1000 user symbols in 10K system (~ 165 symbols / additional 1K memory).
- Flexible format and symbol table allow User to create own language. Reserved symbols : A, B, C, D, E, H, L, PSW, BC, DE and HL. Absolute binary output format (loaded via absolute binary loader). Octal listing format. Single and double precision numerics in decimal, octal and hexadecimal; address references also generated.
- "Text" pseudo-operation.
- Conditional assembly.
- Program counter update to beginning of next memory "page" (256 bytes/page).
- Error count on termination.

- Device independent I/O via I/O control program.

Relocating Assembler (MIREL)

- Requires 4.5K memory.
- Allows user ~ 165 symbols/1K available memory.
- Relocatable binary output format loaded via linking loader.
 - Provides for linkage between program modules:
 - "Title" Program name (ID during load).
 - "Ext" Specify following labels as external.
 - "Ent" Specify following labels as entry points — they must appear in program body.



MDS 1/43 Level 4 software with 24K byte memory, programmer's console.

- Absolute and relocatable addresses may be mixed within program. Ext and

Control Logic with Super Software Support

- Ent linkage within absolute and relocatable portions is valid.
- All other functions equivalent to absolute assembler.

Linking Loader (MILINK)

Provides linkage for loading separate programs written in relocatable format and assembled via the relocating assembler (externals are linked to entry points).
Output is absolute binary, and a load map.

- >>> CKSM Checksum error.
- >>> NO-BLK 1 First block not block 1.
- >>> TOVF Number of modules loaded exceeds limit.
- >>> EOVS Symbol table overflow.
- >>> BKER Relocatable binary format order error.
- >>> OVFL Up and down load overflow (non fatal).
- >>> SYER Symbol ID error.
- >>> MDT Multiple program names.
- >>> MDL Multiple entry point names.

I/O Control System (MICON)

MICON provides for functional, rather than device dependant, software communication with peripheral devices.

Standard calling sequence:

CAL ICON

- < Function >
- < Subfunction >
- < Unit ref # >
- < Return address >
- < Transfer count >
- < Buffer address >

Text Editor (MIEDIT)

The Text Editor provides the user with the means to create and modify source code on tape or file using the following commands:

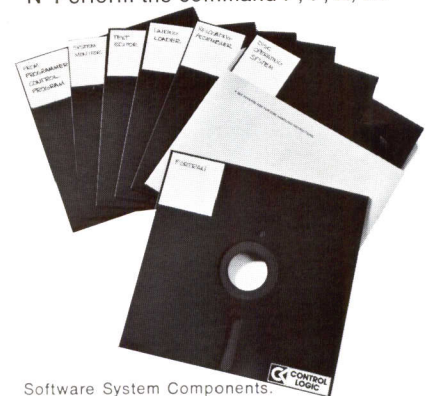
- K Clear the text buffer
- A Append lines to edit buffer
- D Delete lines
- I Insert lines
- C Change lines in the buffer
- S Search a line for a character
- G Search the buffer for a string
- R Ready source data from the input device
- L List source data on the listing device
- P Output source data on the output device
- F Output a form feed to output device
- N Perform the command P, F, K, R.

System Monitor/Debug (MIODT)

- Display and modify memory.
 - Display and modify registers.
 - Punch absolute binary formatted data from memory.
 - List octal data from memory.
 - Find every occurrence of a BYTE or pair of BYTES in memory and list its address.
 - Input from device N and display value.
 - Output to device N the value entered.
 - Set an offset value for use in displaying relocated data.
 - Read absolute binary formatted data into memory.
 - Transfer to memory location PN.
 - Break point functions.
 - Enter BRK Pt.
 - Delete BRK Pt.
 - Continue after BRK Pt.
- Stop on BRK Pt after Nth occurrence. Don't stop on break point; print contents of registers and break point address at each occurrence (snap shot trace).
- Terminate all functions via control C.
 - Modify device reference for I/O function; i.e., change I/O device.



Documentation, software and user group listings.



Software System Components.

Two pass linking loader.

- Reads relocatable binary format.
 - Generates symbol table.
 - Modules can be loaded from lower memory to higher memory or from high memory to low memory.
 - User definable address relocation bases prior to each module load. (One for loading "up" and one for loading "down").
 - Prints the symbol and address of all entry points encountered.
 - Report all unpaired external symbols.
 - Load library routines from a single library — tape or file.
 - Generate a program load map.
 - Generate a library tape.
- Load relocatable binary format tapes or files in any order.
 - Generate absolute binary formatted output.
 - Generate leader/trailer on command. A comprehensive list of error messages is provided.

Gentlemen:

How can MM1 make my products more competitive?

Type of product _____

Product Quantities _____

Required Options _____

Now that I've told you . . . you tell me:

When can Control Logic deliver?

How much does MM1 cost?

Name _____

Company _____

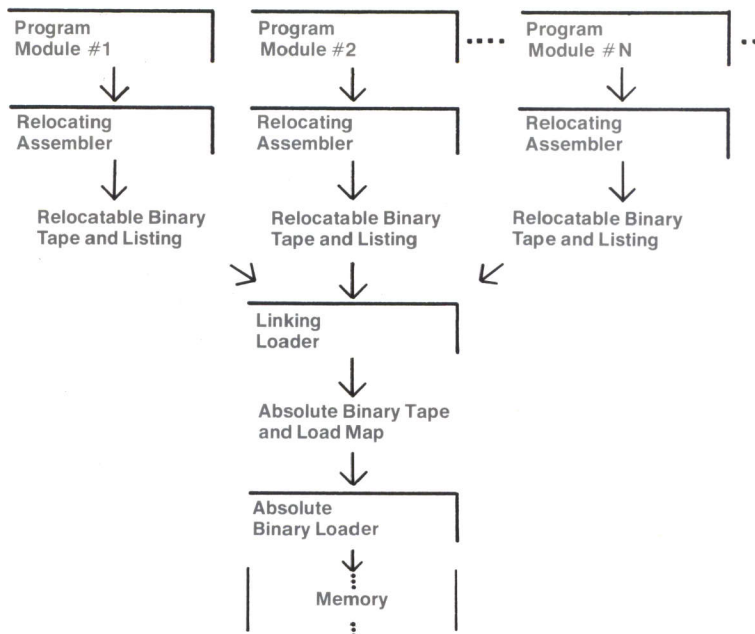
Street _____

City, State, Zip _____

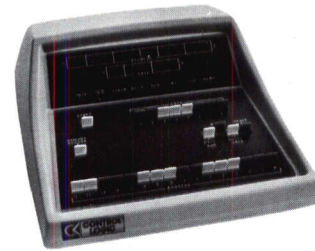
Or Call Me Right Away _____

Area/Number

. . . and while you're at it, refresh my memory about the hardware.



- Logical IF Statements
- Expressions
 - Mixed mode arithmetic allowed: Logical operators work on a bit by bit basis. Relational expressions accepted in logical IF statements only.



Operator's Console; Programmer's Console.

PROM Programmer Control Program (MIPPCP)

The PROM Programmer Control Program allows the user to read absolute binary formatted data into memory and to program this data onto PROM. The program also provides:

- Blank PROM test
- Compare memory vs. PROM
- Transfer PROM to memory
- Data Inversion
- Absolute binary formatted output
- Built-in test features

FORTRAN (MIFORT)

- Statement Labels
 - 4 digits (range 1-9999)
- Variable Names
 - Up to 6 characters
- Data Types
 - Integer (32 bits); Real (32 bits); Hollerith (character strings in data statements, subroutine calls and expressions); Byte (8 bits)

- Specification Statements
 - Dimension, common, equivalence.
- Arrays
 - 1 or 2 dimensions. Subscripts of any form. No variable dimensioned arrays.
- Common
 - Blank (unnamed) common.
- Data Statement and Block Data sub-routines will also be permitted.
- Functions and Subroutines
 - Arguments passed by name. Can pass variables, constants, or arguments to a subroutine, but not statement numbers or external subroutine names. Statement functions not allowed.
- Do Loops
 - Parameters can be of any form.
- Assigned GOTO Statements

- Input/Output
 - Formatted and unformatted I/O allowed. First character on a line is spacing control for formatted output. Encode/Decode is supported.
- Special Extensions
 - Machine indicator functions (switches and lights). A/D input and D/A output. Real time clock control. BCD I/O.

Floating Point Package

Includes floating point add, subtract, multiply and divide. Fixed point arithmetic included in package. Conversion from ASCII character string is also included.

If your requirement can't wait, call the Regional Office nearest you:

Philadelphia (215) 544-7153

Geoff Hawkes

Chicago (312) 671-5228

Paul Fitzner

Los Angeles (714) 558-8035

Paul Montag

International (617) 899-3510

Bruce Campelia

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617-655-1170

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Wescon/76

One of a kind-Again

When Wescon holds its 25th birthday party in Los Angeles for 35,000 close friends, it will be a brand-new show all over again.

That's because the electronics industry cannot tolerate the *status quo*. (You keep up, or you slip out.) This Silver Celebration Year will be another large-scale, full-house WESCON, right up-to-date in a dozen timely and tangible ways.

These are the features you'll find at Wescon/76. And *only* at Wescon/76:

The Red Carpet Treatment,
rolled down every show aisle.

Computerized Registration at two Convention Center entrances.

Freight Service, in and out from the dock, at no charge. (Ditto daily janitorial services.)

Professional Program, keyed to design, specifying and production technologists (no extra charges).

The Great Pink Card guest registration plan for qualified visitors (by the thousands).

The VIV Program for your most-wanted Very Important Visitors.

Product Categories — a floorplan by design, not by chance.

Famous Wescon "Packages": all-inclusive, turnkey display rentals (brand-new again this year).

New Advance Registration system (down with time-in-line!).

Shuttle bus system from major hotels and terminals (no charge, of course).

Industry-wide communications: Nobody won't know there's a Wescon!

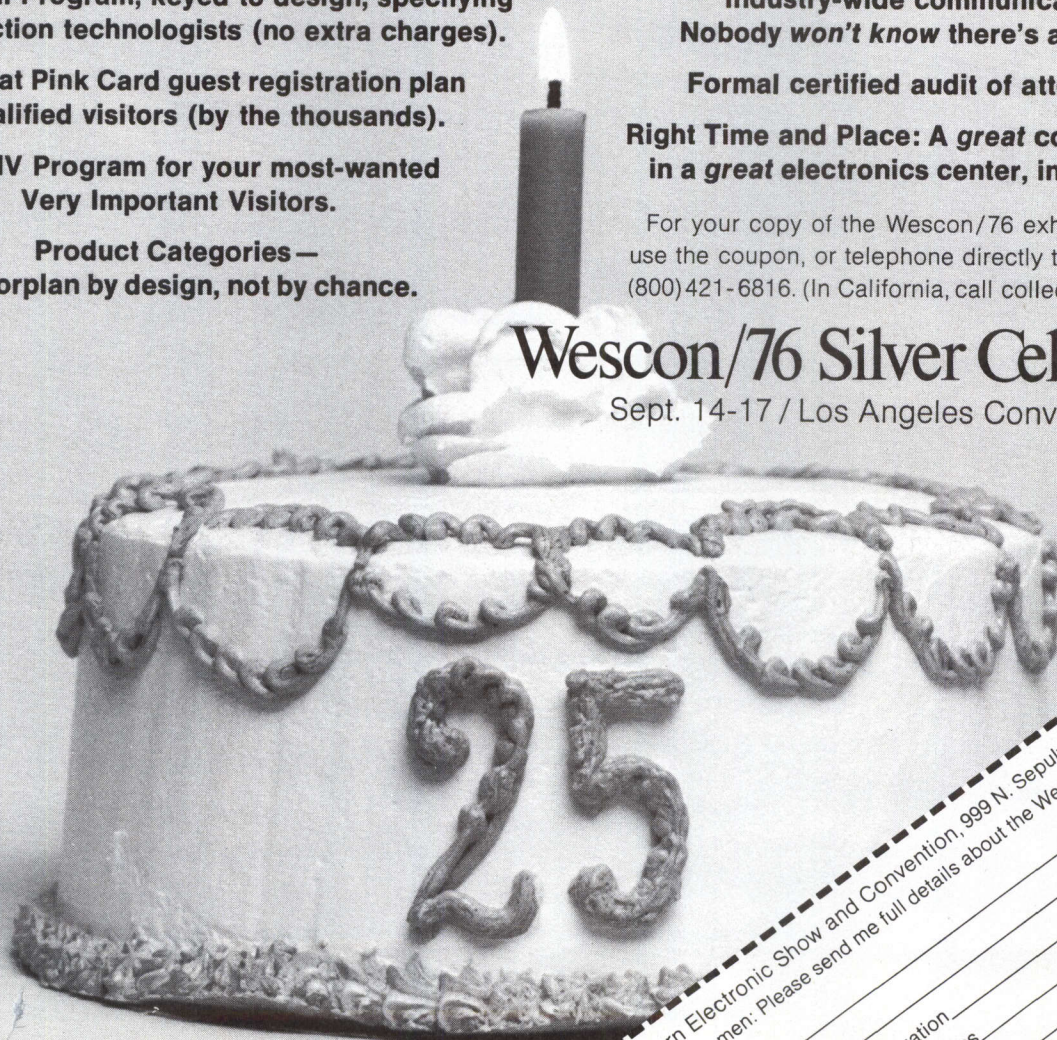
Formal certified audit of attendance.

Right Time and Place: A great convention hall, in a great electronics center, in September.

For your copy of the Wescon/76 exhibit prospectus, use the coupon, or telephone directly to Tom O'Gorman (800) 421-6816. (In California, call collect: 213-772-2965)

Wescon/76 Silver Celebration

Sept. 14-17 / Los Angeles Convention Center



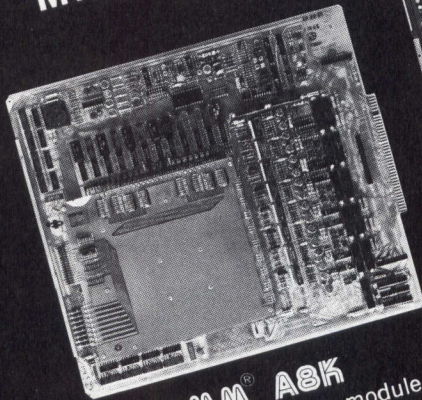
Western Electronic Show and Convention, 999 N. Sepulveda Blvd., El Segundo, CA 90245
Gentlemen: Please send me full details about the Wescon/76 Silver Celebration.

Name _____
Title _____ Organization _____
Address _____
City _____ State _____ Zip _____

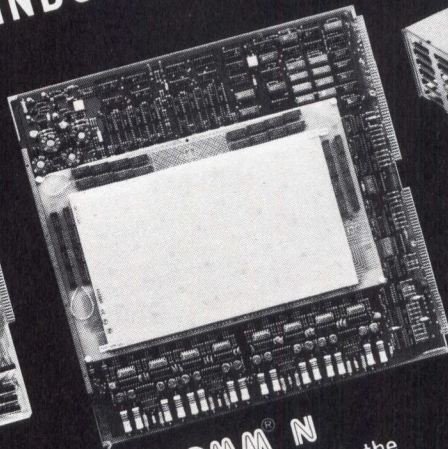
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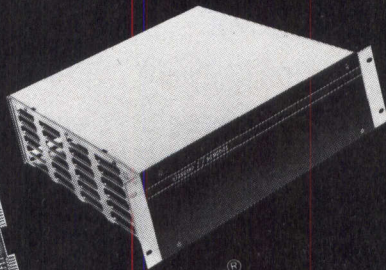
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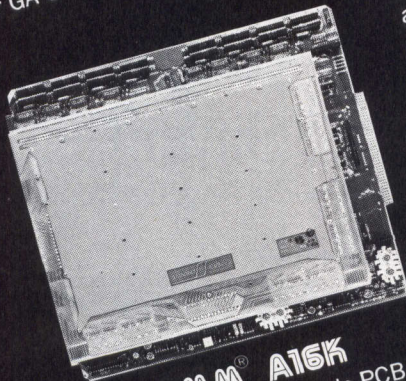
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A replacement memory module
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enhance existing processors to
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The proven reliable, low-cost
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16,384 words on a single PCB
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A 16K word memory module
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Write or call today for complete
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memory requirements.

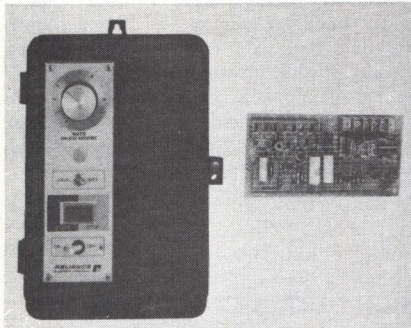
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Suite 105
Newport Beach, California 92660
Phone: (714) 752-8455

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PRODUCTS

MASTER ISOLATED REFERENCE DRIVE CONTROL



Interface unit can control up to 10 separate MinPak, FlexPak, and MaxPak V*S drives with the reference circuit for each drive isolated from all other drives as well as the reference output signal. The reference consists of a signal transmitter and up to 10 signal receivers. Transmitter model 11C90 contains all circuitry required to control up to 10 drives including reference circuits and relays for group start/stop control. **Reliance Electric Co.**, 25001 Tungsten Rd, Cleveland, OH 44117. Circle 203 on Inquiry Card

COMPUTER CONTROL SYSTEM CRT TERMINALS

Featuring 3-dot spacing between char and lines to improve definition, Optrol 340 and 350 have double-faced card sockets in the logic package to make troubleshooting and maintenance easier and faster, by permitting complete accessibility of the card when reversed. A graphics curve drawing option permits two curves to be presented simultaneously, in the upper half, lower half, or middle portion of the screen. The 340 has a 17" monochrome screen with a green phosphor background, the 350 a 19" color screen which displays char or graphics segments in seven colors. **Applied Automation, Inc.**, Bartlesville, Okla. Circle 204 on Inquiry Card

1800-LINE/MIN. PRINTER

A low cost, online system that is plug-compatible with Honeywell 600 and 6000 series computers, model M470G, with free-standing controller, attains 1800-line/min., printing 36 consecutive chars on the 64-char print drum. The entire 64-char set can print at more than 1200 lines/min. The system delivers a full 136-col format and can handle up to 6-part forms. Specially designed paper guides permit fine horizontal and vertical alignment even while printing. **Macro Products Corp.**, 3110 E Willow St, Long Beach, CA 90806. Circle 205 on Inquiry Card

DUAL OUTPUT SWITCHING POWER MODULES

AA series modules provide 120 W of output power at ± 12 V (-12ROS5) and ± 15 Vdc (-15ROS4), with power densities of 2.2 W/in.³ and 45 W/lb at min efficiencies of 78%. Fully regulated (0.2%, line/load combined) positive output and semiregulated (0.1% line, 2.5%/A load) negative output are std. Fully regulated negative output, adjustable output voltage, and battery back-up are also available. Input line range is 100 to 130 Vac rms at 47 to 440 Hz. **Etatech, Inc.**, 187-M W Orangethorpe Ave, Placentia, CA 92670. Circle 206 on Inquiry Card

SWITCHING REGULATOR POWER SUPPLIES

"Red Demon" model CDS 5-60 and 5-100 Controswitcher™ units are up to 75% efficient (at 5.5 Vdc and 100 A), through use of a Controfluxer™ voltage regulator filter. The units operate from 95 to 140 Vac, 47 to 440 Hz 1 ϕ , or 120- to 180-Vdc power. Output voltage is adjustable from 4.75 to 5.5 Vdc. -60 provides 60 A at 40°C; -100, 100 A. Tempco is 0.02%/°C, and stability is >0.1% over an 8-hr operating period. Load regulation is >0.02% for 0 to 100% of specified load current, and line regulation is >0.02% for 95- to 140-V line range. **Adtech Power, Inc.**, 1621 S Sinclair St, Anaheim, CA 92806. Circle 207 on Inquiry Card

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- Low in cost (only \$195 in quantity)
- Compact, reliable. Only 2 moving parts
- "Accu-Rate™", new concept in electronic tape speed control
- Takes only 1 voltage (14-30 VDC)
- "POPS™" cassette release (Push to Open, Push to Shut)

Looking for transport reliability? For low power consumption, short IRG, excellent speed control?

Then we think you'll be impressed with our newest transport. Check it out.

YES!

I'd like to know more about the new CD-200.

Send literature.

Let's arrange for a demo. Call me at _____

Name _____

Title _____

Firm _____

Address _____

City _____ State _____ Zip _____

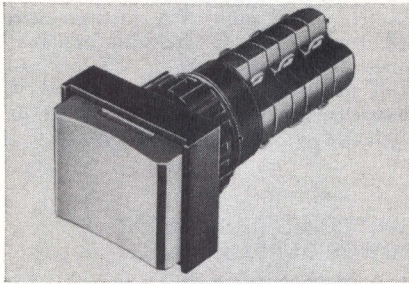
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PRODUCTS

LIGHTED PUSHBUTTON SWITCH



A 1- to 4-pole, momentary or alternate snap-action switch, EAO series 31 is rated up to 5 A, 250 Vac, has gold-laminated double-make, double-break contacts to handle low-level switching, and is only 1.949" deep behind panel. Available in both square (0.71 x 0.71") and rectangular (0.71 x 0.945") versions, the device provides an extra large surface area for the heat-resistant lens caps. Lenses are either flat or concave, in transparent or translucent material in any of 16 colors. **Unimax Switch Corp.**, Ives Rd, Wallingford, CT 06492.

Circle 208 on Inquiry Card

MODULAR ONLINE UPS

Model 5264A is a solid-state 15 kVA 3 ϕ I/O system in nonredundant or redundant configuration. Seismic qualification makes it suitable for installation in nuclear facilities which require earthquake rated equipment. The indicator panel gives a complete functional status of the system using multicolored LEDs to provide instantaneous identification of any malfunction. System control and logic circuitry is on PC boards which plug into a motherboard; all test points are easily accessed at this location. **Deltec Corp.**, 980 Buenos Ave, San Diego, CA 92110.

Circle 209 on Inquiry Card

13-BIT MULTIPLYING DAC FOR TTL APPLICATIONS

Designed for low power, 4-quadrant, multiplying DAC applications, series 877-69 features 13-bit resolution, external ac or dc reference, ac reference frequencies from dc to 10 kHz, MSB inversion input for 2's complement or offset binary arithmetic options, an internal precision thin-film resistor chip to assure high accuracy, and two package options. Typ accuracy of metal package (69M-D1) is $\pm 0.012\%$ at 25°C; $\pm 0.05\%$ at 25°C guaranteed to 0.1% for -69M-D2. **Beckman Instruments, Inc.**, Helipot Div, 2500 Harbor Blvd, Fullerton, CA 92634.

Circle 210 on Inquiry Card

CALCULATOR INTERFACE OPTION

A841 permits Autodata Eight process control monitors to be combined with an easily programmable data manipulator. The package includes an interface board for the monitor, cable, and sample program listing, and is compatible with Tektronix 31 calculator, 154 interface, and related peripherals. With it, the process monitor is put under-calculator control for acquiring time and data from low level analog sensors. No computer is needed to process analog data, since the calculator is programmable by math keystrokes. **Vidar Autodata, Inc.**, 265 N Whisman Rd, Mountain View, CA 94043.

Circle 211 on Inquiry Card

HIGH OUTPUT COLORED LEDs

Red, yellow, and orange T-1 LED discretes for high density panel arrays and lighted pushbutton switches use composite light-emitting chips of GaAsP on a GaP substrate; green use GaP on GaP. All models have cylindrical, diffused encapsulations colored to match the color of light output. Typ luminous intensities are 5 mcd for the CM4-244B red and -444B orange, 4 mcd for the -544B yellow, and 1 mcd for the -344B green. **Chicago Miniature Lamp**, 4433 N Ravenswood Ave, Chicago, IL 60640.

Circle 212 on Inquiry Card

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COILTITE® SLEEVES

COILTITE® BITS

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CONNECTOR PRESSER

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CABLE STRIPPING

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DRUM RELIABILITY AT DISK PRICES

... new
head-per-track
memory combines
non-contact
start/stop reliability
with low cost per bit.

VRC offers you the low cost per bit associated with disk memories *and* the built-in reliability of drum memories in the new Model 4000.

Model 4000 head-per-track memory features a fail-safe head actuation system which eliminates the potential of media damage and data loss present in contact start/stop systems.

It's a compact, lightweight and low cost memory with 19 million bit capacity and access time of 8.5 m/sec.

All electronics are outside the drum enclosure so the drum is not subject to contamination. This feature helps insure MTBF up to 10,000 hours and makes the unit one of the easiest to service in the industry.

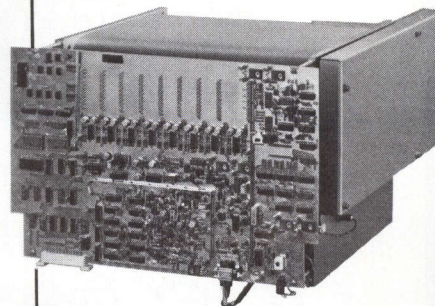
Applications are practically endless . . . point of sale, message switching, key entry, inventory control . . . wherever low cost per bit, fast access and high data storage capacity are required.

For dependable product performance backed by world-wide field service and applications engineering, you can rely on VRC. Write or call today for complete details on the Model 4000 head-per-track memory to improve the reliability of your system at an affordable cost.

**Vermont Research
CORPORATION**

Precision Park
North Springfield, Vermont 05150
Tel. (802) 886-2256 TWX: 710-363-6533

CAPACITY 9.5 or 19.0 megabits
DATA TRACKS 128 or 256
BIT RATES &
ACCESS TIMES 4.25 MHz at 3450 RPM
8.5 m/sec. 50 or 60 Hz power
(1800 and 2400 RPM available)
DIMENSIONS Height—11¾" (29.8 cm)
Width—17½" (44.5 cm)
Depth—21" (53.3 cm)
WEIGHT 89 lbs. (40.5 kg)



PRODUCTS

LOW COST VOICE SYSTEM



Words to form a custom vocabulary for the Votrax LV-50 voice communicator are digitized from a tape recording of the user's voice such that speaker identification is possible, male or female, in any language. Memory modules may be re-programmed or new modules added to meet changing requirements. The basic annunciator is available with 1 to 16 words, each of 0.66 s duration. Total message length can be 10.56 s/unit, but several units may be clustered. **Vocal Interface Div, Federal Screw Works, 500 Stephenson Hwy, Suite 102, Troy, MI 48084.**

Circle 213 on Inquiry Card

DIGITAL POSITION CONTROLLER

With stepping rates as high as 100 kHz, output power of >1 hp, and load inertias equal to motor inertias, digital position controllers also feature selectable motor resolutions of 800 to 8000 parts/rev, 2000-rpm motor speed, and 3 lb-ft torque. Positioning is accurate within a few tenths of a degree. The self-contained units consist of dc motor and digital controller teamed to produce a high stepping speed servo with adjustable position control by thumb-wheel switches. **Unico, Inc, 3725 Nicholson Rd, Franksville, WI 53126.**

Circle 214 on Inquiry Card

ECMA-COMPATIBLE TERMINALS

Designed primarily to prepare data, models 310 and 320 intelligent data entry terminals, for use with Honeywell series 62 and Sweda 1300 small business systems, are equipped with a CRT, electronic typewriter-like keyboard, ECMA-compatible cassette recorder, and microprocessor. Each has 8 kilobytes of ROM and firmware programs that automatically control terminal functions. The 310 provides one cassette recorder and may be equipped with an optional 3K of RAM, 320 includes a second cassette recorder. **Sycor Inc, 100 Phoenix Dr, Ann Arbor, MI 48104.**

Circle 215 on Inquiry Card

MONOLITHIC 8-BIT D-A CONVERTERS

DAC-IC8B, encased in a std 16-pin ceramic DIP that includes bias circuit, stable reference amp, and eight high speed current switches which drive an 8-bit diffused resistor R-2R ladder network, accepts std DTL/TTL-compatible, positive-true digital inputs. External pin interconnection permits the device to deliver either a 2-mA full-scale unipolar output in response to a straight binary-coded digital input or a ± 1 -mA bipolar output in response to an offset binary-coded input. Compliance voltage is 0.5, -0.6 V. **Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021.**

Circle 216 on Inquiry Card

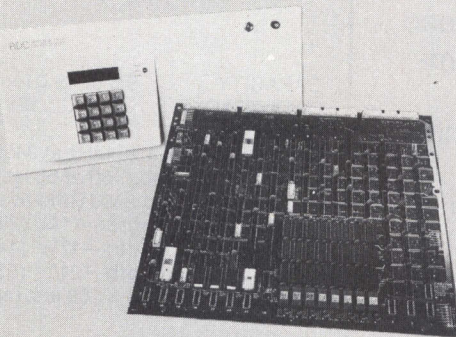
COMMUNICATIONS INTERFACE FOR MATRIX PRINTER

Use of the CDC 9316 matrix printer in receive-only remote communications terminal applications with an asynchronous interface, which connects to standard EIA RS-232-C or CCITT V24 modems or a serial I/O port, assembles asynchronous serial data into 5- or 8-bit parallel characters, and performs single-bit parity error checking. Error-free char are transferred to line or buffer memory. Eight switch-selectable baud rates of 150 to 9600 bits/s can be handled. **Control Data Corp, Box O, Minneapolis, MN 55440.**

Circle 217 on Inquiry Card

The Complete Microcomputer Series 70

• ECONOMICAL • MODULAR • EXPANDABLE • PERIPHERAL SUPPORT • SOFTWARE OPTION



Model 70-100 CPU and
Model 70-131 front panel console

Standard Features

- Intel 8080
- 1K bytes ROM
- 4K bytes RAM
- Async controller
- DMA
- Floppy Disk Controller

Applications

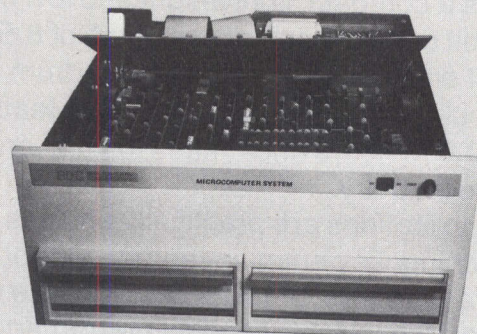
- Communications Systems
- Office Systems
- Small Business Systems
- Word Processing Systems
- Process Control Systems
- Text Editor Systems
- Source Data Entry
- Media Conversions
- Interactive Software Development
- Firmware Development
- Hardware/Interface Development

Options

- Add-on memory to 64K
- Add-in memory PROM to 4K, RAM to 16K
- Front panel console
- Enclosures
- IBM floppy disk
- 3M tape cartridge
- Programmable communication
- PROM programmer
- Line printer controller
- 9 Track tape controller
- Programmable clock
- General purpose I/O controller

Software

- ADC μ Executive for development
- ADC extended BASIC/DOS
- RS232 Firmware



Model 70-132 CPU, Dual Disk

APPLIED DATA COMMUNICATIONS

1509 East McFadden Avenue
Santa Ana, California 92705
Telephone: (714) 547-6954

Also
Add-on Mini
Peripherals for
DEC PDP-11,
Data General
DEC PDP-8

LIKE MONEY IN THE BANK

The new Dataproducts Model 2290 printer offers superior printing quality at 900 LPM with a full 64-character ASCII set.

For about half the cost of current high-speed line printers.

Couple that with extraordinary low operating costs and the 2290 is like money in the bank, twice over.

So why pay twice as much (and more) if 900 LPM is all you need?

PERFORMANCE PLUS ECONOMY

The 2290 was designed (from the proven technology of our 2200 series) to meet the requirements of the new high-performance, minicomputer-based systems.

So you can count on maximum operating economy in medium and large business data processing systems, distributed processing, and remote terminals at 9600 baud and up.

What's more, the 136-column 2290 is interface compatible with our 2230 (300 LPM) and 2260 (600 LPM), and over 70% of its parts are interchangeable with these field-proven models.

A little extra economy you can bank on with Dataproducts.

FEATURES YOU CAN BANK ON

The 2290, like all 2200 series printers, offers two unique systems:

The patented friction-free Mark IV print-hammer system for consistent high-quality printing and unmatched reliability.

And a patented system for automatic detection of lack of paper movement.



Plus, a 90° swing-open gate for fast ribbon and paper loading.

An adjustable paper stacker for uniform stacking of forms.

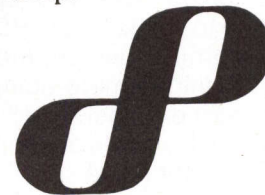
An optional direct-access vertical format unit that eliminates paper tape to allow printing of new formats direct from the CPU.

An acoustical cabinet for quiet operation in office atmospheres.

Little wonder that, with these outstanding features (and many more), Dataproducts is the world's leading independent manufacturer of line printers.

For all the facts and figures on the 900-LPM 2290, write for our brochure.

Better yet, call us collect and bank the unnecessary cost of a stamp.



Dataproducts
The Line Printer Company

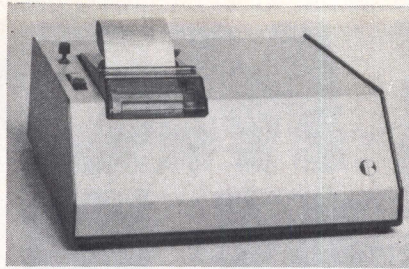
6219 De Soto Avenue/Woodland Hills, CA 91365
(213) 887-8451; Telex: 67-4734

THE NEW 900-LPM 2290

PRODUCTS

MICROCOMPUTER LINE PRINTER

A low cost, 160-char/s line printer with EIA and asynchronous bit-parallel ASCII interface cards, the MP-01 is designed for use with most microcomputers. Self-contained in a 10 x 10 x 4" package that includes power supply, the device uses a Sharp electric-discharge printer to provide 20-col printout on 2.25"-wide paper. Its std 64-char set includes full alpha-



numerics. Designed to facilitate the use of custom interfaces, the unit requires 120 Vac, 20 W power. **The Binary Corp**, 2680 Bayshore Frontage Rd, Mountain View, CA 94043.

Circle 218 on Inquiry Card

SYNCHRO-TO-RESOLVER CONVERTER

Designed for max conservation of space and weight, in a typ DIP with 0.1" pin spacing, the 52290 measures 1/2 x 7/8 x 7/16" and weighs 1/3 oz. 11.8-V line-to-line 400-Hz synchro voltages are converted to 3.2 Vrms sine and cosine resolver voltages; accuracy is 3 arc min. Operation is over the full military temp range. Stability is absolute and there is no accuracy drift with age. **Magneto, Inc**, 182 Morris Ave, Holtville, NY 11742. Circle 219 on Inquiry Card

1/4" TAPE FOR YOUR PDP-11? IN DECIDING, FORGET COMPATIBILITY.



You can, thanks to our TCP-1000—a tape peripheral unlike any other. Using the 3M or IBM cartridge—both solidly proven.

You know the tape. High storage capacity, high transfer speed, maximum reliability, highest data integrity of any removable media, cartridge convenience, more.

Now meet *the* peripheral. Plug-to-plug compatible with the PDP-11—hardware *and* software. Physically compatible—same panel size. Even aesthetically—same bezel design (it looks like it belongs). Completely self-contained—no outside power source required. No SPC slot, either. And *quite* contained—requiring minimal space to add.

That's the TCP-1000 tape peripheral—a uniquely realistic approach to the 1/4" tape/PDP-11 marriage.

Something else uniquely realistic with the TCP-1000 is cost. For all its unique mate-ability, bottom line (installed and running) it's the least expensive 1/4" tape peripheral around.

Now who could ask for more?

Ask us for more.

(Or less: our TCD 300 1/4" tape drive only.
Or TCT-300 tape system RS-232 Compatible)

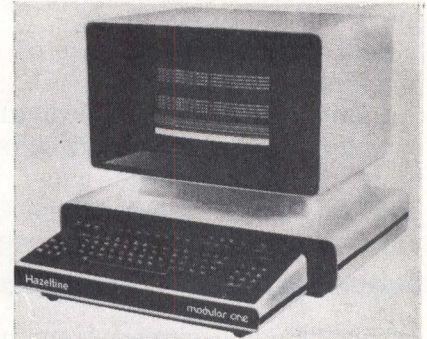


8 years famous for memory testers. Becoming more for peripherals.

THREE PHOENIX COMPANY

10632 N. 21st Ave. • Suite 10 • Phoenix, AZ 85029 • (602) 944-2221

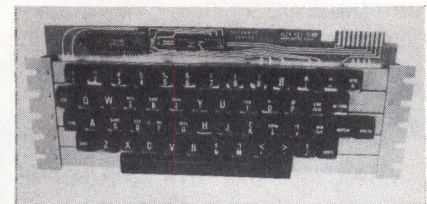
VIDEO DISPLAY TERMINAL



Using microprocessor techniques in conjunction with programmable ROMs to permit modular expansion through addition or deletion of pluggable modules, the Modular One terminal provides 1920 char display (80 x 24) on a 12" bonded screen, incremental and absolute cursor positioning, dual video intensity, 10-key numeric pad on a movable keyboard, choice of eight transmission rates up to 9600 baud, communication interfaces switchable between EIA RS-232 and current loop, choice of block or blinking underscore cursor, and white-on-black or black-on-white display presentation. **Hazeltine Corp**, Greenlawn, NY 11740.

Circle 220 on Inquiry Card

ALPHANUMERIC KEYBOARD



FlexMatic CEK-33, a 53-key, quad mode, USASII-coded ASR-33 keyboard, is available with either 2- or n-key rollover. Using a conductive elastomer switching technique, the unit has a full 0.18" keytravel, 0.05" overtravel, truncated 2-shot molded keycaps, and solid-state ROM encoding, and is fully compatible with TTL and MOS logic arrays. Switches are completely sealed and environment proof and are rated for 50 million operations min. **Flex-Key Corp**, 18 Sargent St, Gloucester, MA 01930.

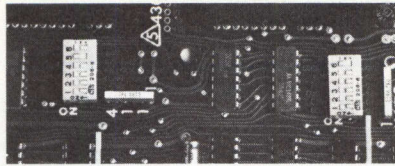
Circle 221 on Inquiry Card

All the people who bought our DUMB TERMINAL (the ADM-3) because of its low \$995* unit price didn't really expect a lot. But they hadn't counted on the 32 switches. Switches that let you turn the DUMB TERMINAL into a pretty clever animal.

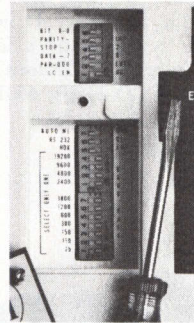
Take the 20 switches under the LSI name plate, for example. Among them, 11 communication rate positive action switches that let you select bauds from 19200 to 75. Also an RS232 interface extension port switch. It allows you to connect the DUMB TERMINAL to all kinds of clever devices — to recorders, printers and smarter terminals. And switches for odd-even parity. Optional upper and lower case (the complete set of 128 USASCII characters) — plus a lot more.

Inside on the PC board, 12 more switches. More positive action types that instruct the DUMB TERMINAL how to behave. And for all those who bought the 24-line optional display, there's a switch to change over from the standard 12-line format. So instead of showing 960 standard characters in 12 rows, you have the option of displaying 1920

The 32 Switches



The 12 switches in the rear, on the PC board.



The 20 switches under the front name plate.

characters in 24 rows of 80 letters. And there are still more switches that make your terminal a cinch to operate.

Now people aren't sure what turns them on: the low price, the 32 switches, or the DUMB TERMINAL's standard features. Features like a full 12" diagonal screen.

59 data entry keys, arranged like on a typewriter. Compatibility with all popular computers. Simple, quiet operation. An optional numeric key pad. And fast data throughput. All features that make this terminal a perfect video replacement for the old teletypewriter.

The fact is, people keep finding more and more jobs for our DUMB TERMINAL. Because they can do anything within reason — with just a little switching and training. And that's why the DUMB TERMINAL really turns out to be a smart buy. Which may be the biggest switch of them all.



For full information, write: Lear Siegler, Inc., E. I. D. / Data Products, 714 N. Brookhurst St., Anaheim, CA 92803; Tel. (714) 774-1010.

INTERFACE '76
See you in booth 105.

**DUMB TERMINAL.
SMART BUY.**



*U.S. domestic price

**THE \$995 DUMB
TERMINAL CAN BE TRAINED
TO DO PRACTICALLY
ANYTHING.**

PRODUCTS

HEAVY-DUTY DC GEARMOTOR

Series GM9213 provide dc servomotor performance combined with a rugged spur-gear reducer that furnishes five std ratios from 5.9:1 to 728:1. Dia is 2"; length is 3.6", excluding output shaft extension. Output shaft speeds from 2 to 1000 rpm are possible. Gears are sintered iron to precision tolerances and gearbox design strength limit is 1000 oz-in. **Pittman Corp.**, Sellersville, PA 18960.

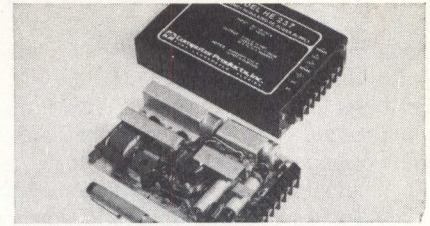
Circle 222 on Inquiry Card

CCD AREA IMAGE SENSOR

A 190 x 244-element sensor for use in imaging and video systems that require low power, small size, sensitivity, and reliability, the CCD-211 contains 46,360 sensing elements organized in an array of 190 vertical columns and 244 horizontal lines. X-Y format of the array provides a 3 x 4 vertical to horizontal ratio. The device dissipates only 100 mW, and includes 190 col of 2-phase vertical analog transport registers, a 200-element horizontal analog transport register, and a low noise output amp. **Fairchild Camera & Instrument Corp.**, CCD Dept., 4001 Miranda Ave., Palo Alto, CA 94304.

Circle 223 on Inquiry Card

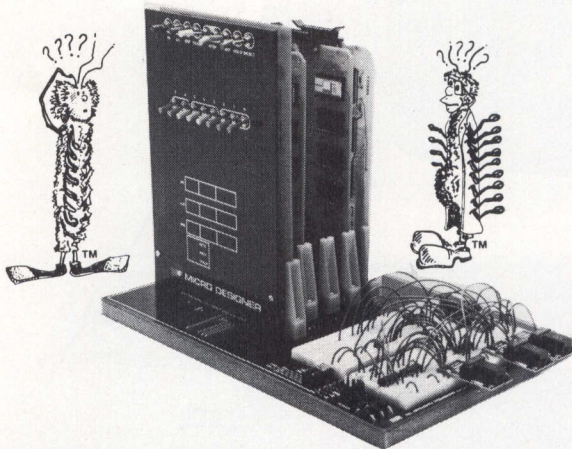
HIGH EFFICIENCY POWER SUPPLY



CMOS logic assists the miniature 25-kHz model HE237 to attain full load efficiency of 75%. Basic specs include output of 5 V, 10 A at 45°C; input of 90 to 130 Vac (180 to 260 Vac in -E model) at 47 to 450 Hz; line and load regulation of $\pm 0.1\%$ max for a 10% change in line and from no load to full load; input isolation of 50 M Ω , 900 Vrms min breakdown; ripple and noise of 25 mV pk-pk max; and derating of 250 mA/°C from 45 to 71°C. Size is 6.5 x 4.5 x 1.5"; weight is 1.7 lb. **Computer Products**, 1400 NW 70th St, PO Box 23849, Fort Lauderdale, FL 33307.

Circle 224 on Inquiry Card

What good is a Micro-Computer if you can't make it work?



Startup time on micro-computers can be a real problem. We know that. That's why we've developed The Micro-Designer. The first complete package of hardware, software and educational materials. All with one purpose: to speed micro-processor system design.

How? By providing the only microprocessor test and development system with solderless breadboarding capabilities. At its heart: the Intel 8080A processor chip, providing all signal functions. A front panel that monitors functions of the microprocessor and allows data I/O with or without an asynchronous terminal. Up to 65 K memory. And the Bugbooks, E&L's innovative approach to self-teaching micro-electronics.

And, when you're ready for your final system, you use the same modules and cards that you learned on. So experiment. Design. Test. Because now there's a system that's caught up with imagination. The Micro-Designer from E&L Instruments. Squander a minute now to write us about it; we'll send you full information. And maybe save you weeks of work.



E&L INSTRUMENTS, INC.

Circuit Design Aids

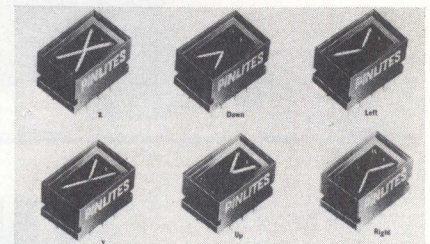
61 First Street, Derby, Ct. 06418 (203) 735-8774

INDICATOR WITH LED LAMP

TEL-LED indicators (series LT-70) for direct, plug-in replacement of T-2 slide-base incandescent lamps, feature long-life solid-state construction, low power consumption and low heat generation, and resistance to wear from normally encountered shock and vibration. A built-in dropping resistor in the indicator permits plug-in replacement of slide base T-1 lamps to reduce maintenance. Choice of red, black, green, white, and yellow bezel permits color coded groups of indicators in small and large jackfields for quick visual identification. **Switchcraft, Inc.**, 555 N Elston Ave, Chicago, IL 60630.

Circle 225 on Inquiry Card

INCANDESCENT DISPLAYS



Capable of showing directional characters \wedge , \vee , $>$, and $<$, as well as letters X and Y, model MD-600XY devices use the four basic segments in the $\frac{5}{16}$ " high char X, with each segment wired so as to display directional information. Available operating voltages are 3, 4, and 5 V; currents are 8, 17, and 18 mA/segment, respectively; and brightnesses are 4500, 9000, and 9000 ft-L. The displays are visible under a wide range of ambient light. **REFAC Electronic Corp.**, PO Box 809, Winsted, CT 06098.

Circle 226 on Inquiry Card

n-CHANNEL MOS ROMs

Two high speed, large scale, factory-programmable memories designed to enhance the speed-effectiveness of MOS micro-processor designs, the Am9208 provides 8192 bits, organized 512 x 8, with access times down to 300 ns, and the -9216 has 16,384 bits, organized 2048 x 8, with access times down to 400 ns. The two units are interchangeable with each other and with 8192-bit erasable p/ROMs. Both operate with 5- and 12-V power supplies, and have two fully programmable chip-selects. Current sinking capability is two TTL loads. **Advanced Micro Devices, Inc.**, 901 Thomson Pl, Sunnyvale, CA 94086.

Circle 227 on Inquiry Card

BILINGUAL TERMINAL

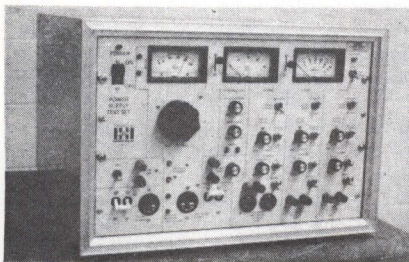


A foreign/dual language terminal (SiR-1000/BL) Farsi and Latin characters displays two char sets as well as all the text writing requirements for two totally different written languages on the same screen. Quality of char presentation is maintained by using a 10 x 15 dot matrix for a total of up to 150 displayable points for each char. **Megadata Computer and Communications Corp.**, 36 Orville Dr, Bohemia, NY 11716.

Circle 228 on Inquiry Card

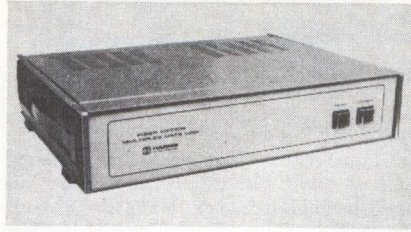
POWER SUPPLY TEST SET

Providing for verification of source effect, max short circuit current, max output current, static load effect, dynamic load effect, recovery time, OVP firing level, and other characteristics, the test set contains three current sinks which can be operated independently and simultaneously. Sink A safely dissipates 2 kW with power supplies from 2 to 40 V and 300 A max; B and C each dissipate 200 W at 2 to 40 V and 30 A max. Each can be amplitude modulated between 10 and 90%. **H & H Automation, Inc.**, 94 Compark Rd, Dayton, OH 45459.



Circle 229 on Inquiry Card

FIBER OPTICS DIGITAL DATA LINK



Model 4359 allows up to 32 asynchronous digital channels operating at any rate up to 50 kilobits/s. For synchronous applications the terminal can accept 32-, 16-, or 8-bit parallel words at significantly higher transfer rates. Data link units are interconnected by two single fiber optics channels. I/O allows convenient handling of up to eight standard RS-232 serial data interfaces; MIL-STD-188C levels are optional. **Harris Communications and Information Handling**, PO Box 37, Melbourne, FL 32901.

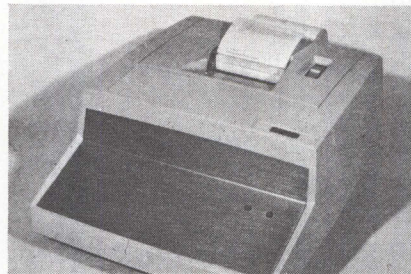
Circle 230 on Inquiry Card

FLOATING-POINT PROCESSOR FOR PDP-11/70

Claimed to have more than twice the speed of previous processors, with typ run times averaging between two and three times faster, the FP11-C processor provides up to 17 decimal digits of accuracy, and is designed to perform more operations in parallel with the -11/70 CPU than did the previous floating-point processor to increase total computer system throughput. It has 46 hardwired instructions, and a set of six 64-bit floating-point accumulators. **Digital Equipment Corp.**, Maynard, MA 01754.

Circle 231 on Inquiry Card

TERMINAL PRINTER



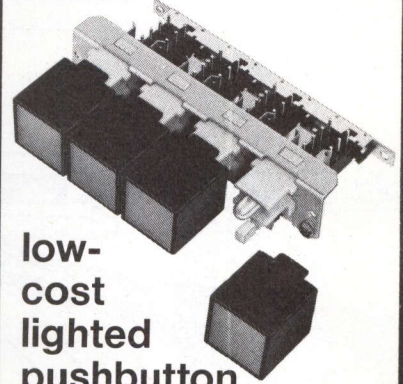
A hardcopy printer, designed for use with terminals having RS-232 communications interfaces, model H prints 32 char/line in a 5 x 7-dot matrix, at up to 40 char/s, with 10 or 12 char/in. Each line can be printed red or black selectively. Transmission speeds of 110, 150, 300, 600, 1200, 4800, or 9600 baud are switch-selectable. An internal strap permits selection of 7- or 8-bit char lengths, one or two stop bits, and odd or even parity. **Informers, Inc.**, 2218 Cotner Ave, Los Angeles, CA 90064.

Circle 232 on Inquiry Card



When it's
your move
check Centralab

NEW!



low-
cost
lighted
pushbutton
switch

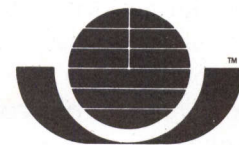
Centralab reliability, low cost and new design freedom can be yours in this new lighted switch. Its T1-3/4 wedge base lamp brings the price way down*. Its many options make it easier than ever to achieve an aesthetically harmonized panel. You get features like these:

- Flat, concave or recessed lenses with uniform light diffusion.
- Eight lens colors.
- PC terminated independent lamp circuit.
- 15mm, 17.5mm or 20mm. spacing options.
- Ganged assemblies through 16 stations.

See your Centralab Pushbutton Distributor or send inquiry card for complete specifications.

* Per station cost at 1000 pieces, \$1.36
...2 PDT switch includes bulb.

Isostat Licensed



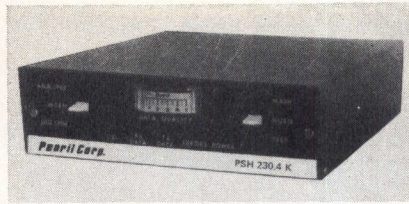
CENTRALAB

Electronics Division
GLOBE-UNION INC.
P.O. BOX 858
FORT DODGE, IOWA 50501

PRODUCTS

230,400-BIT/s SHORT-HAUL MODEM

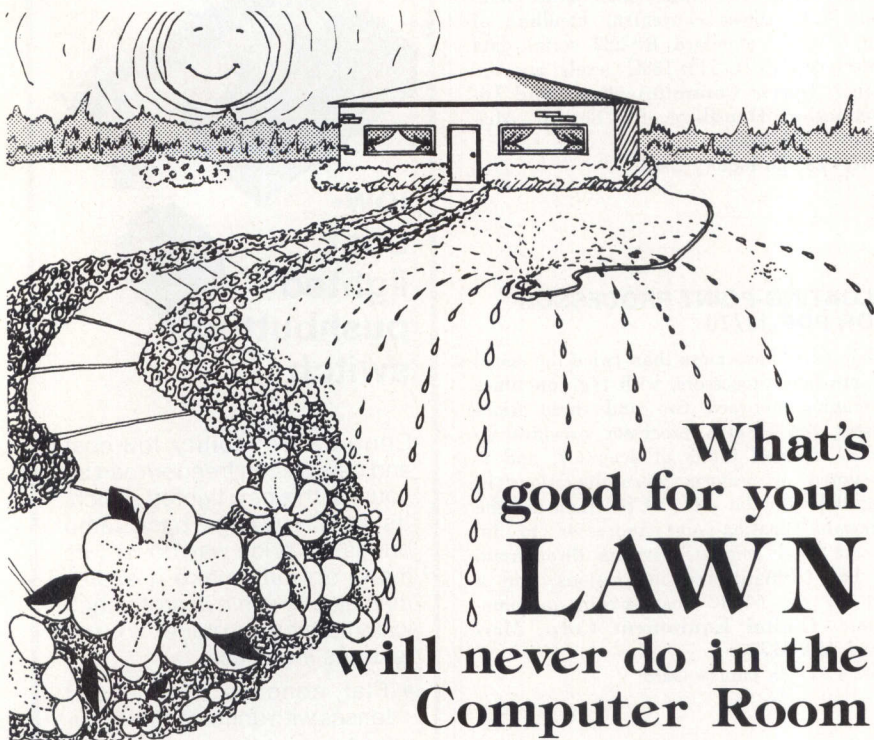
A synchronous modem designed for full-duplex operation over 4-wire shielded, twisted pairs, or dual video coaxial cables, the PSH 230.4 is supplied as std with Bell type 301/303 high speed current interface. Operating distance is up to 5 mi over coaxial cable or up to 2¾ mi over shielded twisted pairs. The modem uses coherent, differentially encoded bi-phase modulation



for improved performance. Typ bit-error rates of $<1 \times 10^{-8}$ can be expected. Features include loopback circuits for both digital and analog circuits and 63-bit test pattern generator for error testing of modem and line. **Penril Corp., Data Communications Div**, 5520 Randolph Rd, Rockville, MD 20852. Circle 233 on Inquiry Card

DIFFERENTIAL TRANSMITTER MODULES

Measuring 2.6 x 3.1 x 0.82" and having std accuracies of ± 4 , ± 15 , or $\pm 30'$ arc, the SCDX40 simultaneously accepts synchro or resolver inputs of 11.8 or 90 V, 400 Hz or 90 V, 60 Hz, and 14-, 12-, or 10-bit binary digital data and provides as an output the sine and cosine of the difference between the two input angles. Std output voltage is 7 Vrms. Output impedance is 10 Ω max. Converters are insensitive to $\pm 10\%$ amplitude and frequency variations and $\pm 5\%$ power supply variations. **Computer Conversions Corp**, 6 Dunton Court, East Northport, NY 11731. Circle 234 on Inquiry Card



What's
good for your
LAWN
will never do in the
Computer Room

WATER & HUMIDITY are just great for Bermuda or St. Augustine, but they will never do around your computer installation. And if Water & Humidity or Heat & Cold do creep into the computer room, how will you know? Easily, with EWA.

EWA monitors what is happening in your controlled environment, even to minute amounts of water and humidity. Should you wish, this system can trigger other mechanisms to protect your precious hardware and software from the dangers of the elements. And EWA is self-supervised, including checking its own power supply.

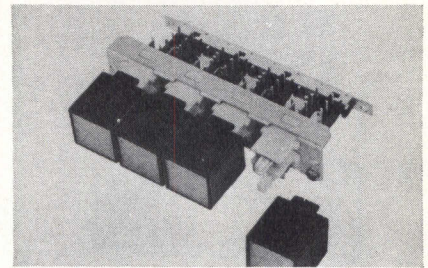
At a most reasonable cost. Isn't your computer installation worth a phone call? Certainly your peace of mind is.



**hydro-temp
controls, inc.**

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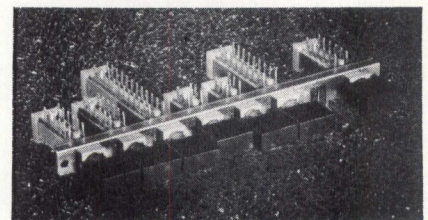
PUSHBUTTON SWITCHES



Three models include lighted design, non-lighted status indicator button, and 5-A line switches. Lighted switches are available with 15-, 17.5-, or 20-mm center-to-center spacings, and concave, recessed, or flat lenses in a choice of eight bright colors. Features include T-1¾ wedge-base lamps, front panel, relampable diffuser lens, filters, and independent PC-terminated lamp terminals. MTBF in multiple-switch assemblies is rated at $>250,000$ operations. **Globe-Union Inc, Centralab Electronics Div**, 5757 N Green Bay Ave, Milwaukee, WI 53201.

Circle 235 on Inquiry Card

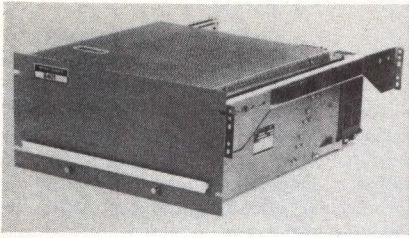
12-POLE, DOUBLE-THROW PUSHBUTTON SWITCHES



Series G switches use modular construction to provide up to 20 stations, 12-pole, double throw, shorting or non-shorting contacts. Basic module offers 0.59, 0.708, and 0.787" spacings. Stator boards are available in 3-, 4-, 6-, 8-, 9-, and 12-pole configurations. All contacts are double wiping and epoxy sealed to protect the switching area. Special functions such as master release, lock-out system, and sequential latching can be supplied. **Seacor Inc**, 598 Broadway, Norwood, NJ 07648.

Circle 236 on Inquiry Card

DISC MEMORY CONTROLLER



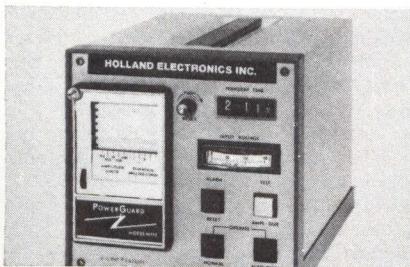
Model 8401 interfaces up to four 5017 disc drives to a DEC PDP-11 minicomputer, providing memory capacities up to 81.92 million 16-bit words. It is functionally equivalent to the DEC RP11-C/RP03 memory system, will operate under applicable software, and has a panel height of 8 $\frac{3}{4}$ " (20.52 cm). With power supplies, it weighs 68 lb (30.87 kg). Op temp range is 10 to 38°C and MTBF is >4000 hr. **Vermont Research Corp**, Precision Park, Springfield, VT 05150. Circle 237 on Inquiry Card

MERCURY-WETTED REED SWITCH

MTHG-2 offers advantages of conventional mercury switches and those of dry reed switching, plus capability of operating in any position. By eliminating the normal mercury pool and replacing it with a minute reservoir of mercury that remains in suspension on one of the reeds, the position of the switch ceases to be a condition for proper operation. Electrical characteristics are 1.2-ms operate time; 1.8-ms release time typ, 0.08- Ω max contact resistance with breakdown voltage of 1 kVdc max. **Hamlin, Inc**, Lake and Grove Sts, Lake Mills, WI 53551. Circle 238 on Inquiry Card

POWER LINE MONITOR

A transient voltage detector and recorder, Power Guard W115 provides a safeguard against computer errors from undetected high speed line transients caused by ac line fluctuations. In use, the monitor is plugged into the same ac line as the computer; when a high speed transient occurs, an audible alarm signals the occurrence and the amplitude and duration of the pulse are simultaneously recorded. A built-in digital clock stops at the exact time of the transient entry. **Holland Electronics, Inc**, 970 E 92nd St, Brooklyn, NY 11236.

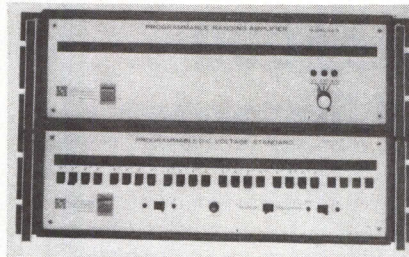


Circle 239 on Inquiry Card

INTELLIGENT REMOTE BATCH TERMINAL SYSTEM

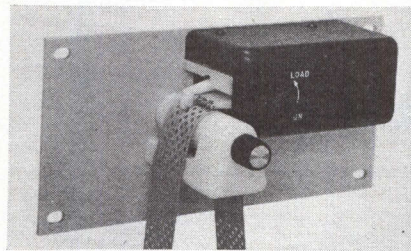
Communicating at speeds to 4800 baud with a 300-card/min. reader and 300-line/min. printer, the system 525 emulates Burroughs DC1100, Univac 1004, CDC UT200, Honeywell 115, and IBM 2700, 3780, and 360/25+ HASP. Standalone features include card reader-to-card punch and print utilities. Other terminal system peripherals include teleprinters, CRTs, a 100- to 285-card/min. punch, and interfaces for slower card punches. **Singer-M & M Computer Industries, Inc**, 2201 N Glassell St, Orange, CA 92665. Circle 240 on Inquiry Card

PROGRAMMABLE RANGING AMPLIFIER



Model RA-3 extends the digitally controllable range of the 501J voltage standard to 200 Vdc in 1-ppm increments (200 μ V) at speeds of 500 μ s (settled to 0.01% of value). Four switch-selectable ranges permit 200 Vdc in 200 μ V steps, 100 Vdc in 100 μ V steps, 10 Vdc in 10 μ V, or 100 mV in 100 nV increments. Accuracy is \pm 0.01% of programmed value, noise is <0.0005% of range, and stability is 0.0001%/24 hr, 0.0025%/90 days, or 0.005%/yr. **Electronic Development Corp**, 11 Hamlin St, Boston, MA 02127. Circle 241 on Inquiry Card

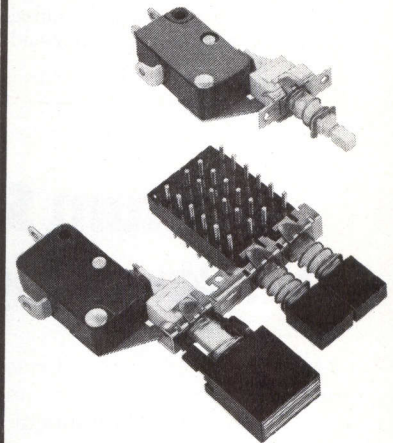
PAPER TAPE READER ASSEMBLY



Capable of manual encoding from operator side of panel by means of transport shaft control knob, and of speeds up to 150 char/s, this 8-channel starwheel sensing reader is available with electromechanical drive unidirectionally at 35 char/s, step motor drive bidirectionally at 150 char/s, or synchronous motor drive at 60, 72, or 105 char/s. Sensing contacts are compatible with RTL, DTL, TTL, and HTL as well as relay systems. All switch contacts are wired to a 24-pin Amphenol connector. **Data Peripheral, Inc**, 14 Porter St, Hackensack, NJ 07601. Circle 242 on Inquiry Card



When it's
your move
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5 amp pushbutton switch

You'll meet even the most stringent requirements with this new line switch. It's UL listed for TV-5 rating (120V, 5A, 78A peak in-rush current).

Other features include:

- Furnished as a single station or for left or right mounting on any Centralab pushbutton switch assembly.
- Three circuit options — SPDT, SPST, normally open and SPST, normally closed.
- Button options include lighted, non-lighted or status indicator button (shown above).

See your Centralab Pushbutton Distributor or send inquiry card for complete specifications.

Isostat Licensed



CENTRALAB

Electronics Division

GLOBE-UNION INC.

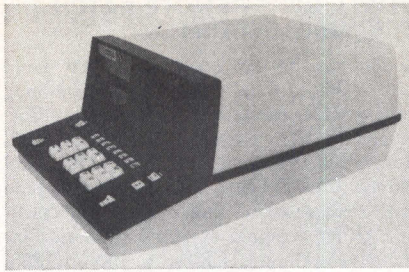
P.O. BOX 858

FORT DODGE, IOWA 50501

PRODUCTS

EDITING RECORDER

The microprocessor-driven AJ 730 combines a reliable Philips-type cassette tape drive with control electronics in a compact desktop console to handle data preparation, word processing, and teleprocessing tasks. In offline mode, an operator can record data, use search and line edit features to correct and update entered material, and print as many copies of data as required. Online the device operates as a store-and-



forward device, and as the central unit in an automatic data collection network. **Anderson Jacobson, Inc.**, 1065 Morse Ave, Sunnyvale, CA 95050. Circle 243 on Inquiry Card

Datum Series 4000 Universal Digital Recorder

The Datum Series 4000 Universal Digital Cassette Recorder performs similar functions to any full-sized tape memory system, but is much more economical when additional sources of smaller capacity are needed. Model 4000 stores more information and transfers it more accurately than any competitive product. Serves all computer-oriented, communication-oriented and stand-alone recording-oriented requirements.

I/O's include:

For Communications: RS232 data terminal or data set, switch-selectable baud rates to 9600 baud.

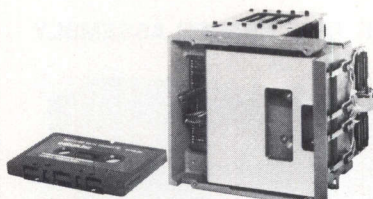
For Peripherals: 8-bit parallel interface, includes strobe line accepting inputs to 1500 8-bit characters per second. Includes custom interfaces to desk-top calculators and portable computers.

For Paper-Tape Replacement: Teletype current-loop interface at 110 baud. H.S. Paper Tape Reader/Punch Emulator to PDP-11 (embedded I/O).

For Stand-Alone Recording: Accepts outputs from Data Loggers, DVM's, A to D Converters, Data Communications Line Monitors, Medical Instrumentation, Range Measuring Systems, Data Acquisition Systems, etc.



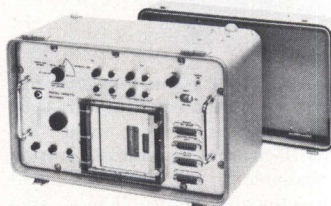
Model 4000-200



Model 4200 Digital Cassette Transport



Model 4000-300



Model 4000-400 Portable Ruggedized Version

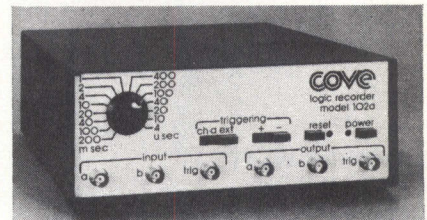
datum inc

1363 South State College Boulevard, Anaheim, California 92806
Telephone: 714/ 533-6333 • TWX 910/592-1289

1.8- AND 15-DEG STEPPING MOTORS

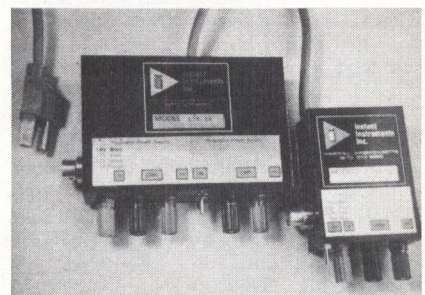
Series 600 Slo-Syn variable reluctance motors have a 15-deg step angle and are completely encapsulated for max durability. Permanent magnet types provide either a 1.8-deg step angle in the full-step mode or a 0.9-deg angle in the half-step mode. They can be driven to over 20,000 steps/s using a properly designed drive circuit. Holding torque ratings from 27 to 150 oz-in. Shielded precision-grade ball bearings assure max reliability and long life. **The Superior Electric Co.**, Bristol, CT 06010. Circle 244 on Inquiry Card

OSCILLOSCOPE STORAGE ACCESSORY



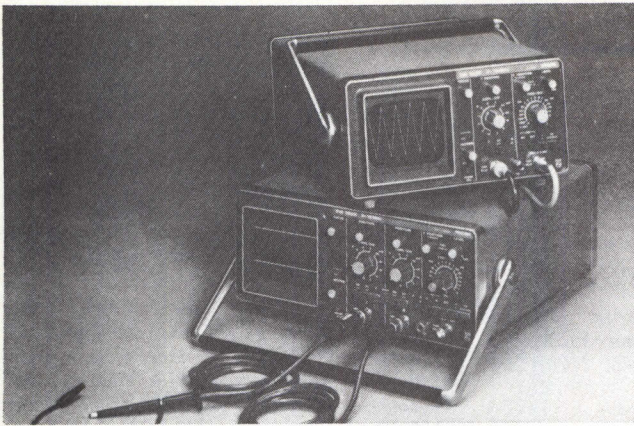
Converting any oscilloscope into a storage scope, the model 102A logic recorder was developed as a high speed, digital data acquisition system. Features include 50 sample points/div, input speeds from 4 μ s to 200 ms/div, and 2-channel operation. It is loaded by pressing a reset button and providing either external or internal trigger pulse. Output is displayed at the constant rate of 100 μ s/div, independent of the speed at which data were recorded. Output voltage is 0 to 5 Vdc and rep rate is 2000/s. **Cove Electronics Inc.**, San Diego, CA 92111. Circle 245 on Inquiry Card

TRIPLE-OUTPUT LAB POWER SUPPLIES



Miniature LT series feature variable dual-tracking output voltages and a preset output (1% accuracy) for logic use. Three models have variable dual voltages from ± 9 to ± 18 Vdc and a preset 5 Vdc at respective current outputs from 100 to 1000 mA. A color-coded knob and ring reference gives visual voltage control resolution accuracy to within 2%. Regulation is 0.05% line and 0.01% load. **Instant Instruments, Inc.**, 306 River St, Haverhill, MA 01830. Circle 246 on Inquiry Card

COMPACT, LIGHTWEIGHT OSCILLOSCOPES

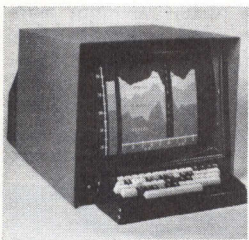


With 15-MHz bandwidth and 2-mV sensitivity, the single-trace PM3225 weighs 8 lb, 2 oz and measures 4.72 x 9 x 12.5", while the dual-track -3226 weighs 9 lb, 10 oz, and measures 4.72 x 10.8 x 12.5". Both offer adjustable-level, automatic, line, and automatic TV line and frame sync pulse triggering. External triggering is also possible. Input impedance of vertical and horizontal channels is 1 M Ω /25 pF; risetime is 25 ns. Dynamic range is 24 divisions for sine wave signals up to 1 MHz. A range of 18 sweep speeds in 1-2-5 sequence are available on the time-base switch from 500 ns to 0.2 s. Chopped or alternate functions are possible for all time-base settings on the dual-trace unit with a 400-kHz chopper frequency. **Philips Test & Measuring Instruments, Inc, a North American Philips co, 400 Crossways Pk Dr, Woodbury, NY 11797.**
Circle 247 on Inquiry Card

MIL-RANGE HYBRID, 12-BIT CMOS A-D CONVERTER

Providing max conversion time of 175 μ s to 12-bit accuracy while consuming only 55 mW, the MN5250 is packaged in a low profile, hermetically sealed 24-pin DIP, and is specified for operation from \pm 12-V battery supplies. For remote battery pack operation (such as long-term data logging) a third supply pin, which connects power to the CMOS logic section only, is provided. Data can then be retained in the logic section while the \pm 12 V power to the analog section is totally disabled during quiescent periods between conversions. Four analog input voltage ranges are: -50, 0 to -10 V; -51, +5 to -5 V; -52, +10 to -10 V; and -53, 0 to 10 V. All have a 50-k Ω input impedance except the -52, which is 100 k Ω . Output code is binary, offset binary, or complementary binary depending on model. **Micro Networks Corp, 324 Clark St, Worcester, MA 01606.**
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INTELLIGENT COLOR CRT DATA TERMINAL

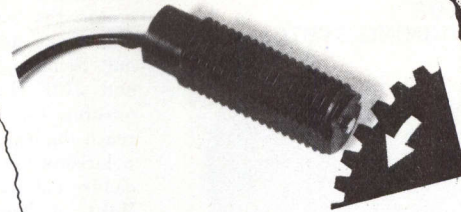


Available in a small easy-to-use single package configuration, the Intecolor 8001 terminal contains an 8080 microprocessor for user programmability, 8-color (seven colors plus black) CRT readout, 19" color shadowmask CRT, keyboard, and the Intecolor 9 sector-convergence system. The system includes an 80-char x 25-line format with ASCII char plus sockets for an optional 64 special programmable char. Also included are ROM software, 4K x 8 RAM, sockets for additional erasable p/ROM, and space for up to 32K of RAM. An RS-232 serial interface provides simple I/O with selectable baud rates up to 9600. Options include a limited graphics mode, an 80-char x 48-line format, 17 and 26" low and 16, 19, and 26" high-resolution CRTs, and background color. **Intelligent Systems Corp, 2405 Pine Forrest Dr, Norcross, GA 30071.**
Circle 249 on Inquiry Card

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sideration. Two 18" PVC lead wires
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CIRCLE 69 ON INQUIRY CARD

DIGITAL SYSTEMS SOFTWARE ENGINEER

You will become proficient in conducting and/or coordinating the development of software requirements for industry application.

Projects will entail the definition and development of software basics and strategy-executives, utilities, drivers, handlers and language translators for real time process control systems.

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Please send resume and salary requirements to:

John Hawkins
**TAYLOR INSTRUMENT PROCESS
CONTROL DIVISION**
95 Ames Street
Rochester, New York 14601

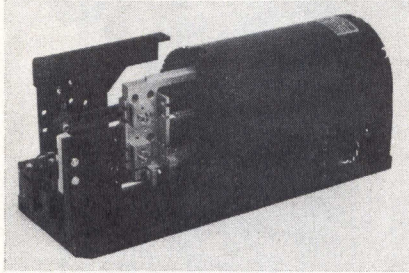


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CIRCLE 902 ON INQUIRY CARD

PRODUCTS

LINEAR MOTOR HEAD-POSITIONING SYSTEM



Designed as an integral unit for positioning read/write heads on high performance disc drives, model 545 uses patented, radially aligned, ceramic magnet construction and has a "Winchester" style 6-bearing carriage assembly for mechanical stability. Supplied complete with velocity and optical position transducer, the system has a 200-track positioning time of 60 ms. Force constant of the motor is 1.5 lb/A, coil dc-resistance is 1.5 Ω , and max continuous rms current rating is 5 A. **Information Magnetics Corp**, 5743 Thornwood Dr, Goleta, CA 93017. Circle 250 on Inquiry Card

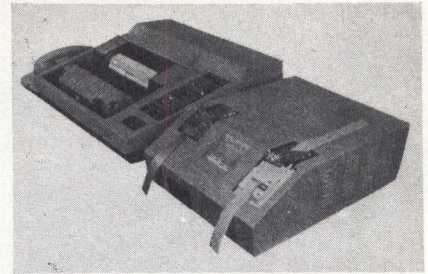
DIMMER INDICATOR LIGHTS

A shutter-dimming device permits an operator to regulate brightness by turning a lens cap. Series includes subminiature, miniature, and polaroid indicator models. Assemblies in 11, 108, 174, 203, and 209 series have rotatable shutters that decrease the size of three triangular openings from max light to complete blackout. Semiblackout unit (2, 109, 175, 203, and 210) shutters have a small central opening that permits a spot of light to reach the lens. Polaroid models have a light polarizing filter that is rotated over the incandescent bulb to reduce the glare. **Dialight, a North American Philips co**, 203 Harrison Pl, Brooklyn, NY 11237. Circle 251 on Inquiry Card

ELECTRONIC DATA PRINTER

Using nonimpact electrosensitive print-heads, EDP1600 provides coincidental printout with digital display in applications involving digital measuring sets, counters, calculators, and computers. Std unit prints 16 numeric char/line from 4-bit binary TTL inputs at up to 2 lines/s; ASCII alphanumeric are available. Char are numeric 5 x 7 dot-matrix type, 0.11 x 0.07". Printout paper is std 2.375"-wide electrosensitive type. **C-Tek, Inc**, 4 Railroad Ave, Wakefield, MA 01880. Circle 252 on Inquiry Card

NC TAPE PREPARATION AND EDITING SYSTEM



The NC-9 system permits high speed original typing, stores all typewritten material on tape, corrects errors electronically from the typewriter keyboard without erasing, and reads back the tape to produce perfect finished copy at speeds of >30 char/s or 350 words/min. It uses TI Silent 700 or DECwriter II printer and includes editing controls on the keyboard. The punch/reader features microprocessor circuitry for max reliability and maintenance-free operation. **International Computer Products, Inc**, 2925 Merrell Rd, Dallas, TX 75229. Circle 253 on Inquiry Card

TRACKING S-D CONVERTER

SDC-520 series are available in 10-, 12-, and 14-bit resolutions with a worst case accuracy due to all conditions of up to ± 4 min. ± 0.9 LSB (for 14-bit resolution). Improved dynamics achieve 10 rps tracking at 14 bits with true $K_a = 40,000$. Std options include all normal synchro and resolver format inputs, 0 to 70°C or 55 to 105°C op temp, and choice of TTL, CMOS, or low-power Schottky logic. Signal and reference voltage or frequency variations do not affect accuracy. **ILC Data Device Corp**, Airport International Plaza, Bohemia, NY 11716. Circle 254 on Inquiry Card

EDITING CAPABILITY OPTION FOR CRT TERMINALS

An option that can be added to any of the company's current terminals equipped with a batch transmit capability permits insertions or deletion of either a complete line of text or a line fragment from cursor position to end of line, affording more rapid text editing with minimum keystrokes. A text wraparound feature allows the operator to open the text at any point and insert an arbitrary amount of additional data. **Ann Arbor Terminals, Inc**, 6107 Jackson Rd, Ann Arbor, MI 48103. Circle 255 on Inquiry Card



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NCR

Terminal Systems Division—Cambridge

NCR's Point-of-Sale Terminal Systems Division in Cambridge, Ohio has several opportunities for computer professionals in the development of present and next generation retail terminal systems.

SYSTEMS ENGINEERS

Systems Engineers needed for the design of Advanced Retail Terminal Systems. Responsibilities will include definition of business system requirements, architecture concepts, performance criteria, design verification, and implementation for the restaurant and hotel/motel vocational systems. BS/MS in Electrical Engineering or Computer Science. Position requires a minimum of 5-10 years experience in digital systems design. Candidates' background should include direct experience in both hardware and software design/development. Knowledge of communications control procedures and operations evaluation techniques would also be helpful.

Candidates should have a BS/MS EE degree or equivalent plus 3-6 years experience in the above areas.

These positions offer a challenging professional environment as well as a very pleasant family life style in this rural, east central Ohio location.

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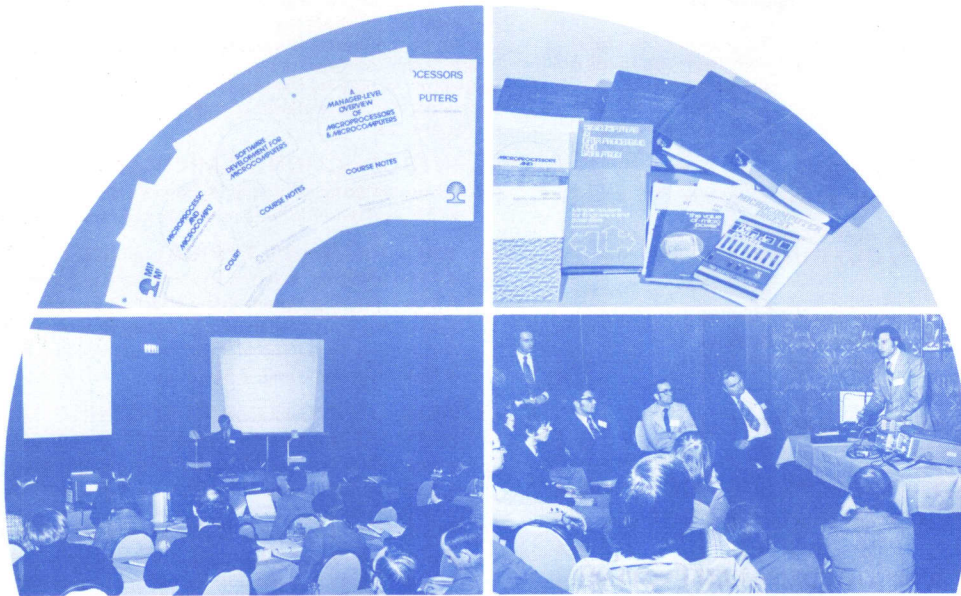
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EDUCATION IS OUR BUSINESS

MICROCOMPUTER CONGRESSES

COURSE 102: 1 DAY – MONDAY

MICROPROCESSORS/MICROCOMPUTERS

A Comprehensive Technical Introduction and Survey

PREREQUISITE: An engineering/scientific background is assumed.

This course provides managers, system designers, engineers and research personnel with the background knowledge and conceptual tools required to direct the development, purchase and implementation of microprocessor-based products and systems.

Throughout the course, applications examples provide concrete illustrations of the concepts presented and are drawn from the fields of military, communications, instrumentation, industrial control, and biomedical applications.

1. INTRODUCTION

- What is a microprocessor? A microcomputer? ■ Suitable and unsuitable applications ■ Alternatives and tradeoffs

2. APPLICATION EXAMPLE – A HEART MONITOR SYSTEM PROVIDING AN OVERVIEW BY ILLUSTRATING:

- Microprocessor functions (replacement of hard-wired control logic, data analysis, operator interface and display)
- Hardware/software and cost tradeoffs.
- Typical system configuration

3. REVIEW OF RELEVANT FUNDAMENTAL COMPUTER CONCEPTS

4. BASIC ELEMENTS OF A MICROPROCESSOR SYSTEM

- CPU, RAM, ROM, PROM ■ I/O structures and techniques (hardware and software)

5. DEVELOPMENT OF A MICROCOMPUTER SYSTEM

- Analysis of system requirements ■ Selecting the best microprocessor for an application ■ Design cycle (why it differs for microprocessors) ■ Alternative software development techniques
- Hardware aids and software support ■ System integration and debug methods

6. MULTI-MICROPROCESSOR SYSTEMS

- Hardware ■ Software ■ Applications

7. TECHNICAL SURVEY OF MICROPROCESSORS INCLUDING:

Intel, Fairchild, Motorola, National, Rockwell, SMS, T.I., Toshiba and others including the new LSI Minicomputers, e.g. Dec LSI-11.

8. HOW TO GET STARTED

- Equipment requirements ■ Personnel requirements
- Sources of information and support ■ Pitfalls to be avoided

9. ESTIMATION OF COST

- Education ■ System design ■ Software development
- Production

COURSE 134: 2 DAYS – TUESDAY/WEDNESDAY

SOFTWARE DEVELOPMENT & APPLICATIONS TECHNIQUES FOR MICROCOMPUTERS

PREREQUISITE: Course 102 or prior knowledge (but not necessarily hands-on experience) with microcomputers.

This course provides the details of programming microprocessors and interfacing them to external devices. The software development section of the course is extremely useful for logic designers who need to apply microprocessors as an alternative to hardwired logic circuits. Equivalent programs for Intel, Motorola, and National Semiconductor microprocessors are developed step-by-step with the participation of the attendees.

1. INTRODUCTION TO MICROCOMPUTERS

- Fundamental concepts ■ Hardware/software trade-offs
- How software affects microprocessor selection

2. PROGRAMMING TYPICAL FUNCTIONS:

- Flow-charting ■ Assembly language programming
- Loading the program into PROM ■ Execution
- Creating control signals and pulses ■ Monitoring input lines and testing bit patterns ■ Serial data block transmission
- Multi-line handling techniques

3. DEVELOPING COMPARISON PROGRAMS FOR REPRESENTATIVE MICROCOMPUTERS

- Intel 4040 ■ Intel 8080 ■ Motorola M6800
- National Semiconductor IMP-16 ■ Rockwell PPS-4

4. PL/M HIGH-LEVEL MICROCOMPUTER LANGUAGE

- Characteristics, advantages, disadvantages
- Implementation techniques using computers and simulators

5. USING DEVELOPMENT SOFTWARE & SYSTEMS

- Editors, assemblers, compilers, loaders, debuggers
- Operating systems ■ Intellec, IMP-16L, Assembler, Exorciser
- Logic analyzers

6. INTERFACING TECHNIQUES

- I/O ports ■ Interrupts, priority, vectoring ■ DMA circuits
- Use of LSI packages ■ Hardware/software integration

7. CASE HISTORY: APPLICATION OF MICROPROCESSOR-CONTROLLED DATA-COMMUNICATIONS MULTIPLEXER SYSTEM

- I/O hardware/software tradeoffs ■ Interrupt techniques (block diagrams/schematics) ■ Software configuration (flowcharts)
- Software development and testing procedure ■ Problems encountered and how they were solved

8. TECHNIQUES FOR OTHER APPLICATIONS

- Industrial controllers ■ Intelligent terminals ■ Signal Processing
- Aerospace display systems

COURSE 101: SPECIAL ONE DAY UPDATE – FRIDAY

A MANAGER-LEVEL OVERVIEW OF MICROPROCESSORS & MICROCOMPUTERS

1. INTRODUCTION

What are microprocessors, microcomputers, minicomputers?

- Historical evolution of digital electronics, minicomputers and microprocessors. ■ Suitable and unsuitable applications

2. IMPACT OF MICROPROCESSORS

- Product marketing philosophy ■ Development costs
- Production-related costs (assembly, inventory, testing, etc.)

3. APPLICATIONS OF MICROPROCESSORS AND EFFECT ON MARKETS

- Consumer goods (e.g. automobiles and appliances)
- Communications ■ Instrumentation, measurements and test equipment ■ Industrial control ■ Computer and peripherals
- Military and aerospace electronics

4. MANAGEMENT DECISIONS IN APPLYING MICROCOMPUTERS AND MINICOMPUTERS

- Should a microcomputer be used? ■ Alternatives and tradeoffs (microcomputer vs minicomputer vs hardwired systems) ■ Management considerations in the selection process

5. ESTIMATING COSTS

- System design ■ Software development ■ Production costs
- Maintenance and inventory costs ■ Training costs

6. SURVEY OF DEVICES AND SYSTEMS AVAILABLE

7. HOW TO GET STARTED

- How to initiate development ■ Pitfalls to be avoided
- Personnel requirements and desirable experience
- Information sources ■ Equipment requirements

COURSE 201: 2 DAYS – TUESDAY/WEDNESDAY

MICROPROCESSORS IN AEROSPACE AND MILITARY SYSTEMS

PREREQUISITE: An engineering/scientific background is assumed.

This intensive short course is specifically designed to meet the needs of project managers, design engineers, research personnel and contract officers who are now or will be involved in the specification, design, advanced research, or procurement of electronic systems for military applications. This course will provide these personnel with the knowledge needed to determine the advisability of incorporating microprocessors in their systems, to evaluate and select the proper microprocessor, and to develop microprocessor systems with necessary reliability and performance for military applications.

1. INTRODUCTION

- What is a microprocessor? A microcomputer?
- The micro vs. the rugged mini
- The micro vs. mil-spec digital logic

2. BASIC ELEMENTS OF A MICROPROCESSOR SYSTEM

- CPU
- Memory – RAM, ROM, PROM, Core, others
- I/O structures and interfacing to peripherals and sensors

3. THE LSI TECHNOLOGIES AND THE MILITARY AND AEROSPACE ENVIRONMENT

- LSI Technologies Review: TTL, SOS, CMOS, I^2L , PMOS, NMOS
- Hybrid Technologies
- Memory technologies
- Comparison of technologies in terms of environmental considerations, including: Radiation hardness, noise immunity, temperature, humidity, shock and vibration, power instability

4. STANDARDIZATION

5. TECHNICAL SURVEY & COMPARISON OF MILITARY MICROPROCESSORS

6. DESIGN CONSIDERATIONS IN MILITARY/AEROSPACE MICROPROCESSOR SYSTEMS

- Systems level considerations
 - Flexibility, maintainability, mobility, reliability (MTBF),
 - Development time and cost
 - Software vs. hardware cost
- Electronics level considerations
- Testing and maintenance

7. DEVELOPMENT OF A MICROPROCESSOR SYSTEM

- Selecting the best microprocessor for an application
- Design cycle (why it differs for microprocessors)
- Alternative development techniques
- High level languages (and Structured Programming)
- System integration and debug methods
- Testing

8. APPLICATIONS OF MICROPROCESSORS IN MILITARY/AEROSPACE SYSTEMS

- Avionics systems
- Tactical military systems
- Command and control systems
- Communications systems
- Electronic warfare applications
- Shipboard systems

9. ADVANCED SYSTEM CONFIGURATIONS

- Failsafe and failure tolerant systems
- Multi-processors and multi-computers

COURSE 187: 2 DAYS – THURSDAY/FRIDAY

BIT-SLICE MICROPROCESSORS, PLA'S AND MICROPROGRAMMING

PREREQUISITE: Course 102 or basic understanding of computers, programming, and digital logic.

This course provides project engineers, logic engineers and programmers with an understanding of the implications of the bit-slice microprocessors and PLA's, specific techniques for designing and implementing systems using these devices. Technical and economic tradeoffs between random logic, bit-slice microprocessors, single-chip microprocessors, and PLA's and suitable and unsuitable applications for each will be emphasized.

The course stresses actual microprogram implementation techniques as they apply to these devices and illustrates them with specific case studies. This course will thus have an immediate cost-effective impact on the attendee's job function by providing him with both general tradeoff considerations, technical visibility of existing devices, and specific implementation techniques.

1. INTRODUCTION AND BASIC PRINCIPLES

- Alternatives to microprogramming (hardwired logic, PLA's, software)
- Cost/speed tradeoffs
- Bit-slice vs simple chips
- Bit-slice organizations
- Microprogramming
- Programmable logic arrays

2. APPLICATIONS OF MICROPROGRAMMING AND BIT-SLICE MICROPROCESSORS

- Control of special purpose digital systems
- High speed functions (e.g. signal or image processing)
- Extending computer instruction sets
- Emulation
- Microdiagnostics and fault-tolerance
- Multiprocessors
- Multi-level hierarchies of processors

3. MICROPROGRAMMING TECHNIQUES

- Design techniques (e.g. pipe lining)
- Microprogram development aids (e.g. microassemblers)
- Microprogramming existing microcomputers (e.g. LSI-11)

4. SURVEY OF MICROPROGRAMMABLE DEVICES

- AMD 2900
- Fairchild 9400 Macrologic
- Intel 3000
- TI SPB-0400
- Monolithic Memories 6701
- National IMP-16
- Western Digital MCP 1600
- Motorola 10800

5. HOW LSI BIT-SLICES AFFECT MICROPROGRAMMING TECHNIQUES & TRADEOFFS

6. CASE STUDIES IN BIT-SLICE MICROPROGRAM APPLICATIONS

- Real-time controller design
- CPU design

7. INTRODUCTION TO PROGRAMMABLE LOGIC ARRAYS

- What are PLA's and FPLA's?
- PLA vs. hardwired logic vs. microprocessor
- Cost and speed tradeoffs
- Survey of PLA's and FPLA's

8. IMPLEMENTATION OF APPLICATIONS FOR PLA'S

- Combinatorial logic (e.g. code conversion)
- Sequential logic (e.g. digital control)
- Use with bipolar microprocessors

Each course includes:

Lectures, lecture-coordinated course notes, extensive reference materials, luncheon and coffee breaks.

Microcomputer Demos follow each course (4:30 to 6:00) and provide the opportunity for informal hands-on-experience.

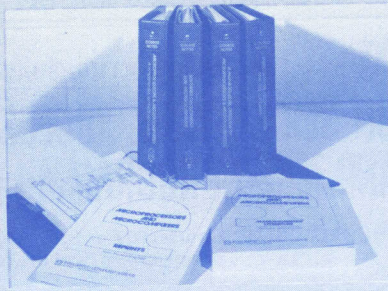


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Course 105: Fundamental Concepts of Minicomputers and Microcomputers

Course 106: Mini-Microcomputer Real-Time Software;
Systems Techniques and Application

Course 134: Software Development and Applications Techniques
for Microcomputers

Course 168: Motorola's 6800 vs. Intel's 8080

Course 187: Bit-Slice Microprocessors, PLA's and Microprogramming

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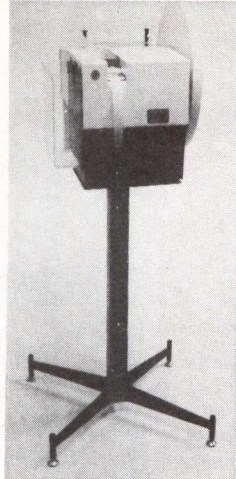
For additional information and prices, contact Ms. Julie Schneider at the above address or call:

(213) 559-9265

RECEIVE ONLY, NONTYPING REPERFORATOR

A free-standing tape punch, series B400 features a reliable and unusually durable punching mechanism capable of handling 5-, 6-, or 8-level inline feedhole tape, or 6-level advanced feedhole, paper, polyester, or laminated or coated composites, in rolls up to 14" in dia. The punch is switch-selectable for any two std speeds up to 30 char/s, and has a 64-char buffer memory that permits instant reception without waiting for motor start-up. Parallel-bit and std serial-bit interface options of RS-232-C, 20/60 mA dc, MIL-188C are available. Input power is 115/230 Vac. Ease of access to interface cards makes maintenance simple. Other features include power, data light, and low tape alarm lights; back space, rubout, and feedout buttons; and V tear-off to indicate tape direction. **Extel Corp.**, 310 Anthony Trail, Northbrook, IL 60062.

Circle 256 on Inquiry Card

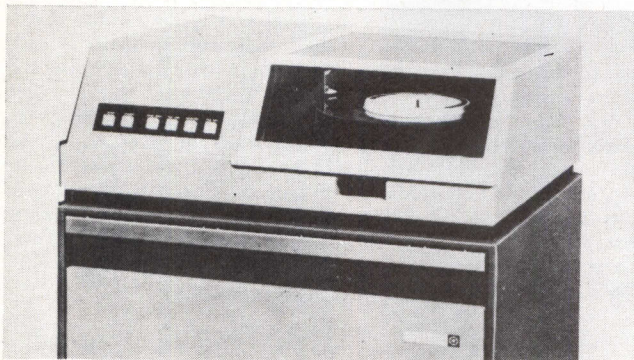


DATA TERMINAL

The 40/4, a private-line offering designed for compatibility with existing software-supported systems for display devices, features binary synchronous protocol at speeds of 2400 and 4800 bits/s. The unit permits clustering of keyboard display and line printer terminals in combinations of up to 24 displays and 12 printers max, enabling users to take advantage of the economies obtained by clustering several terminals on a common controller. Its interactive mode of operation makes it attractive for computer I/O applications such as inquiry response, data entry, and retrieval. Additional features include computer-controlled display, formatting and data entry, full char impact printing, built-in self-diagnostics, and modular construction. **Teletype Corp.**, 5555 Touhey Ave, Skokie, IL 60076.

Circle 257 on Inquiry Card

30-MEGABYTE DISC AND CONTROLLER



A 10-platter, moving-head disc system for Data General Nova and Eclipse, Digital Computer Controls D-116, and Keronix IDS-16 minicomputers, the 4091-N has a storage capacity of 30×10^6 bytes with a recording density of 2200 bits/in. Avg random access time is 55 ms; data are recorded on 20 surfaces at 100 tracks/in., 203 tracks/surface. Transfer data rate is 312 kilobytes/s; write frequency is 5 MHz $\pm 0.3\%$. Storage media are IBM 2316-type disc packs which rotate at 2400 rpm. The single circuit board controller is a fully embedded element in the host CPU and requires no external interface units. It cables directly with up to four disc drives. The system is fully compatible with Data General software, complete with diagnostic and reliability programs. Measurements are 24 x 30 x 38" (60.96 x 76.2 x 96.52 cm). Weight is 400 lb (181.44 kg). **Datum, Inc.**, 1363 S State College Blvd, Anaheim, CA 92806.

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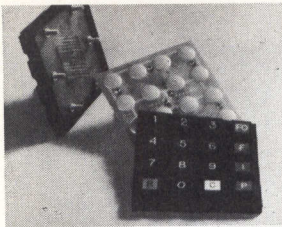
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CIRCLE 72 ON INQUIRY CARD

PRODUCTS

MIL-SPEC SEALED KEYBOARD

The EM keyboard is based on a patented design in which the keyboard is activated by means of a mylar sheet in which "bubbles" invert through a spacer to make contact with a PC board. Environmental sealing is provided by a 1-piece silicone



rubber boot with interchangeable plastic key-legend inserts. Electrical contact is made between the mylar bubbles, which have a conductive undercoating, and an etched, gold/nickel-plated epoxy-glass PC board. System interconnection is through wirewrap pins that protrude from the rear of the keyboard. The keyboard meets environmental requirements of MIL-STD-202 for shock, vibration, salt spray, and moisture, and -STD-810 for dust resistance. The keyboard arrays key on 3/4" centers and can be made with any number of keys. Protrusion above the mounting panel is 1/2". Panel mounting is by means of threaded mounting studs.

The keyboard meets environmental requirements of MIL-STD-202 for shock, vibration, salt spray, and moisture, and -STD-810 for dust resistance. The keyboard arrays key on 3/4" centers and can be made with any number of keys. Protrusion above the mounting panel is 1/2". Panel mounting is by means of threaded mounting studs. **Chomerics**, 77 Dragon Court, Woburn, MA 01801. Circle 259 on Inquiry Card

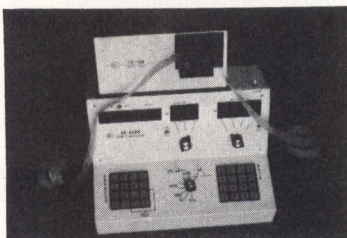
UPS AND STANDBY SYSTEMS

To provide clean continuous electrical power for critical equipment during line power failure, seven UPS models cover 1 ϕ operation from 1.2 to 10 kVA and 3 ϕ operation from 7.5 to 30 kVA; six standby power system models cover 1 ϕ operation from 1.2 to 10 kVA, and 3 ϕ operation from 7.5 to 15 kVA. In UPS systems, line power simultaneously charges a 120-V battery bank and supplies power to an inverter, which supplies power to the load through a sinusoidal constant voltage transformer, regulating output voltage to within $\pm 1/4\%$ of nom, screening out line noise, and maintaining a near-pure sinusoidal wave shape. In event of internal component failure, a mechanical bypass switch automatically transfers the load directly to the ac input line with a max interruption of approx 100 ms; in automatic operation, a solid-state switch completes the transfer in 4 ms. **Sola Electric**, div of **Sola Basic Industries**, 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 260 on Inquiry Card

p/ROM SIMULATOR

In addition to keyboard data entry and text editing capability, the RS-4000 provides dual-channel simulation, a 6-function text editor, and pin-for-pin compatibility with industry std p/ROMs, including chip-enable signals. Each channel, independent of the other channel, will simulate

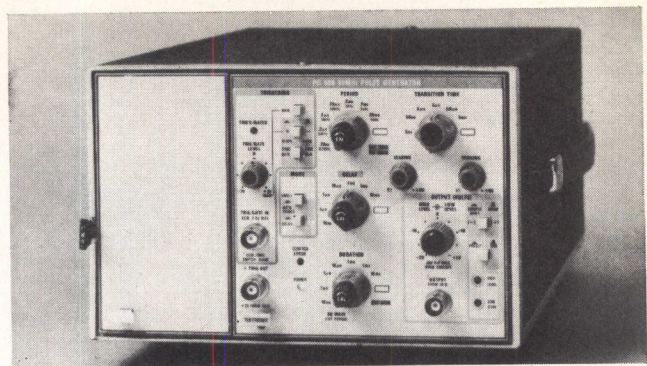


a 32 x 8, 256 x 4, or 512 x 4 p/ROM. Memory channel 1 will simulate a 512 x 8 p/ROM. When channel 1 is operating as a 512 x 8, channel 2 is inactive. Data and addresses are entered simply by pushing the respective keyboard digit.

Visual pointers on the data and address displays indicate the position at which the next keyboard digit will enter. Data are written into memory only when a data key is pushed. Address cycling causes no data alteration. Interface to the unit is via 16- and 24-pin cable. It may be loaded via the keyboard, preprogrammed p/ROM, or TU-150 tape reader. **ElectriCom Co**, PO Box 1235, Hawthorne, CA 90250.

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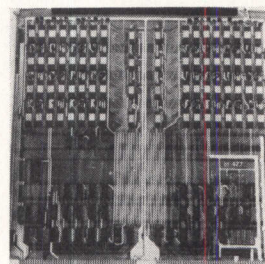
PULSE GENERATOR



The PG 508T has a true 50- Ω output, providing the high level output required to drive CMOS (20 V in a ± 20 -V window to hi Z and 10 V to 50 Ω), and features a control error light that warns of improperly set switch or variable controls of parameters such as period, delay, duration, and transition time. Both high and low levels of the output waveform are independently variable. A 3-state trigger light indicates proper external triggering. Selectable 50- Ω or 1-M Ω trigger/gate input permits use of a 1X or 10X oscilloscope probe. The -T version is a standalone instrument complete with mainframe/power supply, for operation from 100 to 240 Vac, 48 to 440 Hz; the other is a plug-in instrument for operation in a multicompartiment mainframe/power module of the TM 500 series. Both provide preset and external tracking of both output voltage levels. **Tektronix, Inc**, PO Box 500, Beaverton, OR 97077.

Circle 262 on Inquiry Card

SINGLE-BOARD DISPLAY MEMORY SYSTEM



The in-477 CRT display memory, built with 4096-bit RAM circuits, rather than 1024-bit shift registers, is almost four times as compact as conventional display memories and can operate at high speed in a variety of modes. Memory locations can be accessed both randomly and sequentially at data rates up to almost 20 megabits/s, allowing the device to be used in special image processing applications and to refresh displays of virtually any size and image format. Std board access time is 600 ns and cycle time is 850 ns, providing data transfer rates to 1.2 megabits/s in single-bit serial mode and to 20 megabits/s in other modes. All inputs/outputs are at TTL levels. Each board stores 256 kilobits of data in 64 n-channel, silicon gate MOS 4K RAMs. Boards may be used in parallel to create displays requiring greater storage capacities. **Intel Memory Systems**, a div of **Intel Corp**, 1302 N Mathilda Ave, Sunnyvale, CA 94086.

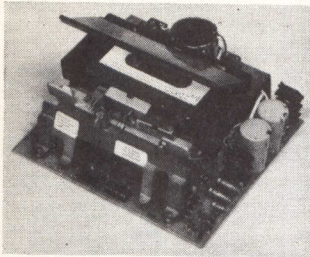
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HIGH SPEED MODEM SERIES

With the inherent reliability and low power consumption of MOS/LSI circuitry, each LST modem is packaged in a 5 1/4 x 8 1/2 x 18" unit that weighs less than 15 lb, and uses <15-W power. 9600, 7200, and 4800 operate at 9600, 7200, and 4800 bits/s, respectively, for full-duplex operation over std 3002, M102, or equivalent voice-grade lines in point-to-point applications. LSI 96FP, 72FP, and 48FP "Fast-Poll" multipoint units provide 9600, 7200, and 4800 bits/s, respectively, on the outbound master side in polled networks. An inbound automatic "gearshift" mechanism permits inbound poll responses to begin at 2400 bits/s and automatically shifts both master and slave modems up to 4800 bits/s if the length of the message makes that speed appropriate. **Codex Corp**, 15 Riverdale Ave, Newton, MA 02195. Circle 264 on Inquiry Card

VARIABLE-SPEED TAPE TRANSPORT FOR MICROPROCESSORS

A low cost, variable-speed cassette tape transport, the Phi-Deck features 4-motor control, remote control capabilities, fast start/stop, <30-s rewind, ac or battery-operation, and variable speed from 0.4 to 10 in./s. Power requirements are 7 Vdc at 600 mA



avg. Four separate motors control take-up, rewind, play or record, and head engagement. Separate motors allow the most complex tape deck function to be accomplished by remote control. Flutter, wow, and jitter are minimal because the capstan drive motor moves only the capstan. Control boards for the TTL-, DTL-, CMOS-compatible

device contain all circuitry for proper control of the tape transport. Options such as EOT/BOT sensing, record/play, read/write, electronics, and cassette-in-place sensing are available. **Triple I, a div of The Economy Co**, 1901 N Walnut, PO Box 25308, Oklahoma City, OK 73125.

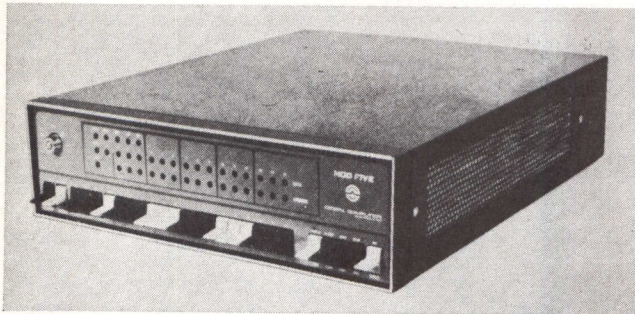
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6-DIGIT FLOATING-DECIMAL CALCULATOR IC

Developed using a metal gate, p-channel MOS process with low end-product cost as the primary objective, the MM5777 allows a complete 4-function, 6-digit calculator to be built using only a keyboard, an NSA1161 LED display stick, a DS8977 digit driver, and a 9-V battery. Leading- and trailing-zero suppression allows easy reading of the right-justified display and conserves battery power. Battery life is from 10 to 20 hr, depending on battery type. Other features include algebraic key entry notation, floating point I/O, and chain operations. Keyboard decoding and key debounce circuitry, clock and timing generation, and output 7-segment display decoding are all included on the chip and require no external discrete components, LED segments can be drive directly as the device typ sources 8-mA peak current. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

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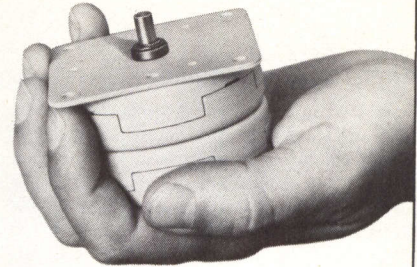
MICROPROGRAMMED MINICOMPUTER



A microprogrammed, fully parallel computer, the MOD FIVE is upward compatible with Data General's Nova 1200, and with the company's D-116, 216, 316, 416, and 616 minicomputers. Features include an enriched single-word instruction set, which provides arithmetic memory to accumulator, arithmetic memory to memory, bit manipulation, multiple logical/arithmetic shifts, extended logical, move memory to memory, and byte manipulation instructions; overlapped instruction-fetch concurrent with instruction execution; and triple-stack processing, coupled with a vectored interrupt system. Interrupt response time is claimed to be 7 to 10 times faster than either a D-116 or Nova 1200. The computer is available in four different configurations with from 4- to 7-slot chassis. **Digital Computer Controls Inc**, 12 Industrial Rd, Fairfield, NJ 07006.

Circle 267 on Inquiry Card

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The 82900 has a lot to offer, particularly in impact and non-impact printers, small X-Y plotters and computer peripherals. It's powerful, compact and moderately priced. And it's reliable. So reliable — in fact — that it can also be used to control pumps and valves in medical instruments and similar devices. In many applications it can replace larger, bulkier steppers at much lower cost.

Standard construction provides 2-phase operation (requiring simplified, low-cost circuitry), a 7.5° step angle and roller bearings. However, 4-phase operation, a 15° step angle or sleeve bearings can be furnished as options.

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CIRCLE 73 ON INQUIRY CARD

THE EUROPEAN MINICOMPUTER PERIPHERALS AND SOFTWARE MARKET

The value of minicomputer peripheral and terminal equipment shipped in Europe in 1974 was \$69 million. Shipments will increase more quickly than for the minicomputer processors, rising to \$621 million by 1984 — almost nine times the current level. The cumulative market for the 1975-1984 period will total more than \$3.2 billion, and an additional \$2.7 billion of main memory modules will be delivered.

Frost & Sullivan has completed a two-volume, 472-page report forecasting the market through 1984, by product (25 products), for: hard copy peripheral units; storage peripheral devices; add-on-memory modules; terminal and data entry equipment and other types of peripheral equipment; and for third-party equipment maintenance services, systems and control software, applications software and turn-key systems. Forecasts are made for Belgium, Denmark, France, Germany, Italy, the Netherlands, Norway, Sweden, Switzerland, the United Kingdom and others.

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LITERATURE

TTL/DTL Logic Modules

Complete line of pre-engineered, g-p logical building blocks is presented in selector guide which also discusses engineering services for special-purpose modules. **Wyle Computer Products**, Hampton, Va. Circle 300 on Inquiry Card

D-A Converter Applications

Application note describes DAC-08, featuring dual complementary, true current outputs; universal logic inputs interfaceable with any logic family; 85-ns settling time; high speed multiplying; and the ability to use any std system power supply voltages. **Precision Monolithics Inc**, Santa Clara, Calif. Circle 301 on Inquiry Card

IC, Circuit Module, System Selection

116-page catalog covers data acquisition and microcomputer input/output systems, data conversion products, op amps, instrumentation amps, isolation and data amps, analog circuit functions, active filters, and power supplies. **Burr-Brown**, Tucson, Ariz. Circle 302 on Inquiry Card

Integrated Circuit Sample/Hold

Brochure gives complete technical data on SHM-IC-1, with a general description, block diagram, mechanical specs, application notes, operating-mode diagrams, and performance-parameter graphs. **Datel Systems, Inc**, Canton, Mass. Circle 303 on Inquiry Card

Intelligent Terminals

Comparison chart describes user-programmable CRT display terminals which feature three microprocessors; high speed architecture; and functional, modular structure; and may be used in a stand-alone or online environment. **Ontel Corp**, Plainview, NY. Circle 304 on Inquiry Card

Minicomputer Access System

Brochure/booklet describe HP 2000, which combines system processor, communications processor, disc drive, mag-tape drive, and paper-tape reader to give interactive access to up to 32 terminal users while functioning as a multi-source RJE station to an IBM or CDC mainframe computer. **Hewlett-Packard Co**, Palo Alto, Calif. Circle 305 on Inquiry Card

Automatic Warehouse Control Systems

Bulletin describing systems based on the concepts of functional modularity and distributed control details modules employing microprocessor/minicomputer technology. **Ann Arbor Computer Corp**, Ann Arbor, Mich. Circle 306 on Inquiry Card

Switches, Indicator Lights

Photos, dimensional diagrams, and specs for pushbutton, basic snap-action, toggle and limit, and PC-board switches are covered in catalog. **Control Switch, a Cutler-Hammer Co**, Folcroft, Pa. Circle 307 on Inquiry Card

Lighted Devices

Included in catalog are 37 categories of LED, neon, and incandescent indicators comprising 15,000 products, plus 500 separate replacement components and lens caps. **Chicago Miniature/Drake, sub of General Instrument Corp**, Chicago, Ill. Circle 308 on Inquiry Card

Switching Regulated Power Supplies

SS series is described in brochure which includes an output rating chart along with prices, specs, and functional block and wiring diagrams. **Powertec, Inc**, Chatsworth, Calif. Circle 309 on Inquiry Card

DC Stepping, AC Synchronous Motors

Design engineer's guide covers terminology, construction/operation, ratings/specs, selection, and applications. **The Superior Electric Co**, Bristol, Conn. Circle 310 on Inquiry Card

Vaneaxial Airmovers

Catalog offers data on 1 to 15" dia fan designs with tech notes detailing performance parameters, dimensions, and other specs. **IMC Magnetics Corp**, Westbury, NY. Circle 311 on Inquiry Card

Digital Tape/Ticket Printer

Detailed in brochure are digital tape printers, modular ticket printers, printer mechanisms, single-decade print modules, and printwheel libraries. **Hecon Corp**, Tinton Falls, NJ. Circle 312 on Inquiry Card

2400-Bit/s Modems

Booklet comparing the company's modem 24 LSI with AT&T's Dataphone 2400 data-set includes pricing policies, line turn-around time, and features, such as reverse and secondary channels and diagnostics. **International Communications Corp**, Miami, Fla. Circle 313 on Inquiry Card

Complementary Metal-Oxide Semiconductor Logic

Booklet contains all technical data for using the company's Cambion CMOS logic cards in the design of digital systems. **Cambridge Thermionic Corp**, Cambridge, Mass. Circle 314 on Inquiry Card

Circular Hermetic Connectors

Illustrated catalog describes GS series of std connectors, designed for applications where partial vacuum, inert gas, or constant or controlled pressure are required to eliminate adverse effects created by atmospheric changes. **ITT Cannon Electric**, Santa Ana, Calif. Circle 315 on Inquiry Card

Linear Interface Circuits

Updated brochure describes over 130 circuits that bridge the gap between otherwise incompatible devices and device families to facilitate development of high-performance electronics systems. **Motorola Semiconductor Products Inc**, Phoenix, Ariz. Circle 316 on Inquiry Card

Data Conversion Products

Catalog contains electrical/mechanical specs for DACs, multiplying DACs, ADCs, S/H amps, precision resistor networks, and a 16-channel data acquisition system. **Micro Networks Corp**, Worcester, Mass. Circle 317 on Inquiry Card

Uninterruptible Power System Batteries

Guide presents tradeoffs in determining battery time and type as well as formulas needed to size the batteries for inverter configurations. **Elgar Corp**, San Diego, Calif. Circle 318 on Inquiry Card

Consoles, Desks

Developed specifically for electronics, aluminum and steel units detailed in brochure provide for mounting instruments above and below work surfaces; hidden cable routing, storage, and 19" panel-mounting are also featured. **Optima Enclosures, Div Scientific-Atlanta, Inc**, Tucker, Ga. Circle 319 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—not the reader service number. Please do **not** circle the page number on the reader service card.

MATERIALS	PAGE	PAGE	PAGE
SHIELDING			
Shielding Materials			
Metex	170		
HARDWARE			
CONNECTORS AND INTERCONNECTION SYSTEMS			
PC Connector			
Amerace/Control Products	88		
Flat Cable/Connector System			
3M	55		
INDICATORS; READOUTS; DIGITAL DISPLAYS; LAMPS			
Indicators			
Mineico/General Time	171		
LED Indicator			
Switchcraft	158		
Dimmer Indicator Lights			
Dialight/North American Phillips	164		
Audio Indicators			
Projects Unlimited	5		
Incandescent Displays			
REFAC Electronic	158		
PACKAGING SYSTEMS			
Packaging Systems			
Cambridge Thermionic	165		
PANELS AND BACKPLANES			
Wire-Wrapped Panels			
Electronic Molding	67		
Wire-Wrapping Equipment			
OK Machine & Tool	152		
PARTS			
Wire Clamps			
dek	165		
SOCKET BOARDS AND CARDS			
Socket Boards and Cards			
EECO	Cover II		
COMPONENTS AND ASSEMBLIES			
MAGNETIC COMPONENTS			
Magnetic Sensor			
Electro	163		
MOTORS; ROTATIVE COMPONENTS			
Stepper Motors			
North American Phillips Controls	167		
Superior Electric	162		
Servomotor			
Portescap U.S.	133		
DC Gearmotor			
Pittman	158		
Linear Motor Head-Positioning System			
Information Magnetics	164		
PHOTODEVICES			
CCD Area Image Sensor			
Fairchild Camera & Instrument/CCD	158		
Color LEDs			
Chicago Miniature Lamp	152		
POWER SOURCES, REGULATORS, AND PROTECTORS			
Power Supplies			
Computer Products	158		
Pioneer Magnetics	139		
Switching Power Modules			
Estatech	151		
Switching Regulator Power Supplies			
Adtech Power	151		
Laboratory Power Supplies			
Instant Instruments	162		
Modular Uninterruptible Power Systems			
Deltac	152		
Uninterruptible Standby Power Systems			
Sola Electric/Sola Basic Industries	166		
Power Line Monitor			
Holland Electronics	161		
Power Supply Test Set			
H & H Automation	159		
SWITCHES			
Miniature Panel Switches			
Airpax Electronics/Cambridge	14		
Pushbutton Switches			
Centralab/Electronics/ Globe-Union	159, 160, 161		
Lighted Pushbutton Switch			
Unimax Switch	152		
12-Pole, Double-Throw Pushbutton Switches			
Seacor	160		
Mercury-Wetted Reed Switch			
Hamlin	161		
CIRCUITS			
CIRCUIT CARDS AND MODULES			
Core Memory Modules			
Ampex/Memory Products	60		
Plessey Memories	86		
Standard Memories	150		
Single-Board Display Memory System			
Intel Memory Systems/Intel	166		
Data Acquisition Module			
Analogic	11		
A-D Converter Modules			
Analogic	142		
Tracking S-D Converter Modules			
ILC Data Device	164		
Differential Transmitter Modules			
Computer Conversions	160		
DIGITAL AND INTERFACE INTEGRATED CIRCUITS			
4K RAMs			
Mostek	140		
n-Channel MOS ROMs			
Advanced Micro Devices	159		
Microprocessors			
Intel	40, 132		
National Semiconductor	97		
Texas Instruments/Digital Systems	16		
Microprocessor Kit			
American Microsystems	44		
Floating-Decimal Calculator IC			
National Semiconductor	167		
Monolithic 8-Bit D-A Converters			
Datel Systems	154		
Synchro-to-Resolver Converter			
Magnetico	156		
HYBRID CIRCUITS			
Hybrid CMOS A-D Converter			
Micro Networks	163		
Multiplying D-A Converter			
Beckman Instruments/Helipot	152		
LINEAR INTEGRATED CIRCUITS			
CCD Area Image Sensor			
Fairchild Camera & Instrument/CCD	158		
MEMORY/STORAGE EQUIPMENT			
FLEXIBLE DISC UNITS			
Flexible Disc Drives			
Pertec/Peripheral Equipment	28		
Flexible Disc Systems			
Shugart Associates	39		
Sykes Datatronics	43		
Flexible Cartridge Disc System			
Process Dynamics	136		
MAGNETIC CORE MEMORIES			
Core Memory Systems			
Ampex/Memory Products	60		
Plessey Memories	86		
Standard Memories	150		
MAGNETIC DISC AND DRUM UNITS			
(See also Flexible Disc Units)			
Drum Memory System			
Vermont Research	153		
Disc Drives			
ISS/Sperry Univac	31		
Pertec/Peripheral Equipment	28		
Cartridge Disc Drives			
Diablo Systems	8		
Disc Systems			
Alpha Data	4		
Datum	165		
General Instrument/ Rotating Memory Products	51		
Disc Drive Controller			
Vermont Research	161		
MAGNETIC TAPE UNITS			
Tape Drives			
Pertec/Peripheral Equipment	28		
Tape Transports			
Kennedy	1		
Cassette Tape Transport			
Braemar Computer Devices	151		
Cassette Tape Transport for Microprocessors			
Triple I/Economy	167		
Cartridge Tape Drive			
Emerson Electric	98		
Cartridge Tape Systems			
3M/Mincom	142		
Three Phoenix	156		

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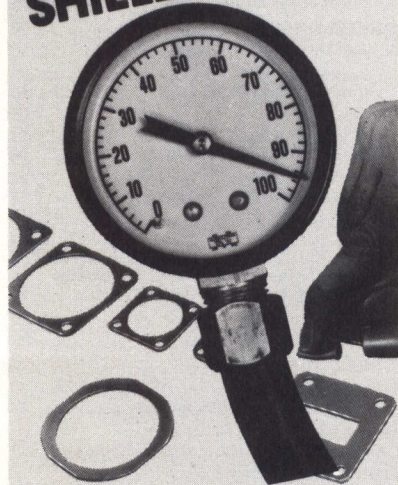
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GUIDE TO PRODUCT INFORMATION

	PAGE
Editing Recorder Anderson Jacobson	162
ROM PROGRAMMERS AND SIMULATORS	
p-ROM Simulator Electri-Com	166
SEMICONDUCTOR MEMORIES	
4K RAMs Mostek	140
n-Channel MOS ROMs Advanced Micro Devices	159
Semiconductor Memory Systems Intel Memory Systems/Intel	27
Single-Board Display Memory System Intel Memory Systems/Intel	166

INPUT/OUTPUT AND RELATED EQUIPMENT

AUDIO RESPONSE EQUIPMENT	
Voice Response System Federal Screw Works/ Vocal Interface/Votrax	154
DATA TERMINALS	
Data Terminal Teletype	165
Display Terminals Applied Automation	151
Lear Siegler	157
Intelligent Display Terminals Hazeltine	156
Hewlett-Packard	19
Color Intelligent Display Terminal Intelligent Systems	163
Bilingual Display Terminal Megadata Computer and Communications	159
Editing Capability for CRT Terminals Ann Arbor Terminals	164
Intelligent Data Entry Terminals Sycor	154
Intelligent Remote Batch Terminal System Singer/M&M Computer Industries	161
GRAPHIC EQUIPMENT	
Sonic Digitizer Science Accessories	116
INTERFACE EQUIPMENT; CONTROLLERS	
Disc Drive Controller Vermont Research	161
Matrix Printer Interface Control Data	154
Calculator Interface Option Vidar Autodata	152
KEYBOARD EQUIPMENT	
Keyboard Chomerics	166
Alphanumeric Keyboard Flex-Key	156
PAPER TAPE EQUIPMENT	
Punched Tape Equipment Jamesbury/Decitek	125
Ex-Cell-O/Remex	117
Paper Tape Reader Data Peripheral	161
Tape Punch Extel	165
NC Tape Preparation/Editing System International Computer Products	164
PLOTTING EQUIPMENT	
Digital Plotters Houston Instrument/Bausch & Lomb	131
PRINTER/PLOTTERS	
Electrostatic Printer/Plotter Versatec	123
PRINTING EQUIPMENT	
Serial Printer Diablo Systems	Cover IV
Line Printers Binary	156
Dataproducts	155

	PAGE
Digital Equipment/Components	15
Macro Products	151
Tally	2
Terminal Printer Informer	159
Digital Printers Addmaster	4
C. Itoh Electronics	124
C-Tek	164
Matrix Printer Interface Control Data	154
PUNCH CARD EQUIPMENT	
Card Reader/Printer ICOM	138

COMPUTERS AND COMPUTER SYSTEMS

AUTOMATIC TEST SYSTEMS	
Automatic Logic Board Tester Fluke Trender	Cover III
Automatic Backplane Test System Teradyne	13
COMPUTER AUXILIARY UNITS	
Floating-Point Processor Digital Equipment	159
MICROCOMPUTERS AND MICROPROCESSORS	
Microcomputers	
Applied Data Communications	154
Computer Automation	48
Control Logic	134, 145-148
General Automation	20
MITs/Altair	135
Texas Instruments/Digital Systems	16
Zilog	132
Microcomputer Develop/Debug System Ramtek Micro Machines	129
Microcomputer Development System E & L Instruments	158
Microcomputer/Assembler/Simulator Automated Computer Systems	135
Microprocessors	
Intel	40, 132
National Semiconductor	97
Microprocessor Kit American Microsystems	44
Microprocessor Development System muPro Associates	135
Microprocessor Program Development Systems Technical Communications	137
MINICOMPUTERS; SMALL- AND MEDIUM-SCALE COMPUTERS	
Computers and Peripherals	
Microdata	121
Minicomputers	
Data General	115
Digital Computer Controls	167
Digital Equipment	126
Hewlett-Packard	119
Honeywell	33-36
Interdata	23-25, 57
Systems Engineering Laboratories	58
Texas Instruments/Digital Systems	16
Medium-Scale Computer Systems Modular Computer Systems	109-112
PROGRAMMABLE CALCULATORS	
Floating-Decimal Calculator IC National Semiconductor	167
Calculator Interface Option Vidar Autodata	152
DATA COMMUNICATIONS EQUIPMENT	
DATA TRANSMISSION EQUIPMENT	
Fiber Optics Digital Data Link Harris Communications and Information Handling	159
MODEMS; DATA SETS	
Data Modems	
Codex	166
Perini/Data Communications	160

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PAGE

DATA ACQUISITION AND CONTROL EQUIPMENT

A-D AND D-A CONVERTERS	
A-D Converter Modules	
Analogic	142
Hybrids CMOS A-D Converter	
Micro Networks	163
Monolithic 8-Bit D-A Converters	
Data Systems	154
Multiplying D-A Converter	
Beckman Instruments/Hellpot	152

DATA ACQUISITION SYSTEMS

Data Acquisition System	
Analogic	11
Analog Signal Processors	
Neff Instrument	47

DATA TRANSFER AND INTERFACE EQUIPMENT

Process-Computer I/O Interface	
Computer Products	7

MONITORING AND CONTROL EQUIPMENT

Digital Position Controller	
Unico	154
Master Isolated Reference Drive Control	
Reliance Electric	151

SYNCHRO-DIGITAL AND DIGITAL-SYNCHRO CONVERTERS

Tracking S-D Converter	
ILC Data Device	164
Synchro-to-Resolver Converter	
Magnetico	156
Differential Transmitter Modules	
Computer Conversions	160

TEST AND MEASUREMENT EQUIPMENT; INSTRUMENTATION

DATA GENERATORS

Pulse Generator	
Tektronix	166

DIGITAL EQUIPMENT TESTERS

Logic State Analyzers	
Hewlett-Packard	68-76
Automatic Logic Board Tester	
Fluke Trendar	Cover III
Automatic Backplane Test System	
Teradyne	13
Digital Logic Recorder	
Cove Electronics	162

INSTRUMENT AMPLIFIERS

Programmable Ranging Amplifier	
Electronic Development	161

METERS

Digital Multimeter	
Hewlett-Packard	142

OSCILLOSCOPES

Oscilloscopes	
Phillips Test & Measuring Instruments/ North American Phillips	163

OTHER PRODUCTS; SERVICES

EMPLOYMENT OPPORTUNITIES

Employment Opportunities	
NCR/Data Processing	124
NCR/Terminal Systems	164
Taylor Instrument/Process Control	163

EXHIBITIONS

Computer Conferences/Exhibitions	
CompDesign/76	61-66, 106
AFIPS/National Computer Conference	144
WESCON/76	149

SOFTWARE

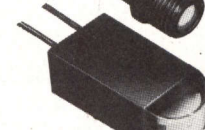
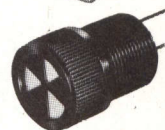
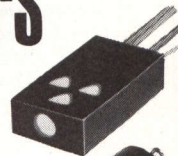
Microprocessor Software	
Micro Tec	130
Motorola Semiconductor Products	136
Programming Language	
Intermetrics	137
Macro Cross-Assembler	
Zeno Systems	137
Microcomputer Program/Time-Sharing Service	
NEC Microcomputers	136

OTHER NON-DIGITAL PRODUCTS

Environmental Control Systems	
Hydro-Temp Controls	160

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171

ADVERTISERS' INDEX

Addmaster Corp.	4
AFIPS/National Computer Conference	144
Airpax Electronics, Cambridge Div.	14
Alpha Data, Inc.	4
Amerace Corp., Control Products Div.	88
American Microsystems, Inc.	44, 45
Ampex Corp., Memory Products Div.	60
Analogic Corp.	11
Applied Data Communications	154
Braemar Computer Devices, Inc.	151
Cambridge Thermionic Corp.	165
Centralab Electronics, Div. Globe-Union, Inc.	159, 161
CompDesign/76	61-66, 106, 107
Computer Automation, Inc.	48, 49
Computer Design Publishing Corp.	i, ii*
Computer Products, Inc.	7
Control Logic, Inc.	145-148
Data General Corp.	115
Datum, Inc.	162
Dataproducts Corp.	155
dek, inc.	165
Diablo Systems, Inc.	8, 9, Cover IV
Digital Equipment Corp.	15, 126, 127
EECO	Cover II
E & L Instruments, Inc.	158
Electro Corp.	163
Electronic Molding Corp.	67
Emerson Electric Co., Industrial Controls Div.	98
Ex-Cell-O Corp., Remex	117
Fluke Trendar, Sub. of John Fluke Mfg., Inc.	Cover III
Frost & Sullivan, Inc.	167
General Automation	20, 21
General Instrument Corp.	51
Hewlett-Packard Corp.	16, 68-76, 119
Honeywell Information Systems	33-36
Houston Instrument, Div. of Bausch & Lomb, Inc.	131
Hydro-Temp Controls, Inc.	160
Integrated Computer Systems, Inc.	164 a-f
Intel Corp.	40, 41
Intel Memory Systems	27
Interdata	23-25, 57
C. Itoh Electronics, Inc.	124
Jamesbury Corp., Decitek Div.	125
Kennedy Co.	1
Lear Siegler	157
3M Co.	55
Metex Corp.	170
Microdata Corp.	121
Microtec	130
Minelco Div., General Time	109-112
Modular Computer Systems, Inc.	109-112
Mostek	140, 141
National Semiconductor Corp.	97
NCR, Terminal Systems Div.	164
Data Processing Div.	124
Neff Instruments	47
North American Philips Controls Corp.	167
OK Machine & Tool Corp.	152
Pertec, Peripheral Equipment Div.	28, 29
Pioneer Magnetics	139
Plessey Microsystems	86, 87
Portescap U. S.	133
Projects Unlimited, Inc.	5
Ramtek Corp.	129
Science Accessories Corp.	116
Shugart Associates	39
Sperry Univac, ISS Div.	31
Standard Memories, Inc.	150
Sykes Datatronics, Inc.	43
Systems Engineering Laboratories	58, 59
Tally Corp.	2
Taylor Instruments	163
Tektronix, Inc.	143
Teradyne, Inc.	13
TEXAS INSTRUMENTS INCORPORATED, Digital Systems Div.	16, 17
Three Phoenix Co.	156
Vermont Research Corp.	153
Versatec, Inc.	123
Wescon/76	149

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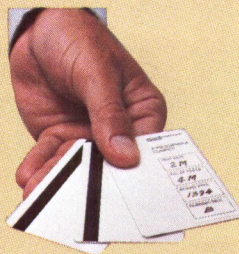
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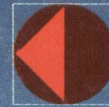
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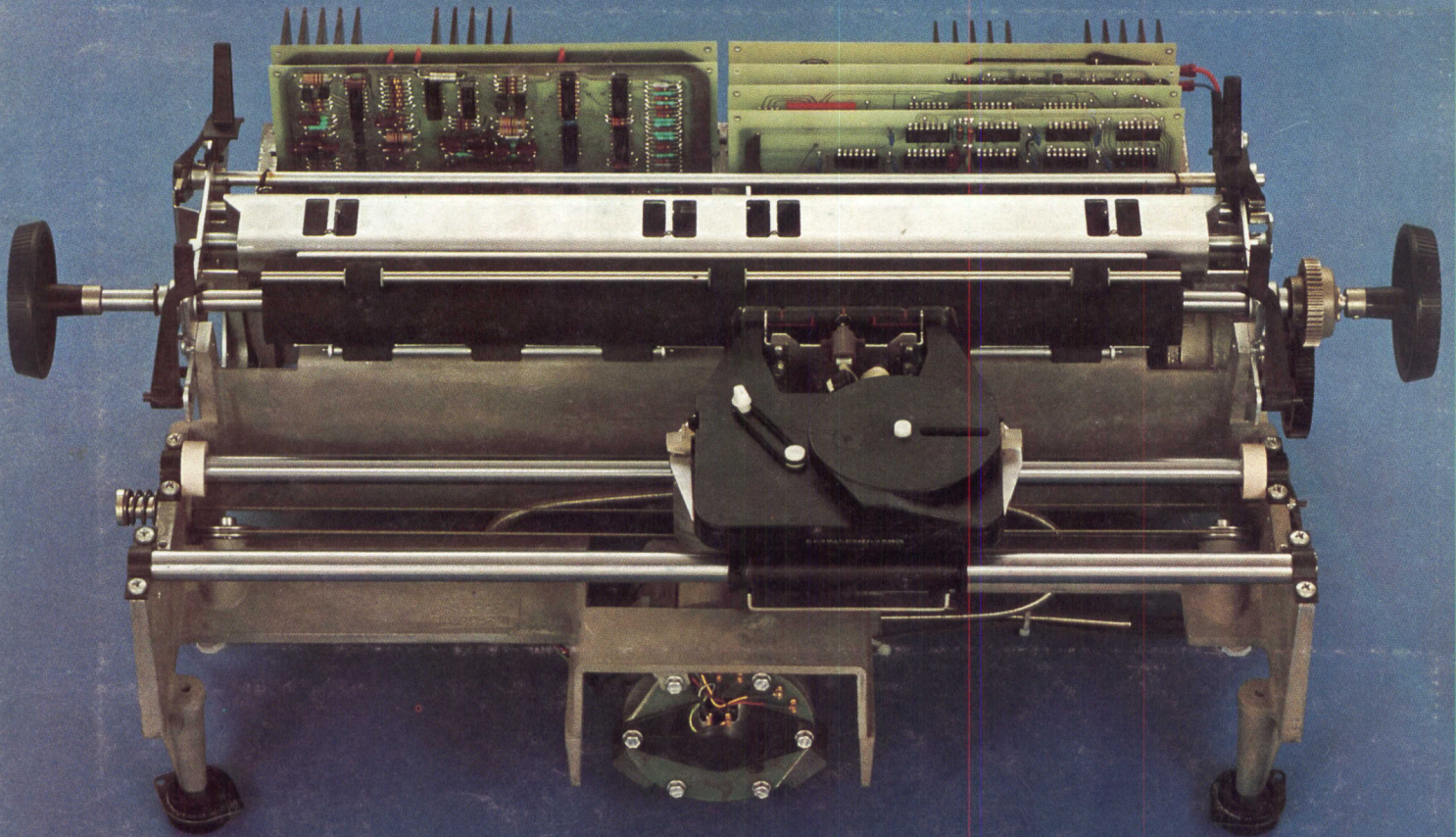
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