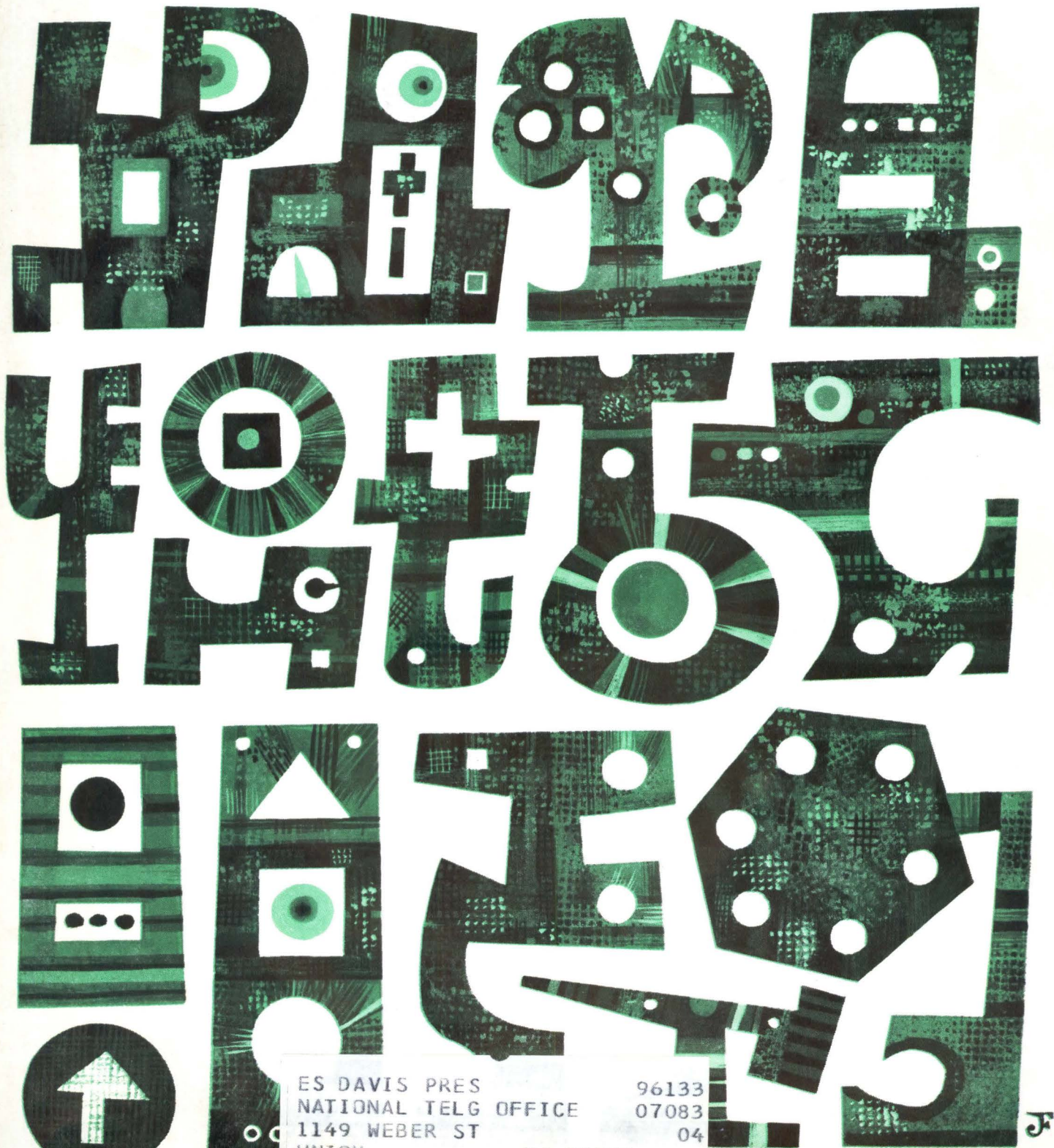


COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

DECEMBER 1967

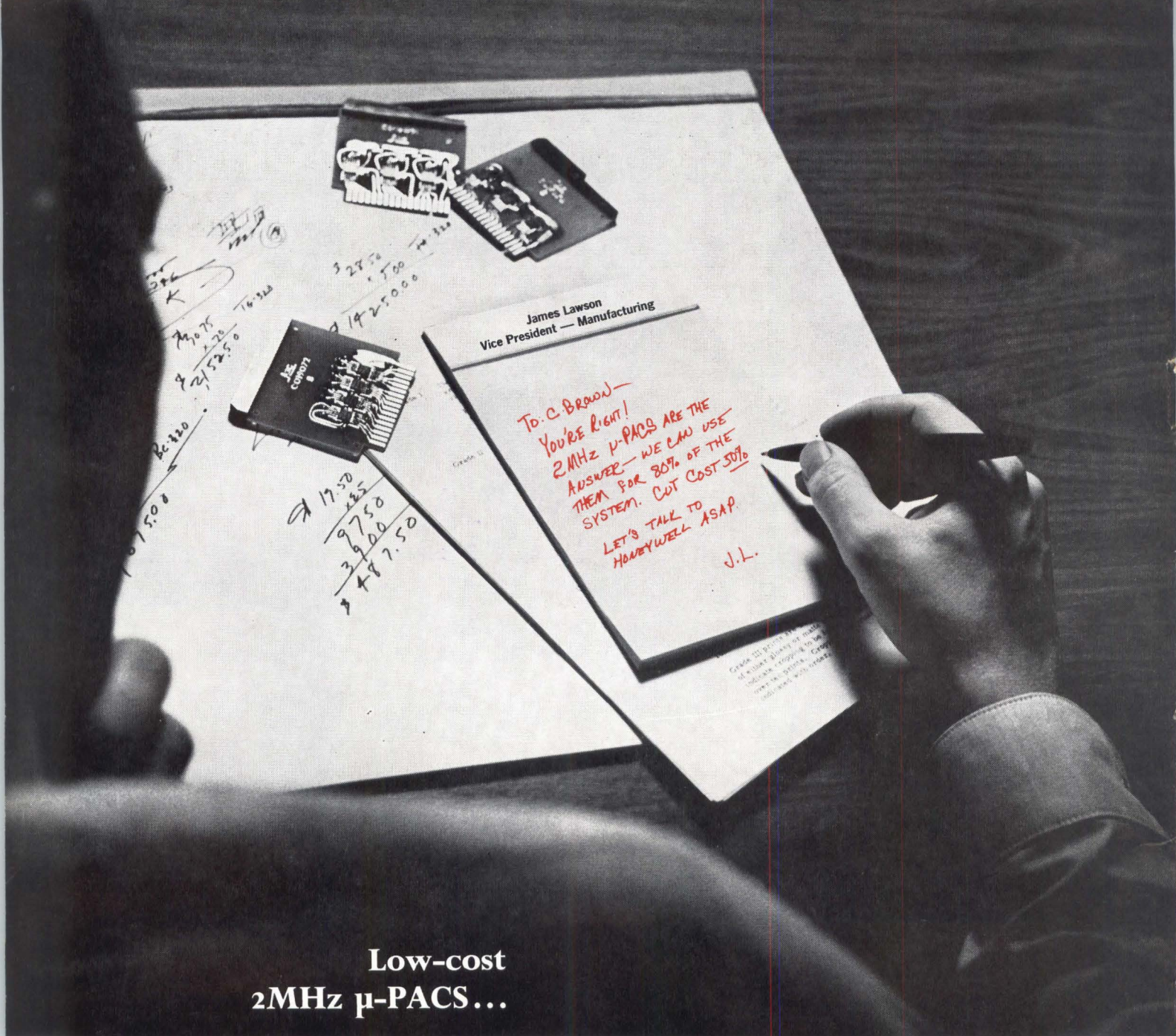


ES DAVIS PRES
NATIONAL TELG OFFICE
1149 WEBER ST
UNION

96133
07083
04

NJ 07083

J



**Low-cost
2MHz μ -PACS...**

**...let you save
up to half the cost
of system logic.**

If you face a make-or-buy evaluation for system logic, maybe you've considered μ -PACS. Now, you can use new I/C 2MHz μ -PACS for up to 80% of your logic needs. Cut costs as much as 50%.

Take another look at your make-or-buy: Think μ -PACS at half the cost. Add more savings for volume discounts. Forget the people and equipment you'd need just to begin making your own. Remember μ -PAC quality and reliability. (Both 2MHz and 5MHz μ -PACS are compatible.) If this changes your cost analysis, write for new spec/price brochure. Honeywell, Computer Control Division, Old Connecticut Path, Framingham, Massachusetts 01701.

Honeywell

CC COMPUTER CONTROL
DIVISION

CIRCLE NO. 1 ON INQUIRY CARD

For Airborne Military and Space Memory Systems

RCA's high-density memory stacks are tested and proved to military specifications

These military-type high-density stacks are available in various capacities up to 4k x 32...operating temperature range from -55°C to +125°C. And we can provide fast delivery of most configurations...just let us know your requirements!

Other sizes available where requirements warrant it.

RCA "building-block" construction provides wide flexibility of electrical capacities, ruggedized construction, improved reliability and faster delivery.

Greater reliability is assured because core mats are continuously wound—solder joints are kept to a bare minimum. Fewer frames result in smaller size, lighter weight, tighter, more compact package. The RCA 30/18 lithium ferrite cores provide wide-temperature operation. The complete package withstands vibrations up to 15G's.

Backed by more than two years of manufacturing experience and strict quality control, these RCA High-Density stacks are proved to MIL specs before you

order them. In many cases we can make initial deliveries in eight to ten weeks.

May we have one of our salesmen arrange for a demonstration for your specific military applications? Contact your RCA Field Representatives for details and availability for your requirements. Or call Marketing Dept. (617-444-7200), RCA Memory Products Division, Needham Heights, Mass. 02194. For Technical Bulletin MP317, write RCA Commercial Engineering, Section FZB-12, Harrison, N.J. 07029.

Designed to meet requirements of MIL Specifications MIL-E-5400, MIL-T-5422

30/18 High-Density Stack	
Capacity: 4096 words 26 bits	Shock: 50g
Temp. Range: -55°C to +125°C	Altitude: 0 to 70,000 ft.
Vibration: 10-500 cps 15g	Humidity: 10 days

4k x 16

4k x 15

4k x 14

4k x 17

4k x 18

4k x 19

4k x 20

4k x 23

4k x 24

4k x 25

4k x 10

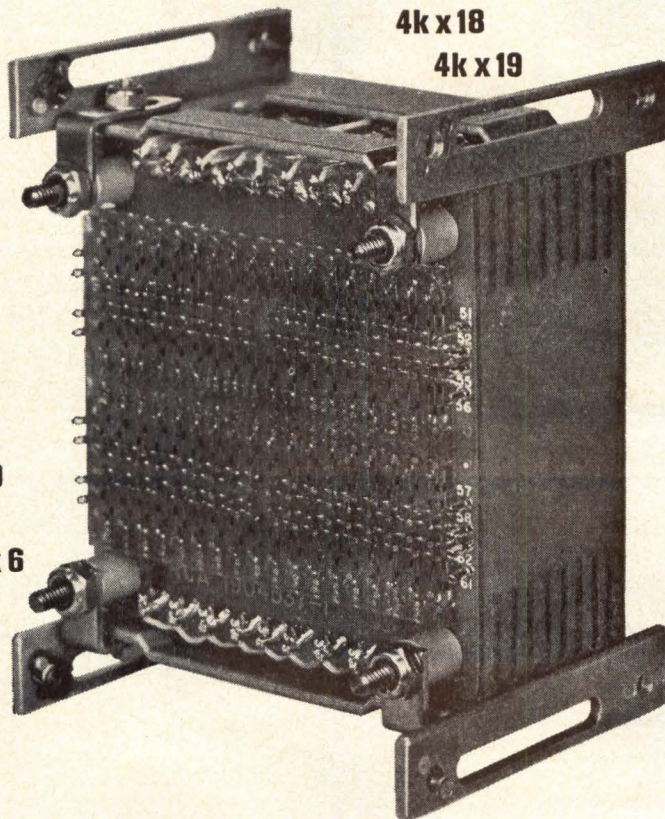
4k x 9

4k x 8

4k x 6

4k x 26

4k x 32



RCA Electronics Components and Devices

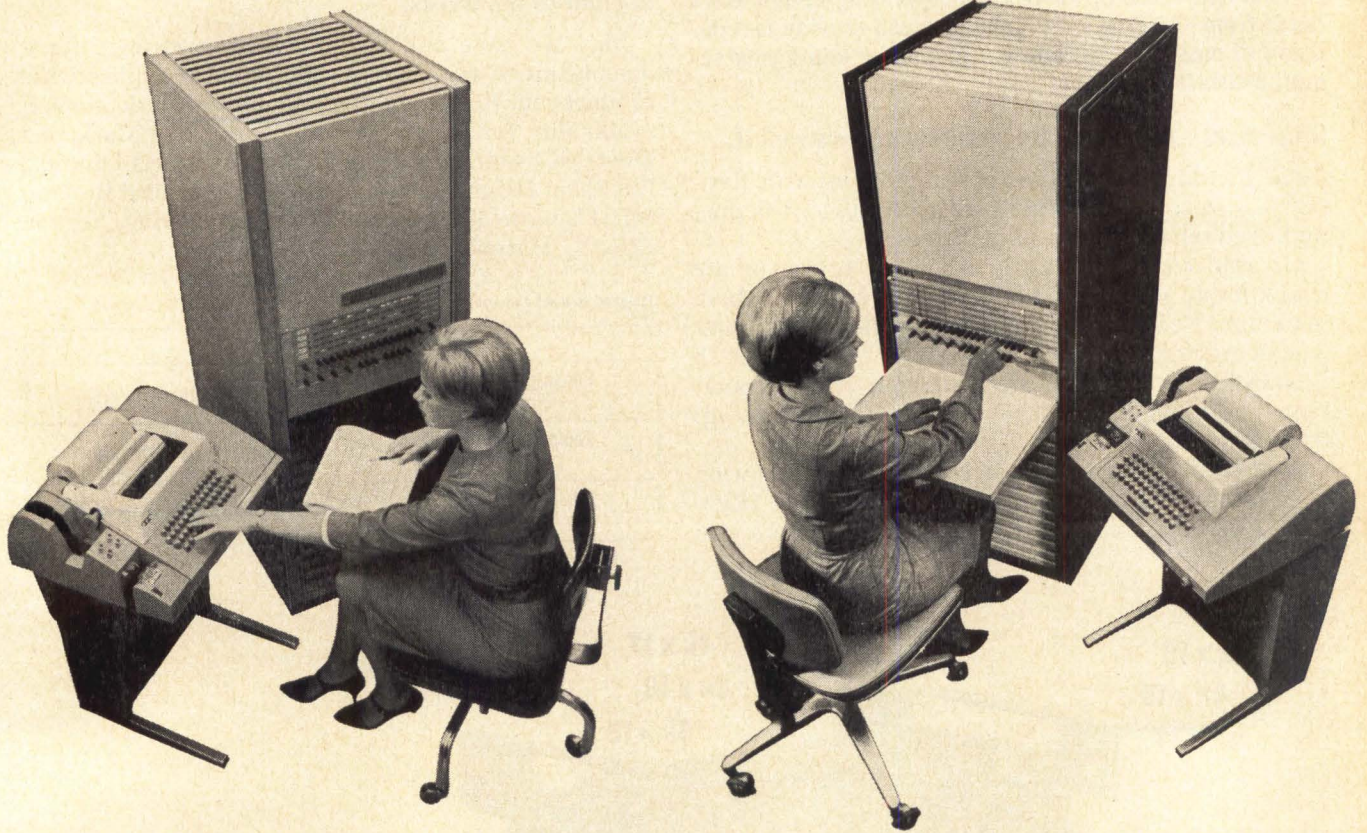


THE MOST TRUSTED NAME IN ELECTRONICS

CIRCLE NO. 2 ON INQUIRY CARD

Anything
the SEL 810A
can do,

the new
SEL 810B can do
twice as fast.



Over 50 SEL 810A, 16-bit computers have been supplied for data acquisition and control. Now meet the SEL 810B, with twice the speed of the A. Yet only about 20% more in price. Same great features: all integrated circuits, 2 levels of priority interrupt, memory expandable to 32K, I/O typewriter, high-speed hardware multiply and divide, and real-time I/O structure. And the software package of the 810B has been proven in the A.

Fixed point execution times of the B are: add/subtract—1.58 microseconds; multiply—4.74 microseconds; divide—6.32 microseconds; cycle time—790 nanoseconds. If you don't need the speed of the SEL 810B, buy the A. For either, call or write: Systems Engineering Laboratories, 6901 West Sunrise Blvd., Fort Lauderdale, Fla. 33310. Area Code 305 587-2900.

Systems Engineering Laboratories

Publisher and Editor
ROBERT BROTHERSTON

Editorial Advisers
RICHARD AHRONS
ELI ANFENGER
JAMES R. BRIGHT
GERHARD L. HOLLANDER
BERNARD M. GORDON
WALDRON S. MacDONALD
ROBERT S. SENATOR
HAROLD H. SEWARD

Contributing Editors
T. PAUL BOTHWELL
A. S. BUCHMAN
M. P. de REGT
RUDOLPH J. KADLEC
ROBERT P. FORAN
RICHARD B. LAWRENCE
WALTER A. LEVY
H. S. MILLER
MADELINE SULLIVAN

Washington Editor
HAROLD V. SEMLING, JR.

Art Director
JAMES FLORA

Production Manager
TERRY ARMENTI

Tech. Illus.
JOHN BROTHERSTON

Editorial Ass't.
PRISCILLA HANLON

Adv. Prod.
JOAN WASLUK

Circ. Mgr.
ALMA BROTHERSTON

Vice Pres.-Sales
LINDSAY H. CALDWELL

Editorial & Executive Offices
Prof. Bldg., Baker Ave.,
W. Concord, Mass. 01781
Tel. 369-6660

COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

FEATURES

36 ARCHITECTURE FOR LARGE COMPUTER SYSTEMS. — A DEBATE

This article provides perspective for the following four companion articles that advocate four different architectures for economical large computer systems:

39 VALIDITY OF THE SINGLE PROCESSOR APPROACH TO ACHIEVING LARGE SCALE COMPUTING CAPABILITIES

41 THE BEST APPROACH TO A LARGE COMPUTING CAPABILITY

A multi-processor approach.

43 ASSOCIATIVE PARALLEL PROCESSING

47 UNCONVENTIONAL SYSTEMS. *An array approach.*

54 A 20-MILLION-BIT, HIGH-SPEED, CORE MEMORY

This article describes in detail a production model of an extended core storage with access time of 1.5 micro-second and cycle time of 2.7 micro-seconds, at a cost below three cents per bit.

62 SYSTEMS IMPLICATIONS OF MICROPROGRAMMING

A qualitative description of the unique functional characteristics of microprogramming control.

67 INPUT-OUTPUT REQUIREMENTS FOR PROCESS CONTROL COMPUTERS

A brief look at the state-of-the-art in interfacing process control computers.

70 NEGATIVE RADIX ARITHMETIC, PART 7. DIVISION CONCLUDED

In this final article on division, Mr. de Regt considers the remaining steps and conventions for manual division.

DEPARTMENTS

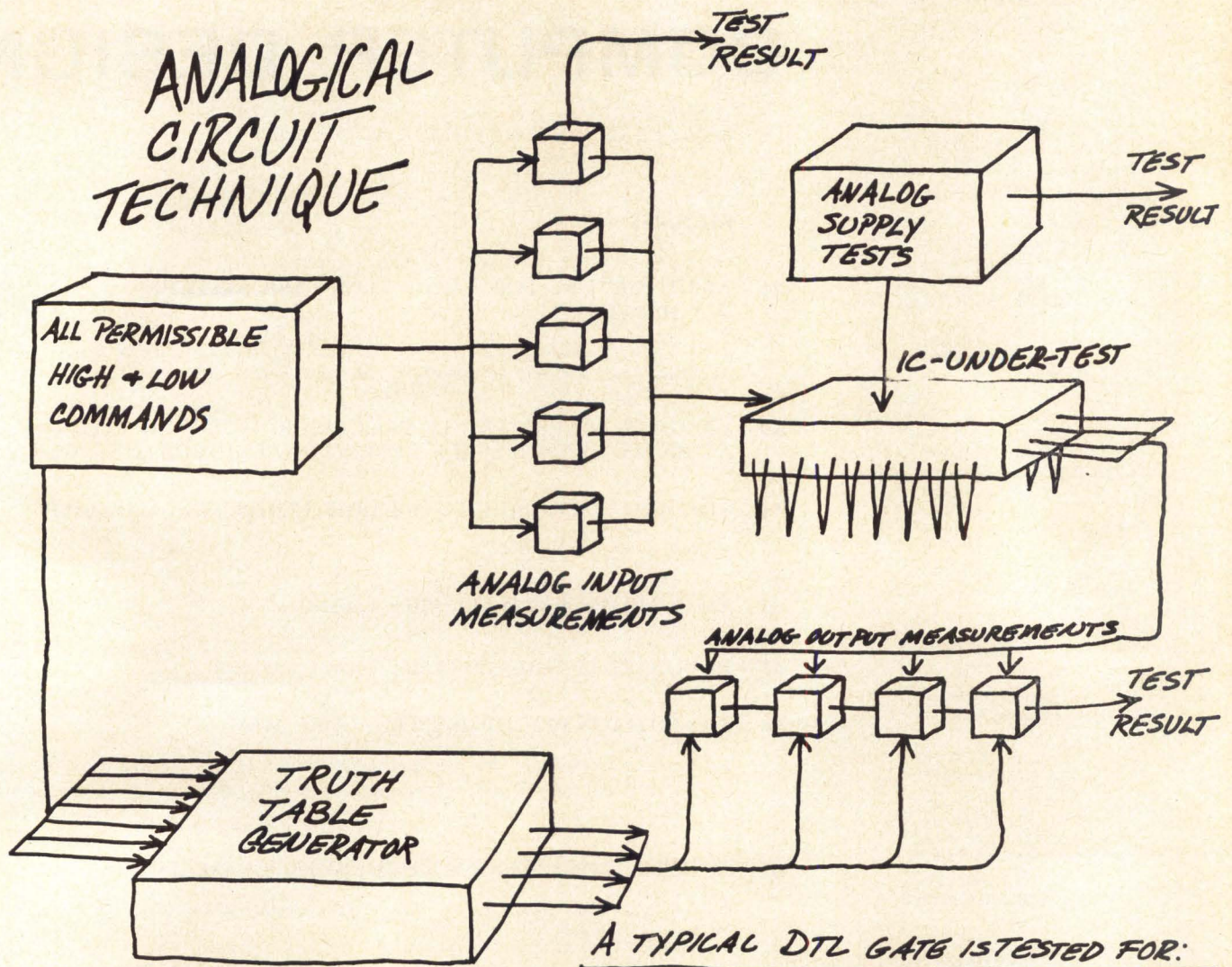
- 24 INDUSTRY NEWS
- 28 CD COMMENTARY
- 34 DC OUTPUT
- 78 NEW PRODUCTS
- 90 NEW LITERATURE
- 96 ADVERTISERS' INDEX

Reader subscription cards opposite Page 1
Reader inquiry cards opposite Page 96

Computer Design is published monthly. Copyright 1967 by Computer Design Publishing Corporation. Accepted as controlled circulation publication at Post Office at Boston, Massachusetts. No material may be reprinted without permission. Postmaster: CHANGE OF ADDRESS — FORM 3579 to be sent to Computer Design, Circulation Dept., P. O. Box A, Winchester, Mass. 01890. Subscription rate to nonqualified subscribers is \$15.00 per year; \$1.50 per issue. Subscription rate to all foreign subscribers is \$25.00 per year; \$2.50 per copy.



Circulation
over 32,000



A TYPICAL DTL GATE IS TESTED FOR:

$I_{IN HI}$	5.1 mA MAX @ 4.1 V
$I_{IN LO}$	1.1 mA MAX @ 1.1 V
$V_{OUT HI}$	2.6 V MIN @ 0.12 mA
$V_{OUT LO}$	0.45 V MAX @ 12.0 mA
I_{CC}	16 mA MAX @ 5.0 V

Intriguing, isn't it, this new way of testing digital integrated circuits?

Now you can make sure ALL of your ic's will work — because you can make both parameter and functional tests simultaneously, and for all permissible combinations of inputs. □ It's done by exercising all the LOGICAL inputs on the ic-under-test and selecting the appropriate ANALOG measurements that should be made. 5,000 such measurements are made in 1/100 of a second.



TERADYNE

CIRCLE NO. 4 ON INQUIRY CARD

□ Even more exciting, our Analogical Circuit Technique is available on a little machine that weighs only 25 lbs. It's a cinch to program, and costs only about \$5,000. □ We call it ACT 1 (because of the fortunate acronym). □ To learn more about analogical testing, just write: ACT 1, Teradyne, 183 Essex Street, Boston, Massachusetts 02111.

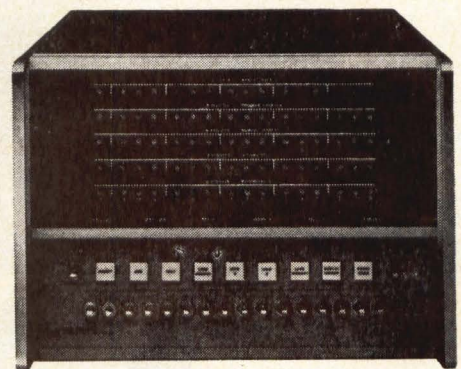
Se habla FORTRAN
Ici on parle ALGOL
Man spricht BASIC

Are we speaking your language?

Hewlett-Packard computers are multi-lingual. They speak languages like extended ASA Basic FORTRAN, ALGOL, and BASIC. You can perform scientific computations—or talk to instrumentation systems—in the language you're comfortable with.

Powerful software available for HP's computers includes FORTRAN, ALGOL and BASIC Compilers, Assembler, and Basic Control System (BCS) with modular I/O drivers for device-independent programming. Compilers and Assembler generate relocatable code—linked by BCS loader at execution time.

Two computers available—2116A and 2115A—fully software compatible. Start speaking to an HP computer now—with a call to your local HP field engineer or by writing Hewlett-Packard, Palo Alto, California 94304. Europe: 54 Route des Acacias, Geneva.



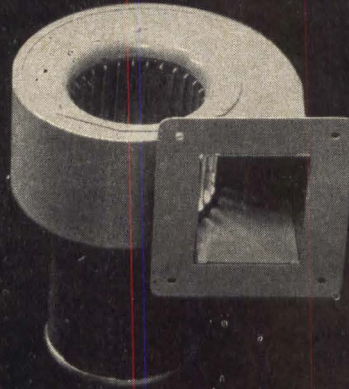
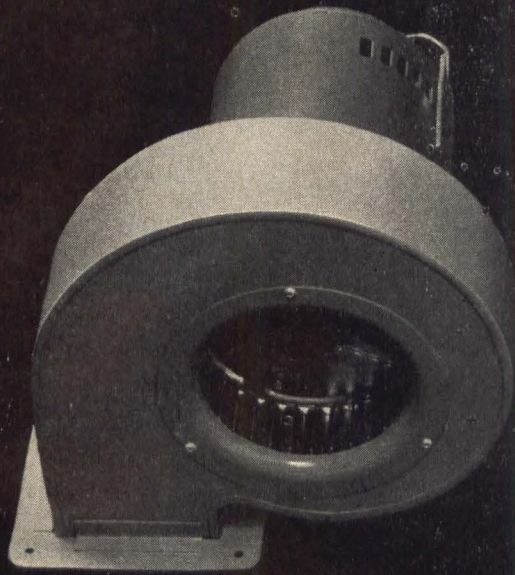
The 2115A has 16-bit words, 2 μ sec cycle time, 4K memory (expandable to 8K) and a \$16,500 price including Teleprinter.

HEWLETT  PACKARD

DIGITAL COMPUTERS

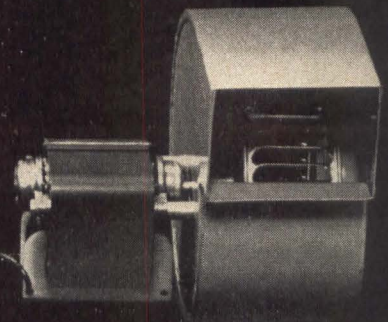
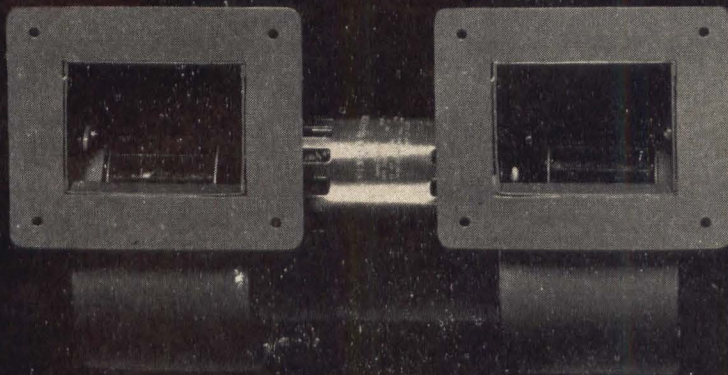
These 5 blowers

belong



to the

world's



biggest

fan club.

TORRINGTON

Despite any resemblance, no two centrifugal blowers shown above are alike. For that matter, neither are any of Torrington's 67 other in-stock blowers identical. Except for one outstanding fact.

All 72 of these blowers are immediately available "off-the-shelf" units . . . models designed to lend themselves to a variety of adaptations. By merely interchanging standard parts these in-stock units have produced 216 different models for Torrington customers, and the end is nowhere in sight.

Whatever your specifications, whether high or low air flow, A.C. or D.C. motors, high or low resistance, single or double inlet, Torrington can make the centrifugal blower you need — faster, more economically, and in any quantity you desire, from mere dozens to the thousands.

We can't illustrate every type of blower produced in our plant. But if you'd care to see how far we'll go to meet your needs, write today for our catalog "Centrifugal Blowers by Torrington." Address your request to Torrington Manufacturing Company, Torrington, Connecticut.

TORRINGTON MANUFACTURING COMPANY

United States: Torrington, Connecticut / Van Nuys, California / Rochester, Indiana Canada: Oakville, Ontario England: Swindon, Wilts. Belgium: Nivelles Australia: Sydney

**we've cut microseconds
we've cut size
we've cut cost**

in the new VersaSTORE II core memory system

VersaSTORE II is a vastly improved version of our field-proven VersaSTORE core memory. It operates at a faster 1.7 micro-second asynchronous speed with 750 nano-second access time—with the same superb operating margins at elevated temperature, and uses IC's for reliability.

The new VersaSTORE II packs 50% more core memory in a 5¼" rack-mounted package.

And VersaSTORE II is more flexible than ever. It's available in increments of 4096 words of 36 bits or 8k words of 18 bits, and conveniently stacks in multiples for bigger memories, thanks to our exclusive Party Line.

And VersaSTORE II offers self-test features, timing and control flags, and test points for easy system check-out.

Remember, you'll get all these features only in the new VersaSTORE II—nowhere else! Why not get a VersaSTORE II brochure? Write or call:



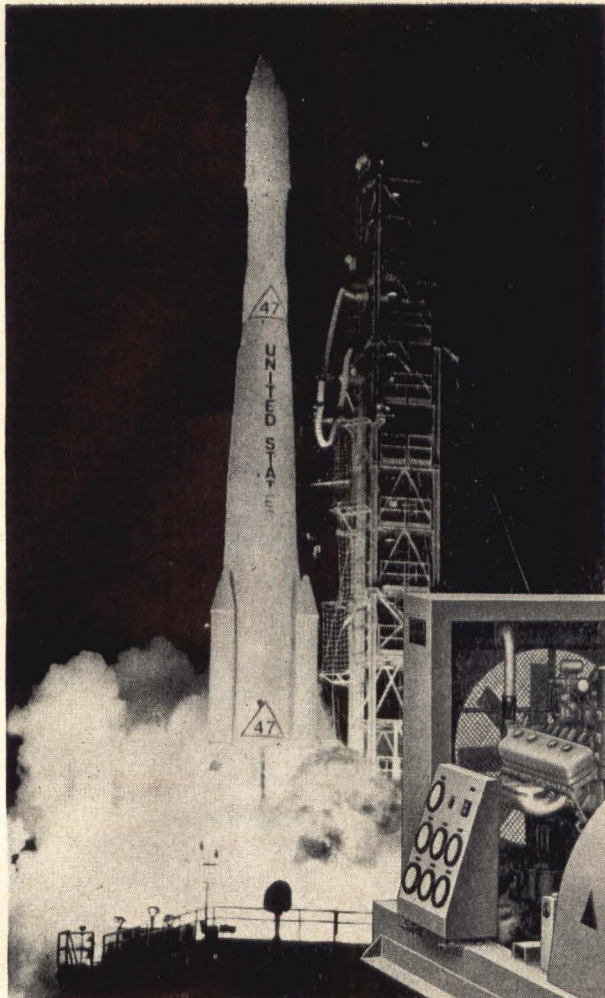
varian data machines
a varian subsidiary
Formerly Decision Control, Inc.



1590 Monrovia Ave., Newport Beach, Calif. TEL. (714) 646-9371 TWX (910) 596-1358

CIRCLE NO. 7 ON INQUIRY CARD

← CIRCLE NO. 6 ON INQUIRY CARD



Continuous clean power for communications at Cape Kennedy supplied by Kato as part of UPS system

Typical UPS unit installed at Cape Kennedy incorporates 250 H.P. Consolidated Diesel Engine that will start instantly, in event of prime power failure. Flywheel, mounted on shaft extension between motor and engine, would maintain constant generator speed during engine start-up to prevent even slightest power interruption. KATO Motor is 250 H.P., 208 volt, 3-phase, synchronous type with brushless excitation. KATO Generator continually feeds 150 kw of pure 120/208 volt, 60-cycle, power to communications system.

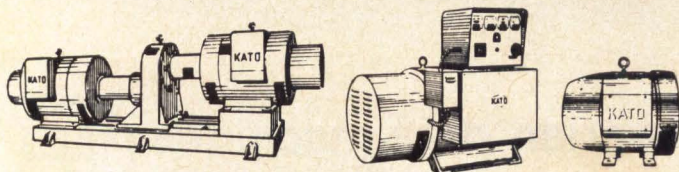
KATO matched Motor-Generator Sets are part of Consolidated Diesel Electric Company's Uninterrupted Power Supply units... used by NASA for Command Control Communications in space launchings and flights.

Pure power, constant power . . . power free from line transients, phase unbalance or frequency fluctuations . . . power completely protected from even split-second interruption. These were the rigid requirements NASA set for its communications system power supply. The UPS units, incorporating KATO M-G Sets in their design, met all specifications and, today, are fulfilling all operating requirements at Cape Kennedy.

KATO M-G Sets are not only serving in a wide variety of critical military and government applications.

Thousands are at work in the computer, process, manufacturing and service industries, performing an almost infinite variety of load-isolation, frequency-change and power-conversion functions, in addition to serving in "no-break" and "no interrupt" systems, such as UPS.

What's your power problem? Write for free 8-page brochure on KATO M-G Sets and control equipment. Over 40 years of power engineering experience is ready to go to work for you.



KATO makes many power products including: M-G Sets, AC Generators, DC Motors and Generators.



KATO ENGINEERING COMPANY

1403 First Avenue • Mankato, Minnesota 56001

CIRCLE NO. 8 ON INQUIRY CARD

WIN A 1970 CAR FROM FAIRCHILD:



Please enter my name in your New Product sweepstakes.

NAME _____

TITLE _____

COMPANY _____

CITY _____ STATE _____ ZIP _____

Void wherever prohibited, licensed, taxed, or in any other way restricted by law. Employees of Fairchild Camera and Instrument Corporation, its advertising and sweepstakes agencies and their families are not eligible.

FAIRCHILD SEMICONDUCTOR SWEEPSTAKES
P. O. Box 68 Los Angeles, California 90051

Now that we have your attention, we have a short announcement to make:

We're introducing our 1970 product line. All monolithic integrated circuits—MSIs, LSIs and new linears. There will be a new one every week for the next 52 weeks. In stock. At Fairchild distributors. Complete with data sheets and reliability information. And, they will be available in volume. (The first eight are on the following pages.)

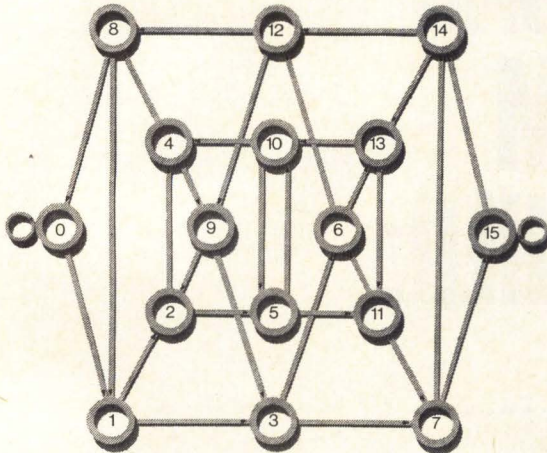
Any week we fail to announce a new product, we'll hold a drawing. The winner gets a 1970 car. To keep. Any model he chooses (up to \$4,000) or the equivalent in cash. Fill in the coupon and return it to us. We'll enter your name in the sweepstakes. Enter now. By 1970 you'll need a new car, anyway.

FAIRCHILD

9300 FOUR-BIT UNIVERSAL REGISTER

1.
Fairchild will introduce a new integrated circuit each week for the next 52 weeks. This is number 1.

The Fairchild 9300 is the first of a new line of highly versatile digital elements. It is an MSI (Medium Scale Integrated) device which requires greater complexity in less space, fewer external connection requirements and improved reliability. At the same time, the 9300 is extremely flexible and can be used in a number of applications. For example, it can function as either a high speed shift register, a high speed counter or a high speed storage element. It features 20 MHz unit frequency, type D input (obtained by tying together the J and K inputs), gated synchronous parallel input, C and Q output and complete compatibility with CCLSI elements. The 9300 comes in a hermetic, ceramic dual in-line package with a 16-lead configuration. It is available in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). The 9300 is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specifications, applications information and descriptions of other Fairchild MSI elements.



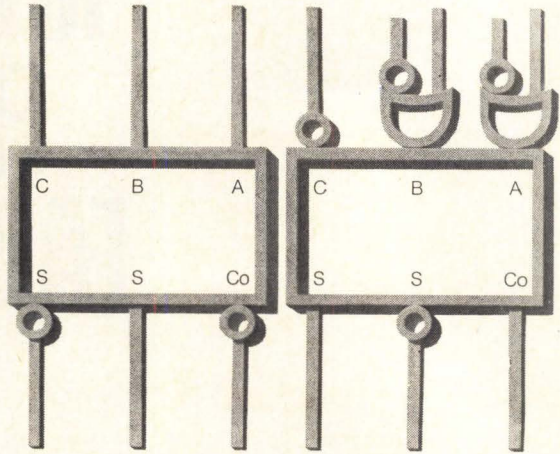
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-5011 • FAX: 916 379-4143

CIRCLE READER SERVICE NUMBER 101

9304 DUAL FULL ADDER

2.
Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number 2.

Fairchild's 9304 is a highly versatile MSI (Medium Scale Integrated) device with extremely fast carry propagation—less than typically 8 nanoseconds. It provides greater complexity in less space, fewer external connection requirements and improved reliability. Separate carry outputs allow the user to tie carry-in and carry-out individually or together. The 9304 is fully compatible with Fairchild CCLSI devices. It is also part of our new family of system building blocks. Others are shift registers, counters, decoder-interface devices, etc. It is applicable in any digital logic system. Its versatility means high volume production resulting in low unit cost. In addition to dual full adder, the 9304 can also be used as a parity checker, an exclusive OR circuit or for a number of other digital logic functions. It comes in a 16-pin hermetic dual in-line package. It is available in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). The 9304 is at your Fairchild distributor now. Write for complete specs, application information and descriptions of our other MSI devices.



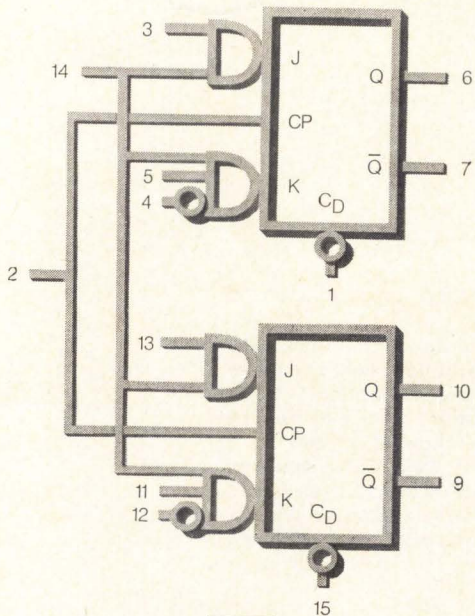
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-5011 • FAX: 916 379-4143

CIRCLE READER SERVICE NUMBER 102

9020 DUAL JK̄ FLIP-FLOP

3.
Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number 3.

The 9020 is a CCLSI device in a dual in-line package. It consists of two JK flip-flops with a common clock, separate J, K and K inputs and a common JK input. The JK input eliminates the need for gating clock waveforms and can result in simplified logic designs and minimized clock skew problems. The K input also allows the 9020 to perform as a dual type D flip-flop by tying the J and K inputs together. Clock loading is reduced by a single clock buffer. The 9020 is fast (50MHz) and flexible. It comes in a 16-pin hermetically sealed package. It is available in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). It can be obtained as a type D flip-flop or as a standard JK. The 9020 is available in volume quantities now. Fairchild distributors have it in stock. Write for complete specifications, applications information and descriptions of our other new products.



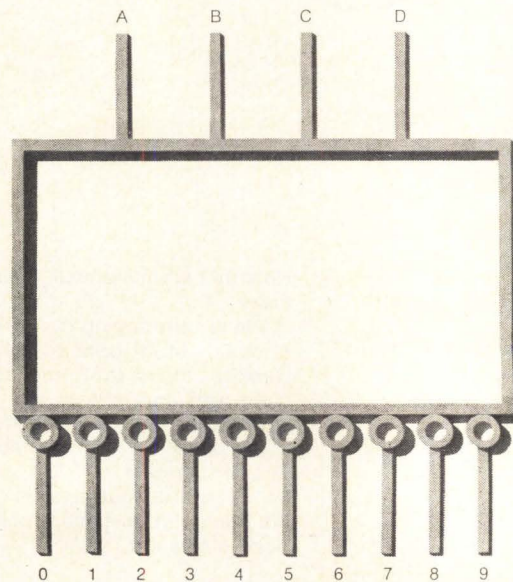
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-5011 • FAX: 916 379-4143

CIRCLE READER SERVICE NUMBER 103

9301 ONE-OF-TEN DECODER

4.
Fairchild will introduce a new integrated circuit each week for 52 weeks. This is number 4.

The 9301 is a CCLSI multi-function decoder in a 16-pin hermetic dual in-line package. It's part of our new family of system building blocks. Others are shift registers, counters, adders, etc. It is applicable in any digital logic system. The 9301 is designed to give added flexibility to Fairchild's Medium Scale Integration (MSI) devices. MSI already offers greater complexity in less space, fewer external connection requirements and improved reliability. As an example of its many applications, the 9301 can serve as an input/output between our universal register (9300), memory cell (9001) and dual full adder (9304). It can also be used as an expanding digital demultiplexer, minimum generator, and as a decoder for any BCD code. It comes in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). The 9301 and other MSI devices mentioned above are available in volume. Fairchild distributors have them in stock now. We also have a comprehensive literature package that discusses, in depth, all the advantages of Medium Scale Integration. Write for your free copy today.



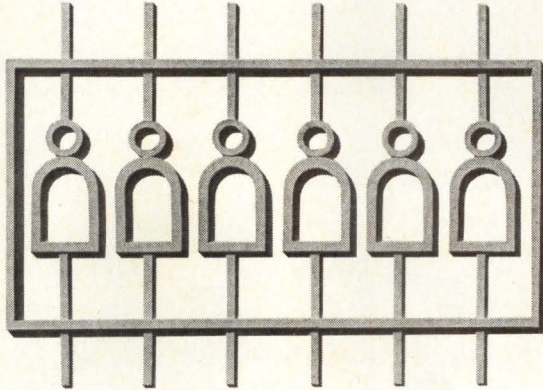
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-5011 • FAX: 916 379-4143

CIRCLE READER SERVICE NUMBER 104

9109 HIGH LEVEL HEX CONVERTER

Fairchild will introduce
a new integrated circuit
each week for 52 weeks.
This is number **5.**

The 9109 is the first member of a new high noise immunity integrated circuit family. It consists of six high-level DTL gates without input diodes. Each gate performs a single inversion operation. It can be expanded with external diodes on the input. Primarily, the 9109 is an interface device to convert high logic levels down to standard levels (CCDL, 800 series DTL, etc.) as well as other levels. In fact, it is ideal for interfacing from MOS to CCDL. It has an open collector output for compatibility with a variety of logic levels. Worst case noise immunity is 5.5 volts. It is a high voltage device suitable over the entire range of 12 to 20 volts. Its operating temperature is 0°C to +70°C. It comes in a hermetic dual in-line package. The 9109 is available in volume quantities. Your Fairchild distributor has it in stock. Write for complete specs, applications information and descriptions of our other new products.



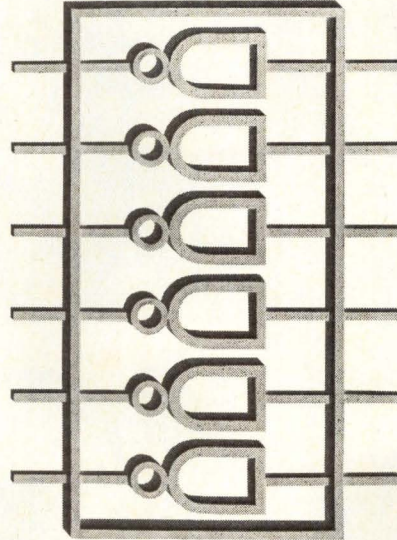
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-3011 • FAX: 510-378-6410

CIRCLE READER SERVICE NUMBER 105

9112 HIGH LEVEL HEX CONVERTER

Fairchild will introduce
a new integrated circuit
each week for 52 weeks.
This is number **6.**

The 9112 is part of our new family of high noise immunity integrated circuits. It is designed to convert CCDL logic levels to high logic levels. It is ideal for driving MOS devices. The 9112 consists of six high-level DTL gates without input diodes. Each gate performs a single inversion operation. Worst case noise immunity is 5.5 volts. It can be expanded with external diodes on the input. This high voltage device (stable over the entire range of 12 to 20V) operates from 0°C to +70°C. It comes in a hermetic dual in-line package and is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



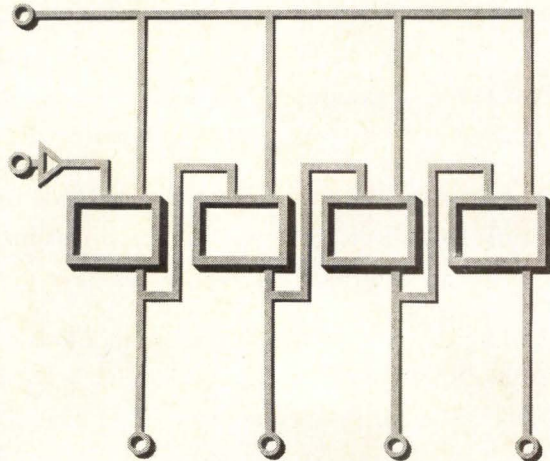
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-3011 • FAX: 510-378-6410

CIRCLE READER SERVICE NUMBER 106

9989 FOUR-BIT BINARY COUNTER

Fairchild will introduce
a new integrated circuit
each week for 52 weeks.
This is number **7.**

The 9989 is a low-cost, high rate, modulo 16 counter in a single package with great capability. It is compatible with the entire C.L. family and can operate directly into RTL, DTL or TTL circuitry. Typical power dissipation is only 130mW; its operating frequency is 15MHz. It is designed to operate in the 0°C to +70°C temperature range with nominal power supply voltage of 3.6 to 5.5 volts. The 9989 comes in a 14-pin hermetic DIP. Primary applications include counters, event meters and logic conversion functions. The four-bit binary counter is available in volume quantities. Fairchild distributors have it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



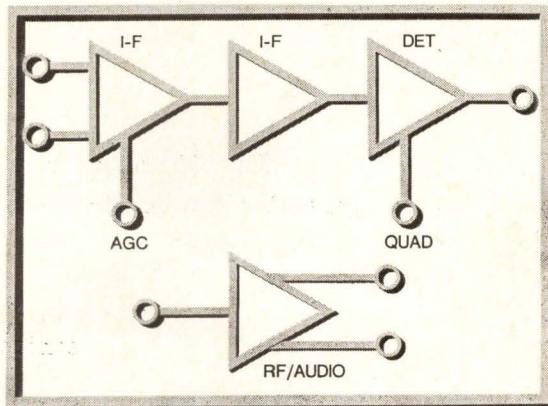
Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-3011 • FAX: 510-378-6410

CIRCLE READER SERVICE NUMBER 107

μA719 HIGH FREQUENCY COMMUNICATIONS SYSTEM

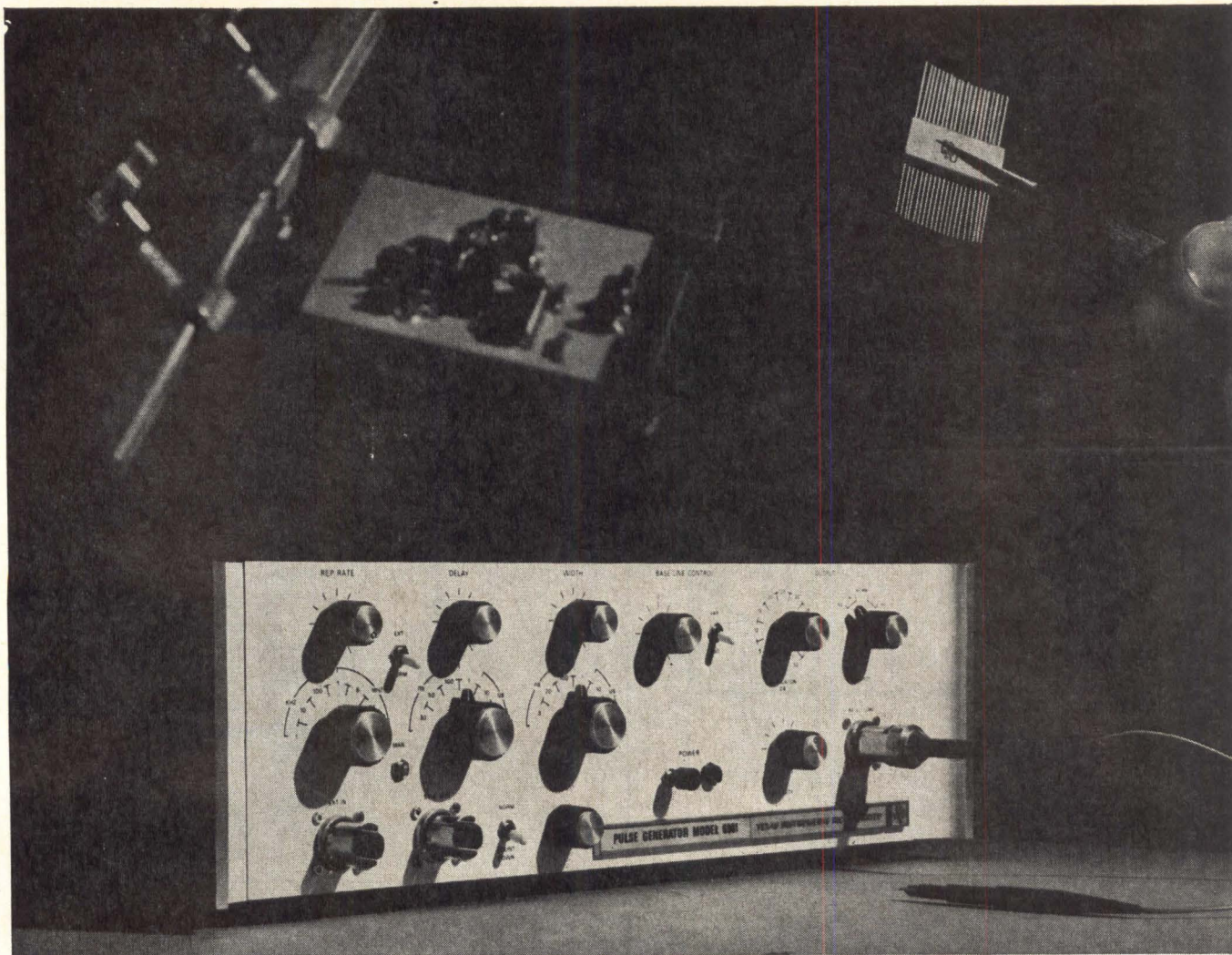
Fairchild will introduce
a new integrated circuit
each week for 52 weeks.
This is number **8.**

The μA719 is a new linear integrated circuit for military and industrial communications systems. It can function as an FM detector, an AM or FM IF amplifier, a modulator or an audio amplifier. It contains two independent amplifiers designed for IF systems to 50MHz. It provides excellent stability (70dB stable gain), AGC capability and extreme flexibility. And, it has three capacitors directly on the chip. The μA719 comes in a hermetic TO-99 package. It is available in quantity in both military and industrial temperature ranges (-55°C to +125°C and 0°C to +70°C). Your Fairchild distributor has it in stock now. Write for complete specs and applications information. Ask about our other new products, too.



Fairchild Semiconductor / A Division of Fairchild Camera and Instrument Corporation
SEMICONDUCTOR 313 Fairchild Drive, Mountain View, California 94035 (415) 961-3011 • FAX: 510-378-6410

CIRCLE READER SERVICE NUMBER 108



Why You Need a Special Pulse Generator for State of the Art Circuit Design



With high speeds and critical design parameters, you need the best test instruments to be sure your designs will be optimum. The TI Model 6901 Pulse Generator gives outputs from 1 KHz to 0.1 GHz; independent amplitude and baseline controls; jitter less than 0.1% of period + 50 psec; and countdown synchronization output.

The 6901 makes your designing simpler, too. Because the pulse amplitude of the generator can be changed without affecting DC offset, you can use the offset instead of an external bias supply for your circuit.

All this, and a price of only \$1950. For more information, contact your TI Field Office, or the Industrial Products Division, Texas Instruments Incorporated, P. O. Box 66027, Houston, Texas 77006.

TEXAS INSTRUMENTS
INCORPORATED

827

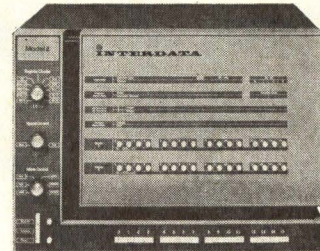
CIRCLE NO. 9 ON INQUIRY CARD

Planned parenthood is a family of computers from **INTERDATA**

● **MODEL 2**

NEW!

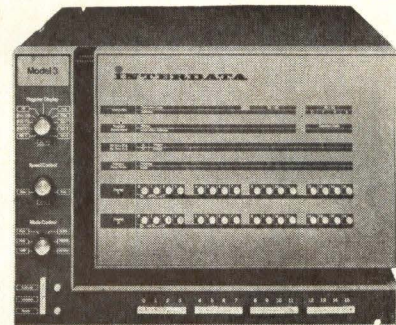
- 1,024 or 2,048 byte memory
- 45 μ s add time
- 3. μ s memory cycle time



\$4,700

● **MODEL 3**

- FORTRAN
- Hardware multiply, divide, and block input/output
- High speed memory access channels
- 4,096 to 65,536 byte memory
- 34 μ s add time
- 1.8 μ s memory cycle time

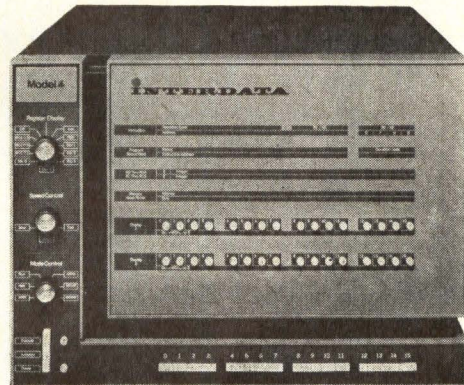


\$7,000

● **MODEL 4**

NEW!

- Hardware floating point
- FORTRAN
- Hardware multiply, divide, and block input/output
- High speed memory access channels
- 4,096 to 65,536 byte memory
- 3.9 μ s add time
- 1.5 μ s memory cycle time



\$10,000

■ The **INTERDATA** family features a basic repertoire of 77 instructions, modular memory expansion plus standard peripheral devices and system components. ■ 16 General Registers used as accumulators or index registers. ■ All memory directly addressable to the byte level by the primary instruction word. ■ Priority interrupt facility provides for interface of 256 devices.

**INTERDATA**

10350 Sunnyvale Road
Cupertino, California 95104
(408) 257-3418

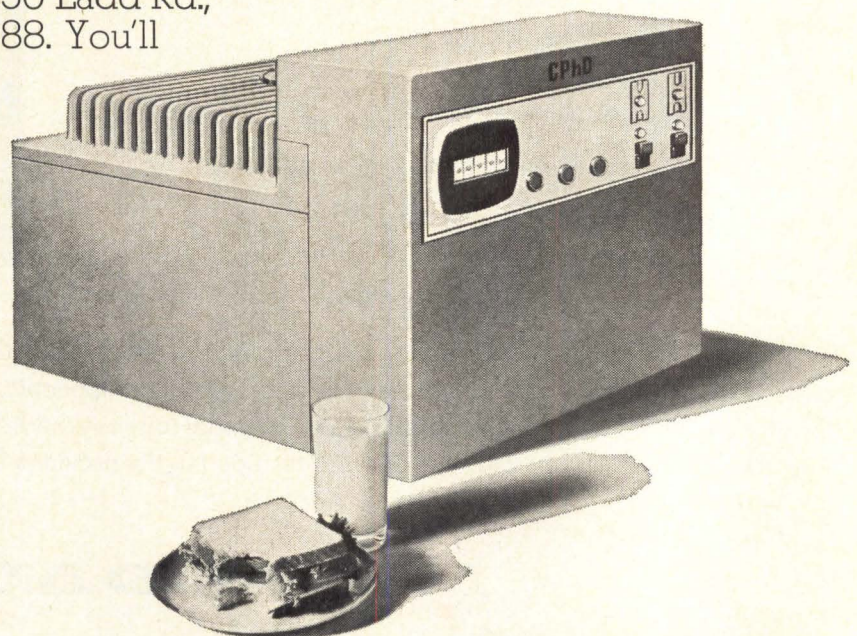
**Sales and Service in
48 states and Canada**

2 Crescent Place
Oceanport, New Jersey 07757
(201) 229-4040

Announcing the Bryant CPhD: 7.25 million bit capacity, no bigger than a breadbox.

No kidding. The new low-priced Bryant 10" drum packs 192 data tracks with Read, Write, and Select Electronics. And an average positioning time of 40 milliseconds. Just right for small and medium-size data processing applications. How do we do it? With Series 9000 integrated electronics—our new monolithic circuitry that's also more reliable and economical than conventional circuits. And more flexible. The mini-giant can be interfaced to nearly any computer system (new or only a gleam in somebody's eye), with either the Bryant XLO-1000 plug-in Controller or your own controller. Sound too good to be true? Contact your local Bryant sales office or write Ex-Cell-O Corp., Bryant Computer Products, 850 Ladd Rd., Walled Lake, Michigan 48088. You'll be a "Bryant Believer" before you know it.

**BRYANT
COMPUTER PRODUCTS**



CIRCLE NO. 11 ON INQUIRY CARD



If you think your system can't afford computer power, take a look at the new **DATA 620/i**

from
varian data machines

Data 620/i was designed from scratch as a powerful systems computer. That's why it so efficiently solves problems previously considered too difficult or expensive for computer solution. Data 620/i has a bigger instruction set, one-half the components, and costs less than any computer in its class.

Data 620/i has speed—1.8 microseconds cycle time, arithmetic power—long 16 or 18 bit words and 4K-32K word memories, control and I/O facilities, multi-level priority interrupts, and field-proven software.

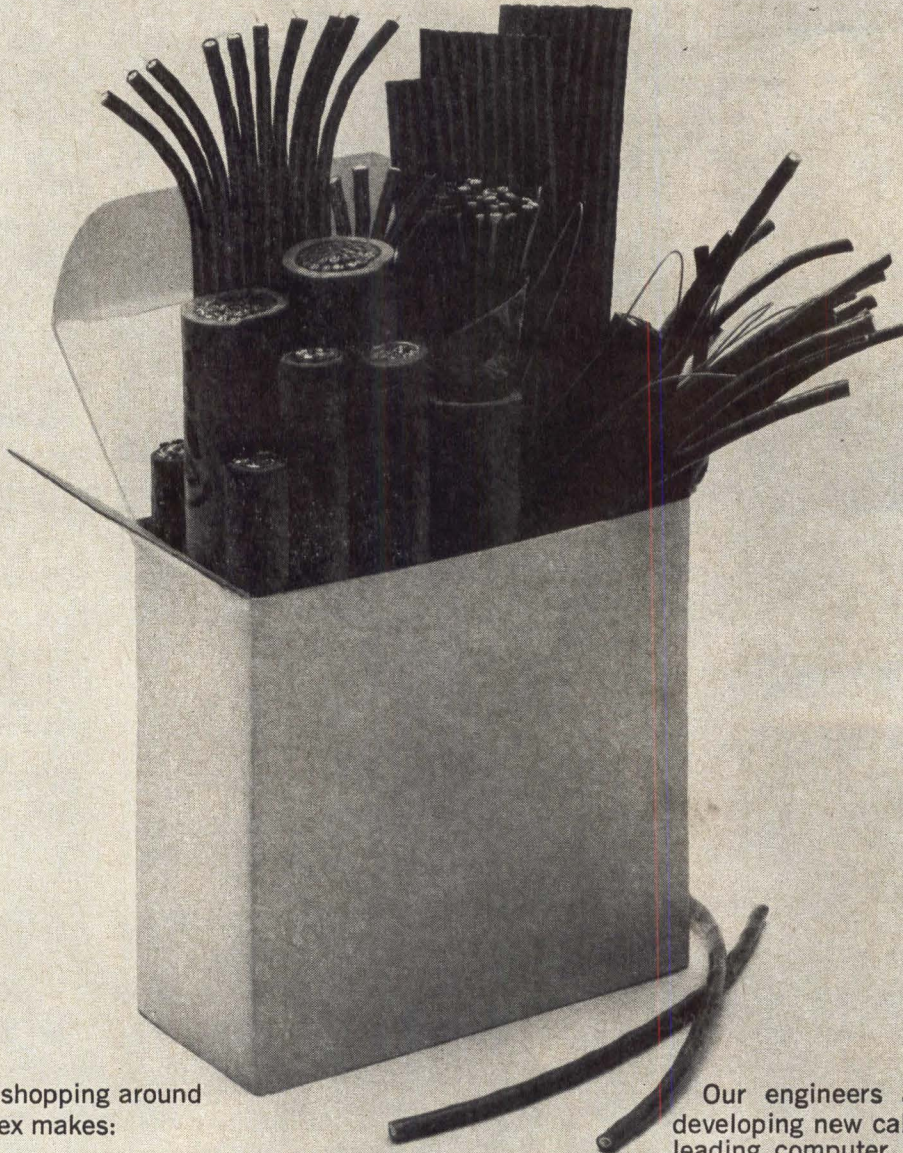
Data 620/i is extremely compact, requiring only 10" of 19" rack space, and comes at an even more compact price, with a 4K 16-bit memory and an ASR 33 Teletypewriter. Write for our new Data 620/i brochure full of facts and figures.



varian data machines
a varian subsidiary
Formerly Decision Control, Inc.

1590 Monrovia Ave., Newport Beach, Calif. (714) 646-9371

**Yes. You can get every
wire and cable you need
for a computer system in
one neat package...from
Brand-Rex**



You save a lot of shopping around because Brand-Rex makes:

- **Back-Panel Wires**
- **Hook-Up Wires**
- **Miniature, Air-Spaced Coaxial Cable**
- **Power Supply Wires**
- **Patch Cord Wires**
- **Interconnecting cables and Communication Cables.**

You can have just about any configuration... single wire, round cable, ribbon cable, custom profiles... and your choice of insulations including Kynar, Polysulfone, Teflon (FEP and TFE), PVC, semi-rigid PVC, PVC/nylon, polyethylene, foamed polyethylene, FEP/nylon, Rulan and Neoprene. Matched colors if you want.

Our engineers are constantly developing new cable designs for leading computer manufacturers. So if existing Brand-Rex products don't meet your needs, we'll come up with new designs that will.

Hooking-up a computer system? Get all the wire and cable from one good source. Ask Brand-Rex.

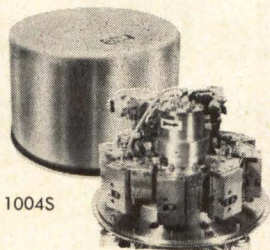
AMERICAN **ENRA** CORPORATION

BRAND-REX DIVISION

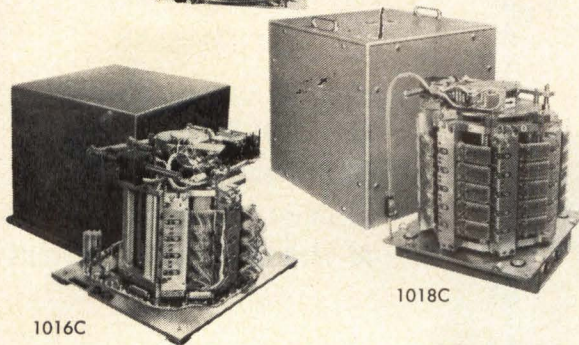
WILLIMANTIC, CONNECTICUT 06226
PHONE 203-423-7771



Fact:

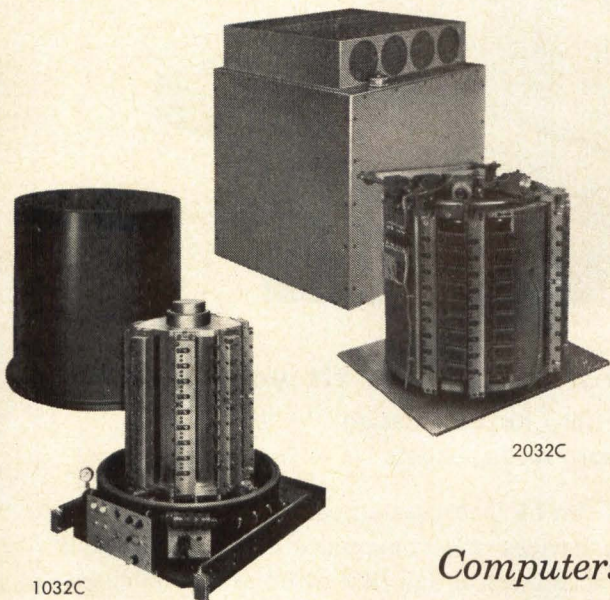


1004S



1016C

1018C



1032C

2032C

Five Standard Drums fill most "Special" Needs

Will a standard VRC drum memory meet *your* particular requirements? The following facts are helping lots of people answer with an emphatic "Yes!"

STANDARD VRC DRUMS ARE EASY TO USE. We supply all five models with *completely self-contained digital interface*. (Model 1004S is optionally available with diode boards only.) A self-clocking feature boosts readout accuracy and adds to application flexibility.

STANDARD VRC DRUMS ARE FLEXIBLE. Our 5-drum line covers a random-access storage range of 328,000 to 64,307,200 bits. Frequencies go up to 1.8MHz and average access to 8.7msec.

STANDARD VRC DRUMS ARE RELIABLE. Non-recoverable error rate is 1 in 10^{13} bits . . . design life, 100,000 hours . . . MTBF, 15,000 hours. All five models take 95° humidity, and operating temperatures from +40° to 105°F. with 100cfm air flow. Dust-tight, pressurized and sealed containers handle various operating environments. And here's the clincher. We back the reliability of all our standard drums with a full year's warranty. Want more details? Send for our new, 12-page Drum Memory brochure, DB-6711.

Computers are known by their MEMORIES

... so is

**Vermont Research
CORPORATION**

Box 20a

Precision Park, North Springfield, Vt. 05150
Tel. 802/886-2256 TWX 710-363-6533

**DRUM
MEMORIES
and
SYSTEMS**

When it comes to engineering opportunities (and the good life, North Country style), the place to come is Vermont Research Corporation. For specific information, contact: RICHARD A. STOVER, Vice President-Engineering.

CIRCLE NO. 14 ON INQUIRY CARD



Now... A bright, bold, readable CRT with broad interface capabilities

- 8-Level Code Compatibility
- Refresher Core Memory
- Integral Character Generator
- Modular Solid State Circuits

TEC CRT Display . . . the one that bends to fit your needs!

- Styling and Mounting Especially for Your Design
- Custom or Standard Keyboard Arrangements

See how comfortably the TEC CRT Display Systems can be incorporated as a data receiving and data transmitting source for computers, hard copy devices and communication links including Dataphone and teletype. Standard interface codes include ASCII and IBM or other 8 level codes. Electrical interface signal level options include 5 volt current sink I-C logic and EIA Standard RS-232B. Its compact screen displays 128 (3/8" high) or more flicker free alphanumeric characters. It's ready now! Floyd Raasch (photo), Director of TEC's Systems Research, which developed this display, is always ready to help tailor the TEC CRT to your special needs. Check the flexible one — write today for complete information.



INFORMATION DISPLAY
AND CONTROL DEVICES

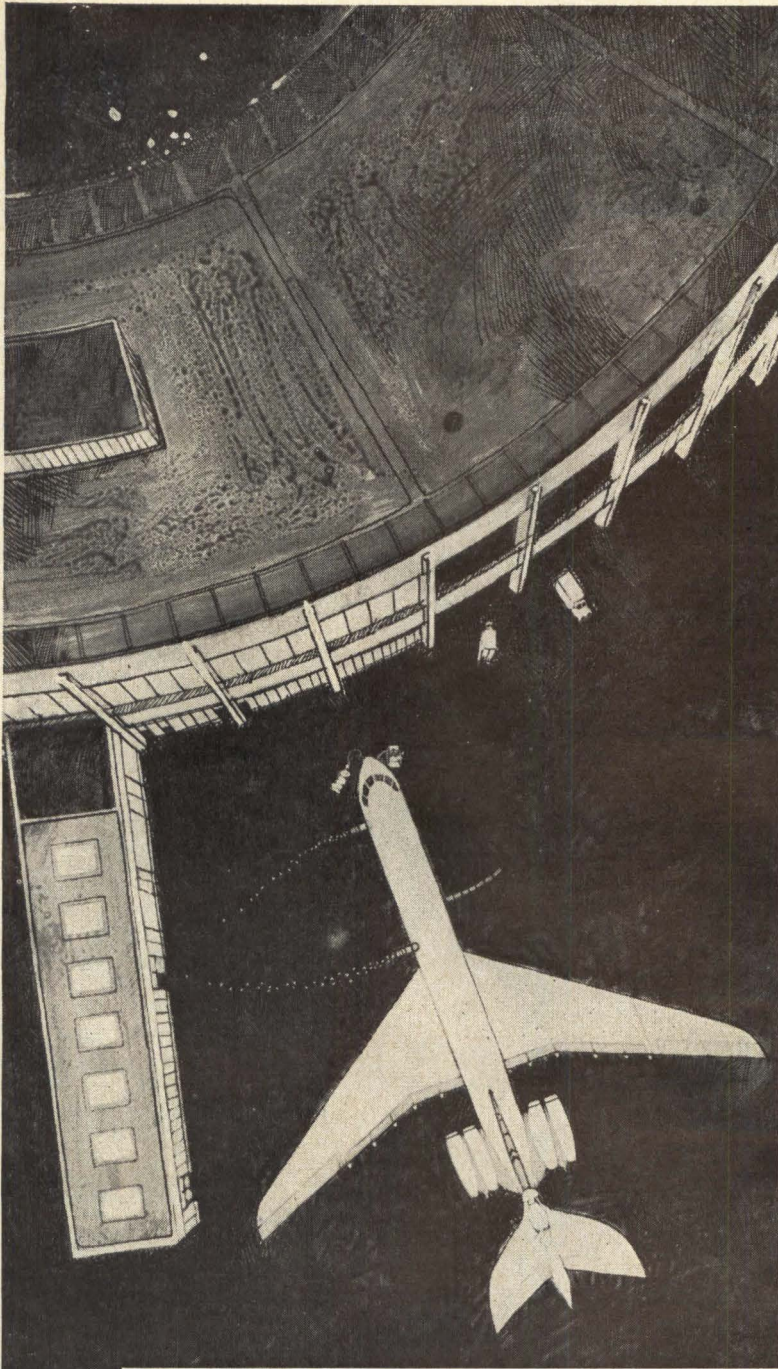
TRANSISTOR ELECTRONICS CORPORATION

Box 6191

Minneapolis, Minnesota 55424

Phone (612) 941-1100

CIRCLE NO. 15 ON INQUIRY CARD



BOAC wants confirmation in print of every passenger reservation made anywhere in the world. Right now.

Easy, when you ask Kleinschmidt.

Kleinschmidt is the language of modern telecommunications.

Home offices talk to division headquarters. Computers talk to production control. And in the case of BOAC, Kleinschmidt data printers in ticket offices provide passengers with fast, convenient flight reservations and confirmation.

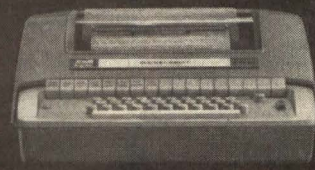
Working in communications systems like BOAC's, the Kleinschmidt 311™ Data Printer "talks" with unbelievable speed and simplicity. It prints-out up to four times as fast as most other teleprinters. Operates with far fewer moving parts and far more reliability. *Outperforms* all competition.

And like other Kleinschmidt data printers, the 311 is compatible with telecommunications equipment of all makes. It can fit directly into the system you now have, or the one you are having designed for you.

Of course, Kleinschmidt is a language most original systems manufacturers already understand.

But we're always glad to repeat the message.

KLEINSCHMIDT
DIVISION OF SCM CORPORATION
DEERFIELD, ILLINOIS 60015 · TELEPHONE: 312 945-1000



6 off-beat 2½ D stacks.

1 HEATED STACK — Built for a process control application, this has an extremely large bit length. (16K x 25 bits). Heaters keep the temperature a constant 55°C ±3°C; but the whole stack with heaters and large capacity only takes up 750 cubic inches.

2 FOLDED STACK — We've built hundreds of these for SDS computers over the past year. With a 4K x 9 bit capacity, the stack uses our 20 mil cores, and turns out a cycle time of 830 nanoseconds.

3 HIGH/LOW TEMP STACK — This 8K x 18 bit 2½ D, built for RCA, uses our special lithium cores. They have a low temperature coefficient and excellent stability over a 10°C to 55°C range. The beauty of this is that the customer doesn't have to bother with temperature compensation.

4 COMPACT STACK WITH LARGE CAPACITY — For Honeywell, we put together a 32K x 18 bit prototype stack in a space of 600 cubic inches (10" x 20" x 3"). This stack uses our

20 mil cores and has a cycle time of less than 650 nanoseconds.

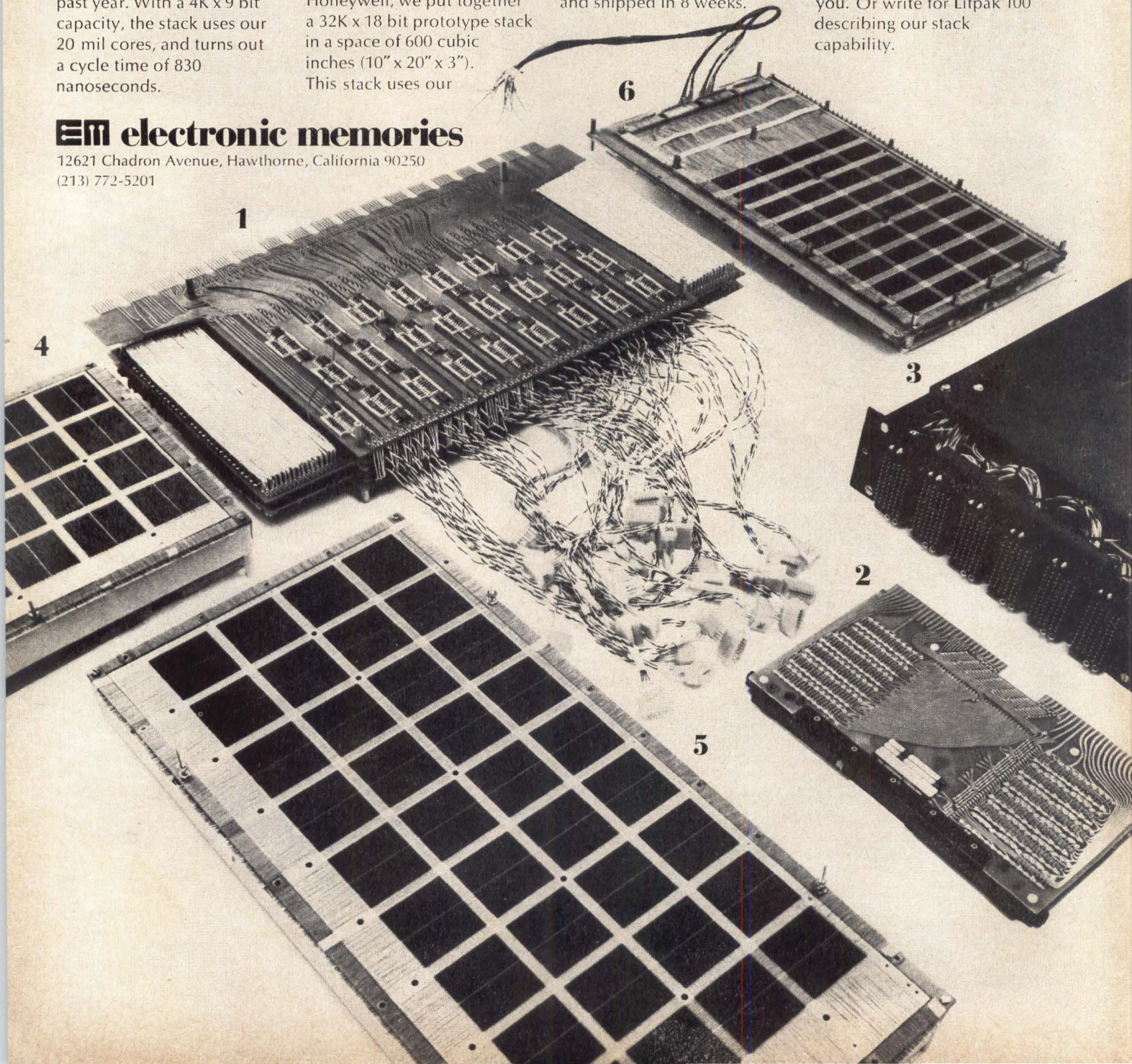
5 SPLIT MODULE STACK — This was a tricky one for Raytheon. It was a special 16K x 18 bit stack, and two sets of diode modules in the word direction had to be placed on each side of the stack. (Usually, they're all on one side.) The whole stack was designed, built, and shipped in 8 weeks.

6 NANOSTACK™ — We use this one in our large capacity NANOMEMORY system, but we've also been making a modified version for over a year and a half for Digital Equipment Corp. The stack has an 8K x 18 bit capacity and measures only 10½" x 20½" x 2".

If your 2½ D requirements are off-beat, call us, and we will see what we can do for you. Or write for Litpak 100 describing our stack capability.

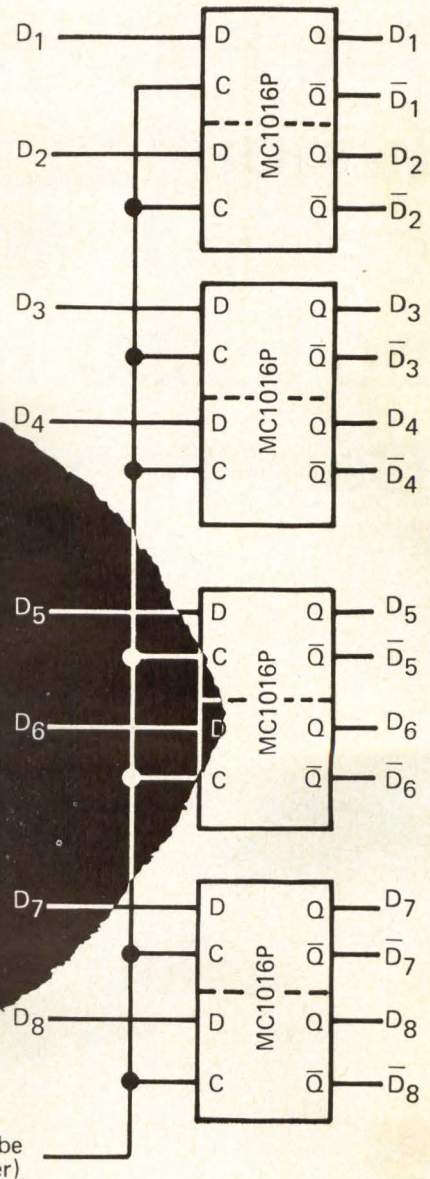
EM electronic memories

12621 Chadron Avenue, Hawthorne, California 90250
(213) 772-5201





Now, you can build a 5 ns
8-bit buffer register
with just four dual R-S flip-flops
(MECL II MAKES IT POSSIBLE!)



Clock or Strobe
(6ns or greater)

Yes, there's a new, simplified, less-expensive way to build a highly-versatile, widely-used 8-Bit Buffer Register. Simply use four MC1016P integrated circuits from Motorola's MECL II line.

These new dual R-S Flip-Flops reduce can count and system cost by increasing the number of functions per package. And, as a result, the interesting logic configuration shown above can be achieved with minimum cost and complexity.

The versatile MC1016P is an excellent clocked R-S flip-flop with single-rail input and dual-rail outputs. It can be used as a temporary storage element (as shown); as a memory data register; or, as a clocked R-S flip-flop with no undefined logic state.

This dual circuit employs two dc Set-Reset flip-flops with a positive enable or clock input provided for each flip-flop. Typical propagation delay is 5.0 ns, operating over the 0 to +75°C temperature range. Typical power dissipation is 125 mW at an operating frequency of 80

MHz. Minimum dc fan-out of 25 for each output is guaranteed.

Available in the 14-pin Unibloc* plastic package, the MC1016P brings to 27 the total number of MECL II functional elements — in the fastest, most flexible I/C logic line available. A comparable circuit — MC1216F — is also available in the 14-pin ceramic flat pack; and, provides identical performance over the -55 to +125°C temperature range.

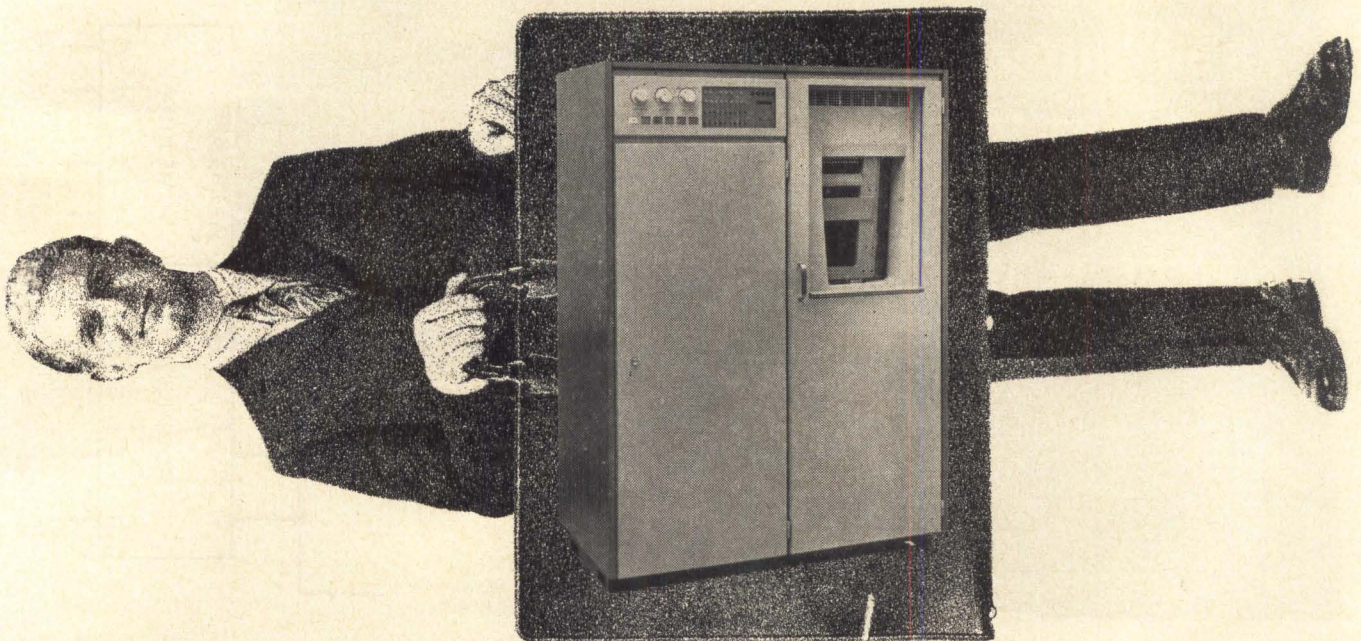
For complete details, including data sheets, application notes and prices, circle the reader service number. Then, contact your franchised Motorola Semiconductor distributor for evaluation units that you can try right now. You'll see why MECL II is being specified for many new system designs.



MOTOROLA
Semiconductors

— where the priceless ingredient is care!

The Peripheral People announce the availability of CRAM 5 (a 580 million bit, 90 to 150 ms retrieval Card Random Access Memory)



They all laughed when we sat down and developed CRAM. Now we announce our third generation, available for OEM sales. Our competitors are still trying to solve the problems of their first born.

Now, instead of 112 million bits, you can store more than five times as many and find your data 1/10th of a second faster.

With a single controller, you can hook up 16 of the new CRAM 5 units to accommodate over nine billion bits. And don't forget, you can change a cartridge in 30 seconds. We have lots of electro-mechanical experience so you know we know how to make it work. And keep on working. Quickly. Accurately. Inexpensively. Reliably. Well.



**THE
PERIPHERAL
PEOPLE**



Card Readers, Tape Punches, Tape Readers, Printers, MICR Readers, CRAM (Card Random Access Memory)

THE NATIONAL CASH REGISTER COMPANY • INDUSTRIAL PRODUCTS DIVISION • DAYTON, OHIO 45409
CIRCLE NO. 19 ON INQUIRY CARD



Our half-price model

I-41 Shuttle printer by Bull General Electric

Most medium speed line printers are really "cost-reduced," high speed printers. They're expensive.

But the I-41 shuttle printer by Bull General Electric was designed specifically to operate at 200 lpm. And it costs only about half as much as most "cost-reduced" printers. OEM quantity prices start under \$3,000.

The price tag is low because there are fewer components. Only one hammer for every four print positions. Fewer operating parts mean greater reliability, sharply reduced maintenance.

The I-41 is available now with 80, 120 or 136 columns, and 64 character set.

Quality and technological know-how are built into every Bull General Electric product.

Mail the attached coupon for full information on the I-41 and our complete line of Card Readers, Card Punches, Card Sorters, Key punches and Verifiers.

Bull Corporation of America, 1 East 57th Street, New York 10022

NAME _____
TITLE _____
COMPANY _____
ADDRESS _____

Please send full information on the I-41.
 I'd like information on your entire line of data processing equipment.
 Have a sales representative call immediately.

995-34

BULL
GENERAL  **ELECTRIC**

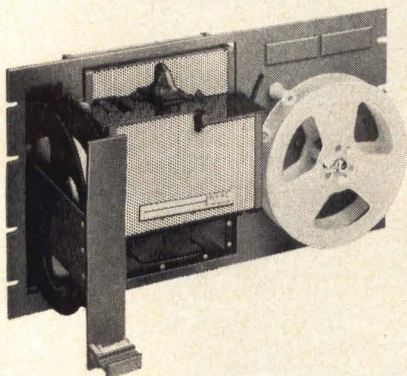
INVAC

MULTI-OPTION

TAPE

PUNCH

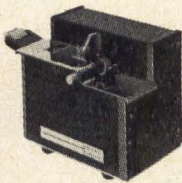
PACKAGES



INVAC Tape Punch Packages, Series PH, feature long-life and reliability essential for compact low-cost data handling systems requiring long tapes and punch speeds up to 60 cps. The many available options adapt these Packages to virtually any system design.

- . . . Compact 10 1/2" panel height
- . . . Optional Punch Speeds
- . . . Optional Power Supply
- . . . Optional Drive Electronics
- . . . Optional Sequencer Electronics
- . . . Optional Code Delete
- . . . Optional Tape Feed

INVAC MODEL P-135 TAPE PUNCH is available separately. Solenoid operation eliminates maintenance-prone motors and clutches and also minimizes drive power requirements. 100,000,000 operations guaranteed.

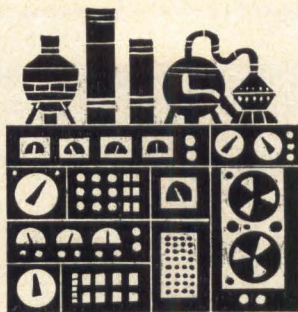


Write for data

••••• **INVAC**
CORPORATION

26 Fox Road, Waltham, Massachusetts 02154
Tel. (617) 899-2380

PHOTOELECTRIC KEYBOARDS • TAPE PUNCHES
READERS AND HANDLERS • I/O TYPEWRITERS
PRINTERS AND SYSTEMS
CIRCLE NO. 21 ON INQUIRY CARD



INDUSTRY NEWS

A WESTINGHOUSE PRODAC 50 COMPUTER SYSTEM IS BEING USED FOR NATURAL GAS DISPATCHING AND REMOTE CONTROL OF SYSTEM PRESSURES by the United Gas Improvement Company of Philadelphia, Pa. The equipment went into operation recently at Reading, the center of UGI's gas territory. In this unique application, the Prodac equipment acts as brain for a telemetering system that measures the flow of gas and controls certain pressures in a pipeline system covering a territory of about 2400 square miles. The computer's real-time operations result in a more economical flow of gas from transmission company lines through UGI's vast distribution system to its customers. The computer also gives UGI officials up-to-the-minute reports on purchases, sales, and storage of gas for demand control and bookkeeping purposes. According to G. Chris Turner, general manager of the Westinghouse Computer Systems Division, the Westinghouse Prodac 50 was selected because it is the only computer control system capable of doing the job at a cost low enough to be economically advantageous to the utility.

.....

COMPUTER GRAPHIC SYSTEMS REACH ECONOMICAL LEVEL— Aerospace firms can economically employ computer graphic systems available on today's market which permit an engineer to communicate directly with a computer during the design process.

This conclusion was drawn in face of disagreement in many aerospace management circles on the cost of using such systems, by Thurber J. Moffett, senior staff engineer for man-computer interactive systems at TRW Systems Group, Redondo Beach, California.

Moffett addressed an afternoon session of the week-long annual meeting of the American Institute of Aeronautics and Astronautics held at Anaheim, Calif., October 23rd through the 27th. "Now that the feasibility and applicability of computer graphic systems have been successfully demonstrated," he said, "Firms with large manpower requirements to produce engineering drawings, are seriously beginning to evaluate computerized drafting as a means to increase drawing output."

He then furnished a general method of analyzing the recurring costs and savings when such systems are employed by aerospace firms, where engineers typically spend the majority of their work days at a drafting board, and where engineering drawings are a principle output.

The analysis concerned the different ways such personnel now spend their time, and how computer graphic systems might be expected to reduce that time. Moffett related the number of graphic consoles that can be employed for the amount that is saved by their use, to an operational savings, loss, or break-even point.

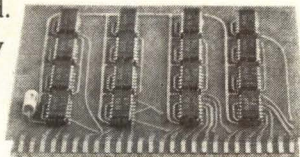


A word to the do-it-yourself module builder:

Don't.

Buy our J Series modules instead.

The J Series is our new family of general purpose, all integrated circuit logic modules. Their performance almost matches that of our famous T Series modules, but they cost about 25% less. They're made to the same dimensions as the T Series, with the same 52 pin connectors, so they're physically interchangeable. We make them for our own seismic recorder systems, so they're rugged and reliable. Now, as of January, you can buy them (com-



These will cost you less.

plete with mounting hardware, racks and power supplies, if you wish) in any of 25 different functions.

And save yourself the time and cost of making your own: designing, assembling, testing, new procedures, new equipment, new personnel, additional training, to say nothing of the added paper work.

If you're building systems, you must have better things to do than go into the module assembly business. Such as reading our J Series catalog.

It's free.

SDS
Scientific Data Systems,
Santa Monica, California

Cinch-Graphik

high speed
plug-in
fixed store
memory
planes
less than
1¢ per bit!



Fixed resistor matrices, using nickel-phosphorus thin-film resistors on G-10 glass-epoxy substrates provide many advantages to the logic or system designer.

FLEXIBILITY: Plug-in card configuration permits rapid language changes and fast, economical programming. Language changes within the same matrix can be made in minimal time at low cost.

PERFORMANCE: Discriminates against capacitive and inductive parasitic coupling. Resistive loading damps drive and sense line transients, particularly at high speeds.

SPEED: 150 nanoseconds.

BIT DENSITY: Up to 100 per square inch.

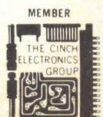
STABILITY: TC is +80 ppm/°C and drift is always positive (less than 2% after 5000 hours @ 75°C @ 2 watts/in²).

For additional information, contact Mr. Leo Thomas, Thin Film Department, Cinch-Graphik, 200 S. Turnbull Canyon Road, City of Industry (Los Angeles), California 91744, phone (213) 333-1201. CG6744

THIN FILM DEPARTMENT

CINCH-GRAPHIK

DIVISION OF UNITED-CARR



CONSISTING OF CINCH MANUFACTURING COMPANY, CINCH-GRAPHIK, CINCH-MONADNOCK, CINCH-NULINE, UCINITE (ELECTRONICS) AND PLAXIAL CABLE DEPT.

He concluded that even the systems available today can be economical to the user. However, he stated, "These systems are far less efficient than systems that will be ready within two years."

PATENT ABSTRACTS JOURNAL—The Patent Office, U.S. Department of Commerce, will begin publication January 2, 1968 of a weekly journal to contain abstracts and drawings of U.S. patents, according to Commissioner of Patents Edward J. Brenner.

The object of the journal will be to provide non-patent oriented scientists, engineers, and businessmen easier access to the important technical information contained in patents, Commissioner Brenner said. For this purpose, abstracts have been required as part of patent applications since January 1, 1967. The Patent Office requires that abstracts be concise summaries of the technical content of patents, avoiding use of the legal and patent phraseology characteristic of patents and patent applications.

Subscriptions to the new journal, entitled Official Gazette Patent Abstracts Section, are being offered on a six-months basis (January through June 1968) by Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402, price \$27.

NEW COMPUTER-CONTROLLED DECOM SYSTEM—An engineering approach to decommutation systems that uses computer program-storing capabilities and cuts the cost of the decommutator has been reported by Stellarmetrics, Inc.

The Santa Barbara aerospace communications firm says that the new design concept reduced the cost of

← CIRCLE NO. 23 ON INQUIRY CARD

a recent decommutation system from the \$80-100,000 region, typical of earlier systems, to a new figure of approximately \$54,000.

Computer-controlled decom systems previously required a high degree of program storage capability which added to the cost. In a Wichita, Kas., Stellar-metrics is using the program-storing capability of a CDC 3200 computer with which the decommutation system will interface. As a result, the decommutator itself needs only a simpler storage for a single program being acted upon at any one time. The company says it believes this is the first time such a technique has been used.

Decommutation systems are the "translators" of computed signals from space vehicles or other sources. In the Boeing application, the new equipment will decommutate tape recordings from flight tests.

.....

ELECTRONICALLY CONTROLLED PRESS—A "new-generation" offset printing press with a built-in-digital logic system to monitor and control its operations has been developed by the Harris-Intertype Corporation. Called the "Harris Lithotronic-78" press, its design is a combination of advanced mechanical features and electronic innovations said to make it the most productive sheet-fed offset press. A typical five-color model is priced at approximately \$800,000.

The most significant control unit developed for this press is an electronic digital logic system that monitors many press functions and supplements the knowledge and skills of the press crew. This system is composed of an electronic logic panel receiving both press and operator command-signals and re-forming these signals into programmed de-

isions to control press-function actuators.

The logic contains three digital registers—counters that store information related to press position and timing. One section forms command signals to control the registers and the output logic. Three matrices utilize the binary output of the registers to fabricate specific signals required by the output logic. A counter-inhibit pulse insures that the output logic is blocked out while the outputs of the registers are changing.

An interface panel is incorporated to eliminate the possibility of transients or crosstalk.

Significant events in the offset printing operation are monitored and controlled by the logic system. Not only is every revolution of the cylinders counted, but 12 specific radial positions—representing specific functions in each revolution—are monitored and controlled.

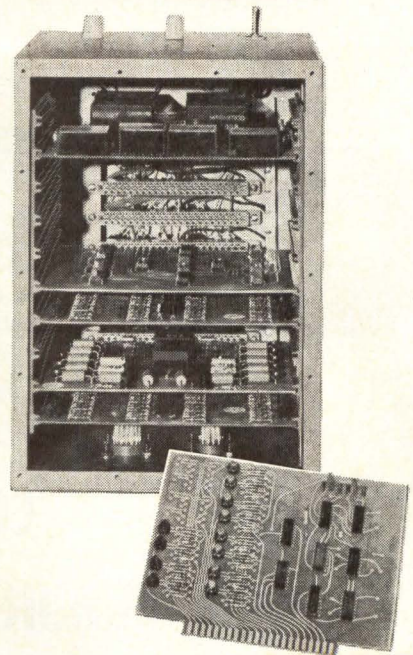
Through the master control console, the pressman can program the press to pull individual color proofs, or any combination of color proofs, prior to or even during the course of a run.

.....

DIGITAL CONTROL SYSTEM FOR STEEL ROLLING MILL—Compat Corporation, of Hicksville, New York, is currently installing the second of three mill control systems ordered by a leading steel company in the U.S. The system provides the interface between a PDP-8 computer, the thickness gauges, and the rollers.

By measuring variations in the thickness of metal being rolled at speeds of up to 600 feet per minute, the system "anticipates" what corrections will be needed to keep the output thickness

NEW!



VERNITRON Solid-state Digital to Two- Speed Resolver Transformer Converter

Already in use on
"HYBRID SERVO SYSTEMS"
to simulate a resolver
transformer

Input of this remarkable unit is 16 bit binary digital data (angle O) and resolver transmitter data (angle O). This input data is converted to two-speed resolver transformer data; sine (O-O) and sine (80-80).

Input logic levels

Binary "1" = 4 VDC

Binary "0" = 0 VDC

Conversion time: less than 10 microseconds

Accuracy: 1 minute; 30 sec. available

Temperature: 0°C to +70°C. Extended temperature ranges available

DC Power required: 15VDC at 500 ma
15VDC at 500 ma

Standard package size

Height: 5.5"; Width: 7.0"; Length: 9.75"

**WRITE TODAY FOR ILLUSTRATED,
FULL-SPECIFICATION BULLETIN**

THE QUALITY NAME IN
DIGITAL DEVICES

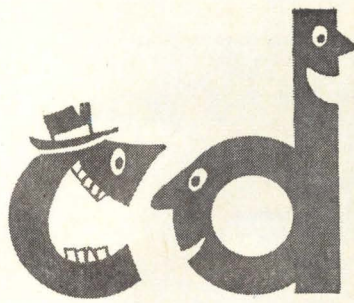


DIGITAL PRODUCTS DIVISION:
80 Central Ave., Farmingdale, L.I., N.Y. 11735
(516) 694-5002 • TWX: 510-224 - 6890

**TORRANCE DIVISION AND
WESTERN REGIONAL SALES:**
1780 South Crenshaw Blvd., Torrance, Calif.
(213) FA 8-2504 • TWX: 910-349 - 6250

**ENCODERS, SOLID STATE CONVERTERS,
SYNCHRO-TO-DIGITAL, DIGITAL-TO-SYNCHRO,
AND DIGITAL-TO-RESOLVER CONVERTERS**

CIRCLE NO. 24 ON INQUIRY CARD



commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

COMPUTER COMMUNICATIONS SYSTEMS

Hardware versus Software

Over the past few years, use of remote communications equipment tied into digital computers has increased tremendously, as a result of the realization that an economical and fast turn-around computer service can be provided to many users simultaneously from one large computer equipped with the appropriate communications equipment and time-sharing software. This increase has led to development of a significant number of time-sharing services which aim to give the user at the end of a teletype line direct, and apparently exclusive, access to a large scale digital computer.

Time-sharing systems can be conveniently divided into those providing a general purpose computing service, and those designed to give a specialized service to one type of user only. In the general purpose category, Project MAC at MIT was the pioneer, and is still the leader in sophistication and in facilities provided to the user. Very large and expensive computers are used in this system, and the user has available a wide range of software facilities as well as very extensive virtual core memory

The author of this month's CD Commentary, Dr. C. B. Newport, is Manager of the Information Systems Department at Honeywell Computer Control Division. He is responsible for communications control, scientific control and display, and applications in the General Systems Section.

facilities. (The word "virtual" refers to the core memory apparently available to the user. In reality he is only using a small amount of core memory and his programs and data are being swapped to and from a large backing store as other users make demands on the time and space in the computer.)

Special purpose time-sharing systems serve a particular group of users and include airline reservations systems; custom-designed commercial computing facilities, such as Keydata; and special remote information handling systems for the medical community, such as Medinet, and for branch-office insurance transactions.

Other computer applications in which communications play a vital part include message switching, data acquisition and control, and simple computer-to-computer information interchange. Remote data collection, in what would otherwise be conventional commercial data processing systems, is also becoming more and more common.

It is interesting to note that with all these applications demanding remote access to computers, and hence the extensive use of long distance communications links, still only approximately 5% of the installed computers have some sort of communication equipment associated with them. However, by 1973, it is anticipated that this percentage will have risen to 60% and possibly to as much as 80% by 1980. These predictions indicate that future computer system analysts and hardware designers will need a clear understanding of the operation of computer communication systems and how to make the most fruitful tradeoffs between hardware and software.

Hardware and Software Design

The first task of the system designer is to consider the cost of the over-all hardware design. Complete minimization of hardware cost is usually undesirable because this almost always increases software and operating costs, and hence does not minimize total system cost.

One of the very significant expenses in a wide-ranging time-sharing system is the cost of the com-

munications lines. The first hardware decision is, therefore, whether data concentrators can be used to minimize the line costs. These devices are designed (1) to receive a number of low-speed lines (50 to 180 bits per second) — all operating simultaneously and (2) to concentrate the information onto one or more high-speed lines (1200 or 2400 bits per second). Although data concentrators may cost from \$5,000 to \$100,000, they may still represent a considerable financial saving on long distance lines when it is realized that the rental cost of a voice-grade line (up to 2400 bits per second) is only of the order of twice the rental of the low-speed line (up to 180 bits per second).

The simplest data concentrators consist of no more than time division or frequency division multiplexers which allocate time slots on the high-speed line to each bit of incoming data from the many low-speed lines. The information on the high-speed lines is therefore not directly usable without a demultiplexing process at the computer end. This requires a data deconcentrator which then presents the computer with the problem of interfacing to the original number of low-speed lines.

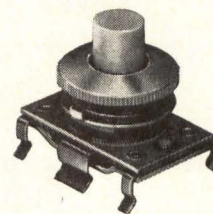
As the complexity of the over-all system increases, the very simple data concentrators do not provide the optimum solution, since a considerable amount of equipment is needed at the computer end to interface the many low-speed lines. Also, a large amount of computer time is needed to provide the information handling and control of these individual lines.

A more satisfactory solution for the larger communications networks is to provide "intelligent" data concentrators — small, high-speed general-purpose digital computers designed to have good communication capabilities: extensive I/O facilities, easy character manipulation, very-high-speed logical and I/O instructions, and low cost. These concentrators can undertake far more than simple multiplexing of the low-speed lines. First, they can accumulate incoming messages into conveniently sized blocks and transfer them, suitably identified, directly to the central computer. Similarly, in the outgoing direction, the concentrators may receive complete messages from the central computer and store them temporarily while low-speed onward transmission is taking place. This eliminates the need for a deconcentrator and a large communications interface at the central computer end, thus justifying the higher initial cost of the computer-based concentrator. Computers provide additional bonuses, moreover, since with little increase in programming cost, they can serve other functions such as parity checking, low-speed line control (initiation and termination of transmissions), calling of remote stations, checking of message validity, "busing out" of low priority lines to prevent central computer overload, handling low-speed lines connected to the switched network (dial-in facilities), and many other incidental communication functions.

The tradeoff, thus far, indicates the use of lines connected directly into the central computer where the total area covered by the network is fairly small. With a widely spread but relatively unsophisticated

Now! Changeable pushbuttons and decorative facing nuts in 7 colors make switch panel color-coding a snap!

Now control panel arrays of unlighted pushbutton switches can be decorative and functionally color-coded . . . in a snap. MSC Building Block Switches feature snap-on, removable pushbuttons in 2 styles and 7 colors . . . decorative aluminum facing nuts . . . and a choice of 2PDT or 4PDT alternate or momentary action switches that can be bench wired then snapped onto a premounted bracket. This versatility lets you change pushbutton colors anytime, or remove a switch for wiring change without disturbing the panel. For detailed data on these and other MSC unlighted switches, write on your letterhead for immediate service or use the publication reader service card.



Series 19

Building Block Pushbutton Switches

RATED AT
5 AMPS/125 OR 250 VAC

7/8" PUSHBUTTON

5/16" PUSHBUTTON

CONCAVE FACING NUT

MOUNTING BRACKET

SNAP-ON SWITCH

CONVEX FACING NUT

TAKE YOUR CHOICE!

PUSHBUTTONS
2 Styles-7 Colors

FACING NUTS
2 Styles-7 Colors

MOUNTING BRACKET

2 PDT or 4 PDT SWITCHES
Mom. or Alt. Action

Master Specialties Company

25 YEARS IN INFORMATION DISPLAY AND CONTROL DEVICES

MSC Master Specialties Company, 1640 Monrovia, Costa Mesa, Calif. 92627 • Telephone (714) 642-2427 • TELEX 6-78433
Offices in Principal Cities.

Also available thru AVNET ELECTRONICS

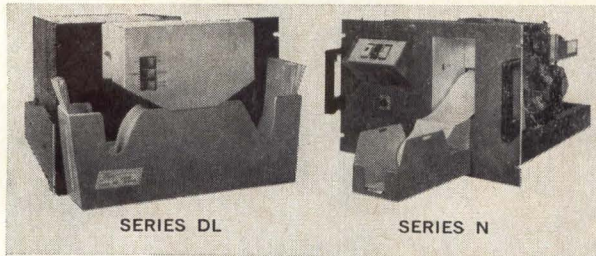
WESTBURY, LONG ISLAND, NEW YORK • (516) 333-5800

CIRCLE NO. 25 ON INQUIRY CARD

everybody else talks

- **LOW COST**
 - **HIGH SPEED**
 - **RELIABILITY**
- for digital printers

— **DI/AN*** has done something about it . . .



DI/AN DIGITAL PRINTERS FEATURING:

- **LOW INITIAL COST (FROM \$2000)**
- **UP TO 40 LINES PER SECOND**
- **ELECTRONIC ADJUSTMENT OF VERTICAL CHARACTER ALIGNMENT**
- **MULTI-PART PAPER (ORIGINAL AND TWO COPIES)**
- **INTEGRAL PARALLEL AND SERIAL ENTRY BUFFERS**
- **UP TO 32 COLUMN CAPACITY**
- **PRE-DESIGNED INTERFACE OPTIONS**
- **PROPRIETARY INKING ROLLER SAVES UP TO \$500 PER YEAR OVER RIBBONS**

SEND FOR COMPLETE INFORMATION ON THE DI/AN LINE OF DATA LOGGING, COMMUNICATIONS AND COMPUTER PRINTERS



*THE INDUSTRY'S ONLY ELECTRONIC SYSTEMS/MECHANICAL HOUSE



DI/AN CONTROLS, INC.

944 DORCHESTER AVENUE, BOSTON, MASSACHUSETTS 02125
PHONE: (617) 288-7700 TWX: 710-333-0774

CIRCLE NO. 26 ON INQUIRY CARD

communications and computing system, simple concentrators are most attractive. As the complexity increases, computer-based data concentrators, with their ability to unload the central computer, prove to be the most economical answer.

Interfacing to the Computer

Computers in communications systems need to interface with a small number of high-speed lines (from sophisticated data concentrators or high-speed data sources) and/or with a large number of low-speed lines (from simple data deconcentrators or from local low-speed terminals). This dictates the design of two distinct types of hardware interfaces: (1) the single-line controller and (2) the multiline controller.

The single-line controller is basically a shift register designed to receive serial data from one communication line (usually high speed, 2400 bits per second) and accumulate characters which are transferred in parallel one at a time into the main computer memory. One of these devices is required for each of the incoming lines; hence the name.

The multiline controller is a more complicated device designed to handle a large number of serial communications lines (usually low speed) and accumulate characters from these lines for transfer into the computer memory. The basic multiline controller module may be designed to handle 128 or 256 lines, and for each line actually connected, a small line termination unit would be provided. This device therefore has a higher initial cost than a single-line controller, but a very much lower incremental cost per line.

The interaction between hardware and software immediately becomes apparent as the design of these controllers is undertaken. Single-line controllers usually operate with synchronous lines. It is reasonable to include hardware for the detection of sync characters, since the software to undertake this operation is particularly time consuming. However, many other message control characters are used, including Start of Heading (SOH), Start of Text (STX), and End of Transmission (EOT). Although there are ASCII codes for these format characters (and a number of others), they are by no means universally used, so the designer must decide whether to incorporate the detection of these in the hardware or the software. Some of the more elaborate systems do incorporate hardware detection of special characters, but this can lead to loss of flexibility and considerable difficulty when communicating between two systems that use different standards. A solution that is becoming more common in large systems is to use a small computer, similar to that employed in the data concentrators, to interface the communication lines directly into the main processor. Simple single-line or multiline controllers can then be used and the format control and processing can be undertaken in the small peripheral computer. Communication with the main machine would then be on direct bus-to-bus, or memory-to-memory, connections. In this case, the tradeoffs indicate **simple** single-line controllers with a minimum of special character detection and con-

trol facilities, and most message control being undertaken in the main computer, or, in very large systems, in a peripheral computer.

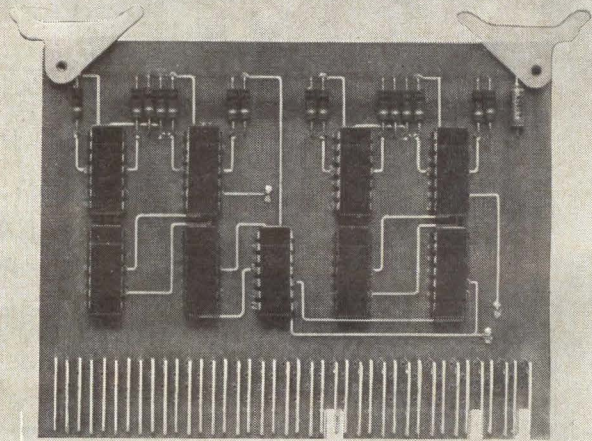
There are two basic types of multiline controllers. In one, the character assembly — and some character checking — is undertaken entirely in hardware, and fully matured characters are transferred into the computer. In the other type, the programmed multiline controller, an absolute minimum of hardware is used; the computer software is relied on to assemble the characters itself.

With the programmed multiline controller, the computer samples the state of the incoming lines at least eight times faster than the lines themselves can change state. From these samples, the software is able to assemble full characters and accumulate them in memory buffers. It can be appreciated that this technique uses a minimum of hardware, little more than one gate per line, but makes extensive demands on the computer software. A peripheral computer, therefore, becomes a necessity in all but the simplest situations. A typical communications computer, having a one-microsecond memory-cycle time, can be expected to handle at least 128 lines by this technique before it becomes overloaded. With the number of lines in this region, it is usually more economical to provide such a peripheral computer than it is to provide the more elaborate hardware.

The design of the hardware multiline controller involves detailed consideration of how the software will handle characters transferred from the controller into the computer memory. At first sight, it may appear convenient to allocate separate blocks of memory to each incoming line and have the controller automatically transfer matured characters to the appropriate blocks. However, additional computer time is required when a block becomes full and it is necessary to allocate a new block before the arrival of the next character. Since character arrivals are random, the system software must be designed to cope with the particular case when all blocks become filled, essentially, simultaneously. The re-allocation time for each block must, therefore, be small enough to allow them all to be serviced in this unusual circumstance. This is an undesirably stringent restriction on the programming. In addition, it is usually necessary for the software to examine each character soon after it arrives to determine whether it is a format control character and possibly to check its validity (parity). Excessive time can therefore be wasted in scanning inactive blocks to determine whether any characters have recently arrived, or blocks become filled.

To relieve this software burden, a tumble-table may be used in which incoming characters are not blocked by a line, but are inserted as they mature into a common table, along with their specific line identification number. This table can be considerably longer than one of the line blocks mentioned above, but need not be nearly as long as the sum of these blocks. The software is now only required to process lines that are active, and only one block needs to be reset in real time as it becomes filled. As a further sophistication, an interrupt can easily

reduce system size 7:1 with MicroVersaLOGIC IC Modules



The complete MicroVersaLOGIC line gives you all the ready-made building blocks you need for anything from a register to an entire digital system — with a 7:1 size reduction because of MicroVersaLOGIC's high density IC packaging.

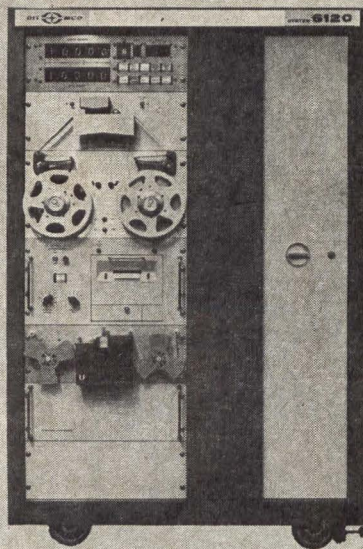
MicroVersaLOGIC also means increased reliability over discrete components, lower power requirements, greatly reduced costs. MicroVersaLOGIC features NAND, NOR logic with wired OR capacity at the collector, operates to 5v. logic levels, has excellent noise rejection of over 1v. There are over 20 basic module types, all meticulously designed and assembled to give you utmost reliability.

Our new MicroVersaLOGIC brochure will show you how easy and economical it is to design digital systems with MicroVersaLOGIC IC Modules. Write or call.



varian data machines
a varian subsidiary

Formerly Decision Control, Inc.
1590 Monrovia Ave., Newport Beach, Calif.
(714) 646-9371 TWX (910) 596-1358



**FASTEST WIRING
SYSTEM ANALYZER
IN THE WEST AND
EAST AND NORTH
AND SOUTH.**

The DIT-MCO System 6120 walks tall in the world of wiring system analyzers. It's a tough, versatile and highly adaptable testing unit that's ready, willing and able to meet today's demand for speed, accuracy and flexibility. Works on the latest fully automatic taped program and printout concept.

**INSULATION TEST
CAPACITY:
2010 PER MINUTE!
CONTINUITY TEST
CAPACITY:
2963 PER MINUTE!**

The DIT-MCO System 6120 has been thoroughly lab and field tested.

Switching Console contains terminal selector and high speed 500-termination Reed relay switching modules that give you a total system capacity of up to 50,000 terminations. Save time, save manpower, save dollars — and — improve both the testing function and the tested product with the DIT-MCO System 6120.

Write for Detailed Specs and Full Information.



DIT-MCO INTERNATIONAL
A DIVISION OF XEBEC CORPORATION

5612 BRIGHTON TERRACE
KANSAS CITY, MISSOURI 64130
TELEPHONE (816) 363-6288
TELEX NUMBER 42-6149

**IT'S NO WONDER APPROXIMATELY 90%
OF ALL MAJOR MANUFACTURERS IN
THE COMPUTER AND AEROSPACE IN-
DUSTRIES ARE SATISFIED USERS OF
DIT-MCO SYSTEMS.**

CIRCLE NO. 28 ON INQUIRY CARD

be provided when the block is partially filled, indicating that resetting is required as soon as conveniently possible.

On output the situation is not quite so critical, since any delay due to software overload does not cause data loss but only a slight reduction in data rate. Simple blocked systems may be used effectively, with block sizes varying from one character upwards. Automatic block chaining, in which each output block contains a pointer to the next block, requires more hardware but does give some reduction in software loading. With multicharacter blocks, the systems designer needs to consider the technique for transmission of partially filled blocks at the end of a message. Should hardware be used to detect the EOT character, or should software complete the block with blanks and then terminate with an EOT? The tradeoffs depend on the specific situation.

Conclusion

The computer communications field, in common with many others, requires the best possible compromise between hardware and software if systems are not to become excessively expensive or exceedingly inefficient. The problem facing the industry is that far too few people are being trained to have a deep understanding of both hardware and software. There are hardware experts who are mystified by the black art of real time programming, and

software experts who wonder vaguely what a ferrite core is, and all too rarely do the twain meet. People who are experts in both areas are urgently needed, not just people with a cursory interest in the area outside their specialty, but those who really understand both. This need, more than any other single obstacle, is delaying the progress of economical and efficient remote computing services which have so much to offer in the reduction of tedium and the extension of man's individual capability.

The Department of Transportation has released a report describing a system of computer storage and retrieval of freight tariff information. The report includes methods for handling tariff features such as routing, accessorial charges, footnotes, rules and regulations. It also identifies how to judge the usefulness and economic efficiency of the computer system as it might be adapted to the individual needs of industrial management. Data storage requirements and possible computer hardware configurations for different classes of users are also discussed. Cost guidelines are presented, based on a comparison of different tariff-related functions as currently performed manually and by computer. The report stems from several years of research performed by the Battelle Memorial Institute, under contract to the Federal government.

No one sells computer bus bars off-the-shelf

...but we come close.

Having pioneered the laminar bus assembly concept for voltage distribution, we've been in on a good deal of the action.

So much so that today, MEKTRON® Laminar Bus Assemblies by Rogers are used by every major computer manufacturer.

Chances are, we have already worked with requirements similar to yours in voltage and current rating, insulation resistance, dissipation factor and capacitance. That means lead time can be substantially reduced. For a scrupulously engineered component — that's as close to off-the-shelf as anybody can come.

Call or write for Mektron data . . . or for help on designing your next bus assembly. We promise an appropriate and prompt response.



ROGERS CORPORATION
ROGERS, CONNECTICUT 06263

Other Mektron products include: flat, flexible cable, circuitry and connective hardware; molded circuits; Mektherm heater circuits.

CIRCLE NO. 29 ON INQUIRY CARD



The Public Health Service is exploring the feasibility of establishing a Center to serve as a clearinghouse for information on hospital automated communication systems. Increasingly hospitals are using computers to speed the exchange of information between individual departments, such as admitting, business office, nursing, pharmacy and others relating to patient care. The Center would gather and analyze the data relevant to this rapidly developing field so Public Health Service consultants will be better prepared to advise hospitals throughout the Nation on their computer applications.

A 6-month study to determine technical and management requirements for the Center is being supported by a \$29,386 research contract executed by the Division of Hospital and Medical Facilities. Herner and Company, consultants in information science, Washington, D. C., will conduct the study.

Computers have been cited as the key to future global conflicts by Dr. Nicholas A. Begovich, a Hughes Aircraft Co. Vice President. Speaking in Washington recently, Dr. Begovich said "any future global conflicts in which electronic command and control systems are used will be won by the nation with the best computer programs and programmers." He pointed out that American industry today is being asked by the military to miniaturize command and control systems, program all tactical defense situations, and automatically detect, clear and track hundreds of targets simultaneously regardless of environment. He emphasized that the key to solving these and other critical problems lies in computer technology — the effective utilization of programs and a new breed of programmer.

Use of computers, now 3,000, by the Federal Government has doubled during the past three years and significant results are evident as a result in all its activities, Comptroller General Elmer B. Staats recently told the Washington Chapter of the National Association of Accountants. GAO will increase its responsibilities in the area of modern information systems if the Senate-passed Legislative Reorganization Act of 1967 is enacted, Staats said. The Senate report on the bill, he added, reflects the concern of Congress that such a modern information system is necessary if Congress is to make informed budgetary decisions.

Staats cited important results of computer use in air safety, health, administration, and space. He predicted further accomplishments in the same and other areas.

National Data Center is still under top consideration by the Bureau of Budget. The question of the ability of such a data center to keep information put into it confidential is being questioned by members of Congress and others. Currently the Bureau of Budget, with other statistical agencies, is attempting to formulate the details of purpose, content, organization and operations of a Federal Statistical Data Center. Particular attention is being given to find ways to insure such a Center does not pose a threat to personal or business privacy. The Bureau of the Budget has told Congress that any proposal for a Center would be presented to Congress for legislative authorization. There is now no target date for advancing a formal proposal. The detailed language of a legislative proposal to insure the Center would not make available to the public or governmental agencies any information about individual persons or businesses has not been developed as yet.

Secretary of State Dean Rusk has warned Congress that if it passes protectionism legislation restricting imports of commodities into the United States "the prospects would be nothing short of appalling." He points out that U. S. import quotas would hurt a number of domestic industries, including computers, by reducing foreign sale opportunities. The U. S. exported computers valued at \$369 million in 1964 — this was 18% of our total domestic output for an industry of 160,000 workers, according to Rusk. Senator Edward W. Brooks (R.-Mass.) has proposed legislation to restrict U. S. imports of electronic components of foreign manufacture.

The National Science Foundation is to support regional computer experiments and has invited a limited number of proposals for cooperative computing experiments. NSF will seek information on the cost and educational value of having educational institutions share computers on a geographical basis. NSF has established an Office of Computing Activities to stimulate new ideas and approaches to computer utilization in the research and educational processes.

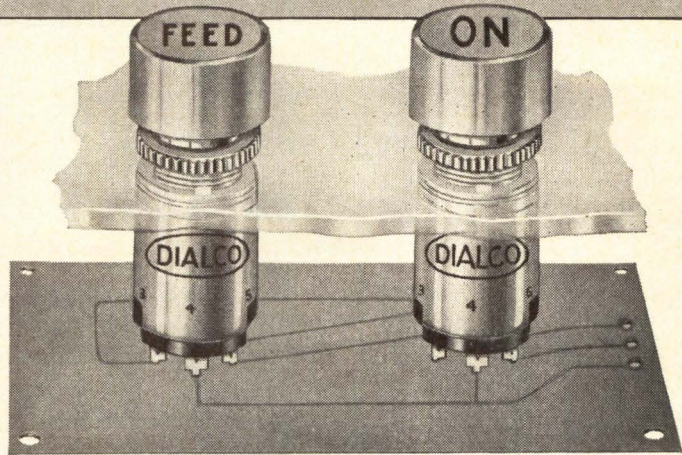
NEW!

REDUCE INSTALLATION COSTS...SAVE TIME...USE ILLUMINATED MOMENTARY ACTION SWITCHES FOR DIRECT CONNECTION TO PC BOARDS!

Switches are of the silent, momentary type. Contact arrangements are: S.P.S.T. normally open or normally closed; S.P.D.T. two circuit (one N.O.; one N.C.). Ratings: 3 amps, 125V AC; 3 amps, 30V DC (resistive load). Button travel is 3/32"; operating forces are: N.O. - 20 ozs. (approx.), N.C. - 10 ozs. (approx.).

The switch is completely enclosed and independent of the light circuit. The light source is the T-1 3/4 incandescent lamp, available in a range of voltages from 1.35 to 28V. Switches are made for single hole (keyed) mounting in panels up to 3/16" thick and mount from back of panel in 1/2" clearance hole. Switches are also available for dry circuits.

Other features: 1/2" or 3/4" interchangeable caps, round or square, rotatable or keyed, in a choice of 7 cap color combinations.



Write for free catalog today!

DIALCO[®]

Foremost Manufacturer of Indicator Lights

DIALIGHT CORPORATION

60 STEWART AVENUE, BROOKLYN, N.Y. 11237 • 212 497-7600



ANOTHER NEW
SWITCH SERIES FROM DIALCO

CIRCLE NO. 30 ON INQUIRY CARD

Much work remains to be done before the securities industry and its customers obtain the full benefits of well planned use of EDP equipment, according to Securities and Exchange Commission Chairman Manuel F. Cohen. In a recent talk in Hartford he emphasized that this work "must proceed at a much faster pace than has heretofore been the case if the securities industry is to maintain the rate of growth that it has achieved in the past two decades." He pointed out that "we are already pushing to the danger point the ability of the Exchange and its members to handle an accelerating volume of trading by antiquated manual methods or a hesitant and limited use of a computer technology and recent communications developments."

Use of new computer-aided photo-interpretation techniques have revealed additional topographic features on Mars. A study of calibrated picture intensities, stored on magnetic tape, used computer enhancement of photographs for reduction of the electronic noise present in each picture, sharpening of detail, changing of contrast to intensify shading and highlights, and a computer-generated picture called a variance plot in which smooth areas are shown in black and rough areas in white. By varying the levels of contrast in reproducing the series of computerized pictures, scientists were able to resolve specific features more clearly. In many cases features not recognized in the original pictures were made visible through these enhancement techniques.

National Commission on New Technological Uses of Copyrighted Works has been approved by the U. S. Senate. The legislation would establish a Commission to study and compile data on the reproduction and use of copyrighted works of authorship in the automatic systems capable of storing, processing, retrieving, and transferring information, and by various forms of machines. The Commission would make recommendations to the President and Congress.

Recent Government contracts:

RADIO CORPORATION OF AMERICA, Washington, D. C., has been awarded a \$1,297,366 contract order for 45 items of electronic data processing equipment. The Defense Electronics Supply Center is the contracting agency.

INTERNATIONAL BUSINESS MACHINES CORP., Dayton, Ohio, has received a \$1,408,833 contract order for 12 items of electronic data processing equipment. The Defense Electronics Supply Center issued the contract order.

INTERNATIONAL TELEPHONE AND TELEGRAPH CORP., Paramus, N. J., has been awarded a \$2,933,848 negotiated cost-plus-award fee contract for programming services for the Fleet Computer Programming Center, Atlantic, tactical data system. The Navy Purchasing Office, Washington, D. C., is awarding the contract. Work will be performed at the Fleet Computer Programming Center, Virginia Beach, Va.

DOCUMENTATION, INC., Bethesda, Md., has received an estimated \$5,563,138 for one year of operation under terms of the incentive fee contract from the National Aeronautics and Space Agency. The company has been operating the Technical Information Facility at College Park, Md., since it was set up in 1962.

THE INTERNATIONAL BUSINESS MACHINES CORP., Federal Systems Div., Gaithersburg, Md., has been selected to negotiate a \$998,000 three-month contract extension for computer programming and engineering support of the Goddard Space Flight Center, Greenbelt, Md.

ARCHITECTURE

for large computer systems

Gerhard L. Hollander
Hollander Associates
Fullerton, California

Large computing capabilities can be achieved through faster uniprocessors, or through configurations of conventional or unconventional computer hardware that can share the load. Any of these approaches can solve most problems. The question is which approach produces the greatest performance per unit cost.

Though initially thought to be limited by circuit speed, the uniprocessor has kept up with most known requirements. Multiprocessors, an aggregation of conventional processors that dynamically share the computing load, are starting to compete effectively now that some of the programming and system-overhead problems are understood. Array computers, a geometrically distributed set of identical processors coordinated by a single instruction stream, are particularly suited for cost reduction by large scale integration. Associative processing, the use of memories in which each word is also a register for basic logical manipulations, allows execution of identical instructions simultaneously in thousands of memory locations; thereby reducing the load on the central processor.

Which problems can be best handled in one or the other configuration, and whether one of these configurations is better for general-purpose environments, is topic for debate. This article provides perspective for the companion articles that advocate four different architectures for economical large computer systems.

Editor's Note: This article, by our new editorial consultant, and the four succeeding companion articles are reprinted, with some additions and modifications, from the AFIPS Conference Proceedings, Volume 30, April 1967. It constitutes the formal part of a debate by leaders in the field of computer architecture which was remarkable for its large and attentive audience and for the spirited informal debate that followed. The articles are published here not only because they are as timely now as when originally presented but also because Computer Design recently discovered a tape recording of the informal debate from which we will publish abstracts in future issues.

Evaluation Criteria

As the computer field reaches maturity, users select their equipment not because of internal structure or features, but by its overall *economy*; i.e., performance per unit cost. Here, *performance* means the computer's ability to do the user's job. *Cost* includes not only the purchase price, but also such associated costs as space, power, operation, maintenance, software, and reliability.

Greater problem complexity stimulates various alternative computer-design approaches; from speeding up conventional processors to using a multiplicity of processors. But if the user is really indifferent to the internal structure provided his job is executed economically, we are confronted with an apparent contradiction: Multiple — and therefore smaller — processors violate the accepted dictum that a larger processor provides more performance per unit cost.² According to Grosch's law,³ manufacturers price equipment to make performance proportional to the square of price; in other words, doubling the price increases the performance four-fold. However, this empirical *pricing* guide stemmed from an era when the manufacturer's only concern was the elasticity of the *total* demand for computers. In a competitive environment, manufacturing cost determines price; and it remains to be seen whether Grosch's law also applies to the *cost* of computers.

In a competitive environment, the user's *economy* becomes the guide of the successful designer. The manufacturing cost of a computer depends on the number and cost of its components. The designer must structure his components so that the fewest and least costly provide the maximum performance. The resultant computer must do the user's job with minimum time expended for overhead or housekeeping operations. Most likely, the components of the most economical computer will have the largest duty factor.¹

TABLE I
SYSTEM-STRUCTURE CHARACTERISTICS

Structure*	Instruction Streams	Data Streams per Instruction Stream	Limitation on Data-Stream Similarity	Level of Work Division	Approximate Cost Division			
					Central Processor	Inter-Connection	Other Execution Elements	
							Total	Each
Uni-Processor	Single	Single	None	None	1.0	0.0	0.0	...
Multi-Processor	Multiple	Single	Minor	Sub-routine	0.0	0.3	0.7	10 ⁻¹
Associative Processor	Single	Multiple	Severe	Boolean	0.6	0.0	0.4	10 ⁻⁴
Processor Array	Single	Multiple	Strong	Macro	0.2	0.1	0.7	10 ⁻²

Competitive System Structures

Over the last two decades, computer economy has grown hundred fold. The primary reason is faster circuitry, which provides more performance at the same cost when the faster circuits are in full production. A computer still faster than the largest economical unit available today could be designed by:

1. Speeding up a single instruction stream
 - a. Faster single primary execution element (Uni-processor)
 - b. Multiple primary execution elements (Array processor)
2. Allowing multiple instruction streams (Multiprocessor).

Uni-Processing. Most past effort has been devoted to speeding up the primary execution element. Faster circuits and components have been cited already. Another approach is faster units, such as speeding the arithmetic element by parallel instead of serial organization and by high-speed carry. Augmenting units, such as memory look-ahead and separate I/O processors, relieve the primary execution element. Finally, a larger primary memory gains time at the expense of storage. All these speed-up techniques have helped make existing conventional uni-processors a hundred times faster during the last decade.

Array Processing. A single instruction stream can be more effective if it can process several data streams simultaneously. For example, a payroll run requires essentially the same operations on the records of hundreds of employees. With an array of a hundred execution elements, the single instruction stream could cause a hundred operations to be performed at the same time.

Two distinct types of array computers have been investigated recently. In one, the associative parallel processor, each execution element contains little more than the exclusive-or function.⁴ Because of its simplicity and low cost, each element can also serve as a storage location; and we might think of all orders being executed in memory (an associative or search memory). A word of such associative memory costs about one order-of-magnitude more than ordinary core memory, but several orders-of-magnitude less than a complete arithmetic unit.

An alternative array approach employs hundreds of processing elements as complex as a small computer.⁵ These elements can execute more complex instructions when stimulated by the primary instruction stream. The processing element's own stored program can be tailored to its specific data stream.

Either form of array processing appears best when the problem itself has geometric properties compatible with the topology of the processing array. When the problem does not have this topological property naturally — for example, inventory or payroll problems — the problem can often be converted to use multiple execution elements effectively.

Array-type processing is inefficient if most processing elements are idle most of the time. In the associative processor, with essentially no decision capability at each processing element, the operations must be identical to the simplest level. The processor arrays, with significant decision-making and logical capability at each execution element, can allow reasonable differences from one execution element to another. However, if most decisions make an element idle, the efficiency will be quite low.

Multiprocessing. The multi-processor computer contains several computers, each capable of executing the job alone.^{6,7} They attack a complex problem by segmenting it into many parts and executing each segment autonomously. This allows dynamic allocation of the program among the *available* processors and provides protection against system failure if one of the processors fails.

Multi-processor-computer task assignments require overhead, either as added hardware or as additional (unproductive) time. Furthermore, if Grosch's law holds also for computer cost, substituting several small processors for a large one starts the trade off in a less favorable performance-per-unit-cost regime.

Comparison of Structures

Table I contrasts key characteristics of the four structures (only pure structures are treated; some structures in the references are hybrids). All but the uni-processor

TABLE II
CONSENSUS OF PROTAGONISTS

Application	Uni Processor		Multi Processor		Associative Processor		Processor Array	
	Ave. Rating	No. of Bests	Ave. Rating	No. of Bests	Ave. Rating	No. of Bests	Ave. Rating	No. of Bests
Open-Shop Scientific	1+	2	2	1	4	0	4-	0
General Commercial	2-	2	2	2	4	0	4-	0
Atomic Research	2-	1	2+	1	3+	0	2+	1
Weather Forecasting	2-	1	2+	1	3+	0	2	2
Pattern Recognition	2+	1	3-	1	3-	1	2+	1
Command & Control	2-	1	2-	2	3+	0	4-	0
On-line Commercial	2-	2	2	2	4	0	4-	0
On-line Scientific	1+	2	2-	2	4	0	4-	0
Info Storage & Retrieval	2-	1	2+	1	2+	2	4-	0

Rating Key:

1. Best
2. Acceptable, depending on the application
3. Marginal, depending on the application
4. No reasonable man would consider

Shaded areas represent consensus that this structure is impractical.

Each companion-paper author rated the merit of each structure for the different applications, each large enough to require approximately 10⁷ executions per second with a conventional processor. The **rating** columns show the average of their ratings. Unless the value is either near 1 or near 4, it probably does not represent a consensus but an average of divergent opinions. The other column in each group shows how many respondents considered this the best structure for the application class.

employ multiple data streams, either as multiple instruction streams with a single data stream, or as single data streams of multiple instruction streams.

Multiple data streams controlled by a single instruction stream must be similar. This restriction is quite severe for the associative processor, because the instruction stream is at the level of Boolean functions. The limitations are strong even for the processor array, where the main instruction stream is closer to a macro-order. While the macro level allows the stored program to adjust each execution element for some data-stream differences, the individual elements must execute the same macro operations or remain idle. For the multi-processor, the running time of the segments should be within one or two orders-of-magnitude, a minor restriction.

The cost-division values between the portions of the system represent an approximate indication of the processing components for hypothetical "typical" systems. In the uni-processor, the entire cost is in the central processor. The multi-processing system has no central processing component, as each processor is one of the execution elements. However, a significant portion of the cost is in the interconnection and the task assignment. These overhead functions, hardware or execution time, represent approximately 30 percent.

For the associative processor, the associative memory usually represents less than half of the system cost. For the processor array of the SOLOMON type, most of the cost is in the execution elements. The cost portion of each processing element illustrates the wide range between uni-processors where the single processing element represents essentially the entire cost, to the associative processors where an element represents on the order of 10⁻⁵ to 10⁻⁴ of the cost.

Efficient use of any unconventional processor calls for new programming approaches. Since during the last

two decades people have been trained to think serial, at least now the programming for the less conventional systems is more difficult until new procedures are developed. Thirty years ago, would it have been more difficult to train people to think parallel instead of serial?

Which Structure Is Best?

No one structure is best for all possible jobs. The controversy revolves around the relative advantages of each architecture for different applications. Even here, definitive answers do not seem to exist.

Each of the companion papers^{4,5,6,8} attempts to show the superiority of its approach for some or many applications. In fact, Amdahl believes the uniprocessor is best for all but a few special-purpose applications. Table II summarizes each protagonist's view of the appropriate application areas for the different computer structures. Their papers state their reasoning. Unfortunately, or fortunately, an "unbiased" chairman cannot inject his own conclusions into a debate. The four authors speak well for themselves.

REFERENCES

1. Hollander, Gerhard L. "Drum Organization for Strobe Addressing." *IRE Transactions on Electronic Computers*. Vol. EC-10, No. 4 (Dec. 1961), p. 722.
2. Knight, Kenneth E. "Changes in Computer Performance." *Datamation*. Vol. 12, No. 9 (September 1966), pp. 40-54.
3. Grosch, H. R. J. "High Speed Arithmetic: The Digital Computer as a Research Tool." *Journal of the Optical Society of America*. Vol. 43, No. 4 (April 1953), p. 310.
4. Fuller, R. H. "Associative Parallel Processing." *AFIPS Conf. Proc.* Vol. 30 (April 1967), pp. 471-75.
5. Slotnick, Daniel L. "Unconventional Systems." *AFIPS Conf. Proc.* Vol. 30 (April 1967), pp. 477-81.
6. West, George P. "The Best Approach to a Large Computing Capability." *AFIPS Conf. Proc.* Vol. 30 (April 1967), pp. 467-69.
7. Hollander, Gerhard L. "Multiprocessor Systems Organization." *IEEE International Convention Record*. Vol. 13, Part 3 (1965), p. 213.
8. Amdahl, Gene M. "Validity of the Single Processor Approach to Achieving Large Scale Computing Capabilities." *AFIPS Conf. Proc.* Vol. 30 (April 1967), pp. 483-85.
9. Gruenberger, Fred. "Are Small, Free-standing Computers Here to Stay?" *Datamation*. Vol. 12, No. 4 (April 1966), pp. 67-68.

Validity of the single processor approach to achieving large scale computing capabilities

Dr. Gene M. Amdahl
IBM Corporation
Sunnyvale, California

For over a decade one faction has contended that organization of a single computer has reached its limits and that truly significant advances can only be made through interconnection of a multiplicity of computers to permit cooperative solution. Various, the proper direction has been identified as general purpose computers with a generalized interconnection of memories, or as specialized computers with geometrically related memory interconnections, controlled by one or more instruction streams.

Demonstration is made of the continued validity of the single processor approach and of the weaknesses of the multiple processor approach in terms of application to real problems and their attendant irregularities.

The arguments presented are based on statistical characteristics of computation on computers over the last decade and upon the operational requirements within problems of physical interest. An additional reference will be one of the most thorough analyses of relative computer capabilities currently published — "Changes in Computer Performance", *Datamation*, September 1966, Professor Kenneth E. Knight, Stanford School of Business Administration.

Parallel Processors

The first characteristic of interest is the fraction of the computational load associated with data management housekeeping. This fraction has been very nearly constant for about ten years, and accounts for 40% of the executed instructions in production runs. In an entirely dedicated special purpose environment this might be reduced by a factor of two, but it is highly improbable that it could be reduced by a factor of three. This overhead appears to be sequential so that it is unlikely to be amenable to parallel processing techniques. Overhead alone would then place an upper limit on throughput of five to seven times the sequential processing rate, even if the housekeeping were done in a separate processor. The non-housekeeping part of the problem could exploit at most a processor of performance three to four times that of the housekeeping processor. A fairly obvious conclusion which can be drawn at this point is that the effort expended on achieving high parallel processing rates is wasted unless it is accompanied by achievements in sequential processing rates of similar magnitude.

Data management housekeeping is not the only problem to plague oversimplified approaches to high speed computation. The physical problems which are of practical interest tend to have rather significant complications. Examples of these complications are as follows: boundaries are likely to be irregular; interiors are likely to be inhomogeneous; computations required may be dependent on the states of the variables at each point;

propagation rates of different physical effects may be quite different; the rate of convergence, or convergence at all, may be strongly dependent on sweeping through the array along different axes on succeeding passes; etc. The effect of each of these complications is very severe on any computer organization based on geometrically related processors in a paralleled processing system. Even the existence of regular rectangular boundaries has the interesting property that for spatial dimension of N there are 3^N different point geometries to be dealt with in a nearest neighbor computation. If the second nearest neighbor were also involved, there would be 5^N different point geometries to contend with. An irregular boundary compounds this problem as does an inhomogeneous interior. Computations which are dependent on the states of variables would require the processing at each point to consume approximately the same computational time as the sum of computations of all physical effects within a large region.

Ideally the computation of the action of the neighboring points upon the point under consideration involves their values at a previous time proportional to the propagation rate. Since the time step is normally kept constant, a faster propagation rate for some effects would imply interactions with more distant points. Finally the fairly common practice of sweeping through the mesh along different axes on succeeding passes poses problems of data management which affects all processors; however, it affects geometrically related processors more severely by requiring transposing all points in storage in addition to the revised input-output scheduling. A realistic assessment of the effect of these irregularities on the actual performance of a parallel processing device, compared to its performance on a simplified and regularized abstraction of the problem, yields a degradation in the vicinity of one-half to one order of magnitude.

Differences or changes in propagation rates may affect the mesh point relationships. To demonstrate the comparative capabilities of different machine organizations at today's state of the art the author has analyzed the relative performance of three approaches, all realized in the same level of componentry. Figure 1 shows a 64-processor unit parallel processor (Curve A), a pipelined vector processor dealing with 8-element vectors (Curve B), and finally a pipelined sequential processor handling one data element per instruction (Curve C). The processors in Curves B and C require about 0.4 as many components as the parallel processor, yet the peak capabilities of all three are nearly identical. The sequential processor's performance falls off least rapidly with reduced problem parallelism because its construction provides a capability to marshal resources on local problem disorder.

An interesting analysis can be made with respect to the number of processors which should be paralleled for the parallel processor organization. The number of pro-

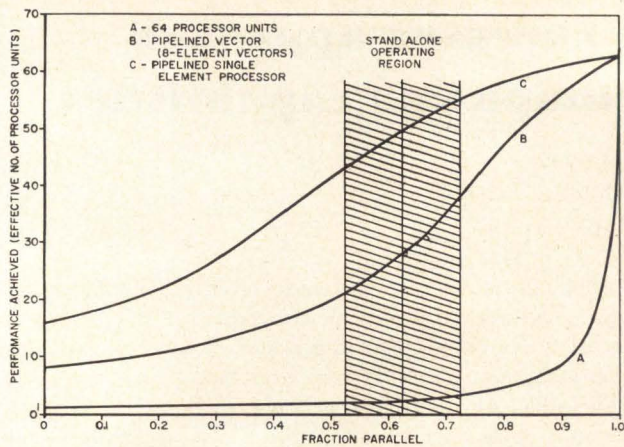


Fig. 1 Comparative capabilities of different machine organizations of today's state of the art.

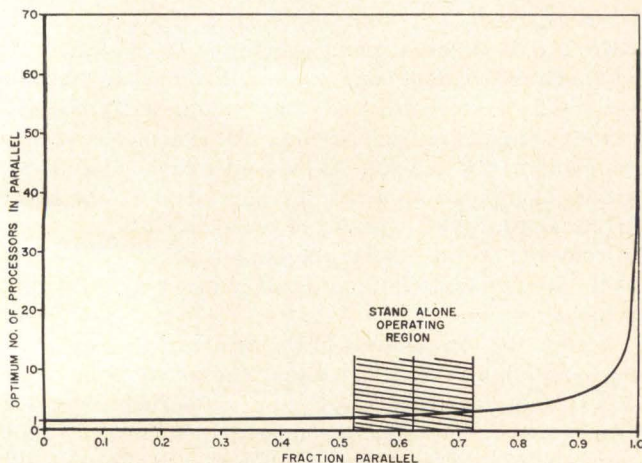


Fig. 2 Number of processors that would execute a workload of a given parallelism with greatest economy.

processors usefully employed is a function of the inherent parallelism of the problem. The cost of the ensemble of course increases with the number of processor units. Assuming a processor to cost about one-fourth as much as a control unit, one can determine the number of processors which would execute a workload of a given parallelism with greatest economy. The resulting curve is shown in Figure 2. A corresponding comparison of the cost effectiveness of a choice of 64 processors compared to having chosen the optimum number of processors is shown in Figure 3. It is readily apparent that an extremely small problem set is best attacked with 64. An additional curve could be drawn comparing the pipelined sequential processor; such a curve would range from 3.0 to 2.5 as the parallelism increased from 0 to 1.

Multiple Processors

The historic performance versus cost of computers has been explored very thoroughly by Professor Knight. The carefully analyzed data he presents reflects not just execution times for arithmetic operations and cost of minimum or recommended configurations. He includes memory capacity effects, input-output overlap experienced, and special functional capabilities. The best statistical fit obtained corresponds to a performance proportional to the square of the cost at any technological level. This result very effectively supports the often invoked "Grosch's Law". Utilizing this analysis, one

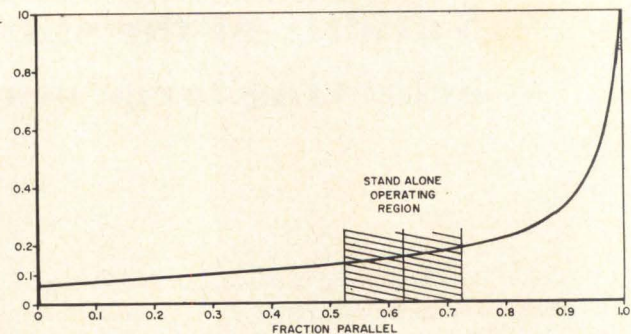


Fig. 3 Cost effectiveness of 64 processors in parallel compared to optimum number.

can argue that if twice the amount of hardware were exploited in a single system, one could expect to obtain four times the performance. The only difficulty is involved in knowing how to exploit this additional hardware. At any point in time it is difficult to foresee how the previous bottlenecks in a sequential computer will be effectively overcome. If it were easy they would not have been left as bottlenecks. It is true by historical example that the successive obstacles have been hurdled to demand that we continue to keep the faith. If alternatively, one decided to improve the performance by putting two processors side by side with shared memory, one would find approximately 2.2 times as much hardware. The additional two tenths in hardware accomplished the crossbar switching for the sharing. The resulting performance achieved would be about 1.8. The latter figure is derived from the assumption of each processor utilizing half of the memories about half of the time. The resulting memory conflicts in the shared system would extend the execution of one of two operations by one quarter of the execution time. The net result is a price performance degradation to 0.8 rather than an improvement to 2.0 for the single larger processor.

Associative Processors

Comparative analysis with associative processors is far more difficult and less obvious. Under certain conditions of regular formats there is a fairly direct approach. Consider an associative processor designed for pattern recognition, in which decisions within individual elements are forwarded to some set of other elements. In the associative processor design the receiving elements would have a set of source addresses which recognize by associative techniques whether or not they were to receive the decision of the currently declaring element. To make a corresponding special purpose non-associative processor one would consider a receiving element and its source addresses as an instruction, with binary decisions maintained in registers. Considering the use of thin film memory, an associative cycle would be longer than a non-destructive read cycle. In such a technology the special purpose non-associative processor can be expected to take about one-fourth as many memory cycles as the associative version and only about one-sixth of the time. These figures were computed on the full recognition task, with somewhat differing ratios in each phase. No blanket claim is intended here, but rather suggests that each requirement should be investigated from both approaches.

The best approach to a large computing capability

George P. West

Systems Development Corporation

Santa Monica, California

The best approach to a large computing capability is to build your own multi-processor system, utilizing the most effective elements available from the leading hardware manufacturers. To understand this approach, it would be useful to describe the type of system which is to be built. It is evident that many of the system characteristics will be prescribed by the application, others will be purely a matter of personal choice. The essential characteristics are few in number and must not be confused with the non-essential characteristics. The remainder of this paper presents a set of do-it-yourself instructions for designing your own multi-processor system which stresses the essential characteristics. The intent being that the reader can follow through these instructions and design his own system for his own particular application. In this way, each reader can have a specific system in mind which he can evaluate critically. Although there would be individual differences in the systems under consideration by different individuals, the essential characteristics would be the same, and discussion would then tend to center about these essential features. The paper concludes with a summary in which the design approach is reviewed in an attempt to emphasize the utility of the approach.

The first step in designing the multi-processor system is to select a computer which is to be the basic module of computational capability. Select one of the many word-oriented full-word computers with a word length of at least 24 bits. Select a computer with multiple memory modules; one with some capability for a shared use of memory. Make the selection based on cost/effectiveness. Select the computer because it gives the most computer power for the money. Don't worry about channel capacity, total memory capacity, etc. These characteristics will be considered later. The criteria for evaluation of competing computers may be simple or complex. If you have no other criterion, you can follow the crowd. Some of the best performing computers in the past have also been the best sellers.

The next step is to select a small character-oriented (byte) computer with good channel characteristics to serve as the I/O, or peripheral, controller and processor. Select the computer so that the large computer's word length is a multiple of the small computer's word length. This is relatively easy for a character-oriented small machine. We will decide how many of each type of module to provide later.

Now, since we have selected a small general-purpose computer as the I/O controller, we will shop for peripherals that have a minimum of control logic in each unit. Simply look for good clean electro-mechanical design and select each peripheral from the most appropriate vendor. It is very unlikely that any one vendor can supply more than one or two types of modules for the system.

Estimate the total system computational capacity, based upon the particular requirements of your application; then select the number of large processors based upon this computational load. Do not include extra capacity for executive functions. The number of memory modules to be provided is based upon the performance you wish to provide to the different classes of users. In general, two memory modules per processor will provide overlapped swap and computer capabilities for a large class of applications. A relatively simple computation will provide estimates of the system performance with different numbers of extra (swap) memory modules. The computation will reflect your own mix of problems, the grade of service you hope to give each class of user, and the expected loading for each class of user. These performance estimates can be as simple as statistical estimates derived from drawing samples from a set of hats with the correct mix of alternatives in each hat, or as sophisticated as detailed simulations. Results derived from published queueing tables should provide sufficient accuracy for determination of the size of the system memory. Next, determine the number of peripherals required for your application, and from this estimate how many small peripheral processors will be required to support your I/O functions. In addition, these small processors must also perform some executive functions, which should require no more than about $\frac{3}{4}$ of the capacity of one of the small computers. This estimate depends upon your own particular application as well as upon the amount of I/O supported. If there are several I/O processors, the executive can be interleaved with I/O idle time so that little extra capacity is required. If your I/O requires most of one small computer's capacity, the executive function might necessitate a separate processor.

The system components must now be interconnected by designing a high-speed communications network so that the memory modules are all accessible to all computers. This network may take the form of a multiple-path, high-speed switch between the processors and the memory modules. It should include special logic to facilitate the executive function. In particular, it should provide hardware for translation of symbolic memory addresses into actual cross-point locations on the switch. It should include hardware to facilitate queueing of processor assignments and should provide for interrupt routing to the appropriate processor.

In addition, a low-speed network should be provided for connecting the peripheral units to the I/O processors. This network might take the form of a multiple-path relay switch. It requires only very simple control logic since it will be controlled by the I/O processors, which execute only I/O and executive programs. Peripheral reconfiguration will seldom occur. I/O functions would normally be grouped, and assigned in groups to

each of the I/O processors. In addition to the assigned I/O functions, any of the I/O processors could be preempted to perform an executive function, such as swapping a program segment in core with one on the backup storage (probably drum or disk). This low-speed network should be required only if graceful degradation is desired.

The final step is to write the executive program and I/O programs for the small I/O processor.

The full-word processors are to be used only for execution of object programs. In order to do this, we must consider the type of object programs which the users of the system will provide. Let us, therefore, define certain aspects of the object programs which are required by this system. The entire computational task, from initial input to final output, in support of a given user of the system is defined as a job. When each task is initiated, it is assigned a sequential job number by the system. If a user attempts to initialize a task which is already in execution in the system, the job number will permit the system to distinguish each use as a separate task. The job number is utilized to assure privacy between users, in that different jobs are not permitted to interact. Communication between jobs is permitted through use of system tables specifically designed for common use by two or more jobs. The system I/O routines also permit shared use of a peripheral storage medium, such as magnetic tape or disk packs, for communication between jobs. Each job is to be broken down into threads of computation. The maximum length of each thread is set by the core limitations of the memory module and the maximum execution time imposed by the executive system, so that, if the time limitation is exceeded, the job may be temporarily swapped out of core.

Threads of code are linked by a macro instruction CUT to X which initiates subsequent threads within the job. The system does not utilize re-entrant code. That is, only one processor will execute a thread of code at a time. System tables and subroutines are replicated in the environments of different threads of code. When a large computer and a memory module are associated in computation, there will be very few memory cycles available for other uses without slowing down the computations. For this reason, system tables can be designated as guaranteed, in which cases the tables will be restored to the system data base when the task is completed, thereby updating automatically the contents of the table in the system data base. System macros provided permit the program to designate parallel threads which could be executed concurrently. The programmer may use recursive coding techniques so that parallel sections of code may be nested. The executive system which includes both hardware and software, does not recognize a macro instruction for automatically synchronizing the tying back of parallel paths. This book-keeping must be provided in the object code itself.

There is no limitation to the user of the system if the synchronizing code is generated by the compiler rather than by requiring the executive program to effect the synchronization. By limiting the executive functions to essentials, the basic system approach may be more easily understood. For this discussion, the non-essential software features, such as the compiler and diagnostic aids are not considered part of the system. Without carefully

defining these non-essential software features, there would be a great deal of uncertainty as to the overall cost of the software system.

There are three system macros provided for programmer identification of parallel threads of computation. They are:

- Cut — Enter a memory assignment in the queue waiting for a full-word processor to become available.
- Wait — Release full-word processor for a new assignment, but retain this thread of computation and its environment (subroutines, tables, etc.) in core, if at all possible.
- Release — Release full-word processor for a new assignment and release the program thread so that guaranteed data items can be updated in the system data base, and a new program thread can be loaded by the I/O processors.

In addition to these system macros, there are three system queues: one for the full-word processors and the other two for the small I/O processors. The queues are:

- Full-Word Processor Queue — Computational threads which are loaded and ready for execution.
- Executive Queue — Calls for executive functions, primarily swapping of program threads between drum (or disk) and core.
- I/O Queue — Calls for I/O. This includes routine loading of program threads upon release of a memory module.

Both I/O and executive calls are handled by the small I/O processors. However, the executive calls take precedence over the I/O calls. These queues would be implemented in the high-speed communications network so that, under normal operating conditions, all processors would simply accept an assignment from the queue and proceed as far as possible with that assignment before accepting the next assignment from the queue. Priority logic complicates this simple mode of operation only by use of the interrupt feature to preempt certain computational assignments. The interrupt releases the processor and automatically inserts a cut into the appropriate queue to reinitiate the interrupted task at a later time.

With this design philosophy, the executive and I/O functions can be developed for the small I/O processors. The system design is now complete.

Without specific applications in mind, cost estimates would be meaningless. The system has been described in such a way as to identify essential functions while simplifying interface considerations so that each element of the system may be costed independently. Having completed the design for your particular application, you should now be able to estimate the total system cost. For a large class of applications, this approach provides the best way of attaining large computational capability.

The system outlined has several interesting characteristics.

1. It provides a high-performance system since we have delineated specific capabilities, such as arithmetic, memory, and I/O, and optimized each independently from a cost/effectiveness point of view.
2. System overhead time is minimal since the central computers perform only job computations. The executive time is confined to a partial use of the character-

oriented I/O processors.

3. System overhead hardware costs consisting of the high- and low-speed interconnection networks are clearly delineated.

I/O and executive software development costs contribute to system overhead. If more manufacturers followed the practice of providing separate cost for hardware and software, a portion of the software costs would be offset by the hidden cost of whatever software operating system the manufacturer provided with his hardware. However, by applying currently emerging management techniques to software development, the system software can be produced at a lower cost.

Let us summarize by attempting to review the rationale

behind this particular design philosophy. The use of peripherals with minimal control logic selected from many vendors will provide the least expensive user interface if the control functions stripped from the peripherals can be supplied at the same cost by the data system. The use of character-oriented small computers instead of special I/O controllers provides an improved level of support to the peripherals and their users at a cost lower than that of special-purpose controllers. The user's arithmetic support is provided by selecting the most economical word-oriented computer for that task. The central question then is whether the high-speed switch and its associated queues simplify the executive functions sufficiently to warrant the extra hardware costs.

Associative parallel processing

R. H. Fuller

General Precision, Inc.

Glendale, California

Several previous investigations¹⁻⁵ have shown associative processors to have utility in solution of problems which allow the same operation to be performed simultaneously over many elements of a data set. Examples of such problems include picture processing, matrix manipulation, signal correlation, ELINT data processing and information retrieval. It is the purpose of this paper to contrast the efficiency of solution of such problems on an associative parallel processor to efficiencies obtained using other computer organizations described in this session. Efficiency is measured as solution rate per unit cost.

The associative parallel processor (APP)⁵ is an array computer exhibiting parallelism of instruction execution similar to that obtained in SOLOMON type machines. It differs from SOLOMON machines in having much less storage (e.g., a single associative memory word) dedicated to each array element. Logic hardware at each array element is minimized by use of a novel computing technique termed Sequential State Transformation. By this technique, data stored within an associative memory having a multiwrite capability may be transformed according to any Boolean function of stored and external variables.

Cell cost for APP is two to three orders of magnitude less than for a SOLOMON type cell. Instruction execution times for APP cells are longer than for SOLOMON cells by one to four orders of magnitude, dependent on instruction complexity. An APP should be more efficient than SOLOMON type machines in applications having small cell memory requirements and simple data manipulation at each cell. Such applications include picture processing, information retrieval, signal correlation and simple matrix manipulations (e.g., solution of assignment matrices). Solutions of complex field problems, particularly when variable

ranges dictate floating point number representation, are not normally efficient on APP, even though these problems allow parallel computation requisite to efficient use of an array computer. Problem solution time for an APP can only approach that of a SOLOMON array if the APP contains, and may effectively use, many more cells than the SOLOMON array. An APP would typically contain several thousand cells as opposed to several hundred for a SOLOMON array.

In regard to the generality of the various processors discussed in this session, the conventional uni-processor employs a single instruction stream operating on a single data stream and is thus uniformly effective on all problems capable of digital solution. An aggregate of conventional uni-processors employs multiple independent instruction streams, each operating on a single data stream. This organization is effective whenever a problem can be partitioned into several subproblems, each of which allows of independent solution. An aggregate of uni-processors is less general than a single uni-processor in that problems which do not allow partitioning do not effectively utilize the machine.

An array processor employs a single instruction stream operating simultaneously on many data streams. This mode of operation can be achieved with an aggregate of conventional uni-processors by supplying the same instruction sequence to each uni-processor. An array processor is thus less general in application than an aggregate of uni-processors.

Among array processors, an APP is further restricted in application than a SOLOMON type processor, in that floating point arithmetic operations are not available within APP. An APP thus has restricted utility in some scientific computations for which a SOLOMON machine is well suited.

It is felt that within its useful range of application, the efficiency of APP exceeds that of other organizations discussed in this session. To illustrate this point, we shall, in the following section, review the organization of APP and discuss its utility in picture processing, a task to which the APP is well suited.

Processor Organization and Command Set

To illustrate the concept of sequential-state-transformation, consider an associate memory which stores two operands, A_i and B_i , in each work of memory. We desire to add operand A_i to operand B_i simultaneously in some subset of these words. Processing is serial by bit, and parallel by word, starting at the least significant bit of each field. Each word has an auxiliary storage bit, C_i stored within the memory array. Bits within operand field A are designated A_{ij} ($j = 1, 2, \dots, N$), where N is the field length. Bits in field B_i are similarly designated. The truth table defining the addition is as follows:

State number	Present state			Next state	
	A_{ij}	B_{ij}	C_i	B_{ij}	C_i
1	0	0	0	0	0
2	0	0	1	0	1
3	0	1	0	1	0
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	1	1
7	1	1	0	0	1
8	1	1	1	1	1

Note that variables B_{ij} and C_i differ in their present and next states only in states numbered 2, 4, 5, 7. The search and multiwrite operations may be used to perform the addition of all number pairs, starting at the least significant bit, as follows:

1. Search words having $A_{ij} = 1$, $B_{ij} = 1$ and $C_i = 0$. For these words, multiwrite $B_{ij} = 0$, $C_i = 1$.
2. Search words having $A_{ij} = 0$, $B_{ij} = 0$ and $C_i = 1$. For these words, multiwrite $B_{ij} = 1$ and $C_i = 0$.
3. Search words having $A_{ij} = 0$, $B_{ij} = 1$ and $C_i = 1$. For these words, multiwrite $B_{ij} = 0$.
4. Search words having $A_{ij} = 1$, $B_{ij} = 0$ and $C_i = 0$. For these words, multiwrite $B_{ij} = 1$.

Steps (1) through (4) are repeated at each bit of the operands. Within each bit time, processing is sequential by state over present states which differ from the next state in one or more variables. All words in a given present state are transformed simultaneously to the desired next state.

Sequential-state-transformation, used to perform the above word-parallel, bit-serial addition, is evidently a very general mode of associative processing. It allows transformation of memory contents according to any Boolean function of stored and external variables. It makes full use of comparison logic, implemented at the bit level within an associative array, and thereby simplifies logic required at the word level.

In the following we describe the organization and command set for a processor using the sequential-state-transformation mode of associative processing.

Elements of an associative processor are shown in Figure 1. The format for associative commands is shown in Figure 2. Each associative command effects a primitive transformation of state variables as discussed above. The left-most bit identifies the command

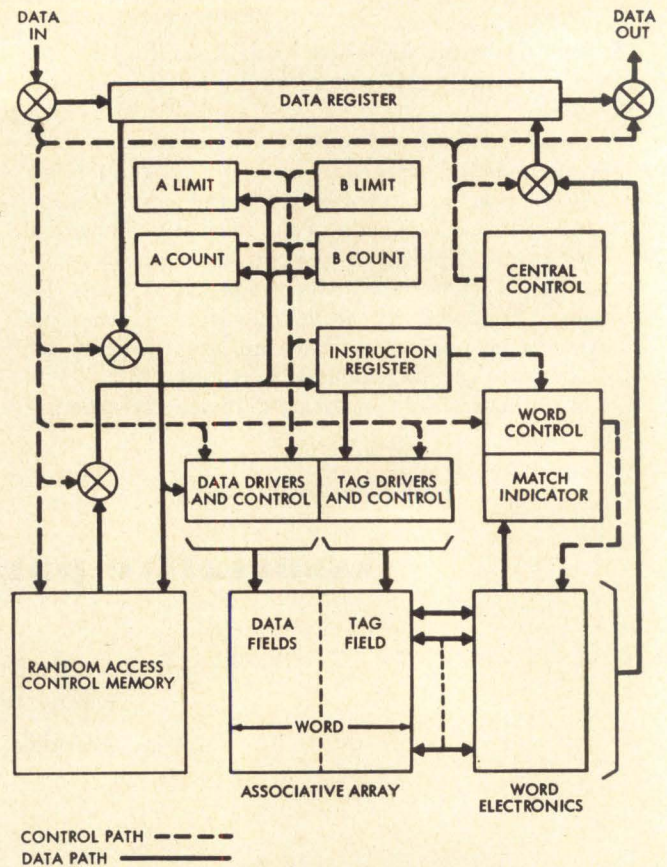


Figure 1—Structure of the associative parallel processors.

as associative. The two adjacent bits define the initial state of match flip-flops in word logic units (i.e., the detector plate). Other bits define search and rewrite criteria for the A field, the B field, and for each of four tag bits. The right-most bit controls rewrite into matching words or their next lower neighbors. Functions of these bits are described in Figure 2.

To illustrate the utility of this command, consider the task of searching the associative memory for words matching the data register over a field having its upper limit stored in the A limit register and its lower limit stored in the A counter. Matching words are to be tagged in tag bit 1.

The following command accomplishes the desired tasks:

1 E_{s1} S L D W I S — — W — S O W
 A control B control Tag 1

The following routine loads data into each word in the associative array. The word field to be written is again defined by contents of the A counter and the A limit register:

1. Set the match flip flop for word 0 to "1."
- 1 N S L D W S — — — — S — W N
- 1 N S L D W S — — — — S — W L
 A Control B Control Tag 1
4. If no match, exit: otherwise go to (3).

Instruction (2) writes into word 0; instruction (3) writes sequentially into each remaining associative word.

Nonassociative commands are provided to load the A and B counters and limit registers, to branch from linear instruction sequencing either unconditionally or when specified conditions are met, and to input or output data.

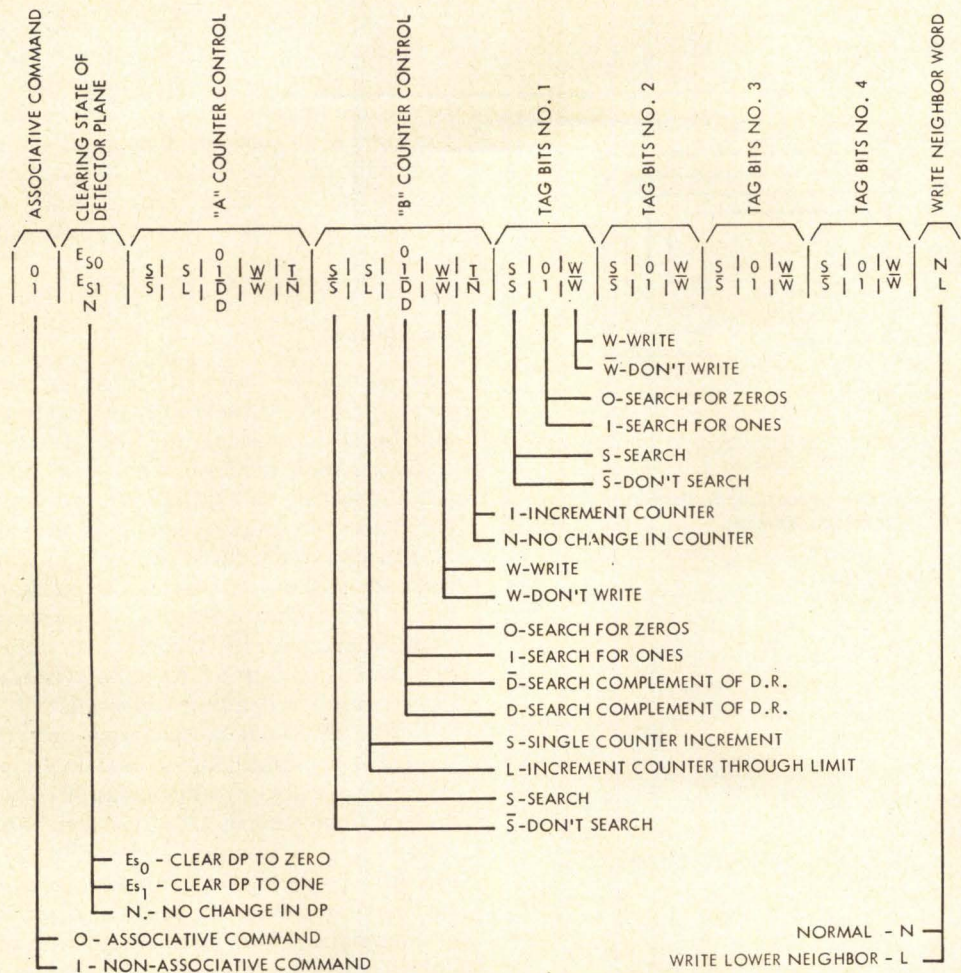


Figure 2—Format for associative command.

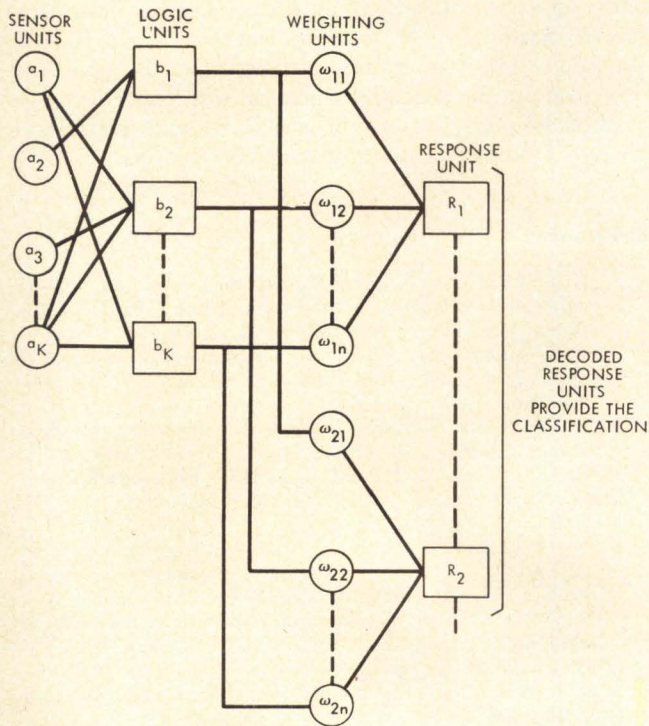


Figure 3—Analog model of pattern recognition system.

Associative Pattern Processing

The parallel processing capability of an associative processor is well suited to the tasks of abstracting pattern properties and of pattern classification by linear threshold techniques.⁶⁻⁸ Threshold pattern recognition devices execute a given operation independently over many data sets, and thus allow the parallelism necessary for efficient associative processing. Associative processing affords the accuracy of digital number representation, and is thus unlimited in fan-in and dynamic range of weights. Weights are simply altered by changing memory contents. Wiring and components are regular and are thus amenable to low-cost, batch-fabrication techniques. The set of measured pattern properties is changeable by changing memory contents, rather than by rewiring as for analog units. Adaptation is thus possible in measured properties as well as in classification.

Figure 3 represents the model of the pattern recognition system to be realized. Binary valued sensor outputs are summed, with weights ± 1 , into some or all of the thresholding logic units. A threshold level is established for each logic unit. If the sum of binary weighted inputs exceeds the threshold, the unit becomes active and its output is "one"; otherwise the output is "zero." Each logic unit has a weighted connection to some or all of the response units. Weights of active

logic units are summed and thresholded at each response unit. A pattern is classified according to the set of activated response units.

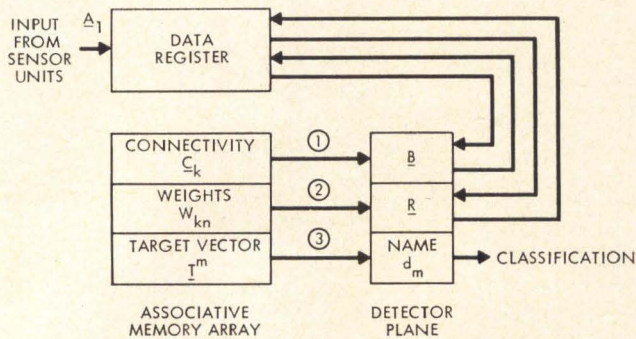


Figure 4—Associative parallel processor realization of pattern recognition system.

To realize this model, the associative memory is organized into three sections containing, respectively, a connectivity matrix defining connections between sensors and logic units; the system of weights associated with inputs to response units, and the target vectors associated with patterns to be recognized. The general organization of the associative memory is shown in Figure 4. Processing takes place as follows: In Phase (1), the set of logic units activated by the input pattern is determined, using the input pattern and the stored connectivity matrix. Logic unit outputs are formed in the detector plane. In Phase (2), the inputs to the response units are calculated, using logic unit outputs and the weights stored in the second sector of the associative memory. This yields the response unit outputs in the detector plane. In Phase (3), the response unit outputs are compared with the target vectors stored in the third sector associative memory, and the pattern classification is determined.

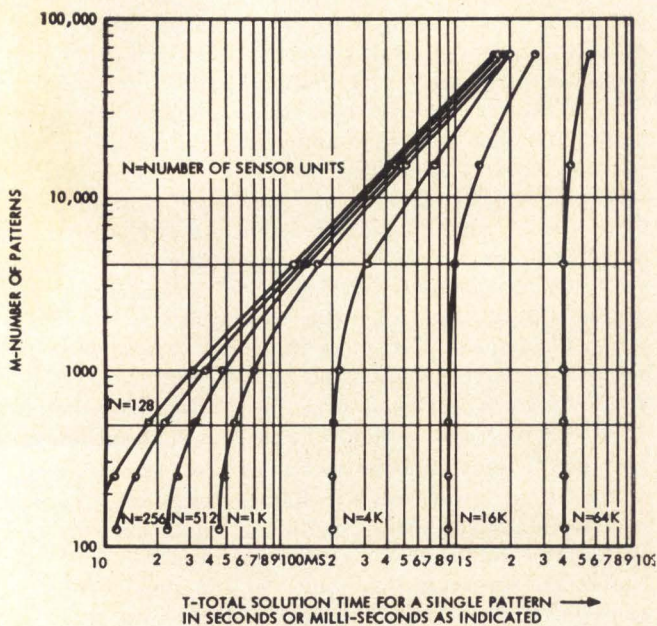


Figure 5—Time for associative classification of a single pattern as a function of the number of patterns and sensors for the W/C data organization.

Figure 5 illustrates pattern recognition times for an associative processor having an execution time for associative commands of 0.8 microseconds. Here, "N" represents the number of sensor units at the input and "M" the number of patterns distinguishable by the processor. The APP can classify an input pattern employing 400 sensors and 512 logic units in approximately 3 milliseconds. Some 2000 words of associative storage are required.

Conclusion

The associative parallel processor, described in this paper, achieves considerable generality with simple word and bit logic through the use of the sequential-state-transformation mode of associative processing. An important feature of the parallel processor, when used as a pattern recognition device, is the ability to modify its functional structure, through alteration of memory contents, without change in its periodic physical structure. This adaptive feature has importance in applications where patterns change with time, or where the processor is used as a prototype of subsequent machines having fixed recognition capabilities.

Linear threshold pattern classifiers of the type here presented are beginning to find many applications. To date, these types of pattern classifiers have been studied and/or implemented for character recognition, photo-interpretation, weather forecasting by cloud pattern recognition, speech recognition, adaptive control systems and more recently, for medical diagnosis from cardiographic data. Other possible applications include terminal guidance for missiles and space vehicles and bomb damage assessment.

In addition to the pattern recognition task herein described, the APP has also been applied to the tasks of job shop scheduling, optimum commodity routing and processing electromagnetic intelligence (ELINT) data. In each instance significant speed gains have been shown possible over conventional sequential digital computers. It is interesting to note that the processor described in the second section of this paper may be applied to this variety of tasks without significant changes in organization or command structure.

References

- 1 G. ESTRIN and R. H. FULLER *Algorithms for content-addressable memory organizations* Proc. Pacific Computer Conference pp. 118-130 March 1963
- 2 Ibid. *Some applications for content-addressable memories* Proc. Fall Joint Computer Conference pp. 495-508 Nov. 1963
- 3 P. M. DAVIES *Design of an associative computer* Proc. Pacific Computer Conference pp. 109-117 Mar. 1963
- 4 R. G. EWING and P. M. DAVIES *An associative processor* Proc. Fall Joint Computer Conference pp. 147-158 1964
- 5 R. H. FULLER and R. M. BIRD *An associative parallel processor with application to picture processing* Proc. Fall Joint Computer Conference Nov. 1965
- 6 R. WIDROW et al *Practical applications for adaptive data processing systems* 1963 WESCON Aug. 1963
- 7 C. H. MAY *Adaptive threshold logic* Rept. SEL 63-027 (TR 1557-1) Stanford Electronics Lab, Stanford, Calif. Apr. 1963
- 8 G. NAGY *System and circuit designs for the tobermory perceptron* OTS AD 604 450 Sept. 1963

Unconventional Systems

Daniel L. Slotnick

Department of Computer Sciences

University of Illinois

Background Observations

For the bulk of the past decade, the computer manufacturer has maintained the "party line" that their successive models of high-end machines possessed all the performance that would be required for the foreseeable future. (This "party line" alternated with abortive attempts to, in fact, build high performance, compatible extensions of the product line which turned out to be neither high performance nor compatible.) While it appears to be true that currently available equipment will for a while continue to be adequate to permit plumbing supply houses to do inventory control, it has always been outrageously false that this equipment comes even close to meeting our scientific or military needs. In these areas, we have witnessed the oft noted paradox of technological advances spurring scientific needs in such a fashion that the disparity between what is needed and what is available continues to grow. In the case at hand, this is no paradox at all in that it is only now that we can realistically envision computers of sufficient speed and capability to make it possible to start using them to solve problems with a non-trivial intellectual content.

Two related sequences of events have in very recent years made it no longer necessary to apologize for grown men to be concerned with producing computing machines of vastly greater capability. These are the consequential gains made by a technology (no thanks whatever to the manufacturer) that was not obliging enough to stand still and secondly that we have the possibility of performing for the first time with the latest generation of equipment, calculations that couple closely to the mental and physical processes of scientific advancements.

Current Status Review

A startling result of the past decade of progress in switching elements is the number of such elements which can be employed in a system of given reliability. For example: A system which contains 10 to 20 thousand vacuum tubes achieved mean-time between failures of at most several tens of hours. Comparable or even somewhat greater mean-time between failures are achieved today by systems with upwards of 10^6 conventional transistors. Within the next five years with the coming large scale integration, this number should go to between 10^8 and 10^9 discrete transistor equivalents.

Now, granting the assumption that we will in the foreseeable future be limited by computer capacity in a broad spectrum of areas, it is legitimate to ask that organizational concept be evolved which can utilize a greater number of components to achieve at least proportionally greater performance. It is an important

practical aside to note that during the same interval of time the cost of a small signal switching element has gone down to an extent permitting the employment of the maximum number which in non-redundant designs yield a reliable system.

Another important factor affecting our approach to computer design is the growing trend to employ design mechanization. Although this field is still very young it has already advanced sufficiently for us to forecast confidently that reduced development costs and lead times should continue to make successively bolder progress tolerable. I am by no means suggesting that computers of vastly greater power will be designed more cheaply and more quickly than their predecessors, but that as a percentage of our gross national product, these costs will be tolerable in their relative magnitude and continue to yield the nation a reasonable return.

The manufacturer continues to bombard our (mercifully) somewhat desensitized ears with the problem of software conversion in an effort to perpetuate hardware that when looked at even ten years from now, will have value only to the historian or antique collector. (In the case of recent compatible families this argument has changed somewhat in that the manufacturer finds that offering even paltry improvements in equipment eliminates compatibility. The new argument is that only the manufacturer can produce software in a timely, economical fashion because of his ability to pool requirements from different customers. The supreme irony of this point of view is already legion.) The value of the machine software investment (notice I said value not cost) has been greatly exaggerated for the same reason by the manufacturer. In particular, the sophisticated user (i.e., the academic and military eggheads with their huge problems) have traditionally been required to program their problems in a low level language. The argument that we must make no further progress in computer organization — a field that is no more than 20 years old — in order to maintain a fictitious compatibility with Baggage's computer and its electronic progeny is arrogant and patently absurd.

In seeking up-to-date criteria for judging the efficiency of organizational concept the following are obviously suggested:

1. That they make efficient use of high-level semiconductor components (i.e., equivalent to from several hundred to several thousand discrete elements), and
2. That the designs keep a maximum number of memory amplifiers working, i.e., maintain maximal traffic on memory distribution busses both productively and without chaos.

A third criterion is the extent to which a given design can employ design mechanization in its implementation. An extension of this last criterion threatens

The Memorex 630 Series Disc Drive For Your System

2311 COMPATIBILITY

The Memorex 630 Series Disc Drive is fully compatible with IBM 2311 disc drive units. It will read/write Memorex Mark I or IBM 1316 disc packs. A separate read/write head with tunnel erase is provided for each of the ten recording surfaces to assure you of total interchangeability. We can also supply the 630 Series Disc Drive with the exact interface *for your system*.

PERFORMANCE

Total performance of the Memorex 630 Series Disc Drive is unmatched by any other competitive machine. The head load/unload is new—for higher data throughput. The positioner is new—for better access time—the best in the industry. These and other Memorex designed performance features guarantee competitive advantages *for your system*.

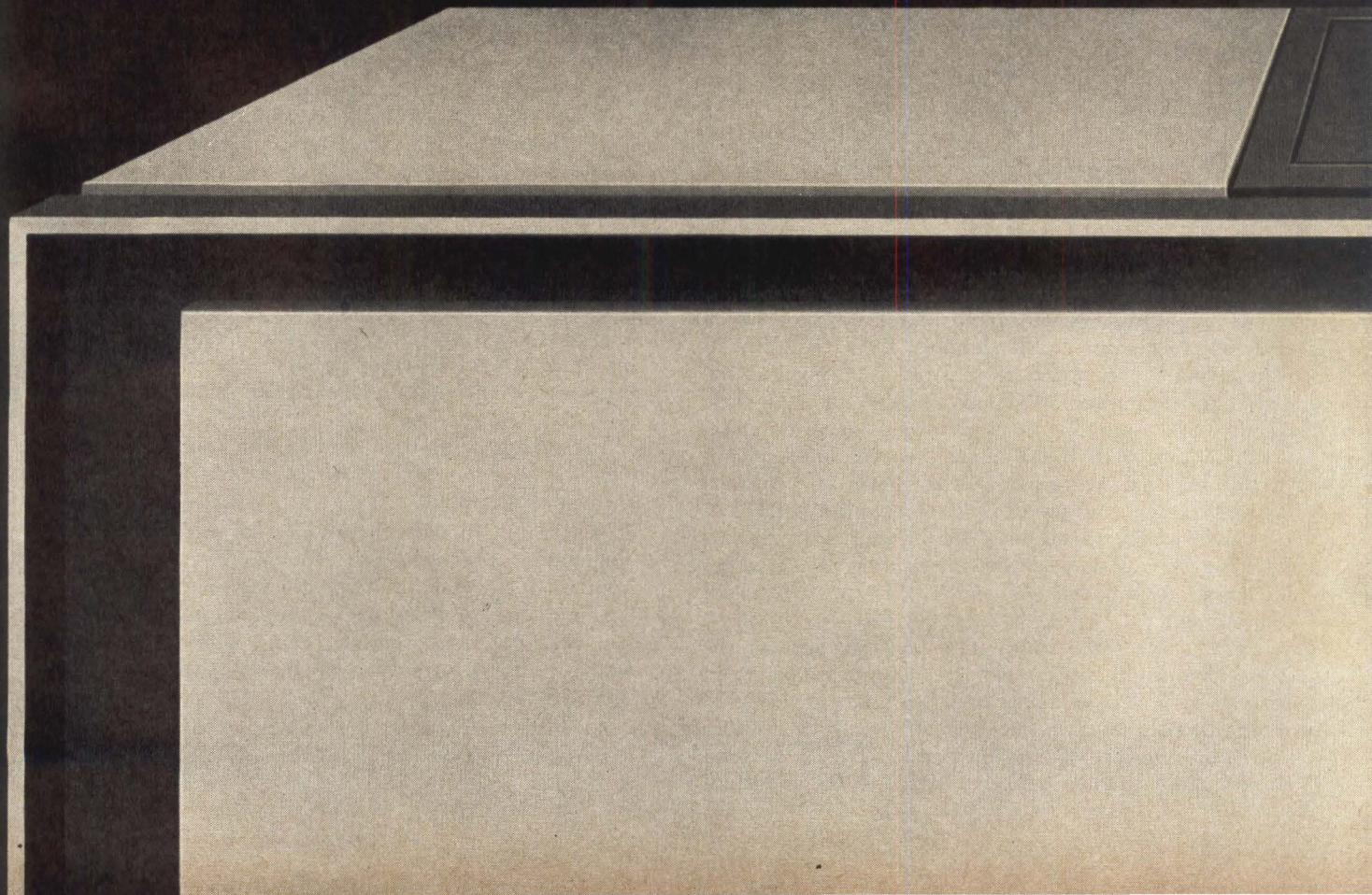
RELIABILITY

The Memorex 630 Series Disc Drive offers superior reliability. Over 75,000 head load/unload operations without error verify reliability and repeatability. The advanced positioning mechanism has fifty fewer moving parts than competitive devices. These and other technical advances guarantee a truly dependable disc drive *for your system*.

For further information about the Memorex 630 Series Disc Drive for your system, contact Peripheral Systems Corporation, 292 Commercial Street, Sunnyvale, California 94086.

Peripheral Systems Corporation

A Subsidiary of Memorex Corporation



MEMOREX

SERIES 630

at some time in the future to explode all our conceptions about computing machines. It is already possible to conceive a machine which will automatically design and fabricate special purpose computers on the basis of a set of instructions not differing greatly from a current machine program. In other words, the filing cabinets full of punched cards would be replaced by filing cabinets full of special purpose computers. It is my current plan to pursue such machines when the current machine we are building at the University of Illinois (ILLIAC IV) is successfully operating. I am greatly heartened that some of the same people who five years ago reacted to the idea of ILLIAC IV with smug incredulity are reacting now in the very same way to this idea.

Some Approaches To Large Computing Capability

To return to 1967: What are the approaches currently being explored to achieve greater speed? The manufacturer has a simple answer. If a problem requires a 1000 times the power of computer "X," use a 1000 computer "X's." Of course, this ignores the fact that attempts to achieve cooperative interactions between general purpose computers using clip leads and other strong medicine have in the past yielded lamentable and sometimes laughable results. This approach we can dismiss out of hand if for no other reason than that it is ponderously inelegant; but there is another reason — it doesn't work.

Another approach is to simply state that the conventionally organized general purpose computer will continue to improve so as to keep pace with requirements. This argument ignores the fact that the requirements which are not generated by the existence of a given computer at a given place, for example those motivated by scientific or military problems where the outside world determines the problems, have already produced requirements greatly in excess of current capabilities. Secondly, as has been pointed out now for many years, improvements in general purpose machines are not open-ended because of speed of light and memory access and buss distribution limitations.

Next, in the current set of ideas to achieve high performance are a number of concepts which achieve their very high performance partially by sacrificing some generality of purpose. I must remark here about the erroneous impression created by referring to our current machines by the name "general purpose" computer. This name makes the false implication that they are uniformly good (or poor) at all things. Moreover, the only high performance computer currently in operation differs markedly in its organization from its predecessors and moreover experience with this machine seems to indicate that the variation in its efficiency of application from problem to problem is quite considerable.

The "pipe line" systems to be available in the next several years offer another order of magnitude of performance over the fastest machine currently available.

These "pipe line" machines achieve speed through the same basic mechanism as parallel machines, i.e., applying a single instruction to a considerable block of data. They, as a consequence, suffer from the same general disadvantage, namely: If the problem does not permit the data to be treated in blocks, their

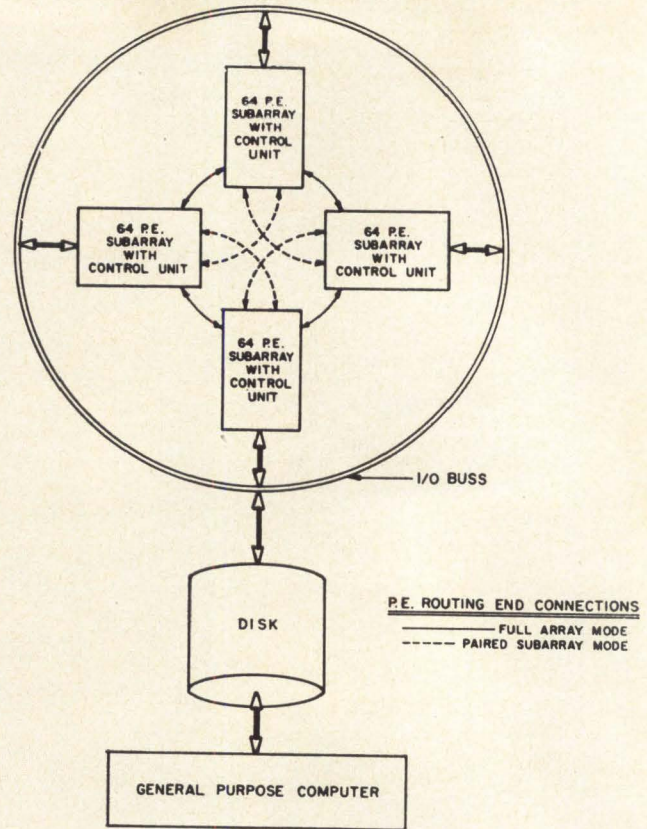


Figure 1—ILLIAC IV General Organization.

efficiency degrades. Most problems examined, however, that require very high performance do seem to possess this property of permitting data to be handled in blocks to a remarkable degree although this is not always obvious at first glance. The "pipe line" approach is novel and merits our closest attention. It is being pursued by the major manufacturers in the field.

The approach that I am personally pursuing is the parallel approach. It is the only current approach which is open-ended. The same remark holds for both parallel and "pipe line" systems, namely: Its generality is not fully established.

I will furnish a brief overall description of the system here and refer you for details to a separate session at this conference dealing exclusively with the ILLIAC IV hardware, software and applications.

The ILLIAC IV System

Simply to illustrate the capacity which current technology permits in a computing system, I will give a brief description of the ILLIAC IV system being developed jointly by the University of Illinois and industry.

Figure 1 illustrates the general arrangement of the ILLIAC IV system, centered on four subarrays, each containing 64 processing elements under the direct control of a subarray (Figure 2) control unit.

Data is transferred between the memory units of the processing elements of the subarrays and a large scale disk file buffer memory via a highly parallel input/output buss. Such input/output transfers are controlled by an external general purpose computer which also supervises the ILLIAC IV program runs. The general purpose computer is provided with a limited set of connections to the subarray control units for this purpose.

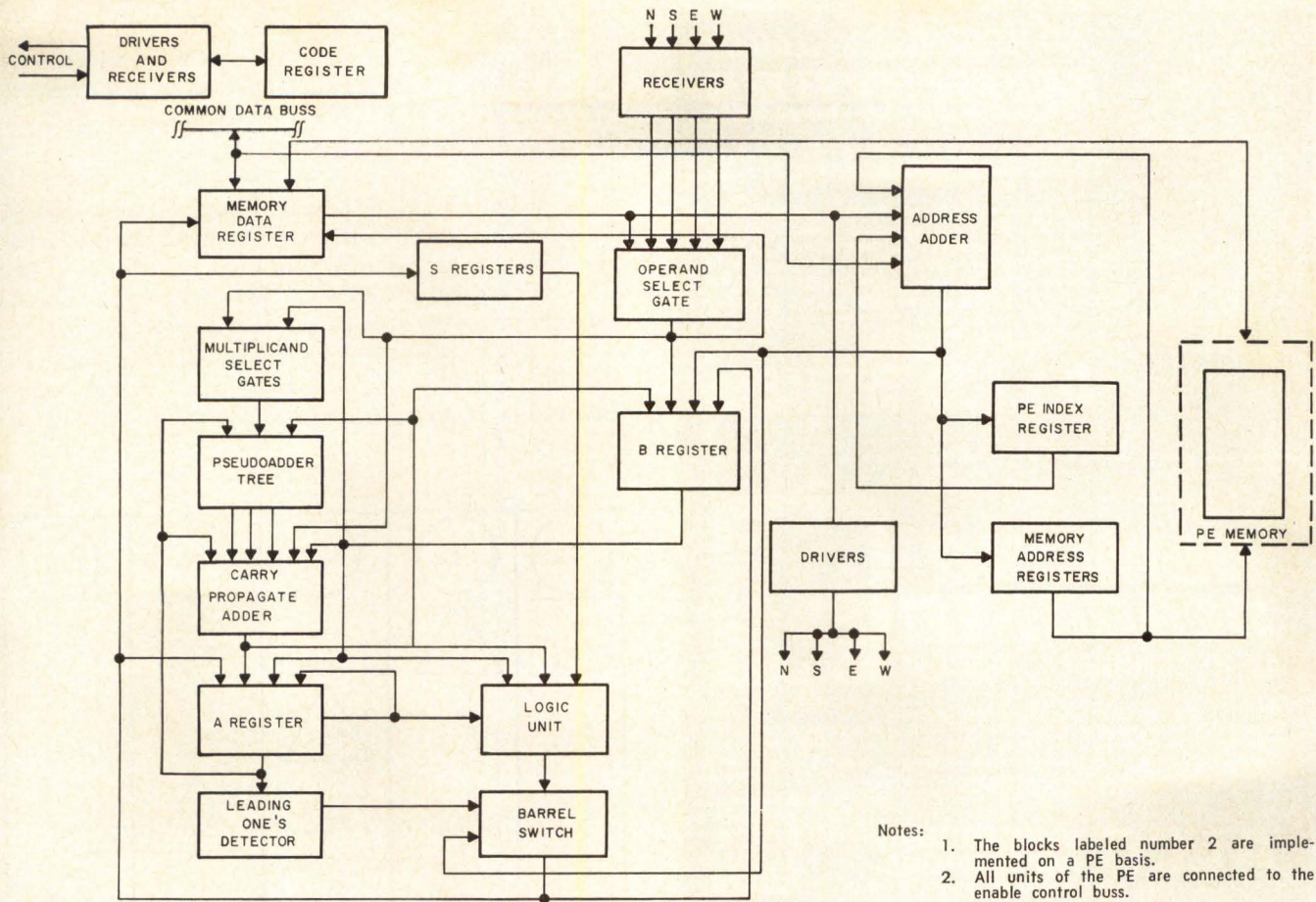


Figure 3—Processing Element Component, Block Diagram.

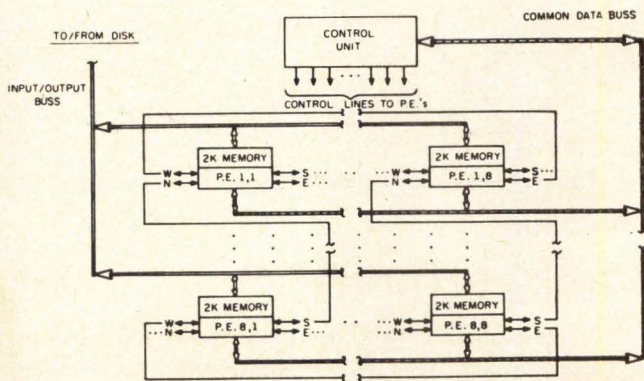


Figure 2—Organization of 64 P.E. Subarray.

The routing connections of the processing elements in the four subarrays are arranged to permit a *united mode* of operation, in which the four subarrays act as a single large array for routing purposes, a *paired subarray mode* of operation which provides routing for two arrays, each containing two of the subarrays, or an *uncoupled mode* in which each subarray operates independently.

Figure 3 shows the structure of one Processing Element (PE). Each PE is provided with three 64-bit arithmetic registers and high speed adders for full 64-bit floating and fixed point operations. The processor is also provided with 2000 64-bit words of thin film memory.

Four routing connections, identified as North, East, South and West are provided in the subarray as shown

in the figure together with busses to and from the control unit and the disk unit for global and input/output data.

It is a vital consideration that the PE is regarded as a complement. It is, in fact, delivered in assembled, tested form to the system supplier by the semiconductor manufacturer. Provision is made in the design of the PE to permit an orderly transition from hybrid LSI components to monolithic LSI components during the course of the program. The technology employed in the design and fabrication of the PE will, it is anticipated, yield a unit price for the first system of this very powerful 64-bit floating point unit of under \$10,000.

Detailed analytical and programming work has been done in the following areas:

- (1) Weapons Effects
 - a. Eulerian flow
 - b. Lagrangian flow
 - c. Neutron transport
 - d. Underground stress-strain model
- (2) Alternating Direction Implicit Relaxation
- (3) General Circulation Weather Model
- (4) Matrix Operations
 - a. Inversion
 - b. Eigenvalue calculation
- (5) Linear Programming
- (6) Multichannel Filter Design and Convolution
- (7) Fourier Transformation

MODERN DESIGN SERIES
MINIATURE
Neon Pilot Lights

1-piece body ideal for space limitations. BNE SERIES has compact lens system protruding slightly above panel. BNF SERIES' lens system extends more for greater illumination. BND SERIES' pilot assembly protrudes beyond panel to provide maximum light intensity.
 Write for details.

ALCO® ELECTRONIC PRODUCTS, INC.
 LAWRENCE, MASSACHUSETTS

COMPACT
NUMERIC
READOUTS
 AT REASONABLE PRICES

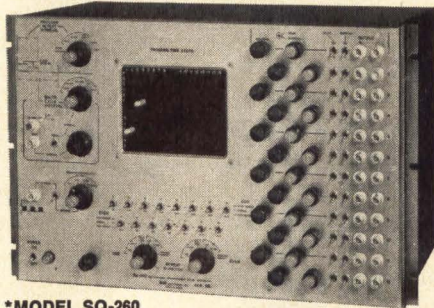
Displays 0-9 numerals by illuminating miniature lamps. Combination of lamps can be controlled with a matrix circuit (not supplied). Decimal points can be used as colon when 2 units are placed together. Indicator provides high illumination with a low voltage and current. Colored filters available. 6 & 12V. Figures 25/32" high. 20,000 hr. bulb life.

ALCO® ELECTRONIC PRODUCTS, INC.
 LAWRENCE, MASSACHUSETTS

PRICES start at \$9.95
 Quantity prices available

CIRCLE NO. 31 ON INQUIRY CARD

A UNIQUE
PROGRAMMABLE PULSE
GENERATOR FOR \$5600



*MODEL SQ-260

Compare this new Model SQ-260 Multiple Pulse Generator with any other and you'll see that it provides the *most* for the *least* cost! Featuring all solid-state integrated logic, the Model SQ-260 also offers: 10 megacycle stepping rate, 12 output channels, 16 time steps, convenient plugboard programming, program repeat capability, step-and-repeat capability, 51 ohm output impedance (change resistor to alter impedance), 12 variable output pulse durations, and 12 variable pulse start delays! All this and more for \$5600.

Call or write for descriptive literature today!
 *Deviations from standard products are available on request.

adar ASSOCIATES, INC. 73 UNION SQUARE
 SOMERVILLE, MASS. 02143
 Telephone: (617) 623-3131

CIRCLE NO. 32 ON INQUIRY CARD

In all the areas listed it was found that highly efficient methods could be evolved, i.e., methods which keep almost all PE's running almost all the time. Thus, the speed-ups observed have been in the order of 256 times N where N relates the speed of the PE to the speed of the computer selected for comparison.

As an illustration of the sort of consideration involved in securing high efficiency on a parallel machine, Figure 4 shows the memory allocation for a 5x5 matrix in 5 PE memories (PEM's). We refer to this storage scheme for matrix elements as skewed storage.

The main reason for skewing a matrix is that rows and columns of a matrix can be accessed with appropriate PE indexing. For instance, to fetch elements

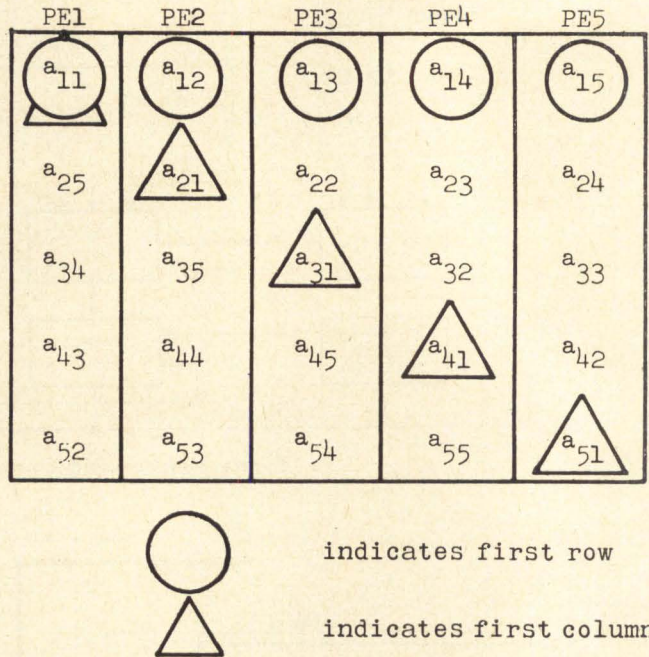


Figure 4—Skewed Storage Technique for Matrices.

of a column, neighboring PE's access elements differing in address by 1.

The illustrated matrix fits nicely into the memory allotted. For matrices where this is not true packing schemes exist to minimize wasted storage space in relation to the operation being performed.

The case of skewed storage just described is an important but simple example of the unique considerations made necessary by the parallel organization of this computer. Manual calculation (like man himself) is essentially sequential. Our electronic calculating aids (computers) have hewn strictly to this "natural" organization of calculations. It is, however, by no means "natural" for a technological innovation to so restrict itself. In fact, man is a slow, highly error prone computing device. The parallel approach to computing, it must be said however, does require that some original thinking be done about numerical analysis and data management in order to secure efficient use. In an environment which has represented the absence of the need to think as the highest virtue this is a decided disadvantage.

Contemporary Electronics is one of the largest producers of computer pulse transformers in the U.S.

SO?

So, maybe you're missing a bet if you haven't checked Contemporary Electronics for *quality, service* and *price*.

Contemporary Electronics *specializes* in pulse transformers. It's not a sideline, but a principal part of our business. Well over 100,000 pulse transformers are produced each month in 75 different designs.

Advantages? Here are some.

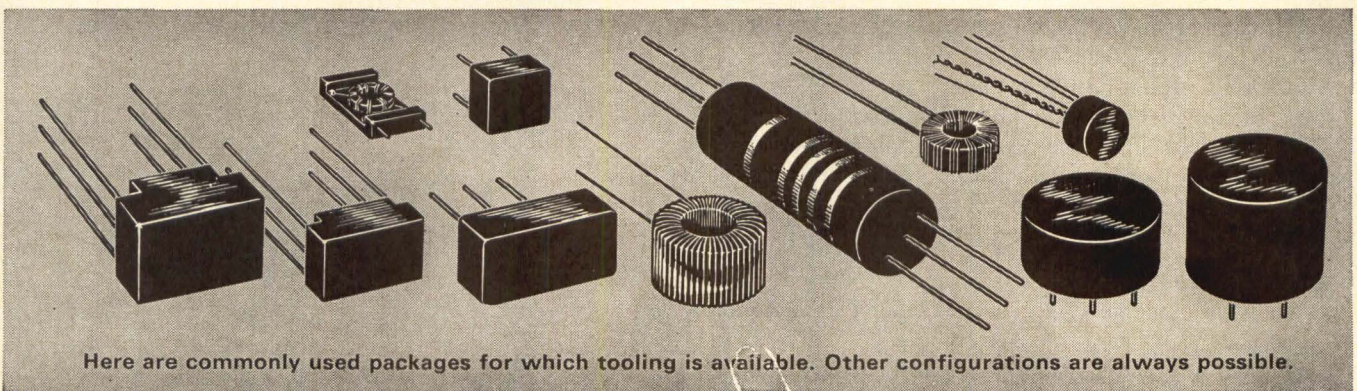
Technical Capability. Contemporary Electronics engineering staff knows computers and can design any special product for any application.

High Quality. Most transformers have special high quality design features. All pulse transformers are 100% inspected as many as three times before shipment. QC system meets MIL-Q-9858, and has been approved for use on the Apollo program.

Fast Sample Service. Samples, small production lots and specials are normally shipped 24 to 72 hours after receipt of request.

Interested in what can be done in terms of performance, size, delivery, or MIL-specs? Get to us—we've got lots more to tell.

WRITE, OR CALL COLLECT AND WE'LL HAVE THE FULL STORY TO YOU WITHIN 48 HOURS



Here are commonly used packages for which tooling is available. Other configurations are always possible.

 **CONTEMPORARY
ELECTRONICS**

4838 West 35th Street, Minneapolis, Minnesota 55416 612/920-6444

EXTRA SERVICE TO THE DATA PROCESSING INDUSTRY

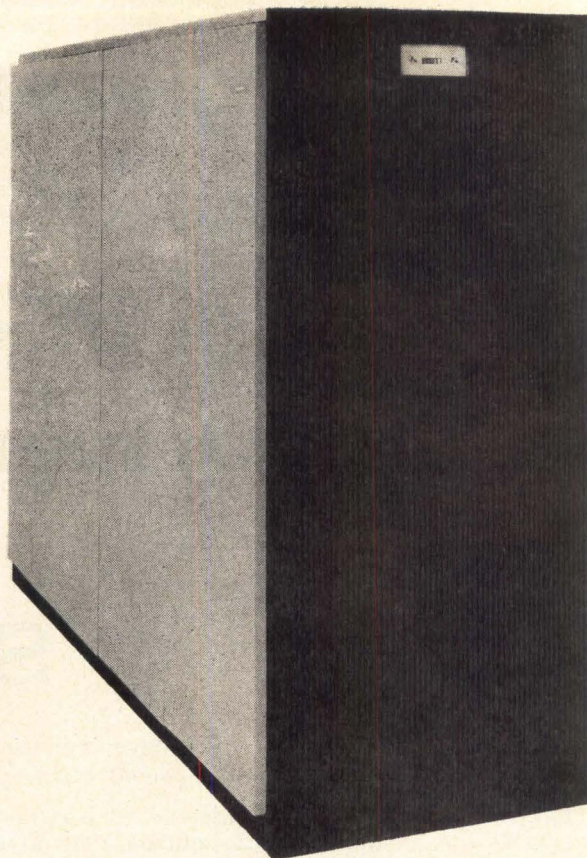
CIRCLE NO. 33 ON INQUIRY CARD

A 20 MILLION BIT HIGH SPEED CORE MEMORY

Roy Norman

Ampex Computer Products Div.

Here is a Production Model of an Extended Core Storage with Access time of 1.5 Micro-second and Cycle time of 2.7 Micro-seconds, at a Cost Below Three Cents Per Bit.



Over the years, the capacity of random access central storage in computer systems has, in general, steadily increased. In addition, the price per bit has decreased at the same time that performance characteristics have improved. Recently, some computer manufacturers have taken advantage of memory designs which represent a dramatic extension of this trend, that is, core memories with very high capacity and significantly lower price per bit compared with conventional memories. The trade off involved in such designs is that cycle time is sacrificed in order to achieve these ends. This type of storage module is variously known as Mass Memory, LCS (Large Core Storage), or ECS (Extended Core Storage). Mass memory may yield overall economies in system design, examples of which appear in the literature.^{1,2,3}

Ampex Computer Products Division now has in production such a memory, which we believe is unique, inasmuch as its cycle time is significantly faster than other memories of comparable price and capacity. This article describes the operation of the Ampex memory system.

Specifications

The memory has a total capacity of 262,144 words. Each word consists of 72 data bits organized into 8 bytes, each byte comprising 9 information bits. Access is random to any of the 262,144 addresses and the data buss carries the 72 bits in parallel. The access time to any address is 1.5 μ seconds and cycle time is 2.7 μ seconds. The memory is logically organized as a two-port entry, four-way interleaved device. This means that the

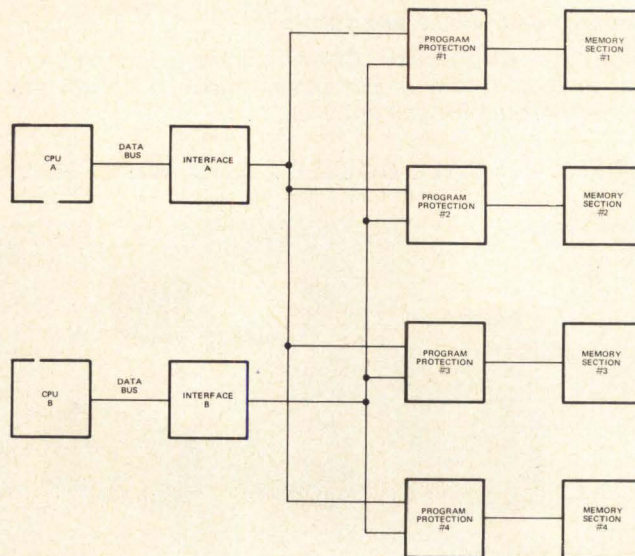


Fig. 1 — Interface block diagram.

memory consists of four 65,536 word sections. Each section is essentially electrically independent of the other three, and hence, the four sections may be operated in parallel. The data buss and the interface circuits are time shared by the four sections, maximum interleave rate being 200 nanoseconds. If sequential interleave between the four sections is employed, cycle time is effectively divided by four to give an equivalent of 675 nanoseconds cycle time.

Two sets of data busses and interface circuits are provided so that two processors may share the memory through the two-port entry facility. Priority logic and

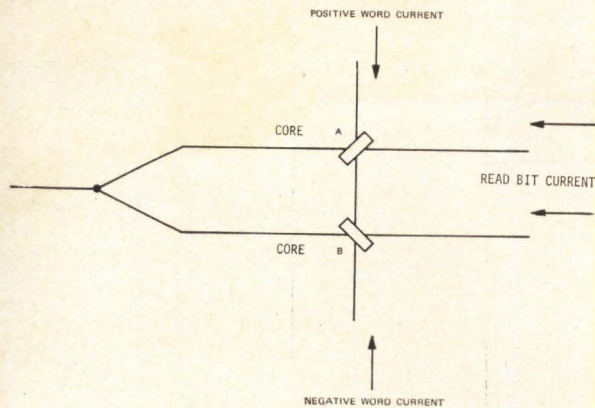


Fig. 2 — Anticoincidence scheme.

an auxiliary keyword memory are associated with each section so that program protection may be provided. Figure 1 shows a block diagram of the interface to the memory sections.

Memory Organization

The memory is organized in a 2-wire 21/2D configuration. The magnetics array has 2048 word lines and 32 lines for each data bit in the bit dimension, hence, a total capacity of 65,536 words of 72 bits each is obtained. Four such arrays with their associated drive-sense electronics and control logic comprise the entire memory module.

A 22-Mil lithium core with a maximum switching time of 235 ns. is employed. It may be noted that the ratio of cycle time to core switching time in this design is 11.5. In smaller 3-wire 21/2D designs this ratio is usually closer to 3. The additional time required in the mass memory results from bit line recovery, current rise times and driver turn off skew. A design compromise was made, so that low cost at high capacity could be maintained at the expense of cycle time.

A novel sensing technique is used which requires only one amplifier for each data bit. The amplifier is connected across the current source side of the bit drivers, so that an automatic routing of the sense signal to the amplifier is achieved, thus eliminating the need for strobed pre-amplifiers.

Figure 2 shows the orientation of the cores with respect to the drive lines. Bit current flows in the direction shown during the read portion of the cycle. Word current may flow in either the positive or negative direction as determined by the address. If the positive direction is selected, then Core B will be switched, and the currents in Core A will buck each other. Similarly Core A would be switched for a negative word current in the read portion of the cycle.

Magnetics Array

In essence, the array is a large double-sided core plane. The plane folds once, as shown in Figure 3. For manufacturing purposes, the cores are arranged in mats of 264 word wires by 288 bit wires, giving a total of 76,032 cores per mat. Spare lines are included in the word dimension for convenience of final test and field service. There is one spare word line for every 32 active lines, so it may be seen that each core mat contains 256 active word lines. A total of 64 mats, or 4,866,048 cores, comprise the total magnetics array.

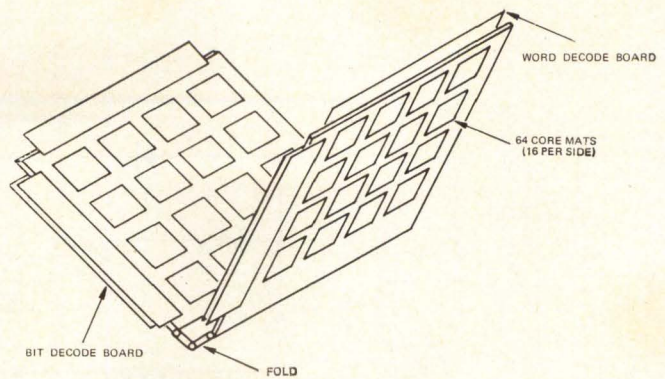


Fig. 3 — Magnetics array.

For optimum sensing conditions, the bit lines forming the pair are adjacent to each other. Thus a single box core formation facilitates employment of the anticoincidence selection scheme.

The drive lines are terminated directly on multilayer printed circuit boards surrounding the array. These boards contain the stack decoding diodes and biasing resistors for both word and bit dimensions.

A single physical wire is used for the entire word line. This wire passes over the fold in the array through flexible material, hence, reducing the number of wire terminations substantially. Only 13,440 solder joints are required for terminating all of the drive lines in an array, including the spare word lines. This represents a very low solder joint to core ratio. Minimization of these solder joints is necessary to ensure good reliability from the design and to achieve cost objectives.

Word Drive Circuit

In each magnetics array, it is necessary to make a unique selection of one out of 2048 word lines. The word dimension is divided logically into two groups. Each group of 1024 word lines is decoded by means of a 32 x 32 selection matrix. A standard 2 diode/line selection scheme, employing both a positive and a negative current source, was chosen. There is a limitation on the size of a selection matrix, in that the capacitance of unselected lines and drivers must be considered. For this reason, a single 64 x 32 matrix was not used in this design.

Since an anticoincidence scheme is used, direction of read word current is a function of the address selection word in any given memory cycle. Obviously, write word current is always of the opposite polarity to read word current within a cycle. Thus, one bit of the address word is used to determine current polarity, one bit is used to select the word group, and ten bits to decode one out of 1024 lines. The remaining four bits in the address word are used for bit dimension decoding.

Figure 4 shows the circuitry surrounding a selected word line. The selected driver and sink are switched on at the beginning of a memory cycle. This enables the charging current, resulting from movement of the array through a voltage excursion, to be fully dissipated before the word selection current is switched on. This does not result in loss of cycle time, since a delay is mandatory for sensing purposes anyway. The current sources are switched and provide a shaped pulse of current to the selection matrix.

The capacitance of the unselected drivers and the

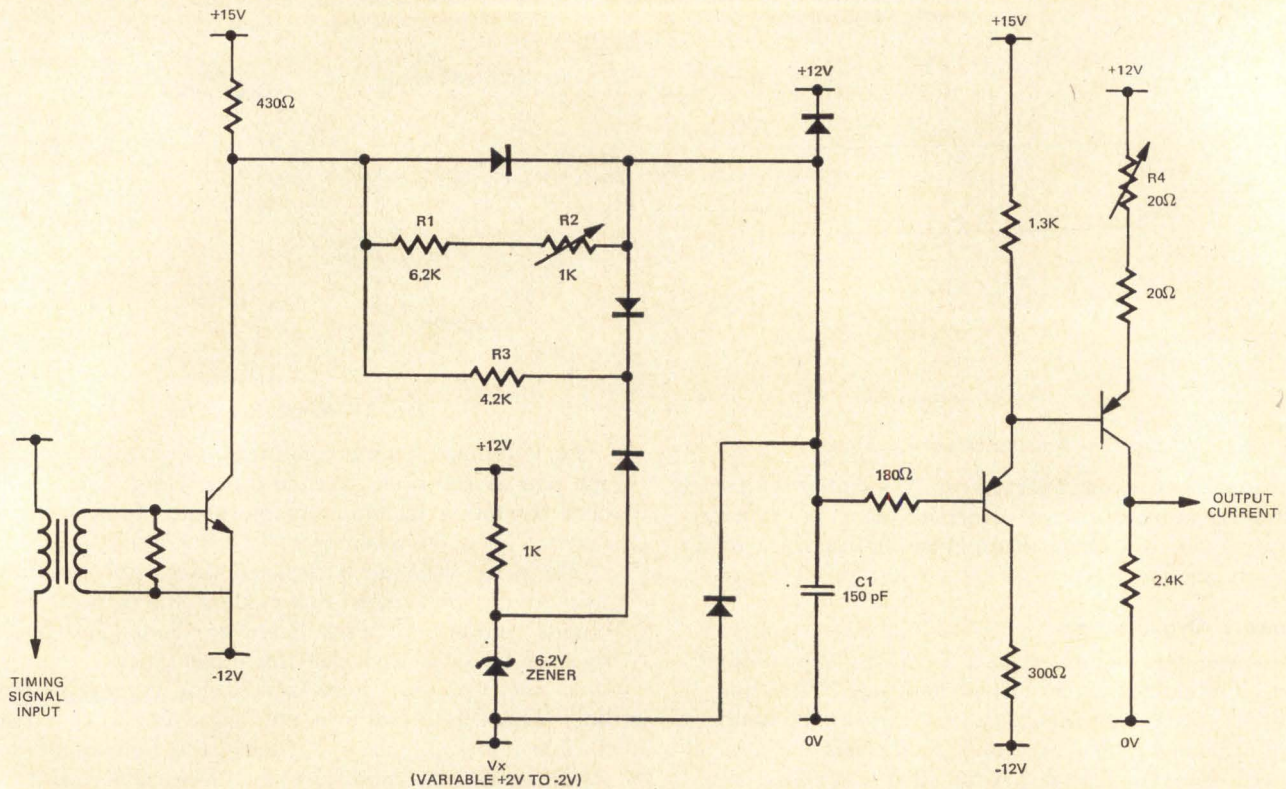


Fig. 6 — Positive word current source.

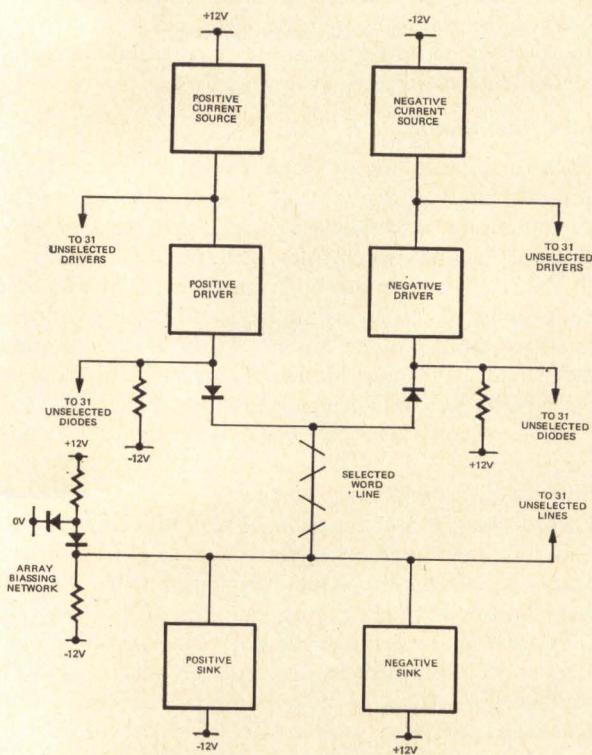


Fig. 4 — Word selection matrix.

inductance of the selected word line form an underdamped LC circuit. This would result in a current overshoot within the selected word line if no compensation were provided. It was found that shaping of the current pulse from the current source yielded better results than any other technique. The design used, produces a double time constant rise time of current from the current source, as shown in Fig. 5 (a). This results in the

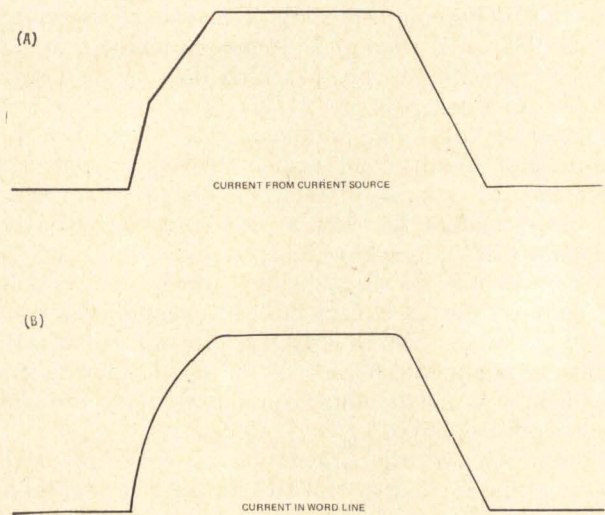


Fig. 5 — Results of shaping the current pulse from the current source.

required waveform of current in the drive line as shown in Fig. 5 (b).

A schematic of the positive current source is shown in Figure 6: the negative current source is of a similar design but modified to operate from the opposite polarity. It may be seen that the output current rise is controlled by the time constant of C1 discharging from +12V to Vx. Initially, the time constant is C1 and R1 in series with R2 shunted by R3. When the voltage across the capacitor reaches (Vx + 6.2V), the shunt resistor R2 no longer determines the time constant and, hence, a slower rate of rise results. Vx is a variable supply which controls output current magnitude and is used to plot shmoo limits on the system. R4 and R2 are used to make initial adjustments in current magnitude and overall rise time respectively.

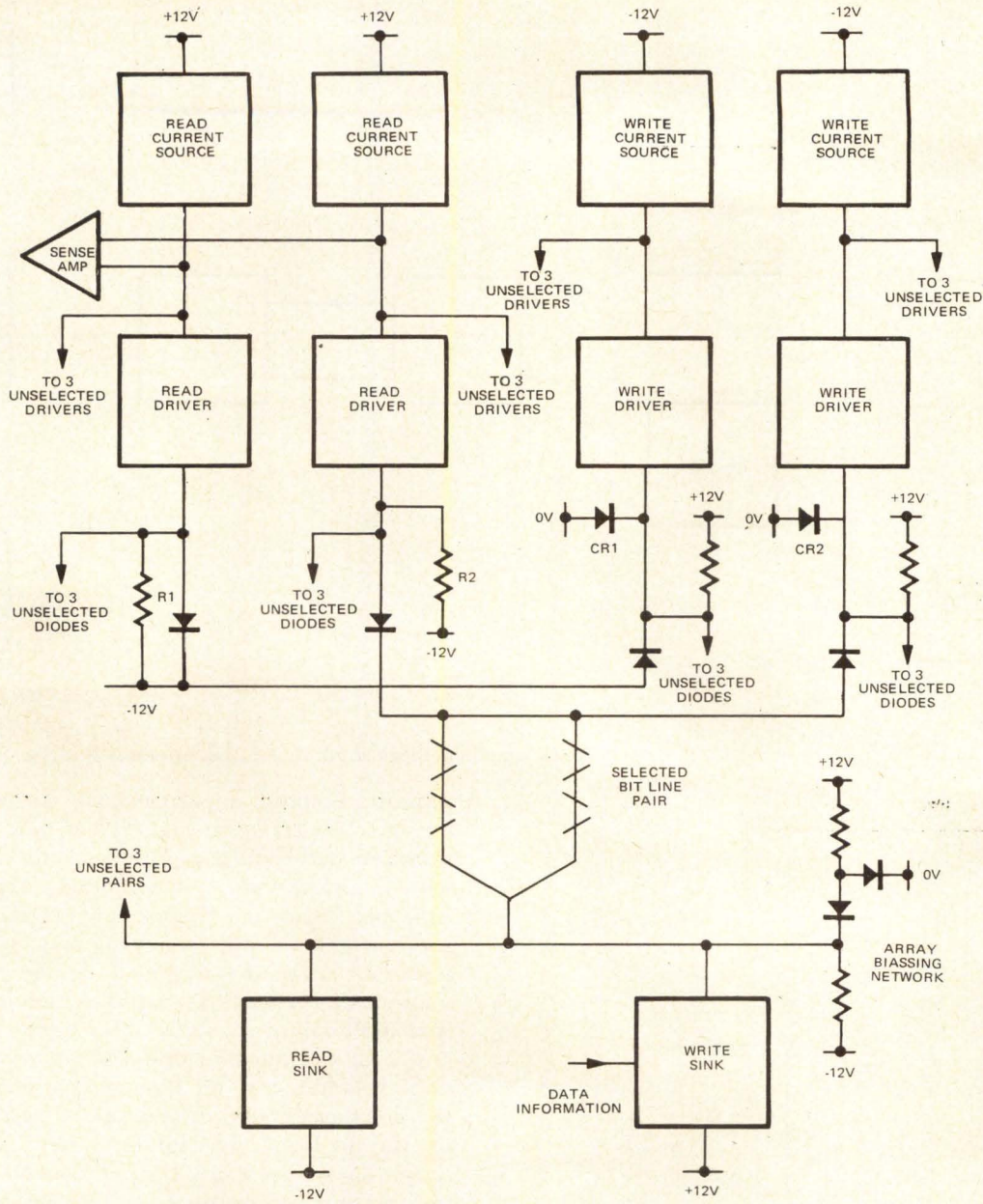


Fig. 8 — Bit selection matrix.

The word drivers and sinks employ transformer coupled floating switches. The primaries of these switches are connected in a 4 x 8 matrix as shown in Figure 7.

Bit Drive Circuit

For each data bit there is a total of sixteen pairs of bit lines. This yields a total of $72 \times 16 \times 2 = 2,304$ lines in the bit dimension, thus, the aspect ratio of the magnetics array is almost square. Since a two-wire array is used, it is necessary for sensing purposes to drive current equally in the selected pair of bit lines. Sensing is then accomplished by detecting the differential signal between the pair of bit lines.

As may be seen from Figure 8, the sink switches pass the sum of the currents from each half of the pair of lines. A 2 diode/line decoding scheme is employed, the sixteen pairs being decoded from four drive pairs and four sinks. In this system, write bit current is conditional on the information to be stored. Data control is

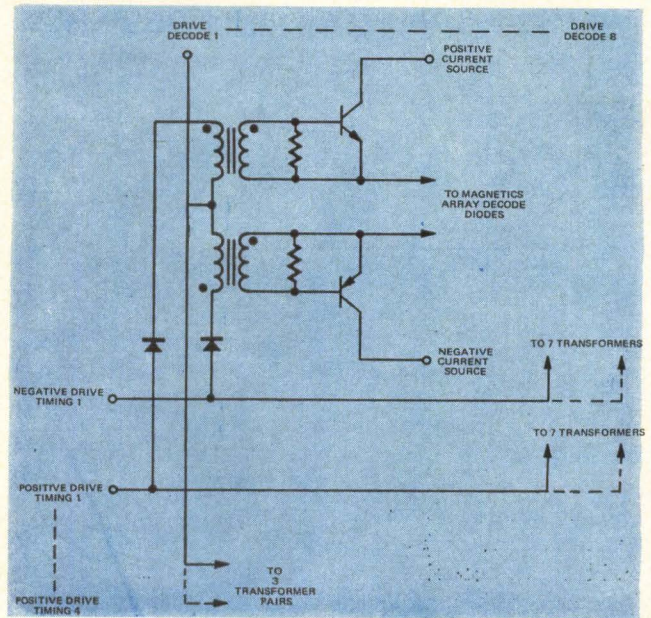


Fig. 7 — Word drive matrix.

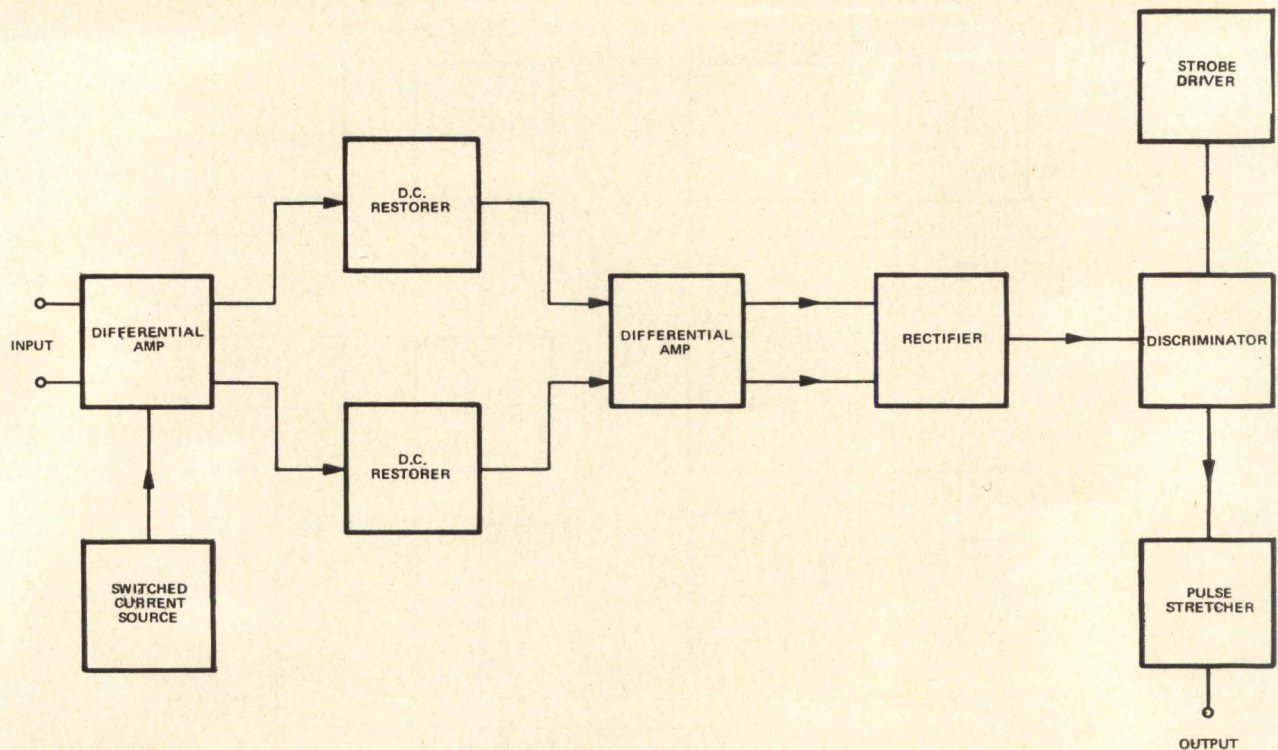


Fig. 10 — Sense amplifier block diagram.

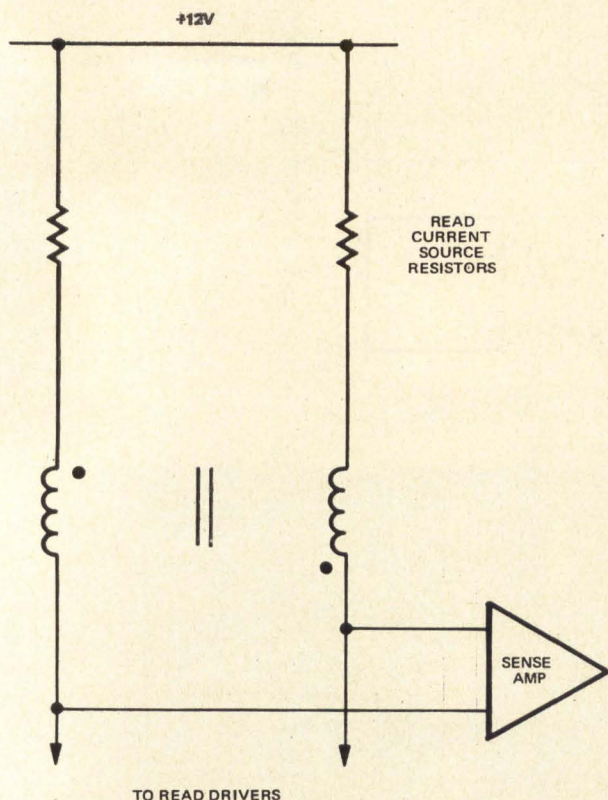


Fig. 9 — Read current source.

achieved by making the write sink enable pulse a function of data information. When a zero is written in a particular address, current flows from CR1 and CR2 into the write drivers and current sources. These diodes provide a current path so that the write drivers do not build up an excessive amount of stored charge resulting from zero collector current and a high base current.

Both read and write current sources consist of a

resistor, resulting in exponential current rise in the bit lines. Referring to Figure 9, it may be seen that a transformer is connected in series with the read current source in an antibalun configuration. This serves a dual function. First, it provides for equalization of the read currents in each half of the pair enabling the differential voltage developed during the rise time to be minimized. Second, it provides differential isolation from the current source resistors during sensing.

The bias resistors R1 and R2 also serve a dual function. In addition to the conventional purpose of biasing the decoding diodes, these resistors form a termination for the bit lines. The bit lines may be considered as transmission lines shorted at the far end. The termination resistors are essential for realizing a rapid settling of the differential signals produced at the start of bit current.

As in the word system, transformer coupled floating switches are used for the drivers and sinks.

It may be readily seen that any DC imbalance in decode diodes, driver transistors or drive lines will produce a DC offset at the amplifier input. Even though DC restoration is performed within the amplifier, there is obviously a limitation on the offset because of the dynamic range of the amplifier prior to DC restoration. In this design, a maximum of 400 mV offset can be accommodated by the amplifier at the input. Therefore, the decode diodes are matched within 100 mV forward drop and the drive transistors are matched within 200 mV difference in V_{CE} . This leaves 100 mV for resistive differences in drive lines and wiring.

Sense Amplifier

The partial disturb problems normally encountered in a 2 1/2 D memory exist to a far greater extent in this mass memory design. A selected pair of bit lines pass through a total of 4,224 cores. These cores are partially

disturbed by the bit current and, under worst case information patterns, a differential signal in the order of a few volts is developed. In addition, the rise of bit current will produce a differential signal at the input to the amplifier since neither the drive lines, diodes nor drive transistors are perfectly matched. The sum of these two effects may well produce a large differential transient when bit current is established which is an order of magnitude larger than the sense signal to be detected.

For this reason, it is necessary to wait until the initial transient has settled before the word current is switched on. This settling time was found to be 700 nanoseconds in practice. When word current is applied, the selected core produces a turnover signal of approximately 30 mV amplitude which is sensed differentially between the bit line pair. At sensing time, a DC voltage offset could exist at the amplifier input as a result of forward voltage drop differences in the bit drive system. This offset, which can be a maximum of 400 mV, must be eliminated by means of DC restoration within the amplifier.

It may be seen that the design requirements of the amplifier are very restricting. A block diagram of the amplifier is shown in Figure 10. The first differential amplifier operates from a switched current source. The current source remains off during the initial transient to prevent the amplifier from going into saturation. Prior to sense time, the current source is enabled as may be seen from the overall timing diagram shown in Figure 11.

The first amplifier has a differential gain of approximately 17. As a result, the output level of the first stage may sit at any point over a range of 6.8 V. The amplifier is designed to have a dynamic range sufficient to accommodate this spread. A "roll off" capacitor is included in the amplifier so that the gain of the amplifier diminishes rapidly at frequencies higher than those composing the turnover signal. This technique provides some measure of filtering against high frequency noise appearing at the input.

DC restoration is achieved using a CR network in conjunction with a chopper transistor. Referring to Figure 12, it may be seen that when the chopper conducts before sensing time, the capacitor charges rapidly to a voltage equal to the output voltage of the first stage with respect to ground. The time constant is essentially controlled by R1 and C1 since the chopper represents a very low impedance in the ON state. Therefore, the capacitor becomes fully charged within 35 nanoseconds. In practice, the chopper remains on for approximately 100 nanoseconds.

Immediately prior to sensing time, the chopper is switched off. The input impedance of the second amplifier is approximately 10 K ohms, thus, the time constant of the coupling circuit becomes 800 nanoseconds. As a result, the core turnover signal which has a base width averaging 220 nanoseconds, is passed through the coupling circuit with essentially no distortion. Since C1 has a voltage across it equal to the DC level of the first amplifier output, the input to the second amplifier is biased at ground. DC restoration is accomplished on both of the differential inputs to the second amplifier and hence, the DC offset is removed while the turnover signal is allowed to pass through the coupling network.

Any voltage drop produced by the chopper transistor

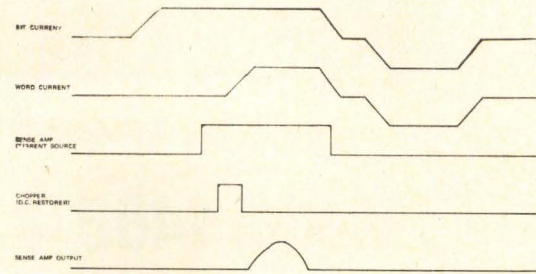


Fig. 11 — System timing diagram.

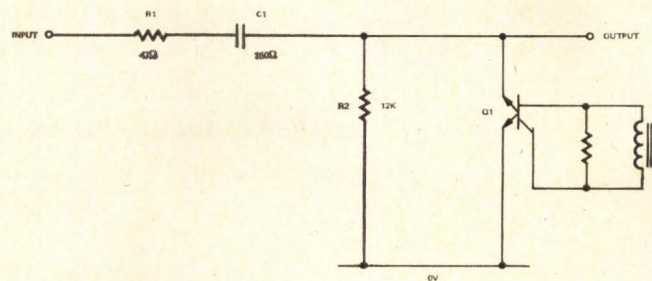


Fig. 12 — D.C. restoration circuit.

is amplified by the second amplifier and appears as an error signal either adding to, or subtracting from, the turnover signal. Thus, it is advantageous to have as much of the overall gain of the amplifier prior to DC restoration as possible. A tradeoff must be made however due to the dynamic range requirements of the first stage of amplification.

The differential gain of the second amplifier is 32. The output is rectified so that only half of the available differential signal amplitude is used. The discriminator circuit compares the signal amplitude with a threshold level during strobe time and, if a "ONE" signal is detected, the pulse stretcher transmits a pulse which sets the data register.

Packaging

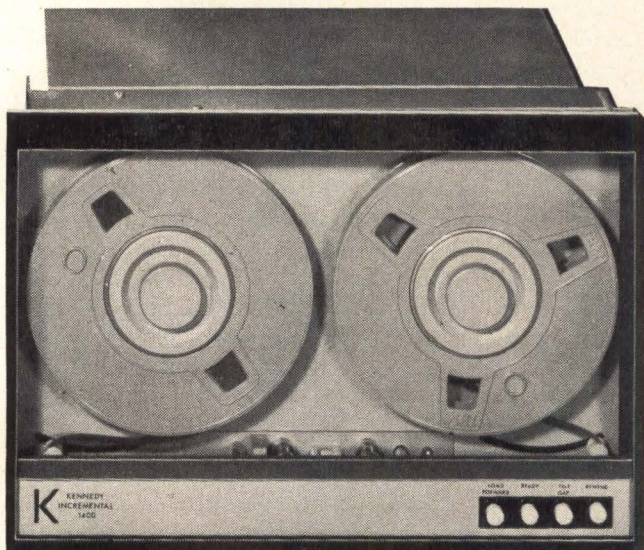
The memory is mechanically divided into two assemblies. The magnetics assembly contains the four magnetics arrays. The arrays are mounted on slide assemblies so that any one of them may be unplugged and withdrawn from the memory. Once out of the memory frame, the array may be unfolded so as to expose all sides of the plane. Thus, if the side covers are removed, any field service necessary may be accomplished on the array without the necessity of removing the array from the machine. A photograph of the folded array and word drivers is shown in Fig. 13.

The electronics assembly houses all of the bit drive, sensing, and control circuitry. Large multilayer printed circuit boards are used for packaging the bit drive and sense electronics. The circuits for nine bits of information are contained on a single board. It may be seen that eight such boards are required for each array or a total of 32 for the whole memory. These boards are housed in a card file assembly and connection is made to the magnetics array by means of flexible cabling.

All other control electronics are packaged on 5" x 6" printed circuit cards which are housed in card files in the conventional manner.

Kennedy Co.

announces the
Model 1400/360
Incremental Recorder
 with IBM System/360
 compatibility
 and
 nine-track
 800 BPI format



The Kennedy Model 1400/360 Incremental Magnetic Recorder has been designed as a low-cost, highly reliable recorder capable of writing IBM System/360 compatible tapes from sources of medium speed data. All special marks and gaps required by System/360, 2400 tape units are internally generated to system specifications. Standard recording speed is 0-500 bytes per second asynchronously. Write for more details.

This is the one you've been waiting for.

Kennedy Co.

540 W. WOODBURY ROAD, ALTADENA, CALIF. 91001 · (213) 681-9314
 CIRCLE NO. 34 ON INQUIRY CARD

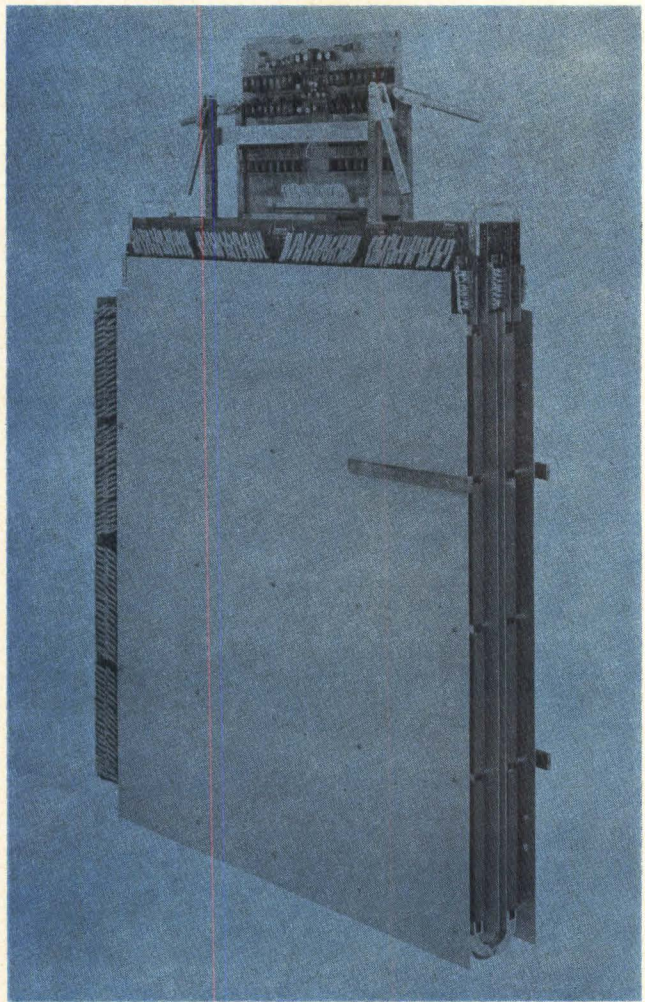


Fig. 13 — Photograph of folded array and word drivers.

A self-test feature is included in the memory. The control and indicator panel for this function forms the front of the machine.

Results

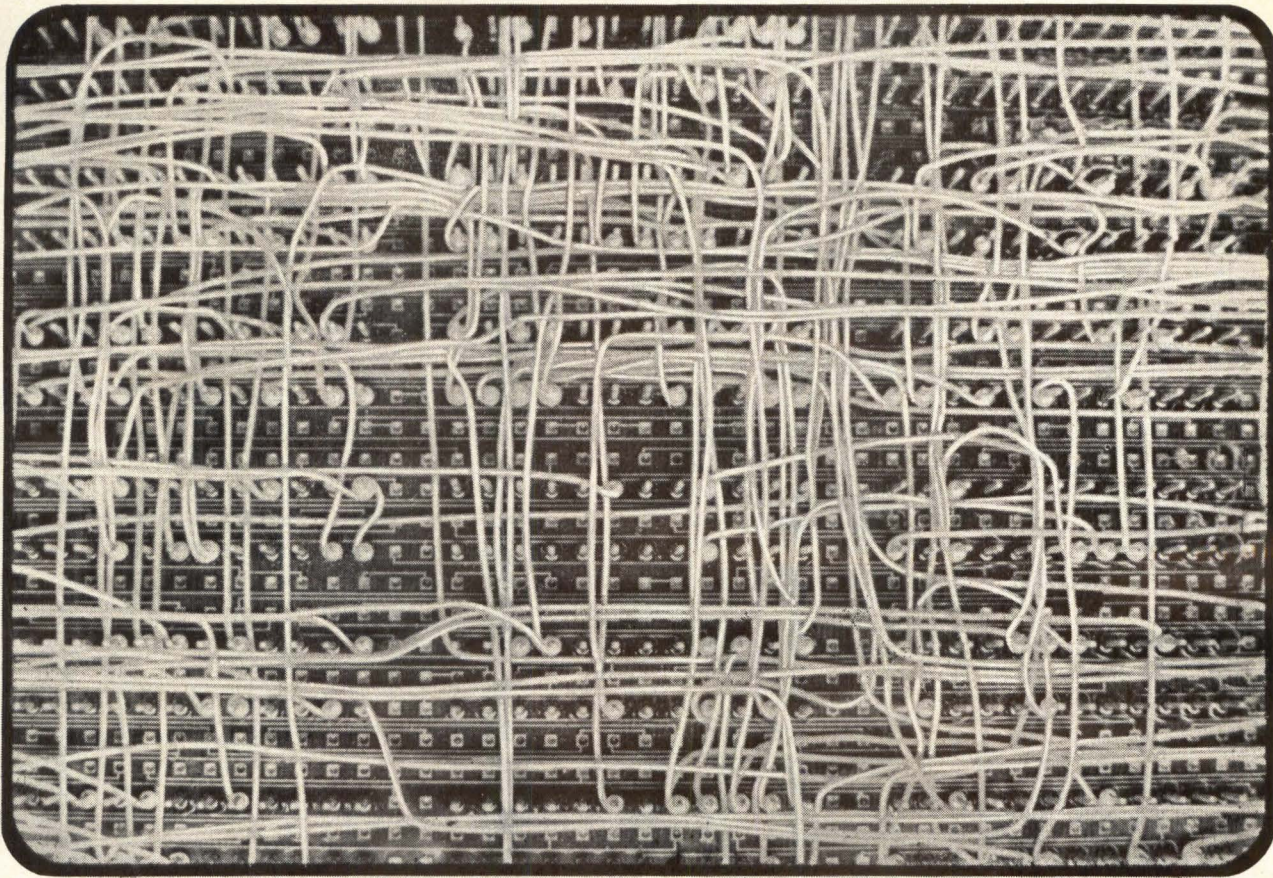
The shmoo limits for the design were found to be large. Typically, the magnetics arrays exhibit an operating current range of $\pm 12\%$.

No delta noise is present at the time of the core turn-over; there is, however, an unwanted signal produced by general system noise. This system noise is produced primarily by the power distribution system when large bit currents are switched in the array. In addition, there is electromagnetic coupling between arrays since the drive lines tend to act as antennae. Both of the above effects are minimized by heavy magnetic shielding and by power supply decoupling. Using these techniques, a more than adequate signal to noise ratio is obtained in the amplifier.

REFERENCES

1. "Large Core Storage Utilization in Theory and in Practice," T. A. Humphrey — *Proc. SJCC* 1967.
2. "Extended Core Storage for the Control Data 64/6600 Systems," Gale A. Jallen — *Proc. SJCC* 1967.
3. "Simulation of an ECS Based Operating System," M. H. MacDougall — *Proc. SJCC* 1967.
4. "Multi Million Bit 2-1/2D Memory," R. J. Petschauer, G. A. Anderson, and W. J. Neumann, *Computer Design*, April, 1966.

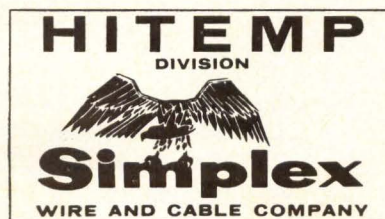
We're wired in!



How does HITEMP meet your "wire wrap" specs? Perfectly. Complete range of sizes up to 36 gauge. Wall thickness as thin as 3 mils. Just name your insulation — Teflon-TFE and FEP, Kynar, Polysulfone, Kapton, PVC. All custom made for automatic and semi-automatic wrapping equipment.

HITEMP is wired in! Our long experience in the field, plus the most modern facilities, assures you of a constant quality product for "wire wrap" application, as well as many other types of wire and cable, including power, signal, and miniature coaxial cables.

Our complete engineering capability is at your disposal. Alert us by phone or letter to your requirements. Let us focus our abilities and know-how on your particular problems.



HITEMP DIVISION • WESTBURY, N.Y. • MONROVIA, CALIF.

CIRCLE NO. 35 ON INQUIRY CARD

Systems Implications of Microprogramming

William J. Patzer, Mgr., Systems Architecture Dept., and Gilbert C. Vandling, Advisory Engineer, IBM Corporation, Owego, New York

To permit the system designer to determine whether to consider a microprogrammed computer for a particular application, this article presents a qualitative description of the unique functional characteristics of microprogrammed control, describes the microprogrammed computer as a system component, and compares the general characteristics of microprogrammed computers with general purpose computers.

Although the concept of microprogramming is not new^{1,2}, only recently have computers incorporating microprogrammed control been delivered in large numbers. While the inherent flexibility of a microprogrammed organization makes it possible to specialize computer instructions and increase efficiency for specific applications, this capability has not been widely exploited; most such machines have been general-purpose data processing systems used in commercial and scientific applications intended to operate on a wide variety of problems and they would benefit little from such specialization. Also, standardization has been considered a more important goal than specialization.

In some applications, such as control systems, a computer and its peripheral equipment are treated as a component of a larger system rather than a system in itself. Many such systems — although they may have an additional capability for offline processing during slack periods — are primarily dedicated to a particular task or process. Here, system performance can often be significantly increased through computer specialization via microprogramming. A microprogrammed computer organization is well suited to applications where very specialized tasks require a significant percentage of total execution time, because complex operations corresponding to subroutines in a conventional computer can be executed as a single macro instruction. Decreased execution time results because the subroutine linkage, multiple instruction fetches, and redundant operations are eliminated. The ease

with which the computer architecture can be restructured via microprogramming is also a significant consideration. (The term architecture is used to describe the attributes of a system as seen by the programmer, i.e., the conceptual structure and functional behavior, as distinct from the organization of the data flow and controls, the logical design, and the physical implementation.)

In addition, microprogrammed computers have an inherent capability for efficient simulation (the execution of machine language programs written for a different computer) which permits a significant reduction in development time and overall system costs in some applications. It makes possible the use of existing programs, permits the use of existing software with little or no modification, and makes possible program and/or system simulation and check-out using another computer.

Microprogrammed Computer Characterization

A microprogrammed computer is a computer incorporating explicit matrix control. Each matrix row, (see Fig. 1) corresponding to a word in control storage, is called a microprogram word and it controls the operation of the arithmetic unit for a well-defined interval of time (one machine cycle, a number of machine cycles, or for one main storage cycle, depending on the design of the particular computer). The matrix columns, either in groups or individually, designate specific control functions, called micro-orders. A group of columns corresponding to bits in a

control word can be used to specify one of a number of mutually-exclusive micro-orders to be performed; for example, micro-orders might identify corresponding internal registers to be gated to an adder input; a single column (bit) can be used to specify which one of two mutually-exclusive micro-orders is to be performed, such as whether or not an adder input is to be complemented. The design of the microprogram-controlled computer is usually such that a number of different micro-orders can be executed during a single machine cycle. This number ranges from two to over twenty, depending on the design of the particular computer.

A microprogram is the sequence varied over a wide range by modifications or additions to the microprogram store.

In practice, many different implementations of microprogram storage exist. Some are electrically alterable, others are mechanically alterable, and some require actual physical replacement of the microprogram storage media.³ Variation of architecture through modification or replacement of microprogram storage is thus characteristic of microprogrammed computers. The ease with which this may be accomplished, the amount of architectural variation possible, and the associated cost of any change depend on the particular design.

To the programmer, the characteristics of a microprogram-controlled computer appear identical to the characteristics of conventionally-controlled general-purpose computer for a particular microprogram storage configuration. Within the restrictions

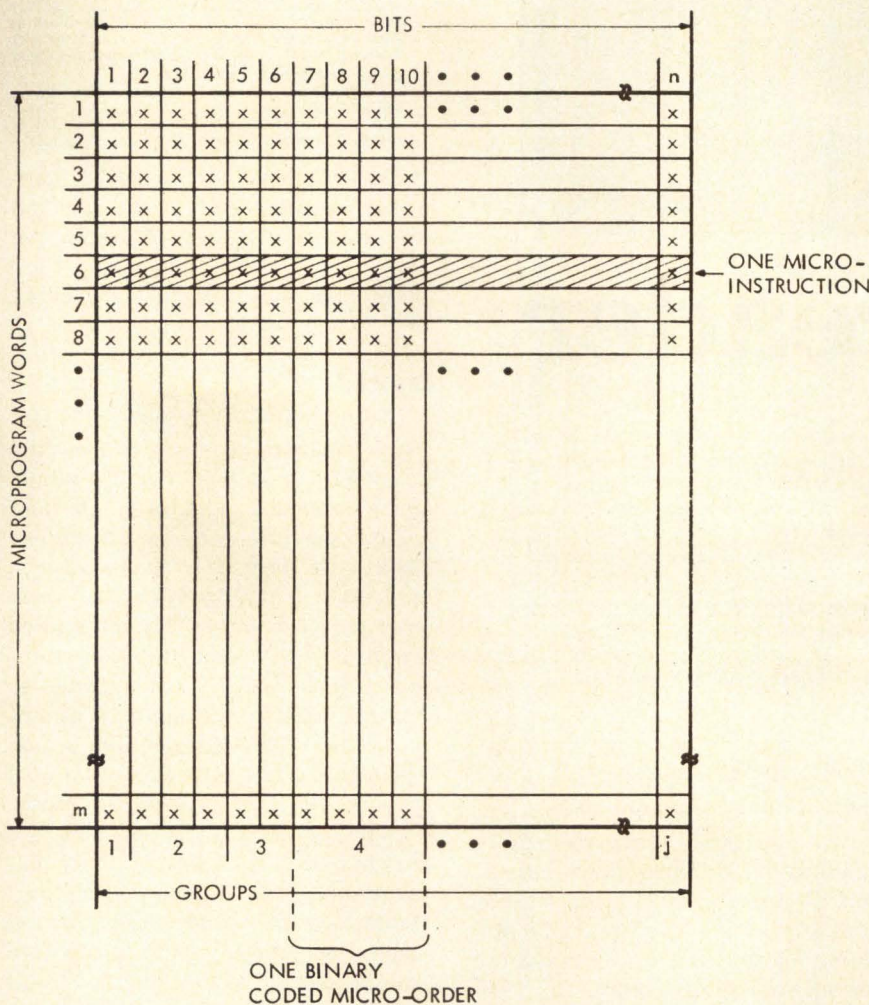


Fig. 1. Control storage partitioning

imposed by the instruction set, storage capacity, and execution time, each can be programmed for a wide variety of problems.

To the systems engineer, a conventional general-purpose computer, unlike a microprogrammed computer, does not have explicit control storage and cannot readily be restructured without redesign and repackaging. Consequently, the conventional computer is difficult to specialize for a particular application.

Computer Specialization

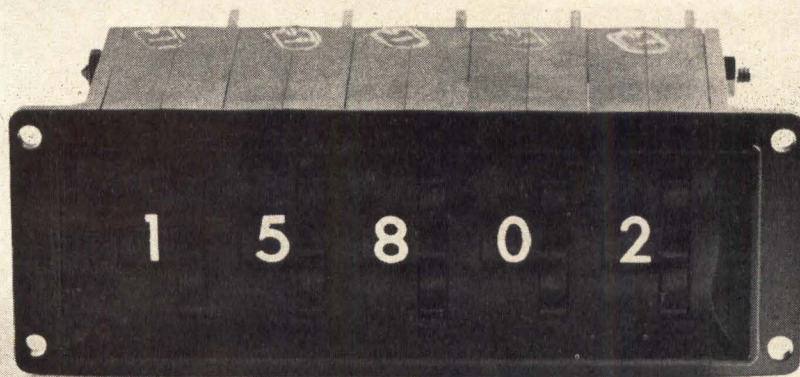
A microprogram-controlled computer is tailored to an application by modification of the control storage matrix, as described above. Among the modifiable processor parameters are instruction set and operand

length. The instruction set may be single address, accumulator-oriented, or it may be two address, register file-oriented. Operands manipulated by these instruction sets may include fractional and/or integer scaling, and operand lengths that are integral multiples of the hardware data flow width (size of the data paths between registers, storage, and the arithmetic-logical unit). A single microprogram-controlled computer design is thus able to satisfy a variety of requirements without extensive logic hardware modification. In addition, microprogramming allows instruction of microprogram words required to perform a specified function, such as ADD or MULTIPLY. Depending again on the design of the particular computer, a microprogram may consist of:

- A fixed sequence of microprogram words containing conditional micro-orders.
- A variable sequence of microprogram words containing unconditional micro-orders.
- Both variable and fixed sequences of microprogram words containing both unconditional and conditional micro-orders.

In a microprogram for MULTIPLY, a computer using a fixed sequence of microprogram words would contain an order of the form "if the current multiplier bit is one, add the multiplier to the partial product; if zero, add zero to the partial product." A computer having a variable sequence of microprogram steps could have one microprogram word containing an order to "add the multiplier to the partial product"; in such a computer, the sequence would be altered depending on whether the multiplier bit is one or zero. In practice, a microprogram-controlled computer may have both conditional and unconditional micro-orders, and a given micro-program word may have only one or a number of successors. Alternative successors are usually specified by the microprogram, that is, groups of matrix columns are encoded to specify multiple successor microprogram words and other groups encoded to specify the conditions associated with each alternative. Conventional control logic is then used to test the specified conditions and select the address of the associated successor.

The microprogram-controlled computer architecture and instruction set is a direct function of the contents of microprogram storage (the $M \times N$ matrix). New instructions or features correspond to additions or changes to the matrix. Thus a new instruction can conceptually be included by adding one or more microprogram words (rows) and/or modifying existing rows. This does not normally require any circuit or logic redesign or any repackaging; i.e., does not alter the column structure and associated micro-order repertoire of the computer. Therefore, the functional characteristics of the microprogrammed computer can be



speed reader

Digitran[®] and Miniswitch[®], the industry's standard in thumbwheel switches. Rapid setting for rapid reading. With large, clear symbols for improved accuracy.

Digitran switches read great. Look great. And save you up to 50% in panel space. Digitran switches make your product look better, sell better. And modular design lets you use any number of digits.

Digitran switches are easy to use,

and we make them easier to use: As the world's largest, most experienced thumbwheel switch manufacturer, we have more application experience than anyone else. We can save you hours of design time.

Send for our complete catalog.

We'll speed it to you.

THE DIGITRAN COMPANY
 Subsidiary of Becton, Dickinson and Company [BD]
 855 S. Arroyo Pkwy./Pasadena, Cal. 91105
 Tel: (213) 449-3110/TWX 910-588-3794

CIRCLE NO. 36 ON INQUIRY CARD

set modification much later in the design cycle than for conventional machines, to allow optimization of the computer for an evolving problem.

Microprogrammed computers provide the control system engineer with a means of including macro instructions, which are application-oriented instructions of considerable complexity. In conventional computers, the complexity of individual instructions is limited by the amount of hardware required to implement the control sequence, and if the hardware cost (including effects on reliability, weight, volume, and power in addition to dollar value) is high in relation to total use for all applications of the same hardware, specialized instructions are not included. Macro instructions, on the other hand, may be changed for each application without affecting the hardware logic design, and thus the incremental cost of each macro can be examined separately for each application. Typical macros include:

- Register operations: extended precision arithmetic, square root, and trigonometric functions.
- Storage operations: data correla-

tion and matrix manipulation.

Any high-usage subroutine may be coded as one or more macro instruction. A strong parallel exists between subroutines in conventional programming and macros executed under microprogram control. In conventional programming, an entire function may be performed by a single subroutine, or a series of shorter more general subroutines may be linked together with conventional instructions to obtain the same result. Microprogrammed macros may also include entire functions or may consist of shorter more general functions interspersed with conventional instructions. Similar functions performed by microprogrammed sequences and conventional subroutines differ in a number of respects:

- Instruction fetch references to main storage are eliminated after entering the macro.
- Intermediate macro results are stored in hardware data flow registers or fast access scratch pad storage to eliminate many references to slower main storage; redundant LOAD and STORE operations are eliminated.

TABLE 1

PROCESSOR CHARACTERISTICS SUMMARY FOR SQUARE ROOT EXAMPLE

Storage Cycle	
Read 32 bits	2.5 μ s
Write 32 bits	3.33 μ s
Logic cycle	416.6 ns
Data flow width	16 bits
Operand length	32 bits, fixed point, fractional
Typical Instruction Execution	
Load 32 bits	5.0 μ s
Store 32 bits	5.83 μ s
Add 32 bits	5.0 μ s
Divide 32 bits	46.67 μ s

- Macros have full access to processor registers and data paths and are not limited by the instruction set.

- Macros substitute machine cycles for longer main storage cycles to obtain short constants or logical masks.

As an example, assume a square root function, $y = \sqrt{x}$, with the argument is 32 bits, and the results for y obtained with both 16- and 32-bit precision. A single address instruction format is assumed. The processor characteristics are summarized in Table 1. The subroutine employs the Newton-Raphson method and includes initial scaling to ensure rapid convergence. The micro-routine uses a one-bit-at-a-time algorithm similar to a conventional pencil-and-paper square root solution.

The results of this example are summarized in Table 2. The improvement obtained by microprogramming the square root function when compared with a program subroutine is 8 to 1 for a 16-bit result and 4.75 to 1 for a 32-bit result. This agrees well with other known comparisons in which performance improvement ranged between 3 and 15 to 1.

The results are very dependent upon the main storage cycle time assumed. However, independent of storage cycle time, the example illustrates the following characteristics of macro instructions:

- Instruction fetch cycles are eliminated.
- Operand store and read cycles are reduced or eliminated.
- Macros have full access to processor facilities to use the most efficient algorithm available and are not restricted to the instruction set capabilities (therefore square root iterations were substituted for shifting and division cycles).

In addition to instruction set and macro modification, microprogram control provides a convenient method

of customizing system features not directly a part of the instruction set. Included in this category are:

- Input/output control
- Initial program load bootstrap routines
- System initialization
- Interrupt recognition and control
- Power transient shutdown and recovery
- Self-test and self-diagnosis aids.

As an example, consider micro-programmed input/output control for a small computer. Only a small amount of interface circuitry need be specific to the channel: the parallel input and output data buses and a number of input and output control lines. The main computer data flow and micro-programmed control unit can be time-shared between the processor and the channel function. When data service is required for a peripheral device, the processor function is pre-empted. The data flow is seized, temporarily stored, used for channel service, and then restored. Although the maximum data rate attainable is lower (and interference with computation higher) than with separate input/output hardware, the function is identical.⁴

Once the channel becomes a conceptual entity, using time-shared hardware, one may have a large number of channels at virtually no cost save the core storage space for the governing control words.⁴ Such multiplexing is very significant for control or communication-based systems. Similarly, additional modes of channel operation can be obtained for the cost of additional micro-program storage. These modes include single word data transfer to augment block input/output, control sequences for an external interrupt system, and control of special peripheral devices.

The microprogram can also be used to translate architectural features to input/output interface sequences so that:

- The use of standard peripheral devices is independent of the instruction set and other architectural features.
- Standard instruction sets can be used with a wide variety of peripheral devices having different characteristics. Provision of complex input/output channel facilities architecturally compatible with larger computers is thus possible.

Table II

Parameter		Subroutine		Microroutine	
		16 bits	32 bits	16 bits	32 bits
COMPARISON OF SUBROUTINE AND MICROROUTINE SQUARE ROOT					
Storage Cycles					
	Instruction read	56.5	66.6	1	1
	Operand read	19	23	0	0
	Operand store	11	13	0	0
Execution Time (μ s)					
	Instruction read at 2.5 μ s	141.25	166.25	2.5	2.5
	Operand read at 2.5 μ s	47.50	57.50	0.0	0.0
	Operand store at 3.33 μ s	36.63	43.29	0.0	0.0
	Divide iterations at 44.17 μ s	132.51	176.68	-	-
	Shifting	47.46	51.61	-	-
	Square root iterations	-	-	37.5	100.0
	Overhead	4.17	4.17	2.08	2.5
	Total μ s	409.52	499.50	51.25	105.0
Execution Time Ratio (Subroutine/Microroutine)					
	16-bit result	8:1			
	32-bit result	4.75:1			

Systems Implications

The systems implications of micro-programmed control are primarily related to the characteristic ease with which specialization and simulation can be achieved, and to overall cost. Specialization — the incorporation of special instructions, macro-operations, and computer facilities for a particular application or class of applications — consists of augmenting and modifying given characteristics. By contrast, simulation is the execution of programs originally written for another computer. Specialization and simulation are not incompatible, and in some applications they are complementary.

One particularly important class of applications for which computer specialization via microprogramming can be anticipated is real-time systems. This class encompasses such diverse applications as: process control, command and control, navigation and guidance, message switching, fire control, reconnaissance and surveillance, time-sharing, and image processing. In these, and many other applications, the computer systems are on-line all or a significant portion of the operating time, and a very significant portion of the processing time is devoted to a few specialized tasks, such as code conversion, interrupt processing, polling,

and function generation. For such applications, a wide variation in performance will occur even among conventional computers having comparable ADD execution times, as a direct result of differences in instruction sets and overall architecture.

Computers specifically designed for real-time applications can be expected to outperform those primarily intended for off-line data processing and scientific calculation. Even so, a significant additional performance increase is obtained when computer characteristics can be specialized for a particular application, or for a small class of applications, rather than for real-time applications in general. One approach is to generate macro instructions as previously described. With microprogrammed control, it is also possible to alter the division of tasks between the central computer, the input/output channels, and peripheral equipment. Thus the decision of whether to perform a particular operation within the processor or devise a new peripheral device can more frequently be decided in favor of the former.

In the above discussion it has tacitly been assumed that the intended application was well-defined. There are, however, many important applications for which the system cannot be well defined *a priori*. In

some programs, the computational load is not completely defined during the initial program phase, and in others the computational requirements change during the development phase. In still other applications, system characteristics and emphasis change as a function of time; for a space program, for example, requirements may change significantly from mission-to-mission. In process control or message switching, requirements can change as a function of time due either to process and system modification or growth. The ease with which the computer architecture can be restructured via microprogramming can thus become a significant consideration for such systems.

A facility for microprogrammed simulation is inherent in microprogrammed control. This makes possible the use of special microprograms designed to provide program compatibility with other computers. Microprogram simulators are conceptually similar to the interpretative routine simulators sometimes used on conventionally-controlled computers. They differ in that for interpretative routine simulators each instruction is simulated by a sequence of instructions at execution time. With the micro-programmed simulator many, if not all, of the instructions required in an interpretative routine simulator are replaced by microprogrammed operations. The resulting performance improvement is analogous to that obtained in using macro instructions in place of sub-routines.

With microprogram simulation, as with any form of simulation or program conversion, the actual program execution time and storage efficiency are very sensitive to differences in overall computer structure. Consequently, significant differences in word length, number representation, and addressing techniques can result in unsatisfactory overall performance. One of the primary limitations inherent in microprogrammed simulation of another computer is in the handling of the input/output interface, interrupts, and the operator's console. Unless there exists a natural correspondence between these facilities, simulation is at best extremely difficult and frequently impossible.

The compatibility afforded by microprogram simulation of another

computer is frequently of benefit as an interim solution when one system is replaced by another, permitting a large portion of the old programs to run on the new system.

Problem language microprogram simulation, wherein simulation is restricted to those instructions associated with arithmetic and logical operations, affords a compromise to total simulation for systems where there is no natural correspondence between interfaces and facilities. When necessary, special macro instructions can be included in the problem instruction set. Input/output instructions, the handling of interrupts, interfacing with the operator's console, and other non-arithmetic operations are tailored to the available peripheral equipment and other system constraints.

Problem language simulation is particularly attractive for real-time systems. First, it provides a high degree of program compatibility. Compilers, problem programs and subroutines will run on the microprogrammed machine with no modifications; assemblers require only relatively minor modification; and in many cases control programs can be adapted with significantly less effort than would be required to develop an entirely new system. Finally, those facilities that cannot readily be simulated, i.e., the interrupt system, console operations, and input/output, correspond exactly to those features that distinguish a real-time system from an off-line system. Therefore, it can be seen that for many real-time applications those primary features of off-line systems that are most difficult to simulate are the least desirable to simulate.

For a specific system application, the cost of a microprogram-controlled computer by itself may or may not be less than that of an alternative computer. However, the system engineer's freedom to modify computer characteristics without major hardware redesign and his ability to extend system life by microprogram changes may lower overall system cost, which includes the cost of the computer, its peripheral devices, other system components, software, operating costs, and any costs assigned to intangibles.

Finally, microprogram control may reduce the lead time normally associated with the development and delivery of conventional computers.

If we assume an existing hardware logic design, the relatively short time required for microprogramming, compared with logic design, may materially hasten computer delivery.

Conclusions

The architecture of microprogram-controlled computers can be varied over a wide range by modifications of, or additions to, microprogram storage. This unique characteristic can be used in many system applications where it provides a more optimum system than would otherwise be possible. It has been shown qualitatively that:

- A microprogrammed computer organization is well suited to applications where very specialized operations and routines require a significant percentage of total execution time. This permits computer optimization through addition of application-dependent instructions.
- The ease with which computer architecture can be restructured via microprogramming is a significant consideration in applications where system problems are not completely defined during initial program phases, requirements change during the development phase, and where system characteristics and emphasis change as a function of time.
- The unique capability for efficient simulation inherent in microprogrammed computers permits a significant reduction in development time and overall cost in many applications.

A significant problem associated with system restructuring via microprogram control is its effect on software support. Implementation of significantly different instruction sets or instruction formats may require different software support programs for each programming language. Addition of application-oriented macro instructions is strongly influenced by the facilities available to define new operations to the software at assembly or compilation time.

REFERENCES:

1. M. V. Wilkes, "The Best Way to Design an Automatic Calculating Machine," *Manchester University Inaugural Conf.*, Manchester, England, p. 16-18, July 1951.
2. M. V. Wilkes and J. B. Stringer, "Microprogramming and the Design of the Control Circuits in an Electronic Digital Computer," *Proc. Camb. Phil. Soc.*, Vol. 49, pt 2, p. 230-238; April 1953.
3. D. M. Taub, "A Short Review of Read-Only Memories," *Proc. I.E.E.*, Vol. 110, p. 157-162, January 1963.
4. G. M. Amdahl, G. A. Blaauw, and F. P. Brooks, Jr., "Architecture of the IBM System/360," *IBM Journal of Research and Development*, Vol. 8, No. 2, p. 87-97, April 1964.

I/O REQUIREMENTS FOR PROCESS CONTROL COMPUTERS

L. Templeton, Section Manager,
Industrial Control Systems,
Computer Control Division,
Honeywell, Inc., Framingham, Mass.

A brief look at the state-of-the-art in interfacing process control computers.

Many people in the process industries have the mistaken impression that the installation of a process control computer automatically obsoletes instrumentation that has been used with conventional control systems. Sometimes this is indeed the case, but frequently it is not. Computer engineers have done a superb job of adapting computer hardware to standard instruments and control devices.

To be sure, a computer requires an electrical input, and thus is superficially incompatible with an all-pneumatic system. In cases where a large investment in reliable accurate pneumatic instrumentation exists in a plant, it is usually cheaper to convert pneumatic signals to electrical signals in the control room with P/I transducers. This approach eliminates the necessity of field wiring. If good dc electronic transmitters and wiring exist in the plant, the installation cost of the computer system is substantially reduced below that for pneumatic instruments since an inexpensive I/V resistor may serve to condition the input signal properly. Thus, there are convenient ways of interfacing existing instrumentation with computers even in cases where incompatibility seemingly exists.

Fundamentally, there are only four types of computer input and output systems: (1) analog input; (2) analog output; (3) digital input; and (4) digital output. Of these, by far the most important — because it provides the basic measuring capability of the system — is the analog input signal.

Analog Input Devices

Perhaps up to 40% of the analog inputs to all process control comput-

ers are from pressure-to-current P/I transducers. These devices, of which fluid flow meters are a typical example, provide a high-level signal within the 5 to 10 volt range (with a suitable I/V resistor), and frequently have a large common mode voltage associated with them, since other instruments may be in the current loop (Fig. 1). The normal maximum frequency of response is on the order of one to two cycles per second or less, and the signal generally falls within one of the following ranges: 1 to 5 milliamperes, 4 to 20 milliamperes, or 10 to 50 milliamperes.

Since the signal from a P/I transducer is relatively clean and high level, with a high signal-to-noise ratio, there is no real necessity for special filters in the system. The need for a differential input is indicated because of the presence of large common mode voltages in certain instances, and multiplexing is, of course, necessary to sample the large number of points that are encountered in most process control applications. Otherwise, the signals from most pressure-to-current transducers present no real technical difficulty.

Another common type of analog input device is the thermocouple — iron constantin, chromel-constantin, or aluminum-constantin. These are inexpensive, relatively sensitive, are usable to 3000°F, and have accuracies approaching 1°F. They provide signals in the 0 to 50 millivolt range, but because the control limits are usually more restricted, the usable signal is generally from 5 to 10 millivolts. Generally, the bandwidth of the signal doesn't extend above 1 cps, and usually is within 0.1 to 0.01 cps, so good (second order) filtering can be employed.

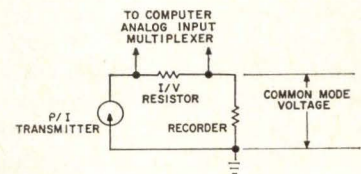


Fig. 1 — The differential flow meter is a typical analog input frequently encountered in the process industries.

Since thermocouples are often grouped in several locations, the input signals also tend to come in groups or batches. These are the most difficult common signal sources to handle. Further, the thermocouples are often grounded at the point of measurement, which means that the computer should have very high common mode rejection to minimize ground loop currents which tend to produce normal mode noise because of lead imbalance. The C. M. R. objective should be to stay above 120 db at 60 cycles and 140 db at dc. For computer inputs, it is generally good practice to twist thermocouple lead wires, although in many environments untwisted wires, shielded by conduit and conditioned with filter circuits, yield satisfactory results.

To compensate for the undesired thermocouple effect when terminating T/C lead wires at the computer, an iso-thermal reference box must be employed. This can be a simple enclosure that, although varying with ambient temperature, maintains a uniform temperature *within* the enclosure. A temperature measuring device which may be read by the computer is included in order that the reference temperature may be calculated (Fig. 2). Another solution, although generally more expensive, is to provide an enclosure which is thermostatically-controlled at a

known temperature — usually elevated (hot junction compensation).

If the user employs a low impedance device such as a multipoint recorder in his system, it may be necessary to duplicate the thermocouple and the wiring in order to achieve satisfactory control. An alternate solution is to use a high impedance amplifier on the recorder or auxiliary device. Otherwise, sharing of the signal can lead to spurious results.

Beyond these rather ordinary problems, there is no real difficulty in interfacing thermocouple devices with computers. Since a considered estimate is that another 30% to 40% of the inputs to process control computers is from such devices, the designer is obviously well advised to satisfy the signal requirements from these and P/I transducers in his basic circuits, and to make special provisions for all other inputs as the situations occur.

When the operating temperatures are below 32°F and fast response to change is unimportant, a resistance bulb thermometer can be used in a bridge circuit. This may entail either a common bridge for multiple inputs, or a bridge completion network per point. The resulting signal is in the 0 to 1 volt range; providing reasonably good signal-to-noise ratio; and requires a frequency response of 1/100 to 1 cycle per second. Filtering is generally unnecessary.

When incorporated in a variable reluctance differential transformer, strain gage transducers can be used to indicate position or pressure and provide a signal of 0 to 1 volt. When used to indicate strain, they are incorporated into bridge type circuits to provide a differential output, typically in the range of 5 to 10 mv. While they may be valuable in many applications, they are not too common in the process industries.

Analytical-type devices, of which mass spectrometers and chromato-

graphs are example, are required for a relatively small percentage of process control applications, and not all computer manufacturers have developed standardized means of handling the inputs. The basic design problems encountered are wide dynamic signal range (1 mv to 10 volts), relatively high sampling rates (up to several hundred samples per second), and synchronization with the device itself usually on an interrupt basis. These requirements are satisfied by the present state-of-the-art and only the relatively low incidence and the rather individualistic nature of this type of device has retarded the widespread development within the industry of standardized hardware and software to handle this type of signal. For economic reasons, many suppliers have chosen to interface these devices as the need arises on a special basis for each application.

Multiplexing

With the large number of points that are monitored in the average computer control system, a reliable means must be employed to multiplex the signals. Reliability is generally more important than speed. With the exception of signals from analytical instruments, analog input devices generally need not be sampled more than 5 to 10 times per second. In total, the average input frequency is on the order of 100 to 200 points per second, and while this will probably grow to from 250 to 300 points per second in the next few years, no radical increases are anticipated. Since most changes in the process industries are evolutionary rather than revolutionary, the computer requirements of today are not likely to become obsolete overnight.

It is advisable to provide some means of fault isolation so that miswiring in the field or sudden surges do not damage the computer. For example, the computer manufacturer might provide Zener diode clipping on a group basis to sense overload voltage and isolate the computer circuits from the system (Fig. 3). While this concept is costly and frequently difficult to sell to the customer, it is far less expensive than major damage to the computer and any resultant process "downtime."

The reliability of the devices that

are commonly employed for multiplexing is very high. Mercury relays, for example, have a life expectancy of 10^9 actuations or better, and reed relays — another popular type — are almost as good. In fact, as far as reliability is concerned, it is yet to be proven that solid state, field effect devices will be significantly better. Reed and mercury relays permit transfer accuracies of 0.1% or better on millivolt signals, generally a requirement in process control computer systems. They can withstand large common mode voltages, and several techniques, such as the capacitor transfer method, have been developed to permit very high common mode rejection ratios and the ability to withstand large common mode voltages (150-200 volts).

It may very well be true that field effect switches will obsolete relays by the time another few years have passed. Their use will probably be dictated by speed and cost factors rather than reliability. However, significant obstacles still must be overcome. For one thing, their cost, which is now approximately twice that of the more conventional multiplexer devices, will have to be substantially reduced. For another, some means must be developed of improving their signal resolution and accuracy on millivolt ranges. In contrast, relays can easily resolve signals in the 2 to 3 microvolt range.

Analog Output

In DDC applications, analog outputs are generally used to position valves and stepping motors. In the first instance, this requires a signal output in one of the following ranges to drive the valves: 1 to 5 ma, 4 to 20 ma, or 10 to 50 ma. For driving a stepping motor, a voltage output is desirable, and some means must be developed of interfacing these motors with the computer.

In supervisory applications, where it is necessary to provide output to

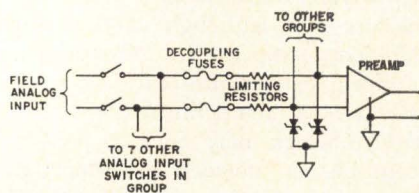


Fig. 2 — When the input is from a thermocouple, an isothermal reference box must be employed. This can be either thermostatically controlled or vary with ambient temperature.

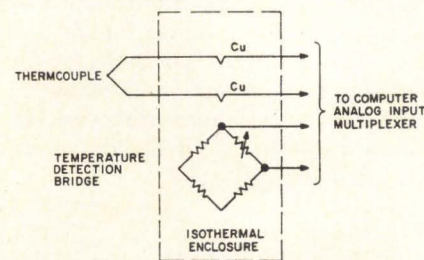


Fig. 3 — Fault isolation circuitry eliminates damage to time-shared portion of system.

instruments or a setpoint to a controller, voltage outputs are generally desirable. However, in many instances, a current output will satisfy an instrument requirement, and the current output to a positioning valve can also provide controller setpoints.

As was recommended for multiplexing circuits, isolation of the output sub-systems from the computer is recommended; this prevents field faults from getting back into the time-shared portion of the system. In addition, battery back-up may be provided to hold power to the load for from 30 minutes to an hour, should the primary system power source be interrupted.

Digital Input

To monitor limit switches, counters, relays and other devices that are commonly employed in process applications, it is necessary to have live voltage and contact sense input capabilities. Additionally, an edge sensitive device that will sense a changing state from open to closed, or vice versa, and interrupt the computer, will greatly enhance the over-all efficiency of the system. Console keyboard pushbuttons are effectively interfaced with the latter type device. In these cases, service requests are generally asynchronous with the system and a premium is placed upon system response time.

Digital Output

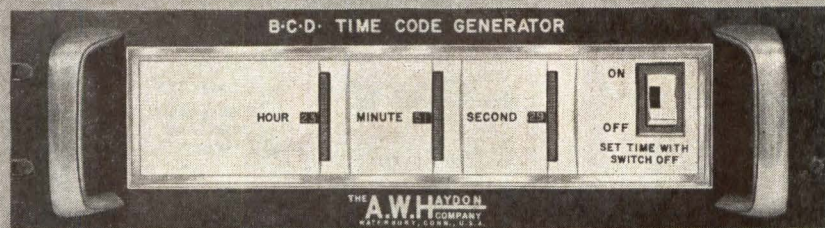
There are two possible variations of digital output, and two types of devices that can be used to achieve the desired results: a pulsed output that provides pulses of predetermined duration; and a memory flip-flop that can be used to pull in relays, light lights, or do other simple tasks. Either solid state or relay devices can be used.

Neither digital input nor output application requirements are likely to change much in the next few years, and the same techniques that are utilized to interface with these devices will probably be used with the machines that are available 3 or 4 years hence.

The Future

Emphasis in the future will probably be toward improving reliability, reducing costs through integrated circuit technology and the utilization of more remote multiplexing to reduce wiring runs and improve signal-to-noise ratio.

**Can you take advantage
of this cost breakthrough in
time code generators?**



**If you're paying for exotic levels
of precision you don't really need
and can't use, this remarkable new
electromechanical unit may cut
your costs in half!**

Here's a precision electromechanical time code generator specifically designed to fill many applications at about half the cost of comparable electronic units!

If you've had to buy costly code generators with fancy specifications because nothing else fit your application, this new development can save you real money. It's designed around standard A. W. Haydon Company components and on a modular basis that allows us to customize it to your exact requirements. The time base is established by a synchronous motor-driven repeat cycle timer which rapidly steps a preset code pattern of output switches. Standard output codes available are straight decimal or binary coded decimal.

Typical applications include computers, data handling system, illuminated time displays, direct printout devices, checkout equipment, telemetry systems, and tape punching devices. These units should be carefully considered for any commercial/industrial equipment requiring a time code. This versatile instrument can be arranged to supply readings in days, hours, minutes, and seconds. It can be used as a master clock to drive slave units. It can be custom adapted to handle special codes. Code output is displayed on the front panel, and setting is by convenient knurled wheels. Standard models are available with time outputs from 59 minutes, 59 seconds, to 369 days, 23 hours, 59 minutes, 59 seconds. Panel fits standard 19" racks. Electrical requirement is 105-125 VAC, 58-62 CPS. Send for further information.

AWH HAYDON
THE COMPANY

232 NORTH ELM ST., WATERBURY, CONN. 06720
Tel: 203-756-4481 TWX: 203-753-3179

4060 INCE BLVD., CULVER CITY, CALIF. 90231
Tel: 213-Upton 0-5461 TWX: 213-836-0444

REPRESENTATIVES THROUGHOUT THE U.S. (SEE EEM). IN EUROPE CONTACT POLYMOTOR, BRUSSELS.

Timing & Stepper Motors • Electromechanical & Electronic Timing Devices & Systems

CIRCLE NO. 37 ON INQUIRY CARD

negative radix arithmetic

Part 7



Division Concluded

M. P. de Regt



One way of taking as much of the mystery and difficulty as possible out of the process of negative radix division is to show how every step in it has a corresponding step in normal division. Many of these corresponding steps are so familiar to us that they have long since stopped being explicit steps. Therefore, the process of making negative radix division less mysterious has entailed making positive radix division seem more difficult and complex.

The reason for persisting in the apparently pure intellectual exercise of developing a manual method is that understanding of negative radix division is not achieved by the development of a single algorithm suitable for machines. Understanding is achieved, if we can successfully divide as human beings, rather than as desk calculators. Such understanding will then provide the basis for design of many machine algorithms so that one can be selected to suit specific general design objectives.

Because negative radix division turns out to be naturally non-restoring, we have had to develop detailed flow charts for both nonrestoring and restoring division so that we could show correspondence between steps. Figure 1 of Part 6, illustrates this correspondence applied to mechanical algorithms — that is, those which use repeated addition or subtraction of a weighted divisor. A further matter considered in Part 6 was the adjustment of the final remainder and quotient for proper division in which

the remainder, if non-zero, is of the same polarity as the original dividend.

In this final article on division, we shall consider the remaining steps and conventions for manual division. They are:

- Use of subtraction only for the diminishing operation.
- Generation of individual quotient digits.
- Use of the divisor as the diminishing operand.
- Estimating the quotient digit.
- Determining the position of the initial quotient digit.

Use of Subtraction and Generating Quotient Digits

The first simplifications to the general flow charts of Fig. 1 of Part 6 which we shall adopt are the use of subtraction only as the diminishing operation, and the generation of individual quotient digits in place of performing arithmetic on the entire quotient. Therefore, instead of using the weighting factor $(-1)^k$ (r^i) on the entire quotient, we use $(-1)^k$ on only the current quotient digit. If k is constant, it can be -1 , 0 , or $+1$; if it alternates between odd and even, it can be i or $i \pm 1$. Since we wish both to simplify and to be "natural", as in normal manual division, we shall assume that for non-restoring division $k = 1$ for negaradix and i for posiradix, and for restoring $k = i + j$ for negaradix and j for posiradix where j is 0 or 1 depending on whether the

quotient is positive or negative.

The above assumptions, when combined with subtraction as the constant diminishing operation, result in the mechanical algorithms illustrated in Figures 1 (a) and 1 (b) for non-restoring and restoring division, respectively. These charts may be compared block by block with Figs. 1 (a) and 1 (b) of Part 6; the block numbers and geometry correspond.

Note that the outside dotted lines for alternating operations have been removed, and a minus sign is used in lieu of the compound sign for calculating ID in block 4. (In Fig. 1, part 6, the second line of Block 4 should read "NEW ID = ID \mp WD;" not \pm .) In block 2 (a) and 2 (b), $(-R)^i$ and $(-1)^j R^i$ substitute for the more general $(-1)^k r^i$ because in:

- negaradix non-restoring, $k=0$, $r=-R$;
- posiradix non-restoring, $k=i$, $r=+R$;
- negaradix restoring, $k=i+j$, $r=-R$;
- posiradix restoring, $k=j$, $r=+R$.

These values for k are given in Table 1 (combined with Fig. 1).

Note that use of a positive radix in Fig. 1 (a) and a negative radix in Fig. 1 (b) will result in quotients expressed in special decimal and special negadecimal, respectively (see Part 1). In these special systems, it will be remembered, the digits in alternate positions are negative. Figure 1 thus illustrates the

many fascinating ways in which positive radix and negative radix, special systems, and non-restoring and restoring division are related. These relations are illustrated in the following examples in which negadecimal is on the left, and decimal on the right.

Example 1. Divide 23536 (+17476) by 23 (-17), using the complete non-restoring mechanical algorithm.

Pass $i = 3$

Interim Dividend	q_i	Interim Dividend	q_i
23536		+17476	
23000	1	-17000	-1
536		+476	

Pass $i=3$ ends at this point, since 536 (+476) is less than one-eleventh of the weighted divisor magnitude, $-1545 \frac{5}{11}$. Hence $q_3 = 1 (\bar{1})$, $q_2 = 0$, and pass $i = 1$ is next.

Pass $i = 1$

Interim Dividend	q_i	Interim Dividend	q_i
536		+476	
230	1	-170	-1
306		+306	
230	2	-170	-2
276		+136	
230	3	-170	-3
46		-34	

Pass 1 ends at this point, because of the polarity change. The test magnitude was $-15 \frac{5}{11}$, which is obviously much less than +136. The next quotient digit, q_1 , is 3 ($\bar{3}$).

Pass $i = 0$

46		-34	
23	1	-17	+1
23		-17	
23	2	-17	+2
0		0	

The quotient digit, q_0 , is 2.

The final quotient is 1032 (+1032). The +1032 in special decimal is easily converted: +0002 + 1030 = 2 -1030 = -1028, which is the answer we would have obtained by performing arithmetic directly upon the weighting factor for each operation.

The reader can demonstrate the algorithm for both negadecimal and decimal by dividing 1,000,000 (+1,000,000) by 191 (+11). If this exercise is repeated for the non-restoring algorithm using only the

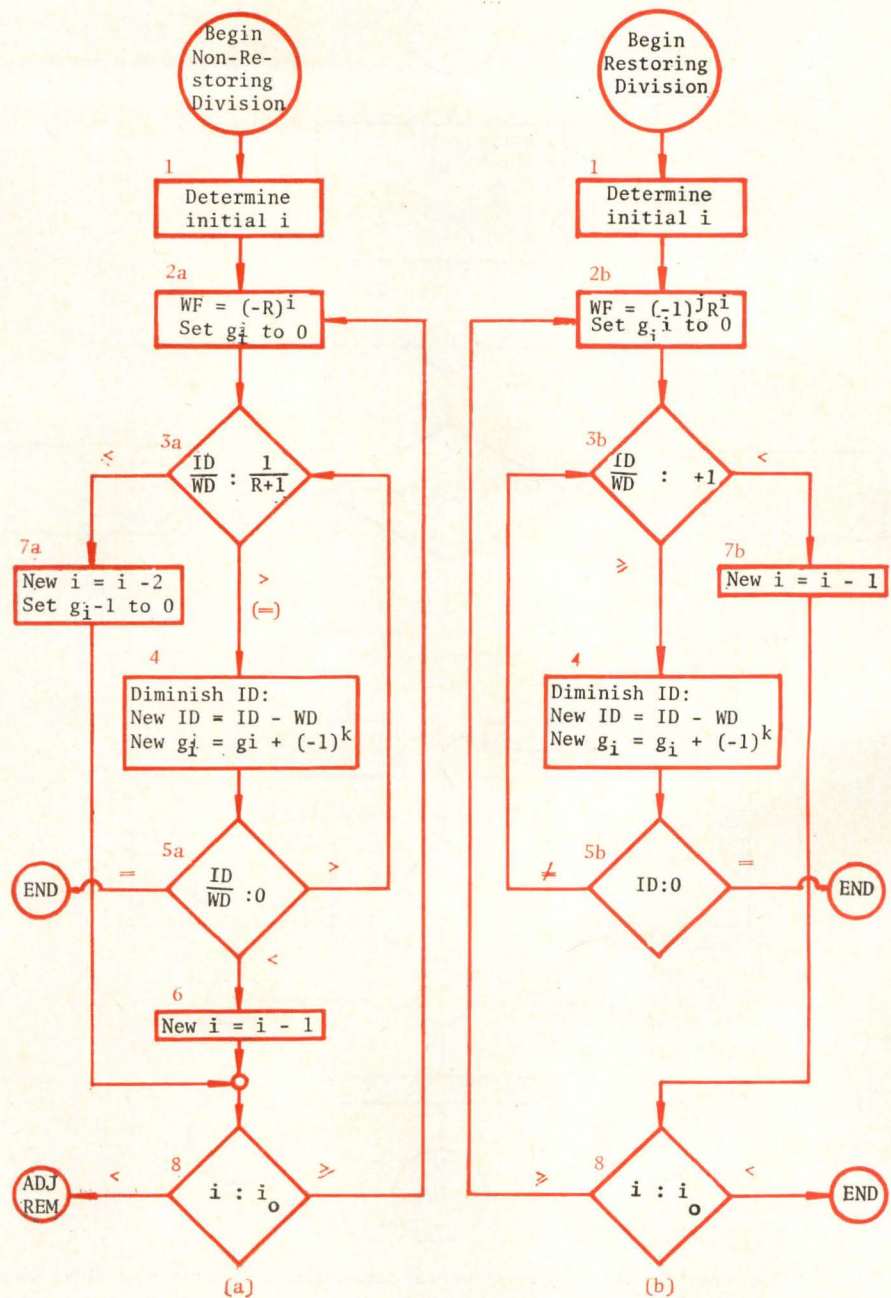


Table 1. The values for k and $(-1)^k$

Division:	Non-Restoring		Restoring		
	Neg.	Pos.	Neg.	Pos.	
k :	0	i	$i+j$	j	A/D
$(-1)^k$:	+1	$(-1)^i$	$(-1)^i$	+1	Pos. ($j=0$)
			$(-1)^{i+1}$	-1	Neg. ($j=1$)

Fig. 1—Flow chart for mechanical division using the magnitude test. See Table 1 for values of $(-1)^k$, the coefficient of r^i in the weighting factor.

polarity test, it will be observed that a string of "tens" is generated; that is, the q_i are all 190 in negadecimal, and alternates between +10 and

-10 in decimal. Thus, a string of tens is the equal of a string of nine/zero pairs. The results of this division are illustrated in Table 2.

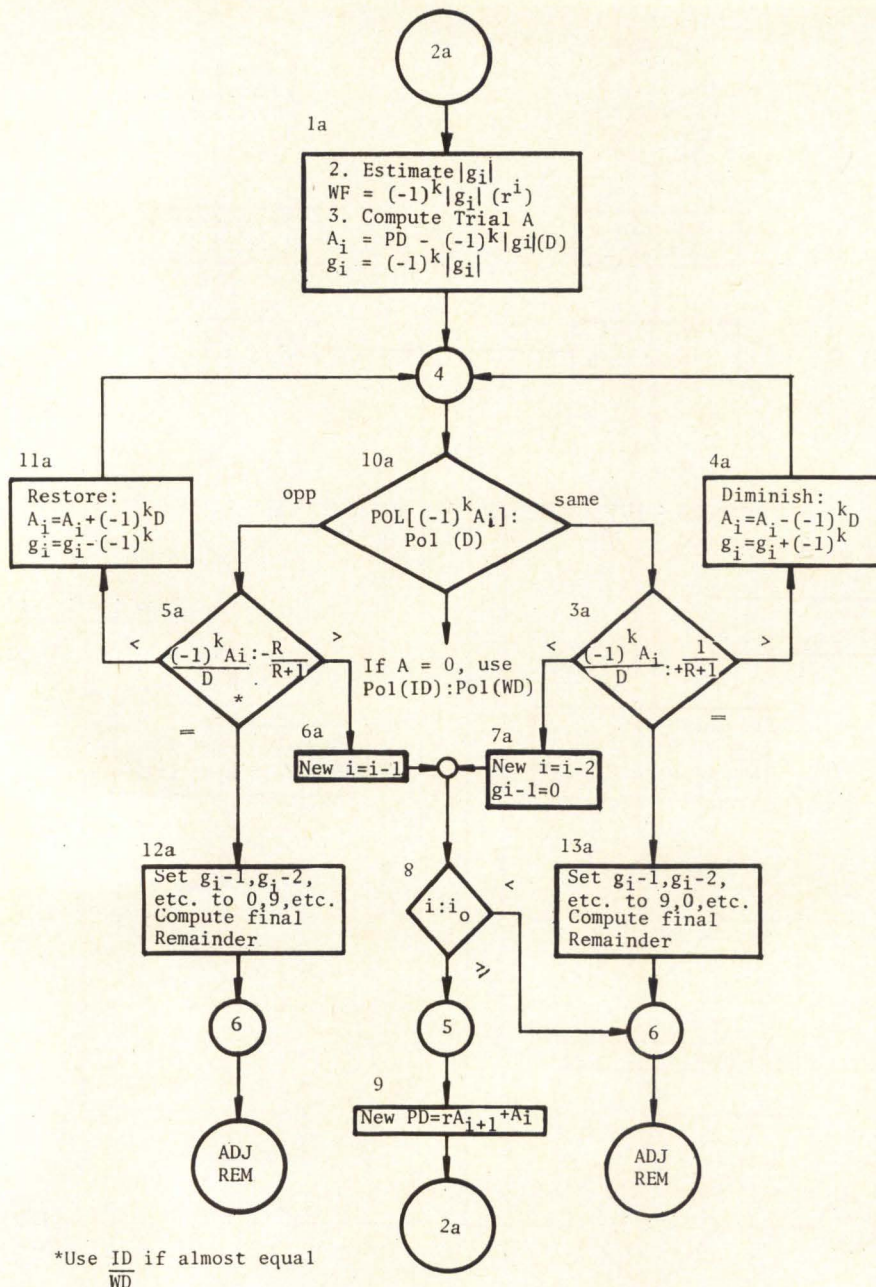


Fig. 2—Flow chart for the complete manual non-restoring division algorithm. Use $k = 0$ for negaradix and $k = i$ for posiradix.

limiting value of unity; similarly, the special negadecimal string of $0.\overline{9999} \dots$ arising from the division of

two nearly equal very large numbers using the negadecimal restoring algorithm has a limiting value of $0.\overline{9090} \dots + 0.0909 \dots$, or $-(-10/11) + (+1/11)$, which equals unity.

In a negabinary computer, the magnitude test would comprise a comparison of the magnitude of the interim dividend with one-third of the weighted divisor. Not only would one-third of the divisor have to be computed, but the comparing operation would have to be performed after every diminishing operation, which would double the number of operations and complicate both the arithmetic and the control hardware. Thus, for negabinary machine divi-

sion, the straight polarity-test, non-restoring algorithm might well be better than one which includes a magnitude test. For the worst possible case — computing $1,000,000 \div 111 = 10101 \dots$, using only the polarity test, we would have two operations for each position (see Table 2). With the magnitude test, we would have one diminishing operation plus three magnitude operations for each pair of positions, or also an average of two operations per position.

The Divisor as the Diminishing Operation

So far, all the flow charts have used a weighted divisor to diminish the full remaining or interim dividend. Both people and machines typically use the divisor on a high-order portion of the interim dividend. It is therefore necessary to make appropriate changes to the flow charts. At the same time, the procedure for generating individual quotient digits will be substituted for the procedure for modifying the entire quotient.

Although these changes are simple ones, they must nevertheless be made with care to preserve polarity values, and they must be accomplished on four algorithms rather than on one algorithm. The four algorithms are the non-restoring and restoring algorithms applied to both negative and positive radix systems, all of which we need to continue our practice of providing examples in both positive and negative radix versions.

In Block 2 of Figs. 1(a) and 1(b) the weighting factor is chosen so that subtraction may be used as the diminishing operation in all passes. The formal procedure for doing this is discussed later. By definition, therefore, the interim dividend (ID) and the weighted divisor (WD) will always have the same polarity with our present assumptions. This fact is reflected in the absence of signs in Blocks 3(a) and 3(b).

To use the divisor (D) as the diminishing operand, we note that the polarity is, of course, constant. In restoring division, the polarity of PD remains the same as that of the divisor, A, by definition, and in negaradix non-restoring, it remains the same, since the brought-down divisor digit at the end of each pass restores the polarity of the remainder, A_i , to

TABLE 2						
RESULTS OF NON-RESTORING DIVISION						
(+1,000,000 ÷ +11)						
	q_1	q_0	q_1	q_0	Rem.	
Magnitude Test						
Negadecimal	9	0	9	0	9	1
Decimal	+9	0	+9	0	+9	+1
Polarity Test Only						
Negadecimal	190	190	190	190	190	10
Decimal	+10	-10	+10	-10	+10	-10

what it was just before the final polarity-changing diminishing operation. In posiradix non-restoring, however, the PD changes polarity at each pass.

In Figs. 1(a) and 1(b), we can therefore use PD instead of ID at the beginning of each pass, and A_i instead of ID after each diminishing operation. We can also substitute D for WD, except for posiradix non-restoring, where D must be prefixed with $(-1)^i$. In the case of restoring division, although PD and D each have constant polarities, the polarities of A and D, and therefore of PD and D, may be opposite. In Fig. 1(b), PD or A_i may be substituted for ID, but $(-1)^j D$ must be substituted for D.

Referring to block 5a, the separate “=” branch to “END” must be eliminated and the “=” combined with the “>” branch, because of the possibility that a PD of zero might indicate a very small but non-zero ID. For the same reason, block 5b must be completely eliminated, and block 4 connected directly to block 3b.

A separate flow chart for these changes is not given; however, they are reflected in the corresponding blocks of the flow charts of Figs. 2 and 3.

Estimating The Quotient Digit

Still assuming that the location of the most significant quotient digit has been correctly established, block 1 of Fig. 1, we shall proceed now to make the last step in the transition from the primitive counting algorithm to the complete manual algorithm. This step substitutes estimating the quotient digit, and adjusting the estimate either up or down, for tallying or counting each quotient digit using single diminishing operations.

Several interesting and arbitrary matters about the quotient digit should be emphasized at this point. First of all, it is clear from Table 1 that the quotient increment $(-1)^k$ is always positive only for negaradix non-restoring division. The polarity alternates between even and odd positions for posiradix non-restoring, meaning that the quotient (for $R = 10$) will be expressed in the “special decimal” explained in Part 1. In negaradix restoring division, the polarity alternates for successive positions, but with the negative digits

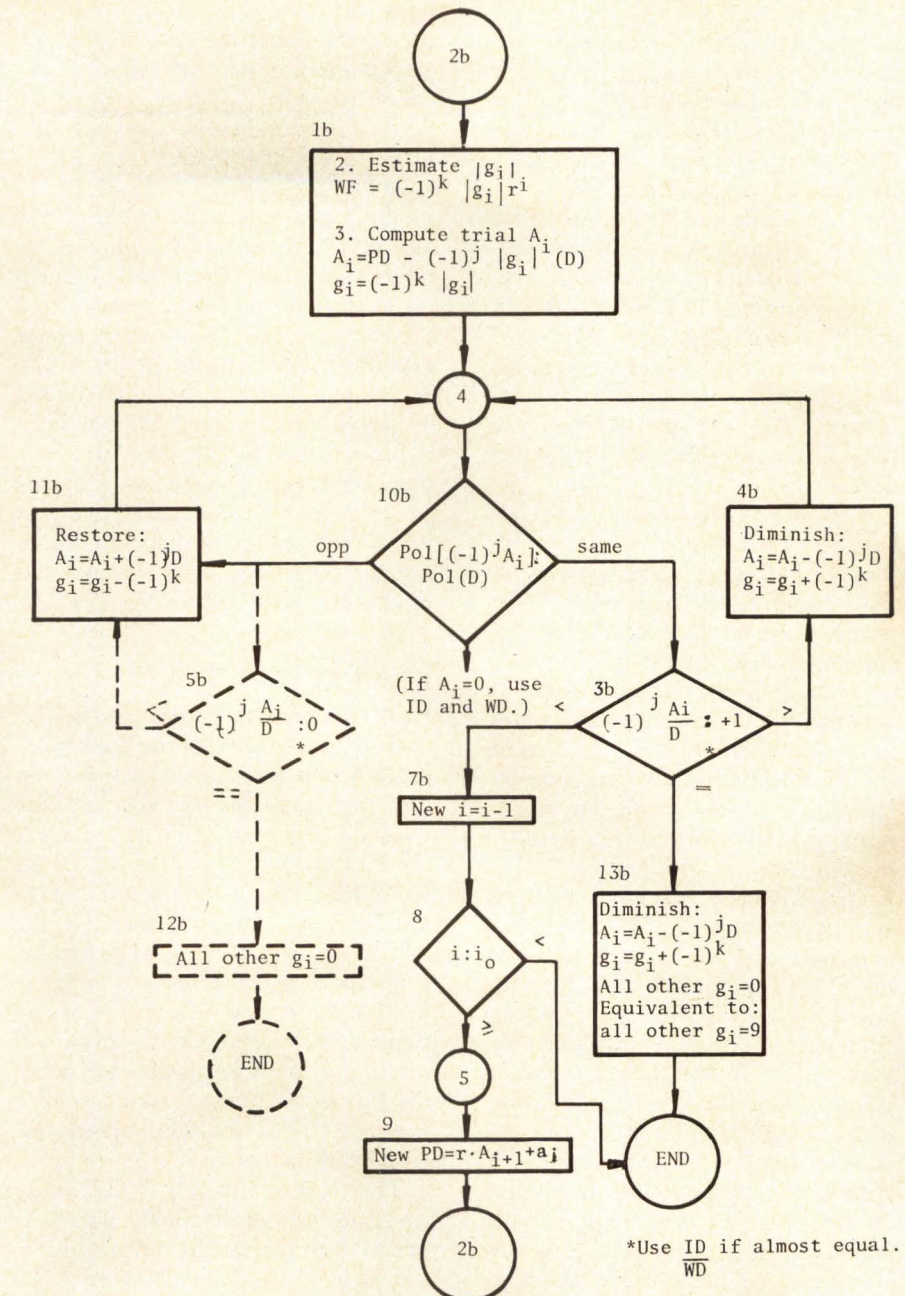


Fig. 3—Flow chart for the complete manual restoring division algorithm. Use $k = i + j$ for negaradix; $k = j$ for posiradix; $j = 0$ if A/D is negative. The dotted portions are provided to preserve the parallel with the non-restoring flow chart, Fig. 2.

being in the odd positions when the dividend (A) and the divisor (D) are of the same polarity, and in the even positions otherwise. For the normal posiradix restoring division, the quotient digits are all positive if A and D are of the same polarity, and all negative if A and D are of opposite polarity. Of course, this is division of signed numbers, rather than of unsigned numbers, and this column of Table 1 is in effect a statement of the rule of signs for normal division. However, to preserve the parallelism, in the flow charts, and in the examples, we shall use signed digits where they occur, using numerals *in italics* to indicate negative

digits. Thus, any adjustments that are necessary will apply only to the current quotient digit, so that no arithmetic need be performed on the quotient as a whole.

It is interesting that, as in addition, subtraction, and multiplication, the algorithm for negaradix non-restoring division applies to operands of both polarities and is independent of their polarities. Of course, because it is non-restoring division, and not because it is negaradix division, a test on the remainder is necessary if proper division is desired. These factors are all of great importance in designing a machine algorithm for a computer.

The flow chart for manual non-restoring division is shown in Fig. 2, and for manual restoring division in Fig. 3. These two flow charts have been drawn so that corresponding steps are in corresponding places, for easy comparison. The unfamiliar steps of negaradix non-restoring division can therefore be related directly to the corresponding step of the familiar normal algorithm. The "normal" restoring algorithm is presented in a highly stylized and detailed fashion, with certain corresponding steps that are not used shown in dotted lines.

The most important differences between these two flow charts and those of Figs. 1(a) and 1(b) are that Figs. 2 and 3 have omitted the "Determine Initial i" block, and have included the polarity test and the additional magnitude test to provide for the possibility of a quotient digit estimate which changes the polarity of the PD. If the quotient digit is too large, one or more restoring operations will be required. The result is the symmetrical arrangement of Fig. 2, in which tests against the upper and lower limits of the test interval blocks 3a and 5a, appear on opposite sides of the polarity test each followed by the appropriate adjusting operation. In Fig. 3, block 5b, the lower limit of the test interval, is zero, so that this "magnitude test" simply repeats the function of the polarity test.

As to the estimate itself, in decimal division the quotient digit is estimated by mental reference to the multiplication tables with which we are thoroughly familiar. In negadecimal, the use of a special table is necessary. This was provided in Table 4 of Part 4; it and the discussion of its use, step 2, are given on page 43 of the August 1967 issue.

Both flow charts use the partial dividend and divisor, rather than the interim dividend and the weighted divisor, so that the transition to the manual algorithm is complete. (Machine algorithms which shift the dividend at the beginning of each pass also use the partial dividend and the divisor.) The remainder is used rather than the partial dividend after the first diminishing operation, because technically, the partial dividend is a specific number representing the start of a new pass, as indicated in block 9. If there are no more dividend digits, block 8, then

the remainder is the final remainder except for adjustments required for proper division. The flow chart of Fig. 2, Part 6 may be used for this final stage of the process.

If the test ratio $(-1)^k A_1/D$ is almost equal to one or the other of the test limits, then ID/WD should be used in its place. If this ratio exactly equals the test limit, then the rest of the quotient may be written down immediately, as shown in blocks 12 or 13, although the final remainder must still be computed. If the ratio is only almost equal, then the first digit of the digit sequence of blocks 12 or 13 may be used as an estimate for the next quotient digit. A simple test for divisibility by $R + 1$ will be briefly described next.

Divisibility by $R + 1$

In decimal and negadecimal, $R + 1$ is eleven, and the test for divisibility by eleven is fairly well known. We present it here because the tests for divisibility by nine and eleven have a dual nature which is reversed in an interesting fashion when applied to negadecimal. In fact, the test for divisibility by eleven in negadecimal is identical to the test for divisibility by nine in decimal: if the sum of the digits of the negadecimal (decimal) number is divisible by eleven (nine), then so is the original number. For example, 29 is divisible by eleven; $+27$ is divisible by 9.

The dual of this test is divisibility by nine in negadecimal, which is identical to the test for divisibility by eleven in decimal: if the sum of the digits in the even positions less the sum of the digits in the odd positions of a decimal (negadecimal) number is divisible by eleven (nine), then so is the original number. For example, in 1837132, the even digits add up to $+7$, and the odd digits add up to $+18$, the difference of which is -11 .

The fact that alternating digits in negadecimal have opposite weight is the basis for this relationship, and the explanation for it may perhaps be more clearly understood if the term and notation for special decimal is substituted for negadecimal. Then, the sum of the digits is actually the difference of the sum of the even digits and the sum of the absolute value of the odd digits.

These tests are, of course, applicable to any pair of positive and

negative radix number systems having the same R . In fact, these tests are expressed quite explicitly, and more generally, by Hall and Knight's **Higher Algebra** sections 82 and 84, on pages 62-64 (first published in 1887):

"82. In any scale of notation of which the radix is r , the sum of the digits of any whole number divided by $r-1$ will leave the same remainder as the whole number divided by $r-1$.

"84. If N denote any number in the scale of r , and D denote the difference, supposed positive, between the sums of the digits in the odd and even places; then $N-D$ or $N+D$ is a multiple of $r+1$."

Number 82 is very well known, and finds applications such as "casting out nines" in checking decimal arithmetic, and parity checking in binary arithmetic. Applied to binary, No. 84 would provide a test for divisibility by three. In negabinary, however, it is No. 82 which tests for divisibility by three, which means that the modulo-three sum of the digits can be used.

Determining the Initial Value of i

In Part 4, we developed a procedure for estimating the first trial quotient digit from the division table, which requires testing the first remainder and adjusting the position of the first quotient digit as indicated by the test. However, it is clear that we can use the magnitude test, slightly modified, to establish definitely the quotient digit position before estimating the quotient digit. While the procedure described in Part 4 is probably quite adequate (and may in fact be faster) a method for determining the exact position provides us with a more elegant and rigorous algorithm and flow charts, which more closely parallels the conventional procedure, and provides the basis for machine designs.

The price of such explicitness in the procedure is added detail, which is more conveniently provided in separate flow charts, Figs. 4 and 5, expanded to include all of the initial decisions and tests.

The procedure is based on computing a trial value for i by taking the difference of the position number

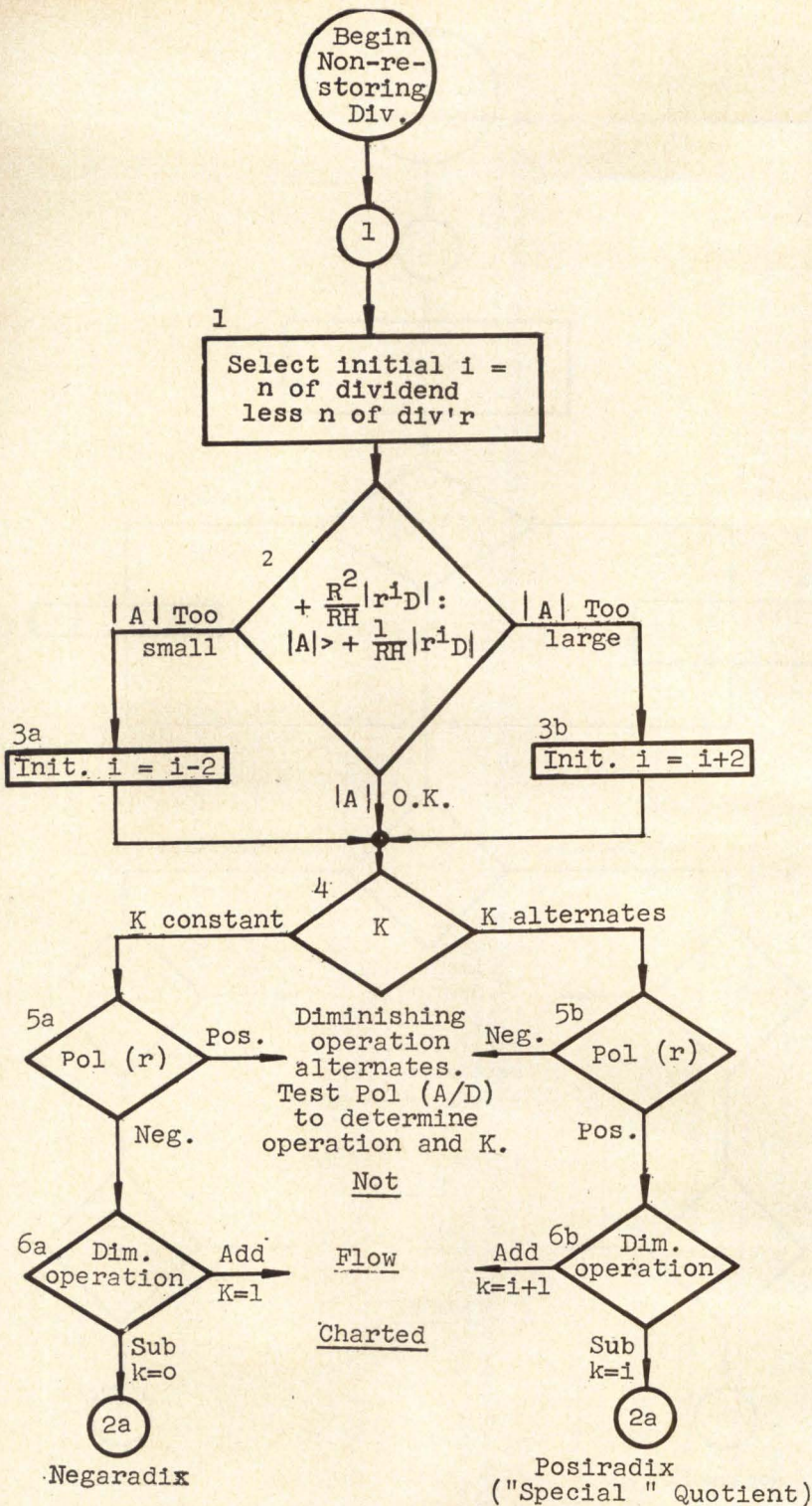


Fig. 4—Flow chart for determining most significant quotient digit position, non-restoring division.

TABLE 3
Limiting Values for A/WD for Trial i
For Trial i to be Correct

Division	Non-Restoring		Restoring		For Trial i as Defined	
	Neg.	Pos.	Neg.	Pos.	Neg.	Pos.
Upper Limit	9.0909...	+9.0909...	9.9999...	+9.9999...	+99.99...	+9.999...
Limiting Value	+100/11	+100/11	+10	+10	+100	+10
Lower Limit	1.9090...	+1.9090...	1.0000...	+1.0000...	+0.010...	+0.100...
Limiting Value	+1/11	+1/11	+1	+1	+0.01	+0.1

of the dividend and the position number of the divisor. For integers, this is simply the difference in the total number of digits in each, which effectively lines up the most significant digits of the dividend and divisor. Appending zeroes to the blank positions of the divisor gives us the weighted divisor, which corresponds to establishing $\pm r^i$ as the trial weighting factor, the sign being selected so as to make the polarities of dividend and weighted divisor the same.

With the most significant digits lined up, the ratio of dividend and trial weighted divisor have maximum and minimum values as follows (for $R = 10$) determined by taking maximum and minimum values for n digits:

$$\frac{A}{WD} = \frac{10^n (0.9090 \dots)}{10^n (0.1909 \dots)}$$

$$= +100 - e, \text{ or } +99.999 \dots \text{ (for negadecimal)}$$

$$\frac{A}{WD} = \frac{+10^n (+0.9999 \dots)}{+10^n (+0.1000 \dots)}$$

$$= +10 - e, \text{ or } +9.999 \dots \text{ (for decimal)}$$

In the same way,

$$\left[\frac{A}{WD} = + \frac{1}{100} + e \right], \text{ or } +0.01000 \dots \text{ (for negadecimal)}$$

$$\left[\frac{A}{WD} = + \frac{1}{10} + e \right], \text{ or } +0.1000 \dots \text{ (for decimal)}$$

However, for the trial i to be correct, q_i must be non-zero, which means that the ratio A/WD will have a definite upper limit starting with 9 and a definite lower limit starting with 1. These are shown for the four algorithms in Table 3, using $R = 10$ for clarity. The table includes the absolute maxima and minima developed above.

Therefore, for non-restoring division, the trial i will be correct if the following inequality holds (reverting back to the general expressions for any radix, in which

$$R = |r|:$$

$$\frac{R^2}{R+1} > \frac{A}{(-R)^i D} > \frac{1}{R+1}$$

If the ratio is too large, then the trial i should be increased by 2, which has the effect of moving the initial quotient digit two places to the left. If the ratio is too small, then i should

be decreased by 2. These rules are given in blocks 2 and 3 of Fig. 4, where absolute values are to permit postponing the selection of k and diminishing operation rules.

For restoring division, the corresponding inequality is:

$$R > \frac{A}{(-1)^j R^i D} \geq 1,$$

where j is selected to make the polarities of the numerator and denominator the same. If the ratio is too large, then the trial i must be increased by 1; if it is too small, the trial i must be decreased by either 1 or 2.

Comparison of the absolute limits and the limits for correct trial i , in Table 3, shows that for non-restoring division, a too-large ratio is possible for both positive and negative radix, since both $+100$ and $+10$ are larger than $+100/11$, but a too-small ratio is possible only in negaradix, since $+0.1$ lies within the limits for posiradix division. Thus, block 3a in Fig. 4 would never be used in the posiradix non-restoring algorithm.

By a similar analysis, we observe the well-known fact that in normal division, block 3b of Fig. 5 would never be used, and that the "init $i = i - 2$ " possibility of block 3a could not arise. For "special negaradix" restoring division, the ratio can be too large by as much as a factor of $+10$ (R), so that block 3b provides for replacing the trial i by $i + 1$. In the case of the lower limit, the minimum possible ratio is 0.01 , so that a shift to the right of either one or two places may be required for q_i (block 3a of Fig. 5).

This much of Figs. 4 and 5 definitely establishes the location of the initial q_i , paving the way for estimating the value of q_i with the assurance that it is non-zero. The balance of the two flow charts deal with decisions concerning the value of k and the choice of diminishing operation. For normal division and negaradix restoring, we wish to have k constant and to use subtraction exclusively as the diminishing operation. These decisions are shown by the left-hand (a-side) of Fig. 4 and the right-hand (b-side) of Fig. 5. The other possibilities involve either an alternating value of k or an alternating diminishing operation. The decisions shown in the flow chart provide for alternating k and the use of subtraction exclusively. None of the other possibilities are flow charted.

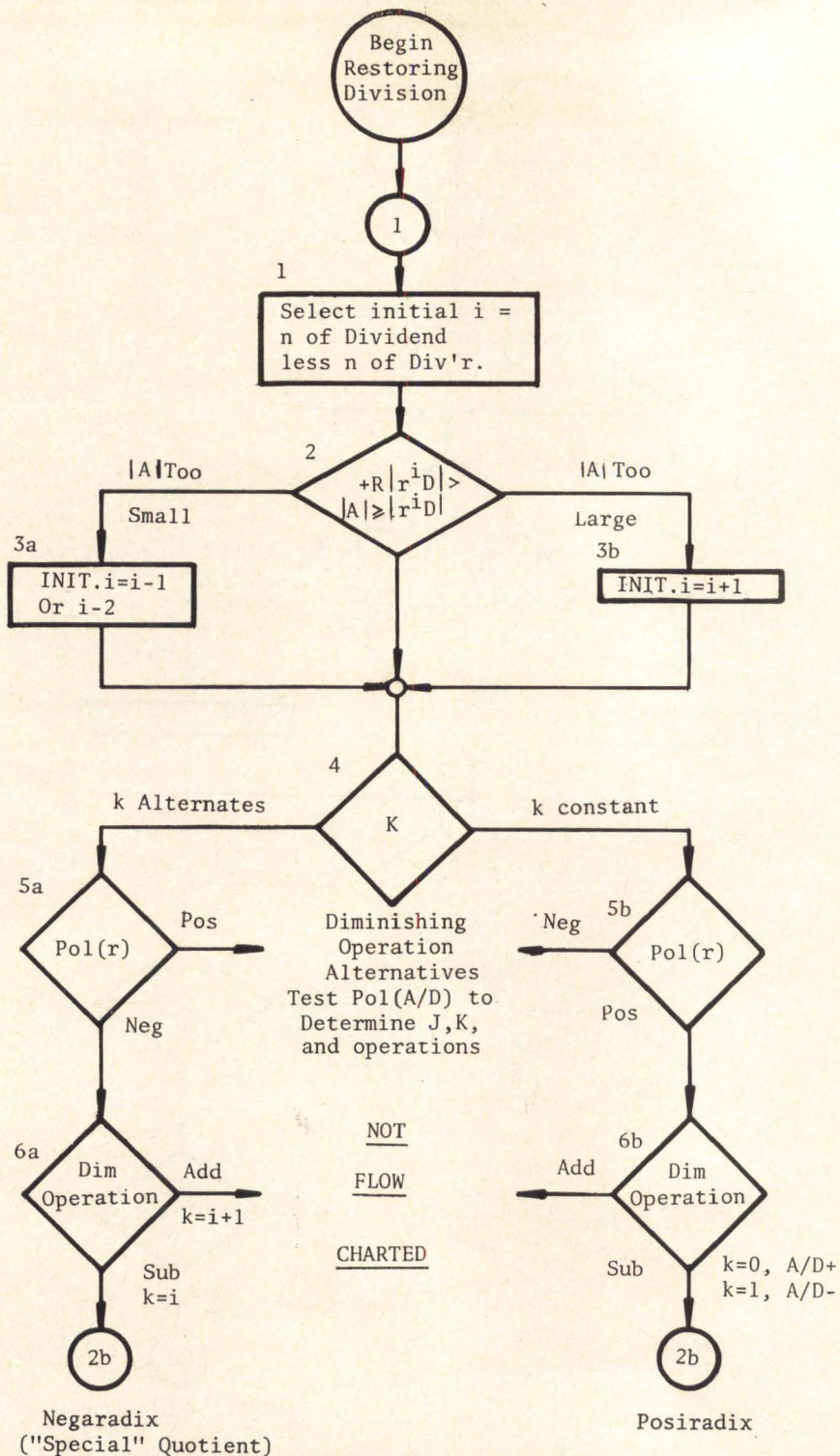


Fig. 5 — Flow chart for determining most significant quotient digit position, restoring division.

Summary

If we review the five steps outlined in the introduction to division in Part 4 for decimal manual division, we find that they can be used for negadecimal division, except for the need to adjust the final results for proper division. The six steps are then as follows:

1. Determine most significant quotient digit position.

2. Estimate initial quotient digit.

3. Compute new remainder.

4. Test remainder and adjust quotient if necessary.

(Use interim dividend if the test is close.)

5. Obtain next partial dividend by bringing down next dividend digit.

(Note: the partial dividend cannot be used for decimal non-restoring division because sign changes cause

subtraction of low order dividend digits.) Repeat steps (2) through (5) until division is complete.
6. Adjust quotient and remainder for proper division.

These steps are indicated in Figs. 4 and 5 in the numbered circles. Examples of division illustrating these steps are shown in Fig. 6.

This completes the discussion on division. If we had been interested only in machine division, we could have ended the discussion after Part 5. If we had done that, we would not only have missed the richest and most interesting aspects of negative radix division, we would also still not have any real "feel" for it. The apparently intellectual exercise of achieving manual negadecimal division has therefore had the very pragmatic effect of forcing a most searching analysis of the process of division in general, positive radix as well as negative radix. In doing so, we have shed light on some previously unexplored properties of non-restoring decimal arithmetic and, as far as the magnitude tests are concerned, on properties of non-restoring binary arithmetic.

We have seen that the apparently synthetic "special decimal" of Part 1 can be used as an arithmetical account of what happens in non-restoring division. We use the magnitude limits of a given number of negadecimal digits, which were derived in Part 2, to develop the magnitude test and to determine the trial "i". We observe the importance of the digit-oriented arithmetic which was explained and fully illustrated in Part 3, an example of which occurs in step 5 of the procedure for non-restoring decimal division where it is not possible to "bring down" the next dividend digit.

In the concluding article of this series, we shall make use of still another fascinating property of negative radix numbers. Because a negative number is completely different from its positive counterpart, operations to produce the additive inverse of the results of normal arithmetic operations become non-trivial. These operations comprise a completely new class of arithmetic operations — another arithmetic. One of the most important properties of complementary arithmetic is that addition has carries of only one sign, making the addition and multiplication tables more like those of normal decimal.

Example 1. Division of a Positive Dividend by a Positive Divisor (+/+):			
373	+ 373	233	+ 233
267/046413	+147/+34393	267/046413	+147/+34393
561	+44100	314	+294
19031	-09707	1501	+499
19189	-10290	-(561)	+441
623	+583	623	+583
561	+441	561	+441
262	+142	262	+142
Example 2. Division of a Negative Dividend by a Positive Divisor (-/+):			
1846	+1846	234	+ 234
267/0175617	+147/-34403	267/0175617	+147/-34403
267	+147000	-(314)	-294
19286	+112597	501	-500
19236	+117600	561	-441
501	-5003	19407	-593
628	-5880	-(628)	-588
937	+877	15	- 5
922	+882		
15	- 5		
Example 3. Division of a Negative Dividend by a Negative Divisor (-/-):			
374	+ 374	234	+ 234
1953/175617	-147/-34403	1953/175617	-147/-34403
1659	-44100	1706	-294
1171	+09697	501	-500
1031	+10290	-(1659)	-441
1407	-593	1407	-593
1592	-588	1592	-588
15	- 5	15	- 5
Example 4. Division of a Positive Dividend by a Negative Divisor (+/-):			
1847	+1847	233	+ 233
1953/0046413	-147/+34393	1953/046413	-147/+34393
1953	+147000	-(1706)	+294
2934	-112607	1501	+499
2984	-117600	1659	+441
1501	+4993	623	+583
1592	+5880	-(1659)	+441
1293	-887	262	+142
1031	-1029		
262	+142		

Fig. 6 Examples of division. These are the inverse of the multiplication examples of Part 4, except that the products have been slightly changed by the addition of -5 to provide non-zero remainders.

The arrangement of these examples is slightly different from previous examples, since we have the usual negadecimal on the left and decimal on the right for both non-restoring and restoring division. Therefore, the examples for all four algorithms are placed in line, in four adjacent columns occupying the whole width of the page. In that way, we have the convenience of being able to compare negadecimal non-restoring with decimal restoring. The order (from

left to right) is: negadecimal non-restoring, special decimal non-restoring, special negadecimal restoring and decimal restoring.

Note that in the special decimal non-restoring, the interim dividends must be used. Note also, in the special negadecimal restoring, that subtraction of a negadecimal number prefixed with a minus sign can be accomplished by "changing the sign of the subtrahend" and adding. As usual, a sign before a number indicates that it is decimal; a number without a sign (within parentheses) is negadecimal.

The examples started in Part 4 will be left as exercises for the reader, starting with the polarity test on the remainder.

Corregendum to Fig. 4, Part 6

Delete $(-1)^i$ from blocks 3 (ab) and 5 (ab)

Correnda to Fig. 5, Part 6

In block 2(ba), $k = i + j$
 $WF = (-1)^j (-r)^i$
 In block 3(ba), substitute j

for exponent i

In block 4(ba), substitute k for the exponent i

In block 2(bb), substitute j for k in three places

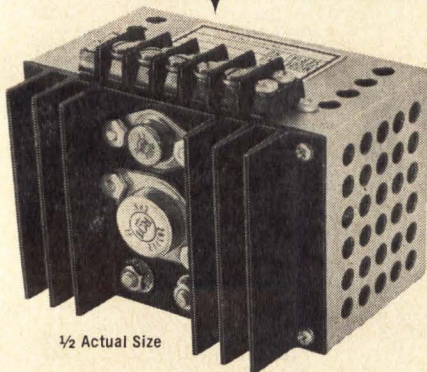
In block 3(bb), substitute j for i

In block 4(bb), substitute j for i

NEW
mini-mod

**I/C POWER
SUPPLY**

**80%
SMALLER!**



1/2 Actual Size

Avtel's new, ultra-miniature power supply is only 4" x 3" x 2 5/8" including heatsink.

Mini-mod is specifically designed for use in lightweight chassis with IC or other digital logic. Output voltages are available from 3 to 30 volts with .05% regulation.

INPUT: 115 Volts 47-440HZ

TYPICAL OUTPUTS:

3 V at 6 A
5 V at 5 A
15 V at 2 A

Mini-mod is currently available from stock. Detailed specifications and price are available upon request.

CUSTOM POWER SYSTEMS

Avtel's experts are capable of solving your most difficult power conversion requirements.

POWERTEC PRODUCTS



AVTEL CORPORATION
1130 EAST CYPRESS STREET
COVINA, CALIFORNIA 91722
PH. (213) 331-0661
TWX (213) 686-6753

DIVISION-AIRTRONICS, INC.

CIRCLE NO. 38 ON INQUIRY CARD



NEW PRODUCTS

PUSHBUTTON SWITCHES

In keeping with the increasing demands and requirements of computer and automatic controls, a new pushbutton switch line is said to have been engineered to encompass more combinations of switching characteristics than any other available device. The new switches feature 3 amp cross bar palladium contacts; lighted or unlighted buttons; continuous key strips to 20 stations on one solid frame; ac or dc reset actuation; key motion-sensing contacts; and interlatch, lockout, one only, momentary, accumulative latch, and push-push action. Underwriters Safety Device Co., Chicago, Ill.

Circle No. 200 on Inquiry Card

DUAL POWER SUPPLY

A new regulated solid-state dual power supply provides two highly-regulated, independent, continuously-adjustable outputs covering the range from 1.2 to 30 volts at currents from 0 to 500 milliamperes and with a ripple level below 1 millivolt rms. When operated in series as one unit, the two supplies will furnish voltages between 2.4 and 60 volts at currents up to 1/2 ampere. Output voltages are monitored by two front panel meters. The output terminals of each supply are isolated so that either terminal may be grounded. Short circuit protection and current limiting are provided. The unit measures 3 1/2 inches high, 15 inches wide, and 8 inches deep. Aul Instruments, Inc., Long Island City, N.Y.

Circle No. 270 on Inquiry Card

MILITARY COMPUTER

A general-purpose militarized digital computer weighs five pounds and measures less than one-tenth of a cubic foot. Functional simplicity,

high speed (100,000 operations/sec.), NDRO/DRO core memory, and monolithic integrated logic and memory circuits are key features of the computer. The memory design is said to combine the reliability of an NDRO wired program with the efficiency of coincident-current selection circuitry common to program and scratch pad storage. In addition, the entire memory may be operated in a standard DRO mode utilizing externally-loaded programs. American Bosch Arma Corp., Garden City, N. Y.

Circle No. 247 on Inquiry Card

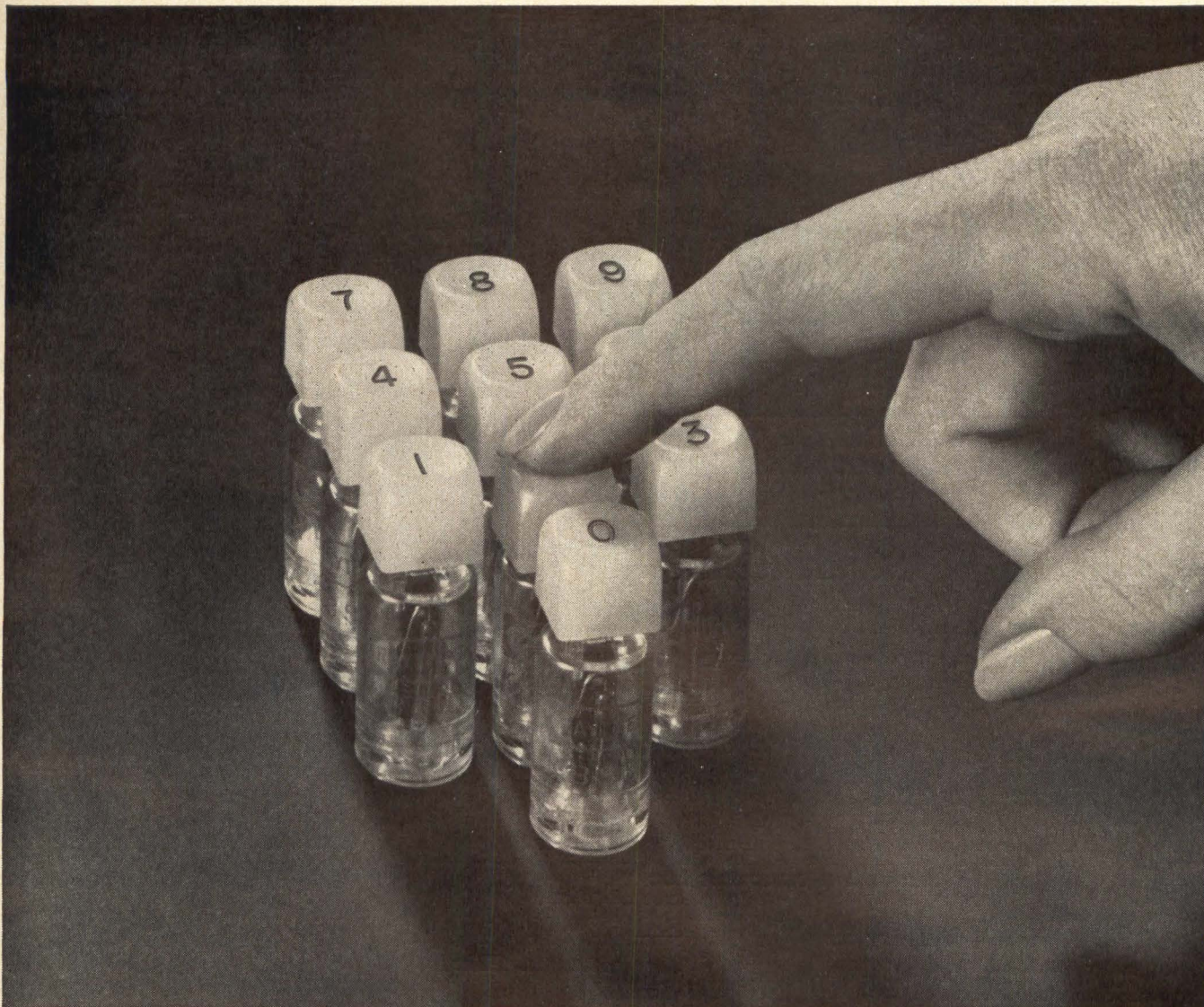
IC LOGIC CARDS

New line of integrated circuit logic cards has complete voltage decoupling on each logic card through use of an emitter follower driven by a highly regulated, low ripple power supply, as well as capacitive decoupling on each board to permit power supply bussing, without detrimental power loss or noise generation. These high density modules will use fast-switching DTL integrated circuit elements in a short circuit proof 14-pin dual in-line package. Use of a standard 44-pin edge connector provides termination flexibility (solder, wire wrap, taper pin, Termini-point, or printed circuit mother board). Units are available for reliable performance up to 5MHz at temperatures from 0°C. to 70°C. Datascan, Inc., Clifton, N. J.

Circle No. 252 on Inquiry Card

MULTIPLEXER/CONVERTER

Multiplexer/converter offers a total throughput rate of 667 kHz. The system utilizes a 1-microsecond conversion speed of an 8-bit converter. It is said to provide the most economical method for digitizing up to 10 channels of high-frequency data. Its unitary addressing code allows



These new keyboard switches feature unusually precise action and low-cost mounting. See for yourself—write for samples.

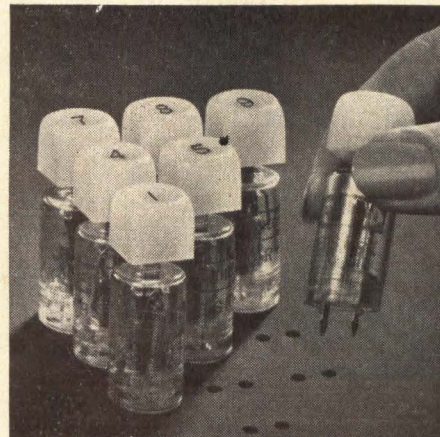
These elegantly styled key switches are especially suitable for computers, learning and business machines, and other advanced control equipment.

Designed by Raytheon, they have a featherlight touch that is precise and reliable. Just a 3-oz. touch activates the switch. Because of the unique design, this action can be repeated more than 10 million times. Yet the switches cost as little as 60¢ in production quantities.

Raytheon key switches are available in a wide range of standard- and custom-cap shapes, sizes, colors,

and alphanumerics. The characters can be illuminated by backlighting. All switches are made of high-quality materials: stain-resistant caps; polycarbonate body parts; stainless steel springs; beryllium and stainless steel contacts. They are available in single- and double-level wipe-action types, and in dry-reed, hermetically sealed single- and double-level types.

Write for samples. For free samples, write on your letterhead describing your application to: *Raytheon Company, Industrial Components Operation, Dept. 2351-CD, Quincy, Massachusetts 02169.*



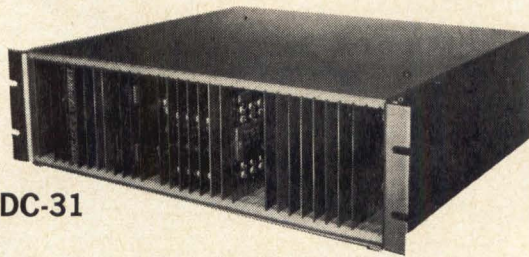
Simple, low-cost mounting. Raytheon switches plug into .125" PC board. Contact pins snap in, firmly lock switch in place for soldering. This permits you to use flow soldering techniques—cut keyboard assembly time and costs.



CIRCLE NO. 39 ON INQUIRY CARD

NEW!

MEMORY BUFFER



MODEL DC-31

- FULL CYCLE TIME1 Microsecond
- ACCESS TIME400 Nanosecond
- CAPABILITY128,256 or 512 Words
Up to 8 Bits/Word
- PRICE\$1260 for 128 x 6
In Small Quantities.
- DELIVERY30 Days.

Many options available . . . I C Logic and all silicon semi-conductors . . . All gold connectors . . . Flat mounted components.

 **DATA CRAFT
CORPORATION**

776 N. E. 40th Court • P. O. Box 23550 • Ft. Lauderdale, Fla. 33307 • Phone (305) 565-9441

CIRCLE NO. 40 ON INQUIRY CARD

control of sampling rates of the 10 input data channels — sampling one channel up to 667,000 times a second if such thin “data slicing” is needed — then sampling each of the other nine channels at a rate selected individually for that channel. Each channel is selected and its data digitized in 1.5 microseconds. Resolution is 8 bits including sign, and accuracy is 0.5% of full scale $\pm 1/2$ LSB. Adage, Inc., Boston, Mass.

Circle No. 271 on Inquiry Card

CORE MEMORY

Small, high-speed 2½D core memory system is designed for OEM and non-severe military applications. The NANOMEMORY trademark 2650 is packaged in a 7” high sliding drawer (including power supply and optional tester) which mounts into a standard EIA 19-inch wide cabinet. According to the Company, the new system is the smallest for its speed and capacity on the commercial market. A combination of integrated circuit electronics with a unique 2½D drive system gives the

NANOMEMORY 2650 a cycle time of 650 nanoseconds and an access time of 350 nanoseconds. Silicon integrated circuits are used for all logic, addressing, decoding, timing, control, and sensing functions. The proprietary drive scheme for which a patent is pending is said to enhance system reliability and storage density. The system can handle up to 16,384 words x 18 bits, 8,192 words x 36 bits or 4,096 words x 36 bits, without any modification of the 7” high x 19” wide x 21” deep configurations. For greater word capacity and extended word lengths, NANOMEMORY 2650’s can be conveniently stacked. Use of a new magnetic selection technique enables stack connections to be significantly reduced — to the extent that all magnetics and system electronics are mounted on plug-in printed circuit boards. Core stacks as well as accompanying circuitry are therefore readily accessible for maintenance and can be quickly removed and replaced if necessary. All modules of a common type are directly interchangeable with each other and no module selection or adjustments

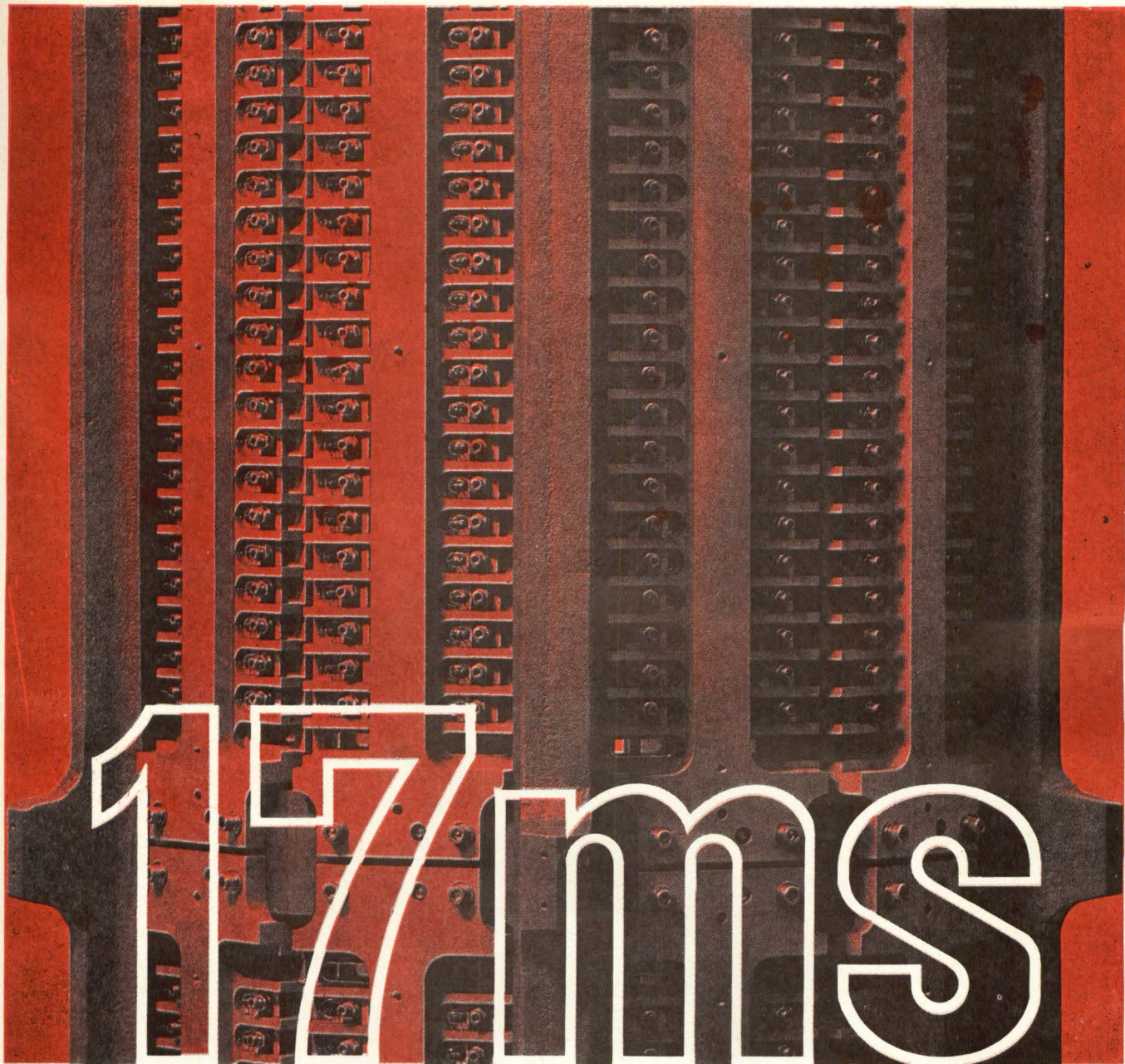
are required to ensure stable performance over the operating temperature range of 5°C to 45°C. For further reliability, the use of a double keying technique prevents misorientation of printed circuit modules or insertion into an incorrect location. The 2650 also includes protection circuitry to ensure that no stored data is lost during power turn-on, turn-off or failure, and no damage can be caused by excessive internal temperature or DC voltage conditions. Front of rack access is provided to all system modules and wiring.

The NANOMEMORY 2650’s high operating speed and compact packaging make it well suited for all applications where high reliability and simplified maintenance are required. Electronic Memories, Inc. introduced the first submicrosecond 2½D commercial memory system in 1964. This unit offers full cycle times down to 650 nanoseconds and capacities up to 16,384 words x 84 bits. In addition to commercial memory systems, Electronic Memories produces cores, stacks, and systems for aerospace and data processing applications. Electronic Memories, Hawthorne, Cal.

Circle No. 249 on Inquiry Card

CONTACTORS FOR DUAL-IN-LINES

The new 029-271 Series Contactors are for use with 14 and 16 lead molded dual-in-line carriers. The carriers themselves accept all standard 14 or 16 packages with flat or rolled leads and have found widespread usage as convenient protective D. I. P. containers. When used with the 029-271 contactors, the carriers can be utilized in testing, aging and breadboarding applications, both at ambient and elevated temperatures. The 029-271 Series contactors are molded of Polysulfone for dependable and continuous operation over the range of -65°C to 150°C. Contacts are spring tempered Ni/Au plated beryllium copper of a wiping-type design which protects against lead deformation during device testing. Interlead capacitance of the contactors is less than 0.4 pf. at 1 megacycle and contact resistance is below 10 milliohms. Flat ribbon-type terminals on the contactors permit either wave solder-



1,000,000,000 BITS—FAST!

More memory! Faster access!! More memory!!! Faster access!!!! This is the constant need of "Time Share" and "Management Information" Systems. How about 1,000,000,000 bits with an access time of 17 milliseconds... enough in a hurry? At Magne-Head, memories are made for this! For information on any of our high-performance Magnetic Memory Systems or Components, write or call today. Write for free 16-page bulletin.

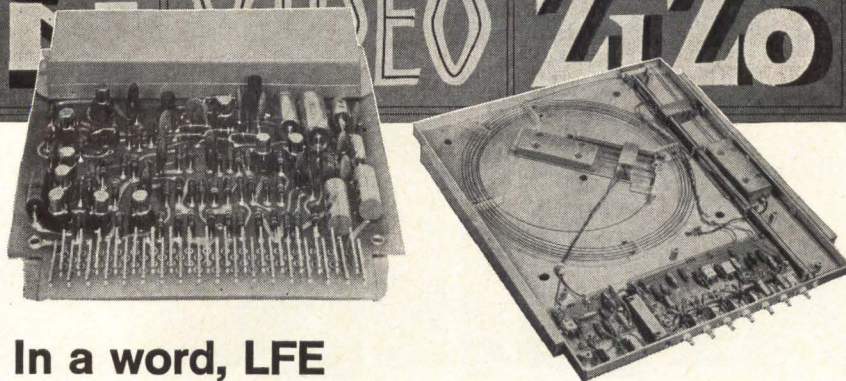


MAGNE-HEAD DIVISION

13040 South Cerise Avenue / Hawthorne, California 90250 / 213 679-3377 / 772-2351 / TWX 910-325-6203

CIRCLE NO. 41 ON INQUIRY CARD

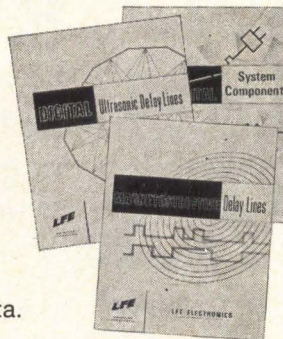
ZERO T.C. **S/N**
SERIAL MEMORY **20,000 BITS**
TORSIONAL DELAY
UNITY GAIN **BI-POLAR**
BULK & BUFFER
VIDEO **ZiZo**



**In a word, LFE
 for glass and magnetostrictive
 delay lines for digital applications**

These are just a sampling of the performance features of LFE's glass and magnetostrictive delay lines. We can supply you with standard delay lines or serial memories with the capacity, bit rate, mode, delay and other parameters you need . . . or, you can specify custom delay lines, with or without associated electronics, to meet your special design requirements.

For the complete story write for technical data.



LFE | ELECTRONICS DIVISION

Laboratory For Electronics, Inc.
 WALTHAM, MASSACHUSETTS 02154
 Tel: 617-894-6600 • TWX: 710-324-0681

CIRCLE NO. 42 ON INQUIRY CARD

ing or hand wired solder connections. The contactors are available with mounting flanges for chassis mounting or without flanges for incorporation into printed circuit boards. Loading and unloading of the carriers into the contactors is a quick and simple one-hand operation, facilitated by prominent polarization notches. Contactor life expectancy is rated in excess of 25,000 carrier insertions. Price is \$1.25 to \$2.55, depending on model, and quantity and delivery is stock to two weeks. Barnes Development Co., Lansdowne, Pennsylvania.

Circle No. 251 on Inquiry Card

ANALOG/HYBRID COMPUTER

Said to be the first desk-top scientific computer to provide advanced analog computing capabilities plus all of the requirements for expansion to a full-scale hybrid computing system. Designated the EAI 580, the system is a general-purpose, 10 volt, 80 amplifier, solid-state computing system that is pre-wired for full expansion. It includes up to 70 servo set potentiometers, provisions for a digital logic system and a hybrid control interface in the main console. The 580 offers a completely self-contained, integrated-circuit logic facility within the console. The addition of hybrid control interface equipment in space provided within the basic system provides for integration with external digital computers, making it readily expandable to a full hybrid system. A full line of peripheral readout equipment is also available. Simplified operating provisions include a new electronic keyboard addressing system for the automatic setting of up to 70 servo-set potentiometers. They can also be set by a "Pot Control Lever" which raises or lowers setting values with a simple bi-directional movement of the lever. Values of setting are displayed instantly on the system's high accuracy digital voltmeter. The new variable diode function generators are designed for easy set-up and are in pull-out drawers so the operator can set them while seated at the console. The high speed amplifiers perform at full amplitude over the entire bandwidth with no velocity limiting. A unique track/store unit provides fast signal tracking (less

than 1 usec time constant) with a small capacitor, and offers low drift by means of a large capacitor. The entire computer—32" high x 51" wide x 29" deep weighs less than 600 pounds when fully expanded. It sets easily on any normal laboratory bench or desk and can be conveniently transported from one area of need to another. It operates from any 110 or 220 VAC outlet, and requires less than 500 watts when fully expanded. No special environmental controls are needed. According to Fred Martinson, vice president of EAI's Computer Division, "The 580 was born out of the need for high performance analog computation, as well as the requirement for a hybrid-oriented desk-top analog computer. It has all of the features a digital computer user needs to add analog and hybrid capabilities to his facility." The EAI 580 was displayed publicly for the first time at WESCON in San Francisco. The 580 ranges in price from below \$10,000 for a basic system to approximately \$55,000 for a fully expanded (without interface, but including logic) system. The first units will be available in October. Electronic Associates, W. Long Branch, New Jersey.

Circle No. 221 on Inquiry Card

COMPACT INCREMENTAL RECORDER

A compact incremental digital magnetic tape recorder featuring the 6" reel holding 250' of tape, requires only 7" of vertical panel space in a standard 19" rack mount. Recording at 200 CPI, 7-channel, the stepping rates are asynchronous to 150 steps per second. Higher stepping rates and density are also offered. Lateral parity is automatically generated as is the LCC and IRG, and the reel drive is full servo. The advantages of magnetic recording are provided at a price competitive with paper tape perforators. Delta-Corders, Inc., Burbank, California 91502.

Circle No. 201 on Inquiry Card

MACHINE TOOL READOUT

A built-in electronic calculator in the Wang Model 100 Position Readout System computes reference point shift and assures the machinist oper-

ator that he will never lose position information by shifting zero. The system uses shaft-angle-to-digital encoders for absolute (not incremental) readout, so that no pulse-counting circuits are required, thus insuring the system against lost counts. The system is also immune to electrical and magnetic "noise" interference from nearby motors and other attenuating influences, and position information is not permanently lost if power is momentarily lost. A major advantage of the system is that it enables semiskilled machinists to turn out the highest precision work with a minimum of time and effort. This efficiency factor leads to an estimate, based on machine-shop study of a wide variety of machine tool work, that the system will pay for itself within six months of use. The price is \$1490 per axis. Display units are only 3 inches high, 7 inches deep, and 13 inches long, and can be conveniently stacked for multiple-axis use. Easy-to-use thumbwheel switches provide digital indication of reference shift. The power supply is separate from the display for ease of installation near encoders.

Circle No. 202 on Inquiry Card

COORDINATE INSPECTION SYSTEM

An improved Z-axis digital readout is available with all PICOMM Coordinate Measuring Systems manufactured by Potter Instrument Co. The Z-axis measurement capability greatly increases the flexibility and capability of the system. It makes possible measurement and layout in three axis with only one set-up. Heights and depths of three dimensional pieces can be quickly determined to an accuracy of 0.0005". Shaft diameters and concentricities are easily checked by mounting between centers and rotating them under the stylus. The Z-axis also converts the PICOMM into a fast and efficient tool setter as the height of the tools can be set very quickly and accurately. The Z-axis has a range of 7 inches. A Z-axis vernier is also available to facilitate setting of the stylus at any desired height in measuring contours and in layout in the third axis. The PICOMM Coordinate Measuring Machine provides a clear, instantaneous digital readout to the nearest 0.0002". Convenient directional

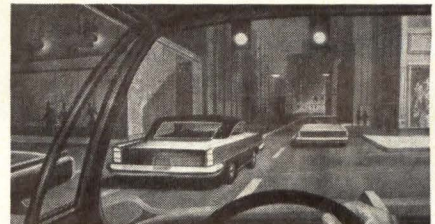
count on
these other



divisions:

Automatic Signal

electronic traffic control systems



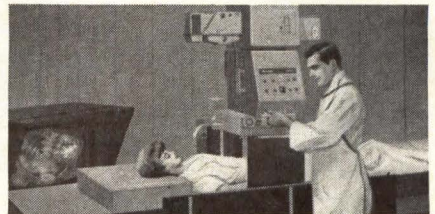
Eastern Industries

pumps and cooling systems



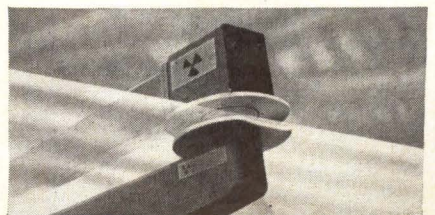
Keleket

medical X-ray equipment and services



Tracerlab

nuclear equipment for research and industrial control



LABORATORY FOR ELECTRONICS, BOSTON, MASS.

CIRCLE NO. 43 ON INQUIRY CARD

THIS IS THE ONLY SYSTEM/360-COMPATIBLE DIGITAL INCREMENTAL MAGNETIC TAPE RECORDER YOU CAN BUY. (THE REASON IS CBD.)

Why is CALMA's Model 800 the only 9-channel, 800bpi, SYSTEM/360-compatible digital incremental magnetic tape recorder currently available? Because no other recorder manufacturer can meet the maximum character spacing variation specifications of the major computer makers.

CALMA's unique CBD (Constant Bit Density) controller guarantees character spacing variations of less than 2%.

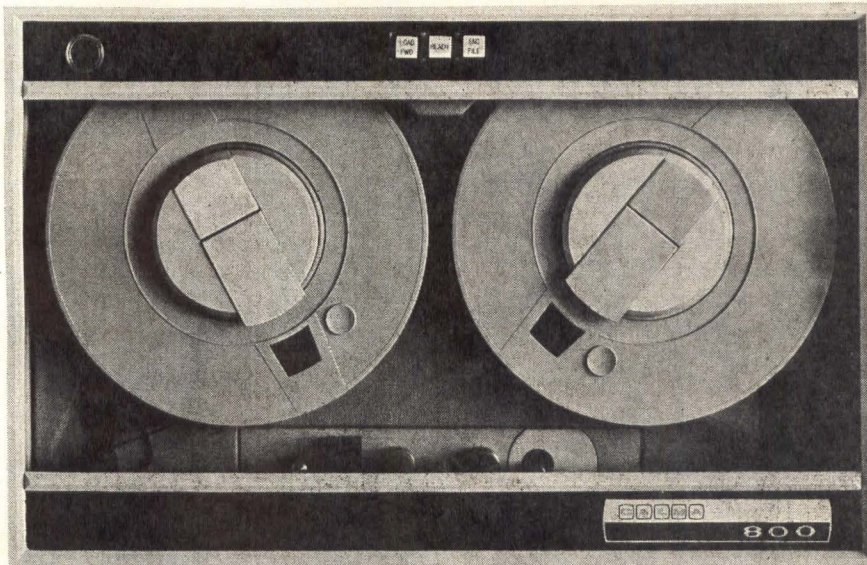
The Model 800 will collect your sporadic (0-500 characters per second) digital data on SYSTEM/360-compatible magnetic tape.

Those of you without SYSTEM/360 can have all the advantages of CBD in our Model 600 (7-channel, 556bpi, 0-500cps) and Model 200 (7-channel, 200bpi, 0-500cps) digital incremental recorders.

Detailed technical information is available. Write, phone, or circle our number on the reader service card for your copy of CALMA Bulletin DR.



346 Mathew Street
Santa Clara, Calif. 95050
Phone: (408) 244-0960



CIRCLE NO. 44 ON INQUIRY CARD

switches located with zero reset switches provide positive readings in any direction. Potter Instrument Co., Inc., Plainview, N.Y.

Circle No. 216 on Inquiry Card

PHASE LOCK FREQUENCY PROCESSOR

A frequency processor has been developed that cleans up contaminated signals. Identified as Model 251, it picks out a signal that is buried in

noise, tracks it over a wide variation in frequency, processes it through a narrow bandwidth phase lock filter, and presents it in the form of a clean high level square wave output. It also multiplies the signal frequency by decade and binary factors up to 128, and it demodulates wideband AM/FM/PM signals. Input frequency range is 1 kHz to 240 kHz in six plug-in steps; bandwidth range is 10 Hz to 5% of the operating frequency. A front panel plug-in card selects the operating frequency, the

bandwidth, and the multiplying factor. Price is \$1830. Interstate Electronics Corp., Anaheim, Cal.

Circle No. 220 on Inquiry Card

MINIATURE DC RELAY

Only 20 milliwatts per pole are required to pull in a new ultra sensitive relay. At this low power level, the relay can be driven directly by existing microcircuits. In a recent application, an SCR and a triad were eliminated by a single ultra sensitive relay driven directly by low level logic. A variety of contacts are available to switch low level to 2 amp loads. Coil voltages range from 2 VDC to 48 VDC. Prices range from \$3.00 to \$6.00, depending on the features and quantity. No charge samples are available to qualified designers. Parelco, Inc., San Juan Capistrano, Cal.

Circle No. 221 on Inquiry Card

13-BIT NATURAL BINARY SYSTEM

Small size, low cost parallel natural binary encoder system using a Baldwin photoelectric, absolute position, direct reading, single turn encoder with a lamp life in excess of 50,000 hours has a capacity of 13-bits per turn, outputs compatible to most DTL and TTL IC logic and requires only two supply voltages including the lamp voltage. The new system was developed to fit a wide range of commercial applications including automatic drafting machines, map readers, x-y plotters and Numerical Controlled feedback loops where high reliability and long maintenance free operation are required. Specifications are: +4.5VDC (open circuit) for a binary "1", output impedance 6000 ohms, +0.5VDC or less for a binary "0" with a maximum sinking current of 7.0ma. Power requirements are +5VDC $\pm 5\%$ @ 260ma and -5.5VDC $\pm 5\%$ @ 450ma nominal. Bearing life in excess of 1×10^9 revolutions. Either direction of rotation for increasing count is selectable. Also available on special orders are, low torque bearings (.3 gm-cm) and low inertia disks (15 gm-cm²). Delivery from stock. Baldwin Electronics, Inc., Little Rock, Ark.

Circle No. 210 on Inquiry Card

NINE TRACK CONTROL BUFFER

Analog or digital data can be converted to the 9 track NRZI computer format by a new format control buffer. Called the 1051, it can be tai-

Move With Advanced Computer Technology At NCR Electronics Division

SYSTEMS FORMULATION

Analysis and development of advanced systems specifications; consultation on systems design, hardware configuration, software trade-offs; analysis of competitive systems. Applicant should have familiarity with very high speed memories, large-scale integration, disc files, drum files, communications and time sharing plus related BS degree and 3 to 5 years' experience in one or more areas mentioned.

SOFTWARE SYSTEMS

Programmers to develop executive and operating systems for third-generation computer systems. Desire experience with medium- and large-scale general-purpose systems employing high speed peripheral units, tapes, random-access files, disc files, drum files, on-line, time sharing and multi-programming. Requires related BS degree and 3 to 5 years' directly related experience. Positions also open for hardware-oriented programmers to do systems diagnostic work.

EDP ANALYST/PROGRAMMERS

Analyst position entails systems analysis in financial and administrative areas. One year of EDP experience required, degree desirable. Programming positions involve accounting and manufacturing systems. Degree and recent experience on medium- to large-scale systems desired.

OPTICAL SYSTEMS

To do computer-aided design of specific elements in complex optical systems, such as field and condenser, as well as image-forming elements.

Activity includes optical-electronic lab work, systems layout and design, technical liaison. Involves geometrical and physical optics. Requires BS in physics or optics plus 2-5 years' directly related experience.

MEMORIES RESEARCH

To design high-speed magnetic memory circuits. Requires knowledge of nanosecond pulse techniques and magnetic memory organization. Familiarity with plated-wire and mass-storage memory concepts desirable. Requires BSEE plus five years' experience.

SYSTEMS ENGINEER

For systems design on advanced computers. Requires extensive knowledge of memory technology, systems logic and large-scale integration as applied to medium- to large-scale general-purpose computing systems. Minimum of BSEE and five years' direct experience required.

LOGIC DESIGN

Several positions available for EE's with 2-5 years' experience in logic design on either special- or general-purpose equipment. Positions require thorough knowledge of logic as related to real-time hardware development or automatic test equipment.

CIRCUIT DESIGN

Positions for both systems- and device-oriented circuits men to work either in developmental projects or standard circuits group. BSEE required plus 3-5 years' design experience and thorough understanding of IC technology. Knowledge of large-scale integration concepts and

ramifications desirable. Projects include thin-film memories, IC utilization and development, project/vendor liaison, systems applications.

FACILITIES/LAYOUT

Work entails projecting needs of expanding division, development of proposals, program implementation. Requires three years of facilities and layout experience, preferably in electronics industry; BSIE or equivalent; ability to deal effectively with all levels of personnel. Knowledge of safety codes desirable.

MACHINE DESIGN

Creative mechanical engineer capable of designing sophisticated manufacturing hardware and of developing machines to do jobs which heretofore have not been encountered. Requires BSME and minimum of two years' experience.

CHEMICAL PROCESSES

Positions in both engineering and manufacturing for man with BSChE and 2-5 years' experience in electroplating and electrodeposition in thin and thick films. Thorough knowledge of related materials, pre-plating surfaces, plating equipment required. Work entails development of advanced processes and techniques for computer development and production.

QUALITY ASSURANCE ENGINEERS

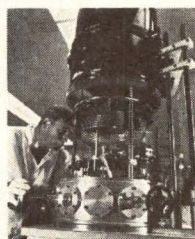
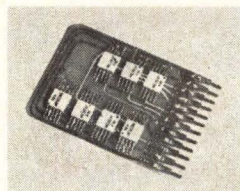
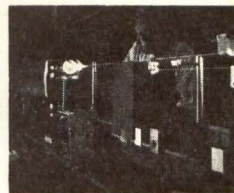
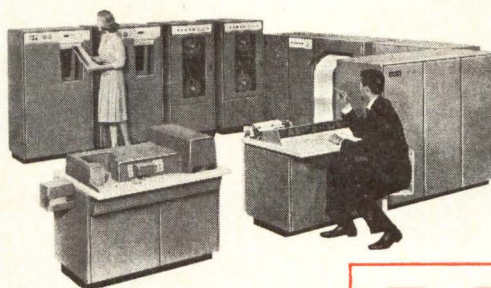
Q.C. assignments include process capability, studies, failure analysis, design reviews, establishment of inspection standards. Position requires 2-3 years' experience with EDP equipment, knowledge of magnetic materials, BSME degree. Reliability positions involve planning, conducting and reporting reliability tests of electronic components, assemblies and units. BSEE required plus experience with reliability mathematics, computer circuitry. Positions also available in systems test.

TO ARRANGE A CONFIDENTIAL INTERVIEW send resume including salary history to: TOM E. LYON

NCR Electronics Division is the largest commercial computer manufacturing facility in Southern California and one of the most advanced in the world. The Los Angeles plant and laboratories have recently been doubled, and an additional manufacturing facility is now under construction in San Diego. At NCR you will enjoy stable, non-defense activity in a

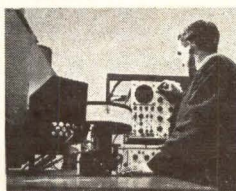
thoroughly professional environment. Your job and your future: the creation of advanced business automation for NCR markets in 121 countries.

Challenge, opportunity and Southern California are waiting for you. Look into these opportunities now.



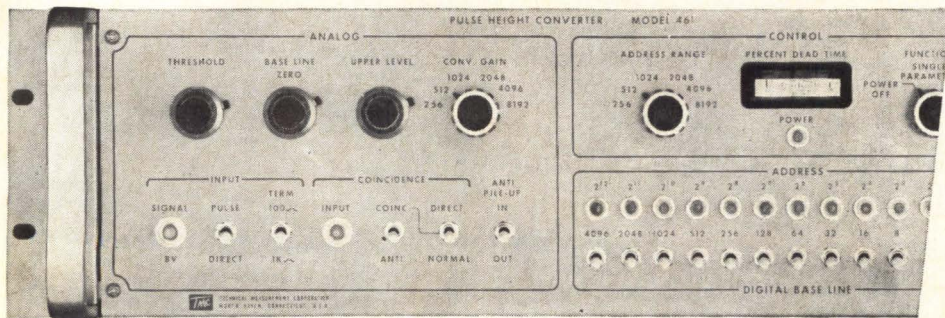
NCR

The National Cash Register Company[®]
ELECTRONICS DIVISION
2807 W. El Segundo Blvd., Hawthorne, Calif.
Telephone: (213) 777-7296
A equal-opportunity employer



CIRCLE NO. 900 ON INQUIRY CARD

THE "NONE-BETTER" ADC



In resolution
In linearity
In flexibility

The Model 461 nuclear ADC features true resolution of 1 part in 8192 (expandable to 12,288) with $\pm 0.025\%$ integral and $\pm 1.0\%$ differential linearity, plus a highly stable 50-MHz digitizing rate. Anti-pileup and DC-restoration circuitry assure minimal distortion, even at count rates as high as 50 kHz.

Its single- and multi-parameter capabilities provide unparalleled versatility. As a starter, the Model 461 is compatible with all modular TMC 1024-channel and 4096-channel pulse height analyzers. Its output flexibility simplifies interface with all types of data storage and processing devices. The Model 461 is also available to GP computer manufacturers desiring a hi-performance ADC for nuclear analysis applications.

Write for complete technical data, Technical Measurement Corporation, 441 Washington Avenue, North Haven, Conn., 06473.

Better yet, call us collect today (203) 239-5270 or 2501. TELEX: 96-3421.

See it at the
APS Show, Booths 438-9.



lored to accept inputs from analog multiplexers, A-D converters, time code generators or tape search and control units. Either fixed or variable sampling rates are easily accommodated, and Binary or BCD codes can be used. Controls are provided for single or multiple block operation and writing speeds up to 100K tape characters per second are offered. The output magnetic tape is suitable for use by IBM 360 or RCA Spectra 70 computers. An optional transient recirculate mode (TRM) is available. Transient information on one or two channels captured by the buffer memory is recirculated for visual display and analysis on an oscilloscope. Electronic Engineering Company of California, Santa Ana, California 92702.

Circle No. 211 on Inquiry Card

ENCAPSULANT, DIELECTRIC AND BONDING CEMENT

A new elastic ceramic dielectric material — a mixture of lead titanate, lead zirconate and borosilicate glass — was recently reported at the American Ceramic Society 20th Pacific Coast Regional Meeting. Called "Composition P," the material can be used for a variety of micro-electronic integrated circuit applications. It exhibits many useful characteristics not shared by other similar compositions known as polycrystalline lead-IVB multiple oxides. It is a good insulating material, has a low dielectric constant, and demonstrates unusual elasticity. These properties permit Composition P to be used as a hermetic encapsulant, as a dielectric substance for printed capacitors, and as a metal-to-ceramic bonding cement. Because of its properties as an insulating material relatively free from the effects of porosity and "pinholing," Composition P has been used successfully as a printed glaze encapsulant to provide a protective coating and hermetic seal for micro-electronic devices, including capacitance and resistance elements. Composition P has a low dielectric constant — in the range of 10 to 100 — and has been used to fabricate printed thick film capacitors. Experimental printed capacitors (2100 picofarads per square inch) were observed to change less than 5 percent in capacitance and dissipation factor for either a

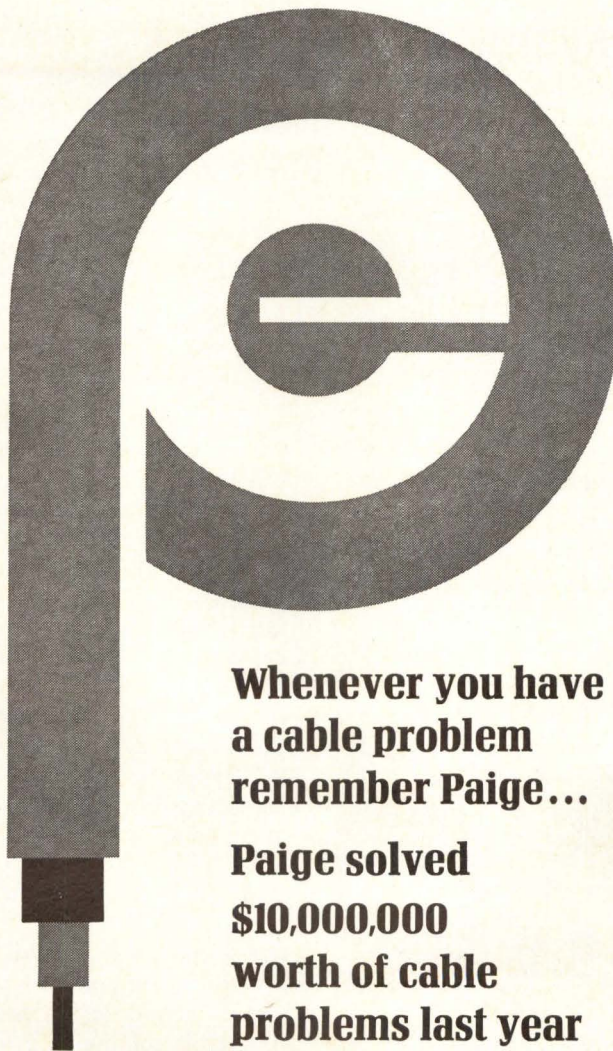
CIRCLE NO. 45 ON INQUIRY CARD

temperature change of 0 to 100°C or a frequency change of 100 hertz (cycles per second) to 100 megahertz (million cycles per second). In addition, because of its unusual elastic properties, Composition P has also been used as a bonding cement for joining metals to ceramic materials. This application is unique in that Composition P can bond two dissimilar materials which differ substantially in their thermal coefficients of expansion. For example, excellent results have been obtained when bonding a bulk silver ribbon (thermal coefficient of expansion is 191×10^{-7}), measuring five mils thick and ten mils wide, to an alumina substrate (thermal coefficient of expansion is 60×10^{-7}). IBM Components Division, East Fishkill, New York.

Circle No. 206 on Inquiry Card

BUFFERED MAG-TAPE MEMORIES

A recently announced line of buffered magnetic tape memories said to be the first offered as standard products, are priced significantly lower than previous, custom-made buffered tape memories. According to the manufacturer, they offer the computer and digital system user a range of tape transport speeds, recording densities, transfer rates and core memory capacities unprecedented in buffered tape memories. The memories, models BTM7, BTM9, BTM11 and BTM12, consist of a digital tape transport with data electronics, magnetic core memory, control panel, d-c power supply and equipment cabinet. They accept asynchronous digital data over a wide range of character rates. The incoming data are stored and recorded in computer-compatible format on magnetic tape. Integrated-circuit control logic permits the buffered tape memories to interface easily with the user's data sources. Optional data conversion and formatting equipment is also available. Flexibility of tape and core memory components enables the BTM models to produce computer-compatible taped data with continuous input rates from zero to 85,000 bytes per second (at 150 ips and 800 bpi with a 4,096-word core memory). Short term data transfer rates up to 500,000 bytes per second are achieved. Size of the data blocks may be varied



**Whenever you have
a cable problem
remember Paige...**

**Paige solved
\$10,000,000
worth of cable
problems last year**

What kind of problem? — design, engineering, availability, delivery, quality control, price?

"Total Service" — Paige solves them all because Paige is a unique organization of specialists. Our entire business, for more than 20 years, has been the design, engineering and supply of electrical and electronic cables.

Every kind of cable — Paige supplies cables for communications, control, data processing, electronic equipments, instrumentation, signal, TV, light and power.

"Problem cables" — Paige is staffed and equipped to supply custom cables which require advanced engineering and often special production equipment.

Saves time and money — Paige becomes an arm of your business. You get all the advantages of a team of specialists at no cost. In fact, you usually pay less for the cable and get faster delivery.



Want more information? — Paige has supplied many of this country's largest corporations as well as its most sensitive Government agencies. For complete information, write for the new brochure, "The Total Service for Wire and Cable".

Paige Electric Corp.

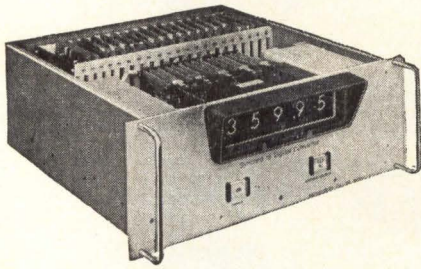
10 Commerce Court, Newark, New Jersey 07102

CIRCLE NO. 46 ON INQUIRY CARD



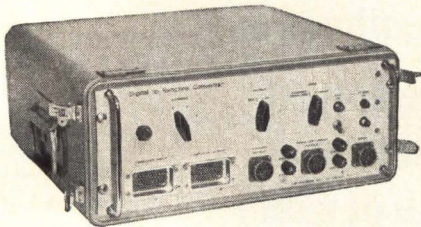
Astrosystems Inc.

Advanced Instrumentation



Synchro-to-Digital Converters

A simple, reliable, accurate method of high resolution conversion with **resolution and accuracy to 18 bits**. Available with straight binary code or BCD code outputs. Ideally suited for use as an interface between analog pickoffs and digital computers or off-line equipment.

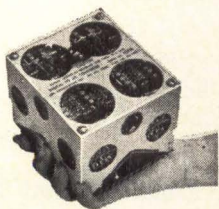


Digital-to-Synchro Converters Digital-to-AC Analog Converters

ASI Converters accept and register digital angles in binary or BCD code and convert these inputs to the equivalent synchro or resolver voltages. Digital-to-Analog AC models convert digital input information to linear AC output signals.

Single-speed resolution and accuracies are available up to **18 bits**.

Miniature Solid-State Airborne Units



All solid-state converters featuring high density packaging and ultra-reliability. Available as:
Digital-to-Synchro

Converters; Synchro-to-Digital Converters; Digital-to-AC Analog Converters; AC Analog-to-Digital Converters.

Astrosystems Inc.

Advanced Instrumentation

6 Nevada Drive, New Hyde Park,
New York 11040 • (516) 328-1600

CIRCLE NO. 47 ON INQUIRY CARD

from 12 bytes, the minimum computer-compatible length, to the maximum capacity of the core memory used — as high as 16,384 bytes. The BTM models can record data in either 7-track or 9-track format, with vertical and longitudinal parity generated for both. Cyclic redundancy characters are recorded in the 9-track format.

Circle No. 204 on Inquiry Card

MASS CORE MEMORY

A mass core memory with a capacity range of 5 to 20 million bits has a full cycle time of 2.5 microseconds for sizes up to 10 million bits and 2.75 microseconds for larger sizes up to 20 million bits. The unit's design provides for a high degree of modularity from the standpoint of total capacity and word lengths. It is a non-volatile data storage and retrieval device that allows for a simplified two-wire memory device. The 2-1/2D selection scheme used permits use of an efficient near-square stack array and yet takes advantage of the economies of coincident current road selection. This technique, combined with a unique sensing device, makes the memory reliable and economical for use in a number of applications. Characteristics of the memory make it suitable for use as a mass storage system. High reliability and low maintenance (functional organization) coupled with high data transfer rate and no latency, enforce its position in a computer system. The memory can be integrated into most computer systems without hardware modification to existing equipment by means of a controller unit. Systems without additional core storage capacity can communicate with the main memory through an I/O channel. Fabri-Tek, Inc., Minneapolis, Minn.

Circle No. 208 on Inquiry Card

LOW-COST UNIVERSAL MEMORY SYSTEM

A compact, low-cost, 1024 word by one bit coincident memory occupying only 214 cubic inches has been announced by Ferroxcube Corporation. The FI-1 Core Memory System, which incorporates integrated circuits, is suitable for a wide variety of applications such as data transmission buffering, CRT refresh, data logging, formatting and general storage requirements. It contains address

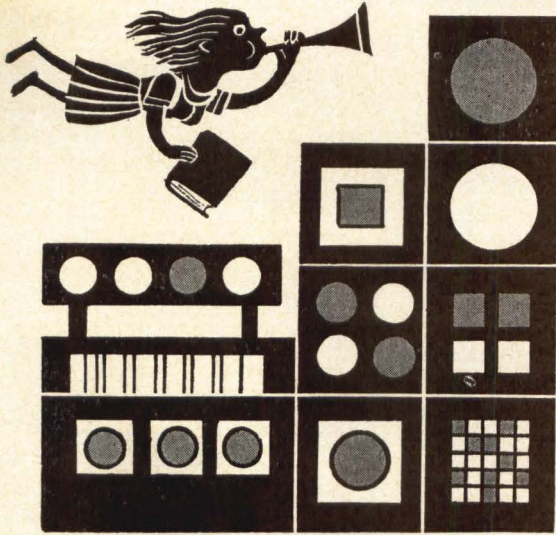
decoding, ferrite core drivers, data input/output circuits and internal timing logic for half cycle operation. A card slot is provided for an extender card or universal card to provide different operating modes. Read or write cycle time for the new memory system is 1 usec and the access time is 900 nsec. Power requirements are plus and minus 6 volts, and the output for Logic "0" is zero volts to +0.45 v at 30 ma, for Logic "1" it is +3.5 to +7.0 v (+Vcc). Designed to provide a maximum of flexibility for integration into a variety of packaging methods, the FI-1 is provided with a dust cover for bench use or remote mounting. With the cover removed, the assembly can be mounted to a 19-inch rack adapter panel or used as a sub-assembly within 3-1/2 or 5-1/4 inch high card racks. The FI-1 weighs less than 5 pounds and measures 3-11/16 x 11-1/8 x 5-7/32 inches with the dust cover. Price is \$650.00. Optional items are (1) Extender card: \$40.00; (2) Universal card: \$35.00. Ferroxcube Corp., Memory System Division, Englewood, Colorado.

Circle No. 209 on Inquiry Card

LOW-COST PCM TELEMTRY SIMULATOR

High-performance simulator of pulse-code modulation (PCM) signals provides all standard IRIG PCM telemetry formats, and also can be programmed to simulate pulse-duration modulation (PCM) telemetry signals. The 2795 has wide application to the test and checkout of data systems employing digital data transmission such as aerospace telemetry systems. Operating modes of the 2795 are switch selectable. It can generate formats having up to 599 digital words in the main frame, and another 599 words in a subcommutated frame, at word lengths of 1 to 33 bits. Serial output is available in any of the seven common digital codes, and a parallel binary (NRZC) output is supplied also. Bit rates from 1 bps to 2 Mbps are selectable. Signal disturbances such as drop-out, baseline offset, bit-rate jitter and noise can be introduced through an external input. At \$7000 the 2795 offers a low-cost self-contained checkout facility for digital data communications and processing systems. Electro-Mechanical Research, Inc., Sarasota, Florida.

Circle No. 207 on Inquiry Card



COMPUTER INDUSTRY ANNUAL 1967-68

**NOW AVAILABLE IN
HARD COVER EDITION**

The industry's first complete reference
guide and directory. 390 pages.

Over 33,000 copies already distributed.

FEATURING

COMPUTER PRIMER FOR MANAGEMENT

COMPUTER MANUFACTURERS' PROFILE . . . sales and earnings records, corporate highlights, stock price performance of 18 computer companies.

MARKET SURVEY . . . results of industrywide survey of annual sales volume of 400 types of computer-related products and services.

SURVEY OF TIME-SHARING FACILITIES

DIRECTORY OF PRODUCTS . . . contains over 400 types of computer-related products with corresponding manufacturers listed after each.

DIRECTORY OF SERVICES . . . contains nearly 200 service firms and 21 different types of computer-related services such as software development, equipment leasing, personnel recruitment, time-sharing etc.

MANUFACTURERS' INDEX . . . Alphabetical list of nearly 2000 suppliers of computer-related products and services. Includes corporate addresses, sales offices, national sales managers, number of employees and annual sales.

EQUIPMENT CHARACTERISTICS REVIEW . . . in-depth review

of all currently available computers, peripherals and major components. Includes 81 pages of Product Summary Charts to aid in equipment selection and competitive analyses. The following products are reviewed in detail:

DIGITAL COMPUTERS

ANALOG & HYBRID COMPUTERS

DATA COMMUNICATIONS TERMINALS & PROCESSORS

GRAPHIC DATA SYSTEMS & DEVICES

EDP FORMS

EXTERNAL STORAGE SYSTEMS

INTERNAL MEMORY SYSTEMS

DIGITAL MAGNETIC TAPE SYSTEMS

COMPUTER PRINTERS

PUNCHED CARD EQUIPMENT

PUNCHED TAPE EQUIPMENT

INPUT TYPEWRITERS & KEYBOARDS

LOGIC CIRCUITS & MODULES

SEND
COUPON
NOW

PRICE:
\$18.50

including
quarterly
updating
supplements.
Make checks
payable
to:
**SIMON &
SCHUSTER,
INC.**

SEND ORDERS TO:

SIMON & SCHUSTER
1 WEST 39th ST., N.Y. 10018

Enclosed is my check for \$.....
for.....copy(ies) of the 1967-68
Computer Industry Annual.

Enter my order for.....copy(ies)
of the 1967-68 Computer Industry Annual.

Bill me \$18.50 per copy plus shipping and
handling charges.

PLEASE PRINT

NAMETITLE

COMPANY

STREET

CITYSTATEZIP

SIGNATURE

ORGANIZATIONAL CLASSIFICATION OF MY COMPANY OR DEPARTMENT (check one best descriptor)

- | | |
|---------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| <input type="checkbox"/> 1. Mfgs. of computers, data processing equipment, or related systems or components. | <input type="checkbox"/> 5. EDP consulting & service organizations (excluding those connected with mfg. co.). |
| <input type="checkbox"/> 2. Mfgs. of consumer or industrial products (other than computer-related equipment). | <input type="checkbox"/> 6. Business & commercial (finance, banking, insurance, real-estate, wholesale & retail trade, etc.). |
| <input type="checkbox"/> 3. Government installations (federal, state or city including military). | <input type="checkbox"/> 7. Utilities (transportation, communications, electric, gas, etc.). |
| <input type="checkbox"/> 4. Educational institutions (colleges, universities, schools, etc.). | <input type="checkbox"/> 8. Other |

**Any day now
you computer
people will
make an
incredible
discovery:**



Nobody has made custom power supplies longer than Varo.

Or with a better performance record.

Or to tougher mil specs.

Funny we haven't crossed paths with you folks.

Funny?

It's incredible!

Let's discover each other.

Write Rex Carter, Varo, Inc., Static Power Division, 1600 Dallas North Parkway, Plano, Texas 75074.
TWX 9108605640
TELEX 73-2713



CIRCLE NO. 48 ON INQUIRY CARD



LITERATURE

IC Flat Packs

Data sheet gives complete information, including a standard configuration chart, on a standard line of flat-packs which utilizes such materials as Corning's 7052 hard glass, nickel iron cobalt, and alumina glass compositions. Also included is a chart showing GTI Flat-Pack Sealing Profiles, and a description of the Dix Model FP-VP-10 Flat-Pack Perimeter Sealer used to seal the standard line of flat-packs. Providence Division, GTI Corporation, Providence, Rhode Island.

Circle No. 318 on Inquiry Card

Subminiature Ceramic Capacitors

Bulletin H29 describes two new series of subminiature capacitors offering high capacitance in small size. Rated at 25 VDC over the temperature range -55°C to $+85^{\circ}\text{C}$, both series are available in capacitance values from $0.01\mu\text{f}$ to $0.15\mu\text{f}$ and meet or exceed the requirements of MIL-C-11015 (latest revision). They are designed for use in computers as well as for by-pass and coupling applications in any circuitry. Encapsulated in wax impregnated phenolic, both series are available with radial or axial tinned copper leads. Gulton Industries, Metuchen, New Jersey.

Circle No. 320 on Inquiry Card

Indicator Lights

Eight-page condensed catalog describes the entire Eldema line of indicator lights for military, industrial and commercial applications. Highlighted are Logic-Lites, indicators with built-in transistorized lamp driver networks, and the RFI/EMI shielded versions of lampholders which provide effective attenuation for interference shielding. Specifications for many varieties of holders and lens caps include those for the R-Lite family of relampable holders for use with the midget flange-based T-1 $\frac{3}{4}$ incandescent and T-2 neon lamps, D-holders designed to mate with corresponding plug-in C-Lite cartridges, and the T-Series family of relampable holders and lens caps for use with the T-3 $\frac{1}{4}$ bayonet-based incandescent and neon bulbs. Also detailed are the permanent

mounted type E-Lites, relampable H-Lites for military applications, and the permanently mounting subminiature J-Lites. Eldema, Compton, California.

Circle No. 321 on Inquiry Card

Motor Catalog

Eight-page instrument motor catalog fully covers a line of servo-control, induction, reluctance, and hysteresis synchronous motors. Each of the four types of motors are available with one of 20 standard gear trains from 0.67 to 1800 rpm, a dual bearing shaft support, and a modernized epoxy-insulated stator. Amphenol Controls Division, Amphenol Corporation, Janesville, Wisc.

Circle No. 322 on Inquiry Card

Relays, Time Delays

Eight-page brochure provides technical data on the complete line of Leach relays and time delay relays. Electrical, physical and environmental specifications are presented for: subminiature relays, dry circuit to 10 amps; power and control relays, 5 to 15 amps; power contactors, 20 to 400 amps; electronic time delays, 50 ms to 200 minutes. Leach Corporation, San Marino, Calif. 91108.

Circle No. 300 on Inquiry Card

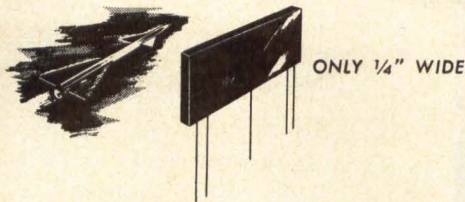
Test Instruments

Thirty-two page document provides complete information on instruments built by the three manufacturing plants of Honeywell's Test Instrument Division located in Denver, Colo.; San Diego, Calif. and Annapolis, Md. Products built by the division include precision analog and digital measuring and recording instruments, signal conditioning and monitoring equipment, laboratory standards, biomedical systems, EMI/RFI surveillance and analysis equipment, and data logger systems. The reference guide also contains information about the division's nationwide network of metrology laboratories that provide repair and calibration service to users of such equipment.

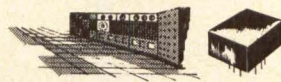
Circle No. 301 on Inquiry Card

ESC DELAY LINES

breakthrough in high density packaging



as sophisticated as your application



An example of ESC's sophisticated design capability is our Model 54-67 (Size: 3"L x 1/4"W x 1 1/2"H). Used in an airborne application, this rugged flat pack unit with an overall thickness of only 1/4" is an excellent example of high density packaging. It has a time delay of 29 usec. with a tap at 11 usec. The rise time is 1.8 usec. maximum with an impedance of 400 ohms and an attenuation of 2 db maximum. It meets the requirements of MIL-D-23859A. The delay line which this unit replaced occupied over three times the volume as the 54-67.

Our Model 13A27 (Size: .490"L x .490"W x .370"H) is transfer molded and illustrates a low cost, high production run unit. Designed for printed circuit board use in a computer application, the 13A27 has become one of a series of "custom standards" to a valued ESC customer. It has a time delay of 7 nsec. with taps at 4, 2 and 1 nsec. ESC's staff of nine design engineers will be pleased to help you solve your delay line and filter problems. Write for complete catalog.



ESC ELECTRONICS CORPORATION

534 BERGEN BOULEVARD PALISADES PARK, N.J. 07650 (201) 947-0400

World's Leading Producer of Delay Lines

CIRCLE NO. 49 ON INQUIRY CARD

Mercury-Wetted Relays

Two engineering manuals describe Clare mercury-wetted contact relays for wired assemblies and printed circuit board applications. All of the relays incorporate the low, constant contact resistant characteristics of Clare HG relays; no contact bounce, maximum reliability over 22×10^9 operations and switching speeds as fast as 1 ms. C. P. Clare & Co., Chicago, Illinois.

Circle No. 253 on Inquiry Card

Design Considerations For Glass Flexible Fiber Optics

Six-page brochure describes optical parameters, chemical resistance, mechanical and environmental characteristics, and end finishing procedures for glass flexible fiber optics. It contains information that system designers can use as design parameters. A table on chemical resistance, for example, shows test conditions in terms of time and temperature and resulting transmission changes, if any, when the fiber optics were subjected to sulphuric acid, engine oil, water, ethylene glycol and gasoline. Other charts, diagrams and graphs include life test results and humidity findings. A detailed explanation of end

finishing requirements for glass flexible fiber optics also is given. An accompanying graph shows specific results in transmission as a function of length for various techniques, including (1) epoxy termination with grinding and polishing, (2) grinding and polishing, (3) the theoretical transmission over length, (4) laser cut, and (5) razor blade cut. Corning Glass Works, Corning, N. Y. Circle No. 254 on Inquiry Card

Graphics Terminal

Twelve-page brochure describes the Adage Graphics Terminal, a comprehensive, general-purpose CRT display system. Included is information describing system highlights, system concept, standard models AGT/10, AGT/30, and AGT/50, as well as standard options and software. The terminal is said to represent a technological breakthrough in the field of computer graphics because of its extraordinary image-processing power which makes possible dynamic 3-D displays which move with full six degrees of freedom. Adage, Inc., 1079 Commonwealth Avenue, Boston, Mass. 02215.

Circle No. 255 on Inquiry Card

Miniature Switches, Relays, Readouts

A twelve-page catalog called Design Ideas for Engineers, features an expanding section for miniature electronic switches, remote control relays, readout indicators and pilot lights, ceramic terminal strips, and machined aluminum knobs. Of special interest to engineers is Alco's "pull to unlock" lever switches designed to safeguard against accidents, 3-pole and 4-pole miniature push button switches, motor start power switches, 12-position adjustable-stop miniature rotary switches, and an isolation relay for industrial remote control applications. Each product section has complete listings and prices, dimensioned drawings, and engineering specifications. Alco Electronic Products, Inc., Lawrence, Massachusetts. Circle No. 312 on Inquiry Card

Precision Relay Sockets

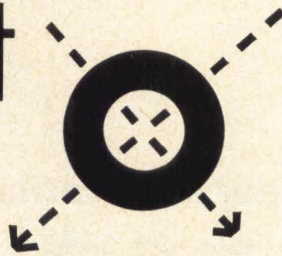
Six-page brochure describes Series 145-8 precision miniature relay sockets for use with plug-in relays. Various universal models are available with 8, 10, 14 and 20 fixed or removable contacts and solderless crimp terminations. Fixed contact types have a choice of solder cups and turret terminals for direct wiring or dip solder pin termination for printed circuit assembly. Mounting styles include tapped inserts with studs fixed in molding for top chassis mounting, through hole, or tapped inserts with removable standoffs and screws for mounting on either side of chassis or panel. Contacts are spring temper copper alloy with gold plate. Molding material is glass reinforced Diallyl Phthalate Type GDI-30 per MIL-P-19833 specifications. Continental Connector Corporation, 34-63 56th Street, Woodside, N. Y. 11377.

Circle No. 304 on Inquiry Card

Neon Glow Lamps

Eight-page illustrated brochure describing neon glow lamps for indicator applications, circuit components, and voltage regulators, provides complete information on evaluating and applying neon glow lamps including discussions on light output, longevity and external conditions acting on the lamp. The brochure includes an ionization time vs. percent over-voltage graph, plus a circuit drawing showing various breakdown measurements. Signalite Incorporated, 1933 Heck Avenue, Neptune, New Jersey. Circle No. 308 on Inquiry Card

Fly First Class at Tourist Prices



WITH A RAYTHEON MEMORY...

Raytheon Computer's new Model 300 memory is now available at more attractive prices and in a wider range of sizes due to expanded production capacity. ■ The Model 300 is a 2½D core memory with full cycle time of 900 nanoseconds. Typical access time is 350 nanoseconds. A single vertical drawer houses a complete memory module including stack and electronics. There are two basic modules—8K by 36 bits and 16K by 18 bits—and memories up to 8K by 144 bits or 16K by 72 bits are readily assembled. Best of all, production units will soon be available on a 60-90 day basis. ■ Complete technical, pricing and delivery data is yours in not quite 900 nanoseconds, but almost as fast. Write or call today. Raytheon Computer, 2700 S. Fairview St., Santa Ana, California 92704. Phone (714) 546-7160.



CIRCLE NO. 50 ON INQUIRY CARD

Telemetry Systems Guideline

Bulletin 36 is a guideline to assist in selecting Stevens Telemetry Systems for data collection, transmission, storage and display. Such systems can be used for data handling of variables such as: flow-rate, gate movement, volume, water level, temperature, etc. A chart shows the various combinations of encoders, transmitters and receivers that can be combined into various systems. The bulletin discusses the advantages and disadvantages of analog, incremental digital and total message digital systems. Information is included on economy, reliability and operation distance. A section on communication channels is included since the system will often be determined by the channel available. Leupold & Stevens Instruments, Inc., Portland, Oregon.

Circle No. 313 on Inquiry Card

16-Bit Data Generator

Technical Bulletin 201 describes a \$680.00 data generator, Model 201, offering 16-bit word lengths, variable

baseline offset to $\pm 10V$, 1-10V NRZ data outputs, and clock rates to 10 MHz. Methods for obtaining variable parameter RZ pulse outputs, extended program outputs and multiple parallel channels are described and information is given regarding pulse generators that may be used as clock source. Datapulse, Inc., A Subsidiary of Systron-Donner Corporation, Culver City, California.

Circle No. 314 on Inquiry Card

Disc Pack

Complete brochure is now available on the new Memorex Mark I disc pack, an advanced random access memory storage media for computers, said to have a high level of performance reliability and ability to reduce access time. Basically an assembly of six discs providing 10 recording surfaces and enclosed in a heavy-duty dust proof container, the Mark I is mechanically and operationally compatible with most existing disc drives. It can be used with drives that record on 100 tracks per recording surface, such as the IBM 1311, or with higher density drives

such as the IBM 2311, which records on 200 tracks. Memorex Corporation, Santa Clara, California.

Circle No. 315 on Inquiry Card

Measure Film Thickness

Four-page folder describes and illustrates a new H/I interference microscope featuring two special interference objectives for thin film thickness measurements with resolving powers of 0.6 and 1.5. William J. Hacker & Co., Inc., West Caldwell, New Jersey.

Circle No. 316 on Inquiry Card

Miniature Ceramic Capacitors

Four 4-page bulletins provide mechanical, electrical and performance specifications on new ceramic capacitors. Series C-331/C-332 and C-333 are miniature capacitors, Class I and Class II respectively, for low loss commercial applications; Class CV sub and ultra-miniature capacitors are designed to bring military environmental performance to the commercial and industrial user. MEPCO, INC., Morristown, N. J.

Circle No. 317 on Inquiry Card

Calibrated Delay Units

Two new calibrated delay units for high frequency RF, pulse and digital applications, feature selectable delays up to 60 ns with better than 1% accuracy and bandpass over 1000 MHz. The manufacturer states the units have been designed to meet either laboratory or systems requirements for precise phase delay measurements between two signals and for calibrating high speed oscilloscope time bases and other fast sweeps. Model 1202A provides delays from 1 to 60 ns in steps of 1 ns. Model 1203 covers the delay range from 0.25 to 60.75 ns, and includes a 0.3 ns delay vernier to provide continuously variable delays over the range. In both models, delays are selected by simple front-panel switches designed specifically for high-frequency use. VSWR is typically 1.05 at 1000 MHz and delay accuracy is specified at 1% or 0.05 ns. Insertion delay is approximately 4 ns in the 1202A and approximately 6.5 ns in the 1203. Gralex Industries Incorporated, Copiague, N.Y.

Circle No. 224 on Inquiry Card

Miniature Ceramic Capacitors

Two-color, six-page short form catalog of miniature ceramic capacitors for military and industrial applications lists all standard USCC ceramic capacitors along with catalog information. Included are typical special capacitor configurations also available. The catalog shows miniature ceramic capacitors for tubular, rectangular, square, round and chip shapes for precision and commercial uses. Also included are general specifications, ordering information and a capacitance change vs. temperature graph. U.S. Capacitor Corporation, 2151 No. Lincoln Street, Burbank, California 91504.

Circle No. 311 on Inquiry Card

Electronic Counters & Controllers

A series of four bulletins describing a new line of electronic counters and controllers has been released by Beckman Instruments, Inc. The 6200 Series of counters and timers includes seven instruments designed specifically for use in industrial applications where requirements dictate compact and reliable instrumentation. The bulletins cover instrument features, typical applications, and complete technical specifications. A photo of each instrument, prices, accessories and ordering information are also included. Although these instruments are primarily for industrial use, they will fit many laboratory applications equally well. Beckman Instruments, Inc., 2200 Wright Avenue, Richmond, Calif. 94804.

Circle No. 306 on Inquiry Card

Hybrid Techniques

Free technical notes describe new hybrid (analog/digital) techniques which offer significant advantages over existing analog circuits. Functions such as multiplication, integration, polar-to-rectangular conversion, ramp (stairstep) generation, D to A conversion, etc., are accomplished through the combination of a few basic "Hybrid Computing Modules." Hybrid Systems Corp., 127 Alewife Brook Parkway, Cambridge, Mass. 02140.

Circle No. 307 on Inquiry Card

Static Inverters for Emergency Power

Six-page illustrated booklet, brochure SA-9929, describes single-phase, fixed-frequency inverters and provides complete mechanical and electrical specifications. Typical applications are emergency a-c power supplies for plant instrumentation and control or well-regulated power sources for normal operation of data processing equipment. Fixed-frequency inverters can also supply short-term power for orderly plant shutdown or while starting auxiliary generators in case of utility power failure. Westinghouse Electric Corporation, P.O. Box 868, Pittsburgh, Pa.

Circle No. 305 on Inquiry Card

Connecto-Blok System

Sixteen-page bulletin, 500.1, contains complete descriptions and photographs of typical applications, showing reliability, high-density wiring, easy access for trouble shooting, and many other advantages as applied to data processing, communication links, information systems, telemetry, signal control and every place where high density wiring is terminated or connected. Technical catalog information containing product dimensions is included. The Thomas & Betts Co., Elizabeth, New Jersey.

Circle No. 309 on Inquiry Card

FREE!



air damping
dashpot

AIRPOT

a basic component for

TIME DELAY

VIBRATION DAMPING

SYSTEM STABILIZATION

... for a wide variety of environmentally severe military and industrial applications.

AIRPOT consists of a low expansion, precision bore, frictionless cylinder and graphite carbon piston encased in a high-impact protective housing.

Send for bulletin to select your FREE AIRPOT model without cost or obligation.

AIRPOT DIVISION ELECTRIC REGULATOR CORPORATION

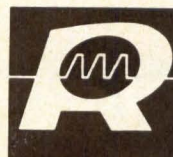
Pearl Street, Norwalk, Connecticut

CIRCLE NO. 51 ON INQUIRY CARD

SCIENTIST/ENGINEER DIGITAL COMMUNICATIONS SYSTEMS

Continuing expansion of our digital communications capability has created a new requirement for a senior level scientist/engineer with advanced education to head a small technical staff. The responsibilities of the staff are to establish the long-range technical objectives of our Data Systems Engineering Department currently employing in excess of 100 engineers, to determine technical requirements to meet the objectives, and to assist in implementation of the resulting development plan. The department is engaged in work in the field of military digital communications and currently designs and builds equipment for Communication Message Centers. Greater expansion into automated equipment is planned and eventually capability will be expanded into total systems for digital voice, message, data and document transmission. Applicant must have a minimum of ten years experience in military communications and electronics system design and analysis. Application of digital computers and understanding of computer programming are mandatory. Experience in analysis of transmission links, development of modems, knowledge of switching theory, bandwidth compression techniques and electronic scanning techniques are desired but not required. PhD required, salary open. Radiation Incorporated is one of the nation's leaders in the development of advanced electronic systems in areas of PCM telemetry, information and communication systems, data link systems, RF and microwave systems, automatic tracking antenna systems and satellite communication terminals. Technically oriented, with broad interests, we offer the opportunity for individual contribution and recognition. To explore your opportunity with Radiation, please forward your resume to

R. W. UNDERILL



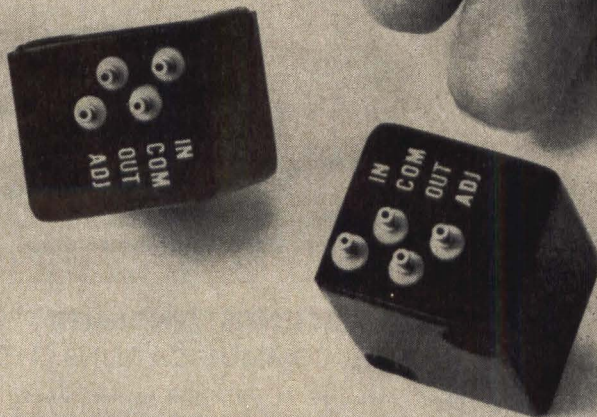
RADIATION
INCORPORATED

Melbourne, Florida 32901

An Equal Opportunity Employer

CIRCLE NO. 901 ON INQUIRY CARD

re Technipower's
CM-95 Series
power modules...
**they're
loaded!**



Technipower's miniature DC-DC power modules are packed with extras not found in other point-of-load regulators.

E.g.:

- Full 1.5 ampere capability with simple chassis mount or specially designed heat sink;
- Fully operational without adding external components;
- Complete line of output voltages, with either positive-common or negative-common versions;
- Easily mounted — input and output terminals are insulated from case;
- Protected against output shorts;
- \$30 each — much less in quantity!

Specifications include $\cong 200:1$ input ripple attenuation, $\pm 0.5\%$ regulation for a full 30% input or full load change, output voltage adjustment $\pm 5\%$, and operation to 95°C case temperature.

Write or call for information.



TECHNIPOWER

A BENRUS Subsidiary

Benrus Center, Ridgefield, Connecticut 06877

Phone: (203) 438-0333 TWX: 710-450-3631



**SALES
OFFICES**

BOSTON

Lindsay H. Caldwell
Professional Bldg.
Baker Ave.
W. Concord, Mass.
phone: (617) 369-6660

NEW YORK

Kaiser, McElwain, Dolbey
Advertising Sales, Inc.
60 E. 42nd St.
New York, N.Y.
phone: (212) YU 6-2654

CHICAGO

Robert Dunn
2 N. Riverside Place
Chicago, Ill. 60645
phone: (312) 372-6266

Donald C. White
616 Dalton Place
Northbrook, Ill. 60062
phone: (312) 272-6459

LOS ANGELES

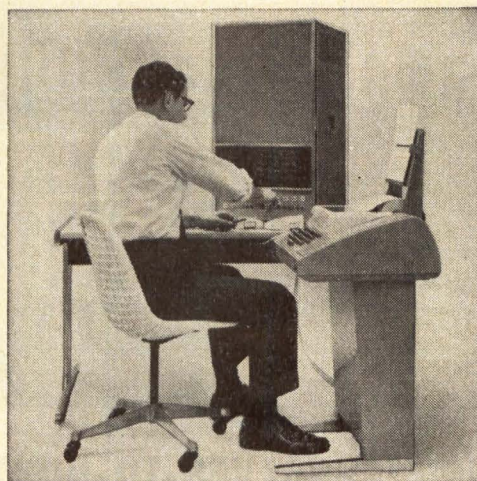
David Barton
672 So. Lafayette Park Pl.
Los Angeles 57, California
phone: (213) 382-1121

SAN FRANCISCO

David Barton
672 So. Lafayette Park Pl.
Los Angeles 57, California
phone: (213) 382-1121

FT. LAUDERDALE

Dan Wiper
2801 E. Oakland Park Blvd.
Ft. Lauderdale, Fla. 33308
phone: (305) 563-1376



**To the computer specialist
who figures he'd show 'em how,
if he ever got the chance:**

You've got the chance.

Now Hewlett-Packard's in the computer business... with a series of versatile, small, high-speed digital computers, so flexible, so well packaged that they're begging to go to work on the applications that only you can find... and sell. We've got the products. We invite you to apply your computer engineering expertise either to advancing our line of computers and software or to marketing them. The choice is yours.

Hewlett-Packard computers have been developed to give the working engineer a direct problem-solving interface with the electronic instruments manufactured by HP, letting him assemble his own computer-controlled instrumentation systems. They're designed to be equally effective as free-standing general-purpose problem solvers. And there's a wealth of experience behind these computers—developed and manufactured by a dynamic company that's spent 25 successful years in the measurement and data-handling business.

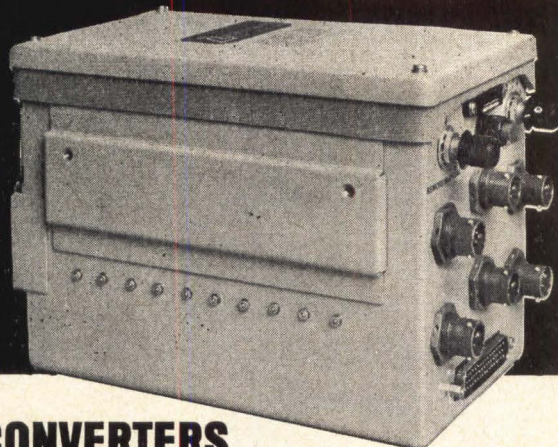
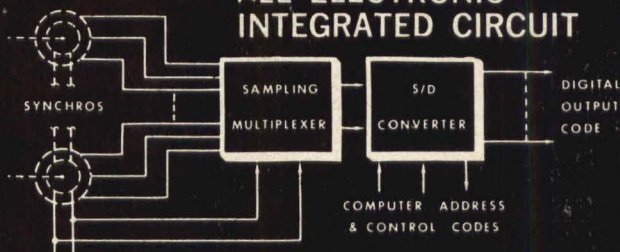
As Hewlett-Packard computers open whole new avenues of measurement capability, so they open new opportunities for the computer engineer whose education and experience are best rewarded by advancement in the field of computer technology. Choose your own course: in R&D, application engineering, software, marketing.

We think our computer is going to revolutionize the measurement and data-handling business. Sound interesting? Write Ray L. Wilbur, 1501 Page Mill Road, Palo Alto, California 94304. An equal opportunity employer.

HEWLETT  **PACKARD**

SHAFT ANGLE ENCODING

ALL ELECTRONIC-
INTEGRATED CIRCUIT



SYNCHRO/RESOLVER-TO-DIGITAL CONVERTERS

This modular equipment series provides a wide range of solid-state multi-channel synchro to digital converters with a binary output directly representing shaft angle • The input multiplexer can provide for any number of synchro inputs with programming via binary address or discrete control. Inputs are sampled, held and encoded at the peak of the synchro excitation voltage • Normal encoding rates are up to 800 per second for 400 Hz systems. The units provide dynamic accuracy of better than $\pm 6'$ of arc over optional temperature ranges of 0°C to 71°C or -54°C to 71°C. Resolution of up to 13 bits (2.63' of arc) is standard • Many special features such as data processors for dual speed synchros, binary to BCD conversion, digital to synchros conversion, linear multiplexed A/D conversion and custom computer interface signal circuits are available • Airborne unit design is consistent with MIL-E-5400 Class 2.

6 channels
6" x 5.2" x 7.75"
7.5 pounds
•
AIRBORNE
SERIES
SD 1000
•
GROUND
SERIES
SD 2000



Designers and manufacturers of CAPCODER and CAPLEXER Capacitive Charge Transfer Devices

TOWSON LABORATORIES, INC.

3500 N. PARKDALE AVE. • BALTIMORE, MD. 21211 • AREA CODE 301 367-4001

CIRCLE NO. 53 ON INQUIRY CARD

ADVERTISERS' INDEX

ADAR ASSOCIATES, INC.	52	LABORATORY FOR ELECTRONICS, INC.	
ALCO ELECTRONIC PRODUCTS	52	Commercial Products Group	82, 83
AMERICAN MICRO-SYSTEMS, INC.	Cover 3	MAGNE-HEAD	
ASTROSYSTEMS, INC.	88	Div. of General Instrument Corp.	81
AVTEL CORP.	78	MASTER SPECIALTIES CO.	29
BRAND-REX		MEMOREX CORP.	48, 49
Div. American Enka Corp.	16	MOTOROLA SEMICONDUCTOR PRODUCTS, INC.	21
CALMA CO.	84	NATIONAL CASH REGISTER CO.	22, 85
CINCH-GRAPHIK	26	PAIGE ELECTRIC	87
CONTEMPORARY ELECTRONICS	53	RADIATION, INC.	93
DATA-CRAFT CORP.	80	RAYTHEON COMPANY	
DIALIGHT CORP.	35	Industrial Computer Operation	79
DI/AN CONTROLS, INC.	30	RAYTHEON COMPUTER	92
DIGITRAN CO.	64	RCA ELECTRONIC COMPONENTS & DEVICES	1
DIT/MCO INTERNATIONAL		ROGERS CORP.	33
Div. of Xebec Corp.	32	SCIENTIFIC DATA SYSTEMS	25
ELECTRIC REGULATOR	93	SCM CORP.	19
ELECTRONIC MEMORIES	20	SYSTEM ENGINEERING LABORATORIES	2
ESC ELECTRONICS CORP.	91	TALLY CORP.	Cover 4
EX-CELL-O CORP.	14	TECHNICAL MEASUREMENTS CORP.	86
FAIRCHILD SEMICONDUCTOR	9, 10, 11	TECHNIPOWER, INC.	94
GENERAL ELECTRIC CO.		TERADYNE, INC.	4
Industrial Sales Div.	23	TEXAS INSTRUMENTS, INC.	12
HAYDON, A. W.	69	TORRINGTON MANUFACTURING CO.	
HEWLETT-PACKARD	5, 95	Air Impeller Div.	6
HITEMP WIRES CO.	61	TOWSON LABORATORIES, INC.	96
HONEYWELL		TRANSISTOR ELECTRONICS CORP.	18
Computer Control Div.	Cover 2	VARIAN DATA MACHINES	7, 15, 31
INTERDATA	13	VARO, INC.	90
INVAC CORP.	24	VERMONT RESEARCH CORP.	17
KATO ENGINEERING CO.	8	VERNITRON CORP.	27
KENNEDY CO.	60		

**American Micro-systems, Inc.
developed thick oxide
into ultra-thick (UTO)-
combined it with 2-phase logic.
Result:**



**Dual 50-bit Shift Register—Part No. R D 10 C
Our telephone number is (408) 246-0330**



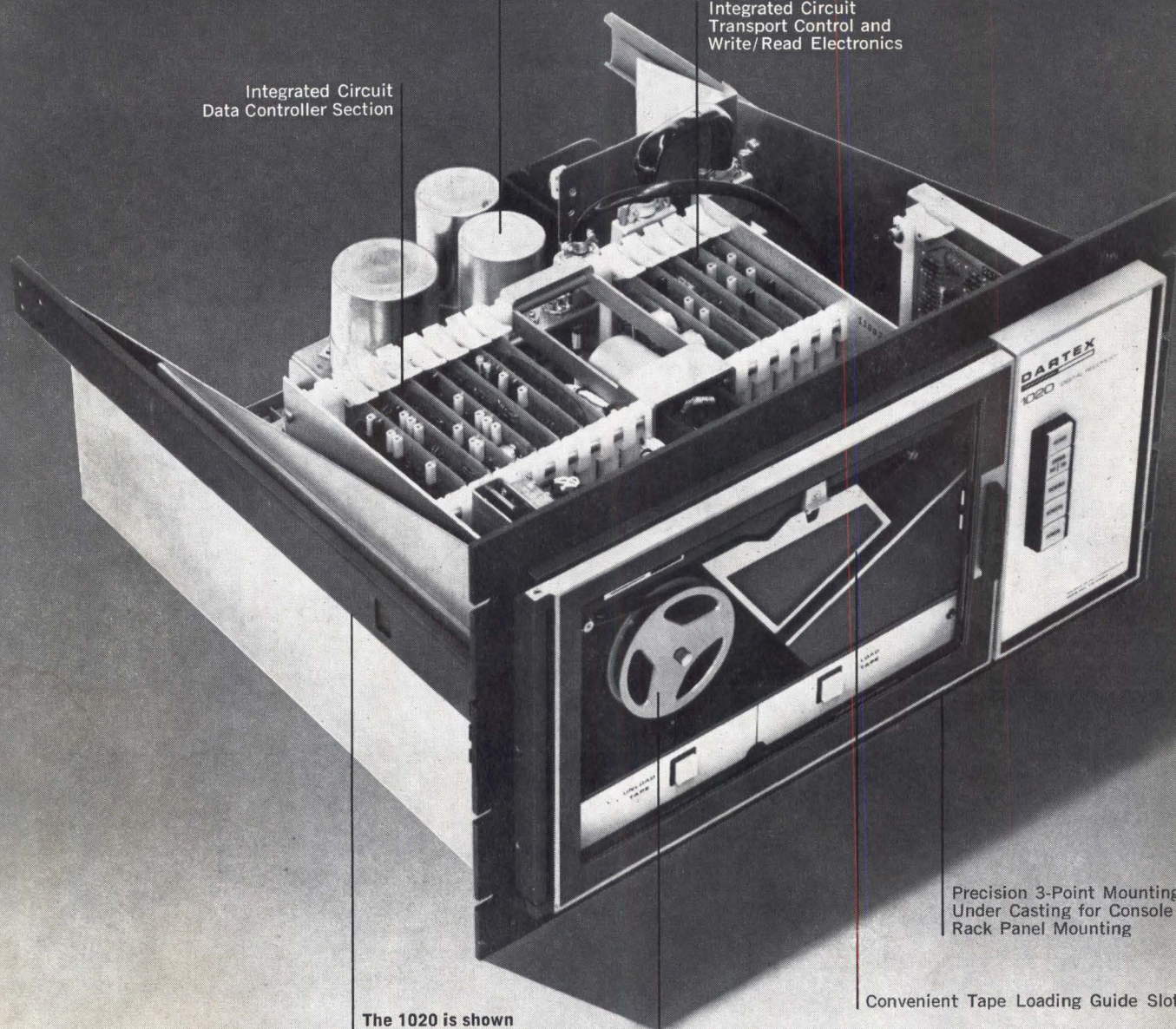
3800 Homestead Road, Santa Clara, California 95051

CIRCLE NO. 54 ON INQUIRY CARD

Solid State Power Supply—Surplus Capacity for External Devices

Integrated Circuit Transport Control and Write/Read Electronics

Integrated Circuit Data Controller Section



Precision 3-Point Mounting Pads Under Casting for Console or Rack Panel Mounting

Convenient Tape Loading Guide Slot

The 1020 is shown mounted in the Optional 19" Rack Mounting, with Control Panel, Manual Switches, Indicators, and Chassis Slides for easy access.

Interchangeable Tape Reel

Rewrite Machine

Basically, our new Tally 1020 Incremental Magnetic Tape Unit transfers data asynchronously at 120 characters per second and continuously at 1600 characters per second. □ We call it a rewrite machine because, uniquely among all incremental units, the Tally 1020 can back space and rewrite a single character (or block of characters) anywhere on the tape. □ Other features include error checking, simplified construction and maintenance, 280,000 character storage on a single 3" reel, and low tape wear because of single capstan drive. □ So if your data problems involve data transmission, computer input/output, numerical control, or the like, it will pay you to investigate the modern low cost Tally 1020.

Please address Tom Tracy, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone: (206) MA 4-0760. In Europe and the U.K., address Tally/APT, Ltd., 6a George Street, Croydon, Surrey, England. Phone: MUN 6838.

TALLY®