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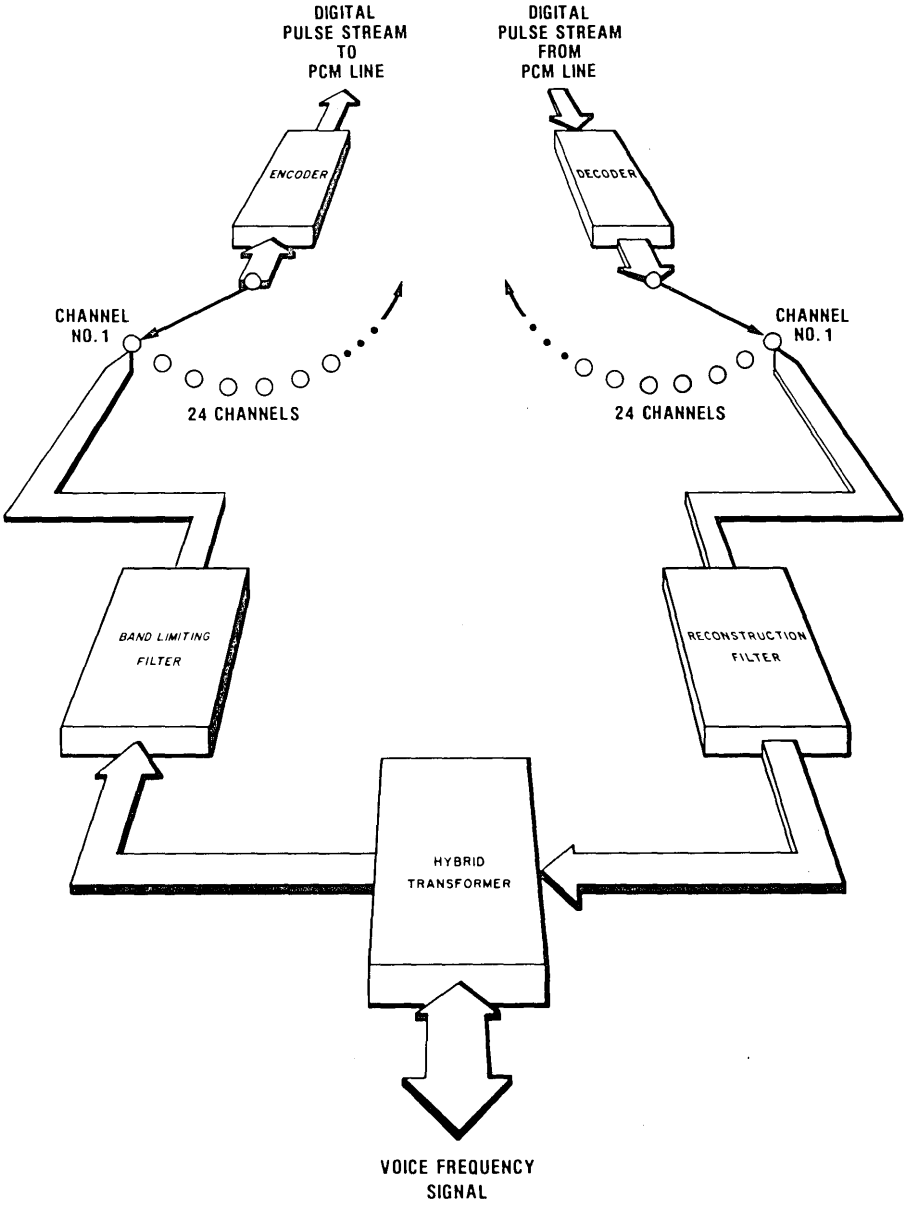
D4 DIGITAL CHANNEL BANK FAMILY



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THE D4 DIGITAL CHANNEL BANK FAMILY

J. J. Lang, Guest Editor

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D4 Digital Channel Bank Family:

Overview

By J. CHERNAK and J. J. LANG

(Manuscript received June 25, 1981)

This article presents an overview of the D4 Digital Bank Family and introduces a series of articles on the subject. The D4 family represents a collection of features and network applications derived from a single design, the basic D4 digital terminal.

In 1962, the first digital carrier system was introduced into the telephone plant as an alternative to metallic interoffice trunks. On this system 24 voice signals are amplitude sampled, time shared, and digitally encoded; each direction of transmission is on a single pair of copper wires. This results in a twelve-to-one improvement in efficiency in the use of copper pairs as compared with the two-wire metallic trunks. The first-generation channel bank is designated the D1 bank, the D1 standing for Digital, first generation. The D1 bank performs the time-shared sampling and digital encoding of the 24 voice signals into a 1.544 million pulses per second signal.

Since 1962 four generations of digital banks have been developed. The present generation—the subject of this special issue—is designated the D4 bank, and was introduced into the field at the end of 1976.

The success of digital banks and associated transmission facilities can be expressed by their penetration into the metropolitan interoffice network. Today, the digital facilities account for about 35 percent of the total metropolitan interoffice trunks. In terms of voice-circuit miles, the digital facilities provide 80 percent of the total, that is, 100 million out of a total of 125 million voice-circuit miles. On a growth basis, the digital implementation accounts for about 75 to 80 percent of this market. By the end of 1980, the Bell Operating Companies

(BOCs) were supplied approximately ten million digital bank channel ends consisting of D1, D2, D3, and the D4 families.

The development of each successive generation of D banks took place as advancements in component and circuit technology offered opportunities for new features, increased compactness, decreased power dissipation, and improved maintenance and reliability. These factors all led to better overall cost-effectiveness. Largely as a result of following the technology learning curve, it was possible, over the period 1962 to 1980, to lower the furnished cost to the BOCs of a typical interoffice exchange digital trunk by a factor of more than three.

The first three generations, D1, D2, and D3, offered a relatively modest set of features. For example, toll quality transmission started with D2. (It was also offered later on an optional basis for D1 as the D1D bank.) As another example, starting with D1, an increasing complement of special functions, normally provided through separate metallic facility terminals, was incorporated into the banks in the form of special service channel-unit circuit packs. The experience gained from these optional features in previous generations of banks led to the decision, during the planning for the D4 bank in 1974 and 1975, to provide for an architecture capable of accommodating on a plug-in basis an extremely broad complement of functions and features heretofore furnished by equipment in separate bay lineups. In time, this initial plan was broadened to include the design of new functions at the plug-in level, e.g., error correction for digital data channels, and at the systems level, e.g., *SLC**-96 carrier system for loop applications.

Two examples shall serve to illustrate the basic concept. The first is the D4 built-in multiplex. The D4 bank is designed for a capacity of 48 channels (the previous generation banks interfaced only 24-channel systems) with optional multiplex plug-ins to deliver either two DS-1 signals to two T1 24-channel lines, or one DS-1C signal to a T1C 48-channel line. [DS-1 is a 1.544-Mb/s bit stream containing 24 pulse code modulation (PCM) coded channels, and DS-1C is a 3.152-Mb/s bit stream containing 48 PCM coded channels.] By interconnecting two D4 banks and by employing another set of multiplex plug-ins, a DS-2 signal is generated for transmission over the T2 96-channel system. (DS-2 is a 6.312-Mb/s bit stream containing 96 PCM coded channels.) If yet another set of plug-ins containing lightwave transmitters and receivers is used, a signal at the DS-2 information rate is generated for transmission over lightguide. The concept of generating various digital signal rates by employing optional plug-ins in the bank results in significant economies as compared with providing the multiplex function with segregated equipment in a separate bay lineup. The econ-

* *SLC* is a trademark of Western Electric.

omies reflect not only the reduced material price and installation costs to the BOCs, but also shortened installation intervals.

A second example is the provision of digital data channels by means of a "dataport" plug-in. This dataport plug-in fits into the physical space of a D4 channel unit, even though the circuitry of the dataport is several times as complex. The dataport plug-in provides functions that otherwise require entire shelves of equipment designed in the early 1970s. This is achieved largely by increased component count per unit area in silicon integrated circuit technology and by the flexibility afforded by the D4 architecture. As we mentioned, the dataport actually incorporates features that are not available in earlier designs. An example is error correction of the digital data signals, which has not only the advantage of improved performance but more importantly shortens installation intervals by eliminating the need to test and select the T-carrier facilities for error performance.

The concept of offering a wide variety of capabilities on an optional basis through the basic D4 architecture proved very successful. It began a new era characterized by expansion of applications through integrating interfaces with other parts of the network. The result is a ubiquitous, flexible, and cost-effective realization of capabilities, which would not have been achieved by separate pieces of equipment. The ubiquity is a consequence of the pervasive deployment of D4 banks in the network. The flexibility stems from the plug-in nature of the realizations. The cost-effectiveness derives from benefits gained in many different phases in the life cycle of equipment, viz., design, manufacture, field engineering, installation, operation, maintenance, and network rearrangements.

When viewed in its entirety, this approach is seen to have brought about the "D4 Digital Bank Family," called the "D4 family" for short, which grew to include the following broad capabilities:

(*i*) Integrated interfaces for the digital line facilities, with interconnection capability for T1, T1C (two options), T2, and lightguide, using a set of D4 common plug-ins.

(*ii*) Integrated interfaces to metallic facilities for the provisioning of special access and private line arrangements by a set of D4 plug-ins called special service channel units.

(*iii*) Direct access for the Digital Data System for the Dataphone* Digital Service (DDS) by a set of plug-ins called "Dataports."

(*iv*) Integrated interfaces for the No. 1, 2, and 3 ESS (Electronic Switching Systems) trunks through channel unit plug-ins.

(*v*) A D4-technology-based subscriber digital carrier system, *SLC*-96, designed for "feeder" cable relief in loop applications. The first

* *Dataphone* is a service mark of AT&T.

three integrated interfaces for the digital line facilities were available with the initial D4 offering. The T2 and the lightguide interfaces were offered in 1979. Dataports were introduced into service in late 1978 and the *SLC*-96 system in the spring of 1979.

The first two articles in this issue describe the basic D4 bank and a maintenance bank designed to test and monitor D4 plug-ins. The basic D4 bank is the kernel for expanded applications, described in the fourth through the seventh articles: namely, the Subscriber Loop Carrier, the *SLC*-96 System, and the dataports for the Digital Data System. Articles eight through ten deal with technology: the physical design aspects of the D4 family, custom silicon integrated circuit design, and thin-film active filters.

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D4 Digital Channel Bank Family:

The Channel Bank

By C. R. CRUE, W. B. GAUNT, JR., J. H. GREEN, J. E. LANDRY, and D. A. SPIRES

(Manuscript received July 2, 1981)

The D4 channel bank is the most recent Western Electric product in an evolution of time-division multiplex terminals for digital transmission facilities. D4 incorporates many technical innovations relative to the earlier developed D1D, D2, and D3 channel banks but is fully compatible with these earlier banks. D4 banks may be operated in any of five different modes as required to connect to a particular digital carrier facility (T1, T1C, T2, or FT2). The D4 channel bank is partitioned into common equipment and channel units. The common equipment provides digital line interface, pulse code modulation coding and multiplexing, alarms, trunk processing power, power fusing, and distribution. Individual channel units provide the circuits that interface to external circuits. There are many different versions of channel units including standard interoffice voice-frequency trunk types and those supplying data and special services.

I. INTRODUCTION

The D4 channel bank was initially proposed as a complementary terminal development to the 3.152-Mb/s T1C line facility to enhance the cost-effectiveness of 48-channel applications.[1,2] As planning progressed, it became clear that because of the introduction of new technology in D4, and the inherent need for an end-to-end compatibility with the forerunner D1D, D2, and D3 channel banks,[3-9] the D4 architecture should be expanded to include 24- and 96-channel, as well as 48-channel, operations. Thus, the early objectives of the D4 were to

develop a more economical, flexible, digital terminal for T1C and T2 applications, as well as a smaller, lower priced, more reliable terminal for T1 applications. In addition, D4 was to have simplified maintenance and to incorporate technological advancements.

Each D4 bank is a completely self-contained, 48-channel terminal consisting of two 24-channel digroups, each with essentially separate common equipment sections and interchangeable digital line interface units. The predecessor 24-channel D3 design required 18 inches of vertical bay height plus space for an external fuse/alarm panel. Because of application of integrated circuit technology in the D4 design and incorporation of fusing into the channel bank frame, a size reduction of better than 2:1 was achieved. The result is that each D4 bank requires only about 19 inches of vertical height for the 48 channels. Electrical compatibility with earlier vintage banks has been realized through the use of the standard 7-5% bit, 15-segment, μ255 nonlinear coding characteristic, and the D3, D2, D1D basic frame and signaling format. D4 uses improved versions of the highly accurate and stable, D3 multiple-pole, resistor-capacitor (RC) active thin-film filters[10,11] to achieve transmission performance that meets toll-grade transmission objectives. The D4 bank can be universally used in direct, tandem, toll-connecting, and intertoll trunks. In addition, by giving each channel direct access to the digital bit stream, synchronous digital data or "dataport"[12,13] channels, for direct digital connectivity up to the 56-kb/s rate, is a reality. Like the D3 Unitized Bay (UTE), which includes Switched Maintenance Access System (SMAS)[14] relays for special services maintenance, versions of a D4 UTE are now available.

Additional features of the D4 bank include improved per-channel maintenance through increased access at the channel unit jack, per-channel trunk processing, and electronic features such as built-in 1000-Hz digital milliwatt for receiver checking and "signaling bit storage"[15] with extended carrier group alarm (CGA) timing. Formerly, CGA timing in digital systems would only allow a 0.3-second maximum out-of-frame condition to exist prior to bank shutdown, trunk conditioning, and office alarming. With the introduction of signaling storage, wherein past-state signaling information is stored and used to hold up the proper connection in the event of an out-of-frame condition, it became permissible to extend the CGA timing from 0.3 second to more than 2.0 seconds. This resulted in over a two-fold reduction of CGA outages and consequential reduction in the number of lost calls. Trunk processing that occurs during a CGA bank shutdown is handled by per-channel trunk processing relays under control of timing from the alarm control unit and the common relays in the trunk processing unit (TPU) plug-in. This has reduced the size, cost, and administration associated with trunk processing.

II. FUNCTIONAL OVERVIEW

2.1 General description

Figure 1 is a block diagram of the D4 bank. Channel units for two 24-channel digroups (designated *A* and *B*) are apparent, accompanied by common equipment that includes transmit, receive, alarm, trunk processing, and line interface units. Power is derived from the −48-volt office supply by means of a dc-to-dc converter unit. Two alarm units are used in all applications except for the special Mode 1, T1C application. Separate digital line interfaces and associated units, such as dual synchronizing/desynchronizing (syndes) units, are used to interface the digital line facilities. Since trunk processing relays are included within each channel unit, a simple dual control, common relay TPU is used. This unit houses one or two digital line equalizers (or line build-out networks) that plug into connectors on the TPU. Common equipment channel-counting options are administered on the TPU. This feature quickly restores a failed transmit or receive unit since there is no need to note and set the options on the new units before making the restoral. The power distribution unit provides a fused −48V distribution arrangement.

Channel units available for the D4 bank range from standard interoffice trunk types to data and special services. These units connect to common backplane signal busses that make all necessary connections to the common equipment, office equipment, and signaling systems.

2.2 Modes of operation

Figure 2 shows how the D4 banks interface with the digital hierarchy. Single D4 banks operating in Mode 2 or 3 have 48 voice-frequency (VF) channel interfaces to DS1C or DS1 rate facilities. Dual bank arrangements, where two D4 banks are connected together, have 96 VF channel interfaces to DS2 rate wire or FT2 lightwave facilities. These are designated Modes 4 and 5, respectively. Also provided is an additional DS1C rate interface (not compatible with the hierarchy), which is a low-cost D4-to-D4 connection designated as Mode 1.

D4 channel banks can be connected to any of four digital transmission facilities (T1, T1C, T2, or FT2). Configuration of the banks for interfacing a particular digital facility is accomplished by simply inserting an appropriate line interface unit (LIU), and in some cases, a snydes unit (SU) plug-in into the bank to set up a mode of operation. The mode configurations are illustrated in Figs. 3 and 4. In all but the FT2 facility connections, small plug-in equalizer or line build-out boards are installed to accommodate cable distances between the D4 channel banks and the office digital cross connect or office repeater bay. Table I summarizes the digital facility connections in terms of D4

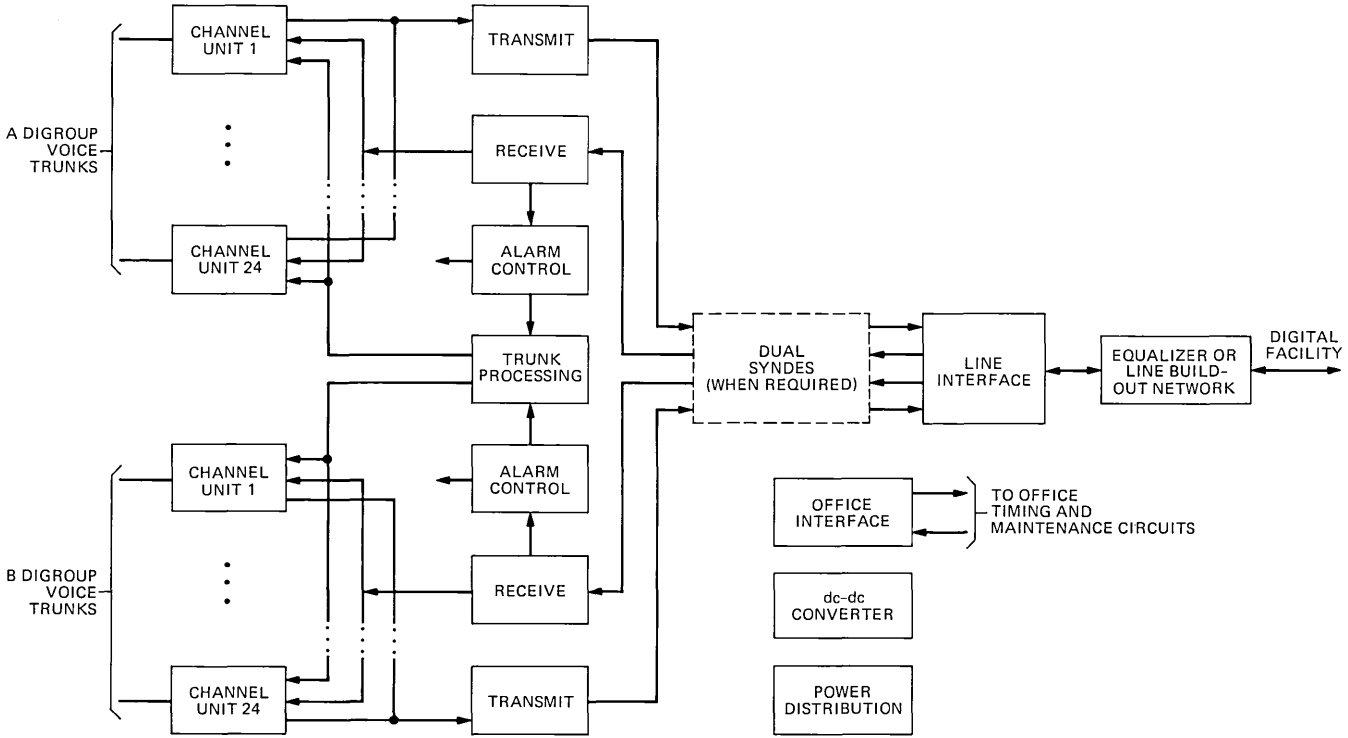

Fig. 1—The D4 channel bank.*

* Acronyms and abbreviations used in these figures are defined in the Glossary at the end of this paper.

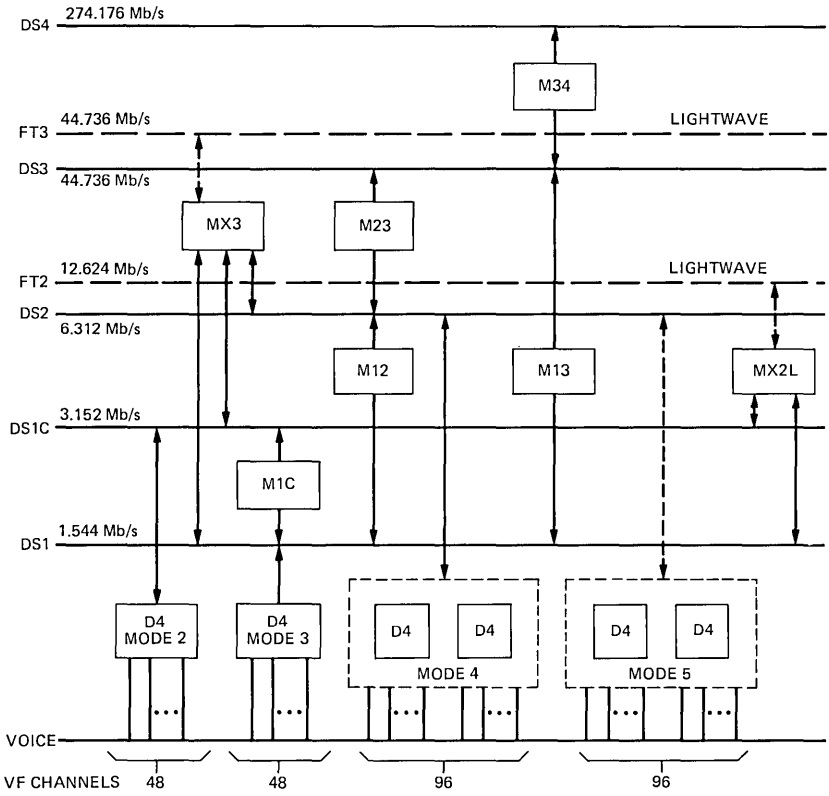

Fig. 2—D4 channel bank interfaces to the digital hierarchy.

Table I—Digital facility connections

D4 Mode	Digital Transmission Facility (System Bit Rate in Mb/s)		Number of Voice Channels	Number of Digroups	Compatible Digital Hierarchy Multiplexer
1	T1C	3.152	48	2	None
2	T1C	3.152	48	2	M1C
3	T1	1.544	24	1	—
4	T2	6.312	96	4	M12
5	FT2	12.624	96	4	MX2L

modes of operation, digital hierarchy multiplex compatibility, and number of voice channels and digroups.

There are two modes of operation over T1C digital facilities. Mode 1 (Fig. 3a) is a low-cost, dedicated D4-to-D4 connection that uses a single clock so that two digroups are synchronized and multiplexed by interleaving PCM bits from each digroup. Mode 2 (Fig. 3b) has a more flexible terminal capability because it uses a syndes unit and an M1C

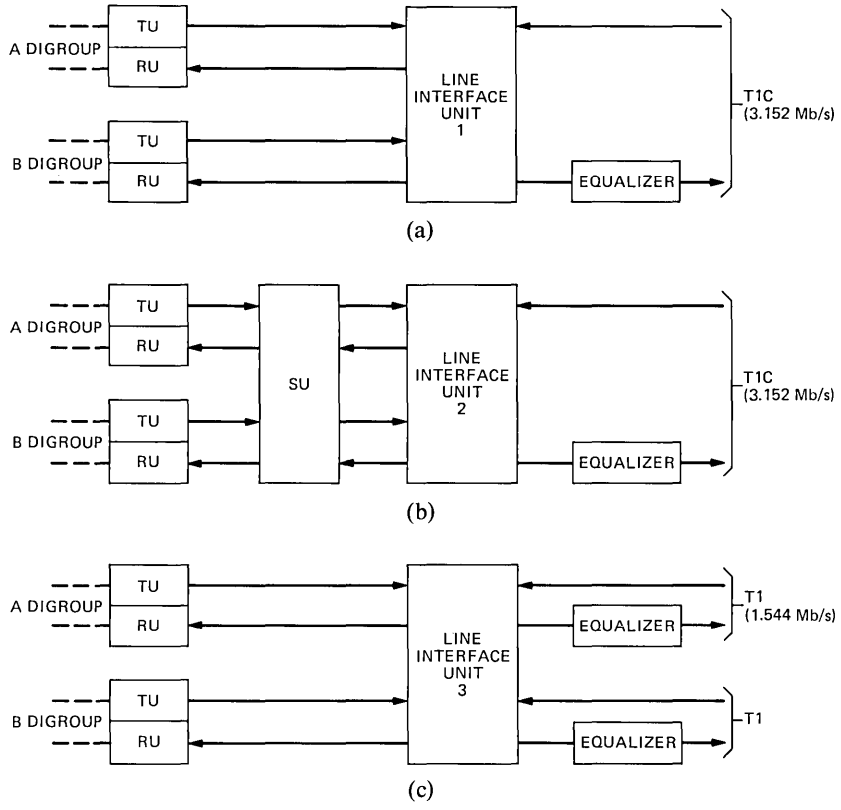

Fig. 3—D4 channel bank mode configurations. (a) Mode 1. (b) Mode 2. (c) Mode 3.

multiplex standard signal format. This mode connects the D4 bank to other digital terminals at the far end using the M1C Multiplexer. Mode 2 also provides alarm and M1C-compatible maintenance features. In addition, Modes 2, 4, and 5 have a unique in-service digroup test capability.

Mode 3 (Fig. 3c) electrically conditions the D4 bank for independent digroup transmission over separate T1 carrier digital lines. The two digroups are then compatible with a similarly configured D4 bank or with any arrangement of D3-, D2-, or D1D-type terminals. Alarming and trunk processing functions are provided on a per-digroup basis to allow for maintenance or restoral work to be done independently. In this mode, some common units such as the power converter, battery filter, and the LIU are shared between digroups.

Interface to T2 digital facilities is provided when two D4 banks are interconnected and each has line interface and syndes units to operate

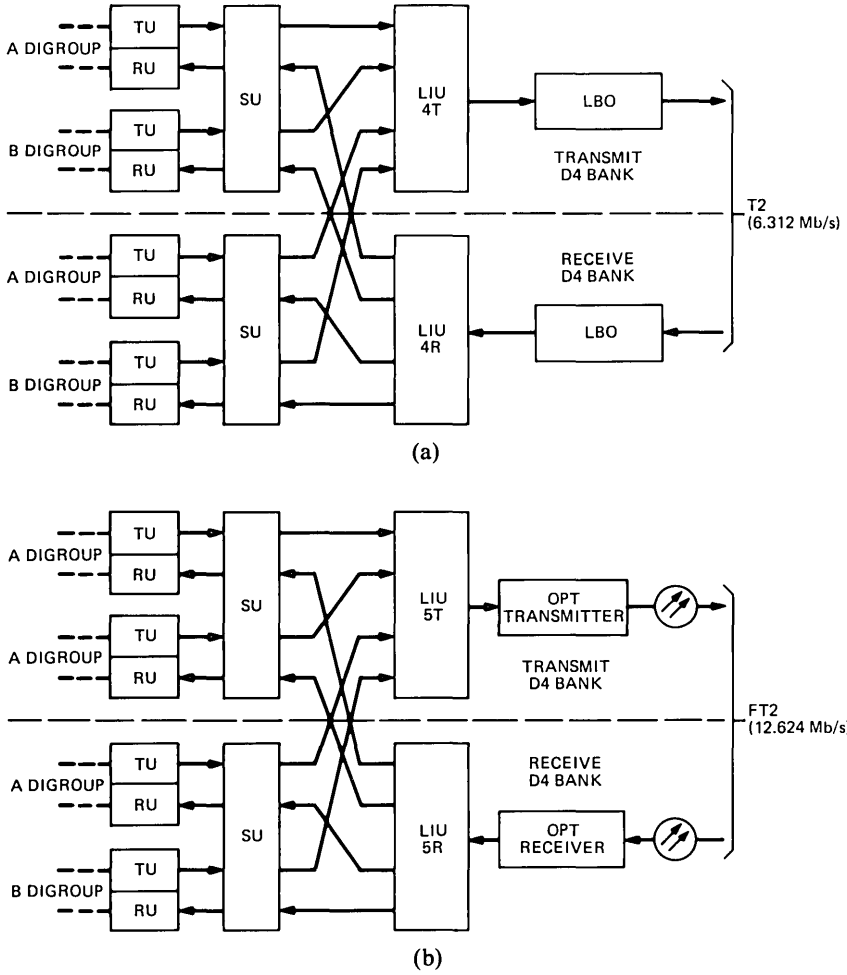

Fig. 4—D4 channel bank mode configurations. (a) Mode 4. (b) Mode 5.

in Mode 4 (Fig. 4a). In this mode, the banks provide an M12 Muldem-compatible signal format and alarm functions.

The most recent expansion of D4 digital facility interface capability is Mode 5 (Fig. 4b), which implements a lightwave system connection. This mode incorporates optical transducers and circuits in the channel banks, as well as multiplexing and coding circuits for optical transmission. The multiplexing circuits are similar to those used in Mode 4. A unique dipulse coding format is employed that takes advantage of the wide transmission bandwidth available and doubles the bit rate (compared to mode 4) to provide for bit-error detection equivalent to bipolar-violation detection employed with wire systems.

III. CHANNEL UNITS

D4 channel units make the D4 channel bank adaptable to a variety of application requirements. The channel unit designs have been responsive to the evolving electronics technology; the functionality and economy of the channel units have been important factors in the success of the D4 channel bank. This section describes conventional channel bank channel units. Other channel-unit designs meet special needs such as those of loop electronics and digital data transmission.

Channel units are the interface between the channel bank common equipment and the central office equipment. The common equipment interface is identical for all channel-unit circuits; the central office equipment interfaces change as a function of the type of service being supplied.

3.1 Generic functions

This section classifies the signals that flow through the channel units into general categories and describes the processing of these signals by the D4 channel unit.

The message signal is typically an analog voice-frequency signal with information flowing from each end of the connection to the other. The channel unit supplies level compensation and, in some cases, gain vs. frequency distortion compensation for each direction of transmission. The electronic processing of the message signal within the carrier system requires that each direction of transmission be separate. In some applications, the message signals for each direction of transmission are on separate pairs of wires at the voice frequency interface to the channel unit. Four-wire channel units are used for this class of application. In other cases, the voice-frequency interface is bi-directional, with the messages for each direction sharing a single pair of conductors for transmission. The appropriate channel unit for this application is called a two-wire channel unit. The circuitry of the two-wire channel unit interfaces between the external bi-directional two-wire interface and the internal four-wire unidirectional format.

All the above functions serve to interface between various external voice-frequency signals (with their associated degradations) and filtering and sampling circuits that reside on the channel unit but are identical for all applications. These circuits interface between a standard internal (to the channel unit) voice-frequency signal format and the pulse-amplitude-modulated and time-division multiplexed signals at the common equipment interface of the channel unit.

In most applications, the digital carrier system must transmit certain control signals in addition to the message signal. This control flow capability is used to oversee the dynamic nature of the traffic that may

be associated with the service. This process is called signaling and, for the purposes of this paper, the signals are subdivided as follows:

(*i*) *Supervisory* signals distinguish between the idle and busy states of a channel. These are typically dc signals that are applied either to the same conductors that carry the message signal or to separate conductors. Supervisory state transitions are used to

(*a*) Seize control of a circuit in response to a service initiation by a customer

(*b*) Oversee the flow of address information between originating and terminating switching machines

(*c*) Inform the originating switching machine when the called party answers or hangs up (control of billing and circuit availability).

Supervisory signals are two-state (busy/idle) signals and change infrequently relative to the digital carrier sampling rate. Robbed bit signaling, which results in 7-5% bit PCM encoding, is the technique typically used to transmit this information from one end of the carrier link to the other. The channel unit must detect the state from the central office equipment and reproduce the state to the central office equipment. Timing signals from the common equipment control the sample, hold, multiplex, and demultiplex functions that are performed in the channel unit to support the transmission of these signals.

(*ii*) *Address* signals transfer call routing information from the originating to the terminating office. These signals are most typically transmitted within the message frequency band and, therefore, require no special processing by the carrier system. For other applications, dc signals are used for addressing. Detection, transmission, and reproduction techniques are similar to those for supervisory signals. Addressing signals (dial pulses) change at a higher rate than do supervisory signals; and, therefore, dial pulse percent distortion performance becomes an important system characteristic.

(*iii*) *Alerting* is the process of indicating to the called party that a message is waiting. For most applications this function is controlled by the local office at the called-party end, which means that the carrier system is not involved. For some special services, the alerting is controlled from a remote office, and the carrier system must transmit information to control the low-frequency ringing signals. An additional dc two-state channel (similar to the supervisory channel) facilitates this function.

3.2 Channel-unit applications

The channel unit has the features necessary to meet the wide variety of applications of the D4 channel bank. There are numerous channel-

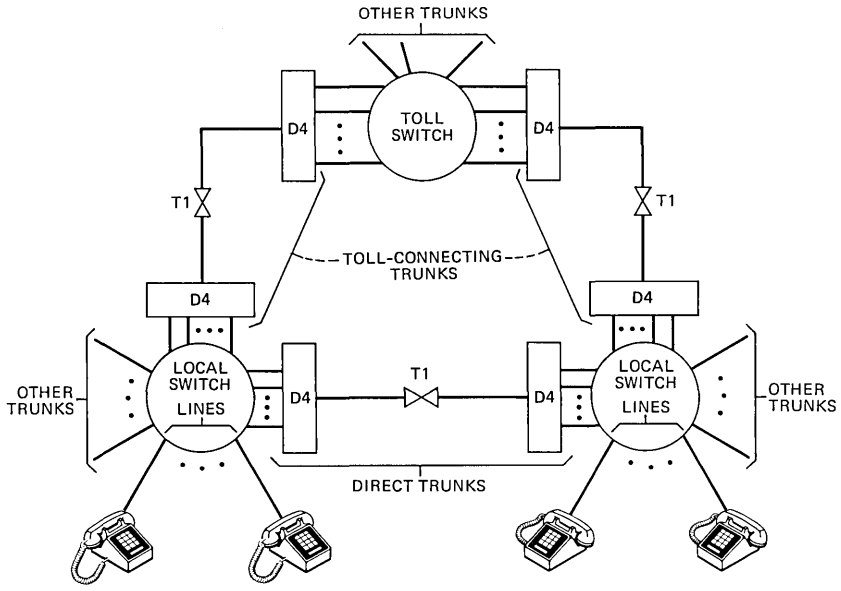

Fig. 5—D4 trunk application.

unit designs; each serves a particular subset of the application spectrum.

Message telephone services interconnect central office switching equipment that serves the switched telephone network. These connections between switching machines are called trunks. The predominant D4 trunk applications are in the local trunk network because of the quantity of trunks involved and because of the suitability of the D4 bank to short-distance applications. Figure 5 depicts these applications. Connections between two local class 5 (or end) offices are called direct trunks. This application represents a large portion of the present D4 applications. These are typically trunks between two-wire switches with superimposed dc signaling except for inband addressing. Toll connecting trunks connect the class 5 local switching machine and the toll switching network. Both two- and four-wire circuits are used for toll connecting trunks. For most applications, the conversion between the four-wire toll switching network and the two-wire local network is performed by the D4 channel unit at the local office end of the toll connecting trunk.

Special services represent a rapidly growing portion of the D4 application spectrum. Transmission equipment is dedicated to a specific customer on a full-time basis. A typical application is diagrammed in Fig. 6. This is a foreign exchange application where a customer is connected to a remote central office by interoffice circuits on a full-

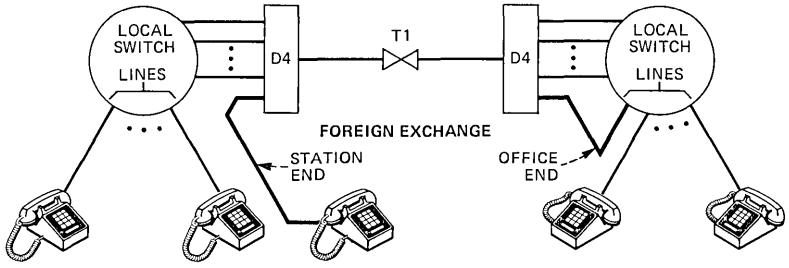

Fig. 6—D4 foreign exchange application.

time basis. The customer with this service is provided local service on the remote telephone exchange. This service is commonly used for a business with a large community of customers in a neighboring city. Other special service applications include trunk connections between the central office switch and a private branch exchange switch, as with a large business customer.

3.3 Functional description

Figure 7 shows the functional block diagram of a typical D4 channel unit. Many of the circuits are customized to the specific applications of each channel-unit type. Manual settings customize each channel unit to a particular application.

Translations between internal logic level signals and the various external signaling conditions from connecting equipment are performed by the signaling circuits. Signaling detectors differentiate among the signaling states from the central office equipment and generate the appropriate logic level signals as inputs to the control logic. Signaling generator circuits receive signals from the control logic and control the output signaling conditions to the central office equipment.

The trunk processing function controls the output signaling conditions when a carrier system fails; the channel unit translates control logic level signals from the D4 common circuits into output signaling conditions or specific conditions on separate wires. This function serves to minimize customer inconvenience and switching machine confusion that would otherwise result from the unpredictable signaling outputs from a failed carrier system.

The hybrid performs the two- to four-wire conversion within two-wire channel units. Internal four-wire operation is used for all channel-unit types. An important performance criteria of the hybrid is how well it isolates signals in the receive direction from signals in the transmit direction. Degradations in hybrid isolation in combination with signal delay, can result in poor echo performance. The degree to

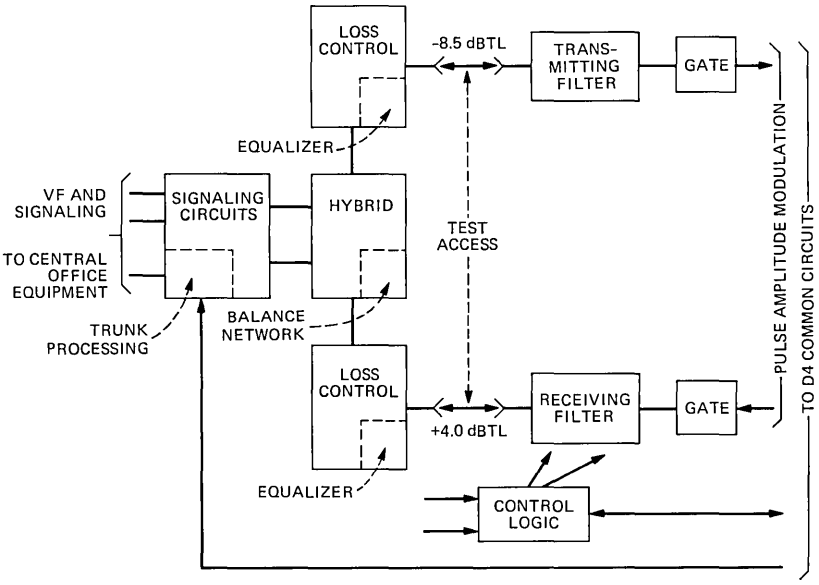

Fig. 7—D4 channel unit functional diagram.

which the balance network of the hybrid circuit matches the two-wire port impedance connected to the hybrid has direct impact on the isolation characteristics of the circuit. Another function of the hybrid (or other input circuit) is to isolate common mode input signals on the balanced input from the unbalanced internal signals. Induction at the fundamental and harmonics of 60 Hz from power lines is the most prevalent source of this interference.

Flat loss (or gain) adjustment is a channel-unit function that allows setting the nominal loss of the end-to-end carrier system and compensating for the transmission loss of the office wiring. Some D4 channel units equalize gain-vs-frequency distortion in external wiring. This is typically required where long lengths of cable interconnect the channel unit to a terminating circuit.

The filter and gate circuits condition the message signals. Thin-film active filters bandlimit the voice-frequency input signals in the transmit direction and reconstruct the continuous voice frequency signals from the PAM output in the receive direction. The input bandpass filter provides attenuation of undesired low-frequency interference and of signals above the 4-kHz Nyquist frequency. The receive reconstruction filter is a low-pass network. The transmission level is the same for all D4 channel units at the input to the transmit filter, [−8.5 decibels-transmission level (dBTL)], and the output of the receive filter (+4.0 dBTL). Each channel unit has a transmit and receive sampling gate.

The transmit gate samples the continuous bandlimited input signal. Under control of the D4 common circuits, the sampling interval is narrow and time sequenced among the channel units in a digroup, with the outputs of all the sampling gates in a digroup wired together to carry out the multiplexing function. The receive sampling gates select the PAM samples for a particular channel from a PAM bus. Timing for this process originates in the D4 common equipment. The function of the control logic on D4 channel units is to interface between the address and timing signals from the D4 common circuits and the sampling and signaling circuits on the channel units. During trouble conditions, trunk processing signals bypass and override the control logic so that proper trunk processing does not rely on the availability of power to the control logic.

3.4 Signaling storage

Signaling storage[15] is an important innovation of the D4 channel bank. In earlier digital bank designs, disturbances in the digital carrier system that cause the channel bank to go out-of-frame temporarily also cause disruption in the trunk and special services network. These short disturbances are a minor impairment for voice message transmission but can cause serious signaling disruptions. Improperly detected idle-to-busy transitions cause multiple false seizures; falsely decoded busy-to-idle transitions may cause disconnection and other difficulties. Predecessors to the D4 channel unit stored only the most recent signaling information as demultiplexed from the receiving common circuits. The D4 channel unit stores multiple successive signaling values. When an out-of-frame event occurs, the common equipment causes the channel unit to cease storing new values and present the oldest stored value to the central office equipment. Because the interval for detecting the disruption is shorter than the interval over which signaling values are stored, the disturbance is successfully bridged. The trunk processing function takes effect for long disturbances.

3.5 Circuit realizations

The signaling interfacing circuits must withstand high-energy signals. For cases where signaling is superimposed on transmission signals, circuit balance must not be seriously degraded by the signaling circuits. Achieving the necessary ruggedness and isolation has led to the predominant use of relay circuits for output signaling states and high-impedance resistive networks for detecting input states. Circuit elements are required to interface between the balanced external transmission circuits and the internal unbalanced circuits. In four-wire channel units this is accomplished by transformers at each interface.

The hybrid circuit provides this function in two-wire channel units. The hybrid function in two-wire D4 channel units is realized with the interconnection of the windings of two transformers to form the four-port network. A compromise network consisting of a series resistor and capacitor may be optionally connected to the network port of the hybrid to approximate the impedance at the switch. In addition, network build-out capacitors are set to compensate for the capacitance of the connecting office wiring. If a VF cable is permanently connected, there is capability for connecting an external precision balance network.

Thin-film resistor networks are used in both the receive and transmit direction to provide settable control of the transmission level of the channel unit. Four-wire channel units typically have lower input transmission levels and higher output transmission levels in contrast to two-wire channel units. The additional gain required is provided by integrated circuit operational amplifiers with resistive feedback gain control elements. The filter circuits consist of operational amplifiers with thin-film RC networks controlling the frequency shaping.[16] The sampling gates are discrete N-channel junction field effect transistors (JFETs). The receive JFET is physically mated to the receive filter so that trimming of the filter can compensate for unit-to-unit variations in the JFET. This results in improved performance. The logic circuit is a custom silicon integrated circuit and is fabricated using the standard buried collector (SBC) technology. The circuit contains about 30 logic gates. The signaling detector is a custom linear SBC integrated circuit. This circuit is a special-purpose comparator and interfaces between the high-impedance signaling interface circuits and the logic circuit. The relay drivers used in the channel units are general-purpose integrated circuits that translate low-energy control signals from the logic into drive signals for the signaling relays. The JFET driver is a custom silicon integrated circuit in the complimentary bipolar integrated circuit (CBIC) technology. High-speed and wide-output signal voltage excursions characterize this circuit that provides an interface between the logic and the JFETs.

3.6 Maintenance and provisioning interfaces

The operational requirements of D4 channel units encompass a wide spectrum. Mechanical options[17] allow each channel unit code to be custom tailored to the application. Increasing the application spectrum for an individual channel-unit type decreases the number of types required at the expense of increased channel-unit cost. The approach in D4 design has been to include only the options that offer significant channel-unit-type reduction with minimal cost penalty, particularly in high-production-volume channel units. One set of option settings con-

figures the channel unit to the type of service being supplied. Examples are the subclass of signaling interface and type of trunk processing. Settings are provided to compensate for external signal degradations and to achieve the desired nominal circuit performance. Gain, equalization, and hybrid balance are all involved. These options are prescription set based on records of the type of connecting equipment, cable gauge and length, and circuit loss requirements.

There is a connector on the faceplate of each channel unit. Test cords are available for interconnecting these connectors and test equipment. Voice-frequency access is provided at the standard internal channel-unit transmission-level point. Access is available in both directions, facilitating both line-side and drop-side testing. Test cords are also available for split-signaling lead access at the same connector. The signaling access point is at the interface between the central office circuits and the channel unit.

Channel units may be connected to a channel bank by a channel-unit extender. The extender splits the access to the transmission and signaling leads at the interface between the channel unit and the distribution frame in the central office. The field-settable options on the channel units are accessible while the channel unit is engaged in the extender.

A maintenance bank facilitates thorough testing of channel units at a centralized location within the central office on an out-of-service basis. Other maintenance functions are also performed; the maintenance bank is discussed in a companion article.[18]

IV. PCM CODING AND MULTIPLEXING

4.1 General overview of transmit and receive functions

The D4 bank is a dual digroup system with nearly independent operation per digroup. Operation is not completely independent because the transmit sections of the digroups share a common clock and both transmit and receive units share a common power converter.

The major functions performed by the transmit and receive units are: encoding, decoding, timing generation for channel units, multiplexing channel-unit signals, frame generation, transmission of data over signaling frame bits, and synchronization of multiple transmit units.

Because the D4 bank must be compatible with D1D, D2, and D3 channel banks, there are three channel-counting sequences. These sequences are electronically controlled by option plugs in the trunk processing unit. In addition, D4 has the option of voice or data channel units. Voice signals are encoded into PAM samples, which are then converted into 8-bit PCM words. Data-channel-unit signals are multiplexed directly into the PCM signal in 8-bit bytes. Special service 5-

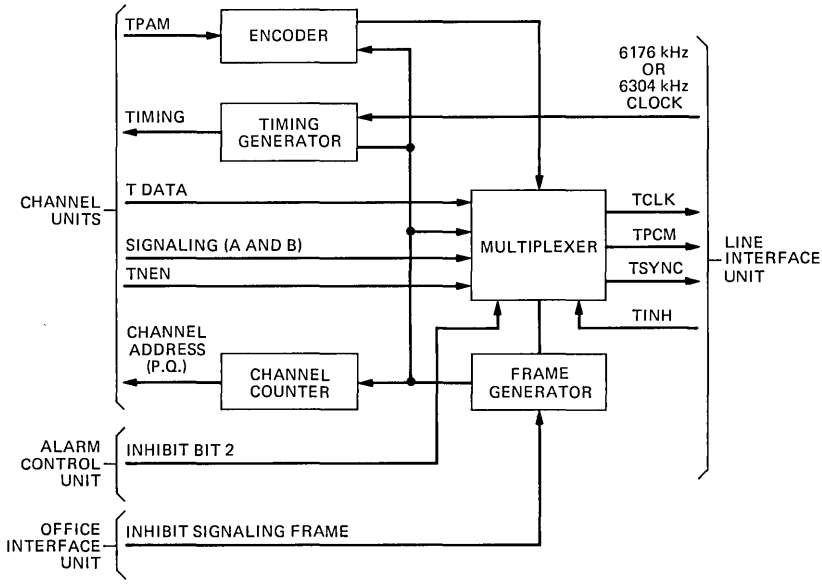

Fig. 8—The transmit unit.

kHz, 8-kHz, and 15-kHz program channel-unit signals are sampled like voice signals but displace one, two, and six voice channels, respectively, to increase the bandwidth. Because the D4 bank has built-in multiplexers, the transmitter and receiver have optionally selectable input clock rates and transmitter and receiver synchronization.

4.2 Transmit unit

The transmit unit (TU) (Fig. 8) provides address and timing signals to the channel units for sampling the voice or data signals, encodes voice PAM samples into 8-bit PCM words, multiplexes the PCM words, and inserts signaling and framing information to form the transmit PCM (TPCM) bit stream. It also provides zero code suppression, which substitutes a fixed word for PCM words having all zeros to meet digital line signal requirements. The signaling frame pattern of the TU can optionally be inhibited so that these frame bits can be used as a slow-speed (approximately 4-kb/s) data channel.

The TU logic is clocked at either 6176 or 6304 kHz by a crystal-controlled oscillator located on the line interface unit.

4.2.1 Timing

The transmit unit generates timing signals used by the channel units to construct time-division multiplexed voice samples on the transmit pulse amplitude modulated (TPAM) bus. These pulses are translated

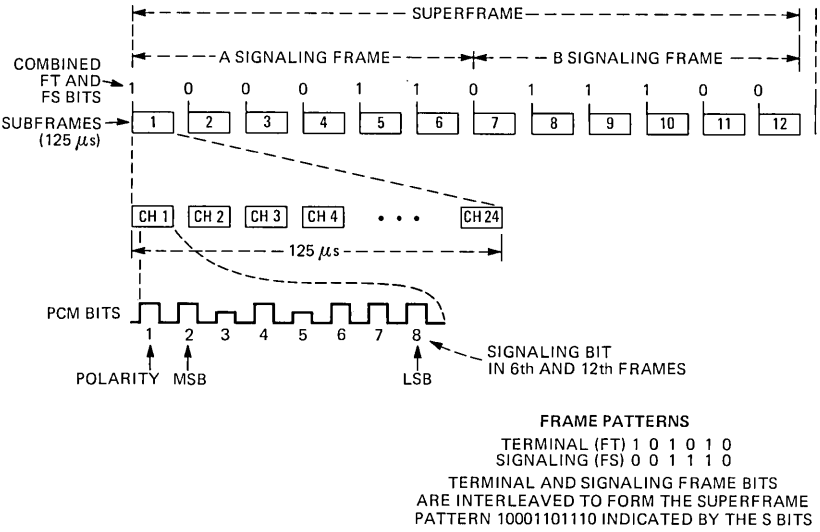

Fig. 9—D4 frame organization.

into 8-bit PCM words within the transmit unit by the encoder. Signaling from each channel unit is substituted for bit eight of these words during every sixth and twelfth frame. To help ensure proper T1 line performance, words with all zeros are substituted with a 00000010 word. This is referred to as zero code suppression. The channel unit has the option of having PAM samples translated in 8-bit PCM words or direct multiplexing of eight data bits. This option is controlled by a bus lead transmit, negated enable (TNEN). When the signal level of TNEN is made a logical zero, PAM samples are encoded into PCM by the transmit unit. When TNEN is a logical one, eight data bits are clocked into the transmit unit and inserted in the digroup bit stream.

The D4 frame organization is illustrated in Fig. 9. It is generated by multiplexing terminal frame (FT) and signaling frame (FS) signal patterns to form a composite superframe that includes 12 subframes. Each subframe includes one frame bit and 24 8-bit PCM words representing the voice samples or data bytes. As indicated in Fig. 9, the composite frame pattern is obtained by multiplexing two frame signals, the terminal frame 101010 pattern and the signaling frame 001110 pattern. The terminal frame pattern is used by the receiver for synchronization to decode the PCM words. The signaling frame pattern identifies the sixth and twelfth terminal frames, which contain the signaling information in bit 8 of each PCM word. The terminal frame must always be sent, but once frame synchronization is achieved, the signaling frame pattern can be replaced by data from some external source. When an external data pattern is substituted for the signaling frame pattern,

per-channel signaling in frames six and twelve is normally disabled although signaling can still be transmitted.

In Modes 2, 3, 4, and 5, each frame consists of 24 8-bit words plus one frame bit (193 bits). When the banks are operating in Mode 1, four additional stuff bits are added (one for each six channels) to form a 197-bit-per-frame signal and the two digroups are frame and bit synchronized.

As we learn in a subsequent section, alarm transmission to the far end terminal is accomplished by suppression of bit-2 (the most significant bit) in every channel time slot.

4.3 Receive unit

The receive unit (RU) decodes the 24-channel PCM unipolar line signal, received from the line interface unit, into PAM signals and necessary control signals for use in the channel units. It also provides signals and controls for maintenance and alarm functions. The functions normally performed by the D4 receive unit are summarized below:

(*i*) Synchronization to the 193-bit-per-frame or the 197-bit-per-frame FT

(*ii*) Synchronization to the FS

(*iii*) Control of signaling storage

(*iv*) Switching from 8-bit to 7-bit decoding during signaling frames

(*v*) Shifting from 7-⅝-bit decoding to 8-bit decoding when common-channel interoffice signaling (CCIS) is being used

(*vi*) Indication of FS and FT bit positions

(*vii*) Channel-unit timing

(*viii*) Provision of electronically controlled 3-mode channel counter

(*ix*) Provision 12-channel shift of the channel counter sequence for testing two-wire channel units

(*x*) Provision of 1-kHz, 0-dBm0 maintenance test code signal

(*xi*) Out-of-frame and loss-of-clock alarm detection

(*xii*) Bit-2 detection for the yellow alarm

(*xiii*) Provision of ac-coupled channel-unit enable pulse to protect channel-unit active filter.

Optional functions that can be performed by the receive unit include:

(*xiv*) Synchronization to the bank transmit frame pattern

(*xv*) Provision of a data channel by means of the signaling frame bits.

Figure 10 is a block diagram of the receive unit. It shows the major functional blocks and interconnections to the other bank circuits. Decoding is done by a shared nonlinear μ255, 15-segment decoder. The output of the decoder consists of received PAM (RPAM) samples, which are supplied to the channel units over a common bus.

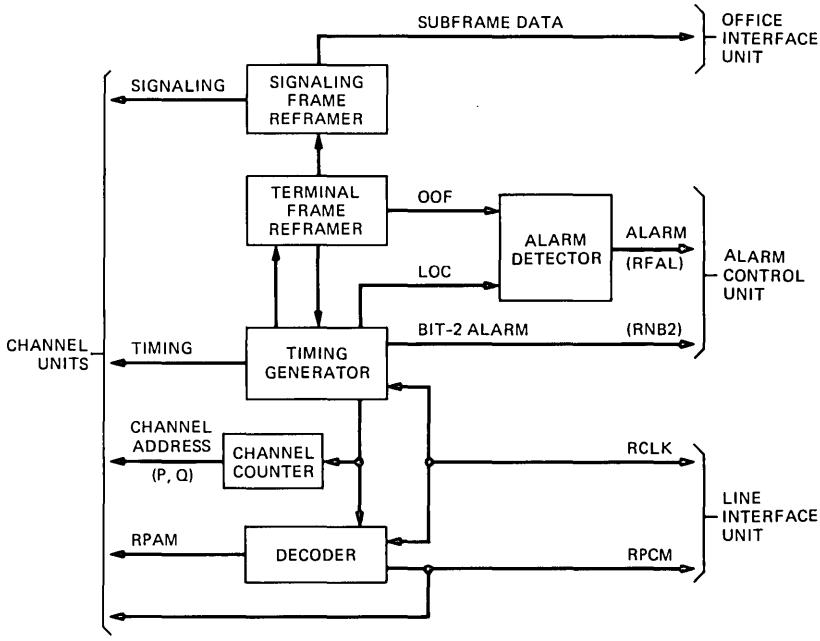

Fig. 10—The receive unit.

The terminal frame reframer synchronizes the timing generator to the incoming 101010 terminal frame bit pattern received from the PCM line. This reframer is an 8-bit-at-a-time reframer with a maximum average reframe time of 43.6 ms. The algorithm for terminal frame reframing is shown in Fig. 11. The signaling frame reframer locks onto the signaling frame pattern to identify the sixth and twelfth frames, which have the signaling information. An out-of-frame (OOF) or loss of clock (LOC) signal is detected by the alarm detector (ALM DET), which sends an alarm signal (ALM) to the alarm control unit. This quiets the voice-frequency noise in each channel unit during the reframe time.

A timing generator, synchronized to the clock recovered from the incoming PCM bit stream, provides timing for the reframers and the receive side of the channel units. This timing generator optionally divides the incoming recovered clock by 193 or 197 to form frame-length words. All frame lengths are 193 except when the bank is operating in Mode 1, which has a 197-bit frame, formed by adding a stuff bit after the frame bit in time slots for channels 6, 12, and 18. As we describe in a later section, when the channel bank is working in Mode 1, a signal derived by the two receive units is used by logic in the LIU to steer demultiplexed data to the proper receive units. This signal is derived from the frame signals of each receive unit, which are

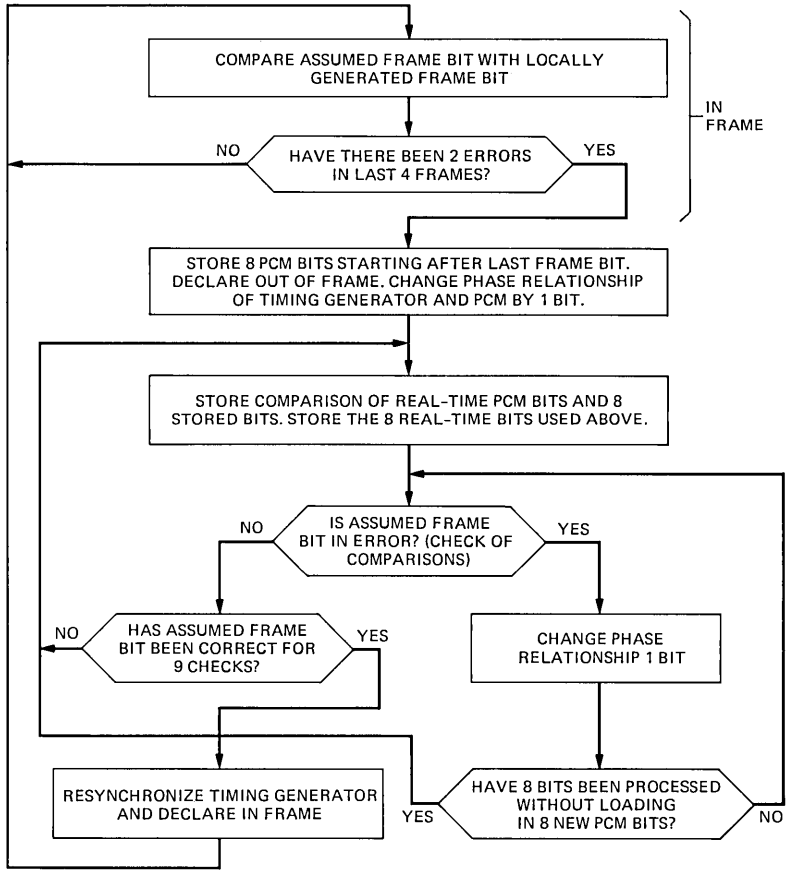

Fig. 11—Reframer flowchart.

algebraically added in receive unit A. The timing generator also extracts the PCM "bit 2" alarm signals for processing in the alarm control unit.

The channel counter derives channel address signals, which are routed over busses to the channel units to activate each channel circuit at the proper time. The signaling frame reframer synchronizes the receiver to the 001110 FS pattern and produces pulses that enable channel units to read the signaling bits into storage registers. The reframer also switches the decoder from 8-bit to 7-bit decoding during signaling frames to prevent the signaling bits from affecting the RPAM samples. The FS reframer is insensitive to errors in the FS bits. In fact, after the circuit has reframed properly on the FS pattern, the FS pattern can be removed, and the receiver will continue to indicate where the FS pattern should be. Insensitivity to FS bit errors provides noise

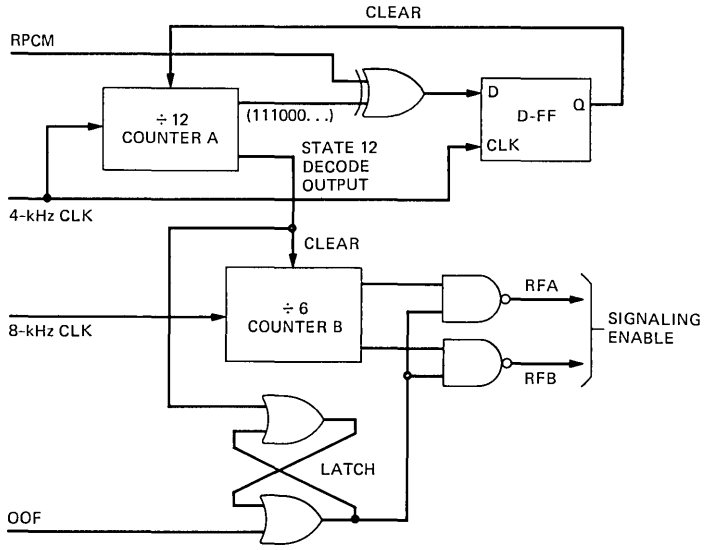

Fig. 12—Signaling frame reframer.

immunity and permits the transmission of data in the FS bit positions while maintaining normal signaling in bit 8 of the voice channels. Data transmission via the FS bit can approach a maximum rate of 4 kb/s. The *SLC**-96 Subscriber Loop Carrier, described in a companion article, uses this subframe data path to send alarm status, concentration, and maintenance information while maintaining full signaling capability.

Figure 12 shows the major portions of the signaling frame reframer. Counter A is a divide-by-twelve counter having an output the same as the 1100 FS pattern. FS bits from counter A are compared with the received FS bits by the exclusive-OR gate. If the FS bits do not match, counter A is cleared and another comparison begins; when the two patterns match over twelve consecutive pairs of FS bits, frame synchronization is recognized; and when counter A reaches state 12, a signal is sent to counter B and the latch circuit. Counter B is then reset and forced into synchronization with the superframe pattern generating the receive frame signal for A digroup (RFA) and the receive frame signal for B digroup (RFB). RFA and RFB are signaling enable outputs to logic in the channel units. If terminal frame synchronization is lost, an out-of-frame (OOF) signal resets the latch and forces RFA and RFB to logic one at the same time to save the stored signaling bits in

* *SLC* is a trademark of Western Electric.

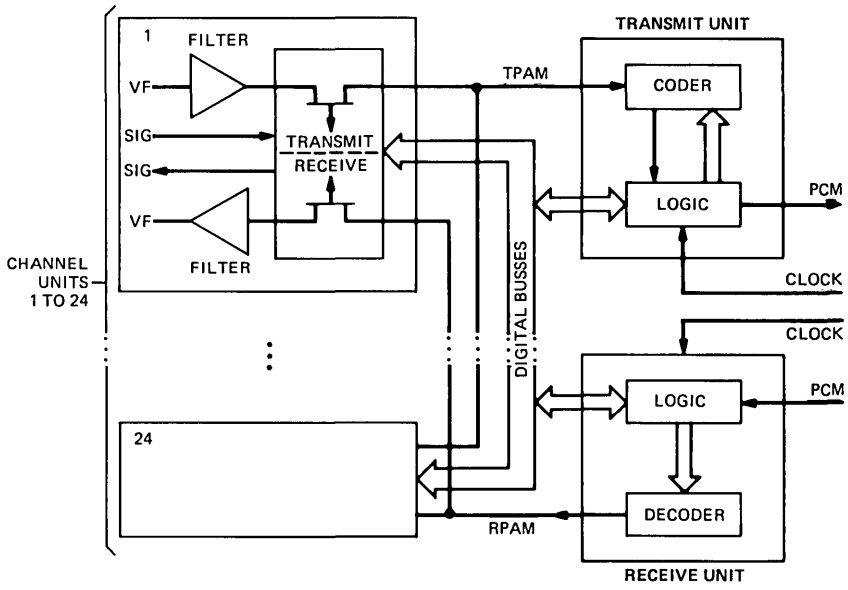

Fig. 13—The CODEC system.

the channel units. The signaling states are maintained until counter A has resynchronized to the signaling frame pattern.

A 1-kHz, 0-dBm0 "digital milliwatt" code generator circuit is provided in the receive logic. It causes the receive unit analog circuits to develop analog PAM samples that are applied to all 24 channel units for receive circuit-level testing. This code generator is activated by inserting a plug into a jack on the faceplate of the receive unit.

4.4 CODEC

The D4 PAM and coder-decoder (CODEC) system is partitioned as shown in Fig. 13. Each of 24 channel units contains a transmit active filter and a receive active filter, plus an integrated circuit that performs voice-frequency sampling and signaling functions for both transmit and receive directions. The remainder of the channel-unit circuitry, not shown in Fig. 13, comprises battery, overvoltage, ringing, signaling, hybrid, and related circuits.

Voice-frequency signals in the channel unit are filtered and then sampled at 8 kHz with a JFET sampling circuit. The PAM samples are time-division multiplexed onto the TPAM bus and sent to the transmit unit, where they are buffered, sampled, held, amplified, and encoded with the nonlinear μ255 successive approximation coder shown in Fig. 14. In the receive direction, serial PCM is formatted by logic in the receive unit into parallel words that are applied to the decoder shown

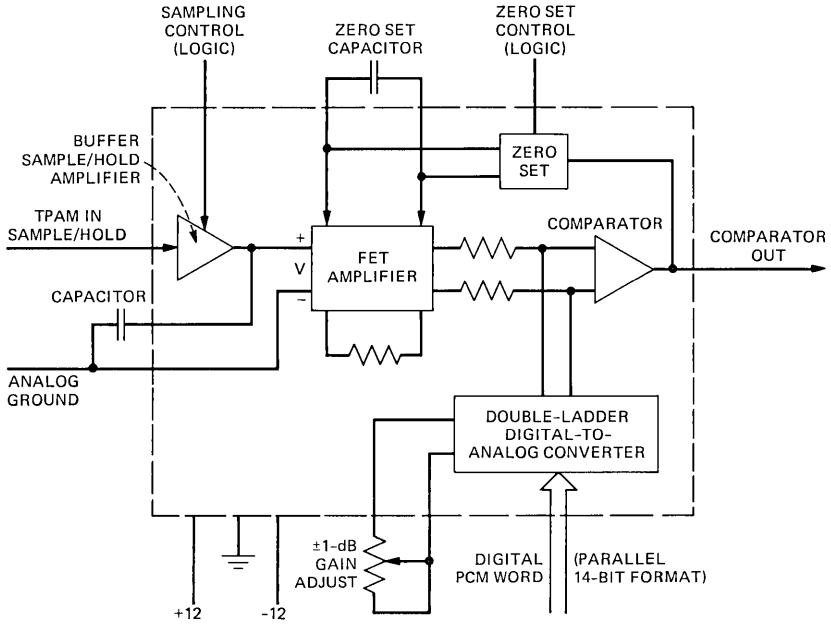

Fig. 14—The coder.

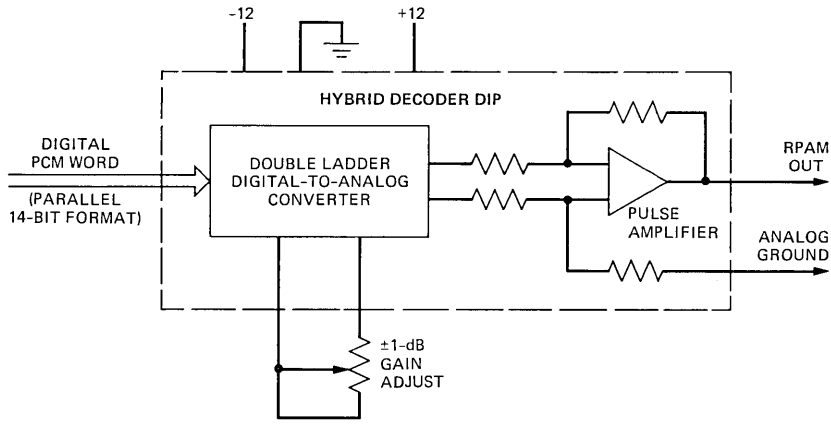

Fig. 15—The decoder.

in Fig. 15. Using the nonlinear $\mu 255$ characteristic, the decoder generates multiplexed PAM samples that are sent to the channel units via the RPAM bus. When each channel unit is addressed (see Fig. 10), a JFET gate applies the proper PAM samples to the receive filter, which reconstructs the voice-frequency signals. The CODEC processes samples

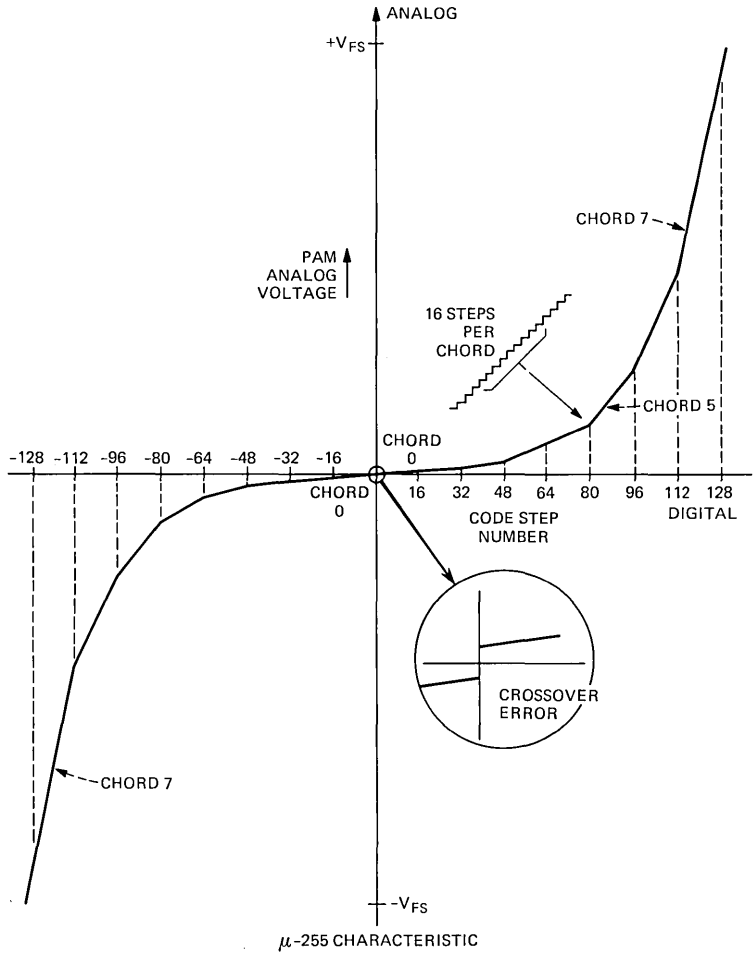

Fig. 16—Nonlinear μ255 companding characteristics of the decoder.

every 5.2 μs (192 kHz). TPAM samples are of approximately 970-ns duration, while RPAM samples are approximately 3.5 μs. The channel-unit operations are timed and controlled by digital busses from the transmit and receive units. The logic devices in these units also control the CODEC timing.

On both the coder and decoder, a digital-to-analog converter (DAC) develops precision voltages that produce the nonlinear μ255 companding characteristic shown in Fig. 16. This DAC consists of one custom silicon integrated circuit and 40 thin-film resistors. A simplified schematic of this DAC is shown in Fig. 17. Any one of the 255 output

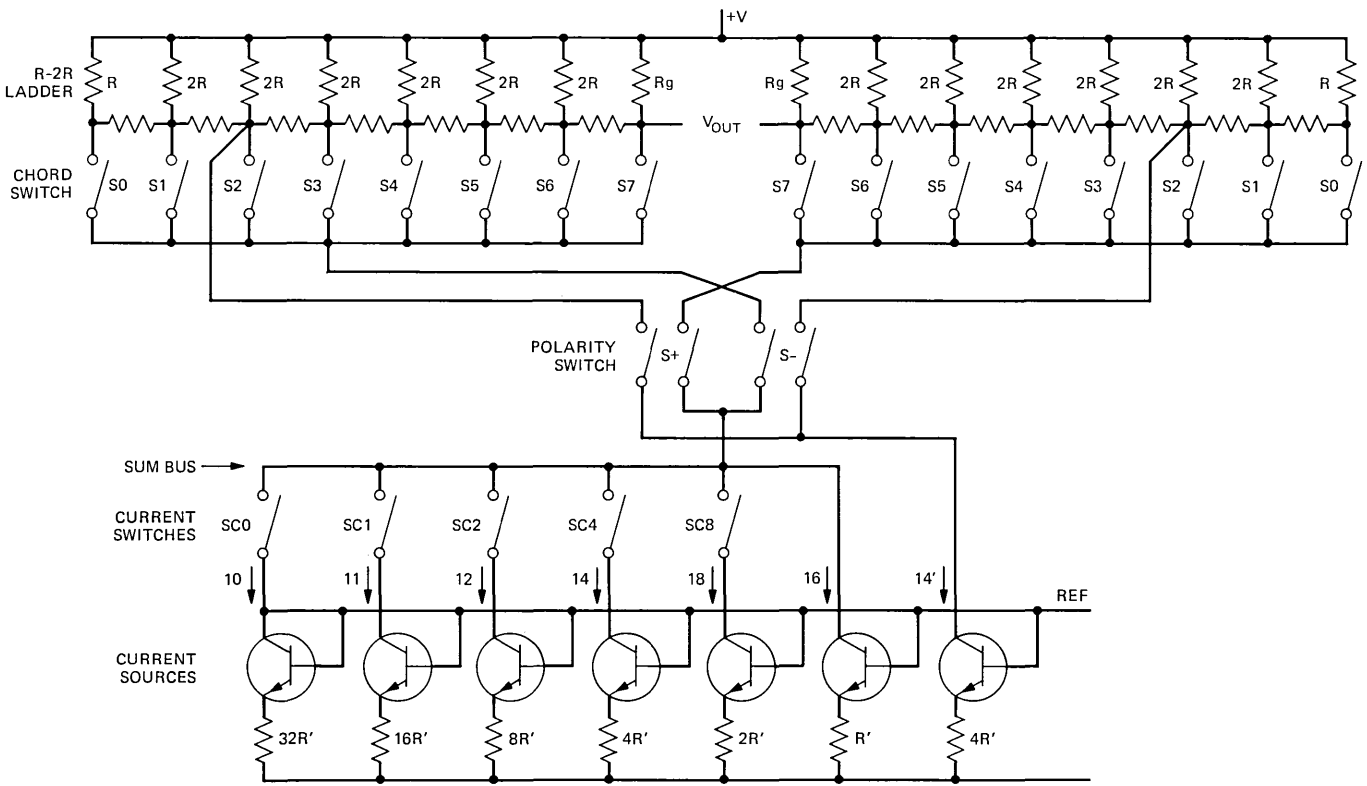

Fig. 17—The digital-to-analog converter.

voltages can be produced at VOUT by choosing an appropriate combination of switches SC8, SC4, SC2, SC1, S+, S−, and S0 through S7. Switches SC1, SC2, SC4, and SC8 can be set to any one of sixteen possible binary combinations, which represent the sixteen possible levels on any chord. Depending on this setting, a specific value of current is drawn from the summing bus (SUM BUS shown in Figure 17). This current is developed by binary-weighted current sources I16, I8, I4, and I1 from a voltage reference (V_{ref}). The polarity of the output voltage is determined by switching on either S+ or S−, thus routing the current to either the positive or negative ladder. Choosing one (but only one) of switches S0 through S7 allows the current to be drawn from the proper node of the R-2R ladder to develop the output voltage. These switches correspond to chords 0 through 7, respectively. At the same time, the polarity switch also routes current I4' (I4' = 14) to the third node of the opposite ladder. This produces a voltage equivalent to I16 through S0 to node 1. Hence, for zero code (either positive or negative) VOUT is ideally zero. In reality, however, a finite voltage difference between positive zero and negative zero exists and causes a nonlinearity, known as crossover distortion (Fig. 16), at the origin of the companding characteristic. This nonlinearity is a primary contributor to gain tracking and signal-to-distortion (S/D) degradation for lower level ($\leq$−40 dBm0) signals. In addition, crossover distortion can seriously impair the crosstalk and idle circuit noise performance of the terminal. To meet system objectives, a crossover error equal to or less than one-third the least significant bit (LSB) is necessary in the DAC. Switch SCO provides a switchable one-half LSB bias for two applications in the CODEC, as follows:

(*i*) One-half code step midtread bias at the origin of the coder, and

(*ii*) Conversion from 8-bit decoding to true 7-bit decoding in the decoder when the eighth bit is robbed for signaling.

To provide the rapid coding of PAM samples (one decision every 325 ns), the DAC settles to 0.1 percent of final value in less than 100 ns. On the decoder, the DAC drives a differential to single-ended pulse amplifier consisting of six thin-film resistors and a wideband operational amplifier. This pulse amplifier settles to 0.1 percent of final value in $\leq$2 μs. Additional circuits are required in the coder. These include a sample/hold amplifier, a FET amplifier, a high-gain comparator, and a zero set circuit. Also included, but not shown in Fig. 14, is a JFET switch driver, which drives a discrete N-channel JFET that clamps the TPAM bus to ground during encoding to prevent crosstalk between samples and to reduce coding noise. Some of the pertinent requirements for the circuit are as follows:

(*i*) Comparator gain $\geq$ 25,000,

(*ii*) Comparator delay $\leq$ 100 ns with ⅛ code step overdrive (code

step size depends on successive approximation algorithm and typically one transition dominates),

(*iii*) Coder dc offset $\leq$ 8 LSB,

(*iv*) Sample/hold-buffer amplifier settling time $\leq$ 900 ns to 0.1 percent of final value,

(*v*) Droop of held sample $\leq$ ⅛ code step (size depends on sample amplitude).

The basis for the D4 CODEC design objectives is the specification for end-to-end system performance. Because the CODEC is only part of the system, however, CODEC design objective allocations must be derived from these specifications. In deriving objectives, it is important to observe that any coder-decoder combination plus VF filters, sampling gates, etc., must meet end-of-life requirements for new facilities. This automatically allocates less than half of each system requirement to the DAC. How much less than half depends on the sensitivity of other system components to the requirement in question and, therefore, is subject to engineering judgment. Because of this, the objectives are somewhat arbitrary but, nevertheless, consistent with overall system requirements. CODEC and DAC objectives, along with the system requirements, are summarized in Table II. There are several points to note concerning these requirements and objectives. First, all requirements and objectives must reflect the D2/D3/D4 7-5%-bit coding format, in which 7-bit coding is used every sixth sample to accommodate signaling information. Second, CODEC S/D requirements cannot be directly inferred from those of a single DAC because, for small DAC errors, most of the distortion power is due to theoretical quantizing noise. Last, idle channel noise and crosstalk are dominated more by physical constraints than by circuit design. Theoretically, the CODEC contributes a maximum 17-dBrnC0 idle channel noise and −71 dBm0 crosstalk power, assuming D4 system constraints of 7-5%-bit coding and a +3 dBm0 virtual overload for the CODEC. The theoretical idle channel noise calculation assumes that low-power white noise perturbs a coder biased at a decision level one LSB. The crosstalk calculation is performed similarly, except that all the power is assumed concentrated in a square wave of peak amplitude one LSB at the crosstalk frequency. This assumption is justified only if the input crosstalk power is sufficiently larger than the input white noise to the CODEC.

DAC gain tracking and S/D performance as specified in Table I can be calculated and plotted by computer simulation, given each of the 255 DAC output voltage levels. However, this method is not practical during laboratory evaluation and production testing. An alternate method, though slightly more stringent, is to directly specify limits on certain output levels. These limits guarantee the aforementioned gain tracking and S/D requirements while simplifying the test procedure. It

Table II—CODEC and DAC objectives

	1-kHz Level (dBm0)	System Requirement (dB)	D4 CODEC Objective (dB)	DAC Objective (dB)
Signal-To-Distortion*	0	33	33	35
	−10	33	33	35
	−20	33	33	35
	−30	33	33	34
	−40	27	27	30
	−45	22	22	26
Gain Tracking*	+3	±0.5	±0.25	±0.08
	0 (Reference)	—	—	—
	−10	±0.5	±0.25	±0.08
	−20	±0.5	±0.25	±0.08
	−30	±0.5	±0.35	±0.12
	−40	±1.0	0.50	±0.23
	−45	±1.0	±0.75	±0.35
Harmonic Distortion	1-kHz Level 0 dBm0	−40	−50	−55
Gain Stability (0°C–50°C)	1-kHz Level 0 dBm0	±0.25	±0.20	±0.05 (150 ppm °C) (0°C–75°C)
Crosstalk Coupling Loss	Level 0 dBm0 200 to 3400 Hz	>65	>75	Not applicable
Idle Channel Noise		23 dBrnC0	20 dBrnC0	Not applicable

* Includes crossover error.

is sufficient to specify only the seven-chord endpoints, zero crossing, full-scale error ratio, and current source ratios to characterize the DAC. Harmonic distortion is calculated assuming a linear gain variation between the positive and negative portions of the coding characteristic. Although this is not absolutely true (different ladders and switches are used), nonlinearities are sufficiently small to make it a good assumption. Second-harmonic distortion is then given by

$$\text{2nd-harmonic distortion} = 20 \log_{10} \frac{2}{3\pi} [1 - \mathrm{R}]$$

$$R = \left[\frac{+V_{FS}}{-V_{FS}}\right] (V_{FS} = \text{full-scale voltage}).$$

Therefore, for a second-harmonic better than 55 dB down, $0.992 \leq R \leq 1.008$, where R is the full-scale error ratio. The power supply rejection ratio is chosen based on available power supplies, associated supply noise, and the desired noise immunity and gain stability. Computer simulation, verified by experimental results, was employed to develop the tolerances on the DAC output levels by using the 255 nonideal DAC output levels as coder decision levels with perfect decoder reconstruction levels. The computer calculated and plotted S/D and gain tracking for sinewave inputs of various amplitudes that were then compared with the DAC objectives in Table II. A summary of the derived specifications for the D4 DAC is given in Table III. The specifications pertaining to the other coder and decoder silicon integrated circuits (SICs) that were stated earlier depend more on the implementation of the coding and decoding than on the system requirements. It is obvious, however, that the remaining circuitry must not significantly impair DAC performance, or system requirements will

Table III—DAC requirements

Chord/ Segment	Lower Endpoint Error	Step Size	Step Size Error (Note 1)
7	0 (Note 2)	128 LSB	±2 LSB
6	±4 LSB	64 LSB	±14 LSB
5	±2½ LSB	32 LSB	±½ LSB
4	±1½ LSB	16 LSB	±¼ LSB
3	±1 LSB	8 LSB	±⅛ LSB
2	±½ LSB	4 LSB	±1/16 LSB
1	±¼ LSB	2 LSB	±1/32 LSB
0	±⅛ LSB (Note 3)	1 LSB	±1/64 LSB

Crossover Error: ≤⅓ LSB
Operating Temperature: −40°C to 85°C
Full-Scale Error Ratio (R): 0.8 percent
Power Supply Rejection Ratio: 1mv/V

Note 1: Because current sources are summed to generate chord steps, error may accumulate for each step on the chord, e.g., the maximum error of the top level of chord 5 would be (2 − ½ LSB + 15 × ½ LSB) = 10 LSB.
Note 2: Normalized as the reference.
Note 3: Neglecting dc offset, which is ≤⅓ LSB.

not be met. Operating temperature range, power supply rejection, and gain stability are implicitly assumed in all specifications.

V. DIGITAL FACILITY INTERFACES

The D4 line interface unit functions include unipolar/bipolar digital conversions, transmit timing, clock recovery, maintenance signal looping, coding, and multiplexing/demultiplexing. All modes except 1 and 3 require syndes units, which work closely with the multiplex/demultiplex circuits. PCM signal synchronization, coding, and multiplexing/demultiplexing are not required for Mode 3 operation, which provides independent digroup transmission over two T1 lines. Also, Mode 5 does not require unipolar/bipolar conversion since unipolar logic signals connect to the optical transducers.

The line interface units provide voltage-controlled crystal oscillator (VCXO) circuits, which function as clock generators for timing the transmit units in the bank. The VCXO oscillator is illustrated in Fig. 18. Depending upon the system arrangement, the oscillator may either be free-running or phase-locked to either an external clock (D4 bank externally timed) or to the clock extracted from the incoming PCM (D4 bank loop timed). In the free-running mode, the VCXO is switched to a stable voltage reference to establish the operating frequency. In the externally and looped timed modes the VCXO output is connected to a quadrature phase detector, which forms part of the phase-locked loop (PLL) to control the oscillator. The VCXO specifications are summarized in Table V. The oscillator frequencies are divided by four to obtain the clock signals for the transmit units. The oscillator frequency is higher for Mode 1 because in this synchronous digroup, D4-to-D4 mode, the bank transmit units are operated at 1.576 MHz instead of 1.544 MHz as in the other modes. This allows the oscillator to drive the T1C digital line as well as the bank transmit units. When operated

Table IV—Typical D4 CODEC performance

1-kHz Level (dBm0)	Signal to Distortion (dB)	Gain Tracking (dB)
+3	37.0	±0.1
0	37.5	0 (Reference)
−10	39.0	±0.05
−20	36.5	±0.05
−30	36.0	±0.10
−40	31.5	±0.15
−45	27.5	±0.20

Harmonic Distortion: −52 dB
Gain Stability: ±0.12 dB
Crosstalk Coupling Loss: >80 dB
Idle Channel Noise: 14 dBrnC0 Average

* 7-%-bit coding: *C*-message weighted noise.

Table IV summarizes typical CODEC performance of production units, which is considerably better than the objectives in Table II.

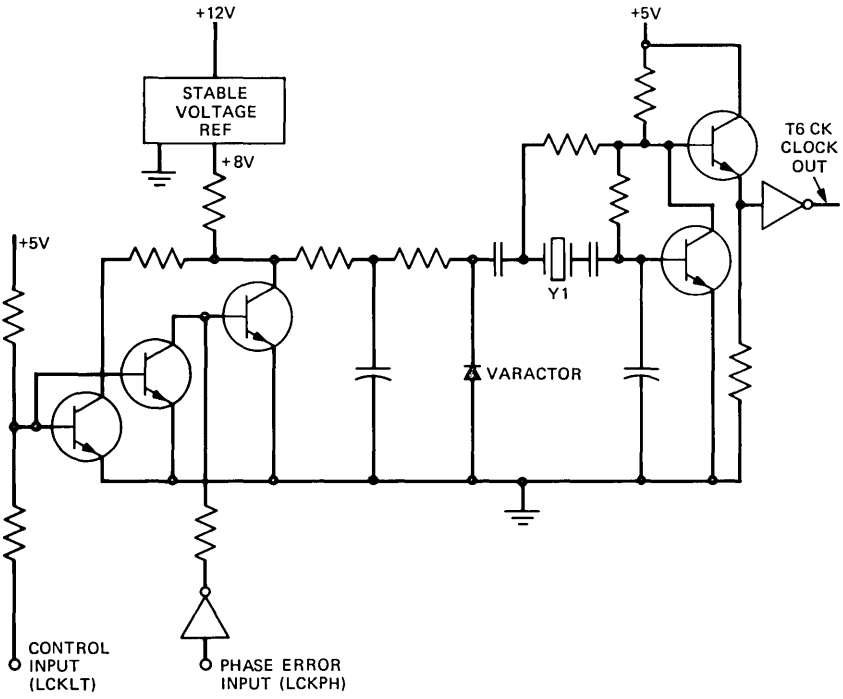

Fig. 18—Voltage-controlled crystal oscillator.

Table V—VCXO specifications

	Specification	
Mode	Frequency (ppm)	Pull Range (Hz)
1	6.304 MHz ± 30	±500
2 to 5	6.176 MHz ± 32	±500

in this mode, the transmit units generate 197-bit frame patterns (instead of 193 bits) by inserting four extra bits per terminal frame, one after every sixth channel. On the receive side, these extra bits are ignored during decoding of the PCM.

5.1 Unipolar-to bipolar conversion

Wire-type digital transmission facilities require balanced bipolar signals. The D4 line interface units provide balanced bipolar signal outputs meeting the requirements depending on the type of facility and far-end terminal to be used in the system.

Figure 19 shows the transmit converter circuit for LIU-1 and -2, along with the associated timing diagram. The unipolar input (TPCM) is converted to bipolar at the output of transformer, T1. The flip-flop

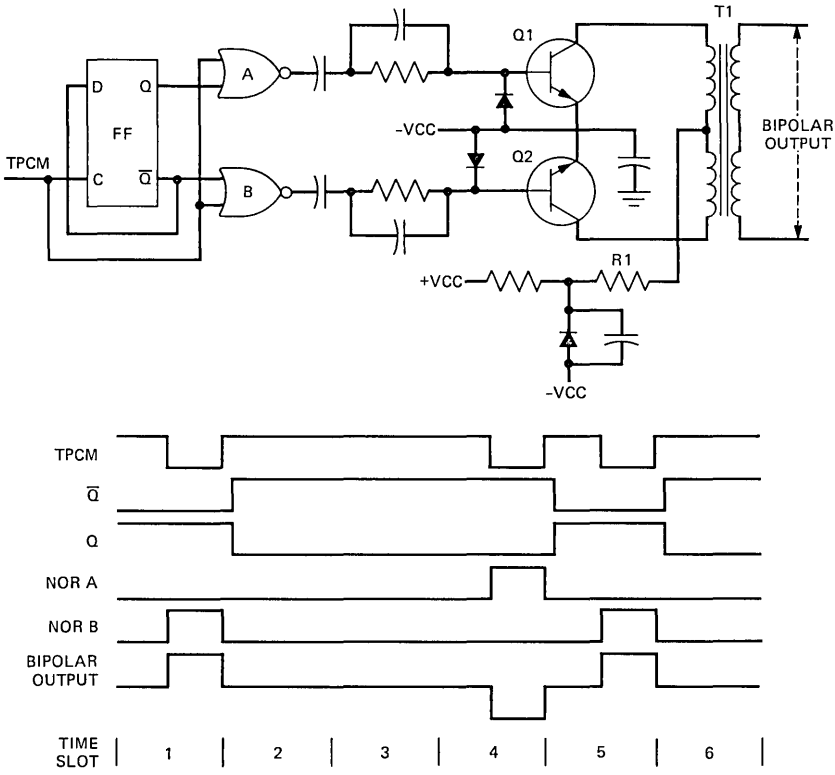

Fig. 19—The transmit converter.

(FF) divides the TPCM input by two, alternately steering the bits through NOR gates to turn ON transistors Q1 or Q2. The outputs of the NOR gates are capacitively coupled to the transistor bases so that, in the absence of the TPCM input, both transistors are OFF. Collector voltage is supplied to Q1 and Q2 by the center tap on T1. Resistor R1 is selected to set the peak pulse amplitude to six volts.

The transmit converter for LIU-3 is a variation of that used for LIU-1 and LIU-2. In LIU-4T the unipolar-to-bipolar conversion circuit is the same as that used in the M12 multiplexer-demultiplexer.

5.2 Clock extraction

Timing of the D4 receive units is derived from the received PCM bit stream. The received clock is extracted from the PCM either by traditional inductor-capacitator, or crystal tank circuits. In the case of the T1 and T1C interfaces, clock is extracted by means of a receive converter circuit,[19] which includes a phase-locked loop. Since the receive converter is embodied in an integrated circuit, this latter

approach has resulted in a significant circuit size reduction for the Modes 2 and 3 line interface units.

Figure 20 shows a block diagram of the receive converter. The circuit accepts the bipolar PCM line signals at the input, extracts the clock by means of the PLL, and provides regenerated PCM data and clock at the output. In addition, the circuit provides unipolar clock and PCM inputs—loop PCM (LPCM) and loop clock (LCLK)—with associated loop control inputs for bank maintenance looping. It also features an automatic output shutdown option to turn off the clock and data outputs in the event of loss of incoming bipolar PCM. This function is provided because when a PLL is used for clock recovery, loss of input signal does not result in loss of clock since the voltage-controlled oscillator continues to operate. Because in some systems a free-running clock is preferred over loss of clock, the circuit provides output shutdown on an optional basis selected by external pin connections. The receive converter, which is implemented in the (CBIC) technology, is described in a companion article describing D4 channel bank integrated circuits.[20]

An important consideration when using the PLL for clock extraction is that the phase comparator must be able to work with a PCM bit stream as an input. This implies that the loop will have the ability to accommodate intervals when timing information is not present. In other words, the output of the clock recovery circuit should ideally remain at its previous phase-locked frequency during the time phase comparisons are not possible (i.e., when a data bit is a logic zero). Since for T1 (1.544-Mb/s) and T1C (3.152-Mb/s) bipolar PCM signals the maximum number of consecutive zeros is restricted to 15, this interval is approximately 9.5 and 4.7 microseconds, respectively.

In the receive converter, these gaps in timing information are spanned by a tristate gate that acts as the phase comparator in the loop. The tristate gate has three output states (logical one, zero, and

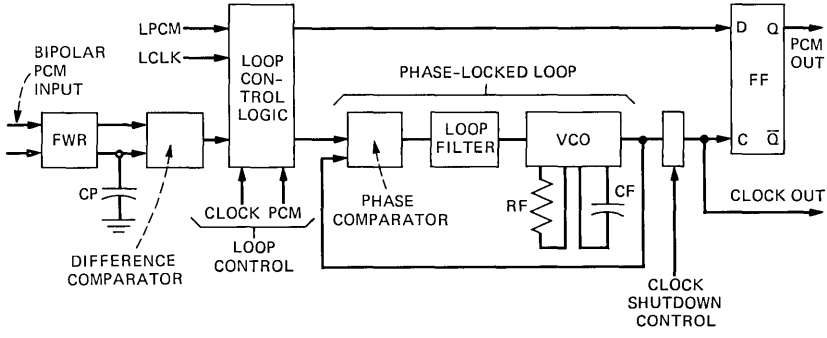

Fig. 20—The receive converter.

high impedance). The gate is forced to the high-impedance state when valid phase comparisons cannot be made because the bipolar PCM input bits are logical zeros. The voltage-controlled oscillator (VCO) frequency is then held by the dc voltage on the loop filter capacitor.

5.3 Maintenance capability

The line interface and syndes unit(s) (SU) provide maintenance capability by means of switchable loop transmission paths so that the transmitted PCM bit stream is looped back to the receiver. If the receiver is able to frame on the looped signal, the bank is judged good. The loop is made as close as is feasible to the digital facility connection in the line interface units to test as much of the bank circuitry as possible.

Because in D4 banks two or four digroups may be multiplexed together, a maintenance loop at the LIU output would disrupt service on any normally operating digroups, as well as those experiencing failures. For this reason, Modes 2, 4, and 5, which have independent digroup operation except for multiplexing, have two levels of looping capability, one in the syndes for individual digroups and another in the line interface unit for the multiplexed output.

The line interface loop capability is unique because it permits an in-service loop test that interrupts the incoming bit stream and bridges the multiplexed output to the input for a period of time long enough to allow frame lock of each receive unit to occur. If any receive units do not achieve frame lock, the logic stores and displays a test fail indication that isolates the cause of failure to the SU synchronizer, or the multiplexer/demultiplexer (MUX/DEMUX).

Whenever a single digroup is looped, an all ones signal is substituted for the PCM and transmitted to the distant terminal. This keeps the digital line repeaters operating and, as discussed in a succeeding section, enables the alarm control unit within the far end terminal to give indication that the near-end digroup has been looped.

The maintenance loop control is derived from the bank alarm control units, which have logic to ensure a normally operating bank cannot be inadvertently looped and interrupt transmission. The LIUS have a special pin-jack option, however, which will override the logic and force loop transmission under out-of-service standby maintenance conditions.

5.4 Equalizers

As we mentioned previously, cable equalizers are installed between the D4 line interface transmit converter and the office digital cross connect or repeater bay. The same set of equalizers is used for the T1 and T1C applications (Modes 1 through 3). There are five equalizer

networks for these applications, each of which is designed to compensate for a range of cable lengths. The equalizers are passive bridged-T-network configurations mounted on small plug-in cards that are installed in the D4 trunk processing unit (TPU).

The Mode 4, T2 interface requires line build-out networks (LBOs) for both directions of transmission. These networks are electrically of the same design as used for the M12 Muldem but have been physically redesigned to fit into the D4 TPU. There are seven different (LBO) codes.

5.5 Multiplexing— Modes 2, 4, and 5

Large-scale integrated multiplex and demultiplex circuits are used in the LIUs for Modes 2, 4, and 5. These custom-designed logic devices are described in a companion article.[20] The same devices are used to optionally multiplex two or four digroups into M1C- and M12-compatible signal formats. The multiplexer, working closely with the syndes unit(s), combines the bit streams of two or four digroups. It also generates and adds a control bit pattern. The control bit pattern is used by the demultiplexer for framing, destuffing, and alarm status indication. The demultiplexer frames on the incoming signal and separates the data into two or four digroup signals along with destuffed clock signals. It also decodes alarm information to indicate a remote terminal alarm status.

The M1C- and M12-compatible multiplexed data formats are presented in Figs. 21 and 22.

5.6 Line interface units

The line interface units supply the circuits and signal connections to other bank common units to set up a particular mode of operation. In addition to line interface units, Modes 2, 4, and 5 require SUs for synchronization of the digroup signals. In this section, the line interface circuits required for each D4 mode of operation will be described.

MODE 2 M1C COMPATIBLE FORMAT:

M1 (52)	C11 (52)	F0 (52)	C12 (52)	C13 (4)	(I1/STUFF) (47)	F1 (52)
M2 (52)	C21 (52)	F0 (52)	C22 (52)	C23 (5)	(I2/STUFF) (47)	F1 (52)
M3 (52)	C11 (52)	F0 (52)	C12 (52)	C13 (4)	(I1/STUFF) (46)	F1 (52)
M4 (52)	C21 (52)	F0 (52)	C22 (52)	C23 (5)	(I2/STUFF) (47)	F1 (52)

- THE FRAME ALIGNMENT SIGNAL IS F0, F1, WHERE F0 = 0 AND F1 = 1.
- THE MULTIFRAME ALIGNMENT SIGNAL IS M1, M2, M3, M4 AND IS 011X, RESPECTIVELY, WHERE X IS AN ALARM SERVICE DIGIT.
- THE STUFFING INDICATOR WORDS ARE Ci1, Ci2, WHERE i = DIGROUP CHANNEL.
- ( ) = NUMBER ENCLOSED REPRESENTS NUMBER OF INFORMATION BITS.
- INFORMATION BIT FORMED BY INVERTING DIGROUP CHANNEL 2 FOLLOWED BY MODULO TWO SUMMATION WITH CHANNEL 1.

Fig. 21—Format of the Mode 2 multiplexed data stream.

MODE 4 M12 COMPATIBLE FORMAT:

M1 (49)	C11 (49)	F0 (49)	C12 (49)	C13 (49)	F1 (I1/STUFF) (48)
M2 (49)	C21 (49)	F0 (49)	C22 (49)	C23 (49)	F1 (1) (I2/STUFF) (47)
M3 (49)	C11 (49)	F0 (49)	C32 (49)	C33 (49)	F1 (2) (I3/STUFF) (46)
M4 (49)	C41 (49)	F0 (49)	C42 (49)	C43 (49)	F1 (3) (I4/STUFF) (45)

- THE FRAME ALIGNMENT SIGNAL IS F0, F1, WHERE F0 = 0 AND F1 = 1.
- THE MULTIFRAME ALIGNMENT SIGNAL IS M1, M2, M3, M4 AND IS 011X, RESPECTIVELY, WHERE X IS AN ALARM SERVICE DIGIT.
- THE STUFFING INDICATOR WORDS ARE Ci1, Ci2, Ci3, WHERE i = DIGROUP CHANNEL.
- ( ) = NUMBER ENCLOSED REPRESENTS NUMBER OF INFORMATION BITS.
- INFORMATION BIT MULTIPLEXING IS I1 I2 I3 I4 I1 I2 ... (I2 AND I4 ARE INVERTED).

Fig. 22—Format of the Mode 4 multiplexed data stream.

5.6.1 Mode 1

Mode 1 provides a unique dual digroup operation over the T1C digital lines. In this mode, full advantage is taken of the inherent synchronization properties of two commonly clocked digroups for an economical D4-to-D4 connection. Both multiplexing and alarm functions are integrally related for the pair of digroups.

A single alarm circuit is provided that responds to failures in either digroup and removes all 48 VF channels from service if either receive unit loses frame synchronization. Only one alarm unit is used because circuits associated with the individual digroups, as well as those shared, must be working normally for proper Mode 1 operation.

Figure 23 is a block diagram of the line interface for Mode 1 bank operation. This unit is designated LIU-1. The circuit multiplexes the two 24-channel digroups (ATPCM and BTPCM) with a bit rate of 1.576 Mb/s into a composite signal at the T1C line rate of 3.152 Mb/s. Multiplexing is done with the two digroups synchronized such that a bit from the A digroup is alternated with a corresponding bit from the B digroup, as shown in Fig. 24. The multiplexed signals are then scrambled in a one-bit scrambler to randomize the bit stream. The transmit converter changes the unipolar format into bipolar to drive the T1C line.

On the receive side, the receive converter accepts the bipolar input from the T1C line, converts it to unipolar, extracts clock, and produces the regenerated, scrambled PCM and clock. After descrambling, demultiplexing is done by alternately clocking two D-type flip-flops. Since demultiplexing in this manner can result in arbitrary steering of the A and B digroup bit streams at start-up, there is equal probability of steering the A digroup bit stream to the B receive unit. Knowledge of A-bit followed by B-bit multiplexing scheme and signals from the A and B receive units provide the means to automatically correct the data steering if it is incorrect. The logic in essence requires that the A frame bit occur before the B frame bit. If the B frame bit precedes the

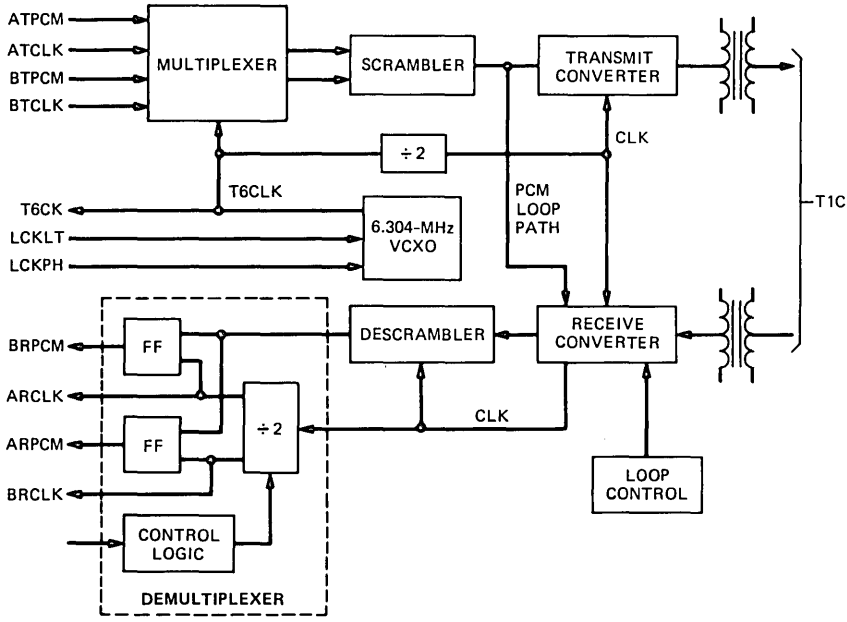

Fig. 23—Line interface unit-1.

MODE 1 MULTIPLEXED DATA FORMAT:

S_A S_B $F1_A$ $F1_B$ (96) $F1_A$ $F1_B$ (96) $F0_A$ $F0_B$ (96) $F0_A$ $F0_B$ (96) ....

CH 1-6 CH 7-12 CH 13-18 CH 19-24

- SUFFIXES A, B REFER TO A AND B DIGROUPS, RESPECTIVELY.
- SUPERFRAME BITS: F1 = LOGICAL ONE, F0 = LOGICAL ZERO.
- S_A, S_B ARE S BITS OF A AND B DIGROUPS, RESPECTIVELY.
- (96) = REPRESENTS 96 PCM BITS, 8 BITS PER CHANNEL, 6 CHANNELS FROM DIGROUP A AND 6 FROM DIGROUP B. PCM INTERLEAVED, I.E. –

1A	1B	2A	2B	3A	3B	4A	4B	5A	5B

B DIGROUP PCM BIT

A DIGROUP PCM BIT

Fig. 24—Mode 1 multiplexed data format.

A frame bit, the logic inverts the phases of ACLK and BCLK to the flip-flops such that the receive units do not go out of frame and the data is properly strobed.[21]

The clock generator has a 6.304-MHz clock (T6CLK), which controls timing for the LIU multiplexer, transmit converter, and the two transmit units.

Maintenance looping to test bank operation is provided through the

receive converter circuit, which is controlled by the bank alarm unit. When the maintenance loop is activated, the receive converter switches from the normal PCM input to the loop path and the transmit converter supplies an all-ones code to the distant terminal.

5.6.2 Mode 2

A block diagram of LIU-2 is shown in Fig. 25. As mentioned previously, Mode 2 is M1C multiplex compatible, requiring that the asynchronous digroups be synchronized for multiplexing. The multiplex/demultiplex circuits work with the syndes circuit (Fig. 26) to synchronize the digroup signals on the transmit side (TPCM) and perform a desynchronizing and smoothing of the digroup signals on the received, negated PCM (RNPCM). There are two identical but independently operating syndes circuits on the SU, one for each digroup. In each syndes 8-bit, elastic store circuits provide temporary storage for both the synchronizing and desynchronizing functions. The elastic store in the synchronizer has data sequentially written in by the transmit clock (TCLK) and data read out by the multiplexer clock (MCK). The multiplexer inserts stuff bits (Fig. 21) when the elastic store stuff request (SR) is activated. Desynchronizer input data is DCH, which is written in by the destuffed clock (DCLK). The read clock (RCLK) is generated by a VCO, which is phase-locked to the write clock. The bandwidth of the phase-locked loop is set to greatly reduce the jitter introduced by bit stuffing and control bit multiplexing.

The multiplexer and demultiplexer circuits (Fig. 25) are complementary metal oxide semiconductor (CMOS) large-scale integration (LSI)

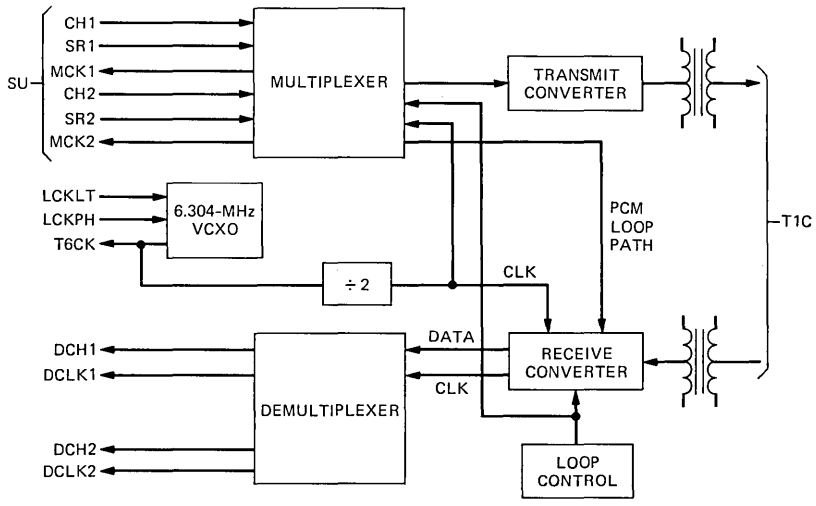

Fig. 25—Line interface unit-2.

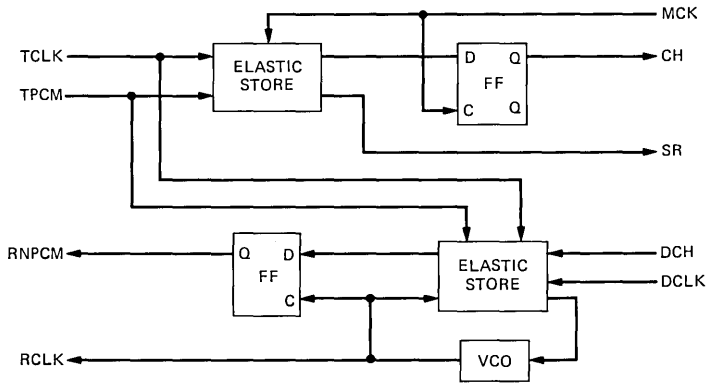

Fig. 26—The syndes circuit.

devices that supply the M1C-compatible format, and the transmit and receive converters provide the line interface functions, both of which we described earlier.

The loop control logic activates the loop path for maintenance. As we noted previously, there are two modes of looping: one is the fast loop, and the other is a maintenance loop, which loops the transmitted data and transmits all ones on the T2 line.

5.6.3 Mode 3

As we see in Fig. 27, the line interface unit for Mode 3 is an essentially independent digroup operation over T1 lines. It consists primarily of transmit and receive converter circuits for each digroup, which interface with the T1 lines. A common 6.176-MHz VCXO provides transmit timing for both digroups. There are independent digroup alarm and maintenance loop functions in this mode.

5.6.4 Mode 4

Mode 4 is a dual D4 bank configuration that multiplexes four digroups into an M12-compatible DS2-level signal. Because two D4 banks must be interconnected to combine the signals, wires must be added between one backplane connector on each of the banks. In addition, a transmit line interface unit (LIU-4T) is inserted in one bank and a receive line interface unit (LIU-4R) in the other. The transmit LIU multiplexes four digroup signals from both banks, and the receive LIU demultiplexes the four digroup signals. Figure 28 illustrates the line interface units and major interconnections between banks.

As with Mode 2, the banks have syndes units installed for the synchronization/desynchronization of the digroup signals. In effect,

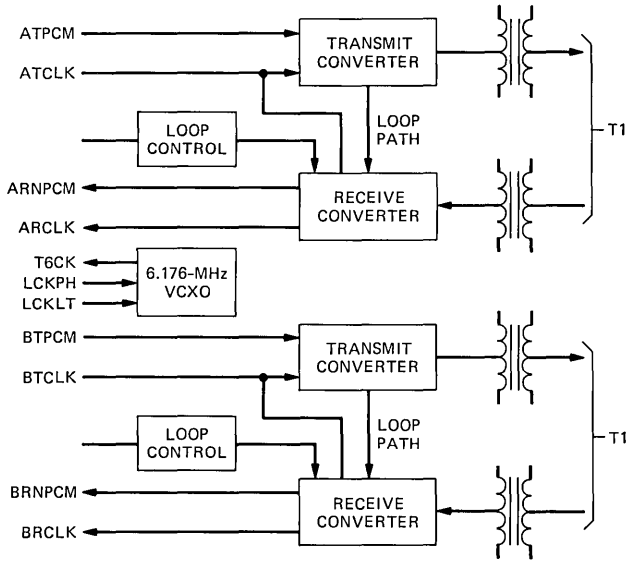

Fig. 27—Line interface unit-3.

Mode 4 incorporates an M12 multiplexer within the banks. This has been made physically possible by the LSI multiplex devices.

The code translator establishes the binary six zero substitution (B6ZS) coding to meet the T2 and M12 compatibility requirements.

Both the in-service fast loop and maintenance loops are included in the LIU circuits. The 6.312-MHz crystal oscillator (XO) provides the timing for both the multiplexer and the T2 line. The 6.176-MHz VCXO oscillators generate transmit clock signals for the bank transmit units.

A variation of Mode 4 is also available that is an M12-compatible interface to T2 facilities at intermediate power stations for add/drop capability. This mode, termed Mode 4A, requires LIU-4TA and LIU-4RA, which are similar to those shown for Mode 4 except that it has lightning protection, since the LIUs interface to T2 lines without intervening T2 office repeaters.

5.6.5 Mode 5

The recent addition of a lightwave system interface capability to the D4 banks illustrates the flexibility of both the electrical and physical architecture of the D4 design. The information-carrying capacity of Mode 5, as well as much of the line interface circuitry, is the same as for Mode 4. In Mode 5, two banks are interconnected, and the four digroups are multiplexed using the same devices as in Mode 4.

Figure 29 is a block diagram of the line interface units for Mode 5. The optical transducer circuits are not physically located in the LIUs

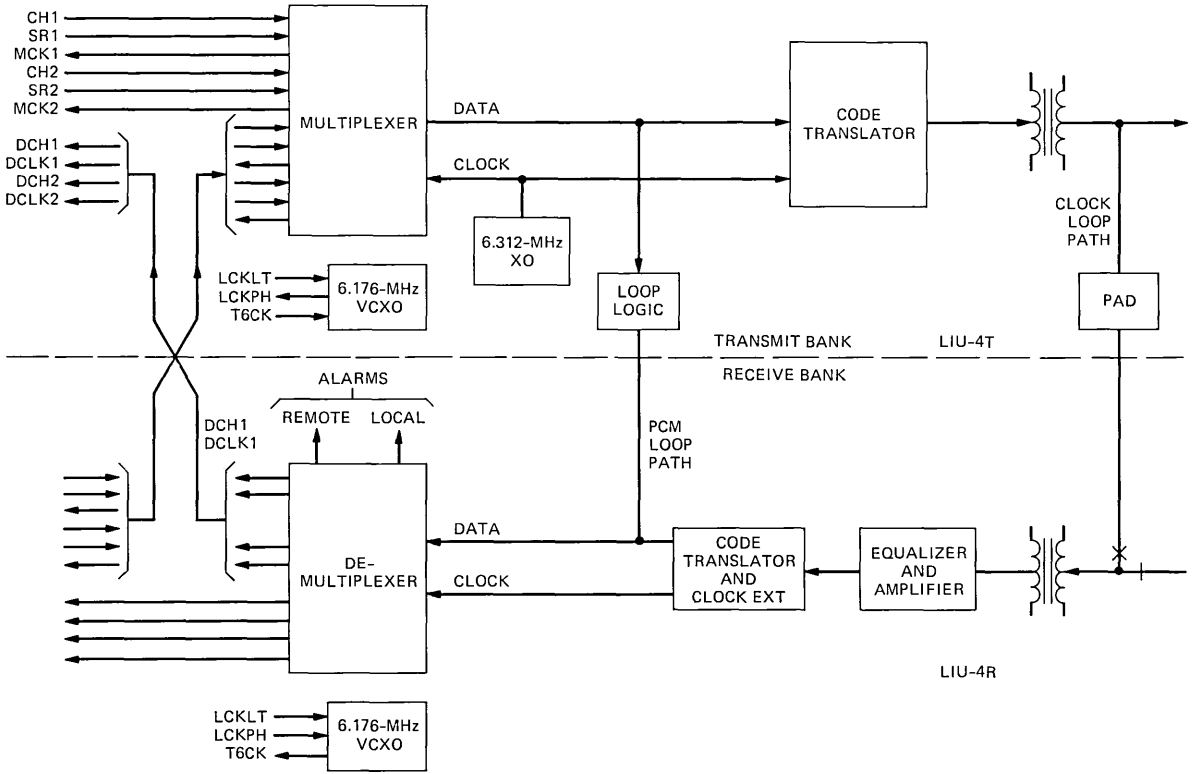

Fig. 28—Line interface units-4T and -4R.

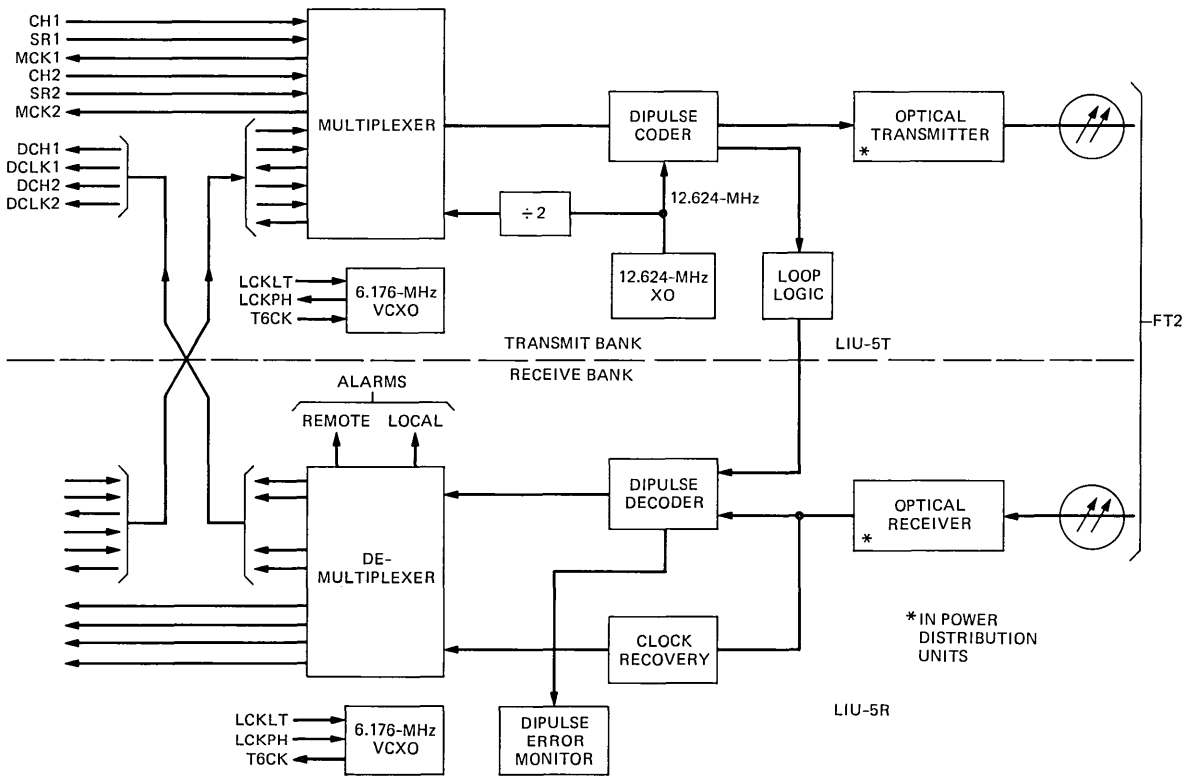

Fig. 29—Line interface units-5T and -5R.

but in special power distribution units where the optical fibers are connected.

Because the lightwave system components have much greater bandwidth available than necessary for the 6.312-Mb/s multiplexed data, the data is dipulse coded. The dipulse code format has several advantages for the lightwave application. It has two levels, avoiding nonlinearity problems with the laser, which would result from a three-level code; there are no long strings of zeros, thus making timing recovery easy; and redundancy is included for error detection.

The dipulse coding scheme uses only two levels to achieve analogous capability to three-level bipolar coding used with the wire systems. Correspondence of the two coding schemes is illustrated in Table VI below. Use of the dipulse code doubles the lightwave system bit rate to 12.624 Mb/s. The dipulse coded signal drives an injection laser transmitter. On the receive side, an avalanche photo diode (APD) detects the lightwave pulses, which are processed by an optical receive circuit. The APD receiver has automatic gain control with a dynamic range of approximately 85 dB.

The dipulse decoder converts the bit stream back to 6.312 Mb/s for demultiplexing. It also detects dipulse code errors that accumulate in the error monitor and turn on an LED indicator if the bit error rate exceeds 10^{-6}. Alarm control units initiate trunk processing to remove the banks from service if the digroup error rates exceed approximately 10^{-3}.

Present lightwave component technology allows this Mode 5, FT2-level signal to transverse lightguide distances of up to 4.5 miles without optical repeaters. This corresponds to maximum optical loss of 48 dB.

Connection to the lightguide cable is made through protected single fibers that connect at the rear of the power distribution units on one end and at the lightguide cable interconnection equipment (LCIE) at the other. The LCIE provides the terminations for the incoming lightguide cable. The lightguide ribbons (12 fibers per ribbon) are connected to a fan-out assembly, which provides separate connectorized fibers. The lightguide fiber is a low-loss graded-index type with a 55-μm diameter core.

Table VI—
Correspondence of bipolar and dipulse coding schemes

Bipolar Code	Dipulse Code
+1	11
0	10
−1	00

D4 Mode 5 and the other FT2 system components utilize modified versions of the optical circuits developed for the FT3 Lightwave Digital Transmission System, as well as the same lightguide cable, LCIE, and hardware. The optical transmit circuit uses a GaAlAs injection laser diode operating at a wavelength of 825 nm. In the optical receiver, the APD circuit current gain ranges from approximately 6 to 120. Bias for the APD is supplied by a ±5 to −575 volt dc-to-dc converter and a high-voltage regulator circuit.

5.7 Office interface

D4 office interface units (Fig. 1) are optionally used as a common access point for connecting the D4 bank to external timing sources. They also are used as circuits for loop timing of the transmitted PCM with the received clock. Loop and external timing of the banks is required by electronic switching system (ESS) switches and digital data system (DDS) applications.

VI. ALARMS AND TRUNK PROCESSING

6.1 ACU functions

The D4 alarm control unit (ACU) is the alarm center for the D4 channel bank. In all modes except Mode 1 ACUs are required for each digroup to monitor alarm status and facilitate location of transmission failures.

As Fig. 30 shows, the ACU monitors outputs from the receive unit to

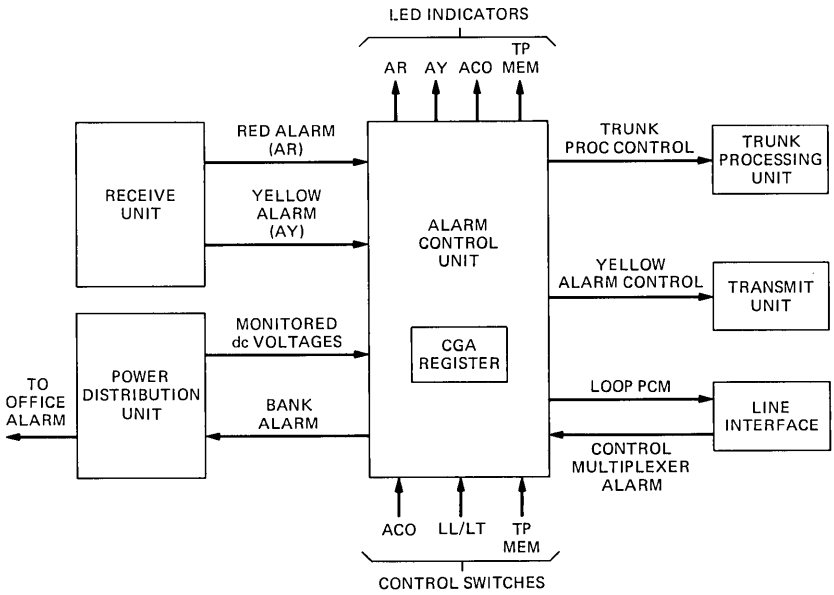

Fig. 30—Bank alarm and maintenance.

detect incoming alarms and control trunk processing, local office alarms, and transmission of alarm signals to banks at distant offices. In addition, it initiates alarms in response to dc power failure. The ACU controls trunk processing to remove trunks from service when a failure occurs (carrier group alarms) and totals the number of times service is lost by an electromechanical register.

Features of the D4 design include a minimum 2.0-second delay before bank and office alarms are turned on and trunk processing is initiated (versus 0.3 second for earlier banks). In addition, the features include hit integration, which reduces sensitivity to sporadic alarm signals while maintaining capability to alarm when intermittent alarm signals persist. The ACU timing circuits utilize current sources to drive capacitors connected to the input of comparators obtaining nearly linear voltage changes. Hysteresis enables positive comparator output switching to occur at the timing threshold voltages. The active circuit portions of the timers comprise two 16-pin dual in-line package (DIP) integrated circuits, and the ACU logic is contained in two custom transistor-transistor logic (TTL) gate array devices. Figure 31 is a functional block diagram of the alarm control unit.

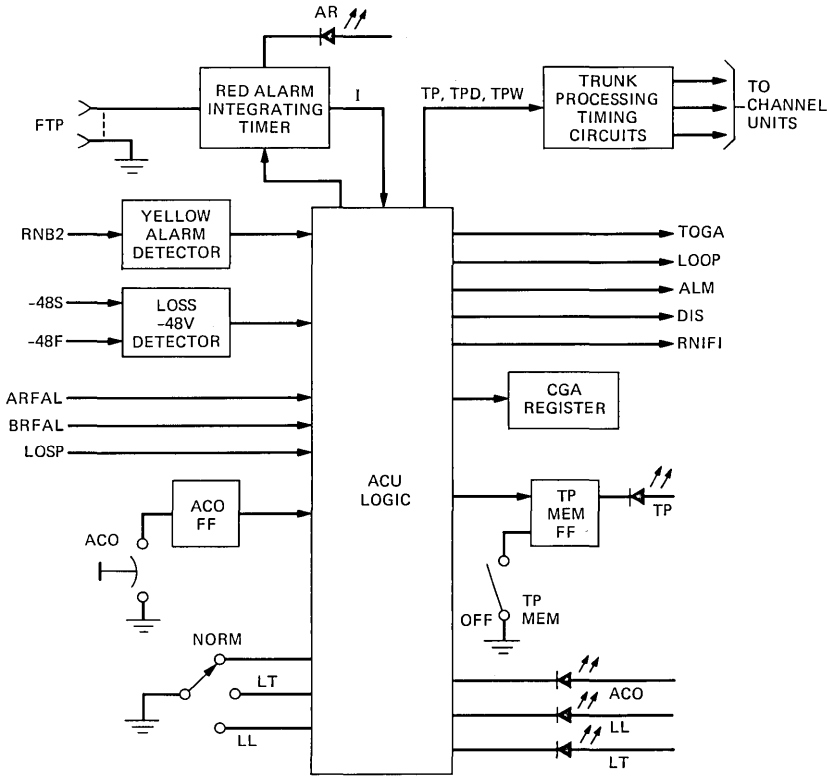

Fig. 31—Functional diagram of the alarm control unit.

6.2 General description of operation

6.2.1 Red and yellow alarms

The ACU responds to several types of alarm conditions that indicate digital line or bank failure. They are designated as red alarm (AR) when locally detected and yellow alarm (AY) when detected at the distant terminal. Red and yellow light-emitting diode (LED) indicators are mounted on the ACU faceplate. The AR indicator is ON whenever an alarm signal is present; however, trunk processing is not started, and bank and office alarms are not turned on until after the 2-second delay interval. In the case of a yellow alarm the indicator turns ON, trunk processing is initiated, and bank and office alarms are triggered simultaneously after the alarm is detected (approximately 450 ms).

A red alarm occurs as a result of loss of incoming digital information, either because of digital line or local bank receive side failure or a bank power failure. A yellow alarm occurs as a result of transmitting line or transmitting side local bank, or receiving side at the distant terminal failure. The yellow alarm is transmitted by the distant bank when it indicates a red alarm. Another alarm situation is presented as simultaneous red and yellow alarms. This happens when a yellow alarm is followed by a red alarm and occurs if the far end detects a red alarm and is looped to determine if the failure is within that bank.

6.2.2 Trunk processing

After initial timing requirements are met, a red or yellow alarm causes the ACU to initiate trunk processing to remove the trunks from service. Circuits within the ACU signal to operate relays located in the trunk processing unit. Contacts on these relays are connected to the channel units to control trunk processing. A yellow LED (TP), located on the ACU faceplate, is turned ON to indicate the bank is out of service. After the alarm has been cleared and a nominal delay interval of 15 seconds has elapsed, the bank is returned to service and the TP indicator is turned OFF. In the case of the yellow alarm, the restoral delay is controlled by the bank transmitting the yellow alarm. This results in a coordinated restoral of the system into service.

6.2.3 Alarm cutoff

The ACU has a pushbutton alarm cutoff (ACO) to turn off bank and office alarms. Depressing the ACO pushbutton will cause the ACO LED to be locked ON and the bank and office alarms to be turned OFF. The ACU panel alarm indicators (AR and AY) are not extinguished, however, until the trouble is cleared. If an alarm occurs as a result of a fuse operation or power converter failure, the ACO pushbutton is

prevented from clearing the bank and office alarms. In these cases, the ACO LED will not turn ON, and the fuse must be replaced, or the power converter turned OFF to silence the alarms.

6.2.4 DC power monitoring

The ACU monitors particular −48-volt office battery leads and the output voltages of the bank dc-to-dc converter and performs the following functions:

(*i*) Loss of −48 volts: Immediately turns on AR indicator, and after approximately 2.5 seconds, it turns on bank and office alarms and initiates trunk processing.

(*ii*) Loss of dc-to-dc converter outputs: Immediately initiates bank and office alarms and causes trunk to be removed from service.

6.2.5 Troubleshooting

The ACU provides a switch (LT/LL) that conditions the bank to aid in locating troubles. The switch is only functional when the trunks are removed from service by the TPU (normally as a result of an AR or AY alarm and ACO operation). With the switch set to the LT position, the maintenance loop is activated. This causes the digital output of the bank to be looped to the input in the line interface unit to determine whether the bank is operating normally. In the LL position, the yellow alarm is transmitted to hold the bank out of service to allow trouble-shooting of digital line problems by transmission loop patches at repeater locations. When the patch provides good transmission, the red alarm at the bank clears but the yellow alarm is looped to hold the bank out of service. Proper operation of the LL feature requires that *both* bank LL switches be thrown to avoid inadvertent restoral of one or both terminals under "noisy line" conditions.

6.3 Circuit overview

Refer to the functional block diagram of the ACU as presented in Fig. 31. The ACU logic is implemented in two custom TTL gate array devices. There are five timing circuits in the ACU; two are illustrated explicitly in Fig. 31 as the red alarm integrating timer and yellow alarm detector. The three remaining timing circuits are incorporated in the trunk processing timing circuits and ACU logic. All of the switches and LED indicators are located on the ACU faceplate.

The red alarm inputs are loss of PCM (LOSP), A digroup of frame alarm (ARFAL), and B digroup frame alarm (BRFAL). The −48F and −48S inputs are monitored by the loss −48-volt detector, which also initiates the red alarm if any of these voltages fail. The receive, negated

bit 2 (RNB2) input is digit (or bit) two of the PCM word, which indicates the yellow alarm when fixed at logic one.

The ACU outputs include TU, TP, trunk processing delayed, and trunk processing wink outputs control relays in the TPU. Transmit outgoing alarm (TOGA) is an output to the TU to control the transmission of the yellow alarm in the PCM output. RNIFI is logic output that controls signaling storage. DIS is a logic output that controls the sampling gates in the channel units. LOOP is a relay drive output signal to operate the looping relay in the line interface unit. Output ALM controls the bank alarm relay.

The purpose of each of the main functional components of the ACU circuit is described in the following paragraphs.

6.3.1 Red integrating alarm timer

The red integrating alarm timer performs the following functions:

(*i*) It provides a nominal 2.5-second delay between receipt of a red alarm signal and initiation of trunk processing.

(*ii*) It integrates intermittent red alarm inputs with a nominal 6 to 1 ratio (i.e., it times out towards the alarm state at a rate six times faster than it recovers toward nonalarm state).

(*iii*) When trunks are processed, it provides a nominal 15-second delay after the last alarm before the service is restored.

(*iv*) It provides a means to force trunk processing without an alarm by shorting a special jack (FTP).

6.3.2 Yellow alarm detector

The yellow alarm detector performs the following functions:

(*i*) It provides a nominal 450-ms delay between receipt of the last PCM bit two pulse (RNB2) and initiation of the yellow alarm and trunk processing.

(*ii*) It provides immunity to noisy lines by integrating the RNB2 pulses.

(*iii*) It provides a nominal 30-ms delay before clearing a yellow alarm to reduce sensitivity to a noisy line.

6.3.3 TP memory flip-flop

The TP memory flip-flop (FF) optionally allows the occurrence of a single trunk processing event to be held indefinitely, as indicated by the TP LED remaining ON after the trunks have been processed and returned to service. The TP LED is placed in this mode by setting the OFF/MEM switch to the memory mode position MEM. This is useful to bring attention to banks that experience intermittent failures. With

the switch in the OFF position, the TP LED is only ON during the time the trunks are out of service and turns OFF when service is restored.

6.3.4 CGA register

The CGA register is an electromechanical register that records the number of times the bank trunks are taken out of service. Each time trunk processing occurs, the register is incremented.

6.3.5 Trunk processing timing circuits

When trunk processing is initiated by a red or yellow power alarm or by forcing the FTP input, a simple sequence of relay drive signals is initiated to operate the relays located in the TPU. The trunk processing timing circuit provides the required sequence of relay drive signals.

6.3.6 ACO flip-flop

The ACO pushbutton switch turns off bank and office alarms when depressed following a red or yellow alarm. The ACO FF holds the alarm OFF. It also serves to enable the LL/LT switch after an alarm has occurred and been cut off. The LL/LT switch is disabled if alarm and ACO have not occurred. This prevents inadvertent looping of the banks while they are in service.

6.3.7 ACU logic

The logic gates interconnecting the functional ACU blocks provide the required digital logic to control the various output signals and status and alarm LEDs. The logic gates are included in two integrated gate array devices.

6.4 Summary of ACU timing

Table VII summarizes the timing functions for the ACU.

Table VII—ACU timing

Red Alarm (AR)	
Initiation	2.5 ± 0.5 seconds*
Integration Ratio	6/1 ± 20%
Time to return trunk to service after alarm clears	15 ± 4 seconds
Yellow Alarm (AY)	
Initiation	450 ± 100 milliseconds
Time to return trunks to service after alarm clears	30 ± 6 milliseconds

* The AR LED is ON whenever an alarm signal occurs, but alarm status and trunk processing is not initiated until this time has elapsed. For intermittent alarms, the initiation time is longer because of the alarm integration.

VII. DC POWER

Power is supplied to the D4 bank circuits by means of an efficient, low cost, dc-to-dc power converter unit (PCU) that operates from the office −48 volt supply. The output voltages for the D4 circuits are +5 and ±12 volts. The power unit consists of an input filter, switching power amplifier, power transformer, output rectifiers filters, and control circuits.

The PCU voltage outputs have ripple voltages of less than 30 mv rms over a 0- to 20-MHz frequency band. Tolerance on the output voltages is ±5 percent for the ±12 volt outputs and ±10 percent for the +5 volt output. The converter has over-voltage protection and low-voltage alarm indication.

The power unit provides an input switch with a mechanical interlock that automatically turns the power off when the unit is being removed from the D4 bank. The faceplate has alarm and alarm cutoff LED indicators and test points for measurement access to the ±12 and +5 output voltages.

A power distribution unit (PDU) furnishes a fused −48-volt distribution arrangement for the bank PCU and other circuits. Office alarms and a local PDU alarm are activated by any fuse or bank failure. The PDU also has a filtered talk battery and 20-Hz ringing supply outputs.

VIII. SUMMARY

The D4 channel bank is a versatile, cost-effective addition to the digital telephone plant. Circuits designed for D4 have been incorporated into many other parts of the digital plant. The most prominent additional applications of the D4 circuits (and some of the D4 hardware) include the *SLC*-96 subscriber loop terminals, and the LT-1 connector.

Many of the D4 LSI integrated circuits have been incorporated into other parts of the digital network, such as the digital interface frame (DIF) for No. 4 ESS, and maintenance systems, such as the digital access and cross-connect system DACS and DATS.

The success of the D4 bank and D4 technology is the result of close and extensive cooperation among many Bell Laboratories organizations.

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GLOSSARY

ACO	alarm cutoff
ACU	alarm control unit
ALM	alarm
ALM DET	alarm detector
APD	avalanche photo diode
AR	red alarm
ARFAL	A digroup receive frame alarm
ARNPCM	A digroup inverted PCM
ARCLK	A digroup receive clock
ATCLK	A digroup transmit clock
ATPCM	A digroup transmit PCM
AY	yellow alarm
B6ZS	binary six zero substitution
BRCLK	B digroup receive clock
BRFAL	B digroup receive frame alarm
BRNPCM	B digroup receive PCM
BTCLK	B digroup transmit clock
BTPCM	B digroup transmit PCM
CBIC	complementary bipolar integrated circuit
CCIS	common-channel interoffice signaling
CGA	carrier group alarm
CH	channel
CMOS	complementary metal oxide semiconductor
CODEC	coder-decoder
CU	channel unit
DAC	digital-to-analog converter
DACS	digital access and cross-connect system
dBTL	decibels-transmission level
dBrnCO	dB above reference noise, measured with C-message weighing at 0 transmission level point
DCH	destuffed channel (PCM)
DCLK	destuffed clock
DDS	digital data system
DEMUX	demultiplexer
DIF	digital interface frame
DIFF COMP	differential comparator
DIP	dual in-line package
EQL	equalizer
ESS	electronic switching system
EXT	external
FET	field effect transistor
FF	flip-flop

FS	signaling, frame signal pattern
FT	terminal frame signal pattern
JFET	junction field-effect transistor
LBO	line build-out network
LCIE	lightguide cable interconnection equipment
LCKLT	line interface unit clock loop time
LCKPH	line interface unit clock phase control
LCLK	loop clock
LED	light-emitting diode
LIU	line interface unit
LL	line loop
LOSP	loss of pulse code modulation
LPCM	loop pulse code modulation
LSB	least significant bit
LT	loop terminal
MCK	multiplexer clock
MEM	memory
MUX	multiplexer
OOF	out-of-frame
OPT RCVR	optical receiver
OPT TRMTR	optical transmitter
PAM	pulse amplitude modulation
PCM	pulse code modulation
PCU	power converter unit
PDU	power distribution unit
PLL	phase-locked loop
RC	resistor-capacitor
RCLK	read clock
RCLK	receive clock
RFA	receive frame signal for A digroup
RFB	receive frame signal for B digroup
RNB2	receive, negated bit 2
RNIFI	logic output that controls signaling storage
RNPCM	receive, negated pulse code modulation
RPAM	receive pulse amplitude modulation
RPCM	receive pulse code modulation
RU	receive unit
S/D	signal-to-distortion
SBC	standard buried collector
SIC	silicon integrated circuit
SMAS	switched maintenance access system
SR	stuff request
SU	synchronizing-desynchronizing unit
SUM	summing

syndes	synchronizing-desynchronizing
T6CK	transmit 6 megahertz clock
TCLK	transmit clock
TINH	transmit inhibit
TNEN	transmit, negated enable
TOGA	transmit outgoing alarm
TP	trunk processing
TPAM	transmit pulse amplitude modulation
TPCM	transmit pulse code modulation
TPD	trunk processing delayed
TPM	trunk processed memory
TPU	trunk processing unit
TPW	trunk processing wink
TSYNC	transmit synchronization
TTL	transistor-transitor logic
TU	transmit unit
VCO	voltage-controlled oscillator
VCXO	voltage-controlled crystal oscillator
VF	voice frequency
XO	crystal oscillator

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D4 Digital Channel Bank Family:

The Maintenance Bank

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The D4 Maintenance Bank (D4MB) is a centralized facility for testing D4 channel units as well as a place for the hot monitored spare of all common equipment used in the D4 channel bank. At least one D4MB equipped with D4 channel units is recommended for each office. The D4MB contains a test set and two digroups of common equipment that simulate the D4 digital system. When a channel unit needs to be tested, it is inserted in the test position of the D4MB and the craftsperson tests it by following simple instructions listed on 3x5 plastic cards. These tests are performed on any given code of channel unit, usually without changing any options in the channel unit under test. Voice-frequency (VF) and signaling tests are performed on the channel unit under test. These tests assure the craftsperson that the unit under test will not affect or impair the transmission of other channel units already installed in working D4 channel banks. The D4MB is an inexpensive and simple D4 plug-in unit test vehicle for craft use. It has proven extremely reliable in determining whether a unit is good or defective. Testing with the D4MB has greatly increased the office personnel's confidence in both channel units and common units that are to be used in a working D4 channel bank. As a result, significant cost savings have been realized using the D4MB by virtually eliminating unnecessary shipping and retesting of good units that might have been previously returned to the factory for repair.

I. INTRODUCTION

With each generation of D-type channel banks, the testing and maintenance facilities have been improved. In the D3 system, a shelf

of "hot spare" common equipment was used with special electronic circuits built into the bank to localize trouble in a specific plug-in unit. With the D4 channel banks, additional maintenance testing features have been developed. The most notable development is the D4 Maintenance Bank (D4MB). The D4MB is a channel unit test set and a common equipment monitoring facility for use in offices where D4 channel banks are installed. It can be used in any centralized testing facility where a -48 volt connection is available. The D4MB contains two Maintenance Bank Test Sets (MBTSs), two complete digroups of D4 common equipment, and one four-Wire E and M (4EM) channel unit. The MBTS is used for testing D4 channel units and for monitoring the performance of the common equipment. The monitored common equipment plug-ins may be used as "safe operable" units for restoring service to a failed D4 bank. The common units are also used in the D4MB to generate the appropriate pulse code modulation (PCM) and timing control signals for testing channel units. The common units function as if they were in a working D4 system. Figure 1 shows a D4MB fully equipped with common equipment and MBTS plug-in units.

II. FUNCTIONS OF MAINTENANCE BANK

2.1 Common equipment monitoring

There are three main functions for which the D4MB can be used: hot spare monitoring, quick check of any D4 unit, and channel-unit testing. The hot spare monitoring function ensures that common units installed in the D4MB are good. Figure 2* shows a typical monitoring mode of operation. In the monitoring mode, the MBTS supplies a 1020-Hz tone to a Channel-Unit Simulator (CU SIM) in the MBTS into a looped digroup of common equipment and then through a second tandem digroup of looped common equipment through a 4EM channel unit. The 1020-Hz tone level out of the 4EM channel unit is monitored by the MBTS voice-frequency level-detector. An alarm is generated by a Maintenance Bank Alarm Unit (MB ALM) if the monitored output level is not within ±0.5 dB of its nominal level. This alarm can be disabled manually by a switch on the MB ALM. While there are certain types of failure in D4 common plug-in units that would not be detected in this monitor mode, the message transmission path including the coder, decoder, clock circuits, and the Line Interface Unit (LIU) multiplexing and demultiplexing circuits are verified as being operative. Therefore, these common plug-in units can be used in an office as new units to correct trouble in a D4 channel bank and restore service.

* Acronyms and abbreviations used in the figures are defined at the back of this issue.

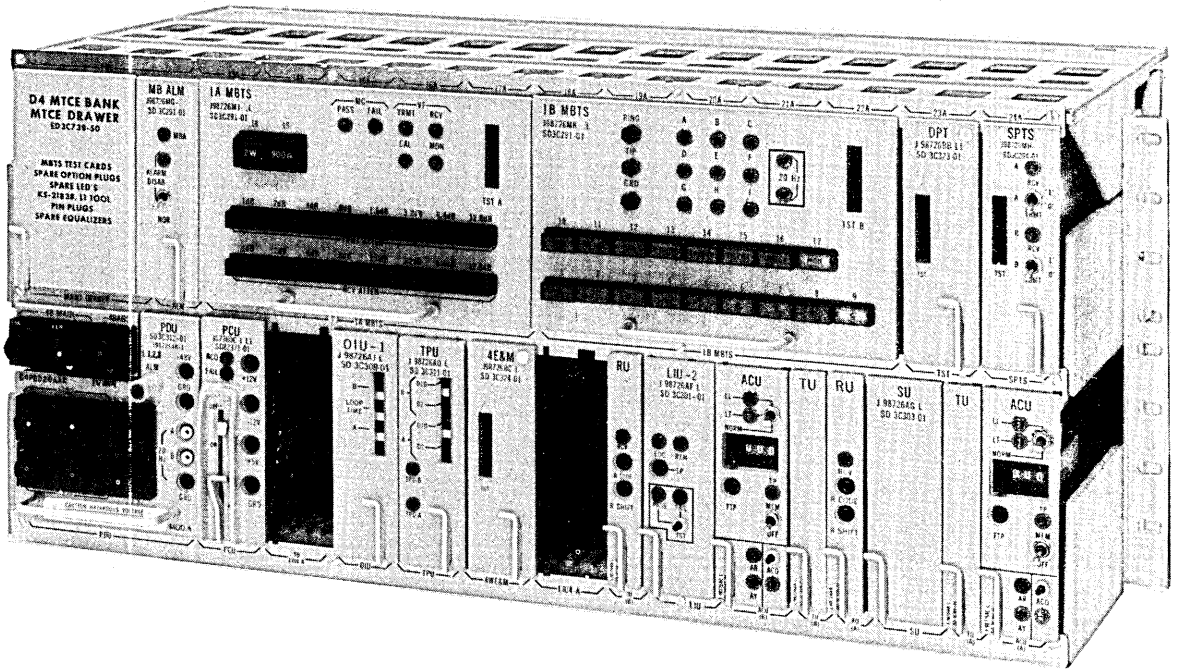

Fig. 1—A fully equipped D4MB with common equipment and MBTS plug-in units.

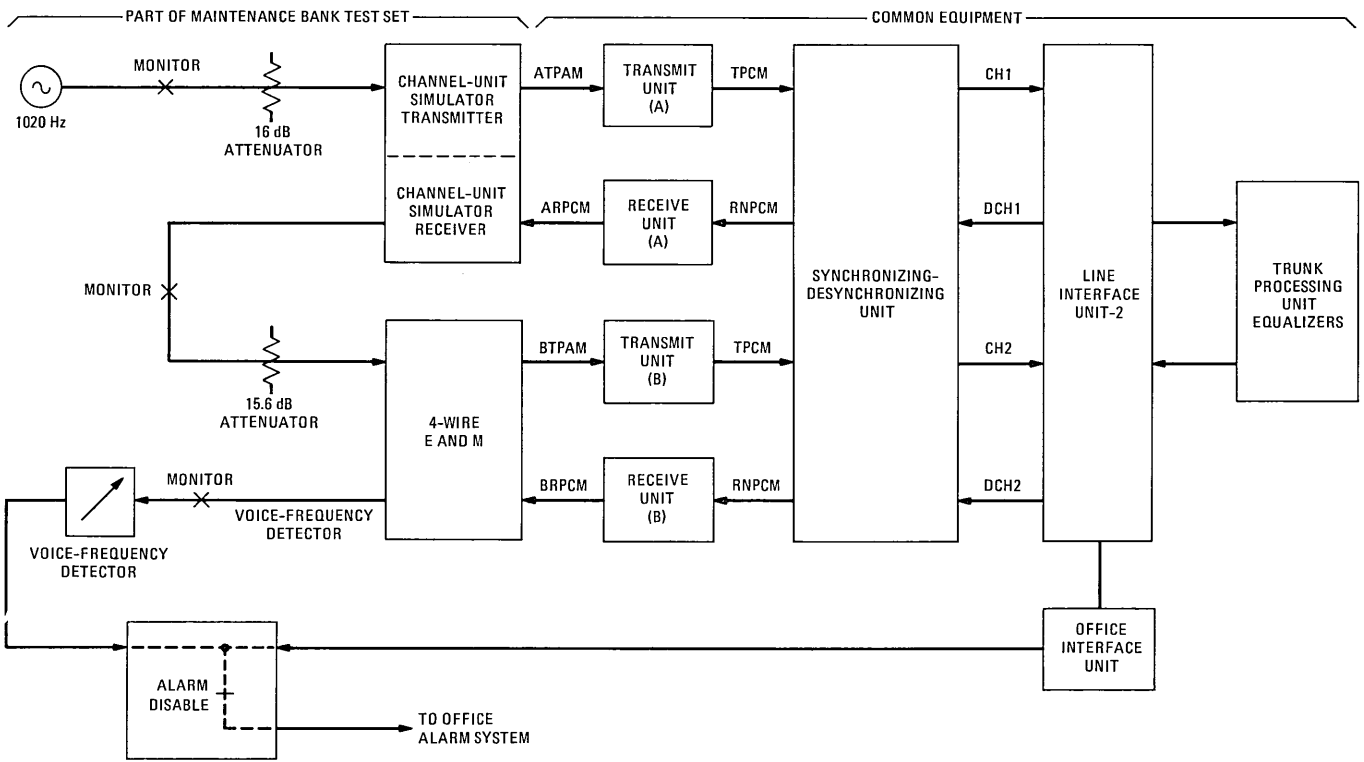

Fig. 2—D4MB monitoring arrangement.

2.2 Testing of ancillary circuits

The D4MB can quickly check a plug-in unit suspected of having a malfunction in a nontransmission-affecting circuit, e.g., alarm circuit. The maintenance bank is a complete D4 channel bank except for the absence of a full complement of channel units. Thus, with ancillary D4 test equipment, it forms a vehicle for performing any D4 test.

2.3 Testing of channel units

The D4MB can also test channel units. This test capability was previously not included in the maintenance equipment for earlier D-type banks. Channel units should be tested in the D4MB if there is any reason to suspect that a unit might be faulty. The test is made to ensure that other channels in a working bank will not be impaired by having a faulty channel unit inadvertently plugged into an in-service bank. The D4MB can also be used in the isolation of an end-to-end transmission of signaling troubles. Figures 3 and 4 show how the D4MB is arranged for channel-unit testing. The transmit and receive sides of the channel units are checked individually. The tests include the drop-side circuits (hybrids, signaling bridge, etc.) of the channel unit. These tests are more complete than previous D-type bank tests although less stringent than tests made at the faceplate four wirepoint. The tests performed on a D4 channel unit are:

(*i*) Loss (or gain) of the transmit portion of a channel unit at 1020 Hz.

(*ii*) Loss (or gain) of the receive portion of a channel unit at 1020 Hz.

(*iii*) Noise and crosstalk introduced into all adjacent time slots from the channel-unit transmitter.

(*iv*) Noise or crosstalk introduced into the channel-unit receiver from the other 23 time slots.

Items (*iii*) and (*iv*) above are called multichannel (MC) interference tests. These tests provide assurance that a newly installed channel unit will not impair the performance of other channels in an in-service D4 bank.

All channel unit tests are made by inserting the unit to be tested in the channel under test (CUT) position. Simple instructions for each code of channel unit to be tested are listed on a 3x5 plastic card. The tests consist of emulating all circuit conditions and displaying the results using LEDs.

III. MAINTENANCE BANK TEST SET CIRCUITS

The MBTS contains the circuit functions necessary to test both directions of transmission and signaling in D4 plug-in units. The following is a brief description of the MBTS circuits.

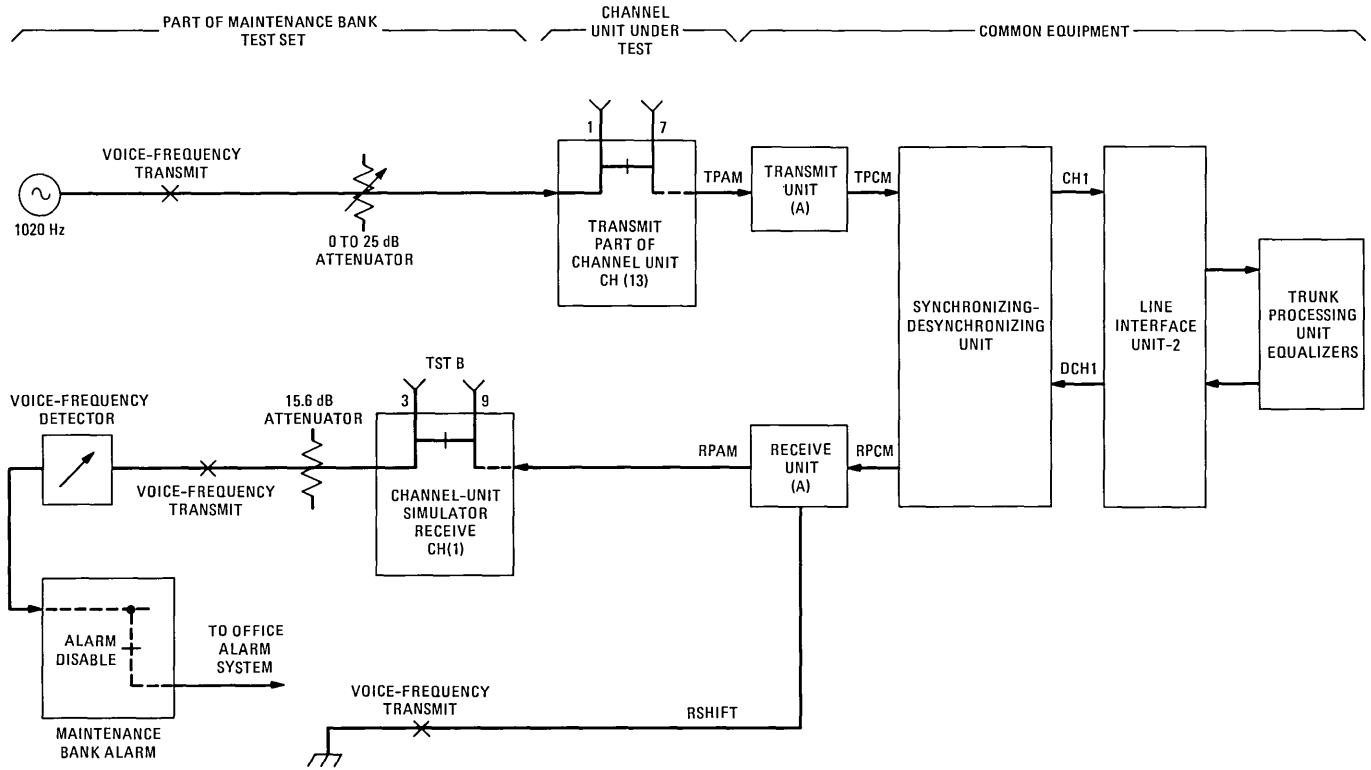

Fig. 3—D4MB voice-frequency transmitting (shown for Mode 2).

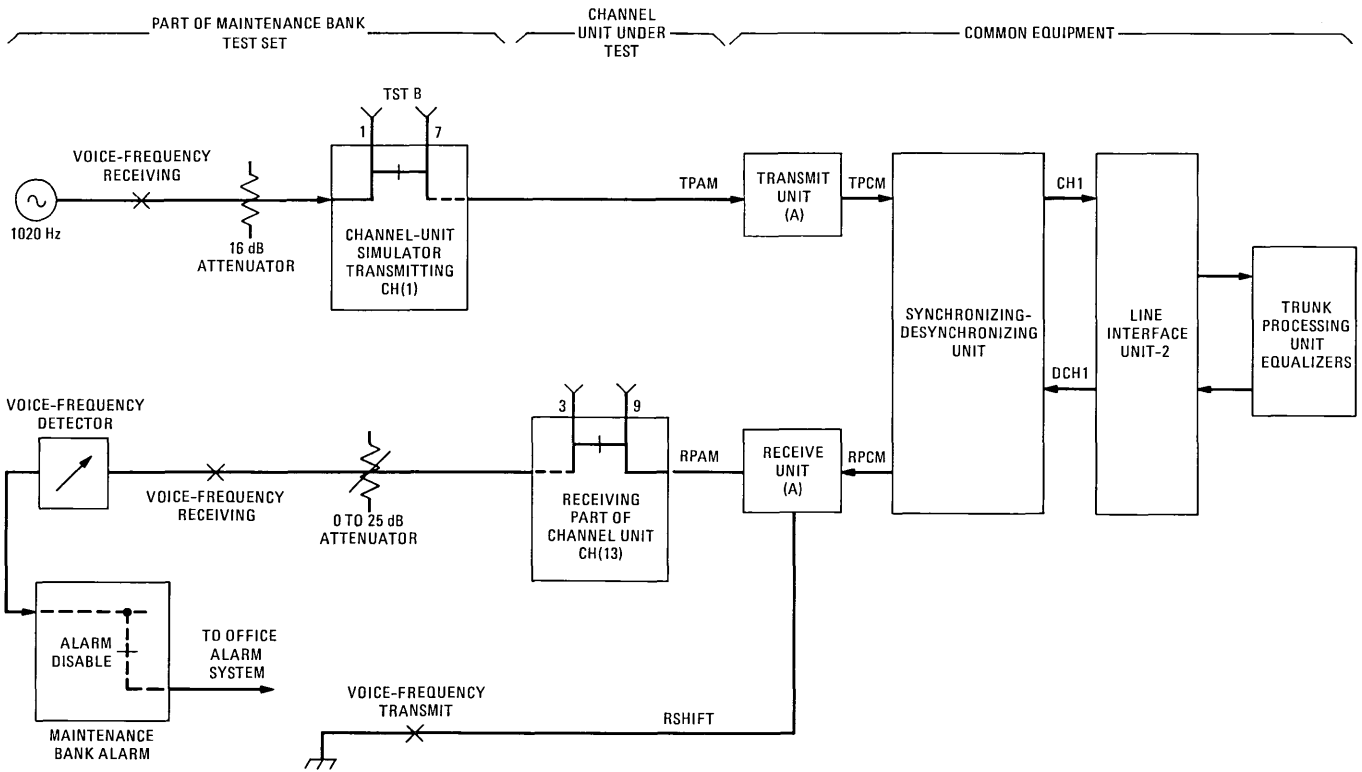

Fig. 4—D4MB voice-frequency receiving (shown for Mode 2).

3.1 VF oscillator

The VF oscillator circuit provides an extremely stable 1020-Hz sine wave for use in testing transmission levels and performing multichannel interference measurements.

3.2 Transmit and receive attenuators

A channel unit to be tested can have a variety of installed loss, depending on the office being served. Variable attenuators controlled by switches on the face of the MBTS are used to complement the installed loss in the channel unit so that these units can be tested at standard transmission levels.

3.3 Channel-unit simulator

The MBTS channel-unit simulator is essentially a D4 channel unit. This CU SIM is assigned to the channel 1 time slot while the channel unit under test is assigned to time slot 13. These two time slots were chosen so that the application of the R-SHIFT feature in the receive unit permits the CU SIM to communicate with the D4 channel unit under test.

3.4 VF-level detector

In the VF test mode, the voice-frequency-level detector compares the internally generated 1020-Hz test tone level with the tone received from the channel unit under test. If the two levels are within ±0.5 dB, a green (PASS) LED lights up. This same circuit is also used similarly during the monitor mode operation. In the monitor mode, it not only illuminates a monitor LED but it also triggers the MB ALM if the monitored level falls out of the ±0.5 dB range.

3.5 Multichannel detector (MC)

In the multichannel tests, analog and digital circuit functions are combined to simulate an interference signal. This signal is sent through the channel unit and the output is monitored. When the level of this interference power in the channel unit under test is less than -45 dBm0, a green LED (MC PASS) lights up. When the interference power in the channel unit is greater than -45 dBm0, a red MC FAIL LED lights up.

3.6 Signaling circuits

The signaling circuits apply steady-state signaling conditions to the channel unit under test. These signaling conditions are controlled by switches on the faceplate of the MBTS. Application of prescribed signaling conditions cause the channel unit under test to output steady-state signals to the signaling detectors.

3.7 Signaling detector circuits

The signal detector circuits interpret the signaling conditions delivered by the channel unit under test and illuminate LEDs on the front of the MBTS corresponding to these signaling states. The signaling condition and the corresponding LED display of the signaling states are given on the test card.

3.8 Alarm circuits

Alarms are processed in the maintenance bank alarm circuit when either the Monitor (MON) LED is not lit or when the Power Distribution Unit (PDU) indicates that the D4 common equipment failed and is in an alarm condition. Two contact pairs operate the office minor alarm audible and visual alarms. An alarm also lights up the maintenance bank alarm (MBA) LED on the face of the alarm unit. This outgoing alarm can be disabled by the ALARM DISAB switch. A yellow LED lights up on the MB ALM unit to indicate that the office alarm from the D4MB has been disabled. The ALARM DISAB switch is used to inhibit office alarms from the D4MB when channel units are being tested or when common equipment from the D4MB is being used to restore service in a failed D4 bank.

3.9 Control switches

Pushbutton switches on the MBTS control transmission and signaling conditions. Each D4 channel unit to be tested has information on instruction cards to indicate how to set the switches and what kind of LED response to expect for transmission and signaling tests.

IV. INSTRUCTION CARDS

Any standard D4 channel unit can be tested by following the instructions on a 3x5 index card for that particular code of channel unit. A craftsperson simply operates switches and compares the lighted LEDs with the indications on the instruction cards. There are more than 32 codes of channel units, each of which contains various options that can be tested with these instruction cards. Figure 5 shows a typical instruction card for voice-frequency and signaling tests.

V. LINE INTERFACE MODES OF D4MB OPERATIONS

The maintenance bank can be operated in any of the five D4 modes by equipping it with appropriate plug-in modules. This is accomplished by simply plugging in the appropriate LIU and, when necessary, a synchronizing-desynchronizing Syndes Unit (SU). Any one of the Office Interface Units (OIUS) can be placed in the bank. The operation and selection of plug-in units for the maintenance bank will be determined

SDPO SIG TESTS 3/78

OPTIONS: NONE CARD 1 OF 1

TEST	SWITCHES 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	LAMPS A	B	C	D	E	F	G	H	J	20 Hz
1.01																				A					F		H	J	
1.02				4																A					F	G			
1.03							7															C	D				H	J	
1.04						6			9																				
1.05	1					6			9											A						G			
1.06		2				6			9											A						G			
1.07																													
1.08																													
1.09																													
1.10																													

SDPO VF TESTS 3/78

1. OPERATE SWITCH ON MB ALM UNIT TO ALARM DISAB POSITION.
2. EXAMINE T ATTENUATOR IN CU TO BE TESTED AND DEPRESS TRMT ATTEN SWITCHES ON 1A MBTS WHICH CORRESPOND TO ATTENUATOR SECTIONS WITH A WHITE JUMPER PLUG IN THE ZERO SIDE.
3. EXAMINE R ATTENUATOR IN THE CU AND REPEAT INSTRUCTION 2 FOR THE RCV ATTEN SWITCHES.
4. TEST THE VF PORTION OF THE CU BY DEPRESSING THE SWITCHES AS INDICATED IN THE TABLE BELOW AND NOTE THE APPROPRIATE LAMP INDICATIONS.
5. IF THE CU FAILS ONE OR MORE OF THE TESTS, FOLLOW INSTRUCTIONS ON VF CALIBRATION CARD.

TEST		SWITCHES 7	9	10	11	12	13	14	15	16	17	18	19	LAMPS VF CAL	VF MON	VF TRMT	VF RCV	MC PASS	MC FAIL
2.01	VF XMT			10					15							TRMT			
2.02	VF RCV			10						16							RCV		
2.03	MC XMT			10			13											PASS	
2.04	MC RCV		9	10				14										PASS	

Fig. 5—D4MB test cards.

by the local operating personnel. This mode should be the same as is used in D4 banks in the office. Where more than one mode is used in an office, each mode can be monitored from time to time so as to be reasonably sure of having a "safe operable" LIU of the proper type on hand. The D4MB should be kept fully equipped with two digroups of common equipment. When one of these plug-in units is used for restoral, a D4 channel unit should be replaced in the D4MB with another unit.

VI. TESTING DATAPORT CHANNEL UNITS

The D4MB was originally designed to test only standard channel units and some early varieties of special service channel units. A recent modification was made to the D4MB back plane wiring to accommodate

testing of the new D4 dataport channel units in conjunction with readily available digital data test equipment. This equipment is the KS 20908, KS 20909 Data Test Sets, and the ED-3C792-31 Test Interface Unit. The modification is a required change to remove a voltage that could damage dataport channel units that are plugged into the CUT position of the D4MB. Further, the change provides an integrated clock signal from the OIU-2 in the D4MB. Since this change was initiated during the last quarter of 1980, a check should be made before dataport channel units are plugged into the D4MB. All D4MB's modified to accommodate dataport channel units are identified by the list numbers "WD" or "WE" stamped on the side of the shelf framework next to the J-code numbering.

VII. SPECIAL SERVICE CHANNEL UNITS

Some special service channel units, such as those with gain transfer, cannot be tested with the levels installed in that unit. The test card for the special service units with nonstandard ranges of transmission levels specify an exact amount of loss to be installed in that channel unit for testing. Also, not all special service units have signaling that can be fully tested in the D4MB.

VIII. PHYSICAL INFORMATION

The D4MB is completely self-contained and can be mounted individually or with D4 channel banks in a shop-assembled bay. It contains two shelves of plug-in units and occupies approximately 9-½ inches vertically on a 23-inch bay. Figure 1 shows a D4MB fully equipped with plug-in units for two D4 digroups of common equipment and one 4EM channel unit. The D4MB may be equipped for any of the D4 operating modes. The upper shelf has storage for the Signaling Path Test Set, a drawer for small maintenance parts and tools, and three Maintenance Bank Test Set plug-in units.

IX. SUMMARY

The D4MB is a monitoring system for ensuring that a set of "safe, operable" D4 common plug-in units is available for service restoral. It also can test channel units for defects that would impair service in a working bank. Furthermore, it is a simple-to-use test set and readily available in every D4 office. The D4MB has proven to be a useful tool for testing D4 units and has significantly reduced the number D4 units that might have been previously assumed bad and returned for repair.

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D4 Digital Channel Bank Family:

The *SLC*™-96 System

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The SLC-96 system is a digital subscriber carrier system that can carry up to 96 subscriber channels, when fully equipped, between a Central Office Terminal (COT) and a Remote Terminal (RT), using T1 digital lines. Typical economic applications are for expanding the service capability of existing cable plant or for new wire center deferral. Recent application studies show that SLC-96 systems will be economically attractive in many permanent subscriber applications. In addition to Message Telephone Service (MTS), the system can provide coin services, voice-frequency special services, and digital data services. The SLC-96 system is based on the transmission and physical format of the D4 system used for interoffice trunks. The system employs μ255 pulse code modulation (PCM) for voice transmission and, as a result, will allow the direct interface of the RT with a digital central office. Its maintenance features include channel and drop testing from a local test desk; single-ended, active, T1 fault-locating; automatic T1 line protection; extensive local and remote alarm displays; and outputs that can be transmitted to a remote operations center such as the Switching Control Center (SCC). The channel and drop testing scheme requires a Pair Gain Test Controller (PGTC) to be installed in each wire center containing one or more SLC-96 systems. Various other features that will enhance the application of the SLC-96 system in the loop plant include extended range channel units, remote T1 line power feed, and a variety of RT enclosures.*

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* *SLC* is a trademark of Western Electric.

I. INTRODUCTION

The subscriber loop is generally represented by pairs of metallic conductors that connect the customer's premises to the telephone network through a central office serving a locality. As low-cost electronic technologies continue to emerge, the subscriber loop, which was previously entirely metallic, is now being viewed as a potentially large market for the application of these technologies.[1] The electronic systems that have evolved to reduce the cost of growth in the loop plant are called pair gain systems. Most recently, the digital carrier-type pair gain systems appear to be well suited to growth of the network because of their high pair gain ratios realized by multiplexing with optional concentration and for their excellent signal quality resulting from digital transmission.

The digital subscriber carrier system is being used in increasing numbers today in the Bell System to bring toll-quality channels to customers in both suburban and rural areas. The *SLC*-96 system is a new, versatile pair gain system that provides an economic means of linking subscriber lines to the central office.[2,3] Like its predecessors, the *SLC*-96 system brings electronic technology to the loop plant, and in addition, the system may be used with the D4 channel bank to provide a new synergy between trunk and loop applications of digital carrier. Representing a significant step toward the Bell System's digital network of the future, the *SLC*-96 system can handle the broad spectrum of telecommunications services needed to meet today's widely varying requirements for both voice message and special communication services.

The new *SLC*-96 system has the versatility to serve rapidly growing suburban, as well as rural, areas with such benefits as conventional facility relief, wire center deferrals and replacements, improvements in transmission quality, and new communication arrangements for business complexes.[4,5] The *SLC*-96 system is a digital system that uses μ255 pulse code modulation, as does the D4 channel bank, and enables the RT to interface directly with a digital central office. Many of the D4 channel units may be used interchangeably in the *SLC*-96 or D4 systems. In addition, new dual-channel subscriber units have been designed exclusively for the *SLC*-96 system to permit as many as 96 single- or multi-party customer lines to be served from a *SLC*-96 channel bank. The full range of customer services offered by the *SLC*-96 system includes single-party, multi-party, and coin services. It can also provide many trunk and special services, including dataport, by using the standard D4 channel units. This paper gives a concise description of the *SLC*-96 system, highlighting its roots in the D4 system. Many of the unique features incorporated in the design of the

SLC-96 system will be described in detail in a future issue of the Bell System Technical Journal.

II. BASIC SYSTEM OPERATION

2.1 System components

The *SLC*-96 system consolidates message channels using time-division multiplexing and optional digital concentration for transmission over digital PCM links, which are standard T-carrier today and will include the more advanced lightwave systems tomorrow. The basic *SLC*-96 terminals are designed to operate between the central office and a remote location serving as many as 96 subscriber lines per system. They operate over four T1 lines and can automatically transfer to a fifth protection line to increase system availability. Three T1 lines are required when the system is concentrated or operating in a pure special services mode. The basic system components of the *SLC*-96 system are:

(*i*) COT equipment and associated apparatus located in the serving central office

(*ii*) RT equipment and apparatus located in the area to be served

(*iii*) Digital lines between the two terminals (in this article, however, digital lines are assumed to be standard T1 lines).

The primary element of the COT and RT equipment is the *SLC*-96 channel bank. The *SLC*-96 channel bank may be configured in three different operating modes: (*i*) a carrier-only mode, (*ii*) a carrier-concentrator mode, and (*iii*) a special services mode. Typical configurations illustrating these modes of operation are shown in Figs. 1, 2, and 3.

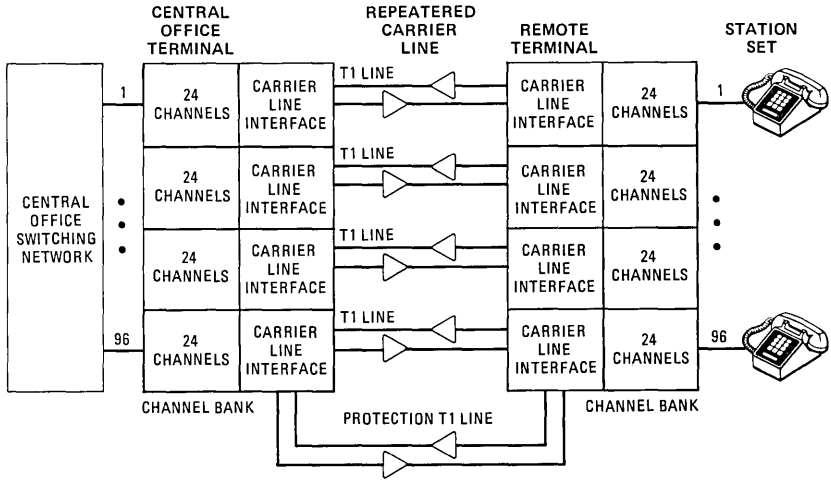

Fig. 1—The *SLC*-96 system—carrier-only configuration, Mode 1.

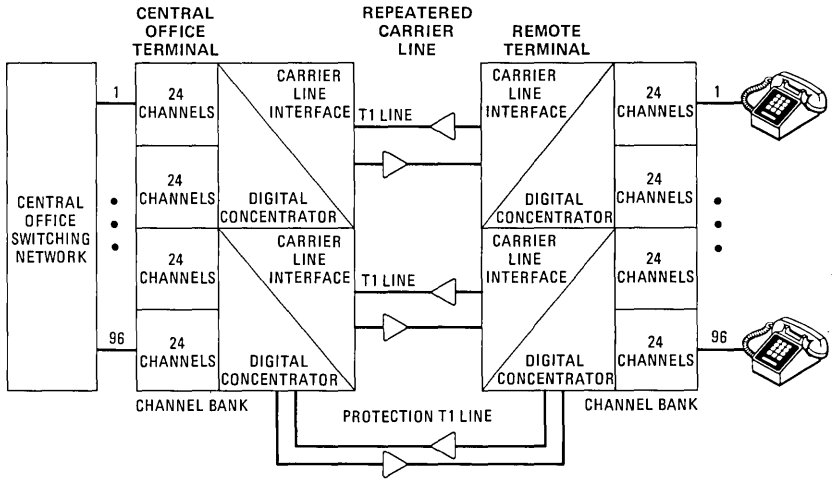

Fig. 2—The *SLC*-96 system—carrier concentrator configuration, Mode 2.

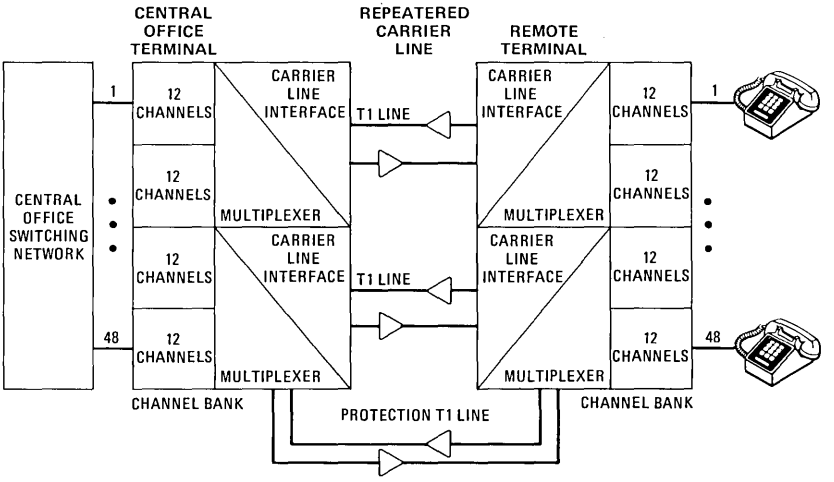

Fig. 3—The *SLC*-96 system—special services configuration, Mode 3.

Physically, the *SLC*-96 channel bank consists of four shelves, as shown in Fig. 4. Each shelf contains 12 slots for channel-unit plug-ins and four additional slots for common equipment. Each MTS channel unit contains two channels for each plug-in, while coin, special service, and dataport channel units contain one channel each. Therefore, each non-MTS channel unit displaces two MTS subscriber channels. Since non-MTS channel units are typically D4 channel units, the *SLC*-96 backplane arrangement is very similar to the D4 backplane. The physical size of the *SLC*-96 channel bank is identical to that of the 48-channel D4 channel bank.

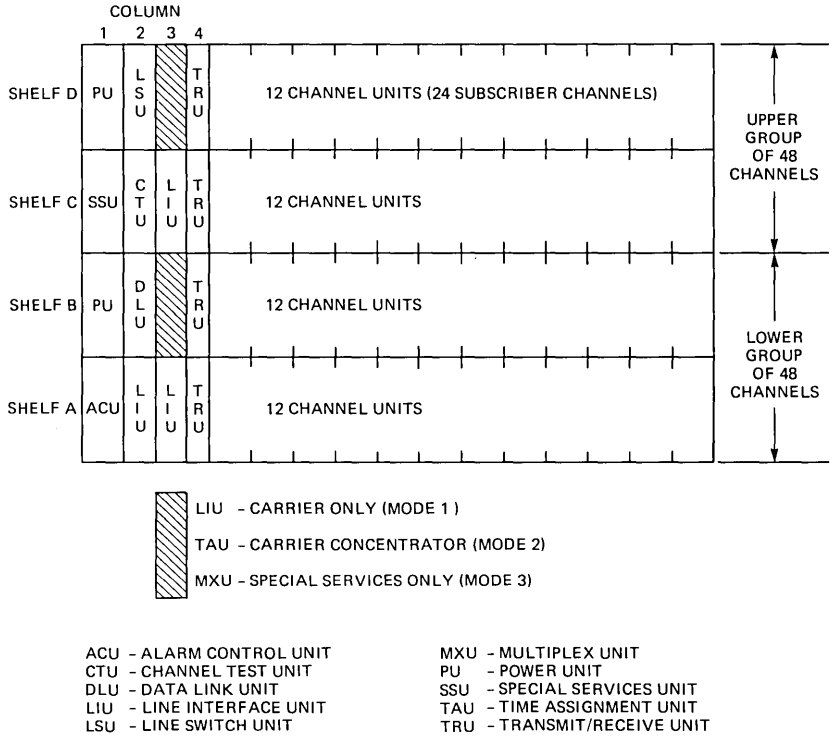

Fig. 4—The *SLC*-96 channel bank.

2.2 Operational modes

System operation is described in terms of modes of operation. Mode 1 is a pure carrier mode designed for high-traffic message telephone service and uses five T1 lines for each 96-line terminal. Mode 2 is a carrier-concentrator mode also intended for message telephone service; but it uses only three T1 lines for each terminal. This mode employs full access, two-to-one digital concentration with a capability for handling traffic sufficiently so that special loading rules are not required or used. A particular mode operates by selecting the proper common plug-in units. For Mode 2, the normal digital Line Interface Unit (LIU) is replaced by a digital concentrator plug-in called a Time Assignment Unit (TAU) using the identical physical slot in the channel bank. Mode 3 is called the special services mode, where the *SLC*-96 channel bank is loaded only with channel units designed initially for the D4 system and a new coin channel unit in the *SLC*-96 collection. It operates on three T1 lines and uses a plug-in called the Multiplex Unit, again in the same physical slot as the units mentioned previously.

III. UNIQUE LOOP CARRIER FEATURES

This section describes some of the features unique to the *SLC*-96 system. Although the *SLC*-96 system has the basic attributes of an interoffice trunk system, such as D4, it has certain special features required in the loop environment. The major differences between the *SLC*-96 and D4 systems are in T1 line powering and interface, maintenance, subscriber line concentration, and remote terminal arrangements. The operation and maintenance of a trunk-type D4 system and T-carrier lines are based on the assumption that the systems are located in central offices and that craftspeople are available at both locations. Since two craftspeople are assumed available, for example, only one alarm indicator for each transmission direction (red and yellow alarm) is required for system maintenance. While the *SLC*-96 COT is located in the central office, its corresponding RT is housed in a stand-alone cabinet, mini-hut, or other outside plant housing. This situation, unique to a loop carrier system, has resulted in a single-ended maintenance philosophy for the *SLC*-96 system, i.e., maintenance of the *SLC*-96 system at the COT location without first dispatching a craftperson to the RT. This is similar to the approach applied to trunk T1 systems operating in the out-state (T1/OS) environment.

Several unique features are built into the system. A T-carrier-protection switching system is integrated into the channel bank design, for which a Line Switching Unit (LSU) was developed. An Alarm Control Unit (ACU) is used to process and display various alarms originating from either the COT or RT. A Channel Test Unit (CTU) is required to allow testing of the channel units and the subscriber drop wires. An optional TAU has been developed to concentrate subscriber lines, thus saving T-carrier lines. A Data Link Unit (DLU) has been designed to provide data link circuits to handle system alarm, per-channel testing, T-carrier line switching, and concentration information between the COT and RT. Also, physical and economic constraints preclude the use of office repeater bays for the digital carrier at the COT and RT. This office repeater function has been integrated into the *SLC*-96 T1 LIU design.

The following sections will further illustrate these unique *SLC*-96 features in more detail.

3.1 T1 line interface, powering, and maintenance

3.1.1 Line interface and powering

The system constraint on available space and application of digital carrier in the loop plant required the integration of the digital line interface within the *SLC*-96 channel bank. Six unique LIUs have been designed to interface T1 carrier. The first four LIUs are used with pulp or polyethylene-insulated conductor (PIC)-insulated cable and the re-

maining two are designed for metropolitan-area trunk (MAT) or intercity and outstate trunk (ICOT) cables. The types of LIU circuit packs available and their distinguishing characteristics are:

(*i*) LIU-1 (rated A&M*)—Current regulator for low-power T1 repeater. It requires −48, ±130-volt office battery plants, dependent upon the T1-carrier span length.

(*ii*) LIU-2—Power looper for use at the RT.

(*iii*) LIU-3—Designed to interface with the office repeater or other digital systems; output level is standard DSX-1.

(*iv*) LIU-4—Similar to LIU-1 except that this unit contains a dc-to-dc converter and requires only −48-volts office battery to power the digital lines from the COT. It can be used at the RT for back powering to extend the span length.

(*v*) LIU-5—Similar to LIU-2 except that this unit is for MAT or ICOT cable.

(*vi*) LIU-6—LIU-4 version for MAT or ICOT cable.

The LIU functions as the interface between the channel bank unipolar PCM bit stream and the bipolar signal format of the T1 digital line, including the powering of a repeatered line span. This simple task grows in complexity as necessary features are added: bank clock generation, T1 line performance monitoring, status display of T1 line, and jack access for T1 line fault locate and power monitoring.

With respect to digital line powering, the repeaters in the *SLC*-96 digital line derive power from a constant current simplexed onto the carrier pairs from LIUs. Where the digital line is powered from the COT, 60-mA repeaters are required. Either 60-mA or 140-mA repeaters may be powered from an office repeater bay. Where the digital line exceeds the length that can be powered from the COT or central office CO repeater bay, additional powering spans are required. The additional powering may be provided by backpowering from the LIUs at the RT or by an intermediate remote-power-feed terminal. A remote-power-feed terminal can supply intermediate powering of long digital lines. This system option is required when the digital line power requirements exceed the range of powering from the CO (and possible extension from the RT). The remote-power-feed terminal uses *SLC*-96-type cabinets, a battery charger, and backup batteries; it also requires apparatus shelves housing constant-current dc-to-dc converters and power insertion transformers. This hardware is also suitable for frame mounting. The dc-to-dc converters operate from a nominal −48V dc and output a constant 60 mA at maximum voltages that may be optionally set at either −135 Vdc only, or ±135V.

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* Manufactured for additions and maintenance only.

3.1.2 Automatic protection line switch

Although most of the trunk T-carrier lines have at least one maintenance line between offices, the maintenance line is usually only available on a manual patch basis. This kind of T1 maintenance procedure requires the services of two craftspeople and violates the *SLC*-96 maintenance philosophy. The LSU directs automatic switching to the shared protection line in the event of a digital line failure. When the trouble is removed or disappears from the main line, the LSU will automatically cause the system to switch back to the main line. This frees the protection line for use in the event of any subsequent troubles.

When not directly in use, the protection line is continually powered and monitored and carries the same bit stream as the A-shelf main line. This powering and monitoring will detect a faulty protection line if it fails while not in direct use, activating an alarm. The LSU communicates with its far-end LSU using bits assigned to it in the data link.

3.1.3 Single-ended fault location

The LIU monitors the incoming T1 bit streams and requests T1 protection switch whenever a digital line trouble occurs. If a T1 line trouble persists, the failed line may be far-end looped via manual switches on the LIU. This allows single-ended testing of the failed T1 line. The T1 lines between the COT and RT are maintained and fault-locating tests are performed using the jack panel and fault locate and order wire panel located in the COT bay.

Fault-locating tests provide a method of locating faulty repeaters or cable sections that may be causing excessive errors on the system or total signal failure. In fault-locating, bipolar violations, inserted at a voice-frequency rate, must be applied to the line under test. The signal is regenerated within an operating line repeater and part of the output is applied to the fault-locate (FL) filter in each apparatus case. The filters extract and amplify the audio component for application to a common FL line via a narrow bandpass filter. The FL line is monitored at the central office by an FL test set for the presence of this return test tone. The absence or low level of the test tone indicates a faulty repeater.

Both active and passive fault locating is applicable to the *SLC*-96 system. The two types of fault locating both use twelve unique frequency assignments. With 1114-type active filters or with passive-fault locating, the FL tests can be performed in the transmit direction only. Therefore, FL tests will be made from the COT on side 1 of the line and from the RT on side 2 of the line. With 1115-type active fault-locate filters, both side 1 and side 2 can be tested from the COT; therefore, this type is termed single-ended fault-locating. Most T1 lines can be

configured for single-ended fault-locating. A signal source will not be required at the RT; however, the line must be looped from side 1 to side 2. This can be controlled from the COT LIU, thereby eliminating a visit to the RT.

3.2 Other maintenance

3.2.1 Alarms

The alarm system for the *SLC*-96 system is designed for two levels of alarm remoting. The first level must return remote terminal alarms to the central office terminal. This is accomplished using the *SLC*-96 data link. The second level must transmit all system alarms to a remote operations center, and the *SLC*-96 system provides such an interface capability. This is in line with a growing trend toward unattended or partially attended offices with surveillance and maintenance operations centralized for a given area.

Alarm reporting for the *SLC*-96 system begins with an Alarm Control Unit plug-in in the COT and RT channel banks. This unit processes and displays common equipment alarms and transmits alarm information to the corresponding unit at the other terminal bank over the *SLC*-96 data link. At the central office, the ACUs common to a single bay pass the alarm information to a fuse and alarm panel, where the alarms are made available to the office alarm system and to a remote telemetry interface by means of relay contact closures. The primary alarm categories are: major, indicating a customer service outage; minor, indicating a trouble that has not yet affected service; power minor, indicating loss of ac power at the remote terminal; and a COT fuse alarm. In addition, the fuse and alarm panel has several status indicators, which are: a carrier line failure; near-end, or far-end, status to aid in fault sectionalization; a system identifier; and other unique alarms from a remote terminal housing called miscellaneous alarms. The miscellaneous alarms may be used for door or smoke alarms and the like.

The *SLC*-96 system is also capable of accepting a pair of remote commands from the SCC through remote signal distributor points that aid in processing alarm reports received at the remote operations centers. The first is called Bank Loop Back, which is used to interrogate the near-end/far-end status indicators for certain classes of major alarm faults. The second is a remote alarm cutoff (ACO), which is used to retire all alarm indications with the exception of the system identifier. The system identifier can only be cleared when the alarm condition for a particular system is truly cleared. The remote ACO allows processing of subsequent alarms with less ambiguity because most alarms, with the exception of the system identifier and miscellaneous alarms, are paralleled to reduce the need for alarm distribution points.

The purpose of the *SLC*-96 alarm reporting system is to alert the proper repair forces to a trouble condition and indicate urgency and a degree of fault isolation, if possible. For example, for unattended offices it would be very desirable to remotely determine whether a *SLC*-96 trouble is in or out of the central office. The *SLC*-96 alarm and status indicators provide the information to dispatch the proper craft to the proper location for many common equipment problems. Detailed Task-Oriented Practices (TOPs) are available to further isolate a *SLC*-96 trouble. Once the repair forces have been dispatched, they can use the TOP practices, built-in *SLC*-96 trouble indicators, and applicable test sets to isolate the trouble to a specific circuit pack, repeater, or cable section.

The *SLC*-96 system continuously monitors performance characteristics involving groups of channels. For the *SLC*-96 system, service-affecting troubles involving twelve or more channels constitute a major alarm condition. Per-channel troubles are viewed as a minor alarm condition and are not alarmed in the *SLC*-96 system. A trouble report for one customer usually indicates that only a single subscriber line is in trouble. This trouble may be diagnosed directly from the Repair Service Bureau (RSB) using the *SLC*-96 loop testing method to be described in the next section.

3.2.2 Loop testing feature

The requirement to provide a capability of testing the customer loop from an RSB has become increasingly important with the growing penetration of digital pair gain systems in the loop plant. The *SLC*-96 system employs a new method of testing most customer loops terminating on the RT. The method requires a new item of central office equipment called the Pair Gain Test Controller (PGTC).[6] The PGTC, under microcomputer control and in combination with circuitry in the *SLC*-96 system itself, provides switching to connect incoming RSB test trunks to a dc bypass path around the carrier system to the distribution pair. In addition, the PGTC performs an automatic test of the appropriate transmission and signaling of the *SLC*-96-derived channel in parallel with testing of the customer loop from the RSB.

The capability just described is offered only on the new channel units designed exclusively for the *SLC*-96 system; they include the single-party, multi-party, and coin units. The trunk and special service channel units that are a part of the D4 family are not tested from the RSB; they also cannot be tested using the PGTC. Studies are under way to develop an appropriate test access method that would, in the future, allow special service channel units used on the *SLC*-96 system to be tested from the Switched Access Remote Testing System/Switched Maintenance Access System (SARTS/SMAS).

The PGTC is a microcomputer-controlled system that operates with a pair of common circuit packs in the *SLC*-96 channel bank called Channel Test Units (CTUS), one each for the COT and RT, and that requires subscriber channel units with a test access relay at the RT. Together with a dc test pair, called a dc bypass pair between the COT and RT, the collection of hardware listed above can establish a physical connection to permit dc testing of the customer loop. This new testing method

(*i*) Presents minimal changes to existing RSB test procedures

(*ii*) Is compatible with automated test systems such as mechanized loop testing (MLT)

(*iii*) Is able to accommodate all types and lengths of loops presently testable from an RSB

(*iv*) Performs transmission and signaling testing of the derived subscriber channel

(*v*) Requires minimal circuitry within the pair gain systems, particularly at the RT, where power and space is at a premium.

As Fig. 5 shows, the PGTC is installed in a wire center that is serving customer loops over *SLC*-96 systems. The PGTC switches office test trunks to dedicated test pairs, each of which may be shared by RTs grouped at a common location. It can test up to four channels simultaneously, provided that the channels are in different channel banks and that these channel banks do not share the same test pair. The incoming test trunks from the RSB are routed through the PGTC before they terminate on the central office switch. When the PGTC is inactive, the test trunks pass through unaltered and the PGTC is transparent to normal dialing and testing activities. The PGTC is activated only when attempting to test a customer loop served from a *SLC*-96 RT. Test access is obtained by first dialing the customer's number over one of the test trunks. This allows testing for continuity and leakage to the input of the COT channel unit. To set up the physical connection bypassing the carrier system, +116 Vdc is applied to the tip side of the test trunk. For example, at a local test desk, the reverse (REV) and positive station (+STA) keys are operated. The COT channel unit recognizes this signature and starts an elaborate interconnection sequence to cause cut-through of the test trunk directly to the customer loop at the RT. The testing facility may now perform normal testing procedures on the customers' loop via the test pair and test trunk. While these tests are in progress, the PGTC automatically checks the channel for transmission and signaling. When all testing is completed, the results of the automatic channel tests are returned to the testing facility by opening the sleeve lead of the test trunk (by operating the 3WO key). The PGTC maintains control of the sleeve lead to the central office switch to prevent the connection from being dropped during the

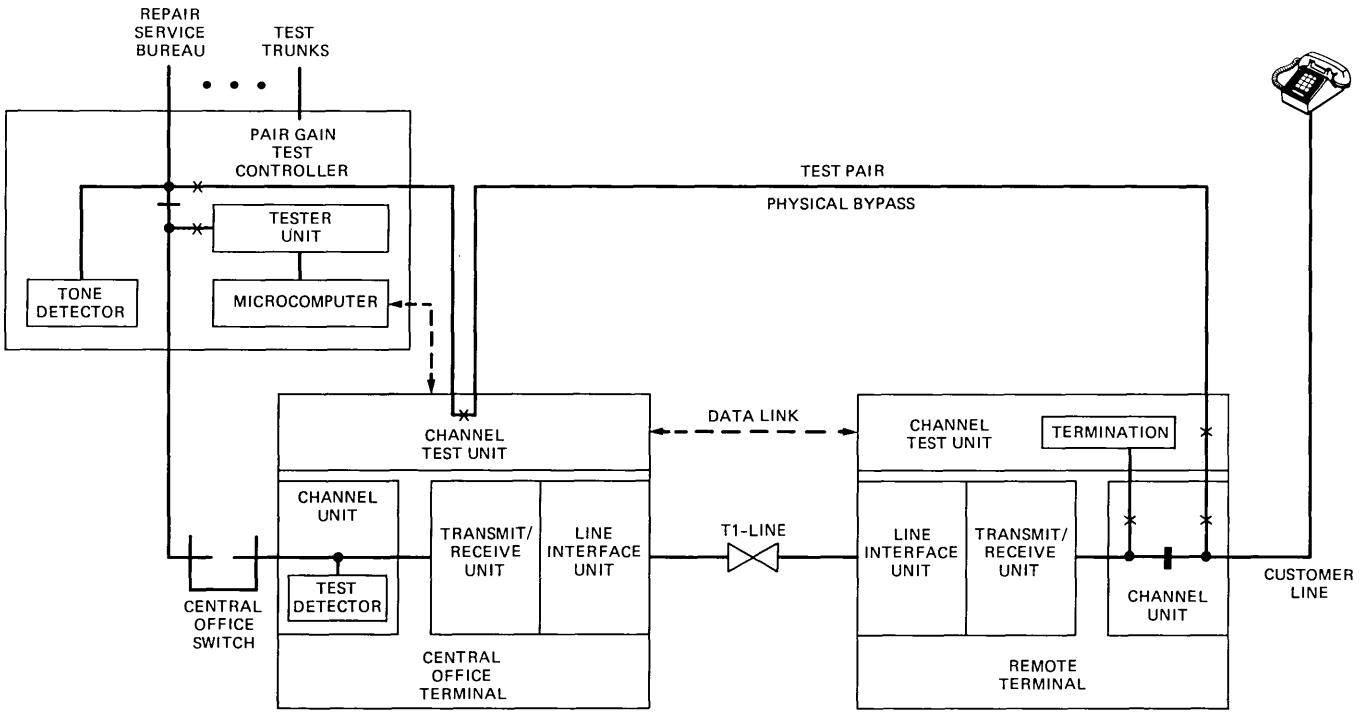

Fig. 5—Testing loops on the *SLC*-96 system.

testing interval. Results of testing are presented by audible tone bursts recognizable to a test person and by voltage levels that are more easily identified by an automated test facility such as MLT. Test results may be repeated as often as desired by closing and opening the sleeve lead.

The PGTC is a compact system consisting of a control shelf, which is always required, plus up to four expansion shelves, depending on the number of test trunks to be served. The control shelf holds the microcomputer, up to four independent tester units, and trunk cards sufficient to switch 12 test trunks. Each expansion shelf may accommodate 20 additional test trunks. The maximum system capacity is 92 test trunks. The interface between the PGTC and the *SLC*-96 systems is a bussed cable arrangement designed to handle any number of *SLC*-96 systems in the wire center.

3.3 Digital concentration

The Mode 2 system operation employs a 2-to-1 digital concentration between the central office and remote terminal to reduce the required number of T1 lines by 40 percent. Circuit packs called Time Assignment Units (TAUs) are used at both the COT and RT for each 48-channel group within the channel bank. The TAUs replace LIUs at either end of the system and require only one T1 line for each 48-channel group. The central office TAU, acting as the master controller, assigns an active channel to a specific time slot on the T1 line and transmits the assignments to the remote terminal TAU. That channel will keep its assigned time slot for the duration of the call. The concentration function is referred to as full access and any of the remaining channels may be assigned to any of the idle time slots until all time slots are active. The 2-to-1 concentration ratio requires no special traffic administration.

Figure 6 is a simplified block diagram of the concentration system operation. Each TAU circuit pack is realized with a pair of identical custom Time-Slot Interchanger (TSI) chips and a *Bellmac**-8 microcomputer. The microcomputers maintain control of channel/time-slot assignments and talk to each other over the *SLC*-96 data links. Off-hook and maintenance messages are also exchanged over the data links. The transmit TSI selectively combines two 1.544-Mb, serial PCM bit streams, one from each of the Transmit/Receive Units (TRUs) it serves. A TRU performs the analog/digital (A/D), digital/analog (D/A) and framing for 24 channels. The resulting T1 signal is sent to the receive TSI at the other end of the system, where it is expanded into two serial bit streams again.

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* *Bellmac* is a trademark of Western Electric.

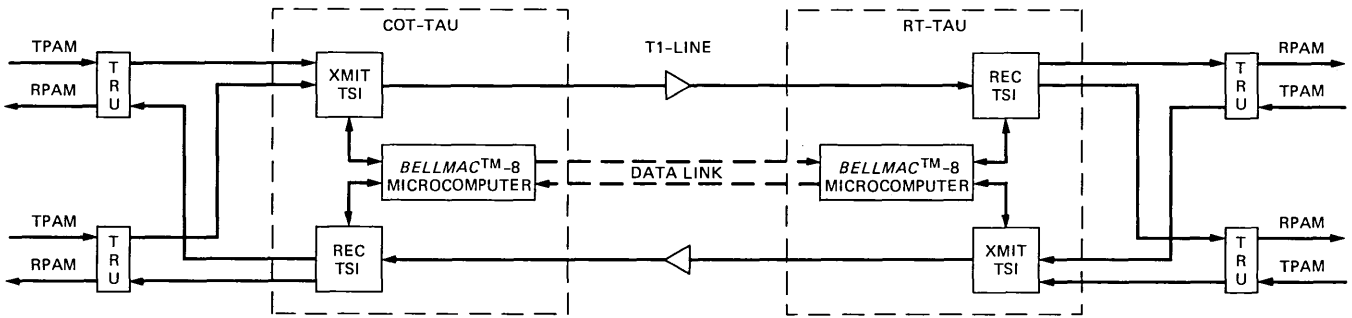


Fig. 6—Time Assignment Unit.

The need to establish a channel/time-slot assignment is initiated by detecting ringing at the COT channel unit or by detecting off-hook at the RT channel unit. This activity, as it is called, is detected by the TAU by monitoring the A and B signaling bits from each of the channels. Activity is stored in the TSI memory from which the microcomputer can retrieve it and establish the necessary channel/time slot-assignments. Activity at the RT is passed over the data link to the COT where channel/time-slot assignments are established.

Mode 2 operation was designed primarily for general message telephone service. The 2-to-1, full-access concentration ratio provides for a traffic-handling capability sufficient to allow full or block loading of a 48-channel group with dual single-party channel units. The concentration ratio is conservative enough to include a limited number of multi-party and/or nonconcentrated (nailed-up) special service (SS) or coin units. The maximum of eight special service or coin units is allowed for each 48-channel group. (For multi-party units the maximum number is sixteen channels for each 48-channel group.) The special service and coin units are single-channel plug-in units. Each of these units that is used in a physical slot in the *SLC*-96 channel bank reduces the number of lines to be concentrated by two. Only one time slot is nailed up and the concentration ratio remains fixed at 2-to-1. The trunk group size is reduced for each nailed-up channel unit added, which slightly decreases the traffic carried by the concentrated portion of a 48-channel group. The traffic carried by the concentrated portion of a group at 0.5-percent probability of blocking and 25-percent intrasystem traffic is presented in Table I. As we can see, Mode 2 operation of the *SLC*-96 system is significant in its traffic-carrying capability, thereby exempting the system from initial loading restrictions.

The central office TAU is designed with several traffic monitoring features. A traffic overload alarm occurs if there have been two or more blocked calls for two out of three weeks running. This activity corresponds to a weekly peak busy hour traffic in excess of nine ccs per concentrated line. This alarm may be used to initiate traffic monitoring to determine whether a two-shelf group should be deloaded. It is expected that the traffic overload alarm will occur only on rare occasions. The central office TAU contains a two-digit display that displays, upon demand, the peak traffic in ccs per concentrated line

Table I—Traffic carried at $P(B) = 0.005$ on the *SLC*-96 system versus number of lines

Number of MTS lines	48	44	40	36	32
Number of SS lines	0	2	4	6	8
Carried MTS load (ccs/line*)	12.02	11.73	11.40	11.02	10.60

* Hundred call seconds (ccs) per line.

and the cumulative number of blocked calls since the internal registers that store these numbers were last cleared. The traffic overload alarm and the internal registers, cited above, may only be cleared manually, by means of pin-jack switches on the front face of the central office TAU. The above displays are remotely monitored by traffic usage recorders using pulsed relay contact closures.

For the blocked call situation, where all time slots are in use, the central office TAU first trips ringing without billing by momentarily operating the channel unit off-hook relay and then provides a digitally generated overflow tone to the central office line-terminating equipment. This tone is provided for approximately 6 to 9 seconds and is used in all electromechanical offices. The electronic switching system (ESS) machines handle overflow in a different manner and use a pair of wires from the TAU to convey the blocked calls state via a relay contact closure. This signal is input to the ESS machines by master scanner applique circuits. For calls originating at the RT, dial tone is delayed until a time slot becomes available; however, there is no overflow indication.

3.4 Data link

The *SLC*-96 system contains several features that require slow-speed data links between the terminal ends. Two 2.2-kb/s data links between COT and RT carry data related to alarm remoting, channel testing, T1 automatic line switching, and concentration of the subscriber lines. The second data link carries data related to the concentrator function for the second 48-channel group in the channel bank. The data link is created by stealing some of redundant PCM bit stream framing bits. The frame organization of the *SLC*-96 system is identical to that of D4 with the 193rd bit in a frame used in a repetitive sequence for two types of framing: terminal and signal frames. The terminal frames at a 4-kb/s rate to synchronize the incoming signal on the individual 193-bit sequences. The signaling framing has a "111000" pattern transmitted during even frames at the 4-kb/s rate to identify 6th and 12th signaling frames. Once the signaling frames have been identified, the "111000" pattern becomes redundant. By time-sharing these bits with other information, a low-speed data channel can be created. Figure 7 shows the signaling frame patterns of D4 and the *SLC*-96 system. Notice that the *SLC*-96 system "111000111000" pattern is used to identify the signaling frames and succeeding data bits. Spoiler bits are used so that the data bits cannot simulate the "111000111000" signaling frame pattern. There are four data fields, including concentrator, channel test, alarm control, and line switch for which effective data rates are 1.2 kb/s, 0.33 kb/s, 0.22 kb/s, and 0.44

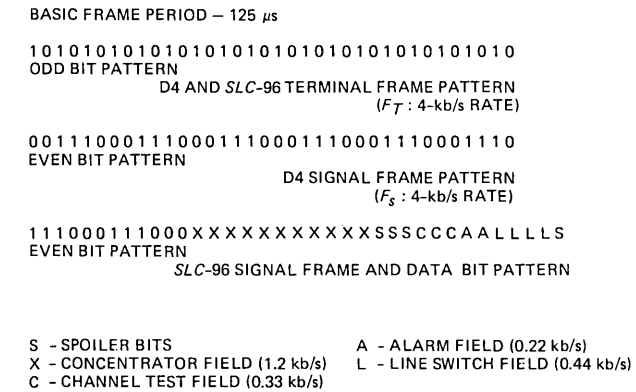


Fig. 7—Bit 193—frame pattern.

kb/s, respectively. The Data Link Unit (DLU), interacting with various units in the *SLC*-96 channel bank, provides the above functions.

3.5 Remote terminal battery plant

The *SLC*-96 RT is powered by a new, compact design battery plant that allows the terminal to operate for a minimum of eight hours during loss of commercial ac power. The battery plant employs rechargeable, sealed, lead-acid batteries as its backup source. The lead-acid system used is unique in that each cell in a battery string is truly sealed and utilizes gas recombination for long, maintenance-free operation.

The use of sealed cells eliminates the need for periodic battery maintenance by greatly minimizing problems caused by corrosion of battery posts; of course, battery watering is not required. The sealed cell also has a safety advantage in that it eliminates the possibility of damage or accidents that might previously have been attributed to electrolyte spillage when using the older flooded cells.

The battery reserve capability for a single *SLC*-96 remote terminal is implemented by connecting four KS-21906, List 4 battery packs in series to form a nominal 48-volt string. Each battery pack supplies a nominal 12 volts and is connectorized for plugging directly into a battery shelf. The connectorized battery pack, in addition to being easy to install, also is necessary for safety reasons to guard against shorting. The sealed, lead-acid battery pack exhibits very low internal impedance, which permits very high current to flow, if short circuited.

The capacity of the battery string is 25 Ah at room temperature of 25°C and at discharge rates of less than 2.5 amperes. As with most battery systems, the capacity per cycle is directly related to temperature and inversely related to the discharge rate. For the *SLC*-96

application, loss of capacity due to high discharge rates is not an issue because the long-term average drain per 96-channel system is less than 2.5A. Temperature variation, however, is another matter. All RT enclosures designed for the *SLC*-96 systems are suitable for use in outdoor environments ranging in temperature from −40° to 50°C. The battery shelves used in the *SLC*-96 RT are equipped with heaters designed to keep the batteries above −4°C in outside ambients down to −40°C. In the event of an ac power failure during the winter months, a fully charged battery string should have at least 20 Ah of capacity, which is sufficient to maintain normal equipment operation for eight hours. When the batteries are warm, battery capacity is not an issue since a fully charged string will exceed 100 percent of its nominal 25°C capacity. However, battery life is an inverse exponential function of temperature above 25°C. The KS-21906 cell has an expected life of five years when used in Bell System float-standby applications. Battery life calculations using U. S. Weather Bureau data, accounting for both mean daily high and low temperatures throughout the year in several regions of the United States, support the above-expected life. The batteries have been designed for and have been tested to operate in ambient temperatures as cold as −40°C and as warm as 65°C.

The *SLC*-96 battery plant is designed to be miscellaneously mounted in standard 23-inch frames as shown in Fig. 8. A typical arrangement consists of front-mounting a 3A battery charger along with up to two battery shelves designated 128A apparatus mountings. The battery charger, shelves, and battery packs are connectorized for easy installation. The battery charger requires 7 inches of vertical mounting space and each battery shelf requires 8 inches, for a total of 23 inches of mounting space. When the battery plant is mounted at the bottom of a 7-foot frame, there is space available to house two complete *SLC*-96 RTs including support items (ringing generators, power distribution fusing, jack panel). To conserve floor space, the battery plant requires front access only.

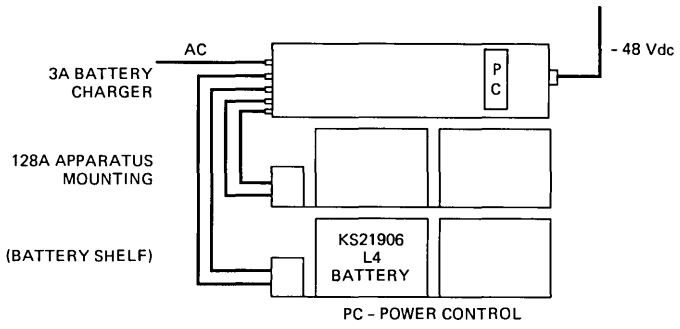


Fig. 8—The battery plant.

The 3A battery charger has been designed to power up to two *SLC*-96 RTs and can also charge up to two 25 Ah battery strings. The battery plant is a 48 Vdc plant with an 8.5A capacity and a total battery reserve of 50 Ah. The rectifier circuit in the battery charger provides two dc outputs. The primary output is 48 Vdc signal grade with 8.5A capacity to power the load; the secondary output is 64 Vdc with a 2.5A capacity to supply the battery charging circuits. The battery charger is a dual rate charger designed to return full capacity to one or two battery strings in 24 hours using a high-rate charge. It then retains this capacity indefinitely by means of a low-rate or float charge. The rectifier uses the principle of controlled ferromagnetic resonance of a transformer to achieve regulation.

IV. PHYSICAL DESIGN AND ENCLOSURES

The general physical design used for the channel bank and associated plug-in units is covered in detail in a companion D4 physical design article.[7] However, some additional requirements that pertain to central office arrangements and remote terminal mounting will be covered here.

4.1 COT physical arrangement

COT equipment consists of a channel bank assembly, fuse and alarm panel, jack panel, and an optional T1 fault locate and order wire panel.

Figure 9 illustrates typical full-bay configurations that are possible for 7-foot, 9-foot, and 11-foot 6-inch bays. These illustrate the maximum number of channel bank assemblies that can be installed in an unequal flange bay.

4.2 RT physical arrangement

The individual remote terminal equipment designs (channel bank, battery charger, etc.) are each configured to be front-mounted to a standard 23-inch frame format. As we stated earlier, all equipment assemblies designed for RT mounting are fully connectorized to make the field installation process faster, easier, and less prone to error. In addition, these connectorized assemblies make possible very rapid removal and replacement if needed.

4.3 Enclosures

One of the primary goals in designing the *SLC*-96 system has been to enable the mounting of electronics of widely varying line sizes (from 100 to approximately 4000 lines) in different environments. This applies to outdoor mountings such as cabinets, buildings, and underground structures, as well as inside mounting in customer-owned facilities.

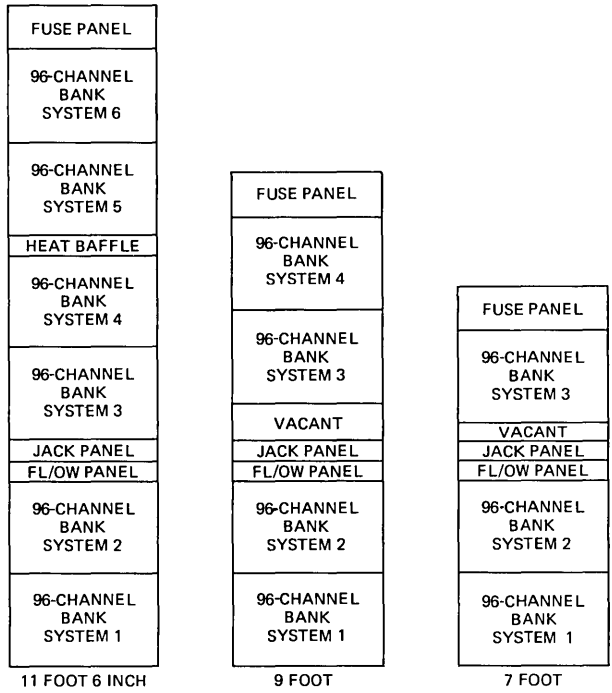


Fig. 9—Typical COT full-bay configuration for 7-foot, 9-foot, and 11-foot 6-inch frames.

There are three different outdoor cabinet designs, including a suburban cabinet, a rural cabinet, and a sign board cabinet. All three are illustrated in Fig. 10.

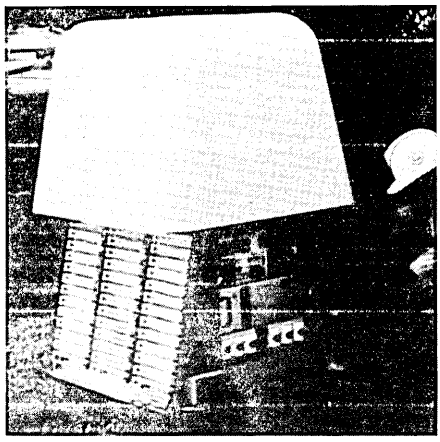
4.3.1 Suburban cabinet

The AT8908 M cabinet shown in Fig. 10 has been designed for suburban applications where appearance and site compactness are of prime importance.

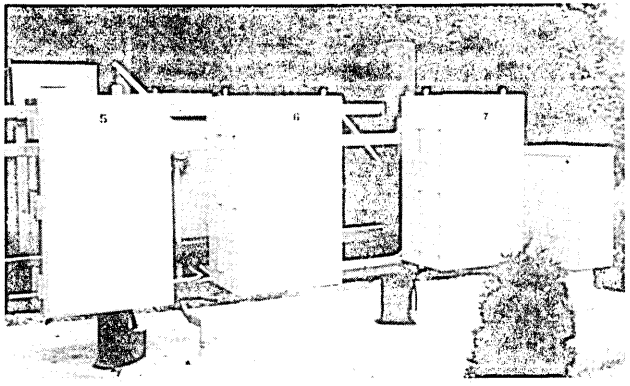
Remote terminal apparatus consists of the cabinet, one connectorized *SLC*-96 RT bank, plug-in circuit packs, connectorized power shelves, and a connectorized battery shelf and packs. With the addition of an optional frame mounting, an interconnection field may be added to the fourth side of the cabinet (required to cross-connect subscriber pairs to feeder pairs from the serving central office). The RT site may be enhanced by placing the interface inside the RT cabinet. This reduces the site size and eliminates the tombstone effect of multiple cabinets.

4.3.2 Rural cabinet

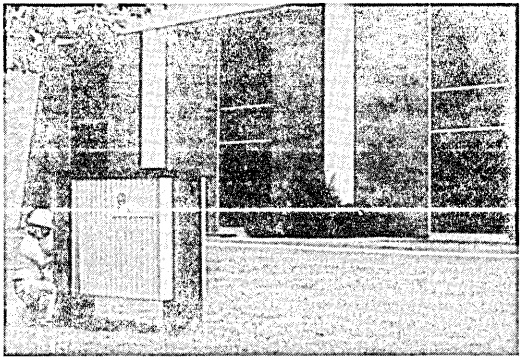
The rural (36-type) cabinet can mount one 96-channel system and has a weatherproof housing with framework very similar to the cabinet



M CABINET–1 SYSTEM



36 CABINET–1 SYSTEM



80 CABINET–2 SYSTEMS

Fig. 10—*SLC*-96 remote terminal cabinets.

used for the predecessor of the *SLC*-96 system. The *SLC*-40 cabinet was described in a previous article.[8] This cabinet is intended for areas where site appearance is relatively unimportant, and it requires that a separate interface cabinet be used.

The mounting hardware is identical to that used for the *SLC*-40 cabinets, so the newer *SLC*-96 cabinet can be mounted on poles or pedestals previously prepared for *SLC*-40 installations.

4.3.3 Community service (sign board) cabinet—80 type

This cabinet is essentially a sheet metal structure configured to resemble a sign board. The cabinet will house two *SLC*-96 systems and a large-capacity interface field. The housing is intended for applications where right of way or similar considerations preclude the use of other housings. This cabinet is a new design which has recently been introduced.

4.4 Small equipment buildings

4.4.1 Mini-hut

When several remote terminals are required at a single location, and land can be obtained, a hut can achieve savings over multiple-cabinet installations. Also, as we see in Fig. 11, the mini-hut makes it easier to provide an aesthetically designed installation than can be achieved with multiple collocated cabinets.

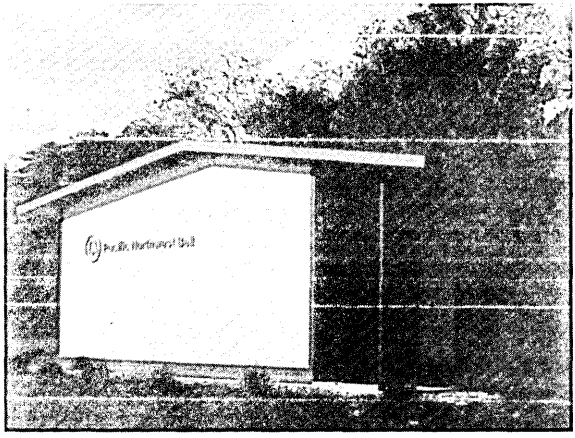
The *SLC*-96 mini-hut is approximately 6 feet by 10 feet by 8 feet high and is designed to accommodate ten *SLC*-96 systems. For hut-mounted applications the *SLC*-96 RT equipment is mounted on standard 7-foot equipment frames with two complete 96-channel systems and ancillary power equipment for each frame. Thus, five frames are used in a 10-system mini-hut.

To conserve floor space (and thereby enhance appearance and decrease costs) the *SLC*-96 equipment requires front access only. Rear access to the channel banks can be obtained by mean of an access shelf. The access shelf is a sheet metal design that allows the channel bank to be removed from the framework, slid out from the frame, and pivoted for rear access.

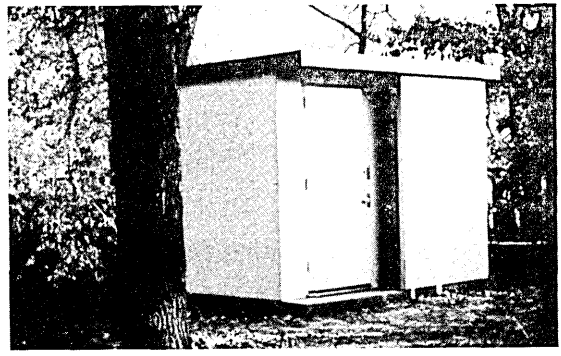
The mini-hut is usually ordered equipped with frames, shelves, cross-connect field, and inside cabling. Western Electric assembles this arrangement and ships the fully equipped hut, without plug-ins, to the RT site.

4.4.2 Electronic equipment enclosure

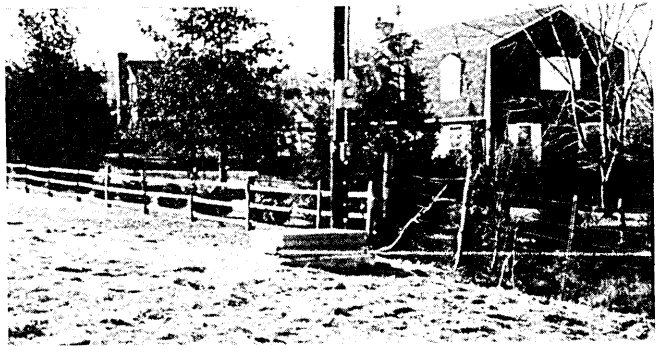
Another small building design is available for applications requiring more than 10 collocated systems. This is the electronic equipment enclosure (EEE), which has about a 10- by 20-foot floor area and can



EEE-40 SYSTEMS



MINI-HUT-10 SYSTEMS



CEV-20 SYSTEMS

Fig. 11—*SLC*-96 remote terminal enclosures.

be equipped with up to forty 96-channel systems on 20 7-foot frames (see Fig. 11).

The EEE (and mini-hut) appearance was developed in conjunction with an industrial design firm, Henry Dreyfuss Associates, to provide an appearance that is judged to be acceptable by most community standards. The cost of the standardized, prefabricated EEE can be expected to be lower than a conventionally constructed Bell System building of comparable size and quality. In addition, the installation interval is drastically reduced over that for conventional construction.

4.5 Controlled environment vault

Above-ground structures, both cabinets and huts, are appropriate choices for RT housing in areas where suitable sites can be found and land can be obtained. However, such sites become increasingly less prevalent as the RTs get closer to the serving central office (and hence into increasingly populated areas). In some sections of this country, such as large parts of the Northeastern United States, it is extremely difficult to find suitable above-ground sites. The Controlled Environment Vault (CEV) has been designed for such applications and is economically very attractive when land costs become appreciable.

The CEV design for *SLC*-96 systems is a 6-foot wide, 16-foot long, 9-foot high, two-piece precast concrete structure with environmental controls and alarms and a palletized *SLC*-96 equipment arrangement. The structure can accommodate ten 7-foot *SLC*-96 racks, or 20 systems, as illustrated in Fig. 12.

4.6 Customer premises arrangements

SLC-96 systems can often be very effective for serving large, single-customer needs, or for other applications where the equipment can most easily be placed indoors on the customer's premises. For these applications, the *SLC*-96 RT equipment is most often mounted on 7-foot racks, as for the previously mentioned large outdoor structures, and placed in telephone equipment rooms. These rooms are areas on a customer's premises where access is limited to telephone personnel only. Such space may already exist in some buildings, while in others, leasing, etc., arrangements may be required.

A future Bell System Technical Journal article is planned to cover the physical design of the *SLC*-96 system in greater detail.

V. SUMMARY

The *SLC*-96 system is fulfilling its traditional role in the loop plant, where it is used as an alternative to capital expenditures for new cable, new structure, or new central offices to provide growth of general message telephone service. In addition, the *SLC*-96 system has the

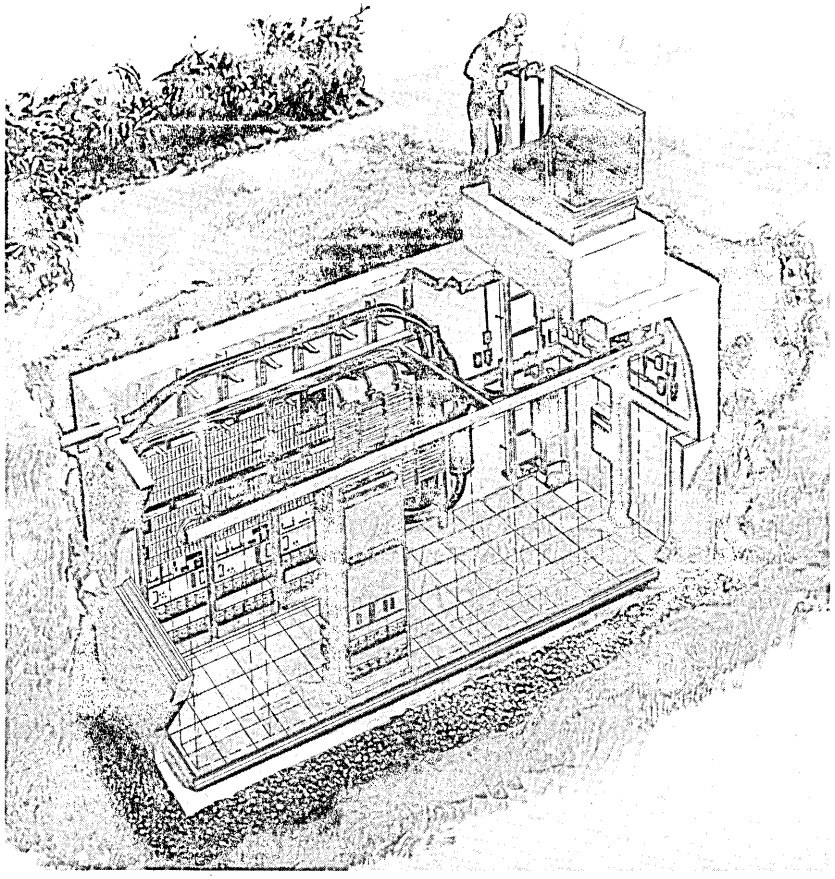


Fig. 12—The Controlled Environment Vault.

versatility to offer services in a variety of new applications, especially involving services to business customers. Digital loop carrier will become even more attractive as digital switching becomes more predominant for both local central offices and private branch exchanges (PBXs). The *SLC*-96 system design approach was based on the D4 system architecture. This approach was chosen to widen the range of application of a digital loop carrier in the Bell System in a timely and cost-effective manner. The capability of the *SLC*-96 system has combined, in one system, many of the attributes of an interoffice trunk system with the unique requirements of a loop carrier system.

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D4 Digital Channel Bank Family:

Dataport—Digital Access Through D4

By T. J. APRILLE, S. NARAYANAN, P. G. ST. AMAND, and F. E. WEBER

(Manuscript received July 10, 1981)

Digital carrier transmission, first introduced into the Bell System in the early 1960s, now offers a nationwide network of digital facilities. A portion of this interoffice digital capability, the Digital Data System (DDS), provides high-quality data channels to support Dataphone* *Digital Service. A new series of D4 channel units, called dataport channel units, has been developed to exploit the potential of the in-plant digital facilities more fully. Dataport channel units are unique in that they allow digital signal access, at rates up to 64 kb/s, to digital T-carrier repeatered lines. This article describes the dataport concept, its capabilities, and its applications in providing ubiquitous access for the Digital Data System. Companion articles in this issue describe in detail dataport designs and the channel encoding techniques used to ensure high-quality service in the existing T-carrier digital transmission plant.*

I. INTRODUCTION

Today the Bell System T-carrier network has digital transmission facilities that serve most major cities in the United States. Since its introduction in 1962 this network has grown to include more than 400,000 channel banks and 80,000,000 channel miles of T-carrier repeatered lines. Digital facilities have enabled each new equipment generation to offer smaller size, less power dissipation, and more features.

* Service mark of AT&T.

To date these digital facilities have been used almost exclusively for voice-frequency (VF) channels. In general, data communication over these facilities is achieved with voiceband data modems that employ digital-to-analog (D/A) conversions to utilize the VF channels. Such analog techniques allow data rates of up to 9.6 kb/s over private line connections, but do not allow the full potential of the 64-kb/s T-carrier channel to be utilized. Moreover, the voiceband data terminals employ relatively complex modulation and detection schemes and essentially duplicate the analog-to-digital (A/D) processes performed by the D-channel banks.

There is a rapidly growing demand in the telecommunications industry to support high-speed digital data services. The Bell System, recognizing the inherent efficiencies in providing digital connectivity to serve the data communications market, began deploying the Digital Data System in 1974. By incorporating a family of dedicated data multiplexers (e.g., T1DM, T1WB4/5, SRDM) interconnected by digital facilities, the DDS eliminated the analog interface and the costly A/D hardware from data connections. Although these conventional DDS arrangements use T-carrier lines to interconnect the data banks, the potential digital connectivity of the vast D-bank/T-carrier network has essentially remained untapped. The dataport channel units uniquely allow direct digital access to channels in the D4 bank. Equipped with dataports, every D4-bank/T-carrier facility can be considered a potential extension of the DDS. By avoiding A/D conversions, each D4-bank/T-carrier channel can accommodate the *Dataphone* Digital Service rates of 2.4, 4.8, 9.6, or 56 kb/s. The dataport capability thus permits efficient voice/data sharing of the D4-bank/T-carrier facilities.

II. DDS BACKGROUND

The dataport channel unit provides a digital signal interface with the extensive D-bank/T-carrier network. Although a variety of new digital services will likely result from this development, the initial application uses the dataport channel to extend the serving areas of the DDS. To better understand this application, a brief review of DDS is given here. A detailed description of the DDS may be found in a recent issue of the *Journal*.[1]

The DDS is a full duplex, private line network designed for point-to-point and multipoint digital data transmission at synchronous rates of 2.4, 4.8, 9.6, and 56 kb/s.[2] (The quantities 2.4, 4.8, and 9.6 kb/s are referred to as "subrates.") In *Dataphone* Digital Service, a typical point-to-point DDS channel interconnects two customer stations in different digital serving areas (DSAs), as shown in Fig. 1. The connection consists of three basic network elements:

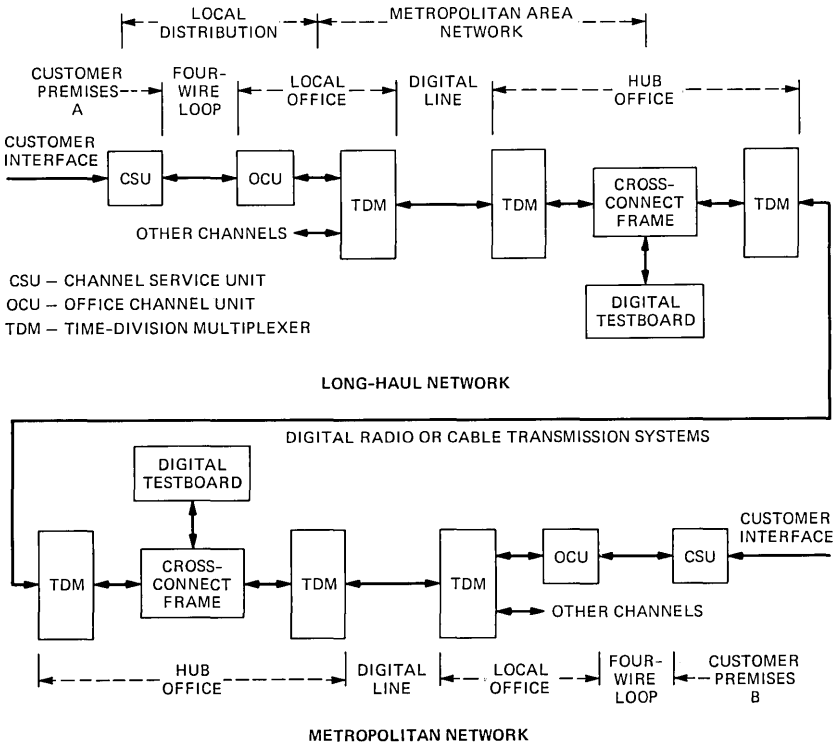


Fig. 1—Point-to-point DDS connection.

(*i*) A local distribution system using four-wire metallic facilities to connect the customer premises and serving central office

(*ii*) A metropolitan network of T-carrier digital lines terminated in time-division multiplexers for collecting customer channels from a number of central offices into a hub that serves as the testing and administrative center

(*iii*) The intercity network of long-haul digital transmission facilities.

2.1 DDS network elements

The local distribution portion of a DDS connection uses metallic, twisted-pair cables for the full-duplex four-wire transmission path between the customer premises and the serving DDS office. A Channel Service Unit (CSU),* furnished as an integral part of a DDS channel,

* A Data Service Unit (DSU) available at customer option provides the following additional features: timing recover, signal encoding and decoding, and EIA standard RS-232C type D or E interfaces for subrates, or a CCITT V.35 interface for 56 kb/s.

serves to terminate the four-wire loop at the customer premises.[3] The CSU is a well defined interface for connecting the customer terminal equipment; it incorporates circuitry to permit signal loopback from a DDS test center.

The digital signal on the four-wire loop is transmitted and received in a bipolar format (50-percent duty cycle, return-to-zero format). This signal has a symbol rate equal to the data rate and uses bipolar violation patterns to encode test and supervisory control information in the bit stream. At the DDS serving office the loop is terminated with an office channel unit (OCU). The OCU encodes the incoming data signals into an 8-bit byte format that adds necessary control information and, regardless of the data service rate, builds the signal up to a rate of 64 kb/s. For example, in the case of a 2.4-kb/s subrate data signal, the OCU adds two bits to each block of six customer data bits to form an 8-bit byte and repeats the byte 20 times in succession (byte stuffing). This procedure is repeated 400 times in a second to achieve the 64-kb/s rate. For the 56-kb/s data rate the OCU merely inserts a control bit after each block of seven customer data bits. This process yields the 64-kb/s signal illustrated in the last two diagrams of Fig. 2. The resulting 64-kb/s signal is defined as the digital signal zero (DS0) level of the digital hierarchy and is used as the standard for interconnecting DDS transmission equipment.

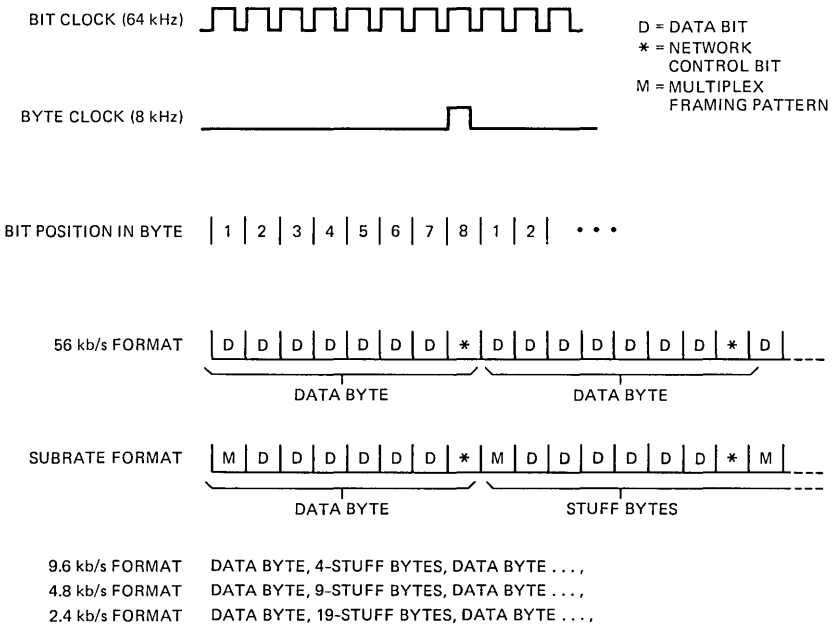


Fig. 2—DS0 signal format.

Individual DS0 signals in the same serving office may then be combined into a 1.544-Mb/s signal by a time-division multiplexer (e.g., T1WB4/5) for transmission over a digital line to a hub office. The hub office acts as a collection point for channels coming from numerous serving offices in a metropolitan area. In the hub office, baseband DS0 channels are recombined with other channels destined for the same distant DSA. These efficiently packaged high-speed signals are transmitted via the long-haul intercity network composed of cable and radio systems. At the destination DSA, the individual channels are again separated for distribution through the metropolitan area network to the terminating stations via the local loop plant.

2.2 Performance objectives

The DDS has been designed to provide high-quality digital signal transmission.[4] The error performance objective is error-free transmission in 99.5 percent of all one-second intervals. Availability, a measure of dependability, is equal to the complement of the average annual down time. The objective is to meet an average availability of at least 99.96 percent.

The major techniques used to meet these objectives include automatic protection switching of digital facilities, centralized and remotely controlled fault isolation, pre-service facility qualification testing, and continuous in-service signal monitoring of digital signal one (DS1) (1.544 Mb/s) facilities.

2.3 Synchronization

The synchronous timing structure of the DDS network is in the form of a master-slave tree ultimately synchronized to the reference frequency standard at Hillsboro, Missouri.[5] The hierarchy of the timing supplies in rank ordering are the master timing supply (at the St. Louis Regional Hub), the nodal timing supply (NTS), the secondary timing supply (STS), the local timing supply (LTS), and T1WB4/5 integrated timing supply (ITS). This ordering reflects relative ability to ensure slip-free operation during loss of input synchronization and to drive other output DDS equipments. In this network, timing supplies are slaved via DS1 facilities to other supplies that are higher or equally positioned in the hierarchy but never to a supply that is lower in the hierarchy. Integrating D4 bank dataport circuits into this network requires a mechanism for the appropriate timing interface.

2.4. Testing and maintenance

Reliability and maintainability of the DDS are important for ensuring that the performance objectives of *Dataphone* Digital Service will be met. The DDS maintenance philosophy is based on the concepts of

single point of contact for customers, centralized administration and restoration control, remotely controlled sectionalization of troubles, and automatic protection switching.[6]

At the DS1 levels the maintenance capability includes performance monitoring and protection switching of T-carrier lines and terminal equipment. Further, on-line monitoring of intercity DS1 transmission facilities is being implemented in the network by means of the Digital Transmission Surveillance System.[7]

At the DS0 and lower rates, equipment is made modular on a customer-circuit basis so that a failure usually affects only one customer. Circuit troubles are sectionalized by a series of remotely controlled loopbacks at OCU and customer-premises station equipment.

III. DATAPORT CAPABILITY

The initial hardware configuration for DDS is ideally suited for central offices that serve many data customers. This equipment, therefore, has been deployed primarily in metropolitan areas. The dataport concept complements the existing arrangements by offering low-cost implementation in low-demand serving offices. The fundamental guideline in dataport designs has been to provide data channels that are interchangeable with those of the existing DDS network.
This requires that dataport channels be:

(*i*) Integrable into the DDS synchronization network

(*ii*) Transparent in performance to the end user in terms of error rate, availability, and transmission delay

(*iii*) Consistent with DDS maintenance

(*iv*) Interface-compatible with existing DDS equipment

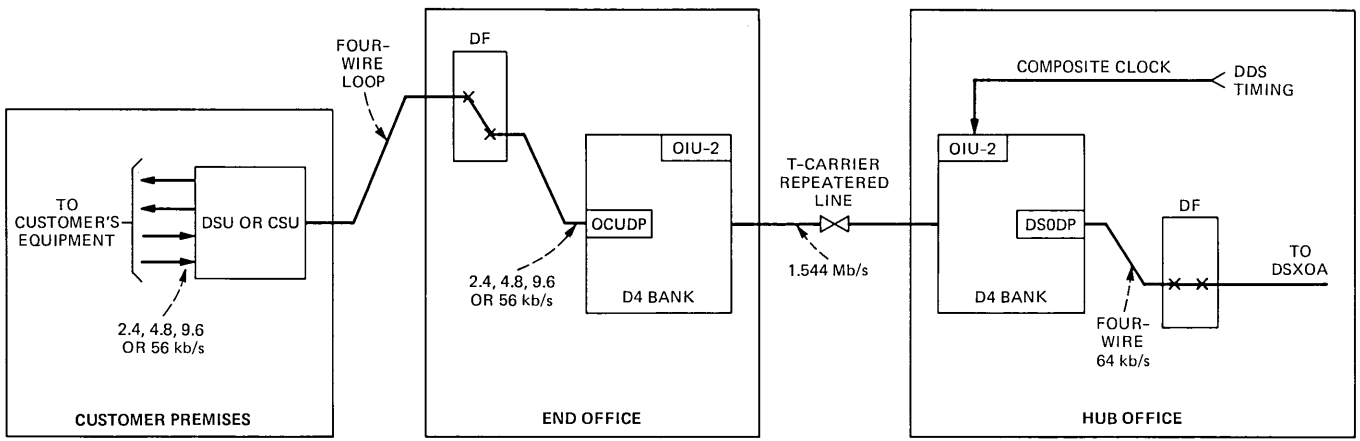
(*v*) Format- and protocol-compatible in a DDS connection.

The following sections describe the dataport applications and discuss the hardware designs that meet these performance requirements.

3.1 The standard application of dataport

Dataport channel units allow digital signal access to the T1, T1C, and T2 digital lines via the D4 banks.[8] Figure 3 shows a typical application of dataports in extending a DSA. In this arrangement a D4 channel acts as a DDS circuit between hub and end offices. At the end office the DDS connection to a DSU or CSU at the customer location is made via the local cable distribution network.

The hub office D4 bank uses a DS0-level dataport channel unit that can be inserted in any of the channel positions. This dataport provides the interface between the DDS 64-kb/s system rate on the drop side and the T1 line rate on the line side of the bank. Drop-side wiring consists of the existing D-bank connection to the distribution frame



CSU – CHANNEL SERVICE UNIT
DSU – DATA SERVICE UNIT
DDS – DIGITAL DATA SYSTEM
DF – DISTRIBUTION FRAME
DSODP – DSO DATAPORT
OCUDP – OCU DATAPORT
OIU – OFFICE INTERFACE UNIT
DSXOA – DSO CROSS CONNECT A

Fig. 3—Standard dataport application.

(DF) and, from there, an installed connection to the DDS entry point (the DSX0 bay).

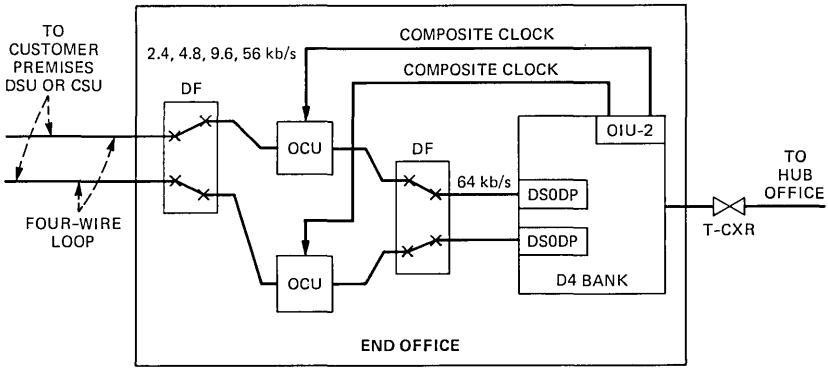
The associated channel slot in the end office D4 bank is equipped with an OCU dataport. This dataport provides an interface between a customer rate of 2.4, 4.8, 9.6, or 56-kb/s and the 1.544-Mb/s DS1 line rate. Again, existing wiring between the D bank and the DF is used; the final connection to the customer-premises DSU or CSU is made with existing loop plant facilities.

Dataport channel units obtain their timing from common circuitry in the D bank. Since DDS is synchronous, this common circuitry must be synchronized to the DDS reference clock. Timing is derived and distributed to the dataports by a new D4 common unit, the office interface unit (OIU). (The OIU is further explained in Section V.) As shown in Fig. 3, a DDS-referenced composite clock (COMP CLK) connection is made to the OIU from a DDS timing source in the hub office. The OIU in the end office bank recovers DDS timing from the receive T line; this timing signal is then used to synchronize the end office D-bank and dataports.

3.2 Alternate configurations using dataport

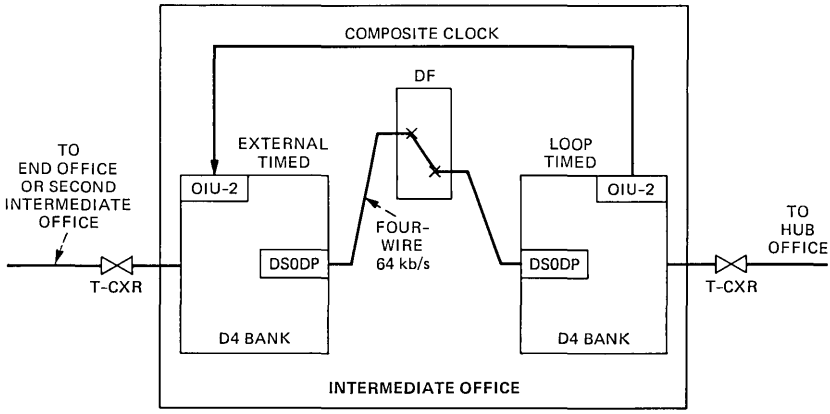
Three alternative configurations of dataport are discussed in this section. Fig. 4 shows a DDS arrangement where the end office uses only DS0 dataports. Note that 64-kb/s DDS channels, derived by the demultiplexing operation of the DS0 dataports, are connected to two external DDS OCUs. This D4 arrangement offers a direct alternative to the T1WB4/5 hardware normally equipped in DDS end-office installations.[9] This arrangement could also make use of the subrate data multiplier (SRDM) and integral subrate multiplexer (ISMX). Each of the OCUs must be synchronized to the DDS reference clock. This timing is provided by the D4 OIU common unit, as Fig. 4 indicates. The OIU generates two independent composite clock signals for such purposes. It should be noted that nothing precludes equipping the D4 bank of Fig. 4 with additional DS0 or OCU channel units.

DDS channels can also be extended using dataports. Fig. 5 shows the equipment setup that would be used in the intermediate office to implement the link. In the hub office, the channel would terminate in a DS0 dataport. The channel termination in the end office would be either an OCU dataport or another DS0 dataport (used as shown in Fig. 4). The intermediate link is created by connecting the DS0 of the system facing the hub-office side to the DS0 dataport of the system facing the end-office side. The DS0 dataports can be assigned independently and arbitrarily to any set of channel unit positions in each DS1 system. For synchronization, a clock signal from the hub-office-side OIU must terminate on the end-office-side OIU. Finally, the data-



CSU – CHANNEL SERVICE UNIT
DSU – DATA SERVICE UNIT
DF – DISTRIBUTION FRAME
DS0DP – DS0 DATAPORT
OCU – OFFICE CHANNEL UNIT
OIU – OFFICE INTERFACE UNIT
T-CXR – T-CARRIER FACILITY

Fig. 4—DS0 dataport in the end office.

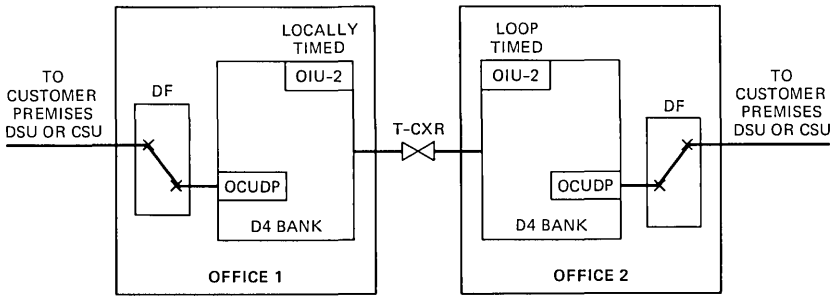


DF – DISTRIBUTION FRAME
DS0DP – DS0 DATAPORT
OIU – OFFICE INTERFACE UNIT
T-CXR – T-CARRIER FACILITY

Fig. 5—A tandem connection.

port channel could be further extended by again linking at a second intermediate office.

To indicate the versatility of the dataport approach, a non-DDS application is included and is shown in Fig. 6. In this situation the customer interfaces with standard DSU or CSU equipment. The system is synchronous, but clock reference is provided by one internal D4 bank oscillator, either in Office 1 or 2. The OIU in that reference bank



CSU – CHANNEL SERVICE UNIT
DSU – DATA SERVICE UNIT
DF – DISTRIBUTION FRAME
OCUDP – OCU DATAPORT
OIU – OFFICE INTERFACE UNIT
T-CXR – T-CARRIER FACILITY

Fig. 6—A stand-alone dataport system.

(e.g., Office 1) is capable of generating the necessary dataport clocks from the internal D4-bank oscillator. The OIU in the other office (Office 2, in this case) generates the necessary dataport clocks from the received T-carrier line signal.

IV. DATAPORT PERFORMANCE

As we mentioned, the DDS provides high-quality data channels to support *Dataphone* Digital Service. The major performance parameters specified are error rate, channel availability, and transmission delay. Dataport channels have been designed to meet the established performance objectives. Thus, channels using dataports and channels using conventional DDS hardware are indistinguishable from a user's point of view. As we will discuss, dataport channels incorporate error control techniques and include maintenance features compatible with existing DDS network capabilities to meet these objectives.

4.1 Dataport connections

Dataport circuits have been integrated into DDS channel connections in configurations that closely emulate the present DDS structure.[10] This is apparent in Figs. 7a and 7b, which contrast a typical DDS connection with one derived via dataports. As shown in Fig. 7a, a DDS connection consists of a long-haul network interconnecting two DSAs with local serving links that consist of two T1 lines in tandem with local baseband facilities. In the conventional arrangement the T1 lines connecting the serving end office to the hub office are dedicated to carrying DDS circuits. These circuits originate from customers served by that wire center and are typically multiplexed into a 64-kb/s T1 channel.

The dataport connection in Fig. 7b is only slightly different in that the T1 line between the serving end office and the hub may be

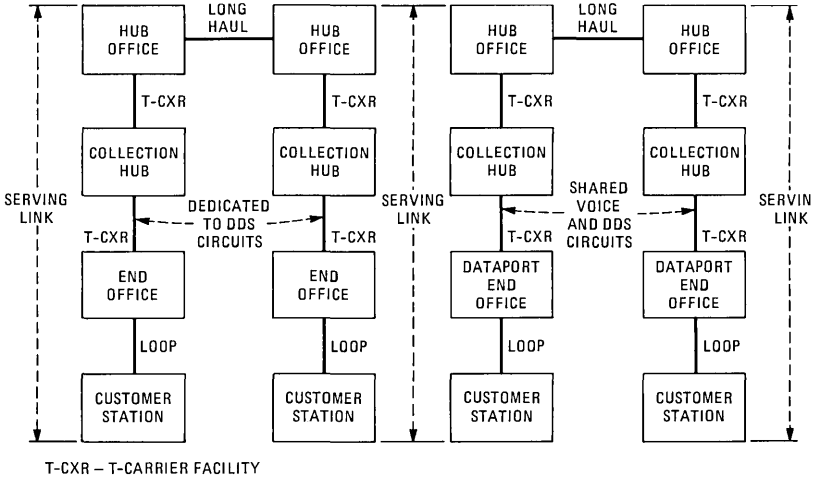


Fig. 7—(a) DDS circuit connection model. (b) DDS dataport connection model.

primarily used for *voice grade* services. This difference is important when the error-free second performance objective of such a connection is considered.

4.2 Error performance

Based on allocation procedures, the error performance requirement of a T1 line used in the DDS network has been established to be 99.6-percent error-free seconds. Surveys indicate that about 80 percent of T1 lines meet this performance requirement. For a T1 facility that is to be dedicated to DDS, performance is ensured by screening prospective connections against a quality criterion; however, dataport channels provisioned on in-service T1 lines intended primarily for voice services may not meet the DDS objective without additional treatment. Forward-acting error-correction techniques have been implemented in the dataport designs to ensure that DDS error performance criteria can be met without qualification of the carrier facility. As is discussed in a companion article[11] two techniques are used. A "vote with majority rule" scheme that takes advantage of the inherent redundancy in the DDS format is used for the subrate channel speeds. For the 56-kb/s data rate, two 64-kb/s carrier channels provide the data and parity bit streams required to implement a cyclic redundancy code. Field studies that take into account the actual bit error characteristics of T1 lines have demonstrated the capability of these codes to meet the DDS error-free-second criterion.

4.3 Transmission delay

A second parameter of importance in data transmission is round-trip delay. Although the circuit connections in Figs. 7a and 7b are

similar, the use of dataport error-correction circuitry results in an increase in transmission delay. This delay is a result of the coding/decoding and buffering required for error correction. For example, a 9.6-kb/s channel may experience a coding delay of at least one byte. The maximum increase in delay caused by the error-correction circuitry has been estimated to be less than 0.6 ms for all subrate speeds and less than 0.4 ms for the 56-kb/s data rate. When compared with the end-to-end transmission delay that may be encountered on a DDS circuit (approximately 50 ms), the effect of the error-correction circuitry may be considered to be insignificant.

4.4 Availability

Much of the DDS equipment operating at DS1 and higher rates employs continuous performance monitoring and manual or automatic switching to standby equipment in the event of failure. Since the DDS uses existing carrier systems for both the exchange area and long-haul transmission, the availability objectives have included allowances for carrier system failures and restoration. On a per-circuit basis the concepts of single point of customer contact and one person testing are important parts of the DDS maintenance philosophy. This philosophy is embodied in test features that permit trouble sectionalization by means of a series of remote loopbacks under control of a centralized maintenance center. The dataport incorporates the circuitry necessary to preserve this important test capability. Thus, from a maintenance viewpoint, the dataports are functionally equivalent to the displaced equipment.

V. DATAPORT IMPLEMENTATION IN D4

The D4 channel bank has two main functions that allow the dataport channel units to operate. The first function is signal translation between the bipolar format on the T-carrier facility and the unipolar, logic-level format on the channel unit backplane. The second basic function is that of timing synchronization between the DDS network and the D4 bank.

5.1 Signal translation

The D4 bank may operate with T-carrier facilities working at the basic T1, T1-C, or T2 rate. In addition, the T2 rate may be carried over regular cable or over a fiber lightguide medium. The bank converts logic-level signals to the appropriate analog bipolar pulse format for transmission on the facility.[8]

The basic T1 carrier rate of 1.544 Mb/s is obtained by performing 8-kHz sampling on analog channels, using 8-bit pulse code modulation (PCM) coding of each sample and grouping 24 such channels together

with one additional bit that provides framing information. Thus, there are 24 groups of eight bits plus a 193rd bit to perform framing every 125 μs. In the direction from the DS1 facility toward the dataport, this digital stream is made available by a common backplane bus to all 24 channel units of a digroup. A 1.544-MHz clock signal is also supplied via the backplane. Regular analog channels ignore the digital bus and accept a signal produced in the common circuits and distributed on a pulse amplitude modulation (PAM) bus. As shown in Fig. 8, the appropriate PAM sample is gated into each analog channel unit under the timing control of two selection leads (P and Q) and a timing pulse (window). These same timing control signals also gate the correct byte of digital data bus information into the dataport channel units.

The data bus presents to each channel one 8-bit byte every 125 μs in a burst at 1.544 Mb/s, for an effective bit rate of 64 kb/s. The dataport channel unit converts the 8-bit burst into the proper DDS DS0 format signal. In the D4 transmit direction toward the T-carrier facility, the dataport units must place onto the backplane bus an 8-bit burst of data at 1.544 Mb/s when directed by the D-bank's timing signals.

One additional control signal is presented to each channel unit to inform the unit that the D bank is "out-of-frame." This information is

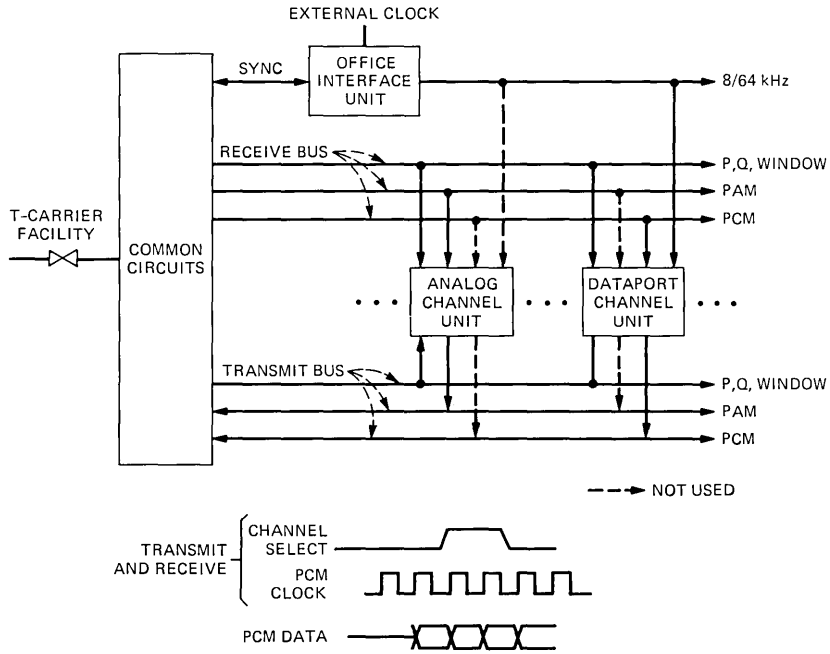


Fig. 8—D-bank channel unit interface.

used to initiate a "multiplex out-of-sync" control signal to the DDS station equipment.

5.2 Clock synchronization

As previously mentioned, the DDS is a synchronous network, and a D4 unit must be locked onto the DDS clock system. As described in Refs. 5 and 6, the cross-connection scheme for all DDS signals within an office requires that DS0 64-kb/s signals be timed to a common 64-kHz bit clock and a common 8-kHz byte clock (see Fig. 2). This allows DS0 signals within an office to be easily interconnected.

5.2.1. DDS clock signals

The clock signal distributed within an office is referred to as a composite clock. This signal is a bipolar 64-kHz waveform with a five-eighths duty cycle. This duty cycle allows for transmission delays between interconnected DDS equipment in the office. Each bipolar pulse marks a new bit in the DS0 signal. All DDS equipment will start a bit transmission on the leading edge of the bit clock and will sample a received bit on the trailing edges of the bit clock. Figure 9 shows the clock waveforms.

The byte information clocking is obtained from bipolar violations contained in the composite clock. Every eighth pulse is a violation that signals the eighth bit of each DS0 byte.

5.2.2 OIU functions

The main dataport task for the D4 office interface unit is to generate a DDS clock and distribute synchronization signals to each channel

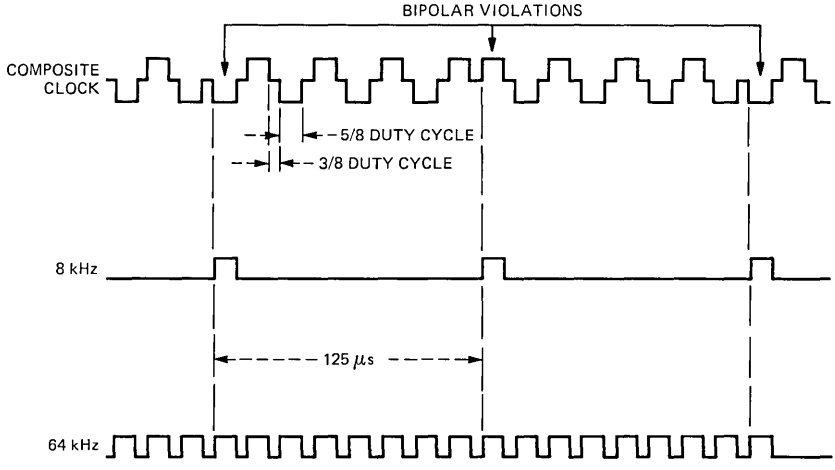


Fig. 9—DDS clock waveforms.

unit. In addition, there are several D4 timing synchronization functions that the OIU performs, as described in Ref. 8. There are three OIU timing modes—local, loop, and external.

In the external-timed mode, used in DDS hub offices, an existing source of DDS composite clock will supply a signal to the D4 bank, which will cause the outgoing T-carrier signal frequency to be locked to the DDS clock (Fig. 3). In the loop-timed mode, the OIU provides signals that lock the outgoing T-carrier signal to the received T-carrier signal. This is the usual case for a DDS end office served by dataport. The DDS synchronization in this case is not obtained directly from a local DDS clock, but comes from the hub office clock through the hub-located D4 bank and the connecting T-carrier facility. The OIU can serve as a source of composite clock to another D bank located in the same office. Such D banks would be conditioned to accept composite clock by being provisioned in the external-timed mode. In this way the DDS can chain a digital connection from a hub office to an end office through an intermediate office (see Fig. 4).

The local-timed mode is used when external synchronization of the D4 bank is not required. This is the case when dataport channel units are installed to provide a point-to-point connection isolated from the DDS network (Fig. 6), or when the D4 is equipped with only VF channel units. For such cases, the D4 bank transmit clock is allowed to run freely. The far-end D bank would be loop-timed for dataport applications. This yields an isolated connection for serving special needs outside the DDS. Figure 10 illustrates the various timing options. The functions of the OIU will be examined next from a block diagram view.

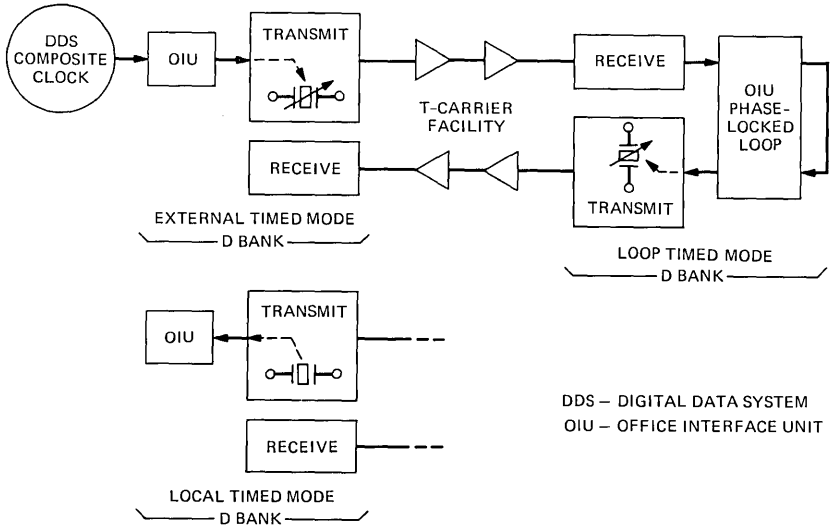


Fig. 10—D-bank timing.

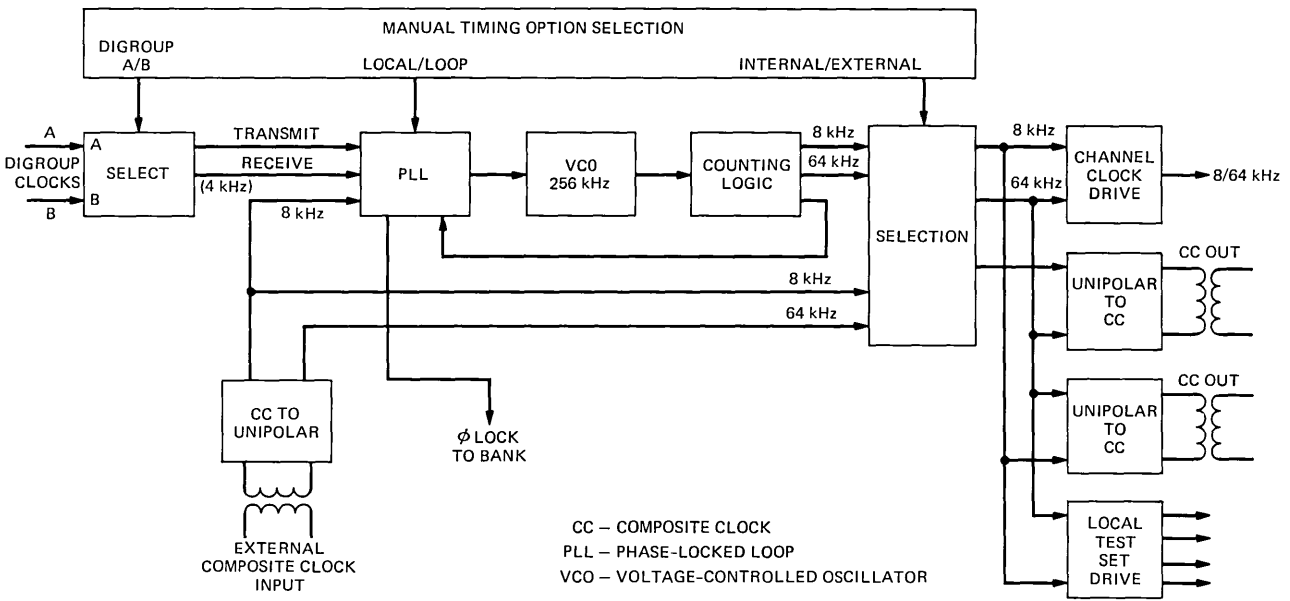


Fig. 11—OIU block diagram.

5.3 The OIU circuit

There are five functional blocks in the OIU circuit (Fig. 11). These blocks serve to properly option the OIU via manual switches, to select *A* or *B* digroup timing, to accept an office composite clock, to synchronize the bank, and to provide output clock signals.

The option settings for the OIU are determined by switches mounted on the faceplate of the unit. One switch selects either the A digroup or the B digroup of the bank to serve as the timing master for synchronization. A second switch serves to select either the external timing option or one of the two internal timing options, local or loop timing. The phase-locked loop (PLL) and voltage-controlled oscillator (VCO) synchronize the bank to the external clock, if present, and, in the absence of an external clock, serve to generate the 8- and 64-kHz clock signals. The output of the 256-kHz VCO is divided down and compared with the reference clocks. Counting logic formats the 256-kHz output into 8- and 64-kHz outputs with appropriate asymmetric duty cycles. An additional stage of selection logic steers either the internally generated or externally supplied 8 and 64 kHz to the output clock drivers.

The output driver section has three functions. An analog circuit converts the 8- and 64-kHz clocks into a tri-level voltage wave (integrated clock) distributed to all channel units in the bank. A duplicated set of drivers converts the unipolar signals back into a composite clock format with appropriate bipolar violations for driving other D banks. Finally, a buffer supplies clocks to local test equipment that can be connected to the bank.

5.4 D4 bank conditioning for dataport applications

As described above, by use of the OIU and dataport channel units the existing D4 channel bank can be conditioned to provide channel connection for the DDS. None of the other existing circuits of the D4 bank need modification to allow this capability. Through the OIU the D4 bank can be synchronized to the DDS system clock. The synchronization information is distributed to the channel units via a backplane bus structure; a similar bus arrangement is used to feed the digital channel information between the common equipment and the dataport.

VI. SUMMARY

The Bell System is continuing to evolve its capability to provide economical, high-quality data channels such as those provided by the Digital Data System. As originally designed, DDS equipment could be used most efficiently to serve geographic areas with a concentrated demand for data services. The dataport feature of D4 has been devel-

oped to complement the high-capacity DDS multiplexing equipment with serving arrangements that can be installed quickly and economically to serve small numbers of customers. Dataports provide a new interface to allow for voice and data sharing of the D family of channel banks and open up many new areas for innovative application of digital channels.

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D4 Digital Channel Bank Family:

Dataport—Channel Units for Digital Data System Subrates

By T. J. APRILLE, D. V. GUPTA and P. G. ST. AMAND

(Manuscript received July 30, 1981)

The single-channel dataports are a series of D4 channel units that convert the digital signal derived from one T-facility time slot by the D4 common circuits to an appropriate format at speeds of 64, 9.6, 4.8, or 2.4 kb/s for use in the Digital Data System (DDS). They come in two formats, the first being the DDS bipolar format for 64 kb/s and the second, for the remaining three speeds, being an EIA RS-449 format. Their error-correction feature ensures 10^{-8} error-rate performance for a 10^{-3} error-rate transmission channel. Advances in large-scale integration (LSI) technology have allowed the packaging of all the digital circuit functions needed into the space of a single channel unit. An on-board power converter unit generates the additional current required by the dataports over that needed by regular analog channel units. The local loop side of each channel unit uses integrated technology to achieve signal equalization and timing recovery. Standard DDS remote maintenance features are provided. The dataport channel units are easily installed and removed; they supply economical digital transmission.

I. INTRODUCTION

The D4 channel bank can be equipped with over forty different channel units, each one designed as a customized transmission and signaling interface between the T-carrier transmission facility and the central office switch or local wire loop. These channel units are used for diverse applications, such as regular telephone grade voice band and radio program wide band, dial-pulse signaling and nonsignaling transmission only, switched service and private line, and analog and

digital loop service. Dataports are the series of D4 channel units that allow a direct digital interface into the T-facility from the customer loop, bypassing the regular analog-to-digital conversion of voice channel units.

As Ref. 1 describes, some dataports connect to the customer's location, while others link inside a telephone office. For each of the above two applications, two kinds of dataports exist, those that serve a customer using one T-facility time slot and those that use two time slots. This article describes the hardware implementation of the class of dataports that serves a customer at a data rate of 2.4, 4.8, or 9.6 kb/s, the so-called "subrate" dataports. A companion article details the designs for the class of dataports that serves a customer at 56 kb/s.[2] The basic D4 bank functions are described in Ref. 3, while the system issues of dataport are fully treated in Ref. 1.

This article briefly reviews the various applications and system issues of dataports. The basic hub office unit, the digital signal zero (DS0) dataport, is then described, as well as the basic end office dataport, known as the Office Channel Unit (OCU) dataport. The last variety of dataport discussed is the Data Service Unit (DSU) dataport. Finally, the subrate error-correction algorithm and the on-board power converter are detailed. Field evaluations show that dataports are reliable, quick to install and remove, and are easy to maintain. Dataport has allowed the Digital Data System (DDS) to expand at low cost to serve the increasing needs of the *Dataphone** Digital Service.

II. GENERAL FUNCTIONS

2.1 Dataport applications

Figure 1 shows the typical dataport configurations.[1,4] The DDS network offers data transmission service to every major metropolitan area in the United States.[5,6] If a customer network requires a termination in a serving area not now covered by regular DDS equipment, a dataport extension can be made. An existing DDS hub office serves as a focal point for gathering various DDS signals and multiplexing them together for transmission across the country. The hub office sends one customer signal in a format of 64 kb/s, the DS0A format, to a DS0 dataport. The DS0 dataport inserts, through the D4 bank interface, the 64 kb/s signal onto the T-facility channel time slot. The T-facility carries the signal to a D4 bank at the local end office that serves the customer location. Each local office has an OCU dataport, which receives the single time slots, corrects errors in the receiver data, and sends out data to the customer at the baseband rate over the local distribution

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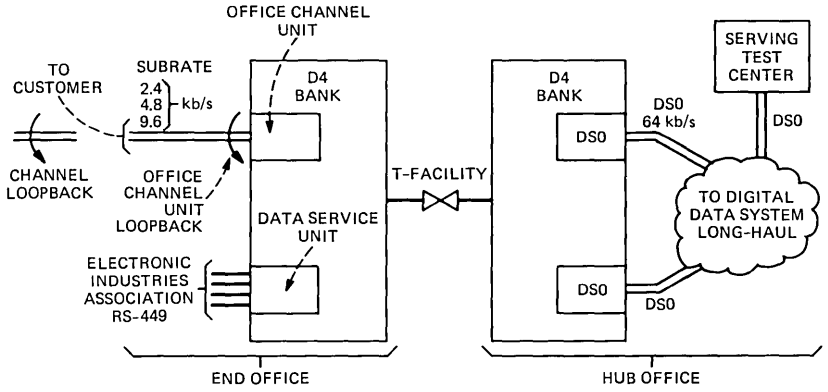

Fig. 1—Dataport applications.

cable. At the customer premises, the local cable pairs terminate either on a DSU or Channel Service Unit (CSU).[7] This DS0, T-facility, and OCU link allows DDS to grow from an existing hub office out to a new serving central office of the *Dataphone* Digital Service. The dataport is designed to handle small numbers of DDS channels economically. Combining voice and data services in the same digital bank lowers capital costs and efficiently uses the T-carrier plant. Offices with many customers could still be served by the separate, dedicated DDS equipments.[8]

For special applications, the DSU dataport has a DDS-type link between two telephone central offices for internal use.[9] In effect, the miles of cable pairs that connect the OCU with the customer-located equipment are shrunk to a few millimeters of printed wiring board path. The DSU dataport has a direct Electronic Industries Association (EIA) connection and does not need a separately mounted DSU. If the two end offices of the point-to-point link are directly connected by one T-system, then a DSU dataport may be used in each terminating D4 channel bank and no OCU dataports are required. The 10A Remote Switching System uses the DSU dataport in precisely this fashion.[10]

2.2 D4 channel bank and channel multiplexing

The D4 channel bank using a digital signal one (DS1) facility has twenty-four time slots of 64 kb/s each. All subrate dataport channel units occupy one physical mounting position in the D4 bank and use one time slot, just as regular analog channel units do. This allows dataports to be installed in any of the channel-unit positions of the D4 bank. One common D4 circuit pack, the Office Interface Unit (OIU), and a connection at the hub office to the DDS network timing system are required to convert a standard D4 bank to a dataport-capable

bank.[1] This simple procedure allows the D4 bank to mix conventional analog and dataport DDS services.

The single customer DS0A signal is handled in the network in bytes of eight bits. Each byte contains a leading multiplexing bit, which for subrate DS0A signals is always a logic zero, six customer data bits, and a control mode bit. In each 8-bit byte only six bits carry data, thus the effective data speed is 6/8ths of 64, or 48 kb/s. The basic subrate DS0 signal contains repeated information. The highest speed signal has five repeated bytes; therefore, the true customer information rate is one-fifth of 48 kb/s, or 9.6 kb/s. The DS0A signals for 4.8 and 2.4 kb/s service similarly have repeated bytes of ten and twenty times. It is the repeated byte pattern that allows dataport to carry out error correction of the local T-facility transmission plant. An additional format exists that allows standard DDS equipment to multiplex subrate data signals for efficient transmission in the national long-haul network.

2.3 Maintenance plan

The maintenance strategy for testing DDS is described in Refs. 11 and 12. The individual customer channels of a dataport circuit are analyzed for trouble conditions in the same manner as a conventional DDS channel. When a trouble is reported by the customer to the DDS Serving Test Center (STC), the customer channel is first monitored in both directions on an in-service basis. The STC checks the data signals for the occurrence of specific repeated control signals, which would automatically replace the customer data in cases of equipment failures. If no indication of a network failure is detected by this monitoring, then the local cable pair is removed from service and checked by loopback tests. There are three dataport loopbacks from the DS0 channel and hub office. The STC can cause a loopback to occur at the output of the OCU dataport, at the end of the loop plant in the customer premises DSU or CSU, and at the output of the DSU. The "OCU loopback" tests out all the network from the STC to the OCU output circuits that drive the local cable pairs. The loopback at the input of the customer-located equipment, called the "channel loopback," tests the local distribution cable from the end office to the customer site. The final "DSU loopback" guarantees the integrity of the data service unit located on the customer premises. Thus, the loopbacks are used to isolate the trouble to the internal telephone company network, the outside cable plant, or the customer-located equipment. To obtain an error-rate performance measure, the STC starts a loopback by sending out a fixed-control-code byte to lock the distant circuit into the loopback state. Next, an alternating pattern of the fixed-control-code byte and a pseudo-random message sequence is sent to the distant circuit. At the loopback point the fixed-control code maintains the

loopback state of the equipment while the message sequence is reflected back to the STC. The received pseudo-random sequence is examined at the STC, and the error-rate performance of the circuit is measured.

If the OCU loopback test fails, then the problem lies in the internal DDS network. To isolate the problem further, a local craftsperson can manually activate dataport loopbacks. Each OCU and DS0 dataport channel unit has a jack access that alllows a looping plug to be inserted, which causes the DDS signal to be looped back for comparison at the STC. In addition, the looping plug also supplies a jack access for use with portable test equipment.

The DSU dataport has all the normal DDS remotely controlled loopback features. In addition, the customer-controlled loopbacks specified in the EIA RS-449 document are included. Maintenance of the DSU dataport is described in Section 5.3.

III. DS0 DATAPORT HARDWARE

The DS0 dataport converts DDS bytes in bursts of eight bits at a DS1, 1.544-Mb/s rate to and from a continuous DS0, 64-kb/s rate. The unit operation is frequency synchronous but allows arbitrary phase difference between the DS1 and the DS0 signals. In this article, relative to the local D4 channel bank, the transmit direction defines signals toward the T-carrier facility and the receive direction defines signals toward the customer.

3.1 Transmit and receive circuitry

A simplified block diagram of the DS0 dataport is shown in Fig. 2. In the receive direction, the 1.544-Mb/s pulse code modulation (PCM) stream is available to the channel unit from the receive PCM bus.[1] The rate converter picks off the 8-bit DDS byte from the PCM stream and in normal operation outputs the same eight bits at the 64-kb/s rate. Since there are 24 8-bit bytes on each frame of the DS1 stream, receive select information from the D4 common circuitry is required to select the proper byte. In Fig. 2, the output of the rate converter is sent to the code insertion function (Section 3.2), and that output is then connected to the input of a 3-out-of-5 error-correction circuit. For subrate data, this circuit allows DDS error-rate objectives to be met without special testing and selection of T-line facilities. A discussion of the operation of this circuit is given in Section VI. The output of the error-correction circuit feeds a buffer that converts the logic signal into a bipolar nonreturn-to-zero (NRZ) signal.

In the transmit direction a similar but reverse process takes place. This path contains no error correction, and the transmit PCM backplane

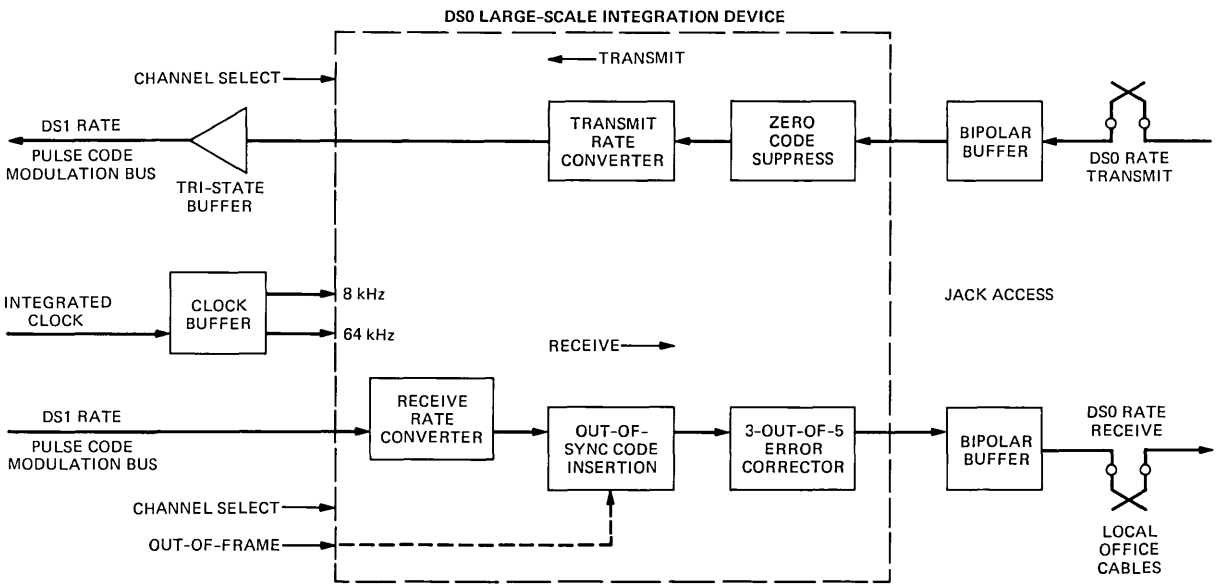

Fig. 2—DS0 dataport channel unit.

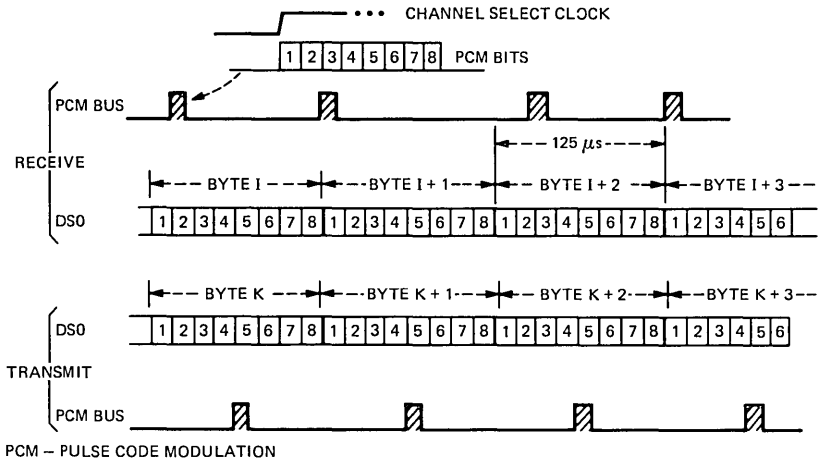

Fig. 3—DS0 input/output signals.

bus that connects all 24 channel units is driven by a tri-state buffer (logic zero, one, or open circuit outputs).

The input and output signals described above are shown in Fig. 3. Only the appropriate dataport PCM bus signals are shown. The DS0 receive and transmit signals are in byte and bit synchronization with the DDS clock. Also, while the receive and transmit D4 bus signals are frequency-synchronized, they are not phase-synchronized with each other or with the DS0 signals.

Circuitry within the dotted lines in Fig. 2 is contained in an N-channel metal-oxide semiconductor (NMOS) LSI chip in a 40-pin dual in-line package (DIP). Since this chip forms almost the entire circuit of the DS0 dataport channel unit, it has been appropriately named the DS0 chip. Further information on the realization of the chip can be found in a companion article.[13]

The integrated clock timing is shown in relation to the D4 bank composite clock and to the 8- and 64-kHz clocks used by the DS0 chip in Fig. 4. The clock buffer circuit shown in Fig. 2 provides level-detector circuitry needed to separate the 64-kHz bit clock and 8-kHz byte clock. It also has a high-input impedance to prevent loading down the clock bus.

3.2 DS0 control code substitution

As we saw in Fig. 2, whenever the near-end or far-end D4 bank is not framed[3] (the near-end bank in red or yellow carrier group alarm), an out-of-frame signal is presented to the DS0 chip. In this mode the receive rate converter outputs, irrespective of the input signal, a special DDS "multiplex out of synchronization" byte code. This informs local customer equipment of a transmission equipment malfunction.

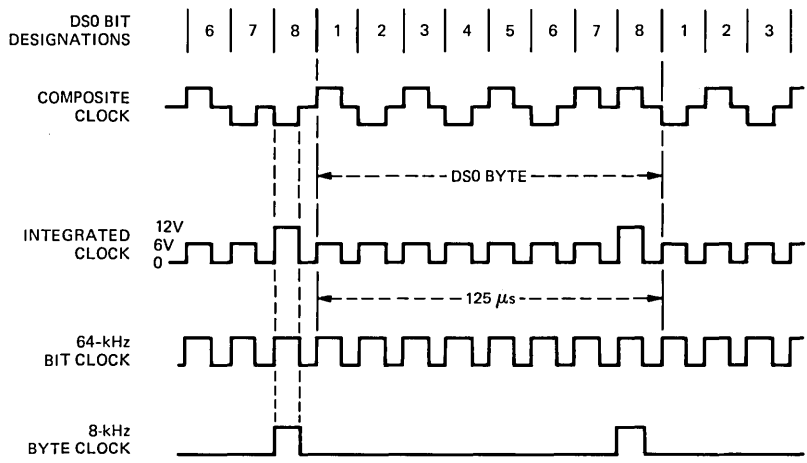

Fig. 4—DDS clock signals.

Similarly, when the transmit rate converter receives an unallowed byte code of all zeros in bits two through eight, the output byte is modified automatically to force bits three and four to logic ones. The receipt of such an unallowed code suggests that a malfunction in the equipment on the customer side of the DS0 dataport has occurred. For example, this code would result if the wire pair carrying the DS0 signal to the dataport were cut.

3.3 Phase synchronization circuit

Figure 5 is a block diagram of the transmit rate converter, which shows three 8-bit byte shift registers. Each register is loaded at 64 kb/s and unloaded at 1.544 Mb/s. Three shift registers are required to synchronize the DS0 byte to the DS1 rate, allowing arbitrary phase difference between input and output. This phase shift can be caused by channel unit placement within the 24 time slots of the bank and by T-facility phase jitter.

The normal operation of the three registers is depicted in Fig. 6. Register A loads byte K at 64 kb/s and then unloads it at the start of bit 5 of byte K+1 at 1.544 Mb/s; it loads and unloads every third byte in the same manner. The loading/unloading sequence is load A, unload C, load B, unload A, load C, unload B, load A, unload C, etc.

If there is a phase shift of the 1.544-MHz transmit clock, a sequence correction may be required to prevent data destruction. The phasing algorithm checks to see if a register is being concurrently loaded and unloaded, and if so, then the same information in the register is unloaded twice. This process will always break the overlap; an example is shown in Fig. 7. The unloading pulse advances a total of three-quarters of a bit (at the 64-kb/s rate). The first overlap occurs in

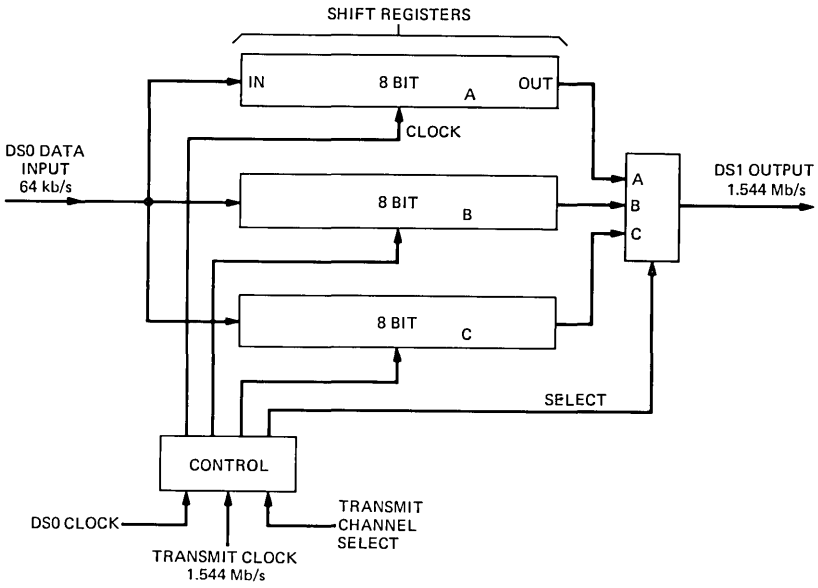

Fig. 5—Transmit rate converter.

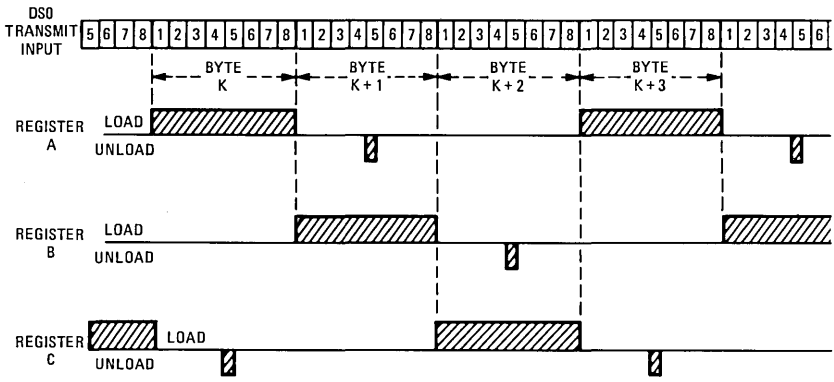

Fig. 6—Transmit rate converter load/unload sequence.

register B, so register B is unloaded twice. An overlap will not take place again as long as the input and output phase difference stays within plus or minus eight bits at the 64-kb/s rate. The receive rate converter is equivalent to the transmit rate converter except for the interchange of input and output bit rates.

3.4 DS0 dataport maintenance

Figure 2 shows two jacks on the office wiring side of the channel unit that can be used for maintenance of the DS0 dataport. By

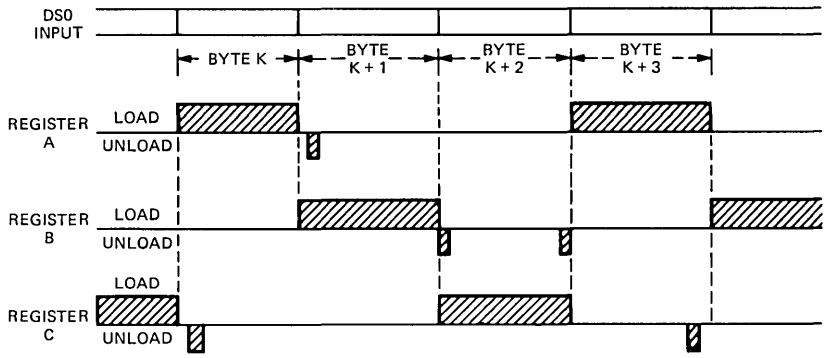

Fig. 7—Transmit rate converter overlap correction.

manually inserting a special plug into the faceplate of the dataport channel unit (accessible from the front of the bank), a loopback is made that connects the bipolar DS0 receive signal back to the DS0 transmit input. This ability makes it easier to locate faulty equipment. The maintenance plug and the DS0 dataport, as well as the OCU and DSU dataports, are shown in Fig. 8. The two jack connectors on the plug can be used to access the channel, in either direction, with portable DDS signal-generation test equipment.

IV. OCU DATAPORT HARDWARE

The OCU dataport contains all the digital circuitry of a DS0 dataport, and it includes the additional circuits to convert the DS0 signal to and from the local loop format used for communication with the customer premises. Figure 9 is a block digram of the office channel unit section of the OCU dataport. The major functions include a synchronous-timing-generation circuit, a rate-matching section, control-code recognition, analog signal conditioning, and a local cable interface.

4.1 OCU signal formats

The DS0 signal, as described in Section 2.2, has a 64-kb/s, byte-oriented format. The signal to the customer over the local cable pairs is at the customer data-bit rate, with a logic one represented by a bipolar pulse and a logic zero represented by no pulse. The six data bits of the 8-bit byte at the DS0 level are sent to the customer in a bit-by-bit, non-aligned fashion. For example, at the 4.8-kb/s service rate, the customer will get the six data bits that are repeated ten times in the DS0 byte at the 64-kb/s rate. This yields six new data bits every ten times 125 μs, or 4800 b/s.

The receive DS0 signal may be pre-empted by the STC during maintenance operations. The control-mode bit is set to a logic zero,

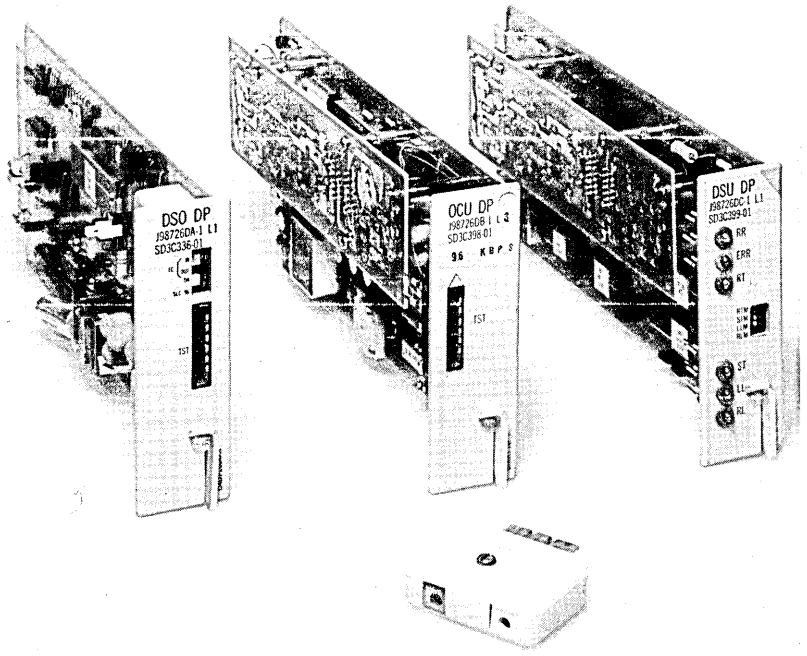

Fig. 8—DS0, OCU, and DSU dataports.

and the six normally allocated customer bits are now used to define a maintenance code, which can be used to start loopbacks or to signify transmission difficulties. Monitoring circuits in the OCU section are designed to recognize the codes for maintenance testing.

No clock signals are separately sent to the customer site; the customer-located DSU must recover the clock frequency from the received OCU data signal. This requires that enough energy always be sent to the CSU or DSU in the signal, which in turn forbids transmission of long strings of zeros (no bipolar pulses) in the customer data. To maintain bit transparency, a zero-code substitution is employed by the OCU, where any DS0 byte containing six data bits as all zeros is replaced on the local cable pair by a bipolar violation sequence. In addition, several control codes are also transmitted to the customer site as coded bipolar violations. Reference 7 describes the code translation from the byte format to the bipolar violation format.

4.2 Digital hardware realization

The digital circuitry for the office channel unit portion of the OCU dataport is contained in the previously mentioned DS0 device and in two smaller LSI devices. These "rate-matching" devices convert the

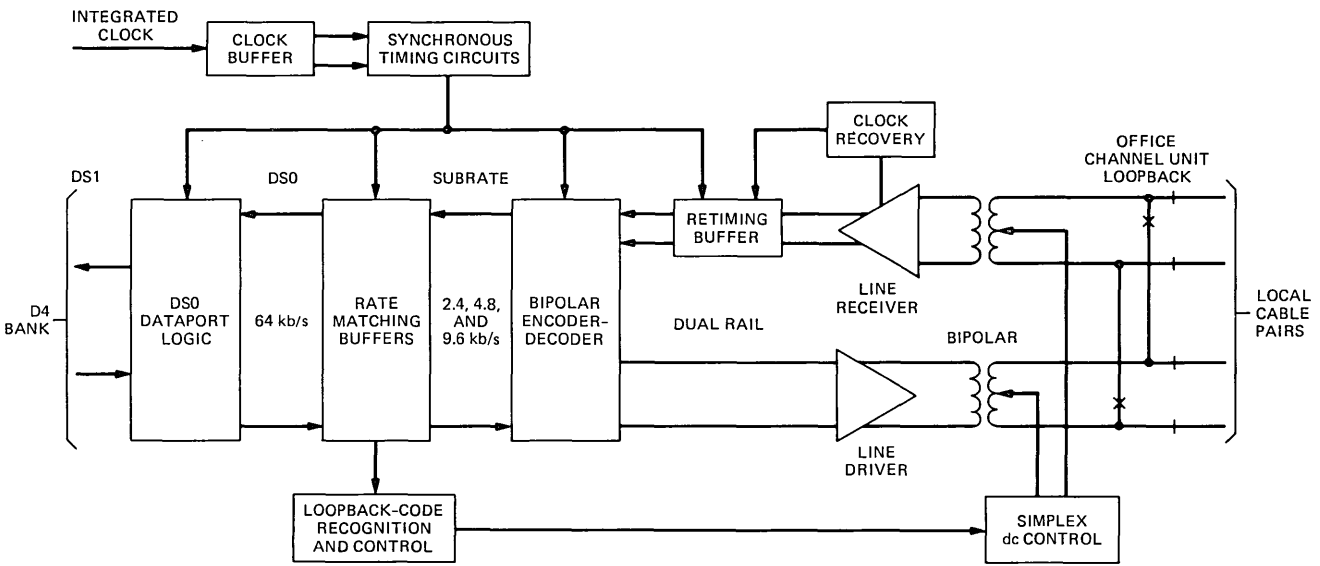

Fig. 9—Block diagram of the OCU dataport.

signal at the DS0 rate to the customer rate, monitor for the presence of control codes, and convert bipolar violations to control codes. The DS0 device has the additional OCU function of providing a high-speed clock and strobe signal to the rate-matching devices. The rate-matching devices use the high-speed clock at 1344 kHz, the least common multiple of 64, 56, and 9.6 kHz, to generate customer bit rates. The OCU loopback command, which causes a relay to connect the output of the OCU back to the input at the local cable pairs interface, is detected in the rate-matching devices.

There are two logic-level outputs from the bipolar encoding logic that together form a dual-rail signal that creates a bipolar loop-line signal. In this scheme, one logic rail supplies the bits for the positive voltage signal, and the other rail supplies the bits for the negative voltage signal. On the loop line during normal data transmission, a logic 1 is transmitted as either a positive or negative pulse with successive pulses alternating in polarity; a logic zero is transmitted as no pulse. Control-code information is transmitted between the OCU dataport and customer premises unit by bipolar violation sequences, i.e., successive bipolar pulses with the same polarity.[7]

4.3 Analog line circuits

In the direction from the T-facility toward the local cable pair, the analog line-drive circuitry transforms the logic signals into bipolar pulses suitable for transmission on the cable pairs to the customer. It contains a level shifter, band elimination filter, line-drive amplifier, transformer, lighting protection circuitry, and two low-pass filters.

A Butterworth filter, with a pole at 1.3 times the signaling rate, limits the high-frequency signal energy on the line. Also, a 28-kHz band elimination filter is implemented to eliminate 28-kHz energy from interfering with other services that may be in the same loop cable.

The line-driver circuitry buffers the filters from the varying impedances of the transmission line. It also converts the dual-rail signal, by means of a transformer, to the bipolar signal for transmission over the cable pair.

In the direction towards the T-facility from the local cable pair, the loop signal passes through the line-receiver circuitry that consists of lighting protection, line transformer, input buffer amplifier, low-pass filter, and line equalizer. It also contains a second-order filter that, when combined with the first filter, forms a third-order Butterworth low-pass filter with a cutoff frequency equal to 1.3 times the signaling rate. The filters in this circuitry are used to increase noise immunity and provide pulse shaping for the following OCU logic circuits.

The local loop plant consist of 19-, 22-, 24-, and 26-gauge metallic

pairs; the insertion loss of these cables is a function of both frequency and length. To compensate for the variously shaped loop losses an adaptive equalizer is required in the line receiver that terminates the cable pair from the customer. The equalizer has variable gain and a movable real zero, both controlled by a single variable resistor, to compensate for the varying loop characteristic. The equalizer output signal drives a slicer circuit, the outputs of which form a dual-rail digital signal that serves as the input to the conversion logic.

The analog portion of the OCU dataport was developed using existing and ongoing designs. The real effort was to realize those designs with much lower power drain and in a much reduced area. To this end, Standard Tantalum Active Resonator (STAR) DIPs[14] were used in the design of the low-pass filters. The gain-zero equalizer was implemented by using the STAR-DIP along with a multiple operational amplifier DIP.

The level shifter and line-driver circuitry are contained in a 12-pin Transmission Equipment DIP (TED).[15] A second 24-pin TED is used for the active circuitry in the transmit side and contains the line terminator, equalizer, and slicers.

V. DSU DATAPORT HARDWARE

The DSU dataport contains all the digital circuitry of the OCU dataport, and it includes the additional circuits to convert the OCU dual-rail local-loop format signal to an EIA-compatible multi-pin interface signal. Figure 10 is a block diagram that shows how the functions of the data service unit are added to the basic OCU dataport. The major functions include a timing synchronization circuit, a control-code-to-

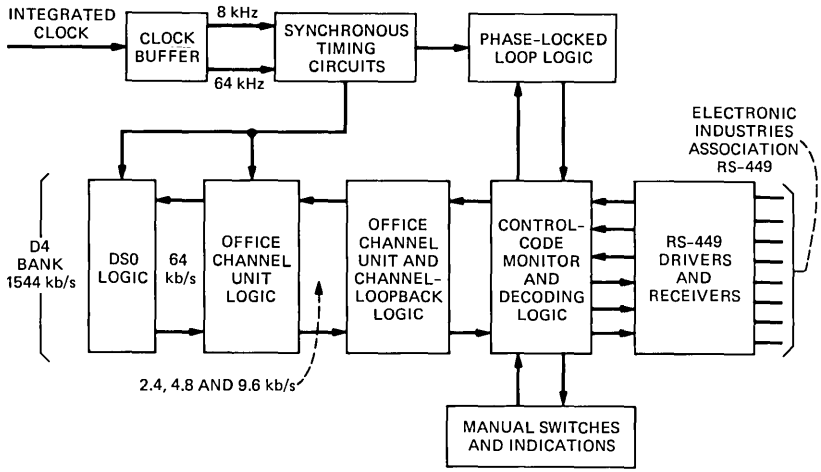

Fig. 10—Block diagram of the DSU dataport.

control-signal section, an EIA RS-449 interface,[16] and maintenance controls and indications.

5.1 Hardware realization

The digital outputs of the OCU section are fed into an LSI device and not into the normal analog OCU circuits. In this application, the normal cable loop pairs to the Data Service Unit do not exist; the customer-located DSU is incorporated directly into the D4 bank channel unit. The equalizers, relays, and analog filters are not needed. The workhorse DS0 LSI device is again used to provide functions needed for the DSU dataport application. The timing synchronization is obtained directly from the clock feeding the OCU section, and it is not recovered from the OCU data stream as would normally be done by a remote DSU. While the frequency is easily obtained, strobe signals used in the DSU LSI device require phase alignment with the data produced by the OCU devices. A phase-locked circuit slips the clock feeding the DSU section until the DSU strobe signal is aligned properly with the OCU data. At this point, the circuits are synchronized and will remain synchronized until power interruption or unit removal. The digital alignment circuit eliminates the need of the regular DSU clock-recovery circuit and crystal oscillator.

The DSU logic monitors the incoming data from the OCU section for control codes, indicated by bipolar violations, which here must be decoded from the dual-rail logic signals. These control signals and other status signals are decoded as individual logic-level leads. These signals, indicating loopbacks, idle conditions, and line errors, are used as maintenance aids and are also presented to the user interface.

5.2 User data interface

The signals to the user from the DSU dataport are in accordance with the EIA RS-449 standard.[16] The D4 bank has provision for only ten leads to be brought out from each channel-unit position, so the full 37-pin format of RS-449 could not be accommodated. Since the dataport is used as a point-to-point, private-line, nondial-up connection, many of the "mandatory" EIA signals are provided with the use of the EIA-termed "dummy" signal generators by simply tying a lead to a dc source voltage through a resistor. The active signals used are transmit clock and data, receive clock and data, signal quality (generated by the D4 bank's out-of-frame detector), local and remote loop commands, and the needed RS-423 common-signal reference leads.

5.3 Maintenance capabilities

Maintenance features, suggested in RS-449, have been implemented in the DSU dataport in addition to all the normal DDS features. The

OCU and channel loopbacks, described above, are provided in the DSU dataport even though there is no real local cable pair connecting an OCU and DSU. The loopbacks are carried out in logic in the center of the DSU dataport function, so that from any remote DDS test facility, the DSU dataport responds in the identical way that a standard OCU and customer-located DSU would respond. The DSU dataport has many additional on-board maintenance features. Internal looping and error-detection circuits rapidly detect faults. The user can initiate, through the electrical RS-449 interface, the "Local" and "Remote" loopbacks of RS-449. This allows automatic fault isolation under user control, without the need of intervention by the regular DDS maintenance craft. An array of light-emitting diodes and toggle switches allows local manual-fault detection and isolation.

VI. ERROR CORRECTION

T-carrier facilities were initially designed for voice quality transmission; as such, the T1 and T1C lines are engineered so that 95 percent of the systems have a probability of line error, p, being $\leq 10^{-6}$. Studies by Brilliant[17] show that a significant number of T-facilities might not, therefore, meet the DDS specification on error-free seconds.[18,19] The DDS solves this problem by selecting only those lines that pass an acceptance test.

If dataport were to require T-facility line selection, the goal of quickly installing a channel unit to meet new customer data needs would be severely impaired; thus, error correction was incorporated as a standard feature for dataport.

To ensure proper service quality, the common equipment of the D4 bank declares the facility out of service and issues a "carrier group alarm" when the short-term error rate is worse than 10^{-3}. Hence, $p = 10^{-3}$ was chosen as the worst-case operating error rate. An error-correction strategy was required to decrease the error rate from 10^{-3} to 10^{-8} or lower, assuming a binary symmetric channel model.

6.1 Encoding and decoding

As we saw earlier, in the transmit direction a 9.6-kb/s OCU dataport takes six customer data bits, and adds both a leading zero and the network control bit to form an 8-bit byte. Next, the OCU repeats the byte five times to build up the data rate to 64 kb/s. For 2.4 and 4.8 kb/s, the 8-bit bytes are repeated 20 and 10 times, respectively. Since a repeat of 10 can be regarded simply as two repeats of five and a repeat of 20 as four repeats of five, the OCU can be regarded as a repeat-of-five encoder.

At the receiver, the five repeated bytes are decoded into the correct message byte one bit at a time. If no errors have occurred, each of the

received five repeats of each bit in the byte will be the same. When they are not received correctly, it can be shown[20] that taking a majority vote on the five bits is the maximum likelihood method of making the correct decision. This majority vote scheme is implemented in the subrate dataports and is performed on each of the bit positions in the received byte. While more efficient coding schemes can be devised, this method is a natural outgrowth of the DDS subrate nonmultiplexed signal format. For multiplexed OCU channels on one time slot, the methods described in Ref. 2 may be used.

Since the rule for recovering each information bit is to take a majority vote of the five received bits, a decoding error is made only if three or more line errors are made. Hence, the probability of bit error after decoding is given by:

$$P_r = \sum_{i=3}^{5} \binom{5}{i} p^i (1-p)^{5-i}, \tag{1}$$

where p is the bit-error probability of the channel and satisfies $p \leq 10^{-3}$, as explained earlier.

Equation 1 is approximately equal to:

$$P_r \approx 10\, p^3 \text{ for } p \ll 1 \tag{2}$$

$$\leq 10^{-8} \text{ for } p \leq 10^{-3}. \tag{3}$$

Thus, for a line error rate of 10^{-3}, the dataport error rate is reduced to less than 10^{-8}.

6.2 Word synchronization

At the receiver, no clock signal is available to mark the start of the five repeated bytes. A word marker must be formed from the statistics of the data. As we see in Fig. 11, the word marker is synchronized when the six data bits of the first byte and the six of the fifth byte are the same. When not synchronized, the first and fifth bytes represent different data bytes from the customer and should be different with high probability. The synchronization algorithm loads in five bytes T_1 times and compares the six data bits of the first byte with the six data bits of the fifth byte. If the number of times the first and fifth byte patterns are different exceeds a threshold T_2, then a mis-synchronization is declared, and a byte slip of the word marker is made as corrective action. A slip in the same direction will be introduced every T_1 trials until synchronization is achieved.

6.3 Probability of false mis-synchronization

Mis-synchronization is declared whenever more than T_2 cases of mismatch occur between the first and fifth byte in T_1 trials. Since the probability p_1 that a bit of the first and fifth byte is the same is the

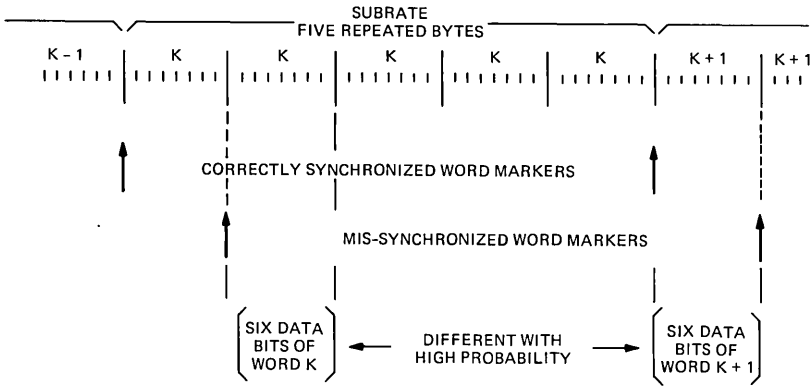

Fig. 11—Error-correction synchronization.

sum of the probabilities of no error either time and an error both times,

$$p_1 = (1-p)^2 + p^2 = 1 - 2p + 2p^2, \tag{4}$$

where p is the probability of a bit error on the T-facility. The probability, p^*, that when properly synchronized the six data bits of the first byte will not match the six data bits of the fifth byte, is given by:

$$p^* = 1 - p_1^6 \approx 12p \text{ for } p \leq 10^{-3}. \tag{5}$$

Hence, the probability, P_F, of false mis-synchronization for this Bernoulli experiment is:

$$P_F = \sum_{i=T_2}^{T_1} \binom{T_1}{i} (p^*)^i (1-p^*)^{T_1 - i}. \tag{6}$$

6.4 *Probability of failure to recognize mis-synchronization*

A failure to recognize mis-synchronization occurs whenever in T_1 trials fewer than T_2 mismatches occur between the assumed first and fifth bytes of the repeating pattern. If we assume two 6-bit customer bytes, a similar Bernoulli experiment can be conducted. Hence, the probability, P_M, of failure to recognize mis-synchronization is given by:

$$P_M = \sum_{i=0}^{T_2 - 1} \binom{T_1}{i} \left(\frac{63}{64}\right)^i \left(\frac{1}{64}\right)^{T_1 - i}. \tag{7}$$

For the error-correcting circuit of the subrate dataports, $T_1 = 160$, and $T_2 = 20$. This results in $P_F = 10^{-12}$ while $P_M = 10^{-195}$. Keeping the probability of failing to recognize a mis-synchronization so low with respect to falsely declaring a mis-synchronization was done to guard against customer data that was not independent. An expanded discussion of the above algorithms can be found in Ref. 21.

VII. ON-BOARD POWER CONVERTER

The dataport units have much more logic circuitry than do normal D4 channel units. The standard D4 bank power converter supplies +5V, +12V, and −12V to each channel,[3] but has a limited current drain allocation. The dataport units require hundreds of milliamperes to run the NMOS LSI devices. To avoid changing the standard bank converter, an on-board dc-to-dc converter was designed onto each dataport to supply the current. This converter uses power from the ample −48V office battery used in regular channel units to power the customer voice loop.

The dc-to-dc converter develops a reference voltage from the −48V office supply and regulates a series pass transistor. The output of the transistor is chopped and fed to a transformer, where two sets of taps are used to obtain +5V, +12V, and −12V. An output filter on each voltage supply keeps the noise down to a few tenths of a volt. The total maximum output power of the converter is over six watts.

VIII. CONCLUSION

Dataport has been designed as an easy, inexpensive way to expand the area served by the Digital Data System. It can be quickly installed into a properly conditioned D4 bank and has all the normal DDS maintenance features. The error-correction ability of the dataport removes the need to select T-carrier facilities to achieve error objectives. Dataport is lower in cost for small numbers of customers than is conventional DDS equipment, and it allows economical voice and data sharing of digital terminals, achieving efficient T-facility usage.

IX. ACKNOWLEDGMENTS

We would like to thank W. D. Farmer for his guidance with the existing DDS; O. Barrimond, who developed the power converter; R. E. Sheehey, who worked on the OCU analog circuits; R. M. Goldstein, and H. C. Poon, A. R. Ross, and A. A. Mammele, who guided our LSI development. We would also like to thank W. P. Frawley, who did our physical design; and R. E. Anderson, who managed our designs in production and field evaluation.

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D4 Digital Channel Bank Family:

Dataport—Channel Units for Digital Data System 56-kb/s Rate

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(Manuscript received July 6, 1981)

Increasing demand for high-speed data services makes it desirable to give more customers access to the Digital Data System (DDS). To provide service at 56 kb/s, the highest DDS rate, "dataport" channel units have been developed to extend DDS network channels over T-carrier lines, using D4 terminals. These 56-kb/s dataport units offer a flexible and economical arrangement for serving smaller cross sections of data subscribers, and make use of a coding scheme for error correction that makes special selection of lines (for error rate) unnecessary. We describe the design of 56-kb/s dataport units, while articles referenced herein discuss dataport system questions and the design of lower speed dataport units.

I. INTRODUCTION

Consider the use of existing T-carrier facilities to extend the Digital Data System (DDS) serving area. "Dataport" channel units are needed for the carrier terminals (such as D4 channel banks) to insert customer data bit streams into the carrier pulse code modulation (PCM) bits tream. Special problems must be addressed with 56-kb/s service; hence, dataports for this speed are treated separately from those for subrate speeds.

Field studies of the performance achieved by T-carrier facilities[1] indicate that a significant number of them , if used to carry DDS channels, will fail to meet an *overall* quality objective of 99.5-percent error-free seconds. T-carrier lines are designed and engineered for a

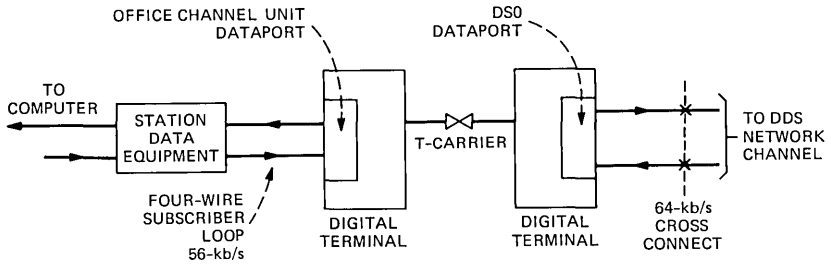

Fig. 1—Basic dataport application.

bit error rate of around 10^{-6} for 95 percent of the systems. This is more than adequate for voice grade services. Major alarms do not appear until the error rate has increased to approximately 10^{-3}. A much lower error rate must hold to support DDS channels for data transmission; Ref. 2 states that the T-carrier line should appear to have at least 99.6-percent error-free seconds (EFS), and an error rate closer to 10^{-8} is needed to insure this. The 56-kb/s dataports use an error-correcting code that translates an error rate of 10^{-3} to an effective error rate on the order of 10^{-8}. Thus, even a barely functioning T-carrier facility should perform adequately as part of a DDS channel, using dataport channel units with error correcting features. In general, the penalty paid for using of error-correcting codes is the need for additional bandwidth. In the case of 56-kb/s DDS transmission, the data and control information[3] occupies the full usable capacity (64 kb/s) associated with the PCM channel time slot. To gain capacity for error correction, a full extra time slot must be used, since borrowing partial capacity would make that carrier channel unusable for normal service in any case. This dictates that the code will have a rate of one-half (the ratio of information bits to total transmitted bits).[4]

With these considerations in mind, let us look at what a dataport for the 56-kb/s rate must be able to do. It must provide those functions which DDS hardware would perform, while ensuring that the carrier facility will meet error-rate requirements. Consider the simplest dataport application, shown in Fig. 1.[5] The DDS network furnishes a channel, working at 64 kb/s ("DS0" rate) to a D4 terminal. A "56-kb/s digital signal zero (DS0) Dataport" conditions this signal for insertion into the digital signal one (DS1) bit stream, which is transmitted over the digital line to the far terminal. At this point, the "56-kb/s Office Channel Unit (OCU) Dataport" removes the signal from the DS1 stream and performs the rate conversions necessary for transmission to the station at the subscriber bit rate. (Reference 6 discusses synchronization to the DDS network clock.) There are several "building block" functions to be implemented (see Fig. 2). Working

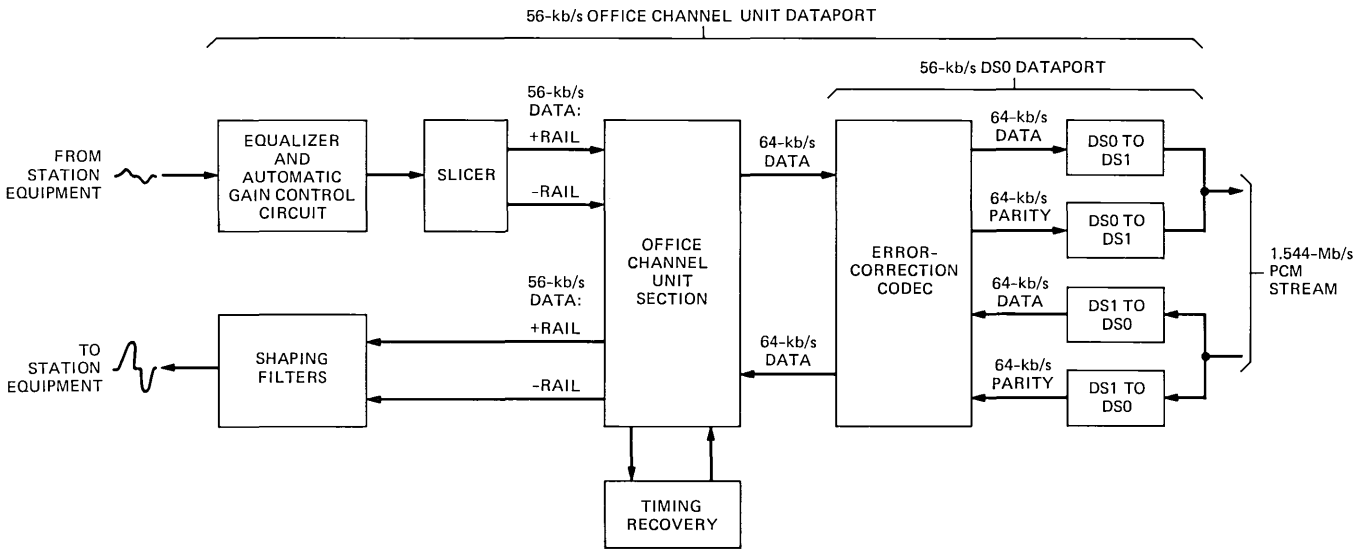

Fig. 2—56-kb/s dataport functions.

from the station toward the network, the pulses arriving from the customer premises equipment must be equalized and amplified to compensate for the loss and dispersion of the cable. The slicer returns the pulses to digital-logic-level signals, and the timing recovery circuit samples the bits and retimes the data. The "office channel unit" section (terminology from DDS[7]) builds the 56-kb/s data signal into the 64-kb/s network signal format. The coding logic processes this signal to obtain the wideband, redundant signal (128 kb/s) for transmission over the carrier. The DS0-to-DS1 interface places this signal into two channel time slots on the 1.544 −Mb/s PCM stream. Transmission from network to station reverses the sense of these functions, except that in this direction filters merely shape the 56-kb/s pulses as they come from the OCU section (since timing recovery is not needed).

Thus, the "56-kb/s DS0 dataport" is implemented with only the error correction and "DS0-to-DS1" blocks, while the "56-kb/s OCU dataport" requires all of the Fig. 2 blocks. Designs for these basic building blocks involve techniques from many fields. Linear and nonlinear "analog" circuits are needed, as well as sequential and combinational digital functions; information theory must be called in as well to implement the error-correction code. Let us look at the building blocks in more detail, progressing from the station equipment toward the DDS network.

II. SUBSCRIBER LOOP INTERFACE

The station uses standard DDS equipment, such as the channel service unit (CSU) or the data service unit (DSU).[7] Figure 3 depicts the dataport line circuits for station-to-network transmission. This circuitry processes pulses arriving from the subscriber loop at 56 kb/s. The second-order filter is in series with a first-order low-pass filter in the network-to-station link, forming a third-order Butterworth low-pass filter with a cutoff frequency 1.3 times the signaling rate. These filters are used to increase noise immunity and to provide pulse shaping.

The local loops are metallic wire pairs of various gauges; their insertion loss is a function of frequency, length, and environmental conditions. An adaptive equalizer compensates for the resultant shaping; it has a variable flat gain and a movable real zero, controlled by the variable resistance of a junction field-effect transistor (FET). Feedback keeps the peak amplitude of the equalized signal at a fixed level at the input to the slicer, this being the ±1.5V pulse amplitude transmitted from network to station.[7] The slicer acts as a comparator with a reference at one half the pulse amplitude, hard-limiting the rectified signal to logic "one" or "zero". This makes it suitable for digital processing. Logic ones retain their identity as having been

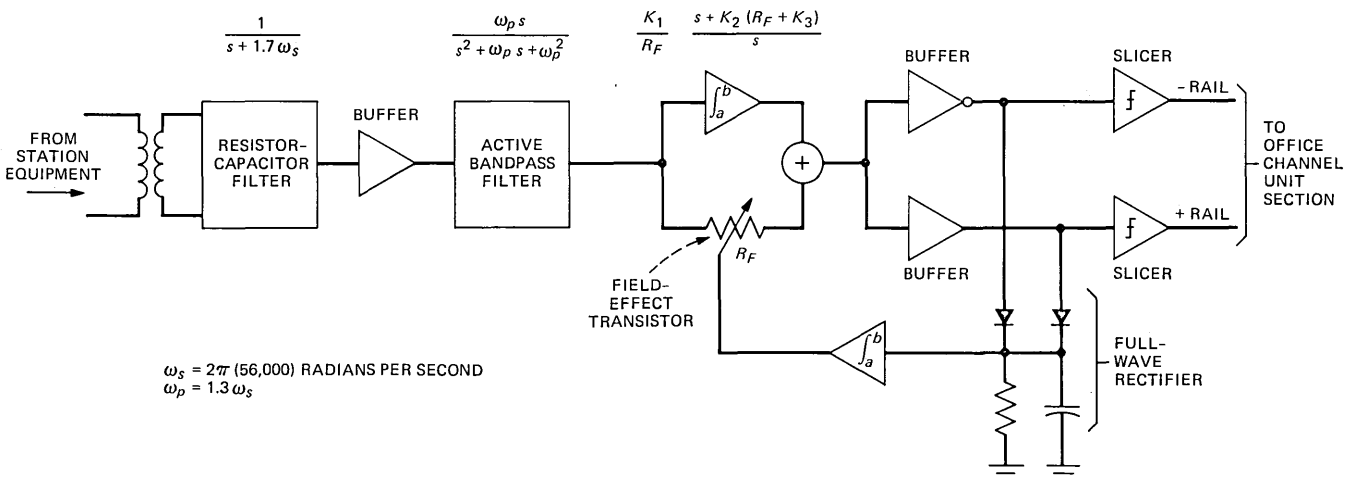

Fig. 3—Station-to-network equalizer and slicer.

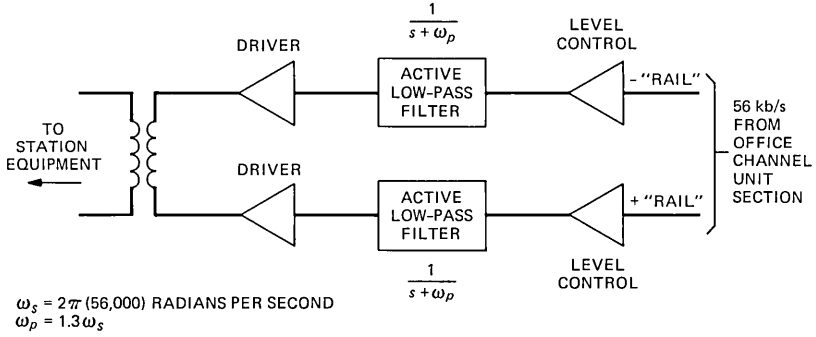

Fig. 4—Network-to-station shaping circuit.

positive or negative pulses by the use of two separate "rails" or leads. In this way, violations of the bipolar encoding rule can be detected.

In the network-to-station direction, data arrives at 56 kb/s from the OCU section, having the aforementioned dual-rail format. Figure 4 shows this circuitry. The level shifter converts the transistor-transistor logic (TTL) signal to a fixed voltage level, appearing as a voltage source to the filters. The line drivers isolate the filters from the variable line impedance and drive the dual-rail signal into the transformer, producing the bipolar signal for transmission over the cable pairs.

Parts of the filter and equalizer circuitry are combined within transmission equipment dual in-line packages (DIPs), known as TEDs.[8] The use of TEDs reduces in large measure circuit size and cost, owing to simpler testing and assembly procedures.

III. TIMING RECOVERY

The DDS network and subscriber loop signals are synchronized in frequency, that is, the 56-kb/s loop pulses occur at exactly seven-eighths the rate of the 64-kb/s network signal. However, since the loop has a variable propagation delay, bits arriving from the station data equipment have unknown "*phase*." This timing must be recovered to ensure that the sampling instants occur at the center of each bit interval.

The 56-kb/s dataport has a 5.376-MHz clock that is phase-locked to the 64-kHz network bit clock. This frequency divides by 96 to yield 56 kHz. By momentarily adjusting the divisor to 95 or 97, the phase of the 56 kHz is advanced or retarded by (1/5.376 MHz)/(1/56 kHz) = 1.04 percent (3.75°). A phase comparator views the data relative to the assumed 56-kHz recovered clock to determine when to change the divisor. The comparator translates this phase difference into a voltage, which is applied to a pair of threshold detectors having a reference

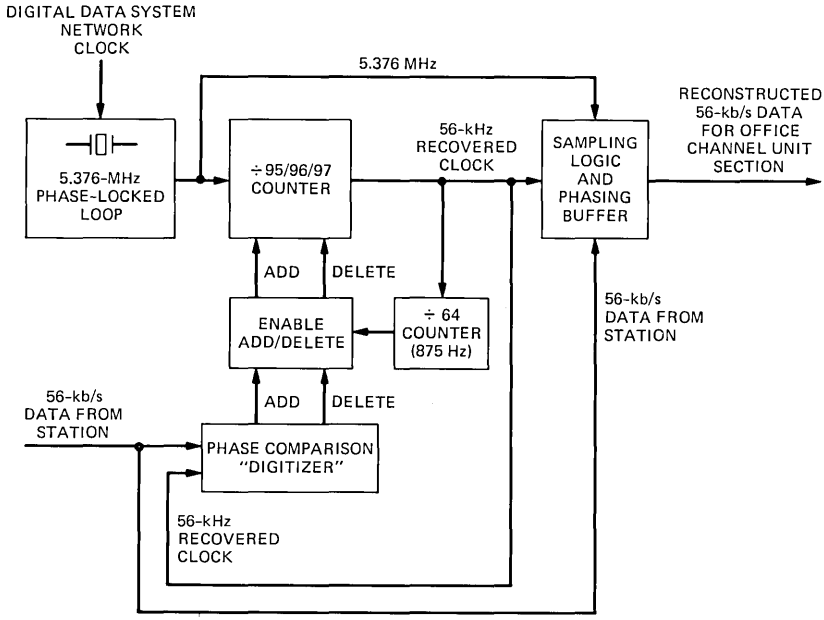

Fig. 5—Timing recovery.

corresponding to approximately four degrees of phase difference. A digital command to add or delete a 5.376-MHz cycle from the present "56-kHz" recovered clock is generated if there are more than eight degrees of phase error. To limit its responsiveness to noise, the system can make only one phase correction for every 64 recovered clock periods (875-Hz maximum correction frequency). Figure 5 summarizes this function. This timing recovery section is, in effect, a "digital" phase-locked loop.

IV. OFFICE CHANNEL UNIT SECTION

The Office Channel Unit (OCU) section provides bidirectional rate conversion between the 56-kb/s subscriber loop signal and the DS0 (64-kb/s) signal and monitors the data stream for control information.[7] The OCU circuitry processes the serial data stream on a byte-by-byte basis, using the DDS bit and byte clocks. This byte structure remains transparent to the customer.

Data on the subscriber loop appears as shaped pulses in a bipolar format. Bipolar encoding ensures that successive data "ones" appear as alternate positive and negative pulses, and "zeros" appear as the absence of pulses during the signaling time interval. Control information is indicated by bipolar "violations", that is, two successive pulses of the same polarity.

Table I—OCU XOV codes in the DS0 to local loop direction

Control DS0 Codes		Name	Definition	Local Loop Code	
*b0**	*b1b2b3b4b5b6b7*			*d0*	*d1d2d3d4d5d6*
Ø	0000001	ZS	Zero Suppression	*b*0	000*X*0*V*
Ø	0011ØØ0	OS	Out of Service	*b*0	001*X*0*V*
0	0101100	LB	Loopback Code	0	010*X*0*V*
Ø	0111ØØ0	TIFP	T1DM Framing Pattern	*b*0	011*X*0*V*
Ø	1001010	—	Reserved	*b*0	100*X*0*V*
Ø	1011010	—	Reserved	*b*0	101*X*0*V*
Ø	1101010	—	Reserved	*b*0	110*X*0*V*
Ø	1111ØØ0	IDLE	IDLE	*b*0	111*X*0*V*
Ø	0101010	OCU	LB	0	010*X*0*V*
Ø	0101000	Channel	LB	0	010100†
Ø	0101100	DSU	LB (DSU on cust. prem.)	0	010*X*0*V*
Ø	0101100	DSU	LB (CSU on cust. prem.)	0	010110†

* The Ø is a "don't care" symbol. The DS0 and loop bits are given the names *b*0, *b*1, *b*2, ···, *b*7, and *d*0, *d*1, *d*2, ···, *d*6, respectively.
† dc sealing current is reversed.

The transmit (station-to-network) circuitry collects seven data bits at a time and appends a "one" in the eighth bit position (to indicate a data byte). The resultant eight-bit byte is clocked out at 64 kb/s, the eighth bit being marked by the DDS byte clock.

Detection of bipolar violations causes a mapping of the loop form of a control code to its appropriate DS0 code (see mapping, Table 1), identifiable by a "zero" in the eighth, or control bit position. Loop-side control codes, containing the violations, are seven bits in length.[7] These seven-bit groups may not correspond with the groups being stuffed into DS0 bytes (that is, byte boundaries may not "align" in time). For continuous data, this is of no consequence, but unknown alignment is important when switching between data and control modes. The OCU section assures the transmission of the last bits of customer data, at the expense of loss of the first few (up to six) bits following a control code.

The receive (network-to-station) logic circuitry retimes and reformats the DS0 data stream to 56 kb/s for the loop. Bytes collected are checked for valid control codes. Non-zero data and invalid control codes are encoded into a bipolar pulse sequence. All-zeros data and valid control codes are mapped into their appropriate prefix and a suffix (designated by *X*0*V*),* which will generate a bipolar violation (see Table II).

* This suffix represents three bits; '*V*' is a logic one transmitted in violation of the alternating sign (bipolar) rule; '0' is a logic zero; '*X*' is a bit transmitted according to the normal bipolar rule, chosen to be logic 'one' or 'zero' to ensure that consecutive '*V*' bits occur with alternating signs.

Table II—OCU code map in the local loop to DS0 direction

Label	Loop Code		Second Generation OCU DS0 Code	
	*d*0*	*d*1*d*2*d*3*d*4*d*5*d*6	*b*0	*b*1*b*2*b*3*b*4*b*5*b*6*b*7
ZS	∅	000*X*0*V*	*d*0	0000001
CA	∅	001*X*0*V*	*β*†	0010010
LB	0	010*X*0*V*	0	0100001‡
CB	∅	011*X*0*V*	*β*	0110010
—	∅	100*X*0*V*	*β*	1000010
—	∅	101*X*0*V*	*β*	1111010
—	∅	110*X*0*V*	*β*	1101010
IDLE	∅	111*X*0*V*	*β*	1111110
No Local Loop Signal§			*β*	0011110

* The ∅ is a "don't care" symbol.

† The *β* symbol indicates a "1" for 56-kb/s service. The *b*0 bit is the *d*0 bit if a customer multiplex option is used, and the network and loop byte boundries align.

‡ The 1 in *b*7 is fixed, but the other 1 can appear anywhere in *b*0 → *b*6, depending on relative alignment of loop and network bytes. If a customer remote test option is used and we are *not* already in a network-commanded loopback, then the 0010*X*0*V* code will be mapped into 00101100 (DSU loopback) to cause a loop on the far-end station equipment.

§ If the OCU receives no signal from the local loop during an interval of time (approximately two seconds), then the indicated code is placed on DS0.

The OCU section interprets certain loopback codes for standard DDS maintenance features. Receipt of "OCU loopback" connects the transmit and receive directions on the loop side, sending the bit stream back toward the network. The "Channel loopback" reverses the polarity of the dc loop sealing current (which is normally circulated through the cable pairs to reduce splice resistance), resulting in a loopback at the loop interface of the station equipment. The "Data Service Unit (DSU) loopback" sends a code recognized by the station equipment and initiates a loop on the side remote from the network (i.e., at the customer interface). Reference 7 discusses in more detail the subscriber loop signal formats, standard DDS loopback commands, and violation coding.

V. ERROR CORRECTION

It has been mentioned that field studies show a need for some form of error correction in the 56-kb/s dataport to ensure that objectives for error performance will be met using any working T-carrier facility. Since voice quality service over T-carrier is reasonably adequate up to error rates near 10^{-3}, major alarms do not appear until the error rate has gone above this threshold. For data transmission, an error rate approaching 10^{-8} is desired. This is a conservative result, based on the error-free second requirements for DDS channels. In the 56-kb/s data-

ports, the error-correcting code allows one to translate a "raw" facility error rate around 10^{-3} to an effective error rate closer to 10^{-8}. Thus, channels of any T-carrier facility that is not in a major alarm condition should, using dataports with error correction, perform adequately as part of a data circuit. The next paragraphs give an overview of the encoding and decoding algorithms used to implement error correction using two 64-kb/s channels. Some background in coding has been assumed.

5.1 Encoding

The (17,9) BCH* code generated by the polynomial

$$g(x) = 1 + x^3 + x^4 + x^5 + x^8, \tag{1}$$

is chosen. Forcing the ninth data bit of the (17,9) code to a zero and not transmitting it shortens the code to a (16,8) code.

If the eight data bits to be encoded are given by

$$\{a_0, a_1, \text{————}, a_7\},$$

define the polynomial $a(x)$ as,

$$a(x) = a_0 + a_1x + \text{——} + a_7x^7. \tag{2}$$

Then, define the parity polynomial $p(x)$ as:

$$p(x) = x^8a(x) \bmod g(x), \tag{3}$$

the right-hand side of which means the remainder left when $x^8a(x)$ is divided by $g(x)$. Since there are eight parity bits for eight data bits, the parity rate is also 64 kb/s, enough to fit into a channel time slot.

It can be shown that the natural length[4] of the polynomial $g(x)$ is 17, i.e., 17 is the smallest integer i such that

$$x^i \bmod g(x) = 1. \tag{4}$$

Hence, it can be shown[4] that the code word

$$c(x) = p(x) + x^8\, a(x) \tag{5}$$

is an element of a cyclic code. For this particular $g(x)$, the cyclic code is a 2-QP (Quasi-Perfect)[4] BCH code and is, hence, optimum for the numbers (17, 9).

In general, $p(x)$ can be generated by feedback shift registers,[4] but can also be generated by a combinational network using the following result:

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* Bose-Chaudhuri-Hocquenghem (BCH) codes are a class of cyclic codes discovered in 1959–60. The designation (n, k) for a binary code indicates that an n bit codeword is transmitted for every k data bits encoded.[4]

$$p(x) = x^8 a(x) \bmod g(x)$$
$$= \sum_{i=0}^{8} a_i x^{8+i} \bmod g(x). \tag{6}$$

Noting that $a_8 = 0$ in this case, and expanding $x^j \bmod g(x)$, for $j = 8, 9, \cdots, 16$, after suitable manipulation,[9] eq. (6) becomes

$$\begin{aligned} p(x) = {} & (a_0 \oplus a_3 \oplus a_4 \oplus a_5 \oplus a_6) && + \\ & (a_1 \oplus a_4 \oplus a_5 \oplus a_6 \oplus a_7)x && + \\ & (a_2 \oplus a_5 \oplus a_6 \oplus a_7)x^2 && + \\ & (a_0 \oplus a_4 \oplus a_5 \oplus a_7)x^3 && + \\ & (a_0 \oplus a_1 \oplus a_3 \oplus a_4)x^4 && + \\ & (a_0 \oplus a_1 \oplus a_2 \oplus a_3 \oplus a_6)x^5 && + \\ & (a_1 \oplus a_2 \oplus a_3 \oplus a_4 \oplus a_7)x^6 && + \\ & (a_2 \oplus a_3 \oplus a_4 \oplus a_5)x^7, \end{aligned} \tag{7}$$

where $\oplus$ denotes binary addition (EXCLUSIVE OR).

Finally, the data sequence $\{a_0, a_1, \cdots, a_7\}$ has the standard DDS zero code suppression performed upon it, if desired, prior to encoding. The parity sequence, $p(x)$, never needs zero code suppression, as the only data sequence that can result in an all-zero parity sequence is the all-zero data sequence, which is not allowed to occur.

5.2 Decoding

When the code word $c(x)$ of (5) is transmitted, suppose one receives

$$r(x) = c(x) \oplus e(x), \tag{8}$$

where $e(x)$ is the error polynomial. Then error correction essentially consists of making a maximum likelihood decision on $e(x)$. This operation, called decoding, is generally the most difficult aspect of error correction. To begin decoding, $r(x)$ is used to form a remainder polynomial $s(x)$, the "syndrome" of $r(x)$:

$$s(x) = r(x) \bmod g(x). \tag{9}$$

Reference 9 develops a simple technique for decoding the (17,9) BCH code using memoryless decoding and "chains" of syndromes. Figures 6 and 7 define a decoder structure that is shown to be maximum likelihood.[9] In our context, notice that the sixteen received bits (eight data and eight parity) form a code word in the (16,8) shortened cyclic code described earlier. A zero is added as the ninth data bit, and the decoder of Fig. 6 decodes the received word as if it were a code word in the (17,9) BCH code described earlier. It should be noted that when the D4 bank framer recognizes a misframe situation or when a major alarm is raised, the decoder creates an "Out of Service" control code for the subscriber loop.

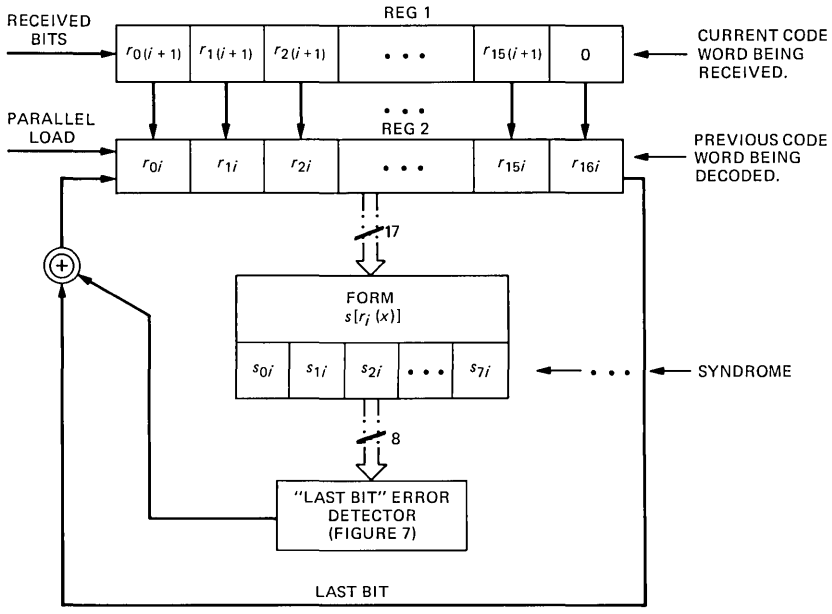

Fig. 6—An implementation of memoryless coding.

5.3 Performance

Given that the (17,9) BCH code is 2-QP and using the decoding strategy outlined in the previous section, the reader can verify that for the (16,8) shortened code the correctable subset consists of the:

(*i*) All-zero pattern

(*ii*) 16 single-error patterns,

(*iii*) $\binom{16}{2} = 120$ double-error patterns

(*iv*) $2^8 - 1 - 16 - \binom{16}{2} = 119$ triple-error patterns.

Thus, the probability of "word" error after error correction is given by

$$P_{we} = \left\{\binom{16}{3} - 119\right\} p^3(1-p)^{13} + \sum_{i=4}^{16} \binom{16}{i} p^i (1-p)^{16-i}, \quad (10)$$

where p is the raw error rate of the T-carrier facility, treating it as a binary symmetric channel.

For $p \leq 10^{-3}$ one finds that

$$P_{we} \doteq 441p^3. \quad (11)$$

Now, words occur at the rate of 8000 per second; and hence the

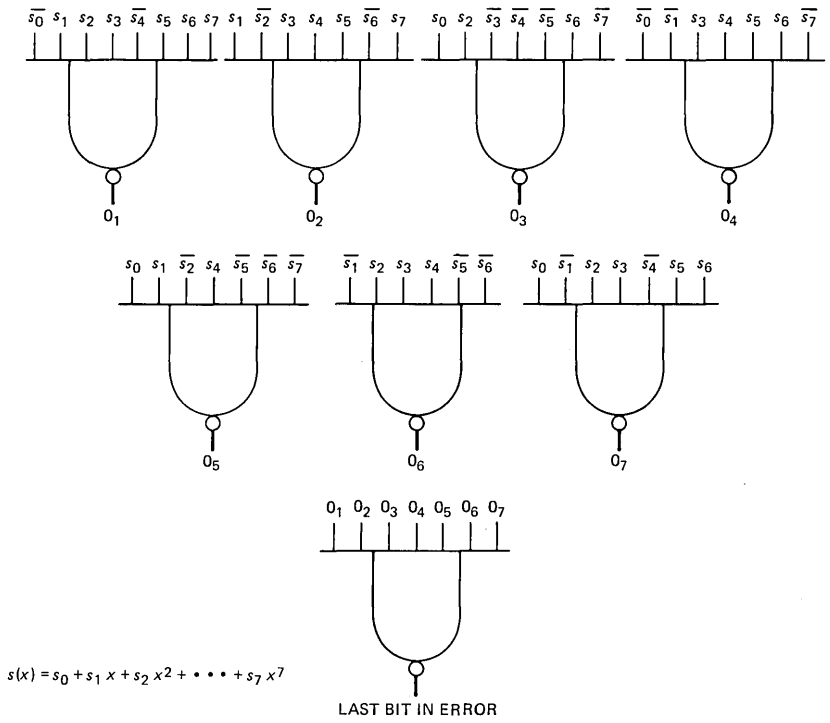

Fig. 7—A realization of the "last bit" error detector.

probability of an error-free second (EFS) is given by

$$P[\text{EFS}] = (1 - P_{we})^{8000}. \tag{12}$$

To compute the effective *bit* error probability, P_e, that will yield the same error-free second count, realize that since data bits occur at 64 kb/s,

$$P[\text{EFS}] = (1 - P_e)^{64000}. \tag{13}$$

Finally, from eqs. (11) through (13),

$$P[\text{EFS}] \doteq (1 - 441p^3)^{8000} = (1 - P_e)^{64000}$$
$$P_e \doteq 56p^3 \quad \text{for} \quad p \leq 10^{-3}. \tag{14}$$

Thus, an error rate of 10^{-3} gets translated to an effective error rate of 5.6×10^{-8}. Substituting this result into (13) yields $P[\text{EFS}] = 0.9964$, or 99.64-percent error-free seconds.

VI. DS0 to DS1 INTERFACE

The DS0 to DS1 interface accepts the two eight-bit words from the coder at 64 kb/s. Each of these words is loaded into a three-register elastic store arrangement identical to the subrate case.[5] The circuitry utilizes the channel sequencing information by which the terminal accepts pulse amplitude modulation (PAM) samples from each voice channel. When the sampling time for the dataport occurs, the unit inserts the longest held eight-bit word from the elastic store into the PCM stream at 1.544 Mb/s. The second eight-bit word (parity) is inserted into a subsequent channel. A counter, using the 1.544-MHz bit clock, determines when the parity word will be inserted, thus allowing that only the first physical channel need be occupied by the dataport unit. The channel position associated with the parity time slot need merely be left unoccupied (or filled with a dummy channel unit). Since each pair of eight-bit words is clocked simultaneously into the elastic store registers from the coder section, each sequential pair that is put within a given DS1 frame corresponds to a 16-bit word from the (16,8) code book. Receiving the data and parity channel from the PCM stream reverses the techniques used when transmitting. Clearly, the time slots used for data and parity must be the same as those selected at the far-end terminal.

VII. PLUG-IN CHANNEL UNITS

Figure 2 groups the functional blocks into two different plug-in channel units for the D4 terminals. The 56-kb/s DS0 dataport includes the two-channel DS0-to-DS1 interface and the algebraic coder for error correction. As such, it serves to place a single DS0 data source into the DS1 stream as one channel or two channels (when the encoding for error correction is used). This interfaces the DDS-format DS0 signals with standard T-carrier. Since the code acts over the entire 64-kb/s time slot, it should be noted that the input data could be multiplexed subrates, the DS0-B signal described in Ref. 3. The 56-kb/s DS0 dataport could be used to provide error correction in this case. The four-wire DS0 input passes through an access point on a faceplate jack, so that testing or loopback is possible at the channel unit, if needed. Driving circuitry for the DS0 office cabling is identical to that used in the subrate DS0 dataport.[5]

The 56-kb/s OCU dataport is more complex and includes all of the Fig. 2 functions; thus, it includes an entire 56-kb/s DS0 dataport as a subset. The 56-kb/s OCU dataport serves a DDS engineered loop,[7] interfacing the loop format with the DS0 format and then with the standard T-carrier. The DS0 signal passes through an access point on the channel unit, enabling access to the midpoint of the circuitry. It is possible to test toward the loop, or near end, or toward the carrier, or

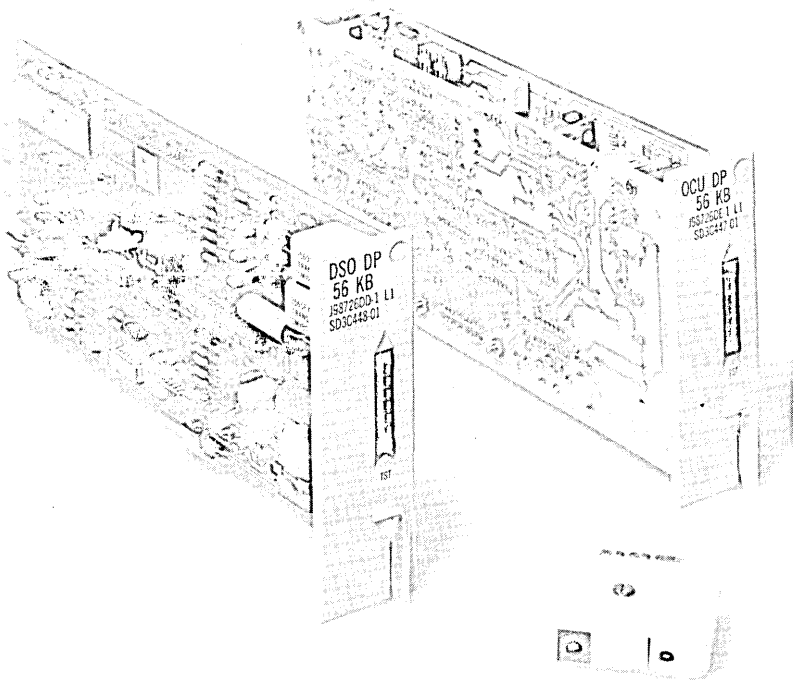

Fig. 8—The 56-kb/s DS0 and 56-kb/s OCU dataports, shown with a test/loopback plug.

far end. A DDS hub office test board[10] may also initiate network loopbacks.

The current available from the channel bank power converter is not sufficient to supply a full bank of dataport channel units or a full mix of dataports and voice units. Consequently, each dataport unit has a dc power supply, fed by the -48 volt office battery. This dc supply is identical to the one used in the subrate dataports.[5]

The units are physically interchangeable with other voice channel units (see Fig. 8, which also shows the test/loopback plug[5]). Two large-scale integrated circuit devices encompass the OCU section (with part of timing recovery) and a conjoint error-correction/DS0-DS1 section, allowing dataport functions to reside within the volume of a D4 channel unit. To serve a data customer, then, the plug-in unit is merely placed in an existing D4 terminal that has been conditioned for network synchronization using the office interface unit (OIU-2).[6] This permits the dataport approach to enjoy economic advantages.[11] Notice

that two 56-kb/s OCU dataports could also provide a *stand-alone* data link over a T-carrier system, independent of the DDS network.

VIII. CONCLUSION AND ACKNOWLEDGMENTS

The 56-kb/s dataports extend the serving area for DDS, and also create opportunities for point-to-point digital data services over existing digital facilities. This is an economical method of transmitting high-speed data over such facilities; it effects ways to keep pace with the growing market for higher bit-rate services.

The authors have drawn on many sources in the course of this work, and would like to specifically acknowledge the contributions of a few individuals not mentioned elsewhere; the aid of J. Kane, J. K. Keller, S. Just, and N. A. Makatenas was indispensable in the design and testing of large-scale integrated devices; W. D. Farmer, G. P. Brooks, and J. D. Roscoe made invaluable contributions to the OCU, timing recovery, and line interface sections. T. J. Lee lent timely support in the study of system performance questions. We have also drawn upon earlier information from the DDS designers.

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D4 Digital Channel Bank Family:

Digital Terminal Physical Design

By W. G. ALBERT, A. G. FAVALE, J. R. HALL, and D. H. KLOCKOW

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This article describes the physical design of the D4 and related SLC™*-96 subscriber loop carrier system digital terminals. A detailed description of the bay, channel bank, and plug-in designs is also included, along with other very important considerations such as thermal design, manufacturability, and the effective use of hybrid integrated circuit technology. The D4 was designed as a system that was significantly smaller, used less power, and had a lower cost than previous digital terminals. These objectives were realized by using the latest technology and the optimal physical design format. Since these are relatively high-production terminals, the basic design has been aggressively reduced in cost and has proliferated with expanding D4 and* SLC-*96 subscriber loop carrier terminal capabilities, lightguide applications, and the use of the D4 hardware in other systems.*

I. INTRODUCTION

In 1962 the D1 channel bank, the voice-frequency (VF) pulse code modulation (PCM) terminal for the T1 carrier system, was first introduced into Commercial Exchange Office service. The 11-foot 6-inch central office bay framework contained equipment for 72 voice channels (three 24-channel banks). Discrete, solid-state technology was used and the typical power consumption was about 7.5 watts per channel.

In 1969 the D2 channel bank was introduced into service for Toll Office applications. Equipment for 96 voice channels (four 24-channel banks) was mounted in a bay. In addition to discrete solid-state

technology, some thin film was used and a typical power consumption of about 6.2 watts per channel was dissipated.

In 1972 the D3 channel bank was first introduced into service. This bank served both Exchange and Toll applications and essentially replaced the D1 and D2 banks for new service. An 11-foot 6-inch bay contained 144 D3 voice channels (six 24-channel banks). Small-scale integrated (SSI) circuit and hybrid integrated circuit (HIC) technologies were employed and a typical power consumption of about 2.8 watts per channel was dissipated.

In early 1977 the first D4 channel bank was cut over to regular commercial service at the Crete Office in Chicago, Illinois. The physical and electrical D4 architecture departs significantly from previous bank designs.

The D4 is a self-contained, 48-channel bank that has optimized access to the T1C system but still retains the basic 24-channel format for efficient access to T1 systems. By using higher levels of integration and modular physical design approaches, the D4 bank achieves a 2:1 size and power reduction relative to the D3 channel bank. Six D4 banks (288 channels) are mounted in an 11-foot 6-inch frame and five D4 banks (240 channels) are mounted on a 9-foot 0-inch frame. Since many new telephone buildings are built with a lower ceiling height in accordance with New Equipment Building System (NEBS) standards, a 7-foot 0-inch frame with four D4 banks (192 channels) is a standard offering. Initial shipping data shows that the 11-foot 6-inch frame accounts for about 80 percent of the D4 production, with the remaining 20 percent divided between the 9-foot 0-inch and 7-foot 0-inch frames. The evolution of the D-type channel bank bay is summarized in Fig. 1.*

II. D4 CHANNEL BANK

The D4 bank is 19 inches high by 12 inches deep and is flush-mounted on a 23-inch wide, unequal flange, duct-type bay. There are four shelves in each bank. As shown in Fig. 2, each shelf contains up to 12 plug-in channel units plus common equipment located on the left side of each shelf in the bank. Each bank is completely shop assembled, wired, and tested and contains provisions for power conversion, fusing, equalization and connections to the office alarm system.

By using different Line Interface Units (LIU) and plug-in unit reconfigurations, the following five modes of operation can easily be established, as we see in Fig. 3.

Mode 1—Offers 48-channel service over a dedicated 3.152-Mb/s facility (T1C line) with another D4 bank at the other end. In this

* Acronyms and abbreviations used in the figures are defined in the section of the same title at the back of this issue.

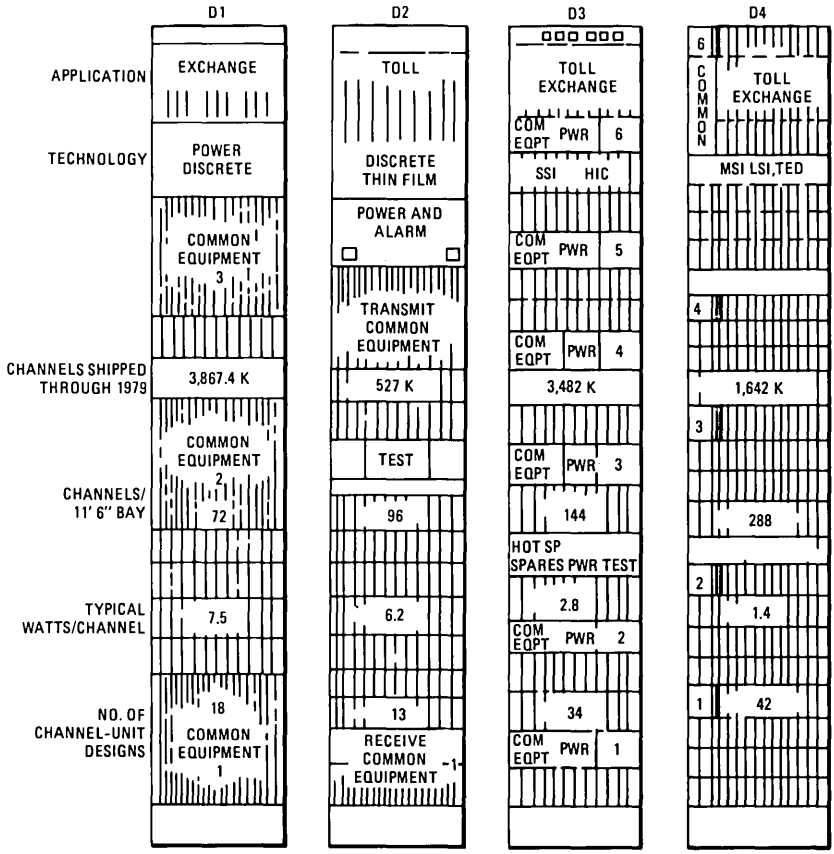

Fig. 1—D-type channel bank bay evolution.

mode, the synchronized digroups (24 channels) are interconnected to produce a unique, cost-effective, 48-channel bank with a special non-standard output signal. Alarming and trunk processing functions are administered on a 48-channel basis.

Mode 2—Provides 48-channel service over a 3.152-Mb/s facility (T1C line) with compatible digital terminals connected via an M1C multiplexer at the other end. (However, Mode 2 D4 banks could be used at both ends.) In this mode, the bank produces a signal identical to that of the M1C. Alarming and trunk processing are administered on a digroup basis. The multiplexer/demultiplexer stage of signal processing also has alarms.

Mode 3—Offers two digroups for connection to two 1.544-Mb/s facilities (T1 lines). In this mode the two separate digroups of the D4 are connected to compatible channel banks or applied to a multiplexer

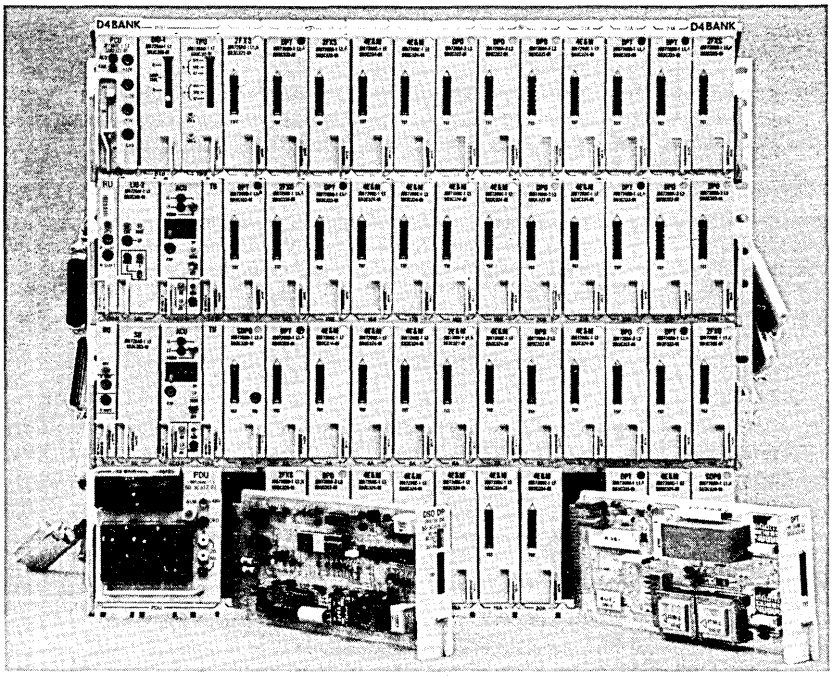

Fig. 2—D4 channel bank.

for a higher rate line. Alarming and trunk processing are administered on a digroup basis.

As shown in Fig. 3, conditioning of a D4 bank to Mode 1, 2, or 3 operation only requires inserting the correct plug-in modules. Modes 4 and 5, which essentially produce a 96-channel bank by combining the output of two banks, also require a modest amount of interbank wiring.

Mode 4—Supplies 96-channel service over a 6.312-Mb/s facility (T2 line) with digital terminals connected by means of a multiplexer at the other end (D4 Mode 4 banks could be used at both ends). In this mode, the interwired banks multiplex the four digroup outputs. Alarming and trunk processing are administered on a digroup basis.

Mode 5—Provides 96-channel service electrically similar to Mode 4 except that the 6.312-Mb/s signal interfaces directly to a lightguide line.

Clearing trouble in D4 is based on the quick replacement of plug-in units. To facilitate restoral, the D4 common units are equipped with built-in alarms. Light-emitting diodes (LEDs) are used for reliable alarm indications. A complete set of common units is shown in Fig. 4.

A common Power Distribution Unit (PDU) and Power Converter

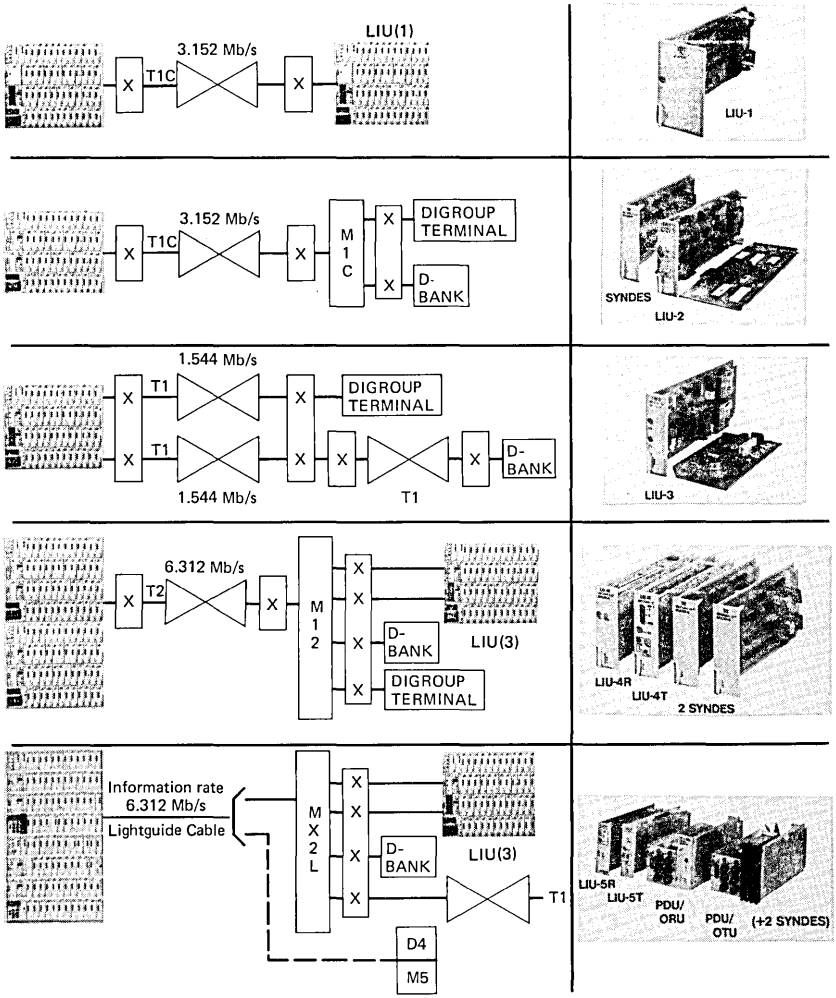

Fig. 3—D4 channel bank operating modes.

Unit (PCU) provides the filtered 48V talk battery power, the other signaling and alarm battery voltages, and ±12 and +5 volt converter power outputs. Converter input power for the common equipment and 48-channel units is about half of the D3 power requirements for 48 comparable channels. The lower D4 power needs are the result of circuit advances and use of low-power components. The channel-unit mix, activity factors, and loop lengths have a significant effect on the total power required. While digroups are largely independent, failures in those units that serve both digroups, such as the power units, are easily determined and quickly restored.

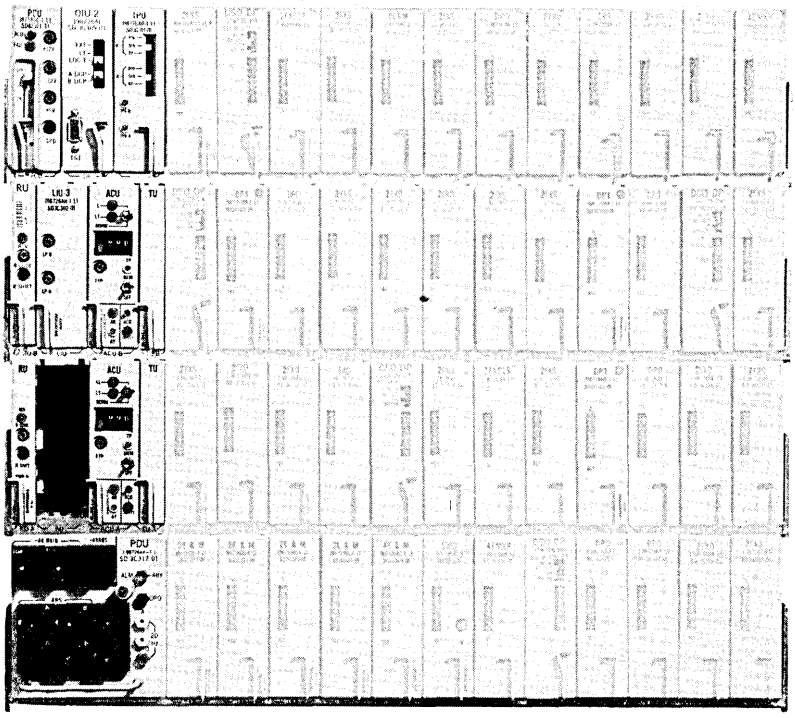

Fig. 4—D4 common units.

Transmit and receive units are provided separately for each digroup, resulting in digroup operational flexibility and independent digroup maintenance and restoral. Trunk processing control circuitry is included within the alarm unit, with trunk conditioning relays distributed in the trunk processing and channel units. Trunk conditioning is maintained during channel-unit removal.

For example, the Alarm Control Unit (ACU) shown in Fig. 5 contains lights and switches for indicating and isolating system troubles. As soon as the ACU recognizes an alarm it lights the appropriate LED, activates the office alarm, and initiates trunk processing. The alarm cutoff button silences the office alarms but maintains the alarm condition on the ACU.

A Carrier Group Alarm Counter that records the number of times the bank is out of service is visible through a window in the faceplate. The register reset switch is also accessible from the front of the ACU.

The dc-to-dc converter in the PCU (see Fig. 6) provides +5 and ±12 volts from the -48V input battery. In addition to the on/off switch,

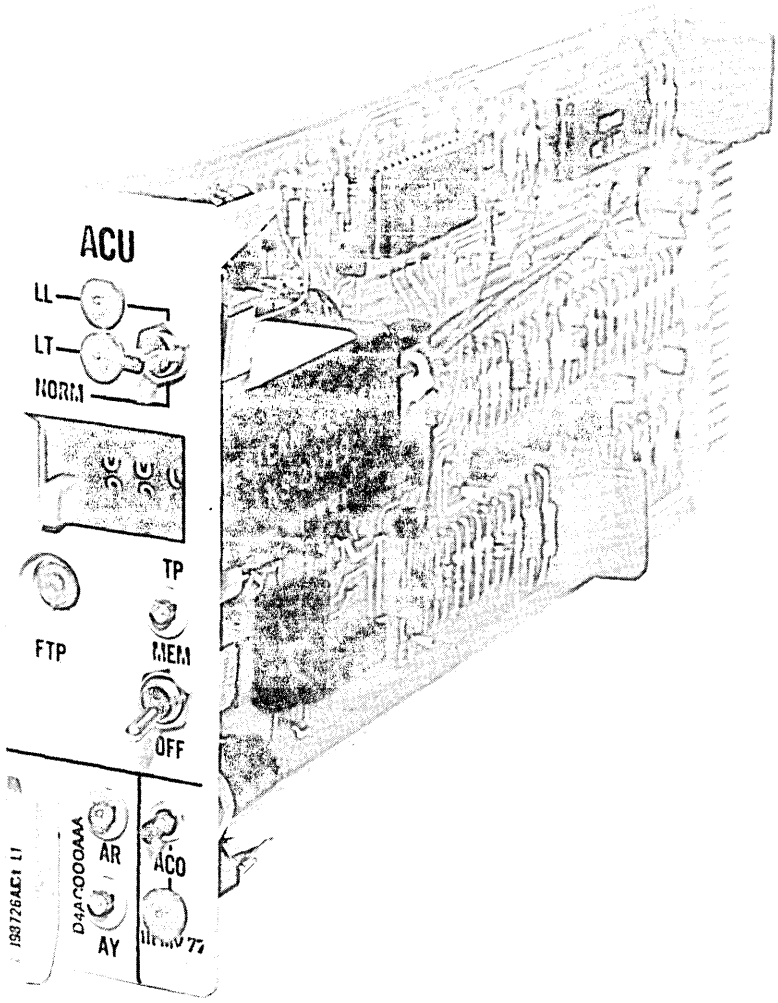

Fig. 5—Alarm control unit.

alarm lamps, and output test voltages, a mechanical interlock has been built into the latching mechanism to prevent the PCU from being plugged or unplugged with its power on. This limits the in-rush current and prevents damaging the plug-in unit or backplane connector contacts.

Over 40 different types of channel units are available to perform a wide variety of Plain Old Telephone Service (POTS) and special service

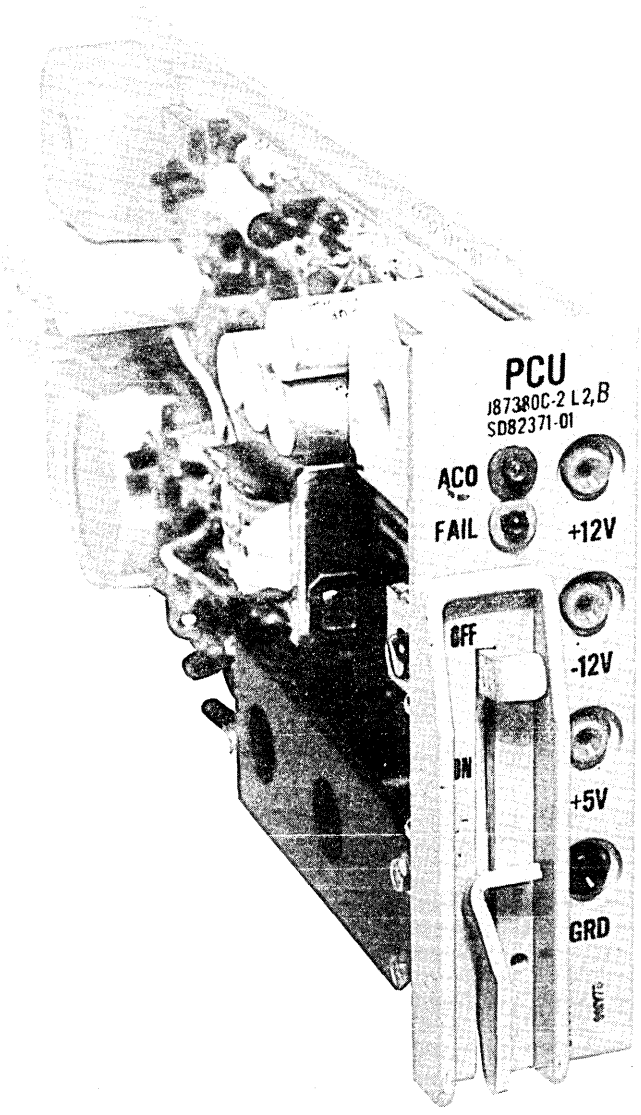

Fig. 6—Power converter unit.

signaling and transmission functions. A few of the features common to all channel units are:

(*i*) Reduction of false disconnects by storing and maintaining supervisory signaling states for up to 2 seconds during out-of-frame conditions before initiating trunk processing.

(*ii*) Card jack accessible through the faceplate that provides split-

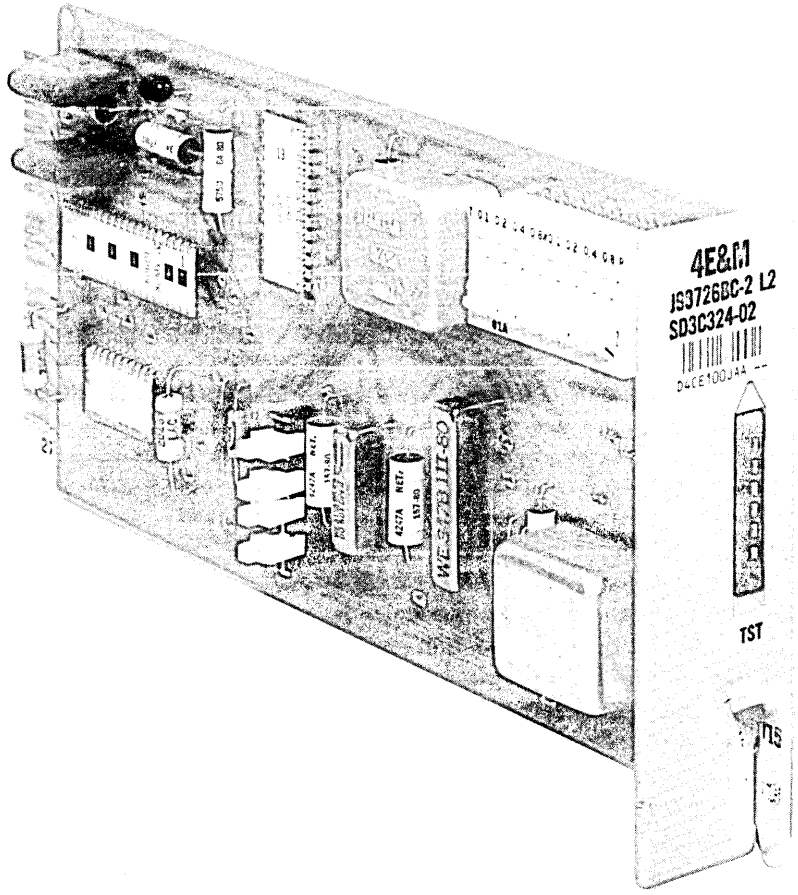

Fig. 7—Four-wire E and M channel unit.

ting access to equilevel test points in the four-wire transmit and receive paths and to the drop side signaling and supervision leads.

(iii) Precision-calibrated attenuators that permit prescription loss settings in 0.1-dB increments.

To ensure complete flexibility for service continuity and channel reassignments, circuitry for a single channel is provided on a single plug-in unit. These units are the interface between the central office trunk or other circuits and the bank common equipment. Different channel units match the two- or four-wire office circuits and also handle a variety of office signaling arrangements. For example, the four-wire E and M channel unit (shown in Fig. 7) interfaces with the four-wire E and M trunk circuits. It is also used to provide some special service arrangements, such as special access trunks and duplex signal-

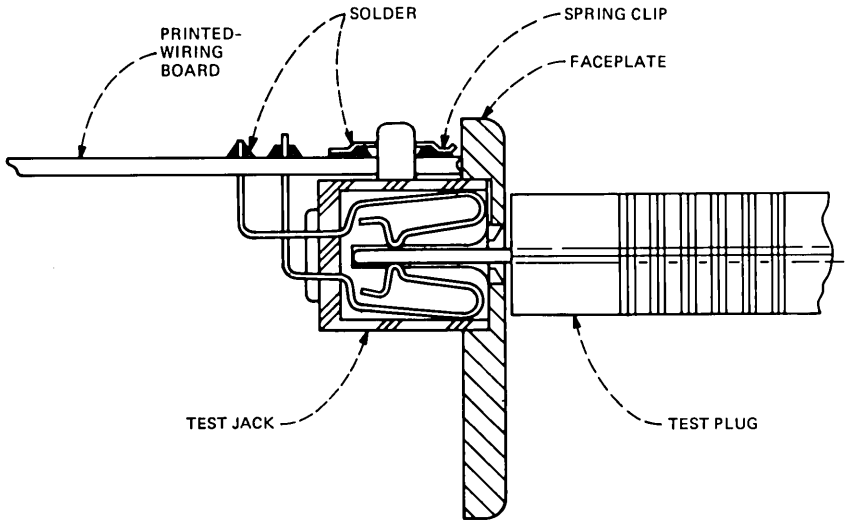

Fig. 8—D4 test access.

ing. This is the least complex, in terms of component and printed wiring density, of the D4 channel units.

A "card jack" connector, designed specifically for D4, is mounted directly on the printed wiring board. This connector has six pairs of shorting contacts that provide split-access for signaling and VF testing when opened by the insertion of an epoxy-coated metal printed wiring board plug. In addition to having the connector terminals soldered to the printed wiring board, a spring clip snaps into the bottom of the connector to hold it in position during mass soldering. It then becomes a solid retaining member when the clip is soldered to the board during the wave-soldering operation. This arrangement requires a minimum amount of board space. The connector is accessed through an opening in the channel-unit faceplate. This arrangement is illustrated in Fig. 8.

The rocker-type switch attenuator provides variable attenuation in the transmit and receive paths by setting a combination of mini-switches. This allows for prescriptively setting the attenuator in precise 0.1-dB increments of loss.

Options on D4 channel units are selected by using printed wiring board socket and plug combinations, as shown in Fig. 9. The plug and socket have been designed to provide a wiping action for high reliability when the plug is inserted. The plug snaps firmly into place, preventing disengagement during shock and vibration. The hybrid integrated circuits (HICs) are described in detail later in this article.

The two-wire Foreign Exchange Office End with Gain Transfer Unit (2FXO/GT) shown in Fig. 10 is one of the most complex channel units. This unit provides an interface to any two-wire foreign exchange

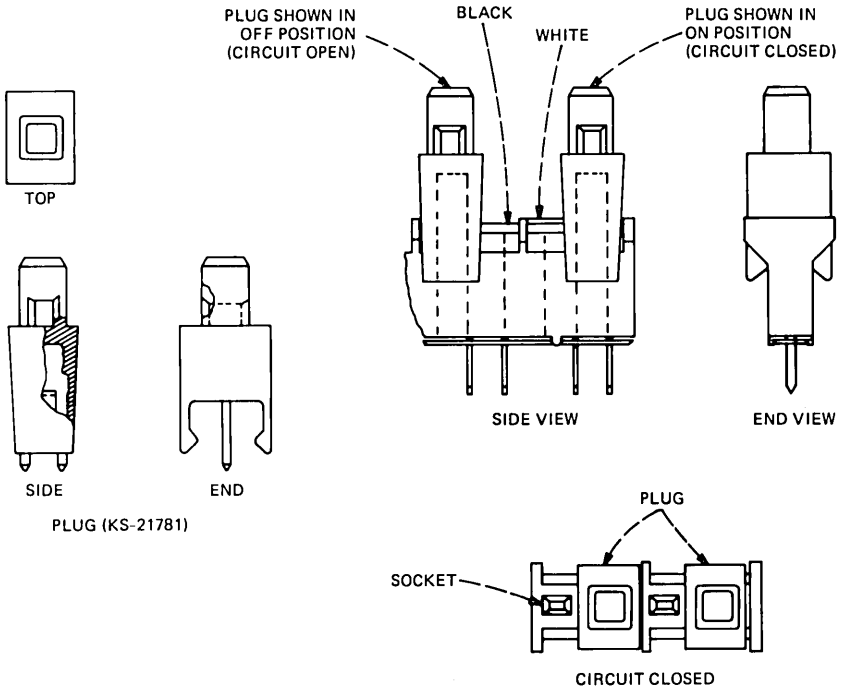

Fig. 9—D4 channel-unit option selector switch.

circuit at the office end of two-wire special service circuits (foreign exchange lines, off-premises station lines, foreign exchange trunks from a PBX, and other special access services). To accommodate the circuitry required for these functions, two printed wiring boards are required. The auxiliary printed wiring board is hinged to provide access for setting attenuator and option switches and is electrically interconnected to the main board through flexible printed wiring.

As the D4 channel bank production increased—it is currently running at about 50,000 banks and over 2-million channel units per year—it was apparent to designers of similar systems under development that a substantial reduction in cost and development effort could be realized by using the very versatile D4 hardware. Its most notable use is in the *SLC**-96 system.

III. THE SLC™-96 SYSTEM

The *SLC*-96 Subscriber Loop Carrier (*SLC*-96) system is a digital subscriber loop carrier system that can accommodate up to 96 subscriber channels between a central office terminal (COT) and a remote terminal (RT) using T1 digital lines. In addition to customer POT

* Trademark of Western Electric.

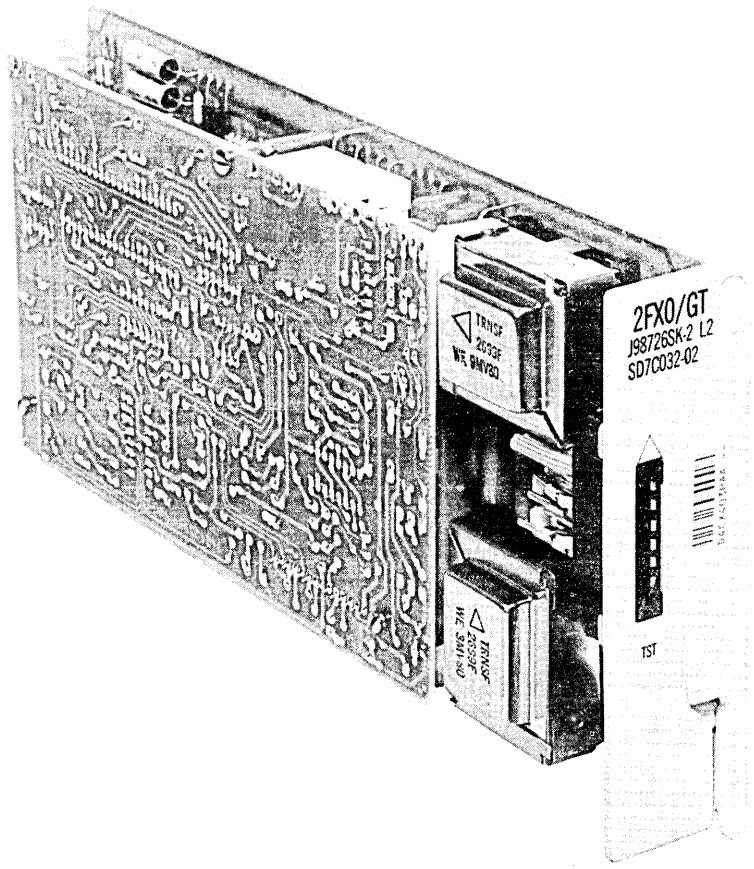

Fig. 10—Two-wire foreign exchange office end channel unit with gain transfer.

service, the system offers coin service, voice-frequency special services, and digital data services. The *SLC*-96 system is based on the transmission and physical design format of the D4 channel bank.

The *SLC*-96 system has two channel-unit designs for subscriber POT service: single-party service and multiparty service, combined with two-party automatic number identification (ANI). Coin service, including both dial-tone-first and coin-first modes, may be offered with a single pair of channel-unit codes. Most of the special service channel units developed for the D4 channel bank may be used in the *SLC*-96 channel bank.

The basic system components of the *SLC*-96 system are

(*i*) COT equipment and associated apparatus located in the serving central office

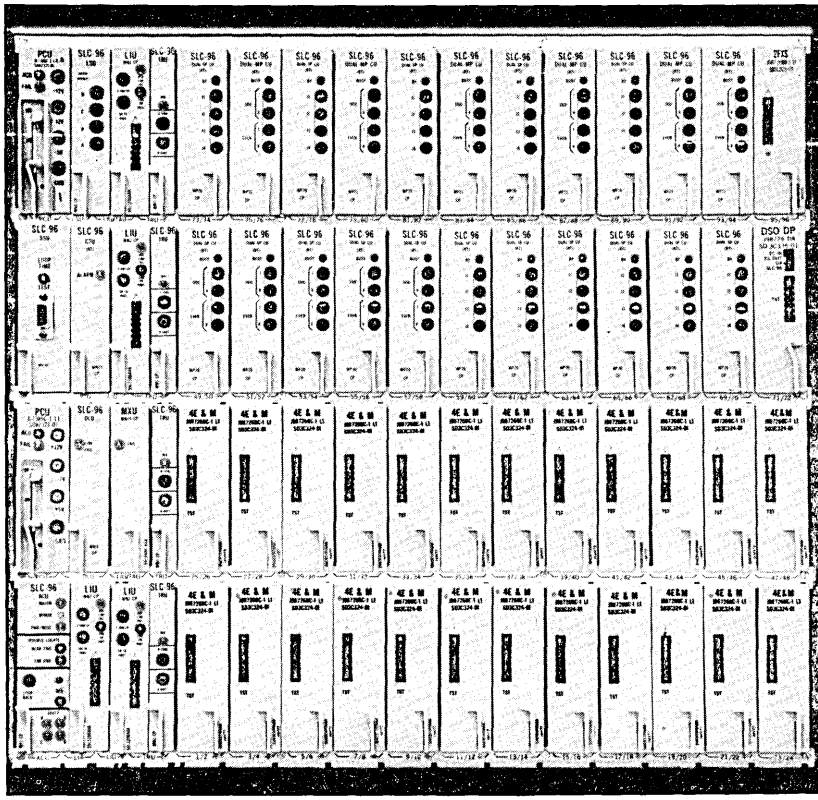

Fig. 11—*SLC*™-96 subscriber loop carrier channel bank.

(*ii*) RT equipment and apparatus located in the area to be served

(*iii*) DS1 facilities between the two terminals

(*iv*) The normal VF distribution facility extending from the RT to the subscribers.

Physically, the *SLC*-96 channel bank consists of four shelves, as shown in Fig. 11. Each shelf contains 12 slots for channel plug-ins and four additional slots for common equipment. Subscriber POTS channel units contain two channels per plug-in, while coin, special service, and dataport channel units contain one channel each. Therefore, each non-POTS channel displaces two subscriber channels.

The *SLC*-96 channel bank may be configured in a carrier-only mode, a carrier-concentrator mode, and a special services mode. Typical configurations illustrating these modes of operation are shown in Figs. 12, 13, and 14.

Mode 1 is primarily intended for subscriber lines with very high traffic. Since all channels are available on a full-time basis, non-POTS channel units may be mixed, as desired, with POTS channel units. Of course, each non-POTS channel unit displaces two POTS channels.

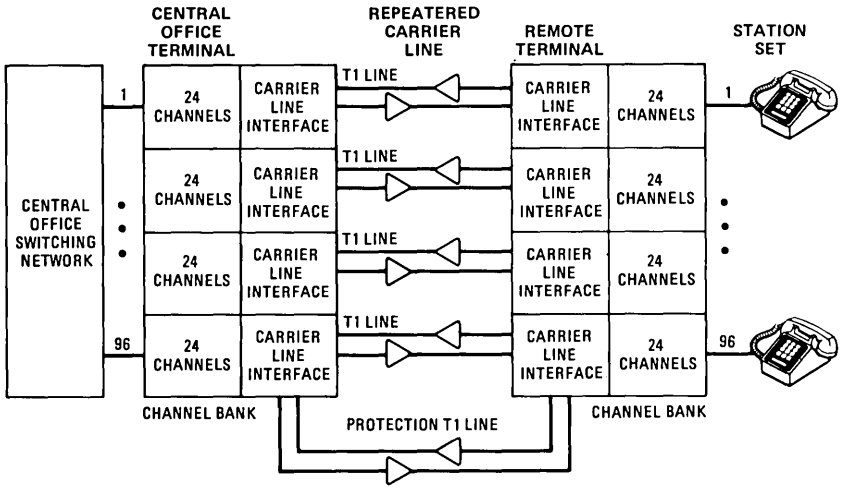

Fig. 12—The SLC^{TM}-96 system carrier-only configuration—Mode 1.

Mode 2 is intended for general subscriber lines. Full-access 48 to 24 digital switching (2:1 concentration) is a very conservative design with regard to traffic-handling capability and accordingly has no special traffic administration. This mode uses DS1 facilities more efficiently.

Mode 3 dedicates a 96-subscriber channel bank to 48 nonsubscriber channels. Each channel is available full time. Subscriber channel units are excluded from a bank operating in this mode. Mode 3 uses T1 lines more efficiently than Mode 1, for applications requiring large quantities of nonsubscriber channels.

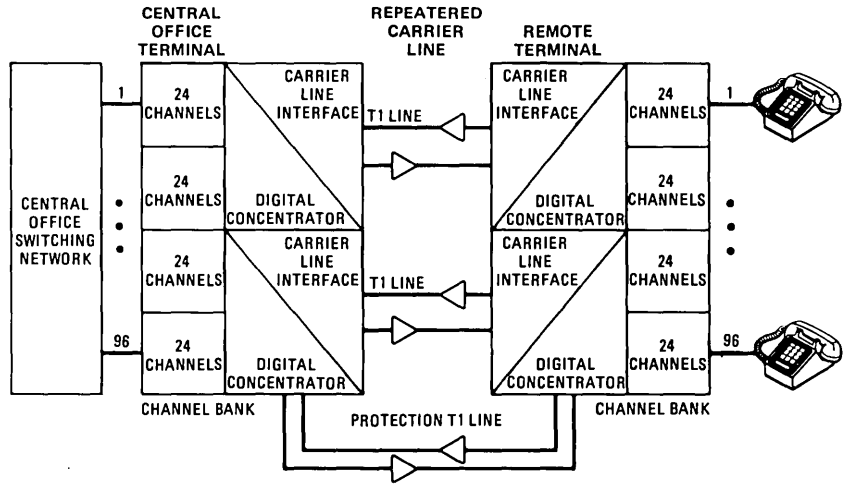

Fig. 13—The SLC^{TM}-96 system carrier-concentrator configuration—Mode 2.

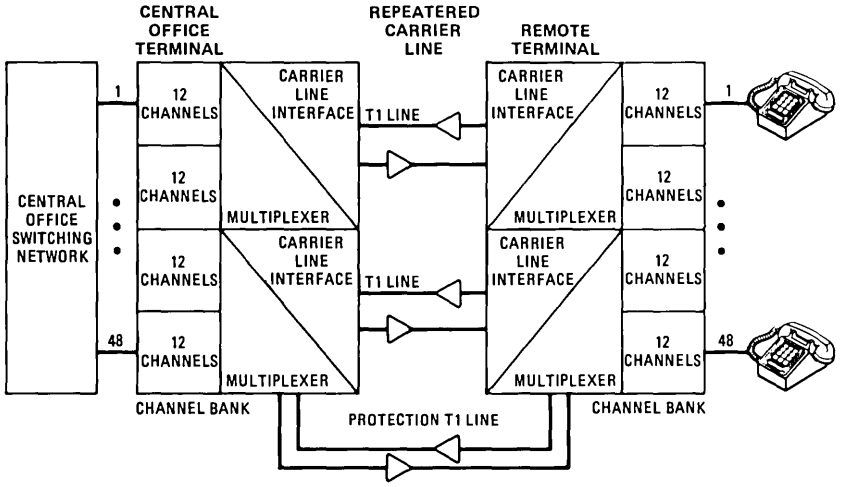

Fig. 14—The *SLC*™-96 system special services configuration—Mode 3.

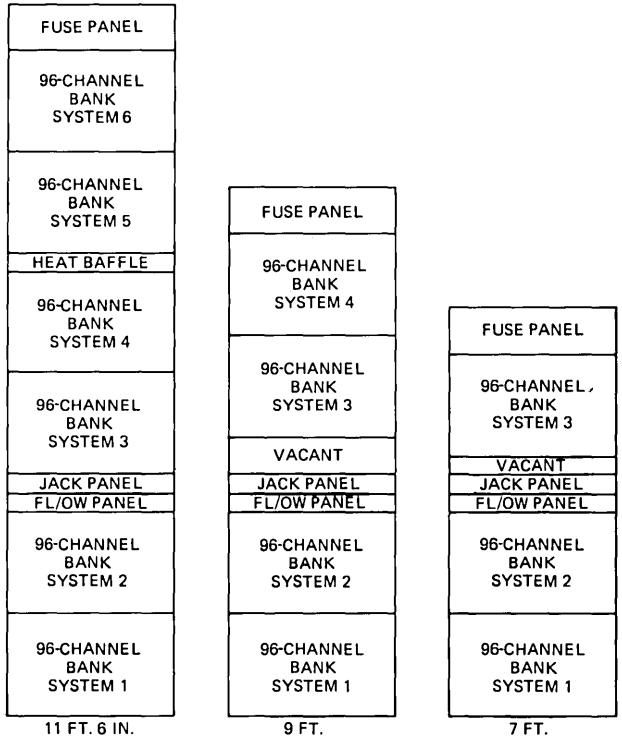

Fig. 15—Typical COT full-bay configuration for 7-foot, 9-foot, and 11-foot 6-inch frames.

COT equipment consists of a channel bank assembly, fuse and alarm panel, jack panel, and an optional T1 fault-locate and order-wire panel. (This section covers only central office channel banks and bays. Discussion of the *SLC*-96 remote terminal includes hut and cabinet considerations and is covered in this issue's article on the *SLC*-96 system.)

The fuse and alarm panel is mounted at the top of the central office bay, and can accommodate up to six *SLC*-96 systems. The panel provides fused -48V circuits to each power converter unit and distributes ±130 and -48V circuits to the LIUs for powering the digital lines. Each system in a bay has major, minor, and power/miscellaneous summary alarm arrangements, including local visual alarm and connections to office and remote alarm systems. One fuse and alarm panel requires five inches of vertical bay-mounting space.

The COT jack panel provides access to the digital lines and associated fault-locate lines for maintenance. The jack panel gains access to the digital line to be tested by means of a cord and card plug, which is inserted into a connector on the faceplate of the LIU serving the digital line. One jack panel is required for each bay and can accommodate up to six channel bank assemblies. One jack panel requires two inches of vertical bay-mounting space and is typically located at a convenient working height from the floor. A fault-locate and order-wire panel may be optionally provided at a COT bay for system maintenance. Figure 15 illustrates typical full-bay configurations possible for 7-foot, 9-foot, and 11-foot 6-inch bays.

IV. BANK HARDWARE

The size of the D4 channel bank was optimized to allow four 4-shelf channel banks to fit in a 7-foot unequal flange duct-type bay framework. The original banks were constructed with die-cast aluminum shelves that had plug-in unit guides cast on the top and bottom. The four connectorized backplanes were attached to the rear of the shelves. The shelves were fastened together with side brackets that were also used to mount the bank to the bay. Additional holes were drilled in the side plates so that the same part could be used for banks that are mounted in bays with a 5-inch front extension. Oversized screw holes were used in the brackets with factory assembly gauges to fix the spacing between shelves before the screws were set. Banks were coupled together in the bay with the top shelf of one serving as the bottom for the one above and with gauges again used to set the proper spacing. The top bank contained a top cover, with plug-in guides on the bottom side only.

A new, inexpensive method of keying plug-in units in the common equipment area was used by providing extra slots in the designation

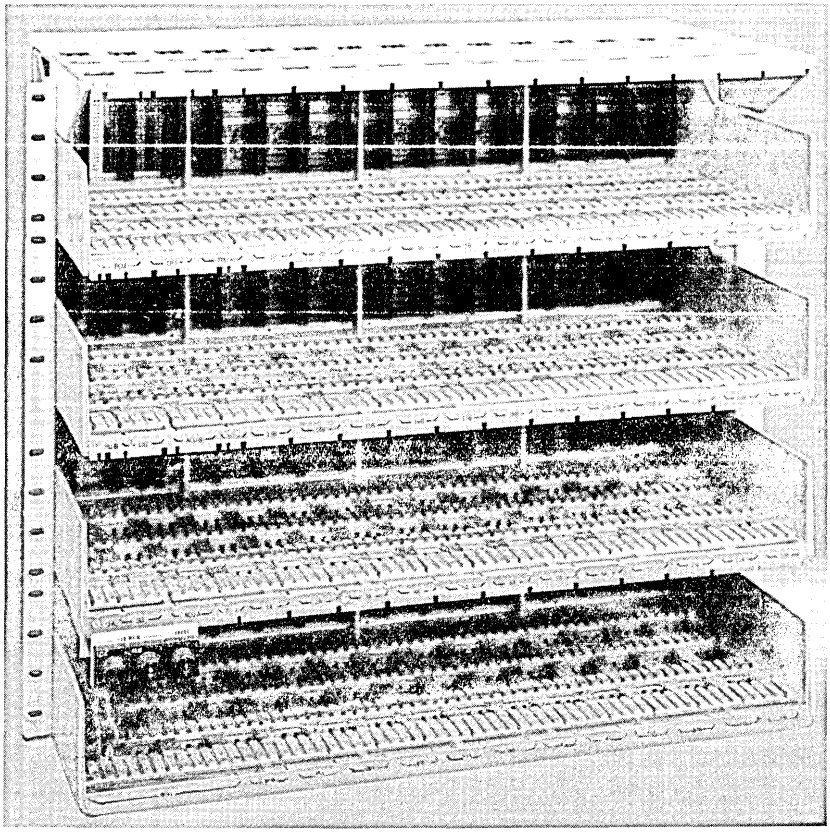

Fig. 16—Aluminum die-casting channel bank assembly.

strips that run along the front edge of the shelves. Distances between these extra slots and the plug-in printed wiring board slots were varied and matching bosses were cast into the rear of the faceplates to align with the slots in the proper plug-in positions. This bank assembly is illustrated in Fig. 16.

A second bank shelf assembly was subsequently designed to reduce cost. Shelf castings were simplified by removing the sides and the rear backplane support framework from the shelf casting. This allows the shelves to be stacked in various heights, making the bank assembly attractive to other systems looking for a low-cost, high-volume production shelf.

Overall bank weight was reduced by 25 percent. Shelves were coupled together with full-width sideplates, and bay-mounting adapters were, in turn, applied against the sideplates. Backplanes were fastened along the bottom edge of the shelf above and the top edge of the shelf below. Gauging of shelf-to-shelf spacing was minimized on all

but the top shelf by using the backplanes as a gauge at the rear of the shelf and using tight diameter screw holes in the sideplates at the front of the shelves. Banks were again coupled together in the bay with the top of one serving as the bottom of the one above. Openings in the shelf were increased from a previous level of 29 percent to 45 percent, resulting in improved cooling with an average decrease in bank operating temperature of 6 degrees Fahrenheit.

At present, because of an ever-increasing demand and cost sensitivity, a new third-generation channel bank shelf assembly has been developed. While the assembly shown in Fig. 17 will initially be used for the *SLC*-96 system, it has been designed to accommodate D4 and other related projects.

Improvement has been made in three areas: a cost reduction of shelf die castings; a simplification of bank and bay assembly; and finally, the incorporation of other desirable features such as independent bank mounting, smaller stand-alone bank size, and increased structural stability. The new shelf die castings have been optimized for strength, weight, and castability while maintaining the improved bank cooling achieved with the second-generation shelf, which has 45-percent open shelf area. The basic structure that led to the optimization is a Z beam that is perpetuated through a lattice, as conceptualized in Fig. 18.

The Z beam is similar in principle to an I beam, minimizing weight while maximizing strength, and in addition allowing easy coring of the die part. To design a shelf of the right strength, the design criterion chosen was that a plug-in unit in the center of a shelf should not fall out of the groove in the shelf above when the bank is subjected to a 3-gram load. While in practice, the backplane connector would likely prevent actual fallout, this degree of conservatism was preferred. Through a tolerance study of the bank assembly and plug-in unit designs, it was determined that the shelf could have a maximum deflection of 0.017 inch under worst-case static loading, or 0.051 inch with a 3g dynamic load. The shelf was then designed to be slightly stronger, with a 0.012-inch (0.036 inch at 3g's) deflection under worst-case loading. Since the shelf is supported on both sides and at the back, the beams were spaced progressively closer from back to front to concentrate the strength where it was most required. The weight of the shelf is just over 3 pounds, and the worst-case load on the shelf was assumed to be 20 pounds.

The structure chosen enhances the die-casting process by virtue of its uniform and thin-cross sections. Metal flow is unrestricted and even, which ensures good fill and minimizes erosive die wear, thus prolonging die life. Also, the die can be efficiently designed with minimum gate sizes and the trim die can be correspondingly simple. Since all cross sections are relatively uniform, all material will solidify

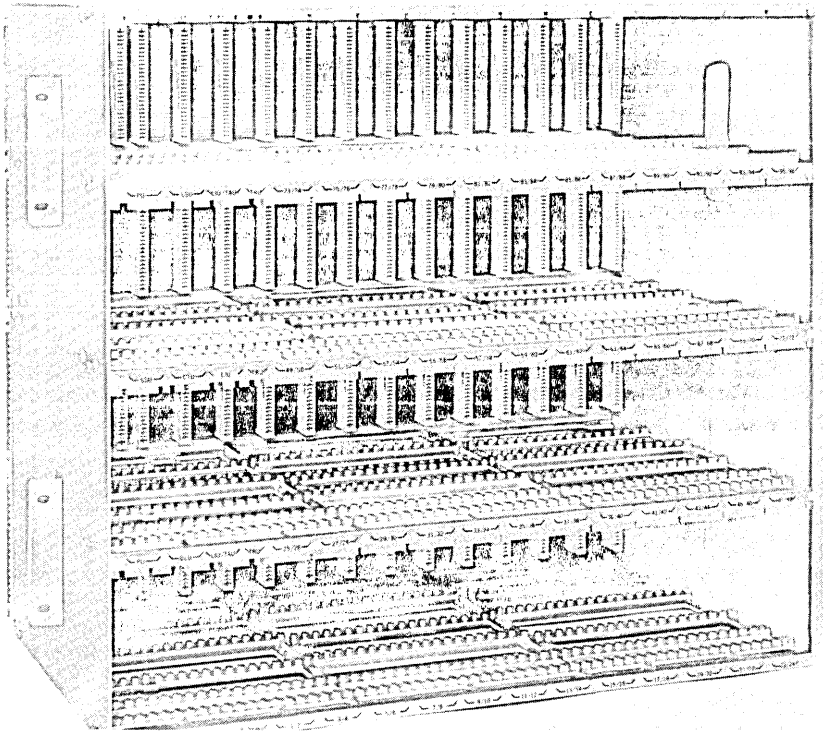

Fig. 17—Third-generation shelf assembly.

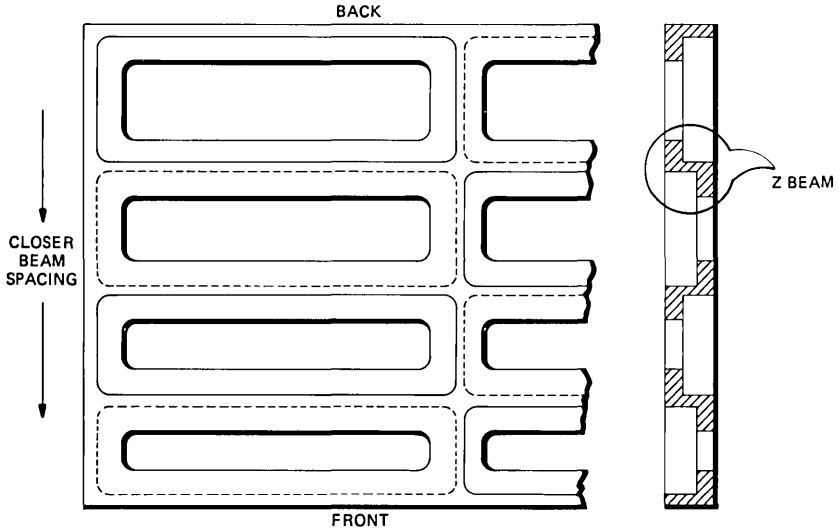

Fig. 18—Z-beam lattice die-cast shelf.

at about the same time, which will minimize shrink areas, microporosity, and residual stresses. Since all sections are relatively thin, the overall cooling time is minimized with a resultant decrease in die casting cycle time. This produces a higher casting rate, which in turn reduces the cost per casting.

Assembly of the new banks and bays has been streamlined by eliminating the need for any type of accurate fixturing and reducing the number of parts and screws. Bank fixturing is eliminated by using round mounting bosses, which are cast into the ends of the shelves and which match up with three slots in the side plates (see Fig. 19). Two slots are used to fix the shelf height, while the third establishes uniform depth. Since the mounting bosses make only tangential contact with the slots, the parts easily mate with even a slight interference fit. The slot width has, therefore, been nominally dimensioned only slightly larger (0.003 inch) than the boss diameter, thus promoting tight registration of the shelf. Mounting bosses have also been used to accurately locate the backplanes on the shelves. In this case space limitations and backplane variations led to the use of one diamond-shaped boss in a round backplane hole and one round boss in a backplane slot.

By using slightly thinner bottom and middle shelves and a substantially thinner top cover, the banks are now designed to mount independently in a bay framework with no sacrifice in space. This eliminates the need for any alignment when the shelf is mounted in a bay. Assembly and piece part costs have been further reduced by combining side plates and bay-mounting adapters into one piece. Also, fewer screws have been used to assemble the side plates to the shelves since the mounting details are also weight-bearing members.

In addition to the shelf and assembly cost reductions, there are several other desirable features incorporated in the new design. The shelves are less susceptible to movement caused by shock and vibration since all shelves are securely positioned via the mounting bosses.

Since banks are independently mounted, removal for repair and replacement of a bank in a bay, especially in the field, is greatly simplified. Independent banks also allow for shipment of partially filled, low first-cost bays for slow growth offices with additions conveniently made in the field as required.

Other applications have arisen where a channel bank may stand alone or be used in a bay with other types of equipment. While the existing design can be used in this single bank mode, the interlocking features on the top and bottom shelves add to its overall height. The new design has been trimmed to 19 inches as opposed to about 20 inches for the existing design. The new one-shelf units, such as the subscriber loop interface module (SLIM), will be five inches high instead

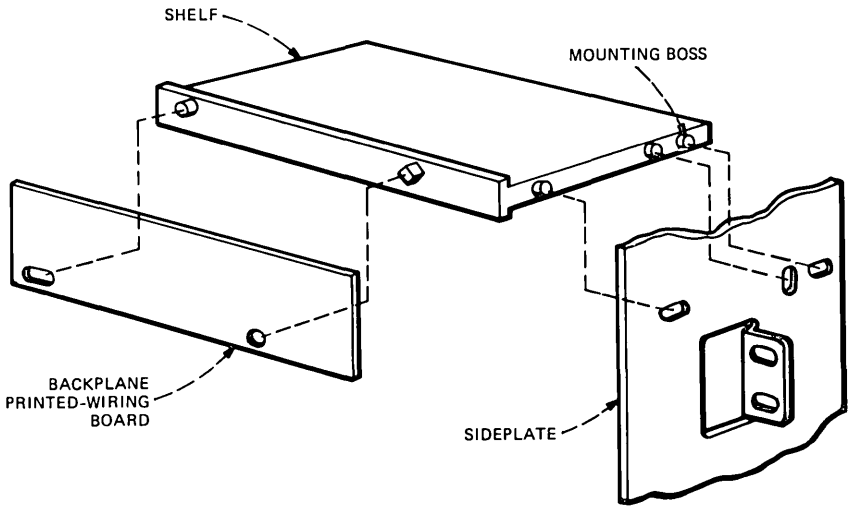

Fig. 19—Bank assembly alignment.

of about 6 inches and new two-shelf units will be 10 inches high instead of about 11 inches.

Holes used to mount the bank to the bay have been positioned at a conventional incremental distance from the bottom of the equipment since they do not have to be placed to accommodate odd-size banks being tied together. This allows for mounting with other equipment above or below, not wasting some portion of an inch.

V. BACKPLANE

In the early D4 channel bank production, rigid aluminum backplanes with press-fit edgeboard connectors were used. There are four backplanes in each bank and sixteen 54-pin connectors on each backplane. The bottom shelf backplane is smaller than the other three to facilitate mounting the Power Distribution Unit (PDU), which is the only unit in the bank that is not a plug-in unit. Insulated 26-gauge wires were wrapped manually to make the intra- and inter-backplane circuit connections. After a sufficient amount of operational experience was gained, a printed-wiring backplane was introduced into production.

The backplane edgeboard connectors are manufactured to Bell System requirements by commercial connector manufacturers. The connector pins are inserted into plated-through-holes in the backplane. The pin-to-board connection is made through a compliant section of the pin, which eliminates the need for soldering. This was especially important, since to efficiently use a printed-wiring board backplane it was necessary to use circuit paths nominally 0.010-inch wide separated by 0.010-inch spaces. The solderless compliant section was approved

for Bell System use after a very extensive qualification program was completed.

The connector housing was designed to support alternate rows of early- and late-make contacts. This arrangement is important to avoid circuit "hits" and also to reduce the force required to insert or remove a plug-in unit. Two sets of "normal through" or "shorting" contacts are provided for each channel-unit position to facilitate trunk processing. Selective plating and other techniques are being used to supply gold in the contact area only.

At present, about 70 percent of the backplane wiring is printed. A three- to four-layer backplane would be required to print the remaining 30 percent of the wires, which at this time would be prohibitively expensive.

VI. PLUG-IN UNITS

There is one basic printed-wiring board size for all plug-in units in the D4 channel bank except for the PDU, which is covered later. The basic plug-in unit design employs an epoxy glass, double-sided rigid printed-wiring board about 9.9 inches long and 4.3 inches high. Each board has 54 gold fingers, 27 on each side, for interconnection to the edgeboard connector in the backplane.

Each plug-in unit contains a faceplate with a simple latching mechanism that aids in extracting the unit and also serves as an automatic lock that prevents the unit from becoming unseated by shock or vibration such as might occur during earthquakes.

The plug-in unit and shelf have been designed to ensure proper insertion and connector mating over a relatively wide tolerance range. When the plug-in unit is inserted in the shelf, the faceplate always comes in contact with the shelf, preventing the printed-wiring board from bottoming in the backplane connector. Since the backplane connector is rigidly mounted, float is provided in the shelf track.

VII. HYBRID INTEGRATED CIRCUITS

Hybrid integrated circuits (HICs) were used extensively to achieve a compact and cost-effective channel bank. A typical channel unit contains two resistor-capacitor (RC) low-pass filter HICs, two planar thin-film integrated circuits as part of the attenuators, and one custom resistor-crossunder HIC for the rest of the integratable electronics.

The principal reason for the extensive use of HIC technology is the small size that is achievable at a cost comparable to, or less than, the cost of a discrete equivalent. The small size allows fewer and smaller printed-circuit boards. The use of hybrids also tends to allow a simpler class of printed board since much of the interconnection is accomplished in the HIC.

The transmit and receive units of D4 were initially designed using predominantly small-scale integration "catalog" silicon devices. The longer term expectation was that larger scales of integration could be used, as cost reductions, when such devices became available. With this in mind, it was desirable to package the existing small-scale devices as compactly as possible to allow for a graceful evolution to larger scales of integration. Initially, the transmit and receive units contained 52 and 51 silicon integrated circuits, respectively. The present transmit and receive units contain only six and five devices, respectively. This evolution of large-scale integration into the receive unit is illustrated in Fig. 20.

In predominantly digital circuits like the transmit and receive units, the hybrids have been replaced by LSI silicon, but in most cases the hybrid remains the optimum packaging technique for providing functional modules of precision passive components and a mix of silicon device technologies.

Two different film-circuit process classes were used for the D4 HICs. The resistor-crossunder class was used for most of the hybrids in the channel bank. The fabrication sequence for this class of circuits is described in the next paragraph. The resistor-capacitor process class was used for the active filter realizations in the channel units and a

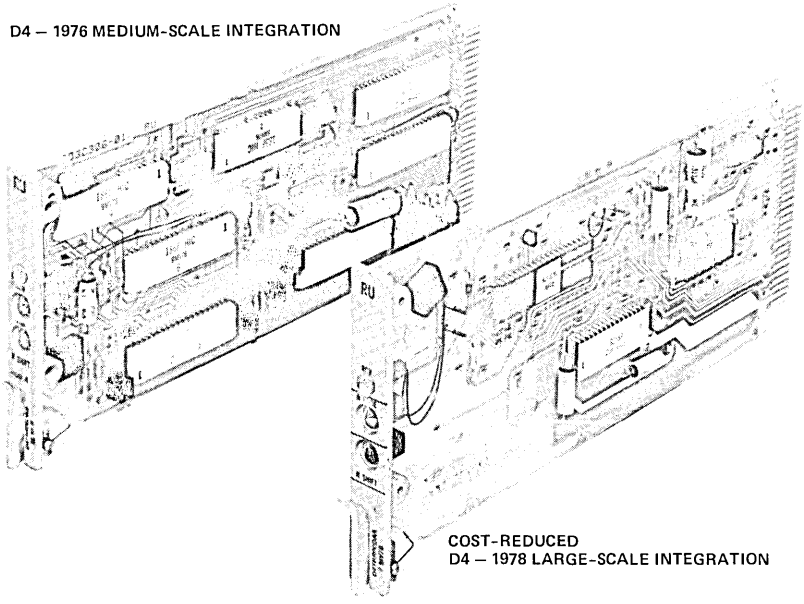

Fig. 20—Evolution of large-scale integration (LSI) into the receive channel unit.

description of this process class follows the resistor-crossunder description. Typical circuits are shown in Figs. 21 and 22.

A combination of thick-film and thin-film technology is used on the resistor-crossunder hybrids. The thick film is used for a rugged crossover structure, and the thin film for resistor fabrication and fine-line conductor metallization. All of the film-circuit processing is done on a major substrate, 3-3/4 inches by 4-1/2 inches. Eighteen of the 24-pin DIP-size circuits are processed at the same time. Briefly, the process sequence is as follows: Starting with a fine-grain, 99-percent alumina substrate, a thick-film gold conductor pattern is screen printed and then fired. Two layers of dielectric glaze are then screen printed and fired on top of the gold conductor, leaving short lengths of gold extending beyond the glaze. This will eventually form part of the crossover structure. Next, the thin-film resistor and conductor films are deposited over the entire substrate. The resistor film of either 100 or 300 ohms per square tantalum nitride is deposited by sputtering. The conductor film consists of thin layers of sputtered titanium and palladium, followed by about 1.5 μm of plated gold. Two pattern-generation sequences are then performed to selectively remove the conductor and resistor metallization. The resistors are then stabilized at 300 degrees Centigrade for four hours and laser trimmed to value. Next, the beam-lead silicon integrated circuits are bonded by thermocompression and the substrate is snapped into individual circuits. Soldered leads are then attached, the room temperature vulcanization (RTV) encapsulant is flow coated, and the circuits are tested and burned in.

A small set of standard sizes had been chosen for all HICs for telephone transmission applications. The specific circuits developed for the D4 system conformed to this standardization. The standard sizes are the 24-, 32-, and 40-pin, 0.600-inch wide, dual in-line packages (DIPs). This external size standardization enables common high-speed handling equipment to be used for burn in and testing.

Standard metallization features have also been incorporated on the

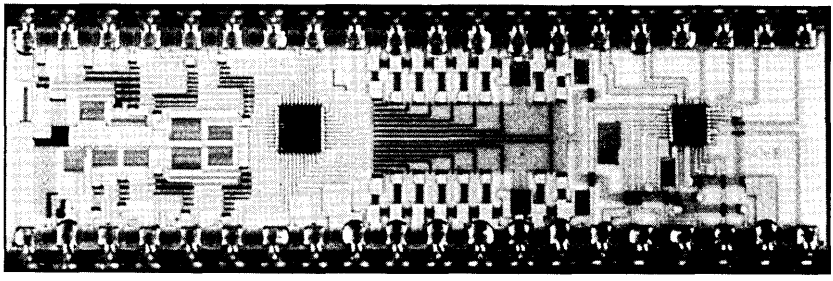

Fig. 21—Typical resistor-crossunder HIC.

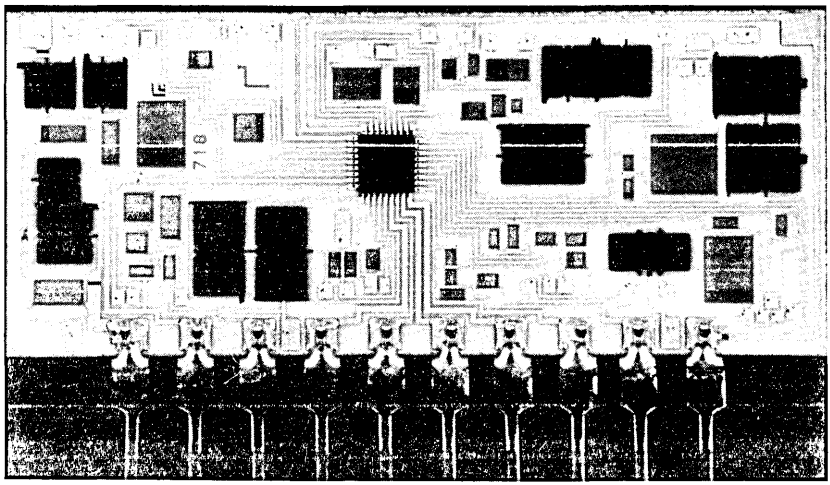

Fig. 22—Typical resistor-capacitor HIC.

ceramic to allow for common probing fixtures for resistor trimming and testing, isolation testing, and fault diagnostics. These features are located along the edge of the ceramic, allowing for maximum layout flexibility on the interior of the circuit.

The resistor-capacitor (RC) circuits used for the active filter functions in the channel units have many similarities to the resistor-crossunder circuits previously described. They use the same substrate material and size standardization, the same laser-trimmed resistor geometries, the same bonding and lead attach techniques, and the same encapsulation procedure. The differences are in the film-circuit process sequence that creates the capacitors and in the functional adjustment of the resistors to provide the required filter characteristics.

The film-circuit fabrication starts with screen printing and firing of a thick-film dielectric glaze to prepare a smooth surface at the future capacitor sites. Then tantalum is sputtered over the complete circuit and thermally oxidized to create a chemically inert surface. Next, the capacitor film (αTa) is sputtered. The capacitor base electrodes are then delineated by pattern generation (photoresist and etching). The capacitor dielectric is generated by anodizing the capacitor film through a photoresist mask. The anodization voltage determines the capacitor dielectric thickness. Next, the resistor and conductor films are deposited over the entire substrate. The resistor film is 300 ohms per square tantalum nitride, and the conductor film is sputtered titalum and palladium followed by plated gold. The conductor and resistor geometries are next pattern generated using standard photolithographic techniques. The capacitors are then tested for leakage current at 55 volts. Circuits passing this test proceed to have their

resistors trimmed to achieve a precise RC product. This is the frequency-determining parameter in the filter. The silicon operational amplifiers are then bonded and the substrates are laser scribed and snapped into individual circuits. The external leads are then attached and the circuits are electrically tested. A small percentage of the circuits require additional functional trimming to achieve a precise gain at 1kHz. The circuits are then encapsulated and retested.

VIII. HEAT TRANSFER

It is generally true that components used in the D4 and *SLC*-96 systems can operate reliably in a 185-degree Fahrenheit ambient temperature. D4 and *SLC*-96 banks have, therefore, been designed to operate with internal ambient temperatures of 185 degrees Fahrenheit or less even during emergency periods and while dissipating typical worst-case power. Emergency periods, as defined in the New Equipment Building System General Equipment Requirements, BSP Section 800-610-164, permit the office ambient to be 120 degrees Fahrenheit for a maximum of three days in a row, not to exceed fifteen days per year. The ambient temperature of an office is measured five feet up from the floor and 15 inches in front of the bay. Typical worst-case power is not an absolute maximum but is a level which few banks are expected to exceed. For D4 tests an assortment of channel units were chosen that were somewhat weighted towards high-dissipating units; a busy level of 75 percent was used. For *SLC*-96 tests a traffic level of 7 hundred call seconds (ccs) or 19 percent was used. Also, *SLC*-96 Line Interface Units (LIUs), which can vary considerably in dissipation level because of the inclusion of T1 office repeaters, were simulated at the high end of their dissipation range.

During the initial stages of D4 development a prototype bay was assembled and tested to determine expected operating temperatures. The bay consisted of six simulated D4 banks mounted in an 11-foot 6-inch bay. The top two banks were equipped with simulated D4 plug-in units. These units consisted of resistors, to dissipate anticipated power levels, and wooden blocks, to simulate air flow restrictions, mounted on printed-wiring boards. In addition, a working prototype of the power converter unit, which is the highest dissipating unit, was mounted in one of the top two banks. The four bottom banks were metal boxes equipped with light bulbs that dissipated equivalent bank power. Testing established that the design should perform adequately without any special measures being taken to cool the equipment. As D4 production bays and plug-ins became available, a production bay was tested as a check on the temperature performance and the validity of the early testing. The configuration tested dissipated 81 watts per bank. Again, when projected to a 120-degree Fahrenheit office, the

equipment did not exceed the 185-degree Fahrenheit limit (shown in Fig. 23). There were, however, some differences between the production and simulation bay results. While the average common-unit temperatures were approximately the same, the hottest production channel unit was 15 degrees Fahrenheit above the same in the simulated bay and the production power converter unit was 9 degrees Fahrenheit higher.

When the *SLC*-96 COT development was initiated, an improved prototype bay was constructed based on the experience gained from the D4 prototype bay. The top four banks were equipped with simulated plug-in units and light bulbs in metal boxes used for only the bottom two banks. Backplane printed-wiring boards and connectors were used. Also, the power dissipated in simulated channel units was asymmetrically distributed as the busy channels were randomly distributed throughout the banks. The power level tested in the bank was 134 watts. This power level was not only higher than D4, it was not as evenly distributed. With the inclusion of a second PCU and T1 office repeaters in each of the five LIUs, 63 percent of the *SLC*-96 dissipation is in the common-unit section, which occupies the left quarter of the bank. As a result, the maximum temperature levels were exceeded with a local ambient temperature in the power converter units of up to 212 degrees Fahrenheit and up to 196 degrees Fahrenheit in the interface units.

To improve the temperature levels several steps were taken. The power converter unit was redesigned with particular attention paid to distributing dissipating components throughout the unit. Heat dissi-

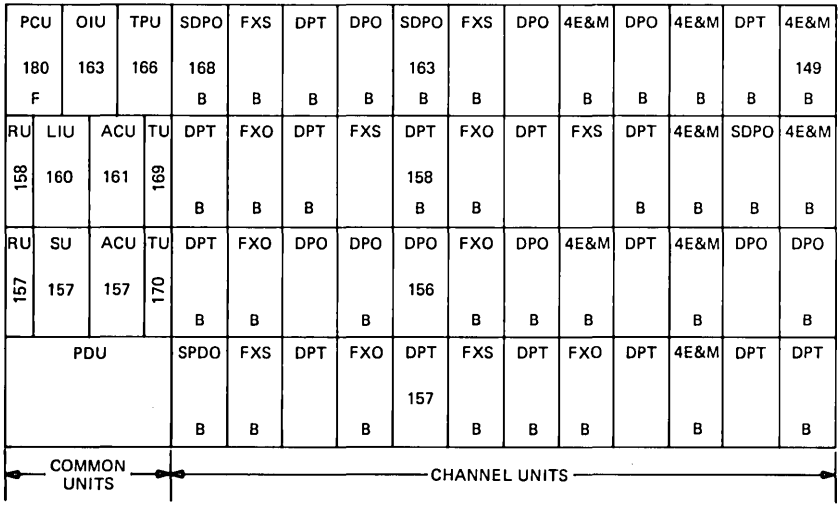

Fig. 23—D4 temperature profile.

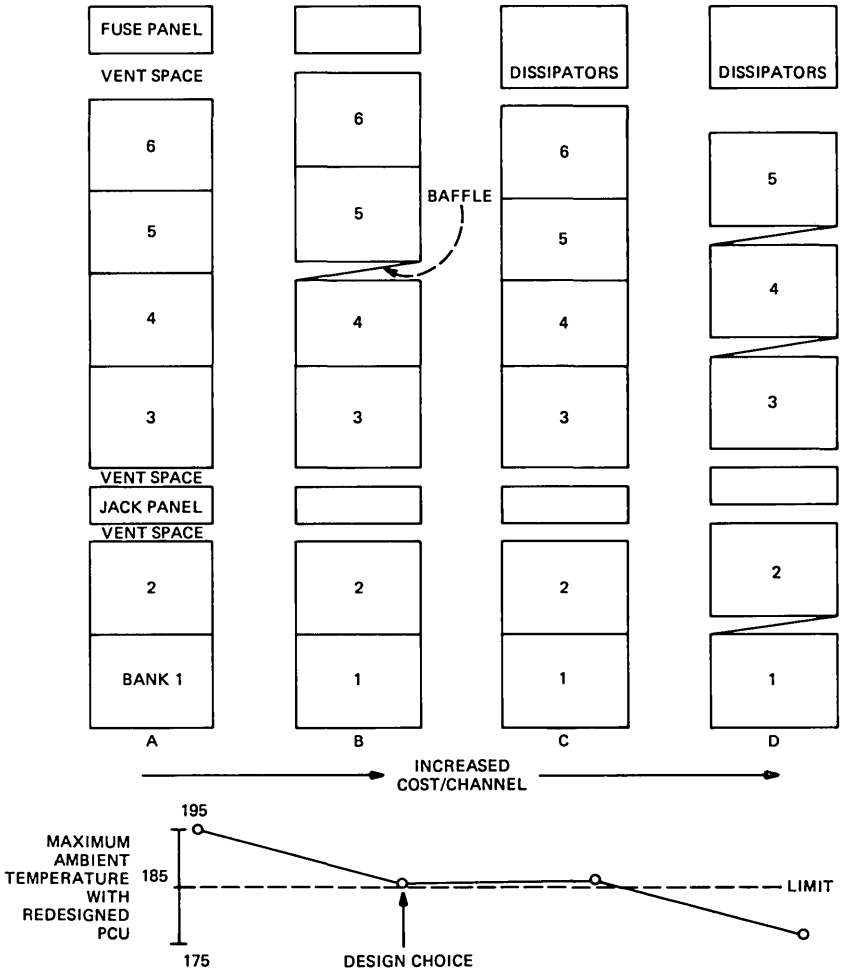

Fig. 24—Effect of bay baffles on bank temperatures.

pation was also improved by using an epoxy-clad metal printed wiring board rather than an epoxy-glass board. The redesign accounted for a 16-degree Fahrenheit reduction in unit temperature. Several approaches were considered to reduce overall bank temperatures, including a reduction to five banks per bay with heat baffles between each bank and external dissipation at the top of the bay of some of the line interface power. However, the most economical alternative that still met the requirements was the use of one baffle between the fourth and fifth banks and ventilation spaces above the second bank, below the third, and above the sixth, as shown in Fig. 24.

After D4 production was well established, a cost-reduced shelf and

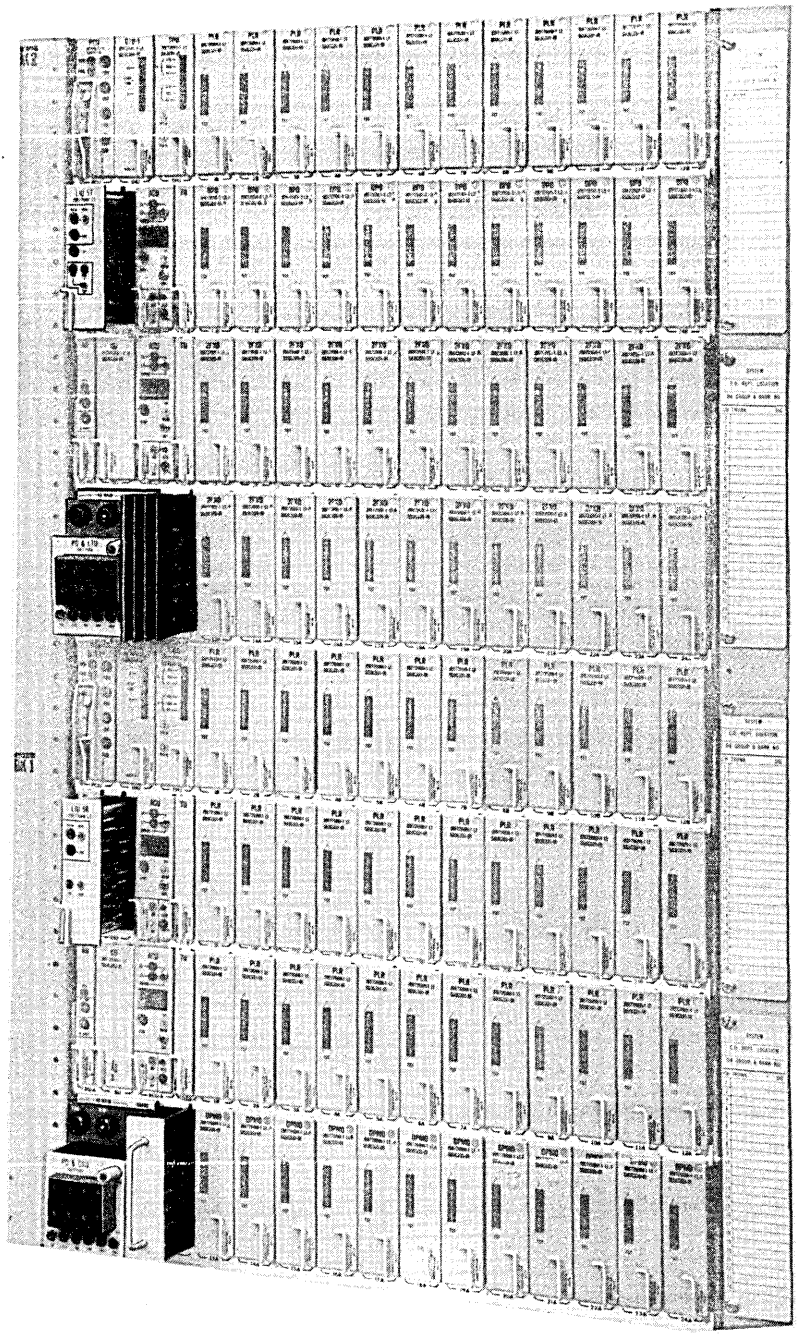

Fig. 25—D4 channel bank—Mode 5.

bank assembly was designed. As part of the redesign, the open area in the shelf was increased from 29 percent to 45 percent. As a result, the average temperature reading in the bank dropped 6 degrees Fahrenheit. This shelf is now being used in production on both D4 and *SLC*-96 systems, thus giving an added margin for temperature performance.

IX. LIGHTWAVE APPLICATION

The D5 Channel Bank Mode 5 (Fig. 25) was introduced to meet the emerging needs of the telephone companies for small cross-section, low-bit rate, lightwave transmission systems. Mode 5 is a 96-voice grade channel facility that can be connected directly to to a maximum of 4.5 miles of lightguide cable. This arrangement is targeted primarily for the short-haul point-to-point routes where the lightwave transmission attributes are required but the cross sections are too small to justify the installation of higher capacity lightwave systems.

D4 Mode 5 expands the versatility of the D4 channel bank family by offering a "built-in" capability for connecting to lightwave systems. D4 Mode 5 is electrically similar to D4 Mode 4, a 96-channel mode of operation that interfaces with DS2 rate-transmission facilities. In the Mode 5 operation, however, the multiplexed DS2 rate signal is dipulse coded and transmitted directly over an optical fiber using either a laser

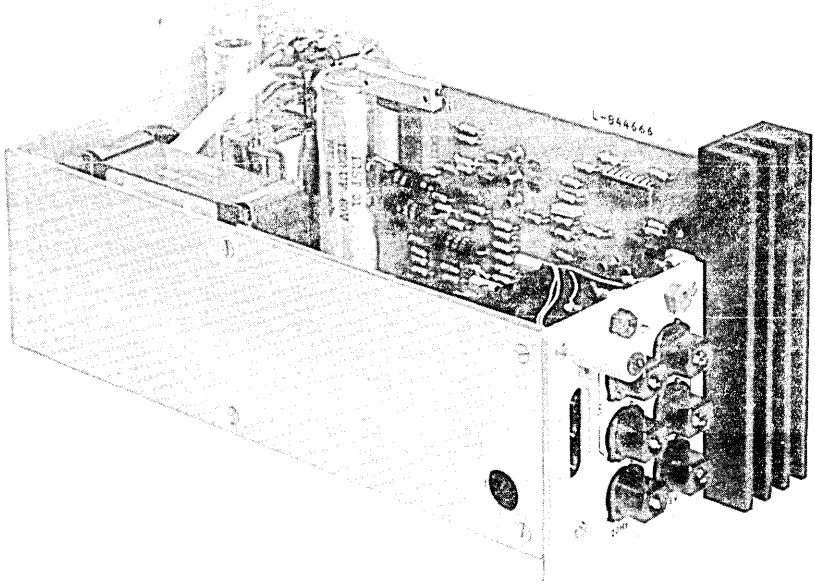

Fig. 26—Power distribution unit equipped with optical transmitter.

diode or an LED transmitter. The transmitter is housed in one of the two Power Distribution Units (PDUs), as shown in Fig. 26. The receive-path optical transducer is located in the second PDU (see Fig. 27), along with a silicon avalanche photo diode (APD) used to convert and amplify the light energy from the optical fiber.

Converting from Mode 4 to Mode 5 only requires changing the PDUs and the transmitting and receiving LIUs and adding a few wires at the rear of the bank. An extensive field trial evaluation was conducted in Sacramento, California. The route used was 2.7 miles long, connecting the Gladstone and Main offices. The lightguide cable contained 36 fibers. In addition to D4 Mode 5, the MX2-L Lightwave Digital Multiplexer-Demultiplexer (Muldem) and DLC-2 Direct Lightwave Connectors were also tested at Sacramento. These designs also use the D4 hardware.

The first commercial service over D4 Mode 5, manufactured by Western Electric, was installed at the 1980 Winter Olympic Games in Lake Placid, New York. The D4 Mode 5 provided flawless voice transmission between the Lake Placid central office and the broadcast center throughout the entire period. A map illustrating the communications route and equipment is shown in Fig. 28.

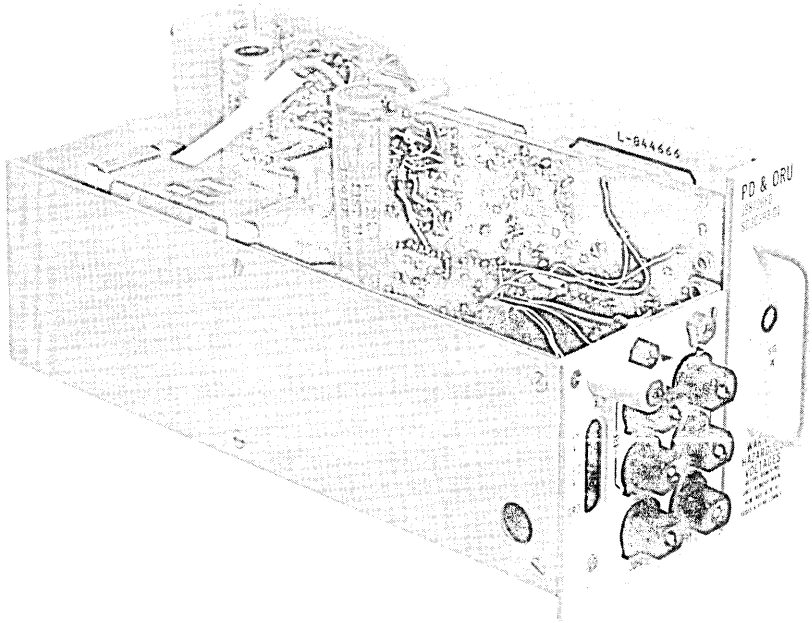

Fig. 27—Power distribution unit equipped with optical receiver.

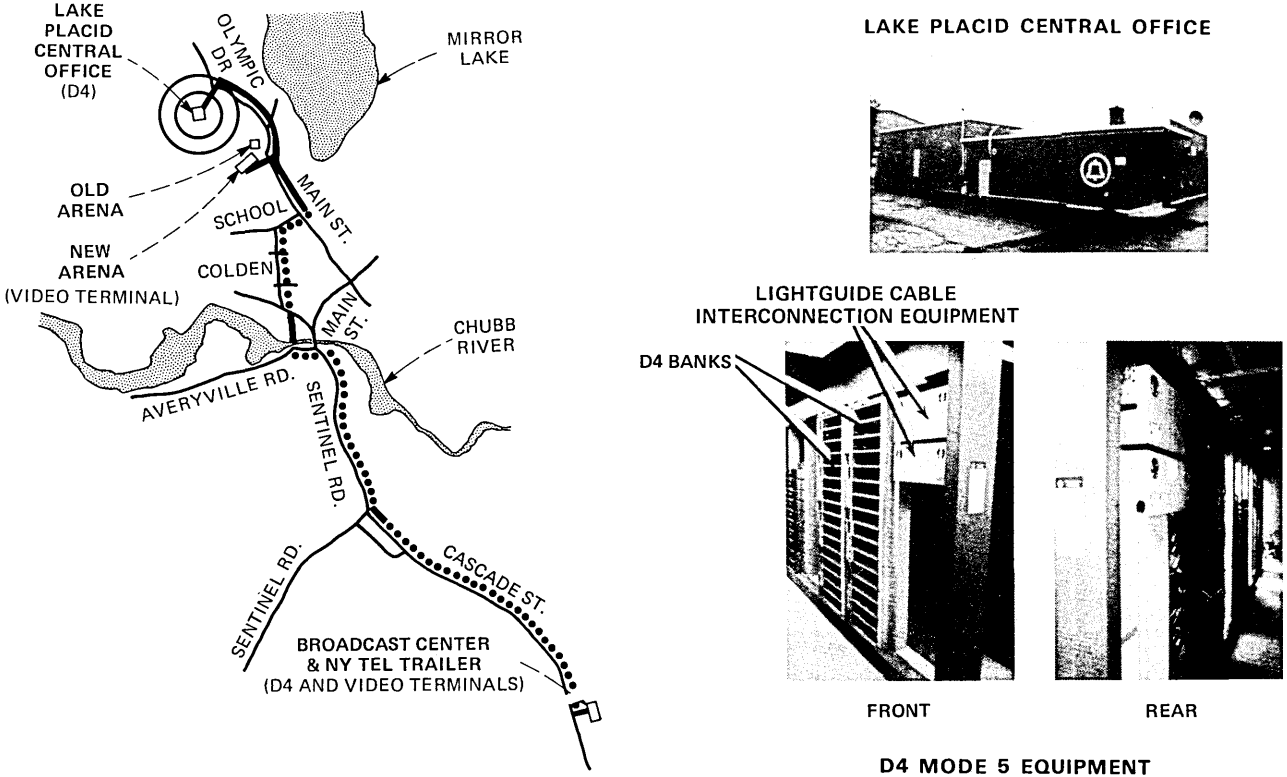

Fig. 28—D4 Mode 5 at Lake Placid, New York during the 1980 Winter Olympic Games.

Fig. 29—Display of different systems using D4 technology.

X. PROLIFERATION OF D4 HARDWARE

In addition to the systems discussed, a number of other systems have been designed using the D4 format. To illustrate the successful utilization of packaging commonality, a display, as shown in Fig. 29, was constructed and placed on exhibit by Western Electric at the International Telecommunication Conference in the fall of 1979 at Geneva, Switzerland. The individual systems comprising the display are:

(*i*) MX2-L Digital Lightwave Multiplexer Terminal, which interfaces T1 or T1C digital lines to FT2 lightwave facilities

(*ii*) DCT Digital Carrier Trunk Terminal, which provides a direct interface between No. 1 ESS and T1, T1C, or T2 digital facilities

(*iii*) LT-L Connector Double Digroup, which offers an economical means of terminating analog on the No. 4 ESS

(*iv*) The D4 Channel Bank, D4 Mode 5 Channel Bank, and *SLC*-96 Systems, which have been described earlier.

XI. SUMMARY

The D4 digital terminal is an integrated composite of efficient and economical bank assembly hardware, plug-in unit, component, and integrated circuit physical designs. High production levels have encouraged continual improvement and cost reduction since its inception, while its attractive features have resulted in a proliferation of the design through a number of systems.

XII. ACKNOWLEDGMENTS

The authors would like to acknowledge the contributions of the many people who made the success of these systems possible.

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D4 Digital Channel Bank Family:

Custom-Integrated Circuits for Digital Terminals

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This article describes the design steps for generating custom and semi-custom integrated circuits for digital terminals. The design styles and processing techniques are discussed with special emphasis on the interaction of the device organization with the system organization. Metal-oxide-semiconductor technology makes possible high-packing-density custom integration. Logic conversion is verified by simulation, layout is performed automatically, and timing is verified by using layout information as input to the timing simulator. Gate arrays facilitate semi-custom designing at low cost for modest scales of integration. The same design automation tools are used for both custom and semi-custom integration. Complementary bipolar integrated circuit technology realizes high-performance analog circuitry and can be combined with buried injector logic to integrate both analog and digital circuitry on the same chip. The combination of these technologies offers cost-effective system integration for digital terminals.

I. INTRODUCTION

Custom-integrated circuits offer significant cost savings for system applications. These savings are achieved by using fewer printed-circuit boards, connectors, and less hand wiring, thereby leaving fewer components to test and assemble and requiring less physical space. This article describes three types of custom-integrated circuits: (1) Custom metal-oxide-semiconductor (MOS) very large-scale integration (VLSI), (2) bipolar gate array, and (3) custom-analog complementary bipolar

integrated circuit (CBIC) combined with analog-digital buried injector logic (BIL) bipolar.

The technology for the digital terminals described in this article was determined by the following considerations. MOS technology offers the advantages of a high packing density for a large number of gates. In addition, the complementary MOS (CMOS) option permits chip power dissipation to be very low. Bipolar gate arrays are especially attractive for the use of minimum work force when gate counts are fewer than 1000 and when the volume is low. Both MOS polycells and bipolar gate array layouts permit quick turnaround for design changes. The CBIC is the best means for realizing high-performance analog functions. The CBIC-BIL combination allows digital logic to be put on the same chip with the analog functions, thereby achieving high packing densities. Whatever the technology choice, the effective support of the system organizations by the device organization has led to a rapid growth of custom large-scale integration (LSI) in the Bell System. Close mutual cooperation between system and device organizations is essential for successful integrated-circuit design and manufacture.

This article is divided into three sections. In the first section custom MOS VLSI chips designed for the D4 channel bank, *SLC**-96, and dataport digital terminals are discussed. The design steps from logic design through manufacture are described. In the second section, gate array technology and design techniques are described. This section includes an introduction to the gate array approach and the motivation for using it. The design steps from logic to manufacture are described, along with the various custom chips for the D4 system. The last section describes the complementary bipolar integrated circuit and the buried injector logic bipolar technologies. Examples described include circuits used both in the channel units and the common equipment of several versions of digital banks.

II. CUSTOM MOS VLSI INTEGRATED CIRCUITS

2.1 Introduction to VLSI custom logic

Over the last six years, custom MOS logic integrated circuits at Bell Laboratories have evolved from 1000-transistor LSI chips to VLSI chips containing tens of thousands of transistors. This evolution has been made possible by two major factors—process technology and design aids. Processing advances have resulted in the reduction of the design rules for custom logic chips from 7.5 μm to the current 3.5 μm. Thus, a chip today has approximately one-quarter the area of the corresponding chip six years ago that had the same logic complexity. In addition,

* Trademark of Western Electric.

Table I—Chip statistics

Code Name	Technology	Number of Gates	Number of Transistors		Operating Frequency (kHz)	Nominal Power (mW)
			Polycell	Memory		
257A	7.5-μm NMOS	250	850	—	3150	350
257B	7.5-μm NMOS	230	730	—	6300	250
229AC	7.5-μm NMOS	500	1580	—	1544/1576	425
229AA	5.0-μm NMOS	1300	4380	—	2048	450
229AB	5.0-μm NMOS	2300	8500	—	1544	445
229AD	5.0-μm NMOS	1960	6000	—	1544	650
257D	5.0-μm NMOS	850	2980	—	56	410
257B	5.0-μm CMOS	2000	7000	—	1544	8
229AG	5.0-μm NMOS	760	2900	—	1544	310
229AR	3.5-μm NMOS	1000	3330	—	4	150
229W	5.0-μm NMOS	600	3020	7200	1544	580

the change from P-channel MOS (PMOS) to depletion N-channel MOS (NMOS) or CMOS has improved the speed performance and reduced the chip power dissipation dramatically. Accordingly, system designers working with transistor-transistor logic (TTL) chips have found it particularly advantageous to cost-reduce their systems by replacing TTL dips and PC boards with a single custom integrated circuit (IC). Besides the obvious reduction of parts, cost savings are achieved by reduced labor costs, increased reliability, decreased system power dissipation, and reduced assembly facilities. Nowhere at Bell Laboratories has this cost reduction been more in evidence than for digital terminals. Eleven custom MOS chips have been designed and manufactured for the D4 channel bank, dataports, and the *SLC*-96 systems (see Table I).

Custom NMOS logic (enhancement and depletion) development at Bell Laboratories has followed NMOS memory development. This strategy has allowed custom NMOS logic chip designs to have the benefit of memory development and fabrication experience; the result is minimal difficulty in achieving high chip yields and high reliability of the custom-designed logic chips with advancing technologies. Both in 5-μm enhancement NMOS and 3.5-μm depletion NMOS, the first logic chips designed in the technology became fully operational without requiring process modifications. Recently, CMOS technology also has become available for custom logic VLSI chips. Currently, 5-μm CMOS custom chips are designed routinely, with 3.5-μm CMOS designs beginning in the second half of 1981.

Custom MOS logic chips at Bell Labs use the polycell design approach. Polycells are predesigned and pre-characterized logic elements (e.g., inverters, flip-flops) that are used to build a function. They all have the same layout height but vary in width, depending on logic complexity. All cell inputs and outputs occur along the cell boundary

at fixed distances called grids. Polycells are laid out according to the appropriate design rules—via interactive layout software in the case of NMOS or by an automatic program in the case of CMOS. The automatic program for CMOS uses symbolic coding to yield polycells that are free of design rule violations. In the case of NMOS, the polycells are thoroughly checked automatically for design rule violations by use of a layout characterization and verification program. For both technologies, programs exist so that all appropriate transistor sizes and capacitances are automatically calculated and put in the appropriate format for circuit timing simulations. In the chip layout phase, the polycells are placed in rows and the layout software optimally connects the appropriate polycell inputs and outputs, leaving a chip pattern of polycell rows and routing interconnections between the rows. Protection input devices, pull-up resistors, and output buffers are placed between chip pads. An example of a polycell chip is shown in Fig. 1. The integrity of the chip design is maintained by having a common connectivity description language, called logic simulation language (LSL),[1] for the design aids (simulation and layout) that describe the logic gates and their interconnections. The result of the polycell approach to chip design is a quick design cycle that is error free and highly flexible for last-minute logic changes.

Logic designs that employ synchronous clocked circuits, minimal gate delays between clocked memory elements (flip-flops and shift registers), RAMs or ROMs, and dynamic logic lend themselves optimally to VLSI chip design. Optimally means race-free, low-power dissipation and smallest chip size. Synchronous design permits various programs to be used to determine large propagation paths before actual timing simulations are run.

2.2 System organization—device organization interface

There are two types of custom MOS design modes—fast turnaround and full custom. In the fast-turnaround mode the system designer does the conversion into MOS polycells and stipulates design validity by simulating it with sequences of vectors. (Vectors are input/output patterns of logic ones and zeros.) After timing simulations are complete, the device organization takes the verified LSL description from the system organization and does the layout, processing, and testing.

In the full-custom mode, the device organization does the conversion to MOS polycells from logic schematics suppled by the system organization. The device organization then proceeds to complete the job in the same way as for the fast-turnaround mode. In either mode, the device designer is available to the system designer for consultation during the front-end system design and conversion to polycells. Also in either mode, a TTL breadboard that is input/output compatible with

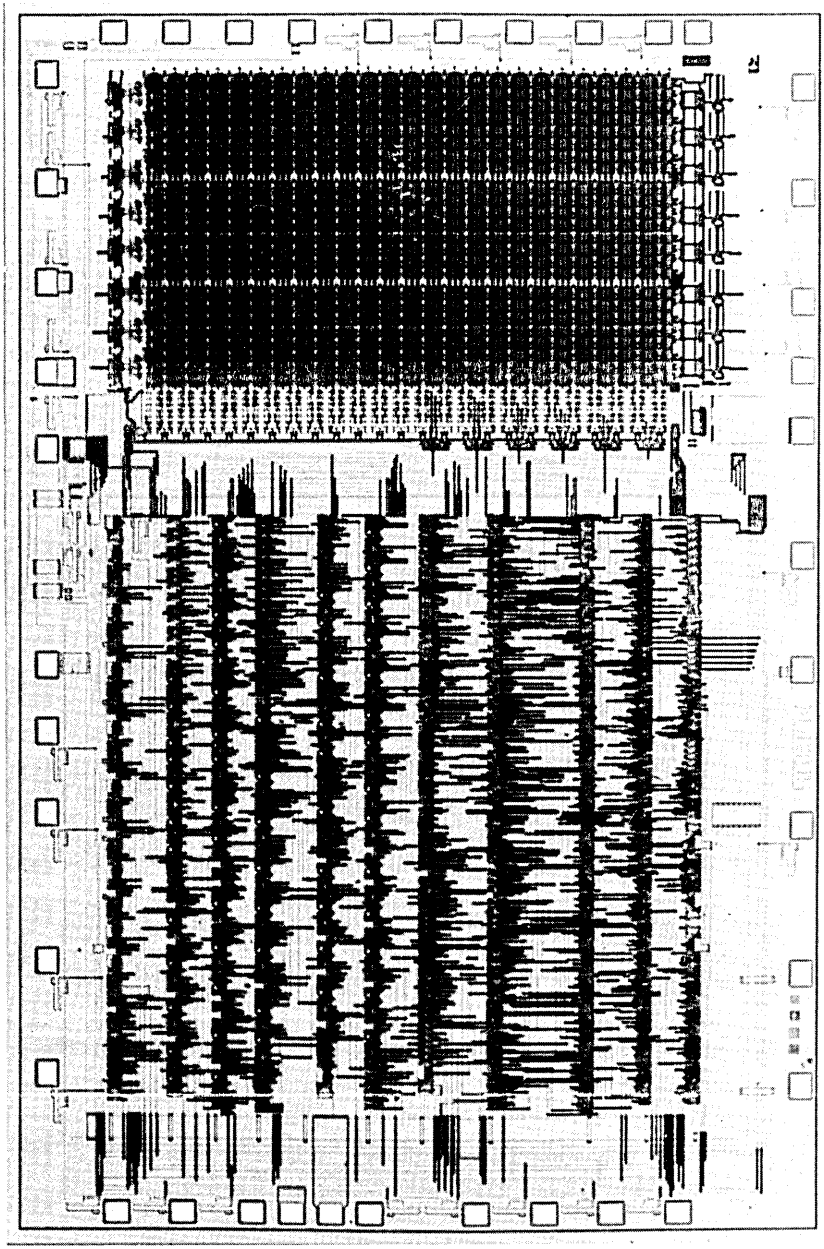


Fig. 1—Typical polycell chip.

the MOS chip and, in some cases, gate-to-gate compatible with the MOS chip, is first verified in the system environment and then transferred to the device organization for test program development. This procedure has been found to be effective in eliminating unnecessary design recycles.

An essential aspect to any custom chip design is an initial joint meeting between the system and device organizations in which chip and system specifications (e.g., frequency, voltage, and temperature variations), functional description of the system, package and testability considerations, and work force and schedule are discussed and documented. Typical current schedule times for first-model dual in-line packages (DIPs) are 8 to 12 weeks for fast turnaround and 12 to 24 weeks for full-custom DIPs.

2.3 Chip design

The first step in chip design is the conversion of the logic diagrams into MOS polycells. If the diagrams are in TTL (as is usually the case), this involves looking up the part number in a TTL catalog (e.g., SN74S163) and implementing the desired function with a minimal number of gates. For example, a divide-by-13 counter in TTL (SN74S163) consists of about 30 combinatorial gates and four D flip-flops consisting of six gates each. The equivalent MOS representation consists of four combinatorial gates and four dynamic registers, for a total of 12 MOS gates and seven polycells. It is evident from this example that the MOS representation of TTL usually involves a significant decrease in gate count. After the logic diagrams have been converted to MOS polycells, the connectivity of the polycells is described in LSL, usually according to functional blocks. These functional blocks are considered as subnetworks of LSL coding that are combined into a single network describing the entire logic design. The logic conversion is given additional logic to ensure that the chip is testable with a minimum number of test vectors.

The polycell conversion is then verified by simulating the LSL description with vector sequences and checking the MOS outputs against the known TTL outputs. This checking is done automatically by a design aid that compares the TTL and MOS vectors. After the verification, other programs are run on the LSL that determine gate delays and fanouts of the gates between clocked flip-flops or registers. By knowing the clock frequency, critical paths can be identified and altered before timing simulations are run. Critical-path improvement is usually done by substitution of a higher power polycell, logic simplification, or reclocking within the critical path.

Timing simulations are done by three types of simulators: (*i*) detailed timing, (*ii*) multiple delay, and (*iii*) mixed mode. Detailed timing takes into account all capacitance, voltage, and temperature effects and is

simulated on a user-selected time step. The multiple-delay simulator ascribes a rise and fall time delay parameter (in ns/pF) for different gate types. The determination of a gate's input and output capacitances then yields appropriate delay in ns. This permits an accurate yet much faster simulation than the detailed-time simulator. The mixed-mode simulator permits a design to be simulated before all of it is converted to MOS. Thus, MOS devices, logic gates (e.g., NAND, NOR), and functional elements (e.g., memory) can be simulated simultaneously. Options under the mixed-mode simulator include a unit delay (no capacitances or voltage or temperature effects) and detailed timing (all capacitance, voltage, and temperature effects). Hence, critical paths can be simulated in the design phase with timing while other paths can use unit delay. Chips containing thousands of MOS gates and tens of thousands of transistors are routinely simulated en masse.

The layout of the chip usually begins after the MOS LSL is unit-delay-verified. Functional block sizes are calculated, tentative input/output pad positions are determined, clock, data bus and power bus distributions, and critical paths are considered in an initial polycell placement. The design aids determine the final position of each polycell by reflecting and exchanging the cells in each row to reduce the routing area between polycell rows. All routing capacitances are then automatically calculated and the designer compares each signal loading to the values estimated in the pre-layout simulation. Post-layout simulations may be judged necessary, depending on the results of this comparison. The layout is completed on an interactive layout system by connecting input and output buffers to pads, adding pull-up resistors, and finishing power bus routing. A final design rule check of the entire layout is made with a design aid before masks are made by EBES,[2] an Electron-Beam Exposure System.

Custom MOS logic chips are fabricated at Western Electric in Allentown, Pennsylvania. Typical processing time for MOS wafers is less than six weeks. Several wafers are returned to the chip designer for testing on the SENTRY test sets. The program to test the chip is written by a test engineer who has a TTL breadboard. The *same vectors that simulated the chip* are applied to the breadboard to ensure validity of the logic design and permit debugging of the test program. Assuming that the chip passes the sequences on the SENTRY test set, packaged models (DIPS) can be delivered to the system organization within a few days for evaluation. Once the system organization approves the chip operation, Western Electric begins production.

2.4 Digital integrated circuits: statistics and system impact

2.4.1 D4 channel bank

Three custom MOS chips have been made for the D4 channel bank. They are referred to by Western Electric code name as the 257A, 257B,

and 229AC. The 257A and 257B replace six digital logic transmission equipment DIPs (TEDs) in the TTL version of the D4 transmit unit. In particular, the 257A provides all of the digital processing necessary to sample and encode each voice channel into 8-bit pulse code modulation (PCM) words. The 257B multiplexes the 8-bit PCM words together with framing bits into a single 1.544 Mb/s digital bit stream. The 229AC replaces four logic TEDs in the TTL version of the D4 receive unit. The 229AC in conjunction with a divide-by-24 counter decodes a 24-bit stream into signals that are used by a digital/analog (D/A) converter. The 229AC also provides signals for use in the receive side of the D4 bank for signaling and alarm functions. The wide usage of these chips has made necessary a design for foreign systems, referred to by Western Electric code name 229AA.

2.4.2 Dataport

Four custom MOS chips have been designed for dataport application. One, the 229AB, consists of a transmit portion, which inputs 8-bit bytes at the DS0 rate (64 kb/s) and outputs the same 8-bit bytes at the DS1 rate (1.544 kb/s), and a receive portion, which inputs 8-bit bytes at the DS1 rate and sequentially outputs the 8-bit bytes at the DS0 rate. A feature of the receive portion is a 3-out-of-5 majority gate error correction circuit, which substantially reduces the effect of facility line errors.

The 229AB is analogous to the 229AD. This chip is used for 56 kb/s data and requires its own error-correcting scheme. (The DS0 function for the subrate dataports has to be modified for 56 kb/s.) Also available is a recent CMOS version of the 229AB, designated as 257F.

The 229AB, together with two other chips, the 140H and 140J, combine to form a 64-kb/s Office Channel Unit Dataport (OCUDP). This dataport permits data from the T-line at 1.544 Mb/s to be converted to and from data at the Digital Data System (DDS) subrate speeds (2.4, 4.8, or 9.6 kb/s). The 257D contains all the digital logic and control functions for a 56-kb/s Office Channel Unit (OCU). In particular, it performs bidirectional rate conversion between the user's rate (56 kb/s) and the DS0 rate (64 kb/s) and monitors the data for control information. This chip, combined with the 229AD, yields a 56-kb/s OCU dataport.

2.4.3 Subscriber loop carrier (SLC-96) system

Three custom codes have been designed for the *SLC*-96 system. The 229AG data link chip replaces the transmit and receive sections of the Data Link Unit (DLU) of the *SLC*-96 system. The transmit section generates control signals and clocks to multiplex data bit streams from the Alarm Control Unit (ACU), the Line Switch Unit (LSU), the Channel

Test Unit (CTU) and the Time Assignment Unit (TAU). The receive section demultiplexes the incoming datastream to these four units. The 229AR data link multiplex chip enables line switch, alarm, channel maintenance, and concentrated information to be transmitted to each of two 48-channel remote *SLC* terminals. The 229W, Time-Slot Interchange (TSI) chip for the TAU digitally concentrates two standard 1.544-Mb/s PCM bit streams into a single stream with a full-access time-slot interchange function. In the transmit mode, any one of the incoming 48 channels can go out on any of the 24 outgoing trunks. In the receive mode, any one of the incoming 24 trunks can go out on any of the 48 outgoing channels. The on-chip scratch pad memory, which sets up the desired trunk connections and busy-word assignments, is written and updated through microprocessor-compatible address and data ports.

III. GATE ARRAYS

3.1 Gate array technology

If more circuitry is placed on an integrated circuit chip, fewer and simpler circuit boards are required. This results in a lower cost, better performing system that enters the marketplace sooner. The scale of integration has an impact in two ways. First, board space is saved over small- or medium-scale catalog logic parts. Second, and more important, if the system can be designed the first time to take full advantage of LSI, it results in a more nearly optimal design. Moreover, significant performance advantages accrue from the use of larger scales of integration. Approximately 80 percent of total system delays are associated with board and connector capacitance. By moving more of the interconnect wiring onto the silicon chip, these delays are greatly decreased, as is the power required to drive these on-chip lines. Higher scales of integration can be used when there is sufficient production volume to amortize the development cost. The alternative is the use of general-purpose small- and medium-scale-integrated catalog parts having a small amount of circuitry. There are relatively few general-purpose catalog parts at high levels of integration, owing largely to the difficulty of defining suitable LSI parts. Gate arrays provide a low-cost, fast-development-time alternative to LSI.

The emphasis in gate array design is on fast turnaround and low user risk. These objectives are accomplished by flexible and conservative generic chip design and an extensive computer-aided design (CAD) support package.

3.1.1 What is a gate array?

A gate array chip consists of digital circuit elements prefabricated on a silicon wafer. The circuit elements are logic primitives, typically

NAND gates, interconnected to accomplish the desired logic function. The processing steps prior to the interconnection levels are the most difficult and time consuming, while the metal wiring deposition is performed quickly. Bell Laboratories has designed a number of gate array generics (basic prefabricated wafer) for various types of applications. These range in size from 22 gates to 1000 gates and in speeds up to more than 40 MHz.

3.1.2 An I^2L gate array

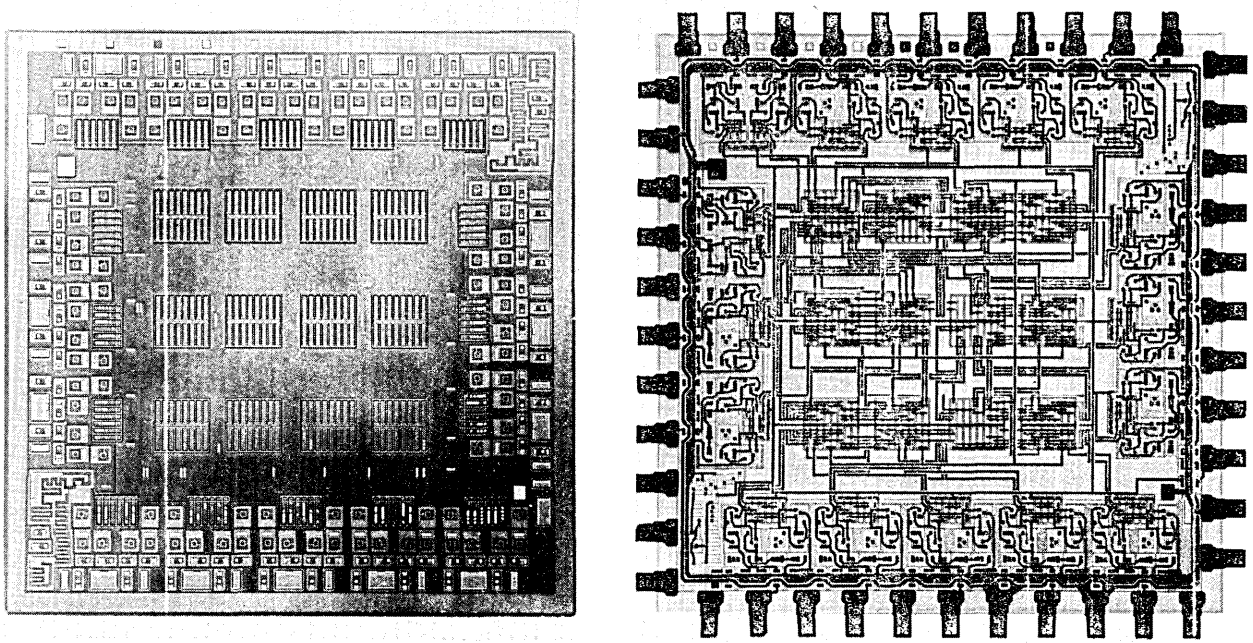
The D4 gate array before and after customization is shown in Fig. 2. It consists of 192 Integrated Injection Logic (IIL or I^2L) gates in an internal array and 32 input-output buffers on the periphery. It is fabricated in standard buried-collector, single-level metal technology. Since the array was designed for low-speed application, n+ crossunders are used at lower cost than two levels of metal. Moreover, customizing the emitter diffusion gives added routing flexibility over the cell.

The buffers translate the relatively large voltages and currents required to provide ample system noise margins to the much smaller power levels internal to the chip. Thus, the majority of logic can be done at low power levels (for this array, about 50 μW/gate) while 10-mA line driving capability is maintained. The buffers consist of a collection of npn and pnp devices, which can themselves be programmed to perform different functions at various power levels. Two voltage regulators provide the capability of driving different portions of the array at different powers, providing speed where necessary and saving power elsewhere.

The internal gates on this particular array are divided into 12 groups of 16 gates. This arrangement is advantageous because of the use of n+ crossunders. Connections between rows are made in predefined vertical channels, since the gate diffusions do not allow crossunders in gate areas. Two-level metal arrays are arranged in continuous rows. The array in Fig. 2 superficially resembles a polycell chip, except that a significant amount of interconnect is located on the gates themselves, rather than connecting at top and bottom. In addition, there are relatively large areas of the chip, and many gates, that are unused. This reflects the emphasis of fast turnaround and design simplicity over packing density.

3.2 Array design techniques

The emphasis on fast turnaround, low risk, and large volume of codes requires a heavy dependence on design aids for design and design verification. The chip shown in Fig. 2 reflects this dependence in its structured appearance. The design process for arrays is discussed below. It is emphasized that the same aids are used for all generic



BEFORE
A GATE-ARRAY CHIP CONTAINS
A STANDARD ARRANGEMENT OF LOGIC CIRCUITS

AFTER
CONDUCTIVE PATHS ARE APPLIED TO PRODUCE
A CUSTOM-DESIGNED DIGITAL LOGIC CHIP

Fig. 2—Typical gate array chip.

arrays. Indeed, some of the aids are shared by both custom MOS and bipolar gate arrays.

3.2.1 Functional description and simulation

The system designer provides a logic diagram and a logic description, the latter in Bell Laboratories' common LSL[1] language. The logic is in the form of gate array primitives (NAND) and a hierarchy of functional blocks such as flip-flops and multiplexers. The input-output buffers are also cited in the logic description. The designer also provides a set of test vectors (a truth table), which is a sequence of binary inputs and outputs designed to test for proper chip operation. The vectors are exercised to ensure information transmittal and to generate the test programs as described below.

3.2.2 Layout

Chip layout is accomplished either semiautomatically or manually. On those jobs on which there is high assurance of first-time success, the layout aids perform gate assignment and channel routing. These are accomplished quickly, since for a given generic the domains, the input-output locations, etc., are predefined and much of the time-consuming work is done once, ahead of time. The layout routine for arrays is the same as for custom NMOS polycell.

In many cases there are special layout requirements and the gate assignment and routing are done semiautomatically on an interactive system. A connectivity audit aid examines the mask description for the interconnect levels and compares it directly with the logic description supplied by the customer. It also ensures that inputs and outputs are in the correct locations, and that the power and ground are connected correctly. Only erroneous or missing connections are reported. The connectivity audit aid is central to the manual layout system. It has resulted in almost 100-percent layout confidence, since the comparison is against logic supplied by customer, with no logic translation or transformation.

3.2.3 Testing

The LSL logic description and the truth table supplied by the customer serve as input to a test program generator aid. This aid writes a program for a commercial test set, providing both functional and parametric testing. The former is specified by the truth table, the latter by a table-driven association of input-output buffer generic names and parametric tests. Thus, each buffer is always tested the same way, which gives assured manufacturing yield.

3.2.4 Introduction of manufacture

The design aids are integrated with aids to generate the manufacturing information transmitted to Western Electric, i.e., logic and mask

descriptions, test program, and specifications. In this way manufacture and design are consistent, and information flow is rapid and accurate.

3.3 Gate arrays for digital terminals

A total of 36 codes were designed for digital terminals, 19 of which were for *SLC*-96 systems and 10 for D4 channel bank export market. In both cases system cost and physical space requirements, together with the need for rapid introduction to manufacture, necessitated the use of gate arrays. The experience of D4 is typical of those systems using gate arrays. Eight codes were begun in about one month, using shared resources, with models derived for all in about nine weeks. Change in system requirements led to a delay in starting the last two codes until the time the first eight were delivered. However, during the interval when the last two were being fabricated, system prove-in could be accomplished on the bulk of the system. Two of the codes were modified as a result of the prove-in. All ten codes worked in the system five months after the first was started.

IV. CUSTOM ANALOG AND ANALOG–DIGITAL BIPOLAR INTEGRATED CIRCUITS

4.1 Bipolar IC technology

4.1.1 Introduction

The analog functions in the early D-channel banks were realized first by using discrete devices and later by using small-scale integrated circuits. Although overall performance objectives were met, it was recognized that integration on a larger scale was needed to resolve physical design and interconnection problems. However, it was also obvious that the usual analog integrated circuit process, Standard Buried Collector (SBC), would not be adequate. Two major improvements were required:

(*i*) A pnp transistor comparable in performance to the npn transistor of the SBC process was needed to implement many of the proposed circuits.

(*ii*) A high-density digital technology fully compatible with analog technology would alleviate the interconnection difficulties encountered with separate analog and digital chips.

These objectives could only be met by the development of a new IC process technology. The high-quality pnp transistor was realized by the development of the complementary bipolar integrated circuit technology. This CBIC structure is illustrated in Figs. 3a and 3b. The fabrication process is given in the appendix. The analog/digital capability was realized with the development of buried injector logic, a new device structure available from the CBIC process. Although these new technologies were not developed specifically for digital banks alone,

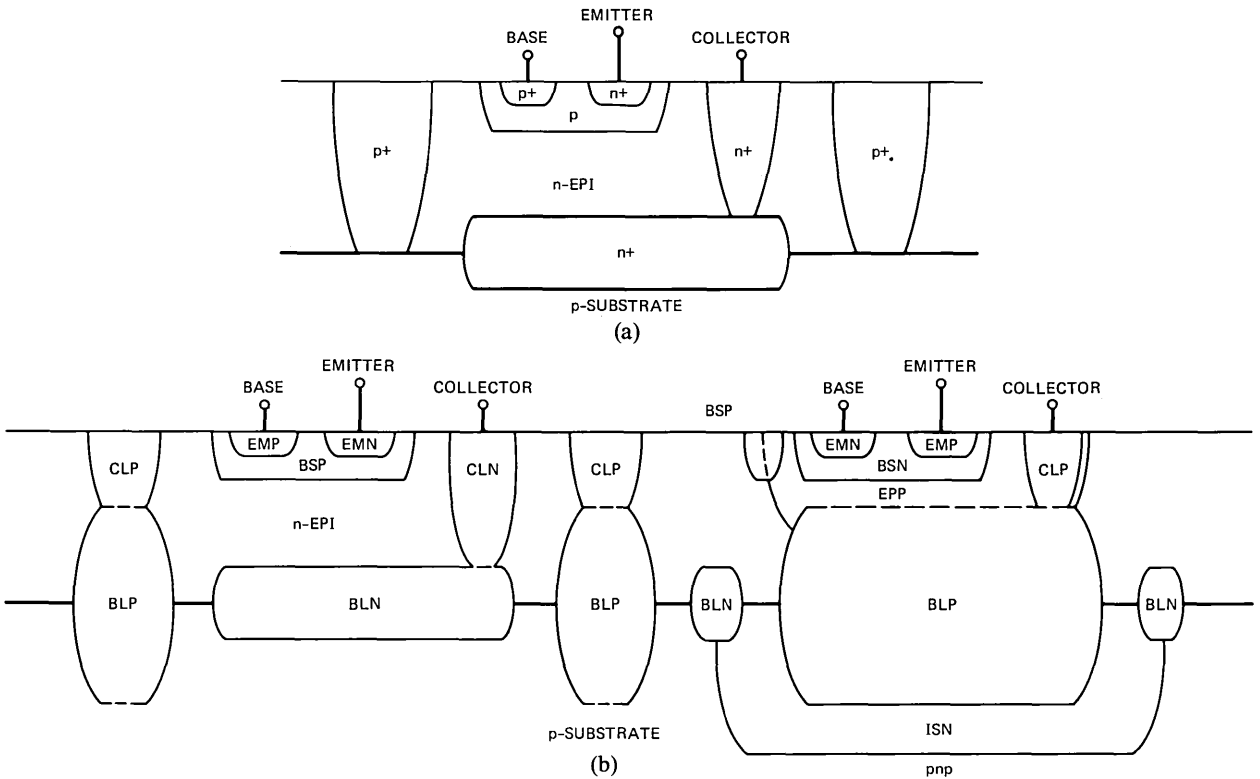


Fig. 3—Transistor cross sections. (a) SBC npn transistor. (b) CBIC npn and pnp transistors.

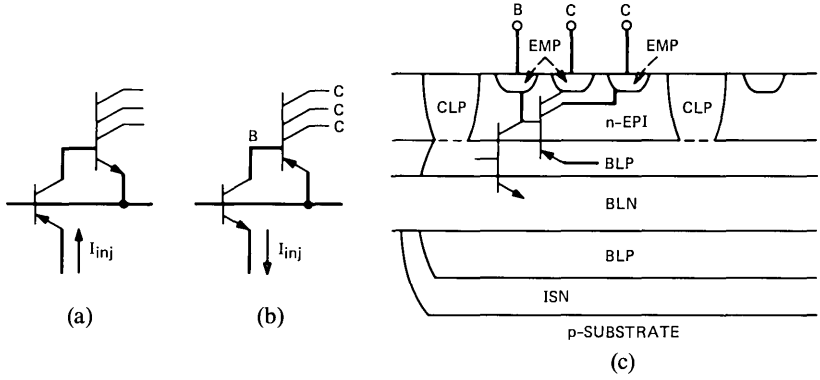


Fig. 4—Injection logic configurations. (a) Schematic representation of integrated injection logic. (b) Schematic representation of buried injection logic. (c) Cross section of buried injection logic.

D4 was one of the first systems to take full advantage of their capability.

4.1.2 Buried injector logic

With the development of Integrated Injection Logic (IIL or I^2L) in the early 1970s, it was hoped that a means for integrating high-performance analog functions and high-density digital circuits on the same chip had been obtained. Unfortunately, the process requirements, particularly epitaxial layer requirements, for I^2L and the analog functions were not readily compatible. However, A. A. Yiannoulos[3] showed that the CBIC process could also be used to obtain a novel form of I^2L. Whereas normal I^2L uses an inverted multi-collector npn switching transistor and a lateral pnp injector, as shown in Fig. 4a, Yiannoulos proposed using a pnp switching transistor and a vertical npn injector (Fig. 4b). The structure is illustrated in Fig. 4c. The n- and p-buried layers and the n-epitaxial layer form a vertical npn injector transistor. The p-buried layer, the n-epitaxial layer, and several diffused pnp emitters form the multi-collector switching transistor. Since the injector transistor is "buried," this type of logic was called buried injector logic (BIL). A major advantage of BIL is that, since the injector is buried, only the signal path interconnections are on the surface, the power being supplied by two buried layers. Thus, gate size, shape, and alignment are essentially unrestricted by power-supply considerations, which lead to very high wiring efficiency. This is illustrated in Figure 5, which shows the layout of a D-type flip-flop. It is interesting to note the variations in gate size, shape, and orientation. The high wiring efficiency compensates for the relatively large size of the BIL gate (compared with I^2L), which is due to the use of the relatively deep

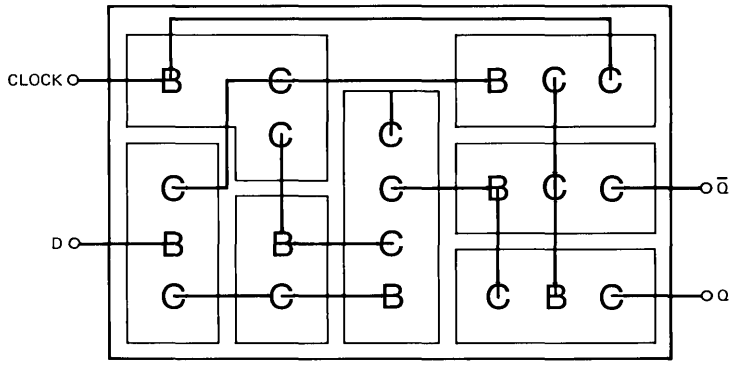


Fig. 5—Layout of edge-triggered D-type flip-flop in BIL illustrating high wiring efficiency.

diffusions associated with CBIC, basically an analog process. CBIC-BIL chips having more than a thousand gates, as well as the usual analog functions, are feasible.

It should be noted that BIL has many of the performance characteristics of I^2L. It is a low-power logic, with a delay power product of less than 1 pJ. However, it is also relatively slow, as is I^2L. Fortunately, many telecommunications applications require large amounts of logic operating slowly—sub-audio rate signaling, for example.

4.1.3 Miscellaneous components

Several other active and passive components normally are provided by the CBIC process. For example, a p-channel junction field-effect transistor (JFET) is obtained by using the pnp collector epitaxial-conversion layer, EPP, for the channel and the n-base for the gate. Two types of resistors are commonly employed—a 200-ohm/square p-base resistor, and an ion-implanted 2000-ohm/square resistor. NMOS capacitors using SiO_2 and the passivation Si_3N_4 as a dielectric are also commonly used.

4.2 Custom integrated circuits for digital banks

In the following sections, three circuits designed specifically for the D4 bank will be described briefly. In each case, realization of the required performance depended on the availability of CBIC technology.

4.2.1 555N Receive Converter

The D4 bank receive converter circuit, designed by C. Crue and H. G. Ansell, derives a clock from the DS1 bipolar-coded bit stream of data and regenerates the data. Deriving a clock from data has previously been accomplished in DS1 and DS1C digital terminal equipment

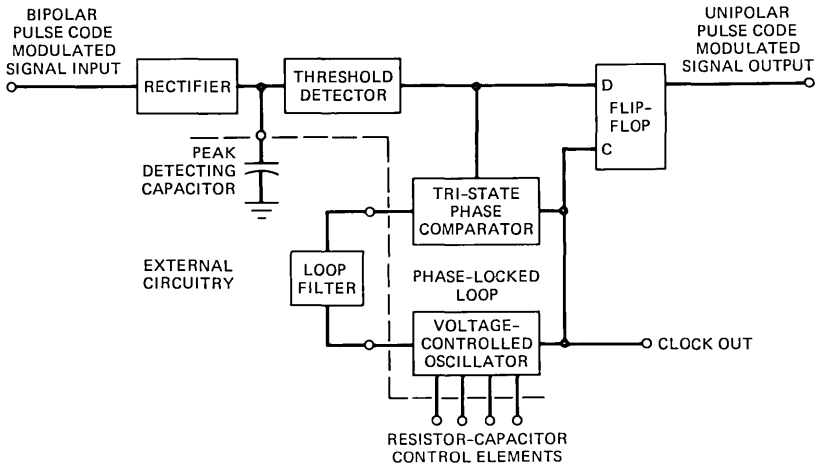


Fig. 6—Simplified block diagram of 555N Receive Converter.

using tuned inductor-capacitor (LC) or crystal circuits. The implementation of such circuits often resulted in awkward physical designs.

To improve the physical design by taking advantage of integrated circuit technology, an RC-tuned phase-locked loop (PLL) approach to clock extraction was taken. The main problem concerned the functioning of the PLL during intervals of logic zeros at the input, intervals that contain no timing information using standard bipolar coding. Reconciling competing requirements on the effective Q of the PLL was another problem, i.e., how to make the Q sufficiently large to suppress jitter, yet sufficiently small to capture the signal.

To solve the first problem, a tristate gate was used as a phase comparator in the PLL. The second problem led to a compromise in the selection of the effective Q of the loop. Figure 6 shows a block diagram of the silicon integrated circuit (SIC) realization of this circuit, the 555N Receive Converter. The loop filter and the indicated RC elements are external to the IC. The PLL consists of the voltage-controlled oscillator (VCO), the phase comparator, and the loop filter. When the input to the receive converter is a logic zero, the tristate-phase comparator ideally has zero output current, the loop filter capacitor holds its charge, and the VCO continues at its previous frequency. The PLL design includes temperature compensation for both the free-running frequency and the loop gain. In addition, this circuit also includes maintenance circuitry and an option allowing automatic shutdown of the output for no input. It operates at 5 volts and 35 mA.

The 555N Receive Converter is fabricated on a 2.8 x 2.8 mm chip using CBIC technology.

4.2.2 608D Sample-and-Hold / Comparator

The successive approximation analog-to-digital converter used in the D4 bank requires several component parts: a sample-and-hold circuit, a digital-to-analog converter, a comparator, and logic to generate the successive approximations. The 608D Sample-and-Hold/Comparator, designed by F. W. Crigler, J. J. Nahas, and D. A. Spires, performs two of these four functions along with an additional function, automatic zero adjustment.

Figure 7 is a block diagram of the 608D. The circuit is designed to operate with a dual R-2R ladder D/A converter. The comparator connects to the main legs of both the positive and negative ladders. The zero adjustment is performed using the zero adjust block and the field-effect transistor (FET) driver. The remainder of the circuit performs the sample-and-hold function.

The comparator consists of multiple stages of npn and pnp emitter-coupled pairs, resulting in a gain in excess of 84 dB and a delay of less than 75 ns.

The sample-and-hold circuit has both input and output amplifiers. The input amplifier is a sequence of npn and pnp emitter followers. The output amplifier uses a high-input-impedance source-follower followed by a Darlington-connected emitter follower. This amplifier is a single-ended voltage to double-ended current converter. The sample-and-hold switch is a diode bridge driven by positive and negative current sources directed by npn and pnp emitter-coupled pairs, respectively. The switch has a transition time of less than 80 ns.

During the automatic zero adjustment, the FET driver is used to turn on a JFET switch connecting the pulse amplitude modulation (PAM) bus to the analog ground. The zero-voltage input signal is sampled onto the hold capacitor. The zero adjustment system then adjusts the voltage on a second capacitor in such a fashion as to balance the comparator. The voltage on the second capacitor controls the current in the right-hand leg of the hold amplifier and thus adjusts the gate-to-source voltage on the right-hand source follower.

The 2.32- by 2.32-mm circuit is fabricated using CBIC technology with p-channel JFETs.

4.2.3 668A Detector / Sampler Family

The 668A Detector/Sampler integrated circuit family, designed by J. H. Green, S. F. Moyer, P. C. Davis, and J. J. Nahas, controls the timing of both the audio sampling and the sub-audio signaling on D4-bank channel units. A block diagram of the circuit is shown in Fig. 8. The receive and transmit audio sample from and to their respective PAM busses is handled with low-resistance (approximately 80 ohms) on-chip JFETs. The JFETs are switched using a fast, efficient driver that

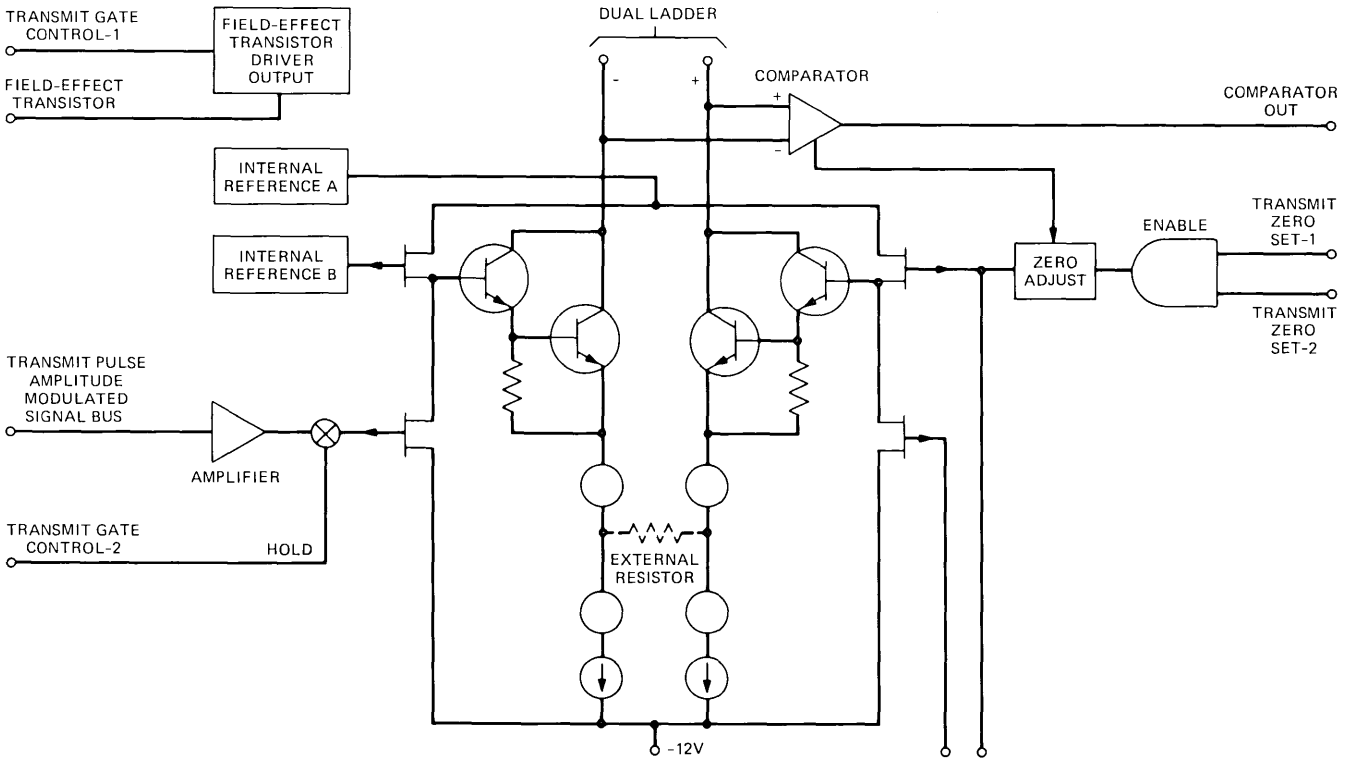


Fig. 7—Simplified block diagram of 608D Sample- and Hold/Comparator.

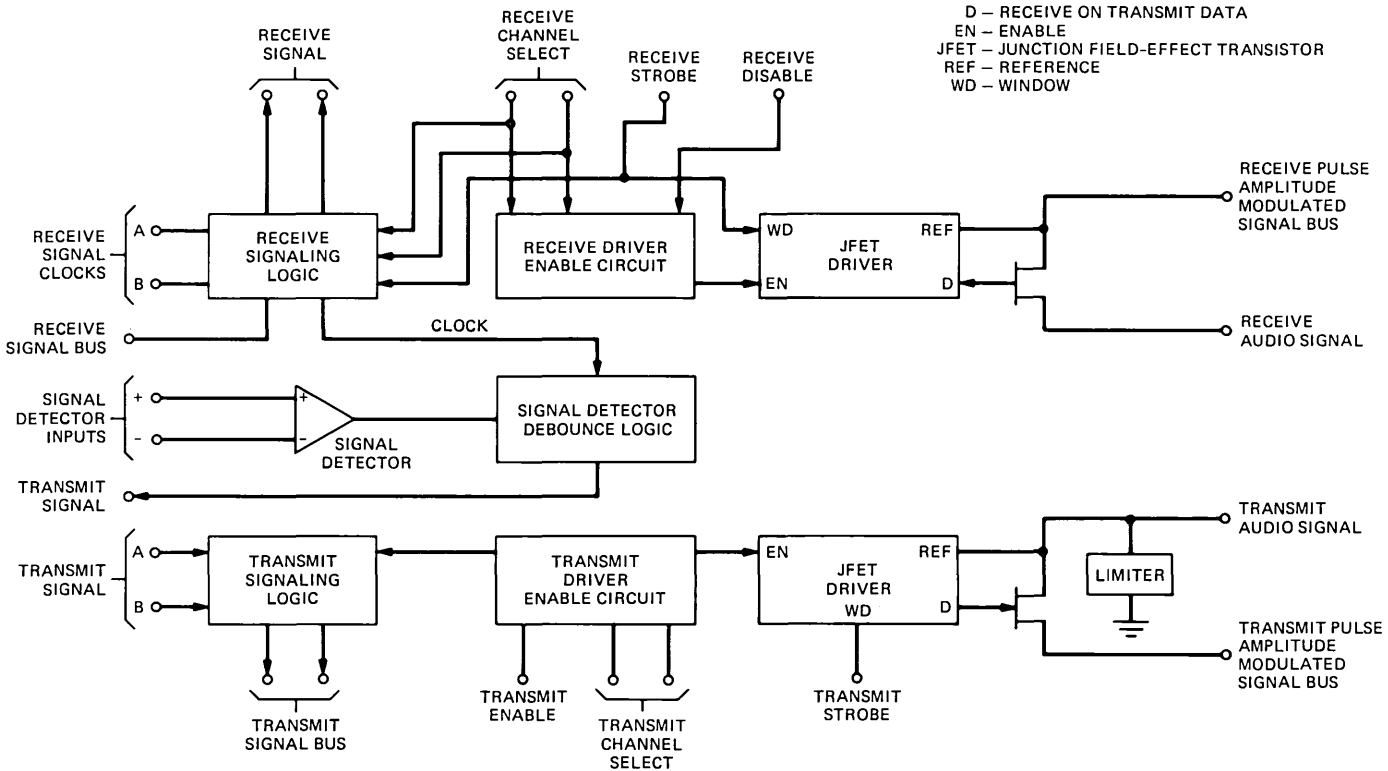


Fig. 8—Simplified block diagram of 668A Detector/Sampler.

can switch the large JFETs either on or off in less than 100 ns using only 1 mA. The JFET drivers have both select and window logic input signals. The high-speed requirements in this portion of the circuit were met using both npn and pnp emitter-coupled logic. In a typical application, the drivers are only enabled for about 4-percent of the time using channel unit selection signals, thus considerably reducing the average power required for the drivers. The sampling window signal occurs within this 4-percent time period.

The channel unit selection and sampling signals clock the receive signaling information into D-type latches. In the case of the primary or A signal, the signal is delayed using two edge-triggered D flip-flops as a shift register to prevent signaling information loss during T-carrier faults. The signaling information is transmitted to a separate off-chip line-reversal circuit.

The transmit signaling is detected using an off-chip resistor network and a simple comparator. The signal from the comparator is debounced, using a digital circuit, to prevent erroneous status signals from being transmitted over the T-carrier system. Simple open-collector outputs are used to connect the transmit signaling information to the transmit signaling bus.

The detector/sampler is a 2.56- by 2.56-mm beam-leaded silicon integrated circuit fabricated using CBIC technology. The relatively slow receive and transmit signaling logic was realized using BIL (approximately 100 gates). A number of variants of the basic detector/sampler have been developed for use in many D4 applications.

V. SUMMARY

Approximately fifty custom-integrated circuits were made for digital terminals by MOS polycells, bipolar gate arrays, or CBIC-BIL techniques. In each case, the circuitry was designed in the technology and design style that was the best match for the particular function requirements. In this manner, the choice of technologies provided a cost-effective system integration capability for digital terminals.

VI. ACKNOWLEDGMENTS

Many people have made important contributions to the successful design and implementation of the MOS LSI chips described here. The following people had chip design responsibility: D. R. Aadsen, S. Aymeloglu, S. Just, J. K. Keller, K. D. Kolwicz, D. L. Kushler, A. A. Mammele, C. R. Miller, R. W. Rau, A. R. Ross, H. R. Poon, R. R. Spiwak, and H. H. Teitelbaum. The following people had design support responsibility: W. E. Carter, J. P. Elward, D. C. Fessler, E. Heinlein, M. R. Hilt, D. R. Koch, W. F. Miller, K. G. Schaffner, T. S. Synder, J. J. Tabone, and N. J. Ziesse.

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APPENDIX

CBIC Technology

The structure of a typical npn transistor fabricated using SBC technology is illustrated in Fig. 3a. To fabricate a comparable pnp transistor, a similar structure with a reversal of doping type, n-to-p type, p-to-n type, is required. Thus, to obtain both npn and pnp transistors on the same chip, the CBIC process requires roughly twice as many diffusion steps as does SBC for the npn alone. Using the CBIC npn and pnp structures shown in Fig. 3b as guides, the CBIC process can be briefly described as follows:

(*i*) Buried layers: The npn requires the usual highly doped, n-type buried layer, BLN, which forms the internal collector contact. The pnp requires two buried layers. The first, a lightly doped, deep n-layer, ISN, isolates the pnp collector from the p-substrate. The second is a highly doped p-layer, BLP, which forms the pnp internal collector contact. Notice that the p-buried layer also forms the lower portion of the npn isolation ring.

(*ii*) Surface-to-buried layer diffusions: To make low-resistance connections to the buried collectors, deep, heavy diffusions, CLN and CLP, are used. The p-diffusion of this step, CLP, provides the remainder of the npn isolation ring.

(*iii*) Epi-conversion: The collector region of the pnp is obtained using a light p-ion implant and diffusion, EPP.

(*iv*) Bases: Both the n- and p-bases, BSN and BSP, of the pnp and npn, respectively, are ion-implanted and diffused. Note that the p-base is used to provide a "channel-stop" around the pnp transistor.

(*v*) Emitters: Highly doped, shallow n- and p-type diffusions, EMN and EMP, are used for the emitters and the contacts to the bases.

(*vi*) Contact windows and metalization: Silicon nitride, Si_3N_4, passivation is used with Ti-Pt-Au metallization. All CBIC devices developed for D4 use beam leads to connect to metallized ceramics.

The transistors obtained by this process provide $f_t \sim 300\ MHz$. The current-carrying capabilities of the npn and pnp transistors are comparable, and they are similar in area. It should be noted that since the p-isolation around the npn transistor is obtained from up- and down-diffusions, BLP and CLP, each moving part-way through the n-epi layer, the total lateral diffusion is significantly less than in the case of the single deep diffusion used in the SBC process. Thus, for a given breakdown capability, the base-to-isolation spacing is significantly less with the CBIC process. The CBIC npn transistor area is therefore approximately 25 percent less than its SBC counterpart; i.e., the increase in process complexity is partially offset by a reduction in chip area needs.

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D4 Digital Channel Bank Family:

Thin-Film Dual Active Filter for Pulse Code Modulation Systems

By R. L. ADAMS, J. S. FISHER, O. G. PETERSEN, and I. G. POST

(Manuscript received August 27, 1981)

This article describes the design of a new thin-film dual active filter for pulse code modulation (PCM) systems. A synergistic combination of circuit, silicon, and thin-film innovations has reduced the size, power, and cost of the filter and has expanded its applications. In the latest design, both the band-limiting and reconstruction filters are fabricated on a single ceramic hybrid integrated circuit in a way which significantly reduces their size, power, and cost, along with improving their performance. The filters are fabricated using laser-patterned and laser-trimmed thin-film resistors, a custom-designed complementary bipolar quint operational amplifier (op-amp), and reduced-capacitance circuit design with an innovative interconnection technique. The techniques used to minimize crosstalk between the filter sections are also described and performance data is presented. The evolution of thin-film filters for Bell System PCM systems is also briefly reviewed.

I. INTRODUCTION

The first major Bell System application of resistor-capacitor (RC) active filters was in the D3 channel bank. These filters were fabricated using tantalum thin-film resistors and capacitors[1] and beam-leaded silicon integrated circuit (SIC) operational amplifiers. They have been manufactured since 1971. Evolution of the technology has reduced the cost, size, and power of these filters and has expanded their application to other systems. The filters are currently being used in D3, D4, DCT,

*SLC**-96 subscriber loop carrier, LT1, and several other PCM systems. This article briefly reviews the history and application of these filters in PCM systems and describes the latest design: a dual filter fabricated for single in-line package (SIP) mounting.

Most PCM systems that encode and decode a voice-frequency (VF) signal require two filters for each channel. A simplified view of the D4 channel bank is shown in Fig. 1. A filter is required to band limit the signal before it is encoded to avoid aliasing from the 8-kHz sampling rate. This is often called the transmit filter. Another filter, called the receive filter, reconstructs or smooths the output from the decoder. Similar filters are required if per-channel coders-decoders (CODECs) are used.

The typical transmit-end and receive-end four-wire response limits for the transmit and receive filters are shown in Figs. 2 and 3, respectively. Since there are other sources of channel-frequency shaping, somewhat tighter limits are applied to the filters alone. Manufacturing yield is high enough that separate designs for the wider two-wire frequency response limits are not needed. The transmit filter must provide gain, 60-Hz rejection, and proper termination for the hybrid transformer. The receive filter must correct for the sin x/x frequency response of the decoder. (Figure 3 shows the total response of the receive filter, including sampling effects.) The exact amount of correction depends on the decoder and whether a shared or per-channel approach is being used. The receive filter must also properly terminate the hybrid integrated circuit (HIC) and provide enough signal power to the line through the HIC. Both filters must have low-noise and low-distortion levels. For D3 and D4 applications the gain at 1 kHz is held to ±0.035 dB for each filter to avoid any gain adjustments on the channel unit.

Figure 4 shows how the filters have evolved in the past decade. In the earlier designs the transmit and receive filters were individually packaged. In the latest design the transmit and receive filters are on the same substrate. Innovations in circuit design, silicon integrated circuit design, and thin-film technology have steadily reduced the cost of the filters (in spite of inflation).

The earliest designs[2] used 125-μm minimum thin-film feature size, 100-ohms-per-square resistors adjusted by anodization, a twin-T circuit[3,4] that required two separate tuning procedures, and individual beam-leaded operation amplifiers. Thin-film components were used for frequency compensation of the amplifiers.

In 1977, the circuit size was reduced by using 300-ohms-per-square laser-adjusted thin-film resistors and 50-μm lines realized in a dual in-

* Trademark of Western Electric.

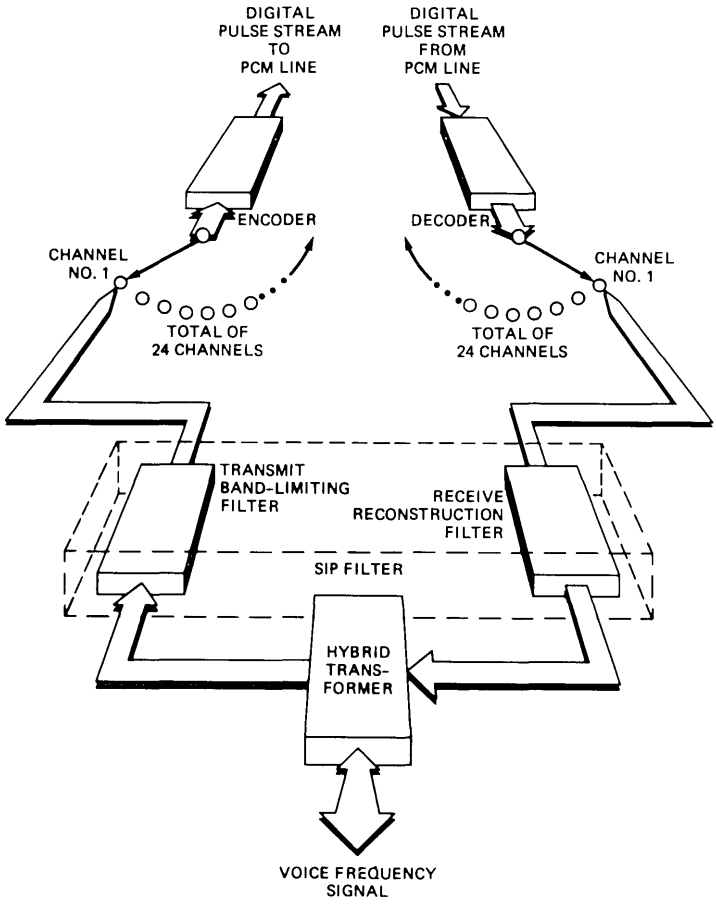


Fig. 1—PCM channel bank.

line package (DIP) format. A lower sensitivity circuit design, improved stability capacitors,[5] and an improved tuning algorithm[6] increased yields and reduced tuning time and cost. The individual beam-leaded operational amplifiers used internal frequency compensation. The same transmit and receive filter film-integrated-circuit layouts were used for all applications. However, they were tuned to somewhat different values for the different applications.

The latest design uses a SIP configuration for vertical mounting and it will be referred to as the SIP filter. Because the transmit and receive filters are packaged together, techniques to reduce crosstalk are required.

Earlier filters have many leads in addition to the few required to connect the filter to other circuits. These are necessary because the tuning procedure requires access to all passive components for mea-

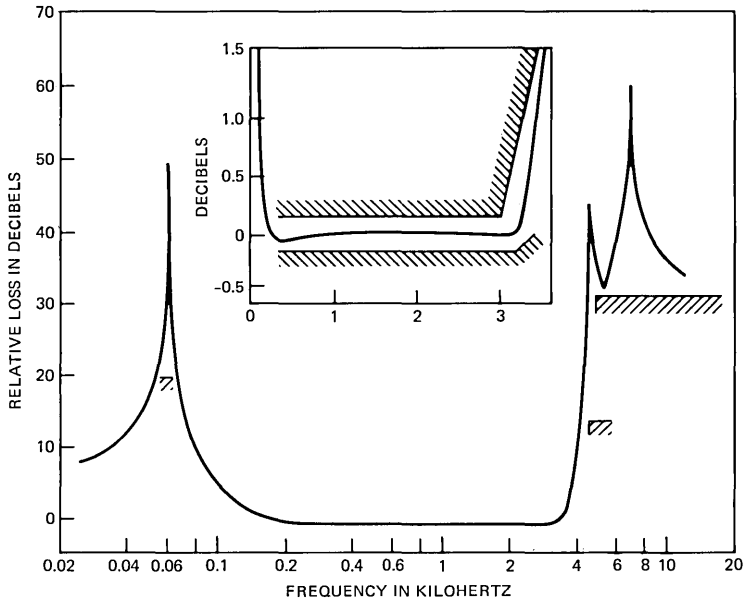


Fig. 2—Transmit filter frequency response.

surement. Some filter-circuit paths must be broken to allow this. The printed-wiring board contains interconnections to complete the filter circuit. Also, each of the four operational amplifiers (op-amps) (two per filter) is an individual SIC. The SIP filter uses a single quint op-amp SIC that consumes 50 percent less power than the four separate op-amps of the earlier designs. When an extra op-amp is installed, a filter circuit with a lower total capacitance can be used. Extra paths on the silicon replace all interconnections formerly provided by the extra HIC leads. Only the functional SIP leads are necessary, which helps size and cost reduction.

The use of a laser-patterned resistor has significantly reduced the size of the filter circuit.[7] Earlier designs used larger photolithographically produced resistor patterns. Also, a "short" RC process involving fewer masks is being used to reduce processing costs even further.[8] A more detailed description of the circuit, silicon, and thin-film design follows.

II. CIRCUIT DESIGN

There are many active filter circuits that can be designed to meet PCM filter requirements. The design must be optimized for the particular manufacturing process being used. Key considerations are parameter values, tuning method, sensitivity, noise, and requirements on

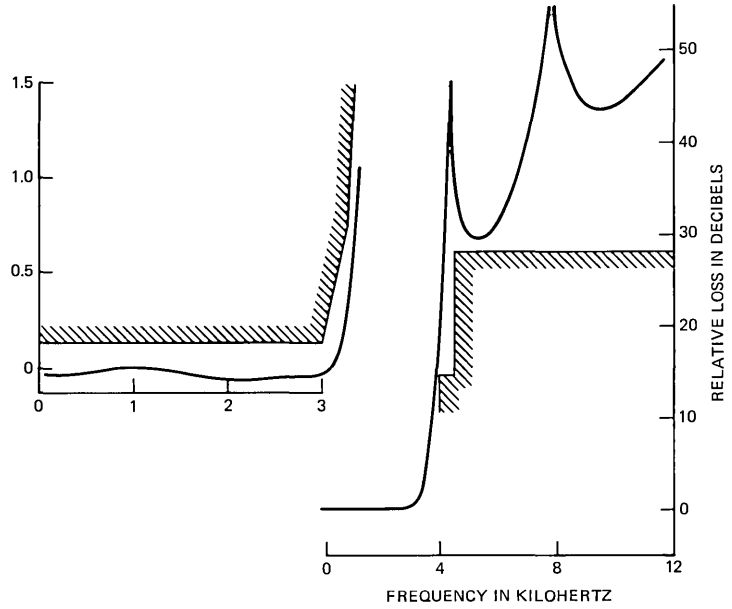


Fig. 3—Receive filter frequency response.

active devices, since these affect size, yields, process time, and performance. To take advantage of the economies of batch processing, the filter circuit size was reduced by reducing total capacitance and improving interconnection strategy.

2.1 Circuit description

Figure 5 is a schematic of the SIP filter. The receive and transmit section are described separately below.

The receive section consists of a four-capacitor input section followed by a second-order notch section. For D4 and similar applications the input signal is a narrow pulse amplitude modulation (PAM) signal from the shared decoder and the demultiplexing junction field-effect transistor (JFET) gate. The demultiplexing gate is switched at an 8-kHz rate. Although the gate is not on the SIP filter, its effect on the filter must be considered in the design. Consequently, the receive filter must be designed as a periodically switched linear network. A switched network analysis program[9] coupled to an optimization routine is used for the design. The optimization procedure determines the parameter values needed to achieve a flat pass band and the desired stop-band rejection with the pulsed input.

In the first section, the JFET demultiplexing gate and the input capacitor approximate a sample and hold operation for the narrow

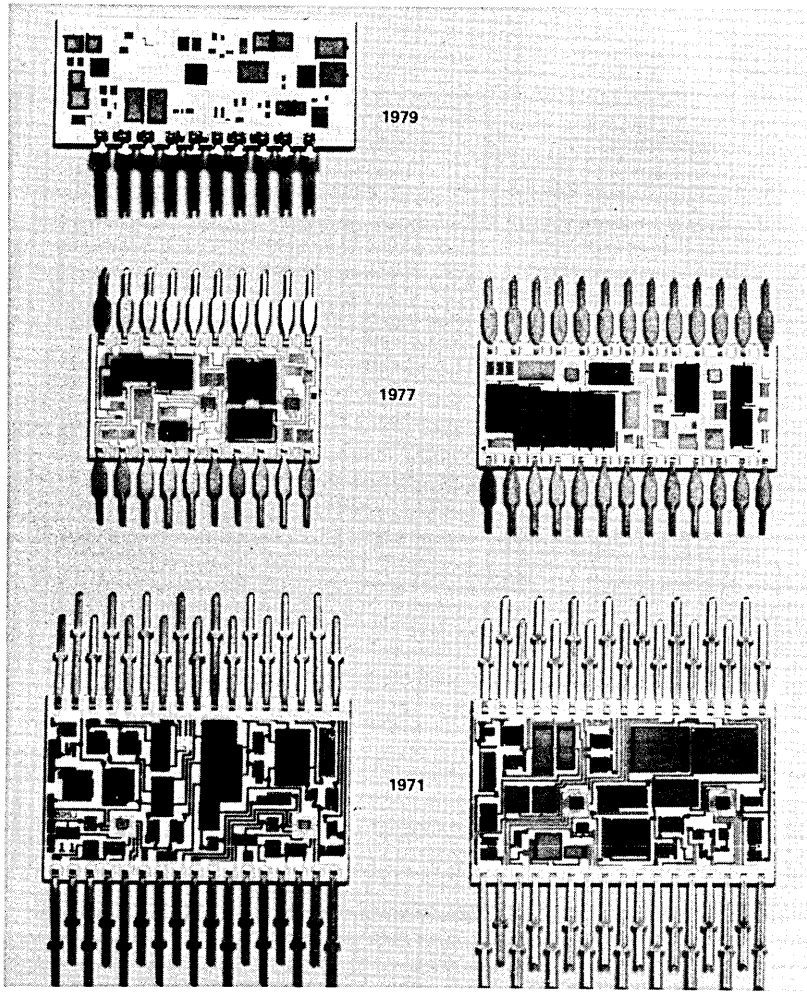


Fig. 4—PCM filter evolution.

PAM input pulses. To minimize effects of variations of JFET device parameters on filter gain, a third-order, low-pass section[10] based upon a second-order Sallen-and-Key low-pass section was chosen to follow the input capacitor. While there is still some interaction between the input capacitor and the third-order stage, this design is less sensitive to JFET device parameters than were previous designs. The second section is a Friend-biquadratic-notch section.[11,12] This section must provide enough power to drive the line through the hybrid transformer and present a proper termination impedance.

The design may be used with per-channel CODECs. In this case the

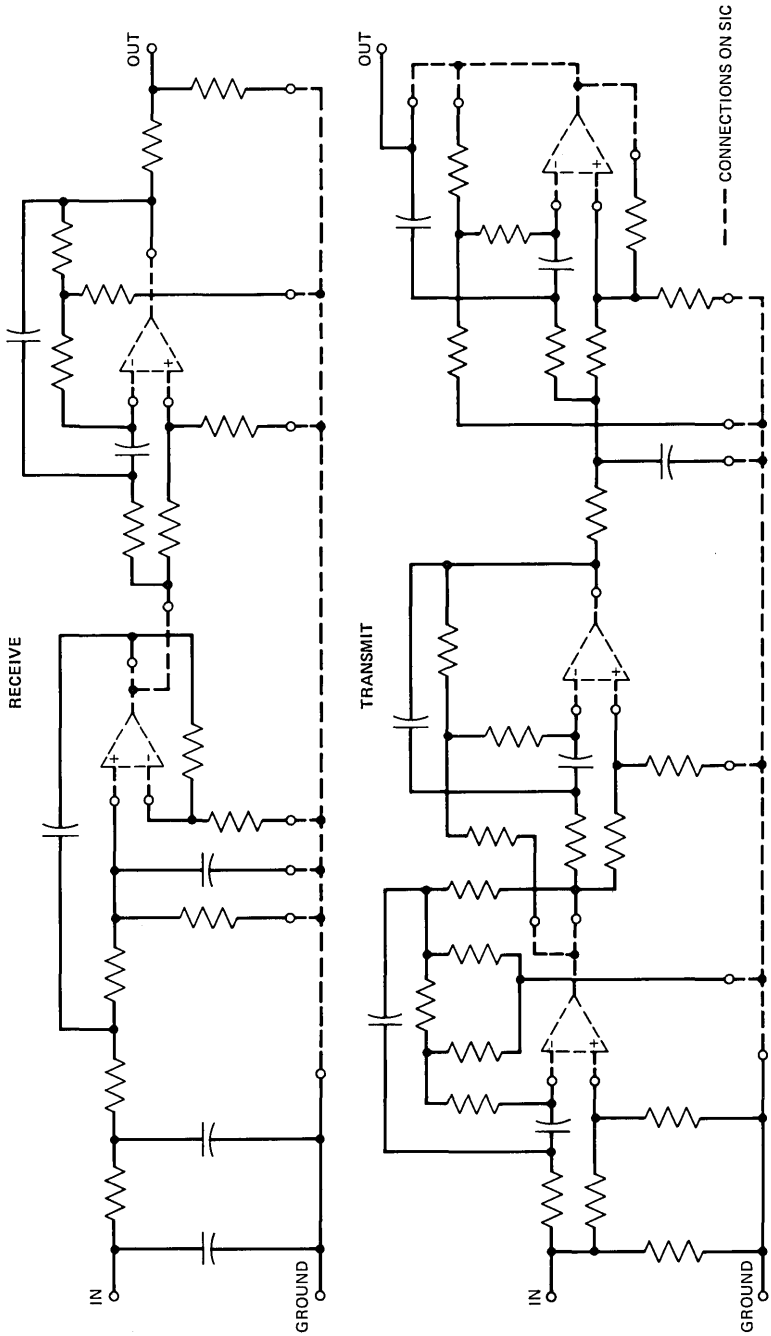


Fig. 5—SIP filter schematic.

input is not sampled but sin x/x frequency-response compensation is still required. The same ceramic circuit can be used if the input capacitor is disconnected (laser scribed open) and slightly different resistor values are used.

The transmit section is a cascade of three Friend-single-amplifier sections. The first section uses additional resistors to reduce the feedback, so-called resistive gain enhancement, and to achieve adequate flat gain. The paralleled input resistor provides proper input termination. A first-order, low-pass RC is combined with a biquadratic notch section to form the third section. The amplifier of the third section must drive the sampling/multiplexing gate preceding the encoder, so adequate settling time with this load must be achieved. The previous transmit design used a fifth-order section to realize a combined third-order, low-frequency, high-pass section and a second-order, higher frequency, low-pass notch. However, although the sensitivity of this stage was adequate, a lower capacitance design could not be achieved without increasing noise. Consequently, a 60-Hz notch section and the low-pass notch are realized as separate sections, requiring an additional op-amp. To further reduce total capacitance below the level of the 1977 design, power supply bypass capacitors are omitted from the HIC.

Pole-zero pairing, section ordering, and gain levels are chosen to minimize noise and achieve adequate dynamic range. The designs are less sensitive to parameter variations than previous designs and tuning is required only to account for passive component tolerances, not for active device parameter variations.

2.2 Tuning and interconnection

In manufacture, capacitors are allowed to vary ±10 percent and resistors must be adjusted to value in the thin-film trimming process. Capacitor variations can be compensated for by measuring capacitors and adjusting resistors to values calculated to achieve the desired transfer function. Alternatively, gain measurements can be used instead of resistor or capacitor measurements. However, resistor and capacitance value measurements can be made faster than gain measurements. As we mentioned in the previous section, tuning to compensate for gain variations because of active device variations is not required in the tuning process.

Individual access is required to measure each resistor and capacitor. However, measurement access is necessary only before silicon attachment. In the SIP filter, the probe pads for measurement access are internal connections rather than edge connections to reduce the size of the layout. The shunting effect of loops of resistors in parallel with a capacitor must be broken to allow measurement of capacitor value and

leakage. Loops of resistors are broken to ease resistor measurement. (Three-terminal resistance measurements can be made, but accuracy is reduced.) After tuning the resistors, the broken loops are connected by extra beams and associated metalization provided on the SIC. The connections made on the SIC are shown in Fig. 5. The extra HIC leads and paths required on the printed-wiring board for previous designs to achieve measurement access are eliminated, resulting in substantial size reduction.

To relax resistor-adjustment-accuracy requirements, a mop-up tuning procedure is used.[6] After all capacitor values have been measured, the value of the first resistor to be adjusted is computed and the resistor is laser trimmed. The trimmed value is measured and is used with capacitor values to compute the value of the second resistor to be trimmed. Succeeding resistors are trimmed to values based on capacitor values and values of previously trimmed resistors to minimize the deviation from the desired transfer function. Using this sequential procedure, a substantial portion of the effects of resistor adjustment tolerances can be eliminated and resistor trim tolerances can be loosened.

Most of the circuits require only this parametric tuning. Because of the tight 1-kHz gain requirement, a small fraction of the circuits require an adjustment of a few resistors based on 1-kHz gain measurements made after the silicon is attached.

Somewhat different filter responses are required for the various applications of the SIP filter. These can be achieved with the same circuit if different resistor values are used. The same ceramic-film integrated circuit (FIC) and quint op-amp SIC are used for all applications. The SIP filter is customized at the laser trim stage to tune to the particular response desired using the appropriate tuning data. Significant economies result, since the different applications can use common film processing and common tooling and fixtures.

III. SIC DESIGN

3.1 Requirements

The quint op-amp SIC was custom designed for use on the SIP filter. As mentioned in the previous section, additional metalization on the SIC provides crossovers and tie-points for the HIC to reduce the number of HIC leads. With transmit and receive filters on the same HIC, cross talk is a concern, so techniques to minimize it are incorporated into the design. By sharing common circuits in the op-amp current supply and by designing peak current capability for each amplifier only as needed, a power savings is achieved. Short-circuit protection is needed only for the output amplifier of the transmit filter section. A power-

shutdown option is also provided. Universal application requires operation from ±4.75V to ±12.6V and allows for a ±16V over-voltage condition. Because of the wide bandwidth of the complementary bipolar process, on-SIC single-pole compensation achieves stability with adequate gain.

3.2 Circuit

Figure 6 shows a quint op-amp circuit diagram. There are three op-amps for the transmit section and two for the receive section. There is a current source for each section and a voltage-reference and power-shutdown circuit serving the entire SIC.

The three stages of each amplifier are of simple design, made possible by the complementary bipolar integrated circuit (CBIC) technology. This technology provides high-quality pnp transistors with β and f_T similar to npn transistors on the same SIC. Dominant pole compensation brings about a 6-dB/octave gain characteristic throughout and beyond voiceband. The approximate total voltage gain can be shown to be

$$A_{VOL} \approx \frac{w_T}{w},$$

where

$$w_T = \frac{I_{inp}}{2V_T C},\ V_T = \frac{kT}{q}.$$

I_{inp} is the total input stage current and C is the compensation capacitance. The adjustment of I_{inp} and C, within the restraint of a minimum A_{VOL}, is made to accommodate the desired noise performance and low-frequency voltage gain, to allow a reasonable compensation capacitor size, and to ensure adequate gain and phase margins at high frequencies. The resistor in series with the compensation capacitor puts a zero in the transmission characteristic to compensate for a second pole near 15 MHz.

Only the output amplifier of the transmit section is directly connected to an external lead. The other amplifiers have some circuit resistance in series to limit output current. Short-circuit protection for the output amplifier of the transmit section is provided in the standard manner.

Each filter section is powered from a separate +V supply. There is a common −V supply that is tied to the SIC substrate. To minimize cross talk, separate transmit-section and receive-section current sources are used from a common zener reference. There is a "current-mirror" circuit in the receive-section current source that guarantees, even at low-supply voltage, a minimum zener-diode current of about

200 μA to eliminate microplasma noise. The shunt resistor across the "current-mirror" circuit is used for startup. The power-shutdown circuit diverts current from the zener diode when the power-down lead is high [transistor-transistor logic (TTL) levels]. This turns off the current sources to disable the amplifiers.

3.3 SIC layout

A total of 20 beams is required to provide the op-amp circuit functions of the SIC. An additional 15 beams are required for crossovers and tie points. A 36-beam SIC has enough area for devices and for the additional metalization paths. The SIC layout is shown in Fig. 7. Superimposed on the SIC is an outline dividing the area according to function.

Electrical isolation between the transmit and receive sides of the SIC minimizes crosstalk. To assure electrical isolation the transmit and the receive amplifiers occupy separate epitaxial tubs isolated from each other by a region biased at the substrate potential. Separate positive supplies bias the epitaxial tubs with respect to the substrate. Also, the positive and negative power supply, the current sources, and the power shutdown circuitry are placed between the transmit and receive op-amps.

Power dissipated in the output transistors creates a thermal gradient across the SIC. The output stage of each op-amp is a Class AB complementary-emitter follower. Of particular concern is a change in the thermal gradient as power switches between the output transistors. Thermal gradients affect offset voltages of the op-amp input transistors so that changes can result in thermal feedback and thermal crosstalk between receive and transmit amplifiers at low frequencies. A thermal-analysis computer program was used to plan the SIC layout.

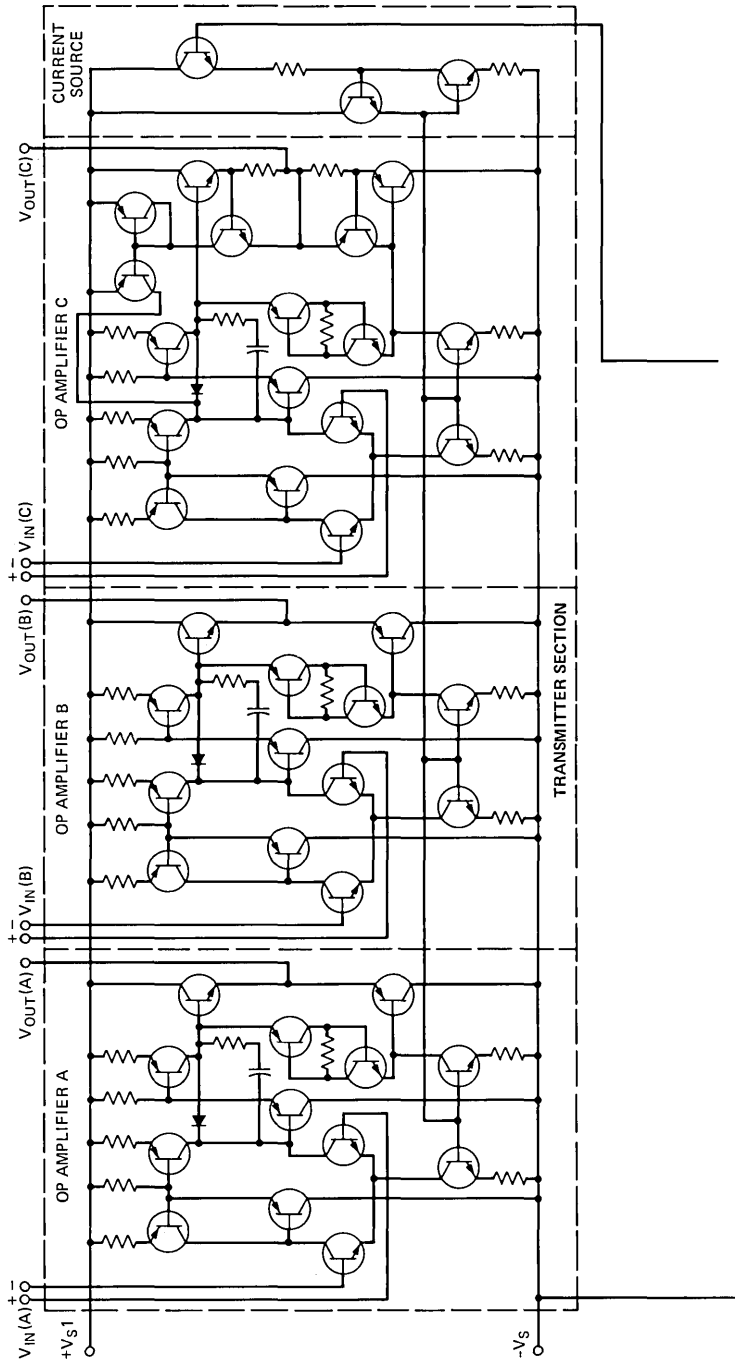
3.4 Performance

Table I lists important measured amplifier parameters.

IV. HIC DESIGN

4.1 Laser-patterned resistor

A new laser-patterned resistor was developed[7] to take advantage of the smaller feature size achievable with laser machining. Line and space widths smaller than those practical with off-contact photolithography are achievable. The new resistor has the high stability of conventionally patterned resistors and is compatible with standard RC processes. Also, for most values, the resistor is significantly smaller than conventional resistors.


CURRENT SOURCE
OP AMPLIFIER C
OP AMPLIFIER B
OP AMPLIFIER A
TRANSMITTER SECTION
$V_{OUT}(C)$
$V_{IN}(C)$
$V_{OUT}(B)$
$V_{IN}(B)$
$V_{OUT}(A)$
$V_{IN}(A)$
$+V_S1$
$-V_S$

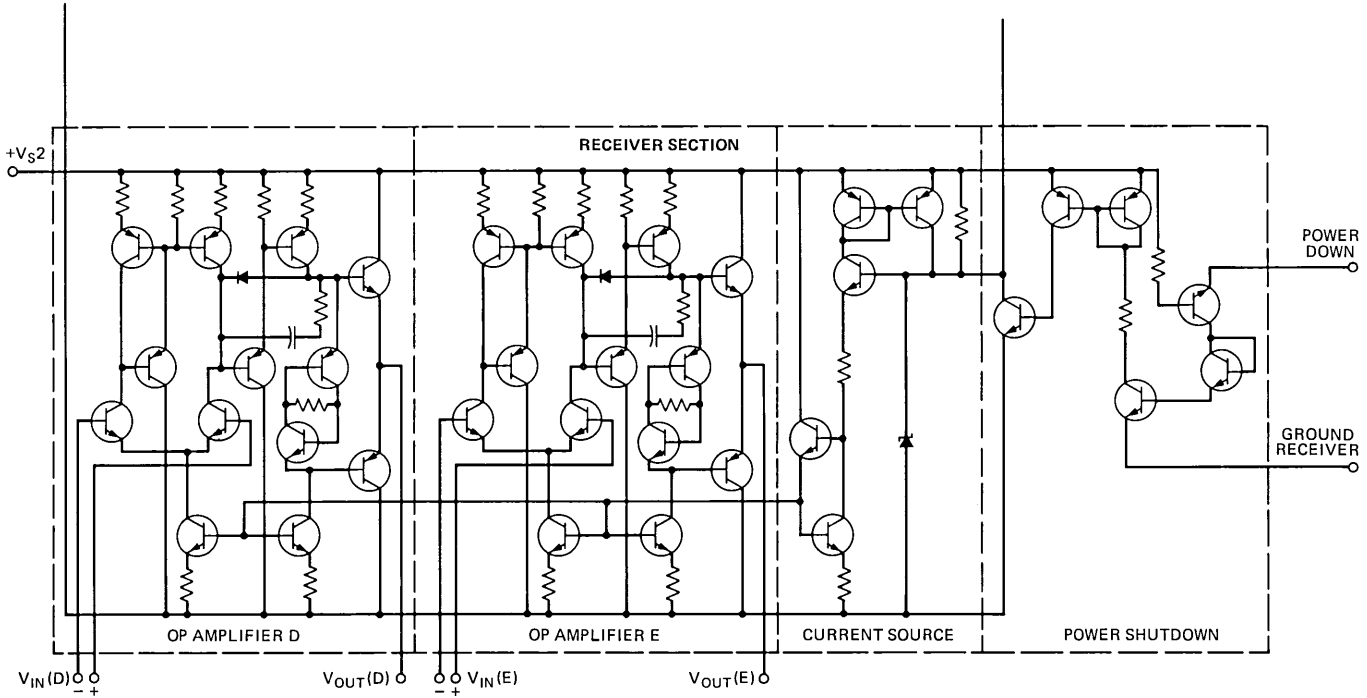


Fig. 6—Quint op-amp circuit diagram.

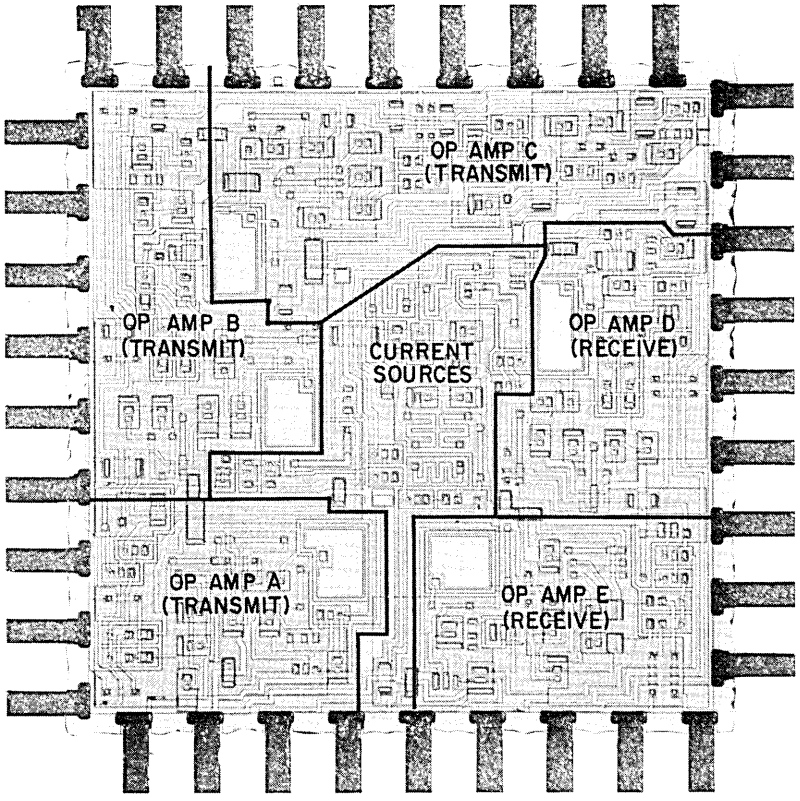


Fig. 7—Quint op-amp.

Figure 8 shows a typical laser-trimmed resistor from a standard library. The pattern is etched using standard off-contact photolithography. In the 1977 filter designs, 50-μm minimum line and space widths are used on 300-ohms-per-square Ta_2N film. The resistors are adjusted

Table I—Typical amplifier characteristics

Unity gain frequency		4.5 MHz
Phase margin		70 degrees
Power	±6V	33 mW (on)
		4.6 mW (off)
	±12V	63 mW (on)
		8.1 mW (off)
Power supply rejection ratio		3 $\mu V/V$
Isolation (Transmit to receive or receive to transmit)	$V_{in}^{T,R}/V_{out}^{R,T}$	≤−130 dB
Noise (Input referred, R_{in} = 1K)	C-message	0.63 μV (rms)
	3-kHz Flat	0.75 μV (rms)
$\Delta A_{VOL}/\Delta V_S$		−0.05 dB/volt (supply)
$\Delta A_{VOL}/\Delta T$		−0.02 dB/°C

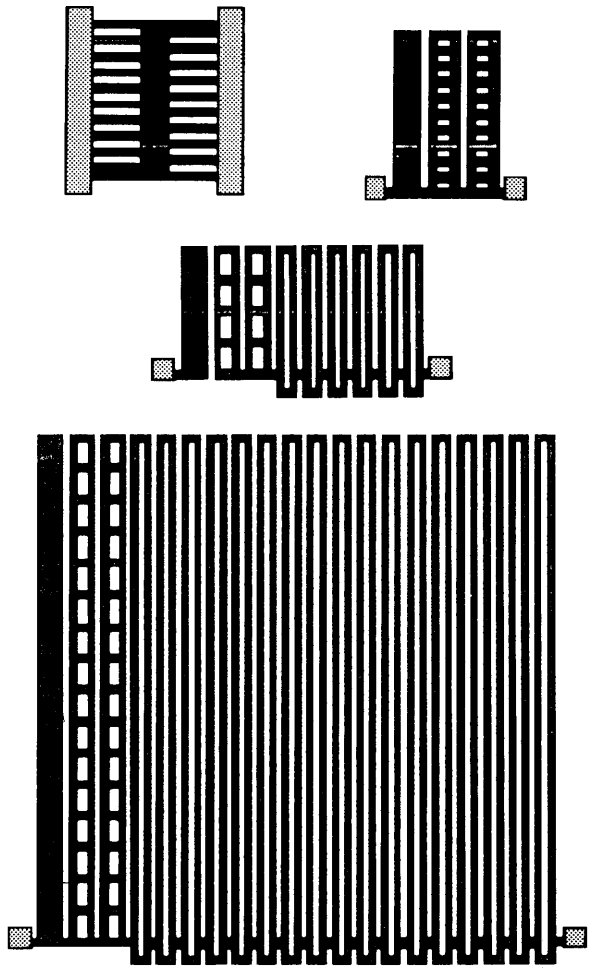


Fig. 8—Typical standard library laser-trimmed resistor.

to value by first scribing open "loop" or "ladder" shunt connections. Final adjustment is made by a continuous-beam laser trim.[13]

Figure 9 shows the design of the new laser-patterned resistor. To minimize resistance drift after laser machining, a wide-space pattern is cut after the narrow-space pattern. The process begins on a rectangular block of thermally stabilized 300-ohms-per-square Ta_2N film. About 90 percent of total resistance is realized using a laser-machined serpentine pattern of 25-μm line and space widths followed by cleaning and thermal stabilization. About a four-percent change in resistance is experienced because of the stabilization of the heat-affected zone contiguous to the laser-cut region. The resistor is now about 94 percent

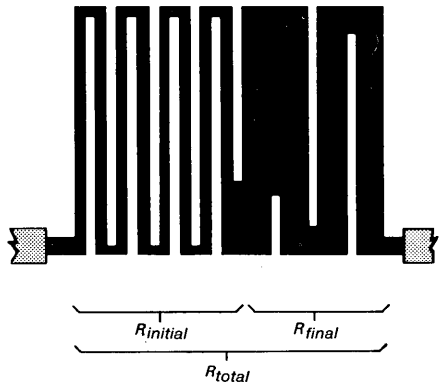


Fig. 9—Laser-patterned resistor.

of the desired value. The remaining adjustment (about six percent of total resistance) is achieved using 100-μm spacing of 25-μm laser cuts. This two-width procedure achieves resistor stability equal to conventional resistors.

In Figure 10 the areas required for the laser-patterned resistor and conventional resistor are compared. Savings of a factor of 1.5 for high values (700 kilohms) to 5 for low values (<5 kilohms) are evident.

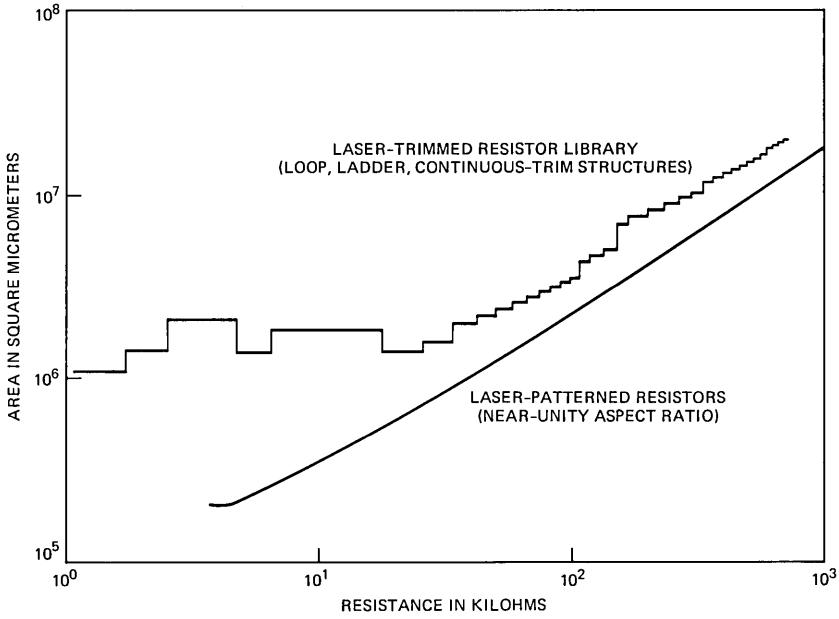


Fig. 10—Comparison of resistor areas.

4.2 Layout

Figure 11 shows the HIC with the quint op-amp mounted and leads attached, but without encapsulation applied. As previously mentioned, a large size reduction was achieved by reducing total circuit capacitance, and by using interior probe points, the laser-patterned resistor and SIC beams and metalization for tie points and crossovers. These allowed both transmit and receive sections to be realized on a single substrate equal to the size of just the previous transmit filter HIC.

Since only ten external leads are required, a single in-line package (SIP) format can be used to reduce the printed-wiring-board footprint. A new lead was designed for SIP mounting. Extensive shock and vibration evaluations were performed to verify mechanical integrity and stability of proposed and final lead designs. For a few applications, height restrictions preclude SIP mounting. Provision is made for two additional leads to be attached to the corners of the side opposite the functional leads. Instead of SIP leads, DIP leads are used and two additional DIP leads are attached to these opposite corners of the HIC to allow horizontal mounting.

To minimize crosstalk between transmit and receive sections, the most sensitive circuit nodes were identified and were separated as much as possible from high-signal amplitude nodes. A wide path, connected to −V, bisects the circuit to provide an electrostatic shield separating transmit and receive sections.

V. PERFORMANCE

Table II summarizes the important SIP-filter characteristics. The composite characteristics of the two 1977 designs are also listed for

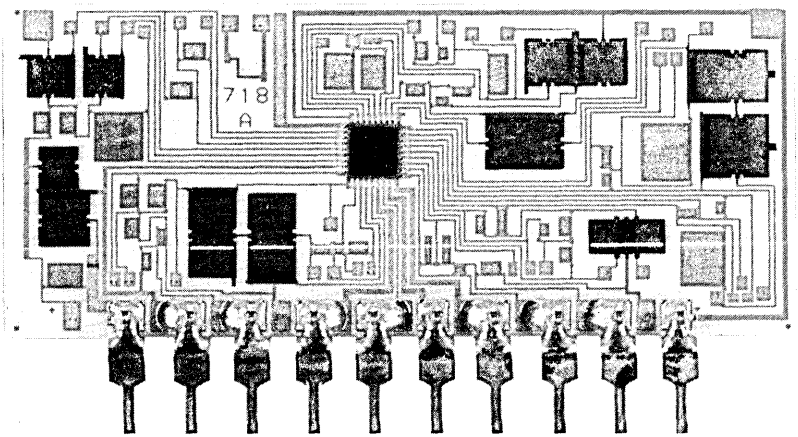


Fig. 11—SIP filter.

Table II—SIP filter performance

		1977 Design	SIP
ΣR		1.7×10^6 ohms	1.9×10^6 ohms
ΣC	Circuit	47 nF	24 nF
	Bypass	19 nF	0
Power	±12V	120 mW	63 mW
	±5V	—	30 mW
Size		0.6- by 1-in DIP 0.6- by 1.3-in DIP	0.6- by 1.3-in SIP
Distortion (typ) (1 kHz, 3 dBm0)		<−60 dB	<−60 dB
Noise (Output)	Receive	<0 dBrnC	<−1 dBrnC
	Transmit	<8 dBrn (15-kHz flat)	< 4 dBrn (15-kHz flat)
1 kHz gain		±0.035 dB	±0.035 dB

comparison. Figure 12 is a plot of measurements of the transmit portion of a sample of 50 SIP filters. The MIN, MEAN, and MAX lines are the minimum, mean, and maximum, respectively, of the ensemble of loss measurements. They do not necessarily represent the response of any one sample. Figure 13 plots the crosstalk performance between transmit and receive sections, referenced to equi-level points in the D4 channel unit. (For D4, the level at the input to the transmit section is 12.5 dB lower than the level at the output of the receive section.) Also plotted is the D4 channel-unit requirement, showing that the contribution from the SIP filter is not significant.

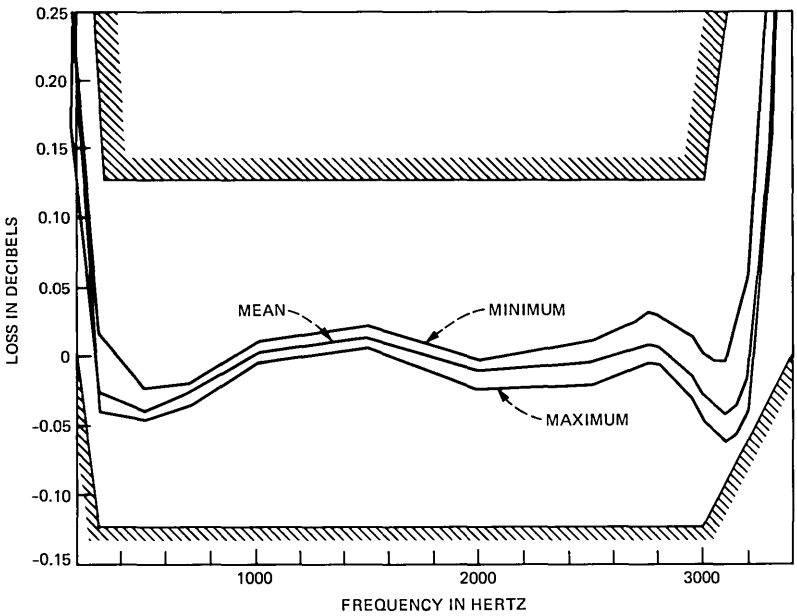


Fig. 12—Ensemble characteristics of measured SIP transmit sections.

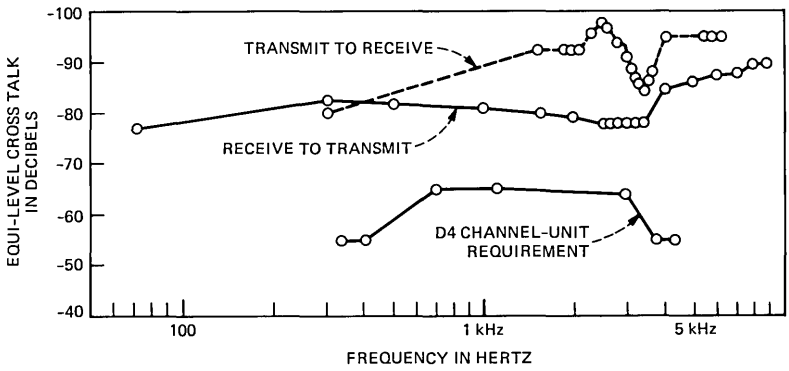


Fig. 13—SIP filter crosstalk performance.

These results, supported by extensive Monte-Carlo analysis and by high-volume production results, show that the SIP filter easily meets *D*-type channel bank requirements.

VI. SUMMARY

The design and performance of a new dual thin-film active filter for PCM channel banks has been described. Synergistic-circuit, thin-film, and silicon technology innovations have resulted in significant size, power, and cost reductions with performance improvements.

VII. ACKNOWLEDGMENTS

Many engineers contributed to the success of the design of this filter. We would particularly like to acknowledge F. J. Witt for his leadership, E. D. Finch for circuit design, L. E. Trego, L. J. Kiszka, and P. L. Scarff for thin-film design, L. D. Heck for silicon design, and M. M. Borek for silicon layout.

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ACRONYMS AND ABBREVIATIONS

2FXO/GT	Two-wire Foreign Exchange Office End with Gain Transfer Unit
4EM	four-wire E and M
ACO	alarm cutoff
ACU	alarm control unit
A/D	analog-to-digital
AGC	automatic gain control
ALM DET	alarm detector
ALM DISAB	alarm disable
ALM	alarm
ANI	automatic number identification
APD	avalanche photodiode
ARFAL	digroup A frame alarm
ARPCM	digroup A receive pulse code modulation
AR	red alarm
ATPAM	digroup A transmit pulse amplitude modulation
ATPCM	digroup A pulse code modulation
AY	yellow alarm
B6ZS	binary six zero substitution
BIL	buried injector logic
BOC	Bell operating company
BRFAL	digroup B frame alarm
BRPCM	digroup B pulse code modulation
BRPCM	digroup B receive pulse code modulation
BTPAM	digroup B pulse amplitude modulation
CAD	computer-aided design
CBIC	complementary bipolar integrated circuit
CCIS	common-channel interoffice signaling
CGA	carrier group alarm
CH	channel
CMOS	complementary metal oxide semiconductor
CO	central office
CODEC	coder-decoder
COT	central office terminal
CSU	channel service unit
CTU	channel test unit
CU SIM	channel-unit simulator
CU	channel unit
CUT	channel under test
D4MB	D4 Maintenance Bank
DAC	digital-to-analog converter
DACS	digital access and cross-connect system

D/A	digital-to-analog
dBrnC0	dB above reference noise, measured with C-message weighting at 0 transmission level point
dBTL	decibels-transmission level
DCLK	destuffed clock
DDS	Digital Data System
DEMUX	demultiplexer
DF	distribution frame
DIF	digital interface frame
DIP	dual in-line package
DLU	data link unit
DS1	digital signal one
DS0	digital signal zero
DSA	digital serving area
DSU	data service unit
EBES	Electron-Beam Exposure System
EEE	electronic equipment enclosure
EFS	error-free seconds
EIA	Electronic Industries Association
EQL	equalizer
ESS	electronic switching system
FET	field-effect transistor
FF	flip-flop
FL	fault locate
FL/OW	fault locate/order wire
FS	signaling, frame signal pattern
FT	terminal frame signal pattern
HIC	hybrid integrated circuit
IC	integrated circuit
IIL (I^2L)	integrated injection logic
ITS	integrated timing supply
JFET	junction field-effect transistor
LB	loopback code
LBO	line build-out network
LCIE	lightguide cable interconnection equipment
LC	inductor-capacitor
LCLK	loop clock
LED	light-emitting diode
LIU	line interface unit
LL	line loop
LOSP	loss of pulse code modulation
LPCM	loop pulse code modulation
LPF	low-pass filter
LSB	least significant bit

LSI	large-scale integration
LSL	logic simulation language
LSU	line switching unit
LT	loop terminal
LTS	local timing supply
MB ALM	maintenance bank alarm unit
MBTS	maintenance bank test sets
MC	multichannel
MCLK	multiplexer clock
MEM	memory
MLT	mechanized loop testing
MON	monitor
MOS	metal oxide semiconductor
MTS	Message Telephone Service
MUX	multiplexer
NEBS	New Equipment Building System
NMOS	n-channel MOS
NRZ	nonreturn to zero
NTS	nodal timing supply
OCUDP	office channel unit dataport
OCU	office channel unit
OIU	office interface unit
OOF	out-of-frame
ORU	office receiving unit
OS	out of service
OTU	office transmitting unit
PAM	pulse amplitude modulation
PCM	pulse code modulation
PCU	power converter unit
PDU	power distribution unit
PGTC	Pair Gain Test Controller
PLL	phase-locked loop
PMOS	p-channel MOS
POTS	plain old telephone service
RCLK	read clock
RCLK	receive clock
RC	resistor-capacitor
RFA	receive frame signal for digroup A
RFB	receive frame signal for digroup B
RNB2	receive, negated bit 2
RNPCM	receive, negated pulse code modulation
RPAM	receive pulse amplitude modulation
RPCM	receive pulse code modulation
RT	remote terminal

RTV	room temperature vulcanization
RU	receive unit
SBC	standard buried collector
SCC	switching control center
S/D	signal-to-distortion
SDPO	2-wire sleeve dial pulse originating
SIC	silicon integrated circuit
SIP	single in-line package
SMAS	Switched Maintenance Access System
SR	stuff request
SSI	small-scale integration
SS	special service
STAR	standard tantalum active resonator
STC	serving test center
STS	secondary timing supply
SUM	summing
SU	synchronizing-desynchronizing unit
syndes	synchronizing-desynchronizing
T1FP	T1DM framing pattern
T6CLK	transmit 6-megahertz clock
TAU	time assignment unit
TCLK	transmit clock
TED	transmission equipment DIP
TNEN	transmit, negated enable
TOGA	transmit outgoing alarm
TPAM	transmit pulse amplitude modulation
TPCM	transmit pulse code modulation
TPD	trunk processing delayed
TPM	trunk processed memory
TP	trunk processing
TPU	trunk processing unit
TPW	trunk processing wink
TRU	transmit/receive unit
TSI	time-slot interchanger
TTL	transitor-transitor logic
TU	transmit unit
UTE	unitized bay
VCO	voltage-controlled oscillator
VCXO	voltage-controlled crystal oscillator
VFDT	voice-frequency detector
VF	voice frequency
XO	crystal oscillator
ZS	zero suppression

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Shiv Verma, B.S.E.E. (Hons.), 1964, University of Jabalpur, India; M.S. Tech. (Electrical Engineering and Computer Science), 1966, Indian Institute of Technology; Ph.D. (Electrical Engineering), 1972, University of Illinois; Tuta Institute of Fundamental Research, Bombay, India, 1965–66; Department of Electrical Engineering, H. B. Technological Institute, Kanpur, India, 1966–68; Department of Computer Science, University of Illinois, 1966–72; Bell Laboratories, 1972—. While at the Tuta Institute in Bombay, India, Mr. Verma was responsible for the design of parts of a real-time process control computer. He served as the associate head of the Department of Electrical Engineering at the H. B. Technological Institute in Kanpur, India. As a member of the Information Processing Engineering group at the University of Illinois, he developed a computer system for real-time, three-dimensional display applications. After joining Bell Laboratories, Mr. Verma worked on the application of large-scale integrated circuits, microprocessors, and a high-speed digital processor in voice-band modems, and a time-division multiplexer. He has supervised groups that have developed products for the Automatic Secured Voice Communications II system and the Digital Data System, and also supervised the Digital Signal Processing Group, which is responsible for developing products for customer access to a data network. He is presently head of the Data Network Exploratory Development Department. Member, IEEE.

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