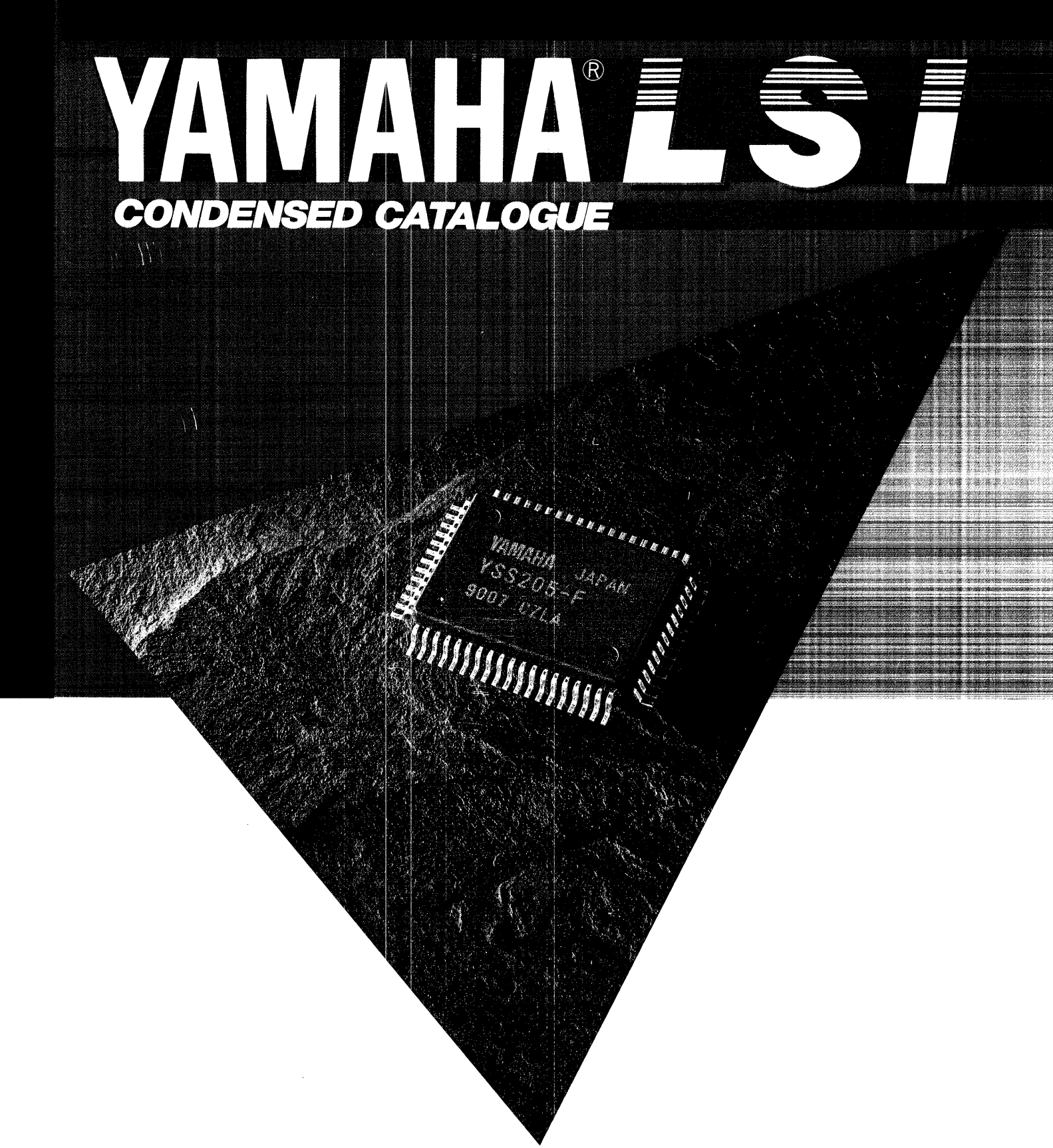
YAMAHA® LSI

CONDENSED CATALOGUE



feelin' **YAMAHA**

LSI CONDENSED CATALOG
CATALOG No.7400001
1990.10

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DIGITAL AUDIO

D/A CONVERTER

SOUND CHIP

GRAPHICS

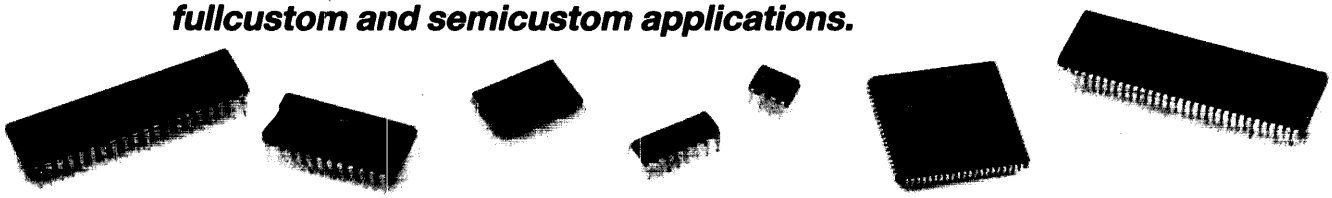
COMMUNICATION

SOUND SIGNAL PROCESSOR

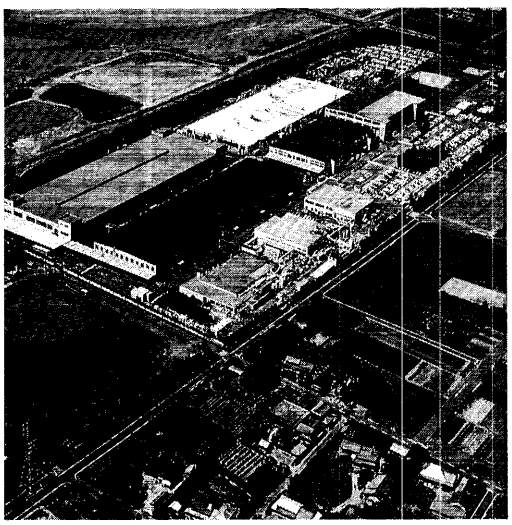
CD-I/CD-ROM

YAMAHA INTEGRATION

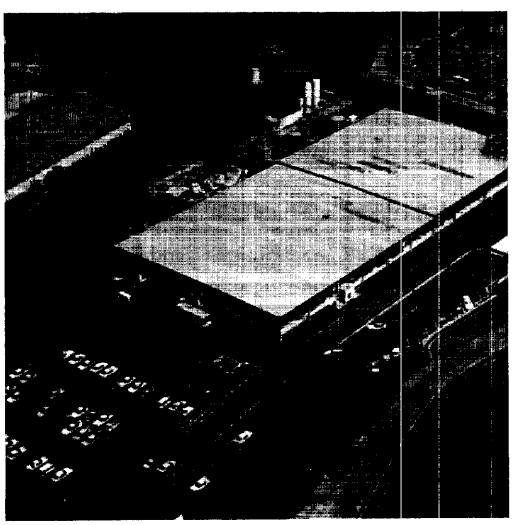
Seeking the best in sound reproduction, Yamaha has captured sound as digital information and created its own sound-oriented semiconductor technology.
By combining its experience in building electronic musical instruments with high-tech R & D work, Yamaha has mastered the art of making sophisticated LSI chips for graphics processing, communications, and fullcustom and semicustom applications.



Milestones in Yamaha® LSI Technology



The Yamaha plant at Toyooka, Japan, produces Electone digital keyboard instruments, wind instruments, and LSI circuits. This plant contains our primary LSI Research and Development Lab.



The Yamaha plant in Kagoshima, Japan – known as the Yamaha Kagoshima Semiconductor Company -- produces LSI circuits.

1969	*● IC manufacturing project initiated.*
1970	*● Construction of first IC manufacturing plant, at Toyooka, Japan, started.* *● IC production started.*
1976	*● Construction of second IC manufacturing plant, at Kagoshima, Japan, completed.* *● Development of FM sound generators initiated.*
1978	*● Dry etcher added to production equipment.* *● Projection aligner—device that aligns the mask, via projection, to allow more dice per water to be obtained—added to production equipment.*
1980	*● VLSI circuit production initiated.* *● Automatic layout program developed.* *● Manufacturing process simulator developed.*
1983	*● Marketing of semiconductor products started—devices marketed include LSI circuits for advanced high-density discs, compact discs, FM musical sound generation, digital-to-analog conversion, and pressure sensors for printing press control.* *● Automatic LSI disign system developed—performs mask-pattern generation; device layout, and standard-cell routing.*
1984	*● Marketing of custom LSI circuits initiated.*
1987	*● Production facility at Kagoshima incorporated as Yamaha Kagoshima Semiconductor Company.* *● Yamaha Corporation of America established Systems Technology Division to market components, boards and system in The United States.*
1988	*● Class 1 clean room completed* *● YST moved to San Jose, California* *● Operation of 1.2μ rule CMOS production line started* *● Marketing of LSI for teletext broadcasting started* *● Marketing of LSI for CDI started*
1989	*● Marketing of 2M, 4M bit high-speed ROM started* *● Marketing of LSI for 9600bps FAX modem started* *● Marketing of LSI set for LV player started* *● Marketing of LSI for ISDN started* *● Marketing of Dolby Pro Logic decorder started*
1990	*● Operation of 0.8μrule CMOS production line started* *● Marketing of karaoke surround processor started* *● High speed SRAM introduced* *● Marketing of facsimile controller started*

DIGITAL AUDIO

Signal Processor & Controller (& RAM) for Compact Disc player

YDC101 SPC6

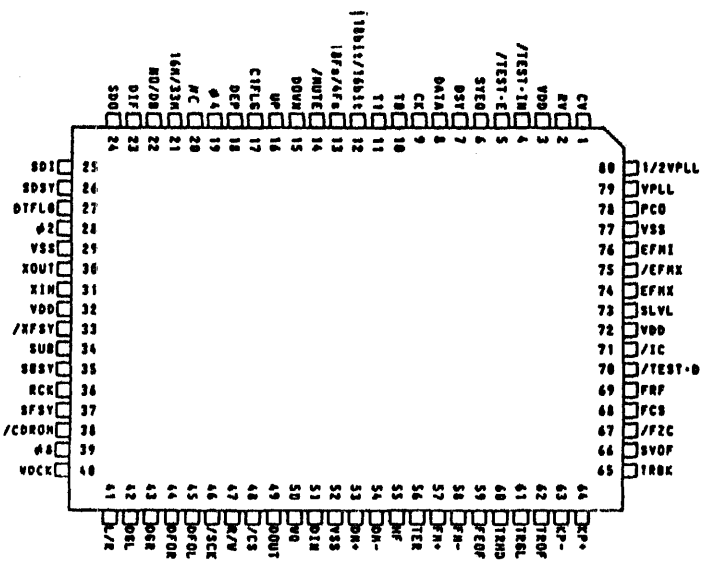
■OUTLINE

YDC101 is one-chip LSI to provide various servo control and signal processing capabilities needed in compact disc player. It has a clock regeneration circuit of EFM signals and 16K RAM to perform EFM demodulation, error detection and correction and jitter absorption. Furthermore, it performs various servo controls for focusing, tracking, feeding and discmotor. This LSI also has capability for various applications by its function of double-speed play-back, peak-level detections, digital di-emphasis and digital attenuator, digital audio interface output capability conforming to EIAJ format and 8 times oversampling digital filter.

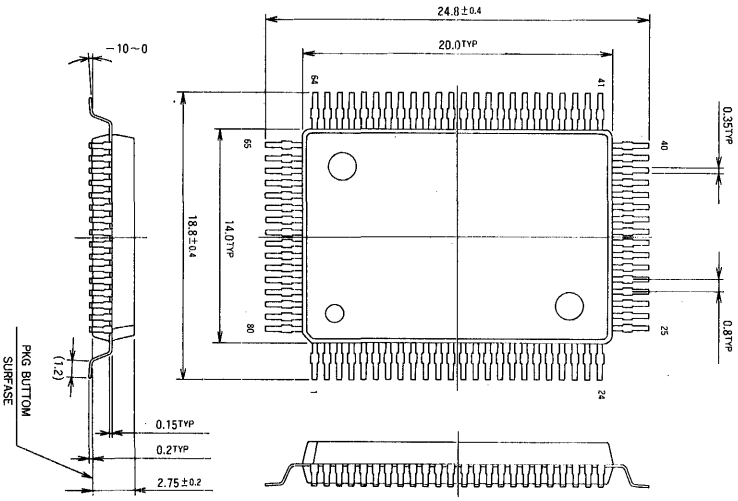
■FEATURES

- X'tal (16.9344MHz or 33.8688MHz in double speed mode) is connected to generate standard clock and timing signals for play-back and double-speed play-back.
- The built-in VCO oscillation and slice level control circuit perform clock regeneration of EFM signals, sync. signal separation and EFM demodulation.
- In addition to sub code separation and output conformed to EIAJ format, Q sub codes are CRC checked for output to a microprocessor.
- Phase between reproduced and standard clock signals is detected to control the disc motor with PWM.
- By the function of focus search control, auto search, one track kick and track-counting, each servo can be controled with a little burden of software.
- The built-in RAM buffers of the EFM demodulation signals to absorb wow and flutter of the disc (Jitter absorption range : ±4 frames) and performs deinterleave.
- Error detection and correction as well as flag processing for digital audio signals (Double error correction for both C1 and C2)
- Linear interpolation is used to replace the uncorrectable error data (up to a maximum 8 consecutive errors). And preceding data hold is applied for errors over eight. And for application as CD-ROM, prohibition of interpolation and output of error flag are possible.
- The data output is MSB first format. Digital di-emphasis processing circuit and 8 times (with noise shaper)/4 times oversampling digital filter are built in.
- Digital audio interface signal is output as conformed to EIAJ.
- Peak level detect function which outputs maximum voice level is available.
- 240 step (0.4dB resolution)digital attenuator is built-in.
- Zero cross muting which holds down mute noise of voice is available.
- 5V single power supply, CMOS, 80-pin QFP.

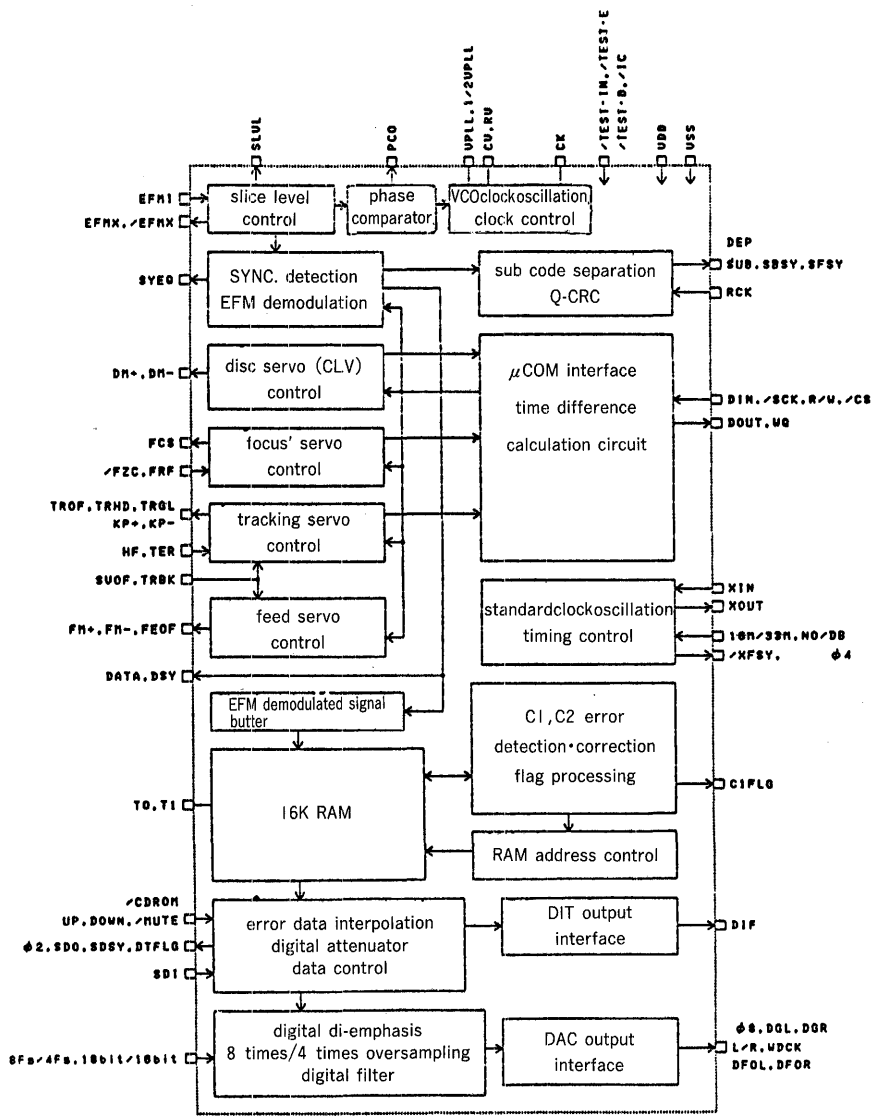
■PIN ASSIGNMENT



■ OUTLINE DIMENSIONS



■ BLOCK DIAGRAM



DIGITAL AUDIO

Signal Processor & Controller (& RAM) for Compact Disc Player

YM7121B 5PC5

■OUTLINE

YM7121B is one-chip CMOS LSI to provide various servo control and signal processing capabilities needed in compact disc players.

It has a built-in slice level control for EFM signals from optical pickup and a clock reproduction circuit; it performs EFM demodulation, error detection and correction, jitter absorption by internal RAM, and operation of various intelligent servo controls for focusing, disc motor, tracking, and feeding.

This LSI also has digital audio interface output capability conforming to EIAJ format and four-times oversampling digital filter adaptable to either 1DAC or 2DAC of MSB first output, to realize various applications.

The microprocessor command system containing conventional SPC with intensive automatic searching and track counting capabilities, and has upper compatibility at software level.

■FEATURES

- X'tal (16.9344 MHz) is connected to generate standard clock oscillation and necessary timing signals.
- The built-in VCO oscillation and slice level control circuit perform clock reproduction sync. signal separation, and EFM demodulation.
- In addition to sub code separation and output according to EIAJ format, Q sub codes are CRC checked for output to microprocessors.
- Phase difference between reproduced and standard clock signals is detected to control the disc motor with PWM.
- Command input on microprocessors administrates various servo controls for focusing search as well as tracking feed for quick access and skipping.
- In addition to automatic searching capability for quick access, track counter for high-speed searching is built in.
- The built-in RAM buffers the EFM demodulation signals to absorb wow and flutter of the disc.
  (Jitter absorption range ± 4 frames)
- EFM demodulation signals are unscrambled and de-interleaved.
- Error detection and correction as well as flag processing for digital audio signals (Double error correction method for both C1 and C2)

■ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	VDD	−0.3 ~ +7.0	V
Input voltage	VI	−0.3 ~ VDD+0.5	V
Working temperature	Top	−20 ~ +75	℃
Storage temperature	Tstg	−50 ~ +125	℃

Recommended Operating Conditions (Condition: Ta = +25°C, VDD = 5.0 ± 0.25V)

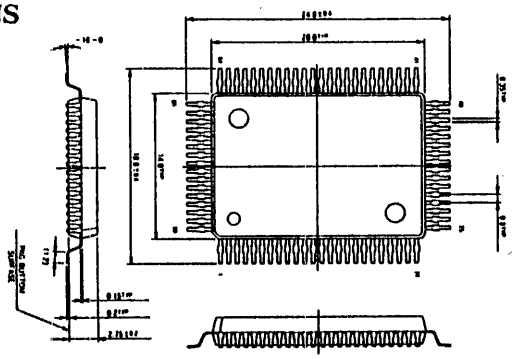
Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	VDD	4.75	5.00	5.25	V
Clock frequency	XI		16.9		MHz
Working temperature	TOP	0	25	75	°C

Electrical Characteristics (Condition: Ta = +25°C, VDD = 5.0 ± 0.25V)

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit	Remarks
Power supply voltage	IDD	VDD=5V				mA	
Output voltage H level	VOH	IDH = 20μA	4.0			V	
Output voltage L level	VOL	IOL = 1mA			0.4	V	
Input voltage H level (1)	VIE 1		3.5			V	Note 1
Input voltage L level (1)	VIL 1				1.5	V	Note 1
Input voltage H level (2)	VIE 2		2.0			V	Note 2
Input voltage L level (2)	VIL 2				0.5	V	Note 2

Note 1: Applicable to EFMI, FZC, FRF, EF and TER Terminal. Note 2: Applicable to RCK, DIN, SCK.

■ OUTLINE DIMENSIONS



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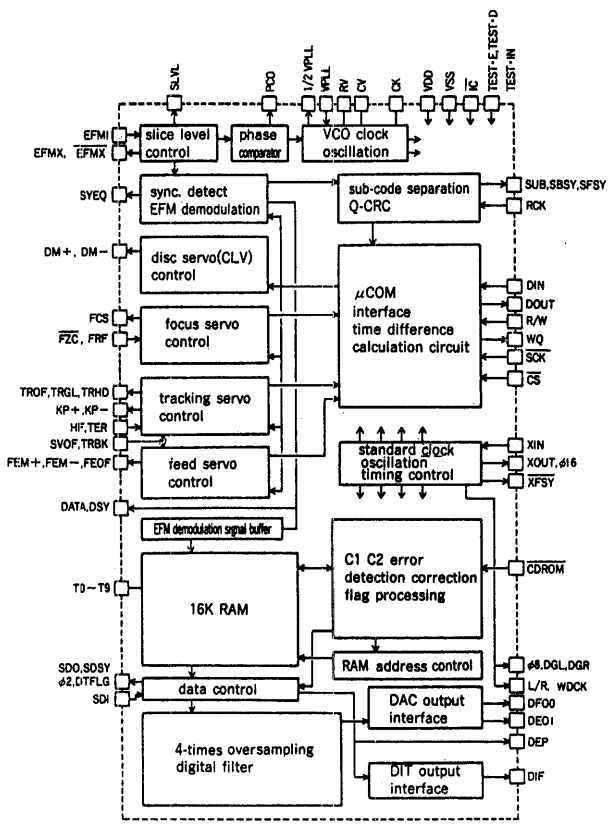


DIGITAL AUDIO

CD/CDV Digital Audio Processor

YM7402 CDVP

■OUTLINE

YM7402 is a one-chip LSI containing various circuits for digital audio signal processing used in optical multi disc compatible players as well as servo control and signal processing capabilities needed in CD players.

In addition, sequential control of tracking/feed for high speed searching, digital audio interface output, digital volume adjustment, and peak holding functions are included for use in high-grade CD players and compatible players.

■FEATURES

- X'tal (16.9344 MHz) is connected to generate standard clock oscillation and timing signals.
- EFM-PLL circuit with built-in VCO reproduces bit clock pulses.
- Built-in slice level controller
- Two switchable modes (CD/LD) are available for EFM input.
- Linear interpolation is used to replace the uncorrectable error data (up to a maximum if 8 consecutive errors). And preceding data hold is applied for errors over eight.
- The data output is in MSB first format and four-times oversampling digital filter with stop band attenuation of 40 dB or more is built in.
- EFM data demodulation and intensive error correction capabilities (double error correction for both C1 and C2).
- Buffering of EFM demodulation signals by 16K built-in RAM (Jitter absorption range ± 4 frames)
- Sub code separation and output conforming to EIAJ.
- Digital audio interface output conforming to EIAJ with arbitrary setting of channel status code.
- MSB first audio data output with switchable audio output method adaptable for bilingual laser disc.
- Facusing servo control compatible with external equipment.
- Tracking & feed servo controls by direct and automatic sequence controls for high-speed searching and linear motor.
- Built-in tracking counter allowing adjustment with a unit of one track.
- PWM spindle servo control containing FG mode realized by frequency generator connection.
- VCXO control for compatible players.
- High performance microprocessor serial interface enabling precise control.
- Digital attenuator for 0.4 dB and 240 steps is built in.
- Zero cross mute functions to suppress mute noises.
- Peak holding capability to output maximum audio level for peak level searching and level meter.
- Error flag output without interpolation for CD-ROM.
- 80-pin flat packaged silicone gate CMOS LSI, operated by + 5V power supply.

■ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	VDD	−0.3 ~ +7.0	v
Input voltage	VI	−0.3 ~ VDD+0.5	v
Working temperature	Top	−20 ~ +75	t
Storage temperature	Tasg	−50 ~ +125	t

(Condition: Ta = + 25°C, VDD=5.0±0.25V)

Recommended Operating Conditions

Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	VDD	4.75	5.00	5.25	V
Clock frequency	XI		16.03		XHz
Working temperature	TOP	0	25	75	℃

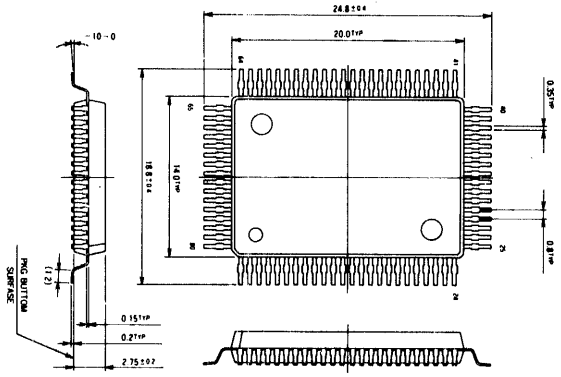
(Condition: Ta = + 25℃, VDD=5, 0±0.)

Electrical Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit	Remarks
Power supply voltage	IDD	VDD=5V				mA	
Output voltage H level	VOH	IOL=20μA	4.0			V	
Output voltage L level	VOL	IOL=1mA			0.4	V	
Input voltage H level (1)	VIH1		3.5			V	Note1
Input voltage L level (1)	VIL1				1.5	V	Note1
Input voltage H level (2)	VIH2		2.0			V	Note2
Input voltage L level (2)	VIL2				0.8	V	Note2

Note1: Must be applied for other terminals than those given in Note2.
Note2: Must be applied for /CS, DIN, / SCK, R/W terminals.

■ OUTLINE DIMENSIONS



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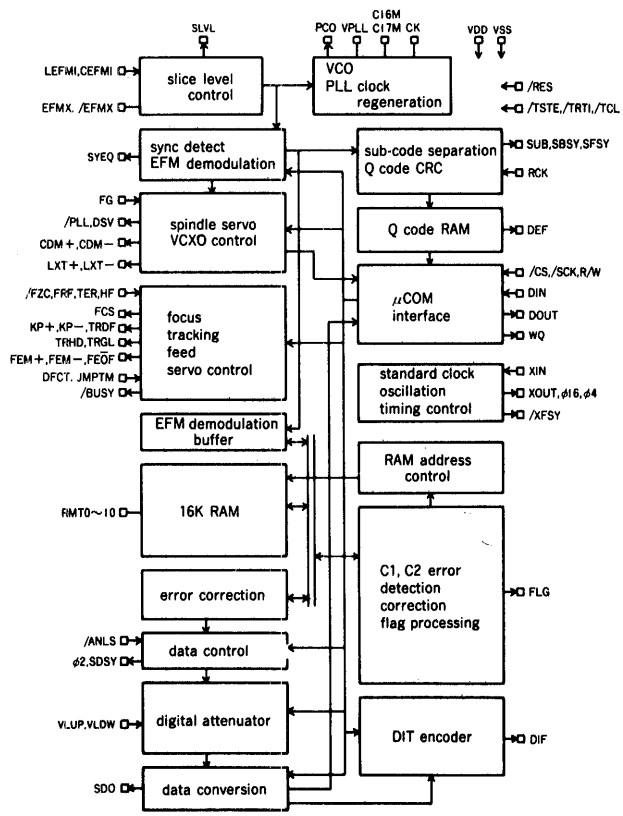


DIGITAL AUDIO

Signal Processor & Controller for Compact Disc Player

YM3805 SPC

■ OUTLINE

The YM3805 is a compact disc player signal processor (SGP) and servo controller CMOS LSI developed by Yamaha.

The YM3805 carries out the digital filtering and other signal processing useful for optical pick-up EFM signal demodulation and erroneous signal detection and correction and improved audio quality, as well all servo control (e. g., focus, disc, tracking, feed).

It is used in conjunction with the special serial input DAC YM3015 or YM3020.

■ FUNCTIONS

1. Simple external connection of a crystal activates reference clock oscillations and the necessary internal timing signals.
2. Digitalizes the EFM signal, and based on that carries out clock regeneration and synchronizing signal isolation.
3. EFM demodulates this digital signal.
4. Isolates the Q sub-code from the EFM demodulated signal, and after carrying out a CRC check, outputs it to an external microprocessor.
5. Outputs a frame phase difference signal derived from the regenerated clock and the reference clock and controls the rotation speed of the disc motor.
6. Carries out tracking as well as feed servo control for calling up the beginning of a selection and for fast forward, etc., upon input of a command from an external microprocessor.
7. Uses EFM demodulated signal buffering to absorb fluctuations in the rotation of the disc and interfaces the external RAM and signals (±4 frame jitter absorption).
8. Carries out unscrambling and de-interleaving of EFM demodulated signals in a set order.
9. Detects erroneous signals and corrects them and performs flag processing as well (double-error correction).
   Performs signal compensation, hold, and even muting.
10. Carries out digital filtering (signal break at 20 KHz) by doubling the sampling period (88.2 KHz for both the left and right channels), outputting a DAC signal. (Modes in which digital filtering is not carried out are also available.)

■ FEATURES

1. Silicon gate CMOS construction
2. 80 pin flat plastic package (saves space)
3. 5 V single power supply

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNITS
Supply voltage	V_{DD}	−0.3 ~ +7.0	V
Input voltage	V_I	−0.3 ~ V_{DD} +0.5	V
Operating temperature	Top	−20 ~ +75	°C
Storage temperature	Tstg	−50 ~ +125	°C

Recommended Operating Conditions

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNITS
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Top	0	25	75	°C

Electrical Characteristics

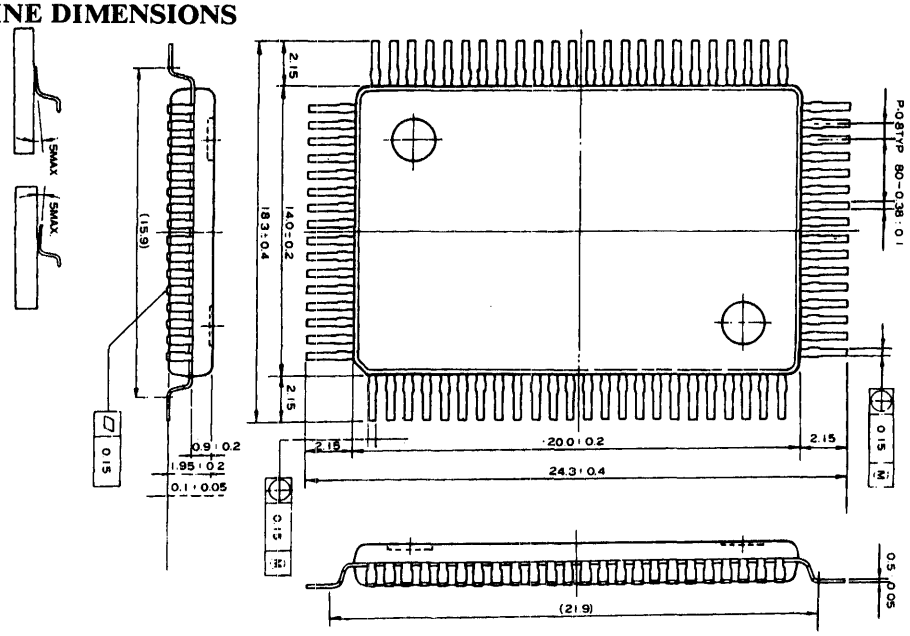
ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	REMARKS
Supply current	I_{DD}	V_{DD} = 5V		25	40	mA	
Output high level voltage	V_{OH}	I_{OH} = 20μA	4.0			V	
Output low level voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	
Input high level voltage (1)	V_{IH1}		3.5			V	(Note 1)
Input low level voltage (1)	V_{IL1}				1.5	V	(Note 1)
Input high level voltage (2)	V_{IH2}		2.0			V	(Note 2)
Input low level voltage (2)	V_{IL2}				0.8	V	(Note 2)
Input leakage current	I_{LK}	V_I = 5V			10	μA	

Condition: V_{DD} = 5.0V±5%, Top = +0 ~ 70°C

Note 1: Applicable to terminals 3.VCOI 8.EFMI 14.$\overline{FZC}$ 15.FRF 16.HF 17.TER.

Note 2: Applicable to terminals 33.$\overline{RCK}$ 38.DIN 39.$\overline{SCK}$ 54.D8- 61.D1.

■ OUTLINE DIMENSIONS



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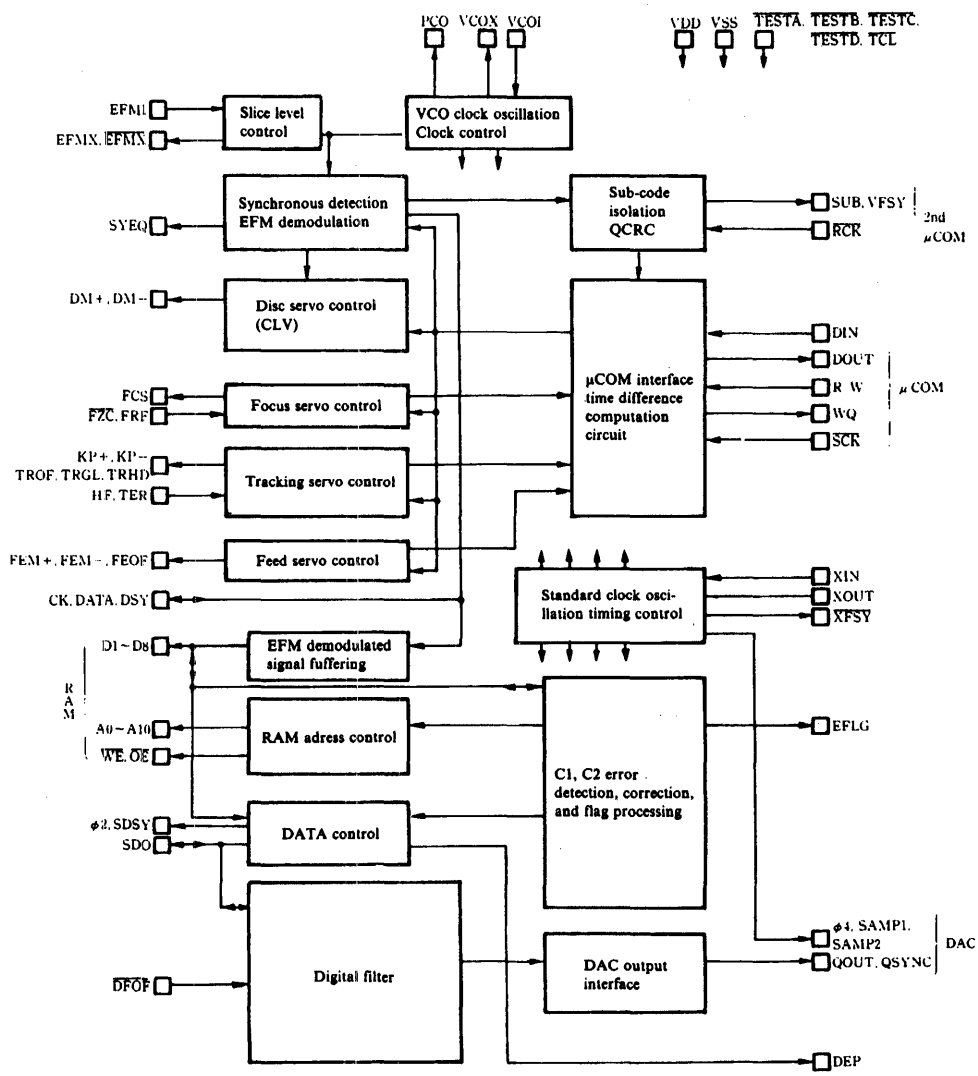


DIGITAL AUDIO

Digital Audio Interface Transmitter

YM3437C (DIT2)

PRELIMINARY

■OUTLINE

The YM3437C is a serial digital audio transmitter LSI. The YM3437C can convert 4 different kinds of serial digital audio data into AES or EIAJ digital audio interface format. In addition, the YM3437C can add a validity bit (V bit), user data bit (U bit), and channel status bit (C bit) to the data.

■FEATURES

- All internal and external timing is defined by the external master clock (MCLK).
- The sampling frequency can be from 30 kHz to 50 kHz.
- Four serial digital audio data input formats.
- With audio auxiliary control, the length of the audio sample word can be changed from 20 bits of data with 4 audio auxiliary bits to 24 bits of data with no audio auxiliary bits.
- V, C, and U bits can be added with appropriate input pins.
- The control code may be input serially or in parallel. With serial input, the first 4 bytes (32 bits) of channel status bits and the first 4 bytes (32 bits) of user data bits may be input. With parallel input, the V, U, and C bits may be input.
- The digital audio interface data output can be forced to zero with the MUTE signal input.
- CMOS 5V single power supply.
- 16 pin DIP , SOP.

■ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating	Units
Supply voltage	$V_{DD}-V_{SS}$	$-0.3\sim+7.0$	V
Input voltage	V_I	$V_{SS}-0.3\sim V_{DD}+0.5$	V
Operating temperature	Top	$0\sim+85$	℃
Storage temperature	Tstg	$-50\sim+125$	℃

Recommended Operating Conditions

Item	Symbol	Min.	Typ	Max.	Units
Supply voltage	$V_{DD}-V_{SS}$	4.5	5.00	5.5	V

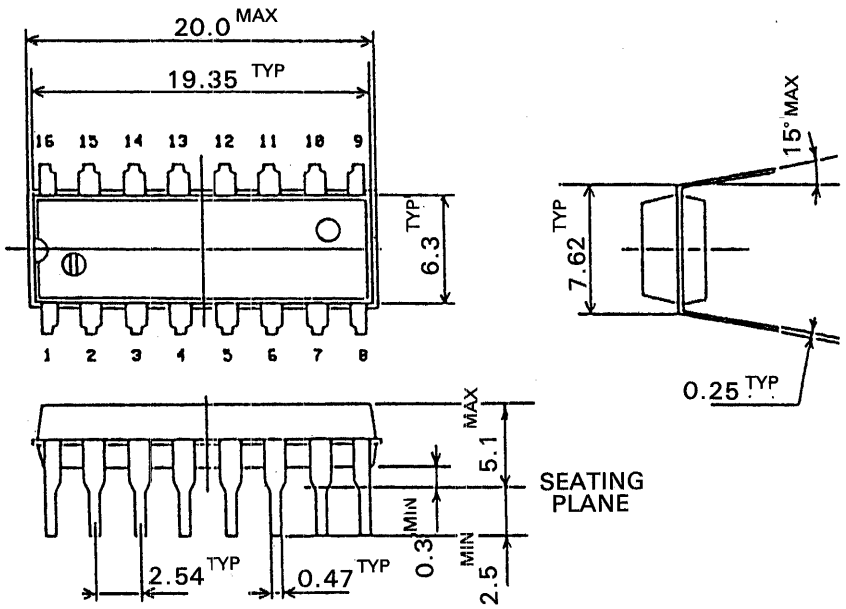
Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}	$V_{OO}=5V$ fc=6,144MHz			5	mA
High-level output voltage	V_{OH}	$I_{OH}=0.4mA$	4.0			V
Low-level output voltage	V_{OL}	$I_{OL}=2mA$			0.4	V
High-level input voltage	V_{IH}		2.2			V
Low-level input voltage	V_{IL}				0.8	V
Input leakage current	I_{LX}	$V_I=5V$	−10		10	μA

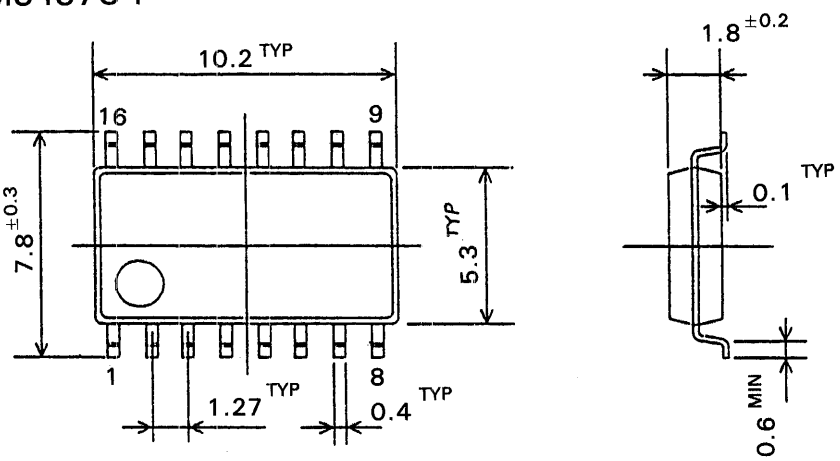
The specifications of this product are subject to improvement changes without prior notice.

■ OUTLINE DIMENSIONS

(1)YM3437C-D



(2)YM3437C-F



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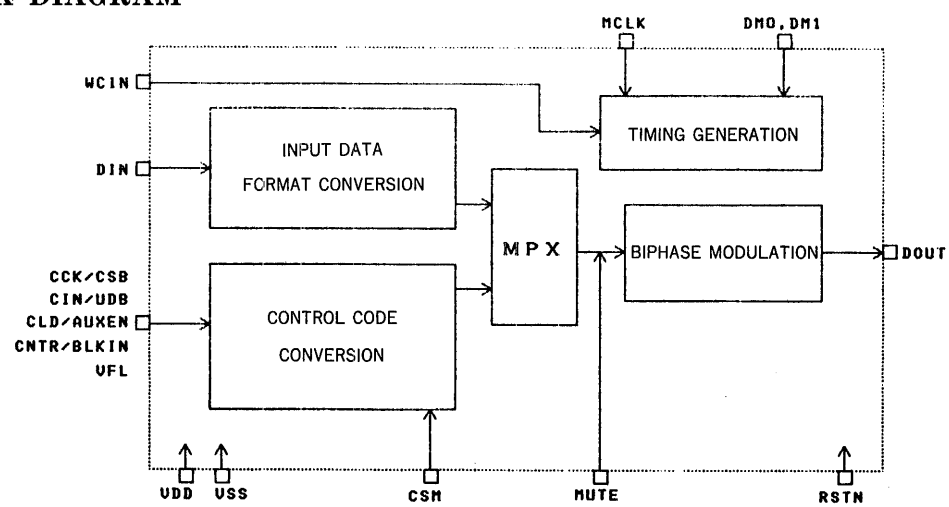


DIGITAL AUDIO

Digital Audio Interface Receiver

YM3436B DIR2

PRELIMINARY

■OUTLINE

YM3436B is a digital audio interface receiver IC which converts a digital audio interface format signal as defined by AES or EIAJ to one of four serial digital audio data output formats. At the same time, the chip generates a validity flag (V flag), user data bit (U bit), and channel status bit (C bit), and various system clocks.

■FEATURES

- Separates the audio data and generates various control codes from bi-phase digital audio interface format signals.
- Generates various system clocks with internal PLL.
- The sampling frequency of the audio interface signal received can be from 30KHz to 50KHz.
- The received digital audio data is formatted into one of 4 serial output formats.
- 3 other serial input formats can be received in addition to bi-phase digital audio interface format.
- Noise is suppressed by an effective data error detection circuit.
- The V flag, U bit and C bit are output with each subframe. In addition, the first 32 bits of U and C bits can be read for each block with the microprocessor.
- With the internal data buffer, multiple asynchronous digital audio interface format signals can be received.
- The C bit format is available for both consumer use and broadcast studio use.
- CMOS +5V single power supply.
- 44 pin QFP package

■ ELECTRICAL CHARACTERISTICS

Maximum Ratings

ITEM	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	−0.3~7.0	V
Input voltage	V_I	V_{SS}−0.3~V_{DD}+0.5	V
Ambient operating temperature	Top	0~+70	℃
Storage temperature	Tstg	−50~+125	℃

Recommended Operating Conditions

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Ambient operating temperature	Top	0	25	70	℃

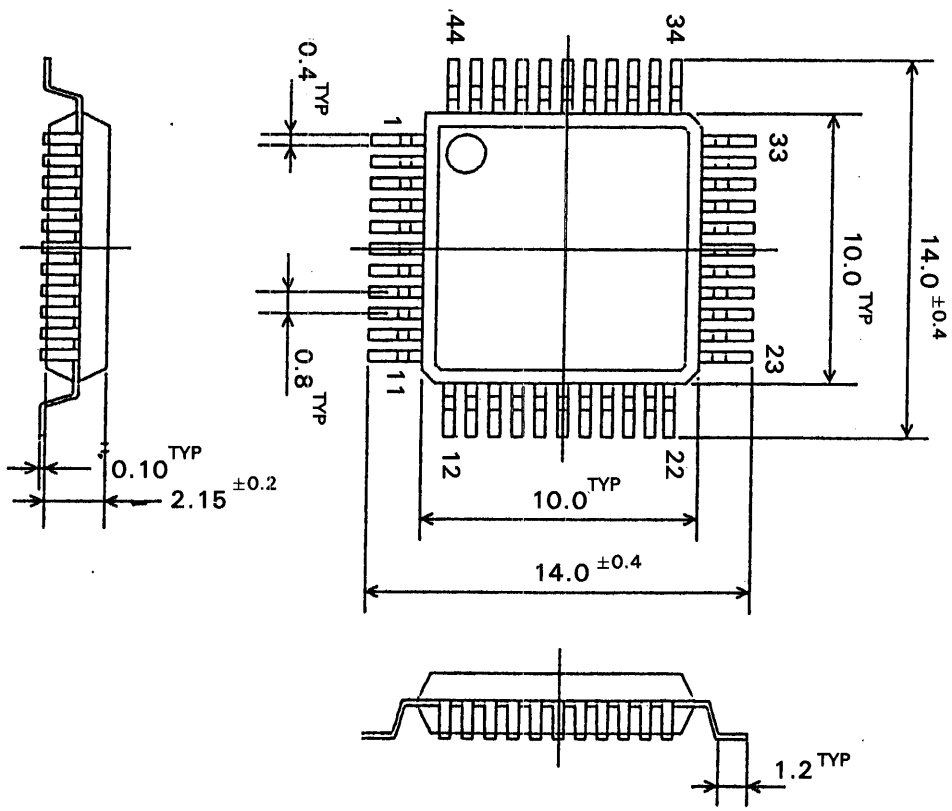
DC Characteristics(CONDITIONS : Ta=25℃, V_{DD}=5.0±0.25V)

ITEM	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Supply current	I_{DD}	V_{DD}=5.0V				mA
High-level input voltage (1)	V_{IH1}	(Note 1)	2.0			V
Low-level input voltage (1)	V_{IL1}	(Note 1)			0.8	V
High-level input voltage (2)	V_{IH2}	(Note 2)	3.5			V
Low-level input voltage (2)	V_{IL2}	(Note 2)			1.0	V
Input leak current	I_{LK}		−10		10	μA
High-level output voltage	V_{OH}	I_{OH}=−50μA	4.0			V
Low-level output voltage	V_{OL}	I_{OL}=2.0mA			0.4	V
Input capacitance	C_I				10	pF
Output capacitance	C_O				10	pF

Note 1: Any input terminal except XI
Note 2: XI terminal

The specifications of this product are subject to improvement changes without notice.

■ OUTLINE DIMENSIONS



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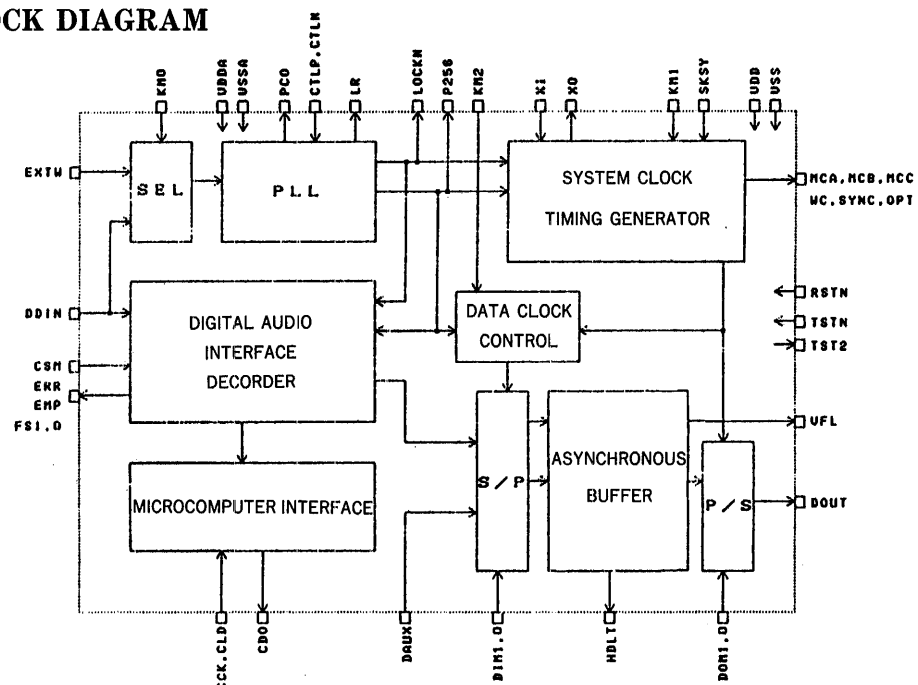


DIGITAL AUDIO

Digital Audio Interface Receiver

PRELIMINARY

YM7136 DIR3

■OUTLINE

The YM7136 is an LSI device, which receives and demodulates the Digital Audio Interface signals that are used between digital audio equipments. The YM7136 has error operation circuit for transferred data and oversampling digital filter which makes it easy to constitute DA conversion circuit with a few external components.

■FUNCTIONS AND FEATURES

- The YM7136 has 4 channels of bi-phase input terminals, and each of these has bias circuit which enables you to input from coaxial and optical line with a few external components.
- It has an internal PLL circuit which generates clock and demodulates bi-phase signal.
- It can detect unlock of PLL and parity error, it keeps previous audio data and mutes when it detects error.
- It outputs channel status information of emphasis, copy prohibition and sampling frequency type.
- Output terminal of sampling frequency type can drive LED directly.
- It has digital di-emphasis function internally.
- It has 4 times and 8 times oversampling digital filter, which has following characteristics
  Pass band ripple : within ± 0.03dB
  Stop band attenuation : At least 60dB
- It can interface for 1 DAC(4 times) or 2 DAC(4 times, 8 times) of 16 or 18 bit.
- CMOS, Single 5V single power supply, 64pin QFP.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	−0.3～+7.0	V
Ambient operating temperature	Top	−40～+85	℃
Storage temperature	Tstg	−50～+125	℃

Recommended Operating Conditions

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Ambient operating temperature	Top	0	25	70	℃

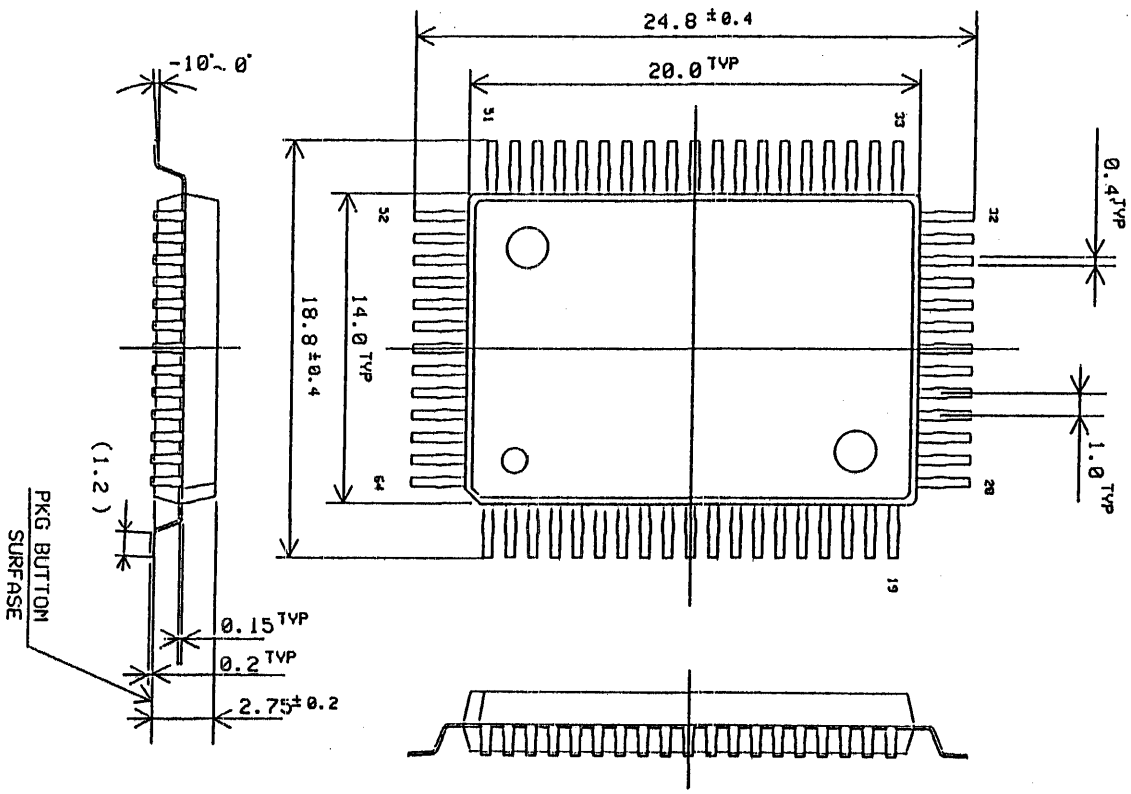
DC Characteristics conditions

ITEM	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Power consumption	W	V_{DD}=5.0V		150		mW
High-level input voltage (1)	V_{IH1}		2.0			V(Note1)
Low-level input voltage (1)	V_{IL1}				0.8	V(Note1)
High-level input voltage (2)	V_{IH2}		3.5			V(Note2)
Low-level input voltage (2)	V_{IL2}				0.8	V(Note2)
Input Peak to Peak voltage	V_{IPP}					V(Note3)
High-level output voltage	V_{OH}	I_{OH}=0.4mA	4.0			V
Low-level output voltage	V_{OL}	I_O=2mA			0.4	V
Output current	I_O					mA(Note4)
Input leak current	I_{IL}	V_I=5V		10		μA
Input capacitance	C_I			10		pF
Output capacitance	C_O			10		pF

Note1 : Any input terminal except DINO～DIN3,CV,RV,XI
Note2 : XI terminal
Note3 : DINO～DIN3 terminal
Note4 : 32K,44.1K,48K terminal

The specifications of this product are sudject to improvement changes without prior notice.

■ OUTLINE DIMENSIONS



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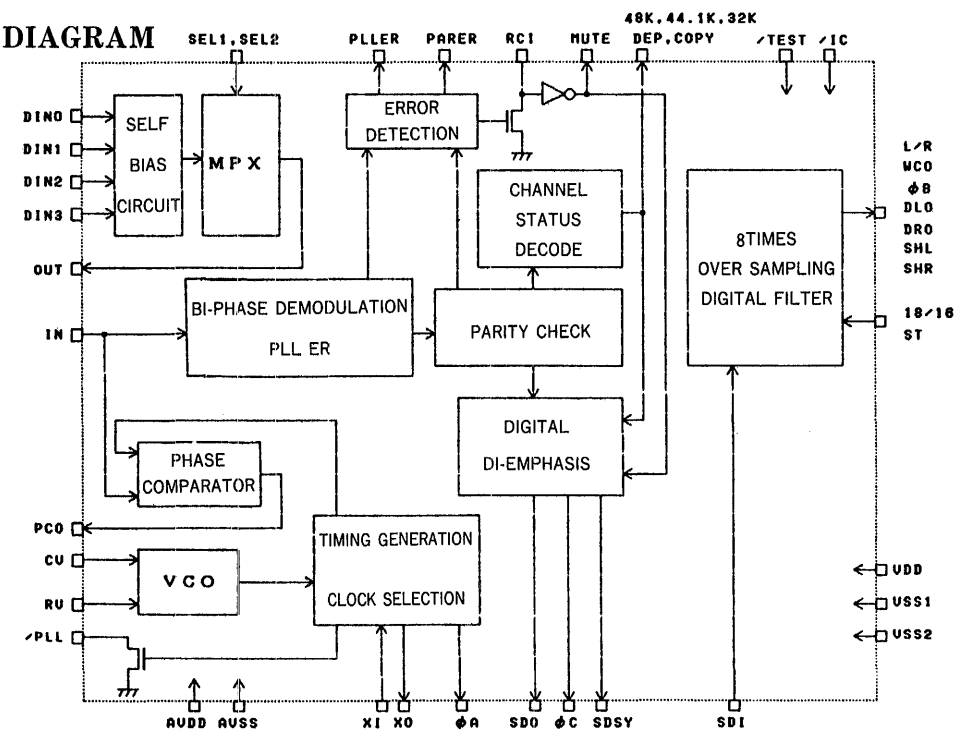


DIGITAL AUDIO

Digital Audio Interface Receiver

YM3623B DIR

■ OUTLINE

The YM3623B is an LSI device, which receives and regenerates the Digital Audio Interface Format signals that are transferred between digital audio equipment. Use of the YM3623B eliminates the need for a special externally- mounted circuit for playback, thereby greatly facilitating the playback of Digital Audio signals.

■ FUNCTIONS

1) The YM3623B has an internal PLL circuit which synchronizes with the Digital Audio Format signals that are sent in from the external equipment.
2) It outputs Audio signals starting with the MSB (Most Significant Bit). In sync with that output, it outputs the Timing clocks for the D/A output sample-and-hold operations and the signals indicating the L or R channel.
3) It has a terminal for outputting a Subcode, making possible the retrieval of Subcode data.
4) It is capable of outputting the sampling frequency, Emphasis ON/OFF status, Copy Enable/Disable status, as well as the Error status of transmitted Audio signals.
5) In case an error is detected in the Digital Audio Interface Format signals, the Audio data preceding the detected error is output again.

■ FEATURES

1) Silicon gate CMOS construction (low power consumption)
2) 28-pin Dual-Inline Package (DIP)
3) +5V power supply

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Units
Supply voltage	V_{DD}—V_{SS}	−0.3 ~ +7.0	V
Input voltage	V_I	V_{SS} − 0.3 ~ V_{DD} + 0.5	V
Operating temperature	T_{OP}	−20 ~ +75	°C
Storage temperature	Tstg	−50 ~ +125	°C

2. Recommended Operating Conditions

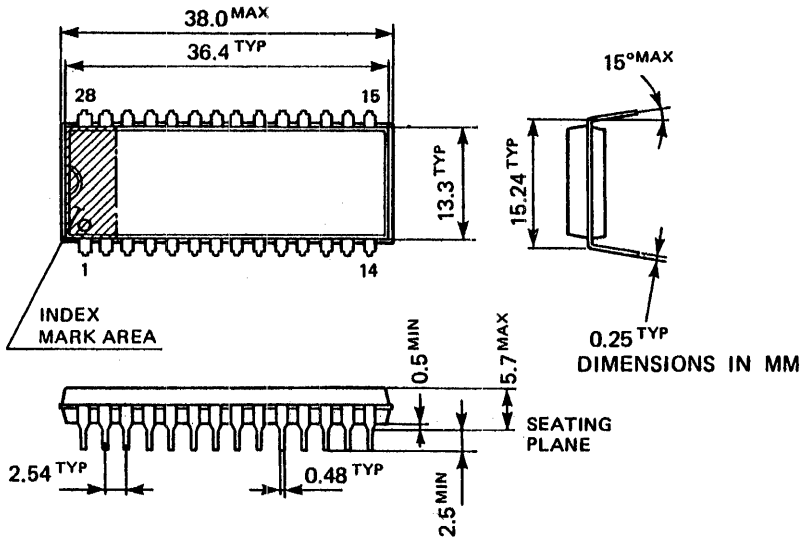
Item	Symbol	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}—V_{SS}	4.75	5.00	5.25	V

3. Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}	V_{DD} = 5V D_{IN} = 5V fc = 16.9344MHz		6	8	mA
High-level output voltage	V_{OH}	I_{OH} = 0.4mA	4.0			V
Low-level output voltage	V_{OL}	I_{OL} = 2mA			0.4	V
High-level input voltage	V_{IH}	X_I pin excluded X_I pin	2.0 4.5			V
Low-level input voltage	V_{IL}				0.8	V
Input leakage current	I_{LK}	V_I = 5V			10	μA

NOTE: The analog VCO pin and the ADJ pin are excluded.

■ OUTLINE DIMENSIONS



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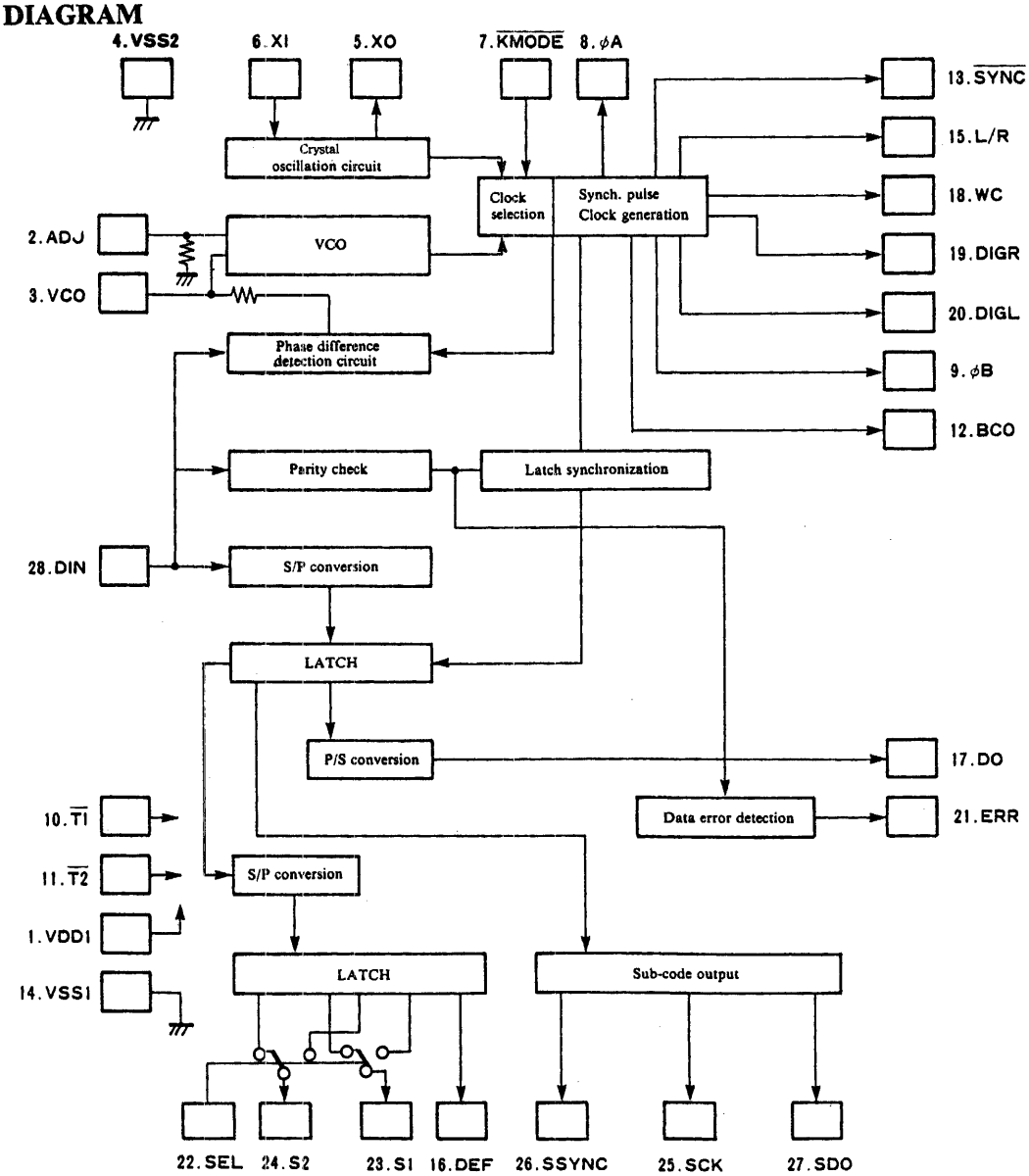


DIGITAL AUDIO

2-Channel 8-times Oversampling Digital Filter

YM3434 AFUDF

■ OUTLINE

The digital filter's own system clock rate must be considerably faster than the input bit clock rate and at the same time synchronism is required in the system as a whole. Thus what is normally required is a high-speed clock which is synchronous with the signal handling pre-processor. Then the major application problem is how to interface these different clock rates.

YM3434 is a high quality 2-channel 8-times oversampling digital filter which has been developed to solve such problems. It can be used easily as an interface in a wide range of digital audio systems. Its filtering capabilities are equivalent to the YM3414.

Since the system clock of this LSI can be different from the serial input signal and it operates normally at any clock rate above 400 clocks for each input sampling frequency (fs), it is not necessary to change the clock rate even if the sampling frequency is changed.

For example, by connecting a 20MHz crystal oscillator, there is no need to change the clock rate even when the sampling frequency is changed to 32KHz, 44.1KHz or 48KHz.

■FEATURES

- Operation at an independent system clock from the serial input signal
- Input signals can be handled at any of the following input bit clock rates without adding any circuit: 32fs, 48fs, 64fs, 80fs, 96fs, 112fs, 128fs, 144fs, 160fs, 176fs, and 192fs,
- Capable to cope with sampling frequencies 32KHz, 44.1KHz and 48KHz.
- Linear phase FIR type filters connected in three vertical stages
  1st filter : 225-order FIR filter
  2nd filter: 41-order FIR filter
  3rd filter : 21-order FIR filter
- Built-in 19 × 18 bit multiplier, floating point calculation with a coefficient of 18 bits
- Built-in overflow limiter
- Filter characteristics (at 8-times)
  Pass band ripple : Within ±0.0001dB at 0 to 0.4535 × fs
  Stop band attenuation : At least 100dB at 0.5465 × fs to 7.4535 × fs
- Output data switchable between 16 bit and 18 bit (directly connectable to PCM56 and PCM58).
- Switchable between 1 DAC (4-times) and 2 DAC (8-times).
- CMOS process, Single 5V power supply, 16-pin DIP package.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Power supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	VI	−0.3	V_{DD}+0.5	V
Working temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

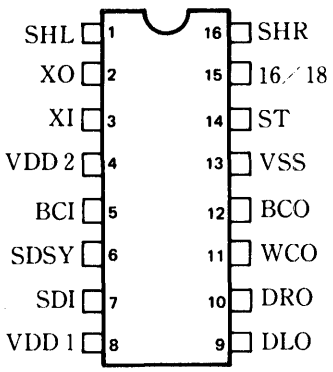
Recommended Operating Conditions

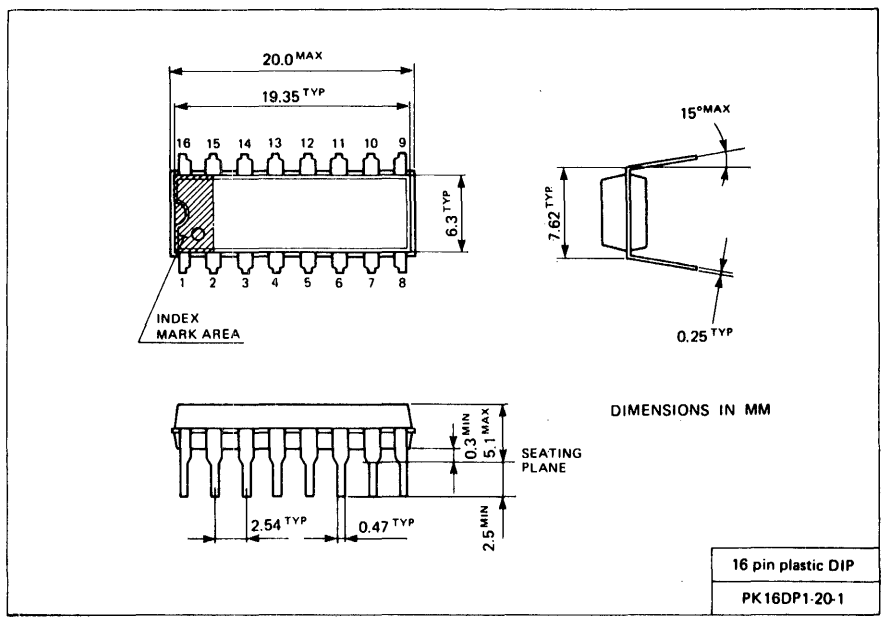
Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Clock frequency	XIN	12.2	(400 Fs)	20.0	MHz
Working temperature	Top	0	25	+70	°C

Electrical Characteristics

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Power consumption	W	V_{DD}=+5V			300	mW
Input voltage H level (XI, 16/18, ST) (BCI, SDSY, SDI)	VIH		3.5 2.7		V_{DD} V_{DD}	V V
Input voltage L level	VIL		0		0.8	V
Output voltage H level	VOH		2.4		V_{DD}	V
Output voltage L Level	VOL		0		0.4	V
DLO, DRO setup time DLO, DRO hold time			15 15			ns ns
Input data setup time (Rise of BCI)			50			ns
Input data hold time (Rise of BCI)			20			ns
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ OUTLINE DIMENSIONS





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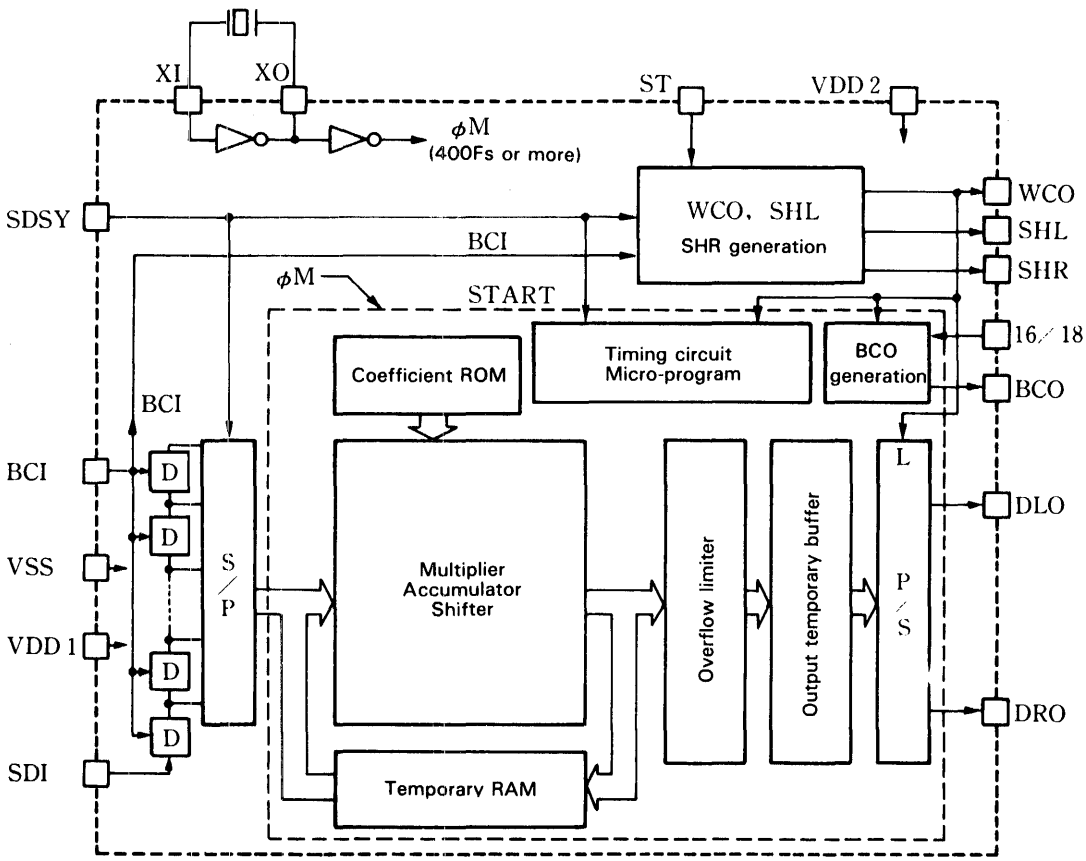


DIGITAL AUDIO

2 channel 8 times oversampling digital filter operates via serial input signal and independent system clock

YM3433B ALCDF

■OUTLINE

This oversampling digital filter operates by repeating the input sample cycle through a sum of products computation process. This calculation must be repeated numerous times for reliable operation. A high speed bit clock rate is required, but only for the part to be oversampled from the input bit clock.

Because of these requirements, the system clock in the digital filter itself operates at a high speed appropriate for the input clock rate. Because it was normal for the cycles to be synchronized by the system, it has been necessary in the past to synchronize the signal processor at the previous step (which received the request) with the high speed clock, and designs used to interface the synchronized high speed clock presented some problems with regard to practical applications.

This LSI chip has solved these problems, resulting in a high grade 2 channel 8 times oversampling digital filter that can be interfaced easily with a wide range of digital audio systems, and it is pin compatible with the YM3434.

This particular LSI chip permits use of a system clock which operates independently from the serial input signal. The input sampling cycle (fs) will operate normally even with input from clocks with more than 400 ticks-for example, even if the sampling frequency is switched between fs = 32kHz, 44.1kHz, and 48kHz when connected with a 20MHz crystal oscillator, there is no need to switch to any other clock.

■FEATURES

- Because this operates with a serial input signal and an independent system clock, this can handle all of the input bit clock rates which follow with no supplementary circuit: input signals-32 fs, 48 fs, 64 fs, 80 fs, 96 fs, 112 fs, 128 fs, 144 fs, 160 fs, 176 fs, 192 fs.
- Linear phase FIR type filter connected in line at 3 levels
  1st filter: 161 order FIR filter, 2nd filter: 33 order FIR filter, 3rd filter: 17 order FIR filter
- Built-in overflow limiter
- Filter capacity (when 8-times)
  Passband ripple 0~0.4535× fs: ±0.002 dB or less
  Cutoff band reduced capacity 0.5465×fs ~7.4535×fs: 70dB or more
- 16 bit/18 bit output switching (compatible with PCM56/PCM58)
- 1DAC(4-times)/2DAC(8-times) switching
- CMOS process, +5V power supply, 16 pin DIP, 24 pin SOP

■ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.5	V
Operating temperature	T_{OP}	−20	+75	℃
Storage temperature	T_{STG}	−50	+125	℃

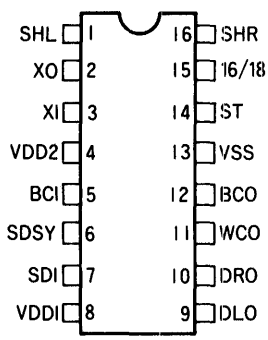
RECOMMENDED OPERATING CONDITIONS

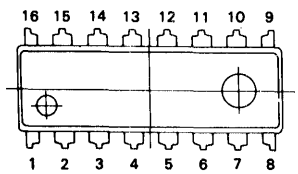
Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Clock frequency	XIN	12.2	(400 fs)	20.0	MHz
Operating temperature	T_{OP}	−40	25	+85	℃

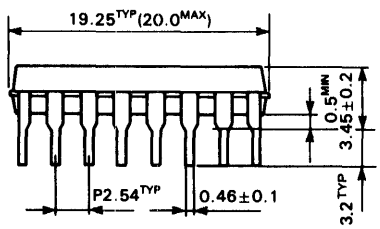
ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 ± 0.25V)

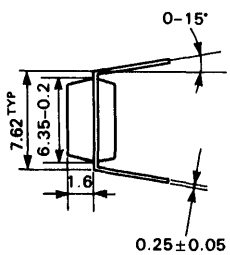
Item	Symbol	Condition	Min	Typ	Max	Unit
Power consumption	W	V_{DD} = +5V			125	mW
High input voltage (XI, 16/18, ST)	V_{IH}		3.5		V_{DD}	V
(BCI, SDSY, SDI)			2.7		V_{DD}	V
Low input voltage	V_{IL}		0		0.8	V
High output voltage	V_{OH}		2.4		V_{DD}	V
Low output voltage	V_{OL}		0		0.4	V
DLO,DRO setup time			15			nS
DLO,DRO hold time			15			nS
Input data setup time (BCI leading edge)			50			nS
Input data hold time (BCI leading edge)			20			nS
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ OUTLINE DIMENSIONS









DIMENSIONS IN MM

*24 pin SOP is available

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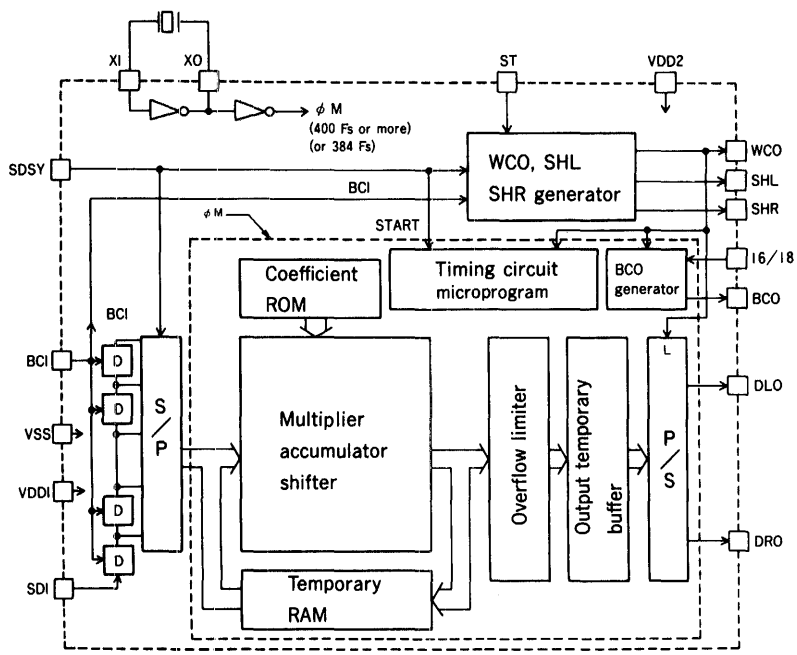


DIGITAL AUDIO

2-Channel 8-times Oversampling Digital Filter

YM3414 ACDDF

■ OUTLINE

The YM3414 (ACDDF) is a super-high performance 8-times oversampling digital filter for use with the digital audio systems developed by Yamaha.

It is connectable directly to LSI, DIT, DIR, etc. for digital audio systems, and can exhibit its excellent performance through simple procedures.

■ FEATURES

- 8-times oversampling in two channels
- Linear phase FIR type filters connected in three vertical stages
  - 1'st filter: 225-order FIR filter
  - 2'nd filter: 41-order FIR filter
  - 3'rd filter: 21-order FIR filter
- 19 × 18 bits multiplier built in
- Floating point multiplier and accumlater having a coefficient of 18 bits
- Overflow limiter built in
- Filter characteristics (fs=44.1 kHz)
  - Pass band ripple: Within ±0.0001 dB at 0 to 20 kHz
    (Within quantization error in 16 bits)
  - Stop band attenuation: At least 100 dB at 24.1 kHz and higher
- High precision oscillator specially designed for use with the filter
- C-MOS process
- Single 5 V power supply
- 16-pin DIP package

■ ELECTRICAL CHARACTERISTICS

▪ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Minimum	Maximum	Unit
Power supply voltage	VDD	−0.3	+7.0	V
Input voltage	VI	−0.3	Vdd+0.5	V
Working temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

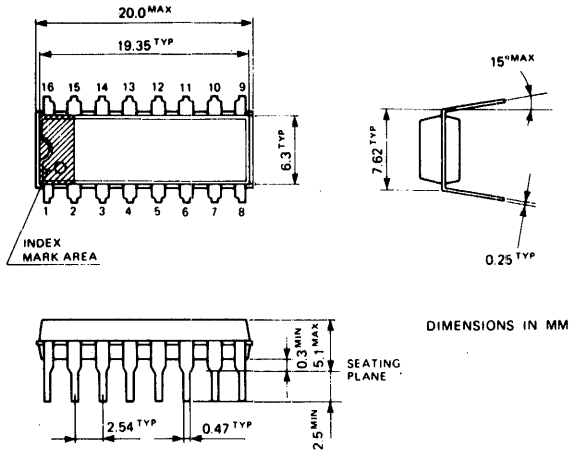
▪ RECOMMEND OPERATING CONDITIONS

Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	VDD	4.75	5.0	5.25	V
Clock frequency	XIN	12.2	16.93	18.5	MHz
Working temperature	Top	0	25	70	°C

▪ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=5±0.25V)

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power consumption	W	Vdd=+5V		200	270	mW
Input voltage H level (XI, TD) (BCI, SDSY, SDI, SyncS)	VIH		 3.5 2.7		 Vdd Vdd	 V V
Input voltage L level	VIL		0		0.8	V
Output voltage H level	VOH		2.4		Vdd	V
Output voltage L level	VOL		0		0.4	V
Output delay (delay from BCO)			5		35	nsec
Input data setup time (Rise of BCI)			50			nsec
Input data hold time (Rise of BCI)			20			nsec
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ OUTLINE DIMENSIONS



DIMENSIONS IN MM

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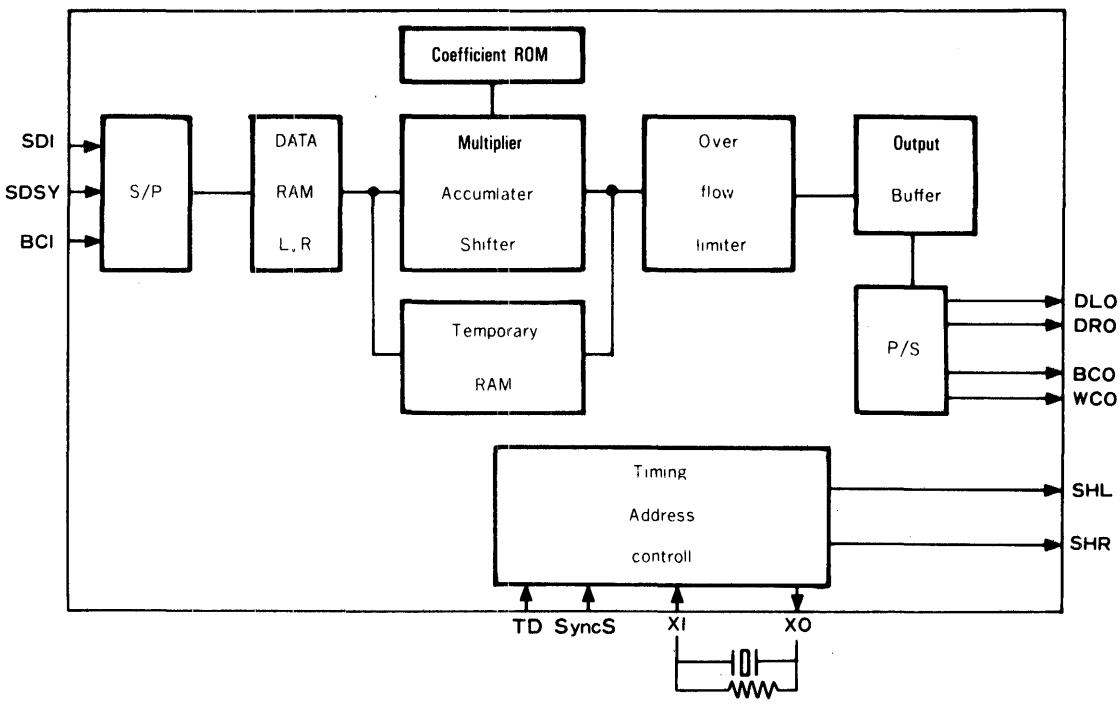


DIGITAL AUDIO

2-Channel 4-times Oversampling Digital filter

YM3404B CDDF

■ OUTLINE

The YM3404B (CDDF) is a super-high performance 4-times oversampling digital filter for use with the digital audio systems developed by Yamaha.

It is connectable directly to LSI, DIT, DIR, etc. for digital audio systems, and can exhibit its excellent performance through simple procedures.

■ FEATURES

- 4-times oversampling in two channels
- Linear phase FIR type filters connected in two vertical stages
  - 1'st filter: 225-order FIR filter
  - 2'nd filter: 41-order FIR filter
- 19 × 18 bits multiplier built in
- Floating point multiplier and accumlater having a coefficient of 18 bits
- Overflow limiter built in
- Filter characteristics (fs=44.1 kHz)
  - Pass band ripple: Within ±0.0001 dB at 0 to 20 kHz
    (Within quantization error in 16 bits)
  - Stop band attenuation: At least 100 dB at 24.1 to 64.1 kHz
    At least 99 dB at 64.1 kHz and higher
- High precision oscillator specially designed for use with the filter
- Clock providing 8.6426 MHz output
- C-MOS process
- Single 5 V power supply
- 16-pin DIP package

■ ELECTRICAL CHARACTERISTICS

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Minimum	Maximum	Unit
Power supply voltage	Vdd	−0.3	+7.0	V
Input voltage	VI	−0.3	Vdd+0.5	V
Working temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

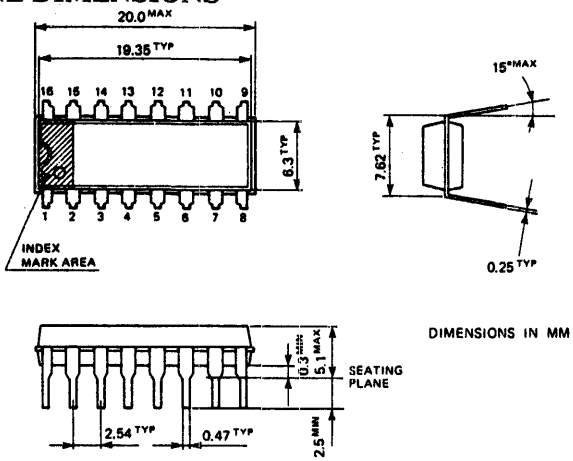
■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	VDD	4.75	5.0	5.25	V
Clock frequency	XIN	12.2	16.93	18.5	MHz
Working temperature	Top	0	25	70	°C

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{DD}=5±0.25V)

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power consumption	W	Vdd=+5V		200	270	mW
Input voltage H level (XI, FEN, ST) (BCI, SDSY, SDI)	VIH		 3.5 2.7		 Vdd Vdd	 V V
Input voltage L level	VIL		0		0.8	V
Output voltage H level	VOH		2.4		Vdd	V
Output voltage L level	VOL		0		0.4	V
Output delay (delay from BCO)			5		35	nsec
Input data setup time (Rise of BCI)			50			nsec
Input data hold time (Rise of BCI)			20			nsec
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ OUTLINE DIMENSIONS



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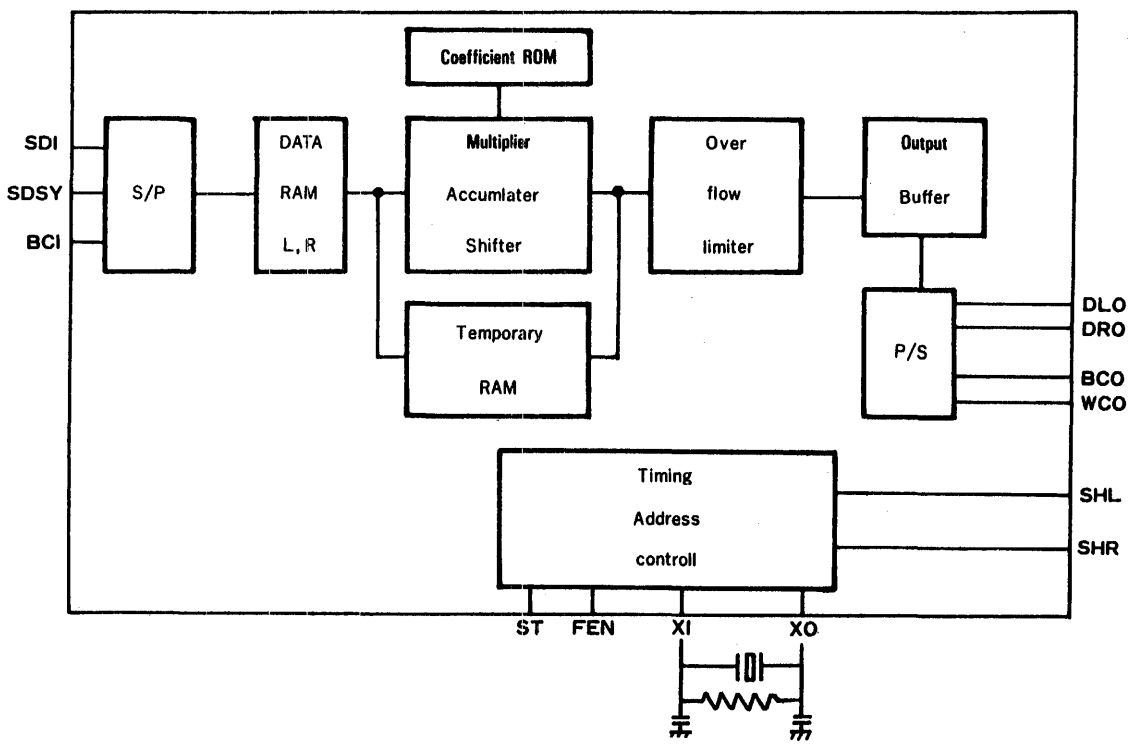


DIGITAL AUDIO

Digital Equalizer

YM3608 DEQ

■ OUTLINE

The YM3608 is a s pecial digital processor developed by Yamaha Corp. for use with digital filters. This processor makes it possible to easily configure IIR and FIR filters for serial sound signals using the internal microprogram.

This processor also makes possible high accuracy calculations and the freedom to rewrite microprogram functions and coefficients using SCI*.

* SCI: Serial Control Interface

■ FEATURES

- All microprogrammable function for digital filter.
- Multiplication is performed with one clock for Data 16 bits × Coefficient 32 bits. (2 clocks for Data 32 bits × Coefficient 32 bits) (This is 5-clock pipeline processing.)
- There are 2 serial input terminals and 2 serial output terminals, both of which can be used with any desired timing. The MSB/LSB first and shift clocks can be selected independently for input and output. Input and output are also possible using an external clock.
- A 50-bit accumulator with 4 bits of head margin and overflow detect is provided.
- The master clock operates at a maximum phase of 4.4MHz and a minimum phase of 2MHz.
- Microprogram and coefficients can be controlled with SCI (Serial Control Interface).
- Up to 128 steps can be used with microprogram.
- Higher calculation performance is possible by making a serial connection to YM3608 (DEQ).
- Operates on a single 5V power supply.
- 24-pin DIP.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating
Power supply voltage	V_{DD}	−0.3 ~ 7.0V
Input voltage	V_I	−0.3 ~ V_{DD} + 0.5V
Operating temperature	T_{OP}	0 ~ 70°C
Storage temperature	T_{stg}	−50 ~ 125°C

Recommended Operating Conditions

Item	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0		70	°C

D.C. Characteristics

Item	Symbol	Minimum	Typical	Maximum	Unit
Input clock frequency	fc	2		4.4	MHZ
Input clock High level time	$T_{\phi h}$	90			n sec
Input clock Low level time	$T_{\phi l}$	100			n sec
Input data set-up time	T_{DS}	50			n sec
Input data hold time	T_{DH}	10			n sec
Output delay time *1	T_{OD}			100	n sec
Bypass delay time *1	$T_{\beta D}$			70	n sec

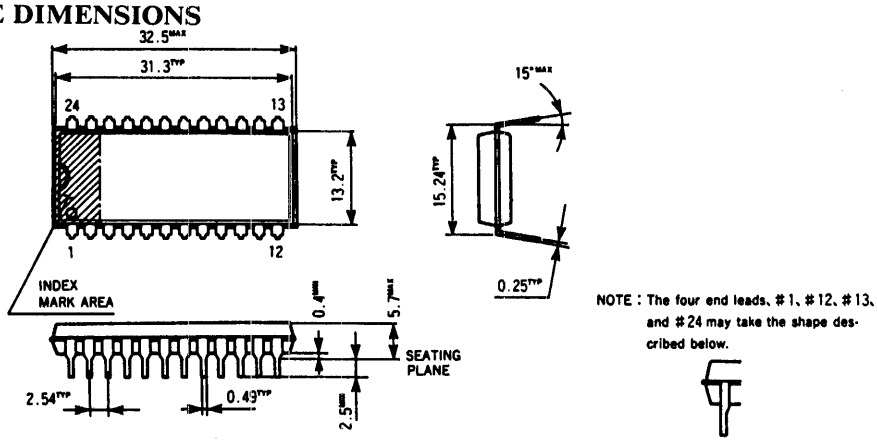
Conditions: V_{DD} = 5.0V ± 5%, T_{OP} = 0 ~ 70°C

A.C. Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Output voltage H level	V_{OH}	I_{OH} = −0.4mA	3.5		V_{DD}	V
Output voltage L level	V_{OL}	I_{OL} = 1mA	V_{SS}		0.4	V
Input voltage H level	V_{IH}		2.4			V
Input voltage L level	V_{IL}				0.4	V
Input leak current	I_{LK}	V_I = 5V			0.1	μA

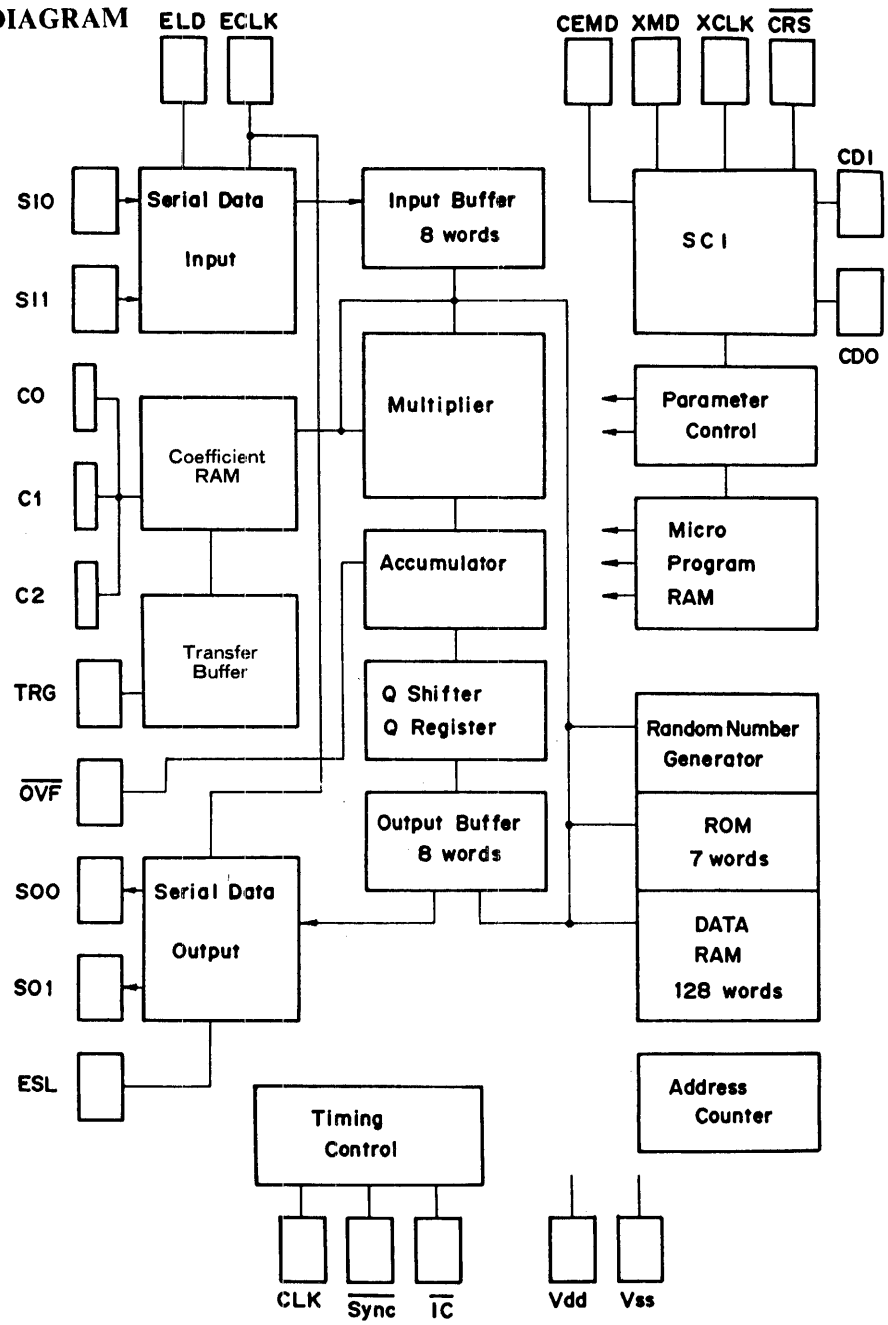
*1: with 100pF capacitance added.

■ OUTLINE DIMENSIONS



NOTE : The four end leads, #1, #12, #13, and #24 may take the shape described below.

■ BLOCK DIAGRAM



DIGITAL AUDIO

Analog Servo Processor

GDR101 ASP

■ OUTLINE

GDR101 is a bipolar LSI for analog signal processing and for servo control of compact disc players, suitable for 3-beam system. CD player system can be constructed easily by combining with YM3805(SPC), YM7121B(SPC5), YDC101(SPC6), YM7402(CDVP).

■ FEATURES

- Single power supply(+5V) or dual power supply system(±5V) are selectable.
- CD player system can be made by using Digital Signal Processor such as YM7121B.
- Almost all the functions for analog system are incorporated.
  - RF amplifier
  - focus error amp
  - tracking error amp
  - slice level control (SLC) amplifier
  - VCO control amplifier
  - focus (FCS) switch
  - tracking switch(TSOF, TRFD, TRGL)
  - laser on/off switch
- Timing signals FRF, /FZC, HF, TWR are output.
- 48 pin QFP.

■ELECTRICAL CHARACTERISTICS

● Absolute maximum ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Power supply voltage	VCC/VEE		±7	V
Power consumption	Pd max	Ta≦75℃	430	mW
Operating temperature	Top		−25～+ 75	℃
Storage temperature	Tstg		−40～+125	℃

● Recommended operating conditions

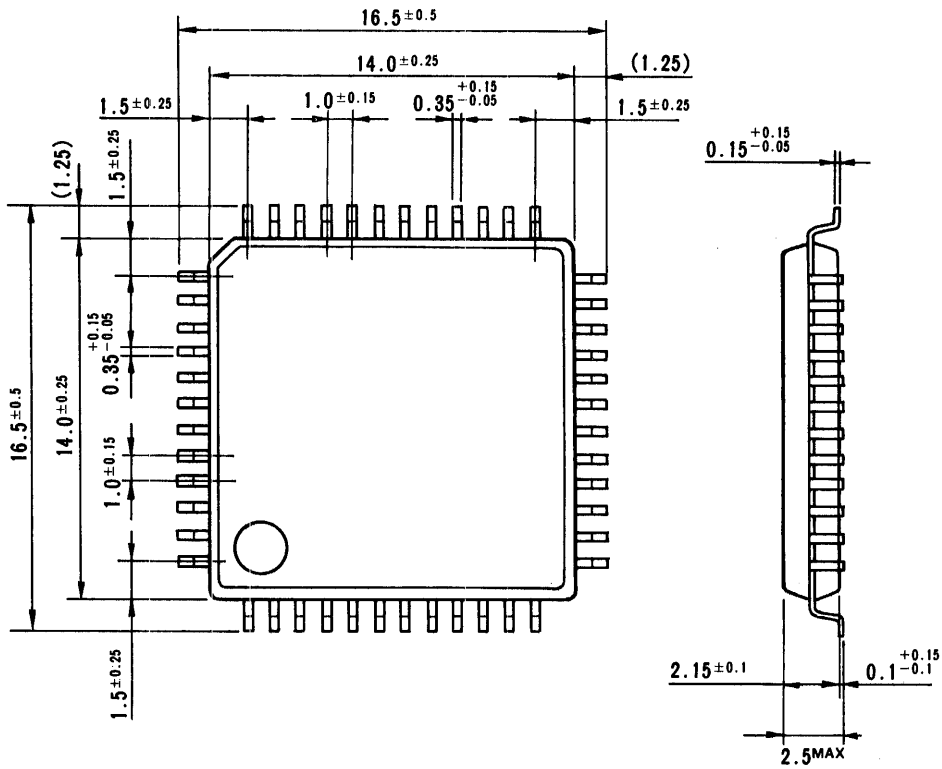
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCCop	+4	+5	+6	V
	VEEop	−6	−5	−4	V
Operating temperature	Top	0	25	75	℃

● Operating characteristics (Condition; Ta=25℃, VCC=±5V, VEE=−5V)

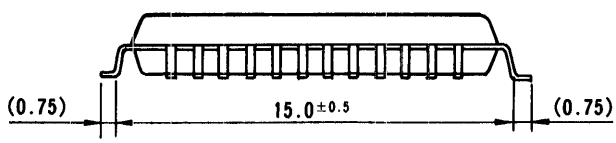
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Consumption current	ICC		12	17	22	mA
	IEE	LDSW off	11	15.5	20	mA
< RF amp. section >						
Offset voltage	V36-0	41,42 pins open	−300	−120	0	mV
Voltage gain	GV36	36～37 pins: 22KΩ 41,42 pins: Rg=10KΩ f=200KHz	25	28	31	dB
Maximum output amplitude	V36H	RL=10KΩ	+4.0	+4.2	+4.3	V
	V36L	RL=10KΩ	−1.6	−1.3	−1.2	V
Frequency characteristics		1MHz/200KHz	−3.0	−0.5	+3.0	dB
< Focus error amp. section >						
Offset voltage	V31-0	41,42 pins open	−150	0	+150	mV
Voltage gain	GV31	33 pin～GND=120KΩ 31～32 pins=120KΩ f=1KHz	31	34	37	dB
Voltage gain difference	dGV	41 pin input and 42 pin input	−1.0	0	+1.0	dB
Maximum output amplitude	V31H	RL=10KΩ	+4.1	+4.25	+4.6	V
	V31L	RL=10KΩ	−4.6	−4.25	−4.1	V
Frequency characteristics	fmax		−3.0	−0.5	+3.0	dB
< Peak hold circuit section >						
Offset voltage	V35-36	41,42 pins open	−100	−40	20	mV
Output voltage	V35-0	41,42 pins input current=5μA	1.0	1.2	1.4	V
< Bottom hold circuit section >						
Offset voltage	V34-35	41,42 pins open	−100	0	100	mV
Output voltage	V34-0	41,42 pins input current=5μA	1.0	1.2	1.4	V
< FRF comparator section >						
Comparator output	V27H	41,42 pins iuput current=3μA	4.0	4.2	4.5	V
	V27L	41,42 pins input current=1μA	0	0	0.5	V
Offset voltage	V35-1	35 pin voltage when V27=H	0.7			V
	V35-2	35 pin voltage when V27=L			0.1	V
< /FZC comparator section >						
Comparator output	V18H	41,42 pins open	4.0	4.2	4.5	V
	V18L	42 pin input current =1μA		0	0.5	V
Offset voltage	V31-1	31 pin voltage when V18=H	−0.35			V
	V31-2	31 pin voltage when V18=L			−0.65	V
< HF comparator >						
Comparator output	V17H	41,42 pins open	4.0	4.2	4.5	V
	V17L	35 pin=0.8V 34 pin=0V	0	0	0.5	V
Offset voltage	V35-1	35 pin voltage when V17=L, 34 pin=0V	0.7			V
	V35-2	35 pin voltage when V17=H, 34 pin=0V			0.3	V
Maximum operating frequency	fmax		100	500		KH_z

NOTE: This LSI can be supplied only combination with YAMAHA signal processors such as YDC101, YM7121B, YM3805 etc. Please contact YAMAHA before design start.

■ OUTLINE DIMENSIONS



DIMENSIONS IN MM



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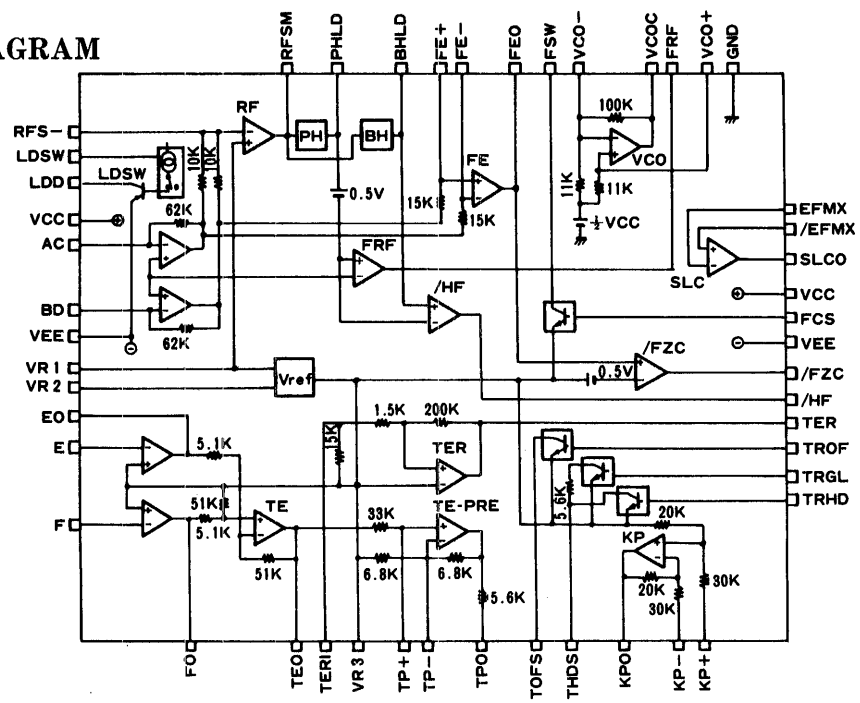


D/A CONVERTER

2-Channel Serial & Binary input Floating D/A Converter

YM3020 DAC[CD]

■ OUTLINE

The YM 3020 : DAC-FS is a floating D/A converter (referred to as DAC hereafter) with the 2-channel serial and 16-bit binary input or 2's complement input. It can produce analog output (16-bit dynamic range) which has 13-bit mantissa and 7-step exponent characteristic for the input digital signal.

■ FEATURES

- 16-bit input format can select either binary or 2's complement (equipped with a built-in floating converter logic).
- Externally equipped with buffer operational amplifier it allows easy analog output.
- 16-bit wide dynamic range.
- Capable of processing PCM sound source up to 2 channels.
- Equipped with a built-in analog switch for sample hold.
- Lower noise and less harmonic distortion and outstanding temperature characteristics. Zero cross distortion is extremely little.
- Made by the monolithic process of highly accurate thin film resistance and CMOS and enclosed in the 16-pin plastic DIL package.

■ Electrical characteristics

1. Absolute Maximum Rating

Item	Rating	Unit
Supply voltage	−0.3 ~ +15.0	V
High-level input voltage	V_{DD} +0.3	V
Low-level input voltage	V_{SS} −0.3	V
Operating ambient temperature	0 ~ 70	°C
Storing temperature	−50 ~ +125	°C

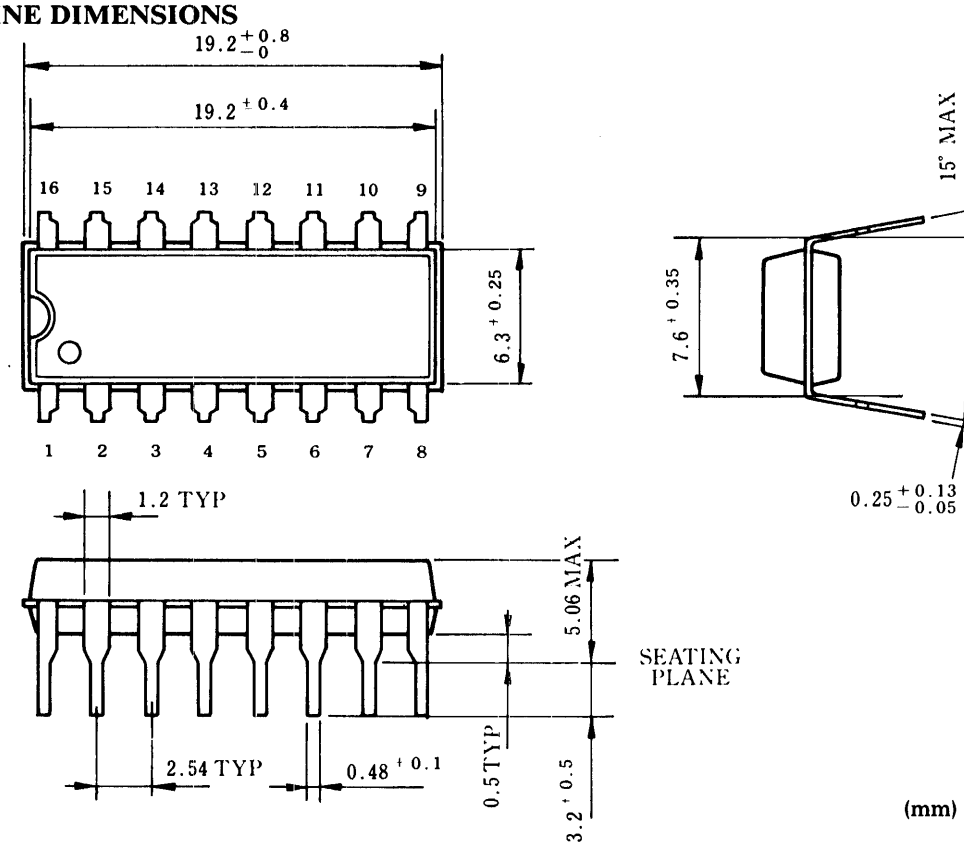
2. Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	9.0	12.0	12.0	V
	V_{SS}	0	0	0	V
Input signal voltage	CLOCK, SD, SMP1, 2, $\overline{ICL}$	0	—	V_{DD}	V
Operating ambient temperature	Ta	0	—	70	°C

3. DC Characteristics

Item	Symbol	Measuring Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	$V_{DD} \geqq 9.0V$	1/3 V_{DD}	—	—	V
Low-level input voltage	V_{IL}	$V_{DD} \geqq 9.0V$	—	—	1.0	V
Input current	I_{IN}	$V_{DD} = 12.0V$	—	—	10^{-3}	μA
Analog output voltage	V_{OUT}		—	0.50V_{DD}	—	Vp−p
Supply current	I_{DD}	$V_{DD} = 12.0V$	—	—	6	mA

■ OUTLINE DIMENSIONS



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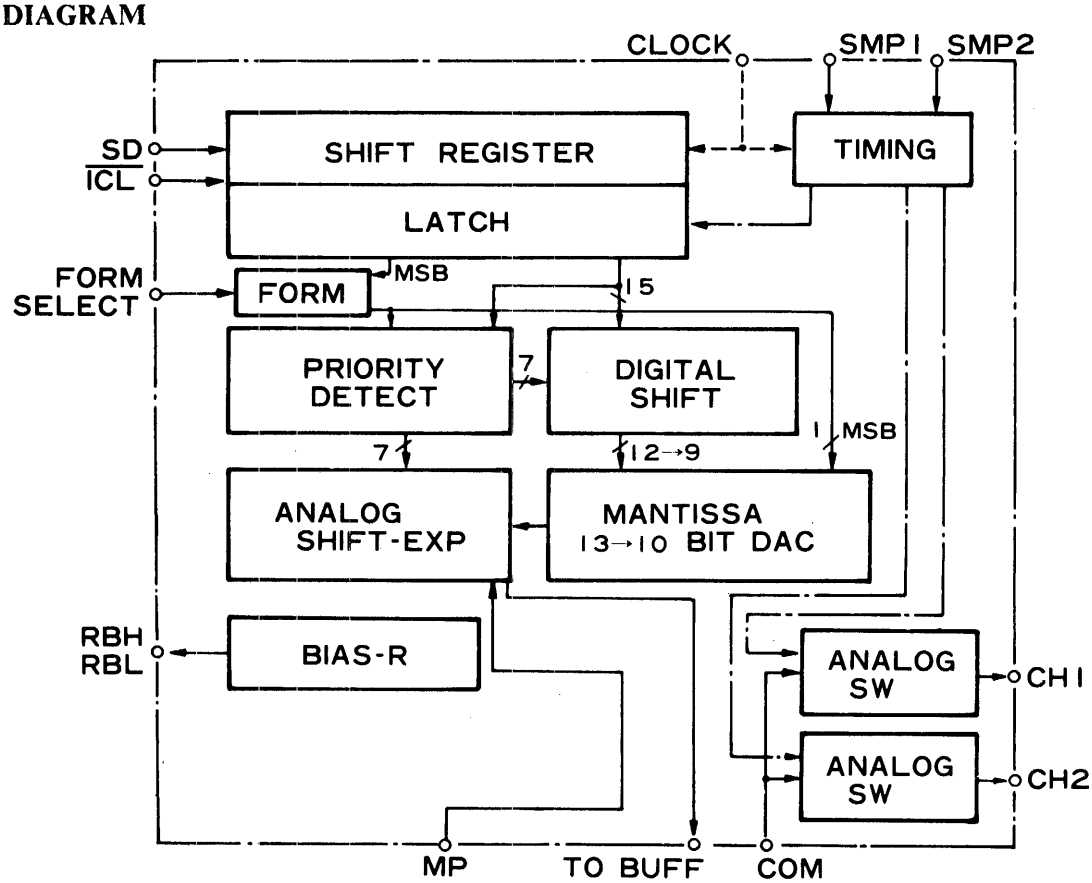


D/A CONVERTER

2-Channel Serial & Binary input Floating D/A Converter

YM3016 DAC[CD]

■ OUTLINE

The YM3016 : DAC-GS is a Floating D/A converter (referred to as DAC hereafter) with the 2-channel serial and 16-bit binary input or 2's complement input. It can produce analog output (16-bit dynamic range) which has 10-bit mantissa and 7-step exponent characteristic for the input digital signal.

■ FEATURES

- 16-bit input format can select either binary or 2's complement (due to built-in floating converter logic).
- Analog output can be obtained easily by adding a buffer operational amplifier, etc.
- 16-bit wide dynamic range.
- Capable of processing PCM sound source up to 2 channels.
- Equipped with a built-in analog switch for sample hold.
- Lower noise and less harmonic distortion and outstanding temperature characteristics.
- Made by the monolithic process of highly accurate thin film resistor and CMOS.
- Package type: 16 pin plastic SOP : YM3016F
  DIP : YM3016D
- +5V single power supply.

■ Electrical characteristics

① Absolute Maximum Ratings

Item	Rating	Unit
Supply voltage	−0.3 ~ +15.0	V
High-level input voltage	V_{DD} +0.3	V
Low-level input voltage	V_{SS} −0.3	V
Operating ambient temperature	0 ~ 70	°C
Storing temperature	−50 ~ +125	°C

② Recommended Operating Conditions

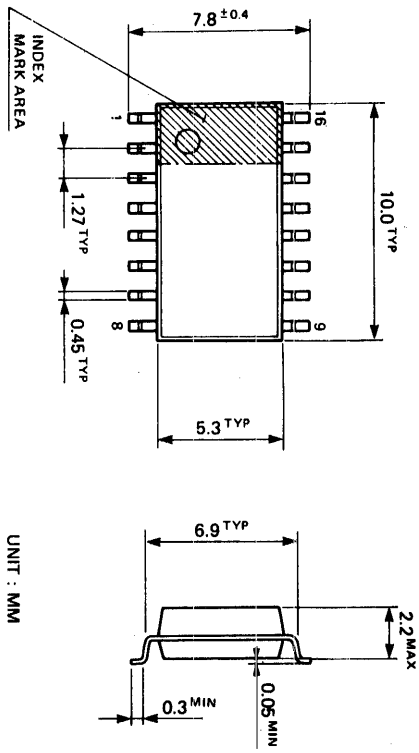
Item	Symbol	Min		Max	Unit
Supply voltage	V_{DD}	4.75*	5.0	5.25	V
	V_{SS}	0	0	0	V
Input signal voltage	CLOCK SD SMP1, 2 ICL	0	—	V_{DD}	V
Operating ambient temperature	Ta	0	—	70	°C

③ DC Characteristics

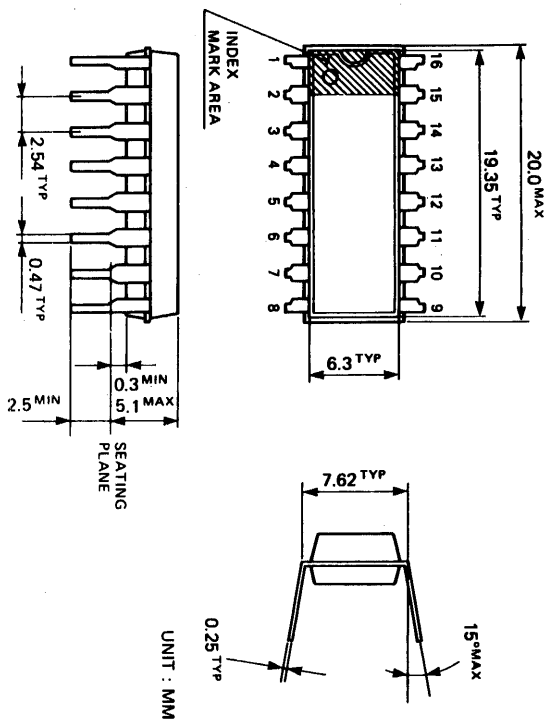
Item	Symbol	Measuring Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}		0.66V_{DD}	—	—	V
Low-level input voltage	V_{IL}		—	—	0.30V_{DD}	V
Input current	I_{IN}	V_{DD} = 5.0V	—	—	10^{-3}	μA
Analog output voltage	V_{OUT}		—	0.50V_{DD}	—	Vp−p
Supply current	I_{DD}	V_{DD} = 5.0V	—	—	6	mA

■ OUTLINE DIMENSIONS

YM3016-F



YM3016-D



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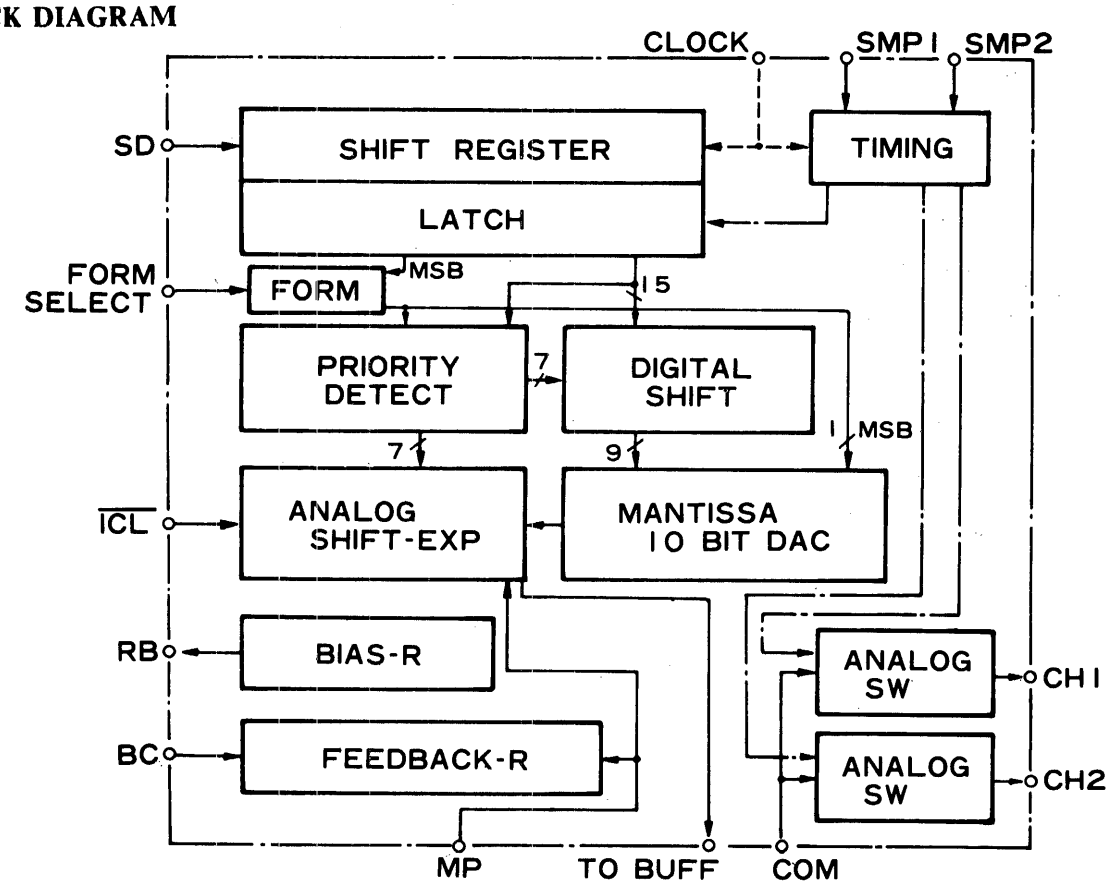


D/A CONVERTER

2-Channel Serial & Binary input Floating D/A Converter

YM3015 DAC(CD)

■ OUTLINE

The YM3015 : DAC-GS is a floating D/A converter (referred to as DAC hereafter) with the 2-channel serial and 16-bit binary input or 2's complement input. It can produce analog output (16-bit dynamic range) which has 10-bit mantissa and 7-step exponent characteristic for the input digital signal.

■ FEATURES

- 16-bit input format can select either binary or 2's complement (equipped with a built-in floating converter logic).
- Externally equipped with buffer operational amplifier it allows easy analog output.
- 16-bit wide dynamic range.
- Capable of processing PCM sound source up to 2 channels.
- Equipped with a built-in analog switch for sample hold.
- Lower noise and less harmonic distortion and outstanding temperature characteristics.
- Made by the monolithic process of highly accurate thin film resistor and CMOS and enclosed in the 16-pin plastic flat package.

■ ELECTRICAL CHARACTERISTICS

① Absolute Maximum Ratings

Item	Rating	Unit
Supply voltage	−0.3 ~ +15.0	V
High-level input voltage	V_{DD} +0.3	V
Low-level input voltage	V_{SS} −0.3	V
Operating ambient temperature	0~70	°C
Storing temperature	−50~+125	°C

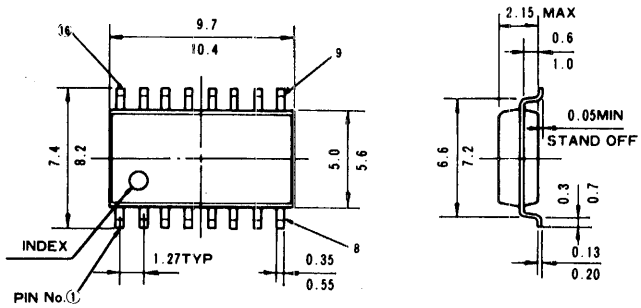
② Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	9.0	12.0	12.0	V
	V_{SS}	0	0	0	V
Input signal voltage	CLOCK SD SMP1, 2 $\overline{ICL}$	0	—	V_{DD}	V
Operating ambient temperature	Ta	0	—	70	°C

③ DC Characteristics

Item	Symbol	Measuring Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	$V_{DD} \geqq 9.0V$	1/3 V_{DD}	—	—	V
Low-level input voltage	V_{IL}	$V_{DD} \geqq 9.0V$	—	—	1.0	V
Input current	I_{IN}	V_{DD} = 12.0V	—	—	10^{3}	μA
Analog output voltage	V_{OUT}		—	0.50V_{DD}	—	Vp-p
Supply current	I_{DD}	V_{DD} = 12.0V	—	—	6	mA

■ OUTLINE DIMENSIONS



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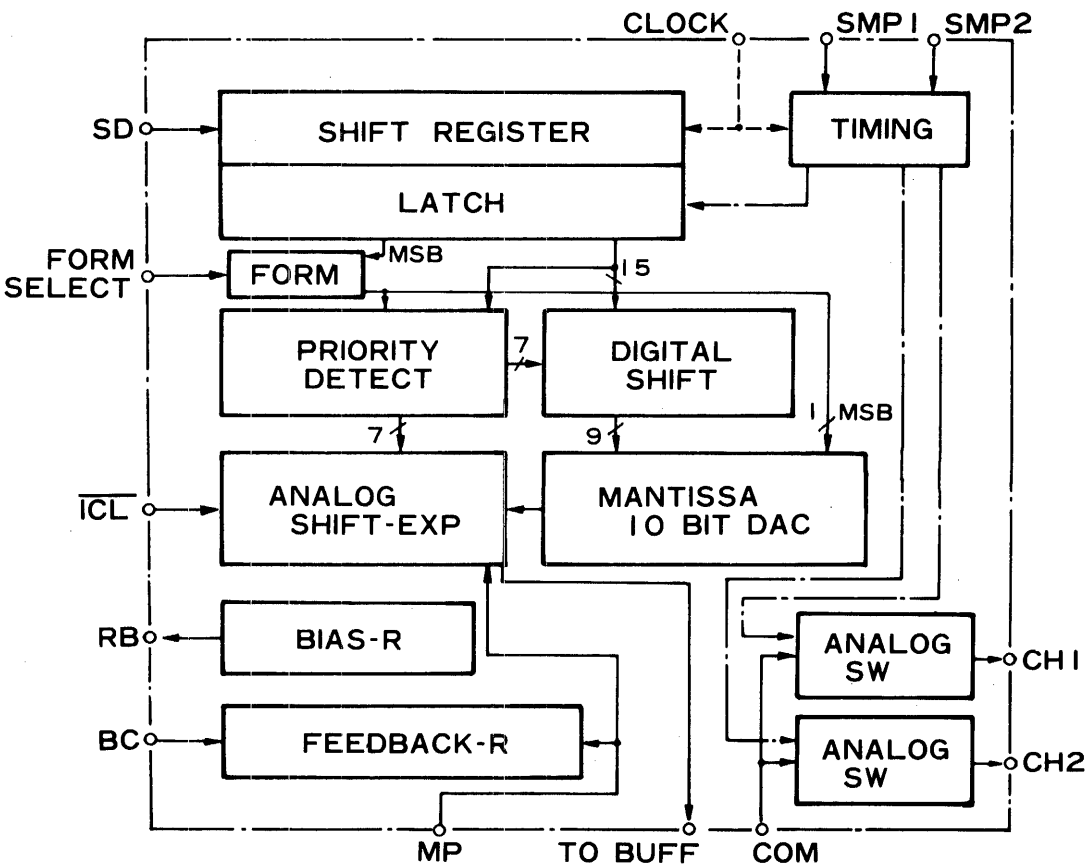


Sound generator

ADPCM Voice Analysis/Synthesis LSI

PRELIMINARY

YM6616

■ OUTLINE

The YM6616 is a voice recording and playing back LSI using the ADPCM analysis/synthesis method. With this method, the difference between voice data and expected data within the required bandwidth is coded in quantized width (appropriate quantized width), which varies flexibly with voice waveform deviation, to maintain sound quality at reasonable levels and enable compression of bit rate required for play.

Using this LSI enables incorporation of record/play functions of human voices and innate sounds of the natural world using a comparatively simple circuit.

■FEATURES

- Adoption of 4-bit ADPCM voice analysis/synthesis method
- Built-in 12-bit AD/DA converter
- Can interface to DRAM and ROM as external memory
  The external memory can be composed of 256k bit×4 pieces or 1M bit×4pieces for both DRAM and ROM.
- Can interface to a 4-bit CPU.
- Built-in 2-bit general purpose output port
- Play repeat capability
- 4 types of sampling frequency can be selected by software for the same master clock . (Fs=4, 5, 6, 8, KHz when master clock is 4MHz) Master clock is 10MHz in maximum.
- Built-in quartz oscillation circuit.
- Low power consumption due to CMOS technology
- 64 pin QFP package
- +5V single power supply

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings(VSS=OV)

ITEM	SYMBOL	RATING		UNIT
		MIN	MAX	
Supply voltage	VDD	−0.5	−7.0	V
Input voltage	Vi	−0.5	VDD+0.5	V
Output voltage	Vo	−0.5	VDD+0.5	V
Input current	Ii	−20	+20	mA
Storage temperature	TSTG	−50	+125	℃

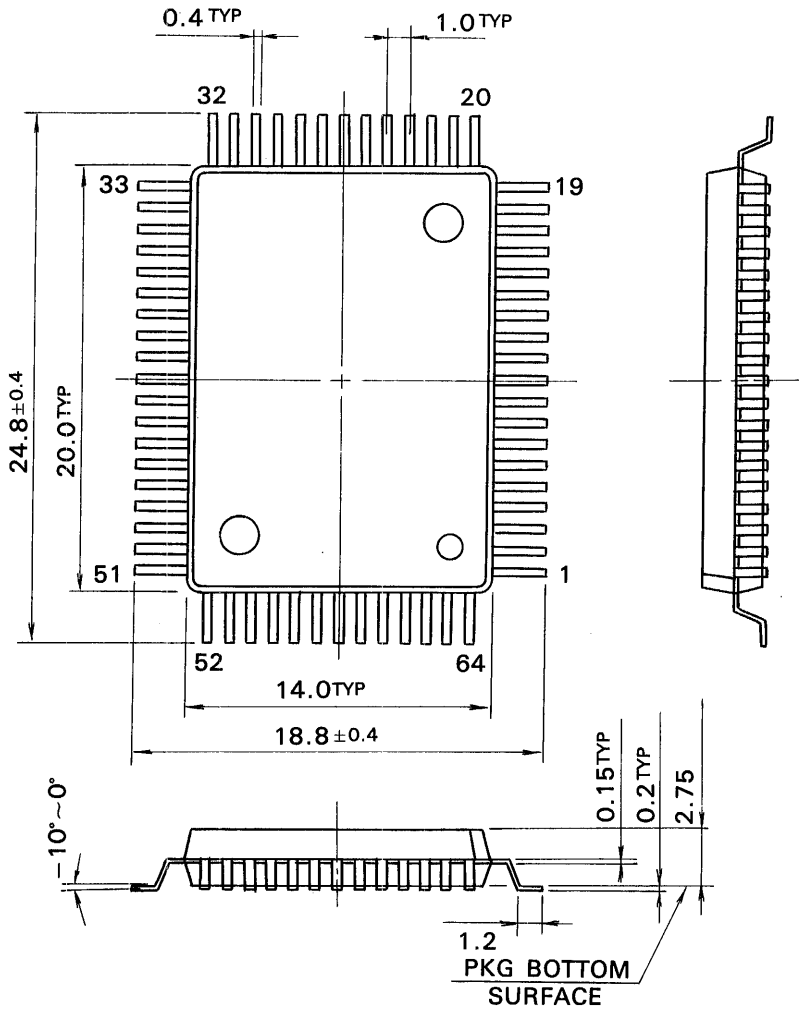
2.Recommended Operating Conditions(VSS=OV)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	VDD	4.75	5.00	5.25	V
Operating temperature	TOP	0	25	70	℃
Clock frequency	ϕM		4	10	MHz

Operations of the LSI may not be guaranteed if it is used underconditions other than those given above.

The specifications of this product are subject to improvement changes without prior notice.

■ OUTLINE DIMENSIONS



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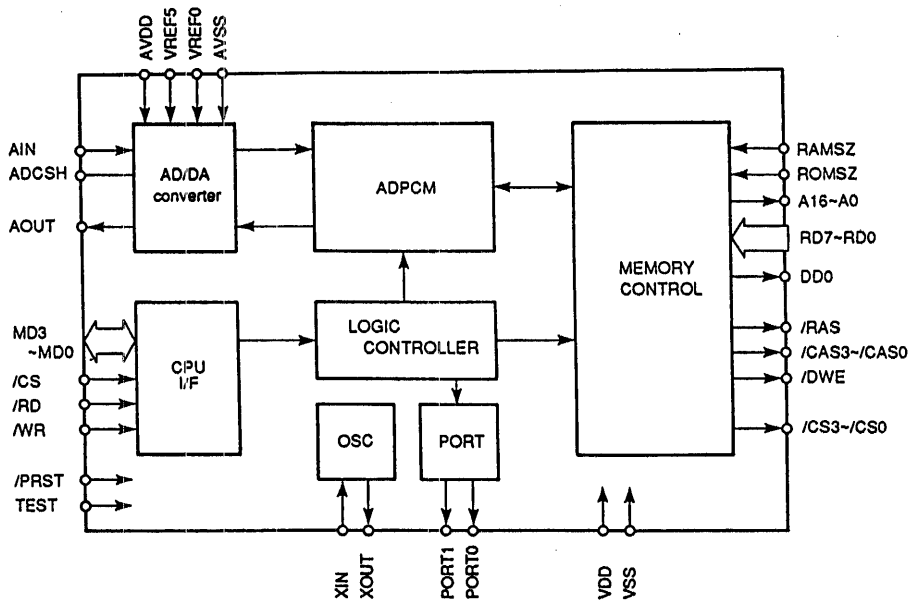


Sound generator

ADPCM Sound Generating LSI

YM7140

PRELIMINARY

■ OUTLINE

- This LSI is a sound reproduction LSI using ADPCM1 cell (Yamaha Standerd-cell for sound reproduction).
- This ADPCM Sound Generator series has built-in ROM and customers can implement arbitrary sound data.
- LSI chip including following DRUM sound is available as an example.
  ① Bass drum ② Snare drum ③ Tom Tom ④ Cymbal ⑤ Hi-hat
- Sampling frequency 8KHz
- ROM capacity 64Kbit
- Total sound generating duration 2seconds
- Start trigger input 5
- Built-in Chattering canceller
- Built-in 8bit DA converter
- Master clock 4KHz
- +5V power supply
- 18pin DIP

■ ELECTRICAL CHARACTERISTICS

Maximum Ratings

ITEM	SYMBOL	RATING		UNIT
		Min.	Max.	
Supply voltage	V_{DD}	$V_{SS}-0.5$	$V_{SS}+7.0V$	V
Input voltage	Vi	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output voltage	Vo	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input current	Ii	−20	+20	mA
Storage temparature	T_{STG}	−50	125	℃

($V_{SS}=0V$)

Recommended Operating Conditions

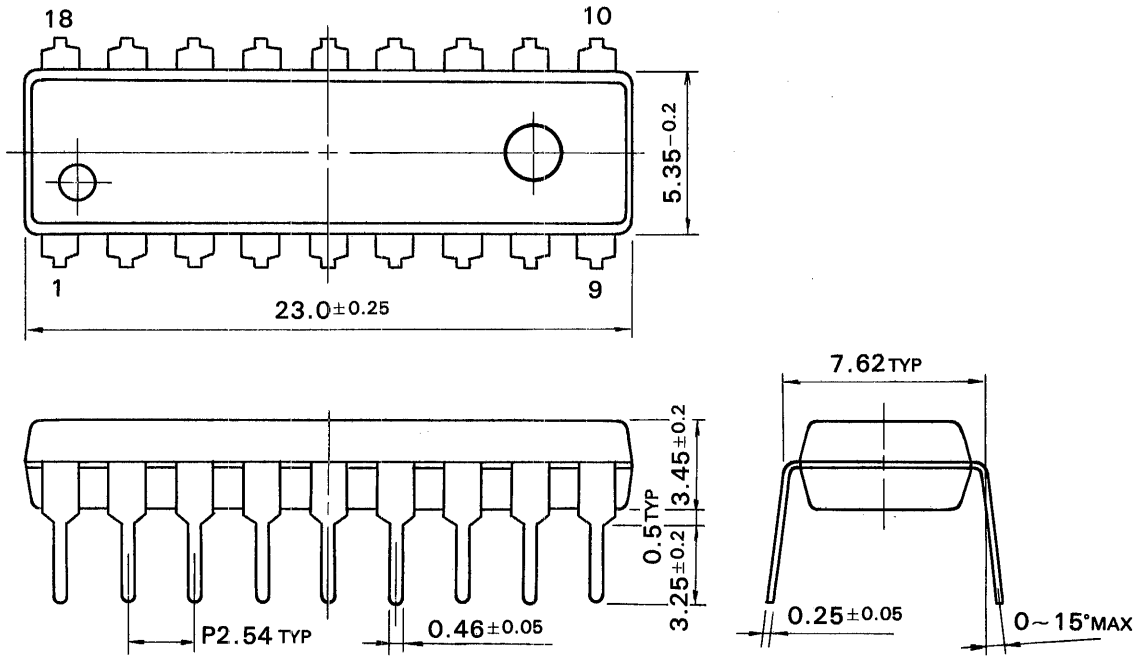
ITEM	SYMBOL	Min.	Typ.	Max.	UNIT
Supply voltage	V_{DD}	4.75	5.00	5.25	
Ambient operating temparature	Top	0	25	70	℃

DC Characteristics

ITEM		SYMBOL	Min.	Typ.	Max.	UNIT
Input high level voltage	All input	V_{IH}	3.5	−	−	V
Input low level voltage	All input	V_{IL}	−	−	1.0	V
Input leak current			−10	−	+10	MA

The specifications of this product are subject to improvement changes without prior notice.

■ OUTLINE DIMENSIONS



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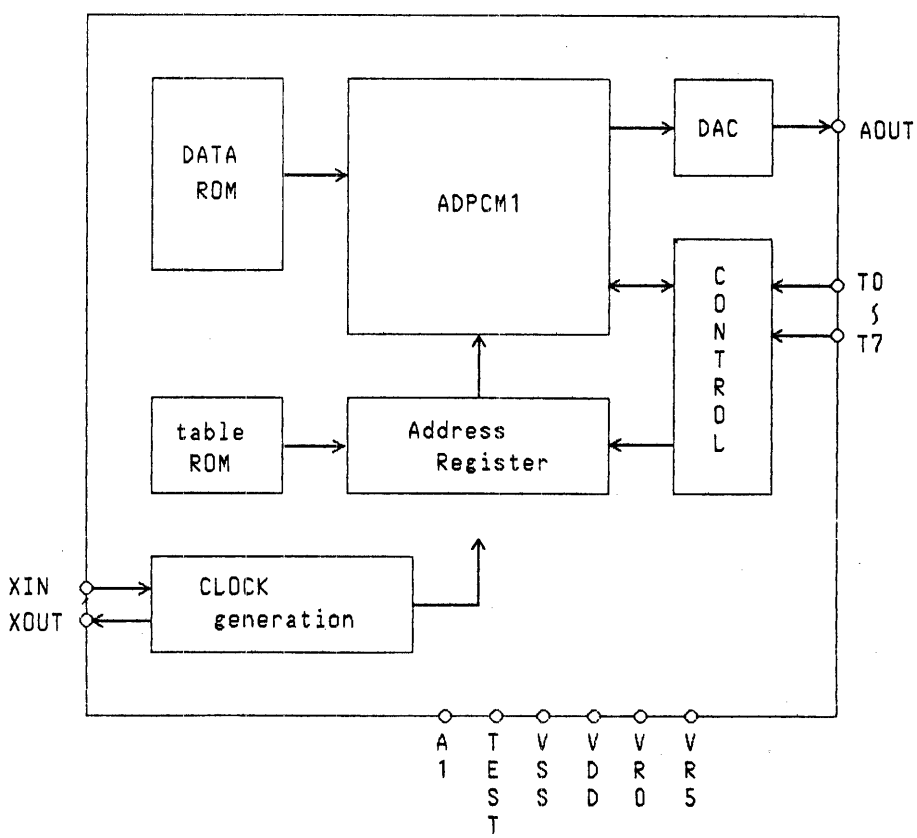

SOUND CHIP

FM MUSIC

YM 64AXX series

■ OUTLINE

The YM64AXX Series is a product line of ICs designed for automatic performance employing FM sound sources.

The IC stores timbre data and performance data in a built-in ROM, and is capable of automatic performance in up to 511 steps (4 melodies selectable), with 4 sounds generated simultaneously and in 3 full octaves of sound range.

Rewriting of this ROM data allows the user to produce various kinds of FM music.

A built-in DAC and crystal oscillation circuit for the simplified circuit configuration also make low cost development of an automatic performance system possible.

■ FEATURES

- Realistic sounds that employ FM sound sources (2-operator mode)
- Number of simultaneous sounds ... Up to 4 sounds (4 independent timbres possible)
- Melody data ... 4 melodies (or 4 phrases) selectable within up to 511 steps)
- Timbre data* ... Up to 4 timbres can be set for 1 melody (or 1 phrase).
  Maximum of 16 timbre presets for 4 melodies.
  * 14 timbres are supplied by the manufacturer.
- Performance modes ... Repeated performance of all melodies or of specified melody is possible.
- Repeated performance is also possible by using the JUMP command.
- Built-in DAC and crystal oscillation circuit.
- C-MOS low power consumption
- +5V power supply
- 16-pin DIP package (plastic)

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Raing	Unit
Input terminal voltage	−3.0−7.0	V
Operating temperature	0−70	°C
Storage temperature	−50−125	°C

2. Recommended operating conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.0	5.25	V
	GND	0	0	0	V

3. DC characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Low-level input voltage	V_{IL}		−0.3		0.8	V
High-level input voltage	V_{IH}		2.0		V_{DD}	V
Low-level clock input voltage	V_{CL}		−0.3		0.8	V
High-level clock input voltage	V_{CH}		2.0		V_{DD}	V
Input current leak	I_{IL}	V_{IN}=0−5V	−10		10	μA
Low-level output voltage	V_{OL}				0.4	V
High-level output voltage	V_{OH}		4.0			V
Analog output voltage	V_{OA}	A_{OUT} maximum amplitude			2.5	Vp-p
Power supply current	I_{DD}				18	mA
Input capacitance	C_I	f=1MHz			10	pF
Output capacitance	C_O				10	pF

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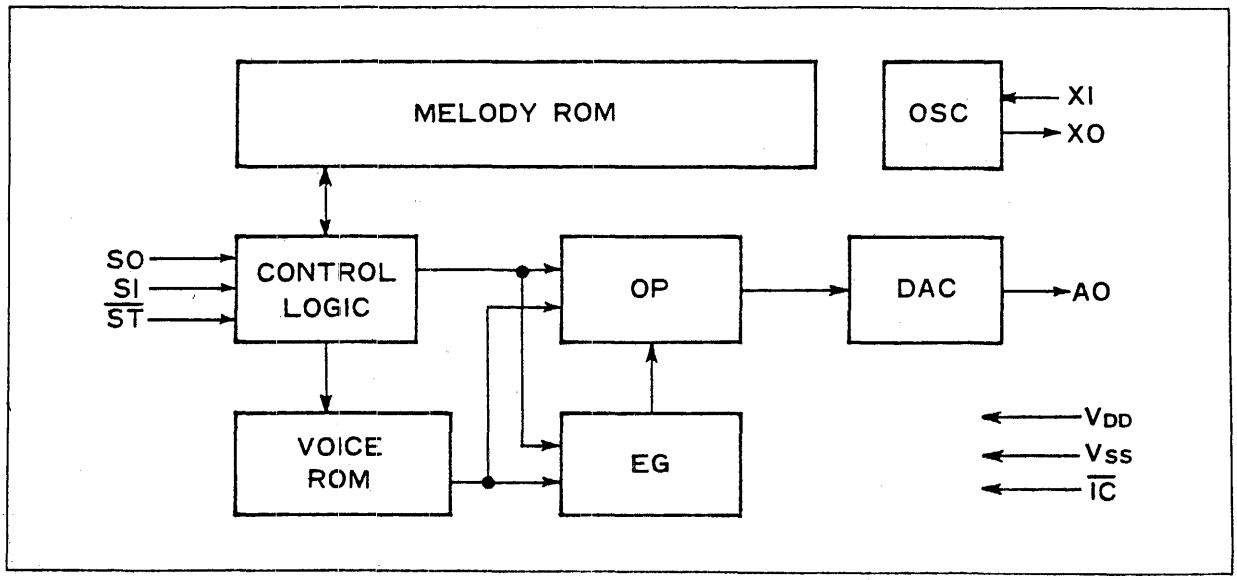
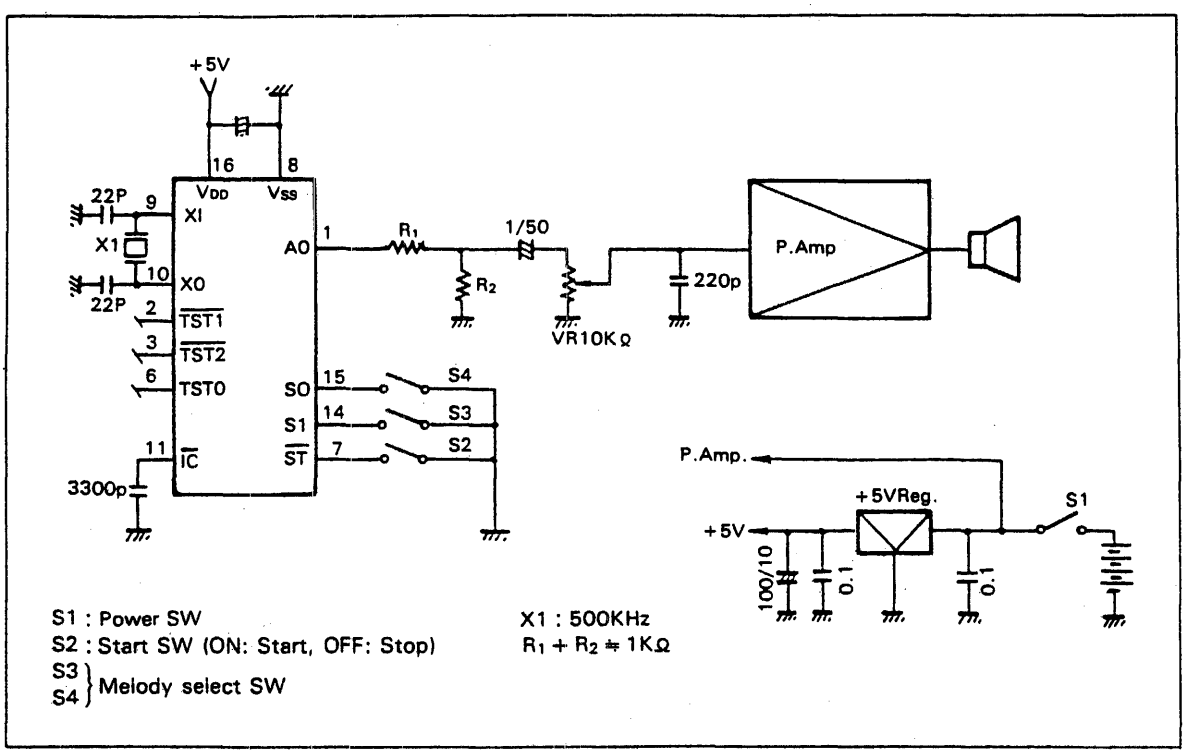


■ EXAMPLES (for reference)

Example of standard circuit



GRAPHICS

Versatile Panel Display Controller

V6388B VPDC

■OUTLINE

The versatile panel display controller (VPDC) is a high-level display controller with functions for controlling large-capacity flat panel displays (hereinafter simply "panels") and for controlling raster-scanning CRT displays. In addition, since application software written for CRTs can be used as is when the VPDC BIOS is used, portable and transportable computers with panels can be configured easily. (Display switching between CRT and panel as necessary is possible.)

This VPDC is completely compatible with the IBM-PS/2 video graphics array(VGA). When a standard monitor is used, this compatibility requires no change to the BIOS or software whatsoever. Even if a non-standard monitor is used, compatibility can be achieved by simply setting the values of switches with the VPDC BIOS. There is no need to change the software at all. For example when an IBM monochrome monitor and 2-tone panel are used, color display software can be executed. (Monitors that can not display colors handle this with gray scaling and hatching.)

It can also be easily configured for higher level display systems, with a built-in color look-up table(LUT) for color mapping.

■FEATURES

- Compatible with the IBM VGA in register level (when CRT is used); CPU interface is PC-BUS specification.
- Since all the functions of the VGA have been included, the VGA board functions can be realized with few parts for IBM PC compatibles. Furthermore, LCD, plasma displays, and EL displays can be controlled as well.
- The VPDC can be connected to the following CRTs:
  - IBM monochrome display
  - IBM enhanced color display
  - IBM 8503 monochrome display
  - IBM 8512 color display
  - IBM 8513 color display
  - IBM color display
  - NEC Multisync monitor (and models from other manufacturers that have the same functions)
- The VPDC can be connected to panels(LCD, plasma, EL and various other panels) with the following resolutions:
  - 640×200 - 320×200 - 640×400 - 720×400 - 640×480 - 640×350
- Eight 64K×4 dynamic RAM chips or eight 32K×8 static RAM chips can be used for video RAM (for a maximum of 256 KB)
- Up to 16 colors can be displayed for 640×480 dots.
- 1-screen panels and 2-screen panels can be used.
- The duty cycle can be set as high as 1/512 when a 2-screen panel is used.
- The AC signal for the LCD panel can be set freely in units of 1 Horizontal scan (with a maximum pulse width of 1024h).
- Data can be sent to the panel in parallel 4 or 8 bits at a time or serially.
- Color liquid crystal displays can be used (320×200 dots by 8 colors)
- 16-shade display is possible with panels and monochrome monitors. (Of these 16, 9 can be converted into 9 hatching patterns.)
- Screen display position compensation is possible when using panels the same as for CRTs (Screen center can also be adjusted).
- Multi-raster scan function (display taking into account the aspect ratio)
- Built-in look-up table (LUT) for color mapping
- CMOS, 128-pin QFP

■ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (with Vss = 0.0V as the standard)

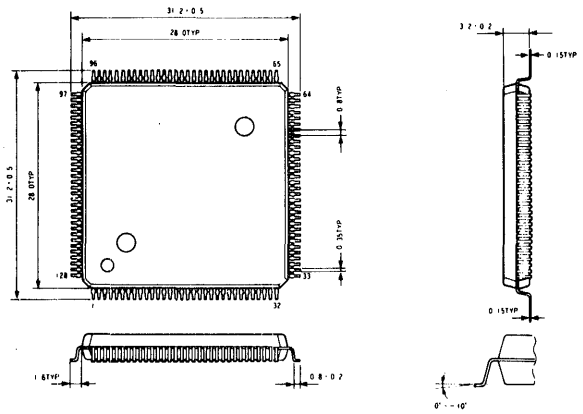
Item	Symbol	Min.	Max.	Unit
Power supply voltage	V_{DD}	-0.3	7.0	V
Input voltage	V_I	-0.3	V_{DD}+0.3	V
Output voltage	V_O	-0.2	V_{DD}+0.3	V
Operating ambient temperature	V_{OP}	0	70	℃
Storage temperature	T_{STG}	-50	125	℃

Recommended Operating Conditions (with Vss = 0.0V as the standard)

Item	Symbol	Min.	Typ.	Max.	Unit.
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating ambient temperature	T_{OP}	0	25	70	℃
Low level input voltage*	V_{IL}			0.8	V
High level input voltage*	V_{IH}	2.0			V

*: except for clock input

■ OUTLINE DIMENSIONS



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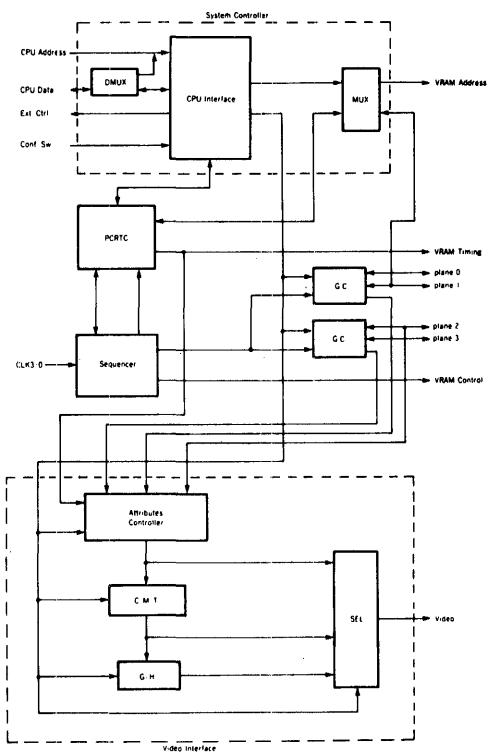


GRAPHICS

Enhanced Panel Display Controller

V6377 EPDC

■ OUTLINE

The enhanced panel display controller (EPDC) is a high-level display controller with functions for controlling large-capacity flat panel displays (hereinafter simply "panels") and for controlling raster-scanning CRT displays. In addition, since application software written for CRTs can be used as is when the EPDC BIOS is used, portable and transportable computers with panels can be configured easily. (Display switching between CRT and panel as necessary is possible.) This EPDC is completely compatible with the IBM-PC enhanced graphics adapter (EGA). When a standard monitor is used, this compatibility requires no change to the BIOS or software whatsoever. Even if a non-standard monitor is used, compatibility can be achieved by simply setting the values of switches with the EPDC BIOS. There is no need to change the software at all. For example when an IBM monochrome monitor and 2-tone panel are used, color display software can be executed. (Monitors that can not display colors handle this with gray scaling and hatching.)

In addition to EGA display capacity, the EPDC has expanded display functions, so it can also display 640 x 480 dots. It can also be easily configured for higher level display systems, with a built-in color look-up table (LUT) for color mapping.

■ FEATURES

- Since IBM EGA CRT-controller functions have been included, the EGA board function is realized with few parts. Furthermore, LCDs, plasma displays, and EL displays can be controlled as well.
- The EPDC can be connected to the following CRTs:
  - · IBM monochrome display
  - · IBM color display
  - · IBM enhanced color display
  - · NEC Multisync monitor (and models from other manufacturers that have the same functions)
- The EPDC can be connected to panels (LCD, plasma, EL) with the following resolutions:
  · 640 x 200, · 320 x 200, · 640 x 400, · 640 x 480,
- Eight 64K x 4 dynamic RAM chips or eight 32K x 8 static RAM chips can be used for video RAM (for a maximum of 256 KB)
- Up to 16 colors can be displayed for 640 x 480 dots.
- 1-screen panels and 2-screen panels can be used.
- The duty cycle can be set as high as 1/512 when a 2-screen panel is used.
- The AC signal for the LCD panel can be set freely in units of 1Horizontal scan (with a maximum pulse width of 1024H).
- Data can be sent to the panel in parallel 4 or 8 bits at a time or serially.
- Color liquid crystal displays can be used (320 x 200 dots by 8 colors)
- 16-shade display is possible with panels and monochrome monitors. (Of these 16, 9 can be converted into 9 hatching patterns.)
- Screen display position compensation is possible when using panels the same as for CRTs (Screen center can also be adjusted).

■ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (with Vss = 0.0V as the standard)

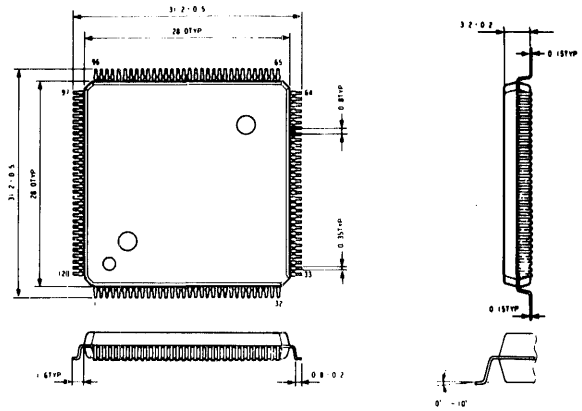
Item	Symbol	Min.	Max.	Unit
Power supply voltage	V_{DD}	0.3	7.0	V
Input voltage	V_I	0.3	V_{DD}+0.3	V
Output voltage	V_O	0.2	V_{DD}+0.3	V
Operating ambient temperature	V_{OP}	0	70	°C
Storage temperature	T_{STG}	50	125	°C

Recommended Operating Conditions (with Vss = 0.0V as the standard)

Item	Symbol	Min.	Typ.	Max.	Unit.
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating ambient temperature	T_{OP}	0	25	70	°C
Low level input voltage*	V_{IL}			0.8	V
High level input voltage*	V_{IH}	2.0			V

*: except for clock input

■ OUTLINE DIMENSIONS



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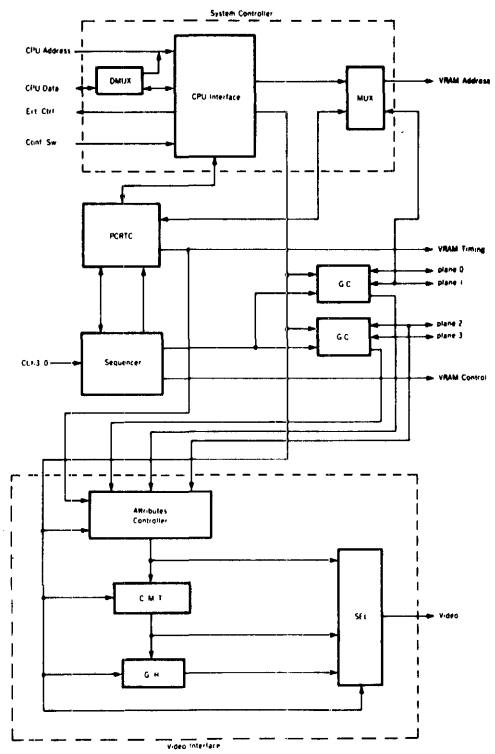


GRAPHICS

Panel Display & CRT Display Controller

V6366C-F PCDC

■ OUTLINE

The PCDC (Panel Display & CRT Display Controller) is a display controller that has the two functions: (1) the display control of a high-capacity flat-panel display (hereafter referred to as a "Panel") and (2) the display control of a raster-scan type CRT. By merely performing initialization, however, even the Panel can be used without changing the software for conventional CRTs, enabling the simple system configuration of a handheld or portable computer which uses the Panel. (If so required, the PCDC can also be used to switch the display monitor between a CRT and a Panel.)

The PCDC is compatible with the CGA (Color Graphics Adapter), MDA (Monochrome Display Adapter), and HGC (Hercules Graphics Card), all for IBM PC application. In case the software and hardware for connecting a regular monitor come as a pair, the PCDC offers compatibility without requiring software changes (initialization is also unnecessary). Even in case of connecting different monitors, initialization will only be performed once at Power Start-Up, then compatibility will be available without requiring any software changes. It is thus possible, for example, to run CGA software using an IBM monochrome monitor and the Panel. (A gray scaling/hatching display can be used with a monochrome monitor.)

Because the PCDC has the display capacity of the IBM PC as well as numerous other expansion functions, including Kanji display, Color Palette, and the capability to simultaneously display up to 256 colors, a high-performance display system can be easily configured.

■ FEATURES

- All functions of MC6845 are built in (excluding the Interlacing & Video Mode and the Skew function).
- In addition to a CRT or LCD, an EL and Plasma Display can also be connected.
- A 640 by 400 PEL (picture element or pixel). Panel can be driven (a 720 by 350 PEL Panel can also be driven).
- A one-screen Panel or two-screen Panel (split into upper and lower halves) can be used.
- A two-screen panel allows, at a maximum duty, display of up to 512 lines (1/256).
- Selection of 1-, 2-, 4- or 8-bit parallel transmission of data to the Panel.
- A gray scaling/hatching display can be used with the Panel or a monochrome monitor.
- IBM PC software for 640 by 200 PELs can be directly displayed on a 640 by 400 PEL screen. (An 8 by 16 character font can be used, and can be displayed even in Double Scan Mode.)
- In addition to the standard IBM PC Graphics Modes, a variety of other Graphics Modes are provided: 320 by 200 PELs ×16 or 256 colors, 320 by 400 PELs × 4 or 16 colors, 640 by 200 PELs × 4 or 16 colors. 640 by 400 PELs × 4 colors, 640 by 350 PELs × 16 colors, and so on.
- A Protect Bit is provided for software protection.
- An SRAM or DRAM can be used as the VRAM. (Because the timing for display and the CPU are separate, the CPU can access VRAM at any time (without awaiting the retrace-timing.))
- Built-in interface for the Light Pen
- With a linear RGB monitor, 16 out of 512 colors can be simultaneously displayed.
- With an EGA monitor, 16 out of 64 colors can be simultaneously displayed.
- A Color Lookup Table can even be used with an IBM color monitor.
- A Standby function is provided to conserve power dissipation.
- Kanji display capacity of 16 by 16, 24 by 24 or 32 by 32 "PELs." (Attributes can also be used).
- The font configuration can be selected. Horizontal: 6, 7, 8, 9, 10, or [8 × integer] PELs (capable of a mixed display of half-width and full-width text); Vertical: 1 to 32 PELs.
- Capable of smooth scrolling and (in Interlace Mode only) external synchronization.
- Simultaneous display capability with an IBM color monitor and a one-screen LCD of 640 × 200.
- CMOS, 5V power supply, 100-pin QFP

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.3	V
Output voltage	V_O	−0.3	V_{DD}+0.3	V
Operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{STG}	−50	+125	°C

(Based on the reference voltage of V_{SS}=0.0V)

Recommended Operating Conditions

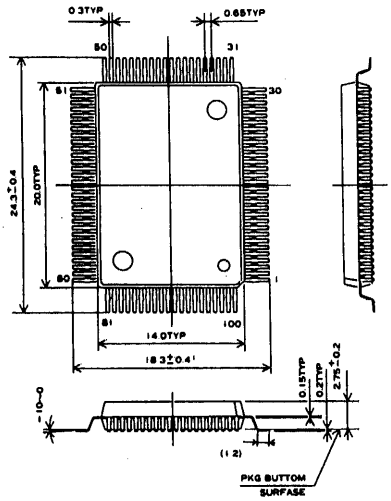
Supply voltage:	+5V±5% (based on V_{SS}=0.0V)
Operating temperature:	0~70°C

DC Characteristics (V_{DD}=5V±5%, T_{OP}=0~70°C)

Item	Symbol	Condition	Min.	Max.	Unit
High-level output voltage (for TTL driving)	V_{OH}	I_{OH}=−0.4mA	2.7		V
Low-level output voltage (for TTL driving)	V_{OL}	I_{OL}=0.8mA		0.4	V
High-level output voltage (for CMOS driving)	V_{OH}	$\|I_{OH}\|$<10μA	V_{DD}−0.4		V
Low-level output voltage (for CMOS driving)	V_{OL}	$\|I_{OL}\|$<10μA		0.4	V
High-level input voltage	V_{IH}		2.2		V
Low-level input voltage	V_{IL}			0.8	V
Input leak current	I_L		−10	10	μA
OFF status leak current	I_{LZ}		−10	10	μA
Power current (during normal operation)	I_{DD}			70	mA
Power current (during Standby)	I_{DD}			10	mA

NOTE: ILZ applies while the CD0-CD7, RD0-RD15, X2, RA4, or $\overline{ESY}$ pins are in input status or while the AD0/$\overline{XR}$ ~ AD15/GPE or MEMRDY pins are in high-impedance status.

■ OUTLINE DIMENSIONS



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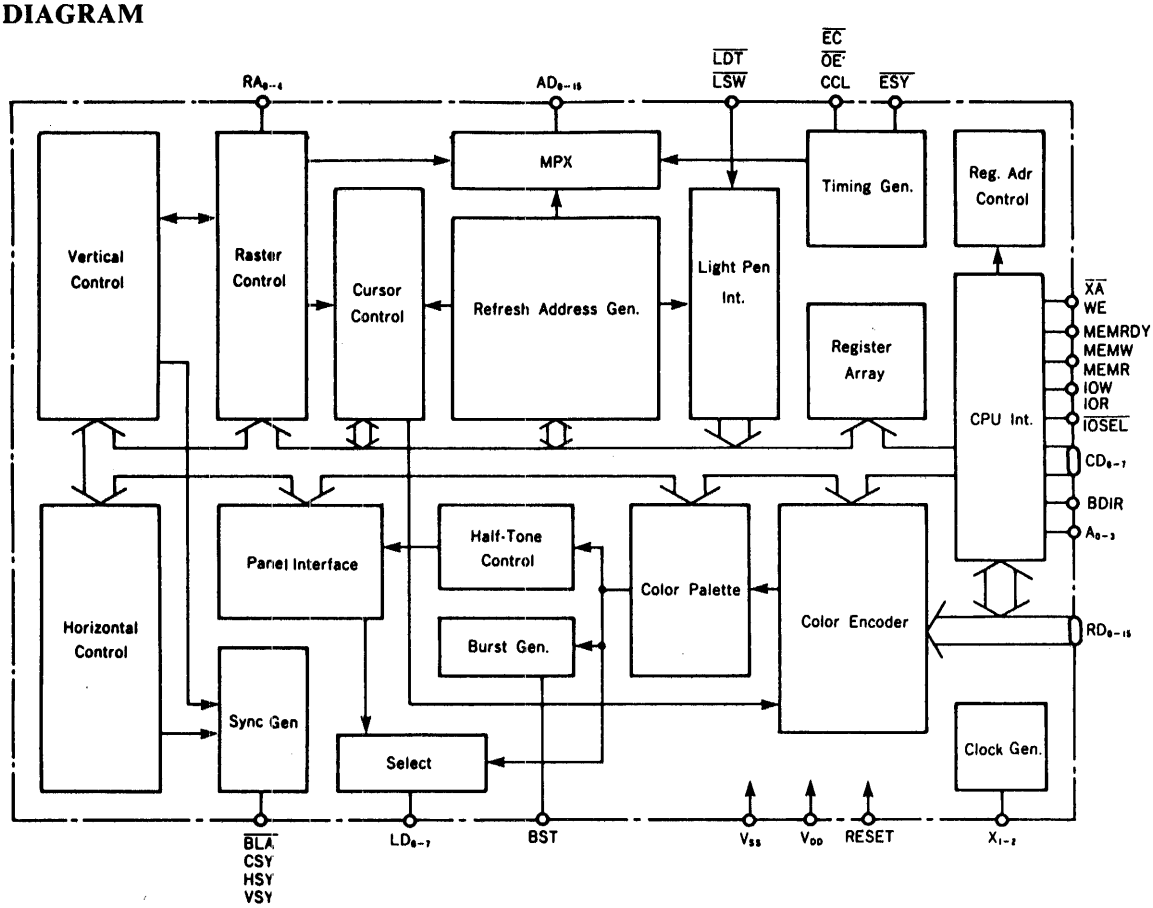


GRAPHICS

Advanced Monochrome Display Controller

YGV603

PRELIMINARY

■OUTLINE

The AMDC is compatible with the IBM-PC CGA (Color Graphics Adapter), the MDA (Monochrome Display Adapter), and the HGC (Hercules Graphic Card). Only the IBM monochrome monitor can be connected to the AMDC, so when using MDA and HGC software, full compatibility is provided without making any modifications to the software (including initial settings). When the CGA software package is used, the software type is recognized by the internal hardware and Emulation Mode is entered. When this mode is entered, the registers of the MC6845 are initialized automatically. In the Graphics Mode, a 5-level gray-scale display is produced. Furthermore, a built-in font ROM allows easy configuration of a display system by adding only a few external components.

■FEATURES

•Compatibility with MDA, HGC, and CGA is provided at the register level.
HGC supports both Page 0 and Page 1.
With CGA, only a monochrome monitor can be connected. (Color monitors are not supported.)
- A 132 Column Mode is supported among the MDA expansion modes.
- All MC6845 functions are built in (except for R8)
- A 5-level gray-scale display is possible with a monochrome monitor.
- A Protect bit is used to provide software protection.
- Only a DRAM can be used for the VRAM.

(Since the timing for the display and that for the CPU are separate, the CPU can access the VRAM at any point (without waiting for line retracing).
- The light pen interface is built in.
- The printer board is built in.
- A smooth-scroll function is provided (only in 132 Column Mode).
- A font ROM for the MDA is built in (external fonts can also be connected).
- An auto-switching circuit is built in.
- A 16 MHz crystal generator circuit is built in.
- A 25 MHz crystal generator circuit is built in.
- CMOS, 5V single power supply, 100-pin QFP

The specifications of this product are subject to improvement changes without prior notice.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	−0.8	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.3	V
Output voltage	V_O	−0.3	V_{DD}+0.3	V
Operating temperature	T_{OP}	0	+70	℃
Storage temperature	T_{STG}	−50	+125	℃

(Based on the reference voltage of V_{SS}=0.0V)

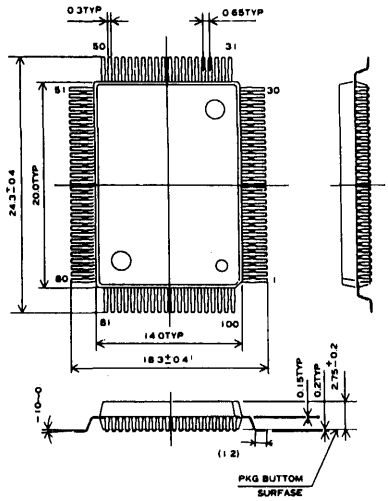
Recommended Operating Conditions

Supply voltage	+5±5% (based on V_{SS}=0.0V)
Operating temperature	0~70℃

DC Characteristics (V_{DD}=5V±5%, T_{OP}=0~70℃)

Item	Symbol	Condition	Min.	Max.	Unit
High-level output voltage (for TTL driving)	V_{OH}	I_{OH}=−0.4mA	2.4		V
Low-level output voltage (for normal output)	V_{OL}	I_{OL}=1.6mA		0.4	V
Low-level output voltage (Power output)	V_{OL}	I_{OL}=8.0mA		0.4	V
High-level input voltage	V_{IH}		2.0		V
Low-level input voltage	V_{IL}			0.8	V
Input leak current	I_L		−10	10	μA
OFF status leak current	I_{LZ}		−10	10	μA
Power current (during normal operation)	I_{DD}			70	mA

■ OUTLINE DIMENSIONS



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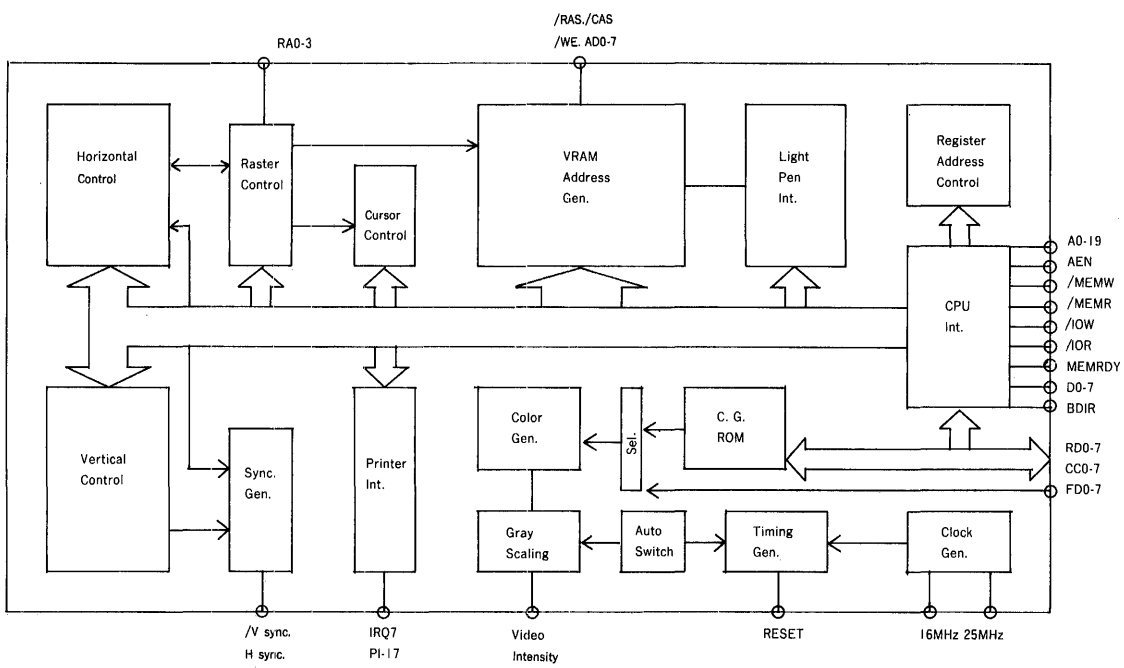

GRAPHICS

Enhanced Video Display Processor

V9978 E-VDP-III

PRELIMINARY

■ OUTLINE

The V9978 is a video display processor (VDP) which features as follows. Having a high-speed drawing and animation functions, it provides various screen modes which can be used for games, AV and OA purposes. Also, as a monitor, it supports many types of display units such as home TV sets, CRT for personal computers and LCD panels.

■ FEATURES

Game Specifications:

For this type, there are two pattern display modes as follows.

- P1 (Display resolution 256 × 212 2 screens)
- P2 (Display resolution 512 × 212)

Various highly advanced functions are available such as powerful sprite function and omnidirectional scroll function.

AV Specifications:

For this type, there are four kinds of bit map display modes which can be displayed on the NTSC or PAL frequency monitor as follows.

- B1 (Display resolution 256 × 212)
- B2 (Display resolution 384 × 240)
- B3 (Display resolution 512 × 212)
- B4 (Display resolution 768 × 240)

- Capable of doubling the resolution in the vertical direction by using the interlace.
- Display is possible up to 32,768 colors/dot.
- Built-in color palette (64 colors selected out of 32,768 colors).
- Omnidirectional smooth scrolling is possible.
- Superimposition and digitization are possible.

- Allows use of the monitor screen to the fullest extent in four directions as the display range by using the over-scan mode (B2, B4) in such application as for the telopper.
- Supports the high-speed hardware drawing commands such as the screen transfer, font color development and line.
- The hardware cursor display function is available.

OA Specifications:

For this type, there are two kinds of bit map display modes which can be displayed on the high resolution monitor as follows.

- B5 (Display resolution 640 × 400)
- B6 (Display resolution 640 × 480)

- Capable of displaying up to 16 colors/dot (Selectyable out of 32,768 colors depending on the color palette).
- Omnidirectional smooth scrolling is possible.
- Supports the high-speed hardware drawing commands such as the screen transfer, font color development and line.
- The hardware cursor display function is available.

Others:

- Built-in DA converter
- Linear RGB output
- Direct connection of CG ROM such as KANJI ROM is possible.
- Useable VRAM

  64K × 4
  128K × 8 } Dual port DRAM (The access time is 120ns, but 100ns for the B6 mode.)
  256K × 4
- As the VRAM capacity, 128KB, 256KB and 512KB configurations are possible.
- Capable of direct access from CPU to VRAM by means of the 16 bit bus.
- Use of the LCD panel (1 screen panel and single drive type of 2 screen panels) is possible.

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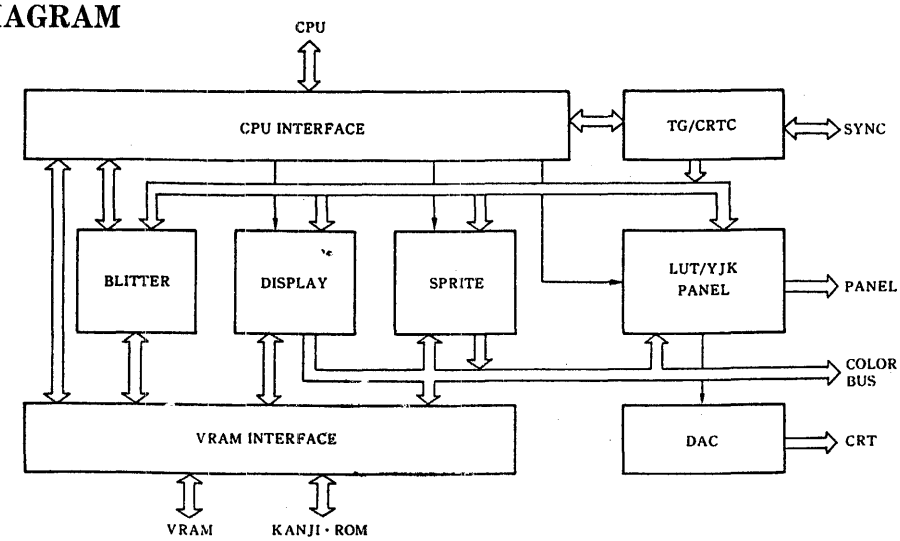
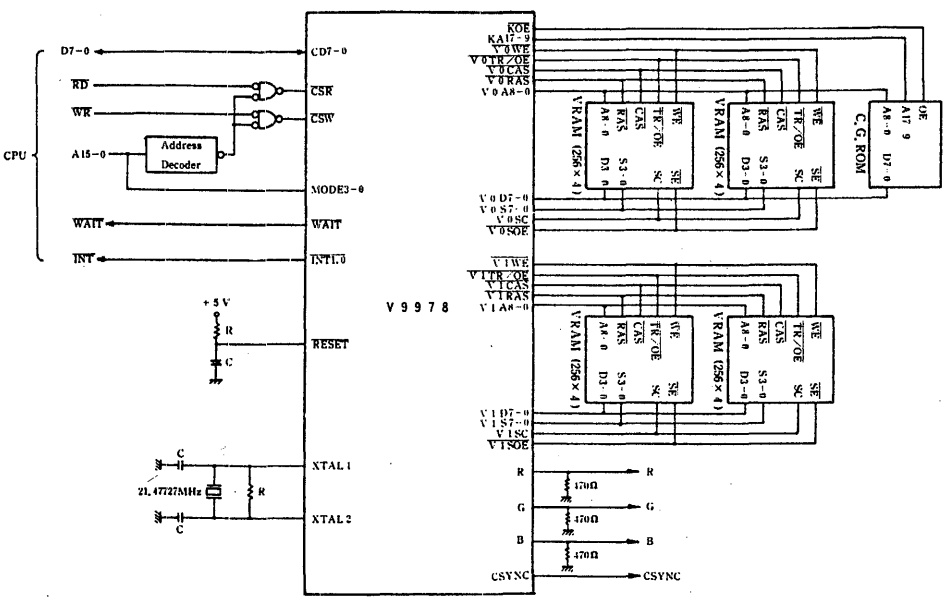


■ SYSTEM CONFIGURATION



GRAPHICS

Enhanced Video Display Processor

V9958 E-VDP-II

■ OUTLINE

V9958 (E-VDP-II) is a video display processor using an N-channel silicon gate MOS and a 64-pin shrink DIL plastic package. It is software compatible with TMS9918A and V9938.

■ FEATURES

- Outputs linear RGB.
- Built-in color palette for display in up to 512 colors.
- Capable of simultaneous display of 19,268 colors by using YJK system display.
- Capable of displaying up to 512 × 424 pixels and 16 colors.
- Bit mapped graphics.
- Capable of displaying maximum of 256 colors simultaneously.
- 16K byte ~ 128K byte useable for display memory.
- 16K × 1b, 16K × 4b, 64K × 1b and 64K × 4b DRAMs are useable.
- 256 addresses, 4ms auto refresh function of DRAM.
- Expansion video memory can be connected.
- Eight sprites can be displayed for each horizontal line.
- Colors for sprites can be specified for each horizontal line.
- Area move, line, search and other commands.
- Command function usable in every display mode.
- Logical operation function.
- Addresses can be specified by coordinates.
- Capable of external synchronization.
- Capable of superimposition.
- Capable of digitization.
- Multi E-VDP-II configurations are possible.
- External color palettes can be added by utilizing color-bus output.
- Vertical and horizontal scroll function.
- Wait function to CPU.
- 5V power supply.

■ ELECTRICAL CHARACTERISTICS

1. Maximum Ratings

Symbol	Item	Rating	Unit
V_{DD}	Power supply voltage	−0.5 ~ +7.0	V
Vin	Input voltage	−0.5 ~ +7.0	V
Ts	Storage temperature	−50 ~ +125	°C
To	Operating temperature	0 ~ +70	°C

2. Recommended Operating Conditions

Symbol	Item	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage	4.75	5.00	5.25	V
V_{SS}	Power supply voltage		0		V
T_A	Operating ambient temperature	0		70	°C
V_{IL} 1	Low level input voltage (group 1)	−0.3		0.8	V
V_{IL} 2	Low level input voltage (group 2)	−0.3		0.8	V
V_{IL} 3	External clock low level input voltage (group 3)	−0.3		0.8	V
V_{IH} 1	High level input voltage (group 1)	2.2		V_{DD}	V
V_{IH} 2	High level input voltage (group 2)	2.2		V_{DD}	V
V_{IH} 3	External clock high level input voltage (group 3)	3.5		V_{DD}	V

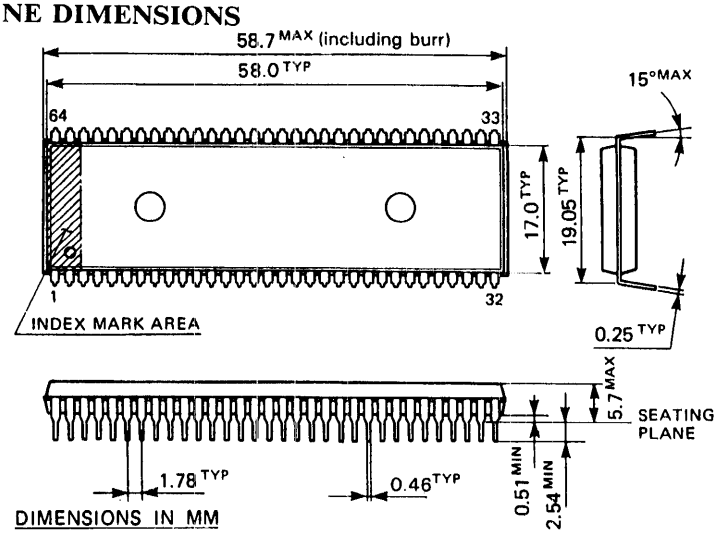
Note: Group 1 $\overline{CSR}$, RD0-7, C0-7, $\overline{LPS}$, $\overline{LPD}$, $\overline{RESET}$, DLCLK, $\overline{VRESET}$, $\overline{HRESET}$
Group 2 CD0-7, MODE 0, MODE 1, $\overline{CSW}$
Group 3 XTAL 1, XTAL 2

3. DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VOL 4	Low level output voltage (group 4)	IOL = 1.6mA			0.4	V
VOL 5	Low level output voltage (group 5)	IOL = 1.6mA			0.4	V
VOL 6	Low level output voltage (group 6)	IOL = 10mA			0.4	V
VOL 7	Low level output voltage (group 7)	IOL = 1.6mA			0.4	V
VOL 4	High level output voltage (group 4)	IOH = 100μA	2.4			V
VOL 5	High level output voltage (group 5)	IOH = 60μA	2.7			V
ILI	Input leak current				10	μA
ILO	Output leak current (when floating)				25	μA
IDD	Current consumption				230	mA

Note: Group 4 CD0-7, RD0-7, AD0-7, $\overline{VDS}$, CBDR, CPUCLK/$\overline{VDS}$, C0-7, $\overline{HSYNC}$, $\overline{CSYNC}$, $\overline{WAIT}$, YS
Group 5 $\overline{RAS}$, $\overline{CAS\ 0}$, $\overline{CAS\ 1}$, $\overline{CASX}$, R/$\overline{W}$
Group 6 $\overline{DLCLK}$, $\overline{DHCLK}$
Group 7 $\overline{INT}$

■ OUTLINE DIMENSIONS



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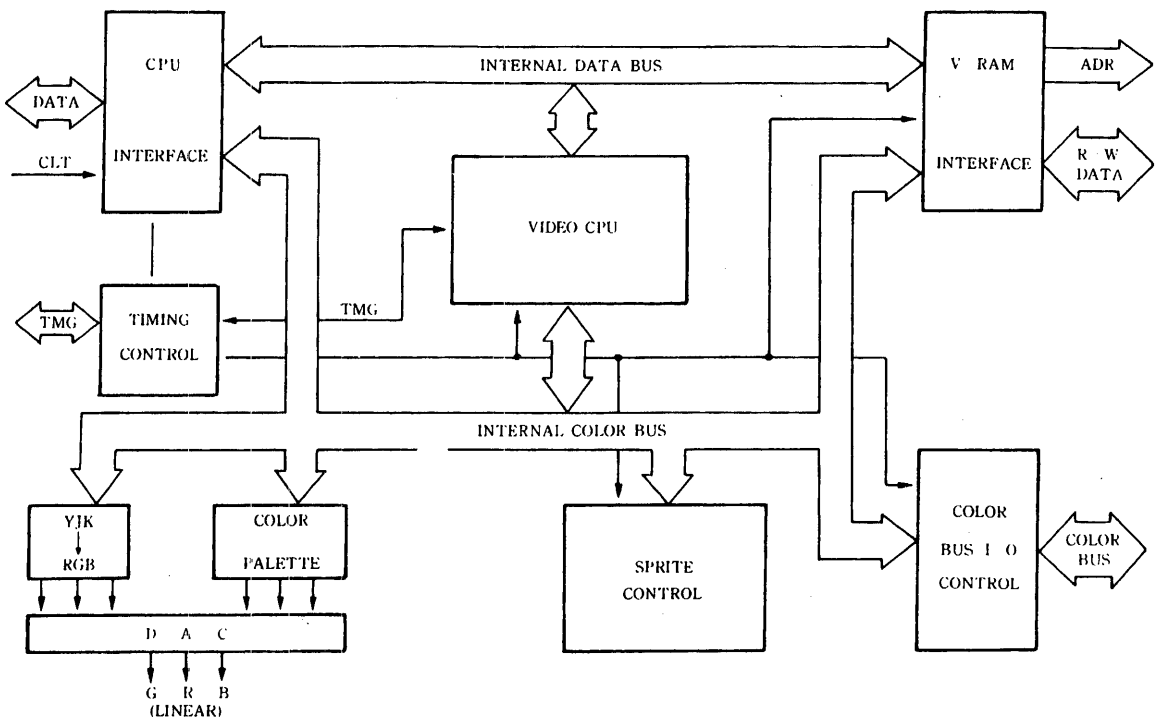


GRAPHICS

Enhanced Video Display Processor

V9938C E-VDP-I

■ OUTLINE

V9938(E-VDP-I)is a video display processor using an N-channel· silicon gate MOS and a 64-pin shrink DIL plastic package. TMS9918A is software compatible.

■ FEATURES

- Linear RGB and composite video output
- Built-in palette for displays in up to 512 colors.
- Maximum of 512 x 424 pixels and 16 colors.
- Bit mapped graphics
- A maximum of 256 colors can be displayed at the same time.
- 16 k-byte ~ 128 k-byte display memory
- 16K x 1b, 16K x 4b, 64K x 1b, 64K x 4b DRAMs can be used.
- 256 address, 4ms DRAM auto refresh.
- Expansion video memory can be connected.
- Built-in mouse and light pen interfaces.
- Eight sprites can be displayed for each horizontal line.
- Colors for sprites can be specified for each horizontal line.
- Area move, line, search and other commands.
- Logical operation function.
- Addresses can be specified by coordinates.
- External sync is possible.
- Superimpose is possible.
- Digitize is possible.
- Multi E-VDP-I configurations are possible.
- Additional external color palettes using the Color-Bus output.
- 5V power supply

■ ELECTRICAL CHARACTERISTICS

1. Maximum Ratings

Symbol	Item	Rating	Unit
Vcc	Power supply voltage	−0.5 ~ +7.0	V
Vin	Input voltage	−0.5 ~ +7.0	V
Ts	Storage temperature	−50 ~ +125	°C
To	Operating temperature	0 ~ +70	°C

2. Recommended Operating Conditions

Symbol	Item	Minimum	Typical	Maximum	Unit
Vcc	Power supply voltage	4.75	5.00	5.25	V
Vss	Power supply voltage		0		V
TA	Operating ambient temperature	0		70	°C
VIL 1	Low level input voltage (group 1)	−0.3		0.8	V
VIL 2	Low level input voltage (group 2)	−0.3		0.8	V
VIL 3	External clock low level input voltage (group 3)	−0.3		0.8	V
VIH 1	High level input voltage (group 1)	2.2		Vcc	V
VIH 2	High level input voltage (group 2)	2.2		Vcc	V
VIH 3	External clock high level input voltage (group 3)	3.5		Vcc	V

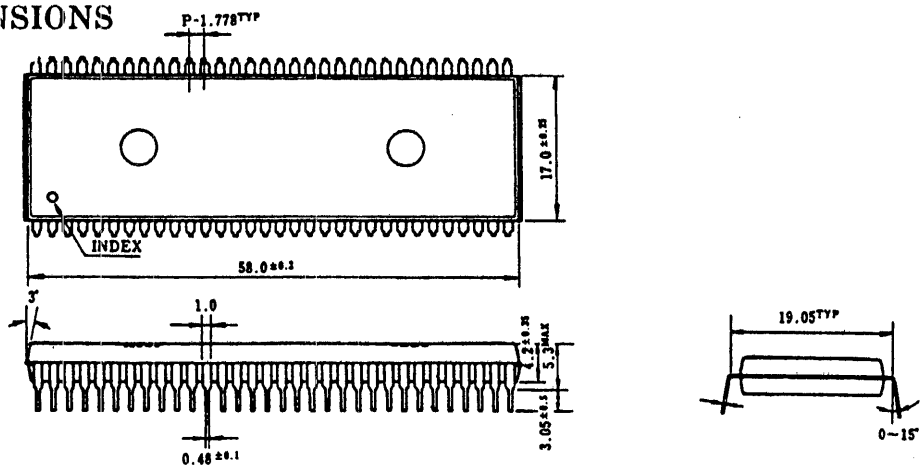
Note: Group 1 $\overline{CSR}$, RDO-7, CO-7, $\overline{LPS}$, $\overline{LPD}$, $\overline{RESET}$, $\overline{DLCLK}$
Group 2 CDO-7, MODE 0, MODE 1, $\overline{CSW}$
Group 3 XTAL 1, XTAL 2

3. AC Characteristics

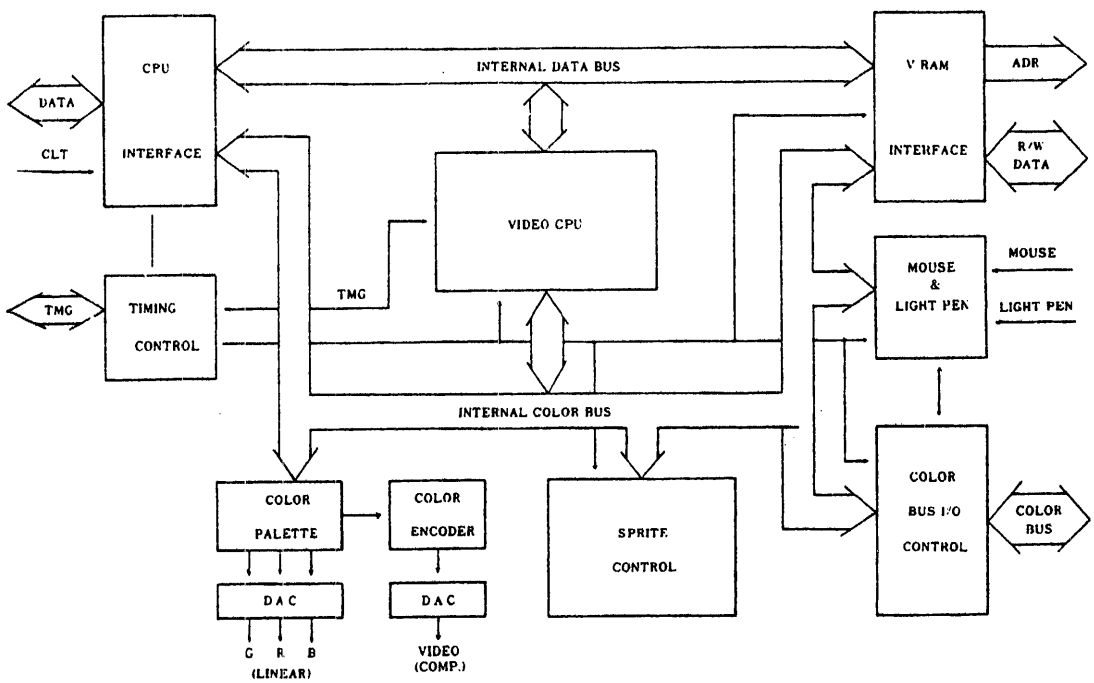
Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VOL 4	Low level output voltage (group 4)	IOL = 1.6mA			0.4	V
VOL 5	Low level output voltage (group 5)	IOL = 1.6mA			0.4	V
VOL 6	Low level output voltage (group 6)	IOL = 10mA			0.4	V
VOL 7	Low level output voltage (group 7)	IOL = 1.6mA			0.4	V
VOH 4	High level output voltage (group 4)	IOH = 100μA	2.4			V
VOH 5	High level output voltage (group 5)	IOH = 60μA	2.7			V
ILI	In-put leak current				10	μA
ILO	Output leak current (when floating)				25	μA
Icc	Current consumption				230	mA

Note: Group 4 CDO-7, RDO-7, ADO-7, $\overline{VDS}$, CBDR, CPUCLK, CO-7
Group 5 $\overline{RAS}$, $\overline{CAS\ 0}$, $\overline{CAS\ 1}$, $\overline{CASX}$, R/$\overline{W}$
Group 6 $\overline{DLCLK}$, $\overline{DHCLK}$
Group 7 $\overline{INT}$

■ OUTLINE DIMENSIONS



■ BLOCK DIAGRAM



COMMUNICATION

Facsimile Controller LSI

PRELIMINARY

YTF405 FAXC

■ OUTLINE

YTF405 is a fax controller LSI that integrates on a single chip, the controls for all of the major components that comprise a standard Group 3 (GIII) fax machine, including modem, image sensor, thermal printer and feeder motors.
The YTF405 supports the Group 3's standard T.4 control functions for image scanning and print-out, data compression, and T.30 standard binary protocols.
Also, with its built-in modem interface, when used in set with Yamaha's MD96FX Modem LSI (YM7109C), the YTF405 Fax LSI provides complete support for CCITT V.29, V.27ter, and V.21ch2 standard data communications.

The YTF405 Fax LSI packs in all necessary commands, protocols and interfaces on one chip, allowing for the design of more efficient and compact fax machines.

■ FEATURES

- Modem Interface
  Connects directly via parallel bus with the YM7109C Modem LSI, and features command functions for CCITT Recommendations V.29, V.27ter, and V.21ch2 communcations.
- Group 3 Fax Data Transmission Protocols
  CCITT T.30 binary protocols (Phase B, C, D) built-in, freeing the host processor from protocol handling tasks.
- Data Compression
  Data compression/decompressions by Modified Huffman (MH) codification.
- B4 Size Transmissions
  Sends and receives fax transmissions in B4 document size. Automatic B4-to-A4 conversion for machines using smaller width A4 recording paper.
- Main Scan Density
  8 dots per mm.
- Sub Scan Density
  3.85 lines per mm, standard mode.
  7.7 lines per mm, fine mode.
- Minimum transmission Time Per Line 5/10/20/40 msec.
- Image Sensor Interface
  Built-in circuitry for handling binary image data inputs and timing various sensor unit control. Supports both contact and CCD sensors.
- Printer Thermal Head Interface
  Built-in circuitry for handling printout data and for controlling the printer unit's thermal head.
- Feeder Motors Interface
  Generates commands for document feeder and printer motor drives.
- External Memory Interface
  Supports up to 8Mbits capacity external memory. This allows for additional memory needed for multiple-destination transmissions, and for plural page data send and data receive buffers.
- Host CPU Interface
  Connects to either 4-bit or 8-bit host processor.
- Built-in Crystal Pulse Generator
  Generates system clock pulses for modem.
- 5V single power supply. Low power consumption (CMOS).
- 100-pin QFP package.

The specifications of this product are subject to improvement changes without prior notice.

■ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(V_{SS}=0.0V)

ITEM	SYMBOL	Min.	Max.	UNIT
Supply voltage	V_{DD}	−0.3	7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.3	V
Output voltage	V_O	−0.2	V_{DD}+0.3	V
Ambient operating temperature	T_{OP}	0	70	℃
Storage temperature	T_{STG}	−50	125	℃

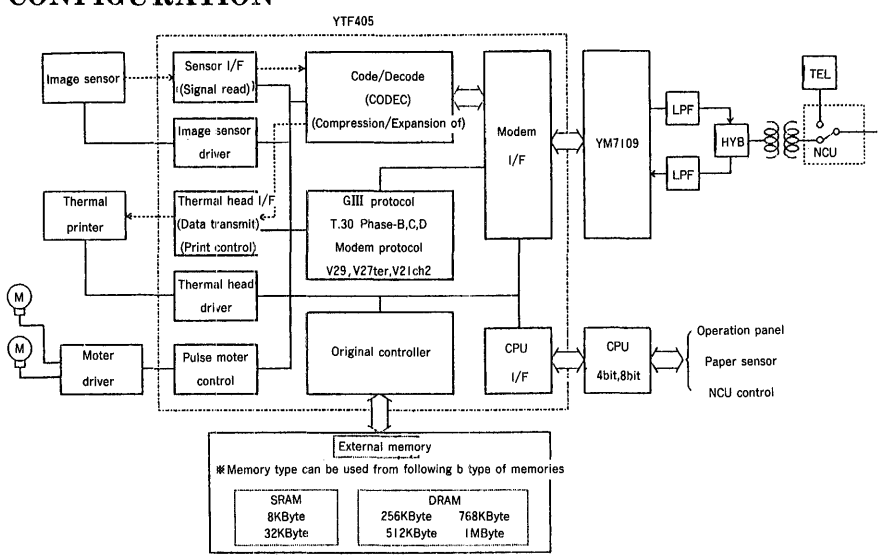
Recommended Operating Conditions(V_{SS}=0.0V)

ITEM	SYMBOL	Min.	Typ.	Max.	UNIT
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Ambient operating temperature	T_{OP}	0	25	70	℃

DC Characteristics(Given under the recommended operating conditions)

ITEM	SYMBOL	CONDITIONS	Minx.	Max.	UNIT
High-level output voltage	V_{OH}	I_{OH}=−80μA	2.4		V
Low-level output voltage	V_{OL}	I_{OL}=1.6mA		0.4	V
Low-level input voltage	V_{IL}			0.8	V
High-level input voltage	V_{IH}		2.0		V
Input leak current	I_L		−10	10	μA
Supply current	I_{DD}				mA

■ SYSTEM CONFIGURATION



COMMUNICATION

9600 bps FAX MODEM LSI with HDLC

YTM401 MD96DX

■ OUTLINE

MD96DX is a one-chip MODEM LSI of 9600 bps, which is upper compatible with our FAX MODEM-LSI MD96FX (YM7109) in pin arrangement and software. It is also provided with HDLC function, power saving functions, simple UART and external clock synchronization function.
MD96DX can execute HDLC function on hardware for any half-duplex communications mode, realizing high speed data transmission without transmission errors. This is the most suitable modem for G3 facsimile machines using ECM (error correction mode).
Incorporation of a simple UART enables non-synchronous full-duplex communications with a simple external circuit.
MD96DX has hardware power saving mode with an external terminals and software power saving mode with register control. Thus, in addition to reduced power consumption during operation (300 mW at max.), considerable power saving is enabled even when MD96DX is not in use. This makes the product suitable for use in portable machines.
MD96DX is packaged as 40-pin DIP, 64-pin QFP and 68-pin PLCC, and operated by +5V power supply to provide you a great advantage in board design.

■ FEATURES

- Upper compatible with YM7109 (our FAX MODEM) in software and terminal arrangement
- CCITT V.29 (9600/7200 bps) – Half-duplex, synchronous
  V.27ter (4800/2400 bps) – Half-duplex, synchronous
  V.21ch2 (300 bps) – Half-duplex, synchronous
  V.23 backward ch (75 bps) – Transmission only
  V.21 (300 bps) – Full-duplex
- BELL 103 (300 bps) – Full-duplex
- Full-duplex communication of V. 27ter reception and V. 23 (75 bps) transmission is available in CAPTAIN mode.

◎ Incorporated HDLC framing function enables use of ECM mode on G3 facsimile

- Compatible with public switched telephone network (two-wire)
- Dual-tone generation (programmable)
- Tone detection (programmable)
- DTMF detection (programmable)
- V.21 ch2 flag pattern detection
- Transmission level: 0 to – 15 dBm (programmable)
- Reception dynamic range: 0 to – 43 dBm (programmable)
- Automatic equalization and subscriber cable equalization
- Bandpass filter, A/D converter, D/A converter, and automatic gain control (AGC) incorporated for transmission and reception
- Parallel and serial interfaces

◎ The serial interface can be used as general purpose input/output terminal when it is not in use.

◎ External clock synchronization function

◎ Incorporated simple UART for start/stop mode (300 bps full duplex)

- 40-pin DIP, 64-pin QFP, or 68-pin PLCC package
- Low power consumption due to CMOS
- Single 5 V power supply

◎ Power saving mode with external terminal and interface register (When power saving applied: 5 μA)
New features of MD96DX is marked with ◎

■ ELECTRICAL CHARACTERISTICS

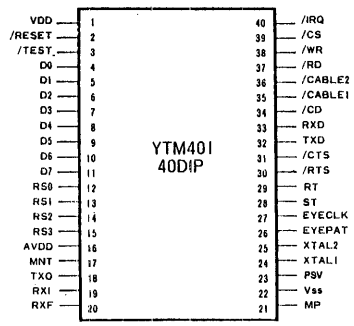
1. Maximum Ratings (VSS shall be 0V)

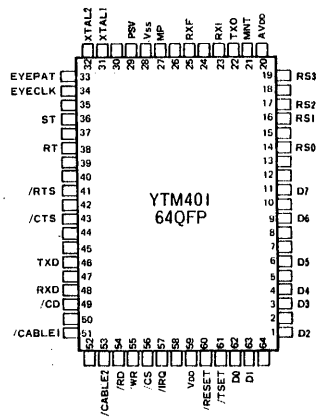
ITEM	SYMBOL	RATING		UNIT
		Min.	Max.	
Supply voltage	VDD	−0.5	7.0	V
Input voltage	VI	−0.5	VDD + 0.5	V
Output voltage	VO	−0.5	VDD + 0.5	V
Storage temperature	TSTG	−50	+125	°C

2. Recommended Operating Conditions (VSS shall be 0V)

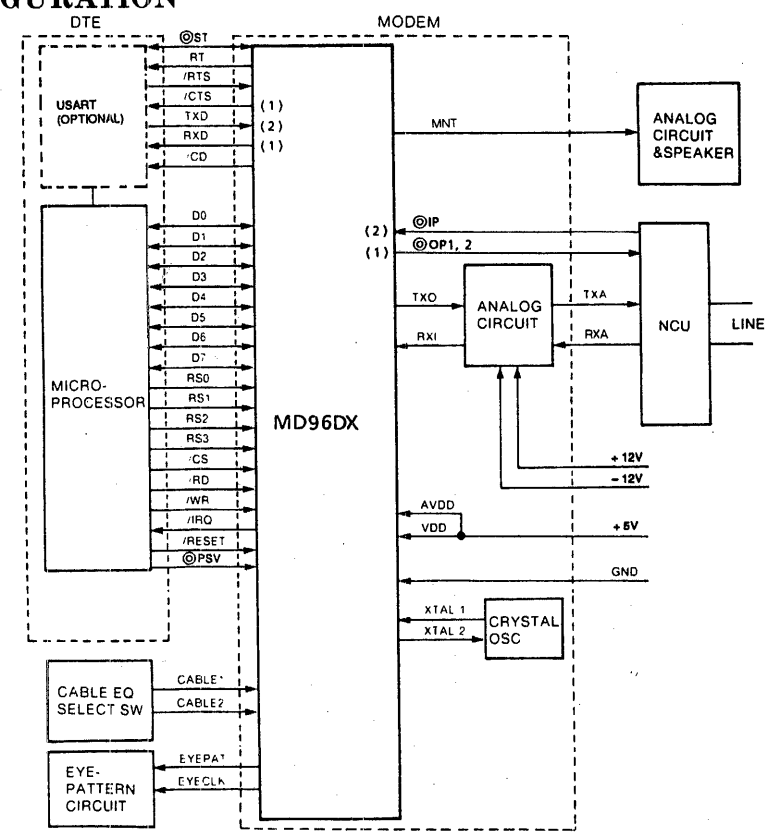
ITEM	SYMBOL	RATING			UNIT
		Min.	Typ.	Max.	
Supply voltage	VDD	4.75	5.0	5.25	V
Ambient operating temperature	Ta	0	25	70	°C
Clock frequency	fCLK	9.82942	9.83040	9.83138	MHz

■ PIN ASSIGNMENT





■ SYSTEM CONFIGURATION



Note) (1) becomes OP1 and OP2 in parallel mode and/CTS, RXD in serial mode.
(2) becomes IP in parallel mode and TXD in serial mode.
◎ Shows the pine added to or changed for MD96DX.

COMMUNICATION

9600bps FAX MODEM

YM7109C MD96FX

■ OUTLINE

The YM7109C LSI is a one-chip modem for half-duplex synchronous data transfer at 9600 bps, 7200 bps, 4800 bps, 2400 bps, and 300 bps (CCITT V.29, V.27ter, V.21 ch2). With its built-in programmable dual tone originating function and programmable tone detection function, this LSI is designed for use with a public telephone line network and is ideal for modem applications for G3 facsimile machines.

In addition,the YM7109C is equipped with function for modulation into full duplex (CCITT V.21 and BELL 103) and a 75 bps (CCITT V.23 Backward channel) transmission function. It can thus also be used as the modem for telecommunications by personal computer or as a CAPTAIN adapter.

The YM7109C also has a built-in interface register which can connect to the data bus of a microprocessor, allowing reading and writing to and from that data bus. By accessing this interface register via a parallel interface, you can set the operating mode, set various parameters, read status flags, transfer the data to be transmitted or received, operate the modem and so on. The transfer of the transmit and receive data as well as modem operation can also be performed via a serial interface. The YM7109C is fabricated in a 40 pin dip unit. Because of its low power consumption thanks to CMOS, the full capability of the LSI can be facilitated with 5V battery power supply, allowing much space to work with in terms of designing. This is a great plus for portability.

■ FEATURES

- CCITT V.29 (9600 bps/7200 bps) Half duplex, synchronous
  V.27ter (4800 bps/2400 bps) Half duplex, synchronous
  V.21 ch 2 (300 bps) Half duplex, synchronous
  V.23 Backward Channel (75 bps) Transmission only
  V.21 (300 bps) Full duplex
- BELL 103 (300 bps) Full duplex
- In CAPTAIN mode, full-duplex reception using V.27ter and full-duplex transmission using V.23 (75 bps) is possible.
- Compatible with the public phone line network (two-wire system)
- Dual tone originating function (programmable)
- Tone detection function (programmable)
- DTMF detection function (fixed)
- Function for detecting flag patterns of V.21 ch2
- Transmission level: 0 dBm to −15 dBm (programmable)
- Reception dynamic level: 0 dBm to −43 dBm (programmable)
- Auto equalizer function, and subscriber cable equalizer function
- Built-in bandpass filter for transmission and reception, A/D converter, D/A converter, and AGC (Automatic Gain Control)
- Parallel interface and serial (CCITT V.24) interface
- 40-pin DIP, 64-pin QFP, 68-pin PLCC package
- Low power consumption due to CMOS use (Typ. 200mw, Max. 300mw)
- 5V single power supply

■ ELECTRICAL CHARACTERISTICS

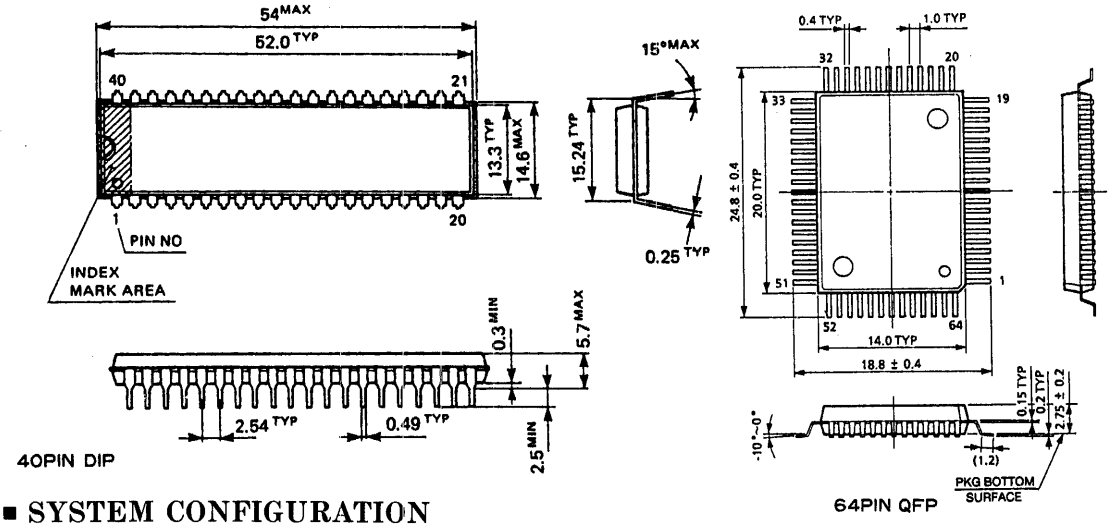
1. Maximum Ratings (VSS shall be 0V)

ITEM	SYMBOL	RATING		UNIT
		Min.	Max.	
Supply voltage	V_{DD}	−0.5	7.0	V
Input voltage	V_I	−0.5	V_{DD} + 0.5	V
Output voltage	V_O	−0.5	V_{DD} + 0.5	V
Storage temperature	T_{STG}	−50	+125	°C

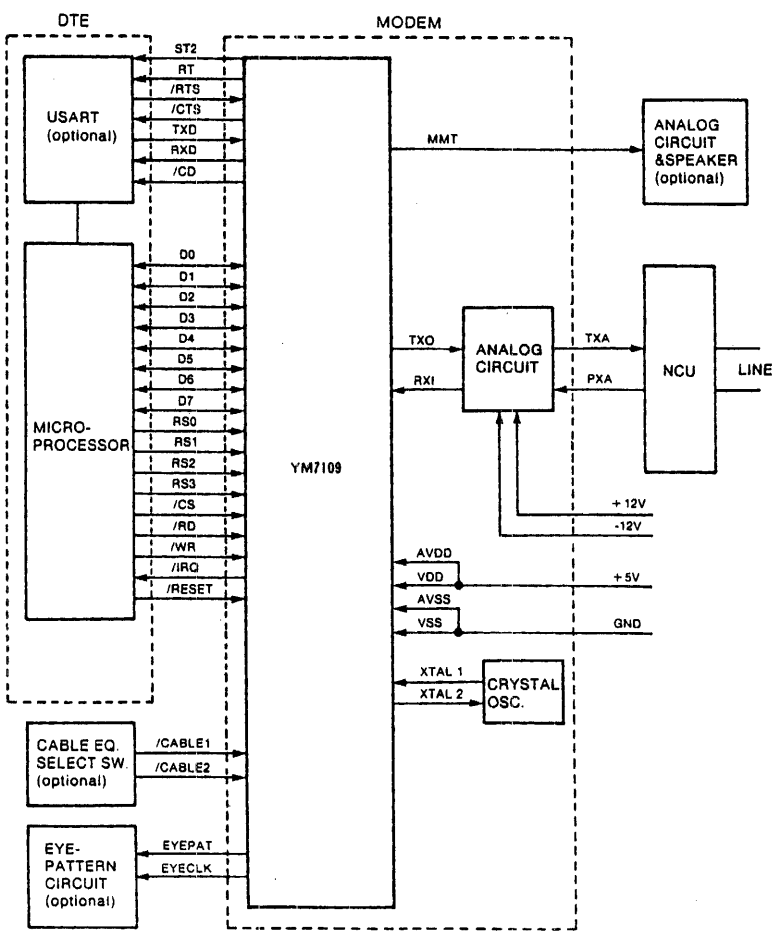
2. Recommended Operating Conditions (VSS shall be 0V)

ITEM	SYMBOL	RATING			UNIT
		Min.	Typ.	Max.	
Supply voltage	VDD	4.75	5.0	5.25	V
Ambient operating temperature	Ta	0	25	70	°C
Clock frequency	fCLK	9.82942	9.83040	9.83138	MHz

■ OUTLINE DIMENSIONS



■ SYSTEM CONFIGURATION



COMMUNICATION

MIDI(Musical Instrument digital Interface) Communication & Service Controller

YM3802 MCS

■ OUTLINE

The YM3802 is an LSI device featuring an asynchronous serial communication interface, a frequency divider that acts a communication rate generator, an interface for the cassette tape recorder, transmit/receive data buffers, timers, counters and a parallel input/output port. With this LSI a part of the MIDI data processing can be performed by hardware.

The YM3802 LSI has two output pins and three counters that synchronize with the MIDI clock and the tape SYNC can be easily realized. The MIDI clock is generated by the MIDI clock timer, the tape SYNC signal or the clock message which is contained in the received serial data. Another way of the generation of the MIDI clock is a process with the host CPU control. This LSI has the priority transmission and reception capability of the MIDI system real-time message over other messages and also can support the processing of the system exclusive message.

Each of the MIDI counters can be utilized as general-purpose timer/counter.

■ FEATURES

- Serial communication
  7- or 8-bits ..... Character
  1- or 4-bits ..... Parity bit,
  1- or 2-bits ..... Stop bit,
  Start bit error detection,
  Automatic break detection and break character generation,
  Character length, Types of parity and stop bits and communication rate are selectable for transmission and reception separately.
- MIDI support functions
  SYNC out, CLOCK out; output of a pulse signal synchronized to the system real-time message.
  Automatic transmitting function, priority transmitting function and priority receiving function (without involving the receiving FIFO buffer) of the system real-time message.
- 8- and 15-bit counters for counting the interpolated, high-accuracy signal of the MIDI clock.
- Special 14-bit timer for determining MIDI clock generation timing. Detecting function of the MIDI clock from the received serial data.
- Tape SYNC function.
- Automatic output of the tape SYNC signal
- Active sense function
- ID code check function for the system exclusive message.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

ITEM	SYMBOL	RATING	UNITS
Supply voltage	V_{DD}	−0.3 ~ +7.0	V
Input voltage	V_I	−0.3 ~ +0.5	V
Operating temperature	Top	0 ~ 70	°C
Storage temperature	Tstg	−50 ~ 125	°C

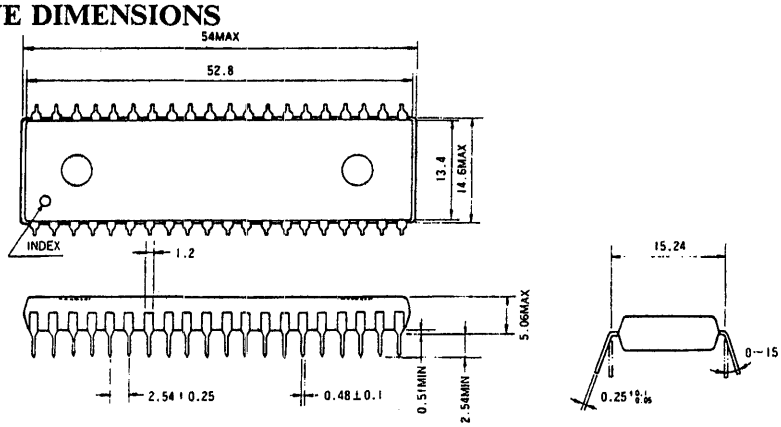
Recommended Operating Conditions (Ta = 0~70°C)

ITEM	SYMBOL	MIN.	TYP	MAX.	UNITS
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Top	0		70	°C

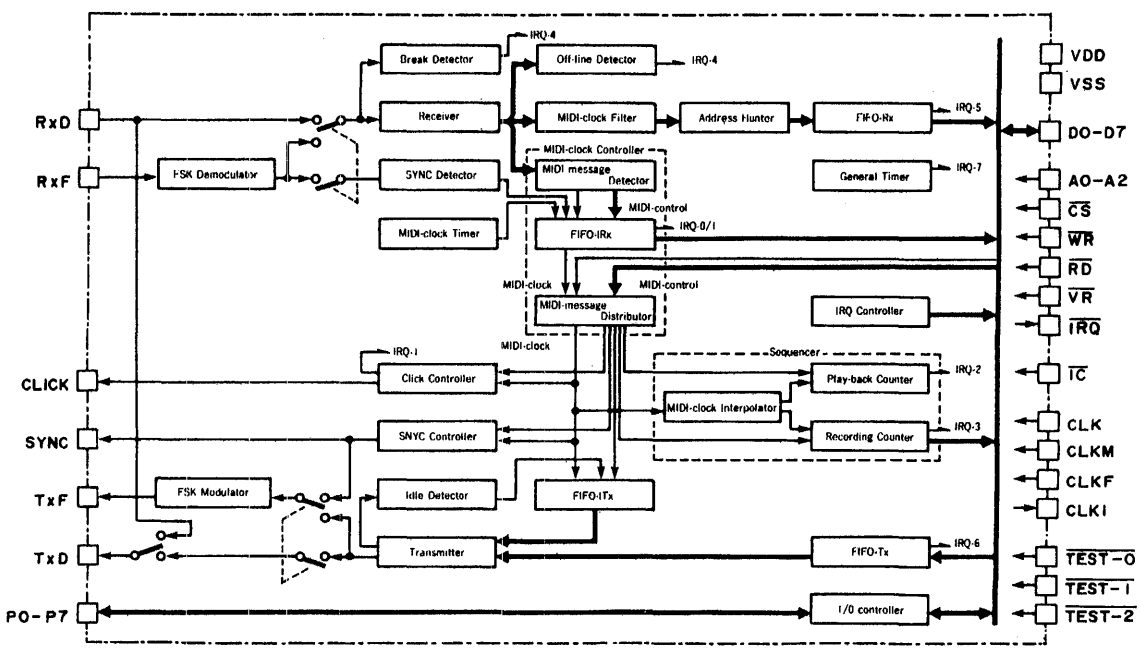
DC characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input low level voltage	V_{IL}		−0.3	—	0.8	V
Input high level voltage	V_{IH}		2.0	—	V_{DD}+0.5	V
Input leakage current	I_{LK}	V_I = 0~5V (Except for the pins with pull-up registers)	—	—	10	μA
Pull-up resister	Ru	($\overline{TEST0}$~$\overline{TEST2}$, $\overline{IC}$)	100	—	1000	KΩ
Output low level voltage	V_{OL}	I_{OL} = 2mA ($P0$~$P7$, $D0$~$D7$, $\overline{IRQ}$)	Vss	—	0.4	V
Output low level voltage	V_{OL}	I_{OL} = 1mA (Output terminals other than shown above)	Vss	—	0.4	V
Output high level voltage	I_{OL}	I_{OH} = −1mA (Except for $\overline{IRQ}$)	4.0	—	V_{DD}	V
Output leakage current	I_{OL}	V_O = 0 ~ 5V	—	—	10	μA
Power supply current	I_{DD}	V_{DD} = 5V	—	6	10	mA
Input capacitance	C_I	f = 1MHz			10	pF
Output load capacitance	C_{L1}	$P0$~$P7$, $D0$~$D7$, $\overline{IRQ}$			100	pF
	C_{L2}	Output terminals other than shown above			50	pF

■ OUTLINE DIMENSIONS



■ BLOCK DIAGRAM



SOUND SIGNAL PROCESSOR

Karaoke Processor

YSS205-F KP

■ OUTLINE

The YSS205 is an LSI chip used to carry out digital signal processing of "karaoke" systems. Using a 256K pseudo-SRAM, this LSI chip executes signal processing such as Key Control, Digital Echo, and Voice Cancel. Integrated A/D, D/A converters make it possible to handle input and output of either digital or analog audio signals. The same hardware can make use of the Digital Surround function with all types of video and music software.

■ FEATURES

- Both a 3-channel, 15 bit floating A/D converter and a 2-channel, 15 bit floating D/A converter have been integrated to handle audio signals from the L and R channels and from the microphone.
- Digital signals from CD and LD sound processing LSI chips can be input directly, and it is possible to output digital signals to oversampling digital filters and DACs.
- 4 operating modes to carry out various processing operations
- A maximum of 370ms of digital data can be stored (fs=44.1 KHz, when connected to one pseudo-SRAM) and then divided for use into Key Control, Echo, and Surround.
- A Key Control function with a maximum variable range of ± 1 octave
- A high-quality Digital Echo made possible by incorporating multiple taps
- All parameters may be set with a microprocessor serial interface.
- Up to two 256K (8 bits x 32K) pseudo-SRAM can be connected for external memory.
- Selection of either 256fs or 384fs for the master clock
- +5V power supply, silicon-gate CMOS, 64 pin QFP plastic package

■ ELECTRICAL CHARACTERISTICS

1 Absolute maximum ratings

Item	Symbol	Rated Value	Unit
Power supply voltage	VDD	–0.3~+7.0	V
Input voltage	V_I	–0.3~V_{DD}+0.5	V
Operating ambient temperature	Top	0~+70	C°
Storage temperature	Tstg	–50~+125	C°

2 Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating ambient temperature	Top	0	25	70	C°

3 DC characteristics (Conditions: Ta = 0~70° C, V_{DD} = 4.75~5.25V)

Item	Symbol	Condition	Min.	Typical	Max.	Unit
Power consumption	W	V_{DD}=5.0V			300	mW
High level input voltage (1)	V_{IL1}		2.0			V *1
Low level input voltage (1)	V_{IL1}				0.8	V *1
High level input voltage (2)	V_{IL2}		3.5			V *2
Low level input voltage (2)	V_{IL2}				0.8	V *2
High level output voltage	V_{OH}	I_{OH}=0.4mA	V_{DD}-1.0			V
Low level output voltage	V_{OL}	I_{OL}=1.6mA			0.4	V
Input leak current	I_{IL}				10	µA
Input capacitance	C_I				10	pF
Output capacitance	C_O				10	pF

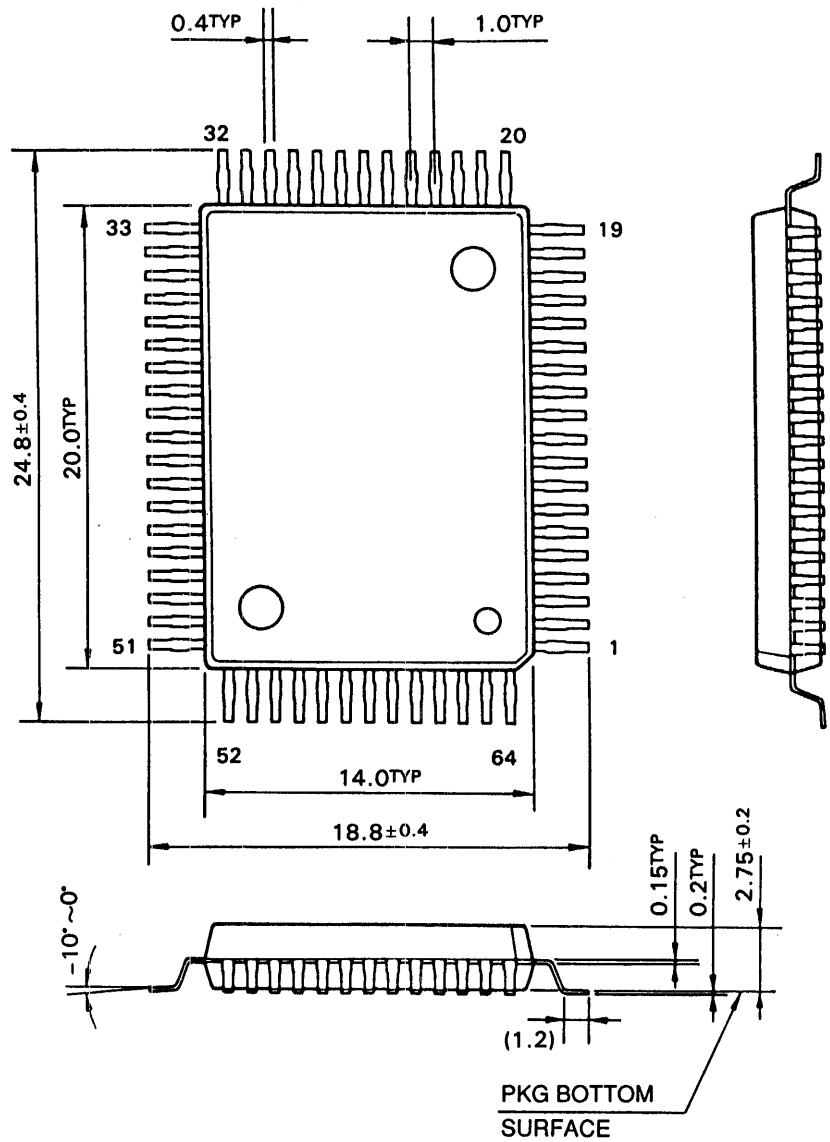
Note 1: Any input terminal except XI, /IC
Note 2: XI, /IC terminal

4 AC characteristics (Conditions: Ta = 0~70° C, V_{DD} = 4.75~ 5.25V)

Item		Symbol	Min.	Typical	Max.	Unit
XI	input frequency	fc	12	16.9344	19	MHz
			8	11.2896	13	*3
XI	duty			50		%
BCI	input frequency	f_{BCI}	1		4.3	MHz

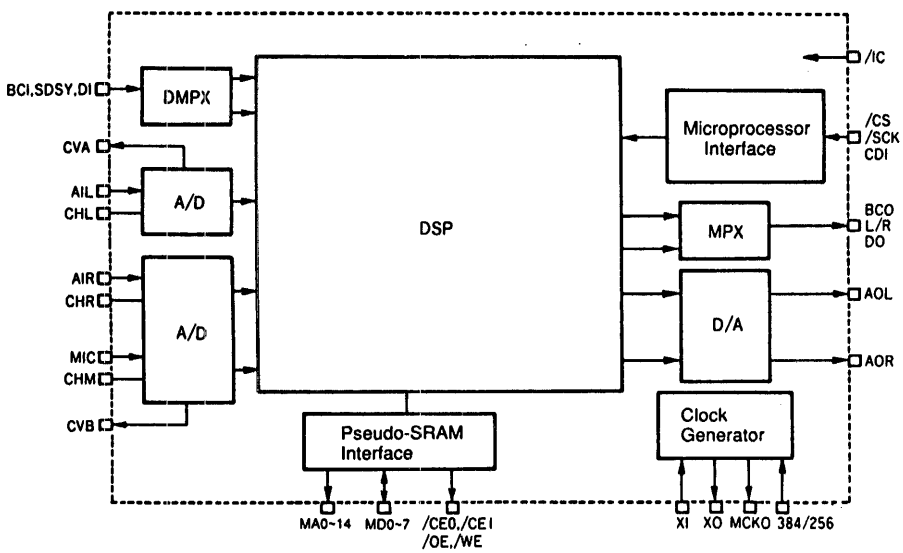
Note 3: The upper is 384fs and the lower is 256fs

■ EXTERNAL DIMENSIONS (YSS205-F)



DIMENSIONS IN mm

■ BLOCK DIAGRAM



SOUND SIGNAL PROCESSOR

Dolby Pro-Logic Decoder

YM7306B DPLD

■ OUTLINE

This LSI is a Dolby Pro Logic decoder based on latest Digital Signal Processing technology. The LSI is capable of digital signal processing for almost all functions needed in Pro Logic. This allows construction of a highly reliable decoder with a small quantity of components.
This LSI also has a sound field simulation circuit with 12 digital delay lines (370 ms at max.), which allows you to design a 2in-4out surround system easily.

■ FEATURES

- Highly accurate signal processing with internal operation word length of 32 bits
- Adaptive matrix, noise sequencer, 7 KHz low pass filter, modified B-type N.R. decoder and A/D & D/A converter are built-in.
- Sound field simulation function using digital delay (maximum delay time: 370 ms)
- External 256K DRAM interface for 16 bits linear digital delay (page mode access)
- Serial interface with microprocessor for parameter control.
- Analog signal processing for the front three channels.
- Master clock frequency is 8.46 MHz and sampling frequency is 44.1 KHz.
- Interface signal output for Automatic Balance Control.
- Dolby reference operate level 300 mVr.m.s.
- 64 pin QFP package, silicon gate CMOS, 5V power supply.

(Note)

Dolby is a trademark of Dolby Laboratories Licensing Corporation. This IC is available only to licensses of Dolby Laboratories Licensing Corporation.

■ ELECTRICAL CHARACTERISTICS

• ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_I	−0.3	VDD +0.5	V
Input current	I_I		10	mA
Operating temperature	Top	−20	+75	°C
Storage temperature	Tstg	−50	+125	°C

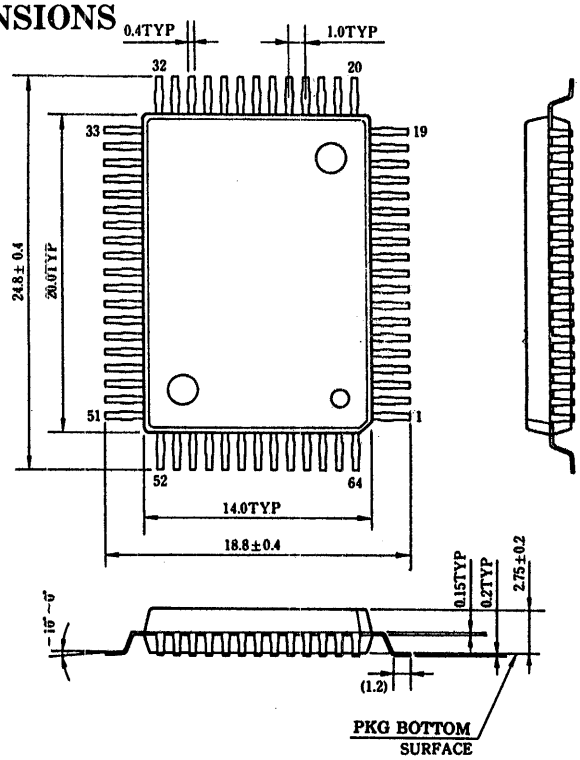
• RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	Top	0	25	70	°C

• ELECTRICAL CHARACTERISTICS (CONDITIONS : Ta=25°C, V_{DD}=5.0±0.25V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	W	V_{DD}=5.0V		200	300	mW
Input Voltage H level	V_{IH}					V
TTL level			2.7		V_{DD}	
CMOS level			3.5		V_{DD}	
Input Voltage L level	V_{IL}					V
TTL level			0		0.4	
COMS level			0		1.0	
Input leakage current	I_{IL}				10	μA
Output voltage L level	V_{OL}	I_{OH}=−2mA	0		0.4	V
Output voltage H level	V_{OH}	I_{OH}=200μA	3.0		V_{DD}	V
XI frequency	X_{IN}		8.0	8.46	9.0	MHz
XI clock duty			40	50	60	%
BCI frequency					2.0	MHz

■ EXTERNAL DIMENSIONS



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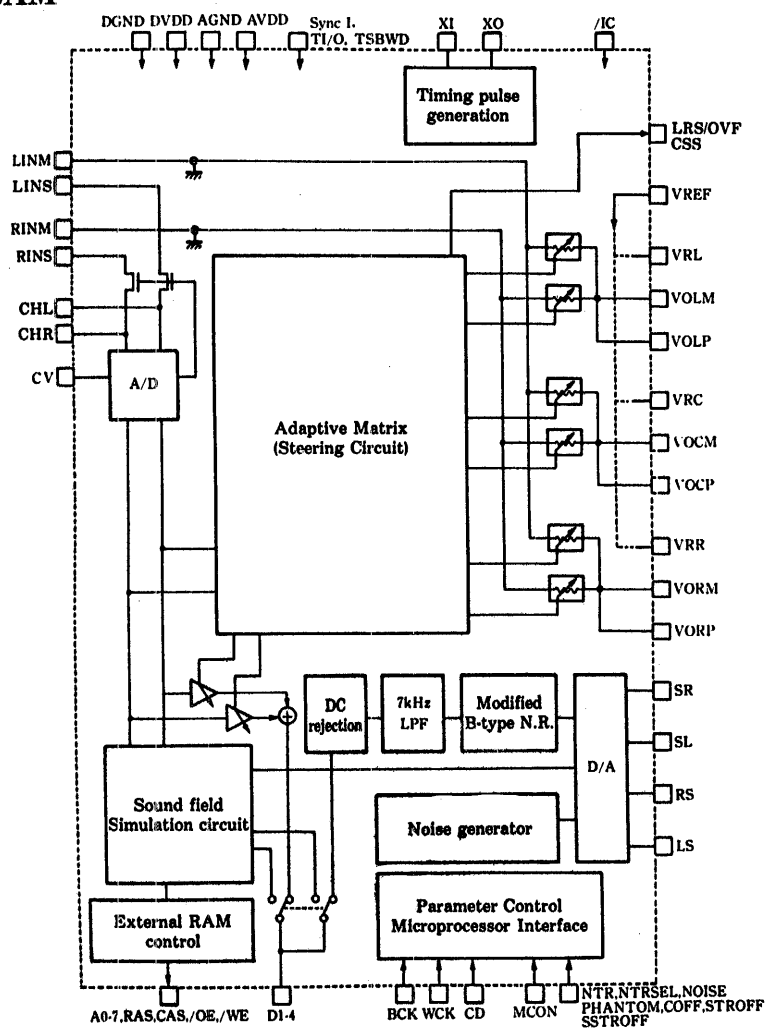


SOUND SIGNAL PROCESSOR

Surround Processor 2

YM7128 SP-2

■OUTLINE

YM7128 is an LSI which has quality digital surround sound capabilities realized by Yamaha's digital audio technology.

The LSI has built-in A/D and D/A converters which enable digital surround sound processing for analog input/output without using any additional devices. Its eight digital delay lines may provide delay time of up to 100 msec. for each, and digital adding up of delay line signals for two-channel output assures a wide range of application.

■FEATURES

- The built-in RAM realizes digital delay time of 100 msec*, at the maximum.
- Feedback loop can be constructed for reverberation.
- Various surround effect can be obtained by controlling this processor with serial data from microprocessors.
- Digital attenuator is built in for surround sound volume control.
- Sampling frequency is 23.6 kHz*, and 14 bit floating A/D converter is built in.
- Two-times oversampling digital filter and 14 bit floating D/A converter are built in.
- 16 pin DIP packaged silicone gate CMOS LSI, operated by 5V.

NOTE: When XI clock frequency is 7.16 MHz (304 fs is required for XI clock)

■ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	VDD	−0.3 ~ +7.0	V
Operating temperature	Top	−20 ~ +85	℃
Storage temperature	Tstg	−50 ~ +125	℃

2. Recommended Operating Conditions (Ta=25℃, VDD=5.0V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD	4.75	5.0	5.25	V
Operating temperature	Top	0	25	70	℃

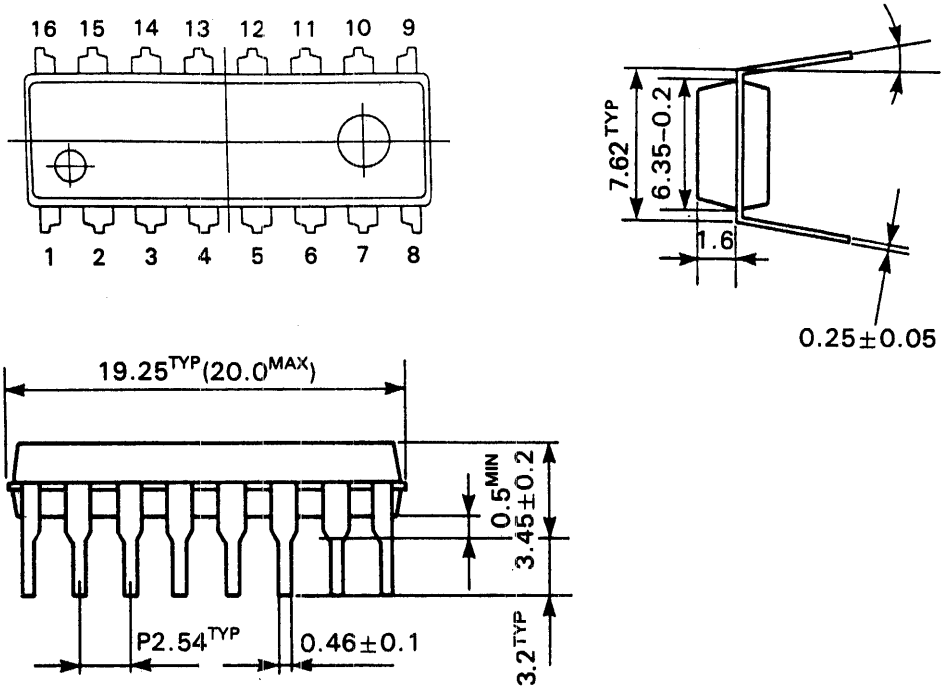
3. DC Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Current	IDD				50	mA
High-level input voltage (1)	VIH1		2.0			V ※1
Low-level input voltage (1)	VIL1				0.8	V ※1
High-level input voltage (2)	VIH2		4.0			V ※2
Low-level input voltage (2)	VIL2				0.8	V ※2
High-level output voltage	VOH	IOH=−0.4mA	4.0			V
Low-level output voltage	VOL	IOL=0.2mA			0.4	V
Input current leak	IIL	VI=0~5V	−10		10	μA
Input capacitance	CI			5.0	12.0	pF
Output eapacitance	CO				10.0	pF

※1: Applicable to input terminals except XI

※2: Applicable to XI terminal

■ OUTLINE DIMENSIONS



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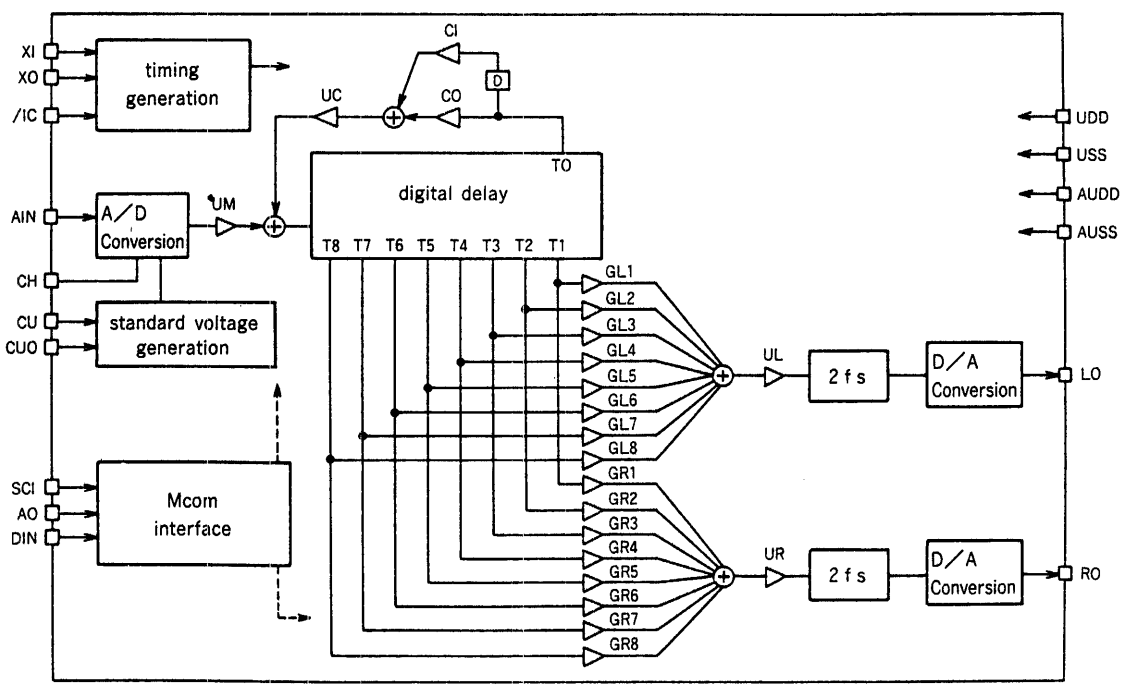


SOUND SIGNAL PROCESSOR

Surround Processor-B

YM3428 SP-B

■ OUTLINE

The YM3428, a 16-pin DIP CMOS LSI, permits to implement quality digital surround sound capabilities realized by Yamaha's digital audio technology.

As the LSI includes A/D and D/A converters, you can easily implement digital surround functions without any additional analog devices.

It has four delay lines each of which may be set for the maximum delay time of 30.24 msec, and outputs are two channels each of which is produced in each pair of delay channels added up digitally. So, the range of application is wide.

■ FEATURES

- Three kinds of surround mode are possible as preset modes without the use of any microprocessors.
- With a use ofmicroprocessor, it is possible to set the four delay lines at different delay times and different volumes and to define parameters of a primary IIR digital low-pass filter.
- The internal signal format is of 14-bit floating point numbers.
- The built-in A/D and D/A converters are of floating type with high linearity.
- The built-in reference voltage generator for A/D Converter permits an easy interface with analog circuits.
- The sampling frequency of A/D conversion is 24.9 kHz, so the bandwidth needed for surround sounds is secured.
- The D/A converter operates at the sampling frequency of 99.4 kHz, following a built-in quadruple oversampling digital filter, so that high cost external output low-pass filter is not needed.
- Distortion is as low as 0.22% (typical) at the maximum output at 1 kHz.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (VSS=0.0V)

Item	Symbol	Rating	Unit
Terminal voltage	VDD—VSS	−0.3~7.0	V
Operating temperature	TOP	0~70	°C
Storage temperature	Tstg	−50~125	°C

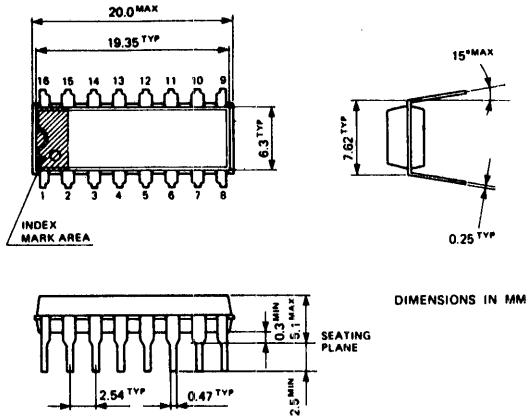
2. Recommended Operating Conditions (VSS=0.0V, TOP=0~70 ℃)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	VDD	4.75	5.00	5.25	V
	VSS, AGND	0	0	0	V

3. DC Characteristics(VDD=4.75~5.25V, TOP=0~70 °C)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low-level input voltage	VIL		−0.3		0.8	V
High-level input voltage	VIH	Except XI	2.0		VDD	V
High-level input voltage	VIH	XI	4.0		VDD	V
Low-level output voltage	VOL	XO : IOL=0.2 mA	−0.3		0.4	V
High-level output voltage	VOH	XO : IOH=0.4 mA	4.0			V
Input current leak	ILK	VI=5V			10	μA
Supply current	IDD			20.0	30.0	mA
Input capacitance	CI	f=1 MHz			10	pF
Output capacitance	CO				10	pF
Pullup resistance	RPU	/IC, MD0, MD1	50		400	KΩ

■ OUTLINE DIMENSIONS



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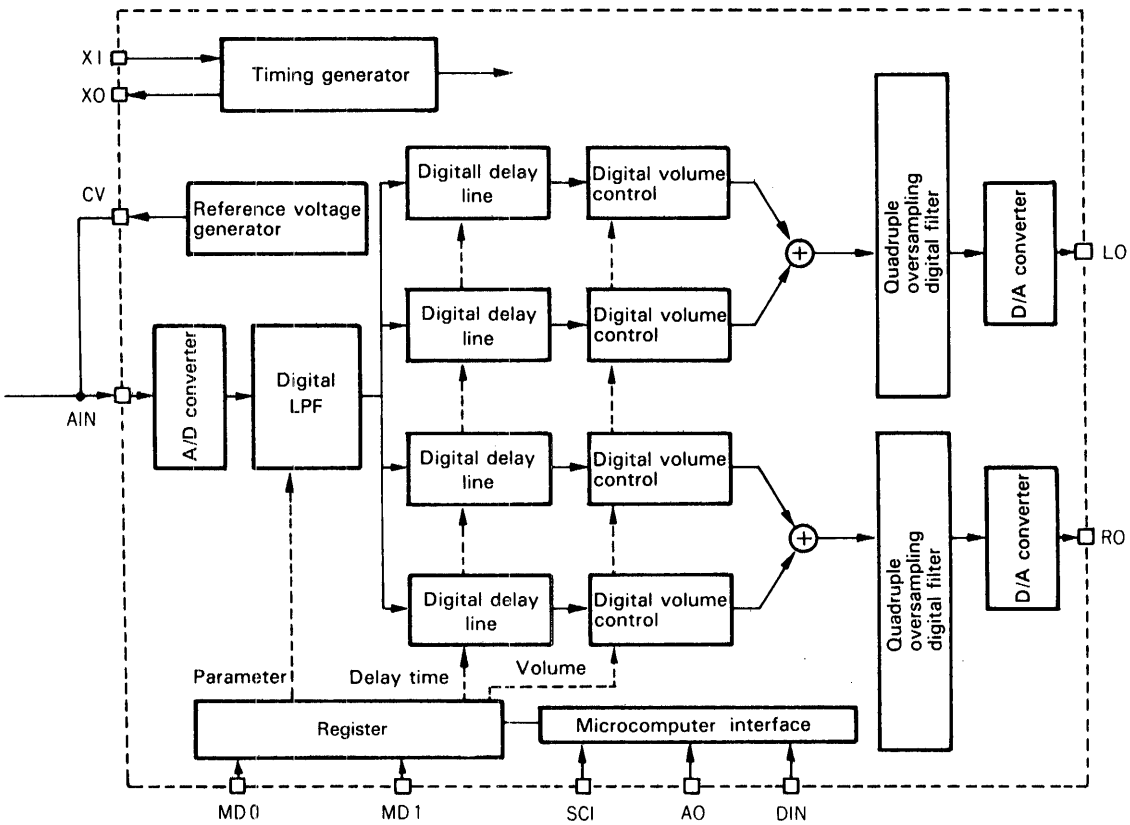


SOUND SIGNAL PROCESSOR

Digital Compressor

YM3412B COMP

■OUTLINE

Wide dynamic range is one of the most significant features of digital audio signals. However, this feature can be a disadvantage of the total system, when digital audio is used with analog system having limited dynamic range such as car CD, portable CD or headphone CD, or when recording CD to a cassette tape.

There is also a problem when part of a low volume signal is lost during attenuation of digital output or during digital volume processing.

The latest Yamaha digital sound processing technology has been used to create an LSI chip with a compressor function (which includes a volume processing option) that will automatically respond to the input level and compress the dynamic range of the digital audio signal.

■FEATURES

- An input signal emulation compressor based on digital sound processing technology. Automatic emulation of low or high volume input signals, based on a unique input signal level detection circuit.
- Capable to cope with MSB first 2's complementary input signals with fs at 32 KHz, 44.1 KHz, 48 KHz or double fs.
- Capability in 2 modes:

<Mode 1> (Compressor)

Four different compression ratios can be employed, determined by the setting of the compression switching terminals (SEL0,SEL1).

Compression ratios vary when detected input level is between −54dB and −18dB. Below −54dB, the input and output values are equal, and beyond −18dB, attenuation is carried out.

DCR (DCR is the dynamic compression ratio when the detected input level is between −54dB and −18dB.)

1. 1/1 Input and output levels are equal.
2. 3/4 When the detected input level is over −18dB, the reduced rate is fixed at −9dB.
3. 2/3 When the detected input level is over −18dB, the reduced rate is fixed at −12dB.
4. 1/2 When the detected input level is over −18dB, the reduced rate is fixed at −18dB.

<Mode 2> (Digital Attenuator with compressing)

When an external microprocessor is used to input volume data (8bit, attenuation at 0.375dB), attenuation of sound of volume is carried out while still maintaining the compressor function. (During initial clear, muting condition is set with the volume value "∞".)

- CMOS, 18 pin , plastic DIP, +5V power supply

■ELECTRICAL CHARACTERISTICS

(1) Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	−3.0	+7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.5	V
Ambient operating temperature	T_{OP}	0	+70	℃
Storage temperature	T_{STG}	−50	+125	℃

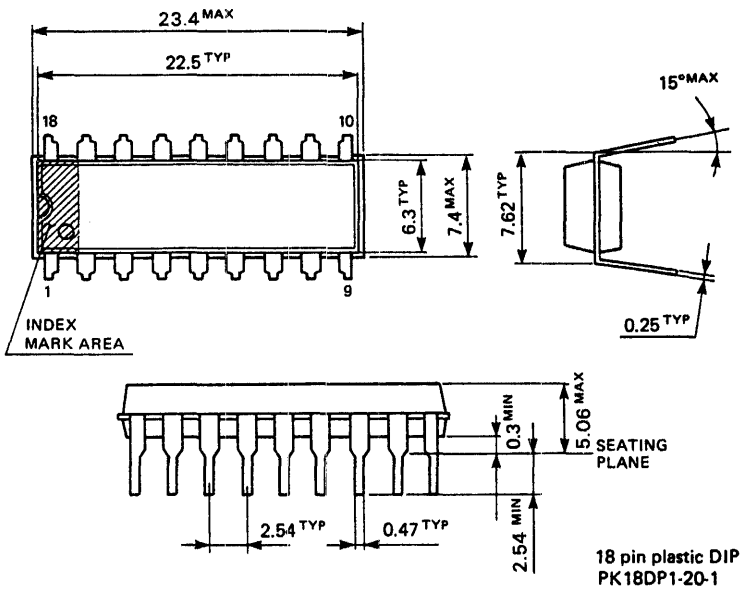
(2) Recommended Operating Conditions

Item	Sybol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Ambient operating temperature	T_{Op}	0	25	+70	℃

(3) DC Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	I_{DD}	$V_{DD}=5V$				mA
High output voltage	V_{OH}	$I_{OH}=20\mu A$	4.0			V
Low output voltage	V_{OL}	$I I_{OL}=1mA$			0.4	V
High input voltage 1	V_{IH1}		3.5			V
Low input voltage 1	V_{IL1}				1.5	V
High input voltage 2	V_{IH2}		2.0			V
Low input voltage 2	V_{IL2}				0.8	V
Input current leakage	I_{IL}		−10		10	mA

■ OUTLINE DIMENSIONS



18 pin plastic DIP
PK18DP1-20-1

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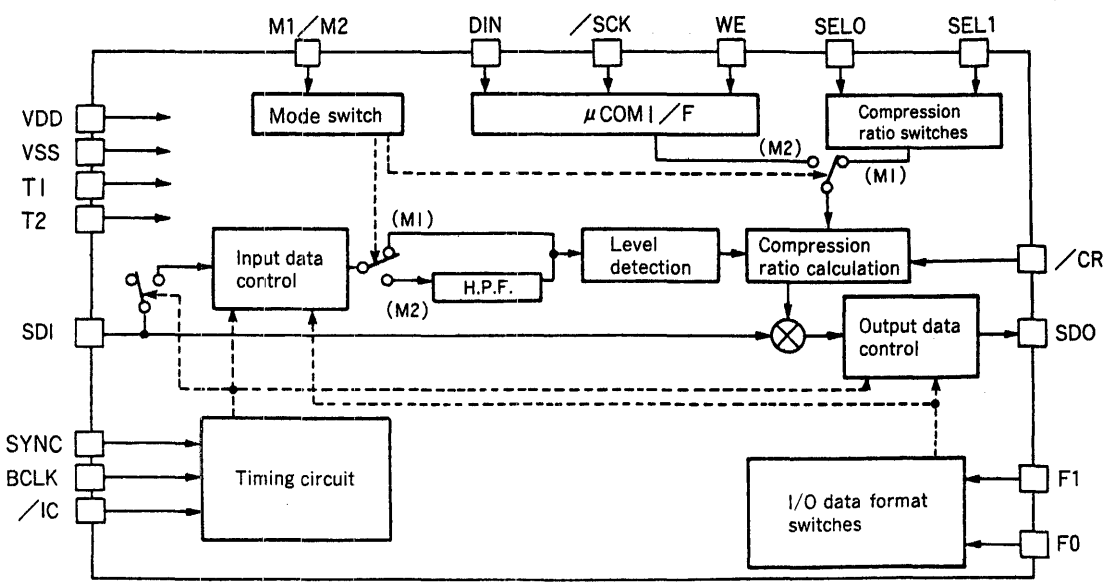


CD-I/CD-ROM

CD-I Data Controller

YM6063B CDC

■ OUTLINE

The CDC (CD-I Data Controller) is a data processor capable of handling data from both CD-I and CD-ROM sources.
This receives data read out from a CD-I disk and detects the synchronous pattern, then descrambles the data and puts it in a buffer. File and channel selection, and data distribution can be done through use of an 8 bit microcomputer.
It is also possible to create a compact CD-I system configuration by using this together with the YM6064 (ADP) and YM7302 (MPC).

■ FEATURES

- Capacity to handle either CD-I or CD-ROM.
- Real time errors can be detected and corrected by the hardware.
- Interface can be accomplished with any CD audio signal processing format, regardless of the maker--e.g. Yamaha, Sony, Sanyo, NEC, Mitsubishi, Toshiba, Hitachi, or Matsushita.
- CD-I ADPCM data can be transferred directly to the audio processor (ADP).
- When used with the YM7302 (MPC), data can be transferred at a rate of 1170 bytes/msec.
- An optimal system can be set up when connected with a 68000- type bus.
- CMOS, 5V power supply, 80 PIN QFP

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

		Min	Max	
Supply voltage	Vdd	−0.3	7.0	V
Power consumption	Pd		150	mW
Input voltage	Vin	−0.3	Vdd+0.5	V
Input current	Iin		10	mA
Ambient operating temperature	Top	0	70	°C
Storage temperature	Tstg	−50	125	°C

2. Recommended Operating Conditions

Supply voltage	Vdd	4.75	5.25	V
Ambient temperature	Top	0	70	°C

3. DC Characteristics

- Input terminals (Numbers shown in ( ) are CK, BCI, and RTCLK terminal coefficients.)

		Min	Max	
Low level input voltage	Vil	−0.3	0.8 (0.4)	V
High level input voltage	Vih	2.0 (2.4)	Vdd+0.5	V
Input leak current	Ili		10	μA

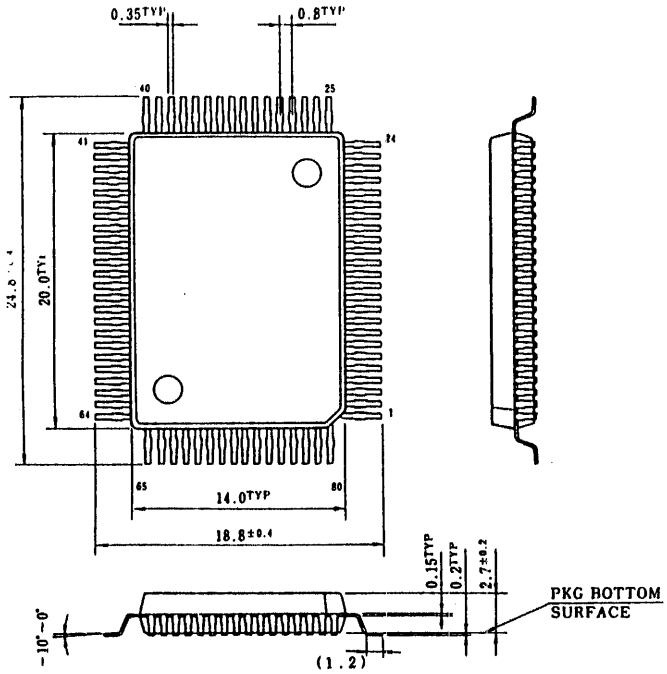
- Output terminals

		Min	Max	
Low level output voltage	Vol	V_{SS}	0.4	V
High level output voltage	Voh	4.0	Vdd	V
Output leak current	Ilo.		10	μA

- Power terminals

		Min	Max	
Power current	Idd		30 (Vdd=5.0V)	mA

■ EXTERNAL DIMENSIONS



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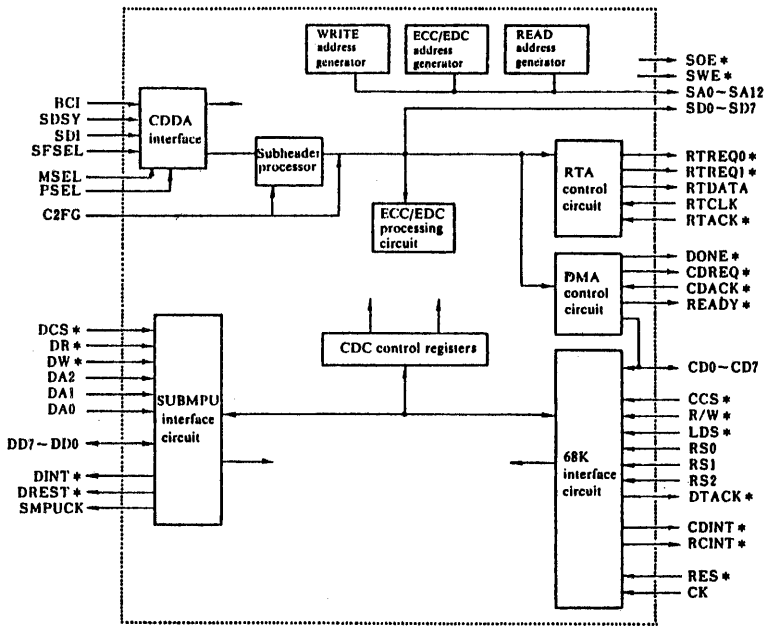
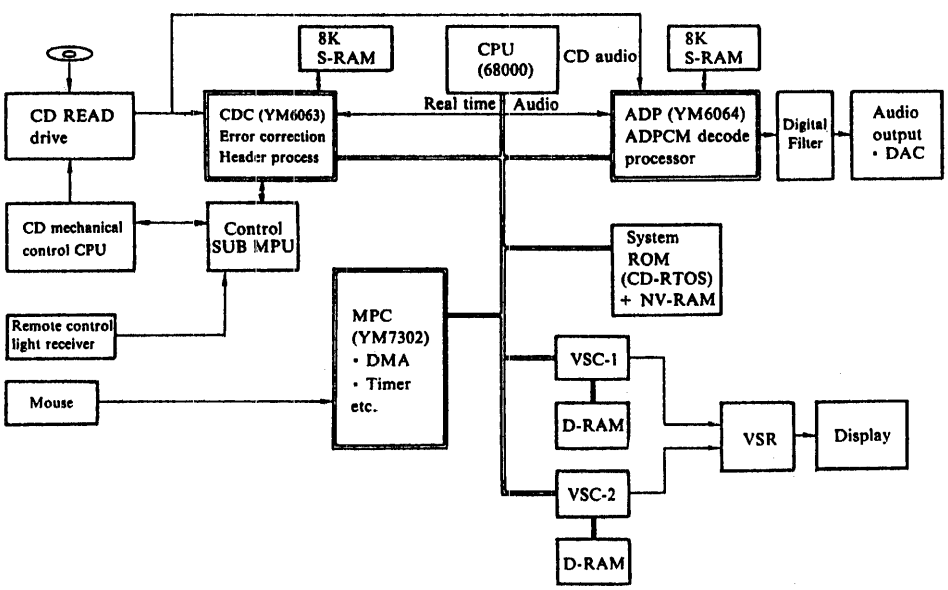


(*indicates a terminal which is active when low.)

■ SAMPLE CD-I CONFIGURATION



CD-I/CD-ROM

CD-I ADPCM Decode Processor

YM6064 ADP

■ OUTLINE

This ADP is an LSI chip used for processing CD-I audio signals (ADPCM decoding).
Reproduction of real time audio and of sound map audio can be done simultaneously by using this in conjunction with the YM6063 (CDC)

■ FEATURES

- CD-I format ADPCM data is converted to 16 bits linear PCM data.
  LEVEL A fs = 37.8 KHz 8 bits
  LEVEL B fs = 37.8 KHz 4 bits
  LEVEL C fs = 18.9 KHz 4 bits
- A circuit has been integrated specifically for digital mixing of real time audio and sound map audio.
- A double oversampling digital filter builtin to the CD-I format for LEVEL C
- A built-in 1dB x 127 step digital attenuation circuit
- A built-in overflow limiter
- A mute control terminal
- A CD audio digital signal input terminal
- A silicon gate CMOS, 80 PIN QFP, 5V power supply

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_{IN}	−0.3	V_{DD} +0.3	V
Ambient operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{ST}	−50	+125	°C

(Based on the reference voltage of Vss, AVss = 0.0V)

2. Recommended Operating Conditions

Supply voltage	+5V ±5% (Based on the reference voltage of V_{SS}, AV_{SS} = 0.0V)
Ambient operating temperature	0 ~ 70°C

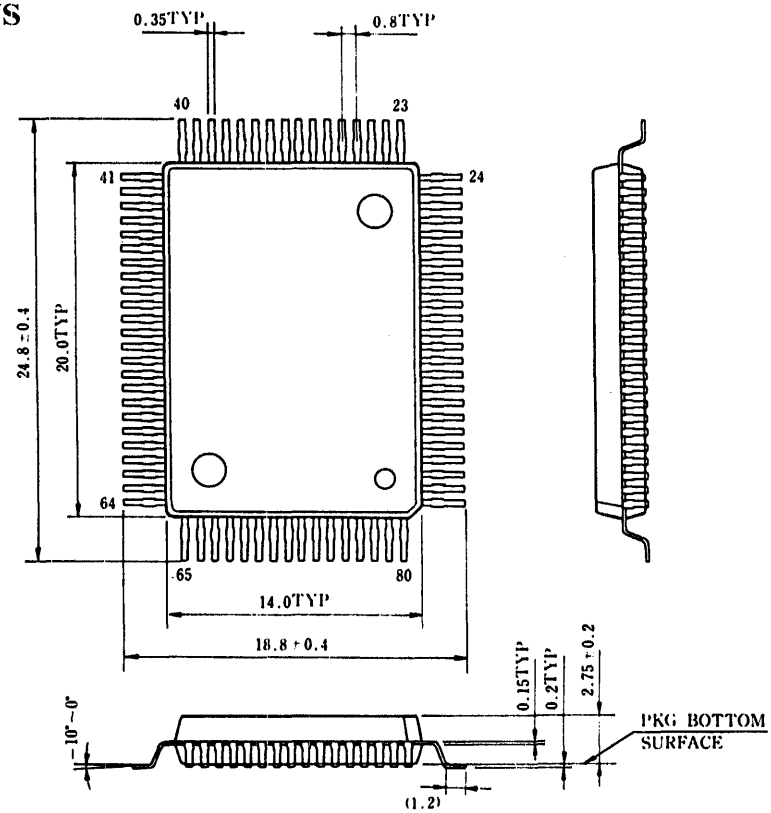
3. DC Characteristics (V_{DD} = +5V ±5%, T_{OP} = 0 ~ 70°C)

Item	Symbol	Condition	Minimum	Maximum	Unit
High level output voltage	V_{OH}	I_{OH} = −0.4mA	2.7		V
Low level output voltage	V_{OL}	I_{OL} = 0.8mA		0.4	V
High level input voltage (TTL level)	V_{IH}		2.2		V
Low level input voltage (TTL level)	V_{IL}			0.8	V
High level input voltage (CMOS level)	V_{IH}		3.5		V
Low level input voltage (CMOS level)	V_{IL}			1.0	V
Input leak current	I_L		−10	10	μA
OFF Input leak current-	I_{Lz}		−10	10	μA
Pull-up resistance	RU		60	600	KΩ
Power current	I_{DD}			50	mA

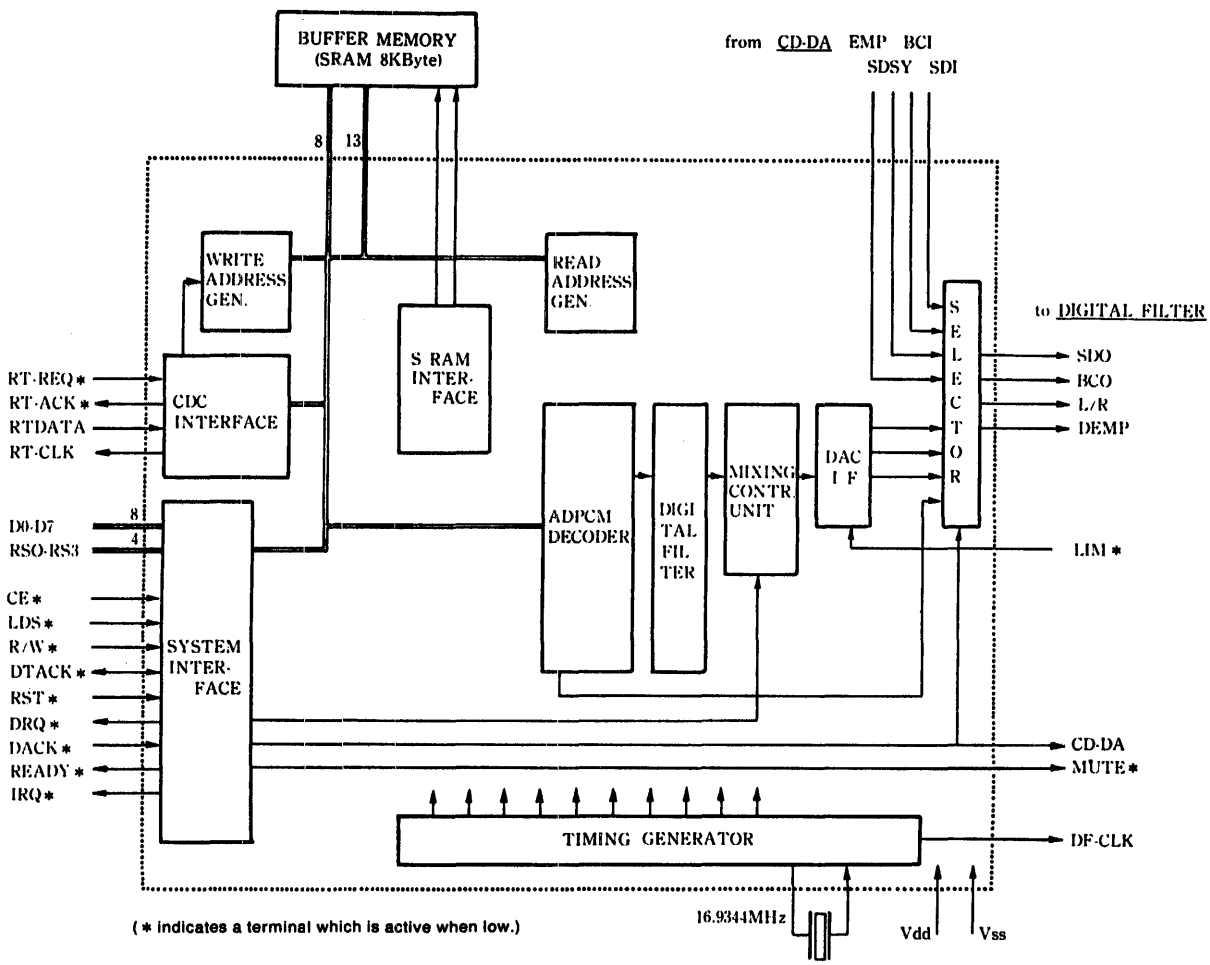
4. Terminal Capacitances (f = 1MHz)

Item	Symbol	Condition	Minimum	Maximum	Unit
Input teminal	C_I			8	pF
Output terminal	C_O	No load		10	pF
I/O terminal	C_{IO}	No load		12	pF
Output load capacitance	C_L			100	pF

■ EXTERNAL DIMENSIONS



■ ADP BLOCK DIAGRAM



CD-I/CD-ROM

Master Peripheral Controller

YM7302 MPC

■ OUTLINE

The MPC (Master Peripheral Controller) is a single chip integrated circuit used to provide compact yet effective control of the peripheral circuits (mouse, DMA, timer, interrupt, etc.) in a CD-I configuration.

■ FEATURES

- Direct interface capability with a 68000 MPU
- An integrated single channel DMA controller
- A built-in 1200 bps mouse interface circuit (when using a 16 MHz master clock)
- Built-in memory and I/O type address decode circuit
- An integrated 6 level order of priority interrupt handler
- A built-in 1.95 K-31.25 Kbps serial interface (when using a 16 MHz master clock)
- Integrated bus arbitration function
- A built-in 40 bit timer counter (battery back-up capacity)
- A built-in 32.768 KHz calendar clock oscillator circuit (battery back-up capacity)
- A built-in 16 MHz master clock oscillator circuit
- An integrated watch-dog timer
- An integrated 16 bit pre-scaling timer counter
- A built-in reset sequence circuit
- CMOS, 5V power supply, 100 PIN QFP

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3 ~ +7.0	V
Input terminal voltage	Vir	−0.3 ~ V_{DD} +0.3	V
Ambient operating temperature		0 ~ +70	°C
Storage temperature		−50 ~ +125	°C

2. Recommended Operating Conditions

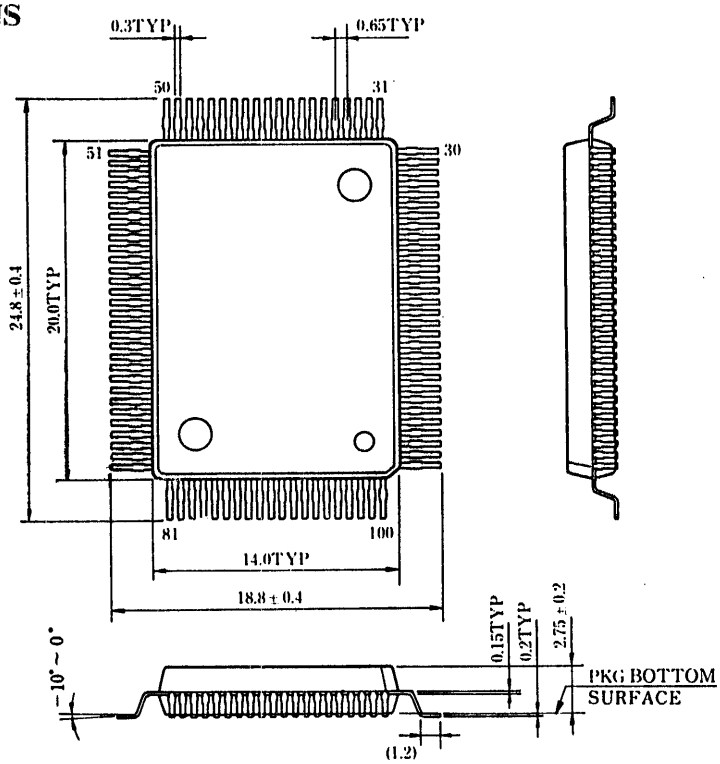
Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage			4.75	5.0	5.25	V
Input voltage	TCLK2 CONT* CKI TEST*	V_{IH} V_{IL}	3.5 −0.3	– –	V_{DD} 1.0	V V
	Other terminals	V_{IH} V_{IL}	2.0 −0.3	– –	V_{DD} 0.8	V V
Data storage voltage			2.0	–	5.25	V
Clock frequency			–	32.768	–	KHz
Operating temperature			0	25	70	°C

3. DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Low level input voltage	TCLK2 CONT* CKI TEST*	V_{IL}	−0.3	–	1.0	V	
	Other terminals	V_{IL}	−0.3	–	0.8	V	
High level input voltage	TCLK2 CONT* CKI TEST*	V_{IH}	3.5	–	V_{DD}	V	
	Other terminals	V_{IH}	2.0	–	V_{DD}	V	
Input leak current		I_L	−10	–	10	μA	(Note 1)
Tri-state input current (when OFF)		I_{LS}	−10	–	10	μA	
Low level output voltage	49 ~ 65 terminals 68 ~ 73 terminals	V_{OL}	–	–	0.4	V	I_{OL} = 1.6mA
	Other terminals	V_{OL}	–	–	0.4	V	I_{OL} = 3.6mA
High level output voltage		V_{OH}	2.7	–	V_{DD}	V	I_{OH} = −0.4mA
Power current (storage)					50	μA	
Power current (operating)					50	mA	
Input capacitance					12	PF	

(Note 1) Internal pull-up resistance of the TEST* and RXDO* terminals: 100 ~ 500 KΩ

■ EXTERNAL DIMENSIONS



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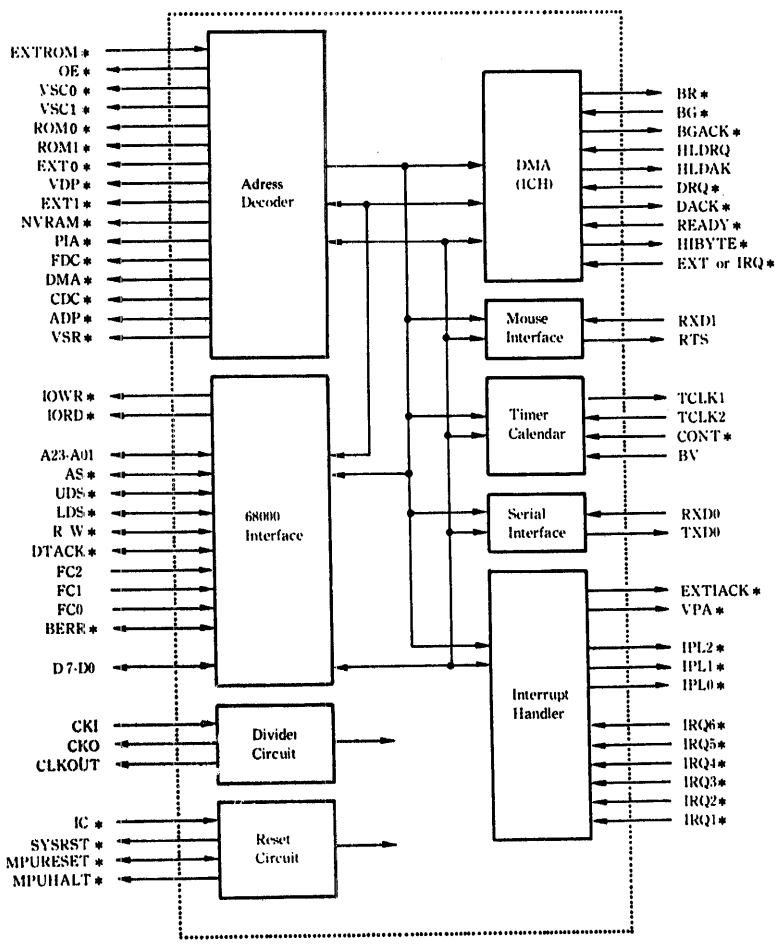

(* indicates a terminal which is active when low.)

Recommendation for surface-mount LSI

1. When using Soldering Iron;
   Temperature at the device lead part shall be controlled as 260 ℃ per 10 seconds or below.

2. Using Flow Soldering / Solder Dip;
   It is not appropriate to use this method for QFP devices and some of SOP devices.

3. By Infra-Red Reflow
   - To avoid character-deterioration or package crack by the absorbed moisture, PRE-BAKE shall be applied at the condition of 125 ℃ for 8 to 24 hours.
   - To avoid damaging local heating,
     Up-down heating is recommended.
   - Temperatures of the surface of package and
     PCB shall be below 235 ℃ and less than 10 seconds.
   - Please refer to Figure 1 for
     recommended Temperature Profile.

4. By VPS (Vapor Phase) Reflow
   - To apply PRE-BAKE as explained in 3.
   - Ambient Temperature shall be;
     Max. 215 ℃, less than 30 seconds.
   - Please refer to Figure 2 for Recommended Temperature Profile.

INFRA-RED REFLOW
Recommended Temperature Profile

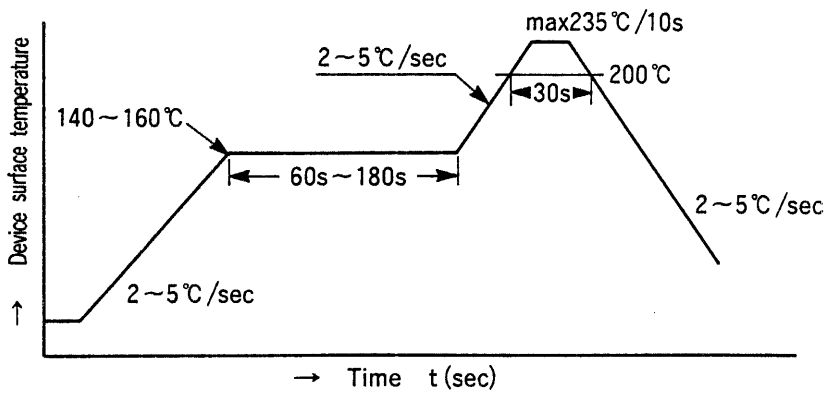

Figure 1

VAPOR PHASE REFLOW (VPS)
Recommended Temperature Profile

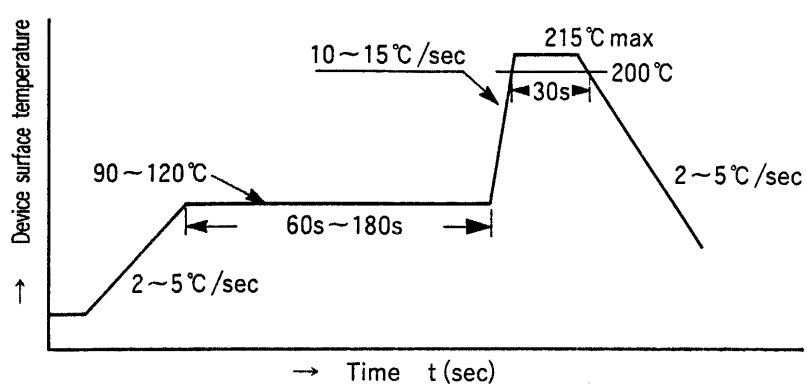

Figure 2

YAMAHA

YAMAHA CORPORATION

YAMAHA CORPORATION

Address inquires to:
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