XCELL

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XILINX®

The Programmable Logic Company℠

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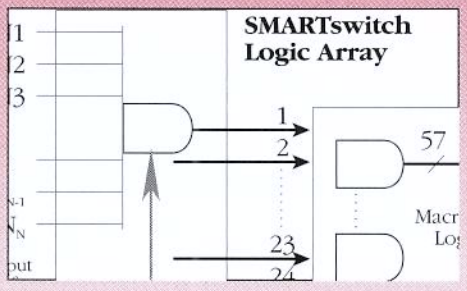

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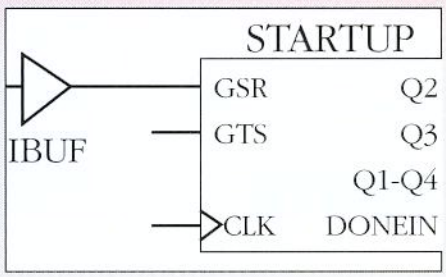

FROM THE FAWCETT

The Emergence of "Soft" Hardware

By BRADLY FAWCETT ◆ Editor

Since their introduction in 1985, FPGA devices have been used in tens of thousands of designs. In most of these, logic implemented in an FPGA could have been implemented with more traditional logic devices — masked gate arrays, or MSI/SSI devices, for example. Still, FPGAs were a better alternative for any number of reasons — no non-recurring engineering costs, lower design risks, less power dissipation, faster design and production cycles, etc.

More than that, however, static-memory-based FPGAs also provide a new and unique capability within electronics systems. With other logic technologies, hardware is indeed hard, and, once implemented in a system, cannot be changed. On the other hand, with SRAM-based FPGAs, changes can be made to a system's logic functions simply by reconfiguring the FPGAs in the system. Thus, systems can contain "soft hardware" — that is, hardware with functions that may be changed easily during normal system operation.

> *"More and more design engineers are taking advantage of this reconfigurable nature of FPGAs in their system designs."*

Now, I don't have any statistical data to prove this, but my gut-level feeling is that more and more design engineers are taking advantage of this reconfigurable nature of FPGAs in their system designs. A session at the recent Fourth Annual PLD Design Conference here in Silicon Valley was entitled "Using Reconfigurability," and included case studies of applications such as an interface to a military-standard computer bus and a tester for microprocessor-based board assemblies. A tutorial on the topic also was a popular part of the conference agenda. At the same time, farther north in Napa Valley, the IEEE Computer Society was holding the second annual IEEE Workshop on FPGAs for Custom Computing Machines (FCCM '94). The era of "engineered reprogrammability" in end-user products has definitely begun.

The types of applications using in-system reconfigurability are many and varied. One common use is the implementation of system diagnostics; the same FPGAs that implement the system's logic can be reconfigured to hold diagnostic logic to test that system. The diagnostic test logic is essentially "cost-free," except for the additional memory space required for the extra FPGA configuration programs. This approach has been used to include diagnostic logic in applications such as computer peripherals, industrial controllers, medical instruments, and IC testers.

Another common use of reconfigurable logic is the implementation of a single hardware design that can be adapted for varying tasks or environments. In such systems, any of a number of potential configuration programs can be downloaded into the system's FPGAs to alter the logic for particular applications or operations as needed. Hence, more functionality is implemented with fewer components, hardware design costs can be

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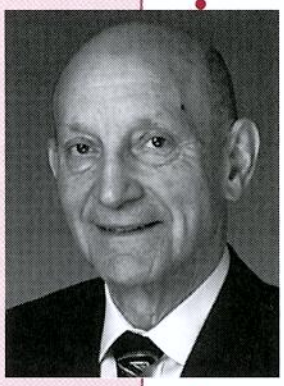
GUEST EDITORIAL

Programmable Logic in the Year 2000

by Bernie Vonderschmitt ◆ *President, Xilinx Inc.*

(The following is excerpted from a keynote address delivered at the recent Fourth Annual PLD Design Conference in San Jose, California.)

The first high-density programmable logic devices were introduced by Xilinx in late 1985. In the last eight years, device densities have grown from 800 to 25,000 gates and speeds have increased from 5 to 60 MHz. The topic of this presentation is the further evolution of programmable logic technologies through the year 2000.



Historically, the IC market has been driven by three major factors: speed, density, and cost. We can use history to guide our projections for programmable logic by examining the first 15 years of the microprocessor market (1971-1985) and the DRAM market (1970-1985). These two evolutions should be reliable guidelines, since programmable logic devices fall between microprocessors and DRAMs; like microprocessors, they can benefit from architectural improvements, and, like DRAMs, they have highly regular structures that benefit from advancements in process technology.

Let's start with speed. Microprocessor speed is best measured in millions of instructions per second (MIPs); from 1971 to 1985, microprocessors increased from .06 MIPs to 6 MIPs, a compound annual growth rate (CAGR) of 36%. About 40% of this improvement was based on process technology, and about 60% on architectural improvements. DRAM speed is best measured in access times, and improved from about 300 ns in 1970 to 80 ns by 1983, a 10% CAGR; almost all the improvement was due to process technology advances. Programmable logic devices fall between these two. FPGA system clock rates have increased from 5 MHz to about 50 MHz (using the PREP benchmarks) in the past eight years, about a 30% per year increase; about 70% of the increase has been due to process advances and 30% from architectural improvements. Based on these trends, we expect to see 100 MHz system clock rates for high-density PLDs within two years, and 250 MHz by the year 2000, a 25% CAGR. In the near term — the next two years — architectural improvements will account for about 40% of this increase, including features for better chip-to-chip performance, improved on-chip interconnect, better clock distribution, and better circuit design. Process technology will contribute nearly 60% of the increase, primarily due to the migration to 0.5 micron CMOS processes and optimized transistor performance.

> *"Based on these trends, we expect to see 100 MHz system clock rates for high-density PLDs within two years..."*

The easiest density benchmark for comparing architectures as diverse as microprocessors, FPGAs, and DRAMs is the number of transistors per chip. For microprocessors, this number grew from 2300 in 1971 (the 4004) to 275,000 in 1985 (the 80386), a 41% CAGR. In that same time period, DRAMs grew from 1,000 transistors to 280,000, a 54% CAGR. FPGAs have increased from 86,000 transistors

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XILINX®

Continued from page 3

in 1985 to over 3.4 million today, a 58% CAGR. Regular architectures advance the fastest, driven by advances in manufacturing processes, and FPGAs should continue to meet or exceed the density growth rate of DRAMs.

Translating this to "usable gates," from today's 25,000 gates (the XC4025), we're projecting 65,000 usable gates by the end of 1995, and 150,000 usable gates by the year 2000, a 42% CAGR. In the short term, 60% of that increase will result from architectural improvements such as more efficient logic blocks, better interconnect, and software improvements. Process improvements, such as 0.5 micron processes and triple-layer metal, will account for the other 40% of this growth.

"We believe the programmable logic segment could grow to 25% of the total CMOS logic market by the year 2000."

Increasing price-performance is probably the most important factor driving the expansion of the high-density PLD market. Again, slightly different metrics apply to the different technologies. For microprocessors, price-performance in terms of dollars per MIPs improved from $5,030 in 1971 to $50 in 1985, a compound annual improvement rate of 29%. For DRAMs, the metric is price per number of bits multiplied by the access time; this metric improved at a rate of 31% per year from 1970 to 1985. For programmable logic, a similar metric would be price divided by the number of gates multiplied by the supported system clock rate, which has improved about 30% per year over the last eight years. Again, these improvements are a result of architectural and process advances.

More usable gates per square millimeter of silicon and higher operating speeds resulting from the smaller die will continue to drive price-performance improvements in the future. For 5,000 gate devices, FPGAs cost four times more to manufacture than equivalent custom gate arrays, with the primary difference being the cost of the die. As die sizes continue to shrink, packaging and test costs will predominate. Thus, as we look near term to 0.6 micron processes, the cost ratio between PLDs and gate arrays will drop from 4:1 to 2:1. As this happens, the market for high-density programmable logic will expand at a very rapid rate.

In 1993, according to market research firm Dataquest Inc., the programmable logic market comprised 8.3% of the $12 billion CMOS logic market. We believe the programmable logic segment could grow to 25% of the total CMOS logic market by the year 2000. ◆

Revised Training Class Focuses on Design Tools and Techniques

The three-day Xilinx FPGA Training Class has been updated to include the features of the latest development system software and several other new topics. This course covers new XACT 5.0 features such as PPR Guide and XSimMake, expands its coverage of popular tools such as X-BLOX and Xilinx-ABEL, and discusses good design practices. The new training class focuses on the XC3000A and XC4000 architectures, putting greater emphasis on laboratory exercises, allowing for more hands-on work in class.

The class is appropriate for anyone new to Xilinx, or with little Xilinx experience. Classes are held in more than 40 locations in North America and 14 countries around the world, and can be brought to your own facility. For more information, call your local sales office. ◆

Reprogrammability in Action in Madrid

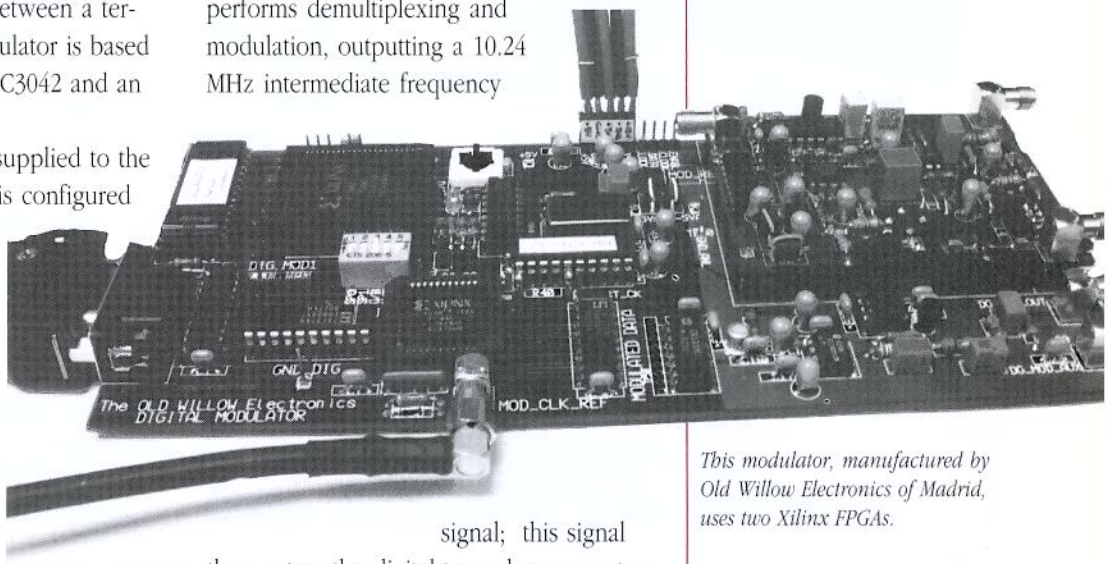
Reconfigurable FPGA technology can be used to create a single hardware design that can be adapted for varying standards, operating modes, or environments. Such a strategy was employed by The Old Willow Electronics of Madrid, Spain, in the design of a high-performance modulator for a data communications network.

The modulator is designed for transmitting data over a VSAT network; this network provides for bursty communications between two terminals or between a terminal and a hub. The modulator is based on two Xilinx FPGAs: an XC3042 and an XC3030.

When power is initially supplied to the system, the XC3042 device is configured from EPROM memory. In this initial configuration, the XC3042 FPGA is a "boot-loader" whose function is to download 32 Kbytes of EPROM contents into high-speed SRAM. The SRAM is loaded with a precalculated table containing 64 samples per bit for every possible 9-bit pattern of data to be transmitted; these samples hold the desired spectral characterisitics of the modulated signal. Once the SRAM is initialized, the XC3042 FPGA is reconfigured to hold the actual logic to implement the modulator. This process of configuring the XC3042 device, downloading to the SRAM, and reconfiguring the XC3042 FPGA takes less than one second.

The board is able to transmit at speeds of 64, 128, 256, 512, or 1024 kilobits per second with BPSK or QPSK modulation. The selection of these parameters is controlled by switches on the unit or through a modem port used to monitor and control system operation.

The XC3042 FPGA contains the interface to the data source and logic to build the data frames. The data is multiplexed into a single data stream (BPSK) or two data streams (QSPK). In either case the data stream is circulated in shift registers whose clock is determined by the data rate selection; the data stream is used to address the high-speed SRAM. The SRAM contents are input to the XC3030 device. Driven by a 40.96 MHz clock, this FPGA performs demultiplexing and modulation, outputting a 10.24 MHz intermediate frequency signal; this signal then enters the digital-to-analog converter. Highly parallelized data paths and careful floorplanning are used to achieve this high performance in the XC3030 FPGA.



This modulator, manufactured by Old Willow Electronics of Madrid, uses two Xilinx FPGAs.

Using a '386-based PC as the design platform, the FPGA designs were entered via schematic capture, using a hierarchical, top-down methodology. The designs were implemented with the Xilinx XACT development system (using placement constraints to floorplan the speed-critical portions of the design); and then thoroughly simulated. Finally, in-

Continued on page 6

> *"This process of configuring the XC3042 device, downloading to the SRAM, and reconfiguring the XC3042 FPGA takes less than one second."*

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	PART NUMBER
FPGAs		
XC3100A Family Overview	Features/benefits	#0010196-01
XC3100A Data Sheet	Technical Data	#0010205-01
EPLDs		
1994 PAL Conversion Guide & Datasheets	Technical data on replacing PALs with Xilinx EPLDs	#0401239-01
EPLD Design Guide	Technical information about creating designs for the XC7000 family of EPLDs	#0401191-01
XC7318 Data Sheet	Technical Data	#0010207-01
HardWire LCA		
HardWire Family Overview	Features/benefits	#0010124-03
HardWire Family Chart	List of FPGA devices and their HardWire equivalents	#100400
Corporate		
1994 Training Schedule	Description of training classes; schedule of world-wide locations	#0010134-03

For a complete list, please contact your sales representative or see XCELL Issue #10.

XNotes

XNotes are vertical market white papers provided for customers interested in learning more about specific markets and applications. XNotes provide technical background, market-oriented information and design tips, including application notes that suggest real solutions for your system needs. The following X-Notes are available: ◆

TITLE	PART NUMBER
PCMCIA Application note	#100490
Incorporating CIS into XC4000 PCMCIA Designs	#100491
FPGAs in the PC Card Market	#100460
Low Voltage Systems	#100469
A Fast Scalable Switch Matrix in an FPGA	#0010195-01

CUSTOMER SUCCESS STORY

Continued from the previous page

circuit testing was performed using a serial download from the PC; typically, the FPGAs have performed correctly on the first attempt.

According to Luis Miguel Brugarolas, The Old Willow Electronic's Engineering Manager, "The Xilinx software is extremely powerful. My experience is that, with the right design methodology, design cycles can be extremely short."

The Xilinx SRAM-based technology has proven to be an almost interference-free solution for this mixed analog-digital design. Although great care was taken in the design of the PC board, there is virtually no trace of interference in the output signals, even at very high clock rates. ◆

Mark Your Calendar

Xilinx will be participating in the technical program or exhibiting at each of the conferences and workshops listed below. For further information about any of these conferences, contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676).

Congratulations to Mark Lerner of Acuson Corp. who won the raffle for the 1994 Kawasaki Ninja ZX-6 motorcycle at the Xilinx booth at the Fourth Annual PLD Design Conference last April!

June 6 - 10
Design Automation Conference
San Diego, CA

June 13 - 16
Canadian Workshop on Field Programmable Devices
Kingston, Ontario, Canada

June 23 - 24
GI/ITG Workshop on User-Programmable Circuits
Karlsruhe, Germany

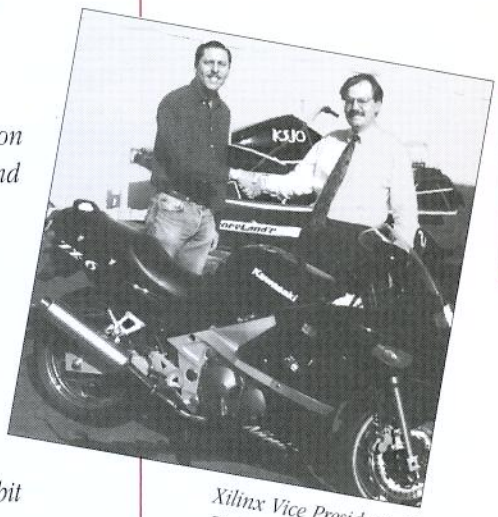
July 26 - 27
IC Card Expo
Santa Clara, California

Sept. 7 - 9
Fourth International Workshop on Field Programmable Logic and Applications (FPL '94)
Prague, Czech Republic

Sept. 19 - 23
EuroDAC/EuroVHDL
Grenoble, France

Sept. 19 - 23
IEEE ASIC Conference and Exhibit (ASIC '94)
Rochester, New York

Sept. 27 - 29
Wescon/IDEA Electronic Conference and Exhibition
Anaheim, California ◆



Xilinx Vice President of Product Marketing Chuck Fox (right) congratulates Acuson's Mark Lerner on his newly-won motorcycle.

For further information about any of these conferences, contact Kathleen Pizzo (Tel: 408-879-5377 Fax: 408-879-4676).

FINANCIAL REPORT

Record Revenue in 1994 Fiscal Year

Xilinx again achieved record revenues in fiscal year 1994 (April 1993 - March 1994), reflecting the strength of our product line and the continued expansion of the programmable logic market. Fiscal 1994 revenues totaled $256.4 million, an increase of 44% over fiscal 1993.

For the fourth quarter (ending April 2, 1994), revenues reached a record $75.4 million, an increase of 50% from the same quarter one year earlier and up 13.4% from the immediately preceding quarter. This revenue growth was driven by continued demand for our highest speed and highest density devices. While much of this revenue growth occurred in the North American market, European sales rebounded by increasing 21% from last quarter.

"In fiscal 1995, the XC4000 family will continue to be the primary contributor to revenue growth for Xilinx. In addition, we intend to bring to market two new product families targeted at lower cost," stated Bernie Vonderschmitt, Xilinx president. ◆

Continued from page 2

amortized over a greater number of systems, and design cycle times are greatly reduced. For example, this strategy was employed in the design of a controller for a 9-track, 1/2-inch tape drive. Using Xilinx FPGA devices, a single card capable of handling several different densities and encoding formats was developed. Users can select the desired format from a menu on the host system's terminal; this selection triggers the downloading of the appropriate FPGA configuration programs. Such "adaptable system" design has been particularly popular among test equipment manufacturers; reconfigurable FPGAs can be used to adapt the same hardware to perform varying types of tests.

Taking the concept of adaptable hardware to the extreme, several vendors, including Quickturn Design Systems, Zycad, and Aptix, offer ASIC emulation systems based on Xilinx FPGAs. In these systems, multiple FPGAs can be used to emulate logic designs comprising tens of thousands of gates. Using these systems, designers can test, debug, and verify large designs rapidly. Such an emulation system was used during the design of the Intel Pentium microprocessor, trimming months from the development cycle

"Reconfigurable FPGA technology already is shaping the future of computing."

In some systems, reconfiguration of the FPGAs is a normal part of the system's operation. This implies that the system has some "mutually-time-exclusive" functions that can be swapped into and out of the FPGAs as needed. For example, at any given time, a tape recorder can read or write, but never both simultaneously. Consequently, an FPGA within a digital tape recorder could be configured to perform one set of functions when writing data (such as data encoding and error code generation), and then reprogrammed to perform another set of functions when reading data (such as data decoding and error detection and correction). These types of "multi-purpose" hardware applications of SRAM-based FPGAs are especially cost-effective; at least twice the hardware would be required to implement the same functionality with traditional logic devices. Similar schemes have been employed in applications ranging from missile guidance systems to printer controllers to telecommunication network testers.

The long-term implications of "soft hardware" are staggering. Reconfigurable FPGA technology already is shaping the future of computing. Several universities and research laboratories have used Xilinx FPGAs to implement multi-purpose, high-speed coprocessors for accelerating operations in computer systems. The twenty-four papers presented at the FCCM Workshop were dedicated to this topic. Emerging companies such as Virtual Computing Corp., National Technology Inc., and Giga Operations Corp. are starting to commercialize this technology. For specific applications, reconfigurable FPGAs are bringing the performance of supercomputers to desktop systems. It's not hard to envision computers of the future automatically altering their own hardware to adapt to the program being executed.

In summary, the advent of in-system programmable, SRAM-based FPGAs has freed the designer from the "hard" nature of traditional logic ICs. New system architectures that take advantage of reconfigurable logic will continue to emerge as FPGA performance and density levels continue to increase. ◆

Xilinx Increases European Presence

As part of a global approach to serving programmable logic users, two recent announcements signaled a greatly increased Xilinx presence in the European marketplace. Xilinx has established a research and development center in Scotland and is planning a manufacturing facility in Ireland.

At the recent IEEE Workshop on FPGAs for Custom Computing Machines in Napa, California, Xilinx announced the establishment of Xilinx Development Corp., a research and development center focusing on the use of FPGAs in computing applications. Xilinx Development Corp., located in Edinburgh, Scotland, is a result of the acquisition of Algotronix Corp. in April 1993. Algotronix founders John Gray, Tom Kean, and Irene Buchanan have joined Xilinx and will continue to explore the use of FPGAs in creating programmable custom computers. Xilinx Development Corp. will also focus on software tools that facilitate logic implementation directly from high level design languages.

In April, Xilinx also announced plans to establish its first European manufacturing facility, to be based in Dublin, Ireland. Scheduled to begin operation in late 1995, this 100,000 square foot facility will provide Xilinx with additional capacity for wafer probe, customer return analysis, test program development, burn-in, reliability testing, quality assurance testing, and final test operations. The site will also be used for IC and software product development.

This $18 million investment is expected to create at least 300 new jobs by 1999. The result will be improved service and faster response times for all European customers. ◆

THIRD PARY PROGRAMMER SUPPORT FOR XILINX PRODUCTS

Manufacturer	XC17XXD	XC17XXL	XC17128	XC7236	XC7236A	XC7272	XC7272A	XC7336	XC7354	XC73108
Advin	X	X	X	X	X	X	X	June 94	June 94	June 94
BP Microsystems	X	X	X	X	X	X	X	June 94	June 94	June 94
Data I/O	X	X	X	X	X	X	X	June 94	July 94	July 94
Elan	X	X	X	X	X	June 94	June 94	June 94	June 94	June 94
ICE Technology	X	June 94	X	June 94	June 94	June 94	June 94	June 94	July 94	July 94
Logical Devices	X	X	X	X	X	X	X	X	X	X
SMS	X	X	X	X	X	X	X	June 94	June 94	June 94
Tribal Microsystems	X	June 94	X	X	X	July 94	July 94	July 94	July 94	July 94
Xeltek	X	X	X	X	July 94	June 94	June 94	June 94	June 94	June 94

COMPONENT AVAILABILITY CHART - MAY 1994

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120	XC3130	XC3142	XC3164	XC3190	XC3195	XC4003	XC4005	XC4006	XC4008	XC4010	XC4010D	XC4013	XC4002A	XC4003A	XC4004A	XC4005A	XC4003H	XC4005H	XC4025	XC7236	XC7272	XC7236A	XC7272A	XC7336	XC7318	XC7354	XC7372	XC73108
44	PLASTIC LCC	PC44	◆	◆			◆					◆										◆																	◆		◆		◆	N	◆				
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48	PLASTIC DIP	PD48	◆																																															
64	PLASTIC VQFP	VQ64		◆	◆	◆						◆					◆																																		
68	PLASTIC LCC	PC68	◆	◆	◆		◆	◆				◆	◆									◆	◆																		◆		◆			◆	◆				
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84	PLASTIC LCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆				◆		◆			◆	◆				
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100	CERAMIC QFP	CQ100				◆		◆																																										
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120	CERAMIC PGA	PG120																									◆								◆	◆	◆													
132	PLASTIC PGA	PP132						◆	◆				◆	◆									◆	◆																										
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144	PLASTIC TQFP	TQ144											◆	◆				◆	◆				◆	N														◆	◆										
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156	CERAMIC PGA	PG156																										◆	◆								◆												
160	PLASTIC PQFP	PQ160							◆	◆				◆	◆									◆	◆	◆		◆	◆	◆	◆	◆	◆			◆	◆												◆
164	CERAMIC QFP	CQ164								◆																																							
	TOP BRZ. CQFP	CB164								◆				N										N			◆																					
175	PLASTIC PGA	PP175								◆				◆										◆	◆																									
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176	PLASTIC TQFP	TQ176												◆						◆				N																										
191	CERAMIC PGA	PG191																												◆	◆							◆												
196	TOP BRZ. CQFP	CB196																													◆																		
208	PLASTIC PQFP	PQ208								◆				◆										◆	◆			◆	◆								◆	◆												
	METAL MQFP	MQ208																												◆	◆	◆																		
223	CERAMIC PGA	PG223																							◆							◆							◆	◆										
225	PLASTIC BGA	PB225																														◆	◆																N
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240	PLASTIC PQFP	PQ240																																															
	METAL MQFP	MQ240																																◆						◆	N									

◆ = Product currently shipping or planned N = New since last XCELL

XILINX RELEASED SOFTWARE STATUS -JUNE 1994

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform				Last Update
					PC1 *6.2*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS									
CORE FPGA	XC2,3,4K Support	Core Implementation	DS-502-xxx	1.42	5.00	5.00	1.42	5.00	07/94
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	4.10	5.00	5.00		5.00	07/94
Mentor[1]	V7.00	I/F and Libraries	DS-343-xxx	4.10			4.20		07/94
Mentor[1]	V8.2_5	I/F and Libraries	DS-344-xxx	1.10		5.00	1.10	5.00	07/94
OrCad[2]		I/F and Libraries	DS-35-xxx	4.23	5.00				07/94
Synopsys[1]		I/F and Libraries	DS-401-xxx	2.00		3.01	3.01	3.01	09/93
Viewlogic[2]	ViewDraw	I/F and Libraries	DS-390-xxx	4.15	5.00				07/94
Viewlogic[2]	ViewSim	I/F and Libraries	DS-290-xxx	4.15	5.00				07/94
Viewlogic[2]		I/F and Libraries	DS-391-xxx	4.15	5.00	5.01			07/94
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	4.30	5.00	5.00			7/94
X-BLOX[1]		Module Generation & Opt.	DS-380-xxx	1.04	5.00	5.00	1.04	5.00	7/94
XILINX PACKAGES									
Mentor 8	Standard		DS-MN8-STD-xxx	1.10		5.00	1.10	5.00	07/94
OrCad	Base		DS-OR-BAS-xxx	1.10	5.00				07/94
OrCad	Standard		DS-OR-STD-xxx	1.10	5.00				07/94
Synopsys	Standard		DS-SY-STD-xxx	1.01		1.10	1.10	1.10	09/93
Viewlogic	Base		DS-VL-BAS-xxx	1.20	5.00				07/94
Viewlogic	Standard		DS-VL-STD-xxx	1.20	5.00	5.00		5.00	07/94
Viewlogic/S	Base		DS-VLS-BAS-xxx	1.20	5.00				07/94
Viewlogic/S	Standard		DS-VLS-STD-xxx	1.20	5.00				07/94
Viewlogic/S	Extended		DS-VLS-EXT-xxx	1.20	5.00				07/94
XILINX HARDWARE									
Prom Pgmr.	Conf. Prom. Pgmr.		HW-112	3.31	5.00	5.00			04/93
Prom Pgmr.	Conf. Prom. Pgmr.		HW-120	3.14					
THIRD PARTY PRODUCTION SOFTWARE VERSIONS									
Cadence	Composer	Schematic Entry	N/A	4.2.2		4.30		4.30	N/A
Cadence	Verilog	Simulation	N/A	1.6.c.5		1.7BP		1.7BP	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.3-P3		1.60		1.60	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	2.0-P11		3.0BP		3.0BP	N/A
Mentor	NETED	Schematic Entry	N/A				7.XX		N/A
Mentor	QuickSim	Simulation	N/A				7.XX		N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2		8.2_5	8.2_5	8.2_5	N/A
Mentor	QuickSim II	Simulation	N/A	8.2		8.2_5	8.2_5	8.2_5	N/A
OrCad	SDT 386+	Schematic Entry	N/A		1.10				N/A
OrCad	VST 386+	Simulation	N/A		1.10				N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.0c		3.1	3.1	3.1	N/A
Viewlogic	ViewDraw	Schematic Entry	N/A		4.1.3a	5.1			N/A
Viewlogic	ViewSim	Simulation	N/A		4.1.3a	5.1			N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A		5.0	5.0			N/A
Data I/O	Synario	Entry and Simulation	N/A		1.0				N/A

NOTE: [1]FPGA Only [2]FPGA and EPLD

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - MAY 1994

Company	Product Name	Version	Function	Vendor Interface Name	FPGA Support	EPLD Support	X-BLOX Support
Accel	Tango	1.4	Schematic Entry	SCH2XNF	✓		
Acugen			Automatic Test Generation		✓		
ALDEC	Susie	6.12	Simulation	SusieXNF	✓		
Altium	P-CAD	6.0	Schematic Entry	PC-Xilinx	2k,3k		
Cadence (Valid)	Concept Rapidsim Composer Verilog	1.6 3.0BP 4.3 1.7BP or 2.0	Schematic Entry Simulation Schematic Entry Simulation	Xilinx Front End Xilinx Front End Xilinx Front End Xilinx Front End	✓ ✓ ✓ ✓		✓ ✓
Capilano	DesignWorks	3.1	Schematic Entry/Simulation	XDK-1	✓		
Compass	Asic Navigator QSim X-Syn		Schematic Entry Simulation Synthesis	Xilinx Design Kit	3k,4k		 ✓
CV (Prime)	Design Entry	2.0	Schematic Entry	Xilinx Kit	✓		
Data I/O	ABEL Synario	5.0 1.0	Synthesis Schematic Entry	Xilinx Fitter Xilinx Fitter	✓ ✓	✓ ✓	
EPS	SIMETRI	2.0	Simulation	XNF2SIM	✓	✓	
Exemplar Logic	CORE	1.2	Synthesis	FS-001	✓	✓	✓
Flynn Systems	FS-ATG		Automatic Test Generation	FS-High Density	✓		
GenRad	System Hilo	4.3	Simulation	Xilinx Tool Kit	✓		
IKOS	2800/2900 Voyager	5.02 1.2	Simulation Simulation	Xilinx Tool Kit Xilinx Tool Kit	✓ ✓		
Intergraph	ACE Plus Advansim VeriBest Design Systems	4.7.5.5 7.0	Schematic Entry Simulation Schematic Entry/ Simulation	Xilinx Design Kit 2.0 Xilinx Design Kit 2.0 Xilinx FPGA VeriBest Design Kit	✓ ✓ ✓		✓ ✓ ✓
ISDATA	LOG/iC	3.4	Synthesis	XNF-PP	✓		
Logic Modeling	Smart Model Library LM1200		Simulation Models Hardware Modeler	(In Library) Xilinx Logic Module	✓ ✓	✓	
Logical Devices	CUPL		Synthesis	Xilinx Fitter		✓	
Mentor Graphics	QuickSim II Design Architect Autologic	8.2_5 8.2_5 8.2	Simulation Schematic Entry Synthesis	Call Xilinx Call Xilinx Xilinx Synthesis Library	✓ ✓ ✓	✓ ✓	✓ ✓
MINC	PLDesigner-XL	3.0	Synthesis	Xilinx Design Module	✓	✓	
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2k,3K		
Nishimura	G-DRAW G-LOG	5.0 4.03	Schematic Entry Simulation	GDL2XNF XNF2GDL	✓ ✓		
Omation (See Accel)							
OrCAD	SDT 386+ VST 386+ PLD 386+	1.1 1.1 2.0	Schematic Entry Simulation Synthesis	Call Xilinx Call Xilinx	✓ ✓ ✓	✓ ✓	✓ ✓
Phase Three Logic	CapFast	2.2	Schematic Entry	SCH2XNF	✓		
Protel		2.0	Schematic Entry		✓	Q2	
Quad Design (Viewlogic Division)	Motive	3.4 Plus	Timing Analysis	XNF2MTV	✓		
Simucad	Silos III	92.115	Simulation	Included	✓		
Sophia Systems	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓	Q3	✓
Synopsys	FPGA Compiler Design Compiler	3.1a 3.1a	Synthesis Synthesis	Call Xilinx Call Xilinx	3K,4K 3K,4K		
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓		
Topdown Design	V-BAK	1.0	XNF to VHDL translator	XNF interface	Q2		
Viewlogic	ViewDraw ViewSim ViewSynthesis	4.1.3a 4.1.3a 2.3	Schematic Entry Simulation Synthesis	Call Xilinx Call Xilinx Call Xilinx	✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓

Speed- and Feature-Enhanced XC3100A Introduced, Includes New -2 Speed

The new XC3100A family combines the high speed of the XC3100 family with all the enhanced architectural features of the XC3000A. Along with improved software support, the XC3100A architecture sets new standards for ease-of-use and programmable logic price/performance. At the same time, this new family maintains footprint, density and package compatibility with the XC3000, XC3100, and XC3000A families, making it a drop-in replacement for those devices.

The XC3100A includes a new speed grade, the XC3100A-2, which is 20% faster than previous devices. With an average PREP benchmark speed of 85 MHz (uncertified), the XC3100A-2 is faster than competitive FPGA offerings. Some key performance parameters for the XC3100A are listed in the chart. The XC3100A is backwards-compatible with all XC3000-class devices, so it can plug into any existing XC3000, XC3000A, or XC3100 socket.

	XC3100A-2	XC3100-3	% Improved
Data path	233 MHz	195 MHz	19%
16-Bit loadable pre-scaled counter	180 MHz	150 MHz	20%
Divide-by-N loadable counter	325 MHz	270 MHz	20%
Average PREP Benchmark Speed	85 MHz	75 MHz	13%
Block Delays (Combinatorial)			
Logic Block	2.2 ns	2.7 ns	19%
Input Block	2.0 ns	2.2 ns	9%
Output Block	3.0 ns	3.3 ns	9%
Block Delays (Registered)			
Setup	1.8 ns	2.1 ns	14%
Clock to Out	1.7 ns	2.1 ns	19%

The XC3100A also contains the enhanced feature set of the XC3000A family, including improved routing resources, higher ESD protection, bitstream checking, and "Soft Startup" (see related article on page XX).

The XC3100A enjoys the benefit of powerful software support, including XACT-Performance™ (a timing-driven "place and route" tool) and X-BLOX (a high-level schematic module generator). All of this leads to increased ease-of-use and the ability to achieve excellent in-system performance. *Contact your Xilinx sales representative for more information.* ◆

Convert MQFPs to PQFPs

Until now, the only surface-mount packages available for the XC4008, XC4005H, XC4010, and XC4013 were metal quad flat packs (MQFPs). All four devices are now offered in plastic versions of the same packages (PQFPs) that maintain the same pinouts and package dimensions. In other words, the PQFPs are inexpensive, drop-in replacements for existing MQFP designs.

This packaging change is one of the benefits of migrating the manufacture of these devices to a smaller process geometry. The resulting smaller die sizes and reduced heat dissipation allow these high-density devices to perform reliably in inexpensive plastic packages. The PQFPs are priced significantly lower than their MQFP equivalents.

The following table outlines the new device/package combinations. The 208-pin PQFP is available now, and the 240-pin PQFP will begin shipments in 3Q94. The PQFP should be used for all new 208- or 240-pin designs, and current users of the MQFP are encouraged to convert their designs to PQFP as soon as the new packages are available.

Pages 4-20 and 4-23 in the *1994 Xilinx Programmable Logic Data Book* contain detailed package dimensions. The device/package table on page 10 of this issue includes the full listing of all XC4000 FPGA family offerings. *Please contact your local sales representative for more information.* ◆

	PQ208	PQ240
XC4005H		✓
XC4008	✓	
XC4010	✓	
XC4013	✓	✓

XC4025 Delivers 25,000 Gates

To meet the market's insatiable demand for higher density FPGAs, Xilinx has introduced the 25,000-gate XC4025. This new device nearly doubles the logic capacity of the XC4013, the previous density leader. The XC4025 has 78% more logic blocks and 33% more I/O than the XC4013.

XC4000 Architecture

As gate densities move above 20,000 gates, the concept of a "system on a chip" becomes a reality. FPGA device architectures must support a robust set of system features to handle this high level of integration.

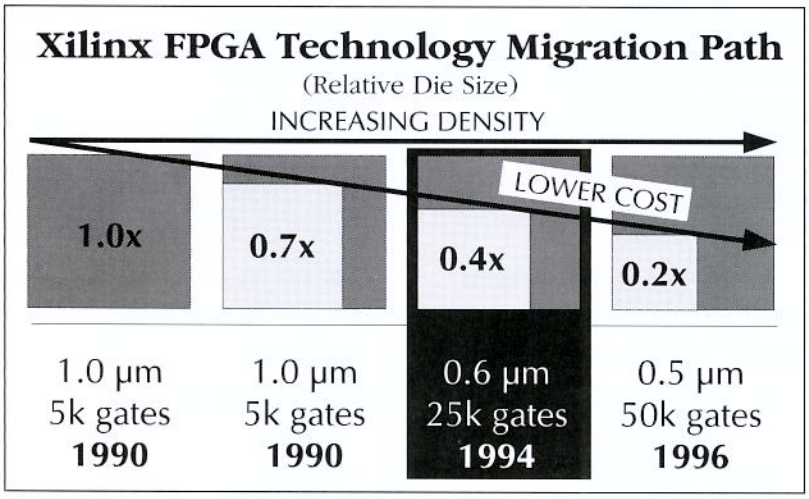


Figure 1

Perhaps the biggest silicon requirement in this density range is on-chip user RAM. About half of the current XC4000 customers use this feature today. However, the number is expected to exceed 75% for designs of 20,000 gates and above. The need for fast on-chip FIFOs, register files, and other temporary storage registers makes this a requirement. Up to 4 Kbytes of user RAM is available in the XC4025 FPGA.

The other system features of the XC4000 architecture strengthen the overall integration capabilities of the XC4025, including three-state buffers for on-chip bussing, eight global clocks, fast carry logic, wide decoders, and dedicated boundary-scan logic.

Process Technology

Advancements in process technology allow Xilinx to build higher density devices, while providing dramatic cost reductions on existing devices (Figure 1). As a high-volume, long-term customer for foundry services and a user of industry standard CMOS SRAM processes, Xilinx gains early access to advanced process technology. The XC4025 is manufactured on a 0.6 micron process, resulting in a die size roughly equivalent to that of the XC4013 on the previous generation process. Further reductions in process geometries should result in over 50,000 gates in a single FPGA device by 1996.

XACT Software

Design tools must provide the fastest possible time-to-design and the highest use of silicon. XACT 5.0 delivers the tools to support high-density designs effectively, such as incremental design support for the entire XC4000 family, new algorithms in PPR to recognize and efficiently place and route structured designs, and im-

	XC4010	XC4013	XC4025
Usable Gates	10,000	13,000	25,000
CLB Array	20x20	24x24	32x32
CLBs	400	576	1024
I/Os	160	192	256
Flip-Flops	1120	1536	2560
RAM Bits	12,800	18,432	32,768

proved support for synthesis designs through the Synopsys FPGA Compiler. Also, the initial software support for the XC4025 includes a pre-production version of the Xilinx Floorplanning Tool (XFT). These new features will provide the best support for the types of designs intended for this device — those with high levels of structure.

Applications

The XC4025 will address new markets for FPGAs while offering a footprint-compatible upward migration path for existing XC4013 designs requiring additional logic resources. With volume pricing approaching $400, the XC4025 will serve as a cost-effective *production* solution for many high-end systems.

Target applications for the XC4025 include highly-structured, bus-oriented, and flip-flop intensive designs such as those found in high-end computing equipment, medical equipment, video/imaging systems, industrial test equipment, and telecommunications systems. In these types of environments, the XC4025's relative contribution to overall system cost is similar to a lower-density FPGA's contribution to the cost of a LAN adapter or modem card. It is this relationship between FPGA cost and total system cost that makes high-density Xilinx FPGAs a good choice for high-end production environments.

Density

Figure 2 compares the logic capacity of the XC4025 to other FPGA devices either on the market or announced to be on the market soon. The chart is based on uncertified PREP Average Benchmark Capacity (ABC) measurements. The XC4025 is the first monolithic FPGA to deliver more than 100 instances.

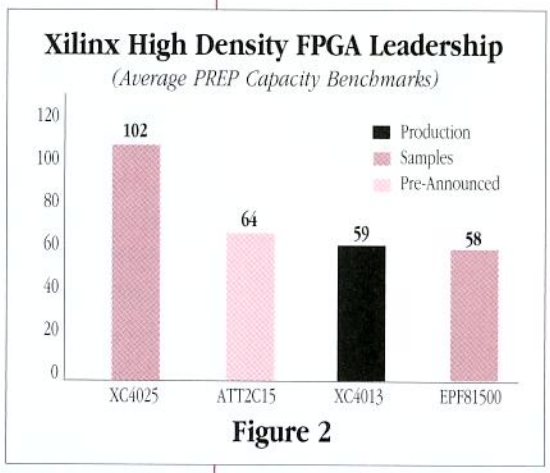
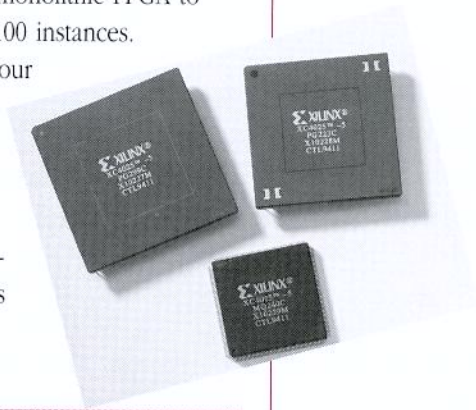


Figure 2

Please contact your local Xilinx sales representative for additional information on how to start designing with the world's largest FPGA. ◆



XC4025 Availability

Package	Available I/O	Samples	Production	Comments
PG223	192	Now	3Q94	Pin-compatible with XC4013
MQ240	193	Now	3Q94	Pin-compatible with XC4013
PG299	256	Now	3Q94	All 256 I/O available

10,000 Gates for $79

At 10,000 gates, the new, low-cost version of the popular, high-density XC4010 device — the XC4010D — helps to further deflate the myth that FPGAs are high priced

Based on the existing XC4000 architecture, the XC4010D supports all XC4000 family features, with the exception of on-chip RAM. This new device addresses cost-sensitive, high-density, "gates only" applications and drives high-density FPGAs into volume markets.

The XC4010D is available now in PC84 and PQ160 packages and is fully supported by the XACT 5.0 software. $79 represents 5,000 piece pricing for an XC4010D-6PC84. ◆

New XC1700L PROM Family Offers 3.3V Operation

The XC1700L family of Low Voltage Serial Configuration PROMs is now available. These devices are designed for operation at the new low-voltage 3.3V standard. They are built with our proven, reliable EPROM technology, and are designed to mate perfectly with the Xilinx ZERO+ family of 3.3V FPGAs.

The XC1718L and the XC1765L are available now. A single XC1765L PROM can be used to completely configure any Xilinx FPGA up to the XC3090L, and multiple PROMs can be cascaded to support multiple FPGAs and/or multiple configurations. Both devices are available in the 8-pin DIP, 20-pin PLCC, or space-saving 8-pin SOIC packages.

The Xilinx Serial Configuration PROM family is the easiest way to configure your Xilinx FPGAs, and Xilinx now provides the complete solution for 3.3V logic requirements. ◆

Xilinx Expands High-Reliabilty XC3000 FPGA Families

In response to customer requests, Xilinx has expanded the High-Reliability XC3000 product offerings to include the XC3000A, XC3100 and XC3100A families. The XC3000A and XC3100 families are available in military temperature range product today. Full Mil-Std-883B versions of the XC3100A will be introduced in 4Q94.

The Xilinx XC3000A family is an evolutionary improvement upon the popular XC3000 family. It is completely pin-and-function-compatible with the XC3000, but offers significant benefits for both new designs and existing applications. For new designs, the XC3000A provides improved routing resources, allowing easier connections between the output of IOBs and CLBs to the internal three-state buffers (TBUFs). It also offers optimized Automatic Placement and Routing (APR) algorithms, resulting in more routable designs, as well as up to 10% higher performance than the equivalent XC3000 devices at the same cost. In existing designs, the XC3000A devices are direct replacements for current XC3000 products, providing significant benefits such as improved ESD protection and reduced ground bounce through "Soft Startup" (see related article on page 24).

The Xilinx XC3100 family is designed to give you the maximum performance available in a Hi-Rel FPGA. While it is also a drop-in replacement for the existing XC3000 products, the XC3100 family offers >50% overall performance improvement over the fastest available XC3000 product. It also provides higher I/O sink/source capability, improved slew rate control, and increased ESD protection. The XC3100 family also offers increased logic capacity; the XC3195 features 40% higher density than the XC3090 (7000 usable gates), while maintaining footprint and pinout compability.

The XC3100A family combines the features of the XC3000A and XC3100 devices. XC3100A devices are fully bitstream- and pin-compatible with the XC3000, XC3000A and XC3100 devices. Thus, the 883B versions coming in the fourth quarter will be drop-in replacements for the military-temperature versions of the XC3000A and XC3100 families. Designers of high-reliability systems can prototype with the XC3000A or XC3100 families today, and then switch to the XC3100A 883B products for production later this year. ◆

Device	Speed Grade	Comments
XC3020	*-50,-70,-100*	
XC3020A	-7	10% faster than -70 at same price
XC3120	-5	fastest Hi-Rel FPGA available
XC3042	*-50,-70,-100*	
XC3042A	-7	10% faster than -70 at same price
XC3142	-5	fastest Hi-Rel FPGA available
XC3090	*-50,-70,-100*	
XC3090A	-7	10% faster than -70 at same price
XC3190	-5	fastest Hi-Rel FPGA available
XC3195	-5	new high-density capability

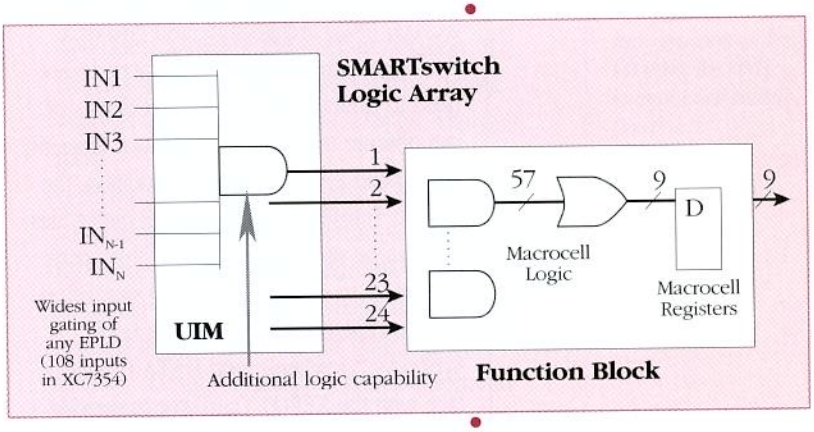
SMARTswitch:
More Logic Automatically

All devices in the XC7000 family of EPLDs incorporate a Universal Interconnect Matrix as the principal means of interconnecting the logic function blocks. This UIM™ gives unrestricted access to all the logic resources within an EPLD logic block. In other words, the XC7000 EPLDs achieve 100% routability with 100% utilization.

SMARTswitch™, a new feature of the Xilinx XEPLD development software, automatically provides the capability to implement logic in the UIM, improving both logic density and performance without any user intervention. Each of the 24 function block inputs can be driven by a very wide logic gate in the UIM whose inputs can be any signal on the chip. This is a powerful capability for implementing complex designs such as long counters and state machines that require wide gating for count enable and decode functions.

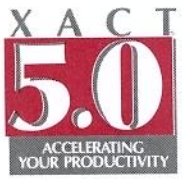
SMARTswitch adds this additional logic capability with no speed penalty. Since UIM switching delays are constant independent of routing, there are no additional timing delays.

XEPLD Translator software version 5.0 will implement SMARTswitch logic automatically, without user intervention. During the automatic logic optimization step, the software looks for logic that can be placed in the SMARTswitch, and then automatically fits it there. Thus, EPLD users can realize the increased density and performance benefits provided by SMARTswitch without having to understand the architecture or perform manual placement. ◆



Improved Routing Success with XACT 5.0

One of the major goals during the development of XACT 5.0 was improved "first-time" success when mapping, placing, and routing FPGA designs with PPR. We can happily report that significant improvements have been made.



In our extensive test suite of customer designs, PPR has shown an overall improvement in design completion ranging from 50% to over 100%, depending on the target device.

Extra effort was directed toward improving PPR's performance for high-density designs (that is, designs targeting the XC3090/A, XC3190/A, XC3195/A, XC4010, XC4013, or XC4025 FPGA).

On average, PPR v5.0 achieved first-time success on well over twice as many difficult high-density designs as with the previous release. Be sure to install your updates to enjoy much higher first-time routing success and increased design performance. ◆

XILINX®

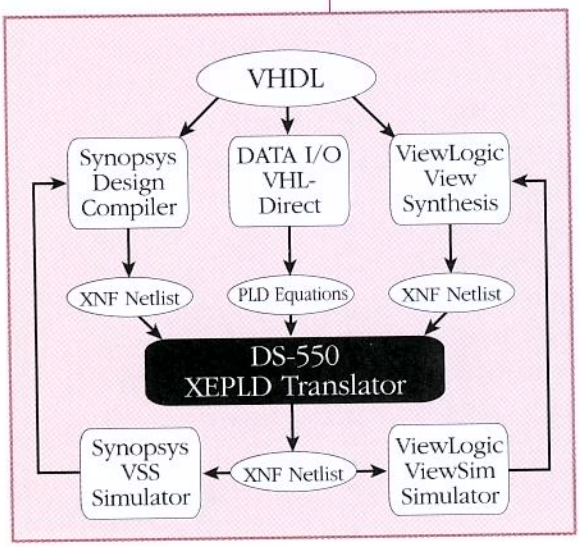
Logic Synthesis Support for EPLDs

XACT 5.0 ACCELERATING YOUR PRODUCTIVITY

The XACT 5.0 Development System, which includes the DS-550 XEPLD Translator, now supports design entry using high-level design languages (HDLs) for the Xilinx XC7000 EPLD family. Complex designs created with an HDL often require less time to develop than those created using traditional schematic or equation-based design techniques. HDLs also can provide a consistent system design methodology for multiple logic technologies. By using an HDL, a designer can focus on circuit functionality without learning a vendor-specific CAE tool or language, yet can still automatically fit the design into a Xilinx EPLD or FPGA.

The Xilinx DS-550 Translator accepts netlist files produced by a variety of HDL compilers. The Translator automatically optimizes the synthesized design, maps it into the XC7000 EPLD architecture, and creates a device programming file. Designers do not need to understand architectural details or use obscure techniques to produce efficient, high-speed EPLD designs. In addition, the DS-550 Translator produces XNF netlist files that can be used by a variety of third-party simulators to support full-timing simulation.

The HDL compilers available from Synopsys, ViewLogic, and DATA I/O interface with the XEPLD Translator to provide a comprehensive development environment that takes a design all the way from concept to implementation. These third-party synthesis compilers offer a variety of features.



Synopsys — FPGA Compiler and Design Compiler

The FPGA Compiler and Design Compiler from Synopsys, along with the Xilinx/Synopsys Interface (XSI) from Xilinx (DS-401), provide fast efficient synthesis of Xilinx EPLDs. Its features include:

- Choice of VHDL or Verilog HDL design languages
- Extensive macro library (useful for explicitly accessing EPLD features)
- DesignWare library (supports efficient implementation of behavioral operators)
- Multiple platform support: Sun, HP, RS6000
- Back annotation for full timing simulation
- Beta version available in July 1994, production in September 1994

ViewLogic - ViewSynthesis

The ViewSynthesis compiler from ViewLogic supports VHDL design entry for both the Xilinx EPLD and FPGA architectures through the Xilinx/Viewlogic Interface. The ViewSynthesis package includes these features:

- Fully integrated with the ViewDraw schematic capture software
- Fully integrated with the ViewSim simulator
- Support for PC, Sun and HP platforms
- Common flow for EPLD and FPGA designs
- ViewLogic tools on the PC, including the ViewSynthesis compiler, are available from Xilinx
- Beta version available in July 1994, production in September 1994

DATA I/O - VHDL-Direct

The VHDL-Direct compiler from DATA I/O is fully integrated into the Open ABEL design environment. Those familiar with ABEL-HDL can quickly become effective with VHDL-Direct, which includes the following features:

- Low cost
- Compatible with the XABEL Design Environment
- Supports PC platforms
- Structural, data flow (RTL), and behavioral language support
- Open-ABEL output file format
- Production version available now ◆

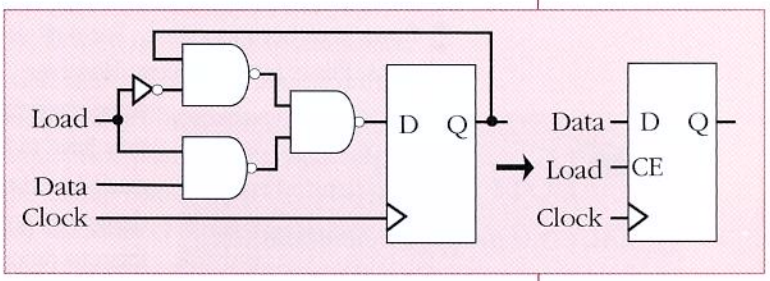
Synopsys Improves FPGA Synthesis Tools

Synopsys is now shipping version 3.1a of their FPGA Compiler and Design Compiler synthesis and simulation tools. These tools contain many new features that enhance the quality of results when synthesizing to Xilinx FPGAs. Principal among these enhancements is the ability to synthesize logic into two important logic resources of the Xilinx XC3000 and XC4000 FPGA architectures: dedicated flip-flop clock enables and I/O block flip-flops and latches. Use of these logic resources frees up internal CLB resources and routing, increasing FPGA capacity and performance.

Synthesis users following recommended design methodologies often generate highly-synchronous circuits that can take advantage of the FPGAs' built-in clock enable function. Both FPGA Compiler and Design Compiler now take advantage of the flip-flop clock enables provided in the XC3000 and XC4000 FPGA architectures. Whenever a multiplexer precedes the data pin of a register, as in the diagram, the synthesis compiler will automatically map the logic using the FPGA's clock enable feature. No additional work is required on the part of the user. This feature typically results in a 10% to 20% area and speed improvement, while also preventing race conditions at the register's inputs.

In addition, both of the compilers can now map to sequential I/O elements (such as INFF, OUTFF, and INLAT). Where applicable (that is, when an input or output signal is registered without using a clock enable or reset), use of the I/O blocks' registers reduces congestion in the CLB array and improves performance. A small patch library with a revised set of sequential I/O elements must be installed to take advantage of this feature. This patch library was sent to all XSI v3.01 users, and is also available from the Xilinx technical support staff.

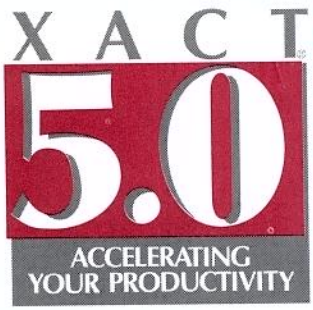
As before, the FPGA Compiler can directly optimize and map logic into XC4000 family CLB and IOB logic structures, allowing the compiler to perform accurate speed/area tradeoffs. Constraint-driven optimization takes into account the timing of CLBs and IOBs. With the release of version 3.1a, the user's timing constraints are placed in the XNF file produced by the Synopsys synthesis compiler; the constraints can then be used by XACT-Performance to optimize placement and routing within PPR, thereby achieving a higher percentage of completed designs that function at the desired speed. FPGA Compiler v3.1a now also reads XNF files, allowing the back-annotation of designs after routing for post-layout timing analysis using the Synopsys Design Analyzer tools.



The synthesis compiler will implement the logic structure on the left using the FPGA's built-in clock enable function.

With the addition of XACT-Performance support and XNF file back-annotation capability, there is more reason than ever to use FPGA Compiler v3.1a for synthesizing designs described in high-level design languages to Xilinx FPGAs. Design Compiler v3.1a is improved over v3.0c as well, so users of this tool will also see significant improvements, although not as dramatic as those of FPGA Compiler.

Synopsys FPGA Compiler and Design Compiler version 3.1a can be used with the current XSI libraries to take advantage of these new enhancements, as described in XSI Technical Bulletin #5. (This bulletin has been sent to all XSI users; additional copies are available though your local Xilinx FAE or the Xilinx technical hotline.) New XSI libraries that will even further improve synthesis results will start shipping this quarter as part of the XACT 5.0 update. Xilinx strongly encourages all Synopsys users to upgrade to v3.1a to take advantage of the significant improvements included in this new release. ◆



Processing Existing Designs With XACT 5.0

The XACT 5.0 release contains many improvements over previous versions of Xilinx software. To implement some of these changes, the place and route design flows have been modified. For new designs, this is not a problem. However, some changes may have to be made to existing designs to get them to process under the new flows.

"You can use the new XACT 5.0 design implementation tools with your existing libraries. New designs should, of course, use the new Unified Library elements."

A document explaining these issues in detail is shipped with the XACT 5.0 release. Entitled "Design Migrations," this document can be found in the "Getting Started" envelope. The remainder of this article summarizes the contents of that document.

The new versions of XDM and XMAKE should look familiar. They do not contain major changes from previous versions. The menu structure is basically the same, although new options have been added to many of the menus. In addition, a new menu appears when running XMAKE from XDM . This "target" menu allows you to choose where you want XMAKE to stop.

Do not mix XACT 5.0 Unified Library elements with components from older libraries. Mixing libraries leads to problems in back annotation and simulation. For this reason, the software will not process a design that contains elements from different libraries. Furthermore, it is not recommended that you replace existing schematic elements with XACT 5.0 library counterparts. The gates and macros are of different sizes, and pin locations will not line up on the schematics. Unless your design is very small, the benefits of switching an existing design to use XACT 5.0 libraries will be outweighed by the amount of time spent moving blocks, connecting wires, and checking connections. You can use the new XACT 5.0 design implementation tools with your existing libraries. New designs should, of course, use the new Unified Library elements.

Reprocessing Existing XC4000 Designs

The XC4000 design flow has been slightly changed for XACT 5.0. A new tool in the place-and-route flow called XNFPREP will identify design errors up front, before the design is sent to PPR. New features such as the PPR guide option will change the way design iterations are processed. Hard Macros have been replaced by RPMs (Relationally-Placed Macros). Any custom hard macros you have created with the HMGEN program must be converted to RPMs; this is done by using the HM2RPM program.

Reprocessing Existing XC2000/ XC2000L/XC3000/XC3100 Designs

The place and route design flow for XC2000 and XC3000 designs has changed only slightly. The main change is that a new program called XNFPREP replaces XNFDRC in performing design rule checks.

Designers should seriously consider targeting the XC3000A or XC3100A families instead of XC3000 or XC3100. The XC3000A family is a pin-compatible superset of the XC3000 line. "A" parts are

See PROCESSING, next page

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Using the XC4000 Startup Symbol

All members of the XC4000 product family include dedicated nets for the Global Set/Reset (GSR) and Global 3-State (GTS) signals. An active GSR sets or resets each flip-flop on the device, depending on which flip-flop primitive is specified in the design. Both CLB and IOB flip-flops are affected. An active GTS places all output pads on the device in a 3-state mode. Both signals are active High.

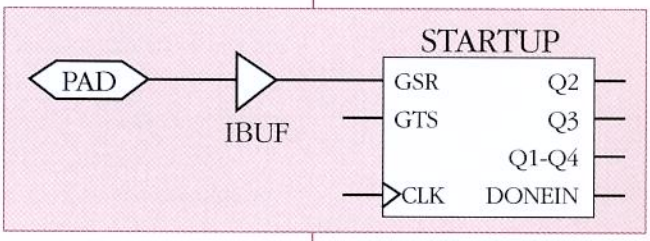
Using these dedicated nets frees programmable routing resources for use by other functions in a design. These nets can be accessed from either external pads or internal signals. In either case, the Startup symbol from the Xilinx XC4000 library provides user access to the GSR and GTS nets.

If user control over the Global Set/Reset and Global 3-State functions is not needed, the Startup symbol need not be included in the design. In this case, only the configuration process makes use of the GSR and GTS nets; after configuration they are inaccessible.

To drive the GSR net from a pad, add the Startup component to your schematic as you would any other library component, or include the Startup module in the HDL code, as described in the appropriate User Guide. Add an IPAD and IBUF; from the IBUF output drive the GSR input pin of the Startup symbol (as in the diagram). To implement an active Low signal, insert an inverter between the IBUF and the GSR pin of the Startup symbol; the inverter is absorbed into the Startup logic block and inverts the sense of the driving input. The same technique applies to the Global 3-State net. The nets driving the Startup symbol can be assigned symbolic names of your choice; however, do not use the names GSR or GTS for any nets in your design, as they are reserved system names. The GSR and GTS pins can also be driven by an internal net by attaching that net to the appropriate pin of the Startup symbol.

The Startup outputs (Q2, Q3, Q1-Q4) display the status of the startup process at the end of configuration. These outputs are rarely used and need not be connected. See page 2-29 and 2-30 of the 1994 Programmable Logic Data book for a detailed explanation of these outputs. The CLK and DONEIN inputs to the Startup symbol typically are left unconnected.

Simulation of the Startup component is not currently supported. GSR and GTS stimulus must be supplied in the simulation input vectors. ◆



Example schematic for driving the Global Set/Reset net from an external pin.

Processing

Continued from the previous page

faster and less expensive than their non-A equivalents. In addition, the "A" parts have increased routing resources and improvements to several other specifications. From the software side, the XC3000A parts use a different design flow (see the next section) that provides access to XBLOX and to timing driven placement-and-routing in the PPR program.

Reprocessing Existing XC3000A/XC3100A/XC3000L Designs

The design flow for XC3000A, XC3100A, and XC3000L designs has changed significantly. The PPR program, formerly for XC4000 design only, is now used to place and route the XC3000A, XC3100A, and XC3000L families. For the first time, this allows access to XACT-Performance and XBLOX for these architectures, which will help increase performance and reduce design cycle time. ◆

Designing for Very Low Power Consumption

Xilinx FPGAs use CMOS technology and are capable of very low power consumption. Here are some hints for the power-conscious user.

Dynamic Power Consumption.

At high clock rates, most power is consumed in charging and discharging internal node capacitances and external load capacitors. The user may have little choice here. Some power-saving techniques (such as clock gating) conflict with the traditional, safe design methodologies that are recommended for high-performance synchronous design. For example, in power-critical designs, the user may be tempted to disable a clock line, instead of running the clock continuously and deactivating it with the CE signal.

The most dramatic change in power consumption comes from reducing V_{CC} from nominally 5 V to nominally 3.3 V, the new standard. This cuts power consumption roughly in half, albeit with a performance penalty. Xilinx offers the XC2000L and XC3000L devices guaranteed and characterized for 3.0 to 3.6 V operation. All other Xilinx FPGA devices need a supply voltage well above 3.5 V, because their internal V_{CC} monitor circuit might respond at 3.5 V and shut down operation and configuration.

"Some power-saving techniques (such as clock gating) conflict with the traditional, safe design methodologies that are recommended for high-performance synchronous design."

Static Power Consumption

Although static power consumption is always below 50 mW, battery-operated XC3000, XC3000A and XC2000 designs can benefit from a significant reduction into the microwatt range.

The largest dc power consumer, using 10 mA = 50 mW max, is the the on-chip linear circuit that reduces the input threshold voltage from 50% of V_{CC}, called CMOS level, to about 1.2 V, called TTL level. The latter is the default because it is compatible with all forms of 5-V logic. For battery operation, it is advisable to change the XC2000 or XC3000 input thresholds to CMOS.

XC4000 devices do not offer this option. Their input thresholds are always at the TTL level in order to be compatible with XC4000 outputs, which use a "totem-pole" structure with n-channel transistors for both pull-down and pull-up. This guarantees only 2.4 V min as V_{OH}, not high enough for a reliable interface to CMOS-threshold inputs. XC4000 devices, therefore, have a static power consumption of up to 50 mW. That is also why there is no PWRDWN input on the XC4000. It does not make sense to battery-backup the XC4000 configuration.

XC3100 and XC3100A devices have an additional 25 mW static power consumption, even with CMOS input thresholds, and, therefore, are not ideal for low-power applications.

Serial PROM

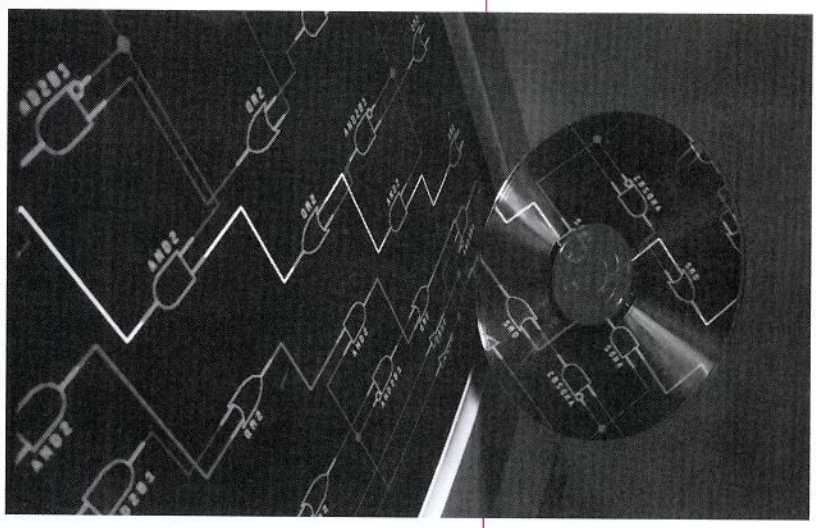
For the power-conscious designer, the idle or stand-by current (I_{CCS}) of the XC17000 Serial PROM may be a cause of concern. For XC17xxxD and L circuits, this

See LOW POWER, next page

XAPP Files on XACT 5.0 CD-ROM

Design files for selected XAPP Application Notes are included on the XACT 5.0 CD-ROM. These files contain macros that can be used directly in larger designs, or modified to suit a specific need. Typically, the files are comprised of a ViewLogic schematic for each macro, a top-level test schematic and implementation notes discussing how the macro is best used.

Files are included on the CD-ROM for the XAPP Application Notes listed below. These files also are available through the Xilinx Technical Bulletin Board Service. ◆



XAPP 001 High-Speed Synchronous Prescaled Counter
XAPP 002 Simple, Loadable, Up/Down Counter
XAPP 003 Synchronous Presettable Counter
XAPP 004 Loadable Binary Counters
XAPP 005 Register-based FIFO
XAPP 007 Boundary Scan Emulator for XC3000
XAPP 009 Harmonic Frequency Synthesizer and FSK Modulator
XAPP 014 Ultra-Fast Synchronous Counters
XAPP 021 Dual-Prescaled Presettable Counter
XAPP 022 Adders, Subtracters and Accumulators in XC3000
XAPP 023 Accelerating Loadable Counters in XC4000
XAPP 026 Multiplexers and Barrel Shifters in XC3000/XC3100
XAPP 028 Frequency/Phase Comparator for Phase-Locked Loops
XAPP 029 Serial Code Conversion between BCD and Binary

Low Power

Continued from previous page

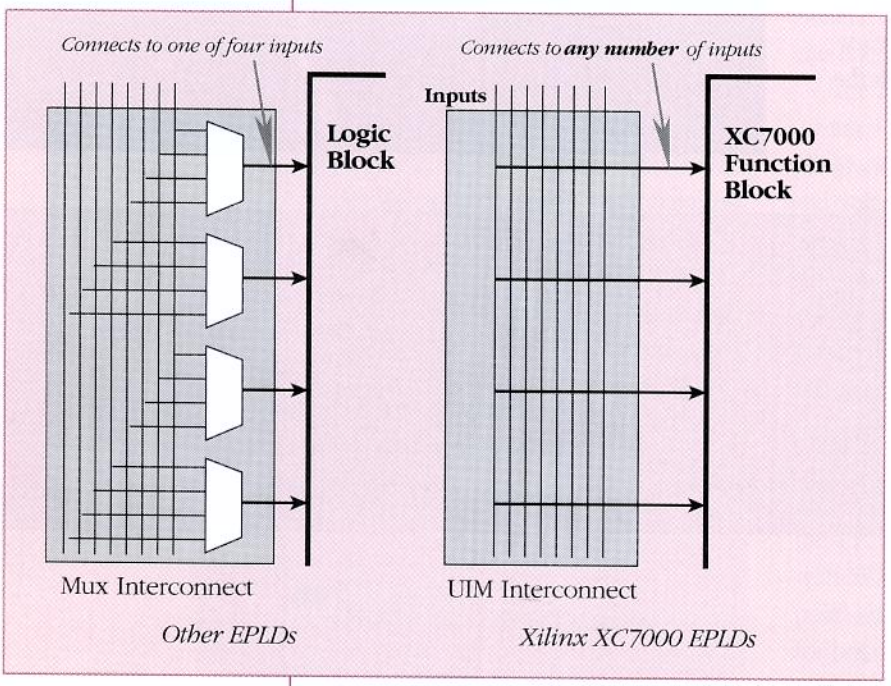
current is 1.5 mA. (The 1994 Data Book incorrectly lists 0.5 mA as the current.) There is, however, a way to reduce this current to zero, as shown on page 2-235 of the 1994 data book. A future redesign of all serial PROMs will reduce this standby current to a few µA.

Powerdown

XC2000 and XC3000 devices can be put to sleep by pulling the $\overline{\text{PWRDWN}}$ input Low. In this state, the device retains its configuration, even if V_{CC} dips as low as 2.3 V. In powerdown mode, the content of all flip-flops and latches is lost, all outputs are 3-stated, and all inputs are ignored (more specifically, all inputs are considered High, irrespective of the actual input level). During powerdown, the V_{CC} monitoring circuit is disabled, and the device will not detect an accidental V_{CC} drop below 2.0 V that might corrupt the configuration. The assumption is that the battery-backup circuit has no reason to dip below 2.3 V. *See page 8-20 in the 1994 Data Book for a proven battery-back-up circuit.* ◆

Go Ahead... Lock Your Pins (with XC7000 EPLDs)

Many designers prefer to start PC board layout before finishing their designs. This allows PCB and circuit design to be performed in parallel, effectively shortening the lead-time for board delivery, if everything goes well. When using simple PAL devices, designers can confidently assign pins and, as long as the product term budget per macrocell is not exceeded, they are assured their designs will fit when programmed. Only Xilinx XC7000 EPLDs offer the same flexibility in high-density EPLDs.



High-density EPLD devices often include architectural tradeoffs limiting their internal connectability. Some vendors have chosen sparsely populated multiplexing structures to connect signals within their products. As shown in the figure, these EPLD manufacturers present limited connectivity by using restrictive multiplexed signals as inputs to the logic blocks — only specific signals pass to the logic block. The payoff is fast pin-to-pin speed, but at the cost of flexibility. The routing restrictions can ultimately lead to designs with rigidly assigned signals.

Once pins are committed to signals, designs cannot be easily altered. Many times, the PC board must be redesigned to accommodate late changes to the EPLD design. Making changes in these situations completely defeats the advantage gained by early PC board layout. Thus, PAL designers can't use these high-density EPLDs with the same aggressive approach to pre-assigning pin-outs.

In contrast, Xilinx XC7000 series EPLDs easily manage "locked pin" designs. The XC7000 EPLD architecture's Universal Interconnect Matrix (UIM™) can accommodate signal changes within the device. Unlike the sparsely populated connection multiplexers of other vendor's EPLDs, the UIM presents a 100% connectable cross point switch as its connecting environment. All signals enter the UIM, where they can be freely assigned and reassigned to the function block inputs. This permits any signal to enter any function block on the chip, resulting in the ability to make design changes without having to change pins. The payoff is tremendous. Fast time to market and simple field upgrades of existing boards result from this powerful architectural feature.

As an added recommendation, designers that lock pins can manage their function budget to accommodate potential future changes. This is done by spreading the logic among the function blocks in an XC7000 device.

With the Xilinx XC7000 family, following the initial fitting process, designers can maintain their pinouts even while iterating the design. This gives designers a head start on PC board layout, resulting in a time-to-market advantage. ◆

Carry and Overflow: A Short Primer

Whenever two binary numbers are added or subtracted, the result may not fit into the same number of bits. For example, if two 8-bit positive numbers are added and they are both near the top of their number range, nine bits are needed to express the result. If a ninth bit is not available, an error condition must be flagged.

Adder/subtractors often provide carry and overflow outputs to flag such out-of range errors. Which of these flags is used depends on whether signed or unsigned operations are being performed. Overflow is only used with 2's-complement signed numbers, and has no significance in unsigned operations. Carry, on the other hand, is only significant as an error flag in unsigned operations, but is used to cascade both signed and unsigned operations.

Unsigned Operations

Separate out-of-range flags are required since the number ranges are different for signed and unsigned numbers of the same bit-length. In an 8-bit unsigned numbering scheme, for instance, the decimal values 0 through 255 are represented by the hexadecimal codes 00 through FF. This is illustrated on the circular number line shown in Figure 1.

The result of an unsigned addition is out-of-range when it is too far around the number line, such that the 255-to-0 boundary is crossed. Since crossing this boundary causes a carry output, carry can be used to flag the error. The output bits remain valid, but only as the eight less significant bits of a 9-bit result. The full result can be recovered by using the carry output as the MSB of the result. Unsigned subtraction is slightly more complicated, but is rarely encountered.

Signed Operations

When using 2's complement notation for 8-bit signed numbers, however, the hexadecimal codes are assigned differently. The decimal values -128 through 127 are represented by the codes 80 through 7F, as shown in Figure 2.

In this case, a result can be out-of-range in two ways; it can be too positive or too negative. If it is too positive, it is too far around the number line in the counter-clockwise direction, and the 7F-to-80 boundary is crossed. If it is too negative, it is too far around in the clockwise direction and the 80-to-7F boundary is crossed.

Consequently, for 2's-complement numbers, the out-of-range flag must be asserted whenever the 7F-to-80 boundary is crossed in either direction, and this is how the overflow output is defined. For unsigned numbers, however, the 7F-to-80 boundary crossing has no obvious significance.

In an overflowing signed operation, the output bits are again valid as the eight less significant bits of the 9-bit result. However, the MSB of the 9-bit result is not carry or overflow, but the inverse of the eighth bit. This relationship can be exploited to obtain a 9-bit signed result from an 8-bit adder/subtractor. XORing the output MSB with overflow provides the additional bit, as in Figure 3. ◆

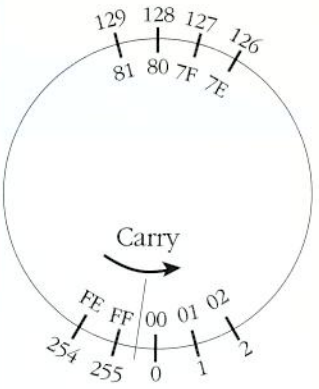


Figure 1: Unsigned Operations

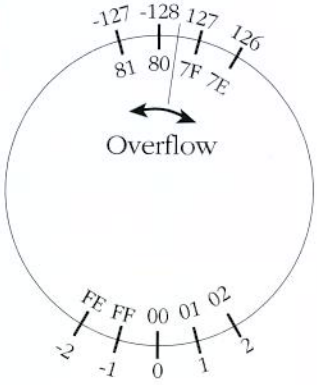


Figure 2: Signed Operations

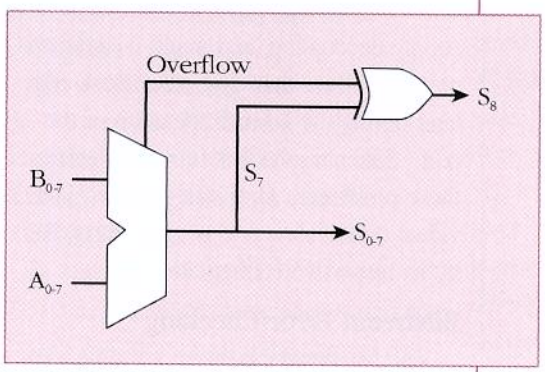


Figure 3: 8-bit signed operation with a 9-bit result.

Take the A-Train ...

(Migrating to the XC3000A and XC3100A)

The XC3000 and XC3100 family FPGAs are now available in improved versions, the XC3000A and XC3100A. All XC3000/XC3100 family users are encouraged to switch over to the enhanced version, even for existing designs.

Obviously, existing designs cannot benefit from the added routing resources in the "A" versions, but they can still take advantage of the other benefits:

"All XC3000/XC3100 users are encouraged to switch over to the enhanced version."

Better Electro-Static Discharge Tolerance

The "A" devices have significantly better ESD protection on their inputs. They can withstand 5,000 V (using the industry-standard human-body model), compared to 2,000 V for the non-A devices. This gives an extra margin of safety, and reduces the chances of damage, especially before and during manufacturing.

Less Ground-Bounce on Start-Up

The "A" devices have the new "Soft Startup" feature. On the first start up after configuration, all outputs will be in slew-rate limited mode (even those configured to be in fast mode). In the XC3000 and XC3100 devices, this first activation of all active outputs can put a heavy load on the supply decoupling, and might create more ground bounce than any other clock edge later during the normal operation of the part. Softening the first turn-on alleviates these problems. After start-up, each individual output slew rate is again controlled by its respective configuration bit.

Bitstream Error-Checking

The "A" devices perform a simple form of bitstream error checking. Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device specific, but each frame in all XC3000 families ends with three stop bits (111) followed by the start bit (0) for the following frame.

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. XC3000/XC3100 devices do not check the trailing stop bits, but XC3000A/XC3100A devices check whether the last three bits of any frame are actually 111, and whether they are followed by a 0 start bit.

Under normal circumstances, all the XC3000 families behave the same way; however, if the bitstream is corrupted, an XC3000/XC3100 device will start a new frame, once it encounters any 0 after the end of a frame, even if the data is completely wrong or out-of-sync. Given enough zeros in the data stream, the device will also go DONE, but with incorrect configuration and the possibility of internal contentions, causing high power consumption.

An XC3000A/XC3100A device starts a new frame only if the three trailing bits of the previous frame are 111, directly followed by the leading start bit 0. If this check fails for any reason, $\overline{\text{INIT}}$ is pulled Low and the configuration process is stopped, although the Master CCLK keeps running. The user must recognize this and initiate a new configuration by applying an active Low level on RESET for at least 6 µs.

RESET Filtering

A separate modification slows down the RESET input until configuration is complete. This delay mechanism uses a 2-bit shift register clocked by the internal oscillator. Microsecond High spikes on RESET

See A TRAIN, next page

Truth Table for XC17000 Control Inputs

The table below assumes RESET is active High. Please note that RESET/$\overline{OE}$ has programmable polarity (except the XC1736A). Chip Enable ($\overline{CE}$) is always active low.

Control Inputs		Internal Address	Outputs		I_{CC}
RESET/$\overline{OE}$	**$\overline{CE}$**		**DATA**	**$\overline{CEO}$**	
Low	Low	if address TC: increment if address >TC : don't change	active 3-stated	High Low	active reduced
High	Low	being held reset	3-stated	High	active
Low	High	not changing	3-stated	High	standby
High	High	being held reset	3-stated	High	standby

In normal use, **CLK** is driven from the CCLK source, and **DATA** is connected to DIN of the lead LCA.

In an XC17000 daisy-chain, all CLK inputs are interconnected, all DATA outputs are interconnected, and each **$\overline{CEO}$** output is connected to the **$\overline{CE}$** input of the next downstream XC17000.

The **$\overline{CE}$** input of the lead (or only) XC17000 device is either driven by the $\overline{LDC}$ of the lead LCA or by its D/P pin (XC2000/3000 families) or the DONE pin (XC4000 families). Using $\overline{LDC}$ for this purpose means that this pin must be unconditionally High, therefore making it useless during user operation. Driving $\overline{CE}$ from D/$\overline{P}$ does not sacrifice a user pin, but means that D/$\overline{P}$ cannot be permanently grounded.

The XC17000 RESET/$\overline{OE}$ pin has programmable polarity (except the XC1736A). It should be active during power-up, and it must be activated by the reconfigure input. It is common practice to drive the LCA and SPROM RESET lines together. ◆

A Train

Continued from previous page

will thus not inadvertently start a configuration. As before, microsecond Low pulses on RESET will not instigate a configuration abort either.

This delay of the internal RESET also allows the use of active Powerdown prior to configuration. When the $\overline{PWRDWN}$ input is active (Low), all other inputs are unconditionally interpreted as High and the internal oscillator is stopped. When $\overline{PWRDWN}$ goes High, the delayed sensing of RESET ensures that the mode and RESET inputs have stabilized before they are interpreted. This also simplifies the "Shorter Power-On Delay" solution described in *XCELL #8*.

How to change from XC3000 to XC3000A or from XC3100 to XC3100A

The simplest change is to just plug in the "A" part. The XC3000A-7 is slightly faster than the XC3000-100, while the XC3000A-6 is slightly faster than the XC3000-125.

In moving from the XC3100 to the XC3100A, the speed nomenclature did not change, but there is an improvement in the IOB input flip-flop set-up time. The XC3100A devices are a few ns faster, and these set-up time values are now specified differently for different device sizes, because the XC3100A design compensates for the increased clock delay in the larger parts. The result is a shorter pin-to-pin input set-up time that is practically constant for different device sizes. This change always results in a better set-up time value. ◆

XACT 5.0 Memory Requirements

The table below gives the XACT 5.0 RAM requirements in kilobytes when running the XACT Design Editor on a PC. This is the minimum amount of memory which must be available to the XACT Design Editor when it starts up. The actual physical memory size must be larger, since it might also be used by XDM, device drivers, RAM disk, Windows, and other utilities, before XACT 5.0 is loaded.

Note that the amount of memory required for the smallest LCAs has gone up. This is due to the increased executable size and the increased size of the runtime stack, which is now 768K bytes.

	-p command line option not used default panning buffer			-p command line option used panning buffer = screen size		
Device	**VGA4**	**VGA8**	**VGA16**	**VGA4**	**VGA8**	**VGA16**
XC2064	3066K	3400K	3734K	2176K	2326K	2476K
XC2018	3403K	3836K	4268K	2293K	2444K	2594K
XC3020	4032K	4679K	5327K	2483K	2634K	2785K
XC3030	4788K	5700K	6612K	2717K	2868K	3019K
XC3042	5685K	6888K	8091K	2995K	3146K	3297K
XC3064	7300K	9058K	10817K	3496K	3647K	3799K
XC3090	9200K	11574K	13949K	4082K	4234K	4386K
XC3195	12300K	15765K	19230K	5046K	5197K	5348K
XC4003	5734K	6456K	7178K	4048K	4198K	4348K
XC4005	8023K	9193K	10363K	5429K	5581K	5732K
XC4006	9385K	10836K	12287K	6246K	6397K	6547K
XC4008	10912K	12647K	14382K	7166K	7316K	7467K
XC4010	12596K	14676K	16755K	8184K	8334K	8485K
XC4013	16442K	19271K	22101K	10515K	10666K	10816K
XC4002A	4154K	4564K	4975K	3090K	3240K	3391K
XC4003A	4835K	5391K	5946K	3511K	3661K	3812K
XC4004A	5647K	6343K	7040K	4003K	4154K	4304K
XC4005A	6560K	7434K	8309K	4568K	4718K	4869K
XC4003H	5923K	6687K	7452K	4175K	4325K	4476K
XC4005H	8278K	9506K	10734K	5589K	5740K	5890K

When the -p option is not in effect, the XACT Design Editor tries to size the large panning buffer to be big enough to draw the entire die at Xlarge In. If the panning buffer cannot be allocated to be that large, the Design Editor will retry the allocation until a buffer is obtained, cutting its size in half in each dimension with each retry. Thus each retry will ask for 1/4 the amount of memory previously asked for the panning buffer.

The -p command line option tells the XACT Design Editor to make the panning buffer only as large as the screen. In this case, any panning activity causes a redraw of the buffer, but this small buffer is redrawn very fast, and its size is device-independent.

Note that the -p option has several sub-options to set the size of the panning buffer to any reasonable value. This gives the user control of the tradeoff between the frequency of redraws, the time per redraw, and the ability to pan without redraw. ◆

The 1994 Data Book is Here

The *1994 Xilinx Data Book* was printed in late February. It is a revision of the *1993 Data Book*, with 72 pages added, and almost half the pages improved in some way.

New Information:

- The **XC4025**, the world's biggest FPGA, was added. Pin-outs on page 2-66/67.
- The **XC4010D**, the RAM-less version of the XC4010, is described on pages 2-69/70.
- In the 1993 Data Book, the timing parameters for several devices, were left blank; this information is now included for the **XC4000-4, XC3000A, XC3000L,** and **XC2000L.**
- The **XC3100A** family was added, see pages 2-177 through 184.
- The **XC7336** and **XC7354** EPLD Product Specifications were added, as well as advance information on the **XC73144**. See section 3.
- Section 4 has package drawings for **VO8, CB100, CB164, TQ176, CB196, BG225, PG299.**
- Section 7 has a better introduction, describes the features of the new **XACT 5** release, and introduces Xilinx software on **CD-ROMs.**
- The applications section adds detailed information on **XC4000 output characteristics** and their affect on **ground bounce** on pages 8-6 through 10.
- Pages 8-21 through 35 describe methods to **improve XC4000 design performance.**
- Two new application notes describe a simple, rugged, and reliable way to implement **RAM**, **shift registers**, and **FIFOs** in the XC4000 , on pages 8-139 through 147.

Improvements:

- Xilinx part numbers are explained on page 1-8.
- Pin-to-pin timing is explained on page 2-6.
- The five XC3000 subfamilies are compared on page 2-152.
- XC4000 configuration modes are described in more detail and more clearly, with detailed explanations for configuration delay after power-up (2-32, 34, 36, 38, 40).
- The XC4000 configuration flow chart is improved.
- Serial PROMs now list all device sizes and add a "Zero Idle Current" application.
- Packages distinguish clearly between inches and mm, as explained on page 4-1.
- Cavity up/down, pin direction and pin #1 location is explained specifically (4-2).
- CB100 and CB164 drawings show the pin-out differences between XC3000 and XC4000.
- Thermal resistances are listed in an easy-to-read table (4-26/27)
- Reflow Soldering Process Guidelines are added for plastic surface-mount components.
- Quality and Reliability data is brought up-to-date, (pages 5-1 through 6).
- The training courses are explained in more detail, (pages 6-6/7).
- App. notes are listed in numeric order (page 8-0) and then described in functional order.
- The Best of XCELL adds a simple RC oscillator, and a ROM design on page 9-22.
- The address list of our 12 Xilinx sales offices and 173 rep locations is brought up-to-date.

1994 Data Book Errata:

2-26 XC4013 got accidentally deleted from the table in fig 19. See the 1993 Data Book.

2-26: # of frames in XC40004A is 438, not 435.

2-40 Top of right column: D0 ... D6 go uncondionally High (not Low).

2-43 Data 4 fell off Master Low mode. Obvious error.

2-101 L3 = 205 = Boundary Scan 56, L15 = 99 = Boundary Scan 385

2-139 XC3030-84 pin: 14 u, not nc.

2-140 VQ64 pin 18 is TCLKIN-I/O

2-165 TCKO for 3000-6 is 4.0 ns, not 3.5 ns

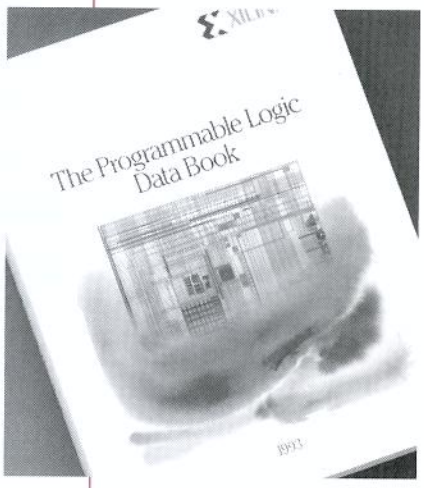
2-191 Figure 5, option 3 should have its two B inputs deleted

2-236/7 ICCS is 0.5 mA for 17128 only, 1.5 mA for all D and L parts.

4-24 left edge letter sequence is wrong: I must be deleted, and V inserted

8-18 CCLK Variation, middle para, 2nd line: "... to - 50%", (not -10%)

8-111 Top Overflow equation: one of the two factors must be CN, not N-1 ◆



General

Q: Where can I find the list of device socket vendors who support Xilinx package types?

A: See page 4-32 of the 1994 Databook.

Q: In general, what elements of the Xilinx architecture can be assigned location constraints?

A: Consult the APR or PPR documentation for specific details, but below are some general ideas.

XC2000 and XC3000 families:

1. Location constraints may be applied to flip flops, CLBMAPs, CLBs, TBUFs and I/O elements.

XC4000 families:

1. Location constraints may be applied to flip flops, edge decoders, FMAPs, HMAPs, TBUFs, and I/O elements.
2. The global buffers (BUFGP, BUFGS) should only be constrained to "corners" of the die and NOT to specific pins. For example, to constrain a global buffer to the top, left corner of the die, use "LOC=TL".

Q: I am using a Data I/O programmer. Please clarify the reset locations for your PROM devices.

A: The "D" series and the new low power "L" series devices contain programmable reset locations, while the older XC1736A has active High reset only. The table below summarizes the reset locations.

DEVICE	ADDRESS (HEX)
1718D/L	8DC - 8DF
1736D	11B8 - 11BB
1765D/L	2000 - 2003
17128	4000 - 4003

To program active High reset, fill these address locations with ones and to program active Low reset, fill these address locations with zeroes. *(Please note that these locations are the logical addresses used by Data I/O and are not necessarily the physical address locations. See XCell #11, page 30.)*

Q: How can I copy the contents of a XC1765 Serial PROM into an XC1765D?

A: Enter the XPP program, set the device type to 1765, specify the output file name, and read the 1765 device contents using the PROM Programmer. The output filename will have a .txt extension. Rename the file with a .rbt extension, set the device type to 1765D, place a 1765D device in the programmer, and program the device with the .rbt file.

Mentor Graphics

Q: I have recently converted my design from Mentor V7 to Mentor V8. However, I am having problems with the VCC and GND symbols converting correctly. What can I do?

A: Some background information will be helpful in explaining this issue. When Xilinx developed the Mentor V7 interface (DS343 v4.10), the ground symbol was copied from Mentor's gen_lib, and, therefore, it contained CLASS and INIT properties with no underlying schematic. However, when Xilinx developed the Mentor V8 interface (DS344 v1.10), the CLASS and INIT properties were removed and an underlying schematic was created. This was done to work around an issue within the Mentor environment. Thus, all you need to do is to delete the CLASS and INIT properties from the VCC and GND symbols in your converted schematic.

Synopsys

Q: When running SYN2XNF, I receive an error similar to the following. I have installed the DS-502 software and I am confident that my PATH and XACT variables are set correctly. What is wrong?

```
@ (#) SYN2XNF Version 3.40 6/30/93 16:39:37
©1992, 1993 Xilinx Inc. All rights reserved.
LCANET, 4
INFO:   Using part type 4005PC84-5
ERROR:  Unable to find the file "partlist.xct" in
        your XACT path.
ERROR:  Unable to find the file "speeds.xct" in
        your XACT path.
```

A: Three files are missing: partlist.xct, speeds.xct, and xnfmerge. For Sun customers, these files are contained in the file "ds401sn2.tar", which can be downloaded from the Xilinx Technical Bulletin Board (see page 6-2 in the 1994 Databook for Bulletin Board instructions). Hewlett Packard (HP700) customers should contact Xilinx Technical Support.

OrCAD

Q: How do I specify attributes such as "FAST", "NODELAY", etc. in my OrCAD schematic?

A: For XC2000 and XC3000 families, select "Edit-Edit-LOC,options-Name", then type ",attribute_name".

For example, to specify the "FAST" attribute to a pad, select "Edit-Edit-LOC,options-Name", then type ",FAST". The comma must be included.

For XC4000 families, select "Edit-Edit-Options_1" (or you may select "Edit-Edit-Options_2" as Options_1 and Options_2 are interchangeable), then type "attribute_name". For example, to specify a divide by 5 attribute to an XBLOX counter, select "Edit-Edit-Options_1" , then type "DIVIDE_BY=5".

Viewlogic

Q: I am attempting to simulate my design within Viewsim, but all of my flip flop outputs are unknown. Why?

A: The XC2000, XC3000, and XC4000 families have a dedicated metal trace that is used as a global reset of all flip flops on the device. This signal requires special care within the Viewsim environment as detailed below:

XC2000, XC3000: The active Low signal name is "GR" or "globalreset-". It must be asserted before simulation begins to avoid unknown values.

For example,

```
SIM> restart
SIM> l gr
SIM> cycle
SIM> h gr
SIM> ....(next command)
```

XC4000: The active High signal name is "GSR". As with the XC2000/XC3000 families, it must be asserted before simulation begins to avoid unknown values. When asserted, it will either set or reset the flip flops depending on their type, i.e. FDRD flip flops are reset, while FDSD flip flops are set.

For example,

```
SIM> restart
SIM> h gsr
SIM> cycle
SIM> l gsr
SIM> ....(next command) ◆
```

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