Winbond Electronics Corp.

STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

W83194BR-B
Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

1. GENERAL DESCRIPTION

The W83194BR-B is a Clock Synthesizer for Intel Brookdale 845 chipset. W83194BR-B provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, 3V66 clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-B provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% and +/-0.25% center type spread spectrum or programmable S.S.T. scale to reduce EMI.

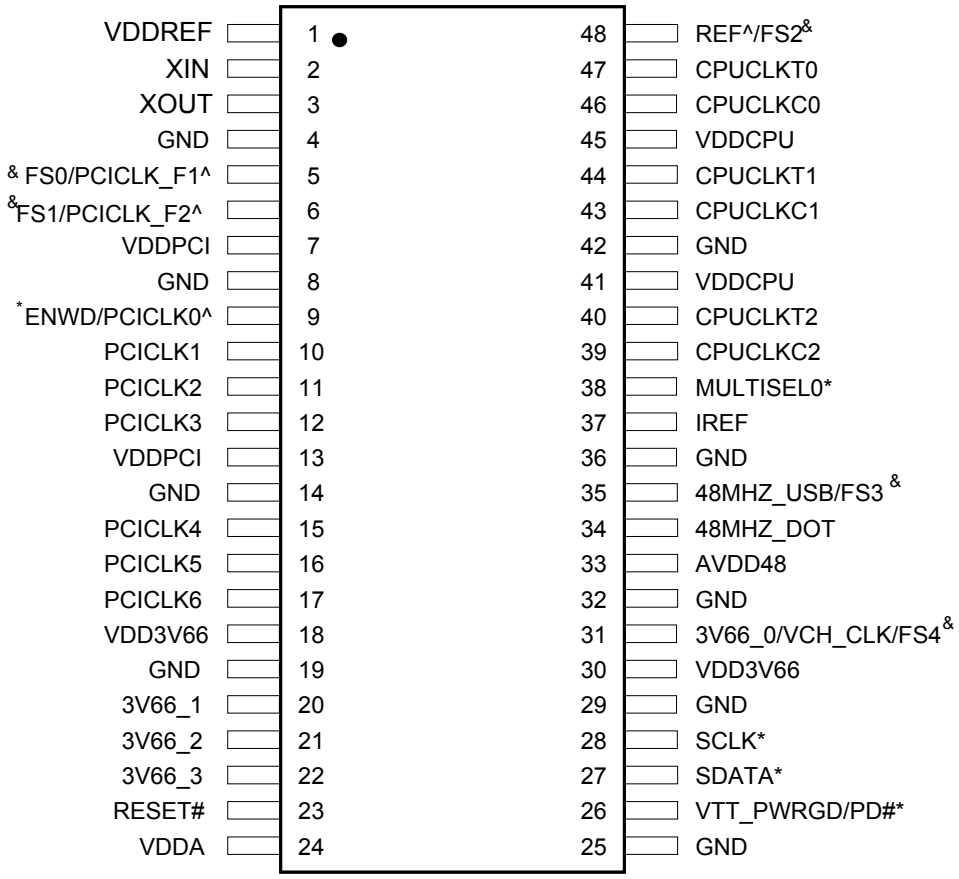
The W83194BR-B also has watch dog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-B accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF and 48 MHz provide better than 0.5V /ns slew rate.

2. PRODUCT FEATURES

- 3 pairs of CPU clock outputs
- 4 3V66 clock outputs
- 9 PCI synchronous clocks
- 2 48 MHz clock outputs for USB and DOT
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.6 to 200MHz
- Step-less frequency programming
- I^2C 2-Wire serial interface and I^2C read back
- -0.5% and +/- 0.25% center type spread spectrum
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

3. PIN CONFIGURATION



#: Active low
^: These outputs have 1.5 ~ 2X drive strength
*: Internal pull up resistor 120K to VDD
&: Internal Pull-down resistor 120K to GND

4. PIN DESCRIPTION

IN – Input

IN_{td120k} – Input

OUT – Output

OD – Open Drain

I/O - Bi-directional Pin

I/OD - Bi-directional Pin, Open Drain

- Active Low

* - Internal 120kΩ pull-up

& - Internal 120kΩ pull-down

^ - 1.5X~2X strength

4.1. Crystal I/O

PIN	SYMBOL	I/O	FUNCTION
3	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
4	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

4.2. CPU, 3V66, and PCI Clock Outputs

<table>
<tr><th>PIN</th><th>SYMBOL</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>47, 46, 44, 43, 40, 39</td><td>CPUCLKT [0:2]
CPUCLKC [0:2]</td><td>OUT</td><td>Low skew (< 250ps) differential clock outputs for host frequencies of CPU and chipset</td></tr>
<tr><td>38</td><td>MULTISEL0*</td><td>IN</td><td>Power on trapping for different current reference. The reference current is referred for Pin 37 (IREF). This pin is latched during VTT_PWRGD. This pin is internal pull up 120K.</td></tr>
<tr><td>37</td><td>IREF</td><td>IN</td><td>Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. There are two mode to select different current via power on trapping the Pin 38 (MULTISEL0). The table is show as follows.
<table>
<tr><th>MULTSEL0</th><th>Board Target Trace</th><th>Reference R, Iref</th><th>Output Current</th><th>Ioh @ Z</th></tr>
<tr><td>0</td><td>50 Ohms</td><td>R=221
Iref=5.0mA</td><td>Ioh=4*Iref</td><td>1.0V @ 50</td></tr>
<tr><td>1</td><td>50 Ohms</td><td>R=475
Iref=232mA</td><td>Ioh=6*Iref</td><td>0.7V @ 50</td></tr>
</table>
</td></tr>
<tr><td>23</td><td>RESET#</td><td>OD</td><td>System reset signal when the watch dog is time out. This pin will</td></tr>
</table>

			generate 250mS when the watchdog timer is timeout.
26	VTT_PWRGD	IN	Power good input signal comes from ACPI with high active. This 3.3V input is level sensitive strobe used to determine FS[4:0] and MULTISEL0 input are valid and is ready to sampled. This pin is high active.
	PD#*	IN	Power Down Function. This is internal 120K pull up. This is multi-function pin. When the VTT_PWRGD signal is asserted (this is, turns from a logical Low to high), the pin will be switched into the function of power down (PD#).
31	3V66_0	OUT	66MHz or 48MHz outputs selected by I2C register.
	VCH_CLK	OUT	
	FS4&	IN_{td120k}	Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU 3V66 and PCI clocks. This is internal 120K pull down.
5	PCICLK_F1^	OUT	3.3V free running PCI clock during normal operation. This pin is with x1.5 ~ x2 driving strength.
	FS0&	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, 3V66 and PCI clocks. This is internal 120K pull down.
6	PCICLK_F2^	OUT	3.3V free running PCI clock outputs. This pin is with x1.5 ~ x2 driving strength.
	FS1&	IN_{td120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, 3V66 and PCI clocks. This is internal 120K pull down.
9	PCICLK0^	OUT	3.3V free running PCI clock outputs. This pin is with x1.5 ~ x2 driving strength.
	ENWD*	IN	Latched input for ENWD at initial power up for H/W enable the watch dog timer. This is internal 120K pull up.
10, 11, 12, 15, 16, 17	PCICLK[1:6]	OUT	Low skew (< 250ps) PCI clock outputs.
20, 21, 22	3V66_1, 3V66_2, 3V66_3	OUT	3.3V output clocks for the chipset.

4.3. I^2C Control Interface

Pin Number	Pin Name	Type	Description
27	SDATA*	I/OD	Serial data of I^2C 2-wire control interface with internal pull-up resistor.
28	SCLK*	IN	Serial clock of I^2C 2-wire control interface with internal pull-up resistor.

4.4. Fixed Frequency Outputs

PIN	SYMBOL	I/O	FUNCTION
48	REF^	OUT	14.318NHz output. This pin is with x1.5 ~ x2 driving strength.
	FS2&	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, 3V66 and PCI clocks. This is internal 120K pull down.
34	48MHz_DOT	OUT	48MHz clock output for DOT.
35	48MHz_USB	OUT	48MHz clock output for USB.
	FS3&	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. This is internal 120K pull down.

4.5. Power Pins

Pin Number	Pin Name	Type	Description
1,	VDDREF	PWR	3.3V power supply for REF.
7, 13	VDDPCI	PWR	3.3V power supply for PCI.
18, 30	VDD3V66	PWR	3.3V power supply for 3V66.
41, 45	VDDCPU	PWR	3.3V power supply for CPU.
24	VDDA	PWR	3.3V power supply for analog core.
33	AVDD48	PWR	Analog power 3.3V for 48M Hz
4, 8, 14, 19, 25, 29, 32, 36, 42	GND	PWR	Ground pin for 3.3 V

5. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS[4:0] value or software programming at SSEL[4:0] (Register 1 bit 6 ~ 2).

FS4	FS3	FS2	FS1	FS0	CPU(MHZ)	3V66(MHZ)	PCI(MHz)	Spread %
0	0	0	0	0	100.90	67.27	33.63	+/-0.25%
0	0	0	0	1	100.30	66.87	33.43	-0.5%
0	0	0	1	0	103.00	68.67	34.33	+/-0.25%
0	0	0	1	1	105.00	70.00	35.00	+/-0.25%
0	0	1	0	0	107.00	71.33	35.67	+/-0.25%
0	0	1	0	1	109.00	72.67	36.33	+/-0.25%
0	0	1	1	0	111.00	74.00	37.00	+/-0.25%
0	0	1	1	1	114.00	76.00	38.00	+/-0.25%
0	1	0	0	0	117.00	78.00	39.00	+/-0.25%
0	1	0	0	1	120.00	80.00	40.00	+/-0.25%
0	1	0	1	0	127.00	84.67	42.33	+/-0.25%
0	1	0	1	1	130.00	86.67	43.33	+/-0.25%
0	1	1	0	0	133.33	88.89	44.44	+/-0.25%
0	1	1	0	1	170.00	56.67	28.33	+/-0.25%
0	1	1	1	0	180.00	60.00	30.00	+/-0.25%
0	1	1	1	1	190.00	63.33	31.67	+/-0.25%
1	0	0	0	0	133.90	66.95	33.48	+/-0.25%
1	0	0	0	1	133.33	66.67	33.33	-0.5%
1	0	0	1	0	120.00	60.00	30.00	+/-0.25%
1	0	0	1	1	125.00	62.50	31.25	+/-0.25%
1	0	1	0	0	134.90	67.45	33.73	+/-0.25%
1	0	1	0	1	137.00	68.50	34.25	+/-0.25%
1	0	1	1	0	139.00	69.50	34.75	+/-0.25%
1	0	1	1	1	141.00	70.50	35.25	+/-0.25%
1	1	0	0	0	143.00	71.50	35.75	+/-0.25%
1	1	0	0	1	145.00	72.50	36.25	+/-0.25%
1	1	0	1	0	150.00	75.00	37.50	+/-0.25%
1	1	0	1	1	155.00	77.50	38.75	+/-0.25%
1	1	1	0	0	160.00	80.00	40.00	+/-0.25%
1	1	1	0	1	170.00	85.00	42.50	+/-0.25%
1	1	1	1	0	66.67	66.67	33.34	+/-0.25%
1	1	1	1	1	200.00	66.67	33.33	+/-0.25%

6. I²C CONTROL AND STATUS REGISTERS

6.1. Register 1: Frequency Select Register (default = 0)

Bit	Name	PWD	Description
7	EN_SPSP	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum enabled
6	SSEL[4]	0	Frequency selection by software via I²C.
5	SSEL[3]	0	
4	SSEL[2]	0	
3	SSEL[1]	0	
2	SSEL[0]	0	
1	EN_SSEL	0	Enable software program FS[4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I²C - Bit 6 ~ 2.
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS[4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 6 bit 4~0.

6.2. Register 2: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	Pin #	PWD	Description
7	47, 46	1	CPUCLKT2 / C2
6	44, 43	1	CPUCLKT1 / C1
5	40, 39	1	CPUCLKT0 / C0
4	-	X	FS[4] Read back.
3	-	X	FS[3] Read back
2	-	X	FS[2] Read back
1	-	X	FS[1] Read back
0	-	X	FS[0] Read back

6.3. Register 3: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	Pin #	PWD	Description
7	-	X	MULTISEL0 trapping pin data read back
6	17	1	PCICLK 6
5	16	1	PCICLK 5
4	15	1	PCICLK 4
3	12	1	PCICLK 3
2	11	1	PCICLK 2

1	10	1	PCICLK 1
0	9	1	PCICLK 0

6.4. Register 4: PCI, 48MHz Clock Register (1 = enable, 0 = Stopped)

Bit	Pin #	PWD	Description
7	34	1	48MHZ_DOT
6	35	1	48MHZ_USB
5	48	1	REF
4	-	1	Reserved
3	EN_VCH_CLK	0	1 = VCH_CLK 48MHz clock output. 0 = 3V66_0 66MHz clock output (default).
2	-	1	Reserved
1	6	1	PCICLK_F1
0	5	1	PCICLK_F0

6.5. Register 5:3V66 Control Register (1 = enable, 0 = Stopped)

Bit	Pin #	PWD	Description
7	-	1	Reserved
6	-	1	Reserved
5	-	1	Reserved
4	-	1	Reserved
3	22	1	3V66_3
2	21	1	3V66_2
1	20	1	3V66_1
0	31	1	3V66_0/VCH_CLK

6.6. Register 6: Watchdog Control Register

Bit	Name	PWD	Description
7	Reserved	0	Reserved
6	EN_WD	X	Enable Watchdog Timer if set to 1. Set to 0, disable watchdog timer. This bit is trapping pin during VTT_PWRGD#. Read this bit will return a counting state. If timer continue down count, this bit will return 1. Otherwise, this bit will return 0.
5	WD_TIMEOUT	0	Watchdog Timeout Status. If the watchdog is started and timer down count to zero, this bit will be set to 1. Clear this bit to logic 0, If set to 1, when the watchdog is restart in the next time. This bit is Read Only.
4	SAF_FREQ[4]	0	Watchdog safe frequency bits. These bits will be reload into FS[4:0], if the watchdog is timeout and enable reload safe frequency bits.
3	SAF_FREQ[3]	0	

2	SAF_FREQ[2]	0	
1	SAF_FREQ[1]	0	
0	SAF_FREQ[0]	0	

6.7. Register 7: Watchdog Timer Register

Bit	Name	PWD	Description
7	WD_TIME[7]	0	Watchdog timeout time. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If the watchdog timer is start, this register will be down count. Read this register will return a down count value.
6	WD_TIME[6]	0	
5	WD_TIME[5]	0	
4	WD_TIME[4]	0	
3	WD_TIME[3]	1	
2	WD_TIME[2]	0	
1	WD_TIME[1]	0	
0	WD_TIME[0]	0	

6.8. Register 8: M/N Program Register

Bit	Name	PWD	Description
7	N_DIV[8]	0	Programmable N divisor value. Bit 7 ~0 are defined in the Register 9.
6	TEST1	1	Test bit 1. Winbond test bit, do not change them.
5	TEST0	0	Test bit 0. Winbond test bit, do not change them.
4	M_DIV[4]	0	Programmable M divisor value.
3	M_DIV[3]	0	
2	M_DIV[2]	0	
1	M_DIV[1]	0	
0	M_DIV[0]	0	

6.9. Register 9: M/N Program Register

Bit	Name	PWD	Description
7	N_DIV[7]	0	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 8.
6	N_DIV[6]	0	
5	N_DIV[5]	0	
4	N_DIV[4]	0	
3	N_DIV[3]	0	
2	N_DIV[2]	0	
1	N_DIV[1]	0	

0	N_DIV[0]	0	

6.10. Register 10: Spread Spectrum Programming Register

Bit	Name	PWD	Description
7	SP_UP[3]	0	Spread Spectrum Up Counter bit 3.
6	SP_UP[2]	0	Spread Spectrum Up Counter bit 2.
5	SP_UP[1]	0	Spread Spectrum Up Counter bit 1.
4	SP_UP[0]	1	Spread Spectrum Up Counter bit 0
3	SP_DOWN[3]	1	Spread Spectrum Down Counter bit 3
2	SP_DOWN[2]	1	Spread Spectrum Down Counter bit 2
1	SP_DOWN[1]	1	Spread Spectrum Down Counter bit 1
0	SP_DOWN[0]	1	Spread Spectrum Down Counter bit 0

6.11. Register 11: Divisor and Step-less Enable and Skew Control Register

Bit	Name	PWD	Description
7	EN_MN_PROG	0	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**. When the watchdog timer is timeout, this will be clear. In this time, the frequency is set to hardware default latched or safe frequency set by EN_SFAE_FREQ (Register 1 bit 0).
6	Reserved	0	Reserved
5	RATIO_SEL[2]	0	CPU, 3V66, and PCI ratio selection. The ratio is shown as following table.
4	RATIO_SEL[1]	0	
3	RATIO_SEL[0]	0	
2	CPU_3V66_SKEW [2]	1	CPU to 3V66 skew.
1	CPU_3V66_SKEW [1]	0	
0	CPU_3V66_SKEW [0]	0	

Table of CPU, 3V66, and PCI clock selection.

Reg10 Bit5	Reg10 Bit4	Reg10 Bit3	VCO / CPU	VCO / 3V66	VCO / PCI
SEL2	SEL1	SEL0	ratio	ratio	ratio
0	0	0	2	4	4
0	0	1	2	5	5
0	1	0	2	6	6
0	1	1	3	6	4
1	0	0	4	4	2
1	0	1	4	6	3
1	1	0	6	6	2

1	1	1	X	X	X

6.12. Register 12: Winbond Chip ID Register (Read Only)

Bit	Name	PWD	Description
7	CHPI_ID[7]	0	Winbond Chip ID. W83194BR-B is 0x32.
6	CHPI_ID[6]	0	Winbond Chip ID.
5	CHPI_ID[5]	1	Winbond Chip ID.
4	CHPI_ID[4]	1	Winbond Chip ID.
3	CHPI_ID[3]	0	Winbond Chip ID.
2	CHPI_ID[2]	0	Winbond Chip ID.
1	CHPI_ID[1]	1	Winbond Chip ID.
0	CHPI_ID[0]	0	Winbond Chip ID.

6.13. Register 13: Winbond Chip ID Register (Read Only)

Bit	Name	PWD	Description
7	SUB_ID[3]	0	Winbond Sub-Chip ID. The sub-chip ID of W83194BR-B is defined as 0001b.
6	SUB_ID[2]	0	Winbond Sub-Chip ID.
5	SUB_ID[1]	0	Winbond Sub-Chip ID.
4	SUB_ID[0]	1	Winbond Sub-Chip ID.
3	VER_ID[3]	0	Winbond Version ID. The Version ID of W83194BR-B is 0001b.
2	VER_ID[2]	0	Winbond Version ID.
1	VER_ID[1]	0	Winbond Version ID.
0	VER_ID[0]	1	Winbond Version ID.

6.14. Register 81: Winbond Test Register I

Bit	Name	PWD	Description
7:0	TEST_REG1	00h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.

6.15. Register 82: Winbond Test Register II

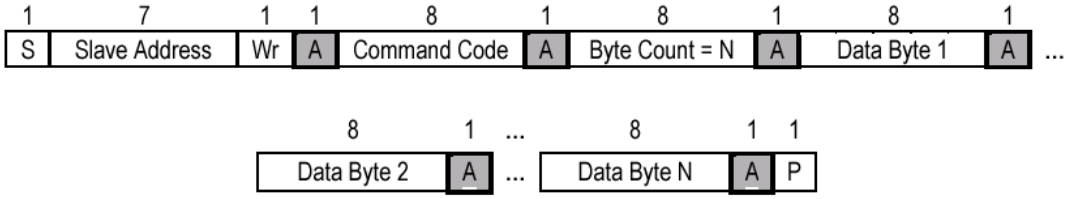
Bit	Name	PWD	Description
7:0	TEST_REG2	04h	Winbond Test Register. User don't write it, otherwise this chip will get an unexpected result.

7. ACCESS INTERFACE

STEPLESS CLOCK FOR INTEL BROOKDALE CHIPSET

The W83194BR-B provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-B is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C address is defined at 0xD2.

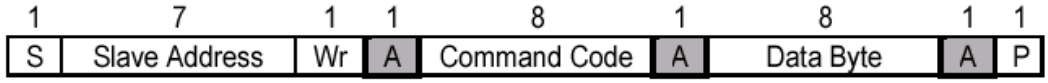
7.1 Block Write protocol



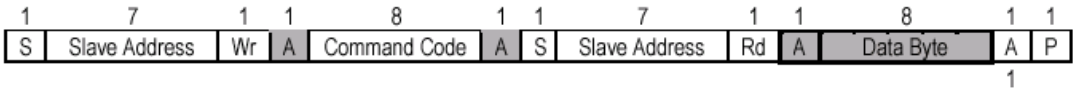
7.2 Block Read protocol

In block mode, the command code must filled 8'h00

7.3 Byte Write protocol



7.4 Byte Read protocol



7.5 The serial bus access timing

(a) Serial bus write to internal address register followed by the data byte

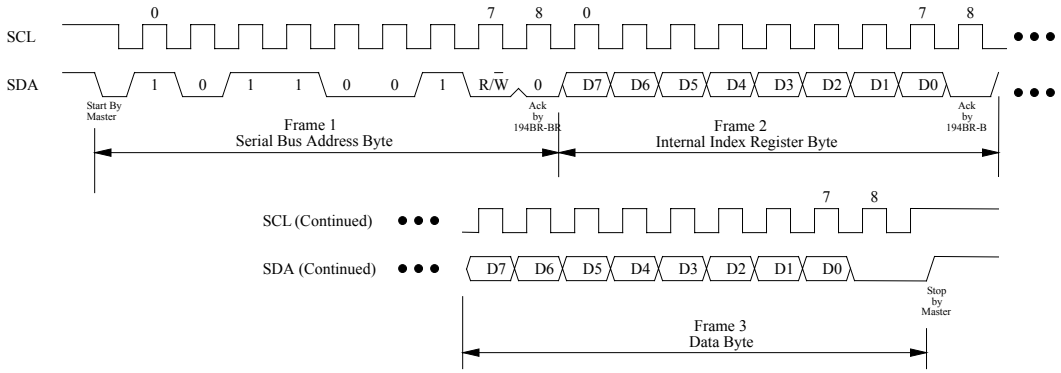


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

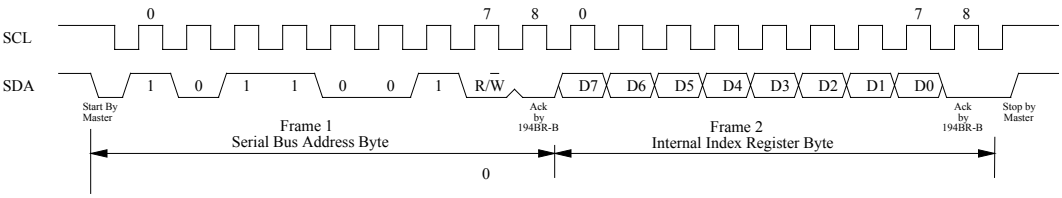


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

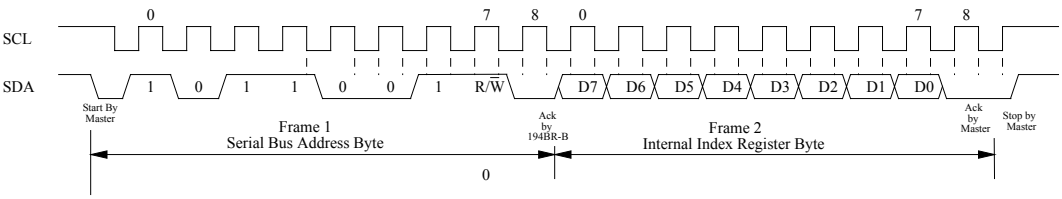


Figure 3. Serial Bus Read from Internal Address Register

(d) Serial bus read from a register with writing to internal address register

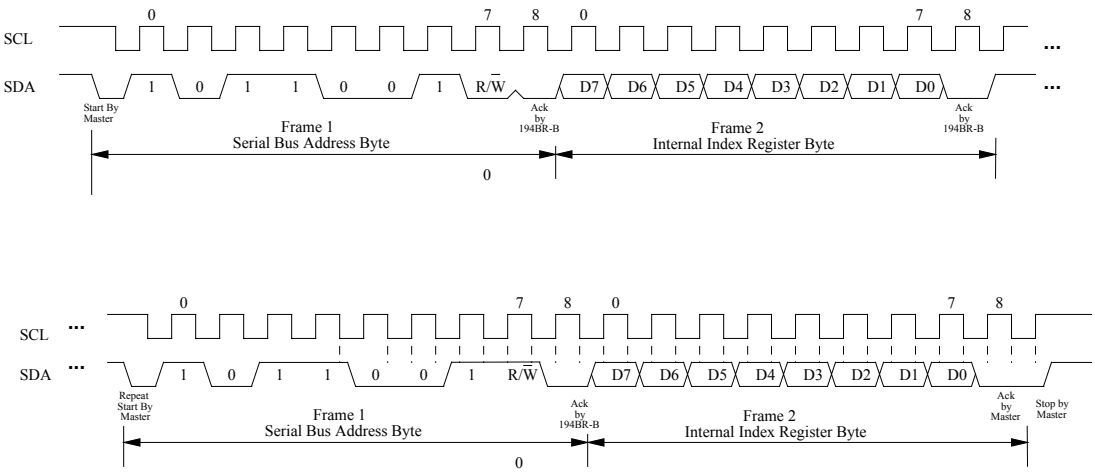


Figure 4. Serial Bus Read from Writing Internal Address Register

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

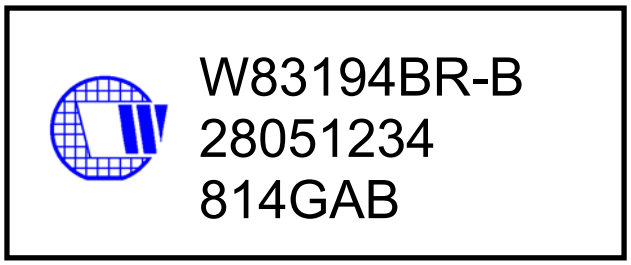
Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

9. ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-B	48 PIN SSOP	Commercial, 0°C to +70°C

10. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-250

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

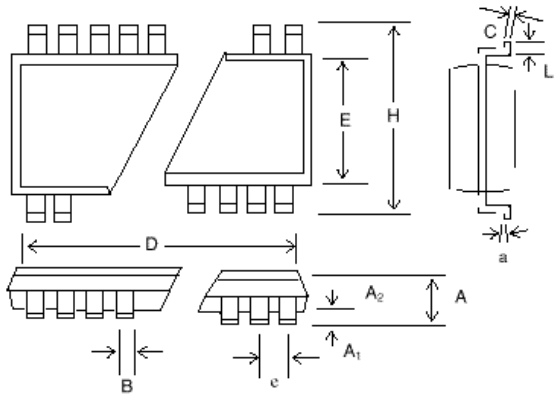
814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

11. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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