The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

The Memory Interface Data Book

for

Design Engineers

1977

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INCORPORATED

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The Memory Interface Data Book

for

Design Engineers

1977

TEXAS INSTRUMENTS
INCORPORATED

LCC4300
74106-47-RS

Printed in U.S.A.

IMPORTANT NOTICES

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Information contained herein supersedes previously published data on Memory Interface Circuits, including data book CC-415.

General Information

1

TABLE OF CONTENTS

*Future product, to be announced

ALPHANUMERIC INDEX

*Future product, to be announced

INTERFACE CIRCUITS INTERCHANGEABILITY GUIDE (MANUFACTURERS ARRANGED ALPHABETICALLY)

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

ADVANCED MICRO DEVICES

EXAMPLE OF NOMENCLATURE

AM	75325	N
Prefix	Device Type	Package Type
		N = Plastic DIP (second source designation for TI Plastic DIP)
		P = Plastic DIP
		J = Ceramic DIP (second source designation for TI Ceramic DIP)
		D = Ceramic DIP

AMD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
AM0026C		SN75369
AM1488	SN75188	
AM1489	SN75189	
AM1489A	SN75189A	
AM26S10C	AM26S10C	
AM26S10M	AM26S10M	
AM26S11C	AM26S11C	
AM26S11M	AM26S11M	
AM5520	SN5520	
AM5521	SN5520	
AM5524	SN5524	
AM5525	SN5524	
AM7520	SN7520	
AM7521	SN7520	
AM7524	SN7524	
AM7525	SN7524	
AM7820A	SN55182	
AM7830	SN55183	
AM7831	DS7831	
AM7832	DS7832	
AM8820A	SN75182	
AM8830	SN75183	
AM8831	DS8831	
AM8832	DS8832	
AM8T26A		SN75136

AMD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
AM9614C	SN75114	
AM9614M	SN55114	
AM9615C	SN75115	
AM9615M	SN55115	
AM55107B	SN55107B	
AM55108B	SN55108B	
AM55109	SN55109A	
AM55110	SN55110A	
AM55234	SN55234	
AM55235	SN55234	
AM55238	SN55238	
AM55239	SN55238	
AM55325	SN55325	
AM75107B	SN75107B	
AM75108B	SN75108B	
AM75109	SN75109A	
AM75110	SN75110A	
AM75207	SN75207	
AM75208	SN75208	
AM75234	SN75234	
AM75235	SN75234	
AM75238	SN75238	
AM75239	SN75238	
AM75325	SN75325	

FAIRCHILD

EXAMPLE OF NOMENCLATURE

75450B	D	C
Device Type	Package Type D = Ceramic DIP P = Plastic DIP R = Ceramic Mini DIP T = Plastic Mini DIP H = Metal Can F = Flat Package	Temperature Range C = Commercial 0°C to 70°C or 75°C M = Military −55°C to 125°C

1

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
μA8T13M	SN55121	
μA8T13C	SN75121	
μA8T14M	SN55122	
μA8T14C	SN75122	
μA8T23C	SN75123	
μA8T24C	SN75124	
μA1488C	SN75188	
μA1489C	SN75189	
μA1489AC	SN75189A	
5524M	SN5524	
5525M	SN5524	
5528M	SN5528	
5529M	SN5528	
5534M		SN55232
5535M		SN55232
5538M		SN55238
5539M		SN55238
7524C	SN7524	
7525C	SN7524	
7528C	SN7528	
7529C	SN7528	
7534C		SN75232
7535C		SN75232
7538C		SN75238
7539C		SN75238
9612C		SN75158
9614M	SN55114	
9614C	SN75114	
9615M	SN55115	
9615C	SN75115	
9616C		SN75188 SN75150
9617C		SN75152 SN75154 SN75189 SN75189A
9626C		SN75136

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
9627C		SN75152
9634C		SN75159
9636C	uA9636C*	
9636M	uA9636M*	
9637C	uA9637C*	SN75157*
9637M	uA9637M*	SN55157*
9638C	uA9638C*	SN75158
9638M	uA9638M*	SN55158
9640C	AM26S10C	
9640M	AM26S10M	
9641C	AM26S11C	
9641M	AM26S11M	
9643		SN75322 SN75363
9644C		SN75361A
9664C	SN75492	
9665AC	SN75466	
9665C	ULN2001A	
9666AC	SN75467	
9666C	ULN2002A	
9667AC	SN75468	
9667C	ULN2003A	
9668AC	SN75469	
9668C	ULN2004A	
55107AM	SN55107A	
55107BM	SN55107B	
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55108BM	SN55108B	
55109M	SN55109A	
55110M	SN55110A	
55121M	SN55121	
55122M	SN55122	
55224M		SN55234
55225M		SN55234
55232M	SN55232	
55233M	SN55232	

*Future product

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
55234M	SN55234	
55235M	SN55234	
55238M	SN55238	
55239M	SN55238	
55325M	SN55325	
55326M	SN55326	
55327M	SN55327	
55450AM	SN55450B	
55450BM	SN55450B	
55451AM	SN55451B	
55451BM	SN55451B	
55452AM	SN55452B	
55452BM	SN55452B	
55453AM	SN55453B	
55453BM	SN55453B	
55454AM	SN55454B	
55454BM	SN55454B	
55460M	SN55460	
55461M	SN55461	
55462M	SN55462	
55463M	SN55463	
55464M	SN55464	
55470M	SN55470	
55471M	SN55471	
55472M	SN55472	
55473M	SN55473	
55474M	SN55474	
75107AC	SN75107A	
75107BC	SN75107B	
75108AC	SN75108A	
75108BC	SN75108B	
75109C	SN75109A	
75110C	SN75110A	
75112C	SN75112	
75121C	SN75121	
75122C	SN75122	
75123C	SN75123	
75124C	SN75124	
75150C	SN75150	
75154C	SN75154	
75207C	SN75207	

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
75208C	SN75208	
75224C		SN75234
75225C		SN75234
75232C	SN75232	
75233C	SN75232	
75234C	SN75234	
75235C	SN75234	
75238C	SN75238	
75239C	SN75238	
75325C	SN75325	
75326C	SN75326	
75327C	SN75327	
75430C	SN75430	
75431C	SN75431	
75432C	SN75432	
75433C	SN75433	
75434C	SN75434	
75450AC	SN75450B	
75450BC	SN75450B	
75451AC	SN75451B	
75451BC	SN75451B	
75452AC	SN75452B	
75452BC	SN75452B	
75453AC	SN75453B	
75453BC	SN75453B	
75454AC	SN75454B	
75454BC	SN75454B	
75460C	SN75460	
75461C	SN75461	
75462C	SN75462	
75463C	SN75463	
75464C	SN75464	
75470C	SN75470	
75471C	SN75471	
75472C	SN75472	
75473C	SN75473	
75474C	SN75474	
75491C	SN75491	
75491AC		SN75491
75492C	SN75492	
75492AC		SN75492

EXAMPLE OF NOMENCLATURE

ITT	75450	–5	D
Prefix	Device Type	Temperature Range –1 = –55°C to 125°C –5 = 0°C to 70°C	Package D = Ceramic DIP N = Plastic DIP

ITT	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
ITT491	SN75491	
ITT492	SN75492	
ITT493	SN75493	
ITT494	SN75494	
ITT1488	SN75188	
ITT1489	SN75189	
ITT1489A	SN75189A	
ITT5520	SN5520	
ITT5521	SN5520	
ITT5522	SN5522	
ITT5523	SN5522	
ITT5524	SN5524	
ITT5525	SN5524	
ITT5528	SN5528	
ITT5529	SN5528	
ITT5534		SN55232
ITT5535		SN55232
ITT7520	SN7520	
ITT7521	SN7520	
ITT7522	SN7522	
ITT7523	SN7522	
ITT7524	SN7524	
ITT7525	SN7524	
ITT7528	SN7528	
ITT7529	SN7528	
ITT7534		SN75232
ITT7535		SN75232
ITT9614	SN75114	
ITT9615	SN75115	
ITT55107A	SN55107A	
ITT55107B	SN55107B	
ITT55108A	SN55108A	
ITT55108B	SN55108B	
ITT55109	SN55109A	
ITT55110	SN55110A	
ITT55138	SN55138	
ITT55234	SN55234	

ITT	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
ITT55235	SN55234	
ITT55324	SN55324	
ITT55325	SN55325	
ITT55450	SN55450B	
ITT55451	SN55451B	
ITT55452	SN55452B	
ITT55453	SN55453B	
ITT55454	SN55454B	
ITT55460	SN55460	
ITT55461	SN55461	
ITT55462	SN55462	
ITT55463	SN55463	
ITT55464	SN55464	
ITT75107A	SN75107A	
ITT75107B	SN75107B	
ITT75108A	SN75108A	
ITT75108B	SN75108B	
ITT75109	SN75109A	
ITT75110	SN75110A	
ITT75138	SN75138	
ITT75207	SN75207	
ITT75208	SN75208	
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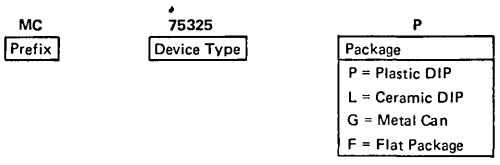
ITT75453	SN75453B	
ITT75454	SN75454B	
ITT75460	SN75460	
ITT75461	SN75461	
ITT75462	SN75462	
ITT75463	SN75463	
ITT75464	SN75464	

MOTOROLA

EXAMPLE OF NOMENCLATURE



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MC8T14	SN75122	
MC8T23	SN75123	
MC8T24	SN75124	
MC8T26		SN75136
MC1411	ULN2001A	
MC1412	ULN2002A	
MC1413	ULN2003A	
MC1416	ULN2004A	
MC1488	SN75188	
MC1489	SN75189	
MC1489A	SN75189A	
MC3443		SN75138
MC3446	MC3446	
MC3453		SN75110A
MC5522	SN5522	
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MC7529	SN7528	
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MC7535		SN75232
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MC7539		SN75238
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MC55108	SN55108A	
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MC75140	SN75140	
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MC75365	SN75365	
MC75368	SN75368	
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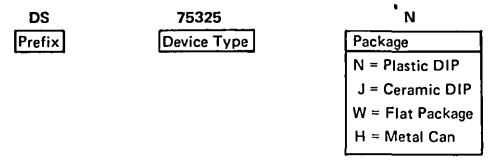
MC75460	SN75460	
MC75461	SN75461	
MC75462	SN75462	
MC75463	SN75463	
MC75464	SN75464	
MC75491	SN75491	
MC75492	SN75492	

NATIONAL

EXAMPLE OF NOMENCLATURE



NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
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DS1489A	SN75189A	
DS1611		SN55471
DS1612		SN55472
DS1613		SN55473
DS1614		SN55474
DS3611		SN75471
DS3612		SN75472
DS3613		SN75473
DS3614		SN75474
DS3629		SN75324
DS5520	SN5520	
DS5520A		SN5520
DS5521	SN5520	
DS5522	SN5522	
DS5522A		SN5522
DS5523	SN5522	
DS5524	SN5524	
DS5524A		SN5524
DS5525	SN5524	
DS5528	SN5528	
DS5528A		SN5528
DS5529	SN5528	
DS5534		SN55232
DS5534A		SN55232
DS5535		SN55232
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DS5538A		SN55238
DS5539		SN55238
DS7520	SN7520	
DS7520A		SN7520
DS7521	SN7520	
DS7522	SN7522	
DS7522A		SN7522
DS7523	SN7522	
DS7524	SN7524	

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
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DS7525	SN7524	
DS7528	SN7528	
DS7528A		SN7528
DS7529	SN7528	
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DS55450	SN55450B	
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DS55452	SN55452B	
DS55453	SN55453B	
DS55454	SN55454B	
DS55460	SN55460	
DS55461	SN55461	

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
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DS55463	SN55463	
DS55464	SN55464	
DS75107	SN75107B	
DS75108	SN75108B	
DS75109	SN75109A	
DS75110	SN75110A	
DS75121	SN75121	
DS75122	SN75122	
DS75123	SN75123	
DS75124	SN75124	
DS75150	SN75150	
DS75154	SN75154	
DS75207	SN75207B	
DS75208	SN75208B	
DS75322	SN75322	
DS75324	SN75324	
DS75325	SN75325	
DS75361	SN75361A	

NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DS75362		SN75365
DS75364	SN75364	
DS75365	SN75365	
DS75450	SN75450B	
DS75451	SN75451B	
DS75452	SN75452B	
DS75453	SN75453B	
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DS75462	SN75462	
DS75463	SN75463	
DS75464	SN75464	
DS75491	SN75491	
DS75492	SN75492	
DS75493	SN75493	
DS75494	SN75494	
DS78LS20		SN55182
DS88LS20		SN75182

SIGNETICS

EXAMPLE OF NOMENCLATURE

75454B
Device Type

V

Package
A = 14 pin Plastic DIP
FH = 14 pin Ceramic DIP
V = 8 pin Plastic DIP
T = 8 pin Metal Can
B = 16 pin Plastic DIP
FJ = 16 pin Ceramic DIP

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
N8T13	SN75121	
N8T14	SN75122	
N8T15		SN75150
N8T16		SN75152
N8T23	SN75123	
N8T24	SN75124	
N8T26		SN75136
N8T26A		SN75136
S8T13	SN55121	
S8T14	SN55122	
DM7820	SN55182	
DM7830	SN55183	
DM8820	SN75182	
DM8830	SN75183	

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DM8880	SN75480	
MC1488	SN75188	
MC1489	SN75189	
MC1489A	SN75189A	
3207A		SN75365
3207A-1		SN75365
7520	SN7520	
7521	SN7520	
7522	SN7522	
7523	SN7522	
7524	SN7524	
7525	SN7524	
55325	SN55325	
55450B	SN55450B	

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
55451B	SN55451B	
55452B	SN55452B	
55453B	SN55453B	
55454B	SN55454B	
75S107		SN75107A
75S108		SN75108A
75S207		SN75207
75S208		SN75208

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
75324	SN75324	
75325	SN75325	
75361A	SN75361A	
75450B	SN75450B	
75451B	SN75451B	
75452B	SN75452B	
75453B	SN75453B	
75454B	SN75454B	

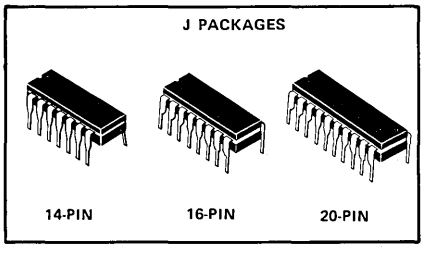
Thermal Information

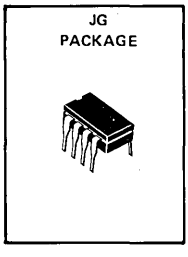
2

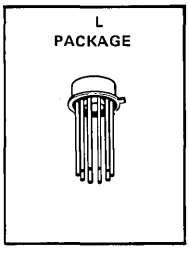
THERMAL RESISTANCE

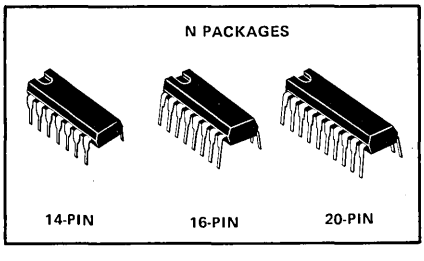
PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$ (°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)
J ceramic dual-in-line (glass-mounted chips)	14 thru 20	60	122
J ceramic dual-in-line† (alloy-mounted chips)	14 thru 20	29†	91†
JG ceramic dual-in-line (glass-mounted chips)	8	58	151
JG ceramic dual-in-line† (alloy-mounted chips)	8	26†	119†
L plug-in	10	51	195
N plastic dual-in-line	14 thru 20	44	108
P plastic dual-in-line	8	45	125

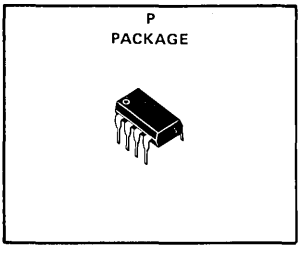
† In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883" have alloy-mounted chips.







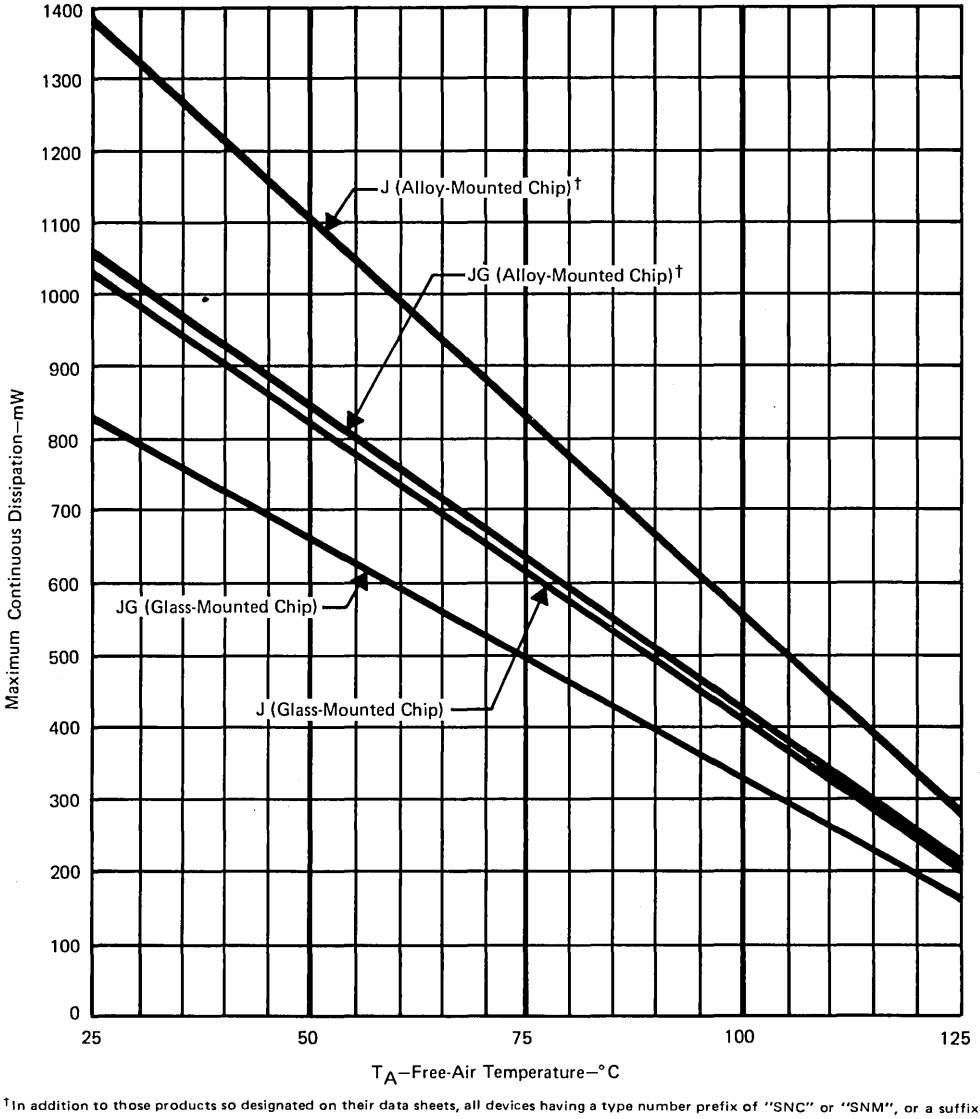




CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883" have alloy-mounted chips.

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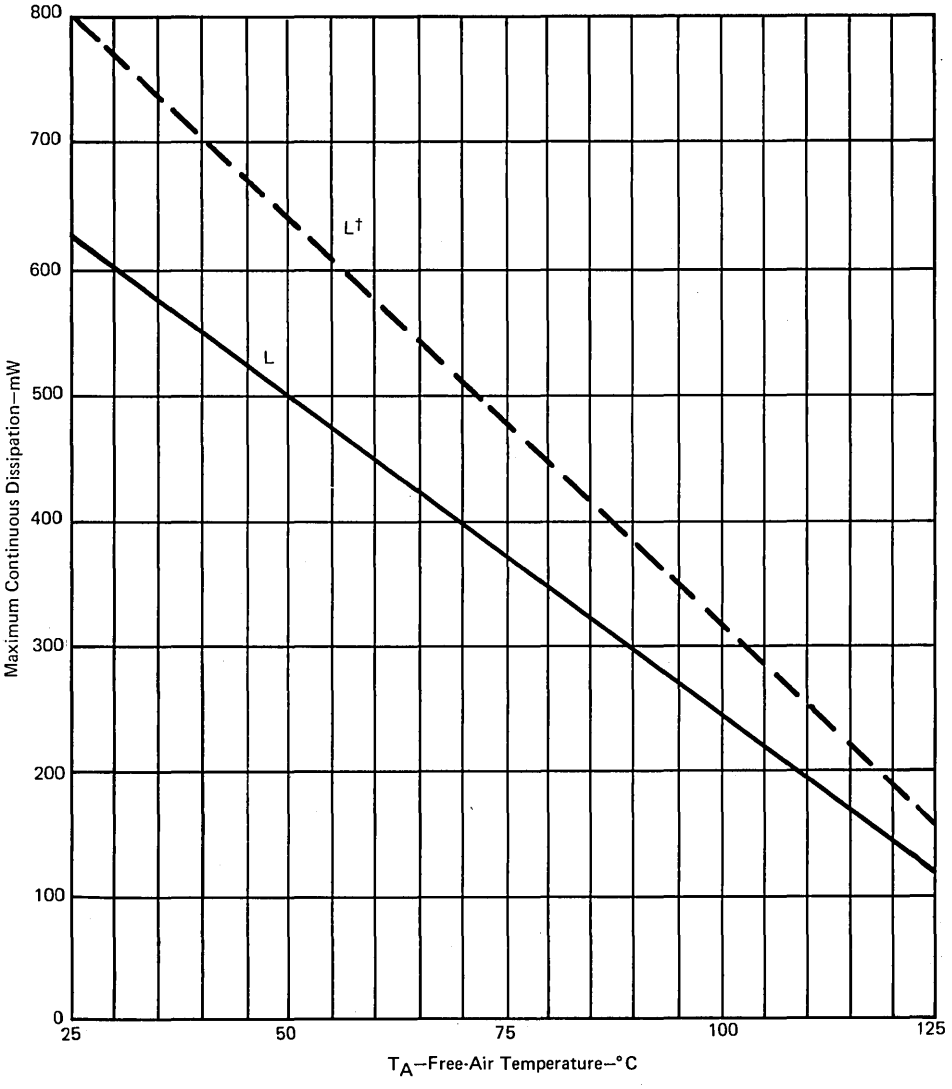
AXIAL-LEAD PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE

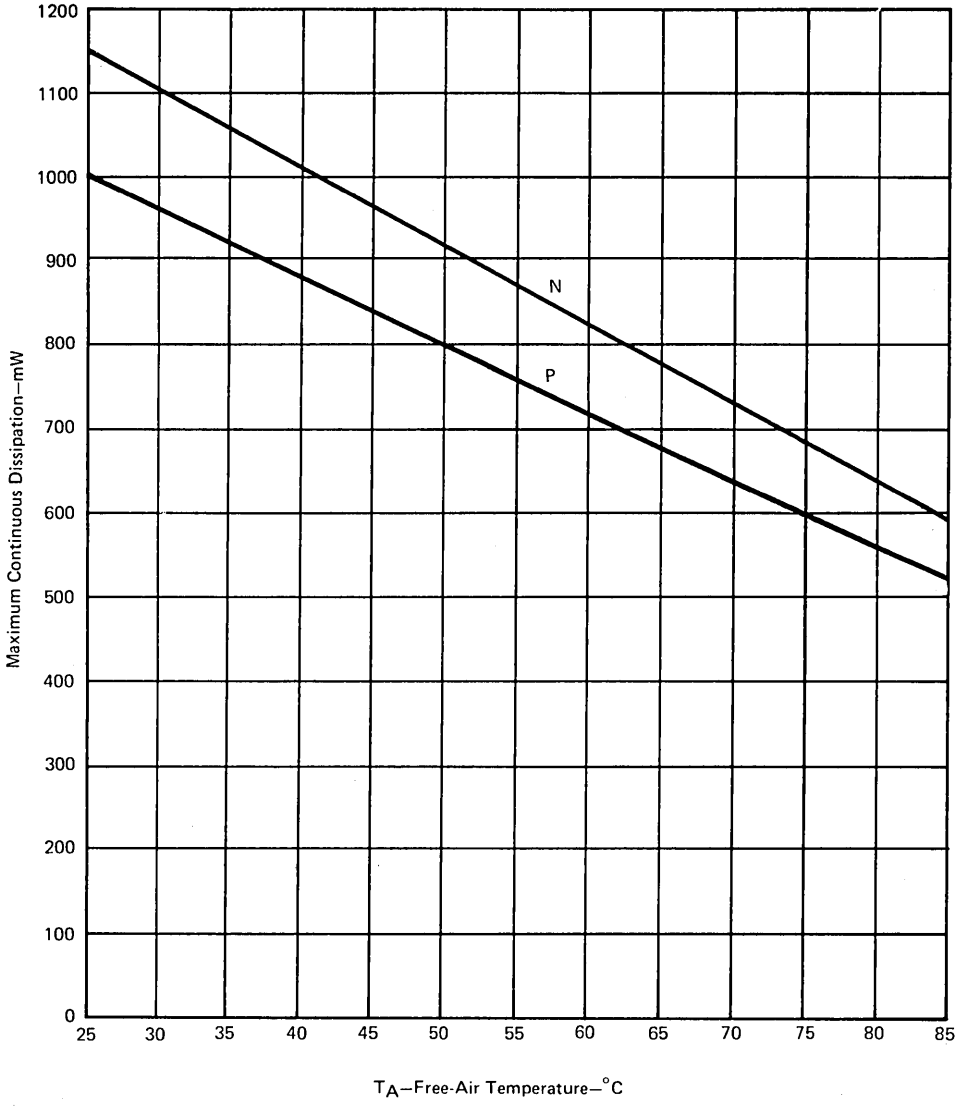


†This rating for the L package requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 105°C/W.

PLASTIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



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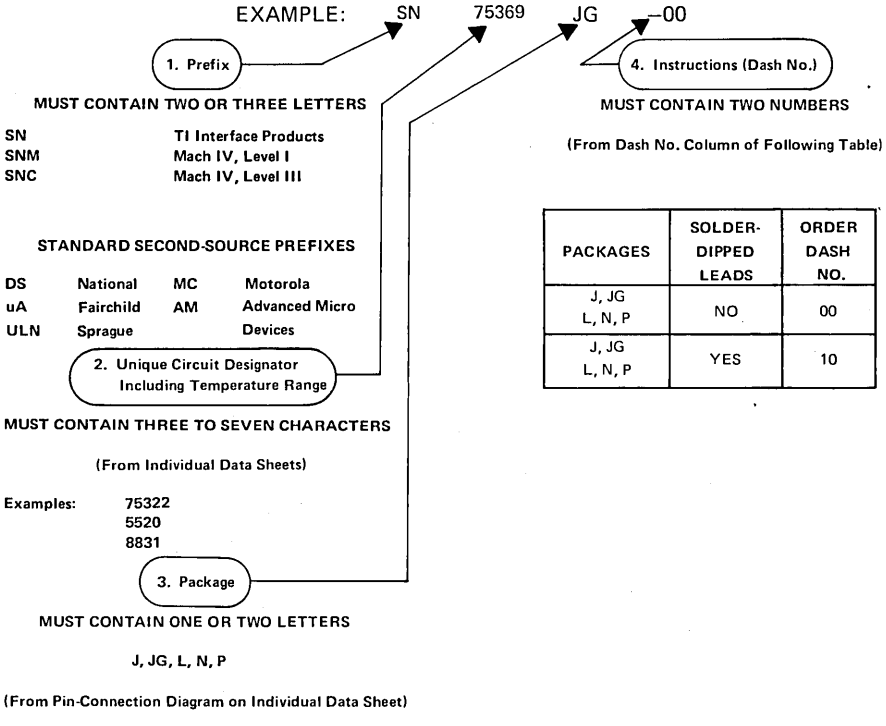
Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book apply for the circuit type(s) listed in the page heading, unless otherwise noted, regardless of package. The availability of a circuit function in a particular package is indicated by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.



PACKAGES	SOLDER-DIPPED LEADS	ORDER DASH NO.
J, JG L, N, P	NO	00
J, JG L, N, P	YES	10

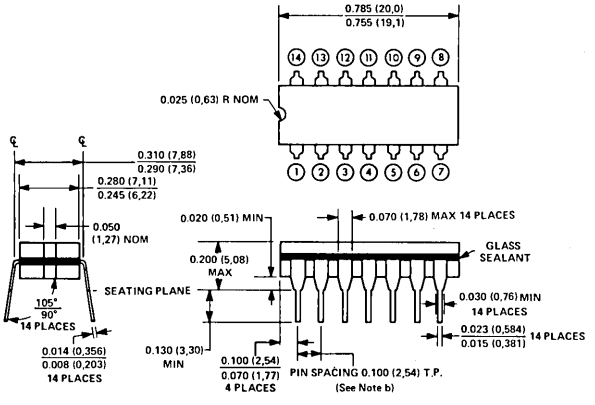
Circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

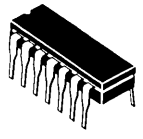
–Slide Magazines
–A-Channel Plastic Tubing
–Barnes Carrier
–Sectioned Cardboard Box
–Individual Plastic Box

J ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 20-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

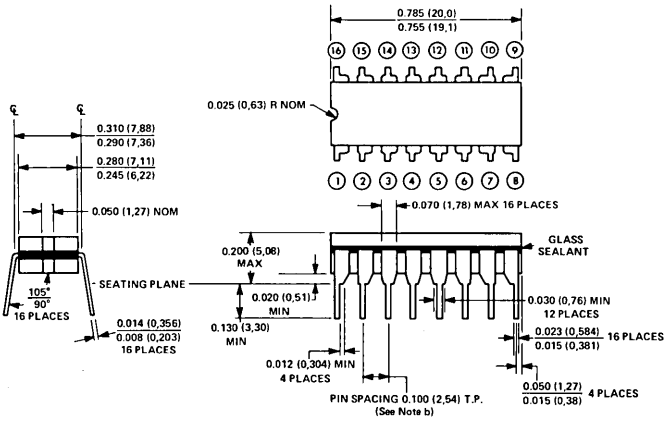
14-PIN J CERAMIC

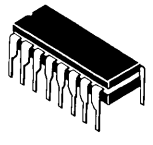




Falls within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC





NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

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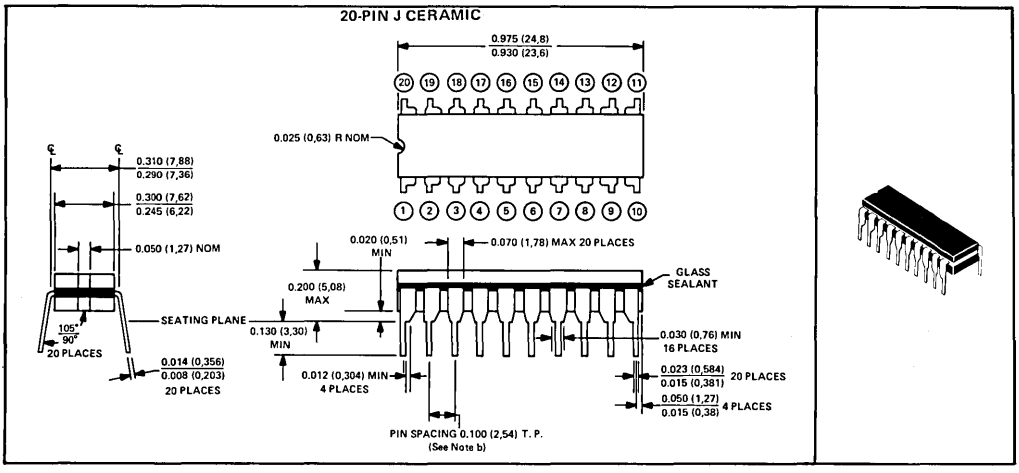
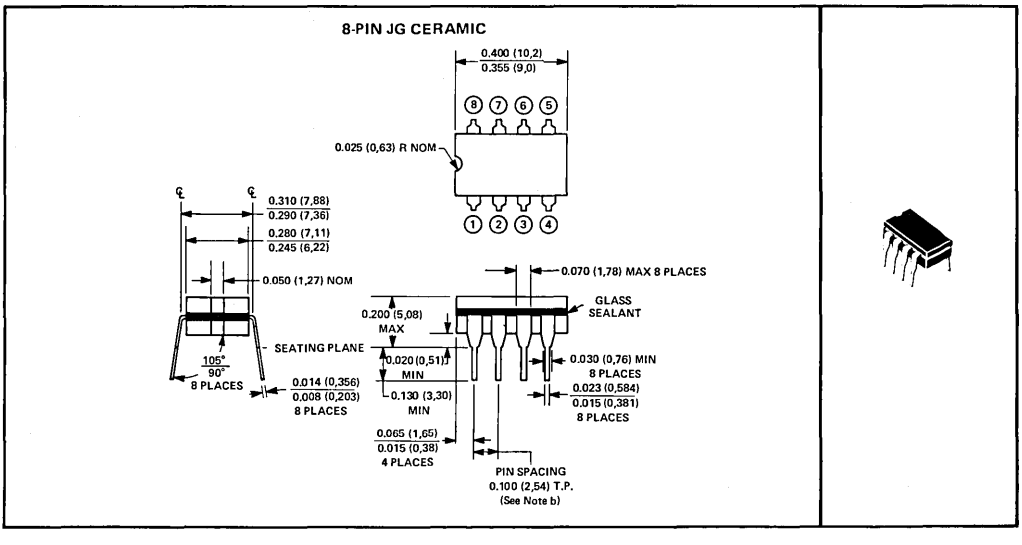
J ceramic dual-in-line packages (continued)



JG ceramic dual-in-line package

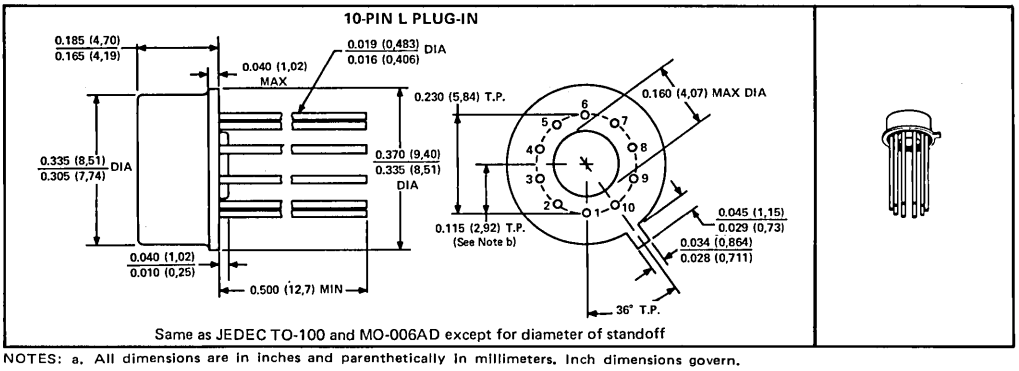
This hermatically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. The package is intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

L plug-in package

This hermetically sealed, plug-in package consists of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

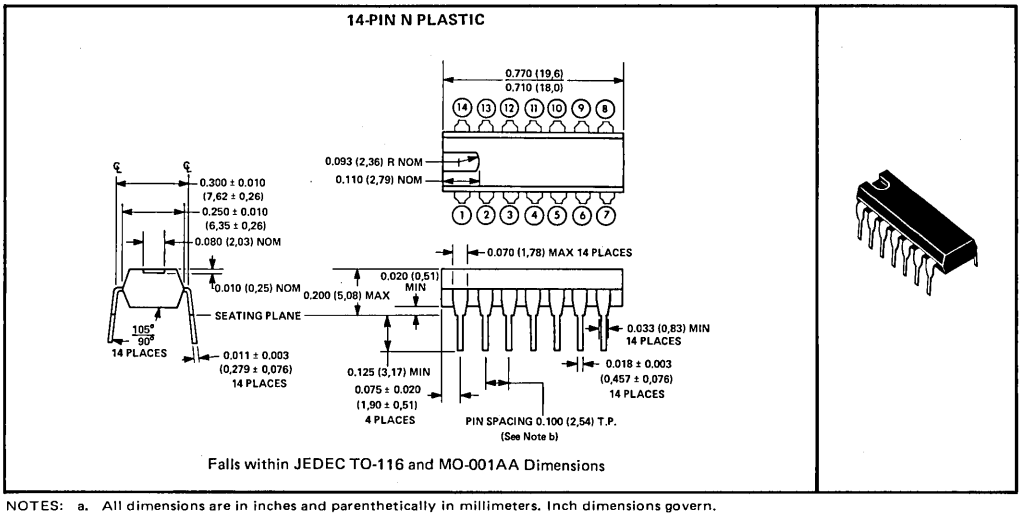


NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each lead is located within 0.007 (0,18) of its true position at maximum material condition.

3

N plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 20-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

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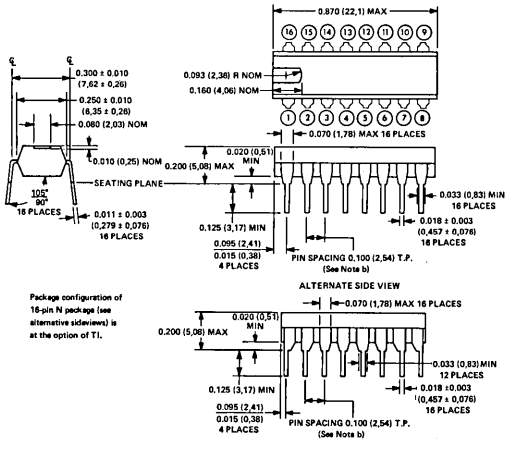
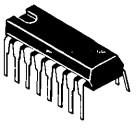
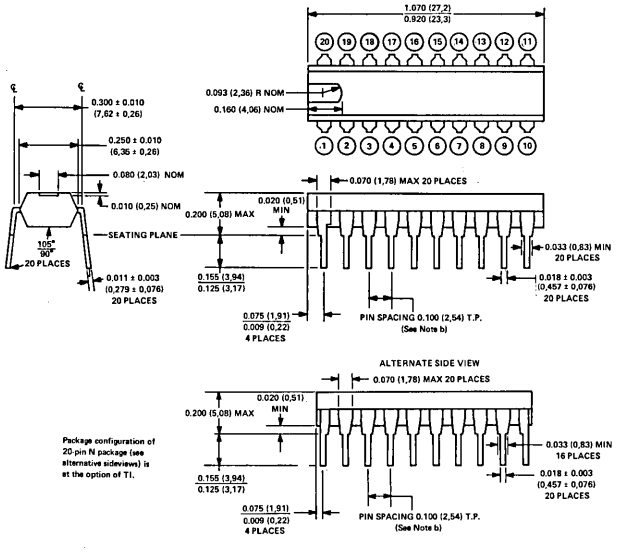
N dual-in-line plastic packages (continued)

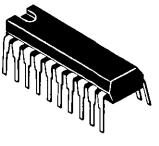
16-PIN N PLASTIC





20-PIN N PLASTIC

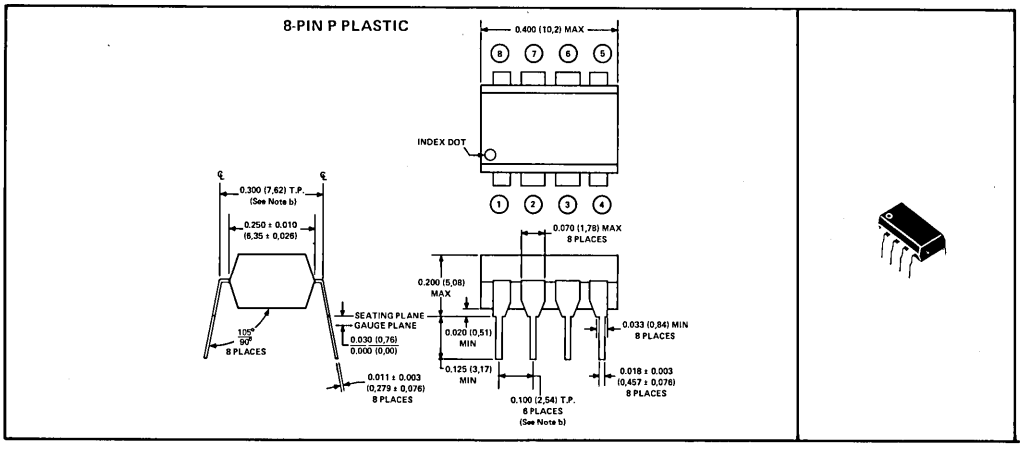




NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated in an electrically, nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated under high-humidity conditions. This package is intended for insertion in mounting hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is within 0.005 (0,127) radius of true position at the gauge plane with maximum material condition and unit installed.

Sense Amplifiers

SENSE AMPLIFIERS

DESCRIPTION	THRESHOLD SENSITIVITY	COMMON-MODE RANGE	TYPE† OF OUTPUT	t_{PD}¶ TYPICAL	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	UNITS PER PACKAGE	ADDITIONAL FEATURES	PAGE NO.
					–55°C to 125°C	0°C to 70°C				
CORE-MEMORY SENSE AMPLIFIERS	±4 mV	±2.5 V	R	35 ns	SN5520	SN7520	J J,N	1	• Provides memory data register • Complementary outputs	33
			O-C or R	30 ns	SN5522	SN7522	J J,N	1	• Dual input channels • Single-ended output	
			R	25 ns	SN5524	SN7524	J J,N	2	• Independent strobes	
			R	25 ns	SN5528	SN7528	J J,N	2	• Independent strobes • Test points for strobe timing adjustment	
			O-C	25 ns	SN55232	SN75232	J J,N	2	• Independent strobes • Internally compensated reference amplifier	
			R	25 ns	SN55234	SN75234	J J,N	2	• Independent strobes • Internally compensated reference amplifier	
			R	25 ns	SN55238	SN75238	J J,N	2	• Independent strobes • Internally compensated reference amplifier • Test points for strobe timing adjustment	
	±3 mV	±1.5 V	T-P	28 ns	SN55236	SN75236	W W	2	• Built in data buffer and data register • Reference amplifier inherently stable	See Note 1
MOS-TO-TTL CONVERTER ARRAY	500 μA		T-P	30 ns		SN75270	J,N	7	• 7 single-ended noninverting drivers per package • Single 5-V supply	89
MOS-MEMORY SENSE AMPLIFIERS	±25 mV	±3 V	T-P	17 ns	SN55107A	SN75107A	J J,N	2	• Independent strobes	See Note 2
	±25 mV	±3 V	O-C	19 ns	SN55108A	SN75108A	J J,N	2	• Independent strobes	
	±10 mV	±3 V	T-P	17 ns		SN75207	J,N	2	• Independent strobes	83
			O-C	19 ns		SN75208	J,N	2		
TMS 4062 I/O INTERFACE	±50 μA		R	25 ns		SN75370	J,N	2	• Combined driver and sense amplifier • Read enable and write enable controls	169

† T-P = Totem Pole, O-C = Open Collector, R = Resistor Pull-Up

¶ t_{PD} = Propagation Delay Time

NOTES: 1. For additional information, contact your nearest TI field sales office.

2. For data sheet, see page 41 of "The Line Driver and Line Receiver Data Book for Design Engineers," LCC4290.

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SERIES 5520/7520 SENSE AMPLIFIERS

BULLETIN NO. DL-S 7711279, AUGUST 1973–REVISED APRIL 1977

HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READOUT TO SATURATED DIGITAL-LOGIC LEVELS

performance features

- High Speed and Fast Recovery Time
- Time and Amplitude Signal Discrimination
- Adjustable Input Threshold Voltage Levels
- Narrow Region of Threshold Voltage Uncertainty
- Multiple Differential-Input Preamplifiers
- High D-C Noise Margin . . . Typically One Volt
- Good Fan-Out Capability

ease-of-design features

- Choice of Output Circuit Function
- TTL or DTL Drive Capability
- Standard Logic Supply Voltages
- Plug-in Configuration Ideal for Flow-Soldering Techniques
- Pins on 100-mil Grid Spacings for Industrial-Type Circuit Boards

description

Series 5520/7520 monolithic sense amplifiers are designed for use with high-speed memory systems. These sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. Low-level pulses originating in the memory are transformed into logic levels compatible with standard transistor-transistor-logic (TTL) and diode-transistor-logic (DTL) circuits.

These sense amplifiers feature multiple differential-input preamplifiers and versatile gating and output circuits, permitting a significant reduction in the circuitry required to accomplish the sensing function. A unique circuit design provides inherent stability of the input threshold level over a wide range of power-supply voltage levels and temperature ranges. Independent strobing of each of the dual sense-input channels ensures maximum versatility and permits detection to occur when the signal-to-noise ratio is at a maximum. The gate and strobe inputs and the outputs are compatible with standard TTL and DTL digital logic circuits.

The SN5520 and SN7520 circuits may be used to perform the functions of a flip-flop or register that responds to the sense and strobe input conditions.

The SN5522 and SN7522 circuits feature a high-fan-out, single-ended, open-collector output stage. In addition, they may be used to expand the inputs to an SN5520 or SN7520 circuit, or to perform the wired-AND function.

The SN5524 and SN7524 circuits provide for independent, dual-channel sensing with separate outputs. SN55234 and SN75234 are similar but have inverted outputs and internal compensation. SN55232 and SN75232 are identical to the SN55234 and SN75234, respectively, except that their output gates each feature an open-collector output.

The SN5528 and SN7528 circuits are identical to the SN5524 and SN7524, respectively, except that the output of each preamplifier is available as a test point. SN55238 and SN75238 are similar to SN5528 and SN7528, respectively, but have inverted outputs and internal compensation.

Series 5520 sense amplifiers are available in the J ceramic dual-in-line package and are characterized for operation over the full military temperature range of −55°C to 125°C. Series 7520 sense amplifiers are available in both the J (ceramic) and N (plastic) dual-in-line packages and are characterized for operation from 0°C to 70°C.

CONTENTS

design characteristics

Series 5520/7520 sense amplifiers are completely d-c coupled. Previous designs have resulted in circuits in which the threshold level could not be closely controlled because they were highly sensitive to changes in the d-c levels throughout the amplifier. This was due primarily to the required tolerances on the absolute value of resistors and the resistor temperature coefficients. The "matched-amplifier" design of Series 5520/7520 circuits depends on resistor ratios rather than absolute values. In this design, excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers increases the versatility of the design.

The basic circuit is used to implement several sense-amplifier designs. Additional logic circuitry is added to the strobe-gate output to provide versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a function not previously available in integrated form. The d-c coupled design eliminates many of the problems associated with overload recovery time and threshold shift (with high input repetition rates) usually encountered in sense amplifier designs that use reactive coupling components.

circuit operation

The basic Series 5520/7520 sense amplifier strobe and threshold circuit is shown in Figure A. The design uses a "matched-amplifier" concept that takes advantage of the inherent excellent component matching and thermal tracking characteristics of monolithic integrated circuits. A reference amplifier is used to generate the collector reference voltage that is distributed to the input amplifiers. Application of an external reference voltage, V_{ref}, establishes the input-amplifier threshold voltage level, V_T. The design is such that there is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal threshold voltage level, V_T. The reference and input amplifiers use identical circuit configurations; therefore, changes in bias levels introduced into the input amplifier through changes in temperature or power-supply voltage levels are compensated by similar changes in the reference amplifier.

The collector reference voltage, supplied by the reference amplifier, can be used to control the threshold-voltage level of more than one input amplifier, thereby establishing equal threshold levels to all of the input sense channels simultaneously.

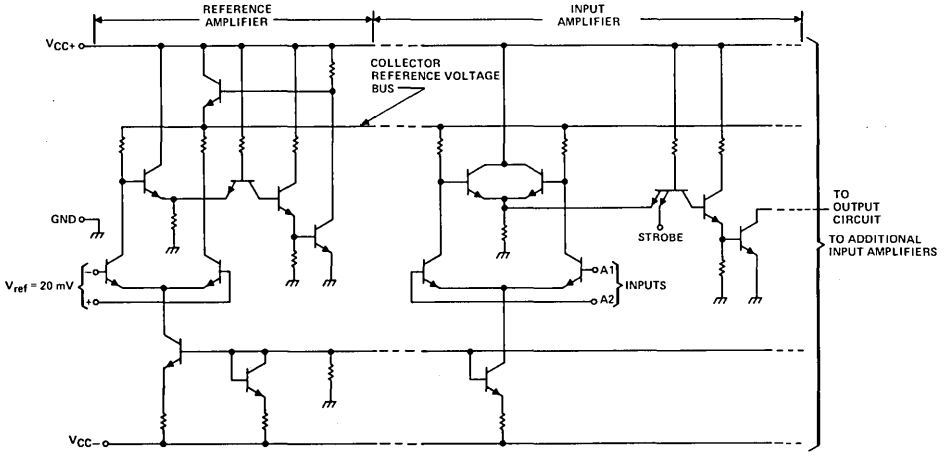

FIGURE A—BASIC SERIES 5520/7520 SENSE-AMPLIFIER CIRCUIT

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circuit operation (continued)

The second stage of the input amplifier is a TTL gate. This gate provides the threshold action for the input sense channel and provides a convenient point in the circuit to accomplish the strobe function. The differential-input sense signal switches the output of the TTL gate only when the strobe input voltage is higher than the logic input threshold voltage. The strobe input, therefore, provides the sense amplifier with the capability of time discrimination, allowing the input signal to be detected when the signal-to-noise ratio is at a maximum.

The logic inputs (i.e., gate and strobe) of Series 5520/7520 sense amplifiers are designed to be compatible with Series 54/74 TTL digital integrated circuits. The multiple-emitter transistors are utilized to provide inherent switching-time advantages over other saturated-logic schemes. The same noise margin and logic threshold voltage as guaranteed for Series 54/74 are assured for each of the gate and strobe inputs. This is accomplished by testing each logic input under standard Series 54/74 test conditions, i.e., 2 volts for high-level input condition and 0.8 volt for low-level input conditions. Since the guaranteed minimum high-level output voltage is 2.4 volts and the guaranteed maximum low-level output voltage is 0.4 volt, a minimum noise margin of 0.4 volt is assured at each input.

SN5520/SN7520 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage and a complementary output stage. The output circuit is composed of two cascaded NAND gates, each with external gate inputs. External connection of the Z output and the G_Y input results in a flip-flop or register that is set by signals at the differential-input terminals. Reset of the register is performed at the G_Z input. Capacitive coupling from output Z to G_Y results in output pulse stretching. With either connection, complementary output levels are available. The gate and strobe inputs and the outputs are compatible with standard TTL logic. The input function of SN5520/SN7520 can be expanded by connecting the Y output of SN5522/SN7522 to the G_Y input of the circuit being expanded.

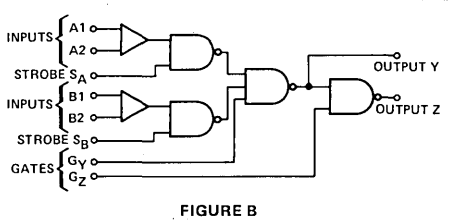

FIGURE B
SN5520/SN7520 LOGIC DIAGRAM

logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

$Z = \overline{G}_Z + G_Y (\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN5522/SN7522 circuit

This circuit is a dual-channel sense amplifier with the preamplifiers connected to a common output stage. The output circuit features an open-collector output that permits two or more of these outputs to be connected in the wire-AND configuration. Each package includes a load resistor that may be used as the output pull-up resistor. High sink-current capability is a feature of this design, and a separate ground terminal is used for the output circuitry. These devices can also be used as input expanders for the SN5520/SN7520 circuit.

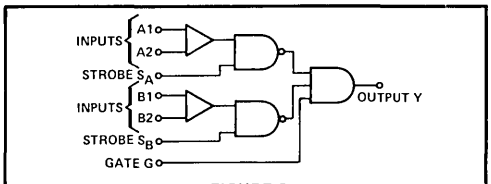

FIGURE C
SN5522/SN7522 LOGIC DIAGRAM

logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

SN5524/SN7524 circuit

This circuit features two completely independent sense amplifiers in a single package. Each amplifier features high fan-out capability.

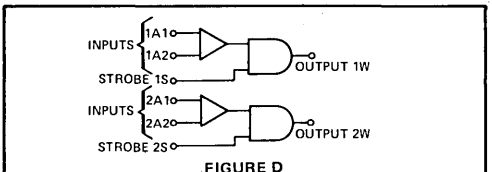

FIGURE D
SN5524/SN7524 LOGIC DIAGRAM
SN55232/SN75232 SAME EXCEPT INVERTED OPEN-COLLECTOR OUTPUT
SN55234/SN75234 SAME EXCEPT INVERTED OUTPUT

logic: W = AS for SN5524 and SN7524

$W = \overline{AS}$ for SN55232, SN75232, SN55234, and SN75234

4

SN5528/SN7528 circuit

This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point. These test points can be used to observe the amplified core signal to facilitate accurate strobe timing. When using this device, care should be taken to avoid coupling the strobe signal or other stray signals to the test point. Excessive loading of the test point is also to be avoided. The result of either coupling or loading will be a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration with a high fan-out capability.

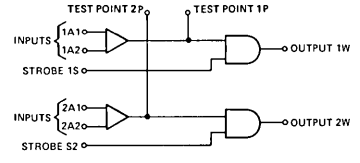

FIGURE E
SN5528/SN7528 LOGIC DIAGRAM
SN55238/SN75238 SAME EXCEPT INVERTED OUTPUT

logic: W = $\overline{AS}$ for SN5528 and SN7528
W = $\overline{AS}$ for SN55238 and SN75238

SN55232, SN75232, SN55234, SN75234, SN55238, and SN75238 circuits

The SN55234, SN75234, SN55238, and SN75238 dual sense amplifier circuits are the same as SN5524, SN7524, SN5528, and SN7528, respectively, except that an additional stage has been added to the output gate to provide an inverted output and internal compensation has been added. Compared to using a separate gate for inversion, not only is package count reduced, but less propagation delay is added. The need for an external roll-off capacitor has been eliminated. SN55232 and SN75232 are identical to the SN55234 and SN75234, respectively, except that their output gates each have an open-collector output. This permits two or more outputs to be connected in wire-AND configuration.

reference voltage considerations

These sense amplifiers feature a variable-threshold voltage level with simultaneous adjustment of both sense channels or both sense amplifiers by a single reference voltage. The operating threshold voltage level of the input amplifiers is established by and is approximately equal to the applied reference input voltage, V_{ref}. These sense amplifiers are recommended for use in systems requiring threshold voltage levels of ±15 to ±40 mV.

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive (V_{CC+}) or negative (V_{CC-}) voltage supplies. See Figure F. This type of voltage divider may be used to supply an individual reference amplifier or to supply a number of paralleled reference amplifiers. The bias current required at the reference amplifier input is low (nominally 30 μA); therefore, voltage dividers of this type may normally be operated with very low current requirements. In noisy environments, the use of a filter capacitor across the inputs is recommended. By locating the capacitor as close to the device terminals as possible, noise and stray signals will be presented common-mode to the reference amplifier and thus be rejected.

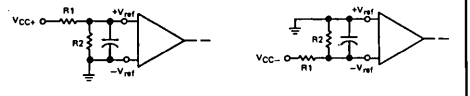

FIGURE F

input line layout considerations

Input sensitivity and device speed require adequate precautions in the routing of signal input and reference lines to prevent noise pickup. Bypassing of supply and reference inputs at the device with low-inductance disc ceramic capacitors and use of a good ground plane to separate strobe and output lines from sense and reference input lines are recommended.

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sense-input termination resistor considerations

Termination resistors are intentionally omitted from the sense-input terminals so the designer may select resistor values that will be compatible with the particular application. Matched termination resistors, (R_T, Figure G), normally in the range of 25 Ω to 200 Ω each, are required not only to terminate the sense line in a desired impedance but also to provide a d-c path for the sense-input bias currents. Careful matching of the resistor pairs should be observed or effective common-mode rejection will be reduced.

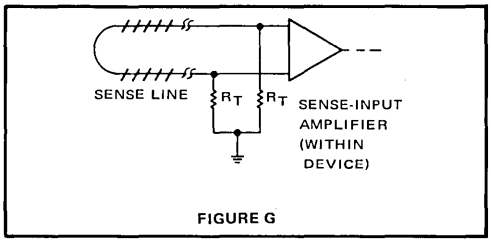


FIGURE G

output drive capability

The output circuits of these sense amplifiers feature the ability to sink or supply load current. This capability permits direct use with both TTL- and DTL-type loads. The open-collector output of the SN5522/SN7522 circuit may be connected to similar outputs to perform the wire-AND function. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuit indicate the actual direction of current flow.

logic input current requirements

Logic input current requirements are specified at worst-case power-supply conditions over the recommended operating free-air temperature range. The logic input currents are identical to those of, and compatible with, Series 54/74 TTL digital integrated circuits. Each logic input of the multiple-emitter input transistors requires no more than a 1.6-mA flow out of the input at a low logic level. Each input emitter requires current into the input when it is at a high-logic level. This current is 40 μA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1)
- V_{CC+} . . . . . 7 V
- V_{CC-} . . . . . −7 V

Differential input voltage, V_{ID} or V_{ref} . . . . . ±5 V
Voltage from any input to ground (see Note 2) . . . . . 5.5 V
Off-state voltage applied to open-collector outputs . . . . . 5.5 V
Operating free-air temperature range: SN55′ circuits . . . . . −55°C to 125°C
SN75′ circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values, except differential voltages are with respect to network ground terminal.
2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC+}	4.75	5	5.25	V
V_{CC-}	−4.75	−5	−5.25	V
V_{ref}	15		40	mV

TYPES SN5520, SN7520
DUAL-CHANNEL SENSE AMPLIFIERS WITH COMPLEMENTARY OUTPUTS

FUNCTION TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

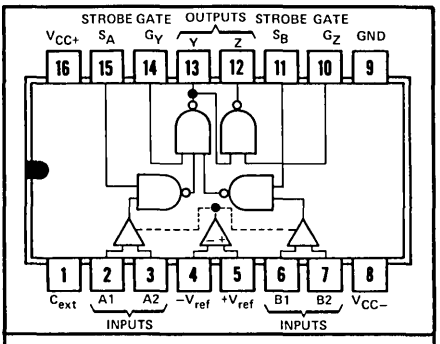
definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

J OR N

DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{G}_Y + A \cdot S_A + B \cdot S_B$

$Z = \overline{G}_Z + \overline{Y}$

$Z = \overline{G}_Z + G_Y(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

electrical characteristics over recommended operating free-air temperature-range, $V_{CC+} = 5$ V, $V_{CC-} = -5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	1	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5520 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5520 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V,	T_A = −55°C to 0°C,	SN5520 only			100	μA
			V_{CC-} = −5.25 V,	T_A = 0°C to 70°C			30	75	
			V_{ID} = 0	T_A = 70°C to 125°C,	SN5520 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3				2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3						0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	28	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	28	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	28	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	28	C_L = 15 pF, R_L = 288 Ω		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	29	C_L = 15 pF, R_L = 288 Ω		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	29	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	30	C_L = 15 pF, R_L = 288 Ω		15		ns
$t_{PHL(GZ, Z)}$						10	20	

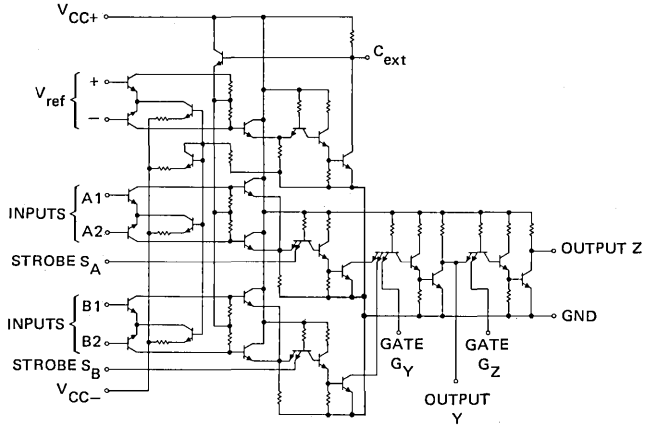
typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

4

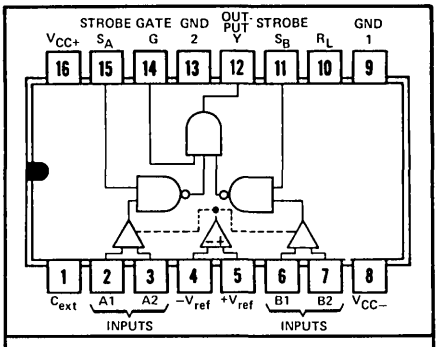
schematic



FUNCTION TABLE

INPUTS					OUTPUT
A	B	G	S_A	S_B	Y
L	L	H	X	X	H
L	X	H	X	L	H
X	L	H	L	X	H
X	X	H	L	L	H
X	X	L	X	X	L
H	X	X	H	X	L
X	H	X	X	H	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = G(\overline{A} + \overline{S}_A)(\overline{B} + \overline{S}_B)$

definition of logic levels

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	7	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5522 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5522 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, *Common-mode input pulse:* $t_r \leq 15$ ns,	$V_{I(S)} = V_{IH}$ $t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN5522 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN5522 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	8				2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	8						0.8	V
V_{OH}	High-level output voltage	8	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	8	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	9	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe and gate inputs)	9	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OH}	High-level output current	10	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	V_O = 5.25 V			250	μA
I_{OS}	Short-circuit output current	11	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		27	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

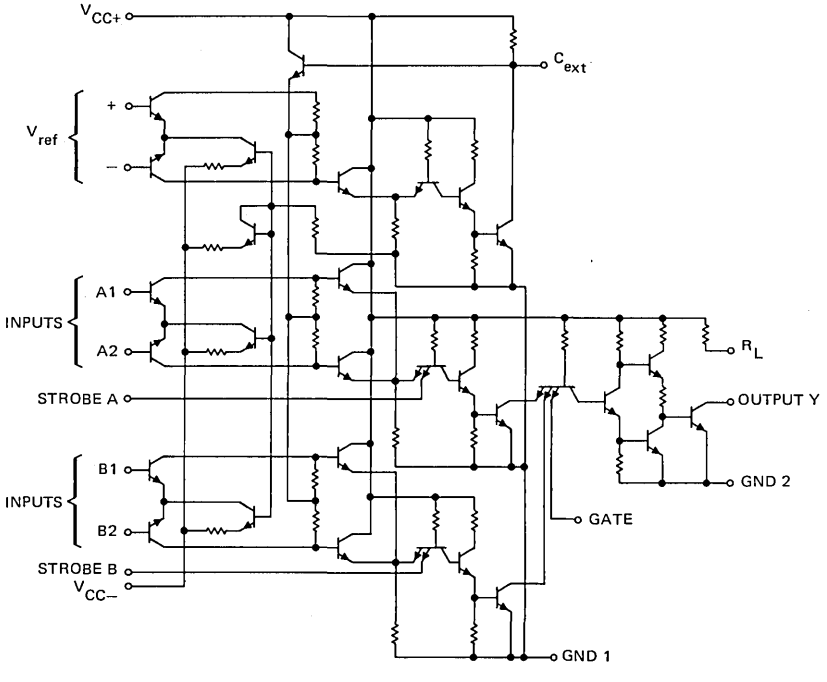
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1-A2 OR B1-B2	Y	31	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(D)}$						30	45	
$t_{PLH(S)}$	STROBE A OR B	Y	31	C_L = 15 pF, R_L = 288 Ω		20		ns
$t_{PHL(S)}$						20	40	
$t_{PLH(G)}$	GATE	Y	32	C_L = 15 pF, R_L = 288 Ω		10		ns
$t_{PHL(G)}$						15	25	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geqslant$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

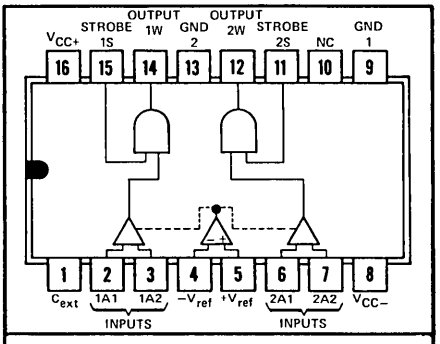
schematic



FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	12	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5524 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5524 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V,	T_A = −55°C to 0°C,	SN5524 only			100	μA
			V_{CC-} = −5.25 V,	T_A = 0°C to 70°C			30	75	
			V_{ID} = 0	T_A = 70°C to 125°C,	SN5524 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	13				2			V
V_{IL}	Low-level input voltage (strobe inputs)	13						0.8	V
V_{OH}	High-level output voltage	13	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	13	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	14	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	14	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	15	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

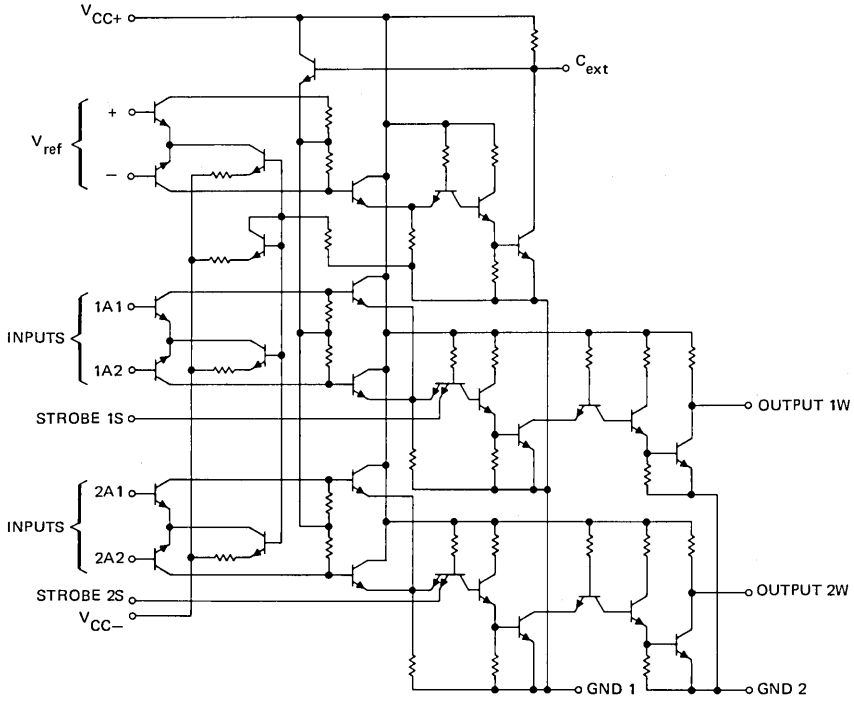
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	33	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		
$t_{PLH(S)}$	STROBE	W	33	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, $C_{ext} \geq$ 100 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

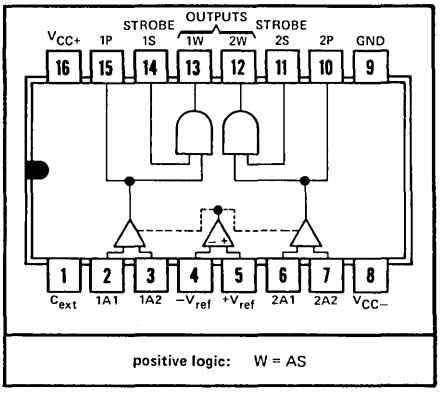


TYPES SN5528, SN7528
DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: W = AS

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	16	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN5528 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN5528 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V,	T_A = −55°C to 0°C,	SN5528 only			100	μA
			V_{CC-} = −5.25 V,	T_A = 0°C to 70°C			30	75	
			V_{ID} = 0	T_A = 70°C to 125°C,	SN5528 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	17				2			V
V_{IL}	Low-level input voltage (strobe inputs)	17						0.8	V
V_{OH}	High-level output voltage	17	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	17	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	18	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	18	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	19	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

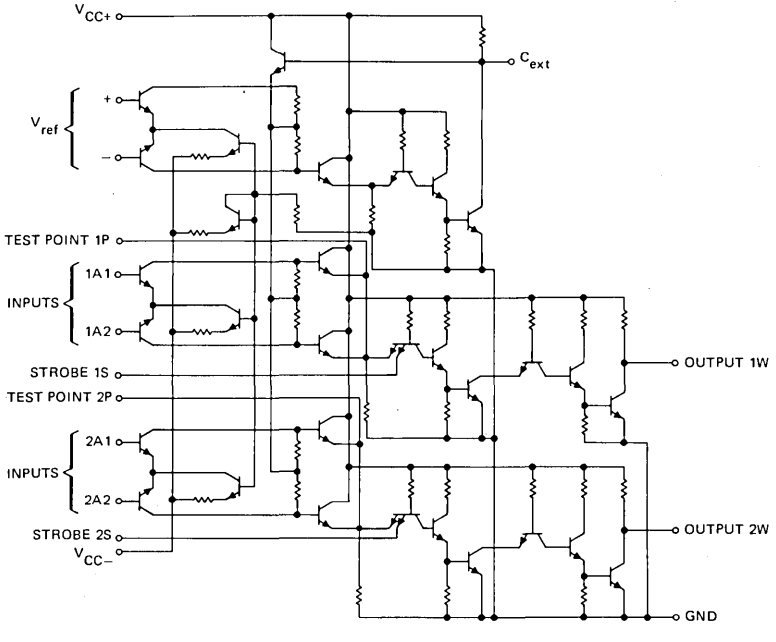
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	34	C_L = 15 pF, R_L = 288 Ω		25	40	ns
$t_{PHL(D)}$						20		ns
$t_{PLH(S)}$	STROBE	W	34	C_L = 15 pF, R_L = 288 Ω		15	30	ns
$t_{PHL(S)}$						20		ns

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

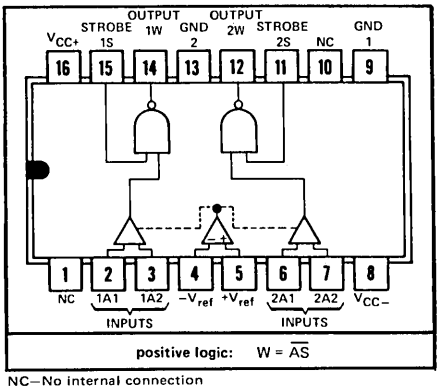


TYPES SN55232, SN75232
DUAL SENSE AMPLIFIERS

FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	20	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN55232 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN55232 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN55232 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN55232 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21				2			V
V_{IL}	Low-level input voltage (strobe inputs)	21						0.8	V
I_{OH}	High-level output current	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	V_{OH} = 5.25 V			250	μA
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

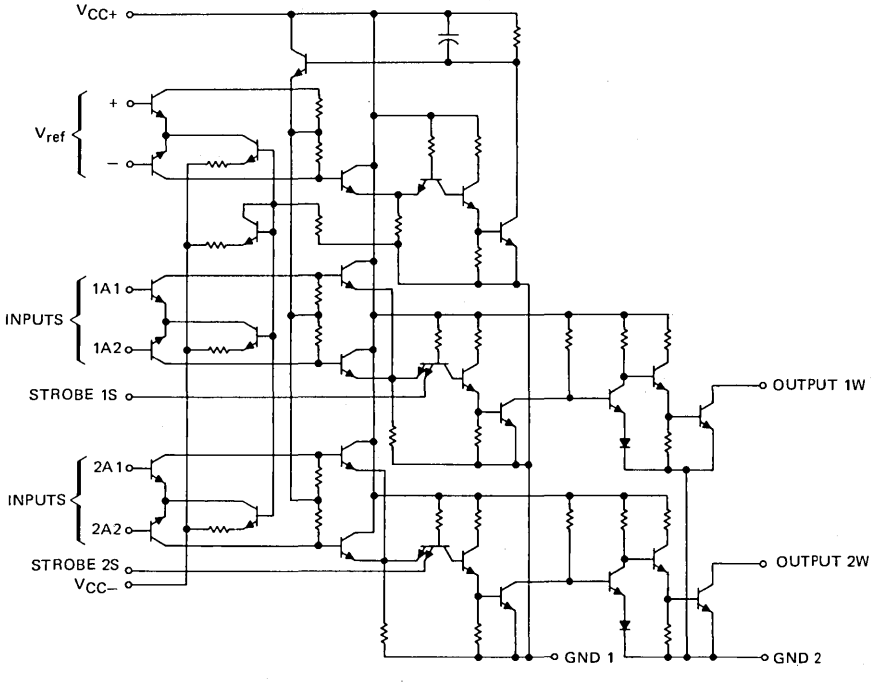
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic

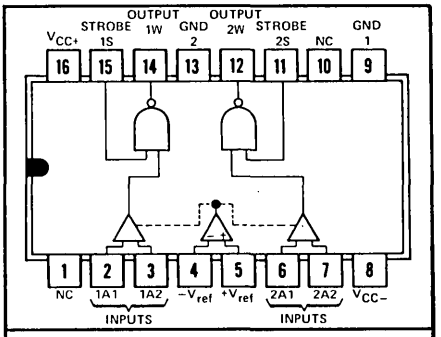


TYPES SN55234, SN75234
DUAL SENSE AMPLIFIERS

FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	20	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN55234 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN55234 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN55234 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN55234 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	21				2			V
V_{IL}	Low-level input voltage (strobe inputs)	21						0.8	V
V_{OH}	High-level output voltage	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	21	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	22	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	23	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

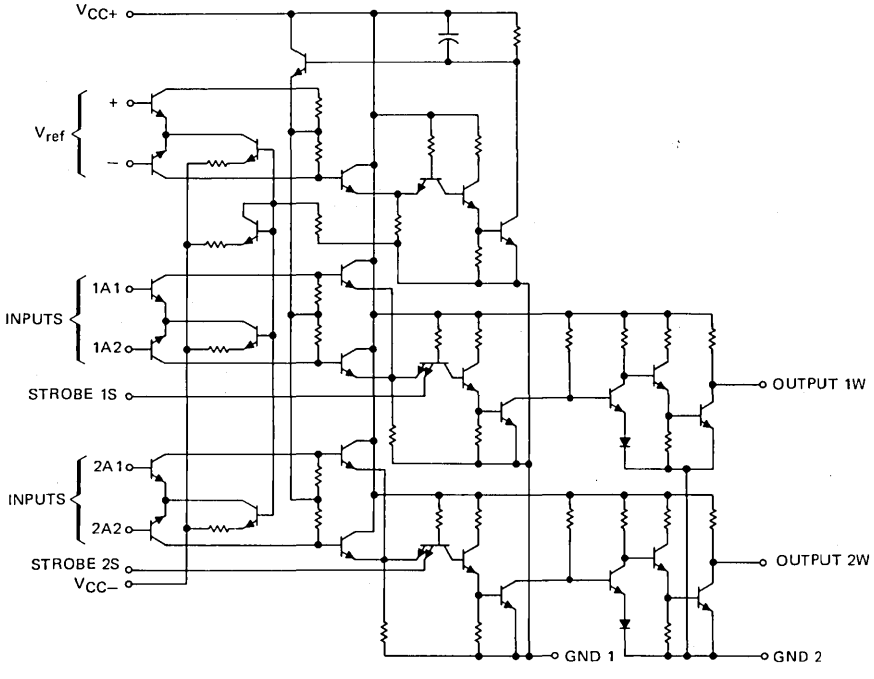
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	35	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

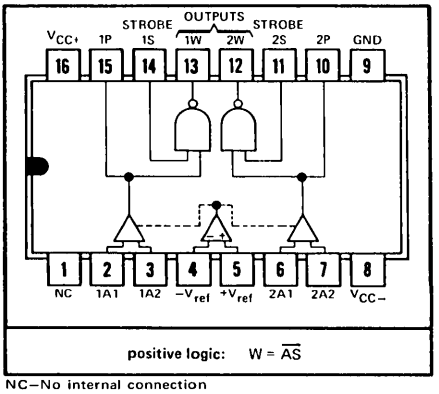
schematic



FUNCTION TABLE

INPUTS A	INPUTS S	OUTPUT W
H	H	L
L	X	H
X	L	H

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

definition of logic levels

INPUT	H	L	X
A†	$V_{ID} \geq V_{T\ max}$	$V_{ID} \leq V_{T\ min}$	Irrelevant
S	$V_I \geq V_{IH\ min}$	$V_I \leq V_{IL\ max}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_T	Differential-input threshold voltage	24	V_{ref} = 15 mV	T_A = 0°C to 70°C		11	15	19	mV
				T_A = −55°C to 125°C,	SN55238 only	10	15	20	
			V_{ref} = 40 mV	T_A = 0°C to 70°C		36	40	44	
				T_A = −55°C to 125°C,	SN55238 only	35	40	45	
V_{ICF}	Common-mode input firing voltage (see Note 3)	none	V_{ref} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns,	$t_f \leq 15$ ns,	t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C,	SN55238 only			100	μA
				T_A = 0°C to 70°C			30	75	
				T_A = 70°C to 125°C,	SN55238 only			75	
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	25				2			V
V_{IL}	Low-level input voltage (strobe inputs)	25						0.8	V
V_{OH}	High-level output voltage	25	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	25	V_{CC+} = 4.75 V,	V_{CC-} = −4.75 V,	I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	26	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	26	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	27	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V,	V_{CC-} = −5.25 V,	T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTE 3: Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The common-mode input signal is applied when the strobe is high.

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switching characteristics, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

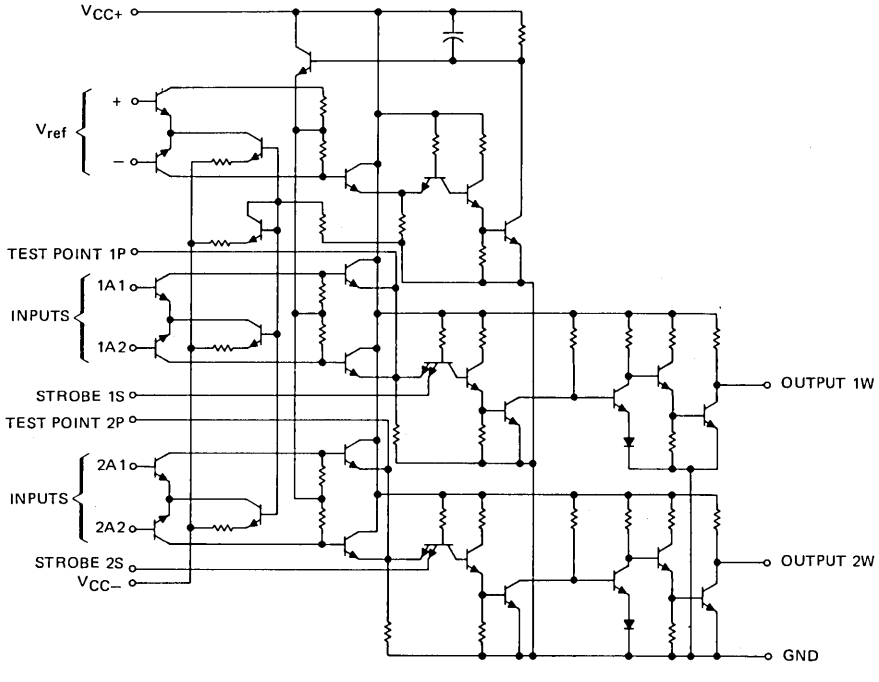
PROPAGATION DELAY TIMES			TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT						
$t_{PLH(D)}$	A1–A2	W	36	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	ns
$t_{PLH(S)}$	STROBE	W	36	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	ns

typical recovery and cycle times, V_{CC+} = 5 V, V_{CC-} = –5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{orD}	Differential-input overload recovery time (see Note 4)	*Differential Input Pulse:* V_{ID} = 2 V, t_f = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 5)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

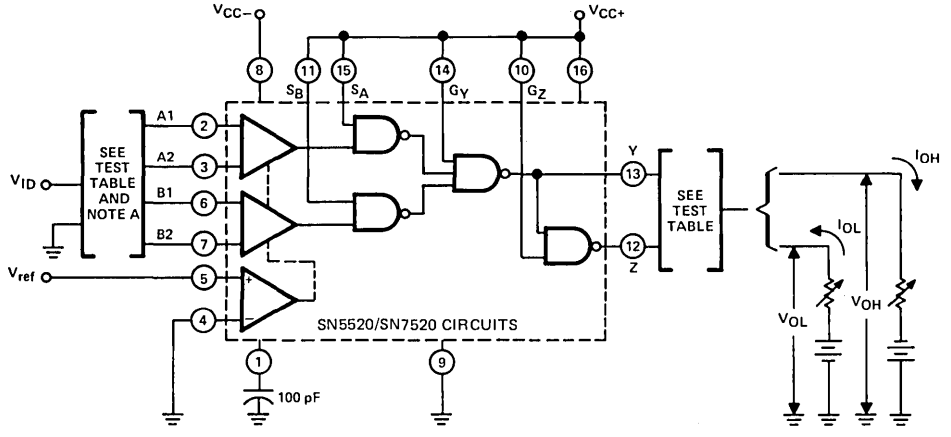
NOTES: 4. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.
5. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

schematic



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN5520/ SN7520	A1-A2 or B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 1–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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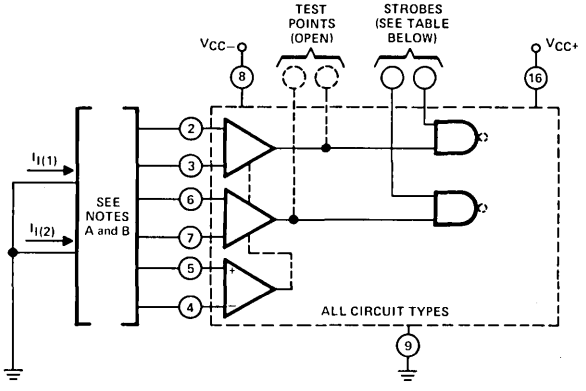
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	100 pF to GND	APPLY V_{CC+}	APPLY GND	LEAVE OPEN	OTHER
SN5520, SN7520	C_{ext} (1)	G_Y, G_Z (14) (10)	S_A, S_B (15) (11)	Y, Z (13) (12)	
SN5522, SN7522	C_{ext} (1)	G (14)	S_A, S_B, GND 2 (15) (11) (13)		R_L, Y (10) (12)
SN5524, SN7524	C_{ext} (1)		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)	
SN5528, SN7528	C_{ext} (1)		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)	
SN55232, SN75232, SN55234, SN75234			1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)	
SN55238, SN75238			1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)	

FIGURE 2–I_{IB}, I_{IO}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

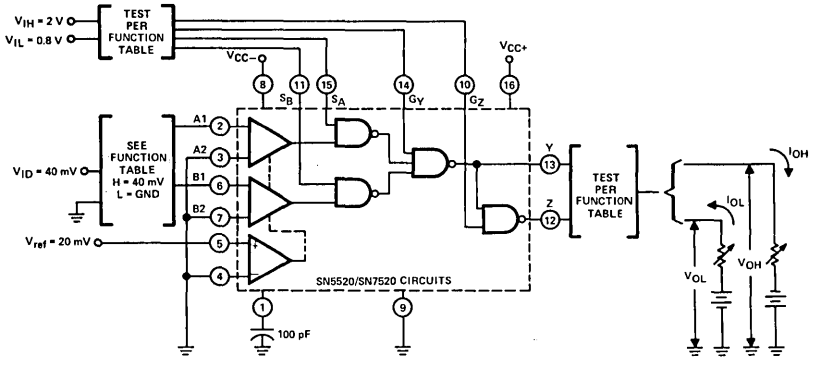
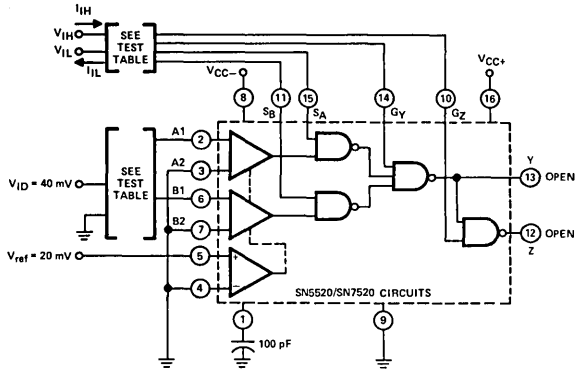


FIGURE 3–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

FIGURE 4–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

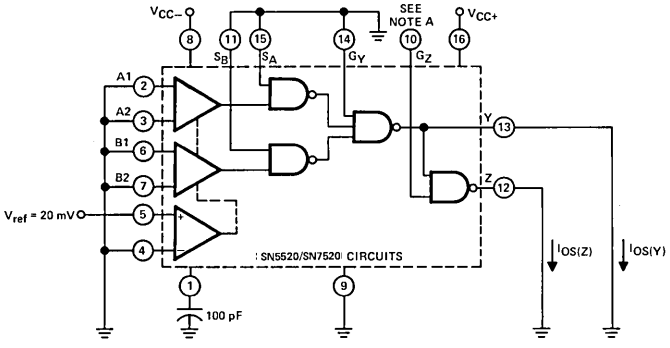
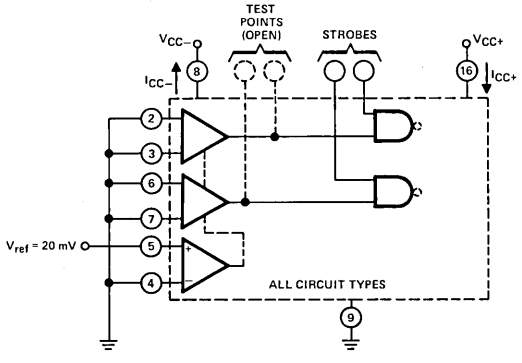


FIGURE 5–I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

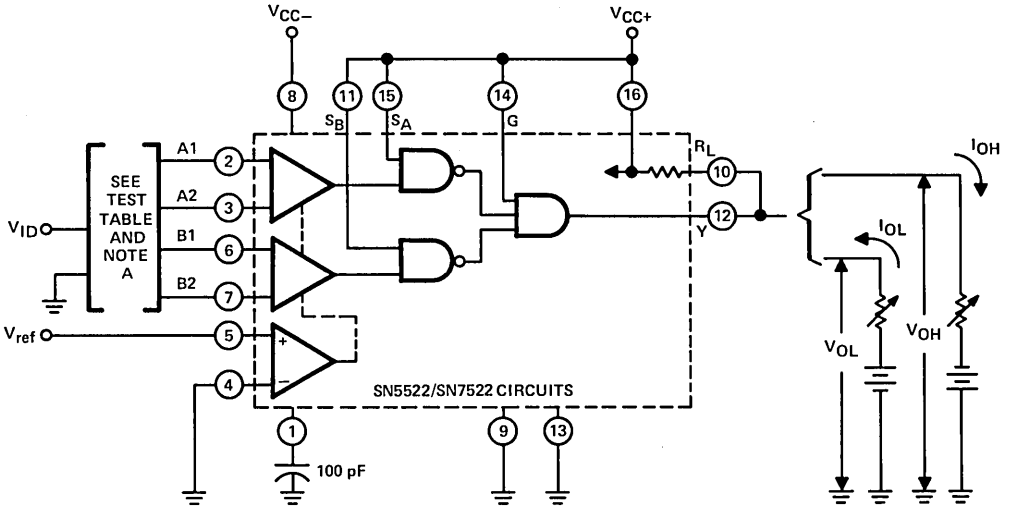
CIRCUIT TYPES	100 pF to GND	APPLY GND	LEAVE OPEN
SN5520, SN7520	C_{ext} (1)	G_Y, G_Z, S_A, S_B (14) (10) (15) (11)	Y, Z (13) (12)
SN5522, SN7522	C_{ext} (1)	G, S_A, S_B, GND 2 (14) (15) (11) (13)	R_L, Y (10) (12)
SN5524, SN7524	C_{ext} (1)	1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN5528, SN7528	C_{ext} (1)	1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)
SN55232, SN75232, SN55234, SN75234		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
SN55238, SN75238		1S, 2S (14) (11)	1P, 2P, 1W, 2W (15) (10) (13) (12)

FIGURE 6–I_{CC+}, I_{CC-}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN5522/ SN7522	A1-A2 or B1-B2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥44 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

FIGURE 7–V_T

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

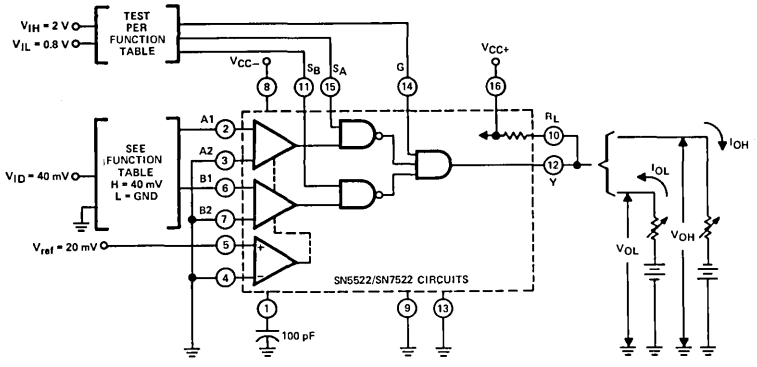
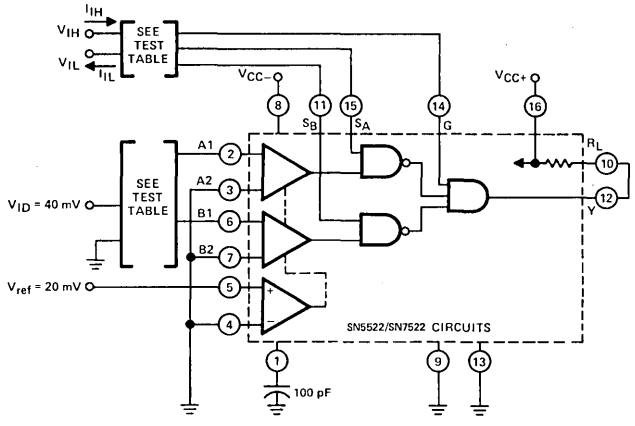


FIGURE 8–V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IH}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IH}
I_{IH} at GATE	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IH}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IH}
I_{IL} at GATE	GND	GND	V_{IL}	V_{IL}	V_{IL}

FIGURE 9–I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

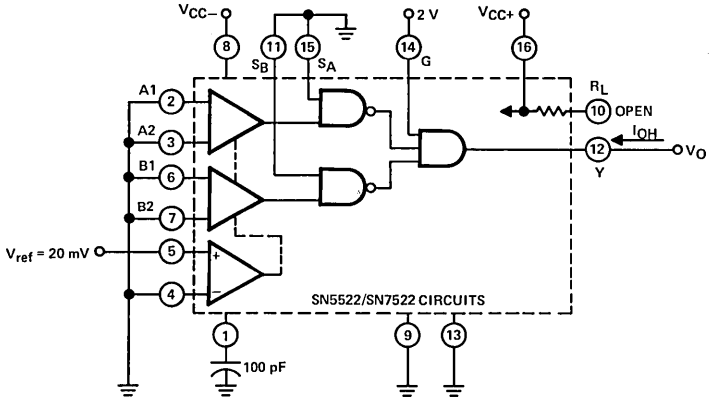


FIGURE 10–I_{OH}

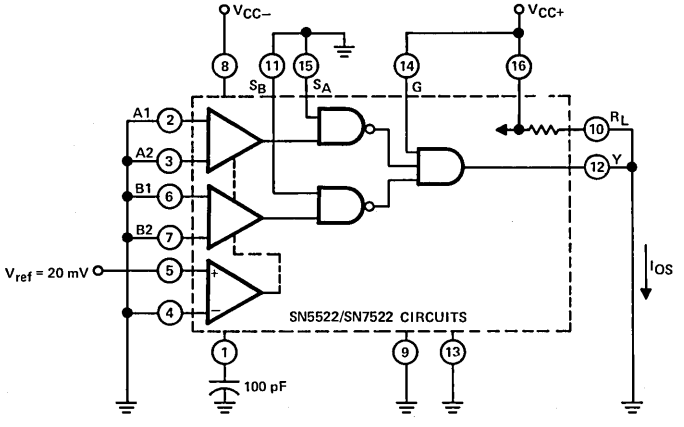


FIGURE 11–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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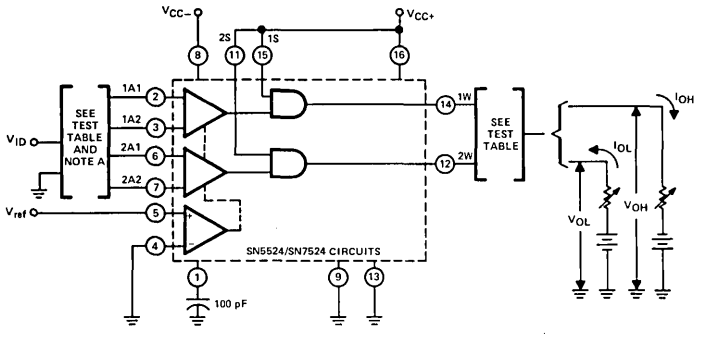
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN5524/ SN7524	A1-A2	15 mV	≤11 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥19 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤36 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥44 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 12–V_T

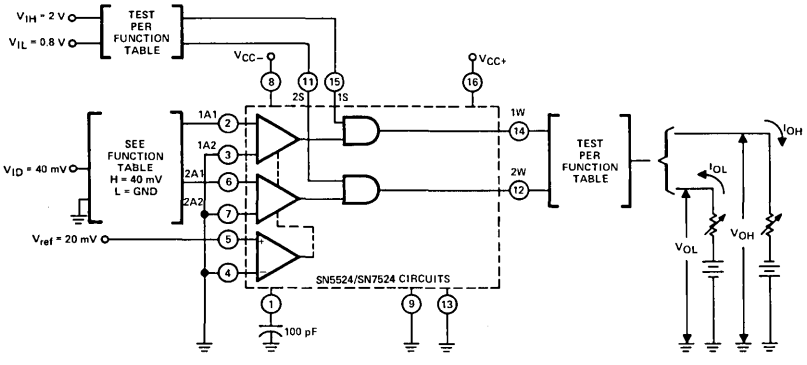
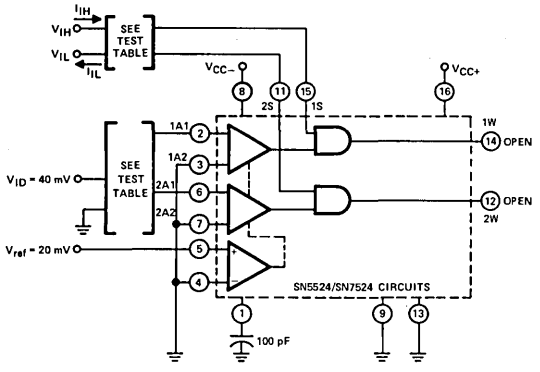


FIGURE 13–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 14–I_{IH}, I_{IL}

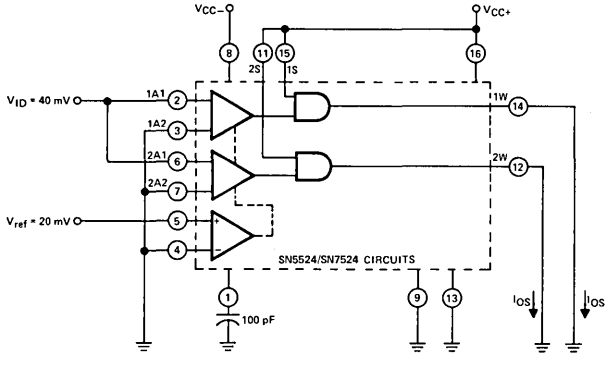


FIGURE 15–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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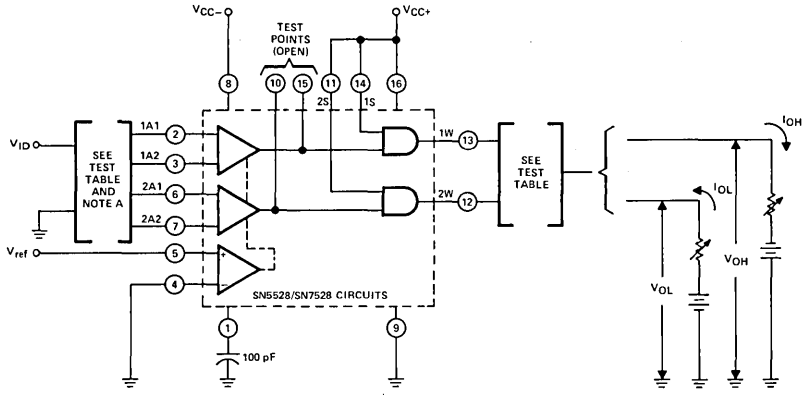
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN5528/ SN7528	A1-A2	15 mV	⩽11 mV	⩽0.4 V		16 mA
	A1-A2	15 mV	⩾19 mV	⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩽36 mV	⩽0.4 V		16 mA
	A1-A2	40 mV	⩾44 mV	⩾2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 16 – V_T

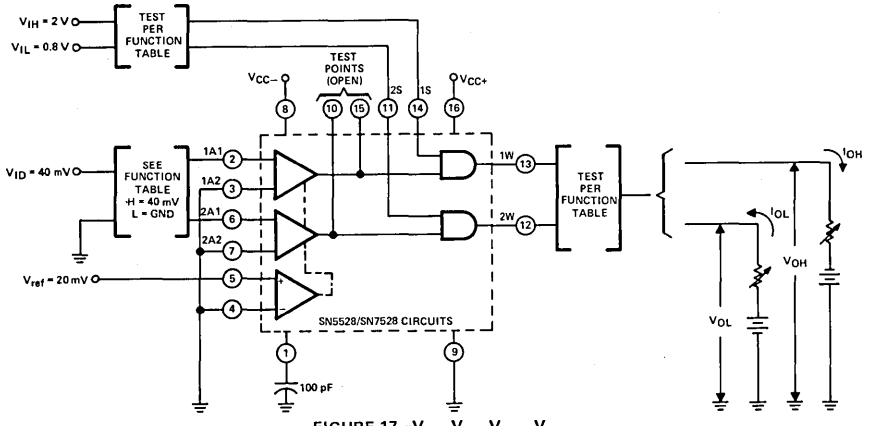
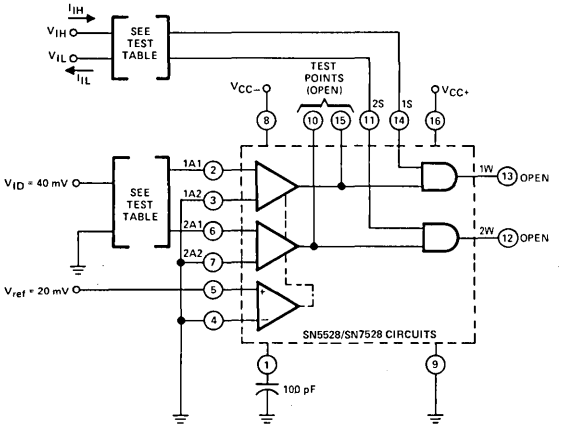


FIGURE 17 – V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 18 –I_{IH}, I_{IL}

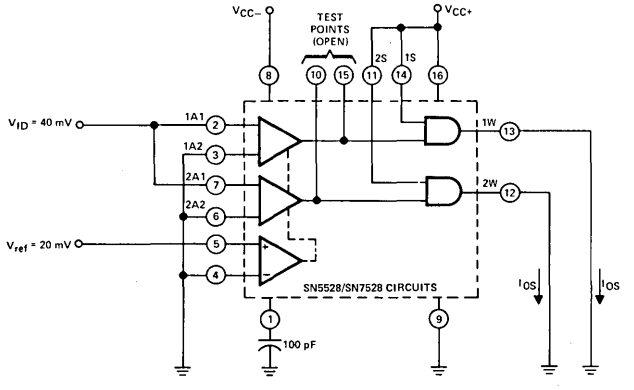
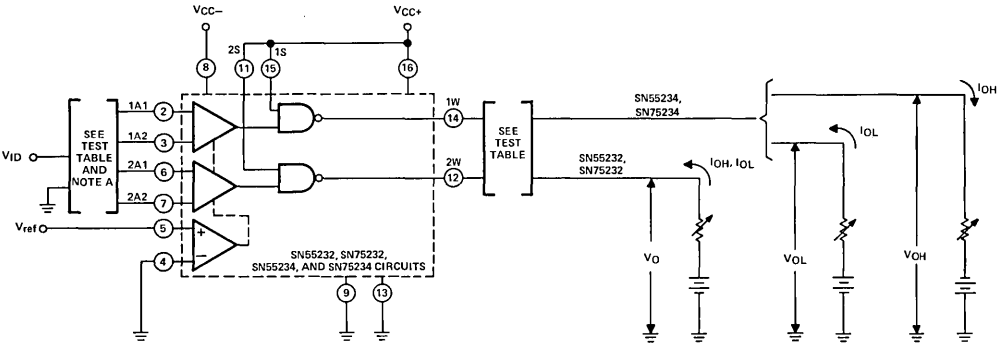


FIGURE 19–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS					
				SN55232, SN75232			SN55234, SN75234		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
SN55232, SN75232, SN55234, SN75234	A1-A2	15 mV	⩽11 mV	5.25 V	⩽250 μA		⩾2.4 V	−400 μA	
	A1-A2	15 mV	⩾19 mV	⩽ 0.4 V		16 mA	⩽0.4 V		16 mA
	A1-A2	40 mV	⩽36 mV	5.25 V	⩽250 μA		⩾2.4 V	−400 μA	
	A1-A2	40 mV	⩾44 mV	⩽ 0.4 V		16 mA	⩽0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

FIGURE 20–V_T

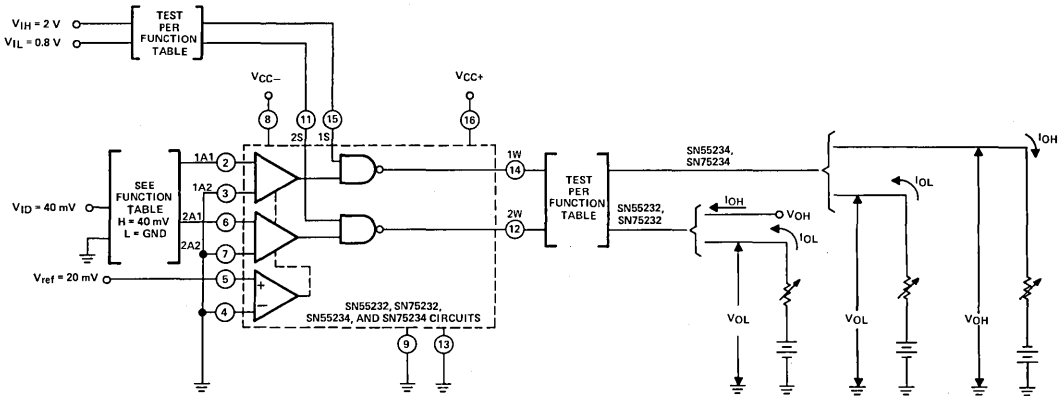
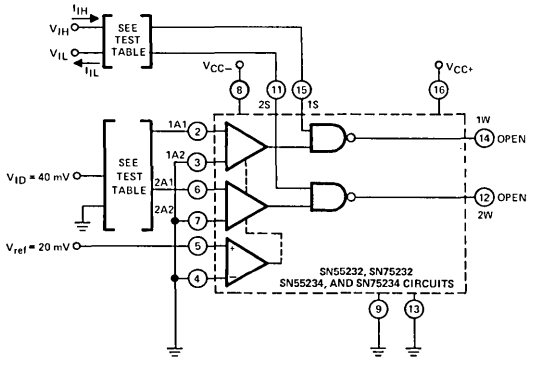


FIGURE 21–V_{IH}, V_{IL}, V_{OL}, V_{OH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 22–I_{IH}, I_{IL}

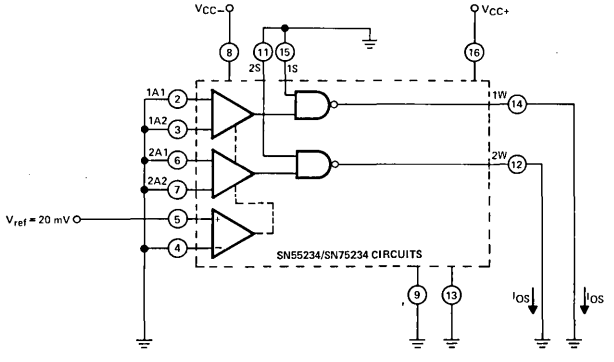
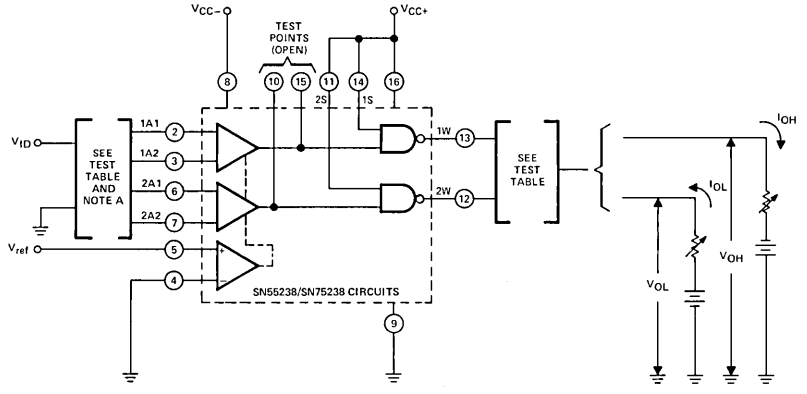


FIGURE 23–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
SN55238/ SN75238	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA

NOTE A: Each pair of inputs is tested separately with its corresponding output.

FIGURE 24–V_T

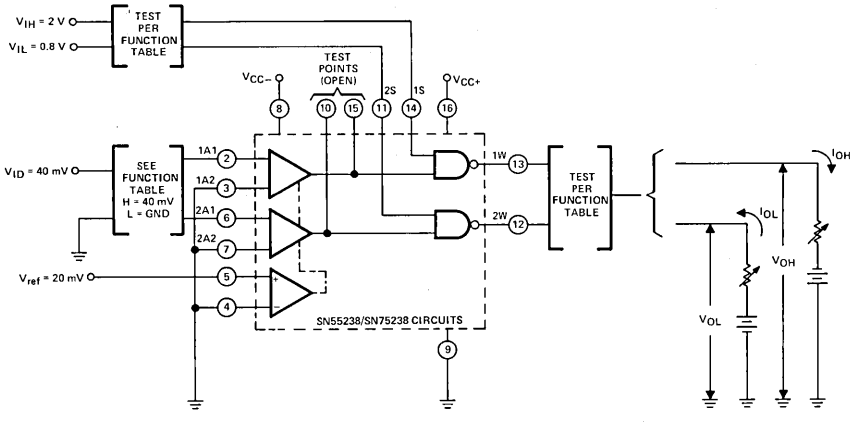
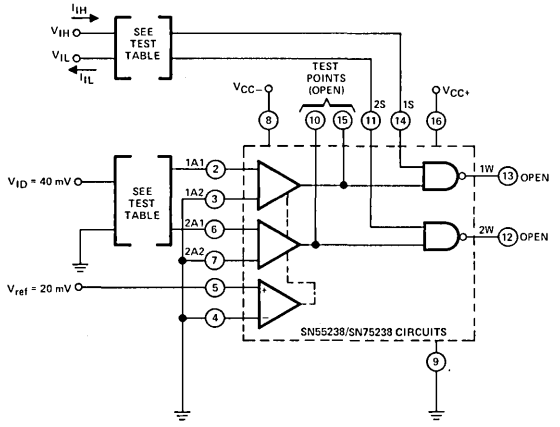


FIGURE 25–V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

FIGURE 26–I_{IH}, I_{IL}

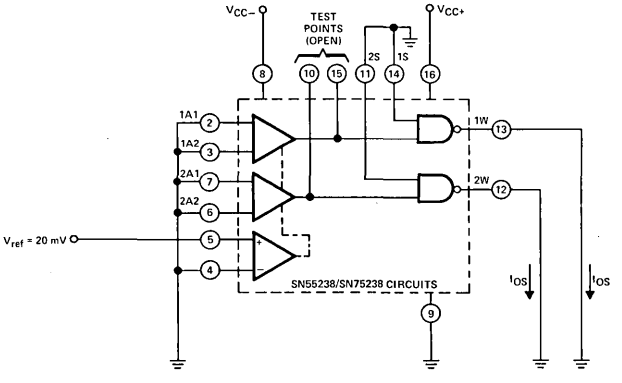


FIGURE 27–I_{OS}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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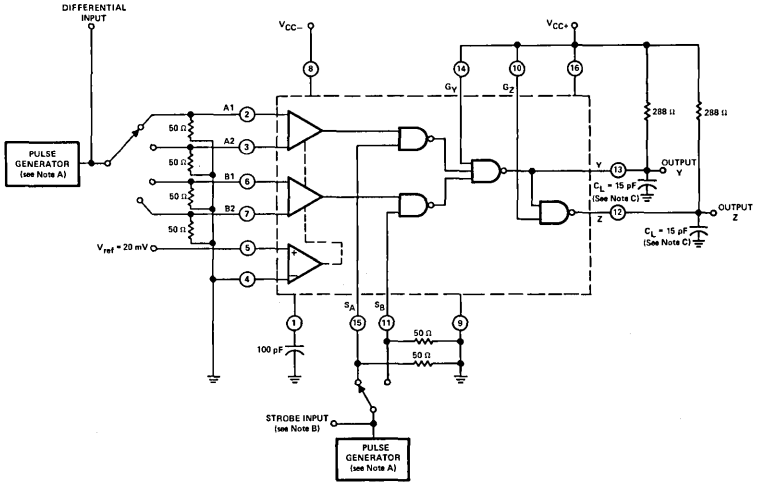
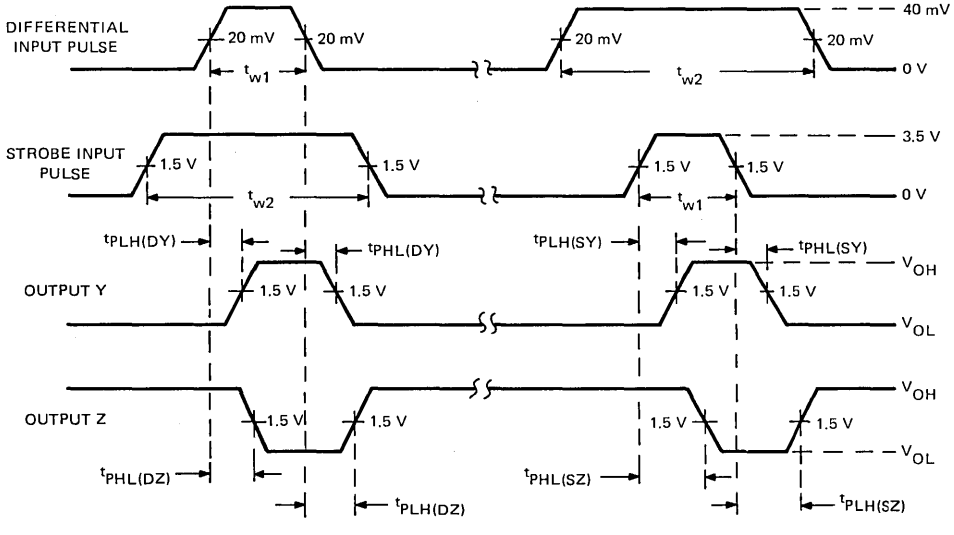
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

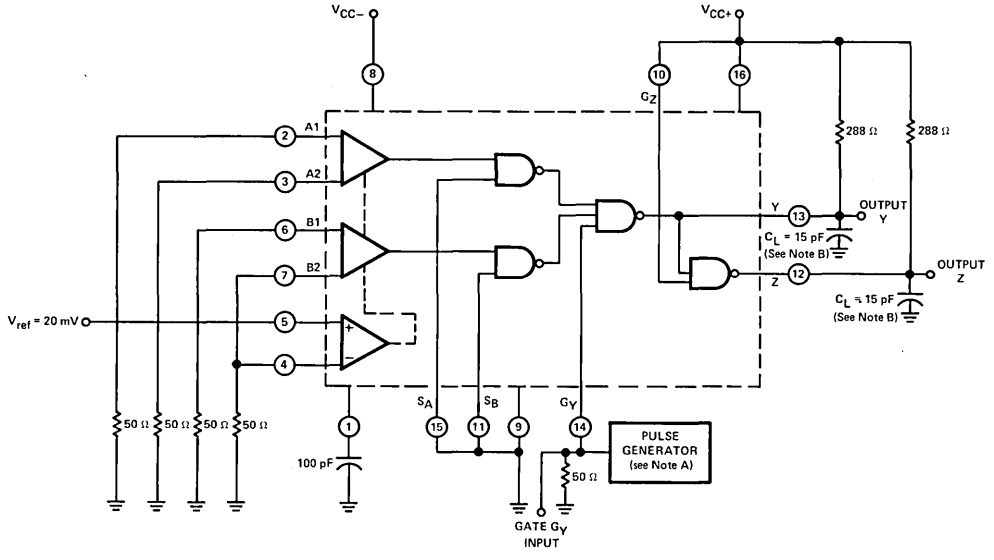
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.

C. C_L includes probe and jig capacitance.

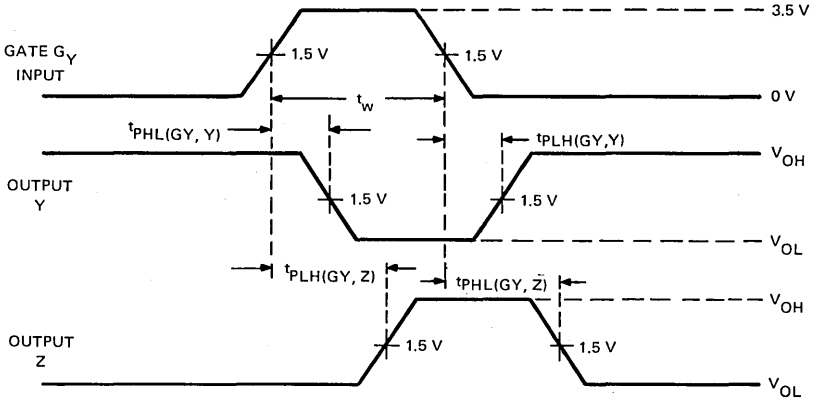
FIGURE 28–SN5520/SN7520 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 29–SN5520/SN7520 PROPAGATION DELAY TIMES FROM GATE G_Y

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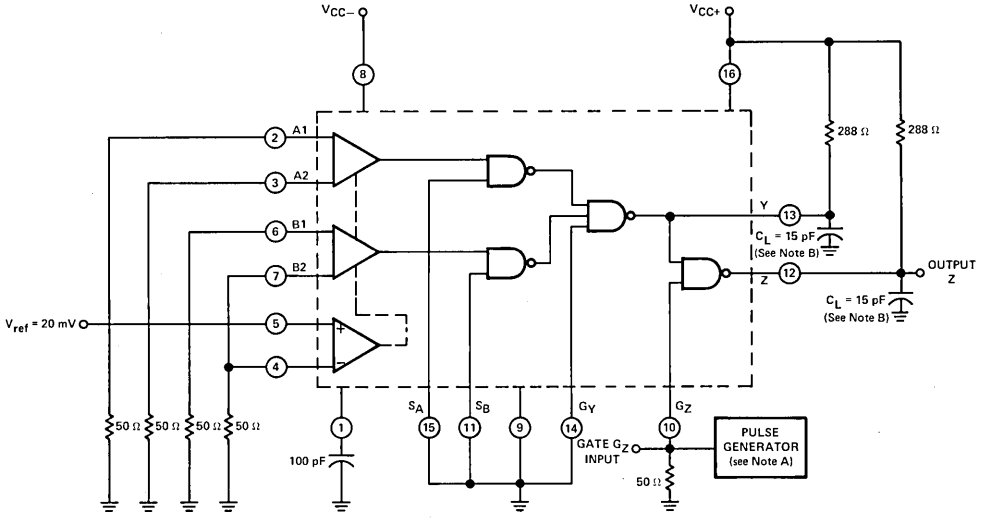
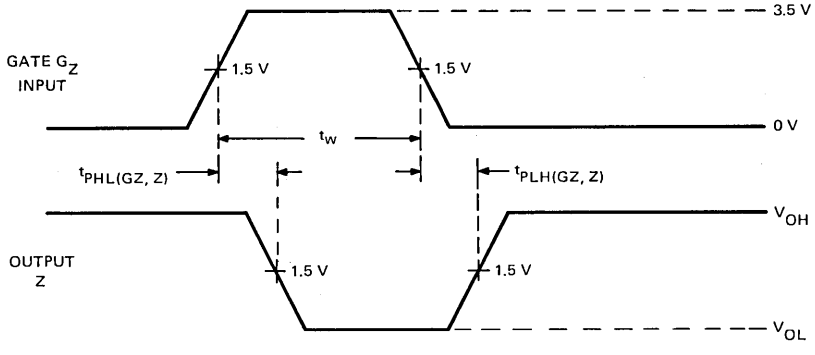
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



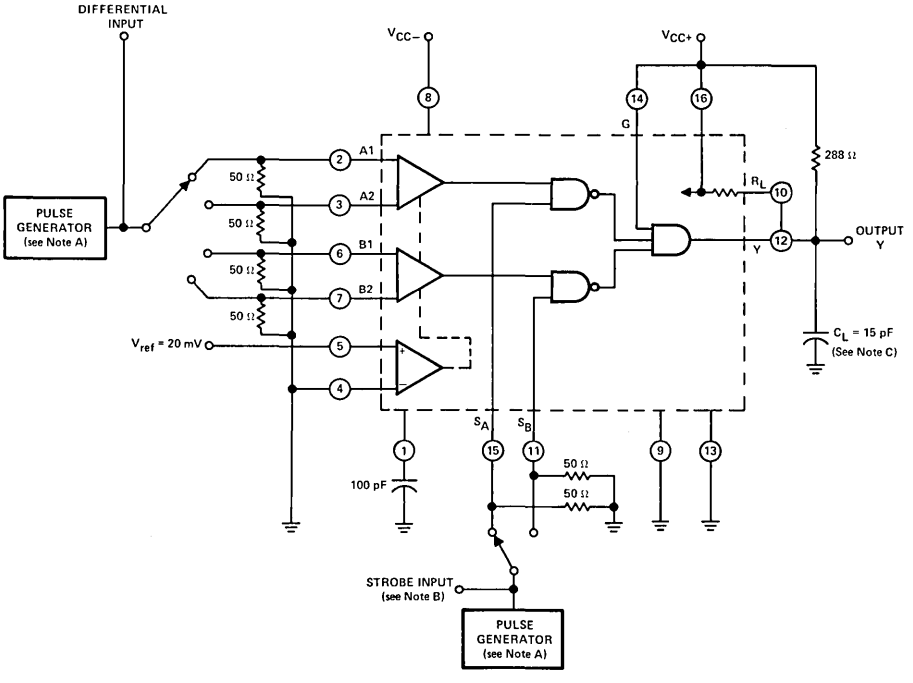
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

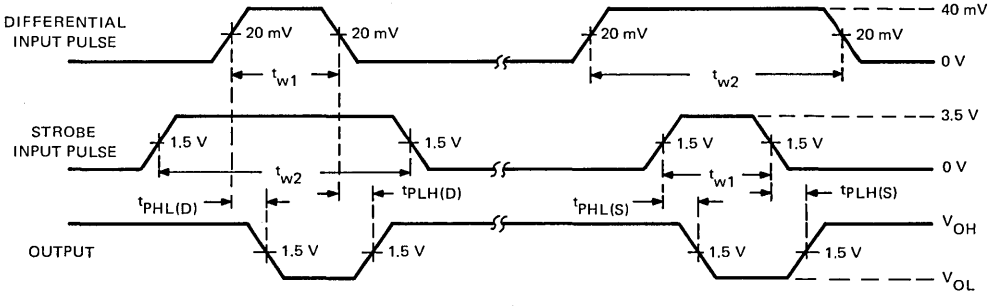
FIGURE 30–SN5520/SN7520 PROPAGATION DELAY TIMES FROM GATE G_Z

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe S_A when testing inputs A1-A2 and to Strobe S_B when testing inputs B1-B2.
C. C_L includes probe and jig capacitance.

FIGURE 31–SN5522/SN7522 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

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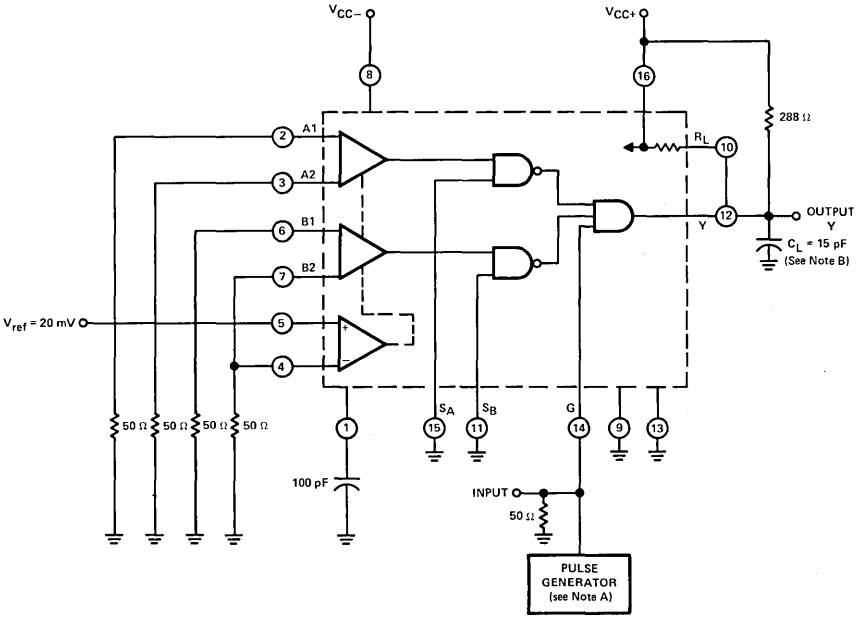
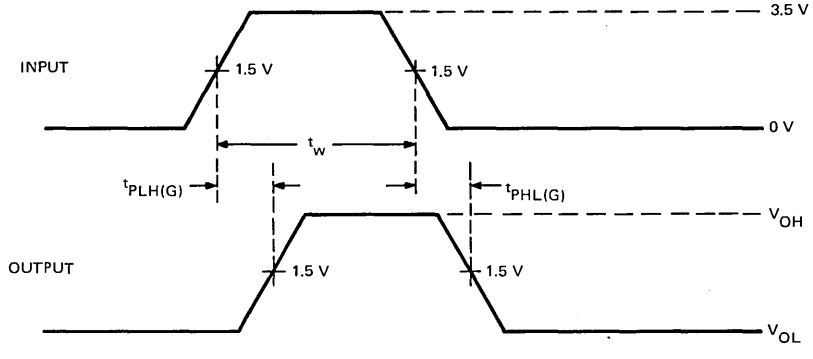
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



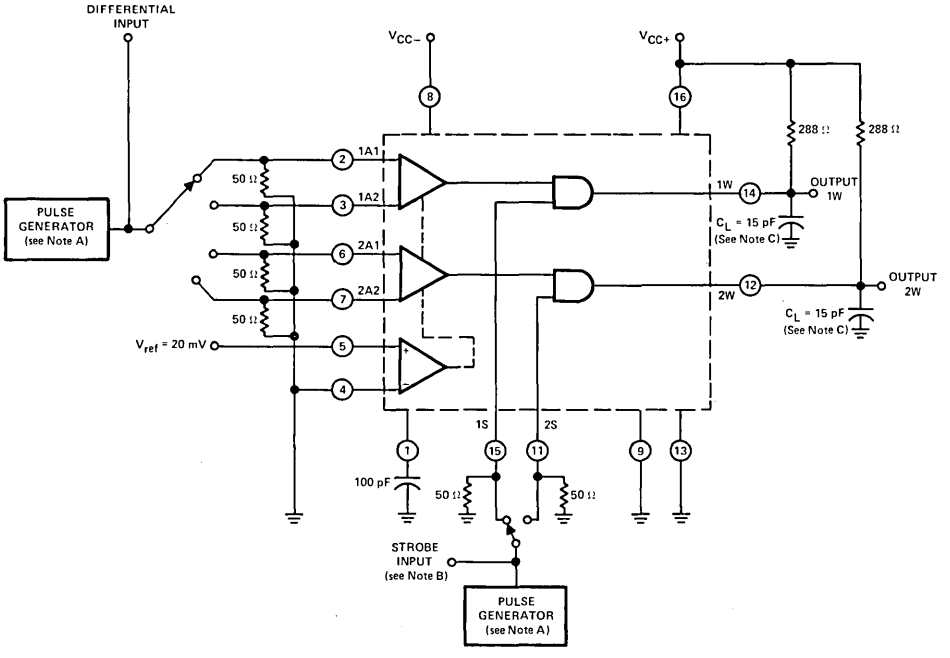
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_w = 100 ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

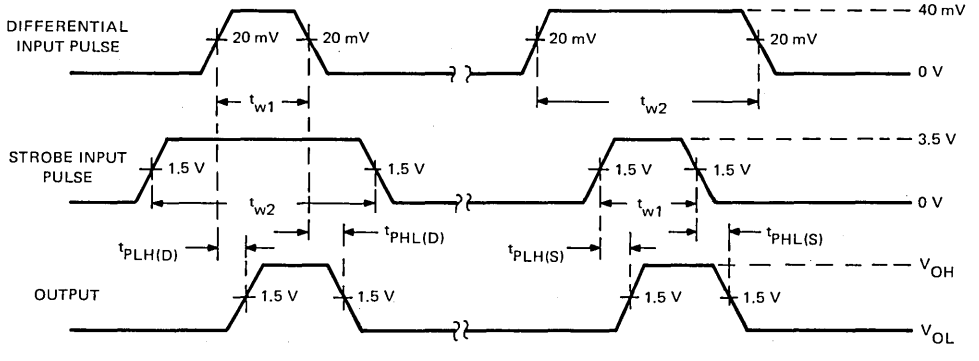
FIGURE 32–SN5522/SN7522 PROPAGATION DELAY TIMES FROM GATE INPUT

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

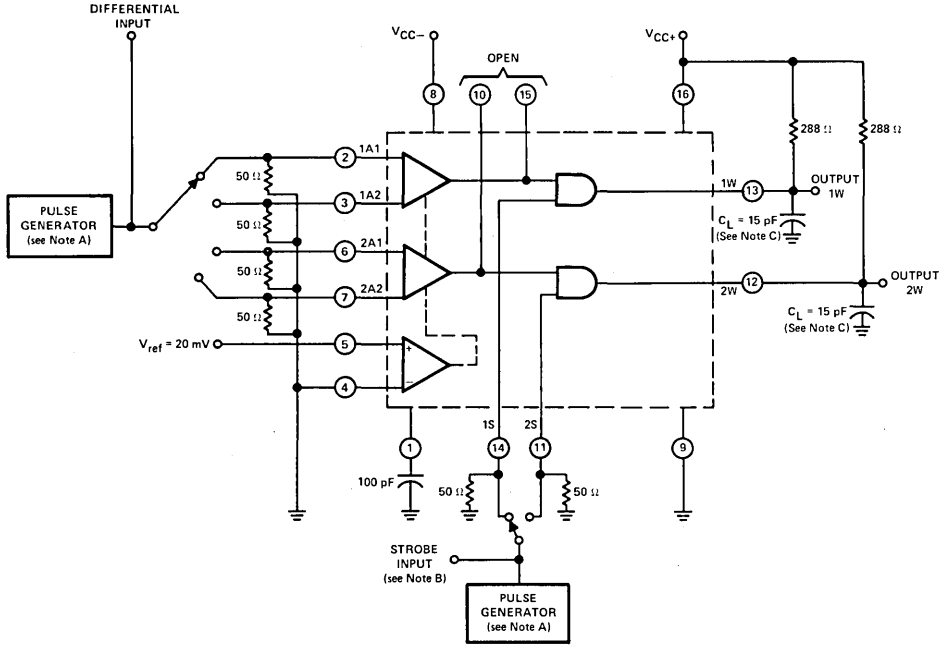
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.

C. C_L includes probe and jig capacitance.

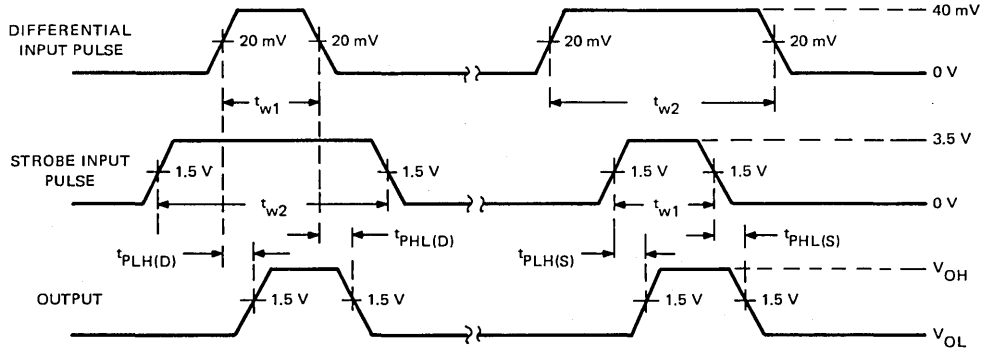
FIGURE 33–SN5524/SN7524 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

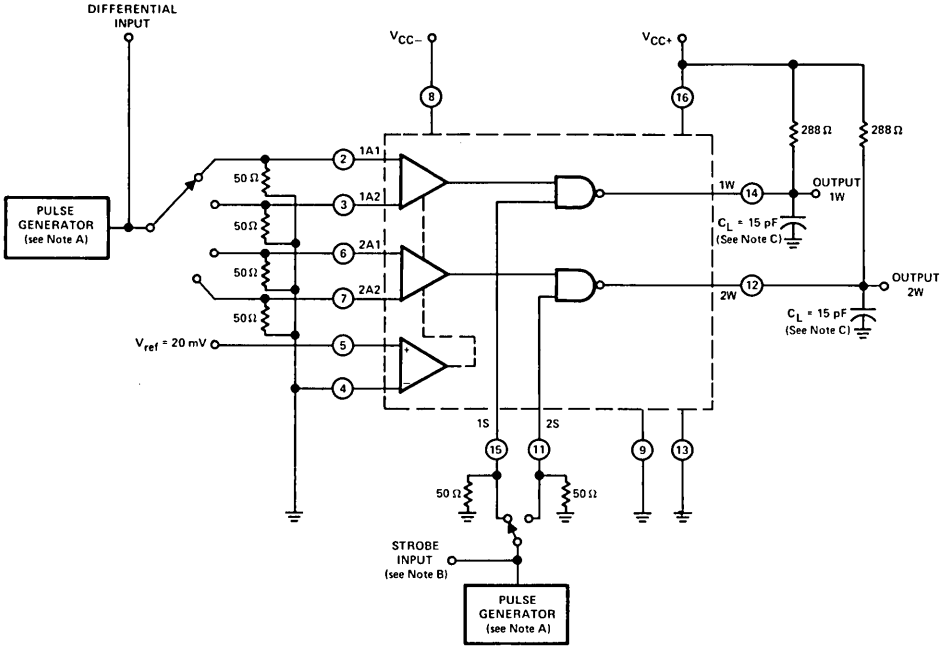
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

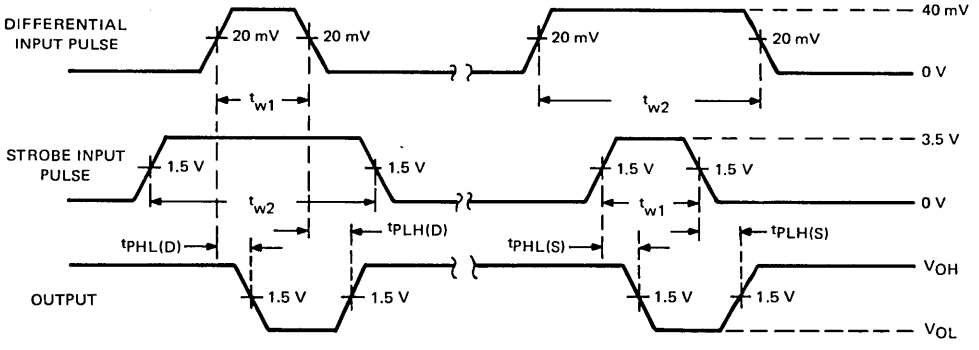
FIGURE 34–SN5528/SN7528 PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

FIGURE 35–SN55232, SN75232, SN55234, and SN75234 PROPAGATION DELAY TIMES

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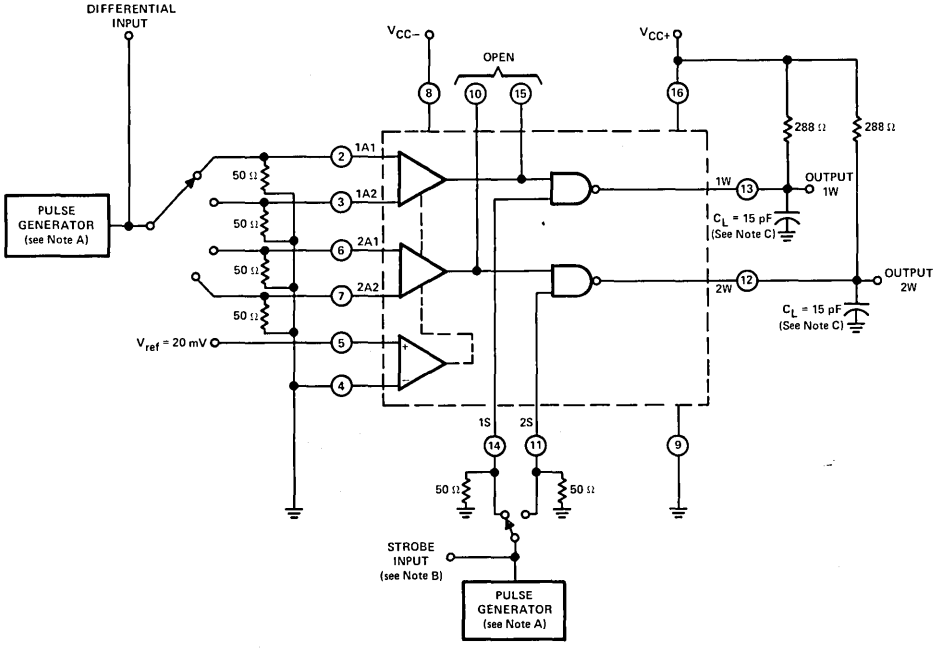
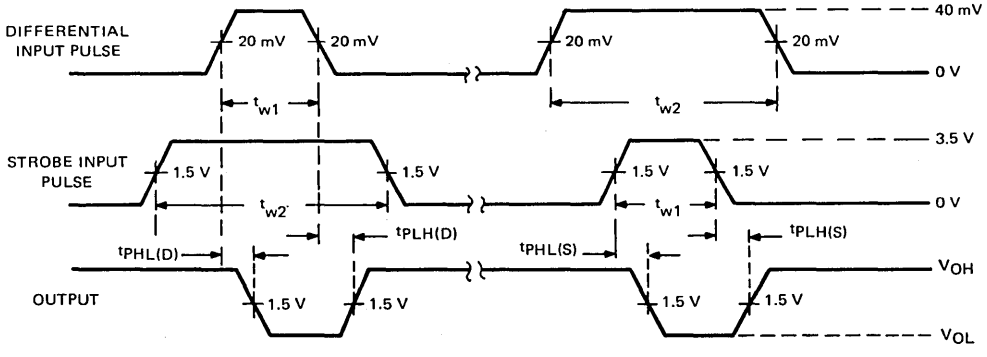
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2S2 are being tested.

C. C_L includes probe and jig capacitance.

FIGURE 36–SN55238/SN75238 PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

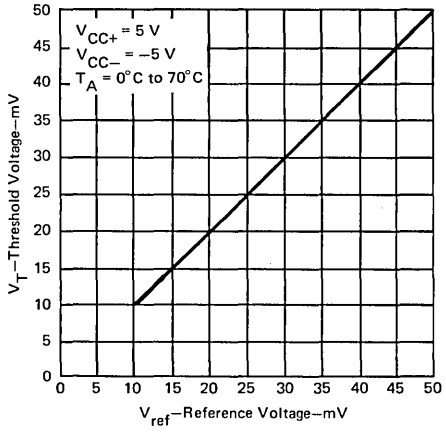


FIGURE 37

THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

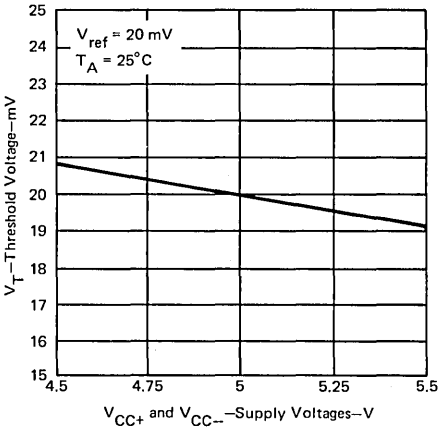


FIGURE 38

4

NORMALIZED THRESHOLD VOLTAGE
vs
PULSE REPETITION RATE

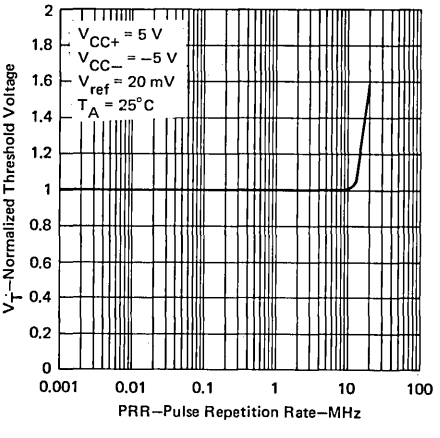


FIGURE 39

COMMON-MODE FIRING VOLTAGE
vs
FREE-AIR TEMPERATURE

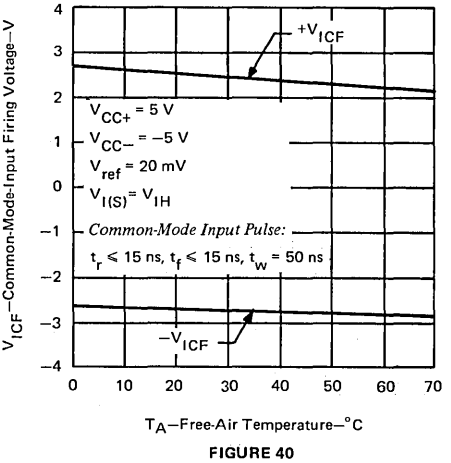


FIGURE 40

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TYPICAL CHARACTERISTICS

DIFFERENTIAL-INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

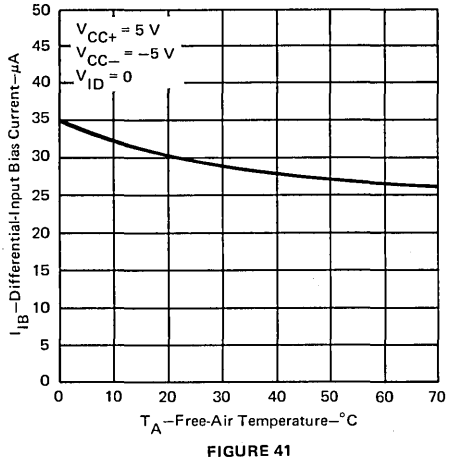

FIGURE 41

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

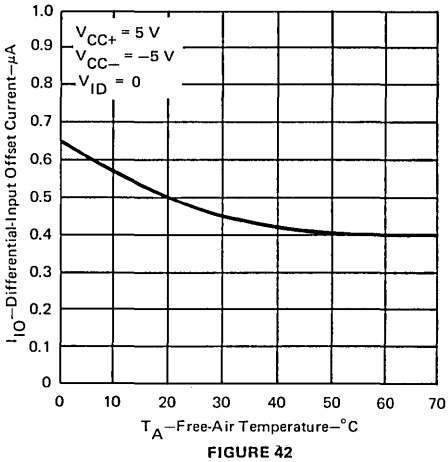

FIGURE 42

HIGH-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

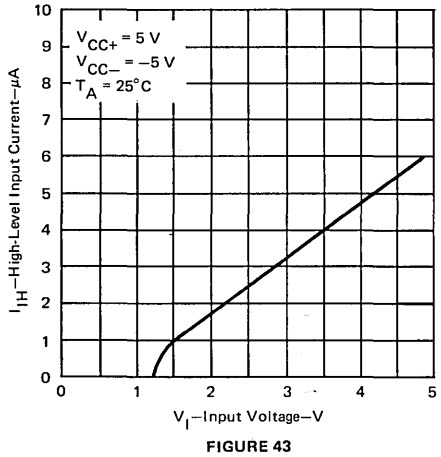

FIGURE 43

LOW-LEVEL INPUT CURRENT
vs
INPUT VOLTAGE

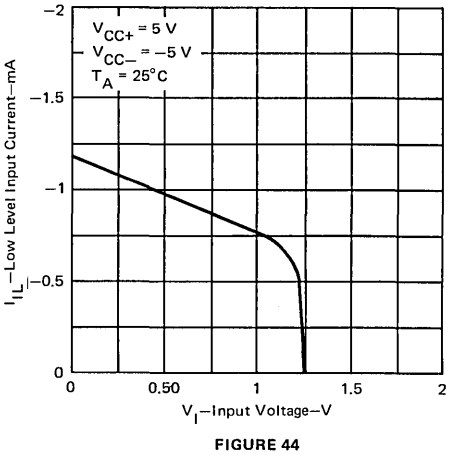

FIGURE 44

4

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

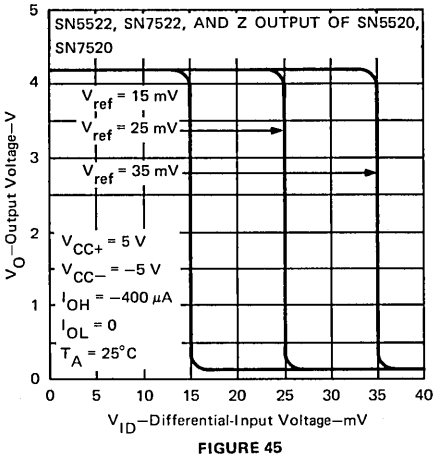

FIGURE 45

OUTPUT VOLTAGE
vs
DIFFERENTIAL-INPUT VOLTAGE

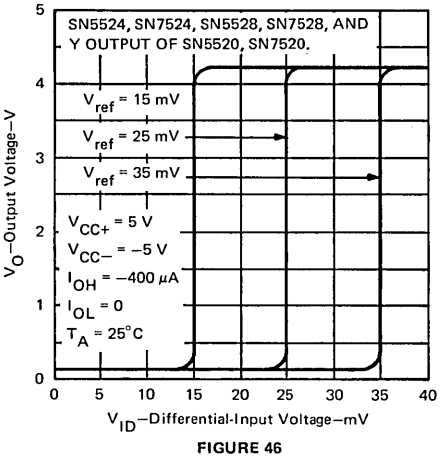

FIGURE 46

4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

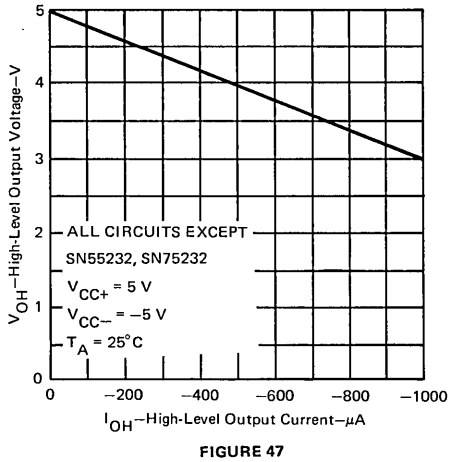

FIGURE 47

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

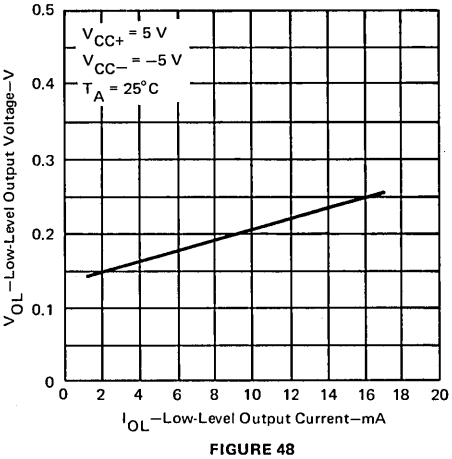

FIGURE 48

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APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54/74 loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54/74 loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the current.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure 49)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

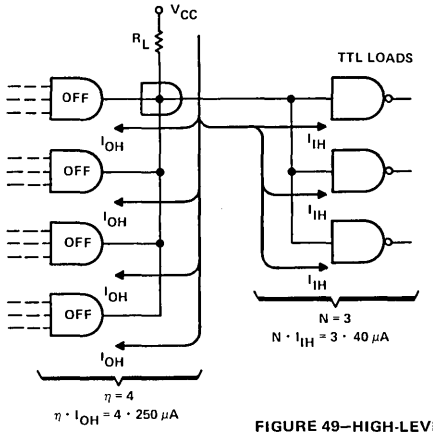
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of TTL loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\ \Omega = \frac{2.6}{0.00112}\ \Omega = 2321\ \Omega$$

FIGURE 49—HIGH-LEVEL CIRCUIT CONDITIONS

APPLICATION DATA

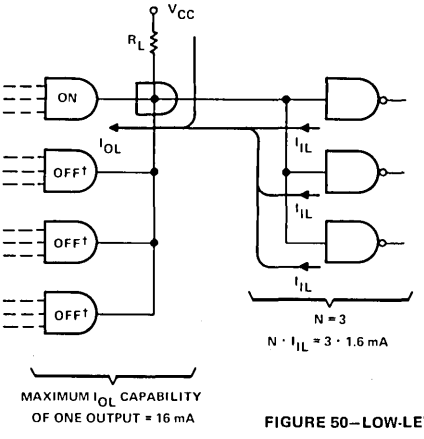
low-level (on-state) circuit calculations (see figure 50)

The current through the resistor must be limited to the maximum sink-current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 16 mA, the maximum current which will ensure a low-level maximum of 0.4 volt.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{OL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE 50—LOW-LEVEL CIRCUIT CONDITIONS

driving series 54/74 loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54/74 loads and wire-AND connecting two to seven parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond seven wire-AND connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54/74 loads, the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$); however, the use of a 4-kΩ resistor in this case will satisfy the high-level condition and limit the low level to less than 0.43 volt.

TABLE 1

FAN-OUT TO TTL LOADS	WIRE-AND OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6341	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	4000§
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

‡—All values shown in the table are based on:
High-level conditions: V_{CC} = 5 V, $V_{OH\ min}$ = 2.4 V
Low-level conditions: V_{CC} = 5 V, $V_{OL\ max}$ = 0.4 V
X—Not recommended or not possible.
§—The theoretical value is ∞. See explanation in text.

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TYPICAL APPLICATIONS

small memory systems

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN5524 or SN7524 sense amplifiers, see Figure 51. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

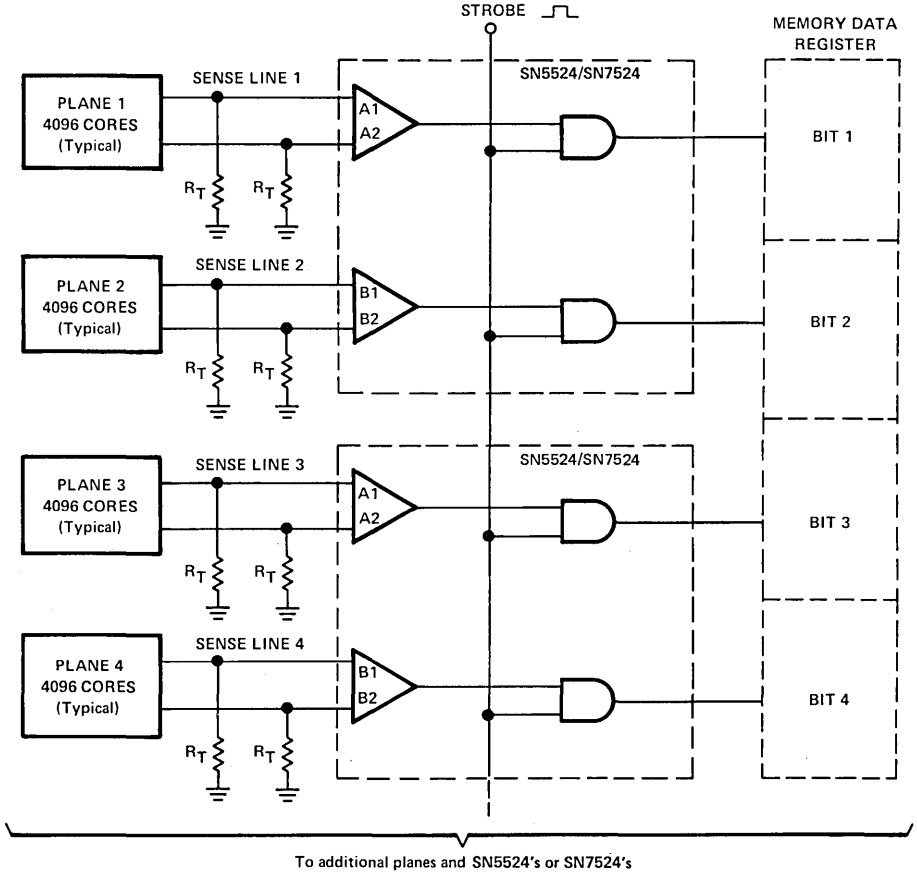

FIGURE 51–SENSING SMALL MEMORY SYSTEMS

TYPICAL APPLICATIONS (continued)

large memory systems

This application demonstrates an improved method of sensing data from large memory systems. The signal-to-noise ratio can be increased by sectioning the large core planes as illustrated in Figure 52. Two segments, usually consisting of 4096 cores each, can be interfaced by each of the dual-input channels of the SN5520/SN7520 or SN5522/SN7522 sense amplifiers. The cascaded output gates of the SN5520/SN7520 circuits may be connected to serve as the memory data register (MDR). A number of SN5522/SN7522 sense amplifiers may be wire-AND connected to expand the input function of the MDR to interface all the segments of the plane. Complementary outputs, clear, and preset functions are provided for the MDR. Rules for combined fan-out and wire-AND capabilities must be observed.

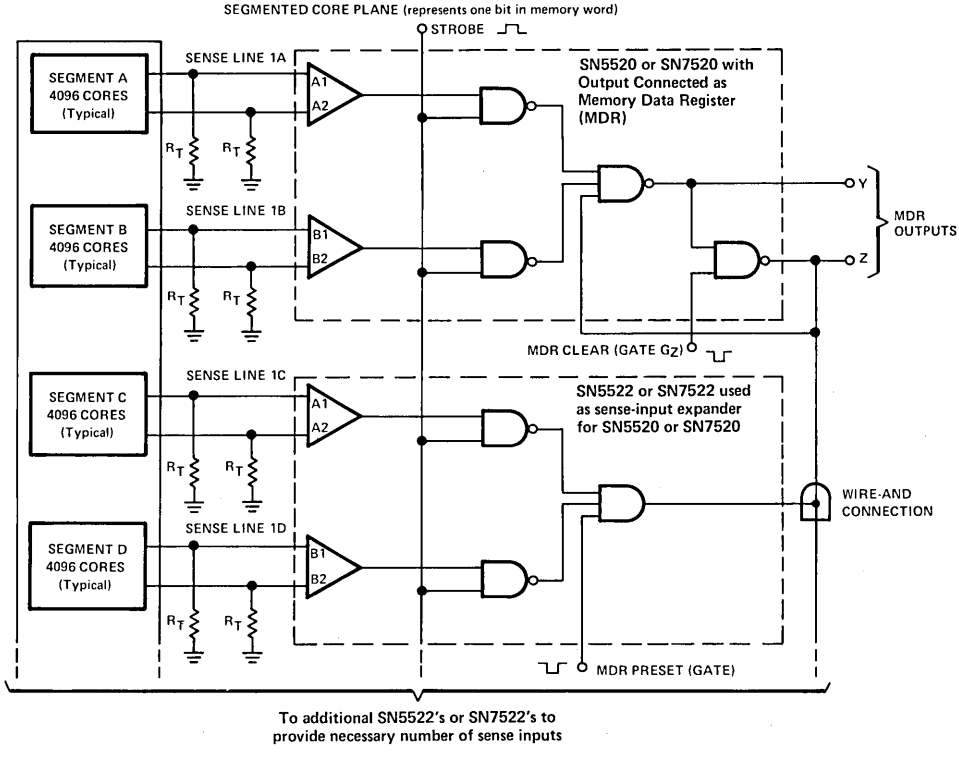

FIGURE 52–SENSING LARGE MEMORY SYSTEMS

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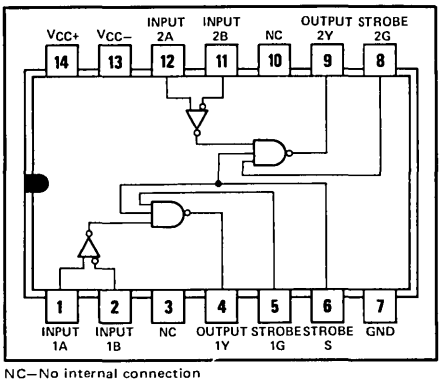
TYPES SN75207, SN75207B, SN75208, SN75208B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

BULLETIN NO. DL-S 7711793, JULY 1973—REVISED JANUARY 1977

- Plug-in Replacement for SN75107A, SN75107B, SN75108A, SN75108B with Improved Characteristics
- ±10 mV Guaranteed Input Sensitivity
- TTL Compatible
- Standard Supply Voltages . . . ±5 V
- Differential Input Common-Mode Voltage Range of ±3 V
- Strobe Inputs for Channel Selection
- '207 and '207B Have Totem-Pole Outputs
- '208 and '208B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN75207, SN75207B, SN75208, and SN75208B are pin-for-pin replacements for the SN75107A, SN75107B, SN75108A, and SN75108B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output. The '208 and '208B each features an open-collector output that permits wired-AND logic connections with similar output configurations. These devices are designed for operation from 0°C to 70°C and are available in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

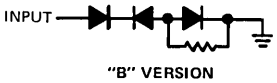
FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} <$ 10 mV	X	L	H
	L	X	H
	H	H	INDETERMINATE
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

The essential difference between the unsuffixed and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

UNSUFFIXED VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

TYPES SN75207, SN75207B, SN75208, SN75208B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

design characteristics

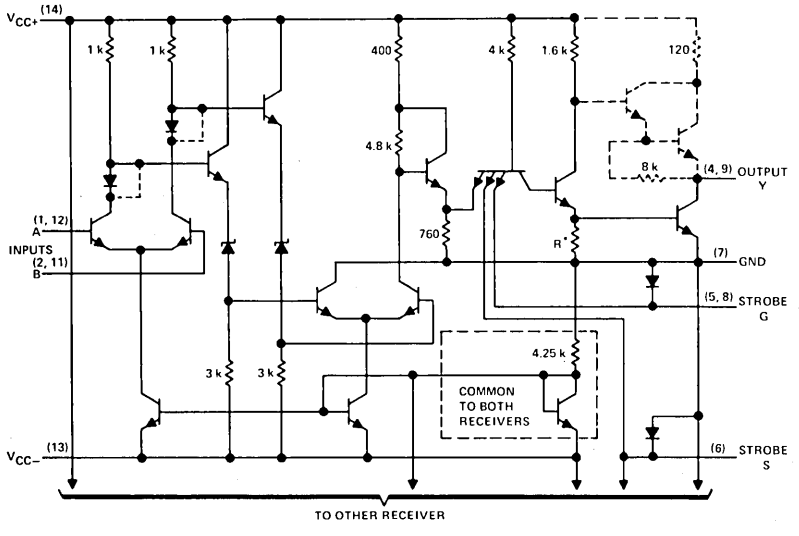
The '207, '207B, '208, and '208B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

schematic (each receiver)



*R = 1 kΩ for '207 and '207B, 750 Ω for '208 and '208B.

NOTES: A. Resistor values shown are nominal and in ohms.

B. Components shown with dashed lines in the output circuitry are applicable to the '207 and '207B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '207 and '208.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	7 V
Supply voltage V_{CC-}	−7 V
Differential input voltage (see Note 2)	±6 V
Common-mode input voltage (see Note 3)	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

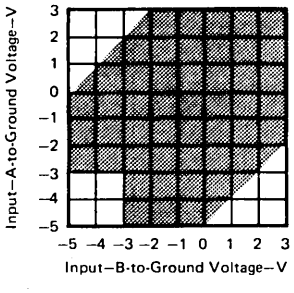
recommended operating conditions (see note 4)

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.75	−5	−5.25	V
Low-level output current, I_{OL}			−16	mA
Differential input voltage, V_{ID} (see Note 5)	−5†		5	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	−3†		3	V
Input voltage range, any differential input to ground (see Note 5)	−5†		3	V
Operating free-air temperature	0		70	°C

†The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure at the right.
6. The common-mode voltage may be as low as −4 V provided that one of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS
OF INPUT VOLTAGES



definition of input logic levels†

		MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	0.01	5	V
V_{IDL}	Low-level input voltage between differential inputs	−5	−0.01	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	0	0.8	V

†The algebraic convention, where the more positive (less negative) limit is designated maximum, is used in this data sheet with logic input voltage levels only.

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		'207, '207B MIN	'207, '207B TYP§	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP§	'208, '208B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, V_{IDH} = 10 mV, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V		2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, V_{IDL} = −10 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current¶		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'207, '207B MIN	'207, '207B TYP	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP	'208, '208B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 15 pF, See Figure 1			35			35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B				20			20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S				17			17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S				17			17	ns

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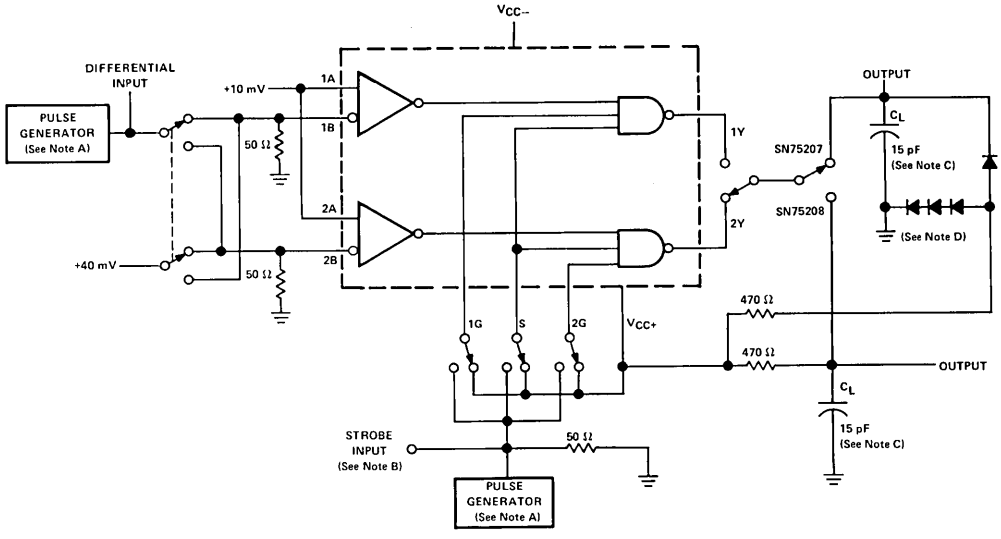
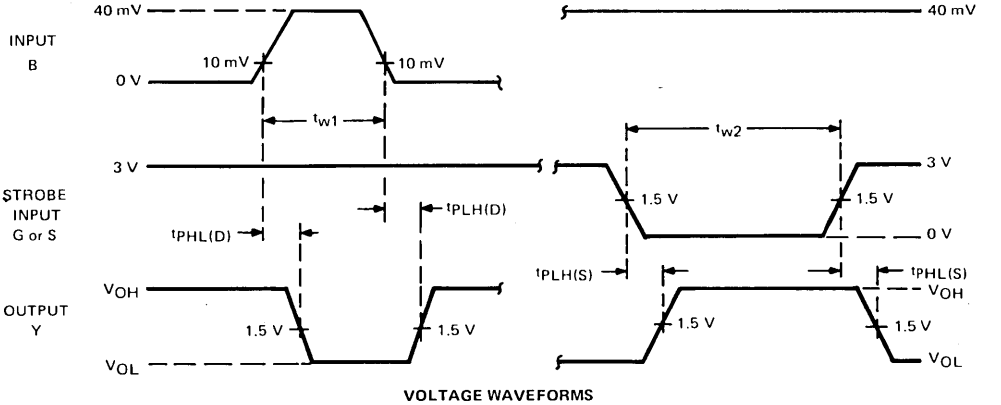
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} = 50\ \Omega$, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $t_{w1} = 500$ ns with PRR = 1 MHz, $t_{w2} = 1$ ms with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL APPLICATION DATA

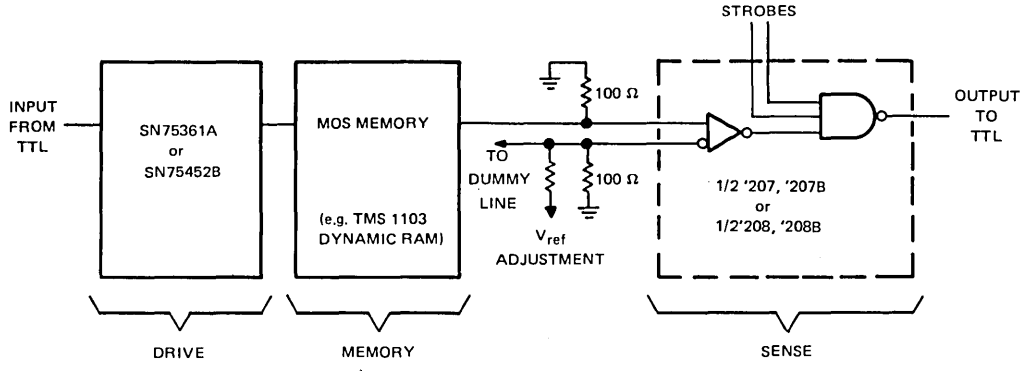
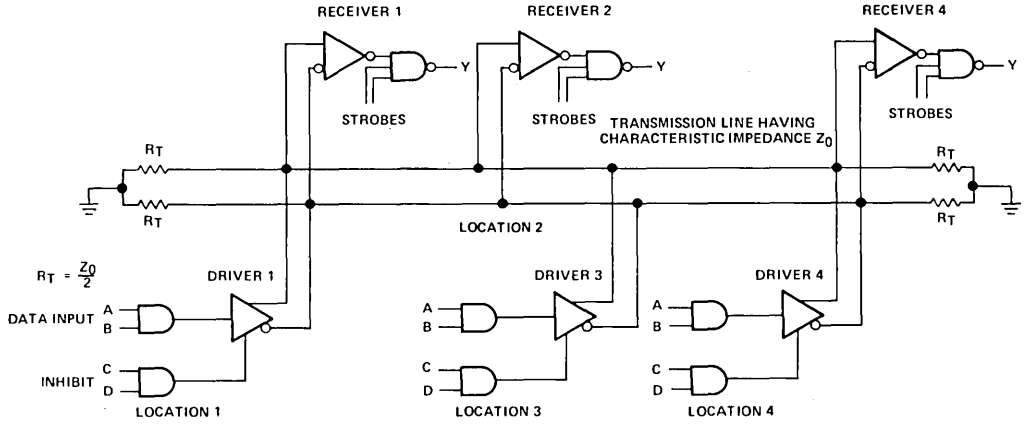


FIGURE 2–MOS MEMORY SENSE AMPLIFIER



Receivers are '207, '207B, '208, or '208B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

FIGURE 3–DATA-BUS OR PARTY-LINE SYSTEM

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

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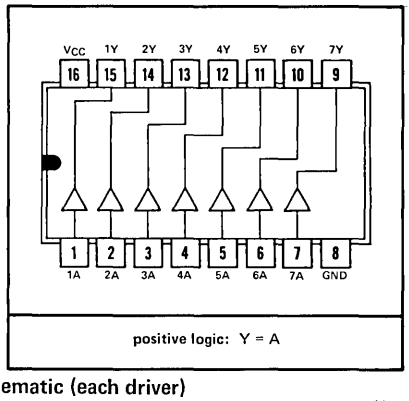
TYPE SN75270
7-UNIT MOS-TO-TTL CONVERTER AND THERMAL PRINTHEAD DRIVER ARRAY

BULLETIN NO. DL-S 7712061, SEPTEMBER 1973—REVISED APRIL 1977

- 7 Single-Ended Noninverting Drivers Per Package
- Inputs Compatible with MOS
- TTL-Compatible Outputs
- Single 5-V Supply

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

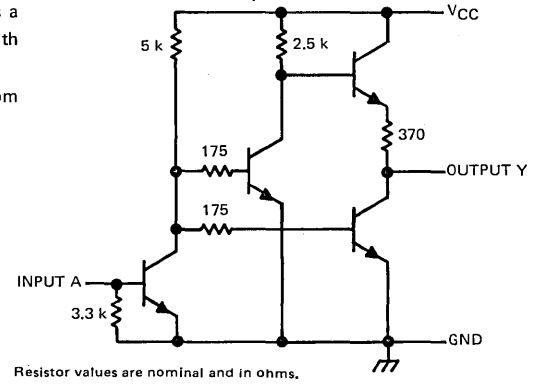


description

The SN75270 is a monolithic integrated circuit designed for use as a sense amplifier or thermal printhead driver. As a sense amplifier, the device can be used to convert from MOS to TTL levels. As a thermal printhead driver, this device is used with EPN3600-type thermal printheads.

The SN75270 is characterized for operation from 0°C to 70°C.

schematic (each driver)



Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input current	4 mA
Continuous total dissipation	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input current, I_{IH}	0.5		2	mA
Low-level input current, I_{IL}	0		0.1	mA
Operating free-air temperature, T_A	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

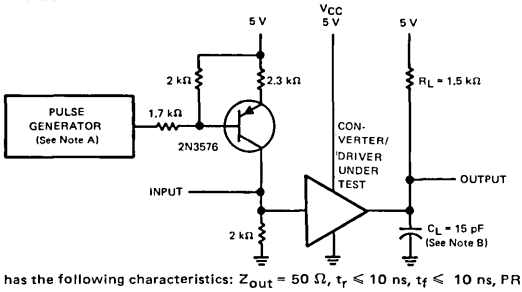
electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	V_{CC} = 4.75 V, I_{IH} = 500 μA, I_{OH} = −80 μA	2.4			V
V_{OL} Low-level output voltage	V_{CC} = 4.75 V, I_{IL} = 100 μA, I_{OL} = 3.2 mA			0.4	V
I_{OH} High-level output current	V_{CC} = 4.75 V, I_{IH} = 500 μA, V_O = 1 V	−5			mA
	V_{CC} = 5.25 V, I_{IH} = 500 μA, V_O = 0.25 V			−15	mA
I_{CCL} Total supply current, all outputs low	V_{CC} = 5 V, I_{IL} = 100 μA, I_O = 0		20	35	mA

switching characteristics, T_A = 25°C

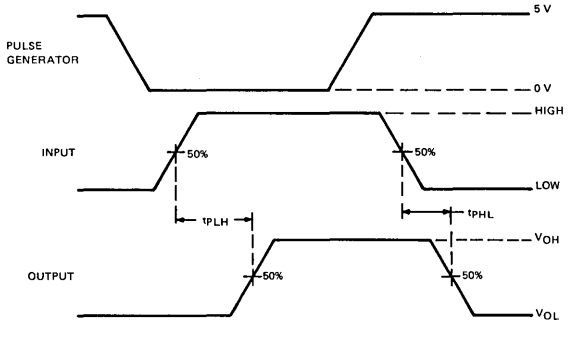
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	V_{CC} = 5 V, C_L = 15 pF,		30		ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 1.5 kΩ, See Figure 1		8		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns, PRR = 500 kHz, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

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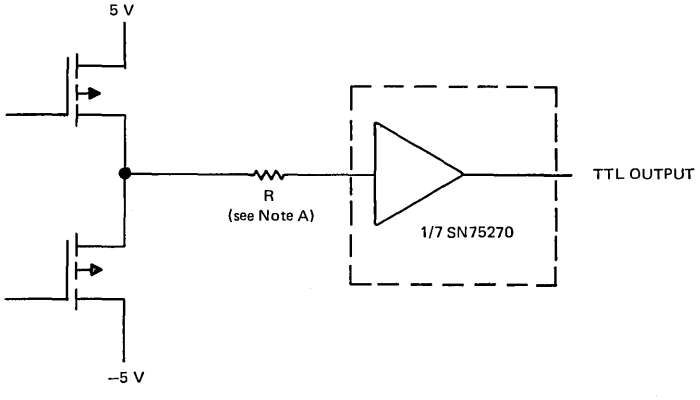
TYPICAL APPLICATION DATA



Note A: $R = \dfrac{V_{OH} - V_{BE}}{I_{OH}}$

V_{OH} = High-level output voltage of MOS device
V_{BE} = Base-Emitter voltage of input transistor of SN75270
I_{OH} = High-level output current of MOS device

example: let $V_{OH} = 4$ V
$I_{OH} = 1$ mA
$V_{BE} = 0.7$ V

$$R = \frac{4 - 0.7}{1} = 3.3\ k\Omega$$

FIGURE 2–MOS TO SN75270 CONNECTION

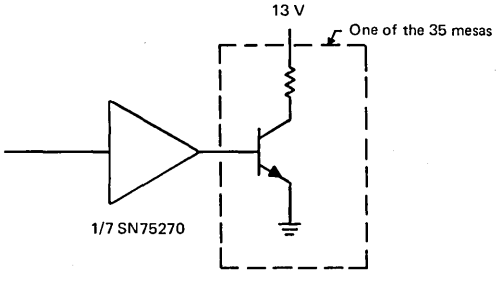


FIGURE 3–THERMAL PRINTHEAD DRIVER FOR THE EPN3600 THERMAL PRINTHEAD

MOS Drivers

MOS DRIVERS

INPUT COMPATIBILITY	POWER SUPPLIES (Nominal)	t_{PD}¶ TYPICAL	V_{OH} (MIN)	V_{OL} (MAX)	DEVICE TYPE	PACKAGE TYPE	DRIVERS PER PACKAGE	ADDITIONAL FEATURES	PAGE NO.
ECL 10K	V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_{EE} = −5.2 V	33 ns	V_{CC2} − 0.3 V	0.3 V	SN75368	J,N	2	• Compatible with many popular MOS RAMs including the TMS 1103, TMS 1103-1, TMS 4030, and 7001 • ECL to MOS/TTL driver	155
	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{EE} = −5.2 V, V_{BB} = −1.3 V	44 ns	V_{CC2} − 0.4 V	0.5 V	SN75320	J,N	2	• Compatible with the TMS 4030 4K RAM and other popular MOS RAMs • Fixed ECL input reference voltage (SN75321) • External reference voltage (SN75320) • Requires two external P-N-P transistors for operation	100
					SN75321	J,N			
TTL	V_{CC1} = 5 V, V_{CC2} = 12 V	20 ns	V_{CC2} − 1.6 V	0.5 V	SN75367	J,N	4	• CMOS applications • 3-state output • Separate address and enable/disable inputs for each driver	151
	V_{CC1} = 5 V, V_{CC2} = 12 V	25 ns	V_{CC2} − 1.6 V	1.3 V	*SN75357	J,N	4	• CMOS applications • Very low transient current during switching • 3-state output • Separate address and enable/disable inputs for each driver	117
	V_{CC1} = 5 V, V_{CC2} = 20 V	31 ns	V_{CC2} − 0.3 V	0.3 V	*SN75375	J,N	4	• Compatible with many popular MOS RAMs • Individual V_{CC2} supplies for each driver • Two drivers have single inputs; two have dual inputs	187
	V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V	31 ns	V_{CC2} − 0.3 V	0.3 V	SN75365	J,N	4	• Compatible with many MOS RAMs including the TMS 1103, TMS 4062, and TMS 4070 16K RAM • V_{CC2} variable from 5 V to 24 V	136
	V_{CC1} = 5 V, V_{CC2} = 12 V	31 ns	V_{CC2} − 0.4 V	0.5 V	SN75322	J,N	2	• Compatible with most popular MOS RAMs • Separate driver address inputs with common strobe • Requires two external P-N-P transistors for operation • Low standby power	105

¶ t_{PD} = Propagation delay time
*Future product

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MOS DRIVERS (continued)

INPUT COMPATIBILITY	POWER SUPPLIES (Nominal)	t_{PD}¶ TYPICAL	V_{OH} (MIN)	V_{OL} (MAX)	DEVICE TYPE	PACKAGE TYPE	DRIVERS PER PACKAGE	ADDITIONAL FEATURES	PAGE NO.
TTL	V_{CC1} = 5 V, V_{CC2} = 15 V	31 ns	V_{CC2} – 1 V	0.3 V	SN75350	JG,P	2	• Compatible with many popular MOS RAMs • Lower-voltage, high-speed version of the SN75361A • V_{CC2} variable from 5 V to 18 V	109
	V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V	32 ns	V_{CC2} – 0.3 V	0.3 V	SN75355	J,N	4	• Compatible with many popular MOS RAMs • Low-voltage version of the SN75365 • V_{CC2} variable from 5 V to 18 V	113
	V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V	33 ns	V_{CC2} – 0.3 V	0.3 V	SN75366	J,N	4	• Compatible with many popular MOS RAMs • Equivalent to the SN75365 with internal output damping resistor	145
	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V	33 ns	V_{CC2} – 0.3 V	0.5 V	SN75363	J,N	2	• Compatible with many MOS RAMs including the TMS 4030 4K RAM and TMS 4070 16K RAM • Separate driver address inputs with common strobe • V_{CC2} variable from 5 V to 15 V	127
	V_{CC1} = 20 V, V_{CC2} = 24 V	34 ns	V_{CC2} – 0.3 V	0.3 V	SN75364	JG,P	2	• Compatible with many popular MOS RAMs and shift registers • Single-ended inverting drivers	131
	V_{CC} = 20 V	35 ns	V_{CC} – 1 V	0.3 V	SN75369	JG,P	2	• Compatible with many popular MOS RAMs and MOS shift registers • Single-ended inverting drivers	163
	V_{CC1} = 5 V, V_{CC2} = 20 V	36 ns	V_{CC2} – 1 V	0.3 V	SN75361A	JG,P	2	• Compatible with many popular MOS RAMs including the TMS 1103, TMS 4062, and TMS 4070 16K RAM • V_{CC2} variable from 5 V to 24 V	118
	V_{SS} = 20 V, V_{REF} = 7 V	80 ns			SN75370	J,N	2	Dual read/write amplifier that is designed to interface with I/O terminals of the TMS 4062 and similar type MOS RAMs	169
	V_{CC1} = 5 V, See features for V_{CC2} and V_{CC3}	85 ns	V_{CC3} – 0.2 V	V_{CC2}+2 V	SN55180	L	2	• Compatible with all MOS devices • 31 V maximum output swing • V_{CC2} variable from –8 V to –25 V • V_{CC3} variable from –20 V to 25 V	97
					SN75180	L			

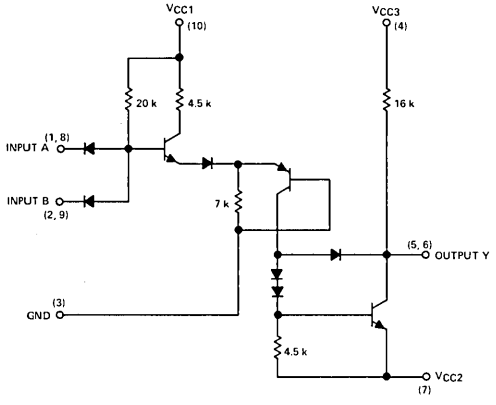
¶ t_{PD} = Propagation delay time

TYPES SN55180, SN75180
DUAL NAND TTL-TO-MOS LEVEL CONVERTERS

BULLETIN NO. DL-S 7311765, AUGUST 1972 – REVISED SEPTEMBER 1973

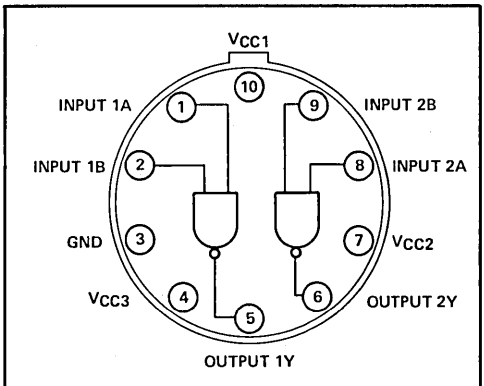
- Output Compatible with All MOS Devices
- Inputs Fully Compatible with Most TTL and DTL Circuits
- Designed to be Interchangeable with National Semiconductor DS7800 and DS8800
- Standard 5 V Logic Supply Voltage
- Variable V_{CC2} and V_{CC3} Supply Voltages
- 31-Volt Maximum Output Swing
- 1 mW Dissipation with Output at High Level

schematic



Resistor values shown are nominal and in ohms.

L
PLUG-IN PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

description

The SN55180 and SN75180 are dual voltage-level converters designed for interfacing between TTL or DTL voltage levels and those levels associated with high-impedance junction or MOS FET-type devices. These devices offer the system designer the flexibility of tailoring the output voltage swing to his application. This can be accomplished by varying the V_{CC2} and V_{CC3} supply voltage within the ranges shown in Figure 1. Typical applications include interfacing with MOS shift registers and analog gates.

The SN55180 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN75180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC1} (see Note 1)	7 V
Supply voltage V_{CC2} (see Note 1)	–30 V
Supply voltage V_{CC3} (see Note 1)	30 V
V_{CC3} to V_{CC2} voltage differential	40 V
Input voltage (see Note 1)	5.5 V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 2)	300 mW
Operating free-air temperature range: SN55180 Circuits	–55°C to 125°C
SN75180 Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds	300°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation of the SN55180 above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19.

recommended operating conditions

	SN55180			SN75180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC2} (See Figure 1)	−8		−25	−8		−25	V
Supply voltage, V_{CC3} (See Figure 1)			+25 −20			+25 −20	V
Operating free-air temperature, T_A	−55		125	0		70	°C

Figure 1 shows the boundary conditions within which it is recommended that the SN55180 and SN75180 be operated for proper functioning of these converters. The range of operation for supply V_{CC2} is shown on the horizontal axis. V_{CC2} must be between −25 V and −8 V. The allowable range for V_{CC3} is governed by V_{CC2}. After a value for V_{CC2} has been chosen, V_{CC3} may be selected as any value along a vertical line passing through the V_{CC2} value and terminated by the boundaries of the recommended operating region. A voltage difference between supplies of at least 5 volts should be maintained for adequate output voltage swing.

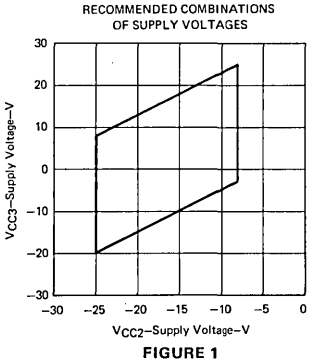


FIGURE 1

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see note 3)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC1} = MIN, V_I = 0.8 V, I_{OH} = 0	V_{CC3}−0.2			V
V_{OL}	Low-level output voltage	V_{CC1} = MIN, V_I = 2 V			V_{CC2}+2	V
$R_{pull\text{-}up}$	Output pull-up resistor (internal)	T_A = 25°C	11.5	16	20	kΩ
I_{IH}	High-level input current	V_{CC1} = MAX, V_I = 2.4 V			5	μA
I_I	Input current at maximum input voltage	V_{CC1} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current	V_{CC1} = MAX, V_I = 0.4 V		0.2	0.4	mA
$I_{CC1(H)}$	Supply current from V_{CC1}, outputs high (both converters)	V_{CC1} = MAX, all inputs at 0 V, outputs open		440	820	μA
$I_{CC1(L)}$	Supply current from V_{CC1}, outputs low (both converters)	V_{CC1} = MAX, all inputs at 4.5 V, outputs open		1.7	3.2	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, outputs high (both converters)	V_{CC3} = MAX, all inputs at 0.8 V, outputs open			20	μA

NOTE 3: Minimum and maximum limits apply for all allowable values of V_{CC2} and V_{CC3}.

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	2	C_L = 15 pF, See Figure 2		85		ns
t_{PHL}	Propagation delay time, high-to-low-level output		C_L = 15 pF, See Figure 2		85		ns

‡All typical values are at V_{CC1} = 5 V, V_{CC2} = −22 V, V_{CC3} = 8 V, T_A = 25°C.

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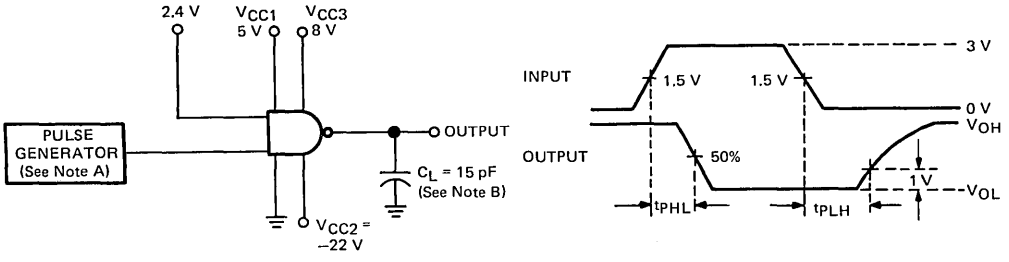
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_r = 10 ns, t_f = 10 ns, PRR = 500 kHz, t_w = 500 ns.
B. C_L includes probe and jig capacitance.

FIGURE 2

TYPICAL CHARACTERISTICS†

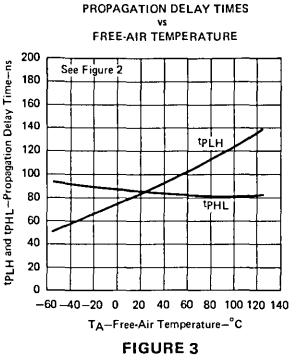


FIGURE 3

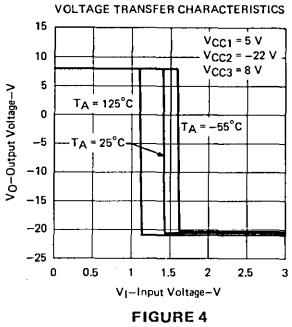


FIGURE 4

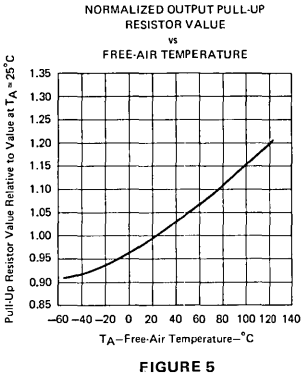


FIGURE 5

†Data for temperatures below 0°C and above 70°C is applicable to SN55180 circuits only.

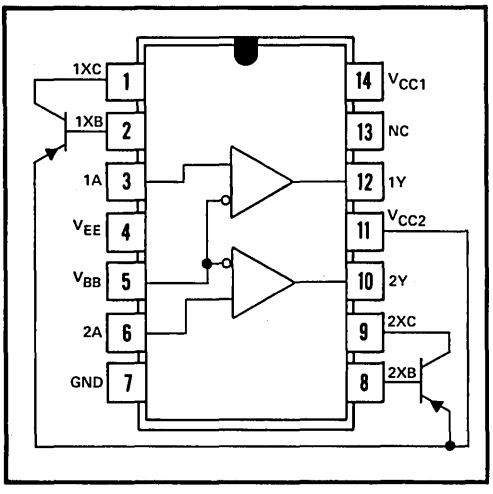
TYPES SN75320, SN75321 DUAL ECL-TO-MOS DRIVERS

BULLETIN NO. DL-S 7712473, APRIL 1977

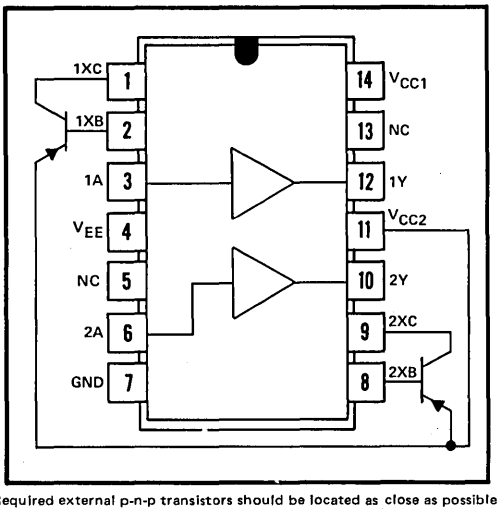
MOS MEMORY INTERFACE

- Dual ECL-to-MOS Drivers
- Versatile Interface Circuit for Use Between ECL and High-Current, High-Voltage Systems
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- Inputs Compatible with Series 10000 ECL and Other Similar ECL Families
- Compatible with Many Popular MOS RAMs
- Negligible 12-V Supply Current and Low 5-V Supply Current when Output is at a Low Level
- Requires 2 External P-N-P Transistors per Package for Operation (Use of TIS149, A5T4260, or A5T4261 Recommended)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
SN75320



SN75321



Required external p-n-p transistors should be located as close as possible to the SN75320/SN75321.
NC—No internal connection

description

The SN75320 and SN75321 are monolithic dual ECL-to-MOS driver interface circuits. The devices accept standard input signals from Series 10000 ECL and other similar ECL families and provide high-current, high-voltage output levels suitable for driving MOS circuits. Due to the low power dissipation when the driver output is at a low level, these devices are ideal for driving N-channel RAMs such as the 4-k TMS 4030.

The SN75320 and SN75321 operate from a standard TTL V_{CC} supply (V_{CC1}), ECL V_{EE} supply (V_{EE}), and the MOS V_{SS} supply (V_{CC2}). These devices have been optimized for operation with a V_{CC2} supply voltage from 12 volts to 15 volts, but they are designed to be usable over a much wider range of V_{CC2}.

Both devices require two external p-n-p transistors per package. Suggested p-n-p transistors are TIS149, A5T4260, and A5T4261. The SN75320 requires an externally generated ECL input reference voltage, V_{BB}, while the SN75321 features an internally fixed ECL input reference voltage, V_{BB}, of $-1.3\ V \pm 10\%$. The SN75320 can also be used with differential inputs. Both devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

H = high level, L = low level

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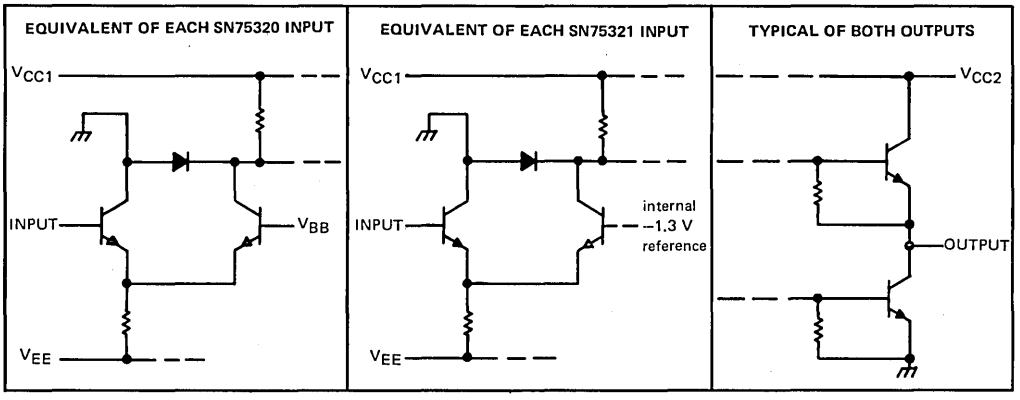
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 15 V
Supply voltage range of V_{EE} . . . . . −8 V to 0.5 V
Negative voltage of V_{CC1} or V_{CC2} with respect to V_{EE} . . . . . −0.5 V
Input voltage range . . . . . −8 V to 0.5 V
Input voltage with respect to V_{BB} (SN75320) . . . . . 5.5 V
Negative voltage at any input with respect to V_{EE} . . . . . −5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75320 and SN75321 chips are glass-mounted.

recommended operating conditions

	SN75320			SN75321			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	4.75	12	15	V
Supply voltage, V_{EE}	−4.68	−5.2	−5.72	−4.68	−5.2	−5.72	V
Supply voltage, V_{BB}	−1.23	−1.3	−1.37				V
Operating free-air temperature, T_A	0		70	0		70	°C
Load capacitance, C_L	200			200			pF

definition of input logic levels (see Note 3)

PARAMETER		SN75320 B (LEAST POSITIVE)	SN75320 A (MOST POSITIVE)	SN75321 B (LEAST POSITIVE)	SN75321 A (MOST POSITIVE)	UNIT
V_{IH}	High-level input voltage at input A	−1.15	−0.7	−0.9	−0.7	V
V_{IL}	Low-level input voltage at input A	V_{EE}	−1.45	V_{EE}	−1.6	V
	High-level differential input voltage	150				mV
	Low-level differential input voltage		−150			mV

NOTE 3: This data sheet uses the algebraic limit system that has been adopted by the International Electrotechnical Commission for logic voltage levels. The A limit is the more positive (less negative) limit; the B limit is the less positive (more negative) limit.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{EE}, and operating free-air temperature (unless otherwise noted) with V_{BB} = −1.3 V for SN75320.

PARAMETER		TEST CONDITIONS		SN75320 MIN	SN75320 TYP†	SN75320 MAX	SN75321 MIN	SN75321 TYP†	SN75321 MAX	UNIT
V_{OH}	High-level output voltage	$V_{IH} = V_{IHB}$	I_{OH} = −10 mA	V_{CC2} −1.1	V_{CC2} −0.7		V_{CC2} −1.1	V_{CC2} −0.7		V
			I_{OH} = −400 μA	V_{CC2} −0.5	V_{CC2} −0.3		V_{CC2} −0.5	V_{CC2} −0.3		
			I_{OH} = −200 μA	V_{CC2} −0.4	V_{CC2} −0.2		V_{CC2} −0.4	V_{CC2} −0.2		
V_{OL}	Low-level output voltage	V_{CC2} = 11.4 V, $V_{IL} = V_{ILA}$, I_{OL} = 10 mA			0.12	0.5		0.12	0.5	V
I_{IH}	High-level input current	V_{EE} = −5.72 V, V_I = −0.7 V			80	800		80	800	μA
I_{IL}	Low-level input current	V_{EE} = −5.72 V, V_I = −2 V				−10			−10	μA
		V_{EE} = −5.72 V, V_I = −5.72 V				−100			−100	
I_{CC1} (H)	Supply current from V_{CC1}, both outputs high	V_{CC1} = 5.25 V, V_{CC2} = 15 V, V_{EE} = −5.72 V, No load			18	26		18	26	mA
I_{CC2} (H)	Supply current from V_{CC2}, both outputs high				9	13		9	13	
I_{EE} (H)	Supply current from V_{EE}, both outputs high				−8	−12		−10	−15	
I_{BB} (H)	Supply current from V_{BB}, both outputs high					−10				μA
I_{CC1} (L)	Supply current from V_{CC1}, both outputs low	V_{CC1} = 5.25 V, V_{CC2} = 15 V, V_{EE} = −5.72 V, No load			18	25		18	25	mA
I_{CC2} (L)	Supply current from V_{CC2}, both outputs low					0.5			0.5	
I_{EE} (L)	Supply current from V_{EE}, both outputs low				−12	−17		−14	−20	
I_{BB} (L)	Supply current from V_{BB}, both outputs low				80	800				μA

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, V_{EE} = −5.2 V, V_{BB} = −1.3 V (SN75320), and T_A = 25°C.

switching characteristics, V_{CC1} = 5V, V_{CC2} = 12 V, V_{EE} = −5.2V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BOTH TYPES MIN	BOTH TYPES TYP	BOTH TYPES MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300 pF, See Figure 1		16	24	ns
t_{DHL}	Delay time, high-to-low-level output			30	43	
t_{TLH}	Transition time, low-to-high-level output			10	20	ns
t_{THL}	Transition time, high-to-low-level output			14	20	
t_{PLH}	Propagation delay time, low-to-high-level output			26	44	ns
t_{PHL}	Propagation delay time, high-to-low-level output			44	62	

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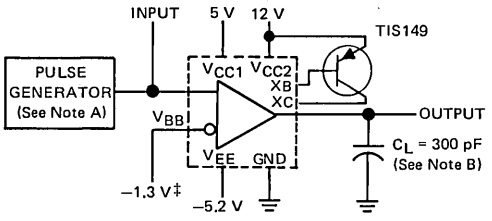
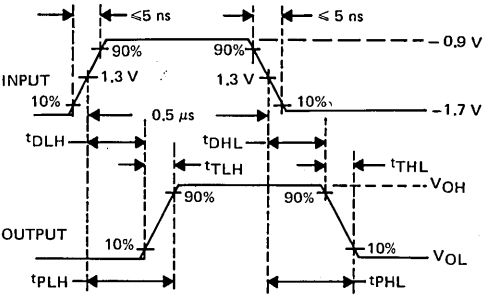
PARAMETER MEASUREMENT INFORMATION



‡V_{BB} is internally generated on SN75321

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

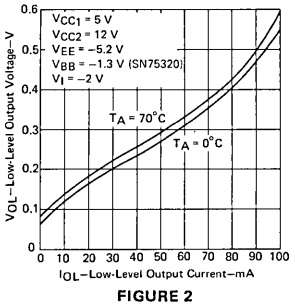


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

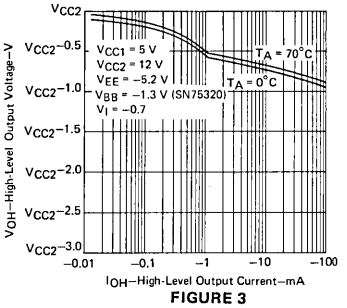


FIGURE 3

INPUT CURRENT vs INPUT VOLTAGE

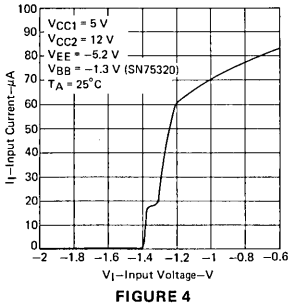


FIGURE 4

OUTPUT VOLTAGE vs INPUT VOLTAGE

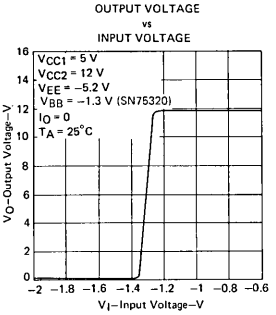


FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

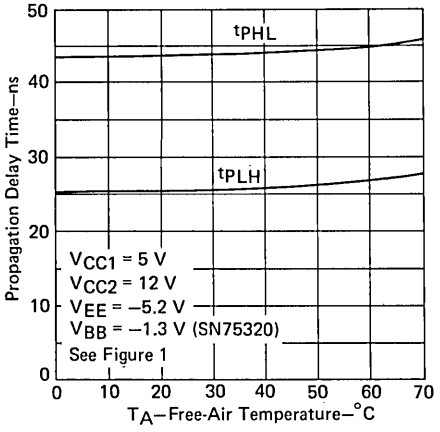


FIGURE 6

DELAY TIMES
vs
FREE-AIR TEMPERATURE

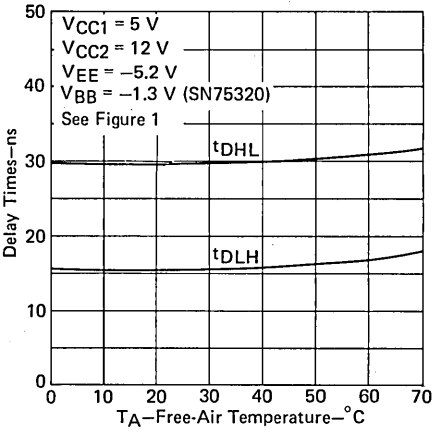


FIGURE 7

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE V_{CC2}

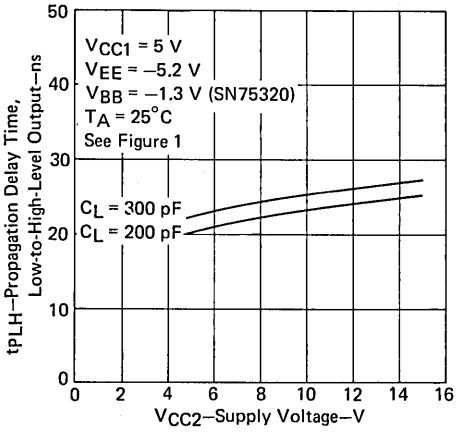


FIGURE 8

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE V_{CC2}

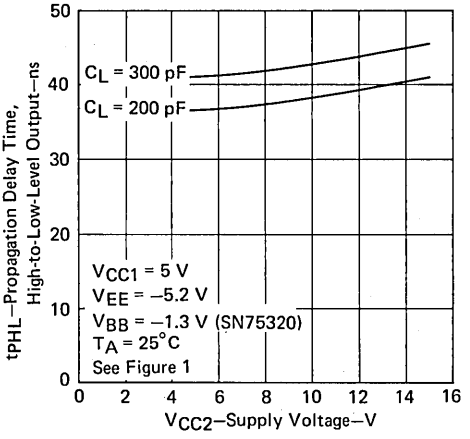


FIGURE 9

TEXAS INSTRUMENTS
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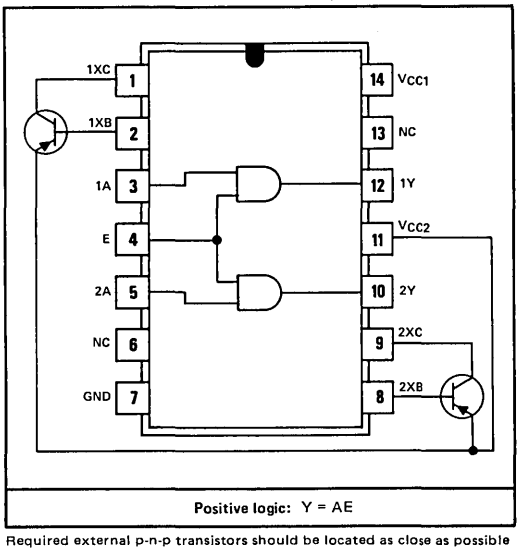
TYPE SN75322
DUAL POSITIVE-AND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712336, MAY 1976–REVISED APRIL 1977

MOS MEMORY INTERFACE

- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- TTL- and DTL-Compatible Inputs
- Separate Driver Address Inputs with Common Strobe
- V_{OH} and V_{OL} Compatible with TMS4030 4K RAM and Other Popular MOS RAMs
- Negligible 12-V Supply Current and Low 5-V Supply Current when Output is at a Low Level
- Output in High-Impedance State if 5-V Supply is Lost
- Requires 2 External P-N-P Transistors per Package for Operation (Use of TIS149, A5T4260, or A5T4261 is Recommended)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



Positive logic: Y = AE

Required external p-n-p transistors should be located as close as possible to the SN75322.

description

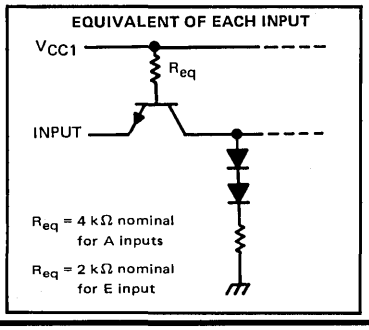
The SN75322 is a monolithic dual TTL-to-MOS driver and interface circuit. The device has separate driver address inputs with common strobe. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. The SN75322 is designed for driving N-Channel RAMs where low power dissipation is desirable when the driver output is at a low level. Specifically, it may be used to drive the chip-enable input of the TMS4030 MOS RAM.

The SN75322 requires two external P-N-P transistors per package. Suggested P-N-P transistors are TIS149, A5T4260, or A5T4261.

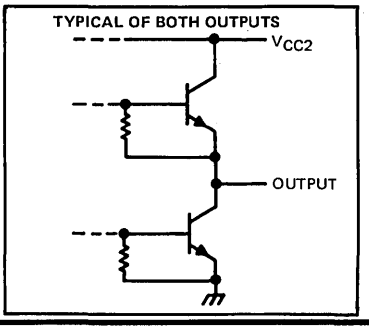
The SN75322 operates from the TTL 5-volt supply and the MOS V_{DD} supply. With the use of an external pull-down resistor, the driver output of the SN75322 will be forced to the low level if the 5-volt supply is lost. The SN75322 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . –0.5 V to 15 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75322 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Operating free-air temperature, T_A	0		70	°C
Load capacitance, C_L	200			pF

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage		V_{IH} = 2 V, I_{OH} = –10 mA	V_{CC2}–1.1	V_{CC2}–0.9		V
			V_{IH} = 2 V, I_{OH} = –400 μA	V_{CC2}–0.5	V_{CC2}–0.25		
			V_{IH} = 2 V, I_{OH} = –200 μA	V_{CC2}–0.4	V_{CC2}–0.2		
V_{OL}	Low-level output voltage		V_{CC2} = 11.4 V, V_I = 0.8 V, I_{OL} = 10 mA		0.23	0.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A Inputs	V_I = 2.4 V			40	μA
		E Input				80	
I_{IL}	Low-level input current	A Inputs	V_I = 0.4 V		–1	–1.6	mA
		E Input			–2	–3.2	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 0 V, No load		15	20	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 0 V, No load		0.01	0.5	mA
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 5 V, No load		24	34	mA
$I_{CC2(H)}$	Supply current from V_{CC2} both outputs high		V_{CC1} = 5.25 V, V_{CC2} = 15 V, All inputs at 5 V, No load		9.5	14	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, and T_A = 25°C.

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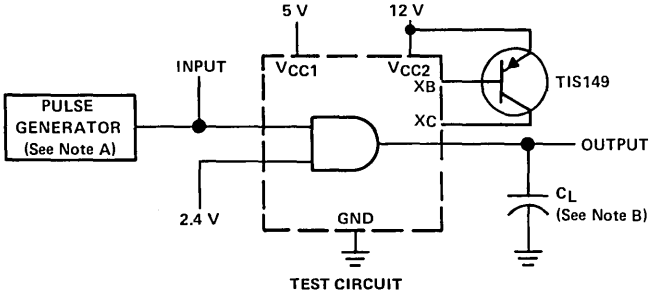
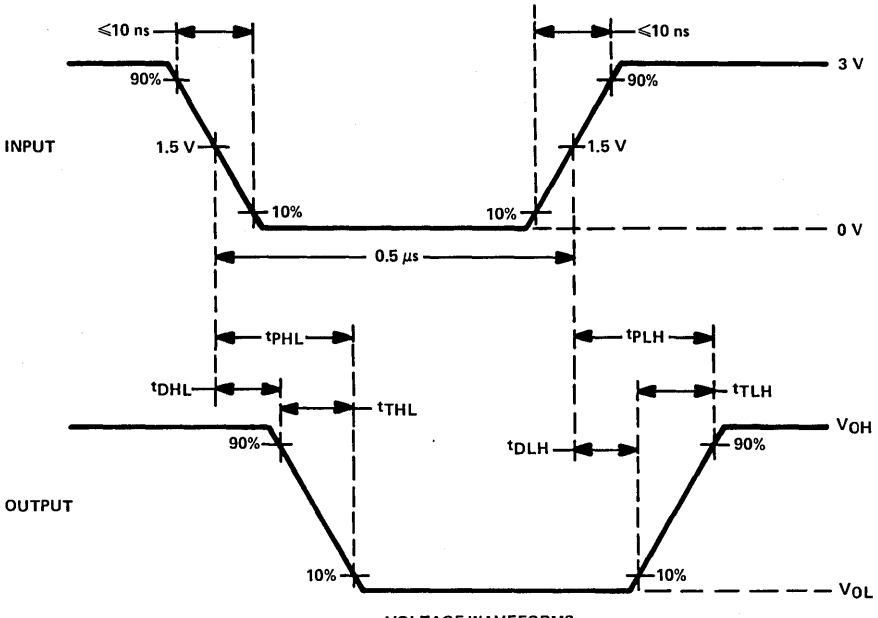
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300 pF, See Figure 1		16	21	ns
t_{DHL}	Delay time, high-to-low-level output			18	24	ns
t_{TLH}	Transition time, low-to-high-level output			11	17	ns
t_{THL}	Transition time, high-to-low-level output			13	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output		12	27	38	ns
t_{PHL}	Propagation delay time, high-to-low-level output		14	31	44	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

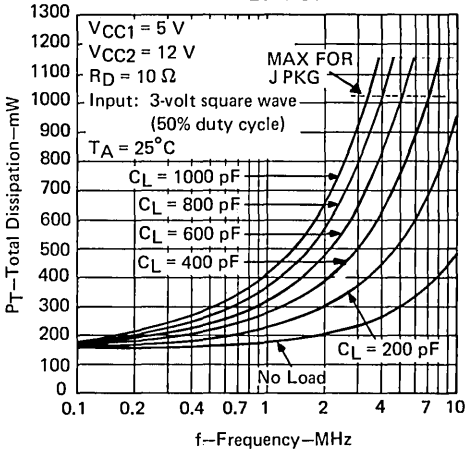
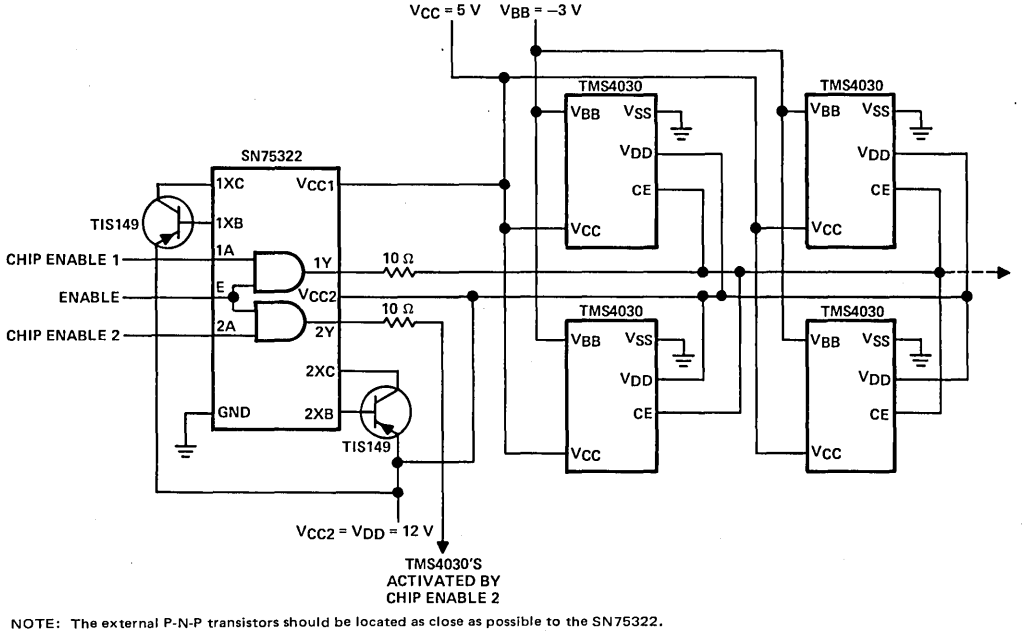


FIGURE 2

TYPICAL APPLICATION DATA



NOTE: The external P-N-P transistors should be located as close as possible to the SN75322.

FIGURE 3–SN75322 DRIVING TMS4030 MEMORIES

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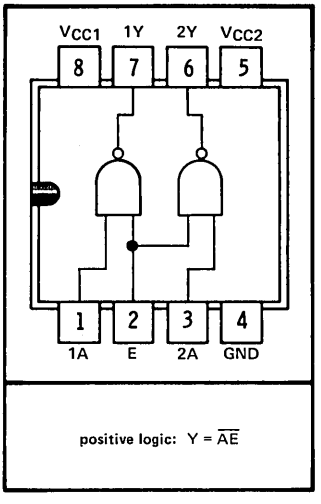
TYPE SN75350
DUAL NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712370, MAY 1976 – REVISED APRIL 1977

MOS MEMORY INTERFACE

- Lower-Voltage, High-Speed Version of SN75361A
- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible With Many Popular MOS RAMs
- V_{CC2} Supply Voltage Variable over Wide Range . . . 5 V to 18 V
- TTL- and DTL-Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Low Standby Power Dissipation
- Special Application . . . 7001 MOS RAM Drivers

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75350 is a monolithic integrated dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs.

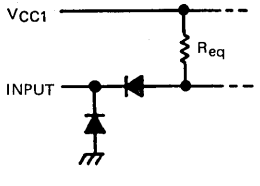
The SN75350 operates from the TTL 5-volt supply and the MOS V_{SS} supply in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 12 volts to 18 volts; however, it is designed so as to be useable over a much wider range of V_{CC2}.

The SN75350 has speed advantages over the SN75361A when driving heavy loads with reduced V_{CC2}.

The SN75350 is characterized for operation from 0°C to 70°C.

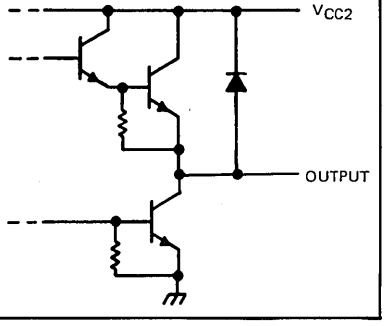
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



R_{eq} = 4 kΩ nominal for A inputs
R_{eq} = 2 kΩ nominal for E input

TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 20 V
Input voltage . . . . . 5.5 V
Inter-input voltage (see Note 2) . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) : JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the JG package, SN75350 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	15	18	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
		V_{CC2} = 12 V to 18 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E input			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E input		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	V_{CC1} = 5.25 V,	V_{CC2} = 18 V,		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	All inputs at 0 V,	No load			0.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low	V_{CC1} = 5.25 V,	V_{CC2} = 18 V,		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low	All inputs at 5 V,	No load		12	17	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, All inputs at 5 V,	V_{CC2} = 18 V, No load			0.5	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 15 V, and T_A = 25°C.

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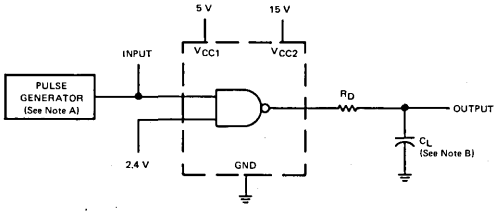
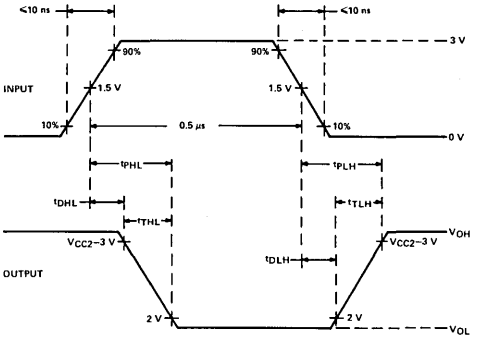
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		16	24	ns
t_{DHL}	Delay time, high-to-low-level output			15	23	ns
t_{TLH}	Transition time, low-to-high-level output			14	22	ns
t_{THL}	Transition time, high-to-low-level output			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level output			30	46	ns
t_{PHL}	Propagation delay time, high-to-low-level output			31	47	ns

PARAMETER MEASURMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following charactersitics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

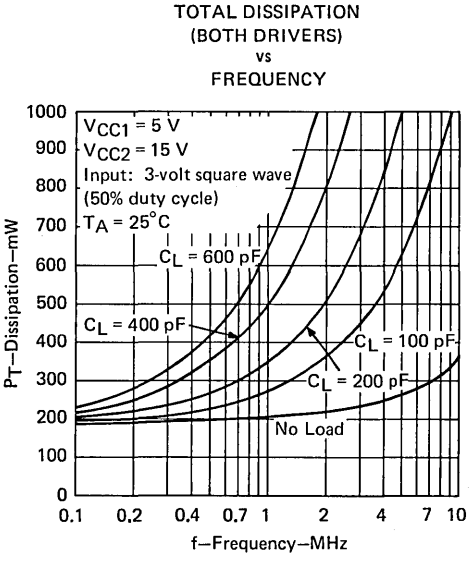


FIGURE 2

5

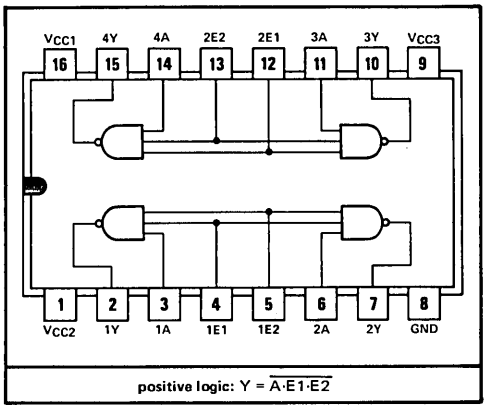
TYPE SN75355
QUADRUPLE NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712371, MAY 1976 – REVISED APRIL 1977

MOS MEMORY INTERFACE

- Quad Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- V_{CC2} Supply Voltage Variable over Wide Range to 18 Volts Maximum
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- TTL- and DTL-Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Two Common Enable Inputs per Gate-Pair
- High-Speed Switching
- Low Standby Power Dissipation
- High-Speed SN75365-Type Device with Lower V_{CC2} Voltage Requirement

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \cdot E1 \cdot E2}$

description

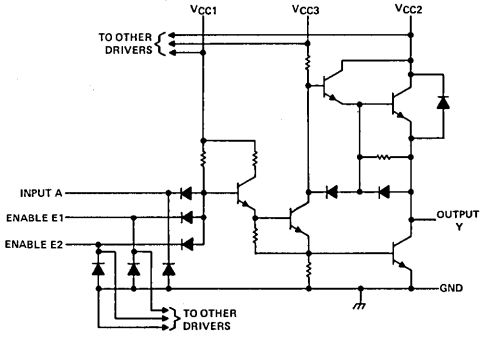
The SN75355 is a monolithic quadruple TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs or microprocessor multiphase clock inputs.

The SN75355 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 12 volts to 18 volts, and with nominal V_{CC3} supply voltage from 3 volts to 4 volts higher than V_{CC2}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

The SN75355 has speed advantages over the SN75365 when driving highly capacitive loads with V_{CC2} reduced to within the range of 12 to 15 volts.

The SN75355 is characterized for operation from 0°C to 70°C.

schematic (each driver)



5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 19 V
Supply voltage range of V_{CC3}	−0.5 V to 19 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75355 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	15	18	V
Supply voltage, V_{CC3}	V_{CC2}	18	18	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	3	4	V
Operating free-air temperature, T_A	0		70	°C

5

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electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3} and operating free-air temperature (unless otherwise noted)

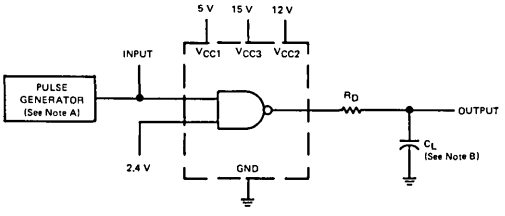
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC3} = V_{CC2} + 3 V, V_{IL} = 0.8 V, I_{OH} = −100 μA		V_{CC2}−0.3	V_{CC2}−0.1		V
		V_{CC3} = V_{CC2} + 3 V, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−1.2	V_{CC2}−0.9		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −50 μA		V_{CC2}−1	V_{CC2}−0.7		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 10 mA			0.15	0.3	V
		V_{CC3} = 12 to 18 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	
V_{OK}	Output clamp voltage	V_I = 0 V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E1 and E2 inputs			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E1 and E2 inputs		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 15 V, V_{CC3} = 18 V, All inputs at 0 V, No load			4.5	6.5	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−3	−4.5	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				3	5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, V_{CC2} = 18 V, V_{CC3} = 18 V, All inputs at 5 V, No load			33	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low				19	31	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 18 V, V_{CC3} = 18 V, All inputs at 0 V, No load				0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, V_{CC2} = 18 V, V_{CC3} = 18 V, All inputs at 5 V, No load				0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V, and T_A = 25°C, except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

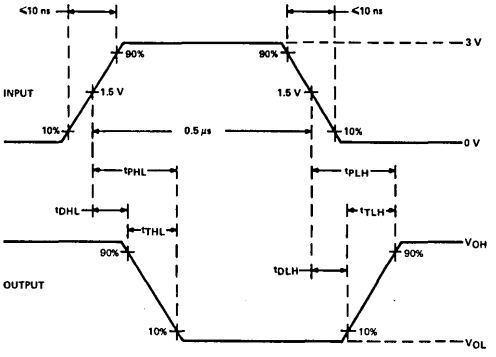
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		18	28	ns
t_{DHL}	Delay time, high-to-low-level output			11	17	ns
t_{TLH}	Transition time, low-to-high-level output			14	21	ns
t_{THL}	Transition time, high-to-low-level output			13	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output			32	49	ns
t_{PHL}	Propagation delay time, high-to-low-level output			24	37	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
(ALL FOUR DRIVERS)
vs
FREQUENCY

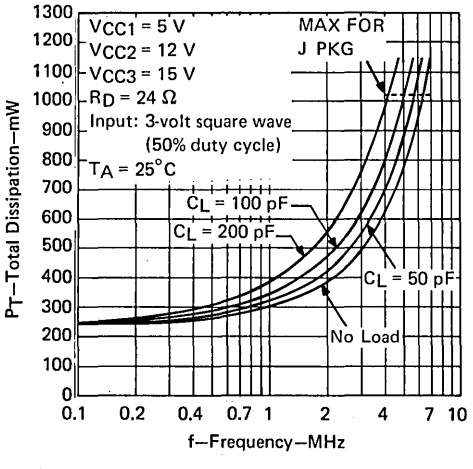


FIGURE 2

TOTAL DISSIPATION
(ALL FOUR DRIVERS)
vs
FREQUENCY

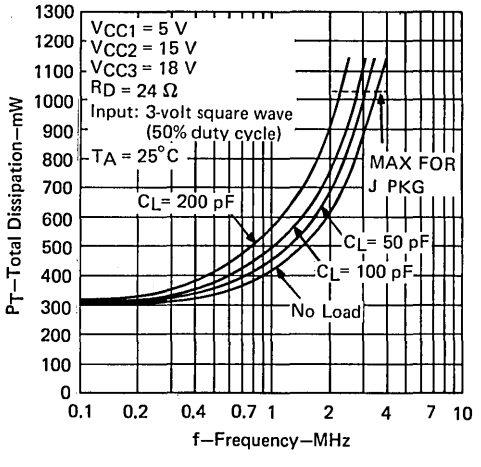


FIGURE 3

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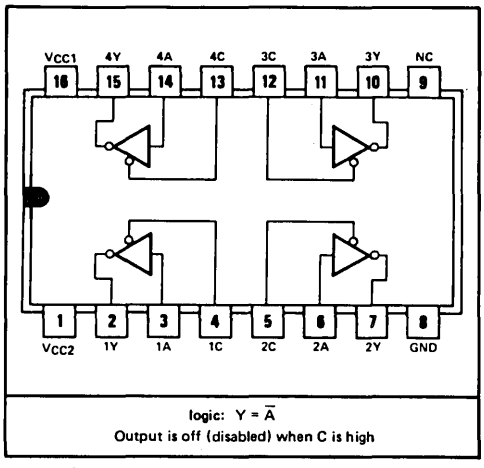
FUTURE PRODUCT
TO BE ANNOUNCED

TYPE SN75357
QUADRUPLE TTL-TO-MOS DRIVER WITH 3-STATE OUTPUTS

APRIL 1977

- Quadruple Inverting TTL-to-MOS Driver
- 3-State Outputs
- CMOS Applications
- Very Low Transient Current During Switching
- Separate Address and Enable/Disable Inputs for Each Driver
- V_{CC2} Variable Over Wide Range . . . 5 V to 15 V
- High-Speed Switching

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: $Y = \overline{A}$
Output is off (disabled) when C is high

NC—No internal connection

description

The SN75357 is a monolithic quadruple TTL-to-MOS driver with three-state outputs. The device has very low transient current during switching. It features a V_{OH} level of $V_{CC2} - 1.6$ volts minimum, and a V_{OL} level of 1.3 volts maximum. The circuit performance is similar to that of the SN75367.

The SN75357 will be characterized for operation from 0°C to 70°C.

supply voltages: $V_{CC1} = 5$ V
V_{CC2} variable from 5 V to 15 V

5

7

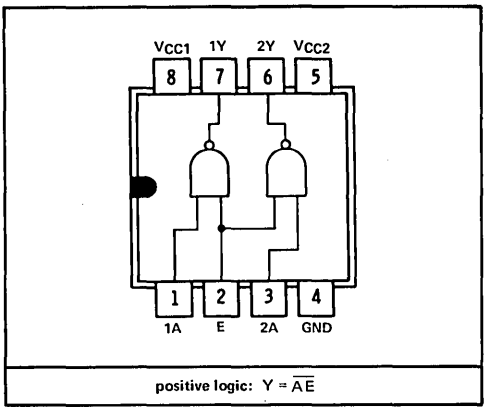
TYPE SN75361A
DUAL NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712054, SEPTEMBER 1973—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



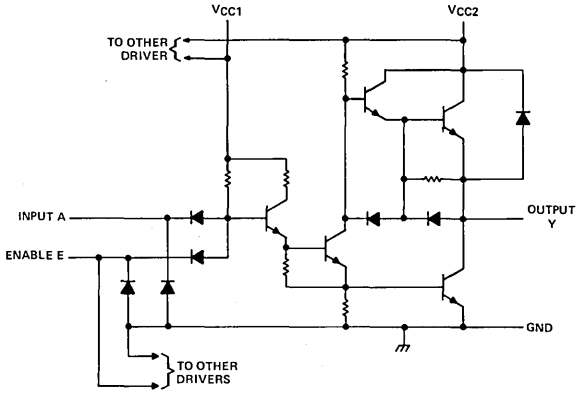
description

The SN75361A is a monolithic integrated dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS 1103 and TMS 4062.

The SN75361A operates from the TTL 5-volt supply and the MOS V_{SS} supply in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16 volts to 20 volts; however, it is designed so as to be useable over a much wider range of V_{CC2}.

The SN75361A is characterized for operation from 0°C to 70°C.

schematic (each driver)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 25 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):	
JG package	825 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between the A input of either driver and the common E input.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the JG package, SN75361A chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Operating free-air temperature, T_A	0		70	°C

5

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
		V_{CC2} = 15 V to 24 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	V
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E input			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E input		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	V_{CC1} = 5.25 V,	V_{CC2} = 24 V,		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	All inputs at 0 V,	No load			0.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low	V_{CC1} = 5.25 V,	V_{CC2} = 24 V,		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low	All inputs at 5 V,	No load		7	13	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, All inputs at 5 V,	V_{CC2} = 24 V, No load			0.5	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, and T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		11	24	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			25	40	ns
t_{THL}	Transition time, high-to-low-level output			21	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	36	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	31	47	ns

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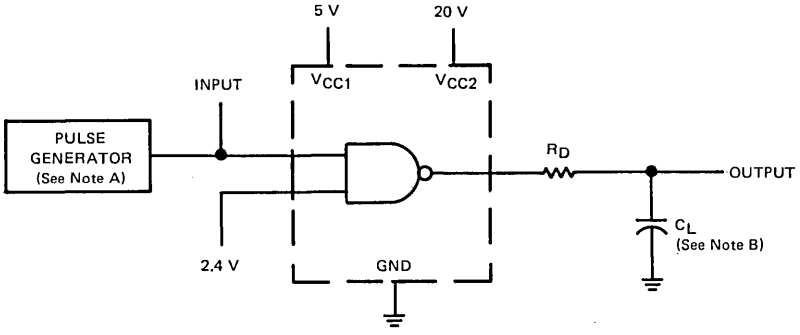
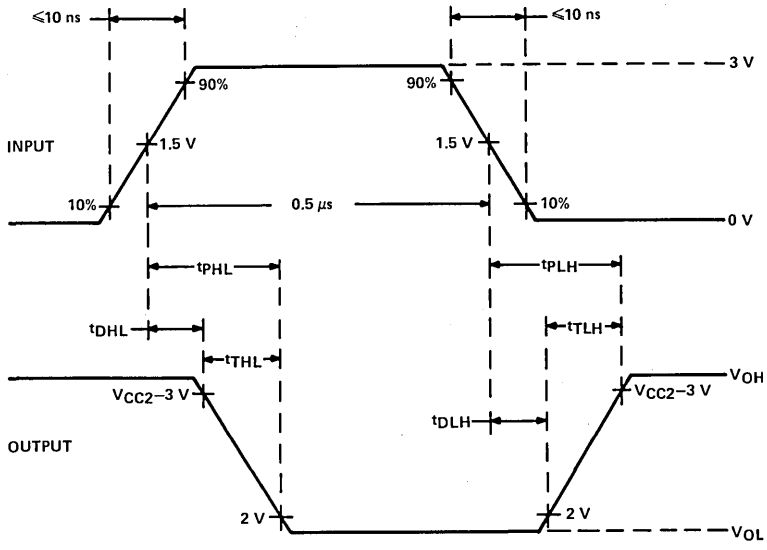
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

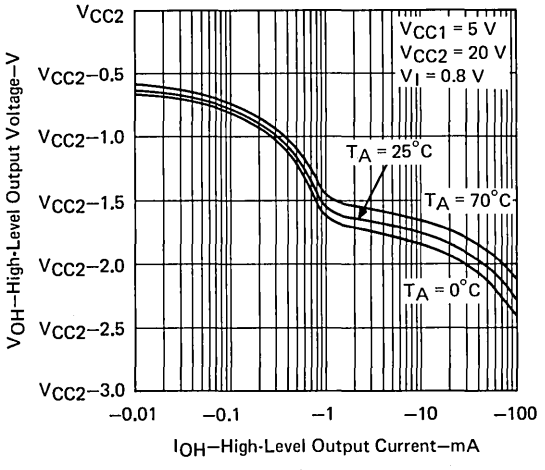


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

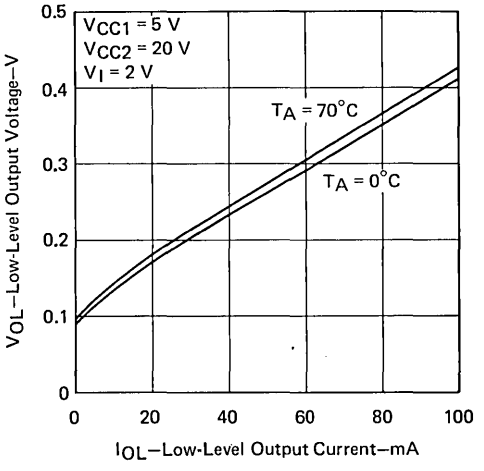


FIGURE 3

VOLTAGE TRANSFER CHARACTERISTICS

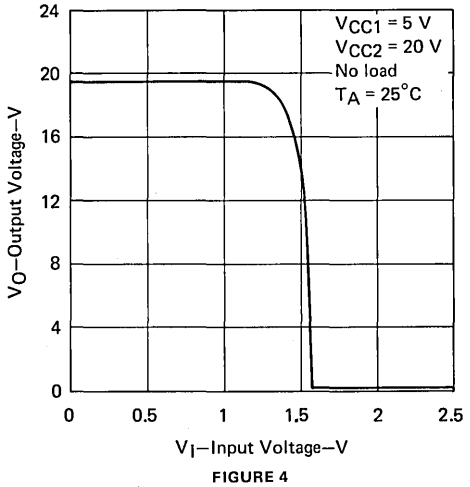


FIGURE 4

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

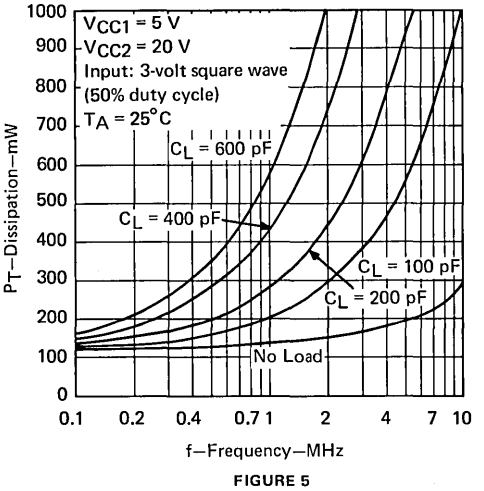


FIGURE 5

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

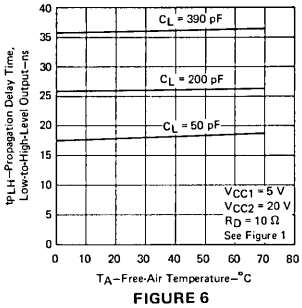

FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

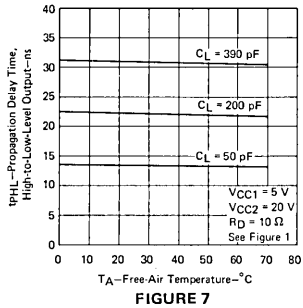

FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

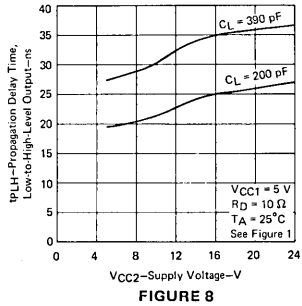

FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

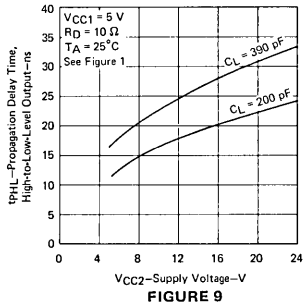

FIGURE 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

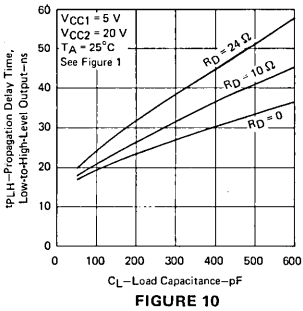

FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

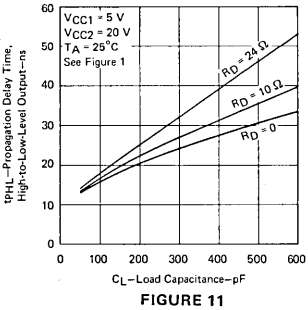

FIGURE 11

5

TYPICAL APPLICATION DATA

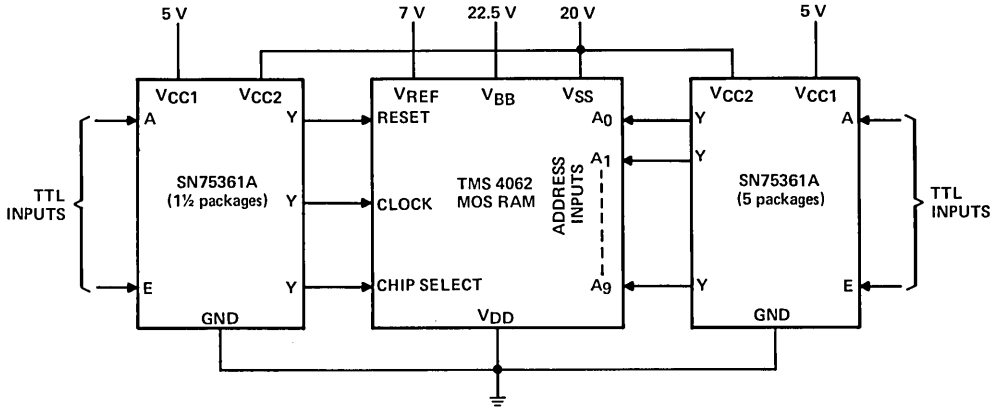

FIGURE 12–INTERCONNECTION OF SN75361A DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM.

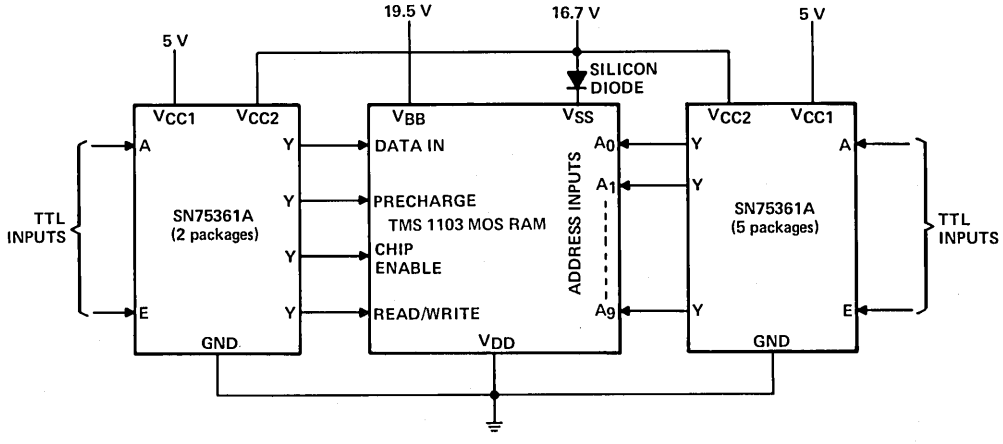

FIGURE 13–INTERCONNECTION OF SN75361A DEVICES WITH '1103-TYPE SILICON-GATE MOS RAM

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TYPICAL APPLICATION DATA

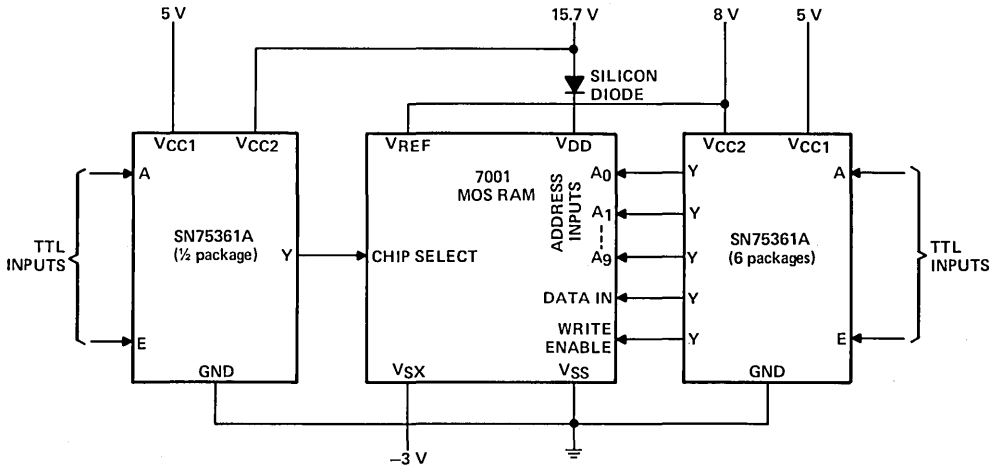
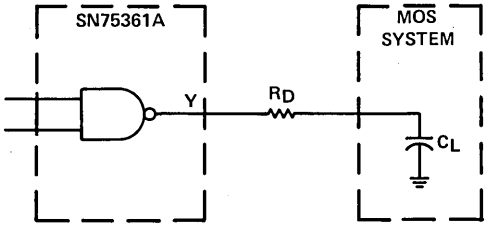


FIGURE 14—INTERCONNECTION OF SN75361A DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM.



NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional).

FIGURE 15—USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75361A APPLICATIONS

Applications using SN75361A as interface devices between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figures 12, 13, and 14. A silicon diode is used in Figures 13 and 14 to increase the SN75361A high-level output voltage to obtain the desired high-level input voltage required by these MOS RAMs. An extra power supply could be used in place of the diode.

Figures 12, 13, and 14 show the use of the SN75361A over a wide range of V_{CC2} supply voltages. The device may even be used as a TTL gate, if desired, by connecting V_{CC2} to 5 volts.

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between $10\ \Omega$ and $30\ \Omega$. See Figure 15.

5

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75361A driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75361A as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{P_L t_L + P_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 16.

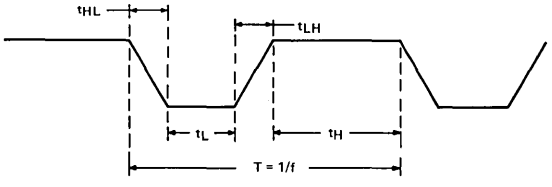


FIGURE 16–OUTPUT VOLTAGE WAVEFORM

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The SN75361A is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. Figure 5 for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5 V, V_{CC2} = 20 V, and duty cycle = 60% outputs high ($t_H/T = 0.6$). Also, assume V_{OH} = 19.3 V, V_{OL} = 0.1 V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{2\text{ mA}}{2}\right) + (20\text{ V}\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{16\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx (200\text{ pF})\ (19.2\text{ V})^2\ (2\text{ MHz})$

$P_{C(AV)} \approx$ 148 mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\ (47 + 148)$

$P_{T(AV)} \approx$ 390 mW typical for total package.

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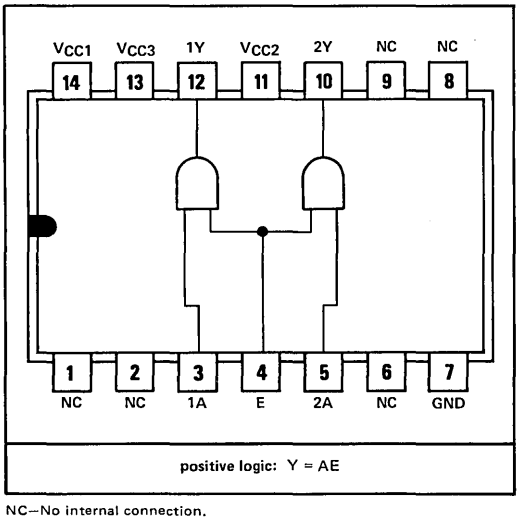
TYPE SN75363
DUAL POSITIVE-AND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712359, FEBRUARY 1976 – REVISED APRIL 1977

MOS MEMORY INTERFACE

- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Operates from Standard Bipolar and MOS Supply Voltages
- High-Speed Switching
- TTL- and DTL-Compatible Inputs
- Separate Driver Address Inputs with Common Strobe
- V_{CC2} Supply Voltage Variable Over Wide Range
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin can be Connected to V_{CC2} Pin in Some Applications
- Damping Resistor Eliminates Undesired Output Transient Overshoot
- Transient Overdrive Improves Fall Time

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection.

description

The SN75363 is a monolithic dual TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive the chip-enable clock input of the TMS4030 MOS RAM and the address, control, and timing inputs for several other types of MOS RAMs.

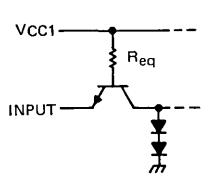
The SN75363 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{DD} supplies. This device has been optimized for operation with V_{CC2} supply voltage from 11 volts to 15 volts, and with nominal V_{CC3} supply voltage from 3 to 4 volts higher than V_{CC2}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

A small series damping resistor has been included in the design to eliminate undesired output transient overshoot due to load or wiring inductance.

The SN75363 is characterized for operation from 0°C to 70°C.

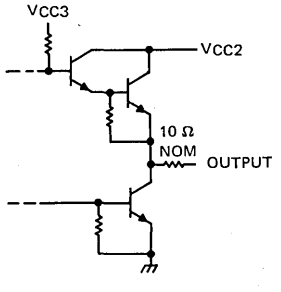
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



R_{eq} = 4 kΩ nominal for A inputs
R_{eq} = 2 kΩ nominal for E input

TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 16 V
Supply voltage range of V_{CC3} . . . . . −0.5 V to 19 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75363 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Supply voltage, V_{CC3}	V_{CC2}	15	18	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	3	4	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage		V_{CC2}+3 V = V_{CC3}, V_{IH} = 2 V, I_{OH} = −10 mA	V_{CC2}−1.2	V_{CC2}−1.0		V
			V_{CC2}+3 V = V_{CC3}, V_{IH} = 2 V, I_{OH} = −100 μA	V_{CC2}−0.3	V_{CC2}−0.15		
			V_{CC2} = V_{CC3}, V_{IH} = 2 V, I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		
V_{OL}	Low-level output voltage		V_{CC2} = 10.8 V, V_{CC3} = 10.8 V, V_{IL} = 0.8 V, I_{OL} = 10 mA		0.3	0.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A inputs	V_I = 2.4 V			40	μA
		E input				80	
I_{IL}	Low-level input current	A inputs	V_I = 0.4 V		−1	−1.6	mA
		E input			−2	−3.2	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, V_{CC2} = 12 V, V_{CC3} = 12 V, All inputs at 0 V, No load		7	11	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low		V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V, All inputs at 0 V, No load		0.8	1.2	
$I_{CC3(L)}$	Supply current from V_{CC3}, both outputs low				5	9	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, V_{CC2} = 12 V, V_{CC3} = 12 V, All inputs at 5 V, No load		17	25	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high		V_{CC1} = 5 V, V_{CC2} = 15 V, V_{CC3} = 18 V, All inputs at 5 V, No load		−0.8	−1.2	
$I_{CC3(H)}$	Supply current from V_{CC3}, both outputs high				0.8	1.2	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V, and T_A = 25°C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

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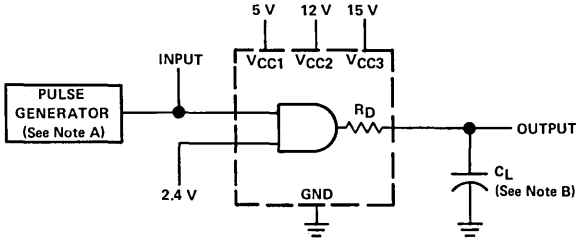
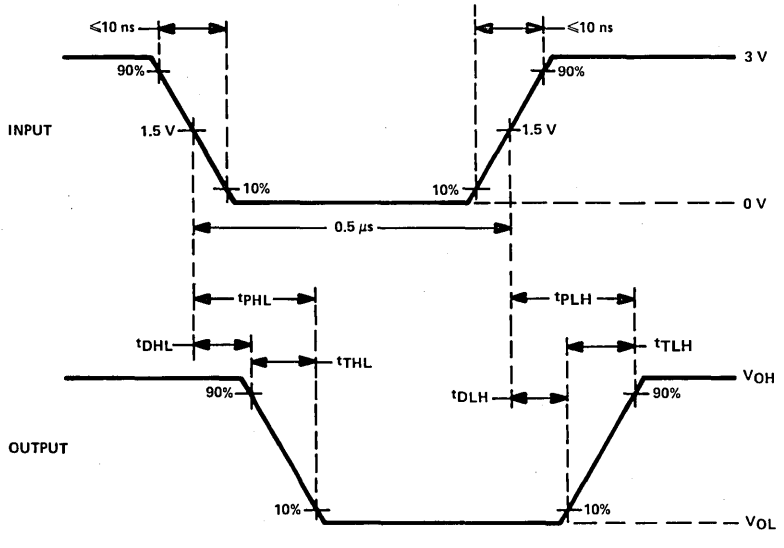
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, V_{CC3} = 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 300 pF, See Figure 1	7	12	17	ns
t_{DHL}	Delay time, high-to-low-level output		10	17	24	ns
t_{TLH}	Transition time, low-to-high-level output		10	16	22	ns
t_{THL}	Transition time, high-to-low-level output		10	16	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output		17	28	39	ns
t_{PHL}	Propagation delay time, high-to-low-level output		20	33	46	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

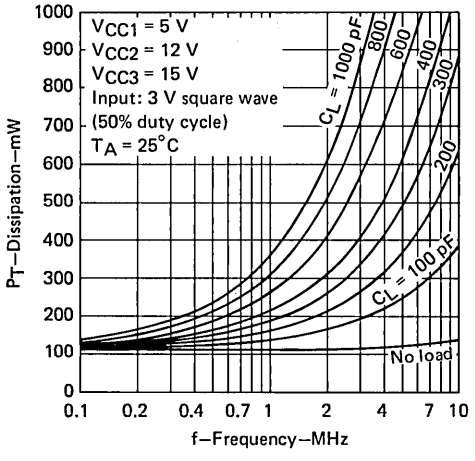


FIGURE 2

SWITCHING TIME
vs
LOAD CAPACITANCE

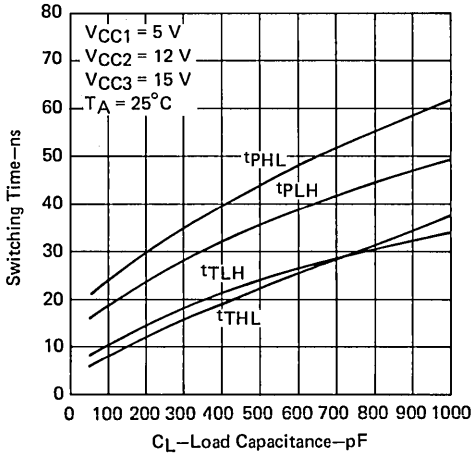


FIGURE 3

TYPICAL APPLICATION DATA

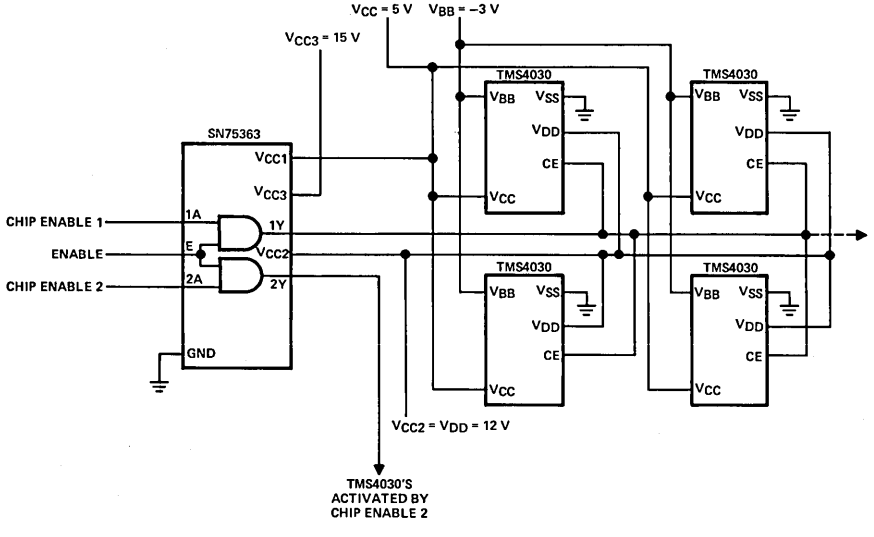


FIGURE 4–SN75363 DRIVING TMS4030 MEMORIES

TEXAS INSTRUMENTS
INCORPORATED
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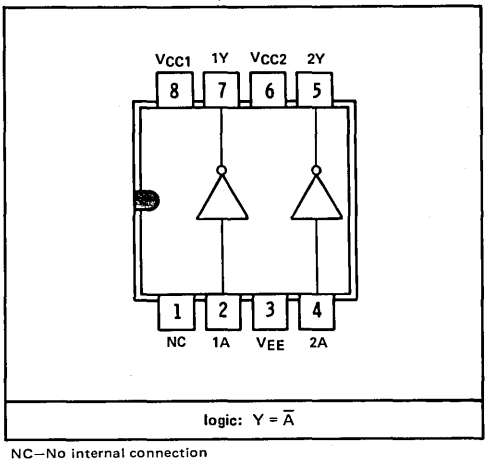
TYPE SN75364
DUAL MOS DRIVER

BULLETIN NO. DL-S 7712373, APRIL 1976—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Inverting MOS Driver
- Versatile Interface Circuit for Use Between TTL Levels and Level-Shifted High-Current, High-Voltage Systems
- Inputs May Be Level-Shifted by Use of a Current Source or Capacitive Coupling or Driven Directly by a Voltage Source
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs and MOS Shift Registers
- V_{CC2} Supply Voltage Variable over Wide Range to 22 Volts Maximum with Respect to V_{EE}
- V_{CC1} Pull-up Supply Voltage Pin Available
- V_{CC1} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- Operates from Standard Bipolar and/or MOS Supply Voltages
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: $Y = \overline{A}$

NC—No internal connection

description

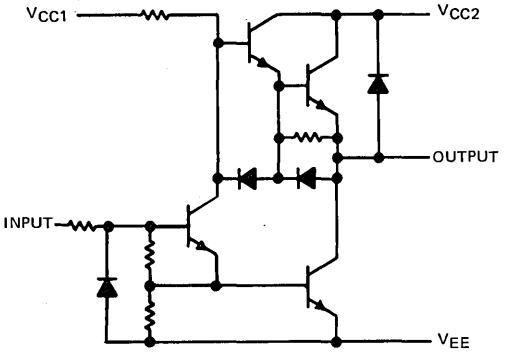
The SN75364 is a monolithic dual MOS driver and interface circuit that operates with either current-source or voltage-source input signals. The device accepts appropriate level-shifted input signals from TTL or other logic systems and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The SN75364 operates from standard MOS and/or bipolar supplies in most applications. This device has been optimized for operation with V_{CC2} supply voltage from 12 volts to 20 volts positive with respect to V_{EE}, and with nominal V_{CC1} supply voltage from 3 volts to 4 volts more positive than V_{CC2}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC1} power supply can be eliminated by connecting the V_{CC1} pin to the V_{CC2} pin.

Inputs of the SN75364 are referenced to the V_{EE} terminal and contain a series current-limiting resistor. The device will operate with either positive current input signals or voltage input signals that are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12 volts to −15 volts with the inputs to be driven from TTL levels or other positive voltage levels. The required negative-level shifting may be done with an external p-n-p transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

The SN75364 is characterized for operation from 0°C to 70°C.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 30 V
Supply voltage range of V_{CC2}	−0.5 V to 22 V
Input voltage	20 V
Positive voltage at any input with respect to V_{CC1}	0.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	
JG package	825 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to the V_{EE} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the JG package, SN75364 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	V_{CC2}	24	28	V
Supply voltage, V_{CC2}	4.75	20	22	V
Voltage difference between supply voltages: $V_{CC1}-V_{CC2}$	0	4	10	V
Input voltage			10	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels

PARAMETER	MIN	MAX	UNIT
V_{IH} High-level input voltage	5	10	V
V_{IL} Low-level input voltage		1	V
I_{IH} High-level input current	8	15	mA
I_{IL} Low-level input current		0.7	mA

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (See Note 3)			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC1} = V_{CC2} + 3$ V,	$V_{IL} = 1$ V,	$I_{OH} = -100\ \mu$A	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC1} = V_{CC2} + 3$ V,	$I_{IL} = 0.7$ mA,	$I_{OH} = -100\ \mu$A				
		$V_{CC1} = V_{CC2} + 3$ V,	$V_{IL} = 1$ V,	$I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		
		$V_{CC1} = V_{CC2} + 3$ V,	$I_{IL} = 0.7$ mA,	$I_{OH} = -10$ mA				
		$V_{CC1} = V_{CC2}$,	$V_{IL} = 1$ V,	$I_{OH} = -50\ \mu$A	$V_{CC2}-1$	$V_{CC2}-0.7$		
		$V_{CC1} = V_{CC2}$,	$I_{IL} = 0.7$ mA,	$I_{OH} = -50\ \mu$A				
		$V_{CC1} = V_{CC2}$,	$V_{IL} = 1$ V,	$I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		
		$V_{CC1} = V_{CC2}$,	$I_{IL} = 0.7$ mA,	$I_{OH} = -10$ mA				
V_{OL}	Low-level output voltage	$V_{IH} = 5$ V,	$I_{OL} = 10$ mA			0.15	0.3	V
		$I_{IH} = 8$ mA,	$I_{OL} = 10$ mA					
		$V_{CC1} = 15$ V to 28 V,	$V_{IH} = 5$ V,	$I_{OL} = 40$ mA		0.25	0.5	
		$V_{CC1} = 15$ V to 28 V,	$I_{IH} = 8$ mA,	$I_{OL} = 40$ mA				
V_{OK}	Output clamp voltage	$V_I = 0$ V,	$I_{OH} = 20$ mA				$V_{CC2}+1.5$	V
V_I	Input voltage	$V_{CC1} = 13.5$ V to 28 V,	$I_I = 15$ mA			9	13.5	V
		$I_I = 8$ mA				5.5	8	
		$I_I = 0.7$ mA				0.7	1	
I_I	Input current	$V_{CC1} = 10$ V to 28 V,	$V_I = 10$ V			17	26	mA
		$V_I = 5$ V				7	11	
		$V_I = 1$ V				1.1	1.6	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	$V_{CC1} = 26$ V,	$V_{CC2} = 22$ V,			1.0	2	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	Both inputs at 0 V,	No load			−1.0	+0.25 −1.6	
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low	$V_{CC1} = 28$ V,	$V_{CC2} = 22$ V,			7	14	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low	Both inputs at 7 V,	No load			0.5	1	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high	$V_{CC1} = 22$ V,	$V_{CC2} = 22$ V,				0.5	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high	Both inputs at 0 V,	No load				0.25	

†All typical values are at $V_{CC1} = 24$ V, $V_{CC2} = 20$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

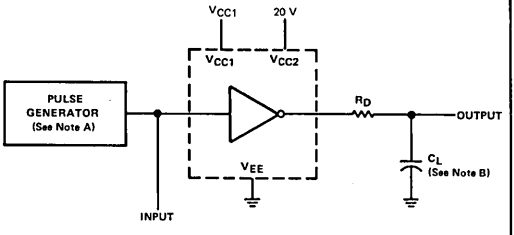
NOTE 3: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

switching characteristics, $V_{CC2} = 20$ V, $T_A = 25°C$

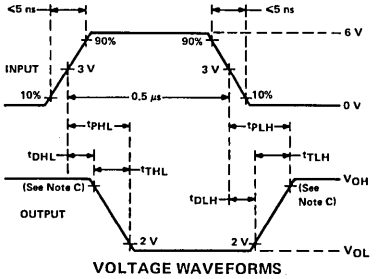
PARAMETER		TEST CONDITIONS	$V_{CC1} = 24$ V			$V_{CC1} = 20$V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{DLH}	Delay time, low-to-high-level output	$C_L = 390$ pF, $R_D = 10\ \Omega$, See Figure 1	2	13	23	3	14	24	ns
t_{DHL}	Delay time, high-to-low-level output		1	9	18	1	10	18	ns
t_{TLH}	Transition time, low-to-high-level output		8	21	24	8	21	34	ns
t_{THL}	Transition time, high-to-low-level output		6	19	30	5	18	29	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	34	57	11	35	58	ns
t_{PHL}	Propagation delay time, high-to-low-level output		8	28	47	8	28	47	ns

5

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The high-level reference point is 17 V when $V_{CC1} = V_{CC2} = 20$ V and is 18 V when $V_{CC1} = V_{CC2} + 4$ V = 24 V.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

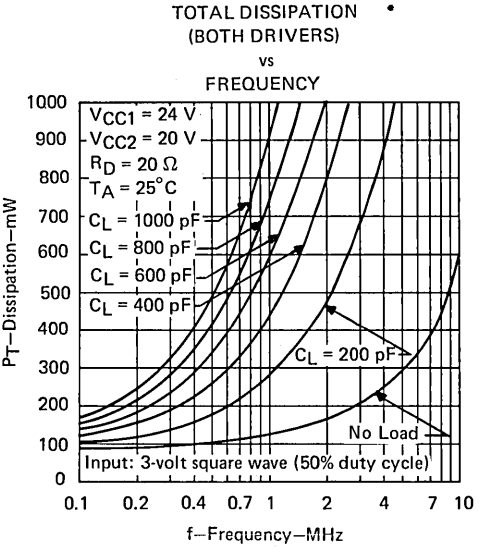
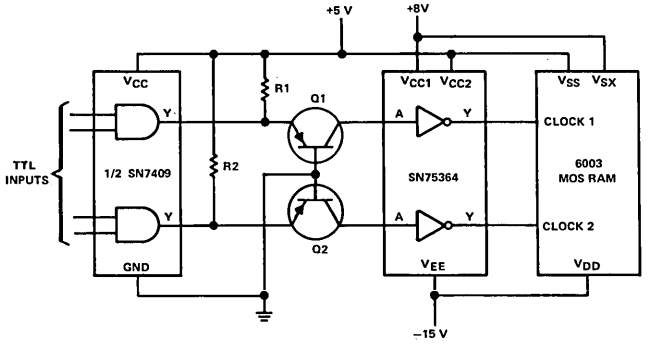


FIGURE 2

TYPICAL APPLICATION DATA



NOTES: R1 and R2 ≈ 350 Ω to 500 Ω.
Q1 and Q2 are 2N3829 or similar p-n-p transistors.

FIGURE 3–MOS RAM CLOCK DRIVER SYSTEM WITH P-N-P TRANSITOR CURRENT SOURCE USED TO LEVEL-SHIFT TO INPUTS OF SN75364

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TYPICAL APPLICATION DATA

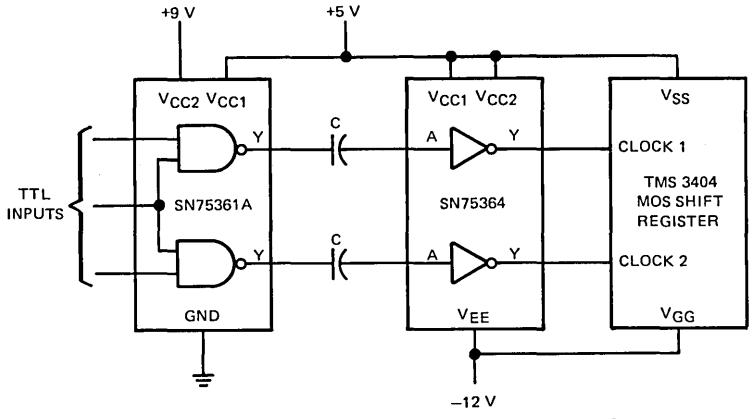
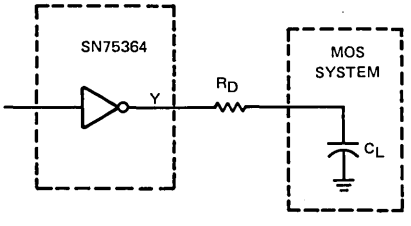


FIGURE 4–MOS SHIFT REGISTER CLOCK DRIVER SYSTEM WITH CAPACITIVE COUPLING USED TO LEVEL-SHIFT TO INPUTS OF SN75364



NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional)

FIGURE 5–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75364 APPLICATIONS

Applications of the SN75364 used as an interface device in systems converting TTL signals to negative polarity MOS clock signals are shown in Figures 3 and 4. In both applications the SN75364 V_{EE} pin is connected to a negative MOS supply voltage. The V_{CC1} supply pin may be connected to the V_{CC2} pin as shown in Figure 4 or connected to a separate voltage more positive than V_{CC2}, as shown in Figure 3. The SN75364 may be used over a wide range of V_{CC1} and V_{CC2} supply voltage. However, for proper operation, the voltage at the inputs of the SN75364 should not be more positive than the voltage at V_{CC1}.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the SN75364, which are referenced to the V_{EE} terminal. A p-n-p transistor current source is used to level shift in Figure 3. Resistor R sets the current and an open-collector TTL gate is used to switch the p-n-p transistor. Figure 4 shows capacitive coupling being used to level shift with the SN75361A TTL-to-MOS driver used as a low-impedance voltage-source driver. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

The fast switching speeds of the SN75364 may produce undersirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 Ω and 30 Ω. See Figure 5.

5

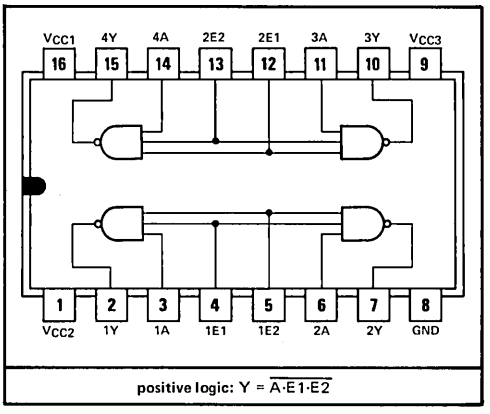
TYPE SN75365
QUADRUPLE NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712058, SEPTEMBER 1973—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Quad Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Designed to be Interchangeable with Intel 3207
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Two Common Enable Inputs per Gate-Pair
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



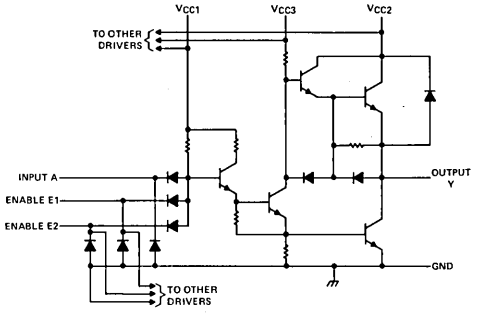
description

The SN75365 is a monolithic integrated quadruple TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS1103 and TMS4062.

The SN75365 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16 volts to 20 volts, and with nominal V_{CC3} supply voltage from 3 volts to 4 volts higher than V_{CC2}. However, it is designed so as to be useable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

The SN75365 is characterized for operation from 0°C to 70°C.

schematic (each driver)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)		−0.5 V to 7 V
Supply voltage range of V_{CC2}		−0.5 V to 25 V
Supply voltage range of V_{CC3}		−0.5 V to 30 V
Input voltage		5.5 V
Inter-input voltage (see Note 2)		5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)	J package	1025 mW
	N package	1150 mW
Operating free-air temperature range		0°C to 70°C
Storage temperature range		−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75365 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	4	10	V
Operating free-air temperature, T_A	0		70	°C

5

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3} and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC3} = V_{CC2} + 3 V, V_{IL} = 0.8 V, I_{OH} = −100 μA		V_{CC2}−0.3	V_{CC2}−0.1		V
		V_{CC3} = V_{CC2} + 3 V, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−1.2	V_{CC2}−0.9		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −50 μA		V_{CC2}−1	V_{CC2}−0.7		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−2.3	V_{CC2}−1.8		
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 10 mA			0.15	0.3	V
		V_{CC3} = 15 V to 28 V, V_{IH} = 2 V, I_{OL} = 40 mA			0.25	0.5	
V_{OK}	Output clamp voltage	V_I = 0 V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E1 and E2 inputs			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E1 and E2 inputs		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 0 V, No load			4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−2.2	+0.25 −3.2	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 5 V, No load			31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low				16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 0 V, No load				0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 5 V, No load				0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, and T_A = 25°C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		11	20	ns
t_{DHL}	Delay time, high-to-low-level output			10	18	ns
t_{TLH}	Transition time, low-to-high-level output			20	33	ns
t_{THL}	Transition time, high-to-low-level output			20	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	31	48	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	46	ns

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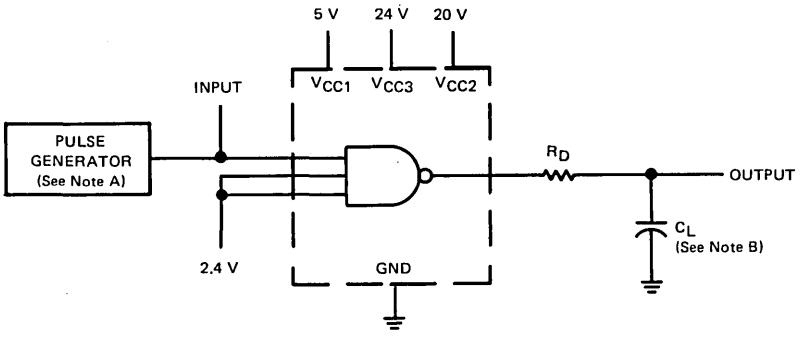
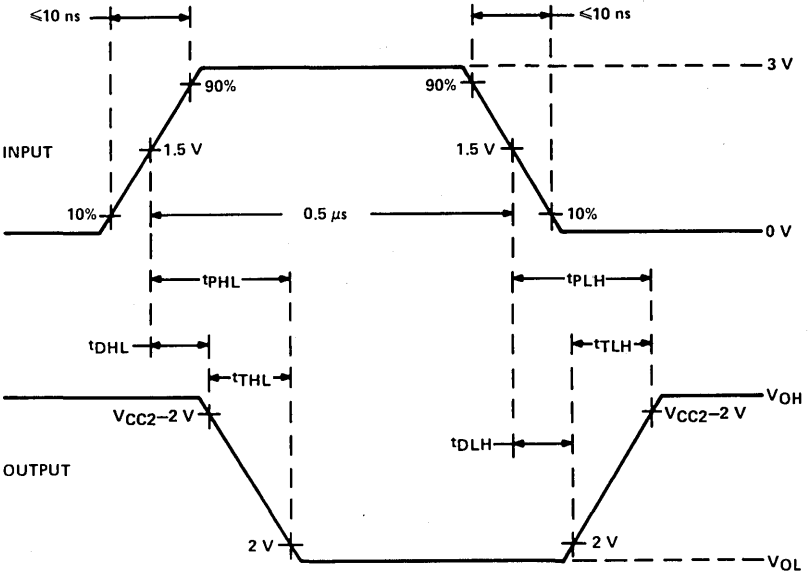
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

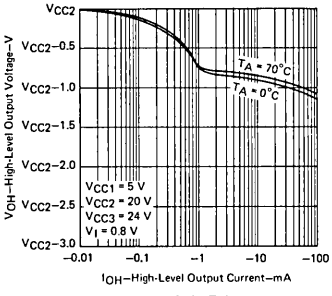


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

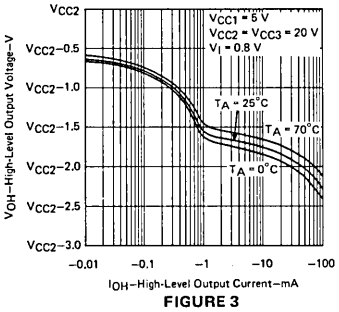


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

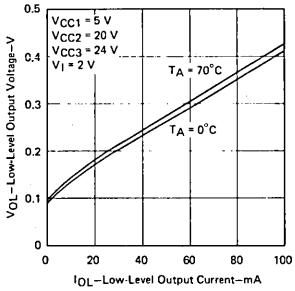


FIGURE 4

VOLTAGE TRANSFER CHARACTERISTICS

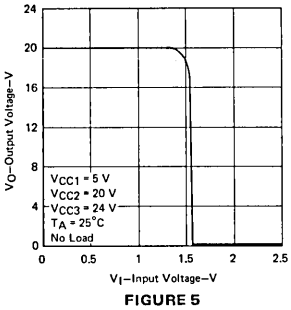


FIGURE 5

TOTAL DISSIPATION
(ALL FOUR DRIVERS)
vs
FREQUENCY

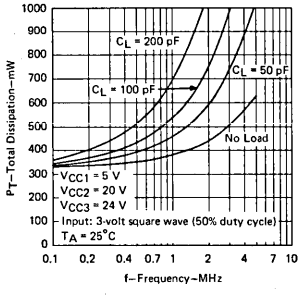


FIGURE 6

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TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

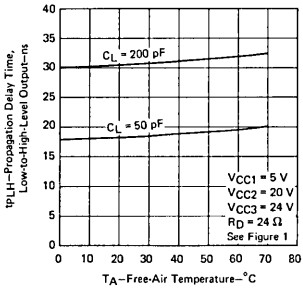

FIGURE 7

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

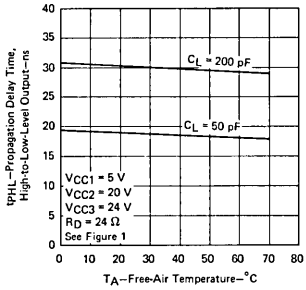

FIGURE 8

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

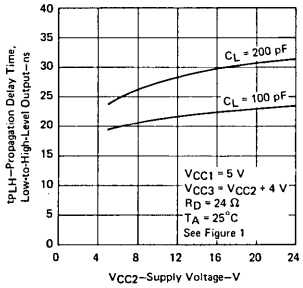

FIGURE 9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

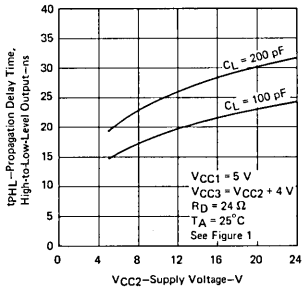

FIGURE 10

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

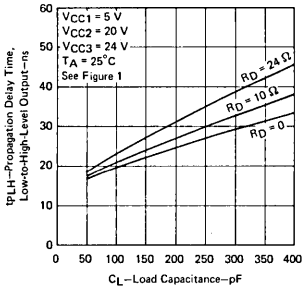

FIGURE 11

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

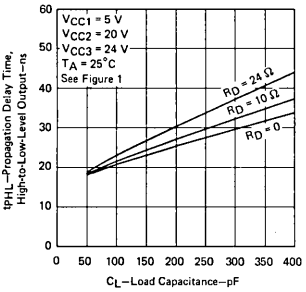

FIGURE 12

TYPICAL APPLICATION DATA

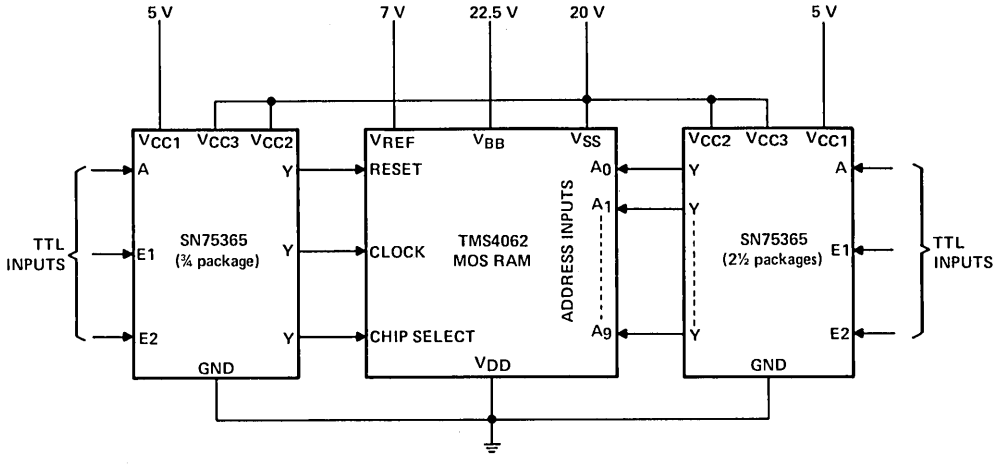

FIGURE 13—INTERCONNECTION OF SN75365 DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

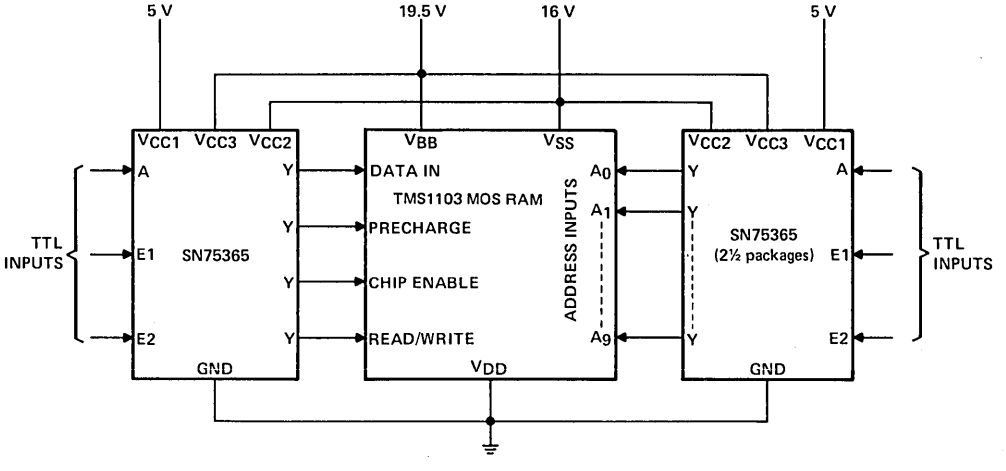

FIGURE 14—INTERCONNECTION OF SN75365 DEVICES WITH TMS1103-TYPE SILICON-GATE MOS RAM

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TYPICAL APPLICATION DATA

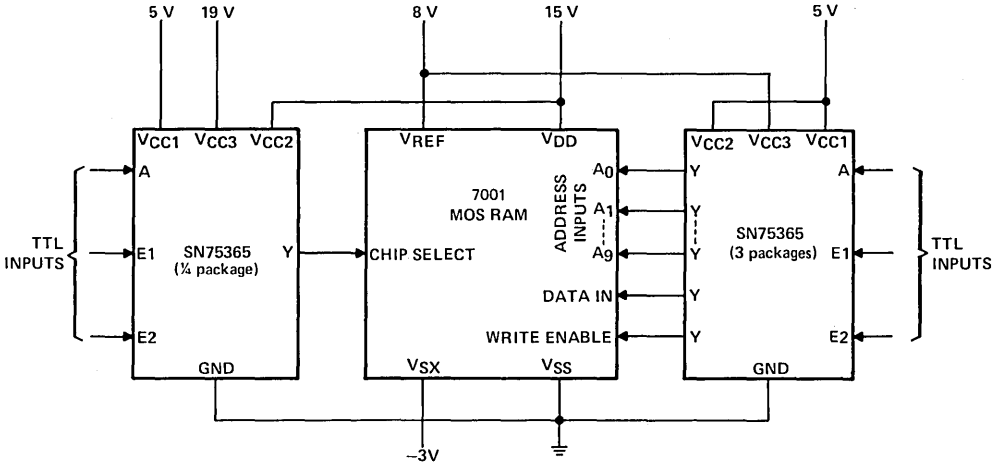
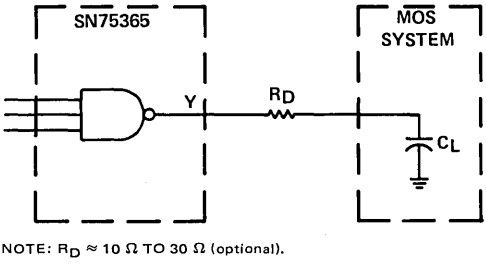


FIGURE 15–INTERCONNECTION OF SN75365 DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM



NOTE: $R_D \approx 10\ \Omega$ TO $30\ \Omega$ (optional).

FIGURE 16–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75365 APPLICATIONS

Applications using SN75365 as interface devices between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figures 13, 14, and 15. The V_{CC3} supply pin of the SN75365 may be connected to the V_{CC2} pin as shown in Figure 13 or connected to a separate voltage higher than V_{CC2} as shown in Figures 14 and 15.

Figures 13, 14, and 15 show the use of the SN75365 over a wide range of V_{CC2} and V_{CC3} supply voltages. The device may even be used as a TTL gate, if desired, by connecting V_{CC2} and V_{CC3} to 5 volts.

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between $10\ \Omega$ and $30\ \Omega$. See Figure 16.

5

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75365 driver when charging and discharging high capacitance loads over a wide voltage range at high-frequencies. Figure 6 shows the power dissipated in a typical SN75365 as a function of frequency and load capacitance. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 17.

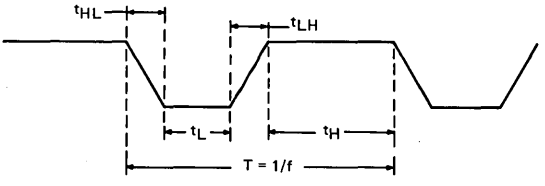


FIGURE 17–OUTPUT VOLTAGE WAVEFORM

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The SN75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H >> t_{LH} + t_{HL}$ so that P_S can be neglected. Figure 6 for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20 V, V_{OL} = 0.1 V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{4\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{-2.2\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{31\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx (100\text{ pF})(19.9\text{ V})^2(2\text{ MHz})$

$P_{C(AV)} \approx 79$ mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \approx 4(58 + 79)$

$P_{T(AV)} \approx 548$ mW typical for total package.

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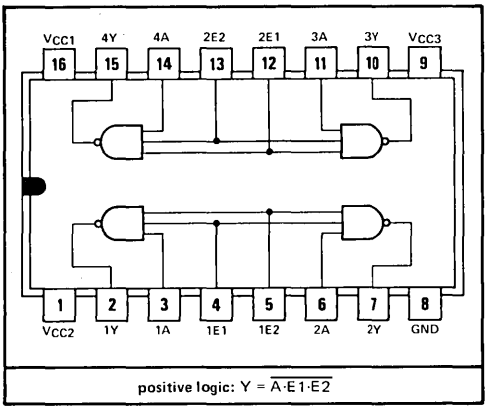
TYPE SN75366
QUADRUPLE NAND TTL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712159, APRIL 1975—REVISED APRIL 1977

MOS MEMORY INTERFACE

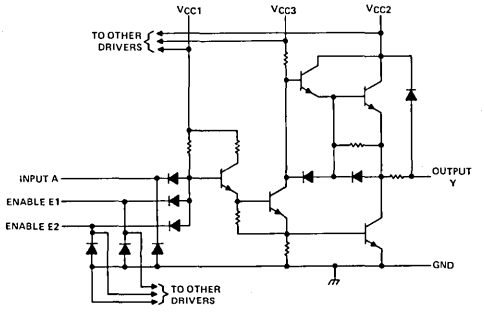
- Quad Positive-Logic NAND TTL-to-MOS Driver
- Versatile Interface Circuit for Use between TTL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Equivalent to SN75365 with Internal Output Damping Resistors
- No External Damping Resistors Needed in Most Applications
- Designed to be Interchangeable with Intel 3207
- V_{CC2} Supply Voltage Variable over Wide Range to 24 Volts Maximum
- V_{CC3} Supply Voltage Pin Available
- V_{CC3} Pin Can Be Connected to V_{CC2} Pin in Some Applications
- TTL and DTL Compatible Diode-Clamped Inputs
- Operates from Standard Bipolar and MOS Supply Voltages
- Two Common Enable Inputs per Gate-Pair
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation
- Low Standby Power Dissipation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \cdot E1 \cdot E2}$

schematic (each driver)



description

The SN75366 is a monolithic integrated quadruple TTL-to-MOS driver and interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS1103 and TMS4062.

The SN75366 operates from the TTL 5-volt supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16 volts to 20 volts, and with nominal V_{CC3} supply voltage from 3 volts to 4 volts higher than V_{CC2}. However, it is designed so as to be useable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

The SN75366 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 25 V
Supply voltage range of V_{CC3}	−0.5 V to 30 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the drivers.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75366 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3}-V_{CC2}$	0	4	10	V
Operating free-air temperature, T_A	0		70	°C

5

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3} and operating free-air temperature (unless otherwise noted)

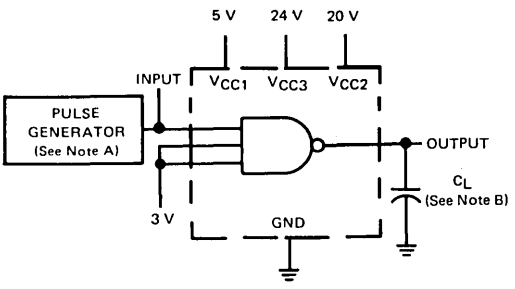
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC3} = V_{CC2}+3 V, V_{IL} = 0.8 V, I_{OH} = −100 μA		V_{CC2}−0.3	V_{CC2}−0.1		V
		V_{CC3} = V_{CC2}+3 V, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−1.7	V_{CC2}−1.2		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −50 μA		V_{CC2}−1	V_{CC2}−0.7		
		V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = −10 mA		V_{CC2}−2.8	V_{CC2}−2.1		
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 1 mA			0.15	0.3	V
		V_{CC3} = 10 V to 28 V, V_{IH} = 2 V, I_{OL} = 30 mA			1.2	1.9	
V_{OK}	Output clamp voltage	V_I = 0 V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_I = 2.4 V	A inputs			40	μA
			E1 and E2 inputs			80	
I_{IL}	Low-level input current	V_I = 0.4 V	A inputs		−1	−1.6	mA
			E1 and E2 inputs		−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 0 V, No load			4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−2.2	+0.25 −3.2	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, All inputs at 5 V, No load			31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low				0.9	2	
$I_{CC3(L)}$	Supply current from V_{CC3}, all outputs low				16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 0 V, No load				0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition	V_{CC1} = 0 V, V_{CC2} = 24 V, V_{CC3} = 24 V, All inputs at 5 V, No load				0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V (unless otherwise noted), and T_A = 25°C.

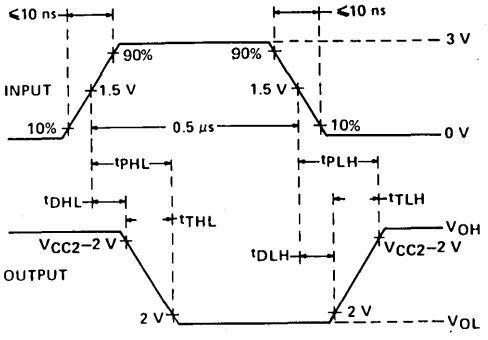
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, See Figure 1		15	22	ns
t_{DHL}	Delay time, high-to-low-level output			14	21	ns
t_{TLH}	Transition time, low-to-high-level output		5	18	33	ns
t_{THL}	Transition time, high-to-low-level output		5	18	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	33	48	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	32	48	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

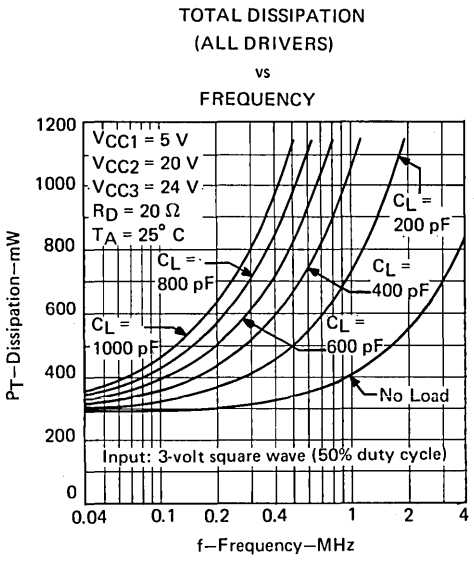


FIGURE 2

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TYPICAL APPLICATION DATA

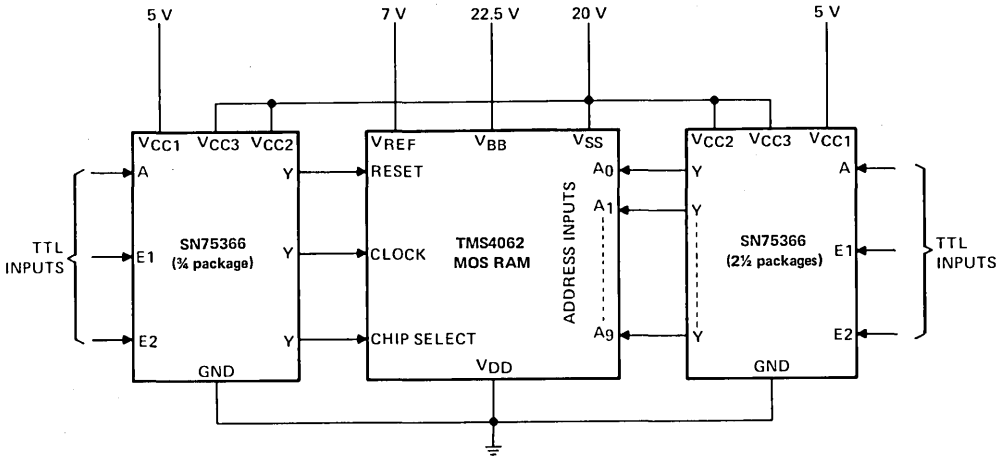


FIGURE 3–INTERCONNECTION OF SN75366 DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

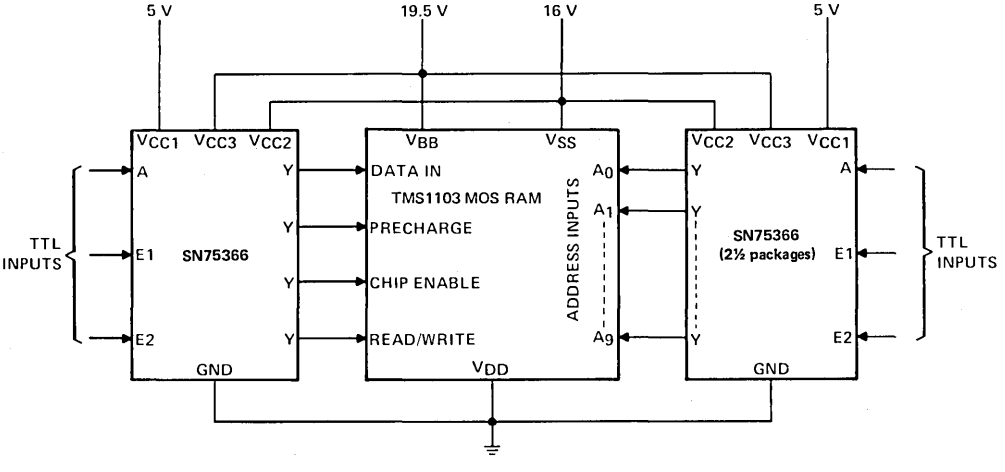


FIGURE 4–INTERCONNECTION OF SN75366 DEVICES WITH TMS1103-TYPE SILICON-GATE MOS RAM

TYPICAL APPLICATION DATA

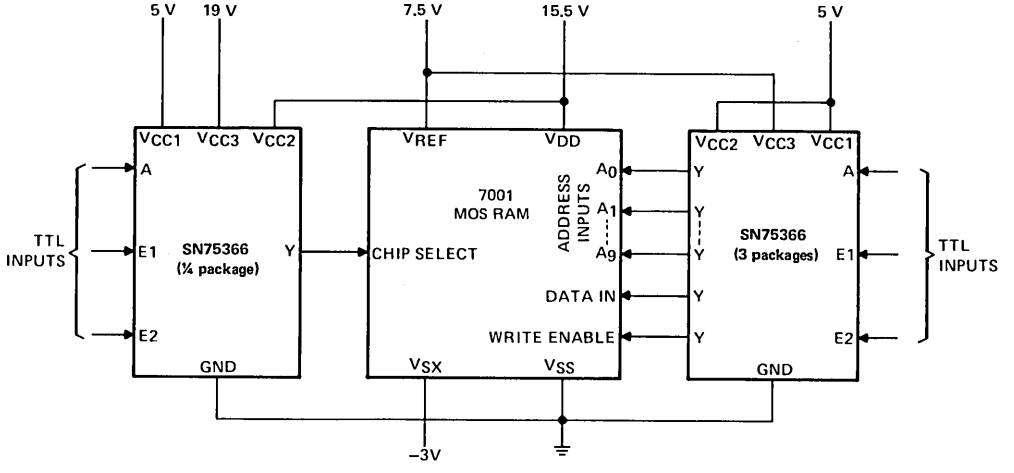
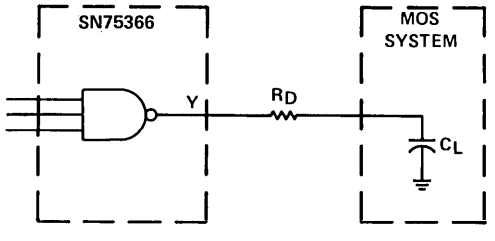


FIGURE 5—INTERCONNECTION OF SN75366 DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM



NOTE: $R_D \approx 5$ to 20 Ω (optional).

FIGURE 6—USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75366 APPLICATIONS

Applications using SN75366 as interface devices between TTL inputs and the address, control, and timing inputs for three types of MOS RAMs are shown in Figure 3, 4, and 5. The V_{CC3} supply pin of the SN75366 may be connected to the V_{CC2} pin as shown in Figure 3 or connected to a separate voltage higher than V_{CC2} as shown in Figures 4 and 5.

Figures 3, 4, and 5 show the use of the SN75366 over a wide range of V_{CC2} and V_{CC3} supply voltages. The device may even be used as a TTL gate, if desired, by connecting V_{CC2} and V_{CC3} to 5 volts.

The fast switching speeds of many MOS drivers produce undesirable output transient overshoot because of load or wiring inductance. Often a small external series damping resistor is used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed.

In most applications the internal damping resistor in the SN75366 eliminates the need for an external damping resistor. However, an external damping resistor may still be desired in some applications. See Figure 6.

TEXAS INSTRUMENTS
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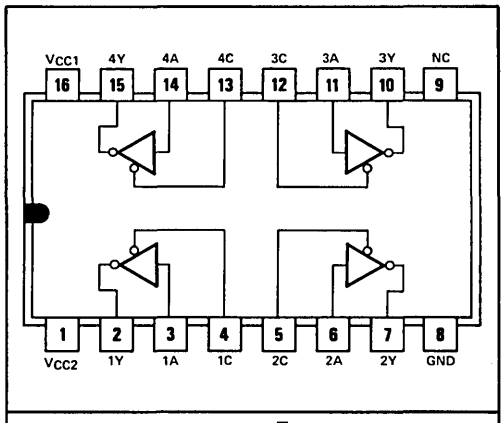
TYPE SN75367
QUADRUPLE TTL-TO-MOS DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7712374, MAY 1976—REVISED APRIL 1977

- Quad Inverting TTL-to-MOS Drivers
- Three-State Outputs
- Versatile Interface Circuit for Use Between TTL and High-Current, High-Voltage Systems
- CMOS Applications
- High-Speed Switching
- TTL- and DTL-Compatible Inputs
- Separate Address and Enable/Disable Inputs for Each Driver
- V_{CC2} Variable Over Wide Range . . . V_{CC1} to 15 V

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: $Y = \overline{A}$

Output is off (disabled) when C is high

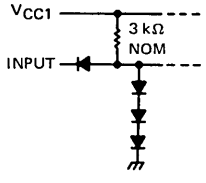
NC—No internal connection

description

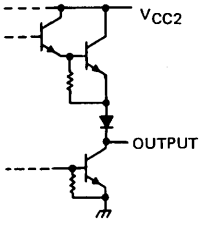
The SN75367 is a monolithic quadruple TTL-to-MOS driver and interface circuit with three-state outputs. Each driver output may be disabled to the high-impedance state by taking the C input high to allow multiple drivers to be connected to the same bus line for selective enable operation. The SN75367 is designed such that the output disable times are shorter than the output enable times to minimize the possibility that two outputs will attempt to take a common bus line to opposite logic levels. The SN75367 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 16 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.

2. For operation above 25°C free-air temperature, refer to Disipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75367 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	12	15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC1} = 4.75 V, A inputs at 0.8 V,	V_{CC2} = 10.8 V, C inputs at 0.8 V,	I_O = −50 μA	V_{CC2}−1.6	V_{CC2}−1.2		V
				I_O = −10 mA	V_{CC2}−2.7	V_{CC2}−2.4		
V_{OL}	Low-level output voltage	V_{CC1} = 4.75 V, C inputs = 0.8 V,	V_{CC2} = 10.8 V, I_O = 10 mA	A inputs at 2 V,		0.3	0.5	V
I_I	Input current at maximum input voltage	V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_I = 2.4 V					40	μA
I_{IL}	Low-level input current, A inputs	V_I = 0.4 V				−1.5	−2.2	mA
	Low-level input current, C inputs						−1.6	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC1} = 5 V, A inputs at 0 V,	V_{CC2} = 12 V, C inputs at 2.4 V,	V_O = 12 V			−250	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC1} = 5 V, A inputs at 2.4 V,	V_{CC2} = 12 V, C inputs at 2.4 V,	V_O = 0 V			250	μA
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 15 V, No load			11	16	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high						0.6	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 15 V, C inputs at 0 V,	No load		17	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					24	37	mA
$I_{CC1(Z)}$	Supply current from V_{CC1}, all outputs off	V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 15 V, C inputs at 5 V,	No load		23	32	mA
$I_{CC1(Z)}$	Supply current from V_{CC1}, all outputs off	V_{CC1} = 5.25 V, A input at 0 V,	V_{CC2} = 15 V, C inputs at 5 V,	No load		22	32	mA
$I_{CC2(Z)}$	Supply current from V_{CC2}, all outputs off	V_{CC1} = 5.25 V, A inputs at 5 V,	V_{CC2} = 15 V, C inputs at 5 V,	No load		26	39	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, and T_A = 25°C except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 250 pF, See Figures 1 thru 4	4	16	26	ns
t_{PHL}	Propagation delay time, high-to-low-level output		8	20	32	ns
t_{TLH}	Transition time, low-to-high-level output		3	15	23	ns
t_{THL}	Transition time, high-to-low-level output		6	21	32	ns
t_{PZH}	Output enable time to high level		9	21	31	ns
t_{PZL}	Output enable time to low level		10	30	42	ns
t_{PHZ}	Output disable time from high level		1	8	15	ns
t_{PLZ}	Output disable time from low level		6	15	27	ns

PARAMETER MEASUREMENT INFORMATION

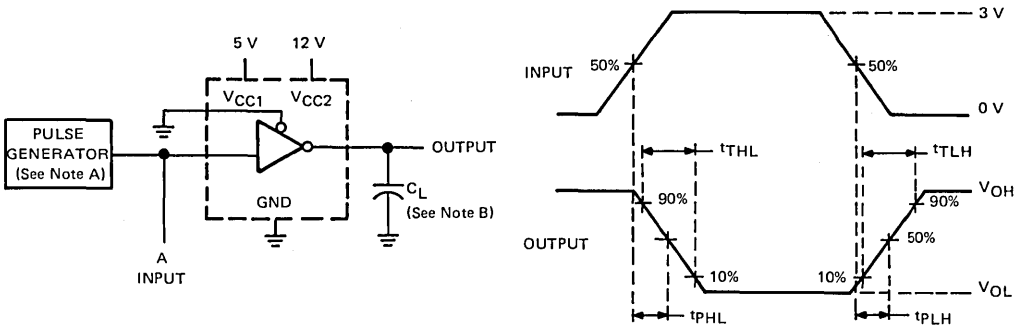


FIGURE 1–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}

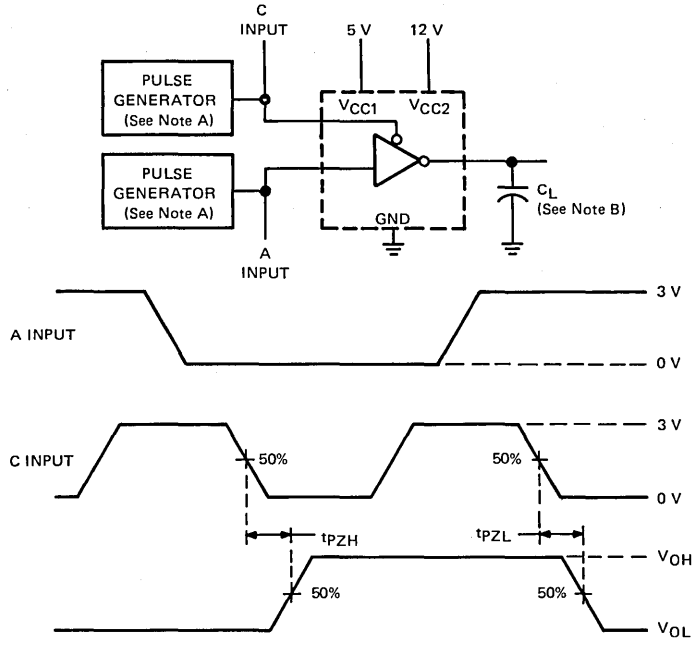


FIGURE 2–TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PZH} AND t_{PZL}

NOTES: A. The pulse generators have the following characteristics: PRR = 1 MHz, (2 MHz for C input in Figure 2), Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

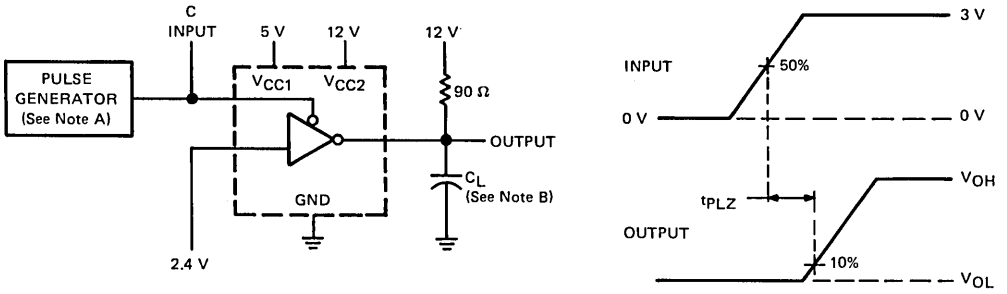


FIGURE 3—TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PLZ}

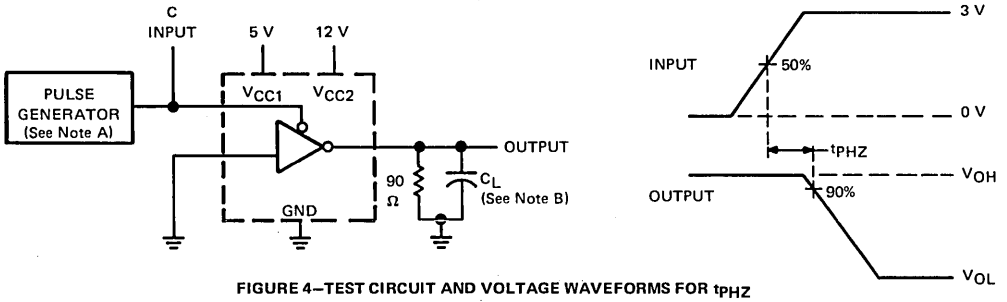


FIGURE 4—TEST CIRCUIT AND VOLTAGE WAVEFORMS FOR t_{PHZ}

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TOTAL DISSIPATION (ALL DRIVERS)
vs
FREQUENCY

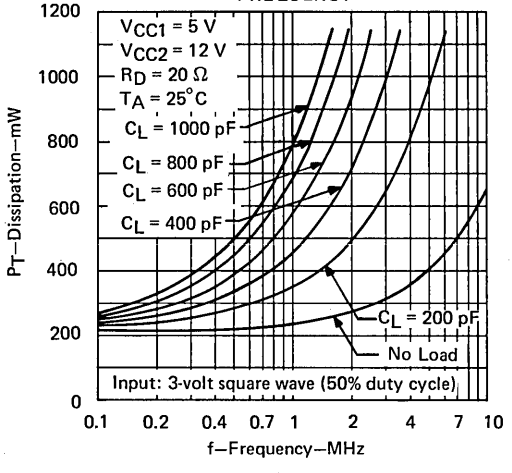


FIGURE 5

TEXAS INSTRUMENTS
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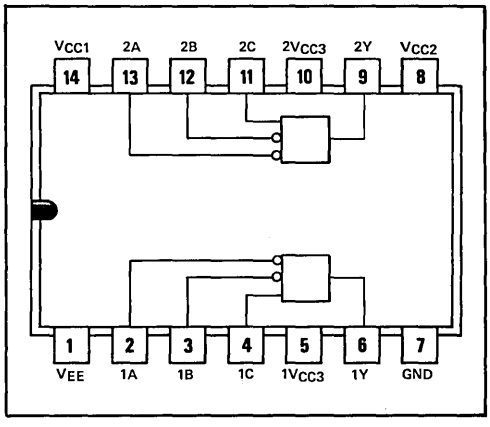
TYPE SN75368
DUAL ECL-TO-MOS DRIVER

BULLETIN NO. DL-S 7712377, APRIL 1976—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual ECL-to-MOS Drivers
- Dual ECL-to-TTL Drivers
- Versatile Interface Circuits for Use Between ECL and High-Current, High-Voltage Systems
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs
- Inputs are Compatible with Series 10000 ECL and Other Similar ECL Families
- Single In-Phase and Dual Out-of-Phase Inputs per Driver
- Operates from Standard Bipolar and MOS Supply Voltages
- V_{CC2} Supply Voltage Variable over Wide Range . . . 4.75 V to 22 V
- Two Independent V_{CC3} Supply Voltage Pins Available
- V_{CC3} Pins Can Be Connected to V_{CC2} Pin in Some Applications
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75368 is a monolithic dual ECL-to-MOS driver and interface circuit. The device accepts standard input signals from Series SN10000 ECL and other similar ECL families and provides high-current and high-voltage output levels suitable for driving MOS and TTL circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS1103, TMS1103-1, TMS4030, TMS4062, and 7001.

FUNCTION TABLE

INPUTS				OUTPUT
DIFFERENTIAL	LOGIC LEVEL			Y
(More positive of A or B)—C	A	B	C	
H ($V_{ID} \geq 150$ mV)	L	H	L	L
	H	L	L	
	H	H	L	
? (-150 mV $\leq V_{ID} \leq 150$ mV)	X	X	X	INDETERMINATE
L ($V_{ID} \leq -150$ mV)	L	L	H	H

H = high level, L = low level, X = irrelevant
See additional function tables in Figure 6.

The SN75368 operates from the TTL V_{CC} supply, the ECL V_{EE} supply, and standard MOS supplies in most applications. This device has been optimized for operation with a V_{CC2} supply voltage from 12 volts to 20 volts with nominal V_{CC3} supply voltages from 3 to 4 volts higher than V_{CC2}. However, the SN75368 was designed so as to be useable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the two V_{CC3} pins to the V_{CC2} pin. By connecting the V_{CC2} pin to the TTL 5-volt supply, the device can be used as an ECL-to-TTL converter.

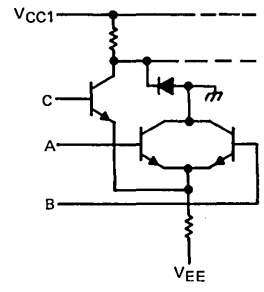
The device has one in-phase and two out-of-phase ECL-compatible inputs per driver. By proper connections of the inputs, the SN75368 may be used three ways: positive-NOR gate, differential ECL line receiver, or noninverting gate. Some applications require one input per gate to be connected to an externally generated ECL reference voltage, V_{BB}.

The SN75368 is characterized for operation from 0°C to 70°C.

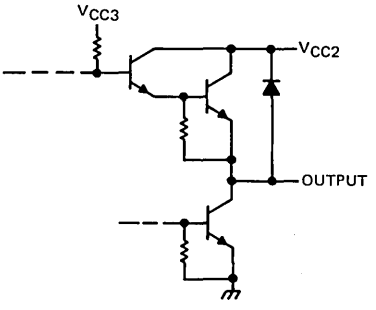
TYPE SN75368
DUAL ECL-TO-MOS DRIVER

schematics of inputs and outputs

EQUIVALENT OF INPUTS



TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 to 22 V
Supply voltage range of $1V_{CC3}$ and $2V_{CC3}$ . . . . . −0.5 to 30 V
Supply voltage range of V_{EE} . . . . . −8 to 0.5 V
Negative voltage at V_{CC1}, V_{CC2}, $1V_{CC3}$, or $2V_{CC3}$ with respect to V_{EE} . . . . . −0.5 V
Input voltage range . . . . . −7V to 0.5 V
Negative voltage at any input with respect to V_{EE} . . . . . −1 V
Differential input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65° to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75368 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	22	V
Supply voltage, $1V_{CC3}$ and $2V_{CC3}$	V_{CC2}	24	28	V
Voltage difference between supply voltages: $1V_{CC3}-V_{CC2}$ and $2V_{CC3}-V_{CC2}$	0	4	10	V
Supply voltage, V_{EE}	−4.68	−5.2	−5.72	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels (see Note 3)

PARAMETER		B (Least Positive)	A (Most Positive)	UNIT
V_{IH}	High-level input voltage at any input	−1.5	−0.7	V
V_{IL}	Low-level input voltage at any input	V_{EE}	$V_{IH}-150$ mV	
V_{IDH}	High-level differential input voltage (see Note 3)	150		mV
V_{IDL}	Low-level differential input voltage (see Note 3)		−150	mV

NOTE 3: Differential input voltage is the voltage at the more-positive inverting input (A or B) with respect to the noninverting input (C) of the same gate.

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electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, V_{EE}, and operating free-air temperature (unless otherwise noted)

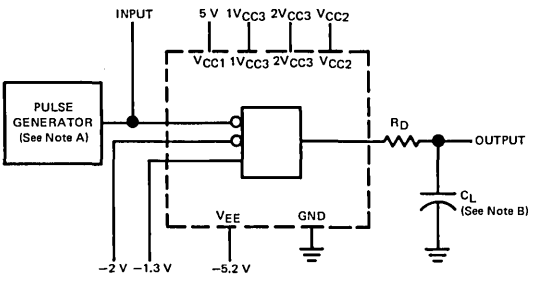
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC3} = V_{CC2} + 3$ V, $V_{IDL} = -150$ mV, $I_{OH} = -100$ μA	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2} + 3$ V, $V_{IDL} = -150$ mV, $I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		
		$V_{CC3} = V_{CC2}$, $V_{IDL} = -150$ mV, $I_{OH} = -50$ μA	$V_{CC2}-1$	$V_{CC2}-0.7$		
		$V_{CC3} = V_{CC2}$, $V_{IDL} = -150$ mV, $I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage	$V_{IDH} = 150$ mV, $I_{OL} = 10$ mA		0.15	0.3	V
		$V_{CC3} = 10$ V to 28 V, $V_{IDH} = 150$ mV, $I_{OL} = 30$ mA		0.2	0.4	
V_{OK}	Output clamp voltage	$V_{ID} = -500$ mV, $I_{OH} = 20$ mA			$V_{CC2}+1.5$	V
I_{IH}	High-level input current	$V_{EE} = -5.72$ V, $V_I = -0.7$ V, All other inputs at −5.72 V		300	800	μA
I_{IL}	Low-level input current	$V_I = -2$ V, All other inputs at −0.7 V			−10	μA
		$V_{EE} = -5.72$ V, $V_I = -5.72$ V, All other inputs at −0.7 V			−100	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high	$V_{CC1} = 5.25$ V, $V_{CC2} = 22$ V, $V_{CC3} = 28$ V, $V_{EE} = -5.72$ V, All A and B inputs at −2 V, Both C inputs at −0.7 V, No load		21	38	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high			−2	+0.25 −3.6	
$I_{CC3(H)}$	Supply current from $1V_{CC3}$ or $2V_{CC3}$, all outputs high			1	1.8	
$I_{EE(H)}$	Supply current from V_{EE}, all outputs high			−21	−38	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low	$V_{CC1} = 5.25$ V, $V_{CC2} = 22$ V, $V_{CC3} = 28$ V, $V_{EE} = -5.72$ V, All A and B inputs at −0.7 V, Both C inputs at −2 V, No load		13	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low			0.5	1	
$I_{CC3(L)}$	Supply current from $1V_{CC3}$ or $2V_{CC3}$, all outputs low			4	8	
$I_{EE(L)}$	Supply current from V_{EE}, all outputs low			−21	−38	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high	$V_{CC1} = 5.25$ V, $V_{CC2} = 22$ V, $V_{CC3} = 22$ V, $V_{EE} = -5.72$ V, All A and B inputs at −2 V, Both C inputs at −0.7 V, No load			0.25	mA
$I_{CC3(H)}$	Supply current from $1V_{CC3}$ or $2V_{CC3}$, all outputs high				0.25	
$I_{CC2(S)}$	Supply current from V_{CC2}, stand-by condition	$V_{CC1} = 0$ V, $V_{CC2} = 22$ V, $V_{CC3} = 22$ V, $V_{EE} = 0$ V, All A and B inputs at −0.7 V, Both C inputs at −2 V, No load			0.25	mA
$I_{CC3(S)}$	Supply current from $1V_{CC3}$/ $2V_{CC3}$, stand-by condition				0.25	

†All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $V_{EE} = -5.2$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC1} and V_{CC2} are as stated under test conditions.

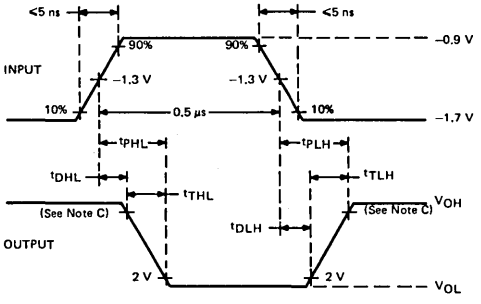
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{EE} = -5.2$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC3} = 24$ V			$V_{CC3} = 20$ V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{DLH}	Delay time, low-to-high-level output	$C_L = 390$ pF, $R_D = 10$ Ω, See Figure 1	4	12	22	5	13	23	ns
t_{DHL}	Delay time, high-to-low-level output		5	13	23	5	15	24	ns
t_{TLH}	Transition time, low-to-high-level output		7	19	32	8	20	33	ns
t_{THL}	Transition time, high-to-low-level output		8	20	33	6	18	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output		11	31	54	13	33	56	ns
t_{PHL}	Propagation delay time, high-to-low-level output		13	33	56	11	33	57	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The high-level reference point is 17 V when $V_{CC3} = V_{CC2} = 20$ V, and is 18 V when $V_{CC3} = V_{CC2} + 4\ V = 24$ V.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

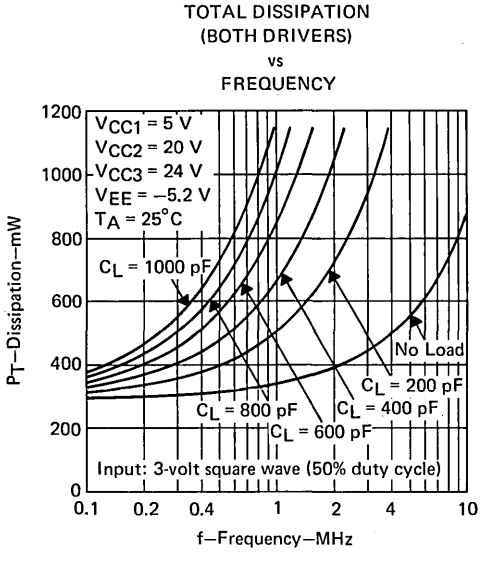


FIGURE 2

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TYPICAL APPLICATION DATA

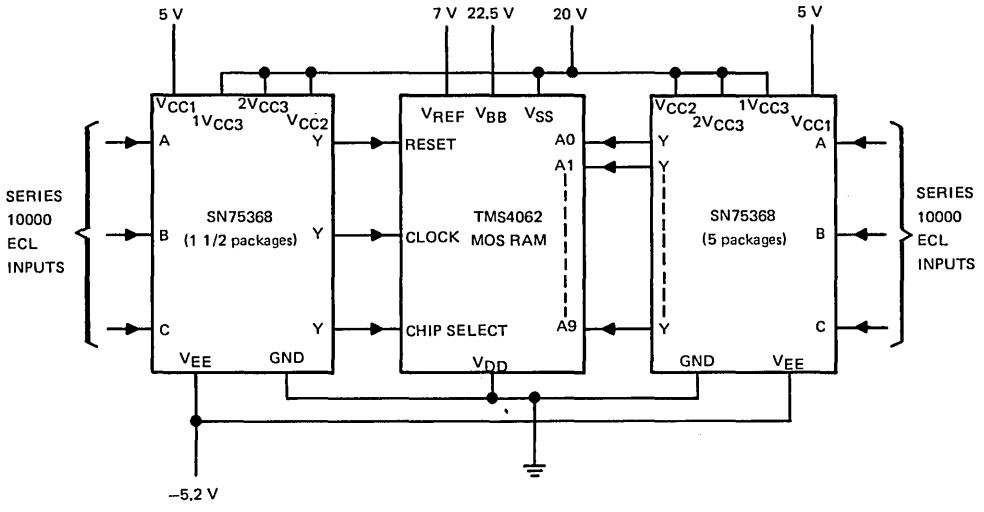


FIGURE 3–INTERCONNECTION OF SN75368 DEVICES WITH TMS4062-TYPE P-CHANNEL MOS RAM

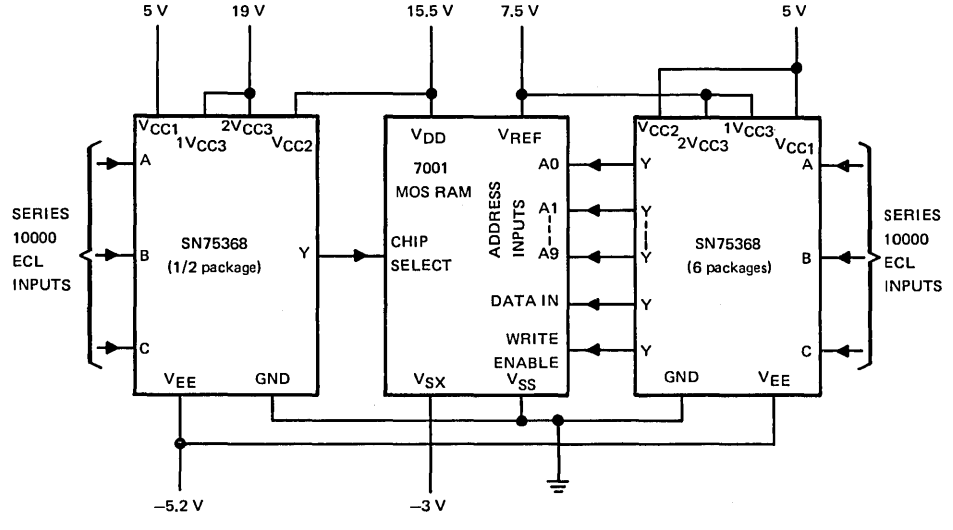
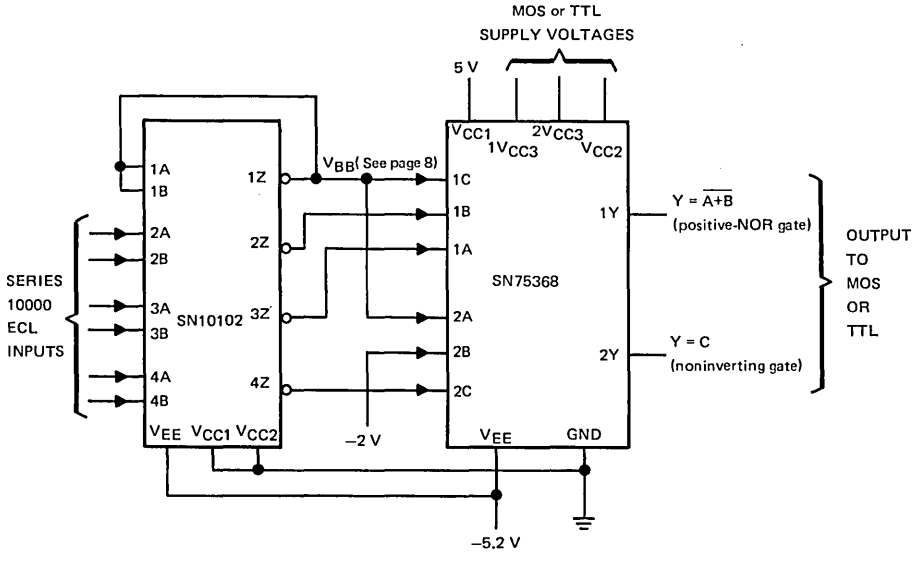
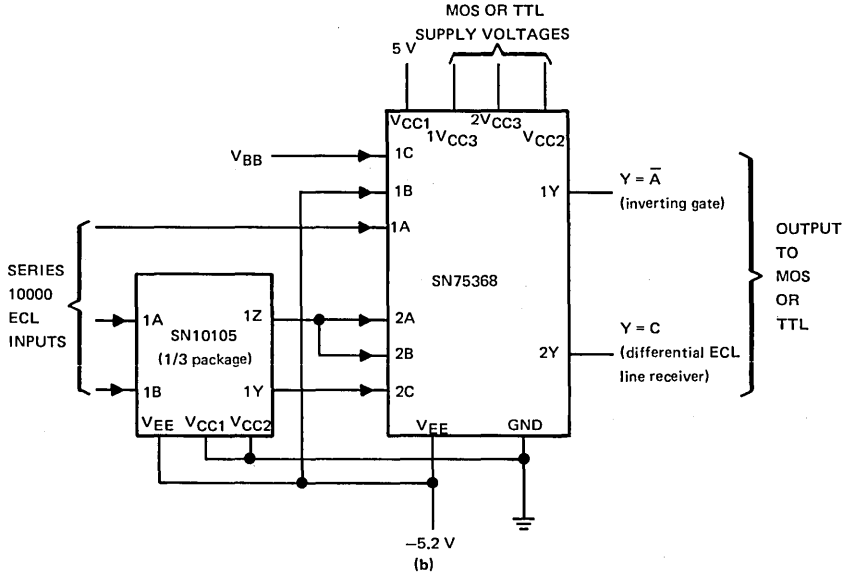


FIGURE 4–INTERCONNECTION OF SN75368 DEVICES WITH 7001-TYPE N-CHANNEL MOS RAM

TYPICAL APPLICATION DATA



(a)



(b)

FIGURE 5–REPRESENTATIVE METHODS OF INTERCONNECTING SN75368 DEVICES WITH SN10000 SERIES ECL

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TYPICAL APPLICATION DATA

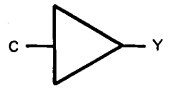
positive-NOR gate

$Y = \overline{A+B}$

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
C at V_{BB}	L	L	V_{BB}	H
	H	X	V_{BB}	L
	X	H	V_{BB}	L

noninverting gate

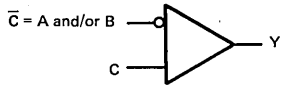


Y = C

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	L
	V_{BB}	V_{BB}	H	H
A at V_{BB}, B connected low	V_{BB}	L	L	L
	V_{BB}	L	H	H
B at V_{BB}, A connected low	L	V_{BB}	L	L
	L	V_{BB}	H	H

differential ECL line receiver



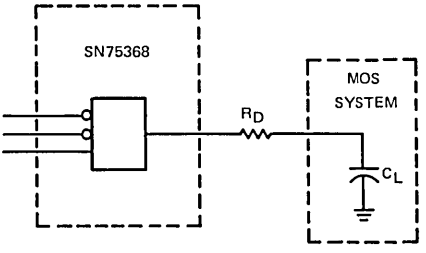
Y = C

FUNCTION TABLE

CONFIGURATION	INPUTS			OUTPUT
	A	B	C	Y
A and B connected together	H	H	L	L
	L	L	H	H
A not used but connected low	L	H	L	L
	L	L	H	H
B not used but connected low	H	L	L	L
	L	L	H	H

H = high level, L = low level, X = irrelevant
V_{BB} = Reference Supply voltage for SN10000 Series ECL.

FIGURE 6–FUNCTIONS



NOTE: $R_D \approx 10\ \Omega$ to $30\ \Omega$ (optional).

FIGURE 7–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75368 APPLICATIONS

Applications using the SN75368 as an interface device between series SN10000 ECL inputs and the address, control, and timing inputs for two types of MOS RAMS are shown in Figures 3 and 4. The $1V_{CC3}$ and $2V_{CC3}$ supply pins of the SN75368 may be connected to the V_{CC2} pin as shown in Figure 3 or connected to a separate voltage higher than V_{CC2} as shown in Figure 4. If desired, the $1V_{CC3}$ pin may be connected to a voltage different from the $2V_{CC3}$ pin.

Figures 3 and 4 show the use of the SN75368 over a wide range of V_{CC2}, $1V_{CC3}$, and $2V_{CC3}$ supply voltages. This device may even be used as ECL-to-TTL-level converters, if desired, by connecting V_{CC2}, $1V_{CC3}$, and $2V_{CC3}$ to 5 volts.

The one in-phase (C) and two out-of phase (A and B) inputs per driver permit much flexibility when using the SN75368. By connecting the correct input to an externally generated V_{BB} (ECL reference supply voltage) positive-NOR gate, inverting gate, or noninverting gate functions may be obtained as shown in Figure 5. By driving the correct inputs differentially as in Figure 5 (b), these devices may be used as differential ECL line receivers and no V_{BB} reference voltage is required. The V_{BB} reference voltage may be generated as in Figure 5 (a) by connecting the output of an ECL gate to its out-of-phase input, by using the V_{BB} pin of certain ECL devices such as SN10115, or by other methods. An unused out-of-phase input may be connected low or connected to the other out-of-phase input of the same gate in many applications. Function tables for many of these applications are shown in Figure 6.

The fast switching speeds of the SN75368 may produce undersirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the overall load characteristics and switching speed. A typical value would be between 10 Ω and 30 Ω. See Figure 7.

5

5

TYPE SN75369
DUAL MOS DRIVER

BULLETIN NO. DL-S 7712380, APRIL 1976—REVISED APRIL 1977

MOS MEMORY INTERFACE

- Dual Inverting MOS Driver
- Low Standby Power Dissipation
- Versatile Interface Circuit for Use between TTL Levels and Level-Shifted High-Current, High-Voltage Systems
- Inputs May Be Level-Shifted by Use of a Current Source or Capacitive Coupling or Driven Directly by a Voltage Source
- Designed to Be Functionally Interchangeable with National DS0026
- Capable of Driving High-Capacitance Loads
- Compatible with Many Popular MOS RAMs and MOS Shift Registers
- V_{CC} Supply Voltage Variable over Wide Range to 22 Volts Maximum with Respect to V_{EE}
- Operates from Standard Bipolar and/or MOS Supply Voltage
- High-Speed Switching
- Transient Overdrive Minimizes Power Dissipation

description

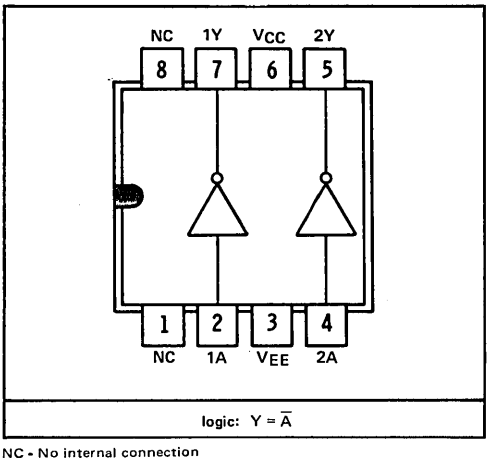
The SN75369 is a monolithic dual MOS driver and interface circuit that operates with either current-source or voltage-source input signals. The device accepts appropriate level-shifted input signals from TTL or other logic systems and provides high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The SN75369 operates from standard MOS and/or bipolar supplies in most applications. This device has been optimized for operation with V_{CC} supply voltage from 12 volts to 20 volts positive with respect to V_{EE}. However, it is designed so as to be usable over a wide range of V_{CC}.

Inputs of the SN75369 are referenced to the V_{EE} terminal and contain a series current-limiting resistor. The device will operate with either positive current input signals or voltage input signals that are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12 volts to −15 volts with the inputs to be driven from TTL levels or other positive voltage levels. The required negative-level shifting may be done with an external p-n-p transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

The SN75369 is characterized for operation from 0°C to 70°C.

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)

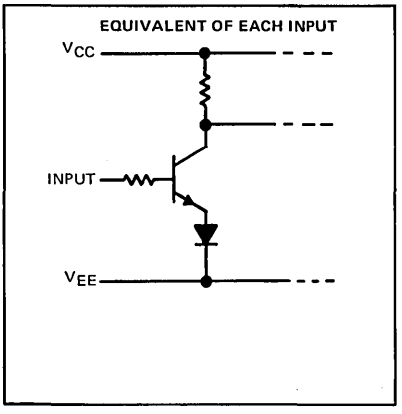


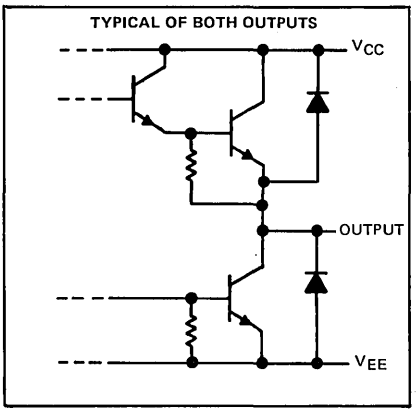
logic: $Y = \overline{A}$

NC - No internal connection

5

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1) . . . . . −0.5 V to 22 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. Voltage values are with respect to the V_{EE} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the JG package, SN75369 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	20	22	V
Operating free-air temperature, T_A	0		70	°C

definition of input logic levels

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.5		4.5	V
V_{IL}	Low-level input voltage			0.5	V
I_{IH}	High-level input current	8		20	mA
I_{IL}	Low-level input current			27	mA

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electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (See Note 3)		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.5 V,	I_{OH} = −50 μA	V_{CC}−1	V_{CC}−0.7		V
		I_{IL} = 0.7 mA,	I_{OH} = −50 μA				
		V_{IL} = 0.5 V,	I_{OH} = −10 mA	V_{CC}−2.3	V_{CC}−1.8		
		I_{IL} = 0.7 mA,	I_{OH} = −10 mA				
V_{OL}	Low-level output voltage	V_{IH} = 2.5 V,	I_{OL} = 10 mA		0.15	0.3	V
		I_{IH} = 8 mA,	I_{OL} = 10 mA				
		V_{CC} = 10 V to 22 V,	V_{IH} = 2.5 V, I_{OL} = 30 mA		0.2	0.4	
		V_{CC} = 10 V to 22 V,	I_{IH} = 8 mA, I_{OL} = 30 mA				
V_{OK}	Output clamp voltage	V_I = 0 V,	I_{OH} = 20 mA			V_{CC}+1.5	V
V_I	Input voltage	I_I = 20 mA			3.7	5	V
		I_I = 8 mA			2.4	3	
		I_I = 0.7 mA			0.4	0.6	
I_I	Input current	V_I = 4.5 V			27	45	mA
		V_I = 2.5 V			9	15	
		V_I = 0.5 V				1.5	
$I_{CC(H)}$	Supply current from V_{CC}, both outputs high	V_{CC} = 22 V, Both inputs at 0 V,	No load			0.5	mA
$I_{CC(L)}$	Supply current from V_{CC}, both outputs low	V_{CC} = 22 V, Both inputs at 3 V,	No load		7	12	mA

†All typical values are at V_{CC} = 20 V and T_A = 25°C.

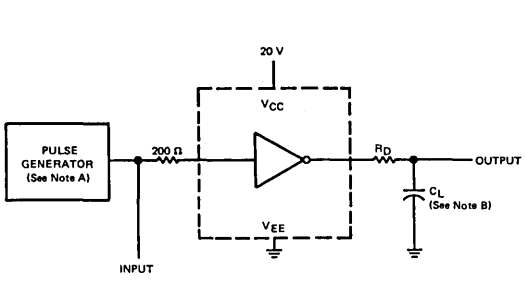
NOTE 3: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

switching characteristics, V_{CC} = 20 V, T_A = 25°C

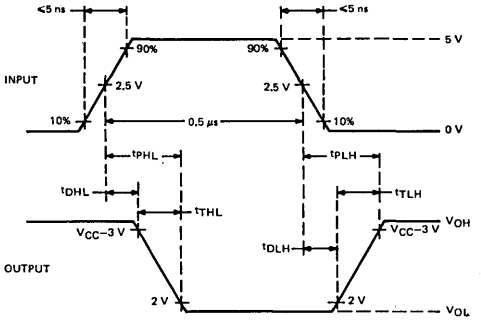
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1	8	16	24	ns
t_{DHL}	Delay time, high-to-low-level output		4	11	20	ns
t_{TLH}	Transition time, low-to-high-level output		8	18	30	ns
t_{THL}	Transition time, high-to-low-level output		6	16	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		16	35	54	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	28	50	ns

5

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

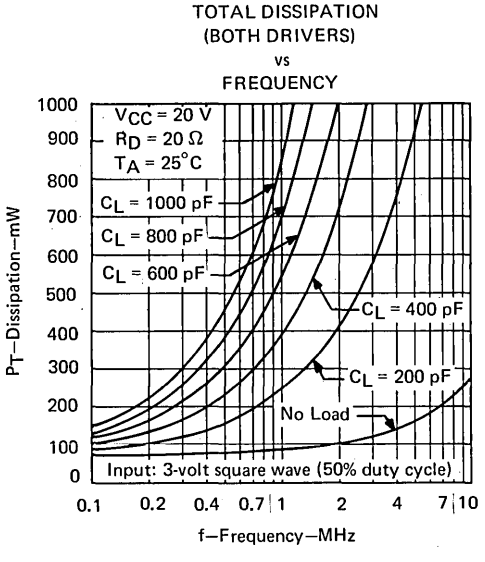


FIGURE 2

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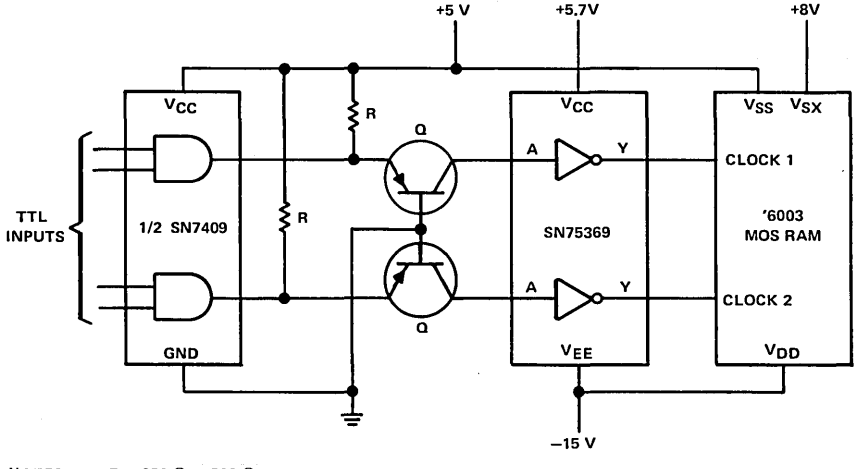
TYPICAL APPLICATION DATA

Applications of the SN75369 used as an interface device in systems converting TTL signals to negative-polarity MOS clock signals are shown in Figures 3 and 4. In both applications the SN75369 V_{EE} pin is connected to a negative MOS supply voltage. Figure 3 and 4 show the use of the SN75369 over a wide range of V_{CC} supply voltages. The device may even be used as a TTL level driver, if desired, by connecting V_{CC} to 5 volts.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the SN75369, which are referenced to the V_{EE} terminal. A p-n-p transistor current source is used to level shift in Figure 3. Resistor R sets the current and an open-collector TTL gate is used to switch the p-n-p transistor. Figure 4 shows capacitive coupling being used to level shift. The SN7437 TTL buffer gate is used as a voltage source driver with pull-up resistor R providing additional high-level drive. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

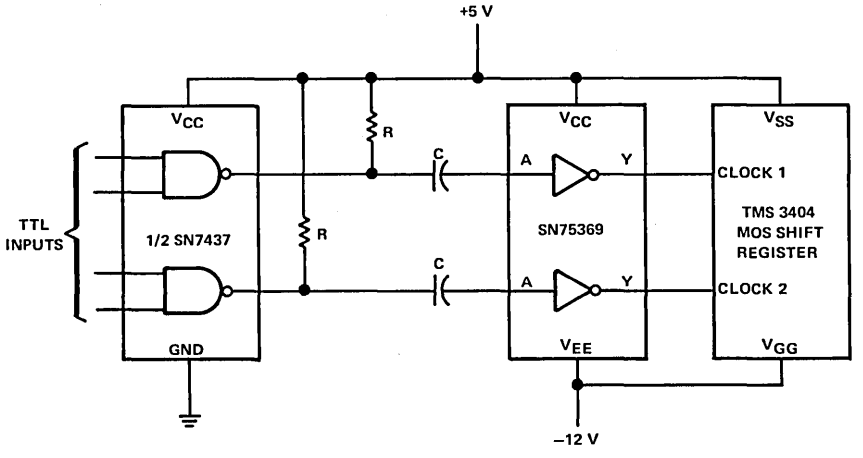
The fast switching speeds of the SN75369 may produce undersirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 Ω and 30 Ω. See Figure 5.



NOTES: A. R ≈ 350 Ω to 500 Ω.
B. Q is 2N3829 or equivalent.

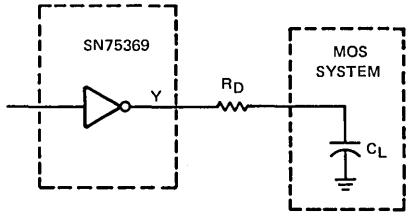
FIGURE 3–MOS RAM CLOCK DRIVER SYSTEM WITH P-N-P TRANSISTOR CURRENT SOURCE USED TO SHIFT LEVELS TO INPUTS OF SN75369

TYPICAL APPLICATION DATA



NOTE A: R ≈ 100 Ω to 250 Ω.

FIGURE 4–MOS SHIFT REGISTER CLOCK DRIVER SYSTEM WITH CAPACITIVE COUPLING USED TO SHIFT LEVELS TO INPUTS OF SN75369



NOTE: $R_D \approx 10\ \Omega$ to 30 Ω (optional)

FIGURE 5–USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN SN75369 APPLICATIONS

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TYPE SN75370
DUAL-CHANNEL INTERFACE TO MOS MEMORIES

BULLETIN NO. DL-S 7712059, SEPTEMBER 1973 — REVISED APRIL 1977

DUAL READ/WRITE AMPLIFIER FOR INTERFACING BETWEEN TTL AND TMS4062-TYPE MOS RANDOM-ACCESS MEMORY (RAM)

performance features

- Node Terminals Connect Directly to I/O Terminals of TMS4062 (AMS6002) and Similar MOS RAMs
- In Write Mode, Write Driver Provides Complementary High-Voltage Outputs at Node Terminals
- In Read Mode, Read Amplifier Responds to Small Differential-Input Current in Node Terminals

ease of design features

- TTL and DTL Compatible Diode-Clamped Inputs
- TTL and DTL Compatible Data Outputs
- 50-mA Data Output Sink-Current Capability
- Data Outputs May Be Wire-AND Connected
- Operates Over Wide Range of Supply Voltages
- Minimizes or Eliminates External Components

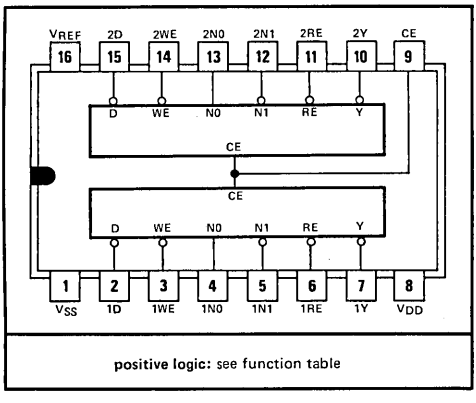
description

The SN75370 is a monolithic integrated circuit read/write amplifier that is designed to interface the Input/Output (I/O) terminals of the TMS4062 (AMS6002) and similar type MOS RAMs with TTL.

The device contains two separate channels. Each channel consists of a write driver and a read amplifier, which are common at the input/output node (N) terminals. These terminals are outputs for the write driver and inputs for the read amplifier. In the write mode, the write driver circuit is designed to write MOS-level binary information into the MOS RAM under control of TTL inputs. In the read mode, the read amplifier is designed to read MOS-level binary information from the MOS RAM and convert it to TTL levels at the data output. This is controlled by TTL inputs also.

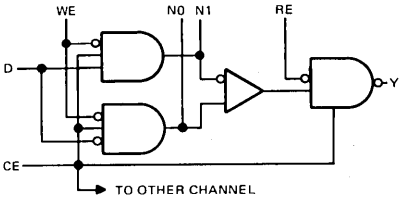
Data outputs are constructed so that they may be wire-AND connected to other outputs and/or be connected to an external pull-up resistor, if desired. The device has a chip-enable input common to both channels which can be used to enable the entire device. Internal voltage regulators permit circuit operation over a wide range of supply voltages.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function table

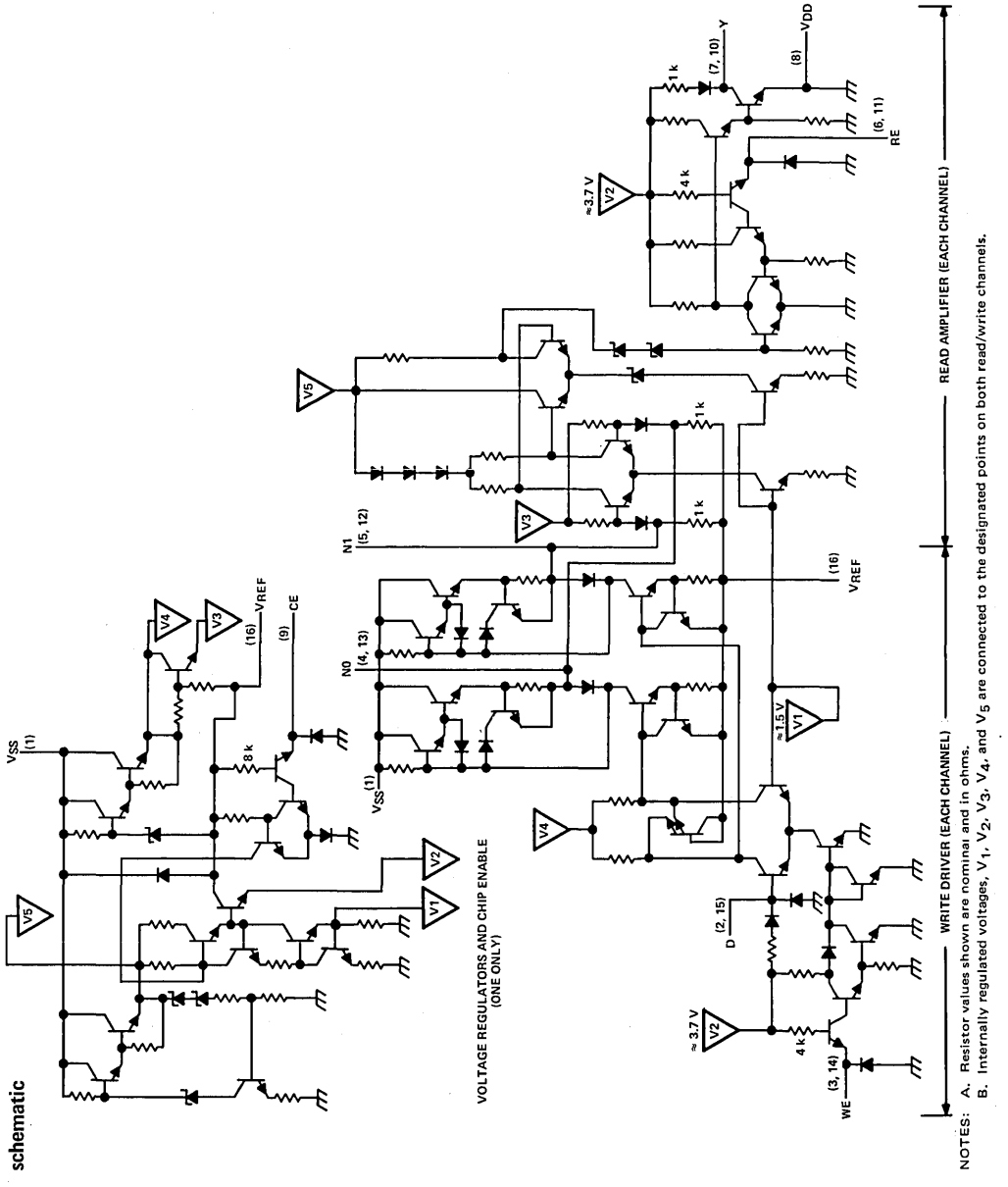
functional block diagram (each channel)



FUNCTION TABLE

MODE	VOLTAGE INPUTS				VOLTAGE OUTPUTS		DIFFERENTIAL CURRENT INPUT	OUTPUT
	CE	WE	RE	D	N0	N1	N1–N0	Y
Write 0	H	L	H	L	H	L	X	H
Write 1	H	L	H	H	L	H	X	H
Read 0	H	H	L	X	L	L	L	L
Read 1	H	H	L	X	L	L	H	H
Standby	H	H	H	X	L	L	X	H
Disabled	L	X	X	X	L	L	X	Off

H = high level (voltage or current), L = low level (voltage or current), X = irrelevant
Input levels at CE, WE, RE, and D, and output levels at Y are TTL-compatible.
Voltage output levels at N fall between V_{SS} and V_{REF}.



NOTES: A. Resistor values shown are nominal and in ohms.
B. Internally regulated voltages, V_1, V_2, V_3, V_4, and V_5 are connected to the designated points on both read/write channels.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{SS} (see Note 1)	−0.5 V to 25 V
Supply voltage range, V_{REF}	−0.5 V to 15 V
Voltage-difference range between supply voltages, $V_{SS}-V_{REF}$	−0.5 V to 20 V
Input voltage at CE, WE, RE, or D	5.5 V
Output voltage at Y	7 V
Continuous output current into Y	50 mA
Continuous current into any node terminal	±40 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) : J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the V_{DD} terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75370 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{SS}	17	20	22	V
Supply voltage, V_{REF}	4.5	7	10	V
Voltage difference between supply voltages, $V_{SS}-V_{REF}$	8	13	16	V
Operating free-air temperature, T_A	0		70	°C

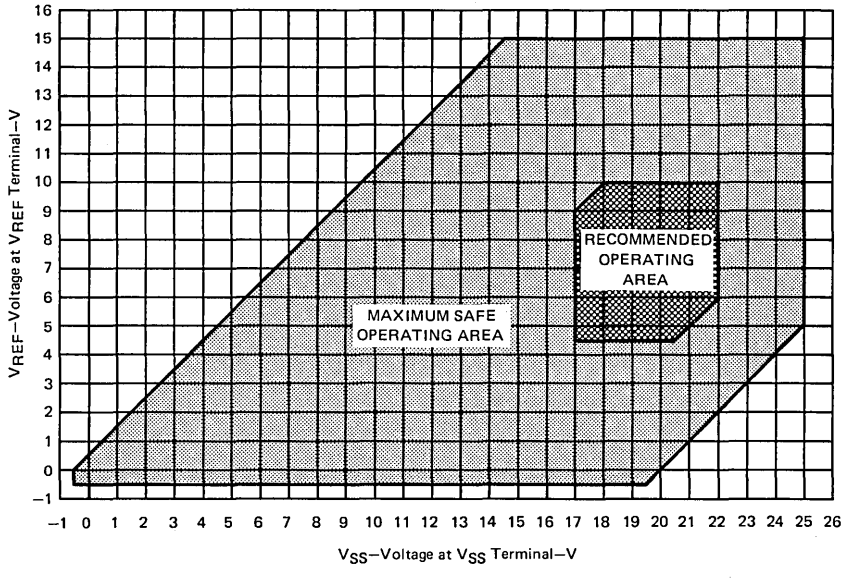


FIGURE 1–MAXIMUM SAFE OPERATING AREA AND RECOMMENDED OPERATING AREA

definition of input logic levels

PARAMETER		B (LEAST POSITIVE)	A (MOST POSITIVE)	UNIT
V_{IH}	High-level input voltage at CE, WE, RE, or D	2		V
V_{IL}	Low-level input voltage at CE, WE, RE, or D		0.8	V
I_{IDH}	High-level differential input current in node terminals (see Note 3)	50		μA
I_{IDL}	Low-level differential input current in node terminals (see Note 3)		−50	μA

NOTE 3: $I_{ID} = I_{N1} - I_{N0}$ with current into a terminal being a positive value.

electrical characteristics over recommended ranges of V_{SS}, V_{REF}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at CE, WE, RE, or D	2	$I_I = -12$ mA				−1.5	V
V_{ONH}	High-level output voltage at node terminals	3	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{NH} = 0$		$V_{SS}-2$	$V_{SS}-1.6$		V
			$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{NH} = -40$ mA		$V_{SS}-3$	$V_{SS}-2$		
V_{ONL}	Low-level output voltage at node terminals	3	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{NL} = 0$		V_{REF}	$V_{REF}+0.2$	$V_{REF}+1$	V
			$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{NL} = 20$ mA		V_{REF}	$V_{REF}+1.2$	$V_{REF}+2$	
I_{OH}	High-level output current into output Y	4	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{IDH} = 50$ μA, $V_{OH} = 5.5$ V				100	μA
V_{OH}	High-level output voltage at output Y	4	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{IDH} = 50$ μA, $I_{OH} = -200$ μA		2.2	2.8	4.5	V
V_{OL}	Low-level output voltage at output Y	4	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{IDL} = -50$ μA, $I_{OL} = 50$ mA			0.25	0.4	V
I_I	Input current at maximum input voltage into CE, WE, RE, or D	5	$V_I = 5.5$ V				1	mA
I_{IH}	High-level input current into CE, WE, or RE	5	$V_I = 2.4$ V				40	μA
I_{IH}	High-level input current into D	5	$V_I = 2.4$ V			−150	+80 −600	μA
I_{IL}	Low-level input current into CE, WE, RE, or D	2	$V_I = 0.4$ V			−0.7	−1.6	mA
r_N	Resistance from any node to V_{REF}	6	V_{SS} open, $V_{REF} = 0$, $I_N = 500$ μA, $T_A = 25°C$		0.7	1‡	1.3	kΩ
I_{OS}	Short-circuit output current into D	7	$V_O = 0$ V	CE at 2 V		−3.2	−4.5	mA
				CE at 0.8 V			−1	

See next page for supply current and dissipation.

†All typical values, except for r_N and $I_{REF(D, O)}$, are at $V_{SS} = 20$ V, $V_{REF} = 7$ V, $T_A = 25°C$.
‡Typical value of r_N is with V_{SS} open, $V_{REF} = 0$ V, $T_A = 25°C$.

supply current and dissipation over operating free-air temperature range (unless otherwise noted)

PARAMETER		MODE	TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I_{SS(D)}$	Current from V_{SS}	Disabled	8	V_{SS} = 20 V, V_{REF} = 7 V		27	35	mA
$I_{REF(D)}$	Current from V_{REF}					−20	−25	mA
P_D	Dissipation					410	500	mW
$I_{SS(SB)}$	Current from V_{SS}	Standby	8	V_{SS} = 20 V, V_{REF} = 7 V		31	39	mA
$I_{REF(SB)}$	Current from V_{REF}					−12	−18	mA
P_{SE}	Dissipation					560	690	mW
$I_{SS(R1)}$	Current from V_{SS}	Read-1	8	V_{SS} = 20 V, V_{REF} = 7 V, I_{N1} = 100 μA		31	39	mA
$I_{REF(R1)}$	Current from V_{REF}					−12	−18	mA
P_{R1}	Dissipation					540	690	mW
$I_{SS(R0)}$	Current from V_{SS}	Read-0	8	V_{SS} = 20 V, V_{REF} = 7 V, I_{N0} = 100 μA		31	39	mA
$I_{REF(R0)}$	Current from V_{REF}					4	10	mA
P_{R0}	Dissipation					640	790	mW
$I_{SS(W)}$	Current from V_{SS}	Write	8	V_{SS} = 20 V, V_{REF} = 7 V, See Note 4		53	66	mA
$I_{REF(W)}$	Current from V_{REF}					−23	−31	mA
P_W	Dissipation					910	1100	mW
$I_{REF(D,O)}$	Current from V_{REF}	Disabled, V_{SS}-open	8	V_{SS} open, V_{REF} = 10 V		2§	5	mA

†All typical values, except for r_N and $I_{REF(D,O)}$, are at V_{SS} = 20 V, V_{REF} = 7 V, T_A = 25°C.
§Typical value of $I_{REF(D,O)}$ is with V_{SS} open, V_{REF} = 7 V, T_A = 25°C.
NOTE 4: Duty cycle in the write mode must be low enough to maintain the average dissipation within the continuous dissipation rated limit when averaged over short intervals.

switching characteristics, V_{SS} = 20 V, V_{REF} = 7 V, $C_{I/O}$ = 40 pF, C_L = 15 pF, R_L = 400 Ω, T_A = 25°C

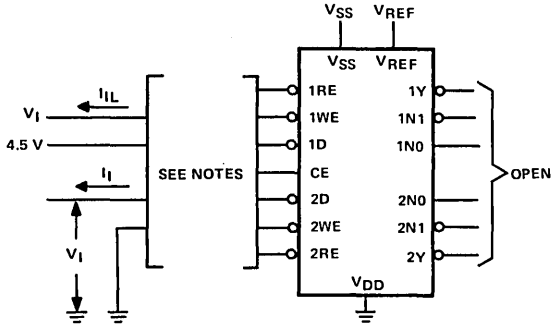
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	WE	N	10			52	80	ns
t_{PHL}						31	47	
t_{PLH}	D	N	11			44	70	ns
t_{PHL}						30	45	
t_{PLH}	CE	N	12			60	95	ns
t_{PHL}						43	65	
t_{PLH}	RE	Y	13	I_{ID} = −100 μA		13	20	ns
t_{PHL}						19	28	
t_{PLH}	CE	Y	14	I_{ID} = −100 μA		25	38	ns
t_{PHL}						32	48	
t_{PLH}	N0	Y	15			25	40	ns
t_{PHL}						25	40	
t_{PLH}	N1	Y	16			25	40	ns
t_{PHL}						25	40	
t_{PLH}	WE	Y	17	I_{N1} = 100 μA		135	190	ns
t_{PHL}				I_{N0} = 100 μA		125	190	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

5

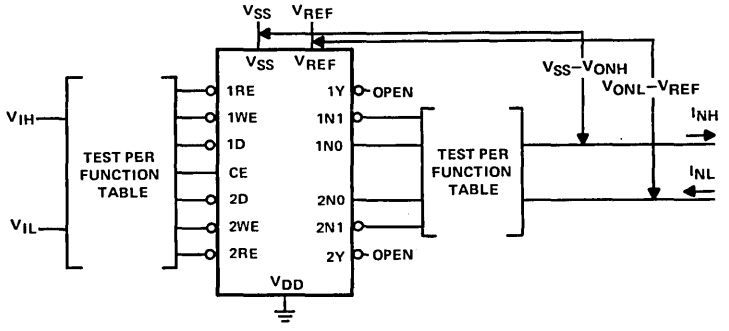
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



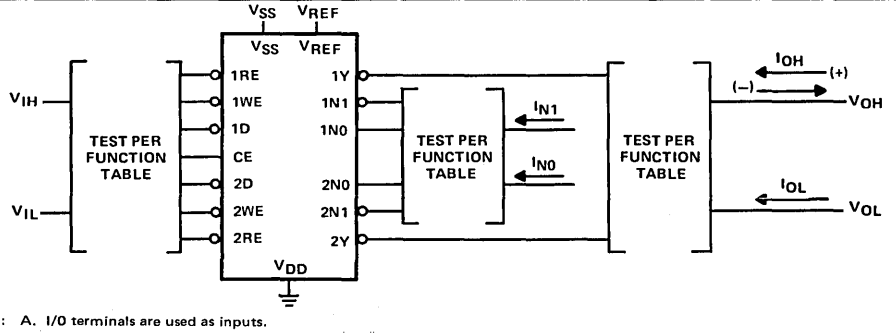
NOTES: A. WE, RE, and D inputs are tested for two conditions of CE: CE at 4.5 V and CE at 0 V.
B. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 µs, duty cycle ⩽ 20%.

FIGURE 2–V_I and I_{IL}



NOTE A: When WE is low, these parameters must be measured using pulse techniques. t_w = 200 µs, duty cycle ⩽ 20%.

FIGURE 3–V_{IH}, V_{IL}, V_{ONH}, and V_{ONL}



NOTES: A. I/O terminals are used as inputs.
B. For testing purposes: $I_{IDH} = I_{N1}$ with $I_{N0} = 0$. (Current into I_{N1} terminal only.)
$-I_{IDL} = I_{N0}$ with $I_{N1} = 0$. (Current into I_{N0} terminal only.)
C. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 µs, duty cycle ⩽ 20%.

FIGURE 4–V_{IH}, V_{IL}, I_{IDH}, I_{IDL}, V_{OH}, V_{OL}, I_{OH}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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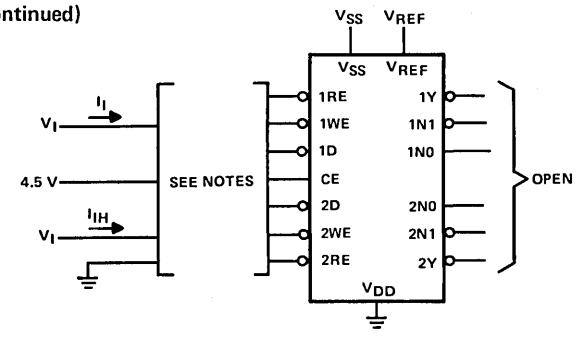
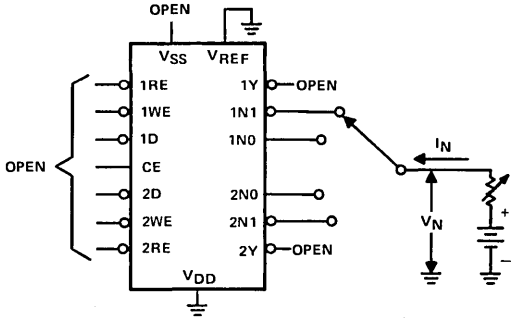
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTES: A. WE, RE, and D inputs are tested for two conditions of CE: CE at 4.5 V and CE at 0 V.
B. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 20%.

FIGURE 5–I_I and I_{IH}



NOTE A: Resistance r_N is calculated using the equation: $r_N = \frac{V_N}{I_N}$.

FIGURE 6–r_N

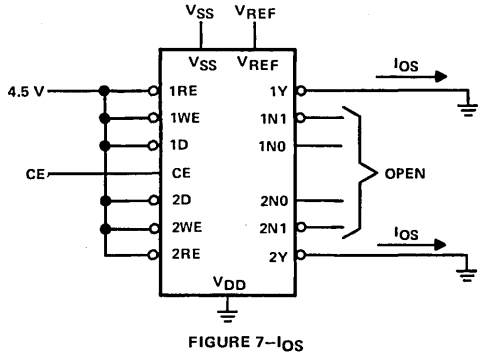


FIGURE 7–I_{OS}

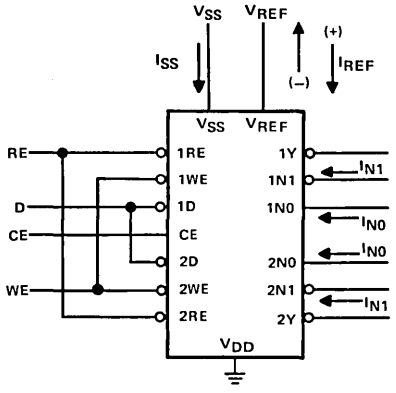
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

TEST TABLE

MODE	CE	WE	RE	D
Disabled	0 V	0 V	0 V	4.5 V
Standby	4.5 V	4.5 V	4.5 V	4.5 V
Read-1	4.5 V	4.5 V	0 V	4.5 V
Read-0	4.5 V	4.5 V	0 V	0 V
Write	4.5 V	0 V	4.5 V	4.5 V
Disabled, V_{SS}-open	0 V	0 V	0 V	0 V

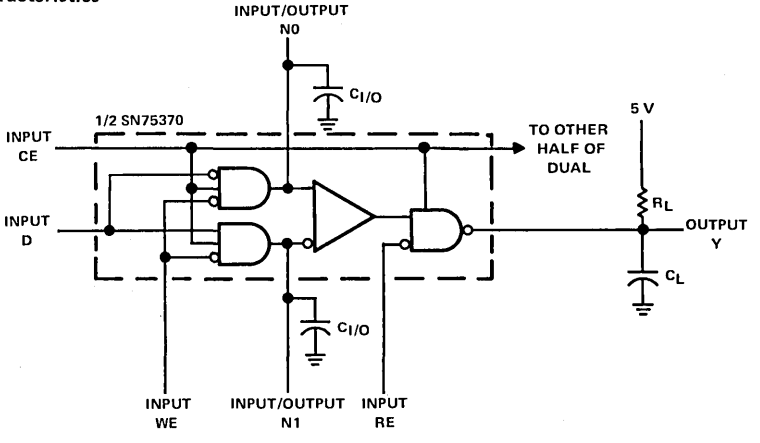


NOTES: A. I_{SS} and I_{REF} are measured simultaneously with both halves of circuit biased identically.
B. All node terminals are open except as noted otherwise in test conditions.
C. When WE is low, these parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 20%.
D. Dissipation is calculated using the equation $P = V_{SS} \cdot I_{SS} + V_{REF} \cdot I_{REF}$.

FIGURE 8–I_{SS}, I_{REF}, and P

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



NOTES: A. Refer to this figure and notes for all switching tests.
B. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
C. C_L and $C_{I/O}$ include probe and jig capacitance.
D. Input conditions for channel not under test: WE and RE at 2.4 V, D at 0.4 V.
E. N terminals are connected only to $C_{I/O}$ unless otherwise noted.

FIGURE 9–SWITCHING TEST CIRCUIT

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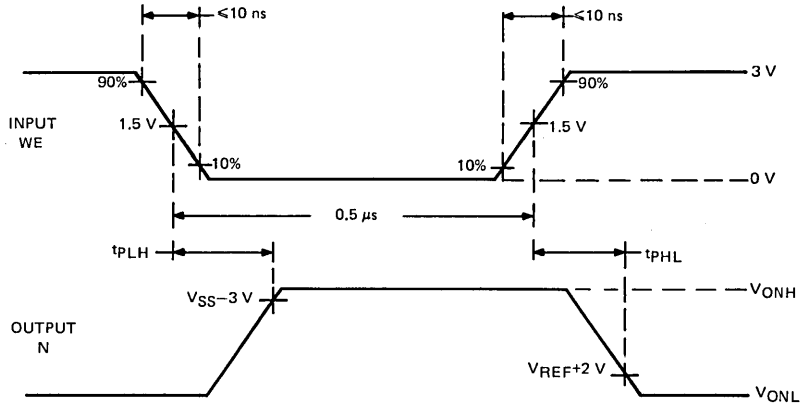
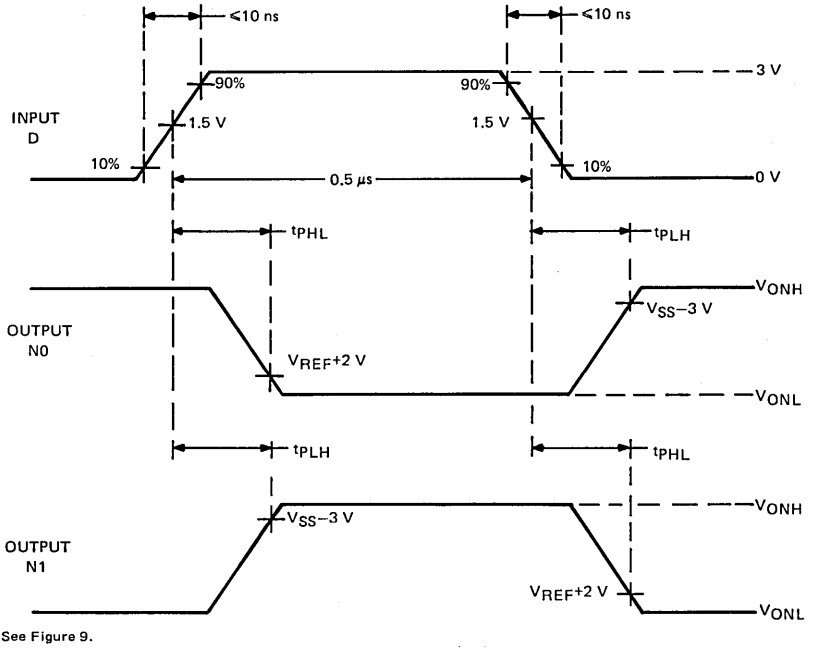
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Output N0 is tested with D at 0.4 V and output N1 is tested with D at 2.4 V.
C. Input conditions for other inputs of channel under test: CE at 2.4 V, RE at 2.4 V.

FIGURE 10–VOLTAGE WAVEFORMS, WE TO N

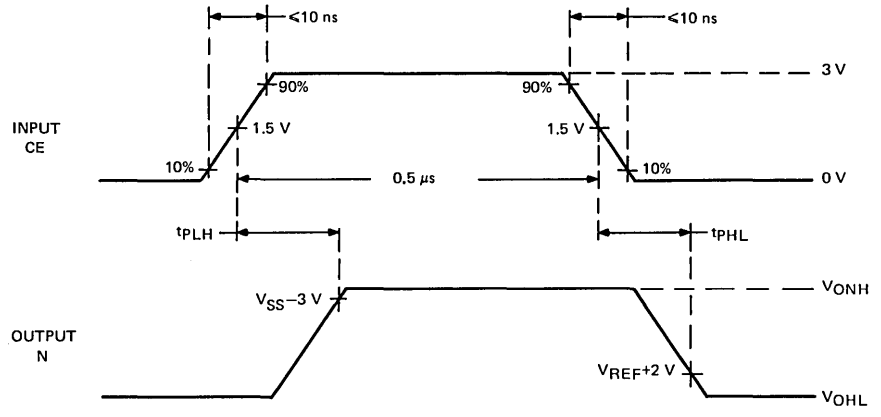


NOTES: A. See Figure 9.
B. Input conditions for other inputs of channel under test: CE at 2.4 V, WE at 0.4 V, RE at 2.4 V.

FIGURE 11–VOLTAGE WAVEFORMS, D TO N

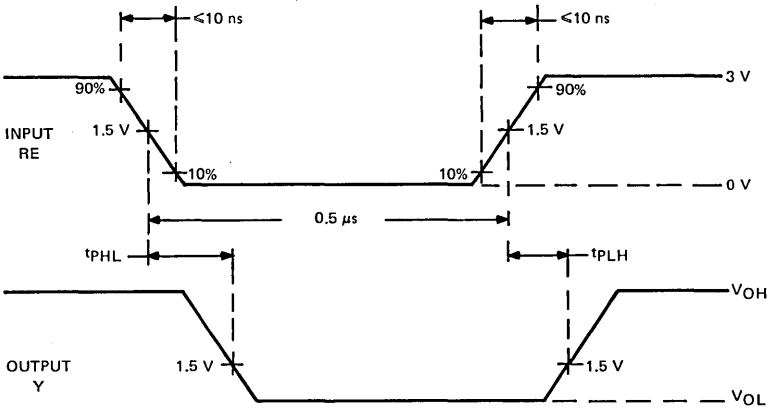
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Output N0 is tested with D at 0.4 V and output N1 is tested with D at 2.4 V.
C. Input conditions for all other inputs of channel under test: WE at 0.4 V, RE at 2.4 V.

FIGURE 12–VOLTAGE WAVEFORMS, CE TO N

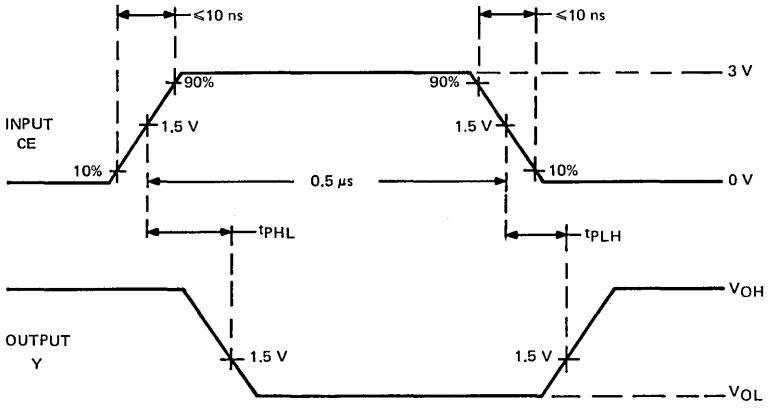


NOTES: A. See Figure 9.
B. Input conditions for all other inputs of channel under test: CE at 2.4 V, WE at 2.4 V, D at 0.4 V.
C. I_{NO} = 100 μA.

FIGURE 13–VOLTAGE WAVEFORMS, RE TO Y

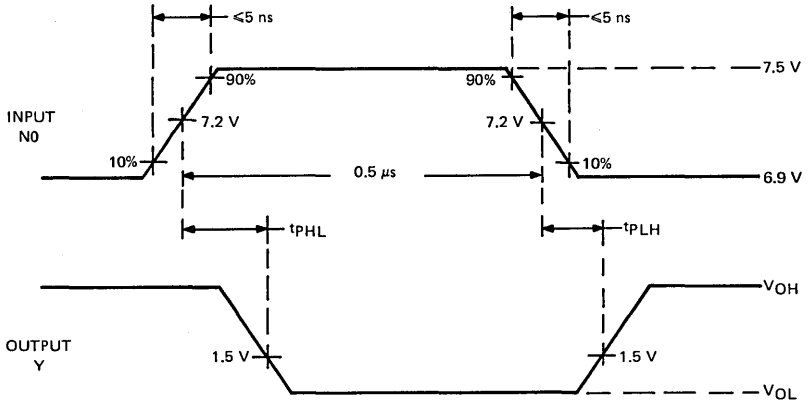
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Input conditons for all other inputs of channel under test: WE at 2.4 V, RE at 0.4 V, D at 0.4 V.
C. I_{NO} = 100 μA.

FIGURE 14–VOLTAGE WAVEFORMS, CE TO Y

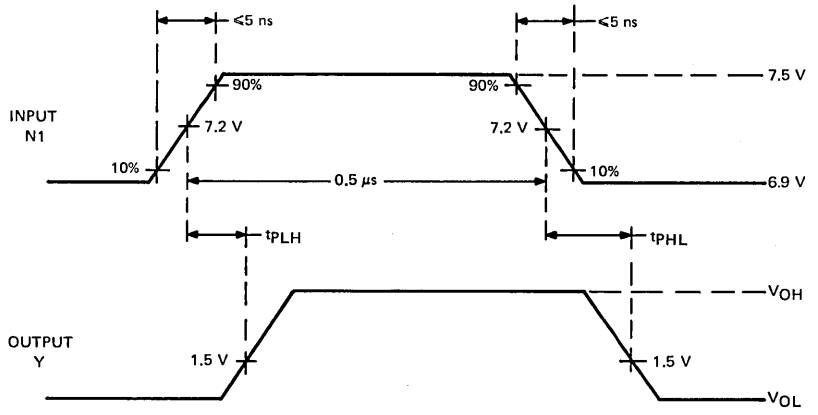


NOTES: A. See Figure 9.
B. Input conditions for all other inputs of channel under test: CE at 2.4 V, WE at 2.4 V, RE at 0.4 V, D at 2.4 V.

FIGURE 15–VOLTAGE WAVEFORMS, N0 TO Y

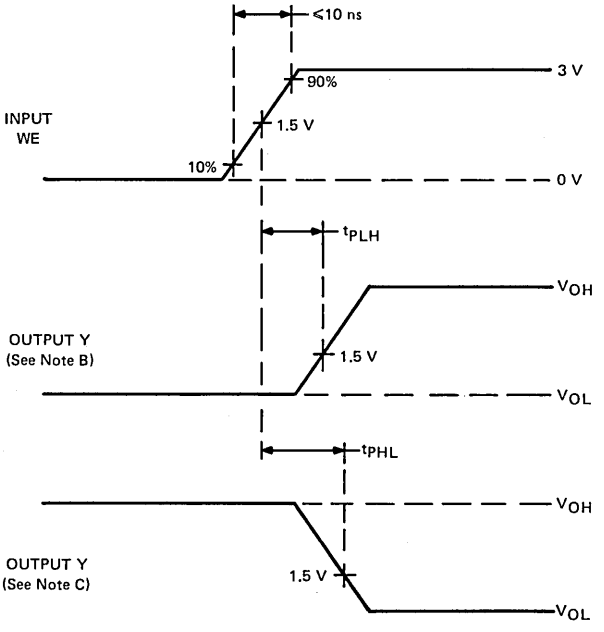
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: A. See Figure 9.
B. Input conditions for other inputs of channel under test: CE at 2.4 V, WE at 2.4 V, RE at 0.4 V, D at 2.4 V.

FIGURE 16–VOLTAGE WAVEFORMS, N1 TO Y



NOTES: A. See Figure 9.
B. t_{PLH} is tested with I_{N1} = 100 μA, D at 0.4 V, CE at 2.4 V, RE at 0.4 V.
C. t_{PHL} is tested with I_{N0} = 100 μA, D at 2.4 V, CE at 2.4 V, RE at 0.4 V.
D. Duty cycle of input WE pulse generator is 50%.

FIGURE 17–VOLTAGE WAVEFORMS, WE TO Y

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TYPICAL CHARACTERISTICS

LOW-LEVEL NODE VOLTAGE
(READ MODE)
vs
NODE CURRENT

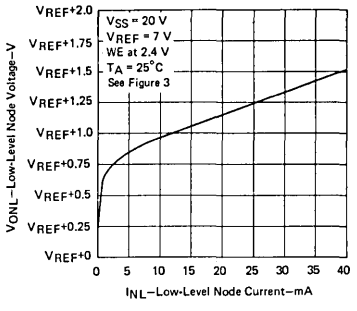

FIGURE 18

LOW-LEVEL NODE VOLTAGE
(READ MODE)
vs
NODE CURRENT

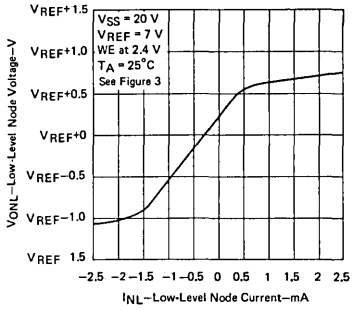

FIGURE 19

DIFFERENTIAL INPUT VOLTAGE
(READ MODE)
vs
DIFFERENTIAL INPUT CURRENT

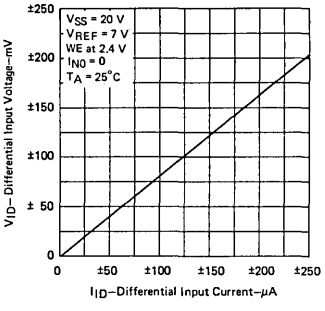

FIGURE 20

OUTPUT VOLTAGE AT Y
(READ MODE)
vs
DIFFERENTIAL INPUT CURRENT

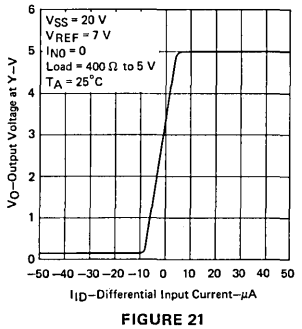

FIGURE 21

SUPPLY CURRENT FROM VSS
(DISABLED MODE)
vs
SUPPLY VOLTAGE VREF

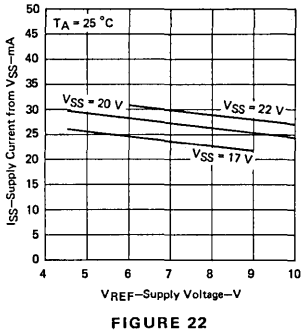

FIGURE 22

SUPPLY CURRENT FROM VREF
(DISABLED MODE)
vs
SUPPLY VOLTAGE VREF

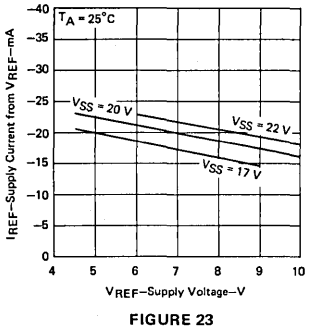

FIGURE 23

TYPICAL CHARACTERISTICS

SUPPLY CURRENT FROM V_{SS}
(READ-1, READ-0, OR STANDBY MODE)
vs
SUPPLY VOLTAGE V_{REF}

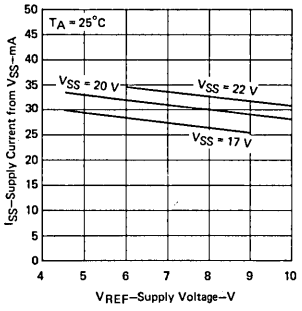

FIGURE 24

SUPPLY CURRENT FROM V_{REF}
(READ-1, READ-0, OR STANDBY MODE)
vs
SUPPLY VOLTAGE V_{REF}

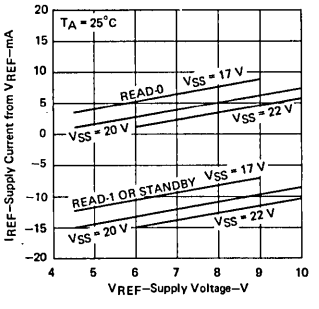

FIGURE 25

SUPPLY CURRENT FROM V_{SS}
(WRITE MODE)
vs
SUPPLY VOLTAGE V_{REF}

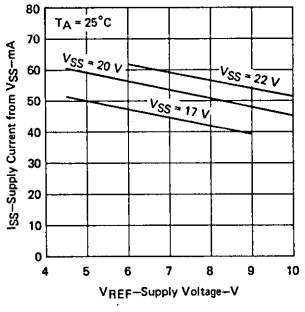

FIGURE 26

SUPPLY CURRENT FROM V_{REF}
(WRITE MODE)
vs
SUPPLY VOLTAGE V_{REF}

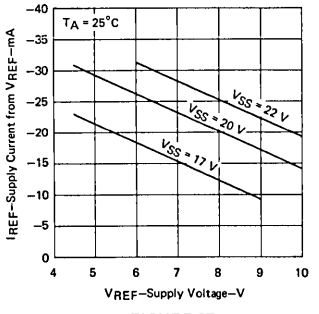

FIGURE 27

SUPPLY CURRENT FROM V_{SS}
vs
FREE-AIR TEMPERATURE

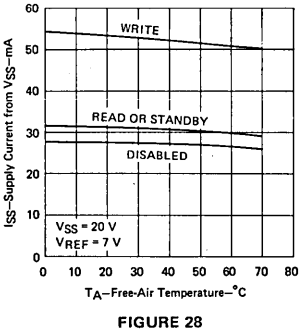

FIGURE 28

SUPPLY VOLTAGE FROM V_{REF}
vs
FREE-AIR TEMPERATURE

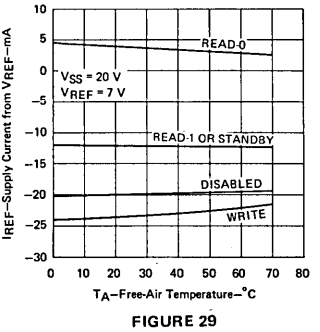

FIGURE 29

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TYPICAL APPLICATION DATA

Figure 30 illustrates a typical MOS memory system using SN75370, TMS4062, and SN75361A. All inputs and outputs from this system are TTL-compatible. The SN75361A is a high-speed monolithic dual TTL-to-MOS driver.The address SN75361As select a cell in each of the 72 TMS4062s. In Figure 30 the I/O terminals of the eight TMS4062 RAMs in each row have been connected to the node terminals of the associated SN75370 channel. Time multiplexing of the column of RAMs (M) by the SN75361A Clock/CS and Reset drivers is then used to write into or read from the cells that have been selected by the address SN75361As.

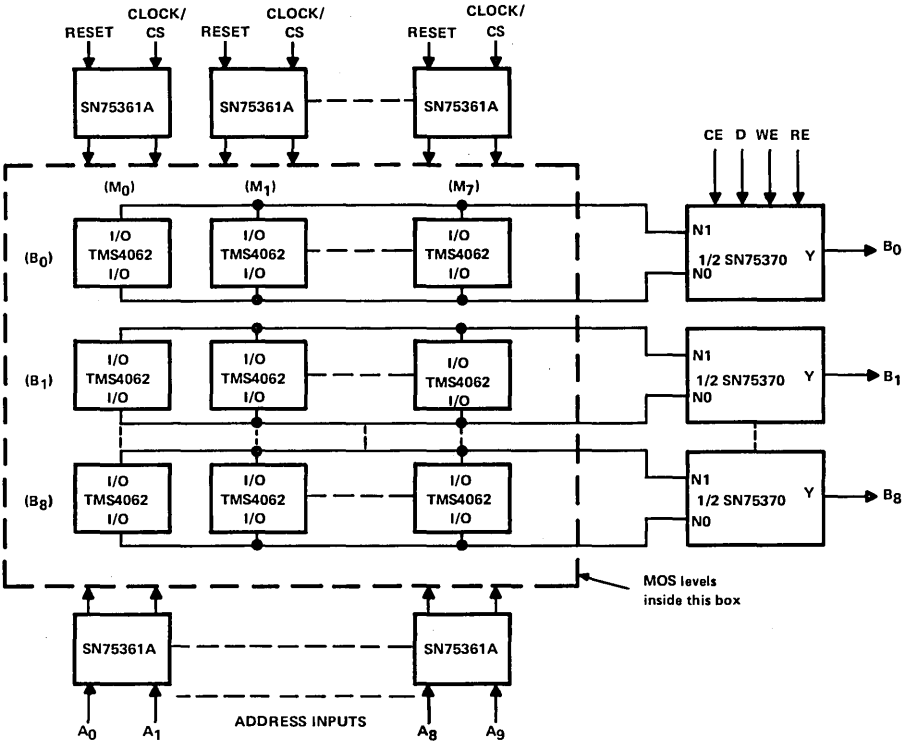


FIGURE 30–BLOCK DIAGRAM OF TOTALLY TTL-COMPATIBLE 8K X 9-BIT MOS-MEMORY SYSTEM USING SN75370, TMS4062, AND SN75361A

TYPICAL APPLICATION DATA

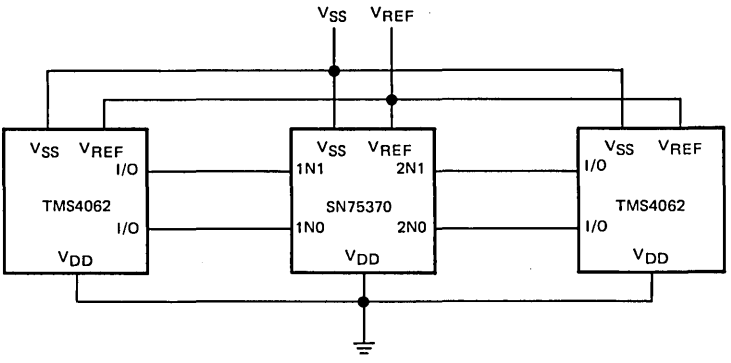
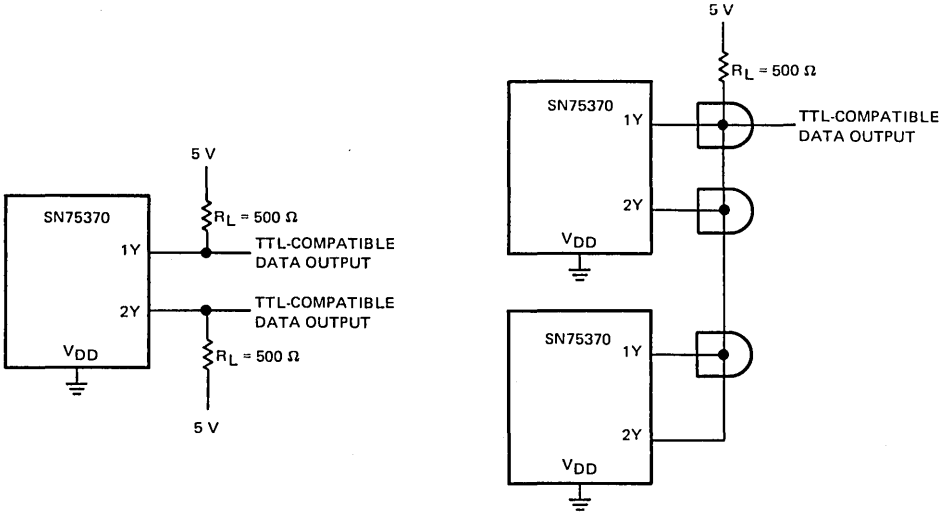


FIGURE 31–INTERCONNECTION OF SN75370 WITH TMS4062 MOS RAM



NOTE A: Pull-up resistor R_L is not necessary, but may be desirable for faster low-to-high-level transition of data output and increased TTL high-level noise margin. The value of R_L is determined by the user based upon the constraints of the system.

FIGURE 32–METHODS OF USING DATA OUTPUTS OF SN75370

TYPICAL APPLICATION DATA

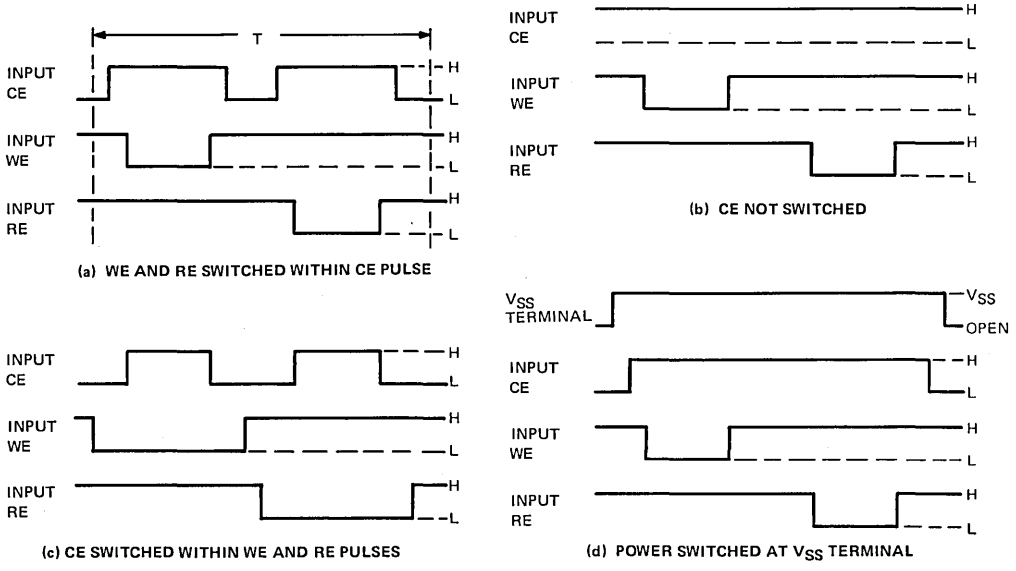


FIGURE 33–TYPICAL OPERATING INPUT VOLTAGE WAVEFORMS FOR SN75370

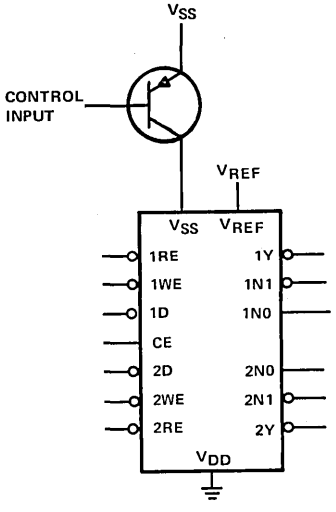


FIGURE 34–SWITCHING POWER TO V_{SS} TERMINAL OF SN75370 USING P-N-P TRANSISTOR

5

THERMAL INFORMATION

Power generated by the device depends on the mode of operation and the supply voltages used. Under some conditions, the SN75370 may generate sufficient instantaneous power to exceed, on average, the rated continuous power dissipation capability of the package. Appropriate duty-cycling of high-power conditions must be used to keep average power generated by the SN75370 within ratings.

Figure 33 shows typical methods to lower average power dissipation by pulsing the CE, WE, and RE inputs. Highest power occurs when both channels are in the write mode. Usually the write mode must be duty-cycled to reduce average power. Figure 33 (d) and Figure 34 demonstrate the use of a discrete P-N-P transistor to switch power to the V_{SS} terminal of the SN75370 to minimize average power. In addition, forced-air cooling or heat-sinking techniques may be used to increase the dissipation capability of the SN75370.

The following example illustrates a method to calculate average d-c supply power for the SN75370. The typical average power over a period T will be calculated using Figure 33(a). Assume both channels are operating identically, except in read mode when one channel is reading a 1 and the other channel is reading a 0. Let $V_{SS} = 20$ V, $V_{REF} = 7$ V and $T_A = 25°C$. The subscripts W, R, SB, and D refer to write, read, standby, and disabled, respectively.

$$P_{AV} = \frac{t_W P_W + t_R P_R + t_{SB} P_{SB} + t_D P_D}{T}$$

$$T = t_W + t_R + t_{SB} + t_D$$

Typical power for each mode is stated in the electrical characteristics table. This example uses duty cycles (t/T) estimated from Figure 33(a). These values are then substituted in order:

$$P_{AV} = (0.25)\ (910) + (0.25)\ \left(\frac{560+640}{2}\right) + (0.2)\ (560) + (0.3)\ (410)$$

$$P_{AV} = 613 \text{ mW}$$

5

FUTURE PRODUCT
TO BE ANNOUNCED

TYPE SN75375
QUADRUPLE TTL-TO-MOS DRIVER

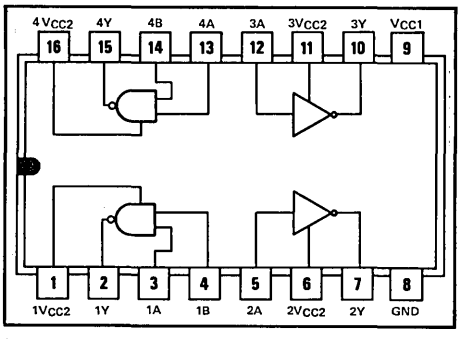
APRIL 1977

- Individual V_{CC2} Supplies For Each Driver
- V_{CC2} Variable Over a Wide Range . . . 5 V to 24 V
- Two NAND Drivers and Two Inverting Drivers Per Package
- High Speed . . . Typical Propagation Delay Time = 31 ns

applications

- TTL-to-MOS Driver
- Data Line Transceiver
- Display Digit and Segment Driver
- TTL Clock Generator
- MOS Clock Generator

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75375 is a quadruple TTL-to-MOS driver that features individual V_{CC2} supplies for each of the drivers. The individual V_{CC2} pins allow for individual adjustment of V_{OH} levels to match various load conditions. The circuit performance is similar to that of the SN75365.

The SN75375 will be characterized for operation from 0°C to 70°C.

supply voltages: V_{CC1} = 5 V
V_{CC2} variable from 5 V to 24 V

5

Memory Drivers

MEMORY DRIVERS

- TTL-COMPATIBLE INPUTS
- CORE MEMORY APPLICATIONS

DESCRIPTION	MAXIMUM OUTPUT CURRENT	t_{PD}¶ TYPICAL	POWER SUPPLIES	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	ADDITIONAL FEATURES	PAGE NO.
				−55°C TO 125°C	0°C TO 70°C			
DUAL SINK/SOURCE MEMORY DRIVERS	400 mA	75 ns	V_{CC} = 14 V		SN75324	J,N	• Internal decoding and timing circuitry • Output short-circuit protection • Source output terminals swing between 14 V and ground	191
	600 mA	35 ns	V_{CC1} = 5 V, V_{CC2} variable to 24 V	SN55325	SN75325	J J,N	• Also used for high-voltage, high-current driver applications • Output transient voltage protection • Source output terminals swing between V_{CC2} and ground	198
QUADRUPLE MEMORY DRIVERS	600 mA	35 ns	V_{CC1} = 5 V, V_{CC2} variable to 24 V	SN55327	SN75327	J J,N	• Also used for high speed magnetic memory applications • Output transient voltage protection • Output capable of swinging between V_{CC2} and ground	213
		40 ns	V_{CC1} = 5 V, V_{CC2} variable to 24 V		SN75328	J,N	• Also used for bubble memory applications • Output transient voltage protection • Output capable of swinging between V_{CC2} and ground • Uncommitted collectors and emitters • Common external base drive control (SN75238) • Individual external base drive control (SN75330)	219
					SN75330			
QUADRUPLE SINK MEMORY DRIVER	600 mA	30 ns	V_{CC} = 5 V	SN55326	SN75326	J J,N	• Also used for high-voltage, high-current driver applications • Output transient voltage protection • 24 V output capability	213
EIGHT-CHANNEL MEMORY DRIVER	350 mA	85 ns	V_{CC1} = 5 V, V_{CC2} = 12 V	SN55329		RA	• Bipolar output currents controlled to within 5% • 3-state outputs • Internal power control — does not require power supply sequencing • Contains 3-line to 8-line decoder • 24-pin ceramic flat package • Temperature range: −55°C to 110°C	See Note 1

¶ t_{PD} = Propagation Delay Time

NOTE 1: For additional information, contact your nearest TI field sales office.

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TYPE SN75324
MEMORY CORE DRIVER WITH DECODE INPUTS

BULLETIN NO. DL-S 7711169, APRIL 1969—REVISED APRIL 1977

SERIES 75 MEMORY DRIVER

PERFORMANCE

- Fast Switching Times
- 400-mA Output Capability
- Internal Decoding and Timing Circuitry
- Dual Sink/Source Outputs
- Output Short-Circuit Protection

EASE OF DESIGN

- TTL or DTL Compatibility
- Eliminates Transformer Coupling
- Reduces Drive-Line Lengths
- Increases Reliability
- Minimizes External Components

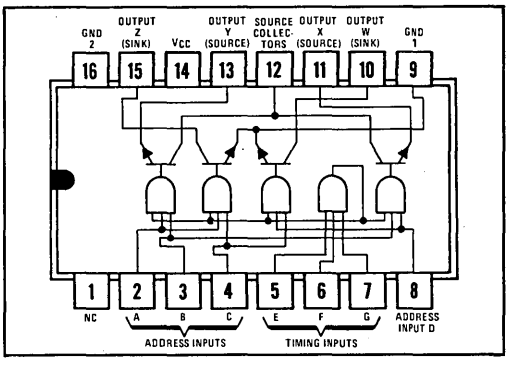
description

The SN75324 is a monolithic memory driver with decode inputs designed for use with magnetic memories. The device contains two 400-milliampere (source/sink) switch pairs, with decoding capability from four address lines. Two address inputs (B and C) are used for mode selection, i.e., source or sink. The other two address inputs (A and D) are used for switch-pair selection, i.e., output switch-pair Y/Z or W/X respectively.

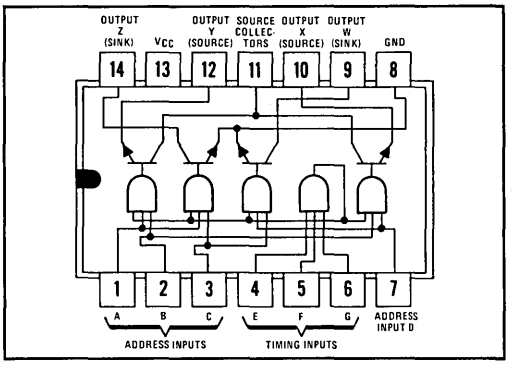
The sink circuit is composed of an inverting switch with a transistor-transistor-logic (TTL) input. The source circuit is an emitter-follower driven from a TTL input stage.

The SN75324 is characterized for operation from 0°C to 70°C.

J CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



N PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection
GND 1 and GND 2 are to be connected together.

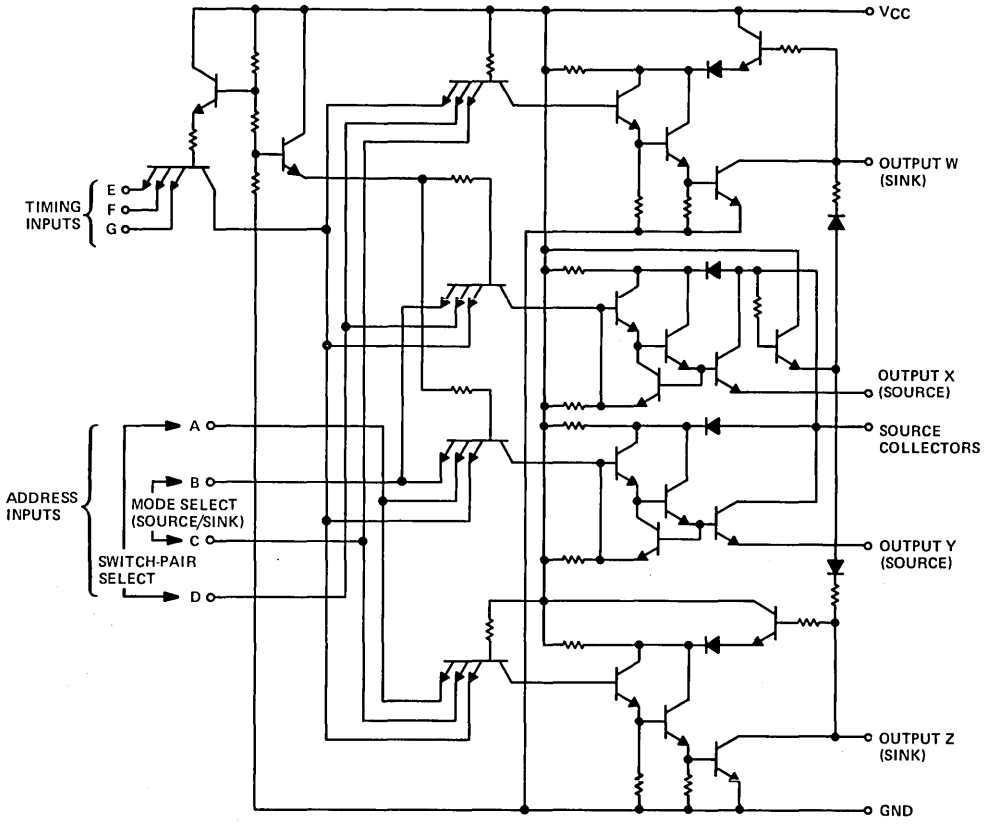
FUNCTION TABLE

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
L	L	H	H	H	H	H	ON	OFF	OFF	OFF
L	H	L	H	H	H	H	OFF	ON	OFF	OFF
H	H	L	L	H	H	H	OFF	OFF	ON	OFF
H	L	H	L	H	H	H	OFF	OFF	OFF	ON
X	X	X	X	L	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	L	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	L	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at one time: When all timing inputs are high, two of the address inputs must be low.

schematic



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 17 V
Input voltage (See Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Continuous total power dissipation at (or below) 25°C free-air temperature (See Note 3):
J package . . . . . 1375 mW
N package . . . . . 1150 mW
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75324 chips are alloy-mounted.

electrical characteristics (unless otherwise noted, V_{CC} = 14 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	1		3.5			V
V_{IL}	Low-level input voltage	1				0.8	V
I_{IH}	High-level input current, address inputs	1	V_I = 5 V			200	μA
I_{IH}	High-level input current, timing inputs	1	V_I = 5 V			100	μA
I_{IL}	Low-level input current, address inputs	1	V_I = 0 V			−6	mA
I_{IL}	Low-level input current, timing inputs	1	V_I = 0 V			−12	mA
$V_{(sat)}$	Sink saturation voltage	2	$I_{sink} \simeq$ 420 mA, R_L = 53 Ω		0.75	0.85	V
$V_{(sat)}$	Source saturation voltage	2	$I_{source} \simeq$ −420 mA, R_L = 47.5 Ω		0.75	0.85	V
I_{off}	Output off-state current	1	V_I = 0 V		125	200	μA
I_{CC}	Supply current, all sources and sinks off	3	V_I = 0 V		12.5	15	mA
I_{CC}	Supply current, either sink selected	4			30	42	mA
I_{CC}	Supply current, either source selected	4			25	35	mA

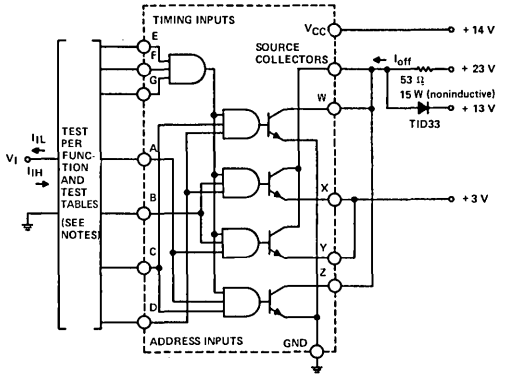
†All typical values are at T_A = 25°C

switching characteristics, V_{CC} = 14 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level source output	5	R_{L1} = 53 Ω, R_{L2} = 500 Ω, C_L = 20 pF			90	ns
t_{PHL}	Propagation delay time, high-to-low-level source output	5				50	ns
t_{PLH}	Propagation delay time, low-to-high-level sink output	6	R_L = 53 Ω, C_L = 20 pF			110	ns
t_{PHL}	Propagation delay time, high-to-low-level sink output	6				40	ns
t_s	Sink storage time	6				70	ns

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

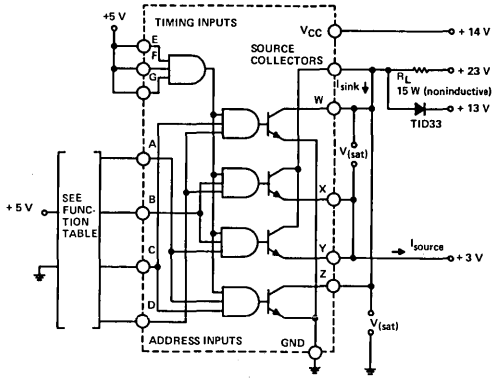


TEST TABLE FOR I_{IL}

APPLY 3.5 V	GROUND	TEST I_{IL}
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

NOTES: 1. Check V_{IH} and V_{IL} per Function Table.
2. Measure I_{IL} per Test Table.
3. When measuring I_{IH}, all other inputs are at ground. Each input is tested separately.

FIGURE 1–V_{IL}, V_{IH}, I_{IL}, I_{IH}, and I_{off}



NOTE: This parameter must be using pulse techniques. t_w = 500 ns, duty cycle ≤ 1%.

FIGURE 2 – $V_{(sat)}$

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

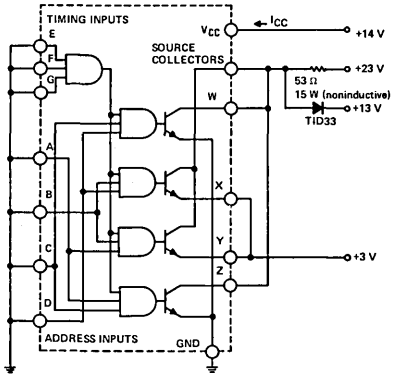
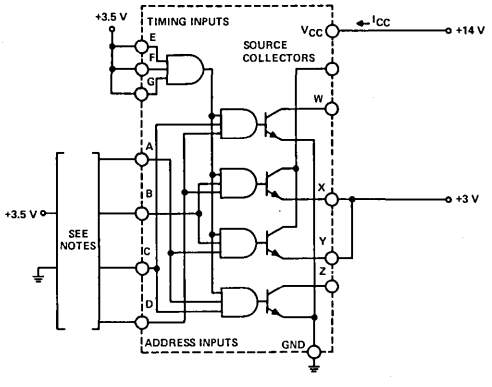


FIGURE 3 – I_{CC} (ALL OUTPUTS OFF)



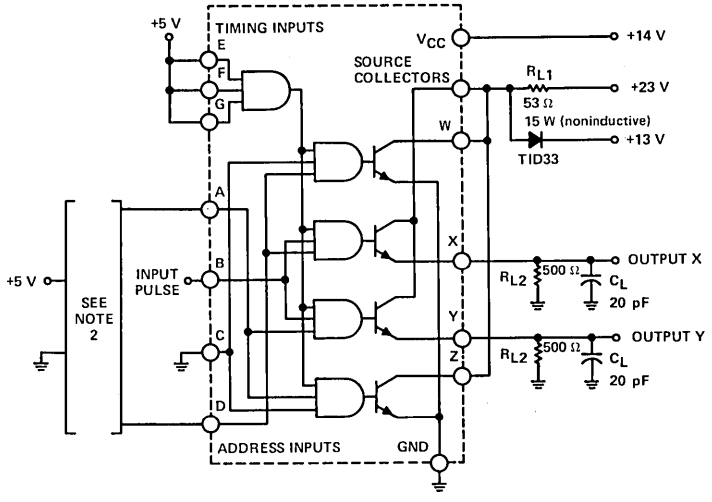
NOTES: 1. Ground A and B, apply 3.5 V to C and D, and measure I_{CC} (output W is on).
2. Ground B and D, apply 3.5 V to A and C, and measure I_{CC} (output Z is on).
3. Ground A and C, apply 3.5 V to B and D, and measure I_{CC} (output X is on).
4. Ground C and D, apply 3.5 V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4 – I_{CC} (ONE OUTPUT ON)

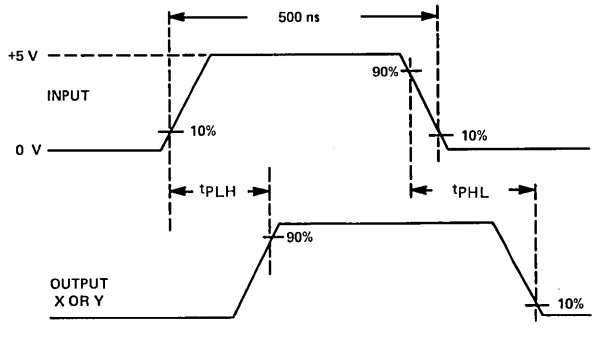
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, and $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output X, apply +5 V to input D, and ground A. When measuring delay times at output Y, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.
4. Unless otherwise noted all resistors are 0.5 W.

FIGURE 5 — SOURCE-OUTPUT SWITCHING TIMES

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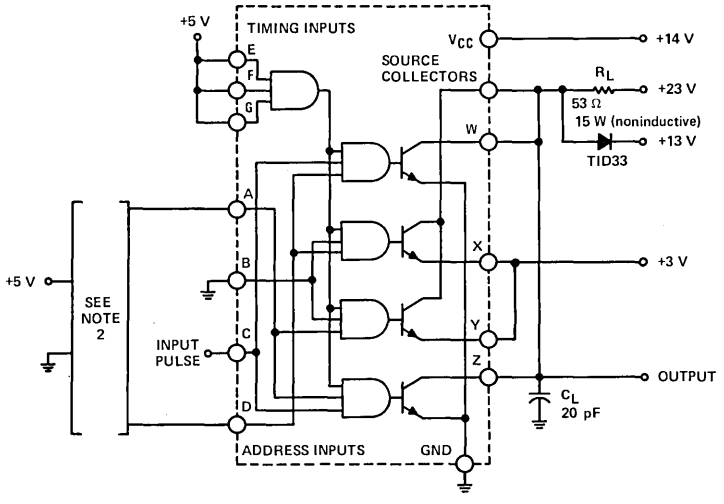
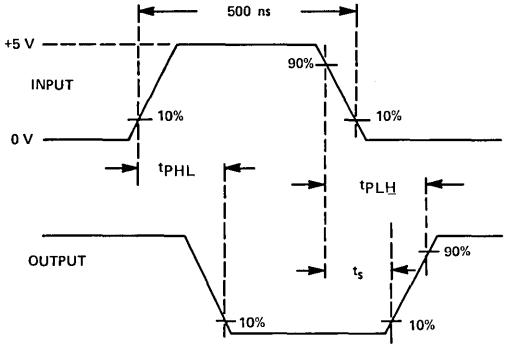
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leqslant 1\%$, $Z_{out} \approx 50\ \Omega$.
2. When measuring delay times at output W, apply +5 V to input D, and ground A. When measuring delay times at output Z, apply +5 V to input A, and ground D.
3. C_L includes probe and jig capacitance.

FIGURE 6 – SINK-OUTPUT SWITCHING TIMES

TYPES SN55325, SN75325 MEMORY CORE DRIVERS

BULLETIN NO. DL-S 7711437, MARCH 1971 – REVISED APRIL 1977

SERIES 55/75 MEMORY DRIVER
featuring

PERFORMANCE

- 600-mA Output Capability
- Fast Switching Times
- Output Transient-Voltage Protection
- Dual Sink and Dual Source Outputs
- Minimum Time Skew between Address and Output Current Rise
- 24-Volt Output Capability

EASE OF DESIGN

- Source Base Drive Externally Adjustable
- TTL or DTL Compatibility
- Input Clamping Diodes
- Transformer Coupling Eliminated
- Reliability Increased
- Drive-Line Lengths Reduced
- Use of External Components Minimized

description

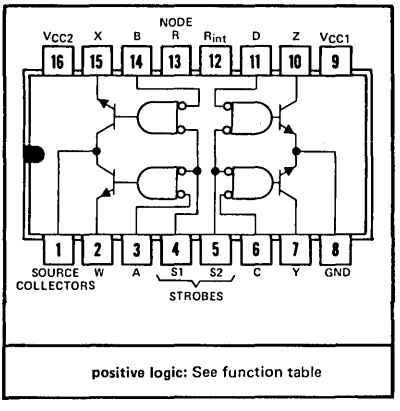
The SN55325 and SN75325 are monolithic integrated circuit memory drivers with logic inputs and are designed for use with magnetic memories.

The devices contain two 600-milliampere source switches and two 600-milliampere sink switches. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

When R_{int} and node R are connected together, the amount of base drive available for the source-1 or source-2 output transistor is set internally by a 575-ohm resistor. This method provides adequate base drive for source currents up to 375 mA with a V_{CC2} voltage of 15 volts or 600 mA with a V_{CC2} voltage of 24 volts.

When source currents greater than 375 mA are required, it is recommended that a resistor of the appropriate value be connected between V_{CC2} and node R and R_{int} must remain open. By using this method the source base current may usually be regulated within ±5%. An advantage of this method of setting the base drive is that the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher source currents for a given junction temperature.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: See function table

FUNCTION TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This arrangement provides protection from voltage surges associated with switching inductive loads.

The SN55325 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN75325 is characterized for operation from 0°C to 70°C.

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REVISED APRIL 1977

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55325	SN75325	UNIT
Supply voltage V_{CC1} (see Note 1)		7	7	V
Supply voltage V_{CC2} (see Note 1)		25	25	V
Input voltage (any address or strobe input)		5.5	5.5	V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J package	1375	1375	mW
	N package		1150	
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J package	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N package	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN55325 and SN75325 chips are alloy-mounted.

electrical characteristics over rated operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS		SN55325 MIN	SN55325 TYP‡	SN55325 MAX	SN75325 MIN	SN75325 TYP‡	SN75325 MAX	UNIT
V_{IH}	High-level input voltage		1 & 2			2			2			V
V_{IL}	Low-level input voltage		3 & 4					0.8			0.8	V
V_{IK}	Input clamp voltage		5	V_{CC1} = 4.5 V, I_I = −10 mA,	V_{CC2} = 24 V, T_A = 25°C		−1.3	−1.7		−1.3	−1.7	V
$I_{(off)}$	Source-collectors terminal off-state current		1	V_{CC1} = 4.5 V, V_{CC2} = 24 V	T_A = full range †			500			200	μA
					T_A = 25°C		3	150		3	200	
V_{OH}	High-level sink output voltage		2	V_{CC1} = 4.5 V, I_O = 0	V_{CC2} = 24 V,	19	23		19	23		V
$V_{(sat)}$	Saturation voltage	source outputs	3	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(source)} \approx$ −600 mA§, See Note 3	T_A = full range †			0.9			0.9	V
					T_A = 25°C		0.43	0.7		0.43	0.75	
		sink outputs	4	V_{CC1} = 4.5 V, V_{CC2} = 15 V, R_L = 24 Ω, $I_{(sink)} \approx$ 600 mA§, See Note 3	T_A = full range †			0.9			0.9	
					T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	address inputs	5	V_{CC1} = 5.5 V, V_I = 5.5 V	V_{CC2} = 24 V,			1			1	mA
		strobe inputs						2			2	
I_{IH}	High-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 2.4 V	V_{CC2} = 24 V,		3	40		3	40	μA
		strobe inputs					6	80		6	80	
I_{IL}	Low-level input current	address inputs	5	V_{CC1} = 5.5 V, V_I = 0.4 V	V_{CC2} = 24 V,		−1	−1.6		−1	−1.6	mA
		strobe inputs					−2	−3.2		−2	−3.2	
$I_{CC(off)}$	Supply current, all sources and sinks off	from V_{CC1}	6	V_{CC1} = 5.5 V, T_A = 25°C	V_{CC2} = 24 V,		14	22		14	22	mA
		from V_{CC2}					7.5	20		7.5	20	
I_{CC1}	Supply current from V_{CC1}, either sink on		7	V_{CC1} = 5.5 V, $I_{(sink)}$ = 50 mA,	V_{CC2} = 24 V, T_A = 25°C		55	70		55	70	mA
I_{CC2}	Supply current from V_{CC2}, either source on		8	V_{CC1} = 5.5 V, $I_{(source)}$ = −50 mA, See Note 3	V_{CC2} = 24 V, T_A = 25°C,		32	50		32	50	mA

†Full range for SN55325 is −55°C to 125°C and for SN75325 is 0°C to 70°C.

‡All typical values are at T_A = 25°C.

§Under these conditions, not more than one output is to be on at any one time.

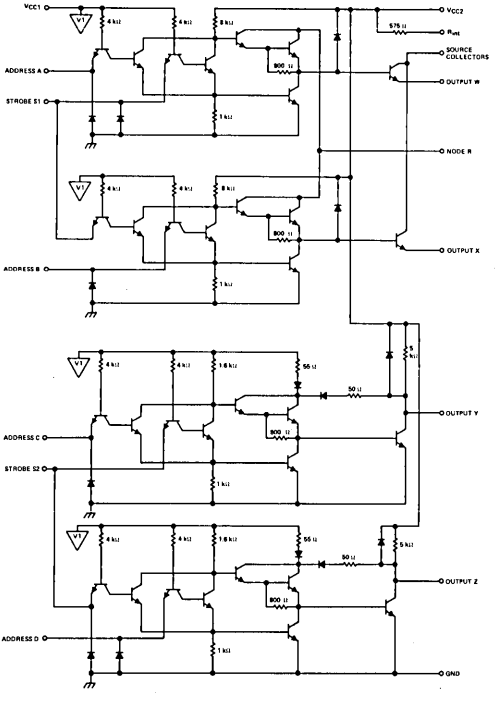
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Source collectors	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		35	50	ns
t_{PHL}					35	50	
t_{TLH}	Source outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ, C_L = 25 pF		55		ns
t_{THL}					7		
t_{PLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		7	15	ns
t_{THL}					9	20	
t_s	Sink outputs	9	V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF		15	30	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{TLH} = transition time, low-to-high-level output
t_{THL} = transition time, high-to-low-level output
t_s = storage time

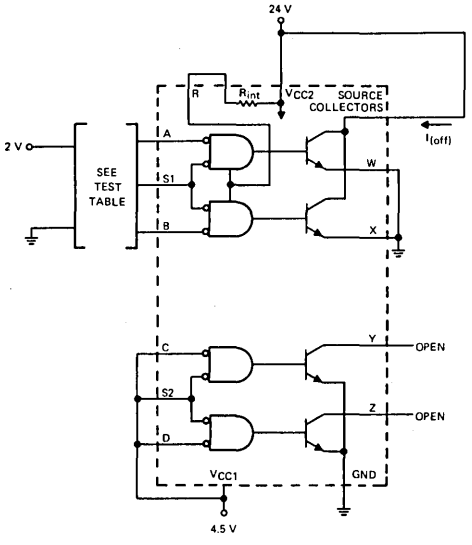
schematic



Component values shown are nominal.
V1 . . . V_{CC1} bus

PARAMETER MEASUREMENT INFORMATION

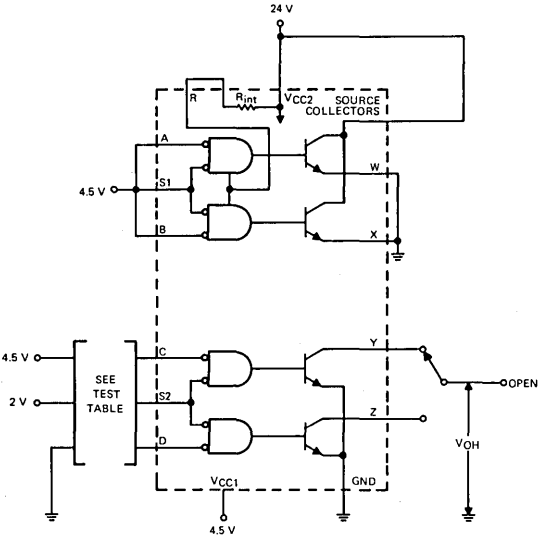
d-c test circuits†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

FIGURE 1–V_{IH} AND $I_{(off)}$



TEST TABLE

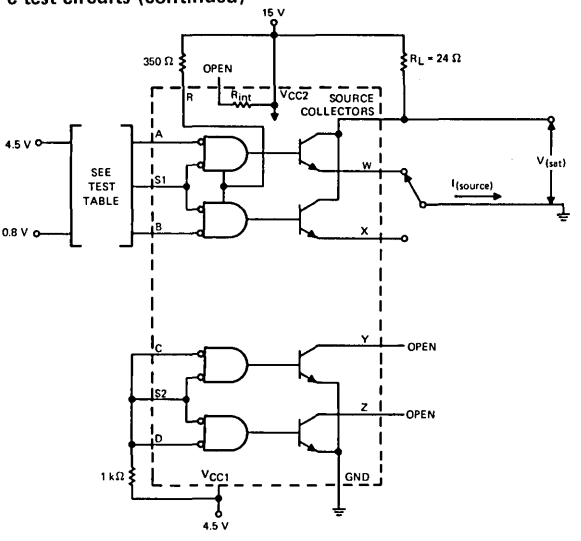
C	D	S2	Y	Z
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

FIGURE 2–V_{IH} AND V_{OH}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†

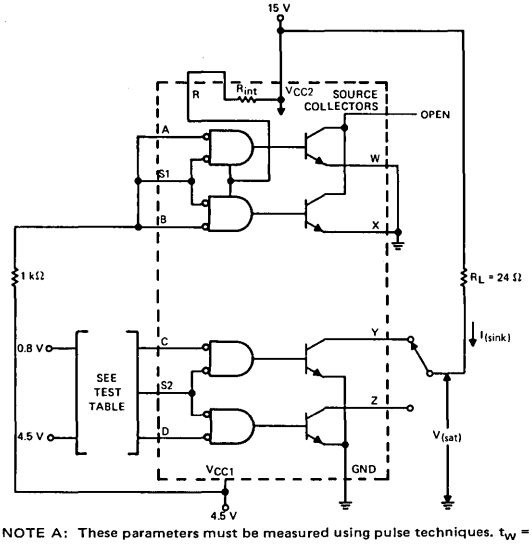


TEST TABLE

A	B	S1	W	X
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

FIGURE 3–V_{IL} AND SOURCE $V_{(sat)}$



TEST TABLE

C	D	S2	Y	Z
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

NOTE A: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ⩽ 2%.

FIGURE 4–V_{IL} AND SINK $V_{(sat)}$

†Arrows indicate actual direction of current flow.

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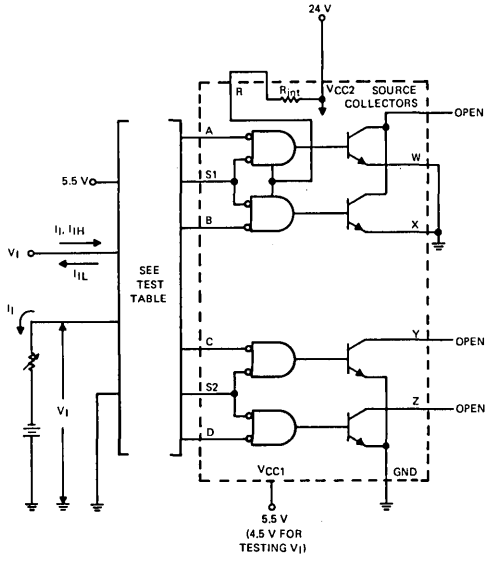
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)†



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5 V, MEASURE I_I / APPLY V_I = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4 V, MEASURE I_{IL} / APPLY I_I = −10 mA MEASURE V_I	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5–V_I, I_I, I_{IH}, AND I_{IL}

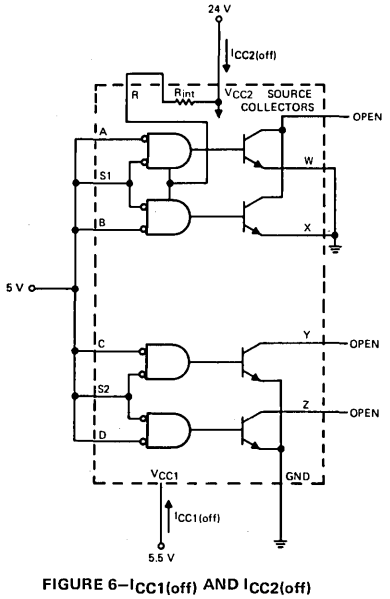
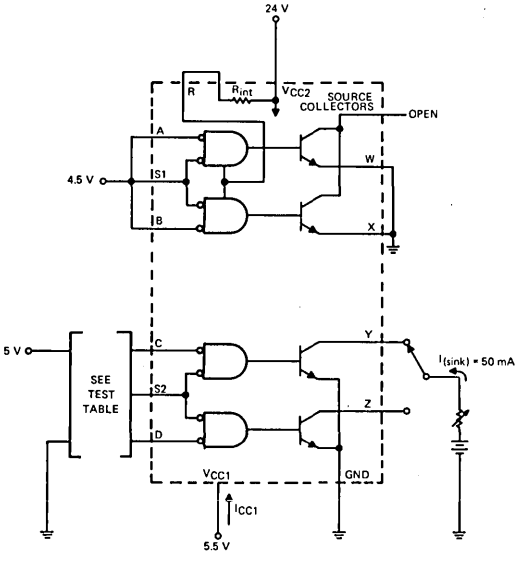


FIGURE 6–$I_{CC1(off)}$ AND $I_{CC2(off)}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

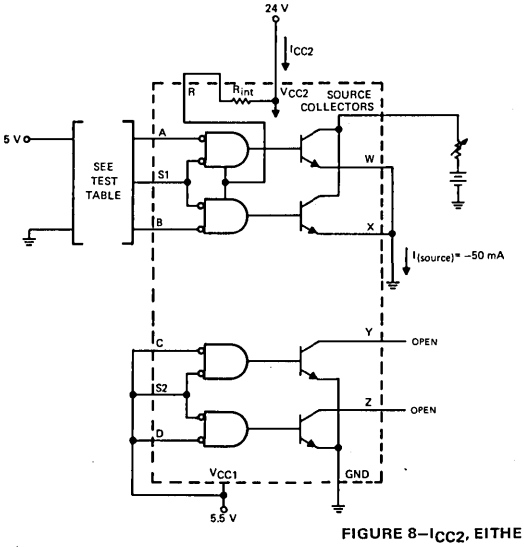
d-c test circuits (continued)†



TEST TABLE

C	D	S2	Y	Z
GND	5 V	GND	$I_{(sink)}$	OPEN
5 V	GND	GND	OPEN	$I_{(sink)}$

FIGURE 7–I_{CC1}, EITHER SINK ON



TEST TABLE

A	B	S1
GND	5 V	GND
5 V	GND	GND

FIGURE 8–I_{CC2}, EITHER SOURCE ON

†Arrows indicate actual direction of current flow.

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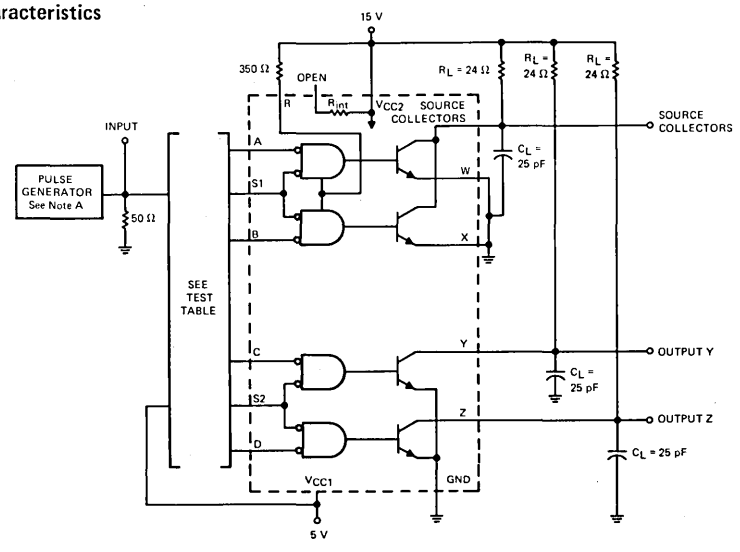
PARAMETER MEASUREMENT INFORMATION

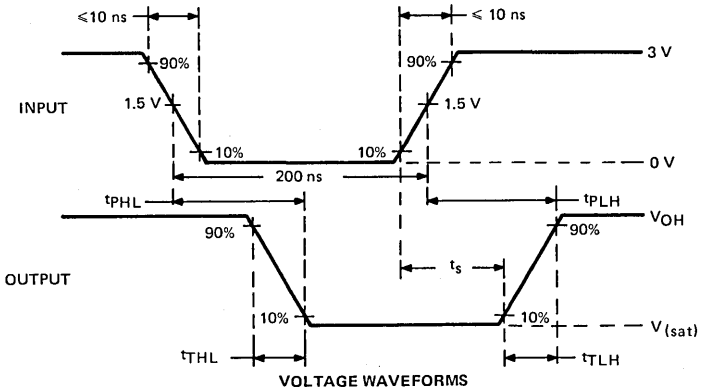
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1



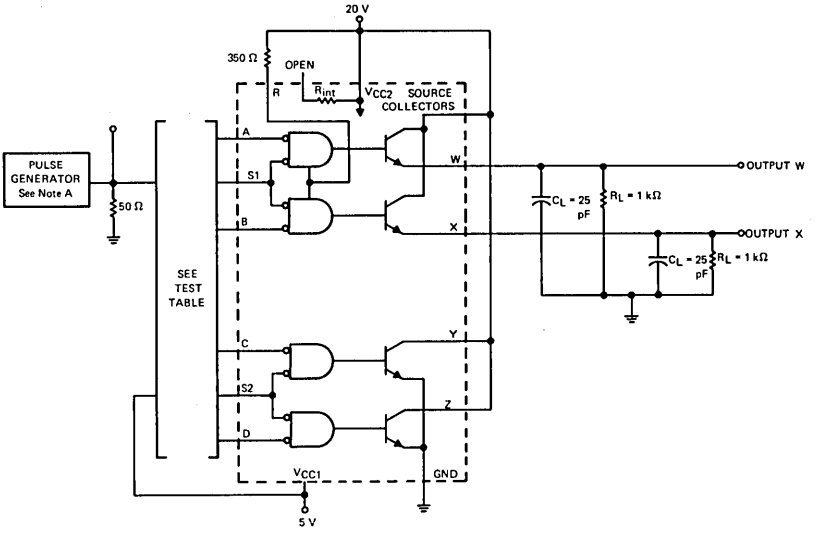
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 9–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

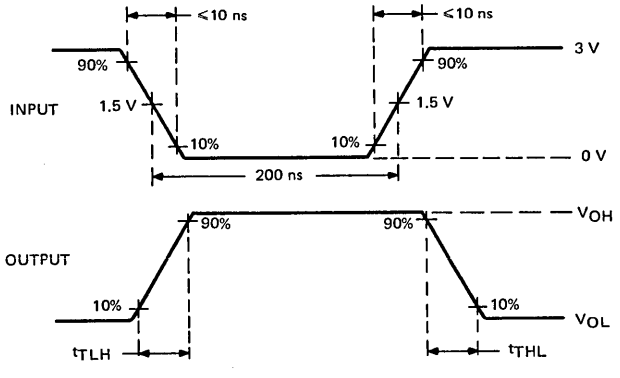
switching characteristics



TEST CIRCUIT

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 10–TRANSITION TIMES OF SOURCE OUTPUTS

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TYPICAL CHARACTERISTICS

OFF-STATE CURRENT INTO SOURCE COLLECTORS
vs
FREE-AIR TEMPERATURE

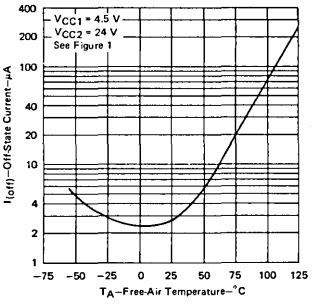


FIGURE 11

HIGH-LEVEL SINK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

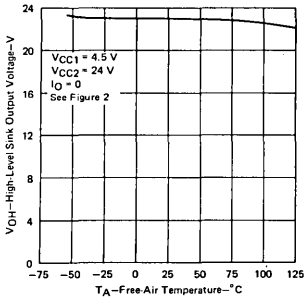


FIGURE 12

SOURCE OR SINK SATURATION VOLTAGE
vs
SOURCE CURRENT OR SINK CURRENT

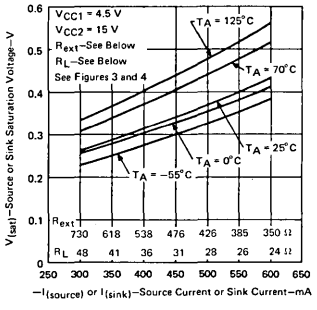


FIGURE 13

SOURCE OR SINK SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

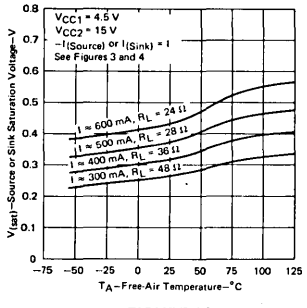


FIGURE 14

SUPPLY CURRENT, ALL SOURCES AND SINKS OFF
vs
FREE-AIR TEMPERATURE

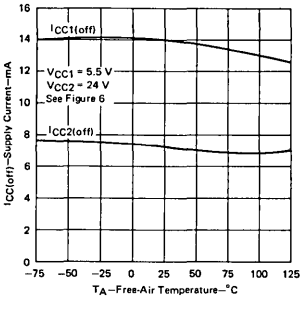
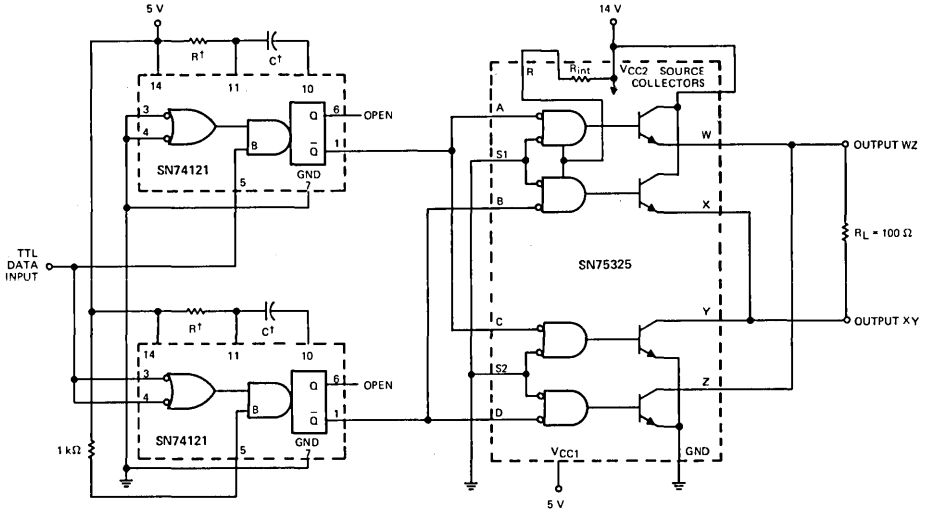


FIGURE 15

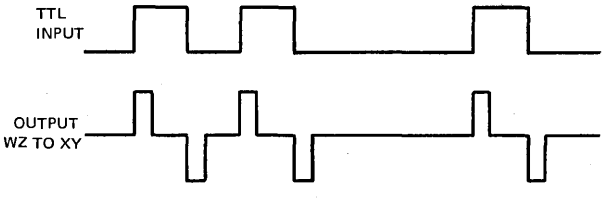
TYPICAL APPLICATION DATA

balanced bipolar logic-line driver

The circuit shown in Figure 16 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5-volt supply; however, the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a three-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several thousand feet in length or low-impedance coaxial lines.



TEST CIRCUIT



VOLTAGE WAVEFORMS

†R and C are adjusted to give the desired bipolar output pulse width.

FIGURE 16–BALANCED BIPOLAR LOGIC–LINE DRIVER

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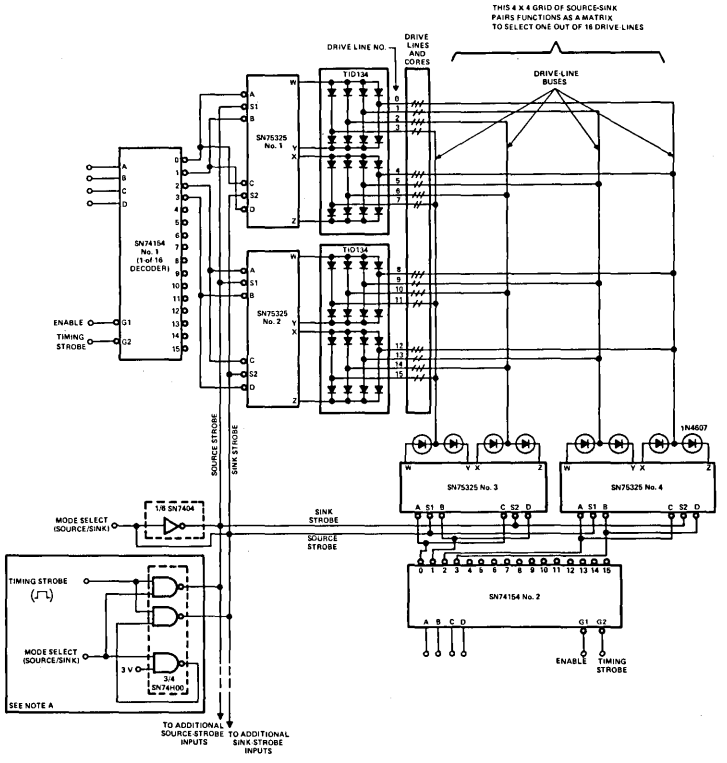
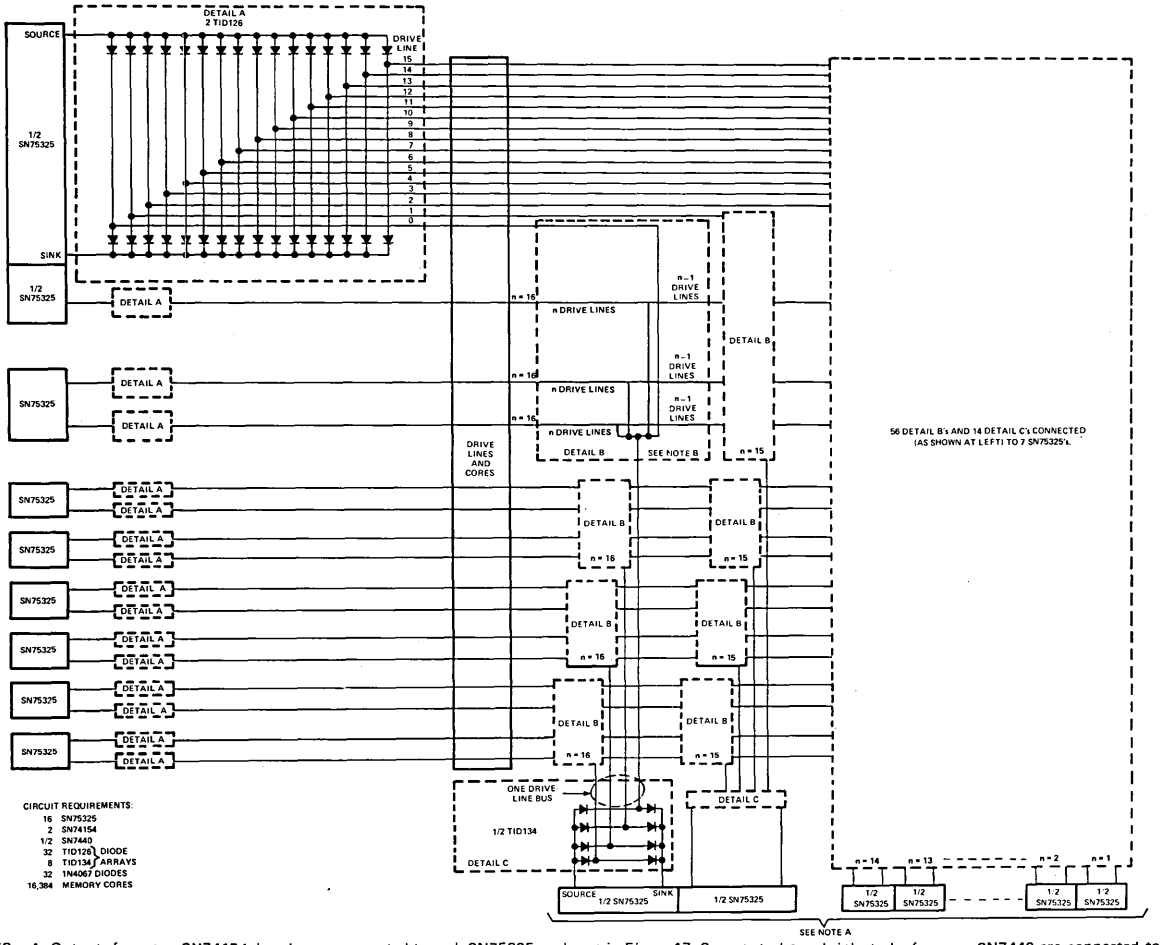
TYPICAL APPLICATION DATA

In memory-drive applications the SN75325 (or for full-temperature operation, the SN55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 17. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, SN74154 No. 1 must be set to 3 (with mode select high), enabling source X of SN75325 No. 2 to drive lines 12 through 15, and SN74154 No. 2 must be set to 2, providing a sink at Y of SN75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 18. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.



NOTE A: This optional mode-select and timing-strobe technique can be used in place of the SN7440 mode-select and SN74154 timing-strobe when minimum time skew is desired.

FIGURE 17–SN75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES



NOTES: A. Outputs from one SN74154 decoder are connected to each SN75325 as shown in Figure 17. Source strobe and sink strobe from an SN7440 are connected to each SN75325 as shown in Figure 17.

B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

FIGURE 18–SN75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY

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TYPICAL APPLICATION DATA

external resistor calculation

A typical magnetic-memory word-drive requirement is shown in Figure 19. A source-output transistor of one SN75325 delivers load current (I_L). The sink-output transistor of another SN75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \qquad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2,

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \qquad \text{(Equation 2)}$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3,

$$I_{CS} \approx 0.94\, I_L \qquad \text{(Equation 3)}$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20 V and V_L = 3 V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\ (20 - 3 - 2.2)}{500 - 1.6\ (20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

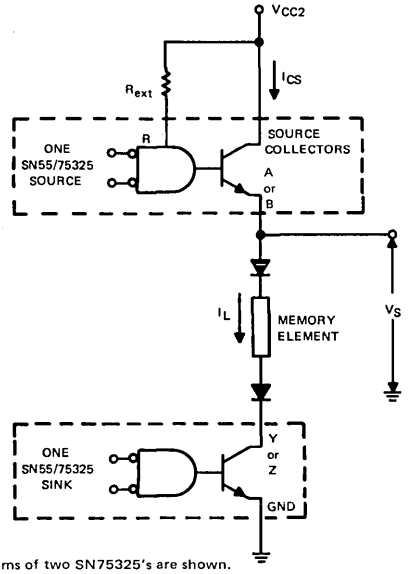
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

external resistor calculation (continued)



NOTES: A. For clarity, partial logic diagrams of two SN75325's are shown.
B. Source and sink shown are in different packages.

FIGURE 19

6

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TYPES SN55326, SN55327, SN75326, SN75327 MEMORY CORE DRIVERS

BULLETIN NO. DL-S 7712063, SEPTEMBER 1973 – REVISED APRIL 1977

SERIES 55/75 MEMORY DRIVERS
featuring

SN55326, SN75326 PERFORMANCE

- Quad Positive-OR Sink Memory Drivers
- 600-mA Output Current Sink Capability
- 24-V Output Capability
- Clamp Voltage Variable to 24 V

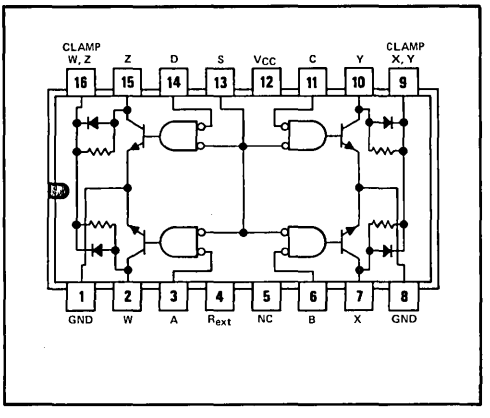
SN55327, SN75327 PERFORMANCE

- Quad Memory Switches
- 600-mA Output Current Capability
- V_{CC2} Drive Voltage Variable to 24 V
- Output Capable of Swinging Between V_{CC2} and Ground

EASE OF DESIGN

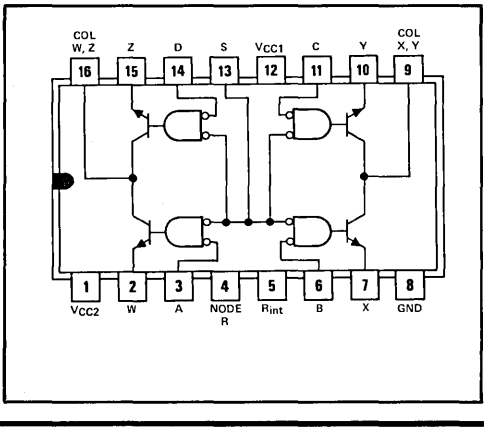
- High-Repetition-Rate Driver Compatible with High-Speed Magnetic Memories
- Inputs Compatible with TTL Decoders
- Minimum Time Skew between Strobe and Output-Current Rise
- Pulse-Transformer Coupling Eliminated
- Drive-Line Lengths Reduced

SN55326, SN75326
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

SN55327, SN75327
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN55326, SN55327, SN75326, and SN75327 are monolithic integrated circuit quadruple memory drivers. These devices accept standard TTL decoder input signals and provide high-current and high-voltage output levels suitable for driving magnetic memory elements. Output transistor selection is determined by using one of the four address inputs and the common timing strobe.

The SN55326 and SN75326 memory drivers can sink up to 600 milliamperes and operate from a single 5-volt supply. Each driver is similar to the sink drivers of the SN55325/SN75325. The four output transistors share a common base-drive resistor and it is recommended that only one of the four driver gates be selected at a time. Output-transistor base current may be increased by connecting an external resistor between R_{ext} (pin 4) and V_{CC}. Each output collector is protected from voltage surges during inductive switching by a clamp diode in parallel with its internal pull-up resistor. The two clamp pins may be returned to a power supply of from 4.5 volts to 24 volts.

The SN55327 and SN75327 memory switches can source or sink up to 600 milliamperes and operate from two supplies; one of five volts and the other from 4.5 volts to 24 volts. Each switch is similar to the source drivers of the SN55325/SN75325. They can function as either sink drivers or source drivers since the voltages at the output transistor terminals are capable of swinging between V_{CC2} and ground. The four output transistors share a common base-drive resistor and it is recommended that only one of the four outputs be selected at a time. An internal base-drive resistor is available on the chip and can be

description (continued)

used by connecting Node R (pin 4) to R_{int} (pin 5). This resistor provides adequate base current to the output transistors for output sink currents up to 375 milliamperes with V_{CC2} at 15 volts or 600 milliamperes with V_{CC2} at 24 volts. Base current can be regulated to within ±5 percent by substituting for this resistor an external resistor connected between Node R (pin 4) and V_{CC2} with R_{int} (pin 5) remaining open. This method is preferable in high-duty-cycle, high-power applications since the power dissipated in this resistor is outside the package. When a source current and V_{CC2} voltage other than the above values are required, it is recommended that the base drive be supplied through an external resistor of the appropriate value calculated using Equation 1 shown in the SN55325, SN75325 data sheet.

FUNCTION TABLE

INPUTS					OUTPUTS			
ADDRESS				STROBE				
A	B	C	D	S	W	X	Y	Z
L	H	H	H	L	ON	OFF	OFF	OFF
H	L	H	H	L	OFF	ON	OFF	OFF
H	H	L	H	L	OFF	OFF	ON	OFF
H	H	H	L	L	OFF	OFF	OFF	ON
H	H	H	H	X	OFF	OFF	OFF	OFF
X	X	X	X	H	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant
NOTE: Not more than one output is to be on at any one time.

The SN55326 and SN55327 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN75326 and SN75327 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55326	SN75326	SN55327	SN75327	UNIT
Supply voltage, V_{CC} or V_{CC1} (see Note 1)		7	7	7	7	V
Supply voltage, V_{CC2}				25	25	V
Input voltage, any address or strobe		5.5	5.5	5.5	5.5	V
Output collector voltage		25	25	25	25	V
Output clamp voltage		25	25			V
Output collector current		750	750	750	750	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J package	1375	1375	1375	1375	mW
	N package		1150		1150	
Operating free-air temperature range		−55 to 125	0 to 70	−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package		260	260	260	260	°C

recommended operating conditions

	SN55326			SN75326			SN55327			SN75327			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} or V_{CC1}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{CC2}							4.5		24	4.5		24	V
Output collector voltage			24			24			24			24	V
Output-clamp voltage, $V_{(clamp)}$	4.5		24	4.5		24							V
Output collector current			600			600			600			600	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal(s).
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, these chips are alloy-mounted.

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SN55326, SN75326 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55326 MIN	SN55326 TYP‡	SN55326 MAX	SN75326 MIN	SN75326 TYP‡	SN75326 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA,		−1	−1.7		−1	−1.7	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	I_O = 0	19	23		19	23		V
$V_{(sat)}$	Saturation voltage		V_{CC} = 4.5 V, $I_{(sink)}$ = 600 mA§, See Note 3	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
$V_{F(clamp)}$	Output-clamp-diode forward voltage		$V_{(clamp)}$ = 0, T_A = 25°C	$I_{(clamp)}$ = −10 mA,			1.5			1.5	V
$I_{(clamp)}$	Output-clamp current, one output on		$I_{(sink)}$ = 50 mA,	T_A = 25°C		5	7		5	7	mA
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off		All inputs at 5 V,	T_A = 25°C		18	25		18	25	mA
$I_{CC(on)}$	Supply current, one output on		$I_{(sink)}$ = 50 mA,	T_A = 25°C		58	75		58	75	mA

SN55326, SN75326 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 3		30	50	ns
t_{PHL}				25	50	
t_{TLH}	W, X, Y, or Z			7	15	ns
t_{THL}				10	20	
t_s	W, X, Y, or Z			24	35	ns
V_{OH}	W, X, Y, or Z	V_S = $V_{(clamp)}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 3	V_S−25			mV

†Unless otherwise noted, V_{CC} = 5.5 V, $V_{(clamp)}$ = 24 V. See Figure 1.
‡All typical values are at T_A = 25°C.
§Under these conditions, not more than one output is to be on at any one time.
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{TLH} ≡ transition time, low-to-high-level output
t_{THL} ≡ transition time, high-to-low-level output
t_s ≡ Storage time
V_{OH} ≡ High-level output voltage (after switching)
NOTE 3: These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.

For typical characteristic curves, Figures 11 through 14 of the SN55325/SN75325 data sheet apply for these circuits.

SN55327, SN75327 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55327 MIN	SN55327 TYP‡	SN55327 MAX	SN75327 MIN	SN75327 TYP‡	SN75327 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V, T_A = 25°C	I_I = −10 mA		−1	−1.7		−1	−1.7	V
$I_{(off)}$	Collectors terminal off-state current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full range			500			200	μA
				T_A = 25°C			150			200	
$V_{(sat)}$	Saturation voltage		V_{CC1} = 4.5 V, V_O = 0, $I_{(source)}$ = −600 mA§, See Notes 3 and 4	Full range			0.9			0.9	V
				T_A = 25°C		0.43	0.7		0.43	0.75	
I_I	Input current at maximum input voltage	Address	V_I = 5.5 V				1			1	mA
		Strobe					4			4	
I_{IH}	High-level input current	Address	V_I = 2.4 V				40			40	μA
		Strobe					160			160	
I_{IL}	Low-level input current	Address	V_I = 0.4 V			−1	−1.6		−1	−1.6	mA
		Strobe				−4	−6.4		−4	−6.4	
$I_{CC(off)}$	Supply current, all outputs off	From V_{CC1}	All inputs at 5 V,	T_A = 25°C		7	10		7	10	mA
		From V_{CC2}				13	20		13	20	
$I_{CC(on)}$	Supply current, one output on	From V_{CC1}	$V_{(col)}$ = 6 V,	$I_{(source)}$ = −50 mA,		8	12		8	12	mA
		From V_{CC2}	T_A = 25°C,	See Note 3		36	55		36	55	

SN55327, SN75327 switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER¶	TO (OUTPUT)	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 3 and Note 4		35	55	ns
t_{PHL}				30	55	
t_{TLH}	W, X, Y, or Z	$V_{(col)}$ = V_{CC2} = 20 V, R_L = 100 Ω, C_L = 25 pF, See Figure 4 and Note 4		30		ns
t_{THL}				10		
V_{OH}	Collectors W, Z or X, Y	V_S = V_{CC2} = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{(sink)}$ ≈ 500 mA, See Figure 3 and Note 4	V_S−25			mV

†Unless otherwise noted, V_{CC1} = 5.5 V, V_{CC2} = 24 V. See Figure 2.
‡All typical values are at T_A = 25°C.
§Under these conditions, not more than one output is to be on at any one time.
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{TLH} ≡ transition time, low-to-high-level output
t_{THL} ≡ transition time, high-to-low-level output
V_{OH} ≡ High-level output voltage (after switching)

NOTES: 3. These parameters must be measured using pulse techniques. t_w = 200 μs, duty cycle ≤ 2%.
4. A 350-Ω resistor is connected between node R (pin 4) and V_{CC2} (pin 1) with R_{int} (pin 5) open.

For typical characteristic curves, Figures 11 through 14 of the SN55325/SN75325 data sheet apply for these circuits.

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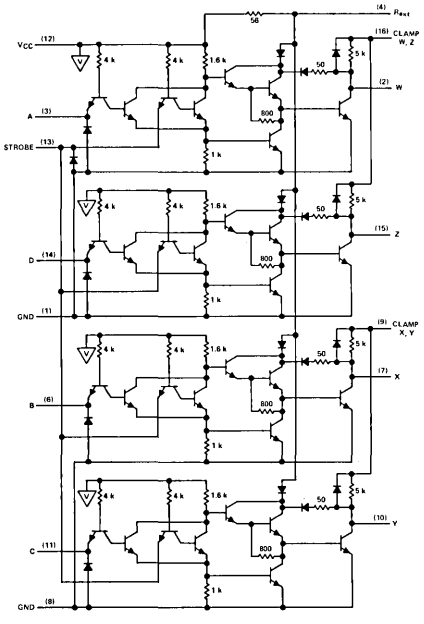
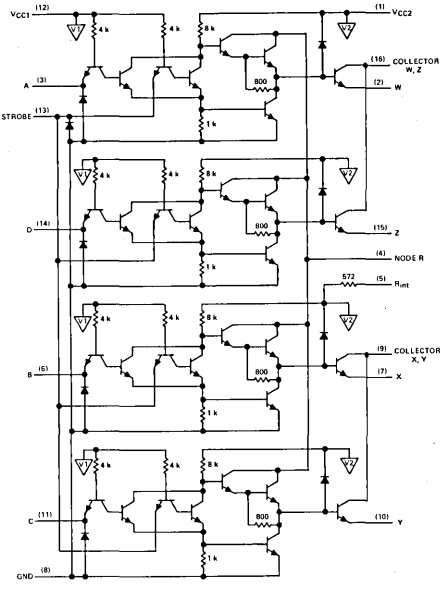
schematics

SN55326, SN75326



▽ ▽ ▽ . . . V_{CC}, V_{CC1}, or V_{CC2} bus, respectively.

SN55327, SN75327



Resistor values shown are nominal and in ohms.

PARAMETER MEASUREMENT INFORMATION

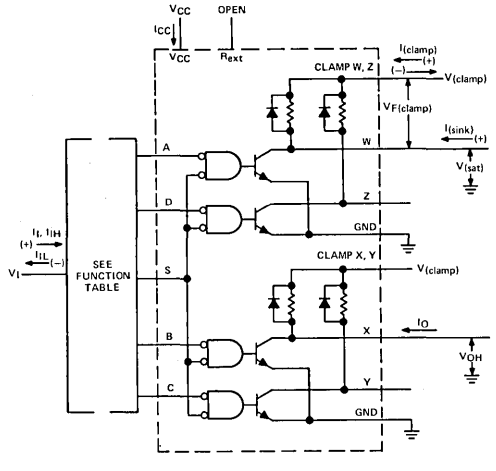
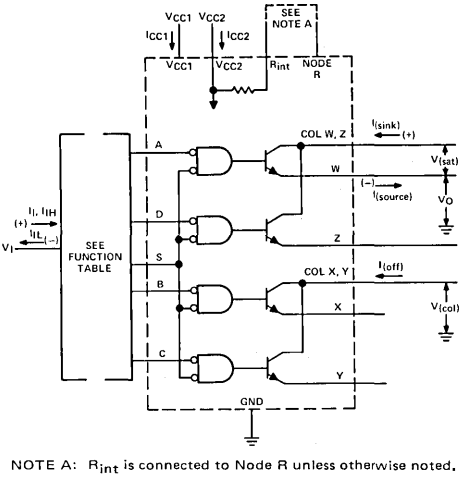


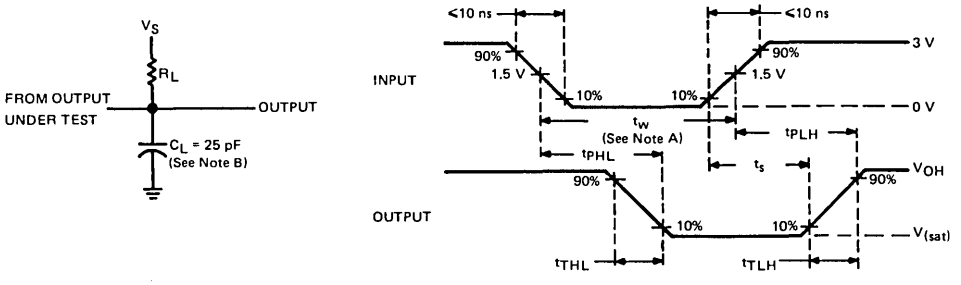
FIGURE 1–GENERALIZED TEST CIRCUIT FOR SN55326, SN75326



NOTE A: R_{int} is connected to Node R unless otherwise noted.

FIGURE 2–GENERALIZED TEST CIRCUIT FOR SN55327, SN75327

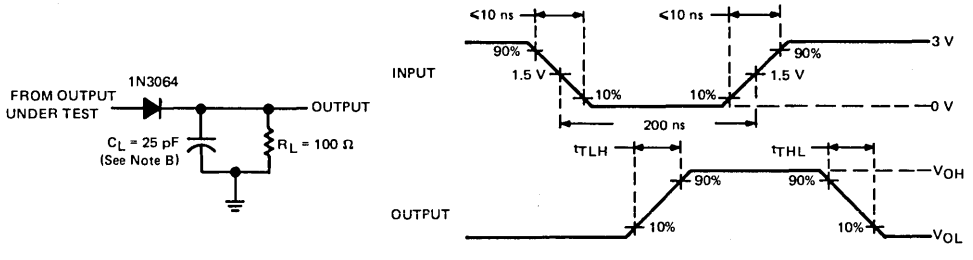
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For testing V_{OH} (after switching), t_w = 40 μs, PRR = 12.5 kHz. For all other tests, t_w = 200 ns, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES



LOAD CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 1%.
B. C_L includes probe and jig capacitance.

FIGURE 4–SWITCHING TIMES

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INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES SN75328, SN75330 QUADRUPLE MEMORY SWITCHES

BULLETIN NO. DL-S 7712458, APRIL 1977

- Quadruple Interface for Core and Bubble Memories
- Characterized for Use to 600 mA
- 24-V Output Capability
- Output Transient Voltage Protection
- Fast Switching Times . . . 40 ns Typ
- Outputs Capable of Swinging Between V_{CC2} and Ground
- Source/Sink Base Drive Externally Adjustable
- TTL- or DTL-Compatible Inputs
- Input Clamping Diodes

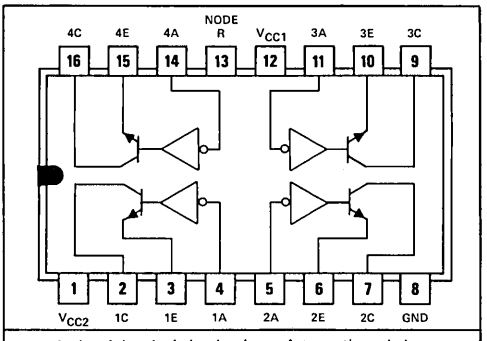
description

The SN75328 and SN75330 are monolithic integrated circuit memory switches with TTL logic inputs that are designed for use with core and bubble memories. Each device contains four 600-milliampere memory switches and operates from two power supplies, one of 5 volts and the other from 4.75 volts to 24 volts. Each switch is similar to the SN75327 except that the strobe circuitry is omitted, which allows the collectors of the output transistors to be assigned to individual package pins.

Each switch can function as either source driver or sink driver since the voltages at the output transistor terminals are capable of swinging between V_{CC2} and ground. On SN75328 the base drive of all four output transistors is provided by connecting an external resistor of the appropriate value between V_{CC2} and Node R. On SN75330 the base drive of each individual output transistor is provided by connecting an external resistor of the appropriate value between V_{CC2} and the corresponding Node R. By using this method the base current may usually be regulated within ±5%, and the power dissipated by this resistor is external to the package and allows the integrated circuit to operate at higher currents for a given junction temperature.

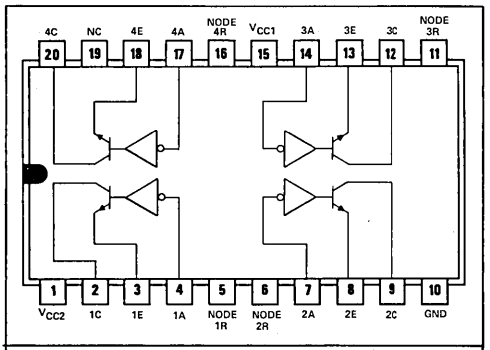
The SN75328 and SN75330 are characterized for operation from 0°C to 70°C.

SN75328
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic: A low logic level at input A turns the switch on.

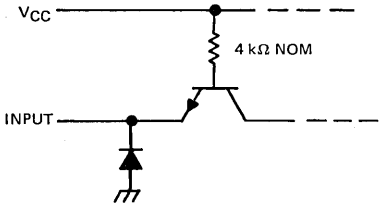
SN75330
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic: A low logic level at input A turns the switch on.

NC = No internal connection

schematic of each input



6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 25 V
Input voltage . . . . . 5.5 V
Output collector voltage . . . . . 25 V
Output collector current . . . . . 750 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 19. In the J package, SN75328 and SN75330 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75		24	V
Output collector voltage			24	V
Output collector current			600	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC1} = 4.75 V, I_I = −10 mA				−1	−1.7	V
$I_{(off)}$	Collector off-state current	V_{CC1} = 4.75 V, $V_{(col)}$ = 24 V, See Figure 1					200	μA
$V_{(sat)}$	Saturation voltage	V_{CC1} = 4.75 V, V_{CC2} = 15 V, See Figure 1, See Note 3	R_L = 285 Ω,	R_{ext} = 3.9 kΩ, $I_{(sink)}$ ≈ 50 mA		120	200	mV
			R_L = 95 Ω,	R_{ext} = 1.3 kΩ, $I_{(sink)}$ ≈ 150 mA		300	400	
			R_L = 48 Ω,	R_{ext} = 650 Ω, $I_{(sink)}$ ≈ 300 mA§		420	550	
			R_L = 32 Ω,	R_{ext} = 430 Ω, $I_{(sink)}$ ≈ 450 mA§		500	650	
			R_L = 24 Ω,	R_{ext} = 350 Ω, $I_{(sink)}$ ≈ 600 mA§		600	750	
I_I	Input current at maximum input voltage	V_I = 5.5V					1	mA
I_{IH}	High-level input current	V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−1	−1.6	mA
$I_{CC(off)}$	Supply current, all outputs off	All inputs at 5 V, T_A = 25°C		From V_{CC1}		7	10	mA
				From V_{CC2}		13	20	
$I_{CC(on)}$	Supply current, one output on	$V_{(col)}$ = 6 V, T_A = 25°C,	$I_{(source)}$ = −50 mA, See Note 3	From V_{CC1}		8	12	mA
				From V_{CC2}		36	55	

†Unless otherwise noted, V_{CC1} = 5.25 V, V_{CC2} = 24 V.
‡All typical values are at T_A = 25°C.
§Under these conditions, only one output is to be on at any one time.
NOTE 3: These parameters must be measured using pulse techniques, t_w = 200 μs, duty cycle ≤ 2%.

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switching characteristics, V_{CC1} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$V_S = V_{CC2}$ = 15V, R_L = 24 Ω, C_L = 25 pF, R_{ext} = 350 Ω, See Figure 2		40	60	ns
t_{PHL}	Propagation delay time, high-to-low level output			30	50	ns
t_{TLH}	Transition time, low-to-high level output			20	30	ns
t_{THL}	Transition time, high-to-low level output			15	25	ns
V_{OH}	High-level output voltage after switching	$V_S = V_{CC2}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, R_{ext} = 350 Ω, $I_{(sink)} \approx$ 500 mA, See Figure 2	V_S – 25			mV

§ Under these conditions, only one output is to be on at any one time.

PARAMETER MEASUREMENT INFORMATION†

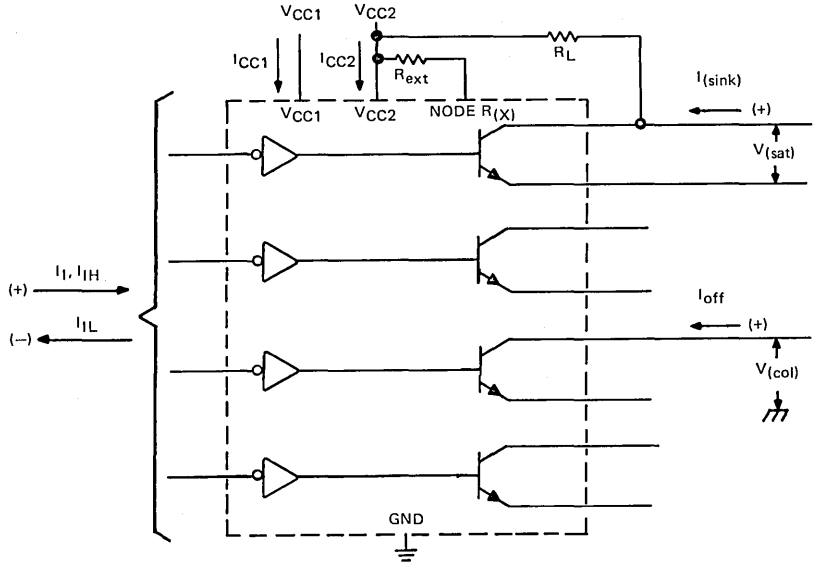
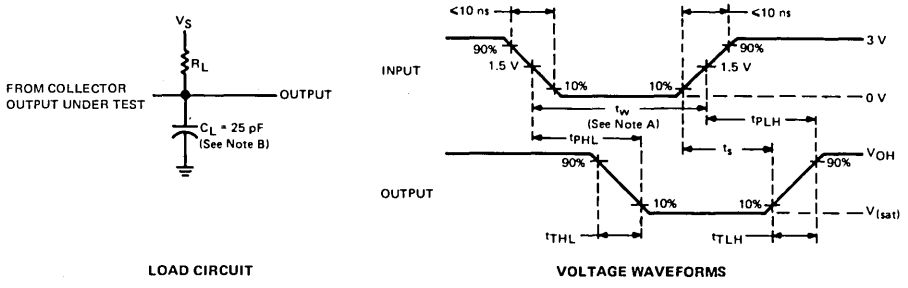


FIGURE 1–GENERALIZED TEST CIRCUIT

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



LOAD CIRCUIT VOLTAGE WAVEFORMS

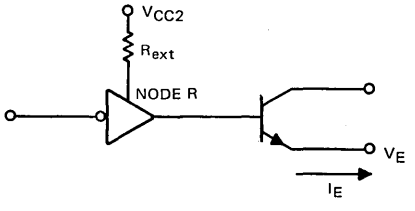
NOTES: A. Input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For testing V_{OH} after switching, $t_w = 40\ \mu s$, PRR = 12.5 kHz. For all other tests, $t_w = 200$ ns, duty cycle $\leq 1\%$.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES

TYPICAL APPLICATION DATA

external resistor calculation

The value of R_{ext} for any particular output current level may be determined by using the following equation:



$$R_{ext} = \frac{16(V_{CC2} - V_E - 2.2)}{|I_E| - 1.6\,(V_{CC2} - V_E - 2.9)}$$

where I_E is in mA and R_{ext} in kΩ.

Example 1. For $I_E = -300$ mA, $V_E = 4$ V, $V_{CC2} = 24$ V
$R_{ext} = 1\ k\Omega$

Example 2. For $I_E = -600$ mA, $V_E = 4$ V, $V_{CC2} = 24$ V
$R_{ext} = 0.5\ k\Omega$

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Selection Guide for Other Interface Circuits

PERIPHERAL DRIVERS

MAXIMUM OFF-STATE VOLTAGE	MINIMUM LATCH-UP VOLTAGE	MAXIMUM RECOMMENDED OUTPUT CURRENT	t_{PD}¶ TYPICAL	OUTPUT CLAMP DIODES	DRIVERS PER PACKAGE	INPUT COMPATIBILITY	DEVICE TYPE AND PACKAGE				LOGIC FUNCTION
							–55°C TO 125°C		0°C TO 70°C		
15 V	15 V	300 mA	15 ns		2	TTL, DTL			SN75430	J,N	AND*
									SN75431	JG,P	AND
									SN75432	JG,P	NAND
									SN75433	JG,P	OR
									SN75434	JG,P	NOR
30 V	20 V	100 mA	22 ns		2	ECL			SN75441	J,N	OR
30 V	20 V	300 mA	21 ns		2	TTL, DTL	SN55450B	J	SN75450B	J,N	AND*
							SN55451B	JG	SN75451B	JG,P	AND
							SN55452B	JG	SN75452B	JG,P	NAND
							SN55453B	JG	SN75453B	JG,P	OR
							SN55454B	JG	SN75454B	JG,P	NOR
35 V	30 V	300 mA	33 ns		2	TTL, DTL	SN55460	J	SN75460	J,N	AND*
							SN55461	JG	SN75461	JG,P	AND
							SN55462	JG	SN75462	JG,P	NAND
							SN55463	JG	SN75463	JG,P	OR
							SN55464	JG	SN75464	JG,P	NOR
35 V	30 V	500 mA	33 ns		2	TTL, DTL			SN75401	NE	AND
									SN75402	NE	NAND
									SN75403	NE	OR
									SN75404	NE	NOR
50 V	50 V	350 mA	1 μs	YES	7	TTL, DTL, CMOS, P-MOS			ULN2001A†	J,N	INVERTING BUFFER
						14-V to 25-V P-MOS			ULN2002A†	J,N	
						TTL and 5-V CMOS			ULN2003A†	J,N	
						6-V to 15-V P-MOS, CMOS			ULN2004A†	J,N	

*With output transistor base connected externally to output of gate.
† 0°C to 85°C
¶ t_{PD} = Propagation delay time

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PERIPHERAL DRIVERS (continued)

MAXIMUM OFF-STATE VOLTAGE	MINIMUM LATCH-UP VOLTAGE	MAXIMUM RECOMMENDED OUTPUT CURRENT	t_{pD}¶ TYPICAL	OUTPUT CLAMP DIODES	DRIVERS PER PACKAGE	INPUT COMPATIBILITY	DEVICE TYPE AND PACKAGE				LOGIC FUNCTION
							–55°C TO 125°C		0°C TO 70°C		
70 V	55 V	300 mA	33 ns		2	TTL, DTL	SN55470	J	SN75470	J,N	AND*
							SN55471	JG	SN75471	JG,P	AND
							SN55472	JG	SN75472	JG,P	NAND
							SN55473	JG	SN75473	JG,P	OR
							SN55474	JG	SN75474	JG,P	NOR
70 V	55 V	300 mA	100 ns	YES	2	TTL, DTL, MOS			SN75475	JG,P	NAND
70 V	55 V	300 mA	200 ns	YES	2	TTL, DTL, MOS			SN75476	JG,P	AND
									SN75477	JG,P	NAND
									SN75478	JG,P	OR
									SN75479	JG,P	NOR
70 V	55 V	500 mA	33 ns		2	TTL, DTL			SN75411	NE	AND
									SN75412	NE	NAND
									SN75413	NE	OR
									SN75414	NE	NOR
70 V	55 V	500 mA	200 ns	YES	2	TTL, DTL, MOS			SN75416	NE	AND
									SN75417	NE	NAND
									SN75418	NE	OR
									SN75419	NE	NOR
100 V	60 V	350 mA	130 ns	YES	7	TTL, DTL, CMOS, P-MOS			SN75466†	J,N	INVERTING BUFFER
						14-V to 25-V P-MOS			SN75467†	J,N	
						TTL and 5-V CMOS			SN75468†	J,N	
						6-V to 15-V P-MOS, CMOS			SN75469†	J,N	

*With output transistor base connected externally to output of gate.
†0°C to 85°C

¶ t_{PD} = Propagation delay time.

DISPLAY DRIVERS
FOR COMMERCIAL TEMPERATURE RANGE

DISPLAY TYPE	DESCRIPTION	INPUT COMPATIBILITY	POWER SUPPLIES	DRIVERS PER PACKAGE	DEVICE TYPE	PACKAGE TYPE	ADDITIONAL FEATURES
AC PLASMA DISPLAYS	AXIS DRIVER	CMOS	V_{CC1} = 12 V V_{CC2} variable from 40 V to 90 V	4	SN75426	J,N	• Independent addressing of each gate for serial and parallel applications • High input impedance (typically 1 megohm) • 30-mA clamp diodes on output • Switches 70 V in 1.2 μs • AND driver (SN75426); NAND driver (SN75427)
					SN75427	J,N	
		CMOS	V_{CC1} = 12 V V_{CC2} variable from 40 V to 100 V	32	*SN75500	N	• High-speed serially shifted data input operation (4 MHz max) • Fast output transitions (less than 150 ns) • 25-mA output current capability • Output short-circuit protection • Latches on all SN75501 driver outputs • X-axis driver — SN75500 • Y-axis driver — SN75501 (performs Y-axis sustaining function)
					*SN75501	N	
LED DISPLAYS	SEGMENT DRIVERS	MOS	10 V	4	SN75491	N	• 50-mA source/sink capability
			Variable from 3.2 V to 8.8 V	4	SN75493	N	• 50-mA regulated source capability • Display blanking provisions
	DIGIT DRIVERS	MOS	10 V	6	SN75492	N	• 250-mA sink capability
			Variable from 3.2 V to 8.8 V	6	SN75494	N	• 250-mA sink capability • Display blanking provisions
		MOS, TTL	Variable from 2.7 V to 6.6 V	7	SN75497	N	• 100-mA sink capability • Input threshold . . . 2.7 V max • Low voltage saturating outputs (0.4 V maximum)
		MOS, TTL	Variable from 2.7 V to 6.6 V	9	SN75498	N	• 100-mA sink capability • Input threshold . . . 2.7 V max

*Future product

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DISPLAY DRIVERS
FOR COMMERCIAL TEMPERATURE RANGE (continued)

DISPLAY TYPE	DESCRIPTION	INPUT COMPATIBILITY	POWER SUPPLIES	DRIVERS PER PACKAGE	DEVICE TYPE	PACKAGE TYPE	ADDITIONAL FEATURES
GAS DISCHARGE DISPLAYS	HIGH-VOLTAGE BCD-TO-SEVEN-SEGMENT DECODER/CATHODE DRIVERS	TTL	5 V	7	SN75480	N	• Outputs regulated to insure constant brightness • Blanking and ripple-blanking provisions • High off-state breakdown voltage (120 V typical) • Designed for seven segment displays such as Beckman and Panaplex II◇.
		TTL, MOS, CMOS	Variable from 4.75 V to 15 V	7½	*SN75484	N	same features as the SN75480 plus: • Decimal point provided • Latches to hold BCD information • Lower supply power requirements • Higher output voltage breakdown capability
	ANODE DRIVER	MOS	V_{EE} = −55 V, V_{BB} = −18 V	6	SN75481	N	• 13-mA output capability • Designed for time-multiplexed displays such as Panaplex II◇
THERMAL PRINT DISPLAYS	THERMAL-PRINTHEAD DRIVERS	TTL, CMOS	±5 V	6	SN75490	J,N	• Common strobe • 30-mA source, 50-mA sink capability
		MOS	5 V	7	SN75270	J,N	• Single ended, noninverting operation

*Future Product
◇Trademark of the Burroughs Corporation

LINE DRIVERS
WITH TTL-COMPATIBLE INPUTS

DESCRIPTION	OUTPUT CURRENT CAPABILITY	t_{PD}¶ TYPICAL	S = SINGLE ENDED D = DIFFERENTIAL	PARTY-LINE OPERATION	STROBE	POWER SUPPLIES	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	DRIVERS PER PACKAGE	COMPANION RECEIVERS	ADDITIONAL FEATURES
							–55°C TO 125°C	0°C TO 70°C				
GENERAL PURPOSE DRIVERS	300 mA	20 ns	S, D	YES	YES	5 V	SN55450B	SN75450B	J J,N	2	SN75122, SN75152, SN75115, SN75182, SN75140 series	
	300 mA	20 ns	S	YES	YES	5 V	SN55451B	SN75451B	JG JG,P	2		
	100 mA	36 ns	S		YES	5 V		SN75361A	JG,P	2		
	100 mA	22 ns	S	YES	YES	5 V	SN55121	SN75121	J J,N	2	SN75122	
	40 mA	12 ns	D		YES	5 V	SN55183	SN75183	J J,N	2	SN75115, SN75182	
	40 mA	15 ns	D		YES	5 V	SN55114	SN75114	J J,N	2		
	40 mA	13 ns	D	YES	YES	5 V	SN55113	SN75113	J J,N	2		• 3-State Output
	40 mA	15 ns	S, D	YES	YES	5 V	DS7831	DS8831	J J,N	2,4§	SN75140 series, SN75115, SN75122, SN75124, SN75125,	• Output clamp diodes to V_{CC} • 3-State Output
	40mA	15 ns	S, D	YES	YES	5V	DS7832	DS8832	J J,N	2,4§	SN75127, SN75128, SN75129, SN75152, SN75182	• 3-State Output

§ 4 for single-ended lines; 2 for differential lines

¶ t_{PD} = Propagation delay time.

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LINE DRIVERS (continued)
WITH TTL-COMPATIBLE INPUTS

DESCRIPTION	OUTPUT CURRENT CAPABILITY	t_{PD}¶ TYPICAL	S = SINGLE ENDED D = DIFFERENTIAL	PARTY-LINE OPERATION	STROBE	POWER SUPPLIES	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	DRIVERS PER PACKAGE	COMPANION RECEIVERS	ADDITIONAL FEATURES
							−55°C TO 125°C	0°C TO 70°C				
360/370 I/O INTERFACE	100 mA	20 ns	S	YES	YES	5 V		SN75123	J,N	2	SN75124, SN75125, SN75127, SN75128	
			S	YES				*SN75126	J,N			CMOS◆
DRIVERS MEETING EIA STANDARDS	40 mA	16 ns	D			5 V	SN55158	SN75158	JG JG,P	2	uA9637, SN75157	RS-422△
	10 mA	60 ns	S		YES	±12 V		SN75150	JG,P	2	SN75152, SN75154	RS-232C≠
	6 mA	220 ns	S		YES	±12 V		SN75188	J,N	4	SN75189, SN75189A	RS-232C≠
	75 mA		S			±12 V	*uA9636M	*uA9636C	JG JG,P	2	uA9637, SN75157	CMOS◆; RS-423▲; RS-232C≠
	50 mA	10 ns	D			5 V	*uA9638M	*uA9638C	JG JG,P	2		CMOS◆; RS-422△
	40 mA	16 ns	D	YES	YES	5V		SN75159	J,N	2	uA9637, SN75157	3-State Output; RS-422△
CURRENT-MODE DRIVERS	18 mA	9 ns	D	YES	YES	±5 V		SN75112	J,N	2	SN75107A, SN75107B, SN75108A, SN75108B, SN75207, SN75207B, SN75208, SN75208B	
	6.5 mA	9 ns	D	YES	YES	±5 V	SN55110A	SN75110A	J J,N	2		
	3.5 mA	9 ns	D	YES	YES	±5 V	SN55109A	SN75109A	J J,N	2		

¶ t_{PD} ≡ Propagation delay time

★ Future product

◆Also CMOS input compatible

≠Satisfies requirements of EIA Standard RS-232C

▲Satisfies requirements of EIA Standard RS-423

△Satisfies requirements of EIA Standard RS-422

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7

LINE RECEIVERS

• OUTPUT STROBE • PARTY-LINE OPERATION

DESCRIPTION	TYPE OF OUTPUT†	t_{PD}¶ TYPICAL	INPUT SENSITIVITY	COMMON-MODE RANGE	POWER SUPPLIES	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	RECEIVERS PER PACKAGE	COMPANION DRIVERS	ADDITIONAL FEATURES
						−55°C to 125°C	0°C to 70°C				
DIFFERENTIAL-LINE RECEIVERS	T-P	17 ns	±10 mV	±3 V	±5 V		SN75207	J,N	2	SN75109A, SN75110A, SN75112	• "B" versions have input protection diodes for power off condition
							SN75207B	J,N			
	O-C	19 ns					SN75208	J,N	2		
							SN75208B	J,N			
	T-P	17 ns	±25 mV			SN55107A	SN75107A	J J,N	2		
						SN55107B	SN75107B	J J,N	2		
	O-C	19 ns	±25 mV			SN55108A	SN75108A	J J,N	2		
						SN55108B	SN75108B	J J,N	2		
SINGLE-ENDED LINE RECEIVERS	T-P	20 ns			5 V	SN55122	SN75122	J J,N	3	SN75121, DS8831, DS8832	• Hysteresis for improved noise immunity
	T-P	22 ns	±100 mV		5 V	SN55140	SN75140	JG JG,P	2	75450B series, SN75361A, SN75113, DS8831, DS8832	• Common reference voltage pin and strobe • Input protection diodes ('141)
						SN55141	SN75141	JG JG,P	2		
						SN55142	SN75142	J J,N	2		• Individual reference voltage and strobe terminals • Input protection diodes ('143)
						SN55143	SN75143	J J,N	2		

†T-P ≡ Totem pole, O-C ≡ Open collector, R ≡ Resistor pull-up
¶t_{PD} = Propagation delay time

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LINE RECEIVERS (continued)

DESCRIPTION	S = SINGLE ENDED D = DIFFERENTIAL	TYPE OF OUTPUT†	t_{PD}¶ TYPICAL	PARTY-LINE OPERATION	STROBE	POWER SUPPLIES	DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	RECEIVERS PER PACKAGE	COMPANION DRIVERS	ADDITIONAL FEATURES
							–55°C to 125°C	0°C to 70°C				
RECEIVERS FOR 360/370 I/O INTERFACE	S	T-P	20 ns	YES	YES	5 V		SN75124	J,N	3	SN75123, SN75126	• Hysteresis
			18 ns	YES		5 V		SN75125	J,N	7	SN75123, SN75126	• Schottky Circuitry • Standard V_{CC} Pinout (SN75127)
								SN75127	J, N	7		
			18 ns	YES	YES	5 V		SN75128	J, N	8	SN75123, SN75126	• Schottky Circuitry
								SN75129	J, N	8		
RECEIVERS MEETING EIA STANDARD RS-232-C	S	T-P	22 ns			5 V or 12 V		SN75154	J,N	4	SN75150	• Hysteresis
	S	R	25 ns			5 V		SN75189	J,N	4	SN75188	• Response Threshold Control • '189A has more hysteresis than '189
								SN75189A	J,N	4		
	D	R	60 ns		YES	±12 V		SN75152	J,N	2	SN75150	• Also meets MIL-STD-188C • Hysteresis
RECEIVERS MEETING EIA STANDARD RS-422/423	D	O-C	20 ns			5 V	*SN55157	*SN75157	JG JG,P	2	SN75158, SN75159, uA9636, uA9638	• Standard V_{CC} Pinout ('157) • Schottky Circuitry
							*uA9637M	*uA9637C	JG JG,P	2		
RECEIVERS WITH RESPONSE TIME CONTROL	D	O-C or T-P	20 ns	YES	YES	5 V	SN55115	SN75115	J J,N	2	SN75113, SN75114, SN75183, DS8831, DS8832	• Input Sensitivity: ±500 mV • Common-Mode Range: ±15 V
		T-P	31 ns	YES	YES		SN55182	SN75182	J J,N	2		

†T-P ≡ Totem pole, O-C ≡ Open collector, R ≡ Resistor pull-up
¶ t_{PD} = Propagation delay time
*Future product

DIFFERENTIAL-LINE TRANSCEIVERS

COMMON FEATURES	RECEIVER CHARACTERISTICS			DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	ADDITIONAL FEATURES
	STROBE OR ENABLE	TYPE† OF OUTPUT	COMMON-MODE RANGE	−55°C to 125°C	0°C to 70°C		
• Single 5-V supply • Party-line operation • TTL-compatible driver inputs • Driver enable for 3-state driver output • Driver output current capability: 40 mA • Driver propagation delay time: 14 ns (typical) • Receiver propagation delay time: 20 ns (typical) • ±500 mV receiver input sensitivity • One transceiver per package	STROBE	O-C or T-P	±15 V	SN55116	SN75116	J J,N	• Receiver frequency response control
		T-P	0 V to 6 V	SN55117	SN75117	JG JG,P	• Driver and receiver connected internally
	ENABLE	O-C or T-P	±15 V	SN55118	SN75118	J J,N	• Same as '116 with 3-State receiver output
		T-P	0 V to 6 V	SN55119	SN75119	JG JG,P	• Same as '117 with 3-State receiver output

SINGLE-ENDED LINE TRANSCEIVERS

COMMON FEATURES	DRIVER CHARACTERISTICS			RECEIVER CHARACTERISTICS		DEVICE TYPE FOR TEMPERATURE RANGE		PACKAGE TYPE	ADDITIONAL FEATURES
	OUTPUT CURRENT CAPABILITY	t_{PD}¶ TYPICAL	STROBE OR ENABLE	t_{PD}¶ TYPICAL	STROBE OR ENABLE	−55°C to 125°C	0°C to 70°C		
• Single 5-V supply • Party line operation • TTL-compatible driver inputs • Totem-pole receiver outputs • Four transceivers per package	100 mA	10 ns	STROBE	10 ns		AM26S10M	AM26S10C	J J,N	• Schottky circuitry • P-N-P inputs to minimize loading • Inverting driver (AM26S10)
	100 mA	12 ns	STROBE	10 ns		AM26S11M	AM26S11C	J J,N	
	100 mA	15 ns	STROBE	8 ns		SN55138	SN75138	J J,N	• 2.3 V receiver threshold for maximum system noise margin
	40 mA	16 ns	ENABLE	8 ns	ENABLE		SN75136	J,N	• Similar to N8T26 • 3-State driver and receiver outputs with Schottky circuitry • P-N-P inputs to minimize loading
	48 mA	30 ns	STROBE	30 ns			MC3446	J,N	• Meets IEEE STD 488 • Receiver input hysteresis • Drivers also MOS compatible

† T-P ≡ Totem pole, O-C ≡ Open-collector, R ≡ Resistor pull-up

¶ t_{PD} ≡ Propagation delay time

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