SPWU003

TMS380 Adapter Chipset User's Guide Supplement

Local Area Network Products

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1. Introduction

This supplement to the *TMS380 Adapter Chipset User's Guide* is provided to supply information on recently announced TMS380 Token Ring Adapter Chipset hardware and software enhancements. Included in this supplement are:

- TMS380-based Data Link Control (DLC) extended software interface provided when the IEEE 802.2 Logical Link Control (LLC) and IEEE 802.5 Medium Access Control (MAC) are resident.
- EPROM-based adapter bus expansion for LLC support.
- DRAM-based adapter bus expansion for LLC support.
- Updated adapter design and bring-up guidelines, including Adapter Debug Software and Ring Interface layout.
- TMS38021 Bridge Application.

Additionally, the appendices within this supplement provide:

- Complete errata for the *TMS380 Adapter Chipset User's Guide* (SPWU001D).
- Detailed engineering change notice for altering the Texas Instruments TMDS380PCF-1 PC Family Token Ring development card to allow it to operate with the TMS380-based Logical Link Control.
- Sample download driver program to allow the TMS380-based Logical Link Control to be downloaded into RAM on the TMS380 Adapter Bus.
- Command comparison at the TMS380 DLC interface with the commands at IBM's PC adapter hardware interface.

The reader is assumed to be familiar with information in the following references:

- *TMS380 Adapter Chipset User's Guide*, Revision D (TI, SPWU001D)
- *IBM Token-Ring Network Architecture Reference* (IBM, #6165877)
- *IBM Token-Ring Network PC Adapter Technical Reference* (IBM, #69X7862)
- ANSI/IEEE Standard 802.2-1985
- *Token Ring Access Method and Physical Layer Specification,* ANSI/IEEE Standard 802.5-1985, ISO Draft Proposal 880215, approved 12/13/85.

2. DLC System Software Interface

This section describes the extended DLC software interface presented by the TMS380 when the IEEE 802.2 Logical Link Control (LLC) software is resident on the adapter. This interface controls the operation of the adapter to effect data transfer to and from the network. Data and control information are passed between the adapter and the attached system by both Direct Input/Output (DIO) and Direct Memory Access (DMA) operations. Four System Interface Registers and a 26-byte Interface Control Block (ICB) are accessed via DIO. The DMA channel is used to pass commands, parameters, and frames to and from attached system memory.

The TMS380 adapter with LLC provides a Data Link Control interface encompassing both the IEEE 802.2 LLC and IEEE 802.5 MAC protocols (see Figure 2-1). This section describes both of these interfaces. The MAC interface described is the same as the Medium Access Control interface described in Section 4 of the *TMS380 Adapter Chipset User's Guide.* Therefore, software written for the MAC-level TMS380 will continue to run to this interface.

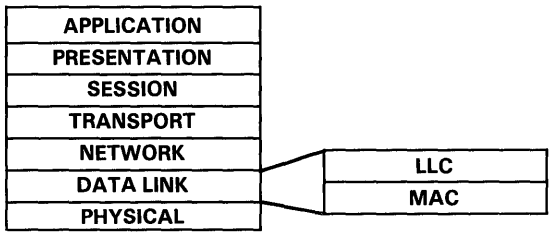


Figure 2-1. Open Systems Interconnect Model

Users programming to the adapter may choose to use only the MAC interface or may take advantage of the higher functionality that the LLC interface provides. The LLC interface supports both Type 1 and Type 2 protocols.

The Adapter Advantage. Because of its use by IBM, and other major implementers of communications protocols, Logical Link Control software has become an important factor on the token ring. LLC is the cornerstone on which IBM's Netbios and APPC, and MAP/TOP's OSI protocols are based.

LLC software executing on the TMS380 adapter has several advantages over LLC on the attached system. First, with the LLC on the TMS380, a user can guarantee the same LLC across an entire product line. For host-based LLC, different code would have to be developed for different hosts, thus introducing the possibility of incompatibilities. TI has provided, on the TMS380, a single version of LLC for compatibility and portability across all product lines, including different host processors and operating systems, such as MS-DOS, UNIX, and VM. Thus, equipment developers using the TMS380 are spared significant development costs through simplified system integration. With LLC on the TMS380, the LAN protocols are independent of the attached product and operating system.

A second advantage of having the LLC on the adapter is that system performance can be increased up to 100% over host-based solutions. This increased performance results largely from the decreased data movement. With host-based LLC, received frames must be transferred to the attached system, an acknowledgment packet built in the attached system, and the acknowledgment packet transferred to the adapter for transmission. With LLC in the adapter, received frames are examined while still in the adapter, and acknowledgment packets are built and sent from within the adapter. This decreased data movement increases overall network throughput.

Another factor in performance improvement is increased available processing time for the attached system. When the attached system is relieved of the LLC protocols, more bandwidth is available for data processing. Thus, frames are queued to the adapter for transmission faster than when the LLC is host-resident. Because the LLC protocols can be handled on the adapter, the attached system is freed from time consuming operations such as sequencing, acknowledgments, link session control, and automatic retries. Therefore, more of the attached system's processor power and memory space is available for user functions.

By putting 802.2 Logical Link Control on the TMS380 adapter, TI has increased performance, confidence of compatibility, portability, and ease of use of the protocols.

2.1 Logical Link Control

This section describes the Logical Link Control functions and parameters necessary to use the LLC programming interface. For more detailed information on the LLC protocols, refer to the *IBM Token Ring Architecture Reference* (IBM, 1986), and the IEEE/ANSI Standard 802.2-1985.

The IEEE 802.2 Logical Link Control sublayer is the top sublayer in the Data Link Layer of the OSI Reference Model. The LLC sublayer is common to all the IEEE 802 Medium Access Control layers. The LLC sublayer provides services for the Network layer protocol. There are currently three types of Logical Link Control operation defined by the IEEE 802 standard. These include Type 1, Type 2, and Type 3. They are provided to satisfy a broad range of applications.

2.1.1 Type 1 — Connectionless LLC

Type 1 LLC provides a connectionless data link service. This type of protocol provides a data link with minimum protocol complexity. Type 1 LLC could be used where the upper layers provide sufficient error detection and recovery, and the user does not wish to duplicate these functions at the data link layer. Type 1 LLC could be used in an application where it is not necessary to guarantee all data link layer transmissions. Type 1 LLC also includes the protocols for determining which type of LLC protocol a node supports. Type 1 is used in the MAP/TOP implementation of ISO protocols.

When using Type 1 communications, each node must open a Service Access Point (SAP) through which communication takes place. A separate SAP is opened for each protocol stack running above the LLC in a node. The SAP is an identifier for the LLC, a pointer to the application above it. When a SAP is opened, the attached system indicates the SAP_VALUE which is to be used. This SAP_VALUE is placed in the Source SAP location of each frame sent from this SAP, and is compared against the Destination SAP in received frames. In turn, when the SAP is opened, the adapter provides a STATION_ID to the attached system. This STATION_ID is used for communications between the attached system and the adapter. It is used in commands in both directions between the adapter and attached system as an identifier. The STATION_ID consists of two

bytes. The first byte indicates a SAP, and the second indicates a Link Station. Link Stations will be discussed later. The adapter assigns the STATION_ID in a round robin fashion. For example, the first SAP opened will have the STATION_ID of >0100.

When a SAP is opened, the user has several configuration options for that SAP. The first is a choice of whether the adapter will respond to XID command frames for this SAP, or whether these frames should be passed on to the host. This is controlled by the XID_HANDLER bit in the OPEN.SAP options. See the description of the OPEN.SAP command for more details. If the attached system selects to receive XID frames, then all received XID commands are passed to the attached system. Conversely, if the SAP is opened such that the adapter will respond to XID commands, then the adapter will respond to all XID commands. All XID response frames received will be passed to the attached system regardless of the state of the XID_HANDLER bit.

The other option a user has when opening a SAP is whether the group SAP corresponding to this SAP should be opened. A group SAP is indicated by a one in the least significant bit of the SAP_VALUE. A group SAP can be used in the destination SAP field of a frame to send frames to more than one SAP at a node. When a frame to a group SAP is received, the adapter duplicates the frame and issues a RECEIVE.PENDING interrupt to each of the individual SAPs belonging to the group SAP.

Once the SAP has been opened, the user of that SAP can transmit and receive any Type 1 frame through that SAP. Type 1 frames are listed below. The frames are described later.

- XID
- TEST
- UI

All communication directly through the SAP is connectionless.

2.1.2 Type 2 — Connection-Oriented LLC

For connection-oriented services, the attached system must open further connections after opening the SAP.

IEEE 802.2 Type 2 LLC provides a connection-oriented data link service. Type 2 LLC is similar to HDLC protocols in use today. Type 2 LLC guarantees the delivery of all data link transmissions with sequencing, acknowledgments, and automatic retries. With Type 2 LLC, connections are established between nodes wishing to communicate prior to any data transmissions. These are referred to as "link stations". Type 2 LLC is the data link layer of IBM's protocols for local area networks.

For illustration, a typical LLC Type 2 session is shown in Figure 2-2. A station wishing to communicate (station 1) sends out a connection request frame to the station with which it wants to communicate (station 2). If station 2 is able (has the resources, is authorized) to establish communications, then station 2 returns a positive acknowledgment to the connection request. Otherwise, a negative acknowledgment is returned and no communication link is established. Assuming that the acknowledgment is positive, the link is established, and data transfer, single or multiple, can take place in either direction. All data is acknowledged; however, not every packet need be acknowledged with a separate acknowledgment. A single acknowledgment may acknowledge multiple packets, and acknowledgments can be piggybacked onto data packets. Once all data has been transferred, either station can send a disconnect request to close the link. This frees resources in both stations for other communications.

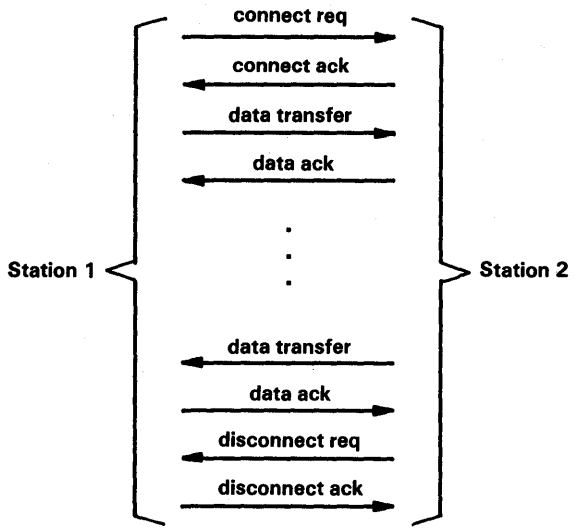


Figure 2-2. A Typical LLC Session

To establish communications for Type 2 operation, the attached system must open a SAP and then open a Link Station associated with that SAP. The link station creates a link from the SAP in this node to another SAP in a different node. One link station can be associated with only one local SAP and only one remote SAP on one remote node. A SAP may have multiple link stations associated with it. This hierarchy is illustrated in Figure 2-3.

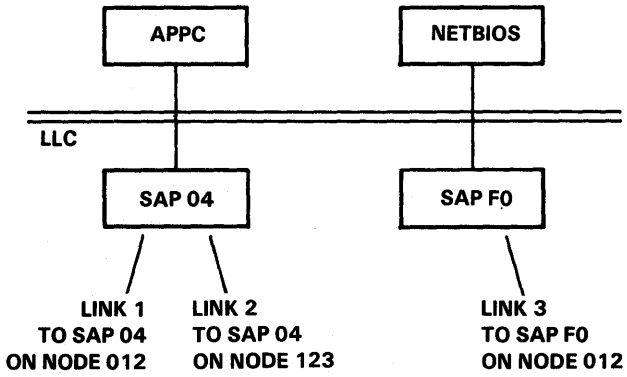


Figure 2-3. SAP/Link Station Association

As with the opening of SAPs, when the attached system opens a link station, the adapter assigns a STATION_ID for use in commands between the attached system and the adapter. The first byte of this STATION_ID will be the SAP STATION_ID, and the second will be the Link Station identifier. That is, a STATION_ID of >0102 indicates the second link station opened, and indicates that it was opened under the first SAP.

2.1.3 Type 3 — Connectionless-Acknowledged LLC

The third type of LLC is specifically intended for use in manufacturing applications. Type 3 is known as "connectionless acknowledged" service. Type 3 supports a protocol where packets are sent and acknowledged one at a time, without establishing the link stations of Type 2. This provides a certainty of delivery without the overhead of a Type 2 link station. For traffic that tends to be bursts of one frame, this type of protocol is suitable. The TMS380 DLC software does not implement Type 3 LLC.

2.1.4 LLC Frames

The following is a description of the frames used for communications with LLC. The LLC frame has the format shown in Figure 2-4.

Figure 2-4. LLC Frame

The MAC HEADER consists of the Starting Delimiter (SDEL), Access Control (AC), Frame Control (FC), Destination Address (DA), Source Address (SA), and Routing Information (RI) fields. The MAC TRAILER consists of the Frame Check Sequence (FCS) and Ending Delimiter (EDEL) fields. These fields are described in the *TMS380 Adapter Chipset User's Guide*. The LLC Header consists of the Destination SAP (DSAP), the Source SAP (SSAP), and the LLC Control fields. These fields are described below:

DSAP: This byte indicates the SAP to which the frame is destined. The receiving node copies the frame due to an address match on the Destination Address (DA), and then routes the frame to the appropriate attached system software based on the DSAP field value.

SSAP: This byte indicates the SAP from which the frame originated. By examining the SSAP and Source Address (SA) fields, the adapter can determine to which link station under the DSAP the frame is destined. Since the source SAP may only be an individual SAP, the least significant bit of the SSAP field is used to distinguish commands from responses. If this bit is zero, the frame is a command. If the bit is one, the frame is a response.

LLC CONTROL: This field is either one or two bytes in length. For unnumbered LLC frames it is one byte; for numbered frames it is two bytes. This field is the "command" field of the LLC. It determines what type of LLC frame this is. The LLC Control field can take on the values described in the following pages. For more information on these frames, see the IEEE/ANSI Standard 802.2 -1985 and the *IBM Token-Ring Network Architecture Reference* (IBM, 1986).

Unnumbered Information. The Unnumbered Information (UI) frame is the means of transferring data in a Type 1 environment. For this frame, the LLC Control field takes on the binary value b'00000011'.

Exchange Identification. The Exchange ID (XID) is a frame used by LLC to identify the properties of a SAP and request the properties of a remote SAP. This frame identifies the type(s) of LLC that are supported by a SAP, and also identifies the receive window size (N3), which will be discussed later. The LLC Control field for this frame contains the binary value b'101p1111'. The "p" value is the poll/final bit of LLC. The poll/final bit is used to check that the remote station is responding to frames. If the poll bit in a command is set to one, then the final bit (same bit position) in the response to that command must also be set to one. This mechanism can be used to match a response with the polled command. The least significant bit of the SSAP field will be zero, indicating a command, in the command XID. The bit will be a one in the response XID. For more information on the poll/final bit and the XID command, see the *IBM Token-Ring Network Architecture Reference* (IBM, 1986) and the IEEE/ ANSI Standard 802.2-1985.

Test. The Test Command frame is sent to cause the remote station to send a Test Response. Any data sent in a Test Command is echoed in the Test Response. For the Test frame, the LLC Control field takes on the value b'111p0011', where the "p" bit is the poll/final bit. The least significant bit of the SSAP field will be zero to indicate a command, or one to indicate a response, as appropriate.

Set Asynchronous Balanced Mode Extended. The Set Asynchronous Balanced Mode Extended (SABME) frame is sent to initiate a link station between two SAPs. This frame is sent as a result of a CONNECT.STATION command issued by the attached system. The value of the LLC Control field is b'011p1111'.

Disconnect. The Disconnect command (DISC) is sent to request that a link between two SAPs be shut down. This frame is sent as a result of a CLOSE.STATION command from the attached system, or various error conditions in the link station. The LLC Control field for the DISC is b'010p0011'.

Unnumbered Acknowledgment. The Unnumbered Acknowledgment (UA) is a response sent to positively acknowledge received unnumbered commands. The UA is sent as a response to the SABME and DISC commands. The LLC Control field for the UA response is b'011f0011'. The "f" bit is the poll/final bit described earlier.

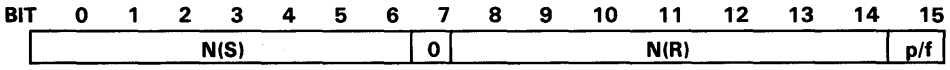
Disconnected Mode. The Disconnected Mode (DM) frame is a response sent to negatively acknowledge received unnumbered commands. The DM is sent as a response to the SABME when resources are not available to establish the requested link. The DM is sent as a response to the DISC command when the receiving adapter is in the Disconnected mode. This usually has resulted from error conditions in the link station. The LLC Control field for the DM response is b'000f1111'.

Frame Reject. The Frame Reject (FRMR) is a response sent when an illegal frame is received. An illegal frame is one of the following:

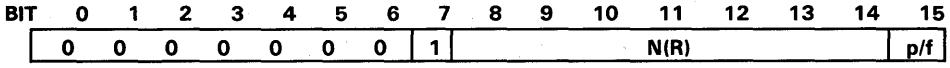
1. An information field in a UA, DM, SABME, or DISC frame, which do not allow information fields.
2. The final bit set to one when no poll bit was set.
3. An unsolicited UA frame.
4. An invalid N(R) from the remote station.
5. An unexpected N(S) from the remote station.

The LLC Control field for the FRMR response is b'100f0111'.

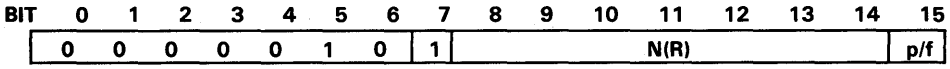
Information Frame. The I Frame is used to transfer data in an LLC Type 2 connection. Each I Frame contains a send sequence number, N(S), that is the sequence number of this I Frame. It also contains a received sequence number, N(R), which has the same meaning as in the RR and RNR frames. Thus, acknowledgments can be piggy-backed on I Frames. The format of the I Frame is shown below. Note that bit 7 of the Control field set to zero indicates an I Frame.



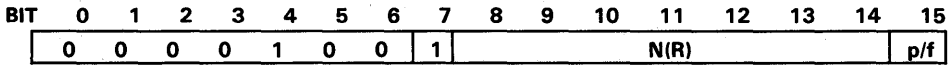
Receive Ready. The Receive Ready (RR) response is sent in response to a received I Frame. This response acknowledges receipt of the frame, and indicates that the receiving adapter is ready to receive additional frames. Contained within the RR frame is the N(R) number, which is the sequence number of the I Frame that the station expects to receive next. That is, an RR frame with N(R) = 3 acknowledges all I Frames through the I Frame with sequence number 2. The RR frame can also be used without the receipt of an I Frame to periodically check that the link station is still functioning. This process is known as checkpointing and is described later. The format of the RR frame is shown below. The p/f bit is the poll/final bit.



Receive Not Ready. The Receive Not Ready (RNR) response is sent in response to a received I Frame. This response acknowledges receipt of the frame, and indicates that the receiving adapter is not ready to receive additional frames. Contained within the RNR frame is the N(R) number, which is the sequence number of the I Frame that the station expects to receive next. That is, an RNR frame with N(R) = 3 acknowledges all I Frames through the I Frame with sequence number 2. The RNR frame can also be used in the checkpointing process. The format of the RNR frame is shown below.



Reject. The Reject (REJ) response is sent to request the retransmission of I frames beginning with the frame whose sequence number is contained in the N(R) field. The format of the REJ frame is shown below.



2.1.5 LLC Protocol States

In Type 2 communications, link stations can take on any of eight (8) primary and seven (7) secondary states. The descriptions of these states follows. For further information on link station states, the user should refer to the *IBM Token-Ring Architecture Reference* (IBM, 1986).

Closed. This is the default state of all non-existent link stations. In this state, all received frames except the SABME will be ignored. This state is entered when:

1. A CLOSE.STATION command issued by the attached system is completed.
2. The attached system issues an LLC.RESET command.

This state is exited to the Disconnected state when the attached system issues an OPEN.STATION command or a SABME has been received and the adapter is waiting for the attached system's response to the connection request.

Disconnected. This state is entered when:

1. The attached system issues an OPEN.STATION command.
2. The adapter has received a SABME frame and opened the station.
3. A DISC command has been received from the remote node, and a UA response has been sent.
4. A DM response to a transmitted DISC command is received from the remote node.
5. The TI timer expires when in the Disconnecting state.

This state is exited to the Opening state when the attached system issues a CONNECT.STATION command, or when a SABME is received; the state is exited to the Closed state when the attached system issues a CLOSE.STATION command.

Disconnecting. This state is entered when:

1. The attached system issues a CLOSE.STATION command, and a DISC command has been transmitted.
2. The remote node has responded to transmitted I frames but has not accepted them, and the retry counts have been exceeded.

This state is exited to the Disconnected state if TI expires or a response has been received to the transmitted DISC command.

Opening. This state is entered when the attached system issues a CONNECT.STATION command, and the adapter has either transmitted an SABME or a UA response to an SABME from the remote node. This state is exited to Opened when an I Frame or RR response is received from the remote node. Since I Frames can be transmitted only in the Opened state, the two adapters in the Opening state will exchange a pair of RR frames before I Frame transmission begins.

Resetting. This state is entered when the adapter receives a SABME frame for an opened link station. This state is exited to the Opening state when a response to the SABME is transmitted. Exit is to the Disconnected state when a CLOSE.STATION command is issued, or a DISC command or DM response is received.

Frame Reject Sent. This state is entered when an illegal frame has been received and a FRMR frame has been sent. This state is exited to the Opening state if an SABME is received. It is exited to the Disconnecting state if TI expires, or if the attached system issues a CLOSE.STATION command. Exit is to the Disconnected state if a DISC command or DM response is received.

Frame Reject Received. This state is entered when a FRMR frame has been received in response to a sent I Frame. This state is exited to the Opening state if an SABME is received. It is exited to the Disconnecting state if TI expires or if the attached system issues a CLOSE.STATION command. Exit is to the Disconnected state if a DISC command or DM response is received.

Opened. This state is entered when the SABME/UA sequence is completed after the attached system issues a CONNECT.STATION command. This is the only state in which data transfer can occur. When in the Opened state, a link station may be in any of seven secondary states. If it is in any of these secondary states, then I Frame transmission is temporarily suspended.

Checkpointing. The Checkpointing state is entered due to a period of inactivity in the link station. When this state is entered, an RR command (or RNR if in local busy) with the poll bit set to one is transmitted. The adapter waits to receive an RR (or RNR) response with the final bit set to one before resuming I Frame transmission.

Local Busy(user). This state indicates that the attached system on the local node is temporarily unable to receive frames. This state is entered when a FLOW.CONTROL command with local_busy_status = 0 option is issued by the attached system.

Local Busy(buffer). This state indicates that the attached system on the local node is temporarily unable to receive frames. This state is entered when a frame has been canceled by the attached system, indicating that the SAP is out of buffers.

Remote Busy. This state indicates that the remote node of a link station is temporarily unable to receive frames. This condition is indicated by the receipt of an RNR frame from the remote station. This state will be exited when an RR frame is received from the remote node.

Rejection. An REJ frame has been sent to the remote station. This state is cleared when the requested I Frame is received.

Clearing. This state is entered when a local busy condition is cleared, yet the link is in a checkpointing state and so cannot inform the remote station of the cleared local busy condition. As soon as the response is received removing the station from the checkpointing state, the remote station will be notified of the local busy clear condition.

Dynamic Window. The station is processing the Dynamic Window algorithm. This occurs when the remote station is on another ring and there is congestion in the bridge.

2.1.6 LLC Parameters

In order to understand the programming interface to LLC, the user should be familiar with some of the operational parameters of LLC. The following section describes those parameters. For further information on the LLC parameters, the user should refer to the *IBM Token-Ring Architecture Reference* (IBM, 1986), the *IBM Token-Ring PC Adapter Technical Reference* (IBM, 1986), and the IEEE/ANSI Standard 802.2-1985.

2.1.6.1 Timers

The LLC protocols make use of three timers:

- The Response Timer, T1
- The Acknowledgment Timer, T2
- The Inactivity Timer, TI.

The T1 timer is started by a link station whenever an I Frame is transmitted. If the timer expires before an acknowledgment to the I Frame is received, then the station enters a checkpointing state and transmits an RR frame (or RNR frame) with the poll bit set to 1. The T1 timer should be set greater than the expected delay of the network in order to avoid unnecessary polls. Normal setting for the T1 timer is 1-2 seconds.

The T2 timer is started by a link station whenever an I Frame is received and the maximum number of I Frames that can be received (N3) has not been reached. If this timer expires before N3 has been reached, then an acknowledgment is sent to the transmitting station. The value of T2 must be less than the value of T1. Normal values for T2 are 80-256 milliseconds.

The TI timer is running whenever T1 is not running. If TI expires, the checkpointing state is entered, and an RR frame (or RNR frame) is sent to the remote station with the poll bit set to 1. This solicits a response from the remote station, and ensures that the link is still active. The TI timer should be 5-10 times greater than T1. Normal values for the TI timer are 5-20 seconds.

When timers are set at the software interface, the timer value is selected in increments of a "tick count". The tick counts are set by the OPEN.ADAPTER command. The tick counts themselves are numbers of 40-millisecond intervals. See the section on OPEN.ADAPTER command for further details. When selecting a timer value, the attached system selects a number of tick counts. The timer value parameters are a number between 1 and 10. If a number between 1 and 5 is selected, the number is multiplied by the short tick count and by 40 milliseconds to achieve the timer value. If a number between 6 and 10 is selected, the number minus 5 is multiplied by the long tick count and by 40 milliseconds to reach the timer value. For example, if in the OPEN.ADAPTER command, the attached system sets the TIMER__T1__2 parameter to 25, and the TIMER__T1 parameter in the OPEN.SAP command to 10, then the value of the T1 timer is:

$$(10\text{-}5) \times 25 \times 40 = 5 \text{ seconds.}$$

2.1.6.2 Numbers

The LLC protocols use six number parameters, mostly used as counters. These parameters are:

- The Maximum I frame length, N1
- The Maximum number of retransmissions, N2
- The Maximum number of received I frames, N3
- The Maximum number of outstanding I frames, Tw
- The Working Window, Ww
- The Window increment, Nw.

The Maximum Length of an I Frame (N1) is the maximum frame size of I Frames for a given SAP. This value is set when the SAP is opened. By using this value, upper layer protocols can determine the maximum frame size on a link.

The Maximum Number of Retransmissions (N2) defines the maximum number of times an adapter will try the checkpointing poll when T1 expires. If the N2 count is exceeded without a successful poll, then the link is closed. This parameter is set in the OPEN.SAP and OPEN.STATION commands. Normal values for N2 will be less than 10.

The Maximum Number of Received I Frames (N3) is the number of I Frames that a link station can receive without transmitting a response. This number must always be less than or equal to the Tw value. This number should be set low enough, so that the adapter has enough receive buffers to hold all received frames.

The Maximum number of outstanding I Frames (Tw) is the number of I Frames that a link station can transmit without receiving an acknowledgment. This number should be set so that the receiving adapter can hold all the transmitted I Frames in its buffers, to avoid unnecessary retransmissions. This number should always be greater than or equal to the N3 value.

The Working window (Ww) and Window increment (Nw) are two counts associated with the dynamic windowing algorithm. The dynamic windowing algorithm alters the maximum number of outstanding I Frames when congestion on a network is detected. When congestion is detected, the maximum number of outstanding I Frames value, held temporarily in the working window (Ww), is set to one. As conditions improve, the Ww is incremented each time Nw frames are acknowledged. When Ww is equal to Tw, the dynamic windowing state is exited.

2.2 System Memory Requirements

The integration of the adapter into an attached system requires that several system memory buffers be allocated and reserved for adapter use. All data buffers created by the attached system must be aligned on a word (even address) boundary. The following data structures listed below are those that must be created by the attached system.

- System Command Block
- System Status Block
- Frame Buffers
- Command Parameter Blocks
- Transmit Parameter List
- Receive Parameter List
- Product ID Block

Note:
When in 808X mode, care must be excercised in maintaining the proper orientation of bytes which are DMA read by the adapter as parameters. When these parameters are manipulated as words, the user must ensure that the byte order in memory is that order desired in the adapter. The byte-swapping hardware, enabled when in 808X mode, will maintain proper orientation of character string data types.

2.2.1 System Command Block

The attached system issues a command to the adapter by loading the request in the System Control Block (SCB) and interrupting the adapter. The adapter will then download the command (and any required parameters) through the System Interface DMA channel. This interrupt may be used as an indication that the SCB is available for additional commands. The SCB is six bytes in length and the adapter will always DMA read six bytes. The SCB format is shown in Figure 2-5.

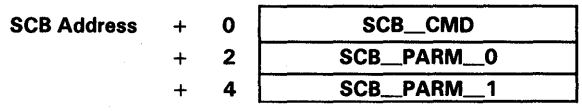


Figure 2-5. System Command Block Format

The SCB_CMD field contains the 16-bit command code request to the adapter. The SCB_PARM_0 and SCB_PARM_1 fields are used to hold command dependent parameters. Usually, SCB_PARM_0 and SCB_PARM_1 are used as a 32-bit address field containing a 24-bit pointer to a Command Parameter Block. In this case the high-order byte of this field is read but ignored. Some commands do not have additional parameters and only the 16-bit command code must be written.

The attached system initiates an adapter command by following the sequence shown below:

1. The attached system writes the command request code into SCB_CMD and any necessary parameters to SCB_PARM_0 and SCB_PARM_1.
2. The attached system writes to the adapter's Interrupt Register and sets the INTERRUPT_ADAPTER, EXECUTE, and SYSTEM_INTERRUPT bits to one. Bit 8 (SYSTEM_INTERRUPT) should be set to one so that incoming interrupts from the adapter are not accidentally reset.

This sequence will cause an interrupt internal to the adapter. The adapter will DMA read the SCB and, if specified, the Command Parameter Block. Once the SCB is downloaded, the adapter will write a zero to the SCB_CMD field. This may be used as an indication that the command has been recognized and the attached system may write to the SCB. If the SCB_REQUEST bit (bit 4) of the adapter Interrupt Register is set to one, an adapter-to-system interrupt will be posted after the parameters are read into the adapter. In most cases, this interrupt will occur on command completion. The attached system is responsible for clearing this interrupt by writing a zero to the SYSTEM_INTERRUPT bit (bit 8) of the adapter Interrupt Register.

There may not be more than one Transmit or Receive command executed at one time. Multiple CONNECT.STATION or CLOSE.STATION commands may be executing. One other command may be executing while these commands are active. Thus the adapter can support a TRANSMIT command, a RECEIVE command, multiple CLOSE.STATION commands, multiple CONNECT.STATION commands, and one other command, simultaneously.

2.2.2 System Status Block

When the status of any command is to be returned to the attached system, the adapter will DMA write this information to the System Status Block (SSB). An interrupt will then be posted (if enabled). After the attached system has read the SSB, the adapter must be notified that the SSB is clear and available for additional status posting. This is done by writing a one to the INTERRUPT_ADAPTER (bit 0) and the SSB_CLEAR bit (bit 2) of the adapter's Interrupt Register. The SSB is eight bytes in length and the adapter will always DMA write the entire eight bytes regardless of the actual length of the returned status. The SSB format is defined in Figure 2-6.

SSB Address	+		
	+	0	SSB_CMD
	+	2	SSB_PARM_0
	+	4	SSB_PARM_1
	+	6	SSB_PARM_2

Figure 2-6. System Status Block Format

The SSB_CMD field contains a 16-bit code which reflects the status type being returned. Valid status types which may be returned to the SSB are RING_STATUS, COMMAND_REJ_STATUS, COMMAND_STATUS, XMIT_STATUS, or RCV_STATUS. The command status field will be written to SSB_PARM_0. The bit field definitions for the different status types may be found in the descriptions of the following interrupts and commands: RING.STATUS, COMMAND.STATUS, COMMAND.REJECT, TRANSMIT, and RECEIVE.

2.2.3 Frame Buffers

The attached system must allocate a portion of its memory for frame buffering. The amount of memory allocated will vary according to the application. All frames, except LLC Type 2 I-frames, are constructed according to the Logical Frame Format defined in Figure 2-7. I-frames consist of only the DATA field, the adapter is responsible for attaching the LAN header. Table 2-1 summarizes the data that the attached system must provide to the adapter for various frame types.

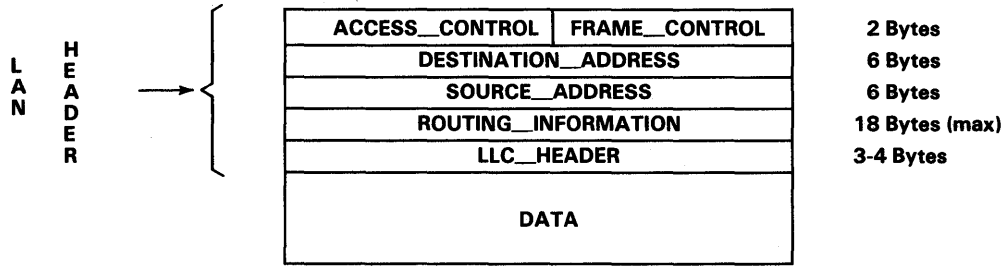


Figure 2-7. Attached System Logical Frame Format

Attached System Frame Fields.

ACCESS_CONTROL: This control field consists of the following bit functions:

BITS 0-2 (ACCESS_PRIORITY) - Selects the Access Priority for the frame. This value (0-7) must be less than or equal to the Authorized Access Priority. The adapter's Authorized Access Priority is 6 unless modified by network management.

BITS 3-7 (RESERVED) - These should be set to zero.

For all type 1 frames, the adapter will fill in the correct value for the AC byte, though the attached system must leave space for the AC in the MAC header.

FRAME_CONTROL: This 8-bit field is defined in Chapter 3 of the *TMS380 Adapter Chipset User's Guide*. If the MAC Indicator bit is set to zero, the Authorized Function Class parameter is used to validate the Major Vector Source Class. MAC frames must be sent through the direct station. For all type 1 frames, the adapter will fill in the correct value for the FC byte, though the attached system must leave space for the FC in the MAC header.

DESTINATION_ADDRESS: This field is 48 bits wide and contains the address of the destination. The address format for this field is defined in Chapter 3 of the *TMS380 Adapter Chipset User's Guide*.

SOURCE_ADDRESS: Unless the PASS_SOURCE_ADDRESS option is selected, the Adapter will store the Node Address into the six bytes of the SOURCE_ADDRESS with the exception of byte 0 bit 0 (the Routing Information Indicator). The Node Address is that address supplied by the Burned-in Address (BIA) or passed during the OPEN command.

ROUTING_INFORMATION: This field must be included if bit 0 of SOURCE_ADDRESS is set to one. The format of the ROUTING_INFORMATION is described in Section 7 of this book.

LLC_HEADER: This field consists of the DSAP, SSAP, and LLC Control fields as described earlier in this section. This field is provided by the adapter, and is not present in direct frames. Space does not need to be provided for this header in attached system memory.

DATA: The Data portion of the frame is transmitted as specified by the attached system. The CRC, Ending Delimiter, and Frame Status (FS) are appended to the data by the Adapter. Note that if the attached system selects the TRANSMIT_CRC option, then the CRC must be included at the end of the DATA field and not appended by the adapter. See the section on TRANSMIT for more information.

Table 2-1. Transmit Data

FRAME TYPE	MAC HEADER SUPPLIED BY	LLC HEADER SUPPLIED BY	DATA FIELD SUPPLIED BY
Direct Frame	Attached System	not used	Attached System
UI Frame	Attached System	Adapter (note 1)	Attached System
XID Command	Attached System	Adapter (note 1)	Attached System or Adapter (note 2)
XID Response Final	Attached System	Adapter (note 1)	Attached System
XID Response Not Final	Attached System	Adapter (note 1)	Attached System
TEST Command	Attached System	Adapter (note 1)	Attached System (optional)
I Frame	Adapter (note 3)	Adapter (note 3)	Attached System

NOTES:
1. The adapter constructs the LLC header information from the STATION_ID parameter and the REMOTE_SAP parameter in the transmit list.
2. If the XID_HANDLER bit in the OPEN.SAP command parameters list was set, the attached system must provide the XID data field. If this bit was not set, the adapter will write over the first three bytes of the data field provided by the attached system. The attached system should take care to save these three bytes of space for the adapter.
3. I Frames may not be transmitted until the attached system has issued a CONNECT.STATION command. The adapter constructs the MAC and LLC headers from information provided in the OPEN.STATION and CONNECT.STATION commands.

2.2.4 Command Parameter Block

Certain commands (e.g., the OPEN command) require that a block of memory be designated as a parameter block. This block of memory will be DMA read into adapter memory after the SCB has been read. Once the command has completed execution, this buffer may be released for other uses. The Command Parameter Block definitions are listed with the command descriptions later in this section.

2.2.5 Transmit Parameter List

The TRANSMIT command requires that Transmit Parameter List(s) be allocated within attached system memory. The amount of memory allocated is dependent upon the size and number of lists used in the application. The size of a Transmit List may be selected upon adapter initialization to be either 14, 20, or 26 bytes in length. The adapter automatically adds four bytes to these values for a start-of- frame list when using the LLC interface. This is to accommodate the extra LLC transmit parameters. The Transmit Parameter List is defined in the TRANSMIT command discussion.

2.2.6 Receive Parameter List

The RECEIVE command requires that Receive Parameter List(s) be allocated within system memory. The memory allocation size is dependent upon the size and number of lists used in the application. The size of a receive list may be selected upon adapter initialization to be either 14, 20, or 26 bytes in length. The Receive Parameter List is defined in the RECEIVE command discussion.

2.2.7 Product ID Block

The OPEN command requires a pointer to an 18-byte Product Identification block as part of the open parameters. The system software designer should reserve 18 bytes of system memory for this function. This Product ID is described further in IBM's *Token-Ring Network PC Adapter Technical Reference* (IBM, 1986).

2.3 Adapter Memory

The adapter contains some amount of memory on its own bus. This memory varies with the application, and is defined by the DATA_RAM_START_ADDRESS and DATA_RAM_END_ADDRESS parameters of the OPEN.ADAPTER command. The amount of RAM on the adapter bus determines the number of SAPs and link stations and the values of N3 and Tw that the adapter can support.

The adapter RAM is configured at the time of the OPEN.ADAPTER command. The following blocks are defined.

1. SAP Control Blocks. These blocks require 52 bytes of memory each. The number reserved is set by the MAX_SAPS parameter of the OPEN.ADAPTER command.
2. Group SAP Control Blocks. These blocks require 2 bytes, plus 2 bytes times the MAX_MEMBERS parameter.
3. Link Station Control Blocks. These blocks require 176 bytes each. The number is set by the MAX_STATIONS parameter.

The remaining RAM is configured for receive and transmit buffers. The number of transmit buffers is manipulated by the TRANSMIT_MIN_COUNT and TRANSMIT_MAX_COUNT parameters.

When a link station is opened, the adapter expects to have enough transmit buffers to be able to hold I Frames, up to the Transmit Window (set by the MAXOUT parameter in the OPEN.SAP or OPEN.STATION command). The attached system must assure that there is ample RAM space for these frames.

The adapter's workspace is contained in Communications Processor RAM, and is therefore not a part of the DATA_RAM as defined by the user.

2.4 Register Descriptions

The System Interface (SIF) contains four registers used for communication with the attached system. This section will describe in detail the functions performed by these registers.

2.4.1 SIF Interrupt Register

The SIF Interrupt Register is used to post interrupts to the adapter and to read interrupt status information from the adapter. The function performed by each bit of the Interrupt Register depends on whether a bit is read or written by the attached system. Bits 0-7 can be set to one but not reset to zero by the attached system. These bits can be cleared only by the Communications Processor. Likewise, bit 8 can be reset to zero only by the attached system and can be set to one only by the Communications Processor. Bits 9-15 can be read only by the attached system. These bits are set or reset by the Communications Processor.

2.4.1.1 Writing to the Interrupt Register

A direct I/O (DIO) write to the most significant bit of the Interrupt Register will cause an interrupt to the adapter. Bits 1-7 provide an interrupt reason code to the adapter. A write of zero to bit 8 will reset the adapter-to-system interrupt level on the SINTR/SIRQ pin.

Figure 2-8 shows the bit assignments of the SIF Interrupt Register. Table 2-2 defines the functions of each bit when written by the attached system. Table 2-3 defines the functions of each bit when read by the attached system.

BIT	
0	INTERRUPT_ADAPTER
1	ADAPTER_RESET
2	SSB_CLEAR
3	EXECUTE
4	SCB_REQUEST
5	RECEIVE_CANCEL
6	RECEIVE_VALID
7	TRANSMIT_VALID
8	SYSTEM_INTERRUPT
9	INITIALIZE
10	TEST
11	ERROR
12	INTERRUPT_CODE
13	INTERRUPT_CODE
14	INTERRUPT_CODE
15	INTERRUPT_CODE

Figure 2-8. SIF Interrupt Register

Table 2-2. Interrupt Register Write Bit Functions

BIT 0	(INTERRUPT_ADAPTER) - Bit 0, when set to one, will cause an internal adapter interrupt. This bit has no effect when set to zero. This bit will be cleared by the adapter after the adapter responds to the interrupt. The purpose of the interrupt is defined by the ADAPTER_RESET, SSB_CLEAR, EXECUTE, SCB_REQUEST, RECEIVE_CANCEL, RECEIVE_VALID, and TRANSMIT_VALID bits described below.
BIT 1	(ADAPTER_RESET) - Setting bit 1 to one forces an adapter reset if bits 2-7 are also set to one. Following an adapter reset, the initialization procedure outlined in Section 2.5 should be followed. This reset function is a software command and certain conditions of hardware failure may prevent its execution.
BIT 2	(SSB_CLEAR) - This interrupt request is used by the system to notify the adapter that the System Status Block (SSB) is available for the adapter to post additional status information.
BIT 3	(EXECUTE) - This interrupt is used to initiate an adapter command contained in the System Command Block (SCB). This block will be DMA read and executed by the adapter.
BIT 4	(SCB_REQUEST) - This interrupt is used to request the adapter to interrupt the attached system when the SCB is available for another command. The adapter will return the SCB.CLEAR interrupt code.
BIT 5	(RECEIVE_CANCEL) - This interrupt discards remaining data on the frame currently being transferred to the attached system. This interrupt is accepted only when the receive is in a halted state. If the LLC Interface is not enabled (Bit 9 of the Initializations Options is set to zero), then this bit has the meaning of RECEIVE_CONTINUE as described in Chapter 3 of the *TMS380 Adapter Chipset User's Guide*.
BIT 6	(RECEIVE_VALID) - This interrupt request signals the adapter that the condition causing list processing suspension (odd forward pointer or invalid list) during receive has been cleared.
BIT 7	(TRANSMIT_VALID) - This interrupt request signals the adapter that the condition causing list processing suspension during transmit has been cleared.
BIT 8	(SYSTEM_INTERRUPT) - Writing a zero to bit 8 resets the adapter-to-attached-system interrupt (i.e., clears the SINTR/$\overline{\text{SIRQ}}$ line). Writing a one to this bit has no effect. See section 2.5.1 to determine correct use of this bit.
BITS 9-15	(RESERVED) - These bits cannot be written by the attached system.

2.4.1.2 Reading from the Interrupt Register

A direct I/O (DIO) read of the Interrupt Register will transfer a 16-bit word, which is used to examine status of the adapter.

Table 2-3. Interrupt Register Read Bit Functions

BIT 0	(INTERRUPT_ADAPTER) - Bit 0 reflects the current state of the system-to-adapter interrupt.
BIT 1	(ADAPTER_RESET) - Bit 1 reflects the current state of the ADAPTER_RESET bit.
BIT 2	(SSB_CLEAR) - Bit 2 reflects the current state of the SSB_CLEAR bit.
BIT 3	(EXECUTE) - Bit 3 reflects the current state of the EXECUTE bit.
BIT 4	(SCB_REQUEST) - Bit 4 reflects the current state of the SCB_REQUEST bit.
BIT 5	(RECEIVE_CANCEL) - Bit 5 reflects the current state of the RECEIVE_CANCEL bit. If the LLC Interface is not enabled, this bit reflects the state of the RECEIVE_CONTINUE bit.
BIT 6	(RECEIVE_VALID) - Bit 6 reflects the current state of the RECEIVE_VALID bit.
BIT 7	(TRANSMIT_VALID) - Bit 7 reflects the current state of the TRANSMIT_VALID bit.
BIT 8	(SYSTEM_INTERRUPT) - Bit 8 is set to one if the adapter-to-attached-system interrupt is valid. In systems not implementing hardware interrupt control, this bit may be polled under software control. The adapter cannot reset this bit to zero. This must be done by the attached system writing a zero to this bit location.
BIT 9	(INITIALIZE) - Bit 9 is set to one when the bring-up diagnostics have completed and the adapter is ready to start the initialization process. This bit is cleared to zero when the initialization process is complete.
BIT 10	(TEST) - Bit 10 is set to one by the bring-up diagnostics following an adapter reset. This bit is cleared when the bring-up diagnostics complete successfully.
BIT 11	(ERROR) - Bit 11 is set if the bring-up diagnostics detect an error or if there is an error during the initialization process. The error condition is specified in bits 12 through 15. The error codes are detailed in Section 2.7.
BITS 12-15	(INTERRUPT_CODE) - Bits 12-15 define the adapter-to-attached-system interrupt reason code. Bits 12-15 are also used to indicate the error code resulting from the execution of bring-up diagnostics or the initialization process. These codes will be defined in the sections that discuss the bring-up operation. The valid 4-bit interrupt codes are shown below: 0000 (ADAPTER CHECK) - This interrupt code is used when the adapter has encountered an unrecoverable hardware or software error. 0100 (RING STATUS) - This interrupt code will be used if the SSB is updated with Ring Status. 0101 (LLC STATUS) - This interrupt code will be used if the status of the adapter's LLC has been changed. The status code can be read from the Interface Control Block (ICB). 0110 (SCB CLEAR) - This interrupt code will be used following a SCB.REQUEST interrupt when the SCB is clear. 0111 (TIMER) - This interrupt will be generated at regular intervals set by the attached system using the TIMER_SET command.

Table 2-3. Interrupt Register Read Bit Functions (Concluded)

1000	(COMMAND STATUS) - This interrupt code will be used when the SSB is updated with COMMAND_STATUS for commands other than TRANSMIT and RECEIVE. This includes COMMAND_REJECT.
1010	(RECEIVE STATUS) - This interrupt code will be used if the SSB is updated with RCV_STATUS.
1100	(TRANSMIT STATUS) - This interrupt code will be used if the SSB is updated with XMIT_STATUS.
1110	(RECEIVE PENDING) - This interrupt code will be used to indicate that a frame is ready to be transferred across the system interface, and that the ICB has been updated with destination information.

Bits 9-15 are set or reset only by the adapter. The attached system cannot set or reset these bits; these bits can only be read by the attached system.

2.4.2 SIF Address Register

The SIF Address register contains the address pointer for internal adapter RAM accesses via the Data or Data/Auto increment registers. All 16 bits of the Address register can be read, although only bits 5-14 can be written by the attached system. This allows the attached system to access a 2K-byte block of the adapter's RAM. The actual starting location of RAM that can be read is determined by how the adapter sets bits 0-4. During reset and BUD code execution, bits 0-4 will be set to b'00000'. After BUD code, these bits are set to b'00001'. Bit 15 is controlled by the adapter as all data transfers on the adapter bus are by 16-bit words only.

2.4.3 Data Register

The Data Register is the "port" into the adapter's RAM through which data may be read or written. The RAM locations read or written through this register are pointed to by the SIF Address Register.

This DIO capability allows initialization parameters to be passed to the adapter. This capability is also used to get quick information from the adapter, and may in some cases diagnose adapter failure.

After the bring-up diagnostics, only the address range >0800 through >0FFF may be accessed through the Data Register.

2.4.4 Data Register with Auto-Increment

This register is identical to the Data Register except that the address contained in the Address Register is automatically incremented following a read or write to this register. For eight-bit operation, note that the Address Register contents are incremented after a write to the most significant byte of this register. This allows adapter RAM to be read or written to sequentially without re-writing the Address Register pointer between each access. If the Address register attempts to increment past >0FFF, the address will reset to >0800.

2.5 Adapter To System Interrupts

This section describes the interrupts that may be posted to the attached system by the adapter. The RECEIVE.PENDING and LLC.STATUS interrupts are enabled only when the LLC Interface has been enabled. A list of all available interrupts follows.

- RING.STATUS
- ADAPTER.CHECK
- TRANSMIT.STATUS
- RECEIVE.PENDING
- SCB.CLEAR
- COMMAND.REJECT
- RECEIVE.STATUS
- COMMAND.STATUS
- LLC.STATUS
- TIMER

2.5.1 Interrupt Handling

This section is intended to give the programmer some ideas of handling interrupts from the adapter. After an adapter-to-attached-system interrupt, the adapter must be re-enabled in two ways for further interrupts. The SYSTEM_INTERRUPT bit (bit 8) of the SIF Interrupt register should be cleared. This re-enables the System Interface hardware for interrupts. Secondly, the adapter should be interrupted with the INTERRUPT_ADAPTER (bit 0) and the SSB_CLEAR bit (bit 2) of the Interrupt register set to one. Issuing the SSB_CLEAR interrupt to the adapter indicates to the adapter's controlling software that the attached system is ready for another interrupt. When the SYSTEM_INTERRUPT bit has been cleared but an SSB_CLEAR has not been issued, the adapter will interrupt the system only for DMA. All other interrupts, even those which do not write to the SSB, will be held until the attached system issues an SSB_CLEAR interrupt.

When programming the adapter, consider the following in decisions involving enabling adapter interrupts.

1. DMA interrupts should be enabled (by clearing the SYSTEM_INTERRUPT bit) as soon as possible after entering the interrupt handling routine.
2. When the interrupt in progress uses the Interface Control Block (RECEIVE.PENDING or LLC.STATUS), the SSB_CLEAR interrupt should not be issued until the contents of the ICB are read and stored. Otherwise information may be lost.
3. For those interrupts which use the SSB (RING.STATUS, TRANSMIT.STATUS, COMMAND.REJECT, RECEIVE.STATUS, and COMMAND.STATUS). The SSB_CLEAR interrupt should not be issued until the contents of the SSB are read and stored.

2.5.2 RING.STATUS

The SSB is loaded with RING.STATUS and an interrupt posted to the attached system when any of the following conditions occur:

1. The adapter detects a signal loss on the ring.
2. The adapter is transmitting or receiving beacon frames to/from the ring. This interrupt condition may be disabled by setting bit 1 of the OPEN command options to one.
3. The adapter transmits a Report Error MAC Frame. This interrupt error condition can be disabled by setting bit 2 of the OPEN command options to one.
4. An open or short circuit fault is detected by the adapter.
5. The adapter receives a Remove MAC frame request.

6. One of the adapter's error counters has incremented from 254 to 255.
7. The adapter has been opened and is the only station on the ring.

Due to the dynamic nature of the report indications and the possibility that the ring status could change before the system can respond to a previous RING.STATUS interrupt, the current ring status could possibly equal the last ring status report. No RING.STATUS interrupts will occur until the adapter has been opened.

SSB_CMD	>0001
SSB_PARM_0	RING_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

SIF_INT		...			0	1	0	0
bit	0		10	11	12	13	14	15

RING_STATUS Field Bit Functions.

BIT 0 (SIGNAL_LOSS): When set to one, indicates that the Adapter has detected a loss of signal on the ring.

BIT 1 (HARD_ERROR): When set to one, indicates that the Adapter is presently transmitting or receiving beacon frames to or from the ring. If bit 1 of the OPEN_OPTIONS is set to one, this bit will never be set.

BIT 2 (SOFT_ERROR): When set to one, indicates that the Adapter has transmitted a Report Error MAC frame. If bit 2 of the OPEN_OPTIONS is set to one, this bit will never be set.

BIT 3 (TRANSMIT_BEACON): When set to one, indicates that the Adapter is transmitting beacon frames to the ring. If bit 1 of the OPEN_OPTIONS is set to one, this bit will never be set.

BIT 4 (LOBE_WIRE_FAULT): When set to one, indicates that the Adapter has detected an open or short circuit in the cable between the adapter and the wiring concentrator. The adapter will be closed and at the state following adapter initialization.

BIT 5 (AUTO_REMOVAL_ERROR): When set to one, indicates that the adapter has detected an internal hardware error following the Beacon Auto-removal process and has de-inserted from the ring. The adapter will be closed and will remain at the state following adapter initialization.

BIT 6 (RESERVED): This bit is undefined.

BIT 7 (REMOVE_RECEIVED): When set to one, indicates that the adapter has received a Remove Ring Station MAC frame request, and has de-inserted from the ring. The adapter will be closed and will remain at the state following adapter initialization.

BIT 8 COUNTER_OVERFLOW): When set to one, indicates that the one of the adapter's error counters has incremented from 254 to 255. The attached system should use the READ.ERROR.LOG command to determine which counter has overflowed.

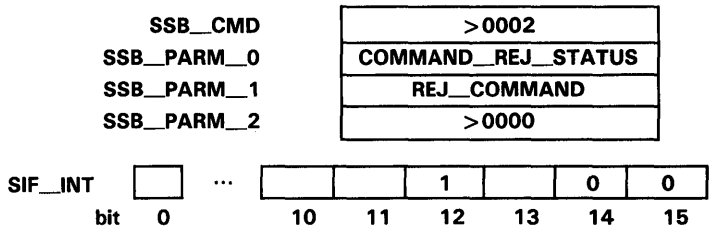
BIT 9 (SINGLE_STATION): When set to one, indicates that the Adapter has sensed that it is the only station on the ring. This bit will be reset to zero when another station inserts into the ring.

BIT 10 (RING RECOVERY): This bit is set to one when the adapter observes Claim Token MAC frames on the ring. The adapter may be transmitting the Claim Token frames. This bit will be reset when a Ring Purge frame is received or transmitted.

BITS 11-15 (RESERVED): Will be set to zero.

2.5.3 COMMAND.REJECT

The SSB will be loaded with COMMAND_REJECT_STATUS if an SCB is passed to the adapter with an error in SCB_CMD or SCB_PARM_0/1. The adapter will set SSB_CMD to >0002 and SSB_PARM_1 with the SCB_CMD field of the offending SCB. The bit positions within the COMMAND_REJ_STATUS indicate the error which caused the adapter to interrupt.



COMMAND_REJ_STATUS Field Bit Functions.

BIT 0 (ILLEGAL_COMMAND): Set to one when an unknown command is issued to the adapter. This bit will be set when commands that are valid only when the LLC Interface is enabled are issued and the LLC Interface is not enabled.

BIT 1 (ADDRESS_ERROR): Set to one if any address field in the SCB is odd (not word-aligned).

BIT 2 (ADAPTER_OPEN): Set to one if a command is issued when an adapter is open and the command is honored only when the adapter is closed.

BIT 3 (ADAPTER_CLOSED): Set to one if a command is issued when the adapter is closed and the command is honored only when the adapter is open.

BIT 4 (SAME_COMMAND): Set to one if a command is issued and the same command is already executing.

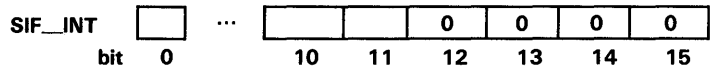
BITS 5-15 (RESERVED): These bits will be set to zero.

2.5.4 ADAPTER.CHECK

The ADAPTER.CHECK Interrupt is generated when the adapter has encountered an unrecoverable hardware or software error. The SSB is not altered when the ADAPTER.CHECK Interrupt is generated. The Adapter is in a closed state waiting to be reset.

ADAPTER.CHECK information can be obtained by writing >05E0 to the Address Register and then reading the ADAPTER_CHECK_BLOCK (8 bytes) through the Data/Auto-increment register.

ADAPTER_CHECK_BLOCK		
>05E0	ADAPTER_CHECK_STATUS	
>05E2	ADAPTER_CHECK_PARM_0	
>05E4	ADAPTER_CHECK_PARM_1	
>05E6	ADAPTER_CHECK_PARM_2	



ADAPTER_CHECK_STATUS Field Bit Definitions.

BIT 0 (DIO_PARITY): Set to one if the adapter detects bad parity on data passed from the attached system to the adapter through a direct I/O access.

BIT 1 (DMA_READ_ABORT): Set to one if the adapter aborts a DMA read operation (from the system). This can be a result of parity errors in excess of the parity abort threshold set during initialization, bus errors in excess of the bus error abort threshold also set during initialization, or if the adapter times out (10 seconds) waiting for the completion of a DMA bus operation (with or without an error). ADAPTER_CHECK_PARM_0 will contain the following information:

>0000 - Indicates a timeout abort.

>0001 - Indicates a parity error abort.

>0002 - Indicates a bus error abort.

ADAPTER_CHECK_PARM_1-2 will contain the failing system address. This address can be within ±6 bytes of the actual failed address.

BIT 2 (DMA_WRITE_ABORT): Set to one if the adapter aborts a DMA write operation (to the system). This can be a result of parity errors in excess of the parity abort threshold set during initialization, bus errors in excess of the bus error abort threshold also set during initialization, or if the adapter times out (10 seconds) waiting for the completion of a DMA bus operation (with or without an error). ADAPTER_CHECK_PARM_0 will contain the following information:

>0000 - Indicates a timeout abort.

>0001 - Indicates a parity error abort.

>0002 - Indicates a bus error abort.

ADAPTER_CHECK_PARM_1-2 will contain the failing system address. This address can be within ±6 bytes of the actual failed address.

BIT 3 (ILLEGAL_OP_CODE): Set to one if the adapter's Communications Processor detects an illegal operation code in the adapter's internal program. ADAPTER_CHECK_PARM_0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.

BITS 4-9 (PARITY_ERRORS): These bits are set to one if the adapter detects a bus parity error on the adapter's internal bus. The specific bit set to one (bits 4-9) depends upon the source of the error. A description of bits 4-9 and the parity error causing the bits to be set to one follows:

BIT 4 Set to one if the Communications Processor detects the adapter bus parity error. ADAPTER_CHECK_PARM_0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.

BIT 5 Reserved. This bit will not be set.

BIT 6 Set to one if the SIF detects the adapter bus parity error. ADAPTER_CHECK_PARM_0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.

BIT 7 Set to one if the PH detects the adapter bus parity error. ADAPTER_CHECK_PARM_0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.

BIT 8 Set to one if the parity error occurred when the adapter was copying a frame from the ring. ADAPTER_CHECK_PARM_0 will contain the buffer address.

BIT 9 Set to one if the parity error occurred when the adapter was transmitting onto the ring. ADAPTER_CHECK_PARM_0 will contain the buffer address.

BIT 10 (RING_UNDERRUN): Set to one if the adapter detects an internal DMA underrun when transmitting onto the ring.

BIT 11 (RING_OVERRUN): Set to one if the adapter detects an internal DMA overrun when receiving from the ring.

BIT 12 (INVALID_INTERRUPT): Set to one if an unrecognized interrupt was generated internal to the adapter. ADAPTER_CHECK_PARM_0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.

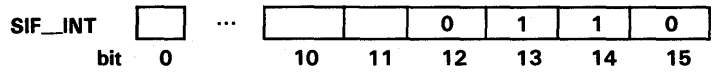
BIT 13 (INVALID_ERROR_INTERRUPT): Set to one if an unrecognized error interrupt was generated. ADAPTER_CHECK_PARM_0-2 will contain adapter registers R13, R14, and R15, respectively.

BIT 14 (INVALID_XOP): Set to one if an unrecognized XOP request was generated in the Communications Processor's code. ADAPTER_CHECK_PARM_0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.

BIT 15 (RESERVED): The value of this bit position is undefined.

2.5.5 SCB.CLEAR

This interrupt is used to signal that the SCB is clear following the initiation of a command. This interrupt is generated only when the SCB_REQUEST bit of the SIF INTERRUPT register is set to one upon execution of the command.



2.5.6 RECEIVE.STATUS

The RECEIVE.STATUS interrupt is used by the adapter if the SSB is updated with RECEIVE_STATUS. The RECEIVE_STATUS field bit definitions are listed with the RECEIVE command in Section 2.32. SSB_PARM_1/SSB_PARM_2 will contain the address of the receive parameter list to which the status pertains.

SSB_CMD	>0006
SSB_PARM_0	RECEIVE_STATUS
SSB_PARM_1	RCV_PARM_LIST (high)
SSB_PARM_2	RCV_PARM_LIST (low)

SIF_INT		...			1	0	1	0
bit	0		10	11	12	13	14	15

2.5.7 TRANSMIT.STATUS

The TRANSMIT.STATUS interrupt will be used by the adapter if the SSB is updated with XMIT_STATUS. The XMIT_STATUS field bit definitions are listed with the TRANSMIT command in Section 2.30. SSB_PARM_1/SSB_PARM_2 will contain the address of the transmit parameter list to which the status pertains.

SSB_CMD	>0004
SSB_PARM_0	XMIT_STATUS
SSB_PARM_1	LIST_ADDRESS (HI)
SSB_PARM_2	LIST_ADDRESS (LO)

SIF_INT		...			1	1	0	0
bit	0		10	11	12	13	14	15

2.5.8 COMMAND.STATUS

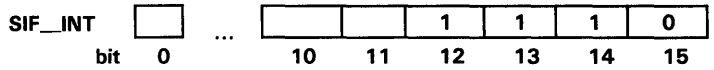
This interrupt is used to signal that the SSB has been updated with COMMAND.STATUS for commands other than TRANSMIT or RECEIVE. The SSB_CMD field reflects the command whose status is being returned. The STATION_ID is present only if the status of LLC interface commands is being returned. The COMMAND_STATUS field in the SSB varies with commands, and is defined in the sections with each command, for that command.

SSB_CMD	COMMAND_CODE
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID (optional)
SSB_PARM_2	>0000

SIF_INT		...			1	0	0	0
bit	0		10	11	12	13	14	15

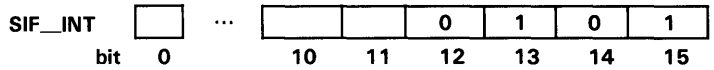
2.5.9 RECEIVE.PENDING

This interrupt is posted by the adapter to indicate that a frame has been received in an internal buffer(s) and is available for transfer to attached system memory. There will be no SSB for this interrupt. Pertinent information will be placed in the Interface Control Block (ICB) before this interrupt is generated. See Section 2.7 for information on the ICB.



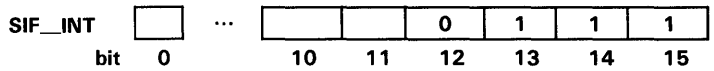
2.5.10 LLC.STATUS

This interrupt is posted by the adapter to indicate that the status of a link station has changed. The nature of the status change may be determined from the LLC_STATUS field written to the Interface Control Block (ICB). There is no SSB for this interrupt. Pertinent information can be obtained from the ICB. The ICB will be updated before this interrupt is generated. See Section 2.7 for information on the ICB.



2.5.11 TIMER

This interrupt is posted by the adapter at regular intervals. This interrupt is enabled when the attached system issues a TIMER.SET command. The time interval is also set by the TIMER.SET command. There is no SSB for this interrupt.



2.6 Interface Control Block

The Interface Control Block (ICB) resides in adapter memory and is read by the attached system via DIO operations. This block contains LLC frame routing and LLC status information for use by the attached system. The ICB exists only if the LLC_ENABLE bit is set to one in the Initialization Options. Portions of this block are updated when RECEIVE.PENDING and LLC.STATUS interrupts are generated. The adapter will update the relevant portion of the ICB before either of these interrupts occurs. The format of the ICB is shown in Figure 2-9.

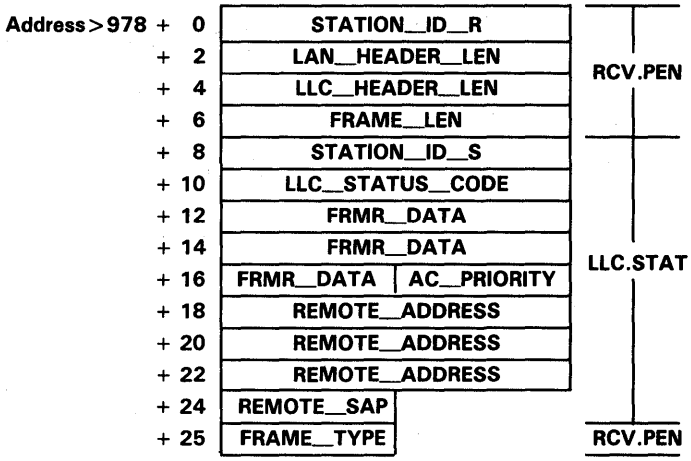


Figure 2-9. Interface Control Block

Interface Control Block Field Definitions.

STATION_ID_R: This field contains the Station ID to which a received frame is destined. This field is updated with a RECEIVE.PENDING interrupt.

LAN_HEADER_LEN: This field contains the length of the MAC header in a received frame. The MAC header includes the AC, FC, DA, SA, and, if present, the routing information fields. This field is updated with a RECEIVE.PENDING interrupt.

LLC_HEADER_LEN: This field contains the length of the LLC header in a received frame. This field is updated with a RECEIVE.PENDING interrupt. The LLC header includes the DSAP, SSAP, and LLC Control fields.

FRAME_LEN: This field contains the length of the entire received frame, including data, LAN header, and LLC header. This count will not include the frame's CRC. If the PASS_CRC option is set for the receive, the attached system must add four bytes to this value to find the frame length. This field is updated with a RECEIVE.PENDING interrupt.

STATION__ID__S: This field contains the Station ID to which an LLC__STATUS__CODE belongs. This field is updated with a LLC.STATUS interrupt.

LLC__STATUS__CODE: This field is used by the adapter to indicate the nature of the LLC status change. This field is updated with a LLC.STATUS interrupt. The bit definitions are as follows:

BIT 0 (LOST__LINK): When set to one, indicates that the link between the adapter and a remote link station has been lost.

BIT 1 (DISC): When set to one, indicates that a Disconnected Mode (DM) or Disconnect (DISC) frame has been received, or that a previously sent DISC frame has been acknowledged by the remote station.

BIT 2 (FRMR__RCVD): When set to one, indicates that the adapter has received a Frame Reject (FRMR) frame.

BIT 3 (FRMR__SENT): When set to one, indicates that the adapter has sent an FRMR frame.

BIT 4 (SABME__RCVD): When set to one, indicates that the adapter has received a Set Asynchronous Balanced Mode Extended (SABME) frame for an open link station.

BIT 5 (SABME__OPEN__LINK): When set to one, indicates that the adapter has received a SABME and has opened a new link station.

BIT 6 (REMOTE__BUSY): When set to one, indicates that the remote station on a link has entered a local busy state.

BIT 7 (REMOTE__NOT__BUSY): When set to one, indicates that the remote station on a link has exited a local busy state.

BIT 8 (TI__EXPIRED): When set to one, indicates that the adapter's Inactivity Timer (TI) has expired. This interrupt is generated only for a link in the Disconnected state.

BIT 9 (LLC__CTR__OVERFLOW): When set to one, indicates that one of the adapter's LLC error counters has been incremented from 254 to 255.

BIT 10 (ACCESS__PRIORITY): When set to one, indicates that the access priority for a local SAP or link station has been reduced. This interrupt will be generated when the user first attempts to transmit from the SAP after the access priority has been reduced.

BITS 11-14 (RESERVED): These bits are reserved and are set to zero.

BIT 15 (LOCAL STATION ENTERED LOCAL BUSY): This bit, when set, indicates that the local link station has entered a local busy state. This interrupt is not generated if the local busy state was entered due to a FLOW.CONTROL command from the attached system.

FRMR_DATA: This field contains the FRMR response contained in a transmitted or received FRMR frame. This field is updated with a LLC.STATUS interrupt.

AC_PRIORITY: This field contains the new access priority for the SAP/Link station specified in STATION_ID_S. This field is updated with a LLC.STATUS interrupt.

REMOTE_ADDRESS: This field contains the 6-byte node address of the remote station. This field is updated with a LLC.STATUS interrupt.

REMOTE_SAP: This field contains the Remote SAP connected to the link specified by the STATION_ID_S field. This field is updated with a LLC.STATUS interrupt.

FRAME_TYPE: This field indicates to the attached system what type of frame has been received. This field takes a value as shown in Table 2-4. A frame type of Bridge Data (> 20) indicates a frame that is not addressed to this adapter. That is, it was received due to copy-all-frames or an external address match. For more information on the other frame types, refer to the section on the TRANSMIT command. This field is updated with a RECEIVE.PENDING interrupt.

Table 2-4. Receive Frame Types

VALUE (HEX)	FRAME TYPE
02	MAC frame
04	I frame
06	UI frame
08	XID cmd (poll = 1)
0A	XID cmd (poll = 0)
0C	XID resp (final = 1)
0E	XID resp (final = 0)
10	TEST resp (final = 1)
12	TEST resp (final = 0)
14	Other (non-MAC)
20	Bridge data

2.7 Adapter Initialization

This sub-section describes the procedures for bring-up diagnostic verification and adapter initialization. First, the bring-up diagnostic entry conditions and return codes are explained. Then the adapter initialization procedure and parameters are discussed.

2.7.1 Bring-Up Diagnostics

The Communications Processsor of the adapter executes a stand-alone diagnostic routine upon one of two conditions:

1. $\overline{\text{SRESET}}$ line of the System Interface becoming active-low.
2. The attached system writing a one to bits 0-7 of the SIF Interrupt Register (>FF00).

These diagnostics are executed independently of the state of the System Interface pins or the lobe media.

2.7.1.1 Bring-Up Diagnostics Verification

Before the adapter can be initialized for proper operation, the bring-up diagnostics must terminate normally. To verify this the attached system should follow the procedure described below.

After either application of the $\overline{\text{SRESET}}$ signal or writing a software reset (>FF00) to the Interrupt Register, the attached system should read the Interrupt Register until one of the following conditions has occurred:

1. If the initialize bit is set to one, and the test bit is zero, and the error bit is zero, then the interrupt_code bits (12-15) should also be zero. This indicates that the bring-up diagnostics completed successfully and the adapter may now be initialized. This combination of bits results in a >0040 in the SIF Interrupt Register.
2. If the TEST and the ERROR bits are set to one, the diagnostics have detected an unrecoverable hardware error. The bring-up error code can be read from bits 12-15. Table 2-5 lists the definitions of these error codes.
3. If neither of the above conditions occurs within three seconds of reset, there is an error preventing completion of the diagnostic routines. It is recommended that the attached system reset and retry this procedure three times. If still unsuccessful, the adapter and attached system should be checked.

Table 2-5. Bring-Up Diagnostic Error Codes

ERROR CODE				ERROR CONDITION
12	13	14	15	
0	0	0	0	Initial Test Error
0	0	0	1	Adapter ROM Checksum Error
0	0	1	0	Adapter RAM Error
0	0	1	1	Instruction Test Error
0	1	0	0	Interrupt Test Error
0	1	0	1	Protocol Handler Hardware Error
0	1	1	0	System Interface Register Error

2.7.2 Adapter Initialization

After successful completion of the adapter's bring-up diagnostics, the system software must initialize the adapter. This initialization involves the transfer of parameters to the adapter using the DIO interface. These parameters specify:

1. The address in the system memory of the System Command Block (SCB) and System Status Block (SSB).
2. Interrupt control parameters.

Before the completion of the initialization process, the adapter initiates a test of the DMA interface. These tests include:

1. DMA writes to both the System Command Block and System Status Block.
2. DMA reads from both the System Command Block and System Status Block and a compare to expected data.

These tests do not require any attached system software to execute; however, in the event these tests fail, the adapter will return an error in the Interrupt Register.

2.7.2.1 The Initialization Block

The Initialization Block is 22 bytes in length and the entire block must be transferred to the adapter. Figure 2-10 defines the 22 bytes of this block:

		High Byte	Low Byte
Word	0	INIT_OPTIONS	
	1	CMD_STATUS_VECTOR	TRANSMIT_VECTOR
	2	RECEIVE_VECTOR	RING_STATUS_VECTOR
	3	SSB_CLEAR_VECTOR	ADAPTER_CHK_VECTOR
	4	RECEIVE_BURST_SIZE	
	5	TRANSMIT_BURST_SIZE	
	6	DMA_ABORT_THRESHOLD	
	7	SCB_ADDRESS (high)	
	8	SCB_ADDRESS (low)	
	9	SSB_ADDRESS (high)	
	10	SSB_ADDRESS (low)	

Figure 2-10. Initialization Parameter Block

INIT_PARM_BLOCK Field Descriptions.

INIT_OPTIONS: This 16-bit field is used to specify the desired initialization options. The bit assignments of the 16-bit Initialization Options field is shown below.

BIT 0 (RESERVED): This bit must be set to one.

BITS 1-2 (PARITY_ENABLE): These bits should be set to one if the system bus provides odd parity on its data. If parity checking is not desired, these bits should be set to zero. If enabled, parity checking is performed on both DIO and DMA transfers between the adapter and attached system.

BIT 3 (BURST_SCB_SSB): If this bit is set to one, the adapter will transfer the SCB from the system and the SSB to the system in DMA burst mode. The burst size will be six bytes for the SCB read, two

bytes for SCB clear, and eight bytes for SSB write. If this bit is set to zero, then these transfers will occur in cycle steal mode.

BIT 4 (BURST_LIST): If this bit is set to one, the adapter will transfer transmit and receive lists from the system in DMA Burst Mode. The burst size will be 26 bytes. If this bit is set to zero then cycle steal mode is selected.

BIT 5 (BURST_LIST_STATUS): If this bit is set to one, the adapter will transfer list CSTAT and length information to the system in DMA Burst Mode. If this bit is set to zero, cycle steal mode will be selected.

BIT 6 (BURST_RECEIVE_DATA): If this bit is set to one, the adapter will transfer receive data to the system in DMA burst mode. The burst size is specified in the RECEIVE_BURST_SIZE field of the Initialization Block. If this bit is set to zero, cycle steal mode is selected.

BIT 7 (BURST_TRANSMIT_DATA): If this bit is set to one, the adapter will transfer transmit data from the system in DMA burst mode. The burst size is specified in the TRANSMIT_BURST_SIZE field of the Initialization Block. If this bit is set to zero, cycle steal mode is selected.

BIT 8 (RESERVED): This bit must be reset to zero.

BIT 9 (LLC_ENABLE): This bit must be set to one to enable the adapter's LLC interface. If this bit is reset to zero, then only the MAC interface will be provided to the user. If this bit is set then the LLC software must be present in the adapter. The LLC software may be downloaded into DRAMs or present in EPROMs on the adapter bus.

BITS 10-15 (RESERVED): These bits must be reset to zero.

CMD_STATUS_VECTOR: This byte contains the interrupt vector that the adapter places on the attached system bus when the SSB is updated with command status for commands other than transmit or receive.

TRANSMIT_VECTOR: This byte contains the interrupt vector that the adapter places on the attached system bus when the SSB is updated with TRANSMIT_STATUS.

RECEIVE_VECTOR: This byte contains the interrupt vector that the adapter places on the attached system bus when the SSB is updated with RECEIVE_STATUS.

RING_STATUS_VECTOR: This byte contains the interrupt vector that the adapter places on the attached system bus when the SSB is updated with RING_STATUS.

SCB_CLEAR_VECTOR: This byte contains the interrupt vector that the adapter places on the attached system bus if an SCB.CLEAR interrupt is generated.

ADAPTER_CHK_VECTOR: This byte contains the interrupt vector that the adapter places on the attached system bus if an ADAPTER.CHECK interrupt is generated.

RECEIVE_BURST_SIZE: This 16-bit field contains a count of the maximum number of bytes that the adapter will DMA during one burst cycle when receive data is written to the attached system memory. If this field is zero, the adapter will set the burst size equal to the amount of data

to be transferred. This parameter is ignored if the BURST_RECEIVE_DATA bit of the Initialization Options field is set to zero, indicating cycle steal mode. The parameter must be even.

TRANSMIT_BURST_SIZE: This 16-bit field contains a count of the maximum number of bytes that the adapter will DMA during one burst cycle when transmit data is read from the attached system memory. If this field is zero, the adapter will set the burst size equal to the amount of data to be transferred. This parameter is NOT ignored if the BURST_TRANSMIT_DATA bit of the Initialization Options field is set to zero, indicating cycle steal mode. Even in cycle steal mode, TRANSMIT_BURST_SIZE is used to limit transmit data bus utilization so that higher priority receive DMA operations can be initiated. This parameter must be even.

DMA_ABORT_THRESHOLD: This 16-bit field contains counts for the number of times the adapter will re-try a DMA operation that is terminated abnormally by a bus error or parity error. The high-order byte (bits 0-7) contains the count for bus errors and the low-order byte (bits 8-15) contains the count for parity errors. The counts specify the total number of times the DMA operation is to be attempted. A count of zero is not permitted.

SCB_ADDRESS: This 32-bit field contains the 24-bit address of the SCB in attached system memory. This value must be an even address aligned on a word boundary. The high-order byte of this field is ignored.

SSB_ADDRESS: This 32-bit field contains the 24-bit address of the SSB in attached system memory. This value must be an even address aligned on a word boundary. The high-order byte of this field is ignored.

2.7.2.2 Writing the Initialization Block

The Initialization Block is passed to the adapter by following the procedure below:

1. Verify that the bring-up diagnostics completed successfully as described in paragraph 2.4.1.1.
2. Write the address >0A00 into the Address Register.
3. Begin transfer of the Initialization Block by writing each byte or 16-bit word to the Data Register/Auto-increment. This will cause the block to be written to successive adapter RAM locations beginning at RAM address >0A00.
4. Write the bit pattern >9080 to the Interrupt Register. This sets the INTERRUPT_ADAPTER and EXECUTE bits, prevents resetting the SYSTEM_INTERRUPT bit, and clears all others.
5. Continue to read the Interrupt Register until one of the following occurs:
   a. The INITIALIZE, TEST, and ERROR bits are all zero. This condition indicates that initialization is complete without error. The SCB should contain >0000C1E2D48B and the SSB should contain >FFFFD1D7C5D9C3D4.
   b. If the ERROR bit is set, the initialization process has failed. The INTERRUPT_CODE (bits 12-15) will contain the initialization error code. These error codes are listed in Table 2-6. The initialization procedure must be restarted from adapter reset.

c. If neither of the above conditions occurs within three seconds of loading the Initialization Parameter Block, then it is recommended that the attached system reset the adapter and retry the initialization procedure three times. If still unsuccessful, then the adapter should be checked for errors.

Table 2-6. Adapter Initialization Errors

ERROR CODE 12	13	14	15	ERROR CONDITION
0	0	0	1	Invalid Initialization Block. 22 bytes were not passed.
0	0	1	0	Invalid Options. This code is returned if the PARITY_ENABLE bits are not equal or Reserved bits are not zero in the INIT_OPTIONS. This code is also returned if the LLC_ENABLE bit is set and the LLC is not present.
0	0	1	1	Invalid Receive Burst Size. RECEIVE_BURST_SIZE is odd.
0	1	0	0	Invalid Transmit Burst Count. TRANSMIT_BURST_SIZE is odd.
0	1	0	1	Invalid DMA Abort Threshold. DMA_ABORT_THRESHOLD is zero.
0	1	1	0	Invalid SCB. SCB_ADDRESS is odd.
0	1	1	1	Invalid SSB. SSB_ADDRESS is odd.
1	0	0	0	DIO Parity. A parity error occurred during a DIO write operation.
1	0	0	1	DMA Timeout. The adapter timed out (10 seconds) waiting for a test DMA transfer to complete.
1	0	1	0	DMA Parity Error. A parity error occurred during the DMA tests and the operation was tried as specified by DMA_ABORT_THRESHOLD.
1	0	1	1	DMA Bus Error. The DMA test encountered a bus error and the operation was tried as specified by DMA_ABORT_THRESHOLD.
1	1	0	0	DMA Data Error. Initialize DMA test failed due to a data compare error.
1	1	0	1	Adapter Check. The adapter encountered an unrecoverable hardware error.

2.8 Adapter Command Set

The following sections describe the commands that are available at the adapter software interface. Figure 2-11 lists the available commands and the corresponding command codes. Command codes indicated as LLC I/F are valid only when the LLC_ENABLE bit of the Initialization options is set to one.

FUNCTION	COMMAND	
OPEN	>0003	
TRANSMIT	>0004	
TRANSMIT.HALT	>0005	
RECEIVE	>0006	
CLOSE	>0007	
SET.GROUP.ADDRESS	>0008	MAC I/F
SET.FUNCTIONAL.ADDRESS	>0009	
READ.ERROR.LOG	>000A	
READ.ADAPTER	>000B	
MODIFY.OPEN.PARAMETERS	>000D	
RESTORE.OPEN.PARAMETERS	>000E	
LLC.RESET	>0014	
OPEN.SAP	>0015	
CLOSE.SAP	>0016	
OPEN.STATION	>0019	
CLOSE.STATION	>001A	
CONNECT.STATION	>001B	
MODIFY.LLC.PARMS	>001C	LLC I/F
FLOW.CONTROL	>001D	
STATION.STATS	>001E	
DIR.INTERRUPT	>001F	
CONFIG.BRIDGE.PARMS	>0020	
LLC.REALLOCATE	>0021	
TIMER.SET	>0022	

Figure 2-11. TMS380 Adapter Command Set

2.9 OPEN Command

Before the adapter can be used for data communications, the attached system must first open the adapter by issuing an OPEN command. The OPEN command sets the adapter's addresses and enables the receipt of frames from the ring. The adapter will suspend processing of all interrupt requests, except reset, during the OPEN process.

If the LLC Interface is enabled, then the OPEN command will also enable the Global(FF) and Null(00) Service Access Points (SAPs) of LLC. The options which are set by this command may be modified by using the MODIFY.OPEN.PARAMETERS command or by closing the adapter via the CLOSE command and then re-opening the adapter with the desired options.

ENTRY

SCB_CMD	>0003
SCB_PARM_0	OPEN_PARM_BLOCK (high)
SCB_PARM_1	OPEN_PARM_BLOCK (low)

EXIT

SSB_CMD	>0003
SSB_PARM_0	OPEN_COMPLETION
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.9.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields of the SCB point to an OPEN parameter block which is used by the adapter to configure itself for operation. The size of this block is dependent on whether the LLC Interface was enabled during initialization of the adapter (LLC_ENABLE = 1). If LLC_ENABLE bit was set to one, the adapter will read a 44-byte block of system memory via DMA, otherwise the block is 32 bytes. The format of the OPEN parameter block is shown in Figure 2-12. The parameters followed by an asterisk are necessary only for LLC operation.

OPEN_PARM_BLOCK				
	+ 0	OPEN_OPTIONS		
	+ 2	NODE_ADDRESS		
	+ 4	NODE_ADDRESS		
	+ 6	NODE_ADDRESS		
	+ 8	GROUP_ADDRESS		
	+ 10	GROUP_ADDRESS		
	+ 12	FUNCTIONAL_ADDRESS		
	+ 14	FUNCTIONAL_ADDRESS		
	+ 16	RECEIVE_LIST_SIZE		
	+ 18	TRANSMIT_LIST_SIZE		
	+ 20	BUFFER_SIZE		
	+ 22	DATA_RAM_START_ADDRESS		
	+ 24	DATA_RAM_END_ADDRESS		
	+ 26	XMIT_BUF_MIN	XMIT_BUF_MAX	
	+ 28	PRODUCT_ID_ADDRESS		
	+ 30	PRODUCT_ID_ADDRESS		
	+ 32	SAP_MAX	STATION_MAX	*
	+ 34	GSAP_MAX	GSAP_MEMBER_MAX	*
	+ 36	TIMER_T1_1	TIMER_T2_1	*
	+ 38	TIMER_TI_1	TIMER_T1_2	*
	+ 40	TIMER_T2_2	TIMER_TI_2	*
	+ 42	MAX_FRAME_SIZE		*

Note: Parameters with an asterisk (*) are necessary only for LLC operation.

Figure 2-12. Open Parameter Block

Open Parameter Block Field Descriptions.

OPEN_OPTIONS: The bit functions of the OPEN Options field are provided below:

BIT 0 (WRAP_INTERFACE): If set, ring insertion process is omitted, and all user transmit data appears as user receive data. The data is transmitted on the lobe from the attached product to the wiring concentrator. This option can be used for system interface debug, system interface DMA testing, or lobe media testing. MODIFY.OPEN.PARAMETERS cannot be used to alter the value of this bit; a CLOSE command must be issued to terminate WRAP mode.

BIT 1 (DISABLE_HARD_ERROR): If set, a RING.STATUS interrupt for HARD_ERROR and TRANSMIT_BEACON will not be generated.

BIT 2 (DISABLE_SOFT_ERROR): If set, a RING.STATUS interrupt for SOFT_ERROR will not be generated.

BIT 3 (PASS_ADAPTER_MAC_FRAMES): The value of this bit determines the action to be taken by the adapter when unsupported Adapter Class MAC frames are received. If this bit is set to one these MAC frames will be passed to the attached system as normal receive data. If this bit is reset to zero, the adapter will purge these frames and transmit a negative response MAC frame to the originating station.

BIT 4 (PASS_ATTENTION_MAC_FRAMES): If set to one, all Attention MAC frames that are not equal to the last Attention MAC frame received will be passed to the system as receive data following normal processing by the adapter.

BIT 5 (PAD_ROUTING_FIELD): If set to one, the adapter will pad the Routing Field to 18 bytes. If no Routing Field is present in the received frame, the entire field will be padded to 18 bytes. This option is voided if the current list's data count is not at least 32 bytes. In this case the frame will be transferred as if the bit were set to zero.

BIT 6 (FRAME_HOLD): If set to one, the adapter will wait for an entire frame to be read from the ring before initiating the DMA transfer of the frame to the system. If this bit is reset to zero, then a DMA transfer will be initiated whenever an adapter internal buffer is filled. This bit will be forced to one if the LLC interface is enabled or if either bit 13 or 14 of the OPEN_OPTIONS is set to one.

BIT 7 (CONTENDER): If set to one, the adapter will participate in the Monitor Contention process when another adapter detects the need for contention and initiates the process. This bit has no effect if this adapter detects the need for contention and initiates the Monitor Contention process.

BIT 8 (PASS_BEACON_MAC_FRAMES): If set, the adapter will pass Beacon MAC frames to the attached system after processing them. After passing the Beacon MAC frame, the next Beacon MAC frame will be passed only if the source address or the Beacon Type Subvector changes.

BIT 9-12 (RESERVED): Should be reset to zero.

BIT 13 (COPY_ALL_MAC_FRAMES): Setting this bit to one causes the Adapter to copy and pass all MAC frames to the attached system which occur on the ring. Note that MAC frames will be copied whether or not addressed to the Adapter. MAC frames which are addressed to the Adapter which require a response will not be passed to the attached system. The following MAC frames will NOT be passed to the attached system when they are addressed to this adapter:

- Request Station State
- Request Station Address
- Request Station Attachment
- Transmit Forward
- Change Parameters
- Initialize Ring Station
- Lobe Media Test

These frames will be passed, however, if they are destined for another adapter on the ring.

Note that MAC frames addressed to the adapter are processed by the adapter before being passed to the attached system. Thus, frames may not be passed to the attached system in the same order in which they were received.

Bit 4 (PASS_ATTENTION_MAC_FRAMES), and bit 8 (PASS_BEACON_MAC_FRAMES) are forced to zero when bit 13 is set to one. Bit 3 (PASS_ADAPTER_MAC_FRAMES) will, however, function in a normal manner.

The first frame copied and passed to the attached system after opening with this option and issuing the Receive command will be the Duplicate Address Test (DAT) MAC frame. This is because the DAT MAC frame is transmitted during the Lobe Media Check Phase (Phase 0) of the Insertion Process. The Lobe Media Test MAC frame, however, is NOT copied by the adapter.

This bit cannot be set if the LLC Interface is enabled unless a CONFIG.BRIDGE.PARMS command is first executed.

BIT 14 (COPY_ALL_NON_MAC_FRAMES): Setting this bit to one causes the adapter to pass all non-MAC frames that appear on the ring to the attached system. All non-MAC frames will be copied whether or not addressed to the adapter.

Note:

Occasionally when the adapter is opened with the copy-all-frames bits set, the OPEN command will fail due to ring poll failure during the insertion process. This can occur when inserting into a ring with heavy traffic, which causes extensive receive activity within the adapter during insertion process operations. If this open failure should occur, reset the adapter and try again. This can be avoided by opening the adapter without the copy-all-frames bits set and using the MODIFY.OPEN.PARAMETERS command (see Section 2.15) to set the desired copy options after the adapter has inserted into the ring.

This bit cannot be set if the LLC Interface is enabled, unless a CONFIG.BRIDGE.PARMS command is first executed.

BIT 15 (PASS_FIRST_BUFFER_ONLY): Setting this bit to one causes the Adapter to pass to the attached system only the first internal buffer of each received frame. The internal buffer size is specified by the BUFFER_SIZE field of the Open Parameter list. Regardless of the size of frame received, the adapter will transfer one internal buffer to the attached system. If the frame received is smaller than the internal buffer size, the data from the last byte of the frame's information field to the end of the buffer will be filled with indeterminate data. If the frame received is larger than the internal buffer size, only the first buffer will be transferred.

When this bit is set, the FRAME SIZE field of the receive list which starts a frame will **always** contain the internal buffer size. It will **not** contain the frame size. The 16-bit frame size value is written in the last two bytes of the buffer passed to the attached system.

The frame will also be marked with an "elapsed time" value. This is the value of a 16-bit counter which is started at adapter reset and incremented every 10 milliseconds. It will thus roll over to zero approximately every 655 seconds. This value is useful for measuring the relative time of appearance of frames on the ring.

For example, if a 34-byte frame is received with an adapter configured with 96-byte buffers, the 16-bit value for the elapsed time will be written in bytes 93 and 94, and the 16-bit value for frame size will be written in bytes 95 and 96 of the internal buffer. If a 128-byte frame is received with an adapter configured with 96-byte buffers, only the first 92 bytes of the frame will be passed to the attached system. The last two bytes passed will contain the size indicating a 128-byte frame was received, and the two bytes preceding the size will indicate the value of the elapsed time variable. The frame size is defined as the number of bytes starting from the Access Control (AC) field through the last byte in the information field.

Note that the PASS_FIRST_BUFFER_ONLY option is independent of the options taken in the rest of the bits in the open options field. Thus, this bit affects the manner in which receive frames are passed to the host regardless of the reason the frames are passed to the attached system. This bit will be forced off when the LLC Interface is enabled.

NODE_ADDRESS: This 6-byte field specifies the node address for the adapter. If this address is all zeros, the adapter will use the Burned-in-address (BIA) read from the BIA PROM.

GROUP_ADDRESS: This 32-bit field specifies the adapter Group Address and will cause the adapter to receive messages that are sent to this address. GROUP_ADDRESS can be any value, but Bit 0 is forced to one by the adapter. Group Address recognition is disabled by specifying GROUP_ADDRESS as zero. The two high-order bytes of the Group Address are set to >C000.

FUNCTIONAL_ADDRESS: This 32-bit field specifies the Functional Address and will cause the adapter to receive messages that are sent to the Functional Address. Bits 0 and 31 are ignored by the adapter. A zero value disables the Functional Address feature. The two high-order bytes of the Functional Address are set to >C000.

RECEIVE_LIST_SIZE: This 16-bit field indicates the number of bytes which must be read by the adapter when obtaining a Receive List from the attached system. A decimal value of 0, 14, 20, or 26 is required. If zero, the default value of 26 is used.

TRANSMIT_LIST_SIZE: This 16-bit field indicates the number of bytes which must be read by the adapter when obtaining a Transmit List from the attached system. A decimal value of 0, 14, 20, or 26 is required. If zero, the default value of 26 is used. If the LLC Interface is enabled, the adapter will automatically add four bytes to the value of the parameter for start-of-frame lists.

BUFFER_SIZE: This 16-bit field indicates the adapter's internal buffer size, in bytes. BUFFER_SIZE must be greater than or equal to 96 and the three low-order bits must be zero. If this field is zero, a default value of 112 bytes is used.

DATA_RAM_START_ADDRESS: This 16-bit parameter defines the starting address of data RAM start address within the adapter. For completely RAM-based adapters, this parameter should indicate non-code RAM only. This is RAM which is to be used for program variables and transmit and/or receive buffers, and not for program instructions or constant data. Data RAM must be within the address range >1000 to >BFFE. The RAM start address must be on an eight-byte boundary minus two bytes (bits 13 and 14 are b'11'). During the open command, RAM and decode logic are tested. If bad parity is detected, an ADAPTER.CHECK interrupt will be generated.

DATA_RAM_END_ADDRESS: This 16-bit field specifies the ending address of adapter data RAM. This value must be even.

TRANSMIT_BUFFER_MINIMUM_COUNT: This byte parameter contains the number of adapter buffers that are to be reserved as transmit buffers. These buffers will be reserved for transmit only and will never be used for receive. If zero is specified, no buffers are reserved for transmit. The minimum transmit buffer count must be less than or equal to the TRANSMIT_BUFFER_MAXIMUM_COUNT.

TRANSMIT_BUFFER_MAXIMUM_COUNT: This byte parameter contains the maximum number of adapter buffers that are to be used for transmit. A minimum of two buffers must be available for receive. If zero, a default value of six is used. The product of TRANSMIT_BUFFER_MAXIMUM_COUNT and (BUFFER_SIZE – 8) determines the largest frame that the adapter can transmit.

PRODUCT_ID_ADDRESS: This 32-bit field contains a 24-bit pointer to the attached system Product ID. Eighteen bytes are read starting from the location specified and stored in adapter memory for use if a Request Station Attachment MAC frame is received from the Network Manager. The 18 bytes are available for attached system use after the OPEN command has been processed. The most significant byte of this field is ignored by the adapter, but should be reset to zero.

SAP_MAX: This parameter is used to specify the maximum number of Service Access Points (SAPs) that may be open at any one time. The value specified in this field will be limited by the amount of adapter RAM available for LLC use. Adapter RAM usage is discussed in Section 2.3. If set to zero, a default of 2 will be used.

STATION_MAX: This parameter is used to specify the maximum number of link stations that may be open at any one time. This number reflects link stations opened for all SAPs and will be limited by the amount of adapter RAM available for LLC use. If set to zero, a default of 6 will be used.

GROUP_SAP_MAX: This parameter is used to specify the maximum number of Group Service Access Points that may be open at any one time. The maximum value specified in this field will be limited by the amount of adapter RAM available for LLC use. This parameter must be less than or equal to the SAP_MAX parameter value.

GSAP_MEMBER_MAX: This parameter is used to specify the maximum number of Service Access Points that may be assigned to a Group. The value specified in this field must be less than or equal to the value of SAP_MAX.

TIMER_T1_1: This parameter is used to specify the number of 40-ms clock periods which make up a group 1 (short) Response Timer period. If the value input is zero, then the default value of 5 will be used.

TIMER_T2_1: This parameter is used to specify the number of 40-ms clock periods which make up a group 1 (short) Receive Acknowledge Timer period. If the value input is zero, then the default value of 1 will be used.

TIMER_TI_1: This parameter is used to specify the number of 40-ms clock periods which make up a group 1 (short) Inactivity Timer period. If the value input is zero, then the default value of 25 will be used.

TIMER_T1_2: This parameter is used to specify the number of 40-ms clock periods which make up a group 2 (long) Response Timer period. If the value input is zero, then the default value of 25 will be used.

TIMER_T2_2: This parameter is used to specify the number of 40-ms clock periods which make up a group 2 (long) Receive Acknowledge Timer period. If the value input is zero, then the default value of 10 will be used.

TIMER_TI_2: This parameter is used to specify the number of 40-ms clock periods which make up a group 2 (long) Inactivity Timer period. If the value input is zero, then the default value of 125 will be used.

MAX_FRAME_SIZE: Maximum number of bytes in a frame (AC through Information) that can be transmitted by the adapter. The value must be at least 15.

2.9.2 Command Completion

Upon completion of the OPEN command, a COMMAND.STATUS interrupt is posted and the SSB updated with command completion information. The OPEN command code is loaded into SSB_CMD, the OPEN_COMPLETION code is loaded into SSB_PARM_0. The bit definitions of the OPEN_COMPLETION field are listed below.

OPEN_COMPLETION Bit Field Definitions.

BIT 0 (OPEN_SUCCESSFUL): Bit 0 will be set to one if the OPEN command completed successfully. All other bits will be set to zero.

BIT 1 (NODE_ADDRESS_ERROR): Bit 1 will be set to one if an error was detected in the NODE_ADDRESS field of the Open Parameters or if the BIA was read as all zeros.

BIT 2 (LIST_SIZE_ERROR): Bit 2 will be set to one if the RECEIVE_LIST_SIZE and/or the TRANSMIT_LIST_SIZE are not equal to 0, 14, 20, or 26.

BIT 3 (BUFFER_SIZE_ERROR): Bit 3 will be set to one if BUFFER_SIZE is less than 96, or if the three low-order bits are not zero, or if there are less than two buffers specified.

BIT 4 (DATA_RAM_ERROR): Bit 4 will be set to one if the data RAM is not specified to be between >1000 and >C000 or if an error (other than parity) is detected in the RAM. If a parity error is detected, then an ADAPTER.CHECK will occur.

BIT 5 (TRANSMIT_BUFFER_COUNT_ERROR): Bit 5 will be set to one if the number of Receive Buffers (total number of buffers minus the TRANSMIT_BUFFER_MAXIMUM_COUNT) is less than two.

BIT 6 (OPEN_ERROR): Bit 6 will be set one if an error is detected during insertion onto the ring. Bits 8-15 in the SSB_PARM_0 field can be read to determine the cause of the error. Bits 8-15 are effectively divided into two 4-bit entities. The first 4-bit field, Open Phase, is set to the OPEN command processing phase in which the error defined in the second 4-bit field occurred. The second 4-bit field, Open Error Code, is set to an error code which reflects the ring-related error that occurred during OPEN command processing. The Open Phase and Open Error codes are listed in Figure 2-13.

BITS 8	9	10	11	OPEN COMMAND PHASES
0	0	0	1	Lobe Media Test
0	0	1	0	Physical Insertion
0	0	1	1	Address Verification
0	1	0	0	Participation in Ring Poll
0	1	0	1	Request Initialization
BITS 12	**13**	**14**	**15**	**OPEN ERROR CODES**
0	0	0	1	FUNCTION_FAILURE
0	0	1	0	SIGNAL_LOSS
0	0	1	1	RESERVED
0	1	0	0	RESERVED
0	1	0	1	TIMEOUT
0	1	1	0	RING_FAILURE
0	1	1	1	RING_BEACONING
1	0	0	0	DUPLICATE_NODE_ADDRESS
1	0	0	1	REQUEST_PARAMETERS
1	0	1	0	REMOVE_RECEIVED

Figure 2-13. OPEN Phases and OPEN Error Codes

OPEN Error Code Descriptions.

FUNCTION_FAILURE: This code is returned when the adapter is unable to transmit to itself while wrapped through its lobe at the wiring concentrator, or if any MAC frames are received before physical insertion.

SIGNAL_LOSS: This code is returned if a signal loss condition is detected at the adapter receiver input during the open process (either when wrapped or inserted onto the ring).

TIMEOUT: This code is returned if the adapter fails to logically insert onto the ring before the insertion timer expires. Each phase of the insertion process must complete before expiration of the 18-second insertion timer.

RING_FAILURE: This code is returned if the adapter times out when attempting a ring purge after becoming the Active Monitor; that is, when the adapter is unable to receive its own Ring Purge MAC frames.

RING_BEACONING: This code is returned if the adapter receives a Beacon MAC frame after physically inserting into the ring. This indicates a break in the ring.

DUPLICATE_NODE_ADDRESS: This code is returned if the adapter finds that another station on the ring already has the address which the adapter wishes to use.

REQUEST_PARAMETERS: This code is returned if the adapter determines that a Ring Parameter Server (RPS) is present on the ring but does not respond to a Request Initialization MAC frame. (If no RPS is present, the adapter will not return this code.)

REMOVE_RECEIVED: This code is returned if the adapter receives a Remove Adapter MAC frame during the insertion process.

BIT 7 (LLC_ERROR): Bit 7 will be set to one if an error is detected during the LLC processing portion of the OPEN command. Bits 8-15 will determine the error as shown in Table 2-7.

Table 2-7. LLC Open Error Codes

BITS 8-15	LLC OPEN ERROR
>06	Invalid Options. The first-buffer-only bit is set, or the copy-all-frames bits are set and a CONFIG.BRIDGE.PARMS command has not been issued.
>30	Inadequate receive buffers to open. The MAX_SAP and MAX_STATION and TRANSMIT_BUFFER_MINIMUM_COUNT parameters are too large for two buffers to be left for receive.

2.10 CLOSE Command

The CLOSE command is used to terminate transmission on the ring or to terminate OPEN with the wrap option. Any frames residing in adapter internal buffers will be purged. All SAPs and Link Stations will be closed. After this command has completed, the adapter should be re-initialized before issuing an OPEN command.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened.

ENTRY

SCB_CMD	>0007
SCB_PARM_0	>0000
SCB_PARM_1	>0000

EXIT

SSB_CMD	>0007
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.10.1 Command Initiation

CLOSE does not require a command parameter block. Both the SCB_PARM_0 and SCB_PARM_1 fields are ignored, but should be set to zero.

2.10.2 Command Completion

Upon completion of CLOSE, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >0007, and updates SSB_PARM_0 with COMMAND_STATUS, as shown in Table 2-8.

Table 2-8. CLOSE Return Codes

VALUE	EXPLANATION
>8000	Good completion

2.11 SET.GROUP.ADDRESS Command

The SET.GROUP.ADDRESS command is used to alter the adapter Group Address after an OPEN command has been issued.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened.

ENTRY

SCB_CMD	>0008
SCB_PARM_0	GROUP_ADDRESS_HIGH
SCB_PARM_1	GROUP_ADDRESS_LOW

EXIT

SSB_CMD	>0008
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.11.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 32-bit address which is the Group Address to be stored in the adapter Group Address Register. Bit 0 is forced to one by the adapter. The most significant two bytes of the 48-bit group address will be >C000.

2.11.2 Command Completion

Upon completion of SET.GROUP.ADDRESS, the adapter will generate a COMMAND.STATUS interrupt. The SSB_CMD field is set to >0008, and the SSB_PARM_0 field is updated with COMMAND_STATUS, as shown in Table 2-9.

Table 2-9. SET.GROUP.ADDRESS Return Codes

VALUE	EXPLANATION
>8000	Good completion

2.12 SET.FUNCTIONAL.ADDRESS Command

The SET.FUNCTIONAL.ADDRESS command is used to alter the adapter Functional Address after OPEN command has been issued.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened.

ENTRY

SCB_CMD	>0009
SCB_PARM_0	FUNCTIONAL_ADDRESS_HIGH
SCB_PARM_1	FUNCTIONAL_ADDRESS_LOW

EXIT

SSB_CMD	>0009
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.12.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 32-bit address which is the Functional Address to be stored in the adapter's internal Functional Address Register. Bits 0 (most significant bit) and 31 (least significant bit) of the Functional Address are ignored. The most significant two bytes of the 48-bit functional address will be >C000.

2.12.2 Command Completion

Upon completion of SET.FUNCTIONAL.ADDRESS, the adapter generates a COMMAND.STATUS interrupt and sets the SSB_CMD field to >0009. The SSB_PARM_0 field is updated with COMMAND_STATUS as shown in Table 2-10.

Table 2-10. SET.FUNCTIONAL.ADDRESS Return Codes

VALUE	EXPLANATION
>8000	Good completion

2.13 READ.ERROR.LOG Command

The READ.ERROR.LOG command is used to read the adapter's error counters. The counters are kept in an Attached Product Error Log. The adapter will reset the Attached Product Error Log after this command has completed.

This command is ignored if the adapter has not been opened.

ENTRY

SCB_CMD	>000A
SCB_PARM_0	ERROR_LOG_ADDR (high)
SCB_PARM_1	ERROR_LOG_ADDR (low)

EXIT

SSB_CMD	>000A
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.13.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to a 14-byte area in attached system memory where the Error Log Table is to be written. The most significant byte of SCB_PARM_0 is ignored. The 14-byte Error Log Table format is shown in Figure 2-14. The error counters are explained following Figure 2-14.

ERROR_LOG			
	+ 0	LINE ERROR	RESERVED
	+ 2	BURST ERROR	ARI/FCI ERROR
	+ 4	RESERVED	RESERVED
	+ 6	LOST FRAME ERROR	RECEIVE CONGESTION ERROR
	+ 8	FRAME COPIED ERROR	RESERVED
	+ 10	TOKEN ERROR	RESERVED
	+ 12	DMA BUS ERRORS	DMA PARITY ERRORS

Figure 2-14. Error Log Table

Adapter Error Counters.

LINE ERROR: The line error counter is incremented whenever: 1) a frame is repeated or copied, 2) the Error Detected Indicator (EDI) is zero in the incoming frame, and 3) one of the following conditions exists:

1. A code violation exists between the Starting Delimiter and the Ending Delimiter of the frame.
2. A code violation exists in a token.
3. A Frame Check Sequence (FCS) error exists.

When the line error is incremented, the EDI of the frame is set to one so that no further adapters will count the error.

BURST ERROR: The burst error counter is incremented when the adapter detects the absence of transitions on the line for 5 half-bit times. The adapter that detects the BURST5 condition begins to transmit idles after the fourth half-bit time without transition so that no other adapters will detect the burst 5 error.

ARI/FCI ERROR: The ARI/FCI error counter is incremented when an adapter receives an Active Monitor Present (AMP) MAC frame with the ARI/FCI bits equal to zero and a Standby Monitor Present (SMP) MAC frame with the ARI/FCI bits equal to zero, or more than one SMP MAC frames with the ARI/FCI bits equal to zero, without receiving an intervening AMP MAC frame. This condition indicates that the upstream neighbor is unable to set the ARI/FCI bits.

LOST FRAME ERROR: The lost frame error counter is incremented when an adapter is in transmit (stripping) mode and fails to receive the end of the frame it transmitted.

RECEIVE CONGESTION ERROR: The receive congestion error counter is incremented when an adapter in the repeat mode recognizes a frame addressed to it but has no buffer space available to copy the frame.

FRAME COPIED ERROR: The frame copied error counter is incremented when an adapter in the receive/repeat mode recognizes a frame addressed to its specific address but finds the ARI bits not equal to zero. This indicates a possible line hit or duplicate address.

TOKEN ERROR: The token error counter is active only in the Active Monitor station. It is incremented when the Active Monitor detects an error with the token protocol as follows:

1. A token with non-zero priority has the MONITOR COUNT bit equal to one. This indicates a circulating high-priority token.
2. A frame has the MONITOR COUNT bit equal to one. This indicates a circulating frame.
3. No token or frame is received within a 10-ms window.
4. The Starting Delimiter/token sequence has a code violation in an area where code violations must not exist.

DMA BUS ERRORS: The DMA bus error counter counts the occurrences of DMA bus errors that do not exceed the abort thresholds as specified in the Initialization parameters.

DMA PARITY ERRORS: The DMA parity error counter counts the occurrences of DMA parity errors that do not exceed the abort thresholds as specified in the Initialization parameters.

2.13.2 Command Completion

Upon completion of READ.ERROR.LOG, the adapter will generate a COMMAND.STATUS interrupt and set the SSB_CMD field to >000A. The SSB_PARM_0 field is updated with COMMAND_STATUS as shown in Table 2-11.

Table 2-11. READ.ERROR.LOG Return Codes

VALUE	EXPLANATION
>8000	Good completion

2.14 READ.ADAPTER Command

The READ.ADAPTER command is used to transfer adapter memory contents across the System Interface to attached system memory.

ENTRY

SCB_CMD	>000B
SCB_PARM_0	DATA_AREA_ADDR (high)
SCB_PARM_1	DATA_AREA_ADDR (low)

EXIT

SSB_CMD	>000B
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.14.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to a buffer in attached system memory which will store the contents of the specified adapter memory locations. The most significant byte of SCB_PARM_0 is ignored. The data area specified by the attached system should be written to in the format shown in Figure 2-15.

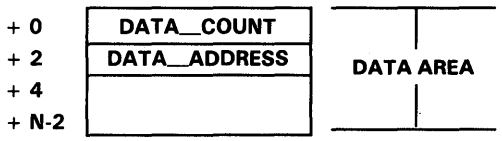


Figure 2-15. Data Area Format

The 16-bit DATA_COUNT field contains the number of bytes to read from the adapter.

DATA_ADDRESS is a 16-bit field containing the address of the data in the adapter to be read. Bit 15 is reset to zero by the adapter. The DATA_ADDRESS is not checked for valid extents. The READ.ADAPTER command will result in an ADAPTER.CHECK interrupt if reference is made to an undefined storage area.

Listed below are some of the internal adapter pointers accessible via the READ.ADAPTER command. These pointers will reside beginning at location >0A00 in adapter memory and are valid only after reset and initialization, but before the OPEN command is issued.

>0A00 Pointer to Burned-in Address.

>0A02 Pointer to Software Level.

>0A04 Pointer to adapter addresses:
pointer + 0 Node address.
pointer + 6 Group address.
pointer + 10 Functional address.

>0A06 Pointer to adapter parameters.
pointer + 0 Physical drop number.
pointer + 4 Upstream Neighbor Address (UNA).
pointer + 10 Upstream physical drop number.
pointer + 14 Last ring poll address.
pointer + 22 Transmit access priority.
pointer + 24 Source class authorization.
pointer + 26 Last attention code.
pointer + 28 Last source address.
pointer + 34 Last beacon type.
pointer + 36 Last major vector.
pointer + 38 Ring status.
pointer + 40 Soft error timer value.
pointer + 42 Ring Interface error counter.
pointer + 44 Reserved.
pointer + 46 Monitor error code.
pointer + 48 Beacon transmit type.
pointer + 50 Beacon receive type.
pointer + 52 Frame correlator save.
pointer + 54 Beaconing station UNA.
pointer + 60 Reserved.
pointer + 64 Beaconing station physical drop number.

>0A08 Pointer to MAC buffer (a special buffer used by the software to transmit adapter generated MAC frames).

>0A0A Pointer to LLC counters
pointer + 0 MAX_SAPs.
pointer + 2 Open SAPs.
pointer + 4 MAX_STATIONs.
pointer + 6 Open Stations.
pointer + 8 Available Stations.
pointer + 10 Reserved.

2.14.2 Command Completion

Upon completion of READ.ADAPTER, the adapter will generate a COMMAND.STATUS interrupt and set the SSB_CMD field to >000B. The SSB_PARM_0 field is updated with COMMAND_STATUS as shown in Table 2-12.

Table 2-12. READ.ADAPTER Return Codes

VALUE	EXPLANATION
>8000	>Good completion

2.15 MODIFY.OPEN.PARAMETERS Command

MODIFY.OPEN.PARAMETERS may be used to modify certain adapter operational parameters that were set by the OPEN command. All OPEN options, with the exception of WRAP_INTERFACE, that were specified in the OPEN_OPTIONS field of the OPEN Parameter List may be modified. The bit corresponding to WRAP_INTERFACE (bit 0) is ignored by this command.

A COMMAND.REJECT will be issued if the adapter has not been opened.

ENTRY

SCB_CMD	>000D
SCB_PARM_0	OPEN_OPTIONS
SCB_PARM_1	>0000

EXIT

SSB_CMD	>000D
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.15.1 Command Initiation

The SCB_PARM_0 of the SCB contains a 16 bit OPEN_OPTION field. The bit descriptions for this field are the same as those specified for the OPEN_OPTIONS field of the OPEN command. SCB_PARM_1 is ignored, but should be set to zero.

2.15.2 Command Completion

Upon completion of MODIFY.OPEN.PARAMETERS, the adapter will generate a COMMAND.STATUS interrupt, set SSB_CMD to >000D and update SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS will take on values according to Table 2-13.

Table 2-13. MODIFY.OPEN.PARAMETERS Return Codes

VALUE	EXPLANATION
>8000	Good completion

2.16 RESTORE.OPEN.PARAMETERS Command

RESTORE.OPEN.PARAMETERS may be used to modify certain adapter operational parameters that were set by the OPEN command. All Open options, with the exception of WRAP_INTERFACE, that were specified in the OPEN_OPTIONS field of the Open Parameter List may be modified. The bit corresponding to WRAP_INTERFACE (bit 0) is ignored by this command.

A COMMAND.REJECT will be issued if the adapter has not been opened.

ENTRY

SCB_CMD	>000E
SCB_PARM_0	OPEN_OPTIONS
SCB_PARM_1	>0000

EXIT

SSB_CMD	>000E
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.16.1 Command Initiation

The SCB_CMD field of the SCB should be set to >000E. The SCB_PARM_0 field of the SCB contains a 16-bit OPEN_OPTIONS field. The bit descriptions for this field are the same as those specified for the OPEN_OPTIONS field of the OPEN command. SCB_PARM_1 is ignored, but should be set to zero.

2.16.2 Command Completion

Upon completion of the RESTORE.OPEN.PARAMETERS command, the adapter will generate a COMMAND.STATUS interrupt, set SSB_CMD to >000E, and update SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS will take on values according to Table 2-14.

Table 2-14. RESTORE.OPEN.PARAMETERS Return Codes

VALUE	EXPLANATION
>8000	Good completion

2.17 LLC.RESET Command

LLC.RESET is used to terminate all outstanding commands for a specified link station or all link stations within a specified SAP. The link station(s) that are affected by LLC.RESET must be reopened for further use. LLC.RESET may also be used as a global reset for all SAPs and all link stations. If all SAPs and link stations are reset, the adapter will be placed in a state identical to the state immediately following the OPEN.ADAPTER command.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened or if the LLC interface has not been enabled.

ENTRY

SCB_CMD	>0014
SCB_PARM_0	STATION_ID
SCB_PARM_1	>0000

EXIT

SSB_CMD	>0014
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.17.1 Command Initiation

The STATION_ID associated with the link station to be reset is placed in SCB_PARM_0. STATION_ID >xx00 resets all link stations in SAP xx and STATION_ID >0000 resets all SAPs and all link stations. SCB_PARM_1 is ignored but should be set to zero.

2.17.2 Command Completion

Upon completion of LLC.RESET, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >0014, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS takes on values according to Table 2-15.

Table 2-15. LLC.RESET Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0040	Invalid Station_ID

2.18 OPEN.SAP Command

OPEN.SAP can be used to activate an individual SAP or a Group SAP. Parameters for SAP operation and default Link Station parameters are passed to the adapter by this command. The parameter values set by this command may be modified with the MODIFY.LLC.PARMS command.

This command will be rejected if the adapter has not been opened or if the LLC interface has not been enabled.

ENTRY

SCB_CMD	>0015
SCB_PARM_0	SAP_PARM_BLOCK (high)
SCB_PARM_1	SAP_PARM_BLOCK (low)

EXIT

SSB_CMD	>0015
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	FAILING-GROUP-SAP

2.18.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to the SAP_PARM_BLOCK, which is shown in Figure 2.16. The most significant byte of SCB_PARM_0 is ignored.

SAP_PARM_BLOCK	+ 0	RESERVED	
	+ 2	RESERVED	
	+ 4	TIMER_T1	TIMER_T2
	+ 6	TIMER_TI	MAXOUT
	+ 8	MAXIN	MAXOUT_INCR
	+ 10	MAX_RETRY_COUNT	GSAP_MAX_MEMBER
	+ 12	MAX_I_FIELD	
	+ 14	SAP_VALUE	SAP_OPTIONS
	+ 16	STATION_CNT	RESERVED
	+ 18	RESERVED	GROUP_MEMBER_CNT
	+ 20	SAP_GROUP_LIST_PTR (HI)	
	+ 22	SAP_GROUP_LIST_PTR (LO)	

SAP_GROUP_LIST	+ 0	GSAP_0	GSAP_1
	+ 2	GSAP_2	GSAP_3
	+ 4	GSAP_4	GSAP_5
	+ 6	GSAP_6	GSAP_7

Figure 2-16. SAP Parameter Block

SAP Parameter Block Field Definitions.

TIMER_T1: This parameter sets the Response Timer value and is specified as an integer between 1 and 10. Timer values between 1 and 5 use the group 1 timer period and values beween 6 and 10 use the group 2 timer period. An I frame is re-tried if an acknowledgment for a transmitted frame is not received within the time period specified. If the value is zero, a default of 5 is used.

TIMER_T2: This parameter sets the Receive Acknowledge Timer value and is specified as an integer between 1 and 10. Timer values between 1 and 5 use the group 1 timer period and values beween 6 and 10 use the group 2 timer period. If the receive window (defined by the MAXIN parameter) is not met, the link station will acknowledge a received frame(s) as soon as possible after this timer expires. The value specified for this parameter must be less than that specified for TIMER_T1. If the value is zero, a default of 2 is used. If the value is greater than 10, the timer will not be used.

TIMER_TI: This parameter sets the Inactivity Timer (TI) value and is specified as an integer between 1 and 10. Timer values between 1 and 5 use the group 1 timer period and values beween 6 and 10 use the group 2 timer period. A link station will perform a test to see if its link with the remote station is still intact if no link activity has been detected within this time period. If the value is zero, a default of 3 is used.

MAXOUT: This parameter specifies the maximum number of unacknowledged transmitted I-frames that may be outstanding at any one time. If this parameter is set to zero, a default value of two is used. The maximum value for this parameter is 127.

MAXIN: This parameter specifies the maximum number of I-frames that may be received before an acknowledgment is sent. If this parameter is set to zero, a default value of 1 is used. The maximum value for this parameter is 127.

MAXOUT_INCR: This parameter is used to specify the dynamic windowing algorithm increment value. If set to zero, a default value of one is used. This is the number of frames that must be acknowledged before the dynamic windowing algorithm increments MAXOUT.

MAX_RETRY_COUNT: This parameter specifies the default N2 value for link stations associated with SAP_VALUE. N2 defines the maximum number of times that an I-format or S-format frame may be retransmitted by the link station. The maximum value of this parameter is 255. If specified as zero, this parameter is defaulted to 8.

GSAP_MAX_MEMBER: If the Service Access Point being opened is to be a Group SAP (GSAP), this parameter specifies the maximum number of SAPs that may be opened as members of the GSAP. This parameter is ignored if bit 6 of the SAP_OPTIONS is zero. This parameter must be less than or equal to the similar parameter in the OPEN command.

SAP_VALUE: This parameter specifies the value of the SAP to be activated. SAP value >00 is reserved and should not be used in this field. The least-significant bit of SAP_VALUE must be zero. The value >FE should not be used for a group SAP.

SAP_OPTIONS: The bit functions of the SAP Options field are provided below:

BITS 0-2 (ACCESS_PRIORITY): The value specified in this bit field will be placed in the AC field of all frames transmitted from this SAP. The maximum allowed access priority is 6.

BIT 3 (RESERVED): This bit should be set to zero.

BIT 4 (XID_HANDLER): When this bit is set, responses to XID commands are managed by the attached system, and the adapter passes all received XID commands to the attached system. If this bit is 0, the adapter automatically responds to XID commands.

BIT 5 (INDIVIDUAL_SAP): When set, the SAP will be activated as an individual SAP.

BIT 6 (GROUP_SAP): When set, the SAP will be activated as a Group SAP.

BIT 7 (GROUP_MEMBER): When set, the SAP will be activated as a member of a Group SAP.

Note:

At least one of the bits 5,6, or 7 must be set. Bit 7 can be set only if bit 5 is set.

MAX_I_FIELD: This parameter specifies the maximum information field length in a frame received for a link station associated with this SAP. If this field is zero, a default value of 600 is used. This parameter is ignored if the STATION_COUNT parameter is zero.

STATION_COUNT: This parameter specifies the maximum number of link stations that may be associated with this SAP. This parameter is ignored if bit 5 of the SAP_OPTIONS is reset to zero. If this parameter is equal to zero, then this SAP can transmit only type 1 LLC frames.

GROUP_MEMBER_COUNT: This parameter specifies the number of GSAPs of which the SAP being opened wishes to become a member. The number specified in this field signals to the adapter how many of the GSAP_0 - GSAP_7 fields are valid. This parameter is ignored if bit 5 or bit 7 of the SAP_OPTIONS is zero.

SAP_GROUP_LIST_PTR: These fields point to a list of Group SAPs, GSAP_0 - GSAP_7, to which the opening SAP belongs.

GSAP_0 - GSAP_7: These fields contain the GSAP values for the Group Service Access Points of which the SAP to be opened wishes to become a member. None of these fields may be skipped (i.e., if membership in 3 GSAPs is desired, the GSAP values must be placed in GSAP_0, GSAP_1, and GSAP_2).

2.18.2 Command Completion

Upon completion of OPEN.SAP, the adapter generates a COMMAND.STATUS interrupt and sets the SSB_CMD field to >0015. The SSB_PARM_0 field is updated with COMMAND_STATUS. The COMMAND_STATUS takes on values according to Table 2-16. The STATION_ID associated with the opened SAP is returned in SSB_PARM_1. If the command fails due to a problem with a Group SAP (error codes >0045 or >0049), the SSB_PARM_2 field will contain the FAILING_GROUP_SAP value.

Table 2-16. OPEN.SAP Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0006	Invalid SAP_OPTIONS
>0008	Unauthorized access priority The maximum access priority allowed is 6, unless altered by net management.
>0042	Parameter exceeds maximum
>0043	Invalid SAP value
>0045	Requested group membership in non-existent group
>0046	Resources not available MAX_SAP number of SAPs are already opened.
>0049	Group SAP has max members and attempted to open another member

2.19 CLOSE.SAP Command

This command is used to deactivate a SAP. A SAP may not be closed if any link stations associated with the SAP are open. A Group SAP may not be closed until all member SAPs have been closed. Any frames received for the specified SAP that are not in the process of being transferred across the System Interface will be purged.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened or if the LLC interface has not been enabled.

ENTRY

SCB_CMD	>0016
SCB_PARM_0	STATION_ID
SCB_PARM_1	>0000

EXIT

SSB_CMD	>0016
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.19.1 Command Initiation

The STATION_ID of the SAP to be closed is placed in SCB_PARM_0. SCB_PARM_1 is ignored by the adapter, but should be set to zero.

2.19.2 Command Completion

Upon completion of CLOSE.SAP, the adapter generates a COMMAND.STATUS interrupt, sets the SSB_CMD field to >0016, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS takes on the values shown in Table 2-17. The STATION_ID of the closed SAP is returned in SSB_PARM_1.

Table 2-17. CLOSE.SAP Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0040	Invalid STATION_ID
>0047	Unclosed link stations on SAP. Must close all link stations first.
>0048	Group SAP cannot close — All member SAPs not closed.
>004C	Sequence Error

2.20 OPEN.STATION Command

OPEN.STATION allocates resources within the adapter to support a connection between a local and a remote link station. The parameters needed by the adapter for allocation of these resources are specified by the user in a Station Parameter Block, which is read by the adapter.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened, or if the LLC interface has not been enabled.

ENTRY

SCB_CMD	>0019
SCB_PARM_0	STATION_PARM_BLOCK (high)
SCB_PARM_1	STATION_PARM_BLOCK (low)

EXIT

SSB_CMD	>0019
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.20.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to the STATION_PARM_BLOCK which is shown in Figure 2.17. The most significant byte of SCB_PARM_0 is ignored.

STATION_PARM_BLOCK			
	+ 0	STATION_ID	
	+ 2	RESERVED	
	+ 4	TIMER_T1	TIMER_T2
	+ 6	TIMER_TI	MAXOUT
	+ 8	MAXIN	MAXOUT_INCR
	+ 10	MAX_RETRY_COUNT	RSAP_VALUE
	+ 12	MAX_I_FIELD	
	+ 14	STATION_OPTIONS	
	+ 16	REMOTE_NODE_ADDRESS_PTR (HI)	
	+ 18	REMOTE_NODE_ADDRESS_PTR (LO)	

Figure 2-17. Station Parameter Block

Station Parameter Block Field Descriptions.

STATION_ID: This field contains the STATION_ID of the SAP under which the new link station is to be established.

TIMER_T1: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

TIMER_T2: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

TIMER_TI: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

MAXOUT: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

MAXIN: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

MAXOUT_INCR: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

MAX_RETRY_COUNT: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

MAX_I_FIELD: As defined for OPEN.SAP. If set to a value other than zero, then that value will be used for this station. If zero, then the value defaults to that value set in the OPEN.SAP command.

RSAP_VALUE: This parameter defines the SAP value of the remote station. The SAP value defined in this field must be for an individual SAP (least significant bit = 0). RSAP_VALUE is used in the DSAP field of transmitted frames and compared to the SSAP field of received frames.

STATION_OPTIONS: The bit functions of the SAP Options field are provided below:

BITS 0-2 (PRIORITY) - This bit field defines the transmission priority for frames transmitted by this station.

BITS 3-15 (RESERVED) - These bits should be set to zero.

REMOTE_NODE_ADDRESS_PTR: This field contains a 24-bit pointer to the location in system memory where the 6-byte ring address of the remote station is stored. The most significant byte of the high order address is ignored.

2.20.2 Command Completion

Upon completion of OPEN.STATION, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >0019, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS takes on a value according to Table 2-18. The STATION_ID of the opened station will be returned in SSB_PARM_1.

Table 2-18. OPEN.STATION Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0008	Unauthorized access priority The maximum access priority allowed is 6, unless altered by net management.
>0040	Invalid STATION_ID
>0042	Parameter exceeded maximum
>0043	Invalid SAP value or SAP value already in use
>0046	Resources not available MAX_STATION number of link stations are already open.
>004F	Invalid remote address — group address invalid

2.21 CLOSE.STATION Command

CLOSE.STATION is used to signal the adapter to initiate the sequence of events necessary to place the specified link station in a closed state.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened or if the LLC interface has not been enabled.

ENTRY

SCB_CMD	>001A
SCB_PARM_0	STATION_ID
SCB_PARM_1	>0000

EXIT

SSB_CMD	>001A
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.21.1 Command Initiation

The STATION_ID of the link station to be closed is placed in SCB_PARM_0. SCB_PARM_1 is ignored by the adapter.

2.21.2 Command Completion

Upon completion of CLOSE.STATION, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >001A, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS takes on one of the values in Table 2-19. The STATION_ID of the closed station is returned in SSB_PARM_1.

Table 2-19. CLOSE.STATION Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0040	Invalid STATION_ID
>004B	Station closed without remote acknowledgment
>004C	Sequence error. Have already issued a close to this link.

2.22 CONNECT.STATION Command

CONNECT.STATION is used to signal the adapter to initiate the protocol necessary to place the local and remote link stations in a data transfer state. The information the adapter needs to establish a logical link is specified by the user in a Connect Parameter Block, which is read by the adapter.

After a CONNECT.STATION command completes successfully, the attached system should assume a DMA-not-ready state. The adapter will generate a TRANSMIT.STATUS interrupt to inform the attached system when the DMA is ready to accept I frames for transmission. This interrupt will occur whether or not a TRANSMIT command has been issued. For more information, refer to the section on the TRANSMIT command.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened or the LLC interface has not been enabled.

ENTRY

SCB_CMD	>001B
SCB_PARM_0	CONNECT_PARM_BLOCK (high)
SCB_PARM_1	CONNECT_PARM_BLOCK (low)

EXIT

SSB_CMD	>001B
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.22.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to the CONNECT_PARM_BLOCK, which is shown in Figure 2-18. The most significant byte of SCB_PARM_0 is ignored.

CONNECT_PARM_BLOCK		
	+ 0	STATION_ID
	+ 2	RESERVED
	+ 4	ROUTING_INFO_PTR (HI)
	+ 6	ROUTING_INFO_PTR (LO)

Figure 2-18. Connect Parameter Block

Connect Parameter Block Field Bit Descriptions.

STATION_ID: This parameter specifies the link station with which a logical connection is desired.

RESERVED: This field is reserved and should be set to zero.

ROUTING_INFO_PTR: This field contains a 24-bit pointer to the system memory location of the Routing Information. The Routing Information is necessary for establishing a link between two stations which are not on the same ring. The Routing Information is ignored if the CONNECT.STATION is issued to a link that has received a SABME. For more information on the routing information field, see the *TMS380 Adapter Chipset User's Guide* or the *IBM Token-Ring Network Architecture Guide* (#6165877). The most significant byte of ROUTING_INFO_PTR(HI) is ignored. The adapter will DMA 18 bytes from the address pointed to by this field. If the value of the pointer is zero, no routing information is used.

2.22.2 Command Completion

Upon completion of CONNECT.STATION, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >001B, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS takes on values according to Table 2-20. The STATION_ID of the connected station is returned in SSB_PARM_1.

Table 2-20. CONNECT.STATION Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0040	Invalid STATION_ID
>0041	Protocol error – Link in invalid state for command
>0044	Invalid Routing Information length
>004D	Unsuccessful connection attempt. The remote station did not accept the connection request.
>004A	Sequence Error

2.23 MODIFY.LLC.PARMS Command

MODIFY.LLC.PARMS is used to modify open link station parameters or default SAP parameters. Parameter values to be modified are passed to the adapter via a Modify Parameter Block.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened or if the LLC Interface has not been enabled.

ENTRY

SCB_CMD	>001C
SCB_PARM_0	MODIFY_PARM_BLOCK (high)
SCB_PARM_1	MODIFY_PARM_BLOCK (low)

EXIT

SSB_CMD	>001C
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	FAILING_GROUP_SAP

2.23.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to the CONNECT_PARM_BLOCK, which is shown in Figure 2-19. The most significant byte of SCB_PARM_0 is ignored.

MODIFY_PARM_BLOCK	+ 0	RESERVED	
	+ 2	STATION_ID	
	+ 4	TIMER_T1	TIMER_T2
	+ 6	TIMER_TI	MAXOUT
	+ 8	MAXIN	MAXOUT_INCR
	+ 10	MAX_RETRY_COUNT	RESERVED
	+ 12	RESERVED	
	+ 14	SAP_OPTIONS	RESERVED
	+ 16	RESERVED	
	+ 18	RESERVED	GROUP_MEMBER_CNT
	+ 20	SAP_GROUP_LIST_PTR (HI)	
	+ 22	SAP_GROUP_LIST_PTR (LO)	

SAP_GROUP_LIST	+ 0	GSAP_0	GSAP_1
	+ 2	GSAP_2	GSAP_3
	+ 4	GSAP_4	GSAP_5
	+ 6	GSAP_6	GSAP_7
	+ 8	GSAP_8	GSAP_9
	+ 10	GSAP_10	GSAP_11
	+ 12	GSAP_12	GSAP_13

Figure 2-19. Modify Parameter Block

MODIFY Parameter Block Field Definitions.

TIMER_T1: This parameter sets the Response Timer value and is specified as an integer between 1 and 10. Timer values are as defined in the OPEN.SAP command. If the value is zero, the current value remains set.

TIMER_T2: This parameter sets the Receive Acknowledge Timer value and is specified as an integer between 1 and 10. Timer values are as defined in the OPEN.SAP command. If the value is zero, the current value will remain set. If the value is greater than 10, the timer is not used.

TIMER_TI: This parameter sets the Inactivity Timer value and is specified as an integer between 1 and 10. Timer values are as defined in the OPEN.SAP command. If the value is zero, the current value remains set.

MAXOUT: This parameter specifies the maximum number of unacknowledged transmitted I-frames that may be outstanding at any one time. If this parameter is set to zero, the current value will remain set. The maximum value for this parameter is 127.

MAXIN: This parameter specifies the maximum number of I-frames that may be received before an acknowledgment is sent. If this parameter is set to zero, the current value will remain set. The maximum value for this parameter is 127.

MAX_XMIT_INCR: This parameter is used to specify the dynamic window increment value. If this value is zero, then the current value remains set.

MAX_RETRY_COUNT: This parameter specifies the default N2 value for link stations associated with SAP_VALUE. The maximum value of this parameter is 255. If this value is zero, then the current value remains set.

SAP_OPTIONS: The bit functions of the SAP Options field are provided below:

BITS 0-2 (ACCESS_PRIORITY) - The value specified in this bit field is placed in the AC field of all frames transmitted from this SAP. This parameter must be filled in.

BITS 3-7 (RESERVED) - These bits should be set to zero.

GROUP_MEMBER_COUNT: This parameter specifies the number of valid fields in the SAP_GROUP_LIST (GSAP_0 - GSAP_13).

SAP_GROUP_LIST_PTR: These fields point to a list of group SAPs as defined below. These fields (GSAP_0 - GSAP_13) are ignored if the GSAP_MEMBER_COUNT parameter is zero.

GSAP_0 - GSAP_13: These fields may be used to either request membership in additional group SAPs or to request that a membership be deleted. If the low-order bit of the SAP value is zero, then the addition of this membership is being requested. If the low-order bit is one, then the request is that this membership be canceled. These fields are ignored if the GSAP_MEMBER_COUNT parameter is zero.

2.23.2 Command Completion

Upon completion of MODIFY.LLC.PARMS, the adapter will generate a COMMAND.STATUS interrupt, set SSB.CMD to >001C, and update SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS will take on values according to Table 2-21. The STATION_ID associated with the command will be returned in SSB_PARM_1. In the event of errors >0045 or >0049, the adapter will update SSB_PARM_2 with the SAP_VALUE of the failing Group SAP.

Table 2-21. MODIFY.LLC.PARMS Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0008	Unauthorized access priority
>0040	Invalid STATION_ID
>0042	Parameter exceeded maximum
>0045	Requested group membership in non-existent Group SAP
>0049	Group SAP has max members
>004E	Member not found in Group SAP

2.24 FLOW.CONTROL Command

FLOW.CONTROL can be used to control the local busy state of a specific link station or of all link stations within a specified SAP. FLOW_OPTIONS are passed to the adapter which specify the state of the local busy status and the local busy status reset condition. A FLOW.CONTROL to STATION_ID of >0000 has no effect.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened, or the LLC interface has not been enabled.

ENTRY

SCB_CMD	>001D
SCB_PARM_0	STATION_ID
SCB_PARM_1	FLOW_OPTIONS

EXIT

SSB_CMD	>001D
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.24.1 Command Initiation

A STATION_ID is placed in SCB_PARM_0 to specify the link station(s) which require data flow modification. A STATION_ID of >xx00 will change the local busy status of all link stations in SAP xx. The FLOW_OPTIONS are placed in SCB_PARM_1. The FLOW_OPTIONS field bit positions are defined below.

FLOW_OPTIONS Field Bit Positions

BIT 0 (LOCAL_BUSY_STATUS) - When set to 0, the specified link station(s) enters the local busy state. Bit 1 is ignored. When set to 1, the specified link stations are reset from a local busy state entered by the condition specified in LOCAL_BUSY_CONDITION (BIT 1).

BIT 1 (LOCAL_BUSY_CONDITION) - When set to 0, a user set local busy condition is reset. When set to 1, an out-of-receive-buffer, a no-receive-command-outstanding, or a receive-canceled state is reset.

BIT 2-7 (reserved) - These bits should be set to zero.

2.24.2 Command Completion

Upon completion of FLOW.CONTROL, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >001D, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND.STATUS takes on values as shown in Table 2-22. The STATION_ID associated with the command is returned in SSB_PARM_1.

Table 2-22. FLOW.CONTROL Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0040	Invalid STATION_ID

2.25 LLC.STATISTICS Command

LLC.STATISTICS is used to read the error counters and statistics for a link station. The error counters may also be reset with this command. The error counters and the LAN header are written to attached system memory at locations pointed to in the Statistics Parameter Block.

A COMMAND.REJECT interrupt will be issued if the adapter has not been opened, or the LLC interface has not been enabled.

ENTRY

SCB_CMD	>001E
SCB_PARM_0	STAT_PARM_BLOCK (high)
SCB_PARM_1	STAT_PARM_BLOCK (low)

EXIT

SSB_CMD	>001E
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	STATION_ID
SSB_PARM_2	>0000

2.25.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields contain a 24-bit pointer to the STAT_PARM_BLOCK, which is shown in Figure 2-20. The most significant byte of SCB_PARM_0 is ignored.

STATS_PARM_BLOCK		
	+ 0	STATION_ID
	+ 2	BUFFER_LENGTH
	+ 4	BUFF_ADDRESS (HI)
	+ 6	BUFF_ADDRESS (LO)
	+ 8	ACTUAL_BUFF_LENGTH
	+ 10	OPTIONS

Figure 2-20. Statistics Parameter Block

Statistics Parameter Block Field Descriptions.

STATION_ID: This parameter specifies the link station whose statistics will be written to attached system memory.

BUFFER_LENGTH: This field contains the length of the buffer pointed to by BUFF_ADDRESS.

BUFF_ADDRESS: This field contains a 24-bit pointer to a buffer in attached system memory where the statistics data is to be written.

ACTUAL_BUFF_LENGTH: The actual length of the statistics data that was requested. This value is returned by the adapter. If the value is greater than the value of BUFFER_LENGTH, then not all of the statistics have been transferred.

OPTIONS: This 16 bit parameter is set by the attached system when the Statistics parameter block is created to indicate actions to be taken by the adapter. The OPTIONS bits to be set by the attached system are defined as follows:

BIT 0 (reset) - If this bit is set to 1, the station error counters are reset to zero after this command is executed.

BIT 1-15 (reserved) - These bits are ignored by the adapter, but should be set to zero.

LLC Statistics Data.

The following is the format of the data that is transferred to the attached system upon execution of the STATION.STATS command.

BYTES 0-1: Number of I-frames transmitted.

BYTES 2-3: Number of I-frames received.

BYTE 4: Number of I-frames received with errors.

BYTE 5: Number of I-frames transmitted ending in error.

BYTES 6-7: Number of times T1 timer expired when not transferring data.

BYTE 8: Last command/response received. LLC Control byte 0.

BYTE 9: Last command/response sent.

BYTE 10: Link primary state. Bit values are shown below.

Link Primary States:
- Bit 0: Closed
- Bit 1: Disconnected
- Bit 2: Disconnecting
- Bit 3: Opening
- Bit 4: Resetting
- Bit 5: FRMR Sent
- Bit 6: FRMR Received
- Bit 7: Opened

BYTE 11: Link secondary state. Bit values are shown below.

Link Secondary States:
- Bit 0: Checkpointing
- Bit 1: Local Busy (user set)
- Bit 2: Local Busy (buffer set)
- Bit 3: Remote Busy
- Bit 4: Rejection
- Bit 5: Clearing
- Bit 6: Dynamic Windowing Algorithm Running
- Bit 7: Reserved

BYTE 12: Send state variable (V(S)).

BYTE 13: Receive state variable (V(R)).

BYTE 14: Last received N(R).

BYTE 15: Length of LAN_HEADER used in transmitting I-frames. This length includes the AC through the RI fields.

BYTES 16-47: LAN_HEADER used in transmitting I-frames.

2.25.2 Command Completion

Upon completion of STATION.STATS, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >001E, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS takes on the values according to Table 2-23. The STATION_ID associated with the command is returned in SSB_PARM_1.

Table 2-23. STATION.STATS Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0015	Log data lost due to not enough space — log reset. If the length is less than eight, then the counters are not reset.
>0040	Invalid STATION_ID

2.26 DIR.INTERRUPT Command

DIR.INTERRUPT can be used to cause the adapter to interrupt the attached system. The adapter reads the SCB, writes a response SSB, and then interrupts the attached system with a COMMAND.STATUS interrupt.

A COMMAND.REJECT will be issued if the LLC Interface has not been enabled.

ENTRY

SCB_CMD	>001F
SCB_PARM_0	>0000
SCB_PARM_1	>0000

EXIT

SSB_CMD	>001F
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.26.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 fields are ignored, but should be set to zero.

2.26.2 Command Completion

Upon completion of DIR.INTERRUPT, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >001F, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS will take on values according to Table 2.24.

Table 2-24. DIR.INTERRUPT Return Codes

VALUE	EXPLANATION
>0000	Good completion

2.27 CONFIG.BRIDGE.PARMS Command

The CONFIG.BRIDGE.PARMS command accomplishes the following:

1. Forces the bridge functional address bit (bit 29) to one in the OPEN.ADAPTER and SET.FUNCTIONAL.ADDRESS commands.
2. Allows the user to set the copy-all-frames options (but not the first-buffer-only) in the OPEN.ADAPTER command. If the attached system tries to set copy-all-frames options in the OPEN.ADAPTER command without first issuing this command, then the adapter will return an error on the OPEN.ADAPTER command.

This command must be issued after adapter initialization and prior to opening the adapter. A COMMAND.REJECT will be issued if the LLC Interface has not been enabled or if the adapter is already opened.

ENTRY

SCB_CMD	>0020
SCB_PARM_0	CONTROL
SCB_PARM_1	>0000

EXIT

SSB_CMD	>0020
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	>0000
SSB_PARM_2	>0000

2.27.1 Command Initiation

The SCB_PARM_0 field contains the CONTROL parameter for this command. If the CONTROL parameter is non-zero then the bridge functional address (>C000 0000 0100) is set. A CONTROL of zero turns off the bridge functional address. The SCB_PARM_1 field is ignored, but should be set to zero.

2.27.2 Command Completion

Upon completion of the CONFIG.BRIDGE.PARMS, the adapter generates a COMMAND.STATUS interrupt, sets SSB-CMD to >0020, and updates SSB_PARM_0 with COMMAND_STATUS. The COMMAND_STATUS will take on values according to Table 2-25.

Table 2-25. CONFIG.BRIDGE.PARMS Return Codes

VALUE	EXPLANATION
>0000	Good completion

2.28 LLC.REALLOCATE Command

The LLC.REALLOCATE command reallocates memory for link control blocks. Additional link control blocks can be allocated for a SAP. Alternately, link control blocks previously allocated to a SAP can be returned to the adapter pool (freed). This effectively alters the STATION_COUNT parameter of the OPEN.SAP command.

A COMMAND.REJECT will be issued if the LLC Interface has not been enabled.

ENTRY

SCB_CMD	>0021	
SCB_PARM_0	STATION_ID	
SCB_PARM_1	OPTIONS	STATION_COUNT

EXIT

SSB_CMD	>0021	
SSB_PARM_0	COMMAND_STATUS	
SSB_PARM_1	STATION_ID	
SSB_PARM_2	ADAPTER_COUNT	SAP_COUNT

2.28.1 Command Initiation

The SCB_PARM_0 field contains the STATION_ID to or from which the control blocks are to be allocated. The SCB_PARM_1 field contains two one-byte parameters described below.

LLC.REALLOCATE Parameter Descriptions.

OPTIONS:

Bit 0: If this bit is equal to one then the link control blocks are to be taken from the adapter pool and added to the SAP pool. If this bit is equal to zero, then the link control blocks are to be taken from the SAP pool and added to the adapter pool.

Bits 1-7: (reserved). Should be set to zero.

STATION_COUNT: This byte parameter is the number of link control blocks to be reallocated.

2.28.2 Command Completion

Upon completion of LLC.REALLOCATE, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD to >0021 and updates SSB_PARM_0 with COMMAND_STATUS, SSB_PARM_1 is updated with the STATION_ID of the station or SAP in question. SSB_PARM_2 is updated with the ADAPTER_COUNT and the SAP_COUNT parameters described below.

Table 2-26. LLC.REALLOCATE Return Codes

VALUE	EXPLANATION
>0000	Good completion
>0040	Invalid STATION_ID

LLC.REALLOCATE Return Parameters.

ADAPTER_COUNT: The number of link control blocks available in the adapter pool (not assigned to any SAP) when the command completes. This byte is valid only if the COMMAND_STATUS was >0000 or >0040.

SAP_COUNT: The number of link control blocks assigned to the SAP designated by the STATION_ID when the command completes. This byte is valid only if the COMMAND_STATUS was >0000.

2.29 TIMER.SET Command

The TIMER.SET command is used to enable and disable timer interrupts generated by the adapter to the attached system. The timer duration is passed as a parameter of this command and specifies the number of 10-millisecond intervals to be used for the timer period. If the TIMER.SET command is issued to enable a timer that has already been started, the old request will be canceled and the timer restarted with the new timer period.

A COMMAND.REJECT will be issued if the LLC Interface has not been enabled.

ENTRY

SCB_CMD	>0022	
SCB_PARM_0	NOT USED	TIMER COUNT
SCB_PARM_1	NOT USED	

EXIT

SSB_CMD	>0022
SSB_PARM_0	COMMAND_STATUS
SSB_PARM_1	NOT USED
SSB_PARM_2	NOT USED

2.29.1 Command Initiation

The LSB of the SCB_PARM_0 field contains the timer count described below. The MSB of the SCB_PARM_0 and the SCB_PARM_1 fields are ignored and should be set to zero.

TIMER.SET Parameter Description.

TIMER_COUNT: This parameter specifies the number of 10-millisecond timer intervals that will make up the requested timer period. A value from >01 to >FF will start or restart the timer. A value of >0 will stop the timer.

2.29.2 Command Completion

Upon completion of TIMER.SET, the adapter will generate a COMMAND.STATUS interrupt, set the SSB_CMD to >0022 and update SSB_PARM_0 with COMMAND STATUS. The SSB_PARM_1 and SSB_PARM_2 fields should be ignored. The COMMAND_STATUS will take on values according to Table 2-27.

Table 2-27. TIMER.SET Return Codes

VALUE	EXPLANATION
>0000	Good completion

2.30 Transmit Operation

The TMS380 adapter with LLC will support the transmission of seven different types of frames. These are listed below, each with a brief description.

Direct Frame. The direct frame is used to transmit data from the direct station. All STATION_IDs other than a direct station are invalid for this frame. For this frame, the entire frame must be prepared by the attached system. MAC frames or LLC frames may be transmitted using this type of frame. This is the only way that MAC frames may be transmitted.

UI Frame. The UI frame is used to transmit an LLC unnumbered information frame for a SAP. This frame is an unacknowledged data frame sent by LLC. The attached system must build the MAC header and data portions of the frame. The adapter builds the LLC header from information provided in the STATION_ID and REMOTE_SAP fields of the transmit list. The user does not account for or save space for the LLC header.

XID Command. This frame is an LLC XID Command frame with the Poll bit set to one. The attached system provides the MAC header. If the XID_HANDLER bit (bit 4) of the SAP_OPTIONS on the OPEN.SAP for this SAP was set to one, then the attached system must also provide the data field. The adapter provides the LLC header, and if the XID_HANDLER bit was set to zero, the data field. If the attached system wishes to add a data field, it must leave the first three bytes of that field empty for the adapter to fill in. The attached system must always have at least three bytes in the data field. The user does not account for or save space for the LLC header. The adapter builds the LLC header from information provided in the STATION_ID and REMOTE_SAP fields of the transmit list.

XID Response Final. This is an LLC XID Response frame with the Final bit set to one. This frame should be transmitted only by those SAPs which were opened with the XID_HANDLER bit on. The adapter does not, however, prevent this frame from being transmitted otherwise. The attached system provides the MAC header and data field. The adapter provides the LLC header. The adapter builds the LLC header from information provided in the STATION_ID and REMOTE_SAP fields of the transmit list. The user need not account for or save space for the LLC header.

XID Response Not Final. This is an LLC XID Response frame with the Final bit set to zero. This frame should be transmitted only by those SAPs which were opened with the XID_HANDLER bit on. The attached system provides the MAC header and data field. The adapter provides the LLC header. The adapter builds the LLC header from information provided in the STATION_ID and REMOTE_SAP fields of the transmit list. The user need not account for or save space for the LLC header.

Test Command. This frame is an LLC Test Command frame with the Poll bit set to one. The attached system provides the MAC header and optional data field. The adapter builds the LLC header from information provided in the STATION_ID and REMOTE_SAP fields of the transmit list. The user need not account for or save space for the LLC header.

I Frame. This frame is used to transmit data for an LLC type 2 connection. This frame is transmitted only by a link station. The attached system provides only the data field. The adapter provides the LAN and LLC headers. The adapter builds the LLC header from information provided in the STATION_ID field of the transmit list. The user does not account for or save space for the LAN or LLC headers. This frame is an acknowledged information frame. The adapter handles waiting for a response frame, and will automatically retry to guarantee delivery of data in an I frame. On reception of an I frame, the adapter will also handle the transmission of the acknowledgment frame.

2.31 TRANSMIT Command

The TRANSMIT command is used to transmit all frame types. Some frames are built entirely in the attached system using the logical frame format described in Section 1 and are moved from attached system memory to adapter internal buffers, via DMA, upon initiation of this command. Other frames are built partially by the attached system and completed by the adapter after DMA completes.

A COMMAND.REJECT interrupt will be posted if the adapter has not been opened, if there is already an executing TRANSMIT command, or if the address passed in the SCB_PARM_0 and SCB_PARM_1 is not aligned on a word boundary.

ENTRY

SCB_CMD	>0004
SCB_PARM_0	XMIT_PARM_BLOCK (high)
SCB_PARM_1	XMIT_PARM_BLOCK (low)

EXIT

SSB_CMD	>0004
SSB_PARM_0	XMIT_STATUS
SSB_PARM_1	XMIT_PARM_LIST (high)
SSB_PARM_2	XMIT_PARM_LIST (low)

2.31.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 contain a 24-bit word aligned address which points to a Transmit Parameter List. The most significant byte of SCB_PARM_0 is ignored. The format of the Transmit Parameter List is shown in Figure 2-21. Transmit Parameter Lists must be aligned on even word boundaries.

XMIT_PARM_LIST			
	+ 0	FORWARD_POINTER (high)	
	+ 2	FORWARD_POINTER (low)	
	+ 4	TRANSMIT_CSTAT	
	+ 6	FRAME_SIZE	
	+ 8	DATA_COUNT	
	+ 10	DATA_ADDRESS (high)	
	+ 12	DATA_ADDRESS (low)	
	+ 14	DATA_COUNT	
	+ 16	DATA_ADDRESS (high)	
	+ 18	DATA_ADDRESS (low)	
	+ 20	DATA_COUNT	
	+ 22	DATA_ADDRESS (high)	
	+ 24	DATA_ADDRESS (low)	
	+ 26	STATION_ID	
	+ 28	REMOTE_SAP	HEADER_LENGTH

Figure 2-21. TRANSMIT Parameter List

Transmit Parameter List Fields.

FORWARD__POINTER: This 32-bit field contains a 24-bit pointer to the next Transmit Parameter List in the chain. When the pointer is odd, the current Transmit Parameter List is the last in the chain. The adapter will continue to process Transmit Parameter Lists until it reads an odd FORWARD__POINTER, at which time the adapter will wait for the last frame (list with ODD address) to be transmitted before exiting the command. If the system updates the FORWARD__POINTER before the transmission of the last frame is completed, the adapter will continue to process Transmit Parameter Lists. The system must update the FORWARD__POINTER from the most significant byte to the least significant byte to ensure that the address is valid before changing to an even address. The FORWARD__POINTER should not be initialized to point to itself, as problems may occur due to the pipelined nature of the adapter's list processing. The adapter will not alter this parameter.

TRANSMIT__CSTAT: This 16-bit parameter is set by the attached system when the Transmit Parameter List is created. It is overwritten by the adapter to report frame completion status. When initially set by the attached system, this parameter field is referred to as the TRANSMIT__CSTAT__REQUEST field. After a frame completes transmission, the adapter will write TRANSMIT__CSTAT__COMPLETE to the list which has START__FRAME set to one. These bits indicate the completion status of the frame, not the TRANSMIT command itself.

TRANSMIT__CSTAT__REQUEST: The CSTAT bits are set by the attached system as follows:

BIT 0 (VALID): The adapter waits for bit 0 to be set to a one before processing the current Transmit Parameter List. The attached system must issue a TRANSMIT.VALID interrupt request when changing Bit 0 from zero to one. This bit is ignored unless the list is an anticipated start of frame (i.e., follows end of frame or is first list of command).

BIT 1 (FRAME__COMPLETE): Should be reset to zero.

BIT 2 (START__FRAME): Must be set to one for a list which defines the start of a frame.

BIT 3 (END__FRAME): Must be set to one for a list which defines the end of a frame.

BIT 4 (FRAME__INTERRUPT): When set to one, an adapter-to-attached-system interrupt is generated when the frame has been transmitted, rather than waiting for all frames on the chain to be transmitted. This bit is ignored unless START__FRAME (bit 2) is a one.

BIT 5 (RESERVED): This bit must be reset to zero.

BIT 6 (PASS_CRC): When this bit is set to one, the adapter assumes the CRC to be transmitted with the frame is contained in the last four bytes of the frame data. In this case, the adapter does not generate the CRC on transmit but uses the CRC passed with frame data. Note that the CRC value is not checked. This option can be used by adapters, such as MAC-layer bridges, that must forward frames without altering the CRC. This bit is ignored unless the START_FRAME bit (bit 2) is set to one.

BIT 7 (PASS_SOURCE_ADDRESS): When this bit is set to one, the adapter will transmit the frame with the source address as given by the host. The adapter will not overwrite the source address with the adapter node address. This option can be used by adapters, such as MAC-layer bridges, that must forward frames without altering the source address. This bit is ignored unless the START_FRAME bit (bit 2) is set to one.

BITS 8-10 (FRAME_TYPE): This field is used to indicate the type of frame to be transmitted. These bits should be set to zero unless the LLC Interface has been enabled. The frame types that may be transmitted are listed in Table 2-28.

Table 2-28. Transmit Frame Types

BIT			
8	9	10	FRAME TYPE
0	0	0	Direct Frame
0	0	1	UI Frame
0	1	0	XID Command
0	1	1	XID Resp. Final
1	0	0	XID Resp. Not Final
1	0	1	Test Command
1	1	0	I Frame
1	1	1	Invalid frame type

BITS 10-15 (RESERVED): These bits must be reset to zero.

TRANSMIT_CSTAT_COMPLETE: The completion code for the transmitted frame is written to this field in the list that has START_FRAME bit equal to one when the adapter has completed transmission of the frame. CSTATs that are not in a list defining the start of a frame, are not altered by the adapter. The TRANSMIT_CSTAT_COMPLETE bit definitions are shown below.

BIT 0 (VALID): Reset to zero.

BIT 1 (COMPLETE): Set to one.

BIT 2 (FRAME_START): Bit 2 has the same value as specified by the attached system in TRANSMIT_CSTAT_REQUEST.

BIT 3 (FRAME_END): Bit 3 has the same value as specified by the attached system in TRANSMIT_CSTAT_REQUEST.

BIT 4 (INTERRUPT_FRAME): Bit 4 has the same value as specified by the attached system in TRANSMIT_CSTAT_REQUEST.

BIT 5 (TRANSMIT_ERROR): Bit 5 will be set to one if the frame transmit or strip process was in error, or if a non-fatal error occurred in processing the transmit list. A non-fatal error will not halt list processing. If this bit is set to one, then Bits 8-15 will contain an error reason code instead of the stripped FS byte. List processing will continue.

BIT 6 (PASS_CRC): This bit reflects the state of bit 6 in the TRANSMIT_CSTAT_REQUEST. This bit is valid only if the START_FRAME bit (bit 2) is set to one.

BIT 7 (PASS_SOURCE_ADDRESS): This bit reflects the state of bit 7 in the TRANSMIT_CSTAT_REQUEST. This bit is valid only if the START_FRAME bit (bit 2) is set to one.

BITS 8-15 (STRIP_FS): If TRANSMIT_ERROR (bit 5) is set to zero, then this field contains a copy of the FS byte returned when the transmitted frame is stripped off the ring. If TRANSMIT_ERROR is set to one, this field contains an error reason code as shown in Table 2-29.

Table 2-29. Transmit Error Codes

ERROR CODE	EXPLANATION
>08	Unauthorized access priority
>23	Error in frame transmit or strip
>24	Unauthorized MAC frame
>27	Link not transmitting I frames
>28	Invalid transmit frame length An XID frame had too much data
>40	Invalid STATION ID
>41	Protocol Error. This error code will be returned if an I frame is issued before the DMA is ready
>44	Invalid routing Information length
>F0	Invalid frame type (111)
>FE	I-frame DMA'd into adapter. Link now in not-ready state
>FF	I-frame DMA'd. Link now ready to DMA another frame

FRAME_SIZE: This 16-bit field contains the number of bytes to be transferred from the attached system for this frame. The FRAME_SIZE value includes all data provided by the attached system. FRAME_SIZE does not include headers and/or trailers appended by the adapter. This parameter is valid only in the Transmit Parameter List which has the START_FRAME bit set to one. FRAME_SIZE must, however, be non-zero in all lists. The adapter will not alter this parameter.

DATA_COUNT: This 16-bit field contains the number of bytes to be read at the address defined by DATA_ADDRESS. There can be a maximum of three DATA_COUNT/DATA_ADDRESS parameters per Transmit Parameter List. If Bit 0 is zero, then this DATA_COUNT is the last DATA_COUNT in the Transmit Parameter List. Bit 0 of the third DATA_COUNT is ignored. A DATA_COUNT of 0 is permitted (with or without Bit 0 set). The sum of the used DATA_COUNT parameters must equal the FRAME_SIZE specified in the list which has start_frame set to one. The DATA_COUNT can be even or odd. The adapter will not alter this parameter.

DATA_ADDRESS: This 32-bit field contains a 24-bit pointer to a portion of (or the entire) logical frame residing in attached system memory. DATA_ADDRESS may be even or odd. The adapter ignores the most significant byte of this field.

STATION_ID: This field contains the STATION_ID of the SAP or link station from which the frame is to be transmitted. This value is valid only in start-of-frame lists.

REMOTE_SAP: This parameter defines the SAP value at the destination station to which the frame is to be sent. This parameter is not used for I frame transmission. This value is only valid in start-of-frame lists.

HEADER_LENGTH: This parameter defines the length of the MAC header, including any routing information. The source routing bit in the source address field will be automatically set if this value is greater than 14. This value is not valid for I frames.

2.31.2 Command Execution

The attached system can create a circular chain of Transmit Parameter Lists by setting the FORWARD_POINTER of the last Transmit Parameter list to the address of the first list. The valid bit of TRANSMIT_CSTAT_REQUEST is manipulated to initiate and suspend frame transmission. When the adapter reads a list with the FRAME_START bit set to one and the valid bit reset to zero, it will suspend processing until a TRANSMIT.VALID interrupt request is issued by the attached system. The attached system is not notified of a transmit suspended condition by the adapter.

If a fixed Transmit Chain technique is utilized and more than one list is used to transmit a single frame, lists that do not have the FRAME_START bit set should have the valid bit reset to zero, since the adapter does not alter the TRANSMIT_CSTAT field for lists that do not have the FRAME_START bit set. Re-validating of the start of frame list will also release the remaining frame lists if the valid bits were initially set.

A circular chain of one frame should not be used due to the pipelined nature of Transmit Parameter List processing. An implementation of this nature can cause the adapter to send the same frame twice.

If the adapter is to read data to an internal odd byte address (due to a previous odd data count), it will transfer a single byte and transfer the remaining data starting at an even internal address.

Since Transmit Lists may be added dynamically to the Transmit Parameter List chain, a test should be made following a TRANSMIT.STATUS interrupt to determine if the adapter has processed all frames that the attached system has placed in the chain. If frames have been added to the chain subsequent to the TRANSMIT command exit,

another TRANSMIT command should be executed with the SCB_PARM_0 and SCB_PARM_1 set to the address of the first valid list.

A chain of transmit lists may contain multiple frames. These frames can be of any type and can be of multiple types.

2.31.3 Command Completion

A TRANSMIT.STATUS interrupt will be generated when one of the following conditions occurs during processing of the TRANSMIT command:

- All the frames specified by the Transmit Parameter List chain have been transmitted.
- A TRANSMIT.HALT command has been issued and completed.
- A frame, other than an I-frame, that had the FRAME_INTERRUPT bit set in TRANSMIT_CSTAT has been transmitted.
- The FRAME_INTERRUPT bit is set, and an I-frame has been DMA'd into the adapter and is being held.
- An I-frame has been acknowledged by the remote station.
- A fatal list error is detected.
- The adapter is ready to DMA another I-frame.

Prior to issuing the TRANSMIT.STATUS interrupt, the adapter will update SSB_PARM_0 with the XMIT.STATUS completion code and SSB_PARM_1/SSB_PARM_2 with the address of the last Transmit Parameter List processed by the adapter if bits 0,1, or 2 are set. If bits 3 or 4 of XMIT_STATUS are set, the SSB_PARM_1 will be updated with the related STATION_ID, and SSB_PARM_2 will have no meaning. The bit definitions of XMIT_STATUS are listed below.

XMIT_STATUS Bit Definitions.

BIT 0 (COMMAND_COMPLETE): Set to one to indicate that the TRANSMIT command has completed. The system must issue another TRANSMIT command to transmit additional frames. SSB_PARM_1 and SSB_PARM_2 will contain a pointer to the Transmit Parameter List of the last frame transmitted. This bit is also set as a result of a TRANSMIT_HALT command. The COMMAND_COMPLETE and FRAME_COMPLETE bits are not set at the same time.

BIT 1 (FRAME_COMPLETE): When set to one, this bit indicates that a frame has been transmitted and the INTERRUPT_FRAME bit was set in TRANSMIT_CSTAT_REQUEST. Since frames in the Transmit Parameter List chain may be transmitted faster than the system can respond to the interrupts and/or faster than the adapter can cause the interrupts, this bit can report the completion of more than one frame at a time. SSB_PARM_1 and SSB_PARM_2 will contain a pointer to the Transmit Parameter List of the last frame transmitted. If lists with the FRAME_INTERRUPT bit set are intermixed with lists that do not have the FRAME_INTERRUPT bit set, FRAME_COMPLETE can include frames that did not have FRAME_INTERRUPT set. The attached system should check the TRANSMIT_ERROR bit (bit 5) of the CSTAT in the returned list for possible non-fatal errors.

BIT 2 (LIST_ERROR): Bit 2 will be set to one if there is an error in one of the lists that comprise the frame. Bits 8-13 define the error. The TRANSMIT command will be terminated and the system must issue another TRANSMIT command to continue transmission. SSB_PARM_1 and SSB_PARM_2 contain a pointer to the list that starts the frame with errors. The TRANSMIT.STATUS interrupt for LIST_ERROR will not be generated until all other transmit status has been posted. The CSTATs of lists found to be in error are not altered by the adapter. Neither FRAME_COMPLETE nor COMMAND_COMPLETE bits will be set with LIST_ERROR.

BIT 3 (I_FRAME_ACK): Bit 3 will be set to one to indicate that an I-frame has been acknowledged by the remote station. When this bit is set, bits 8-15 will indicate the number of I-frames that were acknowledged. When this bit is set, the SSB_PARM1 will indicate the link station associated with this SSB, and SSB_PARM2 will have no meaning. When this bit is set, READY/NOT_READY (bit 4) will indicate whether the adapter can accept more I frames for transmission.

BIT 4 (READY/NOT_READY): Bit 4 will be used to indicate whether a link station is ready to accept further I-frames from the attached system. If this bit is set to one, then the link station can accept I-frames for processing. When the link is ready, the host can DMA I-frames up to the number controlled by this link's transmit window. The adapter can hold the same number of unacknowledged I-frames as the transmit window size. When this bit is set, the SSB_PARM1 will indicate the link station associated with this SSB, and SSB_PARM2 will be zero. When a CONNECT.STATION command has completed, the attached system should assume a NOT_READY state and wait for a READY Transmit interrupt. This interrupt will occur when the adapter is ready for I-frame transmission, whether or not a Transmit command has been issued.

BITS 5-7 (RESERVED): Reset to zero.

BIT 8 (FRAME_SIZE_ERROR): Bit 8 will be set to one if FRAME_SIZE does not equal the sum of the valid DATA COUNT fields or if FRAME_SIZE is less than the required header plus one byte of Information Field (15 bytes plus Routing Field), or FRAME_SIZE was specified as zero in any list, except in lists which define I frames.

BIT 9 (TRANSMIT_THRESHOLD): Bit 9 will be set to one if FRAME_SIZE is greater than the product of (BUFFER_SIZE - 8) and the TRANSMIT_BUFFER_MAXIMUM_COUNT parameters from the OPEN command.

BIT 10 (ODD_ADDRESS): Bit 10 will be set to one if an odd FORWARD_POINTER value is read on a list that does not have END_FRAME set to 1.

BIT 11 (FRAME_ERROR): Bit 11 will be set to one if the START_FRAME bit is set to one on a list that is not an anticipated start of frame or the START_FRAME bit is zero on an anticipated start of frame.

BITS 12-13 (RESERVED): Reset to zero.

BIT 14 (ILLEGAL_FRAME_FORMAT): Bit 14 will be set to one if bit 0 of the FC field was set to one. This bit will only be set if the LLC Interface is not enabled. If the LLC Interface has been enabled, this error is a non-fatal list error, and will be indicated in the CSTAT of the associated list.

BIT 15 (RESERVED): Reset to zero.

2.32 TRANSMIT.HALT Command

The TRANSMIT.HALT command is used to interrupt the Transmit List chain. Following recognition of this command, the adapter will terminate the transmit chain as soon as possible. Any frames queued in the adapter will be purged and the TRANSMIT command will be terminated by posting a TRANSMIT.STATUS interrupt and updating SSB_PARM_0 with XMIT_STATUS and SSB_PARM_1 / SSB_PARM_2 with a pointer to the last Transmit Parameter List processed by the adapter. If TRANSMIT.HALT is issued and no frames have been transmitted, SSB_PARM_1 and SSB_PARM_2 will be cleared.

This command is ignored by the adapter if there is not an executing TRANSMIT command or if the adapter has not been opened. A COMMAND.REJECT will be issued if the LLC Interface has been enabled.

ENTRY

SCB_CMD	>0005
SCB_PARM_0	>0000
SCB_PARM_1	>0000

EXIT

SSB_CMD	>0004
SSB_PARM_0	XMIT_STATUS
SSB_PARM_1	XMIT_PARM_LIST (high)
SSB_PARM_2	XMIT_PARM_LIST (low)

2.32.1 Command Initiation

TRANSMIT.HALT does not require a command parameter block. Both the SCB_PARM_0 and SCB_PARM_1 fields are ignored, but should be set to zero.

2.32.2 Command Completion

Upon completion of TRANSMIT.HALT, the adapter generates a COMMAND.STATUS interrupt, sets SSB_CMD is set to >0004, updates SSB_CMD_0 with COMMAND_STATUS of the TRANSMIT command, and updates SSB_PARM_1/SSB_PARM_2 with a pointer to the last Transmit Parameter List processed by the adapter.

2.33 RECEIVE Command

The RECEIVE command is used to receive frames from other stations on the ring. This command is normally issued only once (after OPEN), since receive data may be dynamically added to a Receive Parameter List chain. The RECEIVE command can be terminated due to a list error.

The logical format of received frames passed from the adapter to the attached system is identical to the logical format shown in Figure 2-6. The Access Control, Frame Control, Destination Address, Source Address, any Routing Information, and LLC fields are transferred to the attached system as they were received from the ring.

ENTRY

SCB_CMD	>0006
SCB_PARM_0	RCV_PARM_LIST (high)
SCB_PARM_1	RCV_PARM_LIST (low)

EXIT

SSB_CMD	>0006
SSB_PARM_0	RCV_STATUS
SSB_PARM_1	RCV_PARM_LIST (high)
SSB_PARM_2	RCV_PARM_LIST (low)

2.33.1 Command Initiation

The SCB_PARM_0 and SCB_PARM_1 contain a 24-bit word-aligned address which points to a Receive Parameter List. The high-order byte of SCB_PARM_0 is ignored. The format of the Receive Parameter List is shown in Figure 2-22. Receive Parameter Lists must be aligned on even word boundaries.

RCV_PARM_LIST		
	+ 0	FORWARD_POINTER (high)
	+ 2	FORWARD_POINTER (low)
	+ 4	RECEIVE_CSTAT
	+ 6	FRAME_SIZE
	+ 8	DATA_COUNT
	+ 10	DATA_ADDRESS (high)
	+ 12	DATA_ADDRESS (low)
	+ 14	DATA_COUNT
	+ 16	DATA_ADDRESS (high)
	+ 18	DATA_ADDRESS (low)
	+ 20	DATA_COUNT
	+ 22	DATA_ADDRESS (high)
	+ 24	DATA_ADDRESS (low)

Figure 2-22. RECEIVE Parameter List

The definitions of the FORWARD_POINTER, DATA_COUNT, and DATA_ADDRESS fields are the same as for the Transmit Parameter List. The RECEIVE_CSTAT field definition is given below.

RECEIVE_CSTAT: This 16-bit parameter is set by the attached system when the Receive Parameter List is created. It is overwritten by the adapter to report frame completion status. When initially set by the attached system, this parameter field is referred to as the RECEIVE_CSTAT_REQUEST field. After a frame has been received, the adapter will write RECEIVE_CSTAT_COMPLETE to lists which start or end a frame. These bits indicate the completion status of the frame, not the RECEIVE command itself. However, if the forward pointer is odd, this field will not be updated until a new list is given to the adapter.

RECEIVE_CSTAT_REQUEST: The RECEIVE_CSTAT bits are set by the attached system as follows:

BIT 0 (VALID):The adapter will wait for bit 0 to be set to a one before processing the current Receive Parameter List. The attached system must issue a RECEIVE.VALID interrupt request when changing Bit 0 from zero to one. This bit is examined for every Receive Parameter List.

BIT 1 (FRAME_COMPLETE): Should be reset to zero.

BIT 2 (START_FRAME): Should be reset to zero.

BIT 3 (END_FRAME): Should be reset to zero.

BIT 4 (FRAME_INTERRUPT): When set to one, an adapter-to-attached system interrupt is generated when a frame has been received. This bit is ignored unless a Isit starts or ends a frame.

BIT 5 (INTERFRAME_WAIT): When this bit is set to one, the adapter will interrupt the attached system when a frame has been received. The adapter will then assume a receive-suspended state, waiting for the attached system to issue a RECEIVE.VALID interrrupt. If the LLC Interface has not been enabled, then the receive-suspended state is cleared by a RECEIVE.CONTINUE interrupt. See Chapter 4 of the *TMS380 Adapter Chipset User's Guide* for detail. This bit is ignored unless a list starts or ends a frame.

BIT 6 (PASS_CRC): When set, the adapter will include the frame's CRC in the information passed to the attached system. The CRC will be the last four bytes passed to the attached system. The additional four bytes will be reflected in the FRAME_LENGTH field of the receive list. This bit is ignored in lists that do not start a frame.

BITS 7-15 (RESERVED): Should be reset to zero.

RECEIVE_CSTAT_COMPLETE: The completion code for the received frame is written to this field in lists which start or end a frame. RECEIVE_CSTATs that are not in lists that define the start or end of a frame are not altered by the adapter. The RECEIVE_CSTAT_COMPLETE bit definitions are shown below.

BIT 0 (VALID): Reset to zero.

BIT 1 (FRAME_COMPLETE): Set to one.

BIT 2 (FRAME_START): Set to one on the list which starts the frame.

BIT 3 (FRAME_END): Set to one on the list which ends the frame.

BITS 4-5 (RESERVED): Reset to zero.

BIT 6 (PASS_CRC): This bit reflects the state of the PASS_CRC bit in the RECEIVE_CSTAT_REQUEST. This bit is valid only in lists that have the FRAME_START bit (bit 2) set to one.

BIT 7 (RESERVED): Reset to zero.

BITS 8-13 (RECEIVE_FS): On lists with start_frame set to one, this field will contain the Frame Status field from the received frame.

BITS 14-15 (ADDRESS_MATCH): When DLC software is used in conjunction with the TMS38021 Protocol Handler, these bits will contain the codes shown in the following table:

Address Match Codes

CODE BIT 14	CODE BIT 15	DEFINITION
0	0	No address Match (Frame copied due to "Copy all Frames")
0	1	Internally address matched
1	0	Externally matched
1	1	Internally and Externally Matched

When the Bridge Options software is used conjunction with the TMS38020 Protocol Handler, these bits have identical meaning. However, the last two codes shown in the table ('10' or '11') will never occur when using the TMS38020.

2.33.2 Command Execution

If the LLC interface is enabled, the following method for routing frame data is to be used. The adapter, upon receiving a frame, updates the Interface Control Block (see Section 2.6) with header information and posts a RECEIVE.PENDING interrupt to the attached system.

The attached system should then read the Interface Control Block (ICB), via DIO, to determine what action needs to be taken. The ICB indicates which SAP or link station the frame is destined for, the lengths of the MAC and LLC headers, and the length of the frame. It also indicates from whom the frame is. The attached system may transfer the frame data to its memory by updating the current Receive Parameter List and issuing a RECEIVE.VALID interrupt. If the attached system does not want the frame, a RECEIVE.CANCEL interrupt may be issued and the frame will be purged from the adapter's internal buffers. The RECEIVE.PENDING interrupt must be answered by the attached system.

Once the adapter has begun to DMA the frame data to the attached system's buffers, if it reaches an invalid receive list, it will suspend operation but does not notify the attached system. If an odd forward pointer is reached, then the adapter will suspend the receive and will notify the attached system. At this point, the attached system may continue the receive process by adding to the receive list chain and issuing a RECEIVE.VALID interrupt. At this point the attached system may also purge the remainder of the frame by issuing a RECEIVE.CANCEL interrupt. Note that the RECEIVE.VALID will start the receive list processing no matter what caused it to stop (valid bit or odd forward pointer). A typical receive flow for an adapter with LLC enabled is shown in Figure 2-23.

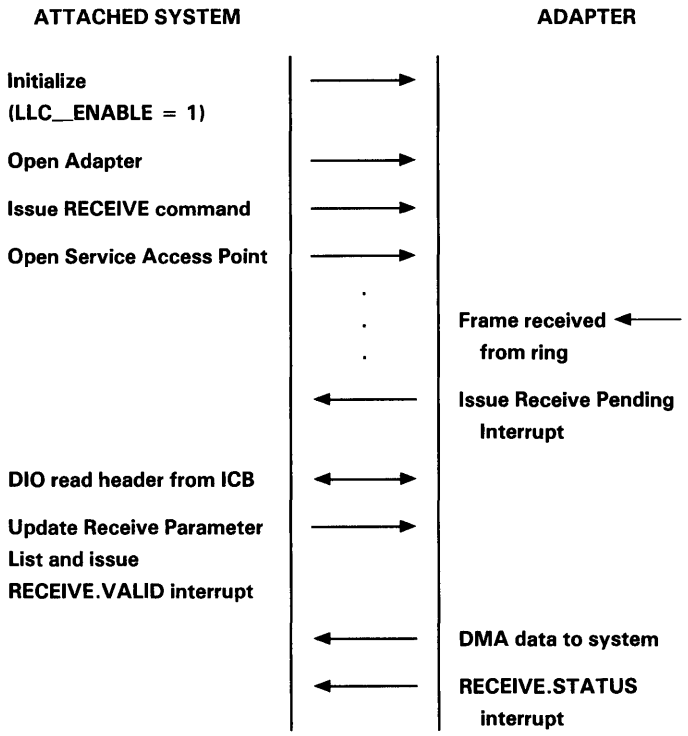


Figure 2-23. LLC RECEIVE Command Flow

Alternately, when the LLC interface is not enabled, the attached system can create a circular chain of Receive Parameter Lists by setting the FORWARD_POINTER of the last Receive Parameter list to the address of the first list. The valid bit of RECEIVE_CSTAT_REQUEST is manipulated to control the flow of data to the attached system. When the adapter reads a list with the valid bit reset, it will suspend the RECEIVE command until a RECEIVE.VALID interrupt request is issued. The attached system is not notified of this receive suspended condition by the adapter. If the adapter reads an odd FORWARD_POINTER or if the FRAME_INTERRUPT bit is set in the RECEIVE_CSTAT, the adapter will suspend the receive command and interrupt the attached system. The adapter will resume processing the RECEIVE command when the attached system issues a RECEIVE.CONTINUE interrupt. For more information on receive operation without the LLC interface enabled, refer to Chapter 4 of the *TMS380 Adapter Chipset User's Guide.*

2.33.3 RECEIVE.STATUS Interrupt

A RECEIVE.STATUS interrupt will be generated when the Receive Parameter List chain has ended (odd address in FORWARD_POINTER) or when a frame is copied into a list that has the FRAME_INTERRUPT bit set in the RECEIVE_CSTAT field. The adapter updates SSB_PARM_0 with the RECEIVE_COMPLETE code and SSB_PARM_1 / SSB_PARM_2 with a 24-bit pointer to the last Receive Parameter List processed by the adapter. The RECEIVE_COMPLETE bit definitions are listed below.

RECEIVE_COMPLETE Field Bit Definitions.

BIT 0 (FRAME_COMPLETE): Bit 0 is set to one when a frame has been received and the the FRAME_INTERRUPT bit was set in RECEIVE_CSTAT. Since frames may be received and transferred faster than the attached system can respond to the interrupts and/or faster than the adapter can cause the interrupts, the RECEIVE.STATUS interrupt may report the arrival of more than one frame at a time. The SSB_PARM_1 and SSB_PARM_2 contain the Receive Parameter List address of the last frame transferred to the system. If lists with the FRAME_INTERRUPT bit set are intermixed with lists that do not have the FRAME_INTERRUPT bit set, RECEIVE.STATUS can include frames that did not have the FRAME_INTERRUPT bit set. The FRAME_COMPLETE bit will not be set with the RECEIVE_SUSPENDED bit also set.

BIT 1 (RECEIVE_SUSPENDED): Bit 1 is set to one when the adapter detects an odd address in the FORWARD_POINTER field of a Receive Parameter List. SSB_PARM_1 and SSB_PARM_2 will contain the address of the list which has an odd FORWARD_POINTER. The attached system must update the FORWARD_POINTER and issue a RECEIVE.VALID interrupt (RECEIVE.CONTINUE if the LLC interface is not enabled) or a RECEIVE.CANCEL to resume the RECEIVE command processing. The RECEIVE_SUSPENDED bit will not be set with the FRAME_COMPLETE bit also set.

BITS 2-15 (RESERVED): Reset to zero.

3. EPROM-Based Adapters

For adapter designs requiring non-volatile program storage, the DLC software is available in two 16K × 8 EPROMs, which are mapped into the address space on the LAN Adapter bus. This section describes memory map and hardware implementation requirements for the TMS380 adapter with DLC residing in EPROM storage. A discussion of Adapter Debug Software (ADS) version A205 for use as a hardware debug aid is also provided.

Further information on the adapter bus memory expansion can be found in the TMS380 ASIC-LAN Toolkit, available from Texas Instruments. This toolkit provides information for users wishing to collect memory expansion logic into a single ASIC device. This option can be an important factor in cost and board area savings.

3.1 EPROM Memory Map

Figure 3-1 illustrates the LAN Adapter bus memory map for EPROM-based DLC code. The memory map locates the 16K × 8 EPROMs starting from LAN Adapter bus address >8000 and extending to >FFFE. A total of 16K bytes of buffer RAM is provided from address >4000 through >7FFE. This amount of buffer RAM is required for all applications. Optionally, additional RAM may be located from address >1000 through >3FFE. Note that addresses >0000 through >0FFE are reserved for adapter registers as well as the on-chip RAM of the TMS38010.

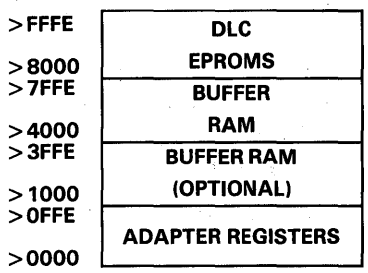


Figure 3-1. EPROM-Based Memory Map

3.2 EPROM Schematic

Figure 3-2 shows the adapter bus schematic using EPROM-based code compatible with the memory map discussed in the previous section. This schematic uses 16K × 8 EPROMs with an access time of 135 nanoseconds. To decrease this access time requirement, the user may add one wait state to EPROM accesses. The addition of one wait state will allow the use of EPROMs with 450-ns access time. Wait states for RAM are not allowed.

Note that the code within the EPROMs completely replaces the code contained within the TMS38020 Protocol Handler (PH) ROM. Thus, the PH is deselected (via the $\overline{\text{PHCS}}$ pin) in the address range >8000 through >FFFE. Note, however, that the PH must be selected in the address range >0100 through >012E so that access to the PH's on-chip registers is allowed. For simplicity, $\overline{\text{PHCS}}$ is connected to the latched address most-significant bit (A0) shown in Figure 3-2.

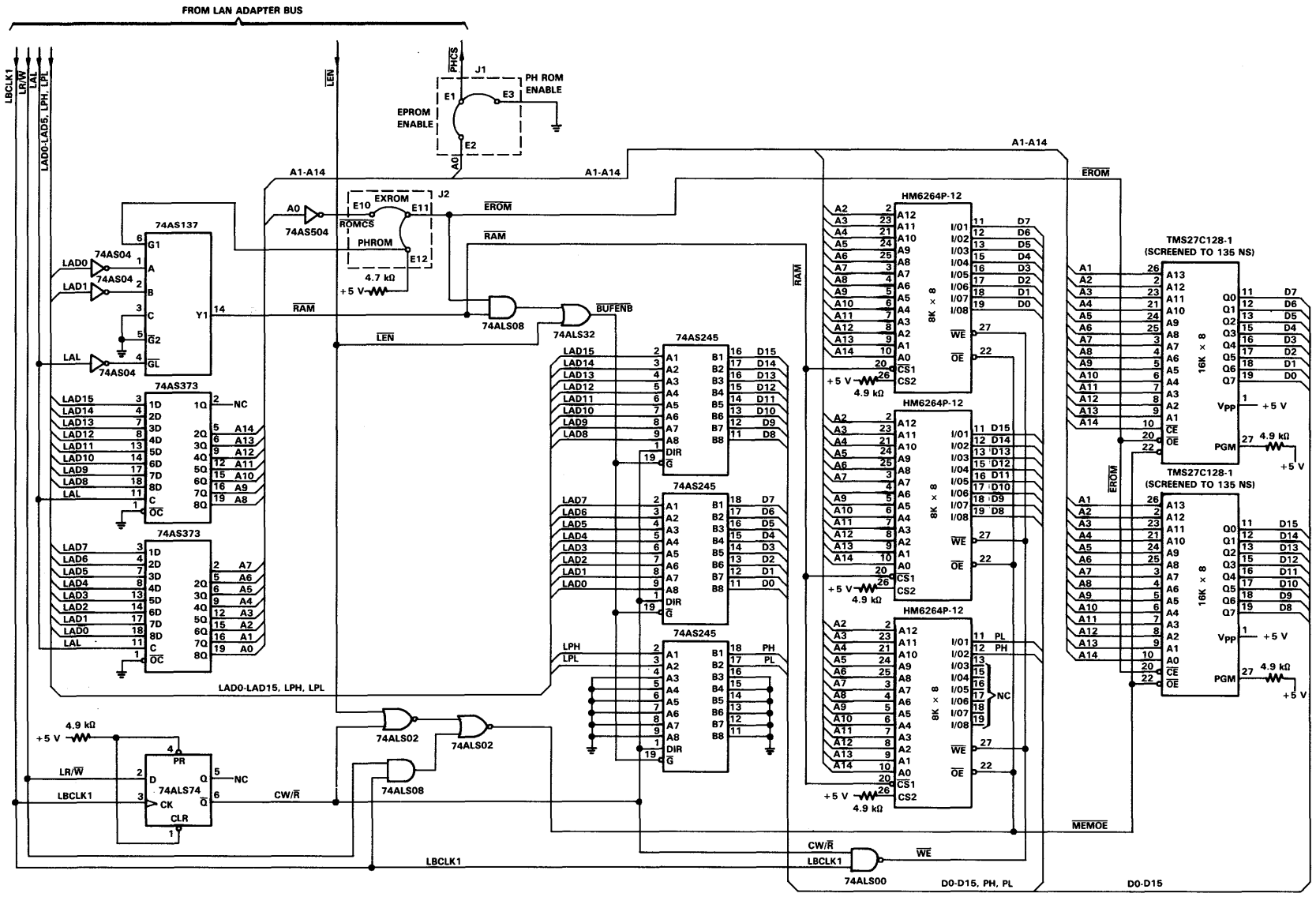


Figure 3-2. EPROM-Based Adapter Bus Schematic

The 16K bytes of static RAM provide buffer storage for frame data and LLC link station tables. The static RAM is enabled for LAN Adapter bus addresses from >4000 to >7FFE. The static RAM must include parity and must operate with zero wait states. To meet these requirements, the static RAMs must have an access time of 120 ns.

For systems requiring the use of byte parity for adapter program EPROM storage, odd parity per byte protection may be added by providing an additional EPROM containing the parity bits and tying the TMS38010 Communication Processor's TEST1 pin to ground. The EPROM containing the parity bits must be connected to the LPH (odd parity high-byte) and LPL (odd parity low-byte) lines of the LAN Adapter bus.

> **Note:**
>
> If a MAC-only adapter is desired by utilizing code contained within the PH ROM, the TEST1 pin should be left unconnected. Unreliable operation will result if the TEST1 pin is connected to ground when PH ROM is used.

3.3 Debug Methodology

The prototype and debug of an adapter card is aided by a software tool called Adapter Debug Software (ADS). ADS resides in two 16K × 8 EPROMs, like that of the DLC software, and is designed specifically for adapter card debug and verification. This section will discuss the installation of ADS EPROMs on the LAN Adapter bus. A detailed discussion of LAN Adapter Bus verification and the command set available for use with ADS is provided in Section 5.

3.3.1 ADS Installation

ADS is supplied in either an EPROM version or as a download version. The designator for the EPROM version is A205. The designator for the download version is B205. ADS version A205 is discussed here. The download version B205 will be discussed in Section 5.

A205 EPROMs map into the LAN Adapter bus memory space starting at bus address >8000. The actual executable code resides in the last half of the EPROM from >C000 through >FFFE. This allows A205 to be used in adapters designed for 8K × 8 EPROMs. Note, however, the most-significant address pin of the A205 EPROM must be kept high.

The revision level of ADS code (A205) is located at location >C000 of the LAN Adapter bus.

> **Note:**
>
> It is recommended that a back-up set of ADS EPROMs be made in case damage occurs to the original set during their use.

The ADS EPROMs should be installed and the appropriate jumpers set so that the EPROM is enabled into the memory map of the LAN Adapter bus and the PH ROM is disabled. Note that the ADS EPROMs replace the standard adapter software contained in the Protocol Handler (PH) ROM. Provisions should be made to deselect the PH ROM (via $\overline{\text{PHCS}}$) for the address range of the ADS EPROMS (>8000 - >FFFE) as shown in Figure 3-2.

Section 5 should be consulted for details on the execution of ADS.

4. DRAM-Based Adapters

As an alternative to EPROM-based DLC software, dynamic RAM (DRAM) may be provided on the LAN Adapter bus and the DLC software downloaded by the attached system into the DRAM. This section provides a memory map, a tested schematic, and download procedures for DRAM-based operation. The DRAM in this hardware solution is used for both program storage and data buffering. DRAMs may offer a cost and space savings over an EPROM/SRAM-based solution. For further cost and space reduction, users may refer to the TMS380 ASIC-LAN Toolkit available from Texas Instruments. This toolkit guides the user in designing a memory expansion and DRAM controller ASIC device for the TMS380 adapter chipset.

4.1 Memory Map

The memory maps shown in Figure 4-1, (a) and (b), are the memory maps required for download of Data Link Control Software. The maps provide for two partitions of 64K bytes of address for a total of 128K bytes of memory. The partition is accomplished by decoding the LI/$\overline{D}$ status pin output of the TMS38010. This pin is asserted high on memory cycles that are instruction fetches and asserted low on memory cycles that are operand data reads or writes. By including this status output as part of the memory address decoding, an instruction space (LI/$\overline{D}$ is High) and a data space (LI/$\overline{D}$ is Low) may be defined.

The presence of the TMS38020 Protocol Handler (PH) ROM in the memory map is controlled by the PHDIS signal. This signal is a latched signal provided by the attached system. After reset, this signal should be low and the PH ROM present. This is because the ROM software is needed to place the adapter in the download state. Once the DLC Software is loaded into the DRAM it executes exclusively out of the DRAM. The occurrence of a hardware reset ($\overline{SRESET}$ driven low) causes the TMS38010 Communications Processor to trap to code contained within the PH ROM. Thus, any time a hardware reset occurs, the DLC Software must be reloaded into DRAM memory.

An advantage of DRAM-based adapters is that in the event that a MAC-only adapter is desired, the PH ROM is still contained within the memory map, allowing MAC-only operation with the balance of the DRAM (>1000 - >BFFE) available as expansion buffer RAM.

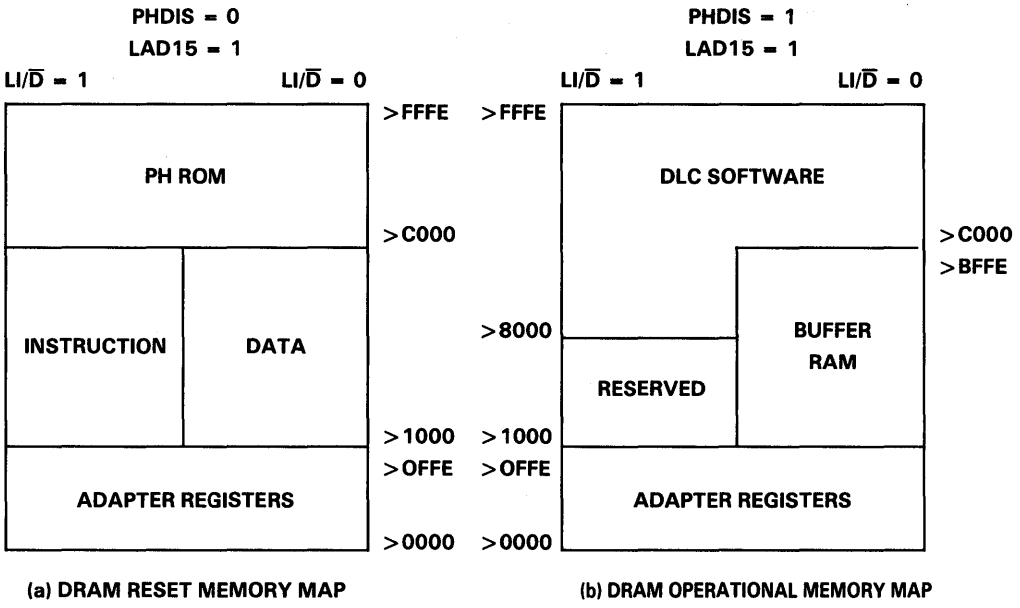
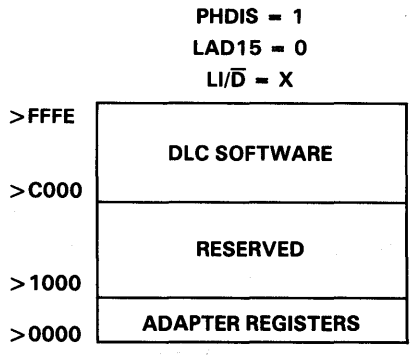


Figure 4-1. DRAM-Based Memory Maps

Since the PH and SIF do not decode LI/$\overline{D}$ when performing DMA as bus masters and always drive the signal low (indicating data), a provision for loading instructions into instruction space must be made. This is accomplished by allowing the state of LAD15 pin during the address phase of memory cycles to define a special "download" memory map. Because the LAN Adapter bus is a 16-bit bus, and only words are transferred on the bus, the LAD15 pin during the address phase is not used and is not normally captured in the address latch for address decode. However, the LAD15 pin on the TMS38010 is tied internally to a software-settable bit in the CPU's status register. Thus, under program control, the state of LAD15 during the address phase of memory cycles can be controlled.

This capability is used in the DRAM memory map to allow another memory map state to exist which disables the instruction/data partitioning and allows the instruction space DRAM memory to be accessed exclusively without regard to the state of the LI/$\overline{D}$ pin. Figure 4-2 shows the adapter memory map when the state of the LAD15 pin is low during the address phase of memory cycles. Note that for normal operation, the LAD15 pin is high during the address phase of memory cycles. After DLC software is downloaded, a startup routine within the downloaded code copies the data partition contents, written during the download procedure, to the instruction partition, using the LAD15 signal.



NOTE: This is instruction part of memory.

Figure 4-2. Download State of DRAM Memory Map

4.2 DRAM Schematic

Figure 4-3 is a block diagram of a DRAM interface to the LAN Adapter bus. Figure 4-4 is a verified schematic of a DRAM interface utilizing a PAL device to aid in chip count reduction. Optionally, all interface glue can be contained in a single ASIC device. For more information on ASIC solutions to the DRAM interface, please refer to the TMS380 ASIC-LAN Toolkit documentation.

The Protocol Handler must be enabled ($\overline{\text{PHCS}}$ low) for addresses between >0000 and >0FFE to allow access to PH registers. It must also be enabled between addresses >C000 and >FFFE, for access to the PH ROM used to download the code, when PHDIS = 0. The DRAM hardware option provides up to 44K bytes of expansion RAM for frame buffering and LLC link station tables. Note that parity is provided as this RAM space is used both for data and instruction storage.

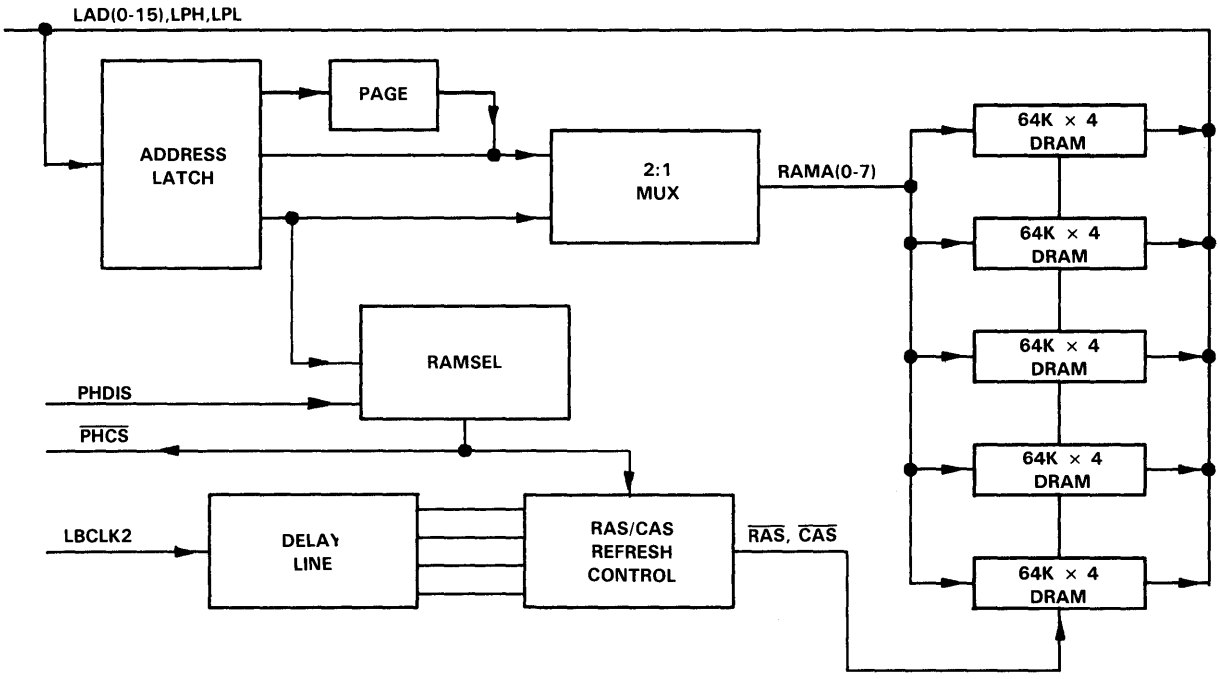
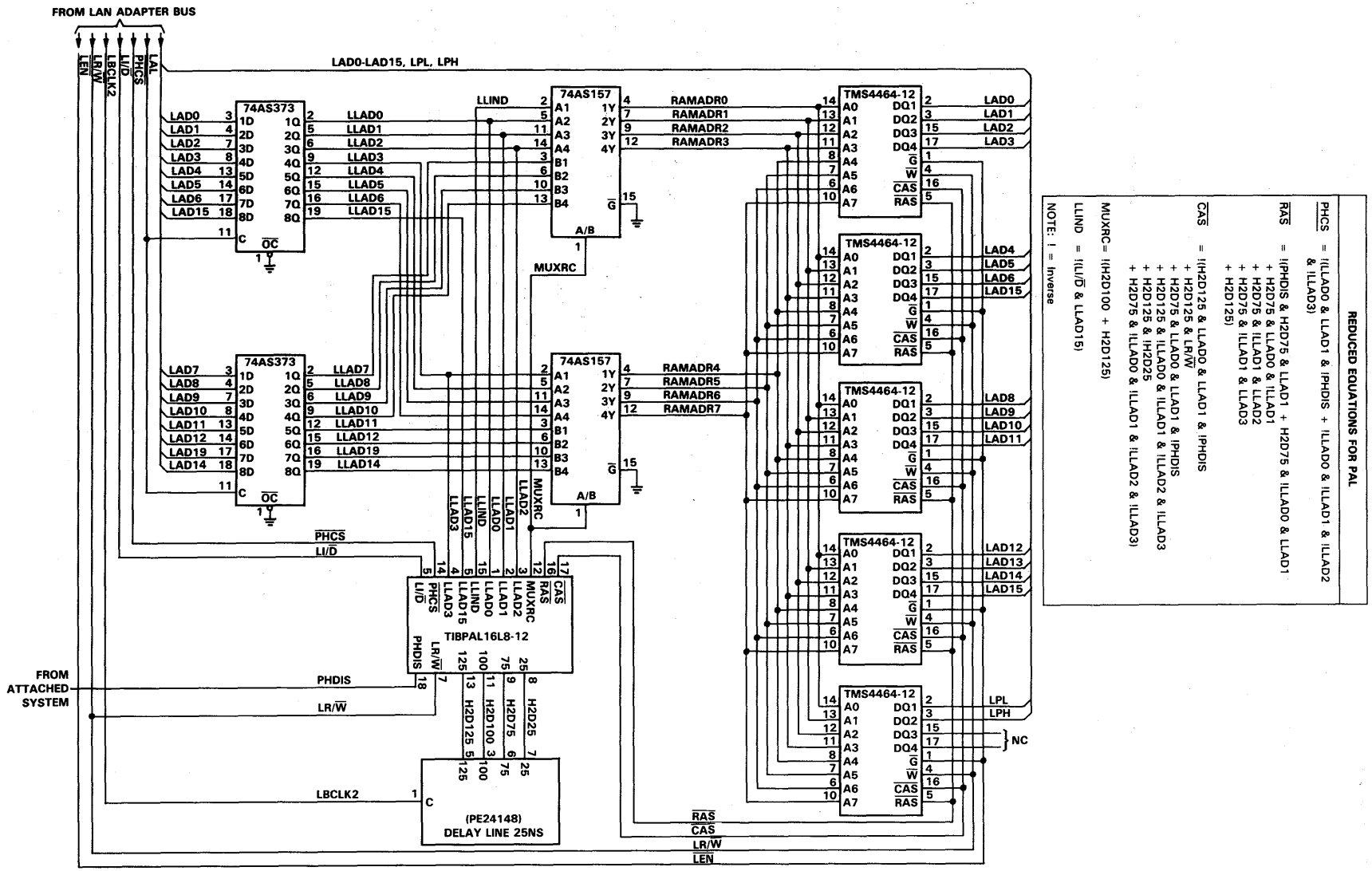


Figure 4-3. DRAM Interface Block Diagram



NOTE: PHDIS signal is controlled by host software to disable PHROM and enable DRAM from >C000 to >FFFE.

Figure 4-4. DRAM Schematic

4.3 Code Download

The download of DLC Software is performed by:

1. Placing the adapter into a download state.
2. Downloading the Enable Memory (ENM) software.
3. Setting PHDIS to one.
4. Downloading the DLC Software object code via direct I/O (DIO) operations.

The special download state of the adapter is entered via the following procedure:

1. Perform two hardware resets ($\overline{\text{SRESET}}$ driven low) no sooner than 12 μs but not more than 1.6 ms apart.
2. Write the value >8000 to the TMS38030 Interrupt Register.

Following the write of >8000 to the Interrupt Register and a delay of 10 milliseconds, the Interrupt Register should be read. If the Interrupt Register is not >0000, then the attempt to enter the download state failed and the procedure should be repeated. If the adapter continues to fail to enter the download state, a possible hardware error may exist.

After successfully entering the download state of the adapter, the object file may be loaded into the adapter RAM. Before this procedure is discussed, the following provides a description of the format of the object file in which DLC software and ENM software is provided.

4.3.1 Object File Format

The file containing the DLC software (OSI2.OBJ) and ENM software (ENM.OBJ) object code is provided in ASCII-encoded tagged object format. This object format is based upon the following four tags:

9 The "9" tag defines the next four hexadecimal characters as a starting address where subsequent object code is to be written. All subsequent object code is assumed to load sequentially until another "9" tag is encountered defining another start address.

B The "B" tag defines the next four hexadecimal characters as a word (16-bits) of object code.

F The "F" tag defines the end of line of object code. All other characters following the "F" tag on the line should be ignored.

: The ":" tag defines the end of file.

Figure 4-5 provides an example of tagged object code.

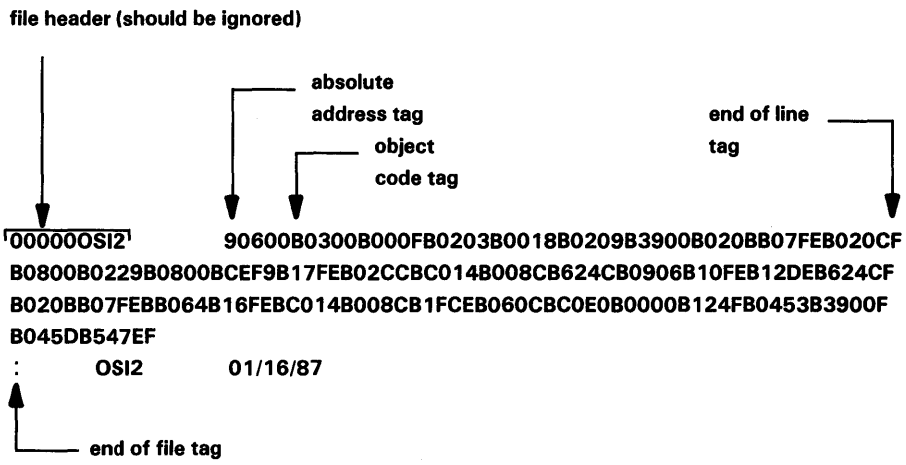


Figure 4-5. Tagged Object Code Format

4.3.2 Download State

When in the download state, the code in the PH will respond to several commands that are written to the most-significant byte of the SIF Interrupt Register.

>E6 — WRITE Command	The WRITE command enables the attached system to write to the Adapter's memory using DIO writes to the Data register and the Data Autoincrement register. The location written is pointed to by the contents of the Address Register.
>FF — STEP Command	The STEP command increments the Address register by >0800. When executed, >0800 is added to the contents of the Address register. Normally, the Address register limits the host system to a 2K-byte window into the LAN Adapter bus. The STEP command allows paging through consecutive 2K-byte windows. When the download state is initially entered, the Address register is initialized to >0000.
>C5 — EXECUTE Command	The EXECUTE command causes code to be executed at the location specified by an address contained at address >0000 on the LAN Adapter bus. Address location >0000 should be initialized to the starting address for code execution prior to writing the EXECUTE command to the Interrupt register.

4.3.3 Download and Execute

After the download state of the PH code is entered, the following procedure should be applied to download and execute code. Note that the Address register is set to zero following entry into the download state.

> **Note:**
> To perform hardware reset and control PHDIS, the attached system must have access to the $\overline{\text{SRESET}}$ and PHDIS signals through a control buffer.

1. The WRITE command (>E6) should be written to the Interrupt register to enable DIO write operations.
2. The value >0A00 should be written to the Data Register. This writes the address vector >0A00 into location >0000 in adapter memory. This is the entry point for ENM software.
3. The ENM software should be downloaded according to the routine described below.
4. After downloading the ENM software, the EXECUTE command should be issued, and the interrupt register should be polled. When the interrupt register becomes >0070, the attached system should turn on PHDIS.
5. The Address Register should be reset to zero, and the value >0600 should be written to the Data Register. This writes the address vector >0600 into location >0000 in the adapter memory. This is the standard entry point for all downloadable adapter code.
6. The DLC software should be downloaded according to the routine described in the next subsection.
7. The EXECUTE command (>C5) should be written to the Interrupt Register to start code execution.

   For DLC Code, normal completion of bring-up diagnostics should be confirmed following the EXECUTE command. Once the execute command is issued, the adapter is no longer in the download state. Information on bring-up diagnostics may be found in Section 2.

Routine for Downloading a Subroutine. The object file should be read and the tagged object code extracted and written to appropriate addresses in adapter memory. Referring to Figure 4-5, after the file header information (which should be ignored), the first tag will always be a "9" tag. The four hexadecimal digits following the "9" tag are the starting address in adapter memory where subsequent object code is to be stored. All subsequent four-digit hexadecimal object code will be preceded by a "B" tag. Loading is accomplished by:

1. Writing the start address into the Address Register. Note that if this address is outside of the current 2K-byte window allowed by bits 0-4 of the Address Register, the STEP command (>FF) must be issued to page to the proper window. The STEP command increments the Address Register by >0800. Thus, if the Address Register was equal to >0842 before the STEP command was issued, the Address Register will equal >1042 after the STEP command is issued.
2. Following the setting of the Address Register, sequential code may be loaded by writing object code to the Data Register Autoincrement until another "9" tag (absolute address) is encountered. Note that more than one "9" tag may exist in a single object file.

3. If a ":" tag is found, the end of file has been encountered.

A flow diagram of the download process is shown in Figure 4-7. An example program, written in the C programming language, is shown in Appendix C.

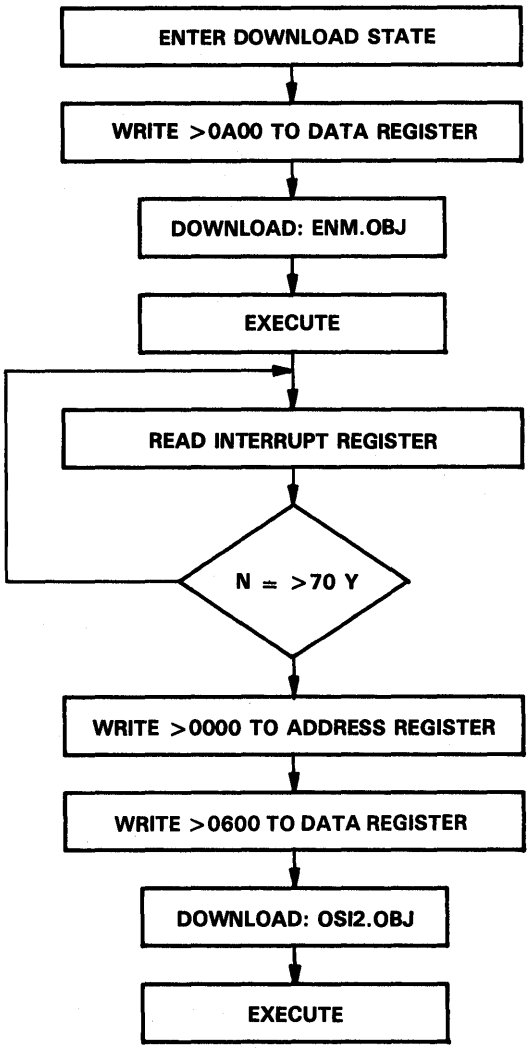


Figure 4-6. Flow Diagram for Downloading a Subroutine

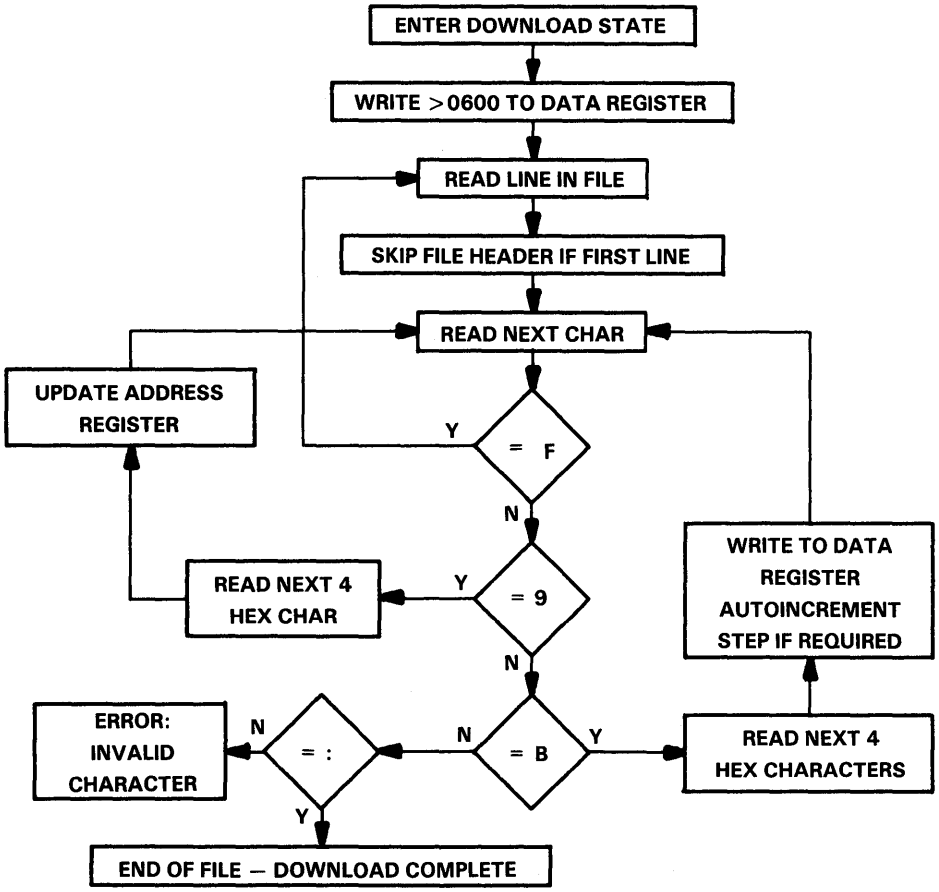


Figure 4-7. General Download Flow Diagram

4.4 Debug Methodology

A downloadable version of Adapter Debug Software (ADS) is available for DRAM-based adapters. This ADS version is designated by code version B205. The download of ADS assumes that the DRAM bus interface logic and interconnection is correct and the DRAM is functioning correctly. The following steps are recommended when debugging or prototyping a DRAM-based adapter:

1. By using the code contained on the Protocol Handler (PH), the adapter may be reset, initialized, and opened without utilizing any of the expansion DRAM and without the need for code download. Note that the adapter functions as a MAC-level adapter in this case. This allows the PH-based Bring-Up Diagnostics to be run, which verifies the interconnect of the basic five-chip set (TMS38010, TMS38020/021, TMS38030, TMS38051, and TMS38052).

2. Issuing the OPEN command with expansion memory extents from > 1006 through >BFFE assigns this memory area for use as buffer RAM. Specifying this as expansion memory during OPEN also tests the read/write capability of this RAM, as the adapter will test this memory during the OPEN processing. It is important to note that when this memory is tested, only the data partition is tested (LI/$\overline{D}$ is

low). The instruction partition of the full memory map shown in Figure 4-1 is not tested at this point. If the memory test fails, the OPEN command fails with an EXPANSION RAM ERROR posted to the System Status Block (SSB).

3. Following successful OPEN with the DRAM specified as expansion RAM, the Adapter Debug Software version B205 may be downloaded to adapter RAM using the procedure detailed in Section 4.3. Following download and execution, B205 will post the results of Phase 1 to the Interrupt Register. This code resides between the addresses of >4000 and >7FFE.

4. Upon completion of ADS download, normal completion of the first stage of ADS execution indicates that instruction partition access (LI/$\overline{D}$ is high) is working properly (see Section 5).

5. B205 contains a memory test command which allows the full extent of the DRAM to be tested in both the data and instruction partitions. A full description of this test command is provided in Section 5.

5. Adapter Debug Software

Adapter Debug Software (ADS) is a software tool that assists the engineer in verifying the design of a LAN adapter card or sub-system using the TMS380 adapter chipset. ADS is software which resides on the TMS380 LAN adapter bus and executed by the TMS38010 Communication Processor. ADS can be used for adapter card design verification and could be used to verify cards as part of a manufacturing test procedure.

ADS provides a two-stage process to bring up a LAN adapter card:

Stage 1: LAN ADAPTER BUS VERIFICATION. LAN Adapter bus verification insures that the TMS380 LAN Adapter bus (connecting the TMS38010 Communications Processor, TMS38020/TMS38021 Protocol Handler, TMS38030 System Interface, and the ADS memory) has been properly interconnected and is functioning correctly.

Stage 2: ADS COMMAND SET. ADS command set presents a set of commands to the attaching system that can be used to verify additional domains of the adapter card. This command set is controlled by the attached system and includes:

- Adapter-to-Host test (DMA write)
- Host-to-Adapter test (DMA read)
- Ring Interface tests (frame transmit/receive tests)
- Adapter expansion memory test
- Watch dog timer test
- Adapter-to-Host interrupt test

ADS is supplied in either EPROM (A205) version or as a download version (B205). A description of A205 EPROM installation is provided in Section 3. A description of B205 downloading procedures is provided in Section 4. Note that since B205 resides from >4000 through >7FFE on the LAN adapter bus, B205 can be downloaded to non-DRAM based adapters as long as 16K bytes of RAM exists within this address range. Throughout this section references to A205 refers to the EPROM version of ADS and references to B205 refers to the download version of ADS.

5.1 Stage 1: LAN Adapter Bus Verification

Upon power-up or application of a hardware reset ($\overline{\text{SRESET}}$ active-low) for A205 or upon execution of the EXECUTE command for B205, ADS automatically executes a LAN Adapter bus verification routine. During execution, the bus verification routine progresses through five phases: Reset verification, ADS code checksum verification, TMS38010 RAM verification, TMS38020 register verification, and TMS38030 register verification.

5.1.1 Phase Completion Reporting

Upon completion of each phase, ADS reports status in two ways. First, ADS will change the signal levels of three pins on the TMS38020 or TMS38021 Protocol Handlers. These pins are FRAQ (pin 48), $\overline{\text{NSRT}}$ (pin 44), and $\overline{\text{WRAP}}$ (pin 46). The interpretation of these signals is described below. ADS will simultaneously post status information in the Interrupt Register of the TMS38030 System Interface. If the attached system bus interface logic is functional, the status information may be read by a direct I/O read of the Interrupt register.

5.1.2 The Five Verification Phases

The bus verification routine of ADS sequences through five verification phases automatically. Upon successful completion of each phase, new status is posted to the TMS38020 pins FRAQ, $\overline{\text{NSRT}}$, and $\overline{\text{WRAP}}$, as well as to the TMS38030 Interrupt Register. A failure of a phase causes ADS to hang at that phase. Application of $\overline{\text{SRESET}}$ or a power cycle will cause A205 to re-execute starting from the first phase. Application of $\overline{\text{SRESET}}$ when ADS B205 is resident requires that the B205 be re-downloaded from the host system.

The five phases execute in the order shown in Table 5-1. If a failure occurs at any phase, ADS hangs at that phase leaving the most current status posted. If no errors are detected, the five phases cause the status to quickly sequence through that shown in Table 5-1, ending with >0005 in the Interrupt Register and the $\overline{\text{NSRT}}$ and $\overline{\text{WRAP}}$ pins changing state approximately once every four seconds.

Table 5-1. Verification Phase Status Posting

PHASE	STATUS POSTED				MEANING
	PH PINS			TMS38030 INTERRUPT REGISTER	
	FRAQ	$\overline{\text{NSRT}}$	$\overline{\text{WRAP}}$		
1	1	1	0	>0000	Reset verification failure. See Section 5.1.3
2	1	1	1	>0001	Code checksum verification failure. See Section 5.1.4
3	1	0	0	>0002	TMS38010 RAM verification failure. See Section 5.1.5
4	1	0	1	>0003	TMS38020 Protocol Handler register verification failure. See Section 5.1.6
5	0	1	0	>0004 or >0055 or >002A	TMS38030 System Interface register verification failure. See Section 5.1.7
Command State	Note	Note	Note	>0005	Normal completion of bus verification stage. No errors detected. ADS is in the command state. See Section 5.2.

NOTE: At this point, FRAQ is indeterminate and $\overline{\text{NSRT}}$ and $\overline{\text{WRAP}}$ change state approximately once every four seconds.

If the status posted indicates a failure, consult the section referenced in Table 5-1 for further information regarding the failure and possible cause. If the status read from the three pins is not listed in the above table, the following should be checked:

1. All V_{CC} and V_{SS} connections to the Protocol Handler (PH) should be verified. If the PH is not correctly connected to power and ground, a correct indication through the three pins cannot be obtained.
2. The $\overline{\text{PHTEST}}$ pin of the Protocol Handler should be verified unconnected. If this pin is inadvertently connected to ground (active-low), the output pins of the PH are put in a high-impedance state providing an indeterminate indication.
3. If no apparent changes are taking place on the three PH pins, it may be the result of no transitions occurring on pin RCLK of the PH. The RCLK input pin **must** have transitions occurring in order for the RINGCMD0 and RINGCMD1 registers of the PH to be written. If no transitions occur, these registers cannot be written, thus no indication is provided on the three pins.

If the direct I/O (DIO) interface is functioning correctly, the Interrupt register should be read to confirm the status as indicated by the state of the three PH pins.

Once normal completion is indicated, ADS enters a command state and the ADS may be passed commands by the attached system by writing to the TMS38030's Interrupt Register (see Section 5.2).

If the adapter is connected to a wiring concentrator when ADS is executed, the four-second state changes of $\overline{\text{NSRT}}$ and $\overline{\text{WRAP}}$ (normal completion of the bus verification stage) will cause repeated indication of insertion and deinsertion to occur.

5.1.3 Phase 1

The first phase provides a cursory test that the TMS38010 Communications Processor and on-chip oscillator are functional and basic access to the A205 EPROM or B205 RAM is successful.

If this phase fails, the following checks should be done:

1. If a problem exists such that the TMS38010 Communications Processor cannot write to Protocol Handler registers, a failure in phase 1 may be indicated when actually the failure is detected in phase 2, phase 3, or phase 4. The Interrupt register should be read, if possible, to confirm the phase 1 failure. Be sure that pin RCLK on the PH has transitions occurring. The ring interface circuit should be populated prior to executing ADS. This assures that pin RCLK is receiving transitions from the ring interface circuit.
2. All wiring should be verified point-to-point on the LAN adapter bus to assure proper interconnect. Make sure that all jumpers are in the proper position and that the EPROMs (if used) are installed in proper order.
3. All interconnect to the EPROM or DRAM/SRAM and interface logic should be verified correct. A failure in this phase indicates a likely wiring error to the expansion memory. If downloadable B205 is being used, attempt to initialize and open the adapter using the PH ROM code. When opening in this manner, specify the RAM space normally occupied by B205 (>4000 - >7FFE) as expansion memory. An open error indicating an expansion RAM error confirms problems with the RAM and/or address decode and interface.
4. Make sure the ADS EPROMs (if used) are still good by comparing the contents to the backup set of A205 EPROMs.
5. The timing of LBCLK1 and LBCLK2 should be measured and compared to the timing requirements specified in the TMS38020/TMS38021 and TMS38030 data sheets. It must be noted that the difference in capacitive loading on LBCLK1 and LBCLK2 should not exceed 10 picofarads. If this requirement is not met, capacitance must be added to the deficient signal to bring the loading difference to within 10 picofarads.
6. LBRDY should be examined to assure that it is at a valid high level. LBRDY must be externally pulled high by a minimum 2.3 kΩ resistor.
7. Connect a logic analyzer to the LAN adapter bus and verify that the bus cycles immediately following removal of $\overline{\text{LRESET}}$ (removal of $\overline{\text{SRESET}}$) are similar to those shown in Figure 5-1 when executing PH ROM code. Note that due to logic analyzer sampling errors, the pattern you see on a logic analyzer may not correspond directly with that shown in Figure 5-1. However, the general pattern of transitions should be observed. If a signal line that normally toggles does not show activity, a short or open condition may be the cause.

Figure 5-1 was generated with a Tektronix Model 9100 logic analyzer set with the following parameters:

Trigger Event: Low to High transition of signal $\overline{\text{LRESET}}$

Sample Clock: 40 nanoseconds

Magnification: 5X

8. All adapter component V_{CC} and ground connections should be verified correct. All V_{CC} and ground pins must be physically connected for proper operation.

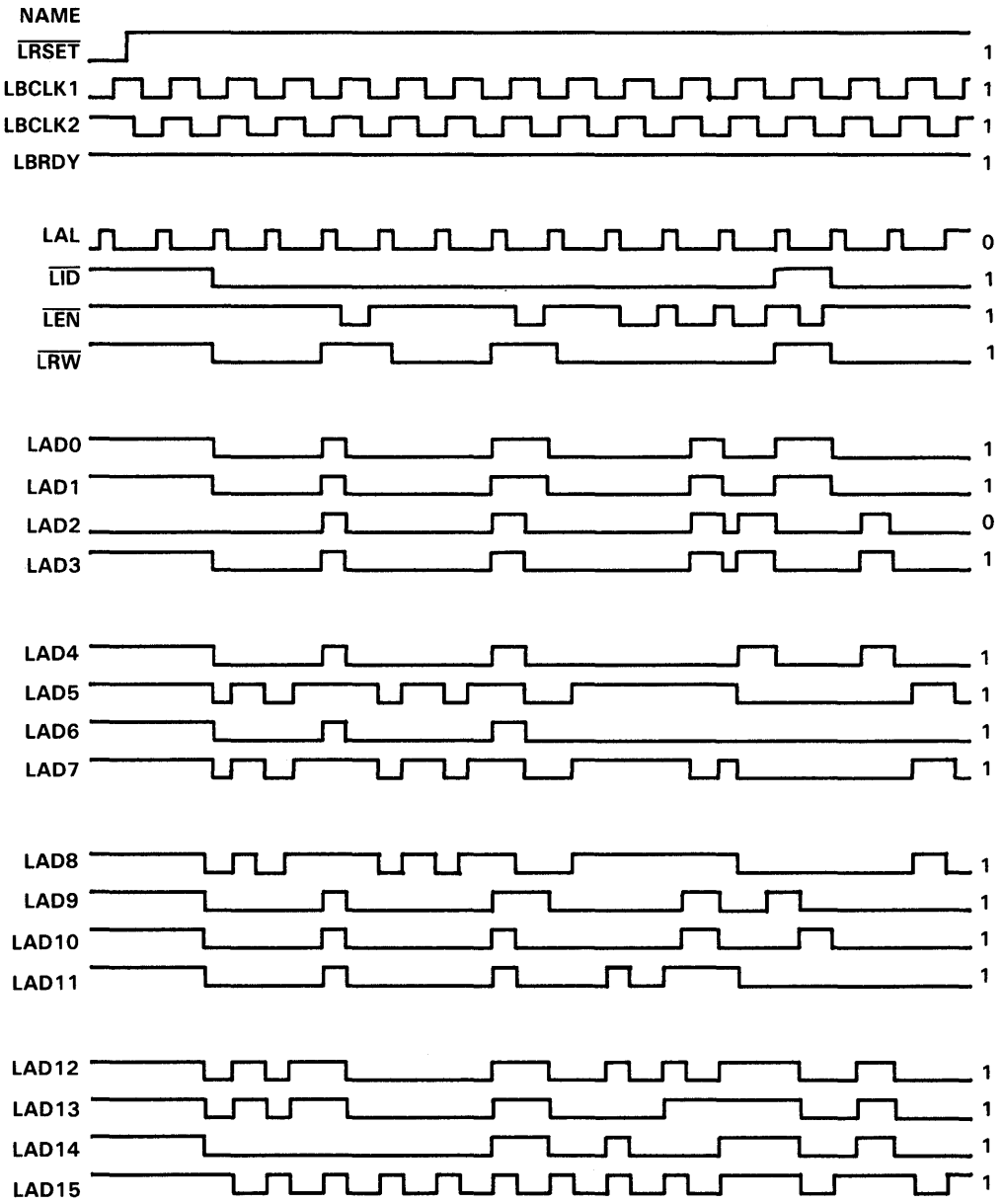


Figure 5-1. Bus Cycles Following $\overline{\text{LRESET}}$ When Executing Out of PH ROM

5.1.4 Phase 2

Phase 2 verifies that A205 EPROM or B205 RAM and the LAN adapter bus interface to the ADS memory is fully functional. This is done by calculating a checksum between the addresses of >C000 and >FFFE for A205 or between the addresses of >4000 and >7FFE for B205. Note that A205 code actually resides from >C000 through >FFFE (the last half of the 16K × 8 EPROMs), and the checksum is calculated only for that region. This allows the A205 EPROMs to be installed in adapter designs only incorporating sockets for 8K × 8 EPROMs. The most-significant address input must be maintained high if A205 is used in sockets intended for 8K × 8 EPROMs only. A full checksum of the entire EPROM contents is provided in a Stage 2 ADS command. The first half of the EPROMs in the address range >8000 through >BFFF is filled with the pattern >AAAA.

The ADS code release number is stored at the first location of ADS code (>C000 for A205 and >4000 for B205), and a checksum value is stored at the second location. This phase calculates a 16-bit checksum from the third word of the ADS code space to the last word. The calculated checksum is compared to the stored checksum, and failure at this phase will occur if the two do not agree.

If a failure is indicated, the following checks should be made:

1. All interconnect to the EPROM or RAM and interface logic should be verified correct.
2. Make sure the data in the A205 EPROMs are still valid by comparing the contents to the backup set of ADS EPROMs.

5.1.5 Phase 3

Phase 3 verifies that the RAM contained in the TMS38010 Communications Processor is functional.

TMS38010 RAM is verified by writing two patterns, >AAAA and >5555, to each RAM location, and reading and comparing the value read. RAM is verified starting at RAM location >0580 and extending to location >0DFE.

> **Note:**
>
> TMS38010 RAM locations >0E00 through >0FFE are used as a workspace for ADS software and are not checked during this phase.

When the TMS38010 accesses internal RAM, the state of the LAN adapter bus is a "don't care" condition. Thus, a failure of this phase indicates a faulty TMS38010 RAM location and the TMS38010 should be replaced.

5.1.6 Phase 4

Phase 4 verifies that the TMS38010 Communications Processor can read and write selected registers of the TMS38020 or TMS38021 Protocol Handler. Successful execution of this phase provides a positive indication that most of the LAN adapter bus connections to the Protocol Handler are correct.

> **Note:**
>
> Successful completion of this phase does not guarantee that the TMS38010 Communications Processor has full access to the on-chip ROM of the Protocol Handler. This will be verified by executing the Bring-Up Diagnostics of the standard adapter software. This will be discussed in Section 5.1.9.

The patterns >AAAA and >5555 are alternately written and then read to selected Protocol Handler registers. If the read value does not agree with what was expected, this phase fails.

Failure of this phase indicates either an error in the interconnect between the TMS38010 and the PH or a failure of the PH device (internal register failure).

> **Note:**
>
> ADS will fail this phase if transitions on the RCLK (pin 2) input do not occur. This is because the RINGCMD0 and RINGCMD1 registers of the Protocol Handler require RCLK input before they can be written by the Communications Processor.
>
> It is important that the ring interface circuit be populated on the prototype board before attempting to execute ADS. This assures that transitions occur on RCLK. An alternative is to temporarily tie MXTALOUT of the Communications Processor to the RCLK input to provide the necessary transitions.

In the event of failure of this phase, the following checks should be made:

1. Verify that the PH chip select ($\overline{\text{PHCS}}$) is active-low when the PH registers are accessed (addresses >0100 through >012E).
2. Verify all connections to the PH are correct.
3. Verify that LBRDY is high during access to the internal registers. The LBRDY state is sampled during register accesses and the access will fail if LBRDY is not maintained at a high level throughout the bus cycle.

5.1.7 Phase 5

Phase 5 verifies that the TMS38010 Communications Processor can read and write selected registers of the TMS38030 System Interface. Successful execution of this phase provides a positive indication that the LAN adapter bus connections to the TMS38030 System Interface are correct.

Again the TMS38010 writes the two patterns >AAAA and >5555 to TMS38030 registers and the registers are read back and the result compared to the value expected.

Failure of this phase indicates either a connection error between the TMS38010 and the TMS38030 or a faulty TMS38030. All connections must have been made properly to the TMS38030 LAN adapter bus interface pins for this phase to pass. If the TMS38030 is socketed, it is important to assure that that device is properly seated in the socket. Verify all connections to the TMS38030 or replace the TMS38030 if suspected faulty.

5.1.8 Direct I/O Interface to Attached System

During this stage of adapter bring up, the direct I/O interface between the attached system and the TMS38030 should be verified. The first step in this verification is to check that the value >0005 can be read from the Interrupt Register of the TMS38030 when all five phases of ADS have completed normally. If this register cannot be read, a possible error in the interface between the TMS38030 System Interface and your attached system (host) bus exists. Any errors in this interface must be corrected before you can issue ADS commands (Stage 2).

The direct I/O interface may be exercised by writing bit patterns in the range >00 through >7F to the most significant byte of the Interrupt register and reading and comparing the expected result. Do not write values greater than >80 as inadvertent activation of ADS commands may result. To exercise the Data registers and the Address register, DIO accesses to internal adapter RAM may be attempted in the address range >0580 through >0DFE.

5.1.9 Bring-Up Diagnostics

An integral part of the standard adapter software contained in the TMS38020's on-chip ROM is an extensive diagnostic termed Bring-Up Diagnostic (BUD). This BUD is executed upon power-up or whenever the adapter is reset, and performs several tests including:

1. A checksum test of the adapter software.
2. An instruction and interrupt test of the TMS38010.
3. A transmit wrap test through the ring interface.
4. A register access test of the TMS38030.

Following completion of the five phases of ADS, the BUD diagnostics should be executed to verify that the on-chip ROM of the PH can be fully accessed by the TMS38010 Communications Processor.

When using A205 ADS, the BUD diagnostic may be run by disabling the EPROM and enabling the PH ROM via jumpers. When using B205 ADS, the PH ROM is already enabled into the memory map. The BUD diagnostic is started by applying reset ($\overline{\text{SRESET}}$ low) or power cycle to execute the BUD diagnostic.

Following reset of the adapter, the attached system should delay approximately three seconds and then read the Interrupt Register of the TMS38030. If the INITIALIZE bit (bit 9) is set to one, the TEST bit (bit 10) is zero, and the ERROR bit (bit 11) is zero, then the bits 12 through 15 should also be zero. This indicates that the BUD diagnostic completed successfully. If this occurs, you may continue with normal operation of the adapter (initialize, open, etc.).

If the TEST and ERROR bits are set to one the BUD diagnostic detected an error. The error code may be read from bits 12 through 15. Table 5-2 lists the definition of these error codes.

Table 5-2. Bring-Up Diagnostic Error Codes

ERROR CODE				ERROR CONDITION
0	0	0	0	Initial Test Error
0	0	0	1	Adapter ROM Error
0	0	1	0	Adapter RAM Error
0	0	1	1	Instruction Test Error
0	1	0	0	Context/Interrupt Test Error
0	1	0	1	Protocol Handler Hardware Error
0	1	1	0	System Interface Register Error

If there is an error in the LAN adapter bus connections to the PH such that access to the full contents of the ROM is not successful, the BUD diagnostic will fail with either error code 0000 or error code 0001 as shown in Table 5-2. This error can occur following successful execution of ADS bus verification, since ADS was executed out of EPROM or RAM and not the PH ROM space. If this error does occur, it indicates that the TMS38010 could not access the internal ROM of the PH. Access to this ROM will fail if a connection error between the TMS38010 and PH exists or the ROM of the PH is faulty.

The BUD diagnostic attempts to transmit frames through the wrap path of the ring interface circuit (not the lobe media). Thus it is possible to get an error code of 0101 as the ring interface has not yet been verified. If error code 0010, 0011, 0100, or 0110 is received, ADS should be executed again and the problem resolved before continuing with Stage 2 of ADS.

Note:

The PH does not internally decode address A1 on the LAN adapter bus for accesses to the internal ROM. Thus, memory address >8000 is mapped identical to address location >C000 (the beginning of the on-chip ROM). Thus, if external memory devices (EPROM or RAM) on the LAN adapter bus occupy locations >8000 through >BFFF, the chip select for the PH ($\overline{\text{PHCS}}$) must be assured to be inactive-high when external memory devices are accessed. Failure to do so may cause a bus conflict to occur.

For more information on the adapter BUD diagnostic, consult the *TMS380 Adapter Chipset User's Guide*.

5.2 Stage 2: ADS Command Set

When stage 1, LAN adapter Bus Verification, has been completed without detecting a failure, ADS goes to a command state. This command state allows the attaching system to send commands to the adapter chipset by writing to the Interrupt register of the TMS38030. This set of commands can be used for verifying new designs as well as providing a foundation for manufacturing test programs. A list of these commands and their functions is shown in Table 5-3.

Table 5-3. ADS Commands

COMMAND BYTE	DESCRIPTION
>81	Clear RAM
>82	Fill RAM with Pattern
>83	Set Interrupt Active
>84	Test DMA to Adapter (DMA Read)
>85	Test DMA from Adapter (DMA Write)
>90	Test Expansion Memory
>91	Test Wrap Function
>92	Test Lobe Function
>93	Test Insert Function
>94	Extended Checksum Test
>95	Test Watchdog Timer
>96	Set PH in Repeat Mode Without Insert
>97	Set PH in Repeat Mode with Insert
>98	Terminate Command
>9A	Test Insert Function with Insertion Delay

These commands may be executed to:

- Verify interface logic between the TMS38030 System Interface and the attaching system bus during DMA operations.
- Test miscellaneous hardware features of the adapter (i.e., the watchdog timer function or DRAM).
- Perform more exhaustive tests of the ring interface circuit.

Warning:

When executing these commands, the watchdog timer must be disabled for all commands except the TEST WATCHDOG TIMER command (>95). If the burned-in address PROM is not present, this function must also be disabled.

5.2.1 ADS Commands

The commands shown in Table 5-3 are initiated by the attached system direct I/O writing the command byte to the most-significant byte of the TMS38030's Interrupt register. Writing a command byte causes the command to be executed immediately by ADS.

Note:

This stage of ADS assumes a functional direct I/O interface between the attached system and the TMS38030 of the adapter. The direct I/O interface should be verified for correct operation so that the four 16-bit registers of the TMS38030 can be properly read and written by the attached system.

Several commands use parameters which may be modified from default values provided by ADS. Modifying parameters involves modifying the contents of memory locations in Communications Processor RAM. Memory locations in CP RAM may be modified using the TMS38030's Address and Data registers. The desired RAM address must be first

written to the Address register. A subsequent read or write of the Data register will result in that RAM location being either read or written by the attached system.

Many commands share identical parameters and the corresponding adapter RAM address locations for these parameters. Thus, changing a default parameter value for one command will affect that parameter value for another command.

The following sections describe each command and its use.

5.2.1.1 Invalid Commands

If a byte written to the most significant byte of the Interrupt register does not correspond to one of the command bytes defined in Table 5-3, ADS responds with >0F written to the least significant byte of the Interrupt register.

5.2.2 Command >81 - Clear RAM

Command >81 is used to clear the specified adapter RAM locations to zero. This command has the following parameters which may be modified by rewriting the defaults via direct I/O.

Table 5-4. Command >81 Parameters

PARAMETER	DEFAULT VALUE	RAM LOCATION
Adapter RAM Starting Address	>0600	>0598
Number of Bytes to Clear	>0024	>0590

Both parameters must be even. If an odd value is provided, ADS will ignore the least significant bit. The starting address can be any location in the address map. For DRAM-based adapters with an instruction and data partition, this command causes the RAM in the data partition to be cleared. The instruction partition is not affected.

Warning:

In B205 applications, specifying the start address to be in the range of executable code >4000 - >7FFE will corrupt ADS code, causing unpredictable operation.

5.2.2.1 Command >81 Completion Status

Upon completion of the command, ADS posts pass/fail status in the least significant byte of the Interrupt register. For this command, the following status is posted:

PASS = >00
FAIL = >7X

The X bits in the fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

Table 5-5. >7 X ERROR CODES

ERROR CODE	MEANING	PROBABLE CAUSE
>71	HOST BUS DMA PARITY ERROR The TMS38030 detected a parity error during a DMA read cycle on the attached system bus.	Since parity on the host bus is not checked, this error should never occur. If this error occurs, an error may exist in the LAN adapter bus connections to the TMS38030.
>72	HOST BUS DIO PARITY ERROR The TMS38030 detected a parity error when the attached system wrote to a DIO register.	Since parity on the host bus is not checked, this error should never occur. If this error occurs, an error may exist in the LAN adapter bus connections to the TMS38030.
>73	DMA BUS ERROR The SBERR pin of the TMS38030 was asserted by the attached system bus during a DMA memory cycle.	Commands which do not exercise the DMA interface of the TMS38030 will not get this error. An error exists in the DMA interface between the TMS38030 and the attached system bus.
>74	LAN ADAPTER BUS PARITY ERROR, EXTERNAL BUS MASTER. The TMS38010 has written to a TMS38030 register and the TMS38030 detected a parity error in the data written.	Faulty interconnect between the TMS38010 and TMS38030.
>75	LAN ADAPTER BUS PARITY ERROR, TMS38030 WAS BUS MASTER. A parity error was detected when the TMS38030 was performing a DMA transfer on the LAN adapter bus.	This may occur if an invalid RAM address was written to the TMS38030 Address Register and a subsequent read or write to the Data Register or Data Register with autoincrement was performed. In this case, the TMS38030 attempted to access a LAN adapter bus location which was not populated by RAM.
>76	LAN ADAPTER BUS PARITY ERROR, TMS38010 WAS BUS MASTER. A parity error was detected when the TMS38010 was performing a bus cycle on the LAN adapter bus.	This error can occur if the TMS38010 is reading TMS38030 registers or adapter RAM. This error indicates: 1) A fault in the expansion RAM or interface to the RAM. 2) The TMS38010 was provided an address pointer which did not point to a valid RAM location. 3) A fault in the connections to the TMS38030.
>78	ILLEGAL INSTRUCTION DETECT. The TMS38010 detected an illegal instruction during the execution of ADS software.	Bad locations within the ADS EPROM or RAM. The address decode and interface to the EPROM or RAM should be verified.
>79	ARITHMETIC FAULT INTERRUPT. The TMS38010 encountered an arithmetic fault (divide by zero) during the execution of ADS software.	Bad locations within the ADS EPROM or RAM. The address decode and interface to the EPROM or RAM should be verified.

5.2.3 Command >82 - Fill RAM with Pattern

Command >82 is used to fill adapter RAM locations with a 16-bit data pattern. This command has the following parameters which may be modified by rewriting the defaults via direct I/O.

Table 5-6. Command >82 Parameters

PARAMETER	DEFAULT VALUE	RAM LOCATION
Adapter RAM Starting Address	>0600	>0598
Number of Bytes to Fill	>0024	>0590
16-Bit Data Pattern	>5555	>05A4

The first two parameters must be even. If an odd value is provided, ADS will ignore the least significant bit. The even restriction does not apply to the data pattern parameter.

For DRAM-based adapters employing an instruction and data partition, this command writes the data pattern to the data partition only. The instruction partition is not affected.

Warning:

In B205 applications, specifying the start address to be in the range of executable code >4000 - >7FFE will corrupt ADS code, causing unpredictable operation.

5.2.3.1 Command >82 Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >00
FAIL = >7X

The X bits in the fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

5.2.4 Command >83 - Set Interrupt Active

Command >83 is used to set the state of the TMS38030's interrupt pin active. When the TMS38030 is configured in 808X mode, the SINTR pin is taken active-high. When configured in 680XX mode, the $\overline{\text{SIRQ}}$ pin is taken active-low. This feature is useful for verifying that the attached system responds properly to adapter generated interrupts.

The interrupt is cleared by writing a zero to bit 8 of the Interrupt register.

5.2.4.1 Command >83 Completion Status

Upon completion of command execution, ADS will post the following status in the least significant byte of the Interrupt register.

PASS = >AA
FAIL = not >AA

If the pattern >AA is not read by the attached system, verify proper direct I/O reads are achieved. A possible result of this command failure is improper interconnect between the TMS38010 and TMS38030.

If the expected interrupt is not received by the attached system, examine the state of the SINTR/$\overline{\text{SIRQ}}$ pin of the TMS38030. If this pin is active yet no attached system interrupts were recognized, the problem lies in the interface logic between the attached system and the TMS38030.

5.2.5 Command >84 - Test DMA to Adapter

Command >84 is used for starting a DMA transfer from the attached system to the adapter (DMA read). Thus, the attached system bus interface logic may be verified for proper operation under TMS38030 DMA operations. The parameters which may be changed via direct I/O from the attached system are shown in Table 5-7.

The Address register of the TMS38030 restricts direct I/O (DIO) access to adapter RAM to a 2K-byte window. The most significant five bits of the Address register are fixed at zero while executing ADS. Thus, only the address range >0000 through >07FE is accessible via direct I/O. It is recommended that memory blocks used for DMA tests remain within this window because this adapter RAM is available for examination and modification.

Table 5-7. Command >84 Parameters

PARAMETER	DEFAULT VALUE	RAM LOCATION
DMA Length (Bytes)	>0024	>0590
DMA Repeat Count	>0080	>0592
DMA System Extended Address	>0003	>0594
DMA System High/Low Address	>0000	>0596
DMA Adapter RAM Address	>0600	>0598

The parameter DMA LENGTH and DMA ADAPTER START ADDRESS are DMA parameters for the adapter RAM space. Parameters DMA SYSTEM EXTENDED ADDRESS and DMA SYSTEM HIGH/LOW ADDRESS are used for specifying the location within attached system memory where DMA data is to be read. This system address is a 24-bit address. DMA SYSTEM EXTENDED ADDRESS contains the extended address byte right justified in the field. DMA SYSTEM HIGH/LOW ADDRESS contains the least-significant 16- bits of system address.

Warning:

In B205 applications, specifying the start address to be in the range of executable code >4000 - >7FFE will corrupt ADS code, causing unpredictable operation.

The parameter DMA REPEAT COUNT sets the number of times the DMA transfer will be repeated before the command is terminated.

5.2.5.1 Command >84 Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >7X

The X bits in the fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

To verify that the data in attached system memory was successfully transferred to adapter memory, the direct I/O interface may be used to examine the RAM locations on the LAN adapter bus corresponding to the locations used for the DMA transfer. If the data found in adapter memory is not the same as the data in attached system memory, the interface logic between the attached system and the TMS38030 should be carefully checked.

5.2.6 Command >85 - Test DMA From Adapter

Command >85 is used for starting a DMA transfer from the adapter to attached system memory (DMA write). Thus, the attached system interface logic may be tested under TMS38030 DMA operations. The parameters which may be changed via the direct I/O interface are shown in Table 5-8.

The Address register of the TMS38030 restricts direct I/O (DIO) access to adapter RAM to a 2K-byte window. The most significant five bits of the Address register are fixed at zero while executing ADS. Thus, only the address range >0000 through >07FE is accessible via direct I/O. It is recommended that memory blocks used for DMA tests remain within this window because this adapter RAM is available for examination and modification.

Table 5-8. Command >85 Parameters

PARAMETER	DEFAULT VALUE	RAM LOCATION
DMA Length (Bytes)	>0024	>0590
DMA Repeat Count	>0080	>0592
DMA System Extended Address	>0003	>0594
DMA System High/Low Address	>0000	>0596
DMA Adapter RAM Address	>0600	>0598

The parameter DMA LENGTH and DMA ADAPTER START ADDRESS are DMA parameters for the adapter RAM space. Parameters DMA SYSTEM EXTENDED ADDRESS and DMA SYSTEM HIGH/LOW ADDRESS are used for specifying the location within attached system memory where DMA data is to be written. This system address is a 24-bit address. DMA SYSTEM EXTENDED ADDRESS contains the extended address byte right-justified in the field. DMA SYSTEM HIGH/LOW ADDRESS contains the least-significant 16 bits of system address.

Warning:

In B205 applications, specifying the start address to be in the range of executable code >4000 - >7FFE will corrupt ADS code, causing unpredictable operation.

The parameter DMA REPEAT COUNT sets the number of times the DMA transfer will be repeated.

5.2.6.1 Command >85 Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >7X

The X bits in the fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

To verify that the data in the adapter was successfully transferred to attached system memory, the data written to attached system memory should be compared to the data contained in the RAM locations on the LAN adapter bus used for the DMA transfer. If the data found in attached system memory is not the same as the data in adapter RAM, the interface logic between the attached system and the TMS38030 should be carefully checked.

5.2.7 Command >90 - Test Expansion Memory

Command >90 tests the specified expansion RAM locations. This is done by alternately writing the patterns >AAAA and >5555 into each memory location and reading and comparing to the value written. The A205 (EPROM) version of this command differs from the B205 (download) version. The B205 version is designed to test both instruction and data partition in DRAM-based adapter designs.

5.2.7.1 A205 Version

The A205 version of command >90 has the following parameters which may be modified by rewriting the defaults via direct I/O.

Table 5-9. Command >90 Parameters

PARAMETER	DEFAULT VALUE	RAM LOCATION
Adapter RAM Starting Address	>0600	>05A0
Adapter RAM Ending Address	>0DFE	>05A2

Both address parameters must be even. If an odd value is provided, ADS will ignore the least significant bit.

A205 Version Completion Status

For the A205 version, the following status is posted in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >35 or >7X

An error code of >35 indicates that a bad RAM location was encountered or a ROM address was provided. The address which failed can be found by reading RAM location >05FE. If this error occurs, the expansion RAM connections and address decode should be verified correct.

Note:

The Protocol Handler (PH) does not decode address line A1 for access to internal ROM. Thus, all PH ROM is shadow-mapped to location >8000; i.e., an access of location >8000 is identical to location >C000. The expansion RAM decode logic must assure that $\overline{\text{PHCS}}$ is taken inactive high if RAM locations within the range >8000 to >BFFE are used. Failure to assure this may cause a bus conflict to occur.

The X bits in the >7X fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

5.2.7.2 B205 Version

The B205 version of this command utilizes the same parameters and locations as shown in Table 5-9. However, by initializing the ADAPTER RAM STARTING ADDRESS to either an even or odd value, either the data partition or the instruction partition may be tested in DRAM-based adapters.

Caution:

Use of the default parameter values as listed in Table 5-9 will cause this test to fail because B205 downloads the test program to CP RAM location >600. These default parameters must be changed prior to executing this command.

By initializing the ADAPTER RAM STARTING ADDRESS to be even (least-significant bit is set to zero), the command will test the data partition (with LI/$\overline{\text{D}}$ low). By initializing the ADAPTER RAM STARTING ADDRESS to be odd (least-significant bit is set to one), the command will test the instruction partition (with LI/$\overline{\text{D}}$ high).

B205 will download the memory test routine into RAM within the TMS38010 Communications Processor. Thus, this command can test RAM addresses occupied by B205 code or data.

B205 Version Completion Status

For the B205 version, the following status is posted in the least significant byte of the Interrupt register.

PASS = >40 or >41
FAIL = >35, >36, or >7X

If the memory test passed, either a >40 or >41 will be returned. If the address range to be tested was specified to be within the range of B205 code or data (>4000 - >7FFE), the test was destructive in that the test causes the B205 code and/or environment to be corrupted. If the test was destructive but the memory test passed, a code of >41 will be returned. If the test was non-destructive to B205 and the memory test passed, a code of >40 will be returned.

A destructive test indicates that B205 must be downloaded again to execute commands other than the >90 test expansion memory command. However, if any status other than a >7X status is returned, the memory test may be re-executed by writing the command byte (>90) to the most-significant byte of the Interrupt register. The parameters specified in Table 5-9 may also be changed as desired.

If the memory test failed, an error code of >35 or >36 will be returned. If the test was destructive and the memory test failed, a code of >36 will be returned. If the test was non-destructive to B205 and the memory test failed, a code of >35 will be returned. An error code of >35 or >36 indicates that a bad RAM location was encountered or a ROM address was provided. The address which failed can be found by reading RAM location >05FE. If this error occurs, the expansion RAM connections and address decode should be verified correct.

The X bits in the >7X fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

5.2.8 Command >91 - Test Wrap Function

Command >91 tests the wrap function of the ring interface circuit and the Protocol Handler (PH). ADS conditions the PH to transmit a frame through the wrap path of the ring interface ($\overline{\text{WRAP}}$ low and $\overline{\text{NSRT}}$ high). The frame is transmitted 20 times. After each transmission, the transmit status and receive status information is examined for errors. The transmit data is also compared to the receive data and an error is indicated if any differences exist. Normal completion indicates 20 frames were transmitted through the wrap path with no errors detected.

The frame transmitted has the following characteristics:

SOURCE ADDRESS = >4000 0666 6666

DESTINATION ADDRESS = >C000 FFFF FFFF (Group broadcast)

INFORMATION FIELD = Random data

FRAME LENGTH = 37 bytes

5.2.8.1 Command >91 Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt Register.

PASS = >40
FAIL = >35 or >7X

An error code of >35 indicates that an error was detected during the wrap test. Either the transmit or receive completion status indicated an error in one of those operations, or the comparison of the transmit data to the receive data failed. This could be due to CRC errors, code violation errors, or an error in the PH DMA interface to the LAN adapter bus.

If an error code of >35 is received, the ring interface circuit should be verified for proper connections. If this error persists, it is recommended that the TMS38051, TMS38052, and BIA PROM (if present) be removed from the ring interface circuit, and the PH jumpered as shown in Figure 5-2. This wraps the driver output to the receiver input pins of the PH, thus isolating the PH from the ring interface. This command should be executed again. If an error occurs, the problem may be with either the PH's DMA interface to the LAN adapter bus or in the PH itself. Be sure that the PH's bus request and bus grant lines ($\overline{\text{LBRQP}}$ and $\overline{\text{LBGRP}}$) are properly connected to the TMS38010. If no error occurs, a possible error in the ring interface circuit may exist. The ring interface circuit should be verified for proper interconnect and physical layout should conform to the guidelines presented in Section 6.

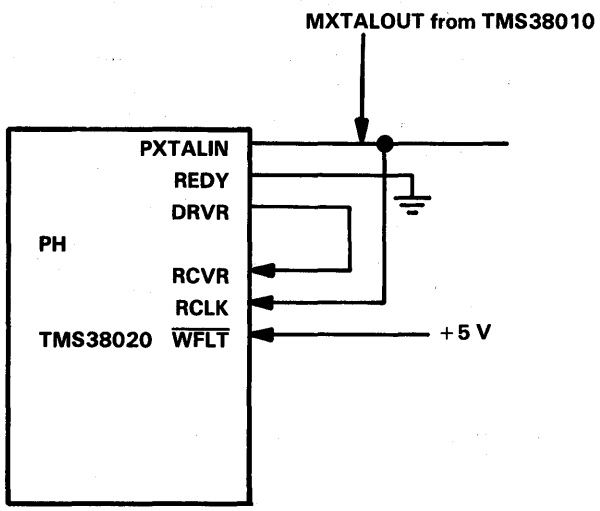


Figure 5-2. PH Jumper Configuration

The X bits in the >7X fail code indicate the failure reason. Table 5-5 provides a list of these codes, their meaning, and possible causes.

5.2.9 Command >92 - Test Lobe Function

The command >92 function is identical to command >91 described above except the ring interface is not put into wrap mode ($\overline{\text{WRAP}}$ is held high). However, the adapter is not inserted ($\overline{\text{NSRT}}$ is held high). This causes the transmit frames to circulate on the lobe media cable. Note that the adapter need not be physically connected to a wiring concentrator for this command to function correctly. However, a lobe media cable equipped with a standard self-shorting connector must be attached for this command to function correctly.

5.2.9.1 Command >92 Completion Status

For this command, the following status is posted in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >35 or >7X

An error code of >35 indicates that either the transmit completion status or the receive completion status, or both, indicate an error condition. This could be due to CRC errors, code violation errors, or an error in the PH DMA interface to the LAN adapter bus. The receive data is also compared to the transmit data and an error will be indicated if they are not equal.

If the wrap test (Command >91) passed yet this command fails, a possible problem exists in the receiver and transmitter portions of the ring interface circuit. The transformer connections and passive components for setting receive hysteresis and equalization should be verified. A faulty or loosely-connected lobe media cable may also cause an error.

If a >7X fail code is indicated, Table 5-5 should be consulted for the meaning and possible cause.

5.2.10 Command >93 - Test Insert Function

Command >93 is identical to command >92 except that the $\overline{\text{NSRT}}$ signal is asserted active-low. This activates the phantom drive of the ring interface which will insert the adapter into a ring when the adapter is connected to a wiring concentrator through the lobe media cable.

Because this command inserts the adapter in a network, do not connect the adapter to a functioning network as this command does not provide Medium Access Control protocols compatible with the network. The adapter should be the only connection on the wiring concentrator when executing this test.

> **Note:**
>
> Command >93 delays approximately 120 milliseconds between the assertion of $\overline{\text{NSRT}}$ (activating phantom drive) and the start of frame transmission. If the wiring concentrator you are using requires several seconds to switch the relays for insertion, Command >9A (TEST INSERT FUNCTION WITH INSERTION DELAY) should be used.

5.2.10.1 Command >93 Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >35 or >7X

If the error code >35 is returned and commands >91 and >92 passed successfully, a possible error in the wiring concentrator or network cabling may be present. The functioning of the wiring concentrator and the network cabling should be carefully checked.

The X bits in the >7X fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

5.2.11 Command >94 - Extended Checksum Test

Command >94 performs an extended ROM checksum from address >8002 through address >FFFE. This command is available only with A205 ADS. This verifies that the full address extent of 16K × 8 EPROMS may be accessed by the Communications Processor. Note that the Phase 2 test of Stage 1 of ADS only calculates a checksum from >C000 through >FFFE since the A205 executable code actually resides from >C000 through >FFFE. This allows the ADS EPROMs to be used in adapter designs which only provide 8K × 8 sockets.

The A205 EPROMs contain a full ROM checksum at the first location within the EPROMs. This command calculates the checksum between >8002 and >FFFE and compares the calculated value with the stored value. The first half of the EPROM between >8002 and >BFFE is filled with the pattern >AA.

5.2.11.1 Command >94 Completion Status

Upon completion of command execution, ADS posts the following status in the least-significant byte of the Interrupt register.

PASS = >40
FAIL = >35 or >7X

An error code of >35 indicates that the calculated checksum did not agree with the checksum stored at address >8000. Verify that the EPROMs and address decode are connected properly.

If a >7X fail code is indicated, Table 5-5 should be consulted for the meaning and possible cause.

5.2.12 Command >95 - Test Watchdog Timer

Command >95 checks the watchdog timer function implemented by the 74LS122 located between the PH and the ring interface. The watchdog timer is tested by:

1. Verifying that the 74LS122 does not timeout for at least 20 milliseconds.
2. Verifying that the 74LS122 has timed out after 40 milliseconds.
3. Verifies that $\overline{\text{NSRT}}$ cannot be asserted when $\overline{\text{WRAP}}$ is activated.

Note that this test will not work when the adapter is connected to a wiring concentrator (WC). However, the lobe media cable should be connected to the adapter before executing this test.

5.2.12.1 Command >95 Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >35 or >7X

An error code of >35 indicates that the watchdog timer function failed this test. Verify that the appropriate time constant components are being used for the 74LS122 one-shot. The timing capacitor should be 0.47 μF and the timing resistor should be 150 kΩ. All connections to the 74LS122 should be verified correct.

If a >7X fail code is indicated, Table 5-5 should beconsulted for the meaning and possible cause.

5.2.13 Command >96 - Repeat Mode Without Insert

Command >96 is used to put the PH Protocol Handler into repeat mode without inserting into the ring ($\overline{\text{NSRT}}$ is maintained inactive-high). This function is useful for performing specialized tests on the ring interface circuit.

The effects of this command may be terminated by executing command >98.

5.2.13.1 Command >96 Completion Status

Upon completion of command initiation, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >7X

If a >7X fail code is indicated, Table 5-5 should be consulted for the meaning and possible cause.

5.2.14 Command >97 - Repeat Mode with Insert

Command >97, like command >96, puts the PH Protocol Handler into the repeat mode, however, unlike command >96, $\overline{\text{NSRT}}$ is taken active-low, inserting the adapter into the ring if the adapter is connected to a wiring concentrator.

To terminate the function initiated by this command, command >98 must be executed.

5.2.14.1 Command >97 Completion Status

Upon completion of command initiation, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >7X

If a >7X fail code is indicated, Table 5-5 should be consulted for the meaning and possible cause.

5.2.15 Command >98 - Terminate Command

Command >98 terminates the effects of command >96 or >97. The repeat mode of the PH is stopped and the adapter is de-inserted if previously inserted.

5.2.15.1 Command >98 Completion Status

For this command, the following status is posted in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >7X

If a >7X fail code is indicated, Table 5-5 should be consulted for the meaning and possible cause.

5.2.16 Command >9A - Test Insert Function with Insertion Delay

This command functions identically as Command >93 except frame transmission is delayed for approximately 15 seconds to allow the wiring concentrator to switch the relays.

This command should be used in lieu of Command >93 if your wiring concentrator requires several seconds to switch.

5.2.16.1 Command >9A Completion Status

Upon completion of command execution, ADS posts the following status in the least significant byte of the Interrupt register.

PASS = >40
FAIL = >35 or >7X

If the error code >35 is returned and commands >91 and >92 passed successfully, a possible error in the wiring concentrator or network cabling may be present. The functioning of the wiring concentrator and the network cabling should be carefully checked.

The X bits in the >7X fail code indicate the failure reason. Table 5-5 provides a list of these error codes, their meaning, and possible causes.

6. Ring Interface Layout Guidelines

The layout of the TMS380 LAN Adapter Ring Interface requires special attention be given to the placement of components to reduce induced noise and parasitic loading. This appendix will define a set of guidelines that can be used for the layout of the Ring Interface circuit. First, the Ring Interface signals will be broken down into four basic categories. Second, layout considerations will be given for each of these categories.

6.1 Ring Interface Signal Classification

The signals within the Ring Interface can be grouped into four types: Digital Data, Digital Control, Analog, and Differential Data. Digital Data signals have voltage swings that are compatible with standard TTL logic. Digital Control signals have identical voltage swings to Digital Data signals but typically have a very low switching rate. Differential Data is any signal that is transmitted or received on the twisted-pair transmission media. Transmitted Differential Data typically has an amplitude of 3.75 V peak-to-peak and received differential data has a minimum amplitude of 50 mV peak-to-peak. Table 6-1 lists the four signal types and their corresponding Ring Interface signals.

Table 6-1. Ring Interface Signal Classification

SIGNAL TYPE	SIGNAL NAME
Differential Data	RCVINA, RCVINB, DROUTA, DROUTB, PHOUTA, PHOUTB
Digital Control	$\overline{\text{WRAP}}$, FRAQ, $\overline{\text{REDY}}$, $\overline{\text{NSRT}}$, $\overline{\text{WFLT}}$, ENERGO, ENERGI ENABLE
Digital Data	RCLK, XTAL, DRVR, RCVR, DCLKIN, DCLKOUT
Analog	VCOCPA, VCOCPB, VCOGAN, LOCKIN, LOCKRF, FILTER, CHGPMP, EQUALA, EQUALB, RCVHYS, NRGCAP

6.2 Layout Guidelines

The following layout guidelines were developed for a four-level board. These guidelines may also be used for a two-level board with the exception of routing digital and analog signals on different levels and providing separate power and ground planes. A two-level layout should dedicate one of the levels as a ground plane.

6.2.1 Differential Data

The following table lists the discrete components that are associated with Differential Data signals.

Table 6-2. Discrete Components — Differential Data

SIGNAL	FUNCTION	PIN	COMPONENTS
RCVINA	Receiver	TMS38051 #14	D5-8, C7-8, R7-10, L1, T2
RCVINB		TMS38051 #15	
DROUTA	Transmitter	TMS38051 #2	D9-13, C9, R12-13, T1
DROUTB		TMS38051 #3	
PHOUTA	Phantom	TMS38052 #18	D1-4, C10-11, R14-15
PHOUTB	Drive	TMS38052 #19	

Component placement and layout guidelines for Differential Data signals are as follows.

- The transmit pair, DROUTA and DROUTB, should be run as close together as possible on both the primary and secondary side of the transformer. The separation of these two signals should not exceed 0.3 inches. Trace distance to transformer T1 should be minimized and both DROUTA and DROUTB should be routed on the same card level.
- Discrete components associated with the transmit pair need not be placed close to DROUTA and DROUTB pins on the TMS38051.
- The receive pair, RCVINA and RCVINB, should be run as close together as possible on both the primary and secondary side of the transformer. The separation of these two signals should not exceed 0.3 inches. Trace distance to transformer T2 should be minimized and both RCVINA and RCVINB should be routed on the same card level.
- Discrete components associated with the receive pair need not be placed close to RCVINA and RCVINB pins on the TMS38051.
- The transmit and receive pair should not be routed near Digital Data signals. If possible, the transmit and receive pair should be routed on a different level from the Digital Data signals.
- Where possible, the transmit pair should be separated from the receive pair by at least one inch. The transformers, T1 and T2, should also be separated by at least one inch.
- Routing of the Phantom Drive pair, PHOUTA and PHOUTB, and the placement of the associated discrete components is not critical.

6.2.2 Digital Control

The Digital Control signals have no discrete components associated with them and require no special layout considerations.

6.2.3 Digital Data

The Digital Data signals have no discrete components associated with them. Routing of these signals should be done in accordance with the following guidelines:

- Digital Data signals should be routed on a different card level than Analog signals.
- DCLKOUT to DCLKIN trace length should be minimized and routed away from the VCO and PLL filter components and pins.
- The TMS38020 Protocol Handler should be placed near the Ring Interface to avoid long trace lengths for RCVR, DRVR, and RCLK.
- Problems can occur with signals operating at the same frequency as, but not phase coherent with, the VCO frequency. To avoid this problem, DCLK should not be routed near the VCO and MXTALOUT should be gated by FRAQ outside the Ring Interface area. The gating configuration for MXTALOUT is illustrated in Figure 6-1.

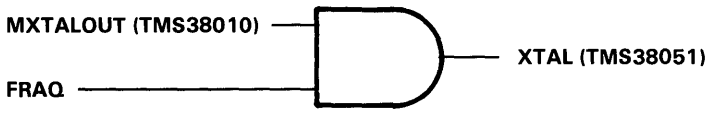


Figure 6-1. XTAL Gating Configuration

6.2.4 Analog

The following table lists the discrete components that are associated with Analog signals.

Table 6-3. Discrete Components — Analog

SIGNAL	FUNCTION	PIN	COMPONENTS
VCOCPA VCOCPB	VCO	TMS38052 #4 TMS38052 #5	C2
VCOGAN	VCO	TMS38052 #2	R3
FILTER CHGPMP	PLL Filter	TMS38052 #3 TMS38051 #18	R5, R16, C4, C5
EQUALA EQUALB	Equalizer	TMS38051 #12 TMS38051 #13	R1, R2, C1
RCVHYS	Hysteresis	TMS38051 #11	R4
NRGCAP	Energy Detect	TMS38051 #20	C3

Component placement and layout guidelines for Analog signals are as follows.

- Analog signals should be routed on a different card level from Digital Data signals.
- Components should be grouped as in Table 6-3. Components within each group should be tightly packed close to the appropriate pin. PLL filter components should be placed close to TMS38051 pin 18.
- Routing from pin to component should be minimized. The maximum distance should be 1/2 inch.
- Signals not associated with the VCO or PLL Filter should not be routed near components, signals, or pins associated with these functions.

6.3 Power and Ground

The following guidelines should be followed for supplying power to and grounding the Ring Interface components:

- The Ring Interface should have power and ground planes that are isolated from the power and ground planes of the rest of the adapter. The power and ground of the Ring Interface should be connected to the adapter power and ground at one point only. The power plane should be filtered at this point. A suggested value for this filter capacitor is 4.7 μF.

- Separate power and ground planes should be used to minimize the inductance to ground or V_{CC}.
- All V_{CC} inputs to the TMS38051 and TMS38052 should be filtered. A suggested value for this filter capacitor is 0.1 μF.
- The shield of the transmission cable should be attached to the chassis ground of the host system, not to the card ground.

7. TMS38021 Bridge Application

Several bridging methods have been proposed by IEEE 802 and various manufacturers. Two of these methods are discussed in Section 7.2: the source routing bridge and the adaptive bridge. Although most bridge types can be implemented directly by the TMS380 chipset, a new feature has been added to the TMS38020 Protocol Handler to enhance performance and flexibility of adapters for these and similar applications. The result is the TMS38021 Protocol Handler. Bridge performance can be enhanced by utilizing the extended copy hardware interface of the TMS38021. Sections 7.13 and 7.14 provide design examples of source routing bridge implementations utilizing the TMS380 with the TMS38021 Protocol Handler and external copy hardware. Section 7.3 contains a description of the TMS38021, and the full data sheet for the TMS38021 may be found in Appendix A.

Most bridging methods have in common several identical adapter characteristics required for implementing the bridge function. These requirements include the ability to maintain the original packet CRC across segment boundaries and the necessity to transmit forwarded packets using the orginal source address of the sender. These are requirements not normally demanded by attaching products on the network.

To provide these capabilities for bridging applications, you may use TMS380 DLC software, or an alternate version of MAC-level software is available. This MAC-level software is identified by the designation Bridge Options software. Section 7.3 provides a description of this adapter software.

7.1 TMS380 Bridging Applications — General

Bridges are a desirable expansion tool for increasing the number of nodes on a Local Area Network (LAN). They allow different LAN technologies to co-exist in a network. Bridges may also ease the management of a LAN, and can increase performance by separating the LAN into distinct sections, such as corporate departments or floors of a building. A bridge, by IEEE 802 definition, is a functional unit that connects two LANs that use a single Logical Link Control (LLC) procedure but may use different Medium Access Control (MAC) procedures. Since other functional units such as routers or gateways are sometimes referred to as bridges, we will qualify an IEEE 802 bridge as being a MAC layer bridge. These MAC layer bridges operate below the Logical Link Control (LLC) level. This allows the expansion of Local Area Networks to more nodes than is currently allowed and interconnection of different LANs. A MAC layer bridge contains a logical "switching" layer, as shown in Figure 7-1.

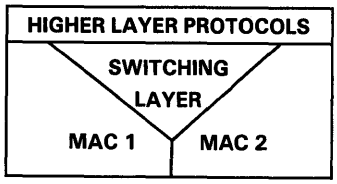


Figure 7-1. Generic MAC Layer Bridge

The attractive aspect of a MAC layer bridge is that the LAN can be expanded without the knowledge of higher layer protocols. Thus, the burden of frame routing is kept at the lower protocol layers, and higher layer protocols can execute other tasks more efficiently. This leads to higher overall network performance. With MAC layer bridges, the source and destination addresses of the frame on the medium are the MAC addresses of the originating and target stations, respectively. The bridge makes a routing decision based on the contents of the frame header preceding the LLC header. This decision may be based on the destination address itself, or on a routing information field. These options will be discussed later. Figure 7-2 shows an example of a MAC layer bridge.

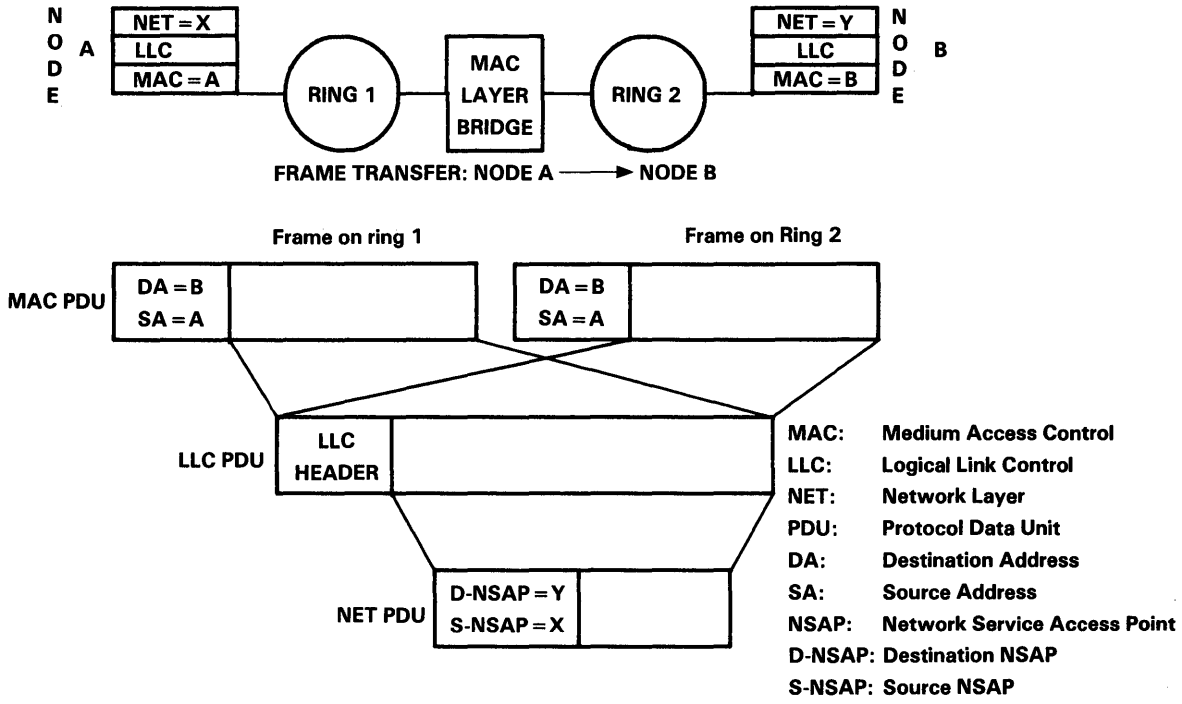


Figure 7-2. MAC Layer Bridge

7.1.1 MAC Layer Bridge Alternatives

There are two types of MAC layer bridges which will be discussed in this section; Source Routing and Adaptive. Before describing the technical merits of each approach, a brief explanation of the capabilities of MAC bridges is in order.

The features which are common to both bridging techniques include:

1. End-to-end Frame Check Sequence (FCS) coverage
2. Higher transmission priority
3. Source address overlay

End-To-End FCS Coverage. End-to-end FCS protection is desired across bridges that connect like MACs to preserve data integrity across the bridge. If a station is communicating with another station over an extended LAN consisting of identical MACs (i.e., token-ring to token-ring, or CSMA/CD to CSMA/CD), the bridge should not recalculate the FCS.

FCS TRANSMISSION — The TMS38020/21 (PH) has a mode for its transmit state machine called Transmit FCS. In this mode, the PH will not generate a FCS, but will transmit one that is stored in adapter memory along with the frame data. Bridge Options software and DLC software support the selection of this mode by the host system (see Section 7.3).

FCS RECEPTION — The PH will always store the received FCS in Adapter memory along with the frame. This information can be passed to the host system for retransmission with the frame (See Section 7.3).

Higher Transmission Priority. A second desirable feature of MAC layer bridges is that the bridge can transmit at a higher priority than other stations on the ring. As the bridge might become a performance bottleneck, having higher priority would allow improved access to the destination LAN by a bridge. The architecture of the token-ring and the TMS380 provides up to seven levels of token priority on the ring. The TMS380 restricts normal stations to priority levels 0 through 3. Bridge Options software and DLC software allow a bridge to transmit on the ring at a priority greater than normal stations. This would assure the bridge the quickest possible access to the ring. Since priority is requested at each frame transmission, the priority of a bridge could be dynamically altered. This would prevent using higher than necessary priority on the LAN if traffic is not heavy.

Source Address Overlay. A MAC layer bridge should not be visible in the MAC address fields of a frame. It is therefore necessary for a bridge to be able to transmit a frame with the source address of the originating station and not its own. In the case of the token-ring, the bridge must ensure proper stripping of the frame from the ring. The TMS38020/TMS38021 Protocol Handler (PH) allows the transmission of a source address other than the one stored in its internal address registers. The Bridge Options software and DLC software allow the attached system to pass the source address of the transmitted frame.

7.1.2 Adaptive Bridging

In the Adaptive bridging technique, a bridge listens to all traffic on LANs connected to it and "learns" where stations are, relative to itself. Individual stations are unaware of whether the destination station is actually on the same LAN as itself or on a remote LAN.

The Adaptive bridge (which copies all frames) routes frames to the LAN where it has learned the destination station resides, or discards the frame if the destination station is on the same LAN as the source station.

Since an Adaptive bridge copies all frames, regardless of their destination address, the bridge should not affect the Address Recognized (ARI) and Frame Copied (FCI) indicators in a frame unless the frame is destined for the bridge itself. This is because of the use of the ARI and FCI bits during a station's insertion onto the ring. Should an Adaptive bridge alter these bits, no station would be able to successfully pass the Address Verification phase of the Open process. Stations would always think that another station existed with the same individual address.

Adaptive Bridges and the TMS380. Both the TMS38020 and TMS38021 Protocol Handler with Bridge Options software or DLC software (see Section 7.3) support a "promiscuous" mode that copies all frames from the ring, regardless of the destination address. In this mode, the ARI and FCI bits are not set unless the destination address in the frame is the Adapter's specific, group, or functional address. Thus, an Adaptive bridge could be implemented using the Bridge Options software or the DLC software.

7.1.3. Source Routing Bridging

A bridging scheme under consideration by IEEE 802 and supported by IBM is source routing. In source routing, a sending station must locate the destination station if it is not on the same LAN segment. After locating the destination, the source station inserts a "Routing Information Field" immediately following the source address in every frame sent to the destination station. The destination station also uses the routing field to reach the originating station.

The routing information field size is variable up to 18 bytes in length. Its presence is indicated by a one in the most significant bit of the source address of a frame. If the MSB of the Source Address is set to one, a routing information field will follow the source address field. The format of the routing information field is shown in Figure 7-3.

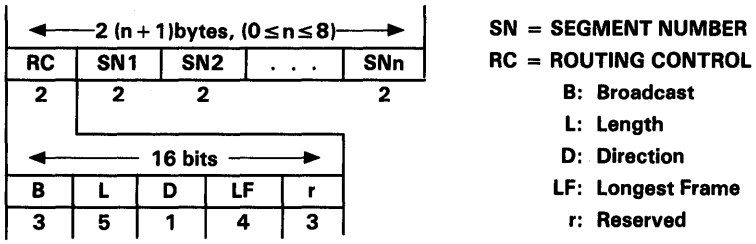


Figure 7-3. Routing Information Field Format

B – Broadcast Bits. These bits indicate whether the frame is to be sent along a specified path, to all rings in a network along all possible paths, or to all rings along designated bridges which result in only one copy on a given ring.

The coding for these bits is as follows:

000 = Non-broadcast. If the bits are set for non- broadcast, the segment number fields contain the specified route through the network the frame is to travel.

100 = All-routes broadcast, non-broadcast return. If the bits are set for all- routes broadcast, the frame will be transmitted on every route within the network resulting in multiple copies on a given ring.

110 = Single-route broadcast, non-broadcast return. If the bits are set for single-route broadcast with non-broadcast return, the frame will be transmitted across designated bridges, which will result in the frame appearing only once on each ring.

111 = Single-route broadcast, all routes broadcast return. If the bits are set for single-route broadcast with all routes broadcast return, the frame will be transmitted across the designated bridges, which will result in the frame appearing only once on each ring. The response frame is on all routes broadcast to the originator.

L – Length. This field indicates the length of the routing information field in bytes, including the control field.

D – Direction. This indicates to a bridge whether a frame is traveling from the originating station to the target or the other way around. This bit allows the ring number segments to appear in the same order, regardless of the direction of transmission.

LF – Largest Frame. The LF bits specify the largest size of the MAC information field that may be transmitted between two communicating stations on a specific route. The coding of the LF indicates the following:

-0000 reserved

-0001 Up to 516 octets in the information field

-0010 reserved

-0011 Up to 1500 octets in the information field

-0100 reserved

-0101 Up to 2052 octets in the information field

-0110 reserved

-0111 Up to 4472 octets in the information field

-1000 reserved

-1001 Up to 8191 octets in the information field

-1010 reserved

-1011 reserved

-1100 reserved

-1101 reserved

-1110 reserved

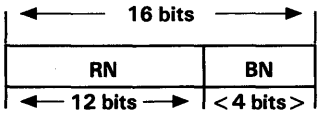
-1111 Initial value of broadcast frames.

r – Reserved. These bits are reserved.

SNx – Segment Numbers. These 16-bit fields indicate the path between nodes on different physical rings. The segment number fields have the construct shown in Figure 7-4.

The ring number portion of the segment number field is different for each ring in the network. Thus, any two bridges connecting to the same ring will have identical RN portions.

The individual bridge number of the segment number field allows two bridges connecting the same two rings to provide alternative paths between the two rings.



where: RN = Ring Number
BN = Bridge Number

Figure 7-4. Segment Number Field

Communicating with Source Routing Bridges. Bridges must examine each frame as it circulates on the LAN segment to determine if the frame should be forwarded to the other ring. Source routing bridges examine the most-significant bit of the source address field to first determine if a routing information field exists. If this bit is set to zero, indicating no routing field exists, the bridge will not copy the frame unless the frame is explicitly addressed to the bridge's ring station specific address. Frames which have a non-broadcast source routing field are transported between two rings if the segment number

of the source ring followed by the ring number portion of the destination ring matches the bridge's values for these parameters.

The bridge must scan the contents of the routing information field to determine if the source ring segment number and destination ring number to which it connects are contained in the field and are in the proper order.

Figure 7-5 illustrates a routing information field which will route a frame from Station A to Station B.

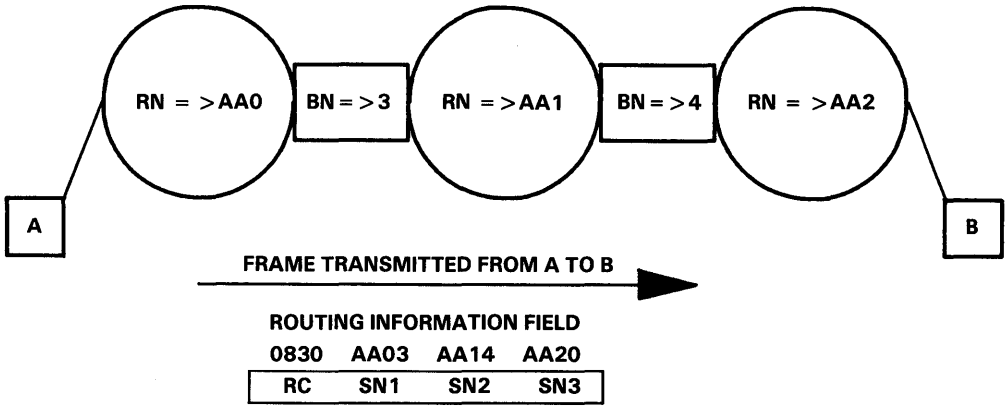


Figure 7-5. Example Routing Between Station A and Station B

In order for Station A to communicate with Station B, the RII bit of the source address field must be set and a routing information field included in the frame to indicate a route between the two stations. Station A will insert the routing information field shown in Figure 7-5 after the source address field. Note that the routing control field (RC) of the frame is set to >0830. This indicates that the source routed frame is a non-broadcast frame; the length of the routing information field is eight bytes; the segment number list should be scanned by the bridges from left to right; and the largest frame that either station can send is 4472 octets.

Remembering that the segment number is made up of two parts, the ring number and the bridge number, bridge 3 would scan the segment number list from left to right looking for the segment number >AA03. >AA0 is the ring the frame is currently being transmitted on and >3 is the bridge's own bridge number. If this segment number was found in the list, the bridge then compares the next segment number in the list for the ring number >AA1, which is the the second ring the bridge is connected to. If the ring number matches, bridge number >3 would forward the frame to Ring.

In the same manner, bridge number >4 would scan the segment number list for the segment number >AA14. In this case, >AA1 is the ring the frame is being transmitted on and >4 is its own bridge number. Bridge >4 would then check the next segment number in the list for a ring number of >AA2. >AA2 is the second ring to which the bridge is connected to. After the compare has been made, bridge >4 would then transmit the frame onto Ring >AA2. Station B copies the frame based on an address match of the destination address field.

Handling of ARI/FCI Bits. A source routing bridge may set the Address Recognized Indicator (ARI) bits and the Frame Copied Indicator (FCI) if it is determined that the frame should be transported across the bridge to the other segment as shown above. However, if upper level protocol software does not examine these bits, the bridge need not set these bits.

Broadcast Frames. In order for stations on different LAN segments to communicate using source routing, a route between the two stations must first be determined. The originating station will send out a frame with the broadcast bits set in the routing contol field. The largest frame bits (LF) will be set to the initial value of b'111' and the segment number fields will be empty.

Each time the frame is copied from a LAN segment and prior to being forwarded to the bridge's other LAN segment, the bridge will scan the segment number list to determine if its respective segment number is already contained in the segment number list. This check ensures that the frame has not been previously forwarded by the bridge and prevents all segment broadcast frames from indefinitely circulating on the network. If the bridge finds that its segment numbers do not exist in the segment number list, the bridge will add its segment number to the routing information field segment number list and forward the frame to its other LAN segment. Thus, the segment number list is dynamically created as the frame propagates across bridges throughout the network.

If the bridge's frame size capability is smaller than that defined by the LF bits in the routing field, the bridge will modify this field to ensure that the bridge can transmit any frame sent between the two communicating stations.

Once the frame has reached the destination station, the destination station will send a response frame back with the broadcast bits set to non-broadcast, the direction bit inverted, and the identical segment number list which was received. Since it is a non-broadcast frame, the frame will travel on the route specified by the segment number list. Once the originating station receives the response frame, both stations have the route needed for communications.

7.1.4 Source Routing Bridges and the TMS380

The TMS380 operates with a source routing bridge and, therefore, allows stations to transmit frames which include a routing information field and a one in the MSB of the source address. The TMS38021 Protocol Handler facilitates design efforts for a bridge with the External Copy Hardware Interface, which gives a station flexibility in its frame copy decision. There are several design approaches by which the TMS380 can be used to implement a source routed bridge. Three of these approaches are briefly described below. As illustrated in Figure 7-6, each of the design approaches defines a MAC bridge as two TMS380 LAN adapters each connected to a separate ring but sharing a common host.

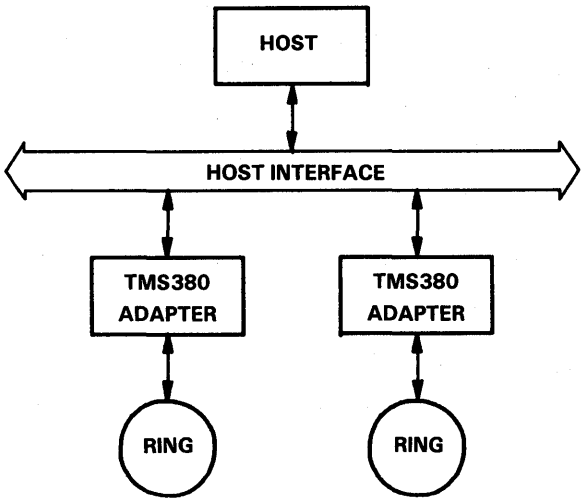


Figure 7-6. Design Examples MAC Bridge

APPROACH 1: Software-Based Source Routing Bridge

This approach is accomplished in software and requires no additional hardware support. Both the TMS38020 and TMS38021 Protocol Handler, along with the "copy all frames" capability of Bridge Options software or DLC software can be used to implement this design. Each bridge on each ring copies and passes to the host system all frames circulating on its specific ring. Since the host would receive all frames circulating on the ring, the host software must inspect each frame to determine if the frame is to be forwarded to the next ring.

APPROACH 2: Software/Hardware-Based Source Routing Bridge

This approach uses the External Copy Hardware Interface of the TMS38021 Protocol Handler to copy only those frames which have the Routing Information Indicator (RII) bit set in the source address field. By using this method, the bridge would not copy a large number of unnecessary frames but only those frames destined across bridges. Once the frame is copied into host memory, the host determines if the frame should be forwarded to the next ring. This forwarding process is done by comparing the bridge's unique segment number with those found in segment number field of the frame. It should be noted that since the adapter copies frames with the RII bit set, all frames which are transmitted by the bridge would be copied by the bridge again. Therefore, the bridge will copy each frame twice to host memory. A detailed hardware example of this implementation can be found in Section 7.12.

APPROACH 3: Hardware-Based Source Routing Bridge

The third method also takes advantage of the External Copy Hardware Interface available on the TMS38021 by implementing a complete routing checker in hardware. The External Copy Hardware (ECH) will not only check to see if the RRI bit has been set, but it will also determine if its own segment number is included in the routing information field. By implementing this compare in hardware, the host would be free for other activities and maximum bridge throughput is obtained. Only those frames which include the bridge in its routing field would be copied. Of course, the compare hardware needed for this bridge is significantly more complex then in the previous two examples. However, by using ASIC design tools available today, the logic necessary for this function can be implemented in a single chip. A high level design example for this function is shown in Section 7.13.

7.2 TMS38021 Protocol Handler

This section provides a brief discussion of the added features of the TMS38021 Protocol Handler over the TMS38020 Protocol Handler. The TMS38021 is a pin compatible replacement for the TMS38020 and provides the following added capability:

- Support for both universally and locally administered station address assignments.
- Provides a unique External Copy Hardware Option (ECHO) interface which allows user-added hardware to define additional frame copy criteria beyond the normal address recognition capability of the Protocol Handler.

7.2.1 Addressing—The TMS38020

Figure 7.7 illustrates the addressing currently provided by the TMS38020 Protocol Handler.

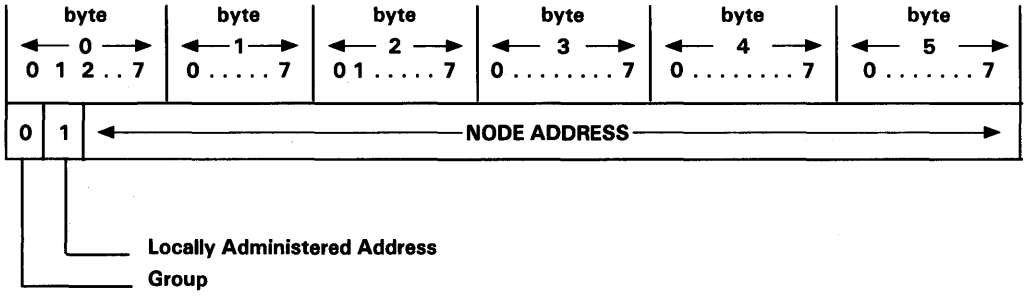


Figure 7-7. Ring Station Address — TMS38020

Note that bit 1 of byte 0 of the node address is required to be set to one (locally administered address). This restriction is because the TMS38020 Protocol Handler hardwires this bit to one in its node address register.

7.2.2 Addressing — The TMS38021

Figure 7-8 illustrates the addressing incorporated into the TMS38021 Protocol Handler.

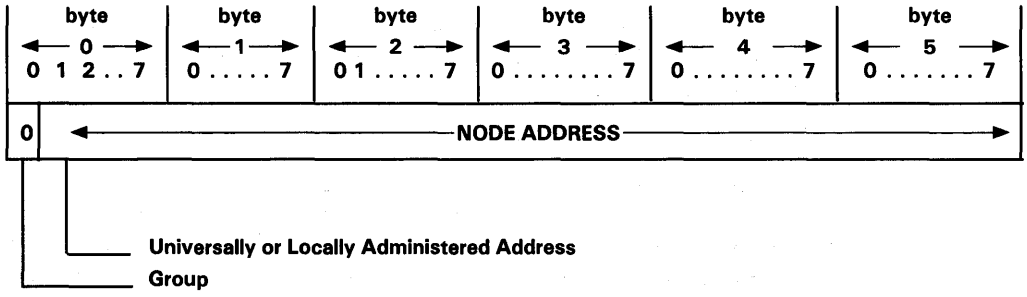


Figure 7-8. Ring Station Address — TMS38021

As can be seen in Figure 7-8, the TMS38021 allows bit 1 of byte 0 of the node address to be set to either a zero or a one. (Either a universally or locally administered address may be assigned.)

7.2.3 Obtaining Universal Address Block Assignments

The IEEE administers the assignment of blocks of universal addresses to manufacturers wishing to use such addresses for a higher degree of uniqueness. The following address may be used to contact IEEE for these assignments:

Secretary, IEEE Standards Board
345 East 47th Street
New York, NY 10017
212-705-7900

7.2.4 External Copy Hardware Option

The External Copy Hardware Option (ECHO) interface provides a method of extending the frame copy decision capabilities of the Protocol Handler beyond the standard ring address recognition function. External hardware may be added by the designer to implement user specific criteria for copying frames from the ring. This external hardware operates in parallel with the internal TMS38021 address checker to determine which frames should be copied. This capability may be used to copy frames based on different addresses, for purposes of adaptive bridges, source routing bridges, system test, line monitoring, or specialized LAN server functions.

These modifications include the addition of the External Copy Hardware Option (ECHO) interface, which provides the medium for the TMS38021 to signal the presence of data, and the ECHO hardware to signal the results of its frame check, selecting to copy or not to copy the frame.

7.2.4.1 Requirements for External Copy Hardware

The ECHO interface makes use of the recoverable buffering technique used by the TMS38021. The TMS38021 writes a frame to memory while it is checking the address of the frame, and then recovers the buffer if the frame is not to be copied. Thus the address fields of the frame are available on the LAN adapter bus for capture by the ECHO hardware.

In order to let the ECHO hardware know which bus cycles carry data, the TMS38021 indicates the first data transfer of a frame. Following cycles are "traced" in the manner described below. The "pass", "fail", and "first-data" signals can share two TMS38021 pins.

The first data transfer of a frame (AC/FC bytes) is indicated to the ECHO hardware so that the address of this write can be latched and used to trace succeeding data transfers. Data is stored sequentially into memory, so incrementing this latched address gives the address of the next data write. By comparing this new address to the address/data bus, the transfer of the next word of the frame can be recognized. The latch is incremented again, and the process continues until the completion of the frame check.

Until both internal and external checks are complete, the Protocol Handler does not know whether to accept or reject the frame. It cannot assume that the external hardware timing is the same as its own. This is especially true for Source Routing, where a decision may depend on the destination address field, or the routing field, depending on the value of the RII bit. The TMS38021 must buffer data until explicitly signaled that the external frame check has been completed. This is indicated by one of two signals: $\overline{\text{XMATCH}}$, or $\overline{\text{XFAIL}}$. $\overline{\text{XMATCH}}$ indicates the frame should be copied, while $\overline{\text{XFAIL}}$ indicates that the frame should not be copied and the buffer should be recovered unless an internal address match occurred.

7.2.4.2 External Copy Hardware Interface Pin Functions

Figure 7-9 illustrates the Protocol Handler pinout for using ECHO hardware. If pins 40 and 42 are not connected, then the operation is the same as the current TMS38020. The TMS38021 has an internal pull-down on pin(40) and internal pull-down on pin(42).

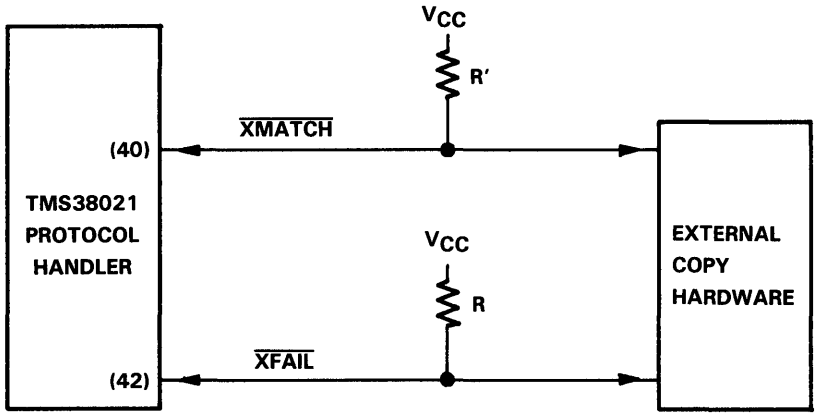


Figure 7-9. TMS38021 External Copy Hardware Interface Pins

The interface consists of two wire-and signal lines $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$, which carry bidirectional information between TMS38021 and an external checker. External pull-ups "R" are required, as the lines are only ever driven low (open collector or open drain drivers are used). The $\overline{\text{XMATCH}}$ signal is output on pin 40 of the TMS38021, and $\overline{\text{XFAIL}}$ on pin 42.

The TMS38021 drives both lines low to indicate the first data transfer of the frame (AC/FC). This causes the external hardware to reset and ready itself for a new frame. When the external hardware has checked the frame it signals its result by driving one of the two lines low: $\overline{\text{XMATCH}}$ if it matches, $\overline{\text{XFAIL}}$ if it does not.

The following table summarizes the above.

Table 7-1. $\overline{\text{XMATCH}}$, $\overline{\text{XFAIL}}$ Pin Functions

$\overline{\text{XMATCH}}$	$\overline{\text{XFAIL}}$	FUNCTION
High	High	Default state of the interface
Low	Low	Asserted by TMS38021 to indicate start of frame and that the FC/AC word of the frame will be transferred on the bus this cycle.
Low	High	Asserted by the external hardware to indicate it has completed its frame check and that the frame should be copied.
High	Low	Asserted by the external hardware to indicate it has completed its frame check and the frame should not be copied unless an internal address match occurs.

7.2.4.3 Timing Requirements

For checking to be successful, $\overline{\text{XMATCH}}$ must be asserted low two LAN adapter bus cycles after the transfer of the last byte of information field on the adapter bus.

7.2.4.4 Disabling the Interface

The TMS38021 has internal pulldowns on $\overline{\text{XFAIL}}$ (pin 42) and $\overline{\text{XMATCH}}$ (pin 40). However, the $\overline{\text{XFAIL}}$ pin takes precedence over the $\overline{\text{XMATCH}}$ pin. This ensures that if the interface is unconnected, the interface always signals $\overline{\text{XFAIL}}$ condition, which is equivalent to disconnecting the interface. (The TMS38021 will match only on its internal address compare.)

7.2.4.5 Receive Options

Externally matched frames will not be copied when the ROPT bits of the RINGCMD1 register are set to "Copy only Express Buffers"; however, ARI bits will be set.

7.2.4.6 No Indication from External Checker

If the external checker does not assert either $\overline{\text{XMATCH}}$ or $\overline{\text{XFAIL}}$, the incoming frame is copied into the adapter until the first adapter buffer is filled. If, at this time, there is no indication from the external checker, or if there are pullups on $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ with no external checker present, unpredictable operation will result. Therefore, external hardware must give an indication at least four bytes before the end of the first buffer.

7.2.4.7 Address Match Codes

The address match codes returned by the TMS38021 indicate whether a frame is copied due to internal, external, or both checks. Information as to the type of address (specific, group, or functional) can be determined from the U/L, S/G, and G/F address bits stored in the frame buffer.

The following shows the Receive Status bits as presented by the TMS38021.

Table 7-2. Receive Status Bit Functions

RCV-STATUS 14	RCV-STATUS 15	MEANING
0	0	No address Match (Frame copied due to "Copy all frames")
0	1	Internally address matched
1	0	Externally matched
1	1	Internally and Externally matched

7.2.4.8 Receive Option Codes

The receive option bits (ROPT(0-1) of the RINGCMD1 register) have been modified to support the ECHO interface.

Table 7-3. Revised Receive Option Codes

ROPT 0	ROPT 1	MEANING
0	0	Normal frame recognition
0	1	Copy only express MAC frames
1	0	Line Monitor mode (externally matched frames are copied, but ARI/FCI are not set)
1	1	Copy all frames

7.2.4.9 No Buffer Operation

Under normal adapter operation there may be times when the TMS38021 has no buffer available for copying a frame, so data cannot be written to memory and its transfer monitored by the ECHO hardware. Therefore, data must be given directly to an external hardware so that the Address Recognized (ARI) bits of the frame can be correctly set.

The TMS38021 does this by writing frame data to address >0200 whenever there is no buffer available (whenever RCP = 0). Data will be written to >0200 until the external checker signals its results.

7.2.5 Other Hardware Differences Between the TMS38020 and TMS38021

7.2.5.1 BURST5 Log Error Interrupt

TMS38020 Implementation. The TMS38020 Protocol Handler does not set BURST5 error indication unless the BURST5 error occurs within a frame (after a valid SDEL received and before a valid EDEL is received).

TMS38021 Implementation. One BURST5 error will be logged outside a frame boundary. After posting of this interrupt, another BURST5 error will not be logged unless the adapter has received a valid DELIMITER. This change is made to improve problem isolation for weak signals where BURST5 errors are encountered during an SDEL or EDEL.

7.2.5.2 Frequency Acquisition Reset

TMS38020 Implementation. The elastic buffer overflow sets a latch that causes a change to Frequency Acquisition state (the assertion of FRAQ). This latch is reset by the transition of $\overline{\text{REDY}}$ from the ring interface chip (TMS38052). During software triggering of FRAQ signal (as would occur during the Beacon process), there may be a timing window which prevents the reset of the elastic buffer overflow latch by $\overline{\text{REDY}}$.

TMS38021 Implementation. Software enabling of the Frequency Acquisition state (asserting NFRAQ in RINGCMD1 register on TMS38021) will hold the elastic buffer latch reset.

7.2.6 Electrical Specifications

The electrical specifications for the TMS38021 are identical to the TMS38020 except for the specifications for pin 40 ($\overline{\text{XMATCH}}$) and pin 42 ($\overline{\text{XFAIL}}$). The specifications for these pins may be found in the TMS38021 Data Sheet in Appendix A.

7.3 Bridge Options Software

This section describes the Bridge Options software, which provides adapter functions useful for implementation of bridge and gateway products. This section serves as an extension to the attached system software interface description found in the *TMS380 Adapter Chipset User's Guide.* This software is designed for the TMS380 Token Ring Adapter and is supplied in EPROMs which reside on the LAN Adapter bus. All features included in the Bridge Options software are also found in the DLC Software.

Features include:

- Receive option extensions which allow the Adapter to copy all frames from the ring.
- Ability to pass CRC on both transmit frames from the host and receive frames to the host. This allows CRC to be maintained (not regenerated) when frames are passed through a bridge or gateway.
- Ability to transmit frames with a host-defined source address field. This allows frames to be passed through a bridge or gateway while maintaining the original source station address in the frame.
- Ability to transmit with access priority requests up to six. This allows specialized adapters in network management and bridging products to utilize priorities above the capability of stations utilizing the standard Adapter software (restricted to priority level three or less).
- Ability to transmit Medium Access Control (MAC) frames with unrestricted source classes (except Ring Station class >0). This allows specialized network management products to transmit formerly restricted MAC frames such as Ring Parameter Server (RPS) MAC frames.
- Ability to set any functional address (except Active Monitor). Formerly, the adapter software restricted the host from setting the Ring Parameter Server (RPS) functional address. Removal of this restriction allows stations implementing the RPS function to utilize the RPS functional address.
- The addition of the "Modify Open Options Command". This additional attached system command allows the bit-significant open options field of the open parameter list to be changed without first closing and re-opening the Adapter on the network. This allows the copy options (i.e., copy MAC frames, Pass Beacon MAC frames, etc.) to be changed dynamically.
- No parity operation. This adapter software version is supplied in two EPROMs. Parity protection of code may be provided if desired.
- When used with the TMS38021 Protocol Handler, the software allows both universally administered and locally administered station addresses to be assigned to the Adapter.

In addition to the enhancements listed above, the Lobe Media Test MAC frame has been shortened and the Beacon Transmit Autoremoval timer has been shortened to speed up both the autoremoval tests and the insertion process.

The Bridge Options software is supplied in two 8K × 8 EPROMs. Since this software is operated without parity, only two EPROMs are necessary. If parity is desired, then three EPROMs will be required. Two EPROMs are labeled MSB and LSB representing the most-significant byte and the least-significant byte, respectively.

To select parity operation of this software, the TEST1 pin (pin 47) of the TMS38010 Communications Processor must be tied to ground. A parity EPROM must be provided with odd parity per byte. The parity bit is presented on the LPL and LPH lines for least-significant and most-significant bytes respectively. Note that parity is required of all expansion RAM on the LAN Adapter Bus regardless of the parity option taken for the software EPROMs. If the TEST1 pin is left unconnected or tied high, then no parity is assumed.

7.4 Pass CRC Option

The pass CRC option is selected via bit 6 of the transmit and receive CSTAT request fields (see Table 7-4). During receive, if this bit is set to one, the CRC is passed to the host system as normal receive data. During transmit, if this bit is set to one, the Adapter assumes that the CRC to be transmitted with the frame is the last four bytes of the frame data. Note that in this case, the Adapter does not generate the CRC on transmit but uses the CRC passed with the frame data. If this bit is reset to zero, CRC is not passed during receive nor assumed to be present in host frame data on transmit.

Table 7-4. Transmit and Receive CSTAT Fields — Summary

BIT	CSTAT REQUEST		CSTAT COMPLETE	
	TRANSMIT	RECEIVE	TRANSMIT	RECEIVE
0	VALID	VALID	VALID	VALID
1	FRAME COMPLETE	FRAME COMPLETE	FRAME COMPLETE	FRAME COMPLETE
2	START OF FRAME	START OF FRAME	START OF FRAME	START OF FRAME
3	END OF FRAME	END OF FRAME	END OF FRAME	END OF FRAME
4	FRAME INTERRUPT	FRAME INTERRUPT	FRAME INTERRUPT	reset to zero
5	set to zero	INTERFRAME WAIT	TRANSMIT ERROR	reset to zero
6	PASS CRC	PASS CRC	PASS CRC	PASS CRC
7	PASS SOURCE ADDRESS	set to zero	PASS SOURCE ADDRESS	reset to zero
8	set to zero	set to zero	STRIP FS BIT 0	RECEIVE FS BIT1
9	set to zero	set to zero	STRIP FS BIT 1	RECEIVE FS BIT2
10	set to zero	set to zero	STRIP FS BIT 2	RECEIVE FS BIT3
11	set to zero	set to zero	STRIP FS BIT 3	RECEIVE FS BIT4
12	set to zero	set to zero	STRIP FS BIT 4	RECEIVE FS BIT5
13	set to zero	set to zero	STRIP FS BIT 5	RECEIVE FS BIT6
14	set to zero	set to zero	STRIP FS BIT 6	reserved
15	set to zero	set to zero	STRIP FS BIT 7	reserved

When passing CRC during transmit, the Adapter does not verify that correct CRC was passed; however, if bad CRC is transmitted on the ring, the normal procedures for detecting and isolating the bad CRC soft error will be used. It must be noted, however, that the Transmit Error Bit (bit 5 of the CSTAT complete field) will **not** be set if incorrect CRC is transmitted with the frame. The receiving station, however, would not copy the frame due to CRC error. Thus, the ARI and FCI bits should be checked to assure normal reception by the destination station.

During transmit, the FRAME LENGTH field on transmit must include the four bytes of CRC. During receive, the FRAME LENGTH field value will include the four bytes of CRC.

When received MAC frames are passed to the host, the CRC option behaves normally except for the Transmit Forward MAC frame in the case when the CRC bytes cross an internal buffer boundary. When this occurs, the Transmit Forward MAC frame will be passed without CRC regardless of the value of bit 6 in the CSTAT request.

When extended receive open option "Pass First Buffer Only" is selected (bit 15 of the Open Options field), the CRC will not be passed to the attached system unless the frame size is such that the entire frame fits within one internal buffer. See Section 7.11 for more information regarding the extended receive open options.

The transmit and receive CSTAT complete fields will leave bit 6 as set in the CSTAT request (see Table 7-4).

7.5 Transmit Source Address Option

When bit 7 of the transmit CSTAT request field is set to one (see Table 7-4), the source address field (six bytes) in the frame data passed to the Adapter will be used as the frame's address in lieu of the Adapter's specific address. When bit 7 is reset to zero, the Adapter will use the node address as specified during the OPEN command, or read from the Burned-in Address ROM, as the source address in the transmitted frame.

This option allows the adapter to transmit a frame with a source address other than its own specific address. This feature may be used with bridge or gateway products which require that the source address of the originating station be maintained across ring or segment boundaries.

Bit 7 of the transmit CSTAT complete field will be as set in the CSTAT request (see Table 7-4).

7.6 Allowed Transmit Priorities

Bridge Options software now provides a power-on default maximum allowed access priority of six. Level seven access priority may not be used unless specifically enabled through receipt of a Change Parameters MAC frame which enables this priority level.

Caution:

Care must be exercised when using priority level seven. The token ring architecture reserves priority level seven for use by the Active Monitor Present (AMP) MAC frame for the Neighbor Notification (Ring Poll) process. Indiscriminate use of priority level seven for non-MAC use could result in high soft error rates or a non-functioning network.

7.7 Added Functional Addresses

The Ring Parameter Server (RPS) functional address (Bit 1) may be set from the host during the OPEN command or the CHANGE FUNCTIONAL ADDRESS command. The functional address of the Active Monitor (bit 0) may be set only by the adapter that is the Active Monitor. Thus, this bit cannot be set by the attached system.

Caution:

Note that if the Ring Parameter Server functional address is set in an Adapter inserted on a ring, the Adapter will recognize and copy the Request Initialization MAC frame sent by all stations inserting into the network. This will result in the ARI/FCI bits of that frame being set. The inserting station will assume the RPS is present on the ring if these bits are set. Failure of the RPS to respond to the Request Initialization (via a Initialize Ring Station MAC frame) will cause the inserting station to deinsert with a Request Initialization error. Thus, stations setting the RPS functional address must be prepared to respond to initialization requests; otherwise, stations will be unable to insert onto the ring.

7.8 Added Transmit Source Classes

Bridge Options software allows source class five (Ring Parameter Server) to be used in MAC frames passed from the host for transmission. Attempting to pass source class zero (Ring Station) MAC frames from the attached system to the adapter for transmission is not allowed unless the transmission of class zero MAC frames is specifically enabled through receipt of a Change Parameters MAC frame.

Caution:

Care must be exercised when passing source class zero (ring station) MAC frames from the host for transmission. Transmit source class zero MAC frames are ordinarily used only by MAC protocols in the Adapter to manage the MAC sublayer. Indiscriminate transmission of ring station class MAC frames could result in unreliable operation of the network.

7.9 MODIFY.OPEN.PARAMETERS Command

The MODIFY.OPEN.PARAMETERS command is used to change the OPEN command bit-significant open options field (bytes 0 and 1 of the open parameter list) without requiring that the adapter be closed and reopened with the new options field. This allows changing the copy option bits without de-inserting from the ring. This command is discussed in Section 2.15.

7.10 Extended Receive Open Options

The Bridge Options software incorporates the copy-all-frames function as described in the DLC software, Section 2.9.

The Extended Receive Open Options are provided as a tool to designers, allowing easier debug of network communications protocols than is provided with the standard Adapter software. Specifically, these extensions allow the Adapter to copy and pass to the attached system as receive data:

1. All frames which occur on the ring. This includes both Medium Access Control (MAC) as well as non-MAC (Logical Link Control) frames.
2. All frames which are MAC frames.
3. All frames which are non-MAC frames.

In addition, this software provides a "first buffer only" option which passes to the attached system only the first internal buffer of each frame copied by the Adapter. Included in the last 16-bits of data transferred to the attached system is the actual size of the frame as received by the Adapter. Thus, performance or traffic monitoring functions within the attached system can be implemented without the need to pass the entire frame.

These additional functions are selectable through previously reserved bits in the options field (first 16-bit word) of the OPEN command parameter list.

> **Note:**
>
> Occasionally when the adapter is opened with the copy-all-frames bits set, the OPEN command will fail due to ring poll failure during the insertion process. This can occur when inserting into a ring with heavy traffic, which causes extensive receive activity within the adapter during insertion process operations. If this open failure should occur, reset the adapter and try again. This can be avoided by opening the adapter without the copy-all-frames bits set and using the MODIFY.OPEN.PARAMETERS command (see Section 2.15) to set the desired copy options after the adapter has inserted into the ring.

7.11 Miscellaneous Differences

The following are changes to the information contained in the *TMS380 Adapter Chipset User's Guide* when Bridge Options software or the DLC software is used.

7.11.1 Lobe Media Test

The lobe media test performed during insertion and the autoremoval tests has been modified as follows:

1. The Lobe Media Test MAC frame has been shortened to 1048 bytes versus the 1500 bytes of Adapter software RC011B.
2. The Lobe Media Test MAC frame will be transmitted on the lobe 511 times versus the 2048 times of Adapter software RC011B.

7.11.2 Beacon Transmit Autoremoval Timer

The Beacon Transmit Autoremoval Timer has been shortened to 16 seconds from the 26 seconds of Adapter software RC011B. This significantly speeds up the beacon autoremoval process.

7.12 Software/Hardware-Based Source Routing Bridge

The TMS38021 Protocol Handler's External Copy Hardware Interface allows users to define additional frame copy criteria beyond the destination address recognition capability of the TMS38020. As shown in Figure 7-13, the signals $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ on the TMS38021 that comprises the ECHO interface notify External Copy Hardware (ECH) that a frame circulating on the ring is being temporarily stored in adapter memory. The ECH that resides on the adapter bus examines the incoming frame to determine if the frame should be copied.

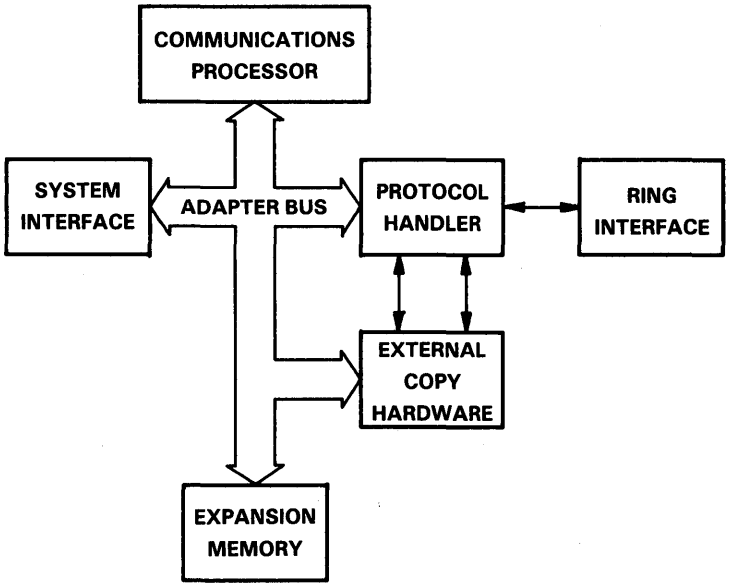


Figure 7-13. TMS380 and ECH Block Diagram

7.12.1 Design Methodology

In this example, the criteria for copying the frame is the value of the Routing Information Indicator (RII) bit. If this bit is equal to a one, the frame contains a routing information field and is copied by the adapter. If the value of this bit is equal to zero, then the frame does not contain a routing information field and therefore should not be copied. The ECH notifies the Protocol Handler (PH) of its copy decision by driving either $\overline{\text{XMATCH}}$ or $\overline{\text{XFAIL}}$ low.

The RII bit is the first bit of the source address field of the frame which corresponds to the fifth word of the frame after the start delimiter. Since frames are stored sequentially in adapter memory, the LAN adapter address of the fifth word of the frame can be calculated from the address of the first word of the frame. Also, since the first word of the frame is always stored in adapter memory starting on a 6-byte address boundary, the value of A13-A14 for the first word of the frame will always be b'11. Taking both of these factors into account, the LAN adapter bus address of the fifth word (source address) can be determined as shown in Table 7-6.

Table 7-5. Address Compare

LAN ADAPTER ADDRESS			FRAME WORD	FRAME CONTENTS
A12	A13	A14		
X	1	1	1st	AC/FC
$\overline{\text{X}}$	0	0	2nd	DEST ADDRESS
$\overline{\text{X}}$	0	1	3rd	DEST ADDRESS
$\overline{\text{X}}$	1	0	4th	DEST ADDRESS
$\overline{\text{X}}$	1	1	5th	SOURCE ADDRESS

By taking advantage of this address compare table, the algorithm to determine the address of the fifth word is as follows:

$$\text{5th word address} = (\overline{\text{A12 of first word}}) \times \text{A13} \times \text{A14}$$

Therefore, when $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ are driven low by the PH, signifying that the address of the first word of the frame is being driven on the adapter bus, the ECH stores the value of A12 in a register. The ECH now examines each address on the adapter bus until the necessary combination of A12, A13, and A14 is seen. When this occurs, the address of the fifth word of the frame is on the adapter bus. The ECH will then examine bit 0 of the source address field (5th data word) to determine if the RII bit is set. Depending on this value, either $\overline{\text{XMATCH}}$ or $\overline{\text{XFAIL}}$ will be driven low by the ECH indicating to the PH its copy decision.

7.12.2 Hardware

Because the criteria for copying the frame are relatively simple, the ECH can be implemented in a 24-pin Programmable Array Logic (PAL20RA10). The PAL pin assignments are shown in Figure 7-14. The PAL equations for the ECH are shown in Table 7-7.

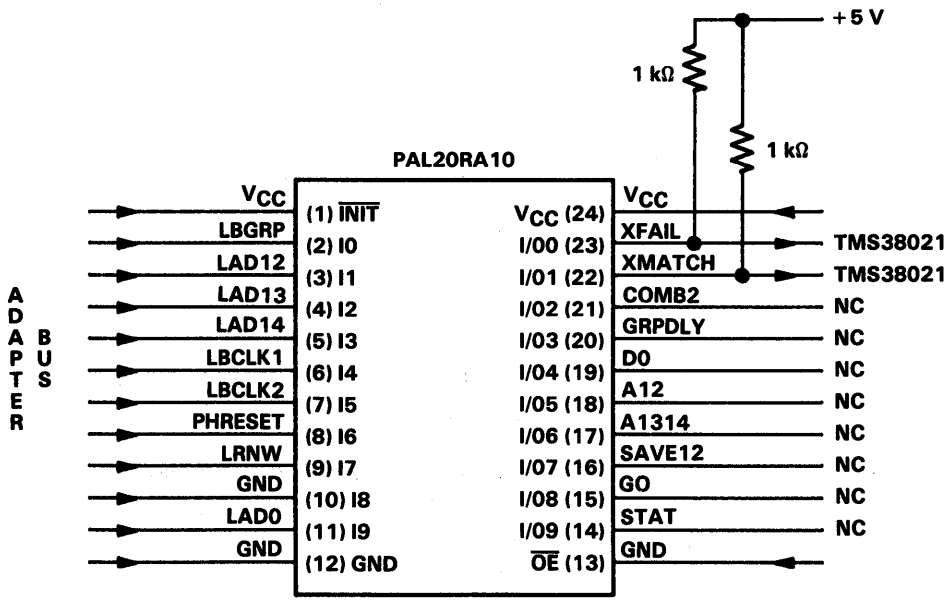


Figure 7-14. ECH PAL Implementation

Table 7-7. ECH PAL Equations

```
PIN ASSIGNMENTS
---------------
VCC,LBGRP,LAD12,LAD13,LAD14,                PIN 1,2,3,4,5;
LBCLK1,LBCLK2,PHRESET,LRNW,GND,             PIN 6,7,8,9,10;
LAD0,GND,STAT,GO,SAVE12,                    PIN 11,13,14,15,16;
A1314,A12,D0,GRPDLY                         PIN 17,18,19,20;
COMB2,XMATCH,XFAIL                          PIN 21,22,23;

PAL EQUATIONS
-------------

STAT            =  GND;
STAT RESET      =  !XMATCH & !XFAIL & LBCLK1 & !LBCLK2 & A1314;
STAT PRESET     =  !PHRESET;
STAT CLOCK      =  !GO;
STAT OE         =  VCC;

GO              =  !COMB2;
GO RESET        =  GND;
GO PRESET       =  !PHRESET;
GO CLOCK        =  !LBCLK2;
GO OE           =  VCC;

SAVE12          =  A12;
SAVE12 RESET    =  GND;
SAVE12 PRESET   =  GND;
SAVE12 CLOCK    =  XMATCH & XFAIL;
SAVE12 OE       =  VCC;

A1314           =  LAD13 & LAD14;
A1314 RESET     =  GND;
A1314 PRESET    =  GND;
A1314 CLOCK     =  LBCLK1 & !LRNW & !GRPDLY;
A1314 OE        =  VCC;

A12             =  LAD12;
A12 RESET       =  GND;
A12 PRESET      =  GND;
A12 CLOCK       =  LBCLK1 & !LRNW & !GRPDLY;
A12 OE          =  VCC;

D0              =  LAD0;
D0 RESET        =  GND;
D0 PRESET       =  GND;
D0 CLOCK        =  !LBCLK1;
D0 OE           =  VCC;

GRPDLY          =  LBGRP;
GRPDLY RESET    =  !PHRESET;
GRPDLY PRESET   =  GND;
GRPDLY CLOCK    =  !LBCLK1;
GRPDLY OE       =  VCC;

COMB2           =  (SAVE12 & A12) # (!SAVE12 & !A12)
                   # !A1314 # GRPDLY # !STAT;
COMB2 RESET     =  VCC;
COMB2 PRESET    =  VCC;
COMB2 CLOCK     =  VCC;
COMB2 OE        =  VCC;

XFAIL           =  D0;
XFAIL RESET     =  VCC;
XFAIL PRESET    =  VCC;
XFAIL CLOCK     =  VCC;
XFAIL OE        =  GO & LBCLK2;

XMATCH          =  !D0;
XMATCH RESET    =  VCC;
XMATCH PRESET   =  VCC;
XMATCH CLOCK    =  VCC;
XMATCH OE       =  GO & LBCLK2;
```

Referring to the timing diagrams in Figure 7-15, $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ are driven low by the PH, signifying the address of the first word. At this time the value of of A12 is saved into the register SAVE12. At the same time STAT is driven high signifying that the frame is being received. After this has occurred, the ECH will compare each address driven onto the LAN adapter bus for the inverse of the SAVE12 and for A13 and A14 to be equal to one. When this occurs, $\overline{\text{COMB2}}$ is driven low signifying that the next word driven onto

the bus is the 5th word of the received frame (the source address of the frame). The ECH then drives either $\overline{\text{XMATCH}}$ or $\overline{\text{XFAIL}}$ low depending on the value of the most significant bit in the source address (D0 = RRI bit).

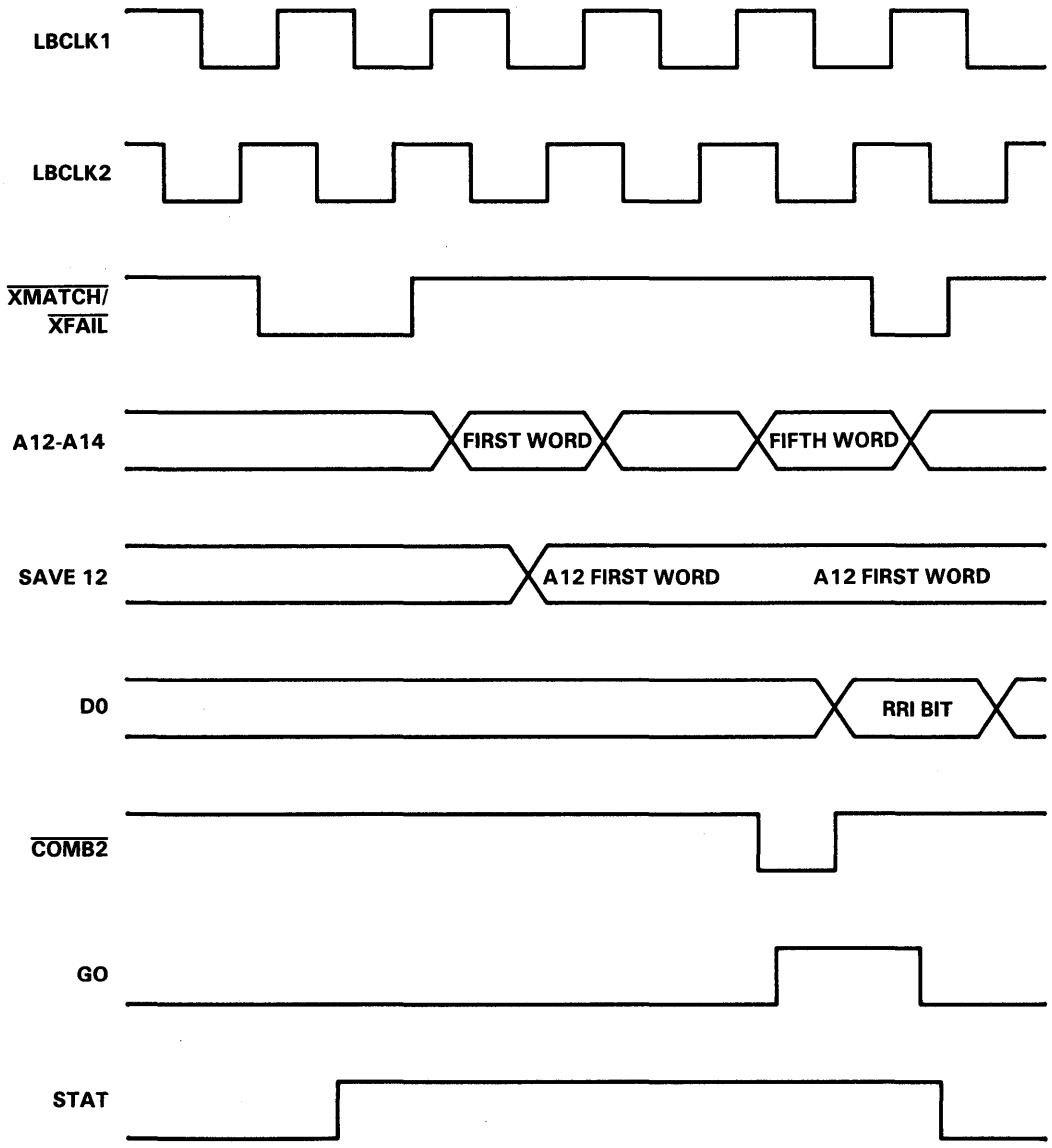


Figure 7-15. ECH Timing Diagrams

If the RRI bit is equal to a zero, $\overline{\text{XFAIL}}$ is driven low by the ECH, notifying the PH that the frame is not a source routed frame. If the PH internal address compare based on the destination address field of the frame does not match, the adapter will halt the copy operation and restore the buffer space.

If the PH internal address compare matches the destination address field of the frame, the adapter will continue to copy the frame regardless of the ECH's copy decision since the frame was destined for the station itself.

If the RRI bit is equal to a one, $\overline{\text{XMATCH}}$ will be driven low by the ECH signifying to the PH that the frame should be copied. The PH will therefore continue to copy the frame regardless of its own internal address compare. After the frame has been copied into adapter memory, the adapter will transfer the frame into host memory and notify the host that the frame has been received.

7.12.3 Software

The Host must initialize each node adapter shown in Figure 7-6 with bridge parameters such as bridge number, ring number for each station, and whether the station is a single route broadcast bridge. Each station is then inserted onto the ring, using the OPEN command, followed by a RECEIVE command. At this point the Host is ready to receive frames from each adapter and form transmit queues for each adapter.

The Host is notified after the frame has been copied by the adapter and transferred into Host memory. The Host can then examine the frame receive status bits in the CSTAT field (see Section 7.4) to determine if:

1. The frame was copied due to internal address match only. In this case the frame destination address matched the station's specific, group or functional address and the frame should be acted on by normal station processing.
2. The frame was copied due to external address match only. In this case, the Host can assume the RRI was set and begin evaluating the Routing Control Field. If the frame is a bridge broadcast frame, then the Routing Information Field is modified and the frame transmitted with regenerated CRC, if appropriate. If the frame is non-broadcast frame, the Routing Information Field is searched for the bridge number and partner segment number in the correct order. If a match occurs, the Host must forward the frame to the partner adapter and pass through the CRC.
3. The frame was copied due to external and internal address match. In this case, items 1 and 2 in this list would both be executed.

7.13 Hardware-Based Source Routing Bridge Example

This example describes, at the block diagram level, a hardware solution for implementing a source routing bridge using the TMS380 and TTL/PALS or ASIC technology. As with the example shown in Section 7.13, this design utilizes the External Copy Hardware (ECH) interface of the TMS38021 Protocol Handler. However, in this approach, the ECH offers the complete solution, and host software will be a minimum. The ECH will not only check to see if the frame is destined for a station on another ring by examining the RII bit in the source address, but will also scan the Routing Information Field to determine if the frame should be forwarded across that particular bridge. Figure 7-16 below illustrates the high-level block diagram of the source routing ECH.

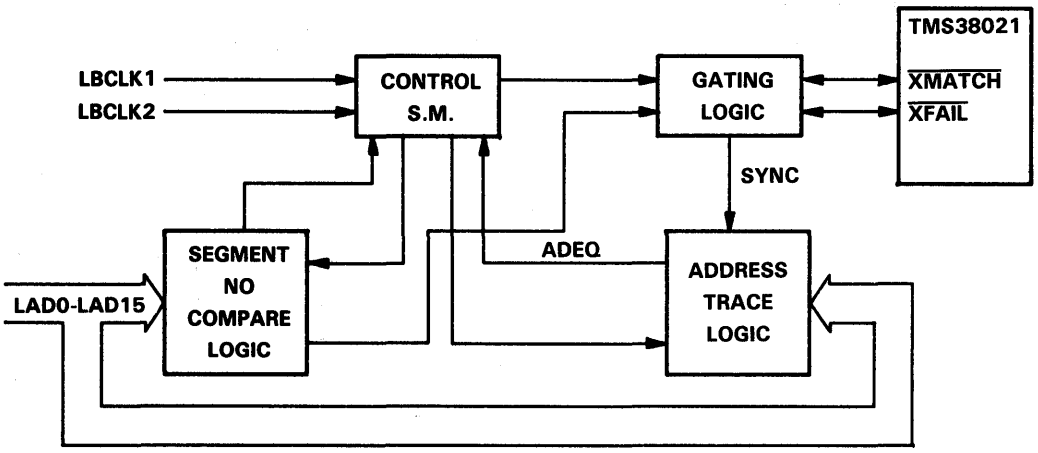


Figure 7-16. Source Routing ECH Block Diagram

The address trace logic will "trace" the adapter bus addresses for TMS38021 receive DMA operations to sequential locations, starting with the address that was on the bus when $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ were both driven low by the TMS38021 (signal SYNC). Whenever the Address Trace Logic senses that the next sequential address is being written, ADEQ will be active.

The segment number compare logic will, at the appropriate time as specified by the control state machine, compare receive DMA data to a Primary Segment Number Register (PSNR) and a Secondary Segment Number Register (SSNR). The sequence of comparison depends upon the state of the Direction (D) bit of the routing control field, as well as the Broadcast bits. If the frame is non-broadcast and the appropriate sequence is found within the segment number list, a corresponding match indication will be presented to the TMS38021. If the frame is broadcast and the appropriate segment number pair does not appear in the segment number list, a match indication will be presented to the TMS38021. The control state machine provides the control and sequencing functions for the Source Routing ECH. This state machine is timed using clocks defined by LBCLK1 and LBCLK2.

7.13.1 Address Trace Logic

Figure 7-17 below illustrates the Address Trace Logic.

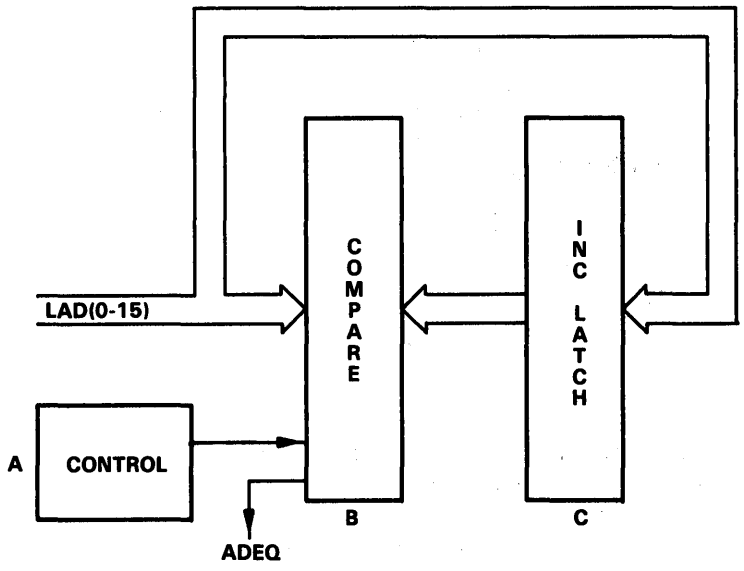


Figure 7-17. Address Trace Logic

C is an incrementer-latch used to trace receive DMA cycles. It is initially loaded with the address of the AC/FC word and then incremented to identify the addresses of succeeding data words. The increment function is disabled on a write to >0200.

B is an equality comparator that compares the contents of the incrementor latch and the LAD bus during the bus address phase.

Control logic A coordinates the operation of B and C. C is caused to load on $\overline{ALE} \cdot \overline{XMATCH} \cdot \overline{XFAIL}$, and is incremented after this load, or whenever the comparator has detected an address match. ADEQ the address match signal from the comparator is passed on to the control state machine and the segment number compare state machine.

7.13.2 Segment Number Compare Logic

The segment number compare logic is shown in Figure 7-18:

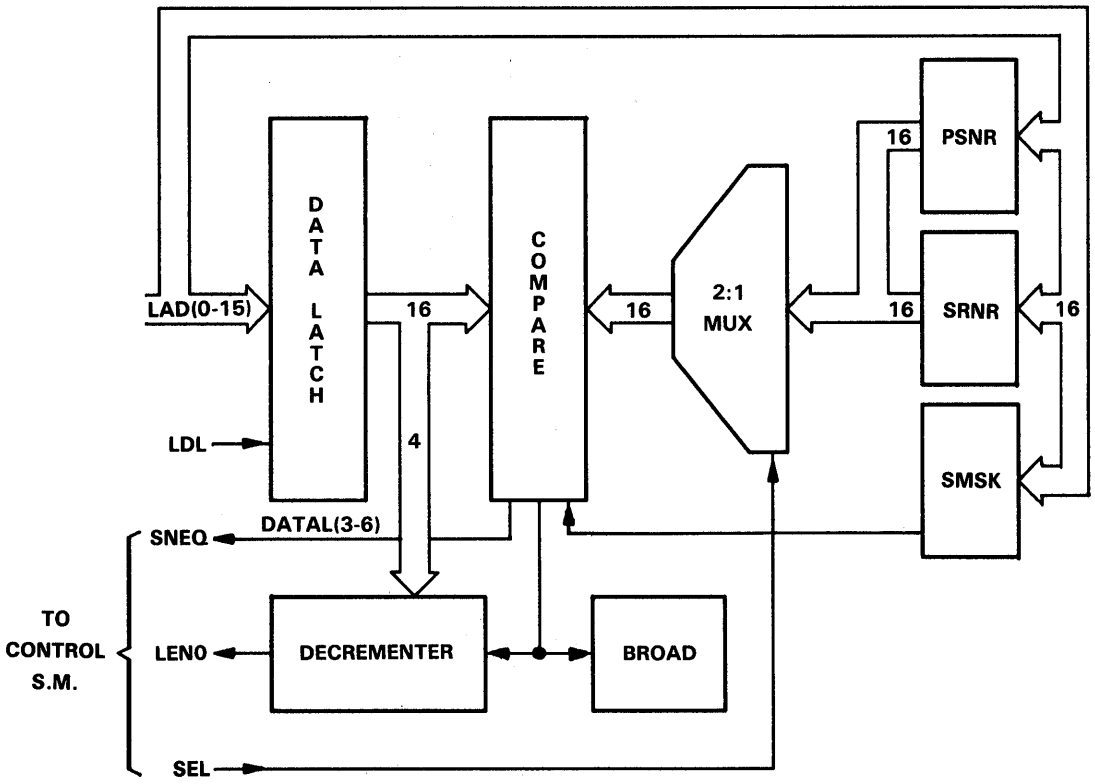


Figure 7-18. Segment Number Compare Logic

The Data Latch is used to capture frame data from the LAD bus. Its latched output is called DATAL(0-15). The Primary Segment Number (PSNR), Secondary Ring Number (SRNR), and Secondary Mask Register (SMSK) are registers readable and writable from the LAN Adapter bus. The PSNR register is loaded with the segment number to which the TMS38021 is attached, and the SRNR register is loaded with the ring number to which another adapter of the host is attached. The SMSK register provides a bit pattern used to mask the bridge number portion of the 16-bit data latch when comparing to the SRNR contents. The PSNR or the SRNR contents will be compared, at the appropriate time, to the contents of the Data Latch. The PSNR or the SRNR contents are chosen for comparison via a 2:1 multiplexer controlled from the state machine. A match (equals) condition is generated and sent to the control state machine.

The Broadcast Indicator (BROAD), loaded by the Control State Machine, determines if a segment number match is desired. If the broadcast bits are such that the frame is a broadcast frame, a segment number match is not desired; however, if the bits are such that the frame is not a broadcast, a segment number match is required in order for the frame to be copied.

The four bit decrementer, loaded from the Routing Control Field by the Control State Machine, contains the length of the routing information field. It decrements every ADEQ. When the contents of the decrementer reach zero, indicating the end of the routing information field, the Control State Machine will indicate to the TMS38021 its copy decision based on whether a segment match occurred.

7.13.3 Required Host Software

As a result of the ECH making all copy decisions on circulating frames, the host software needed to transfer frames between the two adapters is minimum. The only decision the host software needs to make is to determine if the frame is a broadcast frame. If so, the Primary and Secondary segment numbers of the bridge must be added to the segment number field of the routing information field prior to the frame being forwarded to the second adapter. Figure 7-19 shows a flowchart of the required host software function.

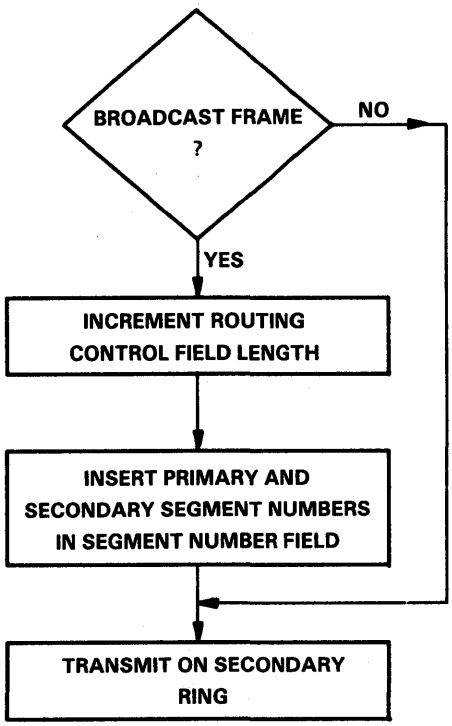


Figure 7-19. Bridge Host Software Flowchart

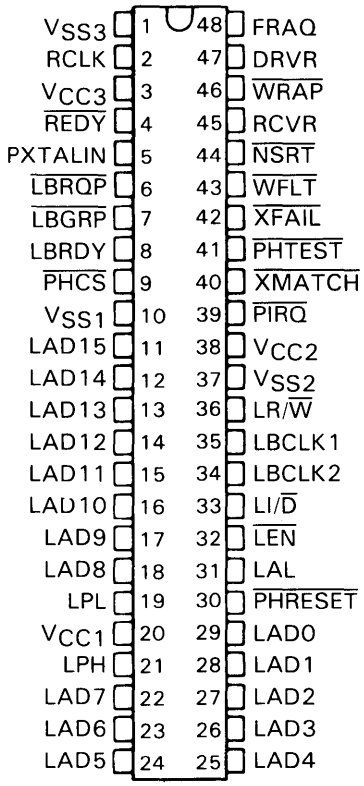
A. TMS38021 Protocol Handler Data Sheet and Errata to TMS380 Adapter Chipset User's Guide

TMS38021 PROTOCOL HANDLER

NOVEMBER 1986

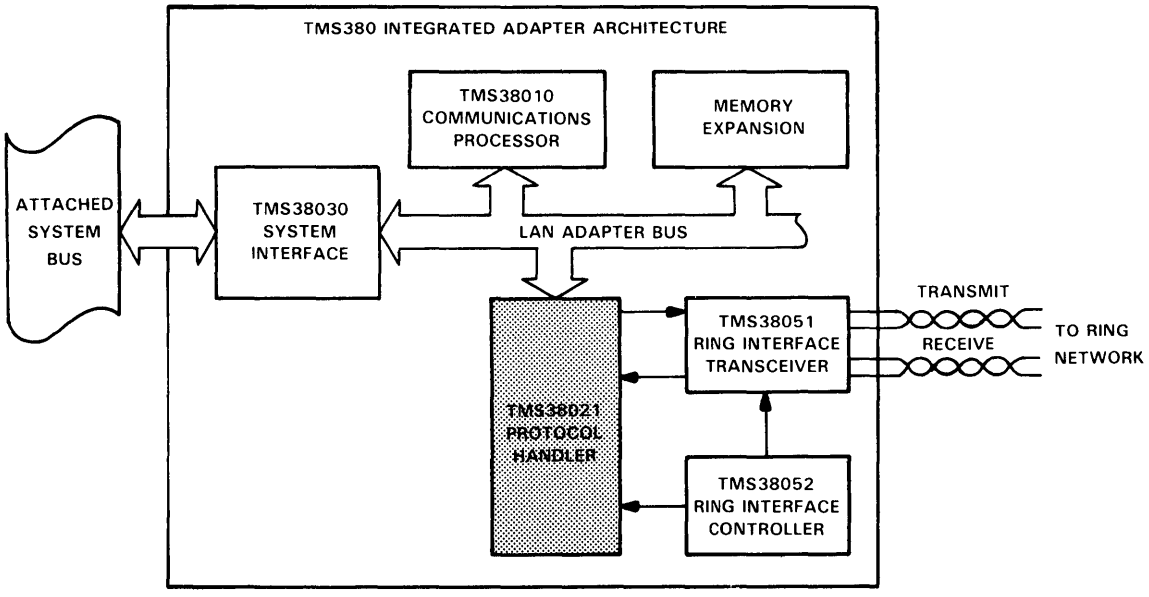
- Compatible with IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications
  - Differential Manchester Code Conversion on 4M-Bit per Second Serial Data Stream
  - Address Recognition (Functional, Group and Specific)
  - Manchester Code Violation Detection
  - Starting and Ending Delimiter Generation and Detection
  - CRC Generation and Checking
  - High-Speed Frame Repeat Path Minimizes Ring Latency (2-Bit Times)
  - Token Transmit and Priority Control
  - Monitor Functions
- Separate Pairs of DMA Channels for Receive and Transmit
- Supports Both Universal and Local Ring Addressing
- Automatic Frame Buffer Management
- External Hardware Interface for User-Defined External Checker Logic
- On-Chip 16K-Byte ROM for Adapter Software
  - 8K x 18-Bit ROM with Byte Parity Protection
  - Single Word Prefetch
- Plug Compatible with the TMS38020

JD PACKAGE
(TOP VIEW)



- Test Pin for Hi-Z, Module-in-Place Testing
- 48-Pin, 600-Mil, Ceramic Dual-in-Line Packaging
- Low-Power Scaled-NMOS Technology

token ring LAN application diagram



TEXAS INSTRUMENTS
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pin descriptions

NAME	I/O	DESCRIPTION
		LAN ADAPTER BUS INTERFACE PINS
LBCLK1, LBCLK2	I	Bus Clocks
$\overline{\text{LAL}}$	I/O	Address Latch Enable
$\overline{\text{LEN}}$	I/O	Data Enable
LBRDY	I/O	Bus Ready
$\overline{\text{PIRQ}}$	O	PH Interrupt Request
$\overline{\text{LBRQP}}$	O	Bus Request
$\overline{\text{LBGRP}}$	I	Bus Grant
LAD0-LAD15	I/O	Address/Data bus. LAD0 is the most-significant bit, LAD15 is the least-significant bit.
LPH, LPL	I/O	Parity High/Parity Low
LI/$\overline{\text{D}}$	I/O	Instruction/Data Bus Status Code
LR/$\overline{\text{W}}$	I/O	Read/Not Write
$\overline{\text{PHRESET}}$	I	Reset
$\overline{\text{PHCS}}$	I	Chip Select
		RING INTERFACE PINS
DRVR	O	Transmitter Data
FRAQ	O	Frequency Acquisition Select
$\overline{\text{NSRT}}$	O	Insert Control
RCLK	I	Recovered Data Clock
RCVR	I	Received Data
$\overline{\text{REDY}}$	I	Ring Interface Ready
$\overline{\text{WFLT}}$	I	Wire Fault Detect
$\overline{\text{WRAP}}$	O	Wrap Select
PXTALIN	I	Ring Frequency Reference Clock
		MISCELLANEOUS PINS
$\overline{\text{PHTEST}}$	I	Module-in-Place Test Mode Select. This pin should be left unconnected.
V_{CC}		5-V supply pins.
V_{SS}		Ground pins.
$\overline{\text{XMATCH}}$	I/O	External frame match select.
$\overline{\text{XFAIL}}$	I/O	External frame fail select.

TEXAS INSTRUMENTS
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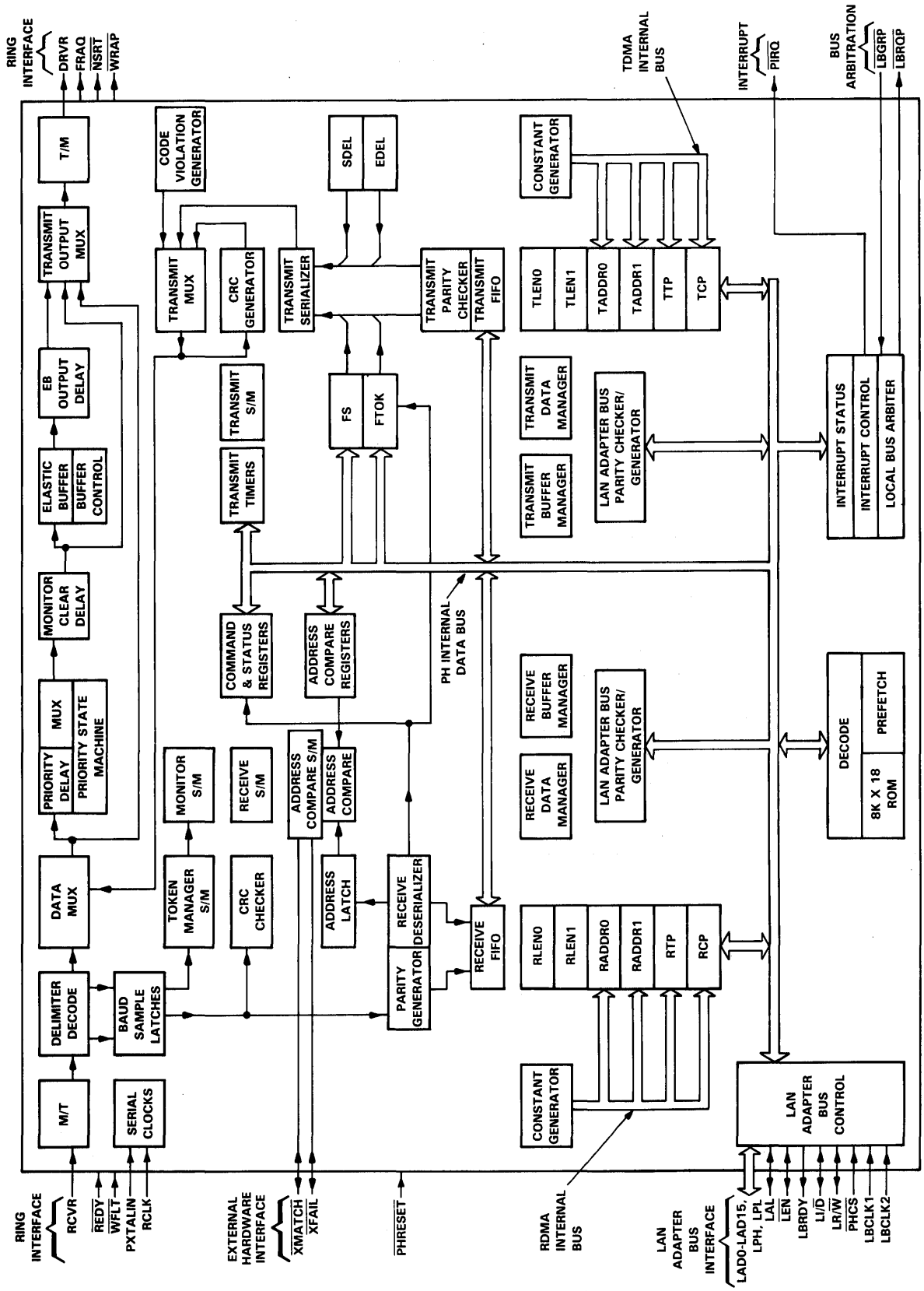
functional block diagram



description

The TMS38021 Protocol Handler integrates onto a single chip the hardware-based protocol functions for a 4 megabit per second token ring Local Area Network (LAN). An on-chip ROM contains 16K bytes of software used by the TMS38010 Communications Processor for implementation of a complete token ring Adapter function. The TMS38021 provides Differential Manchester encoding and decoding, frame address recognition, and includes state machine functions which capture free tokens, transmit and receive frames, manage the Adapter RAM buffers and provide token transmit and priority controls. Four DMA channels, two for transmit and two for receive, insure high-speed transfer of frames between the Adapter's buffer RAM and the ring. Integrity of transmitted and received data is provided by CRC generation and checking, detection of Differential Manchester code violations, and parity on internal data paths and at the LAN Adapter bus interface.

The TMS38021 is pin-compatible with the TMS38020. The TMS38021 defines two pins which were not used on the TMS38020, the $\overline{\text{XMATCH}}$ (pin 40) and $\overline{\text{XFAIL}}$ (pin 42) pins. These pins allow user-defined external hardware to be implemented which can provide a frame copy/frame not copy decision on all receive frames in parallel with the normal address compare capabilities of the TMS38021. Using these pins, the designer can implement extensions to the normal address recognition capability of the TMS38021 for such applications as source routing bridges.

The TMS38021 also differs from the TMS38020 in that both universal and local ring station specific addresses are supported. Thus, bit 1 of byte 0 of the specific address register high (SAH) may be set to either a one or a zero.

The TMS38021, when coupled with the TMS38010 Communications Processor, the TMS38030 System Interface, and the TMS38051 and TMS38052 Ring Interface chips, forms a highly integrated token ring LAN Adapter.

architecture

The TMS38021 Protocol Handler contains a bus master interface to the LAN Adapter bus for transfer of frame data between itself and LAN Adapter bus memory, a bus slave interface to the LAN Adapter bus for control by an external CPU, an interface to the Ring Interface circuit, and a 16K-byte ROM. Internal to the TMS38021 are several finite-state machine-implemented functions which provide bit-and frame-level processing of token protocols as well as control the flow of DMA data to and from buffer RAM resident on the LAN Adapter bus. The following paragraphs describe the blocks shown in the functional block diagram.

address compare state machine

The address compare state machine controls the recognition of addresses in a received frame (including stripped frames). In addition to normal frame address recognition capabilities, the TMS38021 provides an External Copy Hardware Option (ECHO) interface which provides a medium for the TMS38021 to signal to external hardware the presence of receive data on the LAN Adapter bus, and for external hardware to signal the results of its data check, selecting to copy or not to copy the frame. The External Copy Hardware Option (ECHO) interface is implemented via two pins on the TMS38021: the $\overline{\text{XMATCH}}$ pin and the $\overline{\text{XFAIL}}$ pin. The electrical and switching characteristics of these pins are described in the electrical specifications. A description of the ECHO Interface may be found below. A description of frame addressing methodology may be found in the Communications Services section of the User's Guide.

external copy hardware option (ECHO)

The external copy hardware interface consists of the $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ pins and makes use of the recoverable buffering technique used by the TMS38021. The TMS38021 writes a frame to memory while it is checking the address of the frame, and then recovers the buffer if the frame is not to be copied. Thus, the frame data is available to external hardware on the LAN Adapter bus for capture and examination.

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In order to let the external hardware know which bus cycles carry data, the TMS38021 indicates the first data transfer of a frame. Following cycles are "traced" in the manner described below. The "pass," "fail," and "first-data" signals share the same two TMS38021 pins.

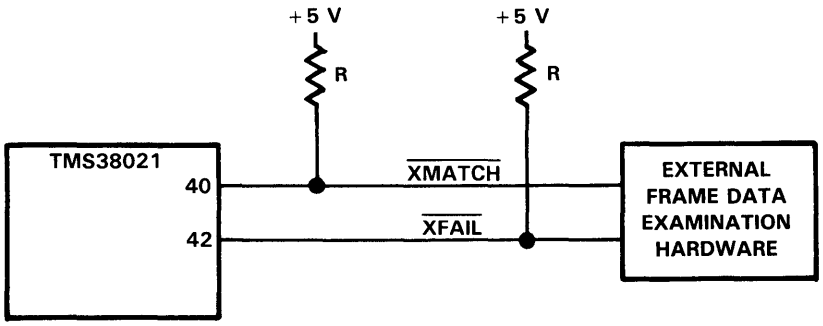
The first data transfer of a frame (AC/FC bytes) is indicated to the external logic by both the $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$ pins being driven low by the TMS38021 (see Table 1). The external hardware must latch the address of this transfer so that succeeding receive DMA cycles may be traced. Data is stored sequentially into memory, so incrementing this latched address gives the address of the next data write. By comparing this new address to the address/data bus, the transfer of the next word of the frame can be recognized. The latch is incremented again, and the process continues until completion of the external check.

Until both the internal address check and some indication from the external hardware is received, the TMS38021 does not know whether to accept or reject the frame. It cannot assume that the external hardware timing is the same as its own. So the TMS38021 must buffer data until explicitly signalled that the external check has been completed. This is indicated by either the $\overline{\text{XMATCH}}$ or $\overline{\text{XFAIL}}$ pin being driven low by external hardware to indicate that the frame should be copied or not be copied respectively. The TMS38021 will not chain past the first buffer it is given. Therefore, the external hardware must give some indication at least four bytes before the end of the first buffer.

TABLE 1. $\overline{\text{XMATCH}}$,$\overline{\text{XFAIL}}$ PIN FUNCTIONS

$\overline{\text{XMATCH}}$	$\overline{\text{XFAIL}}$	FUNCTION
Hi	Hi	Default state of the interface
Lo	Lo	Asserted by TMS38021 to indicate start of frame and that the AC/FC word of the frame will be transferred on this bus cycle.
Lo	Hi	Asserted by the external hardware to indicate it has completed its frame check and that the frame should be copied.
Hi	Lo	Asserted by the external hardware to indicate it has completed its frame check and the check failed.

Figure 1 illustrates the TMS38021 connection to external hardware. The interface consists of two wire-AND signal lines $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$. External pullups are required as these signals are only driven low.



NOTE: Recommended value for R is 2.3 kΩ.

FIGURE 1. EXTERNAL COPY HARDWARE INTERFACE

As the buffer recovery decision is delayed until both the internal address checker and the external hardware check are complete, the external hardware must finish its check in time to allow the buffer to be recovered. Therefore, the result of an external check should be posted by the time of the transfer of the frame word which is two words before the end of the frame.

The TMS38021 has internal pulldowns on $\overline{\text{XMATCH}}$ and $\overline{\text{XFAIL}}$. However, the $\overline{\text{XFAIL}}$ indication takes precedence over the $\overline{\text{XMATCH}}$ indication. Thus, if no external hardware is present, the TMS38021 will copy frames based only upon its internal address compare. This allows the TMS38021 to plug into existing TMS38020 sockets.

Externally matched frames will not be copied when the ROPT bits of the RINGCMD1 register are set to "COPY ONLY EXPRESS BUFFERS". The ARI bits will be set however if a external match is indicated.

Under normal adapter operation there may be times when the TMS38021 has no buffer available for copying a frame, so data cannot be written to memory, and its transfer monitored by the external hardware. Therefore, data must be given directly to the external hardware so that the Address Recognized bits (ARI) of the frame can be correctly set.

The TMS38021 does this by writing frame data to address >0200 on the LAN Adapter bus whenever there is no buffer available. Data will be written to >0200 until the external hardware checker signals its results.

CRC checker

This block contains a 32-bit feedback shift register for calculation of the cyclic redundancy code of frames received. The TMS38021 calculates the CRC for each frame that the TMS38021 receives. If the calculated CRC does not agree with the CRC value of the received frame, the TMS38021 sets an error indicator bit within the frame to flag the occurrence of the error. If the TMS38021 was copying the frame at the time the CRC error was detected (due to an address match), the TMS38021 notifies the LAN Adapter CPU of the error. Mathematically, the CRC is calculated by considering the checked bytes as a polynomial and dividing it modulo 2 by the following polynomial:

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

CRC generator

The cyclic redundancy code (CRC) generator generates the CRC field to be inserted by the TMS38021 when transmitting. The procedure for generating CRC is identical to that described for the CRC checker.

data multiplexer

The data multiplexer selects the source of the data to be transmitted. The source may be received ring data (repeat mode), a constant of zeros (idles), or data to be transmitted by the TMS38021.

delimiter decode

This block detects the Start Delimiter (SDEL) and End Delimiter (EDEL) sequences defined for the protocol.

elastic buffer

The elastic buffer absorbs the accumulated phase jitter in the ring. During normal operation, only one station (the Active Monitor) inserts its elastic buffer on the ring. As the accumulated phase delay around the ring varies, it is "absorbed" by the elastic buffer. The elastic buffer can absorb ± 3 bits of accumulated jitter.

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The total delay through the elastic buffer is 3 ± 3 bits. When the elastic buffer is not inserted on the ring, it permits the TMS38021 to detect when the incoming data frequency falls outside acceptable bounds by detecting overrun and underrun conditions.

The overrun and underrun conditions are defined to occur within a specific number of bit times. To minimize the possibility of overrun and underrun over longer periods of time, the PH re-initializes the elastic buffer every 512 bit times when in standby monitor mode and whenever the PH detects a token when in active monitor mode.

fire token register (FTOK)

The fire token register is used to hold the access control (AC) field that will be used in transmitting a token on the ring.

interrupt status logic

The interrupt status logic contains a register with information concerning TMS38021 interrupts. This logic provides interrupt vectoring, masking, and prioritization.

LAN Adapter bus parity checker

The LAN Adapter bus parity checker checks all data placed on the internal TMS38021 data bus from the LAN Adapter bus. This includes data written to the TMS38021 by an external bus master, data read by the TMS38021 receive or transmit buffer manager, and data read by the TMS38021 transmit DMA unit for transmission on the ring.

LAN Adapter bus parity generator

The parity generator generates the parity to be placed on the LAN Adapter bus when any TMS38021 register is read by an external bus master. However, received data which has parity generated by the serial parity generator has no parity generated by the bus parity generator.

manchester-to-transitional decoder (M/T)

This functional block converts the Differential Manchester code received from th ring into an internal format called "transitional" code. Transitional code is so named because baud† are encoded based upon their transition from the previous baud. The receive data sampled on pin RCVR is sampled by the recovered data clock input on pin RCLK.

monitor delay

The token ring protocol calls for a ring function called an Active Monitor. Each ring will have one Active Monitor which is chosen during a contention process. One function of an Active Monitor is to introduce enough delay in a ring to provide a minimum length ring sufficient to circulate a free token. When the TMS38021 is configured as an Active Monitor [the CXMT bit of the Ring Command 1 (RINGCMD1) register is set], it inserts additional monitor delay to meet the effective ring length requirement. The monitor delay consists of a 7.5-baud (half-bit times) delay preceding the elastic buffer and a 22.5-baud delay succeeding it. The total delay through the TMS38021 when the Active Monitor mode is selected is 4-baud normal delay plus 19-baud for the priority delay plus 30-baud for the monitor delay plus 6-baud average elastic buffer delay. This delay totals 59 ± 6 baud.

monitor state machine

The monitor state machine controls the setting of the Monitor Count bit of busy or priority tokens which are repeated on the ring and the detection of token activity on the ring. This state machine is active when the TMS38021 is configured as an Active Monitor [MON bit of Ring Command 1 Register (RINGCMD1) is set].

†Two baud equals one bit of Differential Manchester encoding.

priority delay and state machine

The TMS38021 provides control of seven levels of token priority. The priority state machine is responsible for controlling the token priority as defined by the protocol. The priority delay of 19 half-bit times is inserted when a station releases a token to allow the station to modify the token according to the priority protocol.

receive buffer manager

The receive buffer manager controls the receive buffer chaining operations on the LAN Adapter bus.

receive data manager

The receive data manager requests and acknowledges LAN Adapter bus cycles for DMA to write the received frame into memory on the LAN Adapter bus.

receive deserializer

The receive deserializer block is a 16-bit serial-in parallel-out shift register. The input is the sampled data from the ring. A serial parity generator unit calculates the parity for each eight bits shifted in and stores this parity with the parallel data. The 18 bits of data and parity are then loaded in parallel into the receive FIFO buffer.

receive DMA registers

The receive DMA registers are indicated in the functional block diagram by the names RCP, RTP, RADDR0, RADDR1, RLEN0, and RLEN1. These registers are managed by the receive buffer manager. Only the register RCP (receive chain pointer) may be accessed by external LAN Adapter bus masters. The remaining registers are not accessible by external bus masters. A brief description of these registers follows.

receive chain pointer (RCP)

This register contains the address of the buffer currently being filled with data from the ring.

receive temporary pointer (RTP)

The receive temporary pointer register contains the starting address of the buffer into which the receive DMA channel will store data when the buffer being used is full.

channel address registers (RADDR0, RADDR1)

The TMS38021 maintains two DMA channels for receive operations. The channel address register for both receive DMA channels contains the LAN Adapter bus address of the word being accessed by that channel.

channel length registers (RLEN0, RLEN1)

The channel length register for each of the two receive DMA channels contains the number of empty bytes left in the buffer currently being filled by that channel.

receive FIFO

The receive first-in, first-out (FIFO) buffer stores up to two words (16 bits) of deserialized data before it is transferred via DMA onto the LAN Adapter bus. Data is transferred onto the LAN Adapter bus under control of the receive data manager block.

serial receive state machine

This state machine controls operation of the receiver portion of the serial data path.

serial transmit state machine

This state machine controls the operation of the serial transmit data path.

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transitional-to-manchester decoder (T/M)

This functional block converts the internal transitional code representation of transmit data to Differential Manchester code.

transmit buffer manager

The transmit buffer manager performs the automatic buffer changing of transmit buffers contained in LAN Adapter bus memory.

transmit data manager

The transmit data manager requests and acknowledges LAN Adapter bus cycles for DMA to read data to be transmitted on the ring.

transmit DMA registers

The transmit DMA registers (TCP, TTP, TADDR0, TADDR1, TLEN0, and TLEN1) are managed by the transmit buffer manager. Of these, only the transmit chain pointer (TCP) may be loaded by external LAN Adapter bus masters. The remaining registers are not accessible by external bus masters. The transmit DMA registers are described briefly below.

transmit chain pointer (TCP)

The transmit chain pointer contains the address of the buffer currently being read for transmit data.

transmit temporary pointer (TTP)

The transmit temporary pointer register contains the starting address of the buffer from which transmit data will be read by the DMA channel when the present buffer had been read.

channel address registers (TADDR0, TADDR1)

The TMS38021 maintains two DMA channels for transmit operations. The channel address register for both transmit DMA channels contains the LAN Adapter bus address of the word being read by that channel.

channel length registers (TLEN0, TLEN1)

The channel length register for each of the two transmit DMA channels contains the number of bytes yet to be transmitted from the current buffer.

transmit FIFO

The transmit FIFO buffers two 16-bit words, allowing the TMS38021 to maintain a constant flow of transmitted data into the transmit serializer. The parity from the LAN Adapter bus is maintained within the FIFO.

transmit multiplexer

The transmit multiplexer selects either the CRC generator or transmit serializer output onto the transmit data path.

transmit parity checker

The transmit parity checker checks the parity of data transferred from the top of the transmit FIFO to the transmit serializer. It performs the final check of data before it is placed in the serializer.

transmit serializer

The transmit serializer is a 16-bit parallel-in, serial-out shift register. The shift register is loaded from the data at the top of the transmit FIFO, from the concatenation of the Start Delimiter (SDEL) and the fire token register (FTOK) or from a concatenation of the End Delimiter (EDEL) and the frame status (FS) register.

transmit timer

The TMS38021 contains a physical trailer timer (PTT). This timer provides a watchdog timer function for halting the frame strip process after transmitting a frame.

command and status registers

The command and status registers of the TMS38021 are registers which may be read/written through memory-mapped I/O by an external bus master on the LAN Adapter bus. These registers are mapped to LAN Adapter bus addresses as shown in Figure 2.

ADDRESS	BITS		DESCRIPTION
	0 7	8 15	
>0100	RINGCMD0		RING COMMAND 0
>0102	RINGCMD1		RING COMMAND 1
>0104	RINGSTS		RING STATUS
>0106	INTSTAT		INTERRUPT STATUS
>0108	00†	PTTLATCH	PHYSICAL TRAILER TIMER LATCH
>010A	RCP		RECEIVE CHAIN POINTER
>010C	TCP		TRANSMIT CHAIN POINTER
>010E	FTOK	00‡	FIRE TOKEN

†Most-significant bits are reserved.
‡Least-significant bits are reserved.

FIGURE 2. TMS38021 COMMAND AND STATUS REGISTERS

ring command 0 (RINGCMD0)

The RINGCMD0 register enables specific receive and transmit modes of the TMS38021 including idle insertion between frames and stripping of transmitted data from the ring. The bits of RINGCMD0 are defined in Table 2.

TABLE 2. RING COMMAND 0 (RINGCMD0) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	XMTIMM	Transmit Imediate Mode
1	BDM	Baud Data Mode
2	NOSTRIP	No Strip Mode
3	XMTCRC	Transmit CRC
4	RNFT	Release No Free Token
5	XMTIDLE	Transmit Idles Mode
6	ETO	Enable Transmitter Output
7	PTEST	Parity Test
8	GAP0	Interframe Gap Bit 0
9	GAP1	Interframe Gap Bit 1
10	GAP2	Interframe Gap Bit 2
11		Reserved. This bit must be zero.
12		Reserved. This bit must be zero.
13		Reserved. This bit must be zero.
14		Reserved. This bit must be zero.
15	NOCHAIN	No Receive Chaining

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ring command 1 (RINGCMD1)

The RINGCMD1 register is the master control register of the TMS38021. This register controls such functions as reset, clock sourcing, ring insertion, and address recognition. The bits of RINGCMD1 are defined in Table 3. The functions of receive options, ROPT0 and ROPT1, are presented in Table 4.

TABLE 3. RING COMMAND 1 (RINGCMD1) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	NRESET	Not Reset
1	NFRAQ	Not Frequency Acquisition
2	INSERT	Insert Into Ring
3	NWRAP	Not Internal Wrap
4	CXMT	Crystal Transmit Mode Select
5	MON	Active Monitor Mode Select
6		Reserved. This bit must be set to zero.
7		Reserved. This bit must be set to one.
8		Reserved. This bit must be set to zero.
9	IGN0	Ignore Control 0
10	IGN1	Ignore Control 1
11	IGN2	Ignore Control 2
12	IGN3	Ignore Control 3
13	ROPT0	Receive Option 0
14	ROPT1	Receive Option 1
15		Reserved.

TABLE 4. RECEIVE OPTION BIT DECODE

ROPT0	ROPT1	DESCRIPTION
0	0	Normal frame recognition
0	1	Copy only express buffer MAC frames.
1	1	Line Monitor Mode. (Externally matched frames are copied, but ARI/FCI are not set.)
1	0	Copy all frames

ring status register (RINGSTS)

The RINGSTS register provides general ring status information, including ring interface status, error logging, and token validation. The bits of RINGSTS are defined in Table 5.

TABLE 5. RING STATUS (RINGSTS) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	NGO	Not Go (Signal Loss)
1	GTDET	Good Token Detect
2	ATDET	Any Token Detect
3	WFAULT	Wire Fault
4	EBOUF	Elastic Buffer Over/Under Flow
5-9		Reserved
10	MAC0	MAC Attention Code Bit 0
11	MAC1	MAC Attention Code Bit 1
12	MAC2	MAC Attention Code Bit 2
13	MAC3	MAC Attention Code Bit 3
14	RIDER0	FS Rider Control Bit 0
15	RIDER1	FS Rider Control Bit 2

interrupt status (INSTAT)

The INSTAT register contains information concerning TMS38021 interrupts. This register provides interrupt vectoring, masking, and prioritization. The bits of INSTAT are defined in Table 6. Table 7 lists the decode for bits 11 through 14 (INTCODE0 through INTCODE3).

TABLE 6. INTERRUPT STATUS (INTSTAT) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	MIE	Master Interrupt Enable
1		Reserved
2	EORBE	End of Receive Buffer Interrupt Enable
3	EOTBE	End of Transmit Buffer Interrupt Enable
4	SLIE	Signal Loss Interrupt Enable
5-7		Reserved
8	ID0	Interrupt Source ID Bit 0
9	ID1	Interrupt Source ID Bit 1
10	ID2	Interrupt Source ID Bit 2
11	INTCODE0	Interrupt Code Bit 0
12	INTCODE1	Interrupt Code Bit 1
13	INTCODE2	Interrupt Code Bit 2
14	INTCODE3	Interrupt Code Bit 3
15	"0"	Always zero

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TABLE 7. INTERRUPT CODE 0 (INTCODE0) THROUGH INTERRUPT CODE 3 (INTCODE3) DECODE

INTCODE0	INTCODE1	INTCODE2	INTCODE3	DEFINITION
0	0	0	0	Reserved
0	0	0	1	LAN Adapter Bus Parity Error
0	0	1	0	Token Error
0	0	1	1	Signal Loss
0	1	0	0	BURST5 Error in Frame
0	1	0	1	Log Error
0	1	1	0	No Buffer Available
0	1	1	1	Attention
1	0	0	0	Reserved
1	0	0	1	Receive Frame Error
1	0	1	0	Transmit Frame Error
1	0	1	1	Receive End of Buffer
1	1	0	0	Transmit End of Buffer
1	1	0	1	Receive End of Frame
1	1	1	0	Transmit End of Frame
1	1	1	1	No Interrupt Pending

physical trailer timer latch (PTTLATCH)

The PTTLATCH register is an 8-bit control register containing a ring-speed-specific time constant. This value is the starting value of a timer which is started following the transmission of a frame so that a lost frame condition may be detected.

receive chain pointer (RCP)

The RCP register contains the starting address of the buffer into which the receive DMA channel, if active, stores receive data.

transmit chain pointer (TCP)

The TCP register contains the starting address of the buffer into which the transmit DMA channel, if active, reads data for transmission.

fire free token register (FTOK)

The FTOK register is used to hold the Access Control Field (AC) to be included in a token that will be generated by the TMS38021 and transmitted on the ring. Writing to the FTOK register causes a token to be released.

address compare registers

The TMS38021 contains 15 registers for use in comparing frame addresses. These registers are shown with their corresponding LAN Adapter bus addresses in Figure 3.

ADDRESS	NAME	DESCRIPTION
>0110	SAH	SPECIFIC ADDRESS BITS 0-15
>0112	SAM	SPECIFIC ADDRESS BITS 16-31
>0114	SAL	SPECIFIC ADDRESS BITS 32-47
>0116		RESERVED. ALWAYS READ AS ZERO
>0118	STRIPHI	STRIP ADDRESS BITS 16-31
>011A	STRIPLO	STRIP ADDRESS BITS 32-47
>011C	GNAM1	GROUP ADDRESS BITS 16-31
>011E	GNAL	GROUP ADDRESS BITS 32-47
>0120	GNAH	GROUP ADDRESS BITS 0-15
>0122	>0000	RESERVED
>0124	>0000	RESERVED
>0126	>0000	RESERVED
>0128	>0000	RESERVED
>012A	>0000	RESERVED
>012C	FNAHI	FUNCTIONAL ADDRESS BITS 0-15
>012E	FNALO	FUNCTIONAL ADDRESS BITS 16-31

FIGURE 3. ADDRESS COMPARE REGISTERS

buffer management

The TMS38021's buffer managers move frame data in and out of buffer RAM, located on the LAN Adpater bus, through one or more singly-linked buffers. These buffers are aligned on 8-byte boundaries and have the organization for transmit and receive as shown in Figure 4.

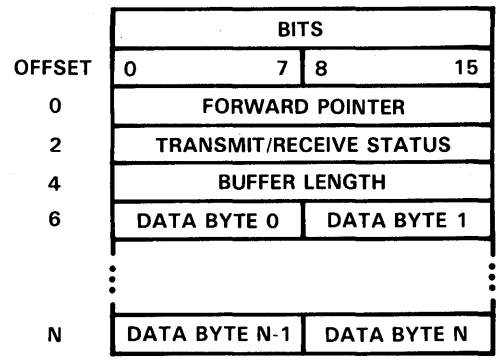

FIGURE 4. BUFFER ORGANIZATION

The forward pointer contains the address of the next buffer in a chain. The transmit/receive status field is used to report frame status. The length field contains the number of bytes in the data field of the buffer. This field is initialized by the LAN Adapter bus CPU.

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transmit buffers

When the buffer organization shown in Figure 4 is used for transmit frames, the status field has the bit functions shown in Table 8 in the last buffer in a chain used to transmit the frame.

TABLE 8. TRANSMIT STATUS FIELD BIT FUNCTIONS

BIT	NAME	FUNCTION
0	INUSE	In Use Indicator
1	LFED	Local Frame Error Detect
2	RTEDI	Returned Error Detected Indicator
3	TCC0	Transmit Completion Code Bit 0
4	TCC1	Transmit Completion Code Bit 1
5	TCC2	Transmit Completion Code Bit 2
6	TCC3	Transmit Completion Code Bit 3
7	EOF	End Of Frame Indicator
8	FS0	Stripped Frame Status Bit 0 (ARI)
9	FS1	Stripped Frame Status Bit 1 (FCI)
10	FS2	Stripped Frame Status Bit 2
11	FS3	Stripped Frame Status Bit 3
12	FS4	Stripped Frame Status Bit 4 (ARI)
13	FS5	Stripped Frame Status Bit 5 (FCI)
14		Reserved. This bit is zero.
15		Reserved. This bit is zero.

The decode function of the transmit completion code bits (TCC) is presented in Table 9.

TABLE 9. TRANSMIT COMPLETION CODE (TCC) BIT DECODE

PARALLEL LAN ADAPTER BUS PATH

TCC0	TCC1	DESCRIPTION
0	0	Normal
0	1	Parity Error
1	0	DMA Underrun
1	1	Next Buffer Unavailable

SERIAL RING DATA PATH

TCC2	TCC3	DESCRIPTION
0	0	Normal Completion
0	1	PTT Timeout
1	0	Invalid Free Token
1	1	Invalid Abort on Strip

For frames to be transmitted on the ring, the data portion of a transmit buffer has the format shown in Figure 5.

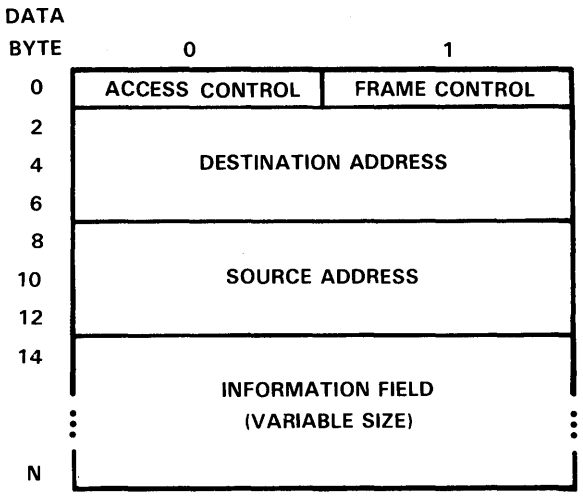

FIGURE 5. TRANSMIT DATA FORMAT

receive buffers

When the buffer organization shown in Figure 4 is used for receive frames, the status field has the bit functions shown in Table 10 in the last buffer in a chain used to receive the frame.

TABLE 10. RECEIVE STATUS FIELD BIT FUNCTIONS

BIT	NAME	FUNCTION
0	INUSE	In Use
1	LFED	Local Frame Error Detect
2	REDI	Receive Error Detect Indicator
3	RCC0	Receive Completion Code Bit 0
4	RCC1	Receive Completion Code Bit 1
5	RCC2	Receive Completion Code Bit 2
6	RCC3	Receive Complation Code Bit 3
7	EOF	End of Frame Indicator
8	FS0	Receive Frame Status Bit 0
9	FS1	Receive Frame Status Bit 1
10	FS2	Receive Frame Status Bit 2
11	FS3	Receive Frame Status Bit 3
12	FS4	Receive Frame Status Bit 4
13	FS5	Receive Frame Status Bit 5
14		Reserved
15		Reserved

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The decoded function of the receive completion code bits (RCC) is presented in Table 11.

TABLE 11. RECEIVE COMPLETION CODE (RCC) BIT DECODE

PARALLEL LAN ADAPTER BUS PATH

RCC0	RCC1	DESCRIPTION
0	0	Normal Completion
0	1	Parity Error
1	0	DMA Overrun
1	1	Next Buffer Unavailable

SERIAL RING DATA PATH

RCC2	RCC3	DESCRIPTION
0	0	Normal Completion
0	1	Error: FCI not set
1	0	Implicit Abort
1	1	Explicit Abort

For frames received from the ring, the data portion of a receive buffer has the format shown in Figure 6.

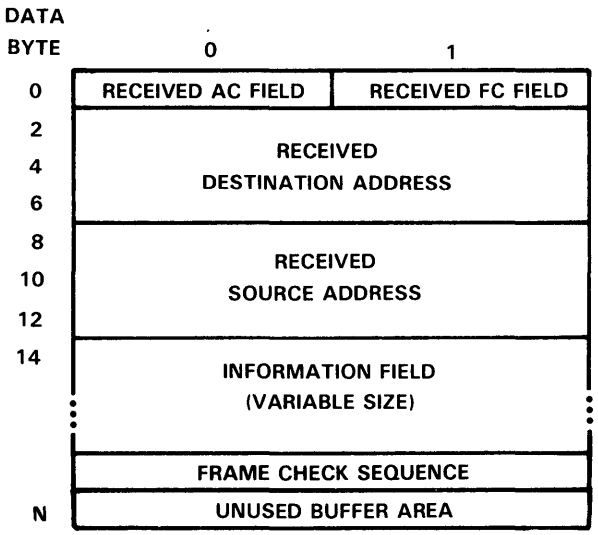

FIGURE 6. RECEIVE DATA FORMAT

TMS38021 ROM

The TMS38021 contains a 16K-byte ROM organized as 8K x 18 bits. Each byte contains an odd parity bit. The ROM is not used by internal TMS38021 logic but is accessed by the LAN Adapter bus CPU for program storage. This ROM contains object code for the TMS38010 Communications Processor. This ROM contains software which provides media access protocols compatible with IEEE Std 802.5-1985, protocol services for network management servers, and diagnostics which verify proper functionality of the TMS380 Token Ring Adapter.

Access to this ROM from the TMS38010 Communications Processor is in one or two LAN Adapter bus read cycles. A prefetch unit reads the word sequentially following the last word read so that sequential accesses occur with no wait states forced on the TMS38010. When access is nonsequential, the TMS38021 deasserts LBRDY in the first cycle to force the CPU to accept a wait state. On the second cycle, the TMS38021 asserts LBRDY and places the ROM data on the bus.

When the TMS38021 is a bus slave, it will also respond if external circuitry deasserts LBRDY; it will continuously drive its output data (on reads) or delay modifying its internal register (on writes) until LBRDY is asserted high.

address decoding

The TMS38021 performs decoding of LAN Adapter bus addresses as shown in Table 13. Note that not all addresses are strictly decoded. For example, the TMS38021 does not decode address line A1 for ROM accesses at >C000. Thus, a memory read at address location >8000 is identical to an address read at location >C000. For this reason, expansion RAM on the LAN Adapter bus should negate $\overline{\text{PHCS}}$ whenever expansion RAM overlays memory addresses >8000 through >BFFF.

TABLE 13. TMS38021 ADDRESS DECODING

$\overline{\text{PHCS}}$	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	SELECTED TMS38021 LOCATION
H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TMS38021 not selected
L	L	L	L	L	L	L	L	L	X	X	X	X	X	X	X	TMS38021 not selected
L	L	L	L	L	L	L	L	H	X	X	L	L	Int'l Decode			Command/Status Registers
L	L	L	L	L	L	L	L	H	X	X	L	H	Int'l Decode			Address Compare Registers
L	L	L	L	L	L	L	L	H	X	X	H	L	Int'l Decode			Compare Address Registers
L	L	L	L	L	L	L	L	H	X	X	H	H	Int'l Decode			Internal Test Registers
L	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	TMS38021 not selected
L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	TMS38021 not selected
L	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	TMS38021 not selected
L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	TMS38021 not selected
L	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	TMS38021 not selected
L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	TMS38021 not selected
L	H	X	◄					Internal Decode							►	TMS38021 ROM

test mode

The TMS38021 features a module-in-place test mode for board-level testing with the TMS38021 in-circuit. This facilitates testing by bed-of-nails testers. This test mode is enabled by tying the $\overline{\text{PHTEST}}$ pin (pin 41) to ground. This has the effect of driving all outputs of the TMS38021 to a high-impedance state. When not used for testing purposes, this pin should be left unconnected. An internal pullup drives this pin high when not externally connected.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range (see Note 2) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to V_{SS}.
2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 80°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage (Note 3)			0		V
V_{IH}	High-level input voltage	LBCLK1, LBCLK2	3.8			V
		RCVR, RCLK	2.6			V
		$\overline{\text{PHTEST}}$	V_{CC}			V
		All other inputs	2			V
V_{IL}	Low-level input voltage	LBCLK1, LBCLK2, RCVR, RCLK			0.6	V
		$\overline{\text{PHTEST}}$			V_{SS}	V
		All other inputs			0.8	V
I_{OH}	High-level output current	All outputs			0.15	mA
I_{OL}	Low-level output current	DRVR			−1.2	mA
		LBRDY			−2.4	mA
		All other outputs			−1.7	mA
C_L	Load capacitance	DRVR			30	pF
		All other outputs			100	pF
T_A	Operating free-air temperature (Note 2)		0		70	°C

NOTES: 2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 80°C.
3. Care should be taken by PC board designers to provide a minimum inductance path between the V_{SS} pins and system ground in order to minimize V_{SS} noise.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.5 V, I_{OH} = 0.15 mA	2.4			V
V_{OL}	Low-level output voltage	All outputs	V_{CC} = 4.5 V, I_{OL} = Max			0.45	V
I_{OH}	High-level output current	All outputs	V_{CC} = 4.5 V, V_{OH} = 2.4 V			0.15	mA
I_{OL}	Low-level output current	DRVR	V_{CC} = 4.5 V, V_{OL} = 0.45 V			−1.2	mA
		LBRDY				−2.4	mA
		All other outputs				−1.7	mA
I_{OZL}	Off-state (high-impedance state) output current with low-level voltage applied, outputs and I/O's only		V_O = 0.45 V			−50	μA
I_{OZH}	Off-state (high-impedance state) output current with high-level voltage applied, outputs and I/O's only		V_O = 2.4 V			50	μA
I_{IL}	Low-level input current	$\overline{\text{PHTEST}}$ (Note 4)	V_I = V_{SS}, V_{CC} at 4.75 V – 5.25 V			−700	μA
		All other inputs				−20	μA
I_{IH}	High-level input current	All other inputs except $\overline{\text{PHTEST}}$ (Note 5)	V_{CC} at 4.5 V – 5.5 V			20	μA
I_{CC}	Supply current		V_{CC} = 5 V, T_A = 25°C		110		μA
			V_{CC} = 5.5 V, T_A = 0°C			175	μA
			V_{CC} = 5.5 V, T_C = 80°C			125	μA
C_I	Input capacitance	LBCLK1, LBCLK2	f = 1 MHz, all other inputs at 0 V			20	pF
		RCVR, RCLK				10	pF
		All other inputs				15	pF

NOTES: 4. $\overline{\text{PHTEST}}$ has an internal pullup resistor implemented. It may be left unconnected; in this case it is interpreted as high.
5. I_{IH} for $\overline{\text{PHTEST}}$ is not specified because it will never be driven.

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LAN ADAPTER BUS CLOCK PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range (see Figure 7)

		MIN	MAX	UNIT
$t_{c(LA)}$	LAN Adapter bus cycle time (Note 6)	333	333.7	ns
t_{d1}	Delay time, LBCLK2 low to LBCLK2 no longer low in next cycle	4Q − 2	4Q + 2	
t_{d2}	Delay time, LBCLK2 rise to LBCLK2 high in next cycle		4Q + 9	
t_{d3}	Delay time, LBCLK2 no longer low to LBCLK1 no longer low	Q − 3	Q + 3	
t_{d4}	Delay time, LBCLK2 rise to LBCLK1 high		Q + 9	
t_{d5}	Delay time, LBCLK2 no longer low to LBCLK2 no longer high	2Q − 2	2Q + 7	
t_{d6}	Delay time, LBCLK2 rise to LBCLK2 low		2Q + 12	
t_{d7}	Delay time, LBCLK2 no longer low to LBCLK1 no longer high	3Q − 15	3Q − 1	
t_{d8}	Delay time, LBCLK2 rise to LBCLK1 low		3Q	
t_{d9}	Delay time, LBCLK1 low to LBCLK2 high	Q		
t_{d10}	Delay time, LBCLK2 high to LBCLK1 high	Q − 4		
t_{d11}	Delay time, LBCLK1 high to LBCLK2 low	Q − 4		
t_{d12}	Delay time, LBCLK2 low to LBCLK1 low	Q − 16		

NOTES: 6. The LAN Adapter bus cycle time is 333.3 ns ± 0.1%. This value shall be used for calculations requiring the time between successive rising edges of LBCLK2.

7. $Q = 0.25\ t_{c(LA)}$.

LAN ADAPTER BUS READ AND WRITE PARAMETERS

timing requirements/switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 7)†

		MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q – 50		
t_{d17}	Delay time, address valid to LAL no longer high	Q – 50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q + 74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q + 84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q + 47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q + 47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q – 12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q – 70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q – 4		
t_{su1}	Setup time, read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q – 41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q – 21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master (DMA). The values given are valid for both modes.

NOTE 7: Q = $0.25t_c$(LA).

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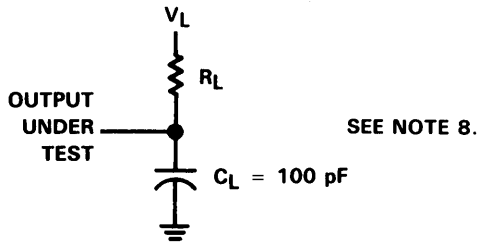
PARAMETER MEASUREMENT INFORMATION

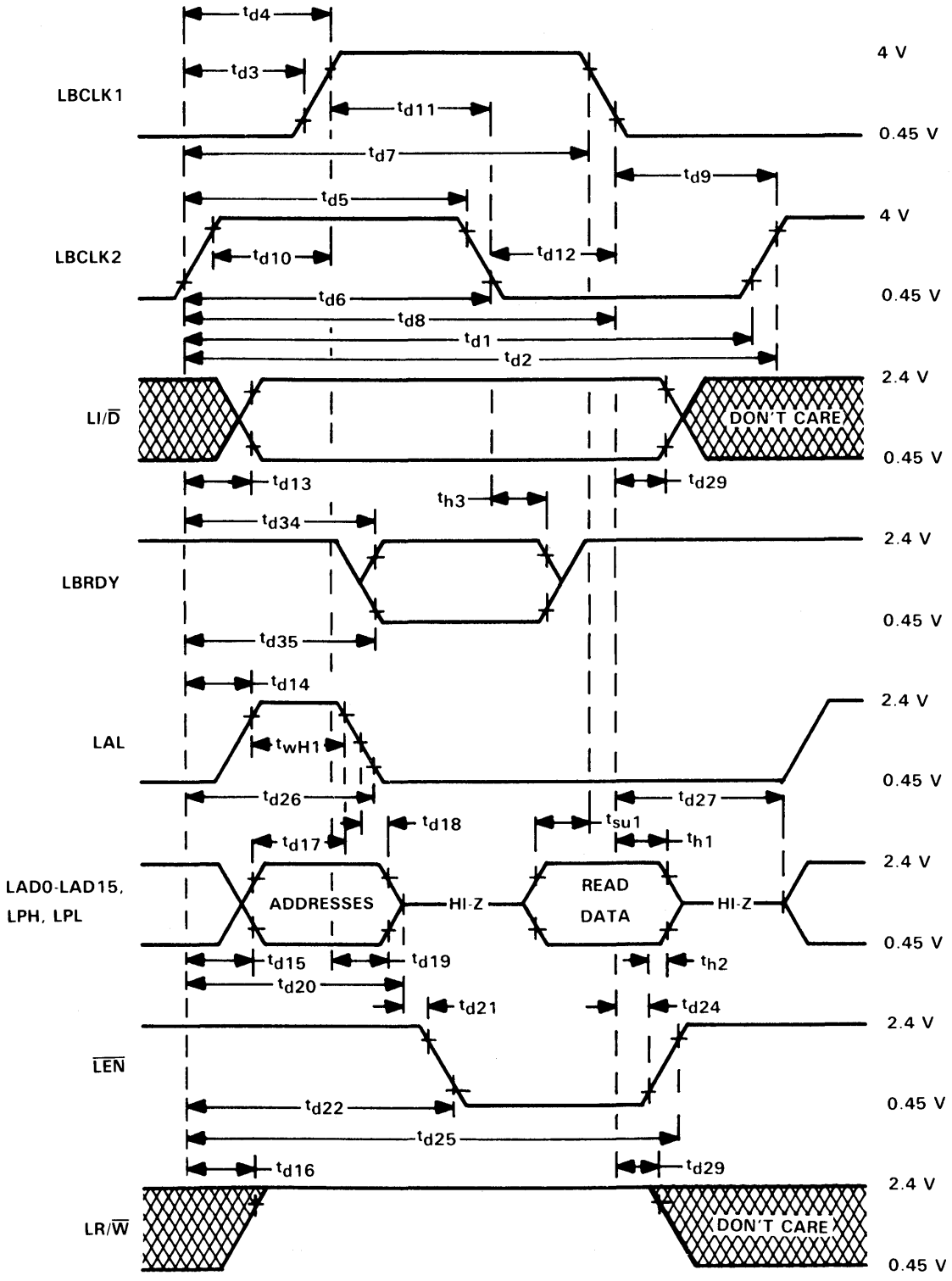


NOTE 8: R_L and V_L are chosen as follows:

$$R_L = \frac{V_{OH} - V_{OL}}{|I_{OL} - I_{OH}|} \quad V_L = V_{OH} - (I_{OH})(R_L)$$

FIGURE 7. LOAD CIRCUIT

LAN Adapter bus read timing



NOTE 9: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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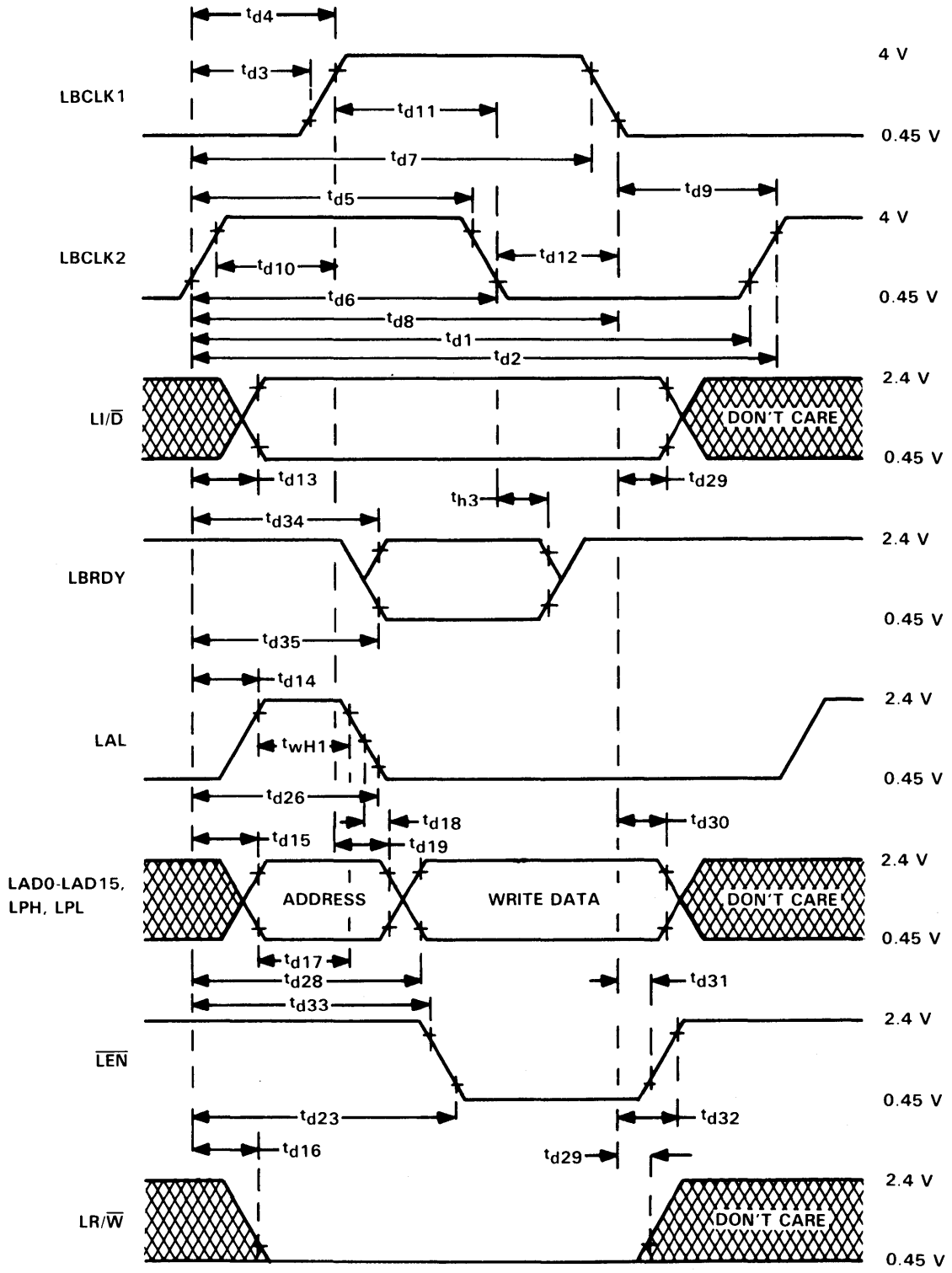
LAN Adapter bus write timing



NOTE 9: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

LAN ADAPTER BUS ARBITRATION PARAMETERS

switching requirements over recommended supply voltage range and operating free-air temperature range (see Figure 7)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay of $\overline{\text{LBRQP}}$ from LBCLK1 low		48	ns
t_{d37}	Delay of $\overline{\text{LBRQP}}$ after LBCLK1 high	0		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer high impedance by TMS38021	2Q – 9		
t_{d39}	Delay time, LBCLK2 rise to LAL driven low by TMS38021		3Q – 15	
t_{d40}	Delay time, LBCLK1 low to $\overline{\text{LEN}}$ no longer high impedance by TMS38021	80		
t_{d41}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ driven high by TMS38021		74	
t_{d42}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL no longer high impedance by TMS38021	80		

NOTE 7: Q = $0.25t_{c(LA)}$.

timing requirements over recommended supply voltage range and operating free-air temperature range

		MIN	MAX	UNIT
t_{d43}	Delay time, LBCLK2 rise to $\overline{\text{LBGRP}}$ valid		2Q – 73	ns
t_{d44}	Delay time, LBCLK2 rise to $\overline{\text{LBGRP}}$ no longer valid	–6		
t_{d45}	Delay time, LBCLK2 rise to LAL no longer driven low from old bus master	3Q – 15		
t_{d46}	Delay time, LBCLK2 rise to LAL high impedance from old bus master		4Q – 2	
t_{d47}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ high impedance from old bus master		74	
t_{d48}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL high impedance from old bus master		80	

NOTE 7: Q = $0.25t_{c(LA)}$.

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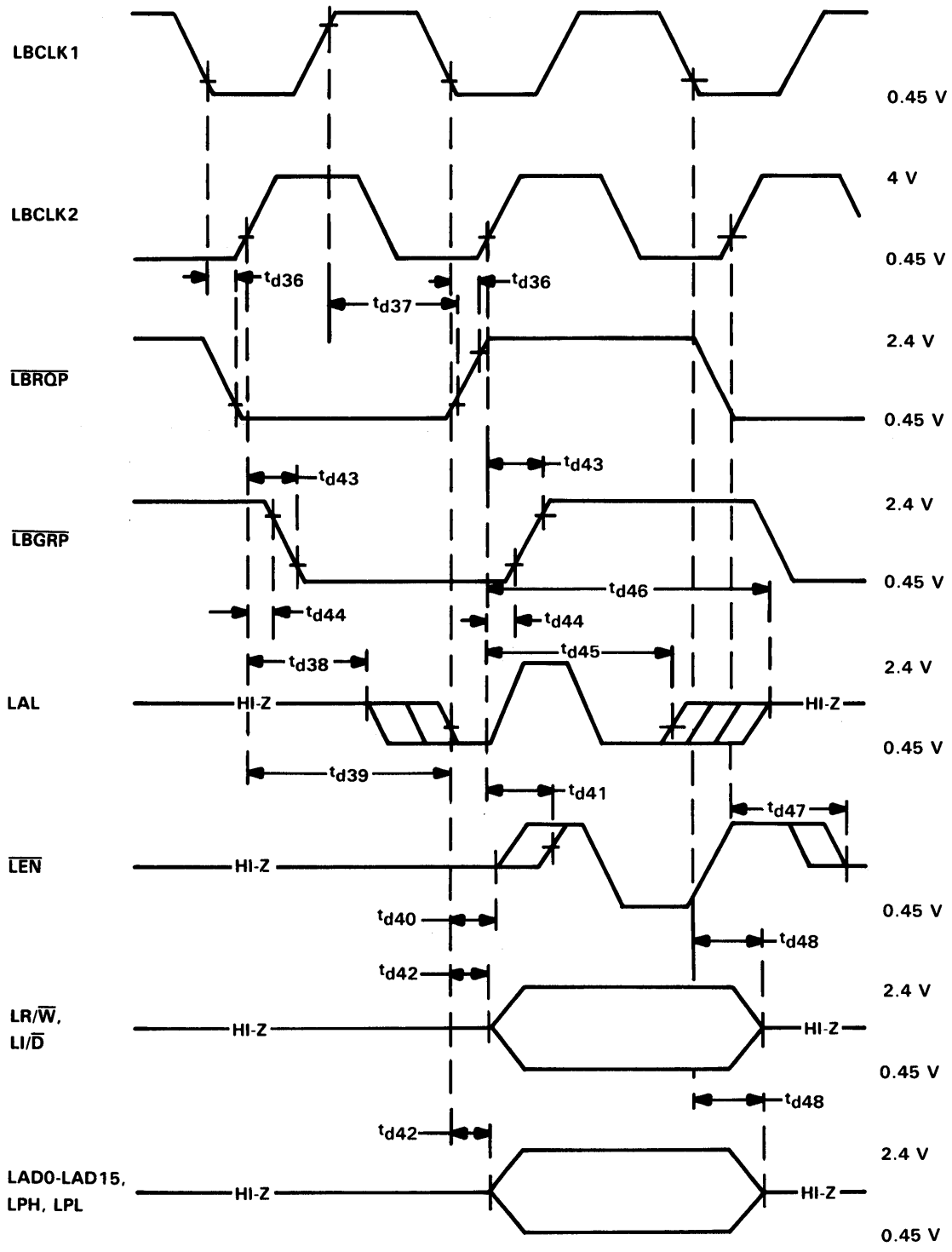
LAN Adapter bus arbitration



NOTE 10: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

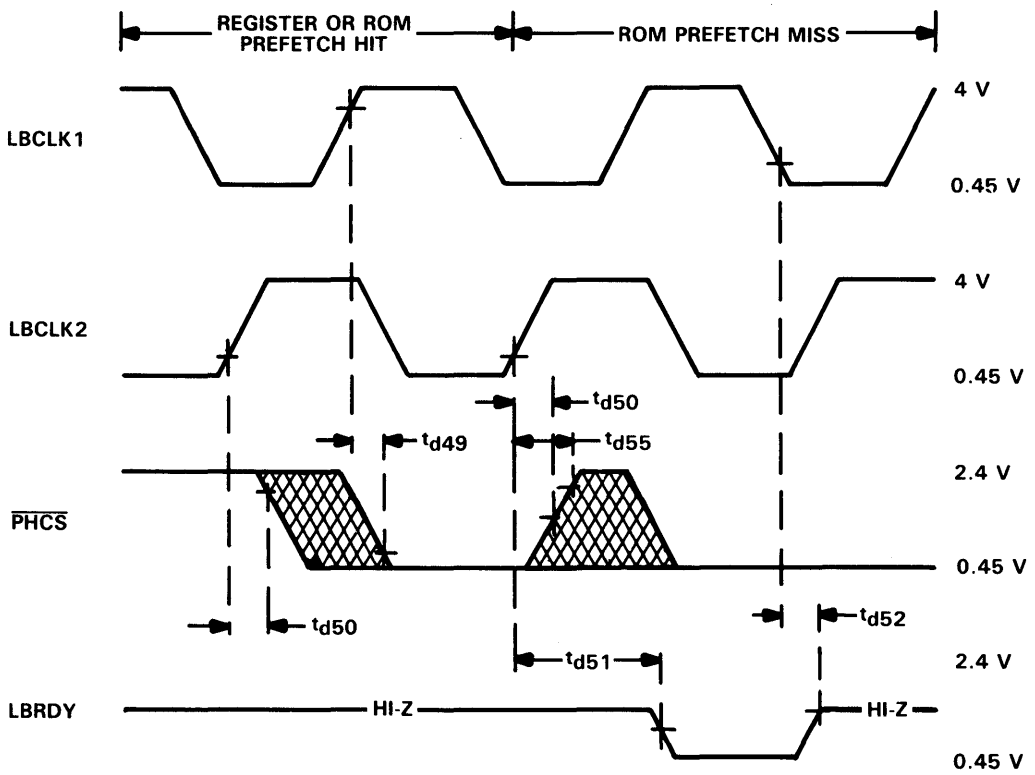
MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

		MIN	MAX	UNIT
t_{d49}	Delay time, LBCLK1 high to $\overline{PHCS}$ low		10	ns
t_{d50}	Delay time, LBCLK2 rise to $\overline{PHCS}$ no longer valid	0		
t_{d51}	Delay time, LBCLK2 rise to LBRDY driven low in ROM prefetch miss		145	
t_{d52}	Delay time, LBCLK1 low to LBRDY high impedance after ROM prefetch miss		45	
t_{d53}	Delay time, LBCLK2 rise to $\overline{PIRQ}$ valid		60	
t_{d54}	Delay time, LBCLK2 rise to $\overline{PIRQ}$ no longer valid	0		
t_{d55}	Delay time, LBCLK2 rise to $\overline{PHCS}$ high		Q – 3	

NOTE 7: Q = 0.25 $t_{c(LA)}$.

$\overline{PHCS}$ and LBRDY timing



NOTE 10: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

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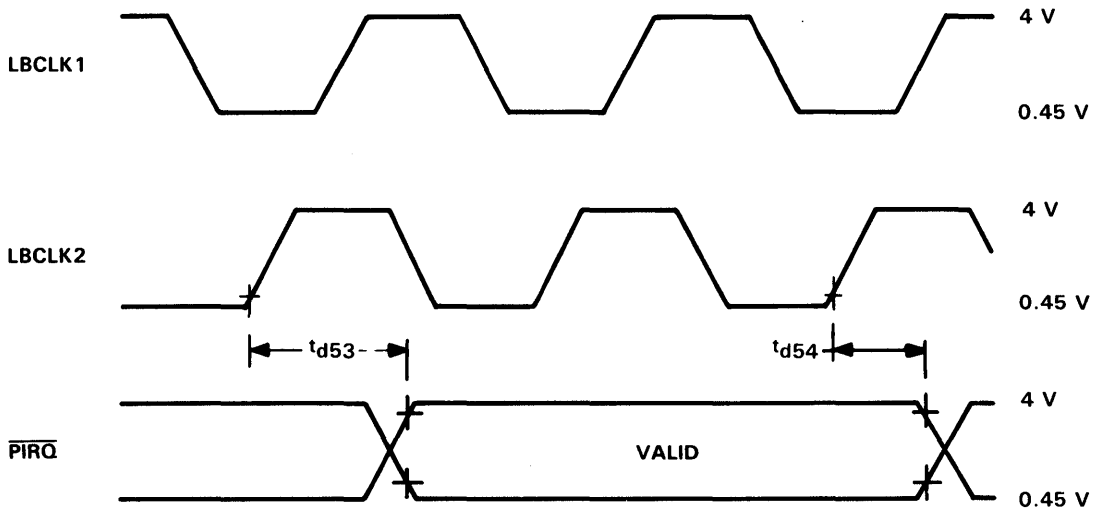
interrupt timing

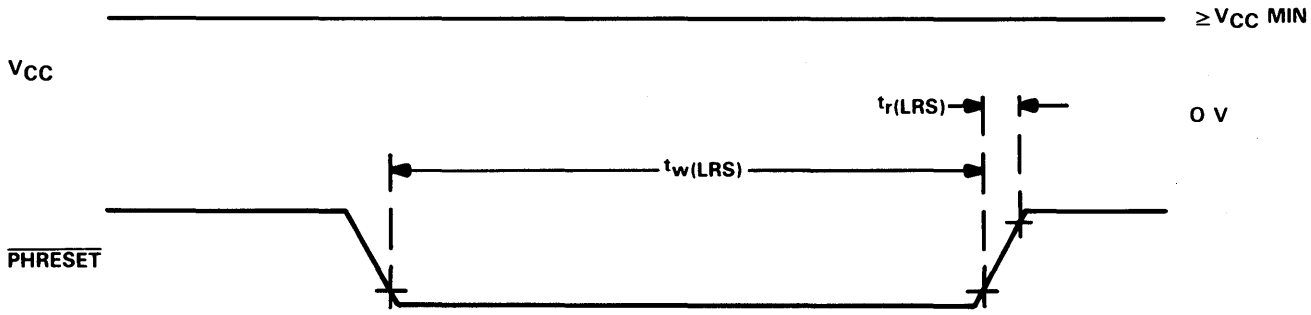


MISCELLANEOUS TIMING PARAMETERS

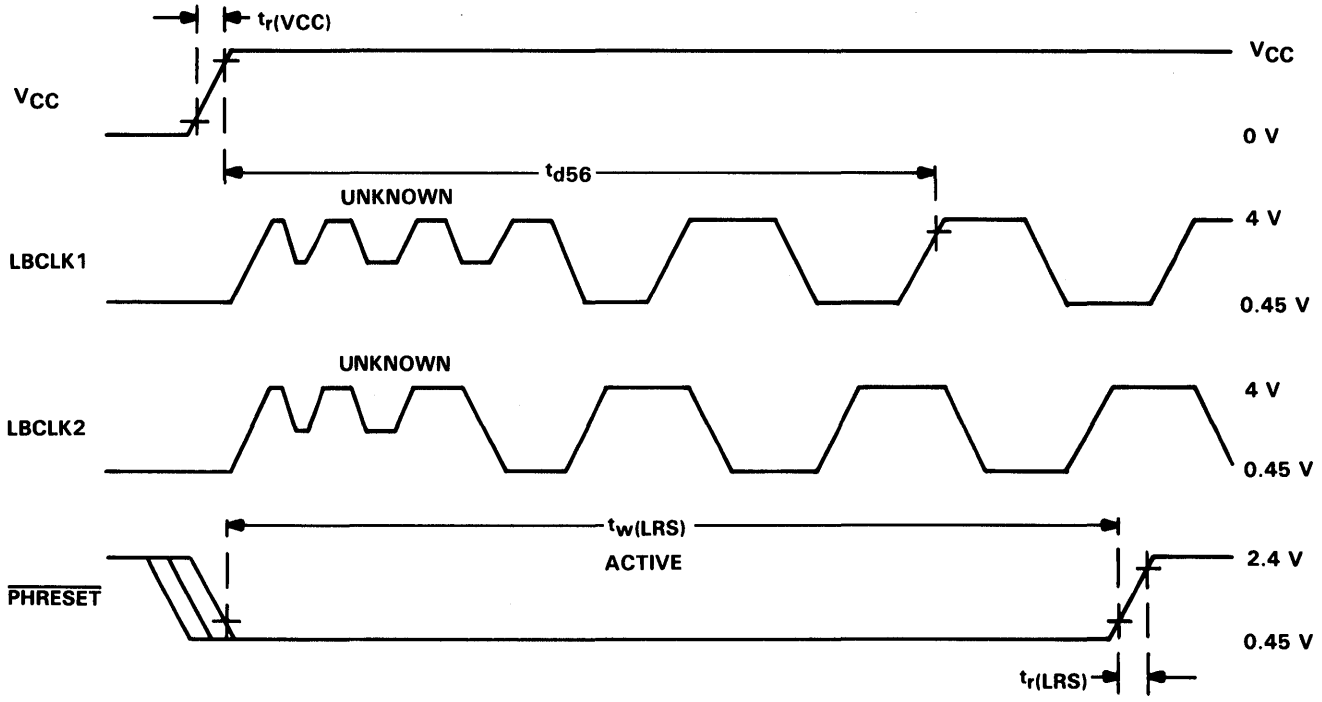
timing requirements over recommended supply voltage range and operating free-air temperature range

		MIN	MAX	UNIT
$t_{w(LRS)}$	$\overline{\text{PHRESET}}$ pulse duration, asserted with minimum V_{CC} or greater applied	14		μs
$t_{r(LRS)}$	$\overline{\text{PHRESET}}$ rise time		100	ns
$t_{r(VCC)}$	V_{CC} rise time from 1.2 V to V_{CC} minimum	1		ms
t_{d56}	Delay from reading minimum V_{CC} during power-up to valid LBCLK1, LBCLK2 with $\overline{\text{PHRESET}}$ active		90	ms

$\overline{\text{PHRESET}}$ timing



power-up, LBCLK, and $\overline{\text{PHRESET}}$ timing



NOTE 11: The timing reference points for V_{CC} are 4.5 V and 1.2 V. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for $\overline{\text{PHRESET}}$ are 2 V and 0.8 V

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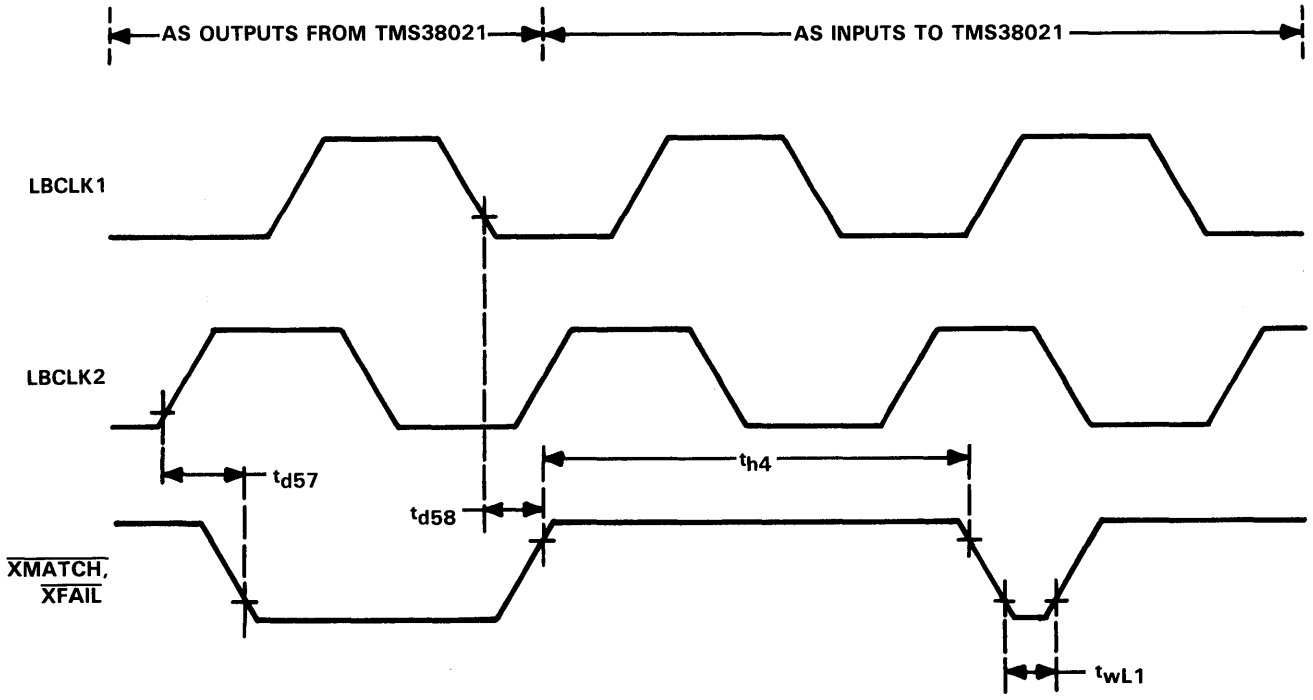
EXTERNAL COPY HARDWARE INTERFACE ($\overline{\text{XMATCH}}$, $\overline{\text{XFAIL}}$)

timing requirements over recommended supply voltage range and operating free-air temperature range

		MIN	NOM	MAX	UNIT
t_{h4}	Hold time, $\overline{\text{XMATCH}}$, $\overline{\text{XFAIL}}$ inactive-high after driven as outputs by TMS38021			6Q	ns
t_{wL1}	Pulse duration low, $\overline{\text{XMATCH}}$, $\overline{\text{XFAIL}}$	50			ns

switching characteristics over recommended supply voltage range and free-air temperature range

	PARAMETER	MIN	TYP	MAX	UNIT
t_{d57}	Delay time, LBCLK2 no longer low to $\overline{\text{XMATCH}}$, $\overline{\text{XFAIL}}$ low when driven as outputs			47	ns
t_{d58}	Delay time, LBCLK1 low to $\overline{\text{XMATCH}}$, $\overline{\text{XFAIL}}$ no longer valid.	20			ns



RING INTERFACE TIMING PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

		MIN	MAX	UNIT
$t_{c(RC)}$	RCLK cycle time (Note 14)	124.875	125.125	ns
$t_{c(PX)}$	PXTALIN cycle time	124.875	125.125	
$t_{w(RCL)}$	Pulse duration, RCLK and PXTALIN low (Notes 15, 16, 17)	46		
$t_{w(RCH)}$	Pulse duration, RCLK and PXTALIN high (Notes 15, 16, 17)	35		
$t_{su(RCVR)}$	Setup time, RCVR valid before RCLK no longer low	20		
$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK high	20		
$t_{t(RC)}$	Transition time, RCLK and PXTALIN		16	

NOTES: 14. The nominal value for $t_{c(RC)}$ is 125 ns ± 0.1%.
15. The nominal value for $t_{w(RCL)}$ and $t_{w(RCH)}$ is 62.5 ns.
16. RCVR and RCLK are driven to a high level of 2.8 V and a low level of 0.45 V during parametric tests. Timing parameters are measured from a high level of 2.6 V and a low level of 0.6 V except where shown otherwise.
17. PXTALIN is driven to a high level of 2.4 V and a low level of 0.45 V during parametric tests. Timing parameters are measured from a high level of 2 V and a low level of 0.8 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
$t_{h(DRVR)}$	Hold time, DRVR after RCLK or PXTALIN to 1.5 V level (Note 18)	12		ns
$t_{d(DRVR)}$	Delay time, RCLK or PXTALIN at 1.5 V level to DRVR at 1.5 V (Note 18)		40	
$t_{d(TRAN)}$	Delay time, data transition on DRVR ($t_{d(DRVR)} - t_{h(DRVR)}$)		5	

NOTE: 18. Timing parameters of DRVR are measured from a 1.5 V level on RCLK or PXTALIN to a 1.5 V level on DRVR.

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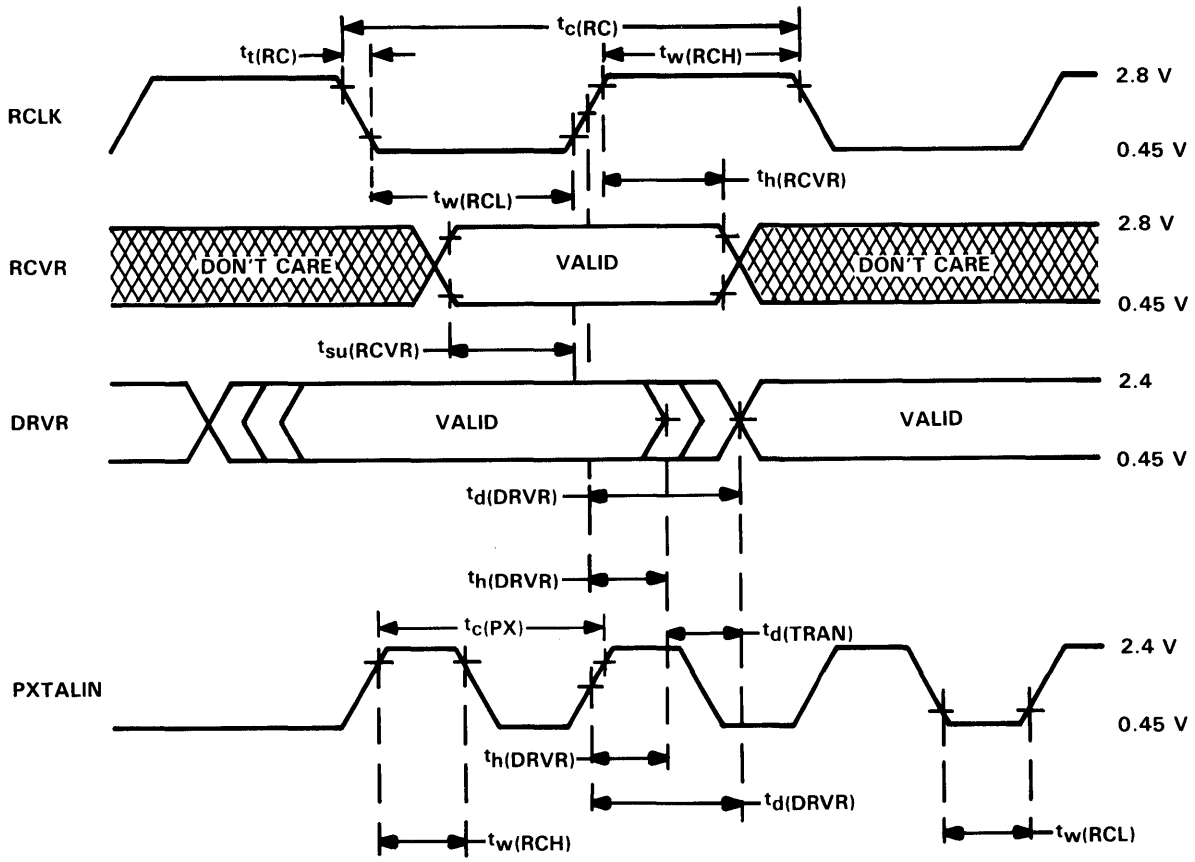
ring interface timing



NOTE 19: The timing reference points for RCVR and RCLK are 2.6 V and 0.6 V. The timing reference points for PXTALIN are 2 V and 0.8 V. The intermediate reference point for RCLK and DRVR is 1.5 V.

TMS380 ADAPTER CHIPSET USER'S GUIDE (SPWU001) MANUAL UPDATE — Revision D to E

This document updates the *TMS380 Adapter Chipset User's Guide,* Revision D, document number SPWU001D, dated July 1986. These revisions reflect a change from revision level D to revision level E.

PAGE	CHANGE OR ADD
2-9	Section 2.4 PC AT Adapter Card Example. The schematic supports standard 6-MHz PC AT buses. For higher speed buses, when the TMS380 is in 16-bit mode, 8-bit PC DIO should be used.
3-8	Add the following paragraph to the bottom of section 3.4.2 Also shown in Figure 3-3 is a structure called an abort delimiter. The abort delimiter consists of a Starting Delimiter and Ending Delimiter sequence. The abort delimiter is transmitted by the TMS380 adapter whenever the adapter detects a "false free token," as described in Section 3.10.2.
3-8	Add the following to Figure 3-3. Abort Delimiter: 
3-15	Section 3.5.2, Source Routing, has been updated per recent IEEE 802.5 activity. Section 7 of the *TMS380 Adapter Chipset User's Guide Supplement* contained in Section 3.5.2.
4-43	The second sentence of the top paragraph should be changed to read as follows: Two address-latch-enable signals, system address latch enable (SALE) and extended address latch enable (SXAL), are provided by the SIF to demultiplex the low-order eight and high-order 16 address bits, respectively.
4-68	Table 4-19. Under the description of Bit 8, remove the last sentence of this description.
4-77	In section 4.4.6.1, the fourth paragraph under item 2, remove subitem b., SSB CLEAR (bit 2), from this list.
4-88	Table 4-28. Under the description of Bytes 24-25 add the following sentence: The value in this field must be even.
4-89	Add the following note to the bottom of the page:

Note:

Under heavy ring loading conditions, especially when the heavy traffic is broadcast address frames or frames addressed to the inserting adapter, the OPEN command will fail due to a ring poll failure during the insertion process. This failure will occur due to excessive congestion on the inserting station with respect to receive activity. The OPEN command should be attempted two more times delaying 30 seconds between each attempt. If the problem persists, the source of the receive traffic to the inserting adapter should be identified and stopped or removed from the ring before attempting another OPEN command.

PAGE	CHANGE OR ADD
4-92	Add the following paragraph after the last paragraph under the section titled "buffer allocation": To avoid the possibility of transmit congestion causing transmit operations to suspend, it is recommended that a RECEIVE command and corresponding valid receive lists be issued as soon as possible following the OPEN command.
4-92	Change the second sentence under the paragraph titled "Buffer Size" to read as follows: The default TRANSMIT MAXIMUM COUNT is six, allowing a transmit frame maximum information field size of 592 bytes, including a 32 byte frame header.
4-109	Section 4.4.7.5 Close Command. The following sentence should be added to the first paragraph in this section. After issuing the CLOSE command, the Adapter should be reinitialized before re-issuing the OPEN command.
A-11	Under the table titled "recommended operating conditions," the reference to TEST0-TEST2 under the specifications for V_{IH} and V_{IL} should be removed. The TEST0-TEST2 pins now have the same V_{IH} and V_{IL} characteristics as all other inputs.
A-67	I_{CC} supply current (V_{CC} = 5.5 V, T_A = 0°C) should be changed from 240 mA max to 260 mA max.
A-77	The TMS38030-6 has been replaced by the TMS38030-8. Under the section titled "timing requirements over recommended supply voltage range and operating free-air temperature range", remove all references to the TMS38030-6.
A-108	Under the section titled "TTL input," remove the reference to FILTER under I_{IH}, I_{IL}, and I_I.
A-110	Under the section titled "phantom driver," the test conditions under the I_{OH} specification should be changed such that NSRT = V_{IH}, and the parameter I_{OL} should be removed in its entirety.
A-112	Under the section titled "energy detect," the test conditions under parameter V_{HYS} should be changed to $V_{HYS} = V_{IH} - V_{IL}$.
A-114	Figure 8. The value 240Ω assigned to the resistor should be changed to 330Ω.

B. Change to TMS380 Development Card

The Logical Link Control software is provided in two 16K × 8 EPROMs. The TMS380 PC AT adapter (TMDP380PCAT) is capable of decoding the entire range of the 16K × 8 EPROMs. The PC Family adapter (TMDP380PCF), however, needs a simple change in order to support the larger EPROMs. The change is detailed in this appendix.

The change is to the decode logic of the PC Family card. In summary, the EPROMs will now be decoded whenever LAD0 = 1. This makes the EPROM address range from >8000 to >FFFE, which is the same as the PC AT adapter.

B.1 Detailed Hardware Rework Procedure

The following procedure should be followed to alter PC Family cards.

1. Cut the trace of the $\overline{\text{ROMCS}}$ signal on the solder side of the board at location U71-15. This disables the current EPROM decode driven by the ALS137. Using an ohmmeter, verify that U71-15 is no longer connected to J2,pin 1.
2. Insert an additional 18-pin socket at the socketed location of the Burned-in Address PROM (U24 - positioned directly below the TMS38020, Protocol Handler).
3. Clip all the leads except pin 7 (Ground) of a 74AS04 (inverter). Keep pin 7 intact so that it can be used to supply Ground to the inverter.
4. Place the component in the socket as shown below. Make sure that the orientation of the component is the same as all others on the board. Pin 1 of the component should be placed at pin 3 of the socket. Since the socket has 18 pins and the inverter is a 14-pin device, place the component to the far left end of the socket so that pin 7 (GND) of the inverter will match with pin 9 of the socket. This will give the component the GND signal. This is illustrated in Figure B-1.

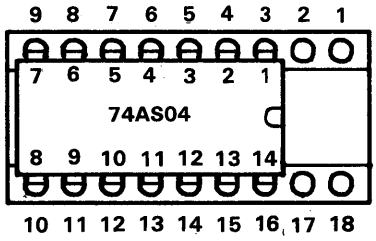


Figure B-1. Inverter in Socket

5. The component should be hotglued to the socket to insure that it will stay secured.
6. On the component side of the board, solder a wire to pin 1 of the 74AS04. Solder the open end of the wire to U8-2. U8 (ALS373) is located at the top left corner of the board above the SRAM. This connects LA0 to the input of the inverter.
7. On the component side of the board, solder a wire to pin 2 of the 74AS04. Solder the open end of the wire to J2 pin 1. This is easily done by removing the jumper clip on J2 and soldering the wire to pin 1 as close to the base as possible. The jumper clip should be positioned over pins 1-2 ON J2. This connects the output of the inverter ($\overline{LA0}$) to $\overline{ROMCS}$.
8. On the component side of the board, solder a wire to pin 14 of the 74AS04. Solder the open end of the wire to the pin 18 opening of the socket. This will give the 74AS04 the V_{CC} signal from the board.
9. Since the BIA PROM socket is being used to hold the 74AS04, the BIA should be disabled by placing the jumper (J3) clip between pins 1-2.

Note:

If the user desires to use a Burned-in Address on the card, then the inverter should be placed upside down on another TTL part, so that ground and V_{CC} are fed to the inverter from the board. It should then be wired according to this procedure. Alternately, the inverter can be placed in the BIOS ROM socket. Refer to the PC Family card schematics to determine Ground and V_{CC} connections.

The following is a marked sheet 3 of the PC Family card logic diagram with modifications shown.

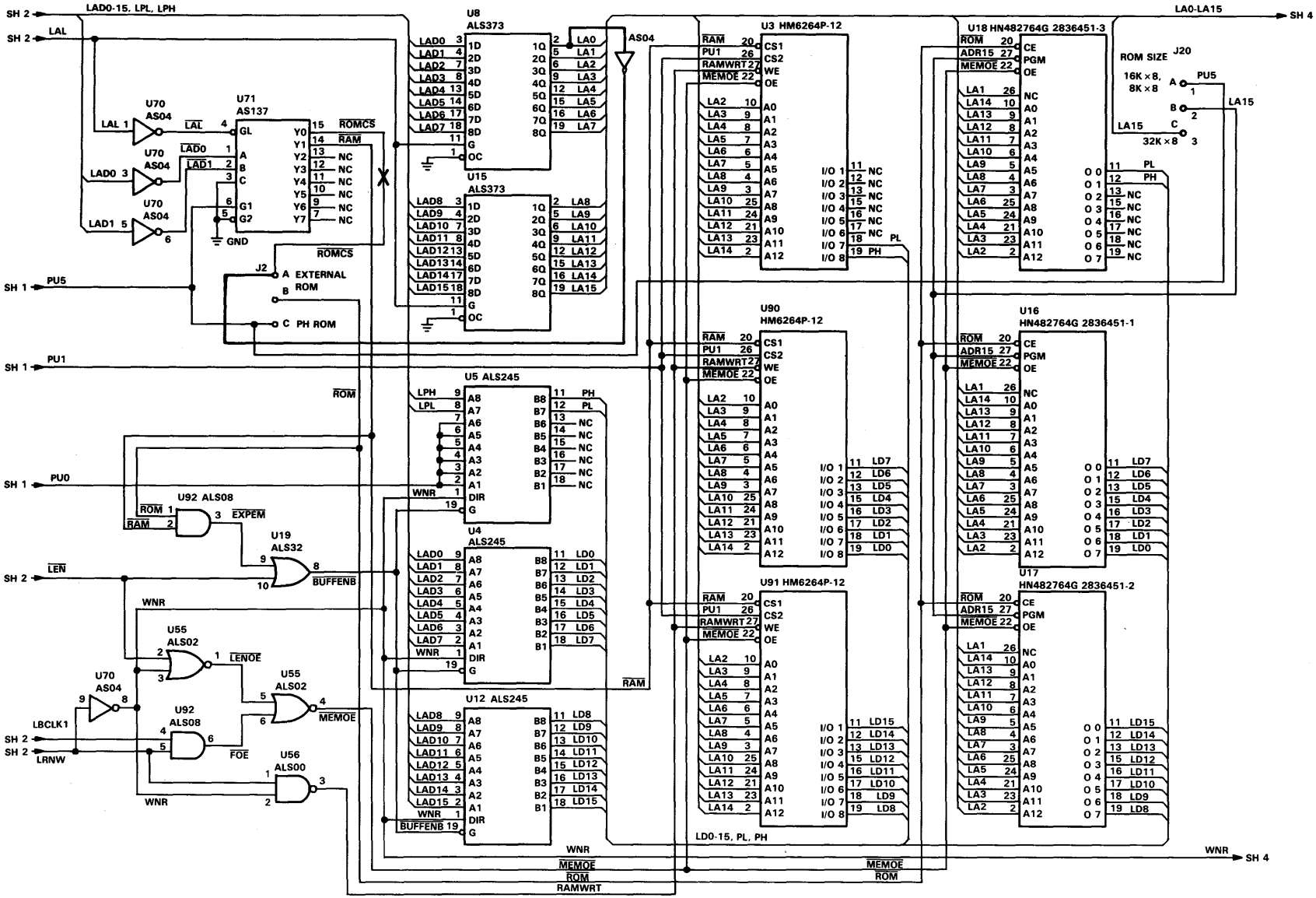


Figure B-2. PC Family Card Logic with Modifications

C. Sample Download Driver

This appendix contains a listing of the C source for a PC based routine that will download TMS380 software into the adapter for execution. This routine can be used for either DLC software or Adapter Debug software, B205 as described in this manual.

```
/*********************************************************/
/*                DOWNLOAD  PROGRAM                      */
/*                                                       */
/* This DOWNLOAD routine takes as input a TI tagged      */
/*  object file.  It places the adapter in the           */
/*  download state, and downloads the input software     */
/*  into the adapter for execution.                      */
/*                                                       */
/* The adapter is assumed to be at locations >xx20       */
/*  thru >xx29 in PC I/O space, where >xx is set by      */
/*  the user on initiation of the software.              */
/*                                                       */
/* The DOWNLOAD routine assumes that the adapter         */
/*  software's starting point is at address >0600 on     */
/*  the adapter bus.  >0600 is the starting address      */
/*  for both the Adapter Debug Software (ADS) B205,      */
/*  and the DLC software (OSI2).                         */
/*                                                       */
/* This listing is for illustration only.                */
/*                                                       */
/* Revision History:                                     */
/*    Initial release: 03/15/87                          */
/*    Modified for new memory map: 5/29/87               */
/*                                                       */
/*********************************************************/

#include        <stdio.h>
#include        <conio.h>
#include        <process.h>

#define CLS             printf("\033[2J")
#define DATA_LO         0x00+base_addr
#define DATA_HI         0x01+base_addr
#define DATAINC_LO      0x02+base_addr
#define DATAINC_HI      0x03+base_addr
#define ADDRESS_LO      0x04+base_addr
#define ADDRESS_HI      0x05+base_addr
#define INTERRUPT_LO    0x06+base_addr
#define INTERRUPT_HI    0x07+base_addr
#define CONBUF          0x09+base_addr
#define PHDISABLE       0x30    /* PHDIS AND HW_INT_ENABLE */
#define HW_RESET        0x04
#define HW_RESET2       0x00
#define HW_INT_ENABLE   0x20    /*  enable interrupts from adapter */
#define DELAY           25      /*  500 usec delay loop constant   */
#define FD_STEP         0xFF    /*  Freezedump commands            */
#define FD_WRITE        0xE6
#define FD_EXECUTE      0xC5
#define CODE_START_LO   0x00    /*  Code entry point for ADS B205  */
#define CODE_START_HI   0x06    /*   or OSI2, DLC softare          */
#define ENMS_START_LO   0x00    /*  Code entry point for PHCS      */
#define ENMS_START_HI   0x0A    /*   disable and freeze dump code  */
#define ENM_DONE        0x70    /*  ENM code finished flag        */
#define YES             1
#define NO              0
```

```
unsigned int lineptr,adp_ad,linenum,try,temp,endflag,
             address,stepcnt,base_addr,done,ENMFILE;
char inline[90],yesno;
int numsteps;

main()
   {
   int temp;
   FILE  *OSI2;
   FILE  *ENM;

   try=1;
   ENMFILE = YES;
   CLS;
   printf("\nADAPTER BASE ADDRESS: ");
   gets(inline);
   sscanf(inline, "%x", &base_addr);

   printf("\nDLC SOFTWARE FILE: ");
   gets(inline);
   if ((OSI2 = fopen(inline, "r")) == NULL)
      {
      printf("FILE %s NOT FOUND. ", inline);
      exit(1);
      }

   printf("\nENM SOFTWARE FILE: ");
   gets(inline);
   if ((ENM = fopen(inline, "r")) == NULL)
      {
      printf("FILE %s NOT FOUND. ", inline);
      printf("  DO YOU WISH TO CONTINUE? (Y/N):");
      gets(inline);
      sscanf(inline, "%c" ,&yesno);
      if((yesno == 'N') || (yesno == 'n'))
        exit(1);
       else
        ENMFILE=NO;
     }

/* Put the adapter in Freeze-Dump Mode  */

start:  outp(CONBUF, HW_RESET);
   outp(CONBUF, HW_RESET2);
   for (temp = DELAY; temp; temp--) ;
   outp(CONBUF, HW_RESET);
   outp(CONBUF, HW_RESET2);
   outp(CONBUF, HW_INT_ENABLE);
   outp(INTERRUPT_HI, 0x80);

   for (temp = DELAY; temp; temp--) ;
   for (temp = DELAY; temp; temp--) ;
   for (temp = DELAY; temp; temp--) ;

   if (inp(INTERRUPT_LO) || inp(INTERRUPT_HI))  {
      try++;
      if(try < 5) {
        printf("\nDOWNLOAD MODE NOT ENTERED - RETRYING\n");
        goto start;
        }
       else {
        printf("DOWNLOAD ABORTED\nPLEASE RESET THE ADAPTER\n");
        exit(1);
        }
```

```
    }
  /* Write the starting address for the adapter into adapter  */
  /*  address >0000.                                          */

  outp(INTERRUPT_HI, FD_WRITE);     /* enable DIO writes       */

  if (ENMFILE == YES) {
     outp(DATA_LO,ENMS_START_LO);      /* write starting address */
     outp(DATA_HI,ENMS_START_HI);
     downcode(ENM);
     done=NO;
     while(done==NO) {
       if ((inp(INTERRUPT_LO) == ENM_DONE) && (inp(INTERRUPT_HI == 0)))
        done = YES;
       }
     outp(CONBUF,PHDISABLE);
   }

  outp(ADDRESS_LO,0);                /* clear out SIF ADDRESS register */
  outp(ADDRESS_HI,0);
  outp(DATA_LO,CODE_START_LO);       /* write starting address */
  outp(DATA_HI,CODE_START_HI);
  downcode(OSI2);
  printf("ADAPTER IS EXECUTING LLC - CHECK FOR BUD CODE COMPLETION\n");
  exit(0);
}
downcode(OBJCODE)

 FILE  *OBJCODE;

 {

  /* Read input file and download the software     */

  adp_ad = 0;
  linenum = 0;
  while (fgets(inline, 90, OBJCODE) != NULL)  {
     linenum++;
     endflag = 0;

     if (linenum == 1)  {
        if (!sscanf(inline, "%*13c9%4x", &adp_ad))  {
           printf("Illegal header in file.  Download aborted");
           exit(1);
           }
         else
           lineptr = 18;
        printf("\nDOWNLOADING.");
        }
     else
        lineptr = 0;

     if (inline[0] == ':')  {
        printf("\n END OF FILE REACHED");
        outp(INTERRUPT_HI,FD_EXECUTE);
        return;
        }
```

```
    else {

      while (lineptr < 90 && !endflag)
        switch (inline[lineptr])
         {
         case '9':
            {
            sscanf(&inline[lineptr], "9%4x", &adp_ad);
            printf(".");
            lineptr += 5;
            break;
            }
         case 'B':
            {
            sscanf(&inline[lineptr], "B%4x", &temp);
            address = (inp(ADDRESS_HI) << 8) | inp(ADDRESS_LO);
            if (address != adp_ad)  {
              outp(ADDRESS_LO, adp_ad & 0xff);
              outp(ADDRESS_HI, adp_ad >> 8);
              numsteps = (adp_ad >> 11) - (address >> 11);
              if (numsteps < 0)
                 numsteps += 32;
              for (stepcnt = 0; stepcnt < numsteps; stepcnt++)
                outp(INTERRUPT_HI, FD_STEP);
              }

            outp(DATAINC_LO, temp & 0xff);
            outp(DATAINC_HI, temp >> 8);
            lineptr += 5;
            adp_ad += 2;
            break;
            }
         case 'F':
            {
            endflag = 1;
            break;
            }
         default:
            {
            printf("\nILLEGAL TAG CHARACTER");
            printf("'%c' in line %u: ",
                    inline[lineptr], lineptr);
            exit(1);
            }
         }          /* end of switch      */
       }            /* end of else        */

      if (!endflag)  {
        printf("\nILLEGAL FORMAT ON LINE %u", lineptr);
        exit(1);
        }

      }      /* end of while loop */

printf("\n FILE ERROR AT LINE %u: ", linenum);
exit(1);
}
```

D. Comparison to IBM Commands

This appendix makes a comparison between the commands at the interface to the TMS380 with DLC (as described in Section 2), and IBM's programming interfaces. Table D-1 compares the commands at the TMS380 with those at the user interface to IBM's PC software interface (per IBM's *Token-Ring PC Adapter Technical Reference,* document #69X7862) program. Table D-2 compares commands at the TMS380 interface with commands at the interface to IBM's adapter hardware.

Table D-1. Comparison to IBM PC Software Interface

IBM TOKREUI COMMAND	TMS380 COMMAND	COMMENTS
DIR.CLOSE.ADAPTER	CLOSE	
DIR.CONFIG.BRIDGE.PARMS	CONFIG.BRIDGE.PARMS	
DIR.INITIALIZE	INITIALIZATION PROCEDURE	EXECUTED THRU DIO
DIR.INTERRUPT	DIR.INTERRUPT	
DIR.MODIFY.OPEN.PARAMETERS	MODIFY.OPEN.PARAMETERS	
DIR.OPEN.ADAPTER	OPEN	
DIR.READ.LOG	READ.ERROR.LOG	
DIR.RESTORE.OPEN.PARAMETERS	RESTORE.OPEN.PARAMETERS	
DIR.SET.BRIDGE.PARAMETERS		DEPENDENT ON SPECIFIC BRIDGE IMPLEMENTATION
DIR.SET.FUNCTIONAL.ADDRESS	SET.FUNCTIONAL.ADDRESS	
DIR.SET.GROUP.ADDRESS	SET.GROUP.ADDRESS	
DIR.STATUS	READ.ADAPTER	CAN BE USED TO GET STATUS INFORMATION
DLC.CLOSE.SAP	CLOSE.SAP	
DLC.CLOSE.STATION	CLOSE.STATION	
DLC.CONNECT.STATION	DLC.CONNECT.STATION	
DLC.FLOW.CONTROL	DLC.FLOW.CONTROL	
DLC.MODIFY	MODIFY.LLC.PARMS	
DLC.OPEN.SAP	OPEN.SAP	
DLC.OPEN.STATION	OPEN.STATION	
DLC.REALLOCATE	LLC.REALLOCATE	
DLC.RESET	LLC.RESET	
DLC.STATISTICS	STATION.STATS	
RECEIVE	RECEIVE	
RECEIVE.CANCEL		USE RECEIVE.CANCEL INTERRUPT
RECEIVE.MODIFY	RECEIVE	USE RECEIVE.VALID INTERRUPT
TRANSMIT.DIR.FRAME	TRANSMIT	FRAME TYPE = 000
TRANSMIT.I.FRAME	TRANSMIT	FRAME TYPE = 110
TRANSMIT.UI.FRAME	TRANSMIT	FRAME TYPE = 001
TRANSMIT.TEST.CMD	TRANSMIT	FRAME TYPE = 101
TRANSMIT.XID.CMD	TRANSMIT	FRAME TYPE = 010
TRANSMIT.XID.RESP.FINAL	TRANSMIT	FRAME TYPE = 011
TRANSMIT.XID.RESP.NOT.FINAL	TRANSMIT	FRAME TYPE = 100
BUFFER.FREE	– EXECUTED ENTIRELY BY PC SOFTWARE	
BUFFER.GET	– EXECUTED ENTIRELY BY PC SOFTWARE	
DIR.TIMER.SET	– EXECUTED ENTIRELY BY PC SOFTWARE	
DIR.TIMER.CANCEL	– EXECUTED ENTIRELY BY PC SOFTWARE	
DIR.TIMER.CANCEL.GROUP	– EXECUTED ENTIRELY BY PC SOFTWARE	
DIR.SET.USER.APPENDAGE	– EXECUTED ENTIRELY BY PC SOFTWARE	
DIR.DEFINE.MIF.ENVIRONMENT	– EXECUTED ENTIRELY BY PC SOFTWARE	
PDT.TRACE.ON	– EXECUTED ENTIRELY BY PC SOFTWARE	
PDT.TRACE.OFF	– EXECUTED ENTIRELY BY PC SOFTWARE	

Table D-2. Comparison to IBM Hardware SRB Commands

IBM SRB COMMAND	TMS380 COMMAND	COMMENTS
DIR.CLOSE.ADAPTER	CLOSE	
DIR.CONFIG.BRIDGE.PARMS	CONFIG.BRIDGE.PARMS	
DIR.INTERRUPT	DIR.INTERRUPT	
DIR.MODIFY.OPEN.PARAMETERS	MODIFY.OPEN.PARAMETERS	
DIR.OPEN.ADAPTER	OPEN	
DIR.READ.LOG	READ.ERROR.LOG	
DIR.RESTORE.OPEN.PARAMETERS	RESTORE.OPEN.PARAMETERS	
DIR.SET.BRIDGE.PARAMETERS		DEPENDENT ON SPECIFIC BRIDGE IMPLEMENTATION
DIR.SET.FUNCTIONAL.ADDRESS	SET.FUNCTIONAL.ADDRESS	
DIR.SET.GROUP.ADDRESS	SET.GROUP.ADDRESS	
	READ.ADAPTER	IBM READS SHARED RAM DIRECTLY
DLC.CLOSE.SAP	CLOSE.SAP	
DLC.CLOSE.STATION	CLOSE.STATION	
DLC.CONNECT.STATION	DLC.CONNECT.STATION	
DLC.FLOW.CONTROL	DLC.FLOW.CONTROL	
DLC.MODIFY	MODIFY.LLC.PARMS	
DLC.OPEN.SAP	OPEN.SAP	
DLC.OPEN.STATION	OPEN.STATION	
DLC.REALLOCATE	LLC.REALLOCATE	
DLC.RESET	LLC.RESET	
DLC.STATISTICS	STATION.STATS	
	RECEIVE	IBM AUTOMATICALLY RECEIVES WHEN OPEN
TRANSMIT.DIR.FRAME	TRANSMIT	FRAME TYPE = 000
TRANSMIT.I.FRAME	TRANSMIT	FRAME TYPE = 110
TRANSMIT.UI.FRAME	TRANSMIT	FRAME TYPE = 001
TRANSMIT.TEST.CMD	TRANSMIT	FRAME TYPE = 101
TRANSMIT.XID.CMD	TRANSMIT	FRAME TYPE = 010
TRANSMIT.XID.RESP.FINAL	TRANSMIT	FRAME TYPE = 011
TRANSMIT.XID.RESP.NOT.FINAL	TRANSMIT	FRAME TYPE = 100

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