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Component Data Catalog

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- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to effect its safety or effectiveness.

Contents

CROSS REFERENCE LIST

DIFFERENTIAL LINE DRIVERS

National Semiconductor	Startech Semiconductor
DS26C31/DS26LS31	ST26C31
DS34C86/DS34LS86	ST34C86
AMD	Startech Semiconductor
AM26LS31	ST26C31

DIFFERENTIAL LINE RECEIVERS

National Semiconductor	Startech Semiconductor
DS26C32/DS26LS32	ST26C32
DS34C87/DS34LS87	ST34C87
AMD	Startech Semiconductor
AM26LS32	ST26C32

DIFFERENTIAL LINE RECEIVERS / DRIVERS

Motorola Semiconductor	Startech Semiconductor
MC34050	ST34C50
MC34051	ST34C51

UARTS

National Semiconductor	Startech Semiconductor
INS8250A	ST16C450
INS82C50A	ST16C450
NS16450	ST16C450
NS16C450	ST16C450
NS16550AF	ST16C550
NS16C552	ST16C2552
Silicon Systems	Startech Semiconductor
SSI73M550	ST16C550
SSI73M1550	ST16C1450 / ST16C1550
SSI73M2550	ST16C1451 / ST16C1551
SSI73M2551	ST16C1552
VLSI Technology, Inc.	Startech Semiconductor
VL82C50A	ST16C450
VL16C450	ST16C450
VL16C550	ST16C550
Western Digital Inc.	Startech Semiconductor
WD16C450	ST16C450
WD16C550	ST16C550

CROSS REFERENCE LIST

Texas Instruments	Startech Semiconductor
TL16C450	ST16C450
TL16C550A	ST16C550
Exar Corporation	Startech Semiconductor
XR16C450	ST16C450
XR16C550	ST16C550
UARTS WITH PRINTER	
VLSI Technology, Inc.	Startech Semiconductor
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Texas Instruments	Startech Semiconductor
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Integrated Circuit Systems, Inc.	Startech Semiconductor
ICS2494XXX	ST49C214-XX
ICS9064	ST49C064
ICS9154-XX	ST49C154-XX
ICS9158	ST49C158
Avasem Corporation	Startech Semiconductor
AV9064	ST49C064
AV9103-XX	ST49C103-XX
AV9104-XX	ST49C104-XX
AV9106	ST49C106
AV9107-XX	ST49C107-XX
AV9155-XX	ST49C155-XX
STEREO CLOCK GENERATOR	
MicroClock Inc.	Startech Semiconductor
MK1418	ST49C418

CROSS REFERENCE LIST

DIFFERENTIAL LINE DRIVERS

Startech Semiconductor	National Semiconductor
ST26C31	DS26C31/DS26LS31
	AMD
	AM26LS31
	National Semiconductor
ST34C86	DS34C86/DS34LS86

DIFFERENTIAL LINE RECEIVERS

Startech Semiconductor	National Semiconductor
ST26C32	DS26C32/DS26LS32
	AMD
	AM26LS32
	National Semiconductor
ST34C87	DS34C87/DS34LS87

DIFFERENTIAL LINE RECEIVERS / DRIVERS

Startech Semiconductor	Motorola Semiconductor
ST34C50	MC34050
ST34C51	MC34051

UARTS

Startech Semiconductor	National Semiconductor
ST16C450	INS8250A
	INS82C50A
	NS16450
	NS16C450
	VLSI Technology, Inc.
	VL82C50A
	VL16C450
	Western Digital Inc.
	WD16C450
	Texas Instruments
	TL16C450
	Exar Corporation
	XR16C450
Startech Semiconductor	National Semiconductor

CROSS REFERENCE LIST

ST16C550	NS16550AF
	Silicon Systems SSI73M550
	VLSI Technology, Inc. VL16C550
	Western Digital Inc. WD16C550
	Texas Instruments TL16C550A
	Exar Corporation XR16C550
ST16C1450 ST16C1550	Silicon Systems SSI73M1550
ST16C1451 ST16C1551	SSI73M2550
ST16C2552	SSI73M2551
ST16C2552	National Semiconductor NS16C552
UARTS WITH PRINTER Startech Semiconductor ST16C452AT	VLSI Technology, Inc. VL16C452
	Exar Corporation XR16C452
ST16C452AT/PS	Western Digital Inc. WD16C452
ST16C452AT/PS	Texas Instruments TL16C452
	VLSI Technology, Inc.

CROSS REFERENCE LIST

ST16C552/553	VL16C552
	Exar Corporation XR16C552
	Western Digital Inc. WD16C552
	Texas Instruments TL16C552
VIDEO DOT CLOCK GENERATOR	
Startech Semiconductor ST49C064	Avasem Corporation AV9064
	Integrated Circuit Systems, Inc. ICS9064
Startech Semiconductor ST49C103-XX ST49C104-XX ST49C106 ST49C107-XX ST49C155-XX	Avasem Corporation AV9103-XX AV9104-XX AV9106 AV9107-XX AV9155-XX
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FREQUENCY SYNTHESIZERS 1

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ST49C001

Printed August 3, 1995

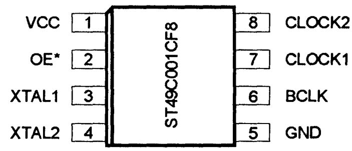
PREPROGRAMMED HIGH SPEED FREQUENCY SYNTHESIZER

1

DESCRIPTION

The ST49C001 is a mask programmable monolithic analog CMOS device, designed to replace existing high frequency crystal/oscillator with single low frequency crystal. The ST49C001 provides two high speed and low jitter clock outputs.
ST49C001 is designed for Magneto-Optical Disk Drive (MODD) appplication.

SOIC Package



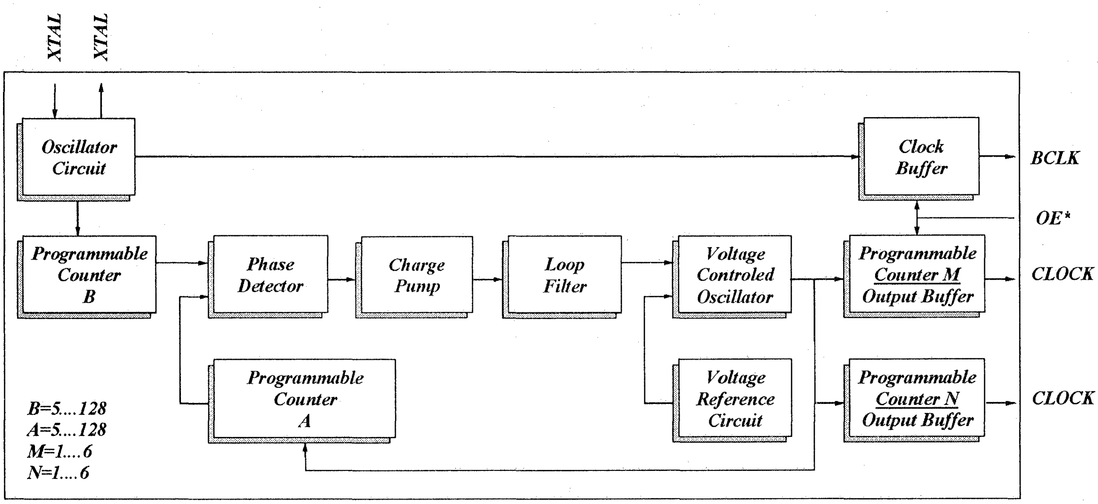
FEATURES

- Can replace expensive high frequency oscillators.
- Mask programmable analog phase locked loop
- On board loop filter
- 5V 1.2μCMOS technology
- 8 pin SOIC package.
- Crystal oscillator circuit on board

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C001CF8	SOIC	0° C to +70° C
ST49C001CP8	Plastic-DIP	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
VCC	1	I	Supply voltage. Single +5 volts.
OE*	2*	I	Output Enable (Active low). CLOCK1 and BCLK outputs are disabled and forced to low state when this pin is low. CLOCK2 output pin is active when CLOCK1 and BCLK outputs are disabled.
XTAL1	3	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
GND	5	O	Supply ground.
BCLK	6	O	Buffered reference clock output.
CLOCK1	7	O	Preprogrammed clock output.
CLOCK2	8	O	Preprogrammed clock output.

* Has internal pull-up resistor

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047μF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C001 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C001 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK1 = (Reference clock) X 2A/B X 1/M
CLOCK2 = (Reference clock) X 2A/B X 1/N

where A=5, 6, 7,.........128
B=5, 6, 7,.........128
M=1, 2,...6
N=1, 2, ...6

ST49C001-01 Frequency table

INPUT FREQUENCY	OUTPUT FREQUENCIES
16.934 MHz	49.143 MHz 29.486 MHz

ST49C001

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0-70° C, Vcc=4.0 - 5.5V unless otherwise specified.

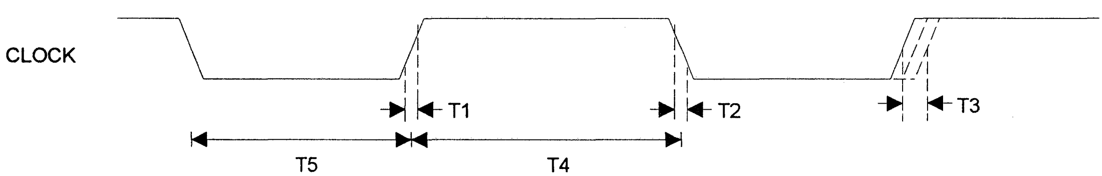
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-100	μA	Pin 2 only
I_{IH}	Input high current			1	μA	VIN=Vcc Pin 2
I_{CC}	Operating current		45	55	mA	No load, OE High, All Clock outputs active
R_{IN}	Input pull-up resistance	60	85	110	kΩ	OE Pin

AC ELECTRICAL CHARACTERISTICS

T_A=0-70° C, Vcc=5.0 V unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	CLOCK rise time		3	5.5	ns	CL=20pF 0.4V - 2.4V
T_2	CLOCK fall time		3	5.5	ns	CL=20pF 2.4V - 0.4V
$T_{4,5}$	Duty cycle	40	47	60	%	CL=20pF @ Vcc/2
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	

TIMING DIAGRAM

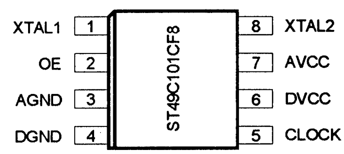


PREPROGRAMMED HIGH SPEED FREQUENCY MULTIPLIER

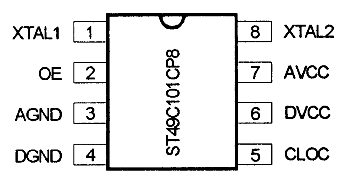
DESCRIPTION

The ST49C101/102 is a mask programmable monolithic analog CMOS device, designed to replace existing high frequency crystal/oscillator with single low frequency crystal. The ST49C101/102 provides high speed and low jitter clock output.
ST49C101/102 is designed in a 1.2μ process to achieve 100 MHz speed for high end frequencies.

SOIC Package



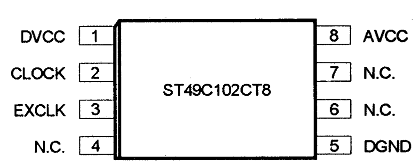
Dip Package



FEATURES

- Can replace expensive high frequency oscillator.
- Mask programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package.
- Crystal oscillator circuit on board

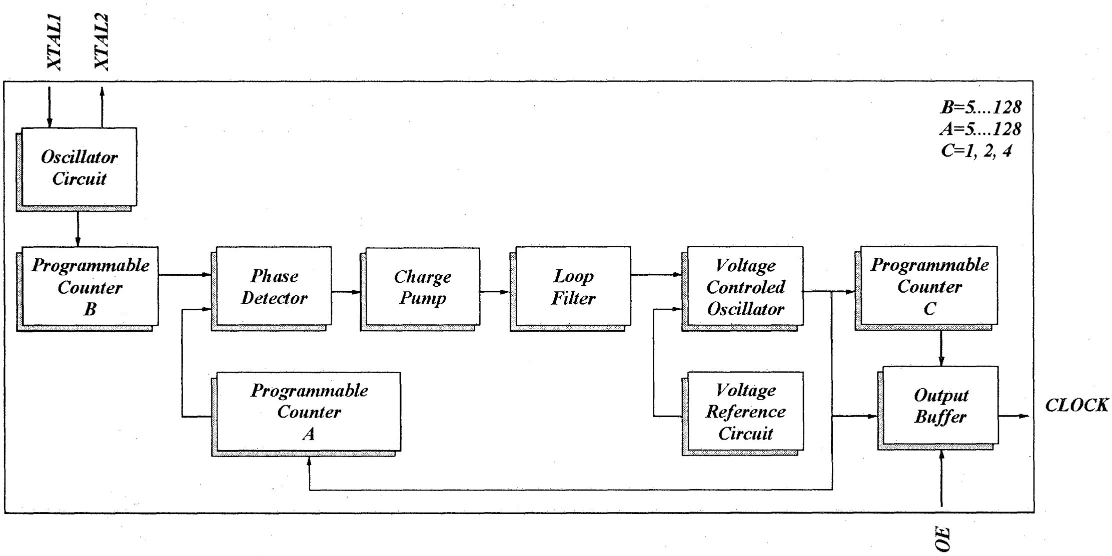
TSSOP Package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C101CP8	Plastic-DIP	0 ° C to +70° C
ST49C101CF8	SOIC	0° C to +70° C
ST49C102CT8	TSSOP	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C101)

Symbol	Pin	Signal Type	Pin Description
XTAL1	1	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external clock, XTAL2 is left open or used as buffered clock output.
OE	2*	I	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
AGND	3	O	Analog ground.
DGND	4	O	Digital ground.
CLOCK	5	O	Programmed output clock.
DVCC	6	I	Positive supply voltage. Single +5 volts.
AVCC	7	I	Analog supply voltage. Single +5 volts.
XTAL2	8	O	Crystal output.

* Has internal pull-up resistor

SYMBOL DESCRIPTION (ST49C102)

Symbol	Pin	Signal Type	Pin Description
DVCC	1	I	Digital Positive supply voltage. Single +5 volts.
CLOCK	2	O	Pre-programmed output clock.
EXCLK	3	I	External Clock input. Input reference clock.
DGND	5	O	Digital ground.
AVCC	8	I	Analog supply voltage. Single +5 volts.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047μF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C101/102 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C101/102 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X 2A/(BXC)

where A=5, 6, 7,.........128
B=5, 6, 7,.........128
C=1,2,4

Preprogrammed options:

ST49C101-X	Factor	Max. Output Frequency
ST49C101-01	12	100 MHz
ST49C101-02	6	100 MHz
ST49C101-03	8	130 MHz
ST49C101-04	4	100 MHz

ST49C102	Input Frequency	Output Frequency
ST49C102	40MHz	60MHz

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0 - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-100	µA	Pin 2 only
I_{IH}	Input high current			1	µA	VIN=Vcc Pin 2
I_{CC}	Operating current		55	65	mA	No load. CLOCK=100MHz
R_{IN}	Input pull-up resistance	50	75	100	kΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=0 - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
$T_{1,2}$	CLOCK rise/fall time		1.5	3	ns	Load=30 pF, 0.6V - 2.2V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	VCC/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	
T_{IN}	Input reference frequency	7	10	25	MHz	
T_{OUT}	Output frequency			130	MHz	

DC ELECTRICAL CHARACTERISTICS (ST49C101-02 and -04 ONLY)

T_A=0 - 70° C, Vcc=3.0V ± 10% unless otherwise specified.

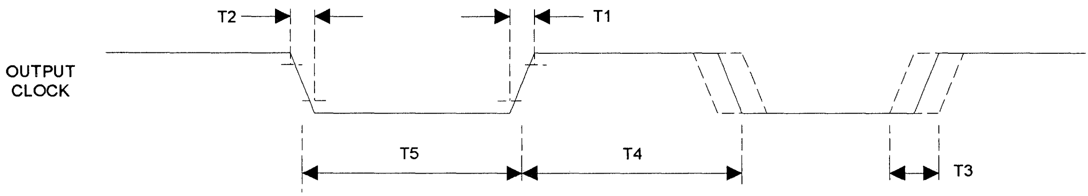
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 4.0 mA
V_{OH}	Output high level	2.0			V	I_{OH} = 4.0 mA
I_{IL}	Input low current			-100	μA	Pin 2 only
I_{IH}	Input high current			1	μA	VIN=Vcc Pin 2
I_{CC}	Operating current		40	60	mA	No load. CLOCK=80 MHz
R_{IN}	Input pull-up resistance	50	75	100	kΩ	

AC ELECTRICAL CHARACTERISTICS (ST49C101-02 and -04 ONLY)

T_A=0 - 70° C, Vcc=3.0V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
$T_{1,2}$	CLOCK rise/fall time		2	3	ns	Load 30pF, 0.6V - 2.2V
T_5	Duty cycle	45	48/52	55	%	VCC/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	
T_{IN}	Input reference frequency	7	10	20	MHz	
T_{OUT}	Output frequency			80	MHz	

TIMING DIAGRAM



STARTECH
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ST49C103
ST49C104

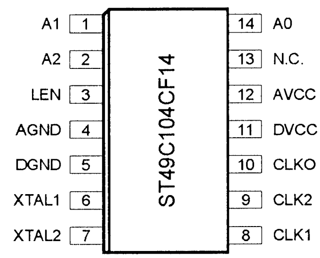
Printed August 3, 1995

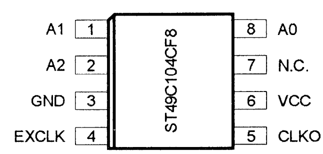
PREPROGRAMMED FREQUENCY GENERATOR

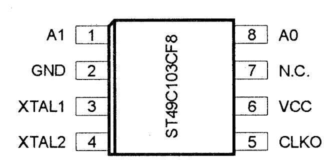
DESCRIPTION

The ST49C103 and ST49C104 are mask programmable monolithic analog CMOS devices designed to generate up to 8 single frequency outputs from a single input clock. The ST49C104 will provide eight different output frequencies and the ST49C103 will provide four different output frequencies. They are designed in a 1.2μ process to achieve 80 MHz.
The ST49C103 and ST49C104 are designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C104 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The latch enable pin is also mask programmable to be active high, active low or rising or falling edge sensitive.

SOIC Package







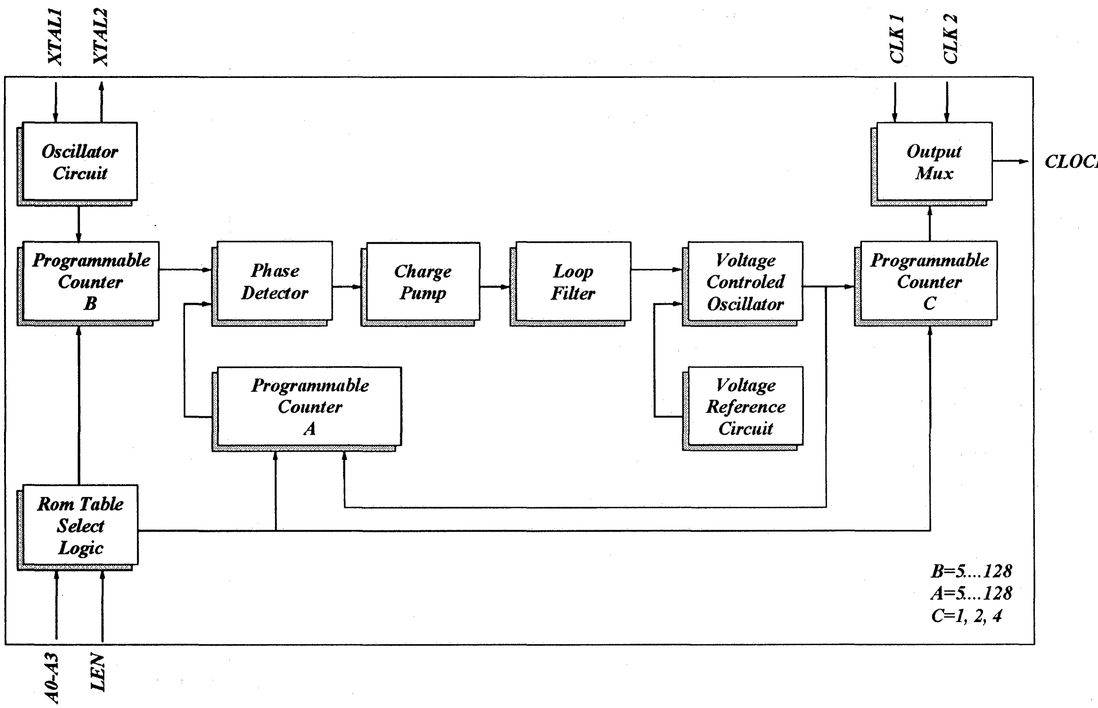
FEATURES

- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9103/104
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 or 14 pin DIP or SOIC package.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C103CP8	Plastic-DIP	0° C to +70° C
ST49C103CF8	SOIC	0° C to +70° C
ST49C104CP8	Plastic-DIP	0° C to +70° C
ST49C104CF8	SOIC	0° C to +70° C
ST49C104CP14	Plastic-DIP	0 ° C to +70° C
ST49C104CF14	SOIC	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C104 14 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
LEN	3*	I	Address latch enable input. To latch selected programmed clock output.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
XTAL1	6	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	O	Crystal output.
CLK1	8	I	External clock 1 input.
CLK2	9	I	External clock 2 input / output select.
CLKO	10	O	Programmed output clock.
DVCC	11	I	Digital supply voltage. Single +5 volts.
AVCC	12	I	Analog supply voltage. Single +5 volts.
N.C.	13		
A0	14	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

SYMBOL DESCRIPTION (ST49C104 8 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
GND	3	O	Digital ground.
EXCLK	4	I	External clock input. Internal phase locked loop reference clock .
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
N.C.	7		
A0	8	I	Frequency select address input 1.

* Has internal pull-up resistor on input

SYMBOL DESCRIPTION (ST49C103 8pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
GND	2	O	Digital ground.
XTAL1	3	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
N.C.	7		
A0	8	I	Frequency select address input 1.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047μF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C104 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C104 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B X C)

where A=1,2,3,.........127
B=8, 16, 32 ,64
C=1,2,4,8

MASK OPTIONS

The following mask options are provided for custom applications.

- Latch Enable can be edge triggered or level sensitive.
- Latch Enable can be active high or active low.
- Any frequency can be in any decoding position.
- CLK 1 and CLK 2 can be included in decoding table.
- CLK2 can control selection of either CLK 1 or the internal frequencies.

FEATURE	ST49C104 14-pin	ST49C104 8-pin	ST49C103 8-pin
8 output frequencies	X	X	
4 output frequencies			X
Programmable LEN pin	X	X	X
Clock input only		X	
Crystal or clock input	X		X
CLK1, CLK2 available for output mux	X		

Address latch (LEN)	State
ST49C104-1	Transparent for LEN high
ST49C104-2	Transparent for LEN high
ST49C104-3	Transparent for LEN low

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

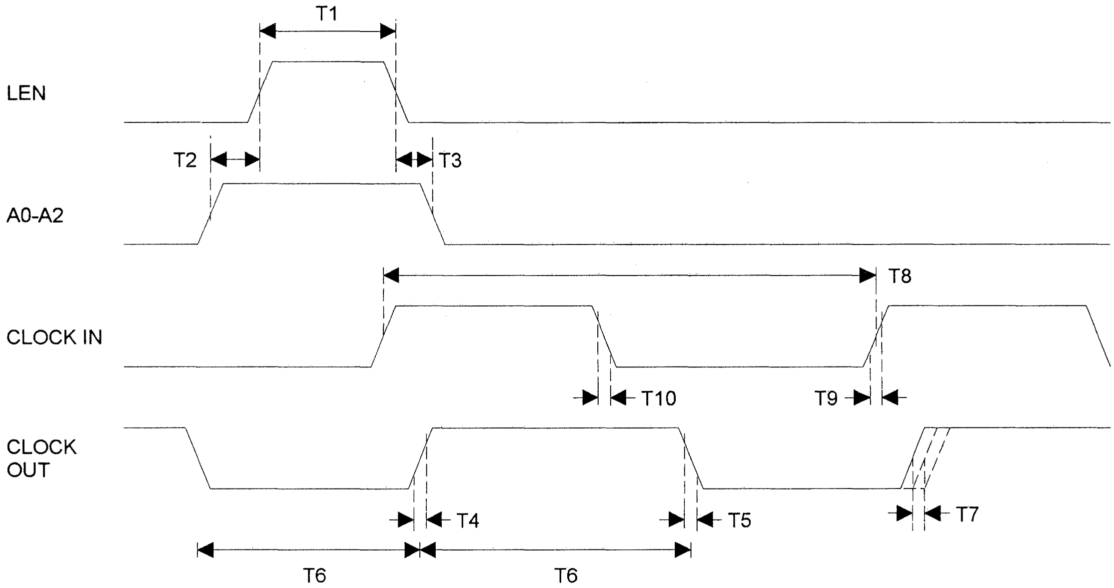
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	VIN=Vcc
I_{CC}	Operating current		30	50	mA	No load. DCLK=80MHz
R_{IN}	Input pull-up resistance	15	20	25	kΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1.5	3	ns	0.8V - 2.0V, 15 pF
T_5	Fall time		1	1.5	ns	2.0V - 0.8V, 15pF
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter 1 sigma		±0.5	±2	%	
T_7	Jitter absolute		±2	±5	%	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	

TIMING DIAGRAM



A2 A1 A0	ST49C104-1		ST49C104-2		ST49C104-5*		ST49C103**		ST49C104-6**	
	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NORMAL	ACTUAL	NOMINAL	ACTUAL
0 0 0	Xtal	Xtal	25.175	25.280	39.000	39.000	32.000	32.00	25.500	25.500
0 0 1	16.257	16.331	28.322	28.412	25.000	25.000	40.00	40.00	16.500	16.500
0 1 0	Clk2	Clk2	32.514	32.663	30.750	30.750	50.00	50.00	20.750	20.750
0 1 1	32.514	32.663	36.000	35.795	26.250	26.250	1.00	1.002	2.500	22.500
1 0 0	25.175	25.056	40.000	39.822	32.000	32.000	N/A		24.500	24.500
1 0 1	28.322	28.412	44.900	44.744	25.250	25.250	N/A		19.500	19.500
1 1 0	24.000	23.938	50.000	50.113	31.250	31.250	N/A		15.000	15.000
1 1 1	40.000	39.822	65.000	65.326	37.500	37.500	N/A		14.000	14.000

Input clock frequency = 14.318 MHz
* Input clock frequency = 16.0 MHz
** Input clock frequency = 8.0 MHz

ST49C106

Printed August 3, 1995

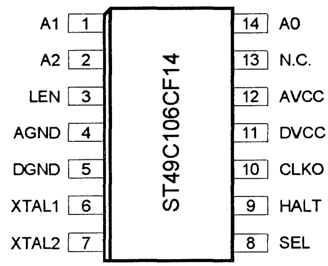
PREPROGRAMMED FREQUENCY GENERATOR

DESCRIPTION

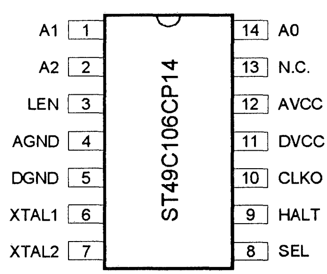
The ST49C106 is a mask programmable monolithic analog CMOS device designed to generate up to 8 single frequency outputs from a single input clock. The ST49C106 is designed in a 1.2μ process to achieve 80 MHz.

The ST49C106 is designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C106 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The ST49C106 contains de-glitch circuit so that full clock cycles are provided whenever the HALT pin stops or starts the output clock.

SOIC Package



Plastic-DIP package



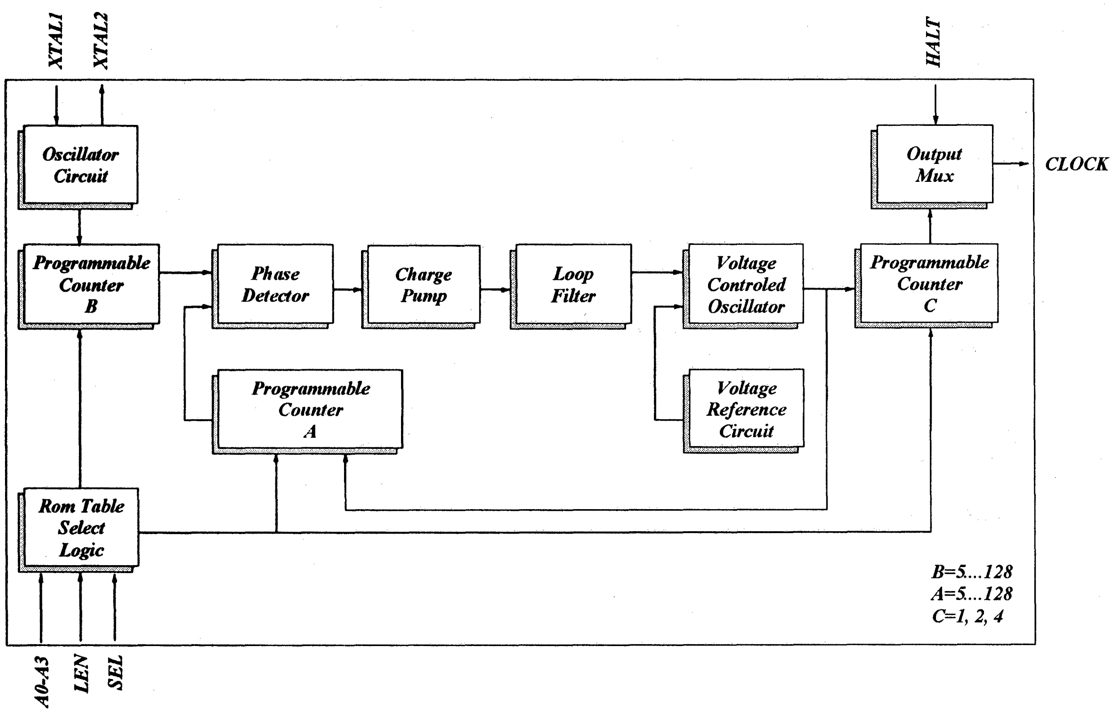
FEATURES

- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9106-14
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 14 pin DIP or SOIC package.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C106CP14	Plastic-DIP	0 ° C to +70° C
ST49C106CF14	SOIC	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
LEN	3*	I	Address latch enable input. To latch selected programmed clock output.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
XTAL1	6	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	O	Crystal output.
SEL	8	I	Clock level select / CLK1. When HALT is asserted, SEL selects whether the clock is high or low. This level must be selected before the clock is halted. SEL pin can be used as an xternal clock input when HALT is active.
HALT	9	I	Start / Stop output clock.
CLKO	10	O	Programmed output clock.
DVCC	11	I	Digital supply voltage. Single +5 volts.
AVCC	12	I	Analog supply voltage. Single +5 volts.
A0	14	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C106 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C106 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B X C)

where A=1,2,3,.........127
B=8, 16, 32 ,64
C=1,2,4,8

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	VIN=Vcc
I_{CC}	Operating current		20	40	mA	No load. DCLK=80MHz
R_{IN}	Input pull-up resistance	15	20	25	kΩ	

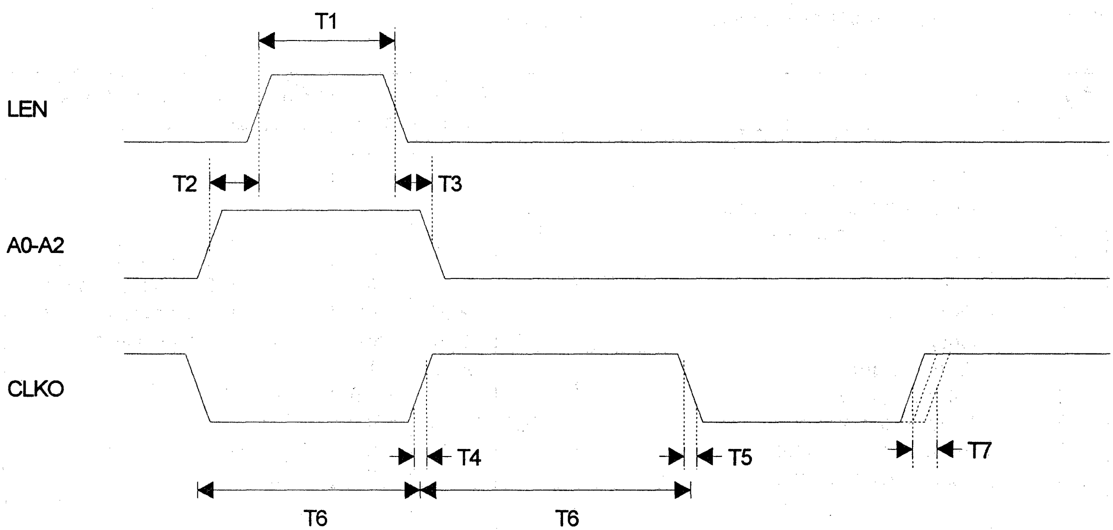
AC ELECTRICAL CHARACTERISTICS

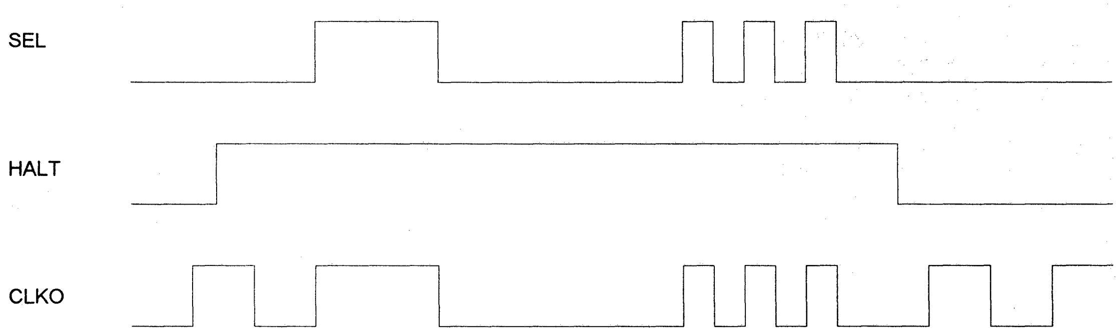
T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1.5	3	ns	0.8V - 2.0V, 15pF
T_5	Fall time		1.5	3	ns	2.0V - 0.8V, 15pF
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter 1 sigma		±0.5	±0.2	%	
T_7	Jitter absolute		±0.2	±0.5	%	
T_8	Input frequency	14.318		32	Mhz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	

A2 A1 A0	ST49C106-5* NOMINAL	ST49C106-5* ACTUAL
0 0 0	39.000	39.000
0 0 1	25.000	25.000
0 1 0	30.750	30.750
0 1 1	26.250	26.250
1 0 0	32.000	32.000
1 0 1	25.250	25.250
1 1 0	31.250	31.250
1 1 1	37.500	37.500

TIMING DIAGRAM





STARTECH
An EXAR Company

ST49C107

Printed August 3, 1995

PREPROGRAMMED CPU MOTHER BOARD FREQUENCY GENERATOR

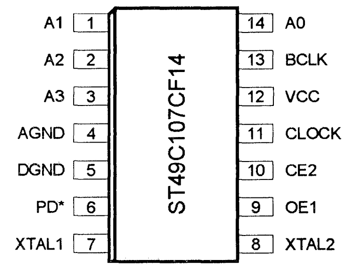
1

DESCRIPTION

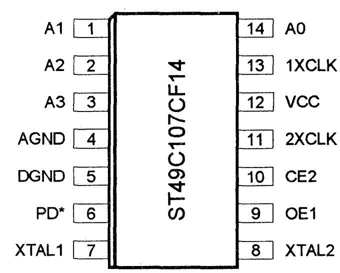
The ST49C107 is a mask programmable monolithic analog CMOS device designed to generate two simultaneous clocks. One clock is either the BCLK (buffered reference clock) or programmable. The other clock (called CLOCK or 2XCLOCK in different versions) is programmable only. The output frequency can vary from 2 to 100MHz, with up to 16 single selectable preprogrammed frequencies stored in internal ROM.

The ST49C107 is designed to replace existing CPU mother board clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via four address lines (two address lines for ST49C107-05).

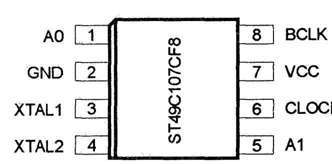
SOIC Package



ST49C107CF-03



ST49C107CF-04



ST49C107CF-05

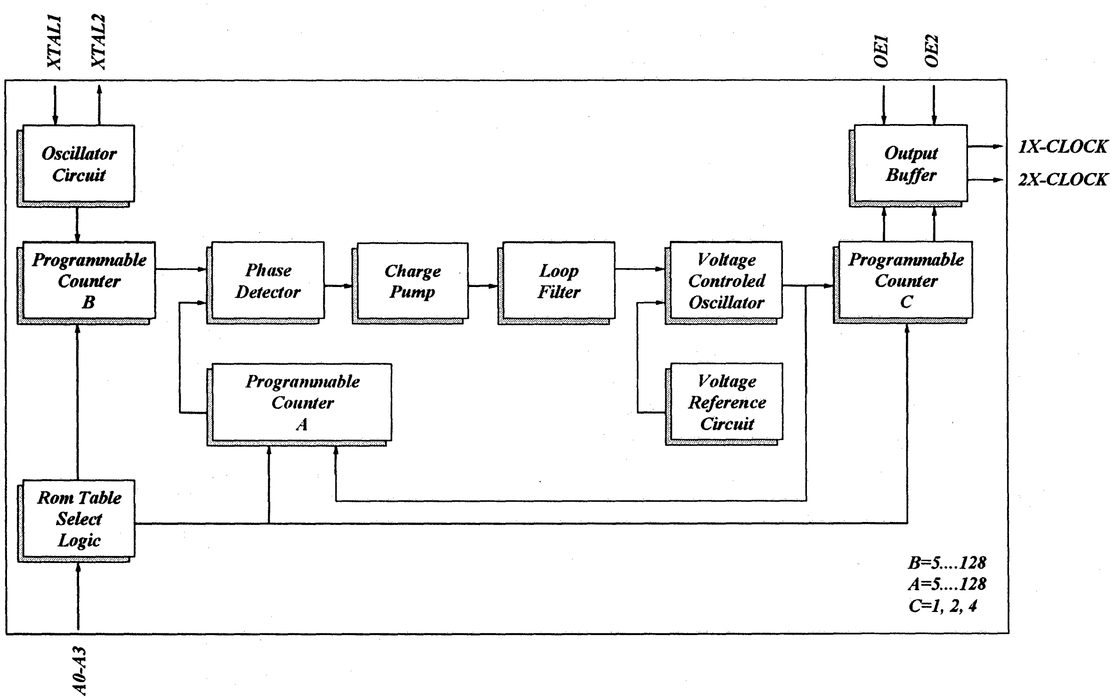
FEATURES

- Provides reference clock and synthesized clock
- 5 to 32MHz input reference frequency
- Pin-to-pin compatible to Avasem AV9107
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- Up to 16 frequencies stored internally
- 8/14 pin DIP or SOIC package.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C107CP8	Plastic-DIP	0 ° C to +70° C
ST49C107CF8	SOIC	0° C to +70° C
ST49C107CP14	Plastic-DIP	0 ° C to +70° C
ST49C107CF14	SOIC	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C107-03 package)

Symbol	Pin	Signal Type	Pin Description
A1	1*	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
A3	3*	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6*	I	Power-Down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9*	I	Buffered clock Output Enable (Active high). BCLK output is three stated when this pin is low.
OE2	10*	I	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
CLOCK	11	O	Programmed output clock.
VCC	12	I	Positive supply voltage. Single +5 volts.
BCLK	13	O	Buffered crystal clock output.
A0	14*	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

SYMBOL DESCRIPTION (ST49C107-04 package)

Symbol	Pin	Signal Type	Pin Description
A1	1*	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
A3	3*	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6*	I	Power-Down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9*	I	1X-CLOCK Output Enable (Active high). 1X-CLOCK output is three stated when this pin is low.
OE2	10*	I	2X-CLOCK Output Enable (Active high). 2X-CLOCK output is three stated when this pin is low.
2XCLK	11	O	Programmed output clock.
VCC	12	I	Positive supply voltage. Single +5 volts.
1XCLK	13	O	2X-CLOCK Divide-by-two output.
A0	14*	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

SYMBOL DESCRIPTION (ST49C107-05 package)

Symbol	Pin	Signal Type	Pin Description
A0	1	I	Frequency select address input 1.
A1	5	I	Frequency select address input 2.
GND	2	O	Supply ground.
XTAL1	3	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLOCK	6	O	Programmed output clock.
VCC	7	I	Positive supply voltage. Single +5 volts.
BCLK	8	O	Buffered crystal clock output.

EXTERNAL CLOCK CONNECTION
To minimize the noise pickup , it is recommended to connect 0.047μF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C107 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C107 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B X C)

where A=5, 6, 7,.........128
B=5, 6, 7,.........128
C=1,2

For proper output frequency, the ST49C107 can accept a reference frequency from 5 - 32 MHz and divider ratio up to 15.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-10	µA	Exc. crystal input
I_{IH}	Input high current			1	µA	VIN=Vcc
I_{CC}	Operating current		45	55	mA	No load. CLOCK=100MHz
I_{SB}	Standby current		25		µA	No load.
R_{IN}	Input pull-up resistance	500	900	1300	kΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	1X, 2X-CLOCK rise time		1	2	ns	C_L=20pF 0.8V - 2.0V
T_2	1X, 2X-CLOCK fall time		1	2	ns	C_L=20pF 2.0V - 0.8V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±3	±5	%	
T	Input frequency	2		32	MHz	
T_7	Buffered clock rise time			20	ns	
T_8	Buffered clock fall time			20	ns	

CLOCK OUTPUT TABLE FOR ST49C107-03 (using 14.318 MHz input. All frequencies in MHz).

A3 A2 A1 A0	CLOCK
0 0 0 0	16.00
0 0 0 1	40.01
0 0 1 0	50.11
0 0 1 1	80.01
0 1 0 0	66.58
0 1 0 1	100.23
0 1 1 0	8.02
0 1 1 1	4.01
1 0 0 0	8.02
1 0 0 1	20.00
1 0 1 0	25.06
1 0 1 1	40.01
1 1 0 0	33.29
1 1 0 1	50.11
1 1 1 0	4.01
1 1 1 1	2.05

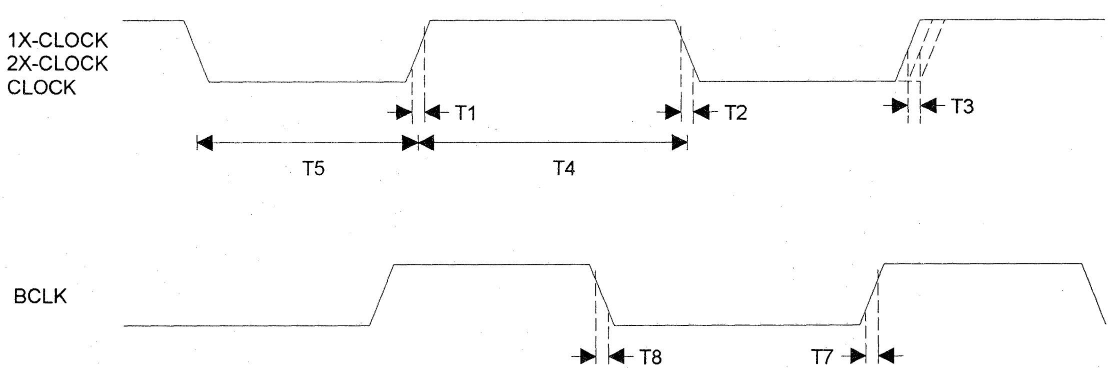
CLOCK OUTPUT TABLE FOR ST49C107-04 (using 14.318 MHz input. All frequencies in MHz).

A3 A2 A1 A0	2X-CLOCK	CLOCK
0 0 0 0	80.02	40.01
0 0 0 1	66.62	33.31
0 0 1 0	50.11	25.06
0 0 1 1	40.01	20.00
0 1 0 0	100.23	50.11
0 1 0 1	33.31	16.66
0 1 1 0	32.01	16.00
0 1 1 1	25.06	12.47
1 0 0 0	64.02	32.01
1 0 0 1	2X-Input	1X-Input
1 0 1 0	3X-Input	1.5X-Input
1 0 1 1	8X-Input	4X-Input
1 1 0 0	0.5X-Input	0.25X-Input
1 1 0 1	0.25X-Input	0.125X-Input
1 1 1 0	120.00	60.00
1 1 1 1	129.96	64.98

CLOCK OUTPUT TABLE FOR ST49C107-05 (using 14.318 MHz input. All frequencies in MHz).

A1 A0	CLOCK
0 0	40.01
0 1	50.11
1 0	66.61
1 1	80.01

TIMING DIAGRAM



STARTECH
An EXAR Company

ST49C154

Printed August 3, 1995

PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C154 is a monolithic analog CMOS device designed to generate upto six simultaneous clock outputs for mother board and disk drive applications. It is designed in a 1.2μ process to achieve 100 MHz operation with low clock jitter.

The ST49C154 may be used to replace existing BUS, I/O, and disk drive clocks generated from individual oscillators so that board space and number of oscillators are reduced. The high speed analog CMOS phase locked loops use the 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).

The ST49C154 is metal mask programmable to provide any custom set of CPUCLK frequencies. The programmed clock outputs are selectable via four address lines for 1XCLK / 2XCLK outputs. The CPU clock makes glitch-free transitions from one frequency to the next and follows Intel's processors input clock specification.

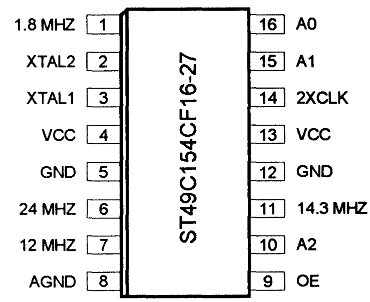
FEATURES

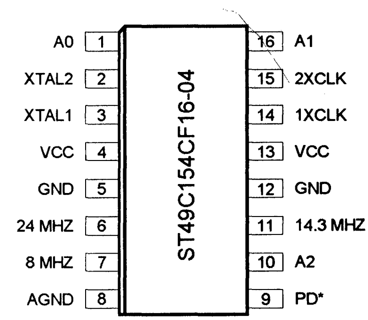
- Pin -to-pin compatible to AV9154
- Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Skew controlled 2X and 1X clocks
- Programmable analog phase locked loop
- High speed (up to 100 MHz output)
- Low power single 3V / 5V CMOS technology
- 16 pin dip or SOIC package

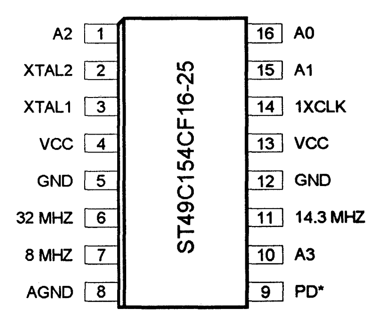
ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C154CP16-xx	Plastic-DIP	0° C to +70° C
ST49C154CF16-xx	SOIC	0° C to +70° C

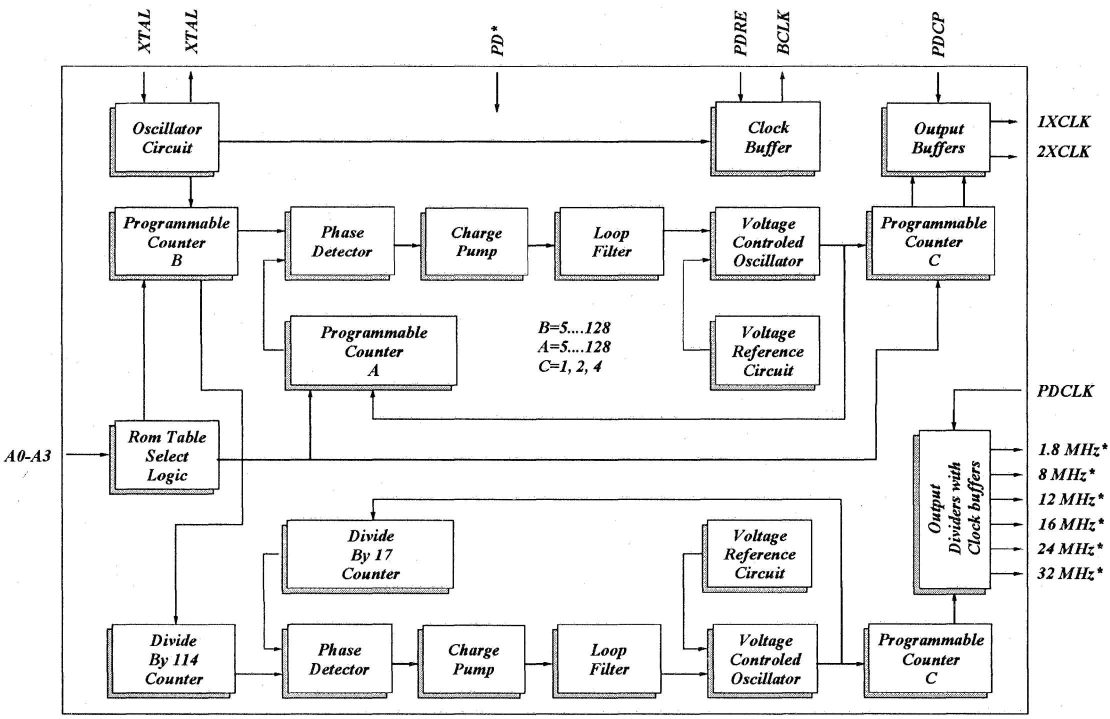
SOIC Package







BLOCK DIAGRAM



* *a Subset of these frequencies is available in each option*

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL2	2	O	Crystal output.
XTAL1	3	I	Crystal or External clock input.
VCC	4,13	I	Digital supply voltage. Single +3 / +5 volts.
GND	5,12	O	Digital signal ground.
AGND	8	O	Analog ground.
A0	*	I	CPU clock frequency select address 0. ST49C154-4, -6, -16, -26, -60 > pin 1. ST49C154-5, -10, -25, -27 > pin 16.
A1	*	I	CPU clock frequency select address 1. ST49C154-4, -6, -16, -26, -60 > pin 16. ST49C154-5, -10, -25, -27 > pin 15.
A2	*	I	CPU clock frequency select address 2. ST49C154-4, -26, -27 > pin 10. ST49C154-5, -25 > pin 1. ST49C154-6, -16, -60 > pin 15.
A3	*	I	CPU clock frequency select address 3. ST49C154-5, -25 > pin 10.
PD*	*	I	Power down (active low). Shuts off entire chip when low. ST49C154-4, -5, -25, -26 > pin 9.
OE	*	I	Output enable (active high / internal pull-up). Three states outputs when low. ST49C154-27 > pin 9.
PDCPU	*	I	Power down (active high). Shuts off 2XCLK output when high. ST49C154-6, -16, -60 > pin 10.
PDREF	*	I	Power down (active high). Shuts off the 14.318 MHz reference clock output. ST49C154-6, -16, -60 > pin 9.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
PDCLK*	*	I	Power down (active low). Shuts off the 1.846 MHz, 8 MHz, 16 MHz, and 24 MHz clock outputs. ST49C154-10 > pin 9.
1XCLK	*	O	Selectable CPU clock output. ST49C154-4, -5, -6, -10, -16, -25, -60 > pin 14.
2XCLK	*	O	Selectable 2X-CPU clock output. ST49C154-4, -6, -60 > pin 15. ST49C154-27 > pin 14.
1.846 MHz	*	O	1.846 MHz clock output. ST49C154-10 > pin 7. ST49C154-27 > pin 1.
8 MHz	*	O	8 MHz clock output. ST49C154-4, -5, -25 > pin 7. ST49C154-10 > pin 1.
12 MHz	*	O	12 MHz clock output. ST49C154-16, -26, -27 > pin 7.
14.318 MHz	*	O	14.318 MHz reference clock output. ST49C154-4, -5, -6, -16, -25, -27, -60 > pin 11. ST49C154-10 > pin 10.
16 MHz	*	O	16 MHz clock output. ST49C154-5, -10 > pin 6.
24 MHz	*	O	24 MHz clock output. ST49C154-4, -6, -16, -26, -27, -60 > pin 6. ST49C154-10 > pin 11.
32 MHz	*	O	32 MHz clock output. ST49C154-25 > pin 6.

SYMBOL DESCRIPTION (ST49C154-22 with 25 MHz reference frequency)

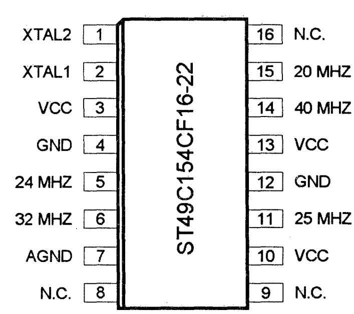
Symbol	Pin	Signal Type	Pin Description
128 kHz	*	O	128 kHz clock output. ST49C154-6, -60 > pin 7.
XTAL2	2	O	Crystal output.
XTAL1	1	I	Crystal or External clock input.
VCC	3,10,13	I	Digital supply voltage. Single +3 / +5 volts.
GND	4,12	O	Digital signal ground.
AGND	7	O	Analog ground.
20 MHz	15	O	20 MHz clock output.
24 MHz	5	O	24 MHz clock output.
25 MHz	11	O	25 MHz clock output.
32 MHz	6	O	32 MHz clock output.
40 MHz	14	O	40 MHz clock output.

ST49C154 ACTUAL OUTPUT FREQUENCIES (using 14.318 MHz input. All frequencies in MHz).

A3 A2 A1 A0	CLK -5	CLK -6	CLK -10	CLK -16	CLK -25	CLK -27	CLK -60
0 0 0 0	2.15	16.11	PDCPU	16.11	2.15	75.17	8.182
0 0 0 1	8.18	20.05	40.09	20.05	8.18	31.94	16.11
0 0 1 0	16.11	25.06	50.11	25.06	16.11	60.136*	20.05
0 0 1 1	20.05	33.24	66.48*	33.41	20.05	40.09	25.06
0 1 0 0	25.06	40.09		40.09	25.06	50.11	33.24
0 1 0 1	33.24	50.11		50.11	33.24	66.48*	40.09
0 1 1 0	40.09	66.48		66.48*	40.09	80.18*	50.11
0 1 1 1	50.11	80.18*		80.18*	50.11	51.90	66.48*
1 0 0 0	4.30				4.30		
1 0 0 1	16.11				16.11		
1 0 1 0	32.22				32.22		
1 0 1 1	40.09				40.09		
1 1 0 0	50.11				50.11		
1 1 0 1	66.48*				66.48*		
1 1 1 0	80.18*				80.18*		
1 1 1 1	100.23*				100.23*		
I/O Clocks	8.00 14.318 16.00	0.128 14.318 24.00	1.846 8.00 14.318 16.00 24.00	12.00 14.318 24.00	8.00 14.318 32.01	1.846 12.00 14.318 24.00	0.128 14.318 24.00

ST49C154-04, -26 ACTUAL OUTPUT FREQUENCIES (using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0	2XCLK	1XCLK
0 0 0	100.23*	50.11
0 0 1	80.18*	40.09
0 1 0	66.48*	33.24
0 1 1	50.11	25.06
1 0 0	40.09	20.05
1 0 1	32.22	16.11
1 1 0	24.23	12.12
1 1 1	15.75	7.88
I/O Clocks	8.00, 24.00 14.318	12.00**



*These selections will only operate at 5V.
** ST49C154-26 only

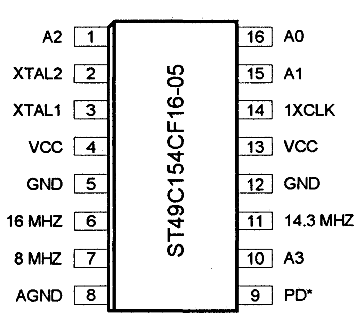
ABSOLUTE MAXIMUM RATINGS

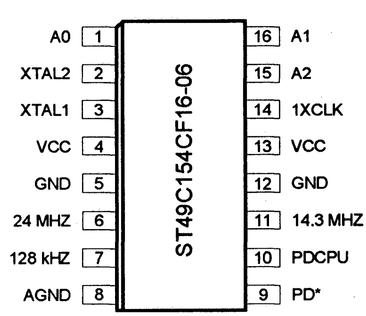
Supply voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = -8.0 mA
I_{IL}	Input low current			-5	µA	VIN=0V
I_{IH}	Input high current			5	µA	VIN=Vcc
I_{CC}	Operating current		45	60	mA	No load.
I_{SB}	Stand by current		15		µA	Power down.
I_{SC}	Short circuit current	25	40		mA	Each output clock
C_I	Input capacitance		10		pF	Except Xtal1,2
C_L	Load capacitance		20		pF	

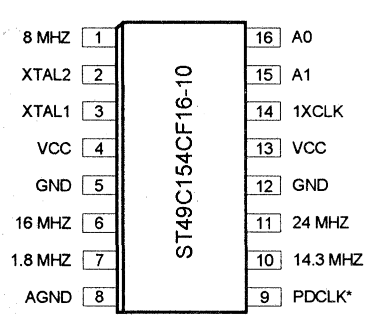


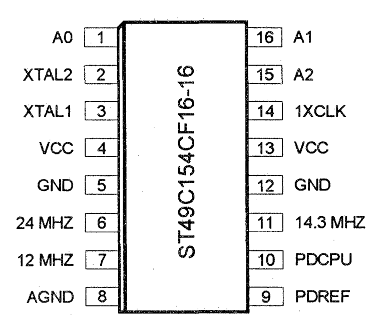


AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_4	Rise time		1	2	ns	15pF load 0.8 to 2.0V
T_5	Fall time		1	2	ns	15pF load 0.8 to 2.0V
T_6	Duty cycle	40	48/52	60	%	15pF load
T_R	Reference clock duty cycle	40	48/52	55	%	
T_T	Frequency transition time			20	ms	From 2-20MHz
T_P	Power up time		15		ms	From off to 50MHz
T_I	Input frequency		14.318		MHz	
T_{JIS}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T_{JA}	Jitter, absolute		±2	±5	%	All frequencies
T_8	Input frequency		14.318		MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_E	Enable pulse width	20			ns	
T_S	Clock skew berween 1XCLK and 2XCLK		0.5	1.0	ns	





ST49C154

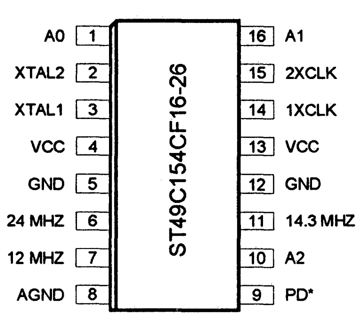
ABSOLUTE MAXIMUM RATINGS

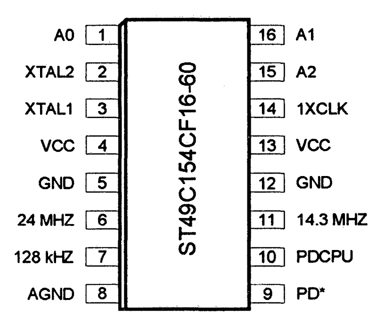
Supply voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.15VCC	V	
V_{IH}	Input high level	0.7VCC			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	VCC-0.4V			V	I_{OH} = -4.0 mA
I_{IL}	Input low current	-5		-5	µA	VIN=0
I_{IH}	Input high current	-5		5	µA	VIN=Vcc
I_{CC}	Operating current		20		mA	No load.
I_{SB}	Stand by current		15		µA	Power down.
C_I	Input capacitance			10	pF	Except Xtal1,2
C_L	Load capacitance		30		pF	



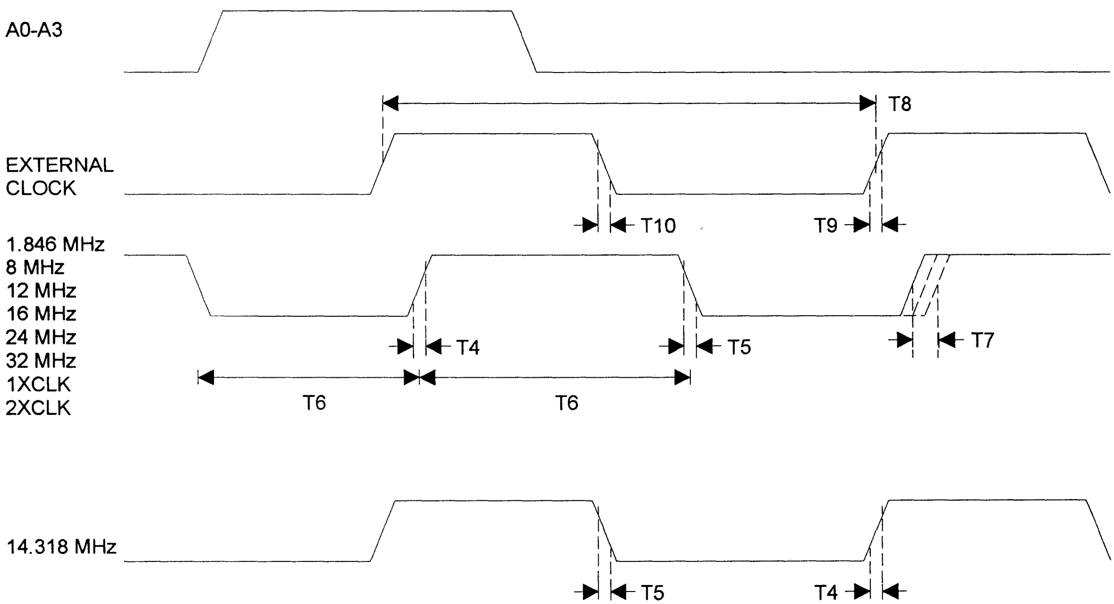


AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_4	Rise time			4	ns	15pF load.
T_5	Fall time			4	ns	15pF load.
T_6	Duty cycle	40	48/52	60	%	15pF load.
T_T	Frequency transition time			20	ms	From 2-20MHz
T_P	Power up time		15		ms	From off to 50MHz
T_F	Output frequency	2		50	MHz	
T_8	Input frequency	2	14.318	32	MHz	
T_{IF}	Input clock rise/fall time			20	ns	
T_{JIS}	Jitter, 1 sigma		±0.5	±2	%	All frequencies
T_{JA}	Jitter, absolute		±3	±5	%	All frequencies
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_E	Enable pulse width	20			ns	

TIMING DIAGRAM



ST49C155

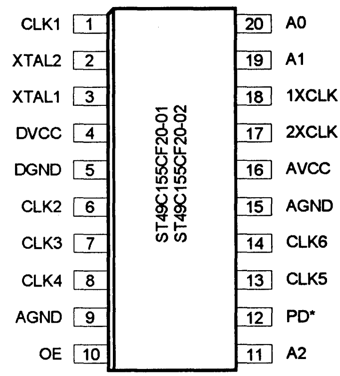
Printed August 3, 1995

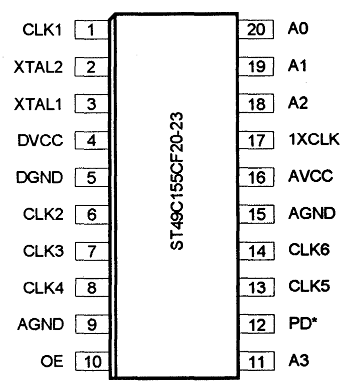
PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C155 is a monolithic analog CMOS device designed to generate eight simultaneous clock outputs for mother board applications. It is designed in a 1.2μ process to achieve 100 MHz operation with low clock jitter.
The ST49C155 may be used to replace existing BUS and I/O clocks generated from individual oscillators so that board space and number of oscillators are reduced. The high speed analog CMOS phase locked loops use the 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).
The ST49C155 is metal mask programmable to provide any custom set of CPUCLK frequencies. The programmed clock outputs are selectable via four address lines for 1XCLK / 2XCLK outputs.

SOIC Package





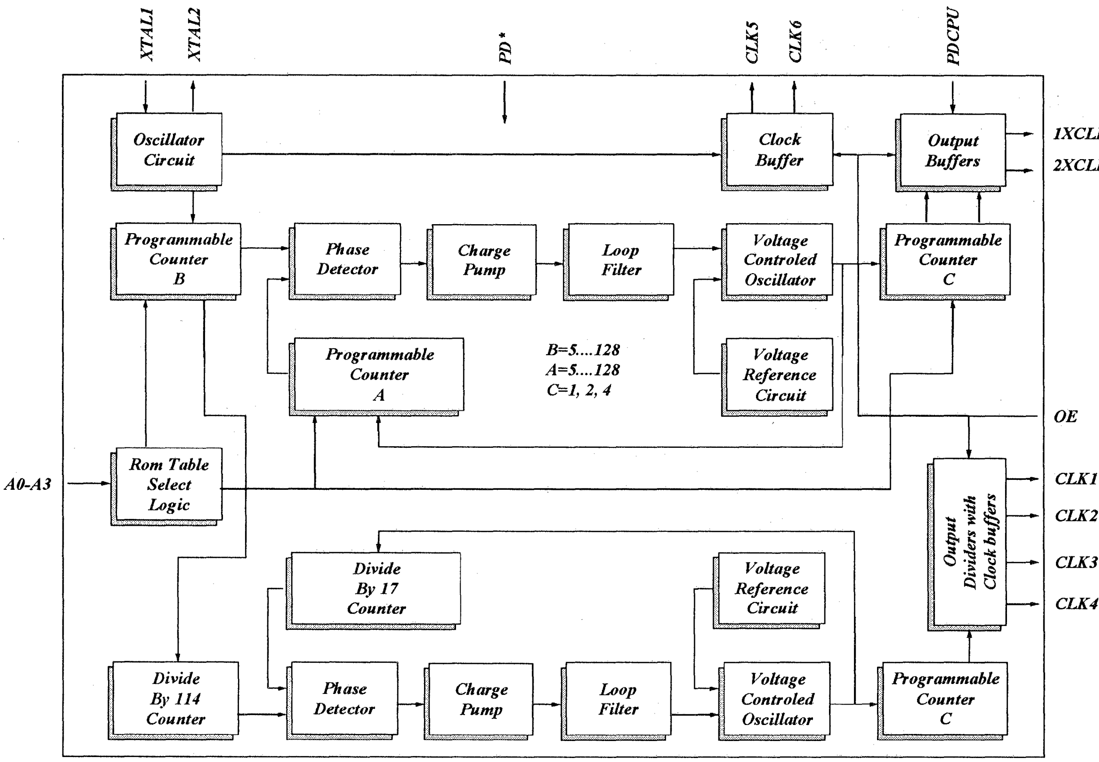
FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to AV9155
- Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Skew controlled 2X and 1X clocks
- Programmable analog phase locked loop
- High speed (up to 100 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C155CP20-xx	Plastic-DIP	0° C to +70° C
ST49C155CF20-xx	SOIC	0° C to +70° C
ST49C155CJ20-xx	PLCC	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C155-01/ -02)

Symbol	Pin	Signal Type	Pin Description
CLK1	1	O	1.8432 MHz clock output.
XTAL2	2	O	Crystal output.
XTAL1	3	I	Crystal or External clock input.
DVCC	4	I	Digital supply voltage. Single +5 volts.
DGND	5	O	Digital signal ground.
CLK2	6	O	16 MHz (ST49C155-01) or 32 MHz (ST49C155-02) clock output.
CLK3	7	O	24 MHz floppy disk clock output.
CLK4	8	O	12 MHz keyboard clock output.
AGND	9	O	Analog ground.
OE	10*	O	Output Enable (active high). Low on this pin sets all the outputs to three state mode.
A2	11	I	CPU clock frequency select address 2.
PD*	12*	I	Power down (active low). Shuts off entire chip when low.
CLK5	13	O	14.318 MHz reference clock output.
CLK6	14	O	14.318 MHz reference clock output.
AGND	15	O	Analog ground.
AVCC	16	I	Analog supply voltage. Single +5 volts.
2XCLK	17	I	2X CPU clock output.
1XCLK	18	I	1X CPU clock output.
A1	19	I	CPU clock frequency select address 1.
A0	20	I	CPU clock frequency select address 0.

*Have internal pull-up resistor on inputs

SYMBOL DESCRIPTION (ST49C155-03)

Symbol	Pin	Signal Type	Pin Description
CLK1	1	O	6 MHz clock output.
XTAL2	2	O	Crystal output.
XTAL1	3	I	Crystal or External clock input.
DVCC	4	I	Digital supply voltage. Single +5 volts.
DGND	5	O	Digital signal ground.
CLK2	6	O	24 MHz floppy disk clock output.
CLK3	7	O	16 MHz bus clock output.
CLK4	8	O	8 MHz keyboard clock output.
AGND	9	O	Analog ground.
OE	10*	O	Output Enable (active high). Low on this pin sets all the outputs to three state mode.
A3	11	I	CPU clock frequency select address 3.
PD*	12*	I	Power down (active low). Shuts off entire chip when low.
CLK5	13	O	14.318 MHz reference clock output.
CLK6	14	O	14.318 MHz reference clock output.
AGND	15	O	Analog signal ground.
AVCC	16	I	Analog supply voltage. Single +5 volts.
1XCLK	17	I	CPU clock output.
A2	18	I	CPU clock frequency select address 2.
A1	19	I	CPU clock frequency select address 1.
A0	20	I	CPU clock frequency select address 0.

*Have internal pull-up resistor on inputs

CPU CLOCK TABLE FOR ST49C155-01, -02 (using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0	2XCLK	1XCLK
0 0 0	8	4
0 0 1	16	8
0 1 0	32	16
0 1 1	40	20
1 0 0	50	25
1 0 1	66.66	33.33
1 1 0	80	40
1 1 1	100	50

ST49C155-23 (using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0	2XCLK	1XCLK
0 0 0	75	37.5
0 0 1	32	16
0 1 0	60	30
0 1 1	40	20
1 0 0	50	25
1 0 1	66.66	33.33
1 1 0	80	40
1 1 1	52	26

ST49C155-03 (using 14.318 MHz input. All frequencies in MHz).

A3 A2 A1 A0	1XCLK
0 0 0 0	16
0 0 0 1	40
0 0 1 0	50
0 0 1 1	80
0 1 0 0	66.66
0 1 0 1	100
0 1 1 0	8
0 1 1 1	4
1 0 0 0	8
1 0 0 1	20
1 0 1 0	25
1 0 1 1	40
1 1 0 0	33.33
1 1 0 1	50
1 1 1 0	4
1 1 1 1	2

PERIPHERAL CLOCK TABLE FOR ST49C155-01

CLK1	CLK2	CLK3	CLK4
1.8432	16	24	12

PERIPHERAL CLOCK TABLE FOR ST49C155-02

CLK1	CLK2	CLK3	CLK4
1.8432	32	24	12

PERIPHERAL CLOCK TABLE FOR ST49C155-03

CLK1	CLK2	CLK3	CLK4
6	24	16	8

PERIPHERAL CLOCK TABLE FOR ST49C155-23

CLK1	CLK2	CLK3	CLK4
1.843	16	24	12

ACTUAL OUTPUT FREQUENCIES

CPU CLOCK TABLE FOR ST49C155-01, -02

A2 A1 A0	2XCLK	1XCLK
0 0 0	7.5	3.75
0 0 1	15.51	7.76
0 1 0	32.22	16.11
0 1 1	40.09	20.05
1 0 0	50.11	25.06
1 0 1	66.82	33.41
1 1 0	80.18	40.09
1 1 1	100.23	50.11

CPU CLOCK TABLE FOR ST49C155-03

A3 A2 A1 A0	1XCLK
0 0 0 0	15.51
0 0 0 1	40.09
0 0 1 0	50.11
0 0 1 1	80.18
0 1 0 0	66.82
0 1 0 1	100.23
0 1 1 0	7.58
0 1 1 1	4.30
1 0 0 0	7.76
1 0 0 1	20.05
1 0 1 0	25.06
1 0 1 1	40.09
1 1 0 0	33.41
1 1 0 1	50.11
1 1 1 0	3.79
1 1 1 1	2.15

CPU CLOCK TABLE FOR ST49C155-23

A2 A1 A0	2XCLK	1XCLK
0 0 0	75.170	37.585
0 0 1	31.940	15.970
0 1 0	60.136	30.068
0 1 1	40.090	20.045
1 0 0	50.113	25.057
1 0 1	66.476	33.238
1 1 0	80.181	40.091
1 1 1	51.903	25.952

PERIPHERAL CLOCK TABLE FOR ST49C155-01

CLK1	CLK2	CLK3	CLK4
1.8432	16	23.71	11.86

PERIPHERAL CLOCK TABLE FOR ST49C155-02

CLK1	CLK2	CLK3	CLK4
1.8432	32.01	24	12

PERIPHERAL CLOCK TABLE FOR ST49C155-03

CLK1	CLK2	CLK3	CLK4
6	24	16	8

PERIPHERAL CLOCK TABLE FOR ST49C155-23

CLK1	CLK2	CLK3	CLK4
1.843	16	24	12

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-1	mA	Except pins 2, 10, 12
I_{IH}	Input high current			1	mA	VIN=Vcc
I_{CC}	Operating current		45	65	mA	No load.
R_{IN}	Internal pull-up resistance		680		kΩ	Pins 10,12

FREQUENCY TRANSITIONS

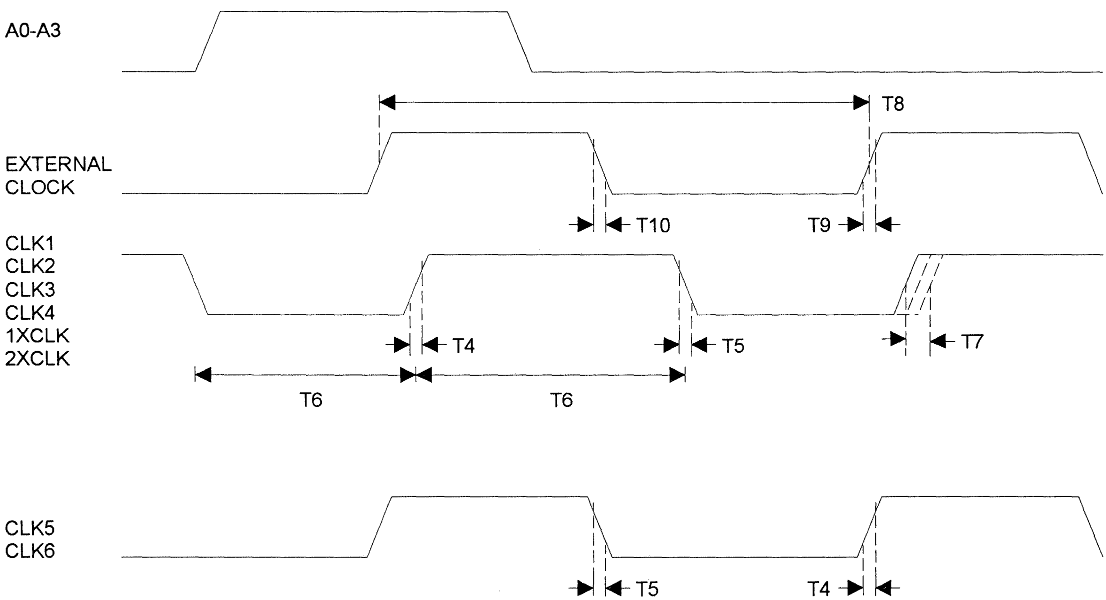
The ST49C155 is designed to provide smooth, glitch-free frequency transitions on the 1XCLK and 2XCLK clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_4	Rise time		1	2	ns	0.8V - 2.0V, 15pF
T_5	Fall time		1	2	ns	2.0V - 0.8V, 15pF
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	40	48/52	55	%	Vcc/2 switch point
T_7	Jitter 1 sigma		±0.5	±2	%	
T_7	Jitter absolute		±2	±5	%	
T_8	Input frequency		14.318		MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	

TIMING DIAGRAM



STARTECH
An EXAR Company

ST49C158

Printed August 3, 1995

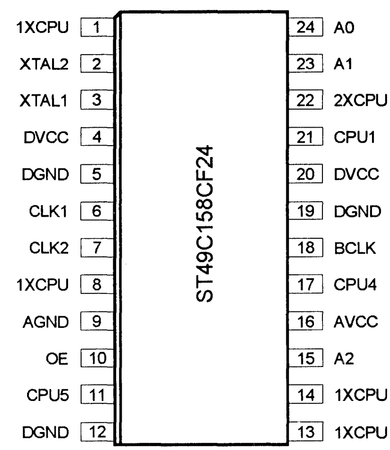
1

PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

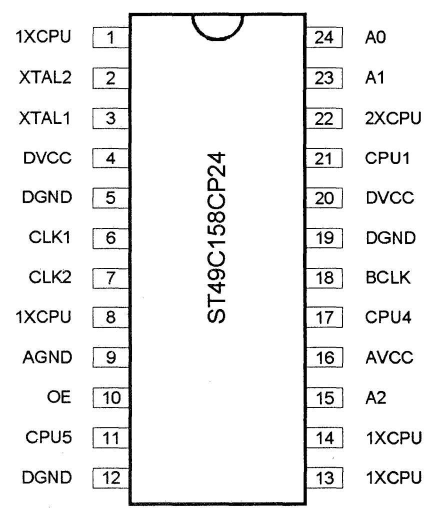
GENERAL DESCRIPTION

The ST49C158 is a monolithic analog CMOS device designed to generate eight simultaneous clock outputs for mother board and green PC applications. It is designed in a 1.2μ process to achieve 100 MHz operation with low clock jitter. The CPU and 2XCPU outputs are skew controlled within 250 psec.
The ST49C158 is designed for desktop and notebook PC's and supports Energy Star PC's. The ST49C158 can accept 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).
The ST49C158 is metal mask programmable to provide any custom set of 2XCPU frequencies. The programmed clock outputs are selectable via three address lines for CPU clocks.

SOIC Package



DIP Package



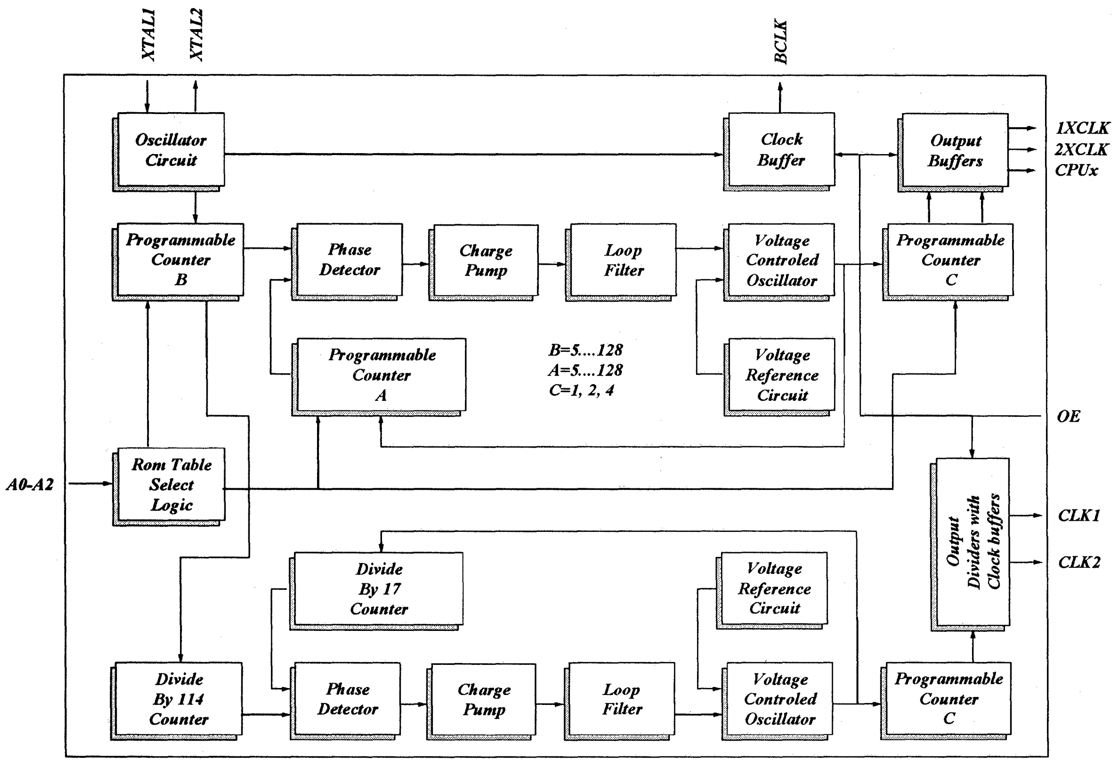
FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS9158
- Compatible with 286, 386, and 486 CPUs
- Skew controlled 2X and 1X CPU clocks
- Programmable analog phase locked loop
- High speed (up to 100 MHz output)
- Low power single 5V CMOS technology
- Smooth and glitch-free clock transitions
- 24 pin PDIP or SOIC package

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C158CP24	Plastic-DIP	0° C to +70° C
ST49C158CF24	SOIC	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
1XCPU	1	O	1X-CPU clock output.
XTAL2	2	O	Crystal output.
XTAL1	3	I	Crystal or External clock input.
DVCC	4	I	Digital supply voltage. Single +5 volts.
DGND	5	O	Digital signal ground.
CLK1	6	O	Fixed clock output.
CLK2	7	O	Fixed clock output.
1XCPU	8	O	1X-CPU clock output.
AGND	9	O	Analog ground.
OE	10*	O	Output Enable (active high). Low on this pin sets all of the programmable outputs to three state mode.
CPU5	11	O	1X or 2X CPU clock output.
DGND	12	O	Digital signal ground.
1XCPU	13	O	1X CPU clock output.
1XCPU	14	O	1X CPU clock output.
A2	15*	I	1X and 2X CPU clock frequency select address 2.
AVCC	16	I	Analog supply voltage. Single +5 volts.
CPU4	17	O	1X or 2X CPU clock output.
BCLK	18	O	Buffered 14.31818 MHz clock output.
DGND	19	O	Digital signal ground.
DVCC	20	I	Digital supply voltage. Single +5 volts.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CPU1	21	I	1X or 2X CPU clock output.
2XCPU	22	I	2X-CPU clock output.
A1	23*	I	1X and 2X CPU clock frequency select address 1.
A0	24*	I	CPU clock frequency select address 0.

*Have internal pull-up resistor on inputs

ACTUAL OUTPUT FREQUENCIES

CPU CLOCK TABLE FOR ST49C158-03 (using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0	2XCPU	CPU 2, 3,6,7	CPU 1, 4, 5
0 0 0	32.00	16.00	16
0 0 1	32.00	16.00	32
0 1 0	32.00	16.00	16
0 1 1	32.00	16.00	32
1 0 0	50.00	25.00	25
1 0 1	50.00	25.00	50
1 1 0	66.67	33.33	33.33
1 1 1	60.00	30.00	30

PERIPHERAL CLOCK TABLE CHART FOR ST49C158-03 (MHz)

CLK1	CLK2
40	24

FREQUENCY TRANSITIONS

The ST49C158 is designed to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

STOP CLOCK (Mask Option)

The OE pin can either three state the CPU output clocks or stop them in the low state without a glitch. The selection between the two features is done through a metal mask option.

ST49C158-03 uses the three state option.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

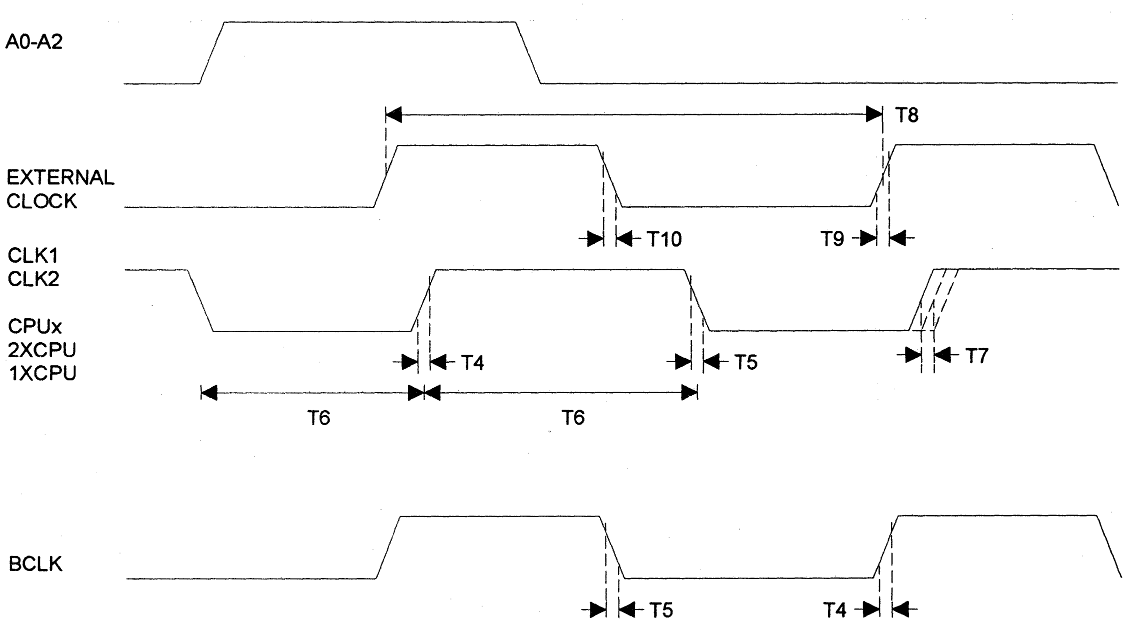
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = -8.0 mA
I_{IL}	Input low current			-40	µA	Except pins 2, 10
I_{IH}	Input high current			40	µA	VIN = Vcc
I_{CC}	Operating current		50	80	mA	No load.
R_{IN}	Internal pull-up resistance		800		kΩ	Pin 10

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_4	Output rise time		1	2	ns	0.8V - 2.0V, 20pF
T_5	Output fall time		1	2	ns	2.0V - 0.8V, 20pF
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_7	Jitter 1 sigma		±0.5	±2	%	
T_7	Jitter absolute		±2	±5	%	
T_8	Input frequency	7	14.318	20	MHz	
T_9	Input clock rise time			20	ns	
T_{SK}	Clock skew between CPU outputs		±100	±300	ps	

TIMING DIAGRAM



STARTECH
An EXAR Company

ST49C214

Printed August 3, 1995

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C214 is a monolithic analog CMOS device designed to generate dual frequency outputs from sixteen possible combinations for video Dot clock frequencies and four memory clock frequencies for high performance video display systems. The ST49C214 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2μ process to achieve 100 MHz speed for high end frequencies.
The ST49C214 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C214 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device) or external crystal connected between XTAL1 and XTAL2.
The ST49C214 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and two address lines for memory clock selection.

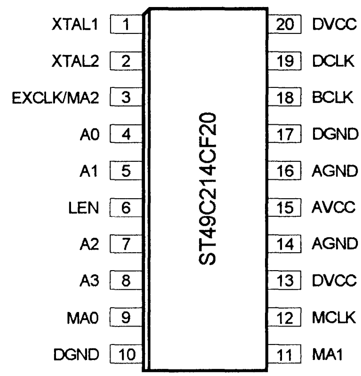
FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS2494, AV9194
- Programmable analog phase locked loop
- High speed (up to 100 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

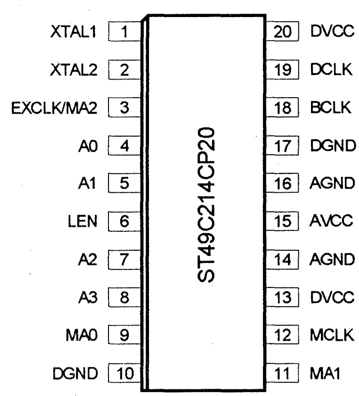
ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C214CP20-xx	Plastic-DIP	0° C to +70° C
ST49C214CF20-xx	SOIC	0° C to +70° C
ST49C214CJ20-xx	PLCC	0° C to +70° C

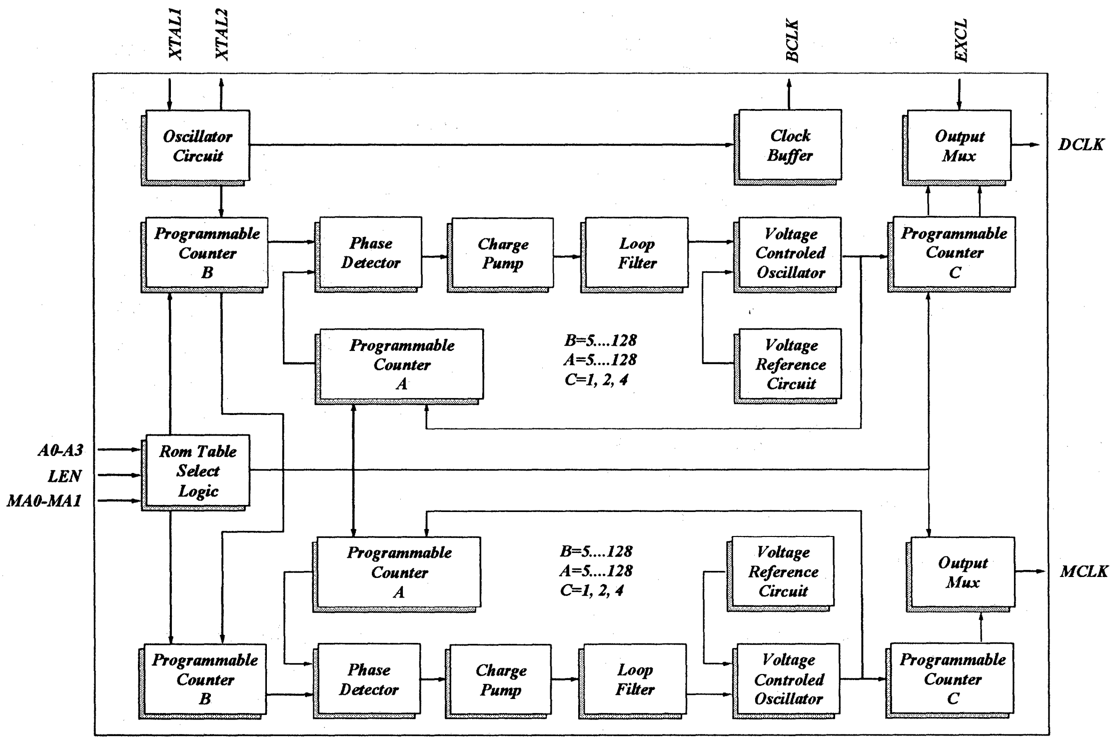
SOIC Package



Plastic-DIP Package



BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL1	1	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	2	O	Crystal output.
EXCLK/MA2	3*	I	External clock input or Memory clock select address 3
A0	4*	I	Dot clock Frequency select address 1.
A1	5*	I	Dot clock Frequency select address 2.
LEN	6*	I	Address latch enable input (active high). To latch selected programmed clock output.
A2	7*	I	Dot clock Frequency select address 3.
A3	8*	I	Dot clock Frequency select address 4.
MA0	9*	I	Memory clock Frequency select address 1.
GND	10	O	Digital and Analog ground.
MA1	11*	I	Memory clock Frequency select address 2.
MCLK	12	O	Programmed memory clock output frequency.
DVCC	13	I	Digital supply voltage. Single +5 volts.
GND	14	O	Digital and Analog ground.
AVCC	15	I	Analog supply voltage. Single +5 volts.
GND	16	O	Digital and Analog ground.
GND	17	O	Digital and Analog ground.
BCLK	18*	O	Buffered crystal clock output frequency.
DCLK	19	O	Programmed video clock output frequency.
DVCC	20	I	Digital supply voltage. Single +5 volts.

* Have internal pull-up resistor on inputs.

FREQUENCY SELECT CALCULATION

The ST49C214 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.
The accuracy of the frequencies produced by the ST49C214 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

XCLK = (Reference clock) X A/(B X C)

where A=5, 6, 7,.........256
B=5, 6, 7,.........128, AND
C=1, 2, 3, 4, 6, 12

For proper output frequency, the ST49C214 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask option are provided for custom applications.

*Any frequency can be in any decoding position.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

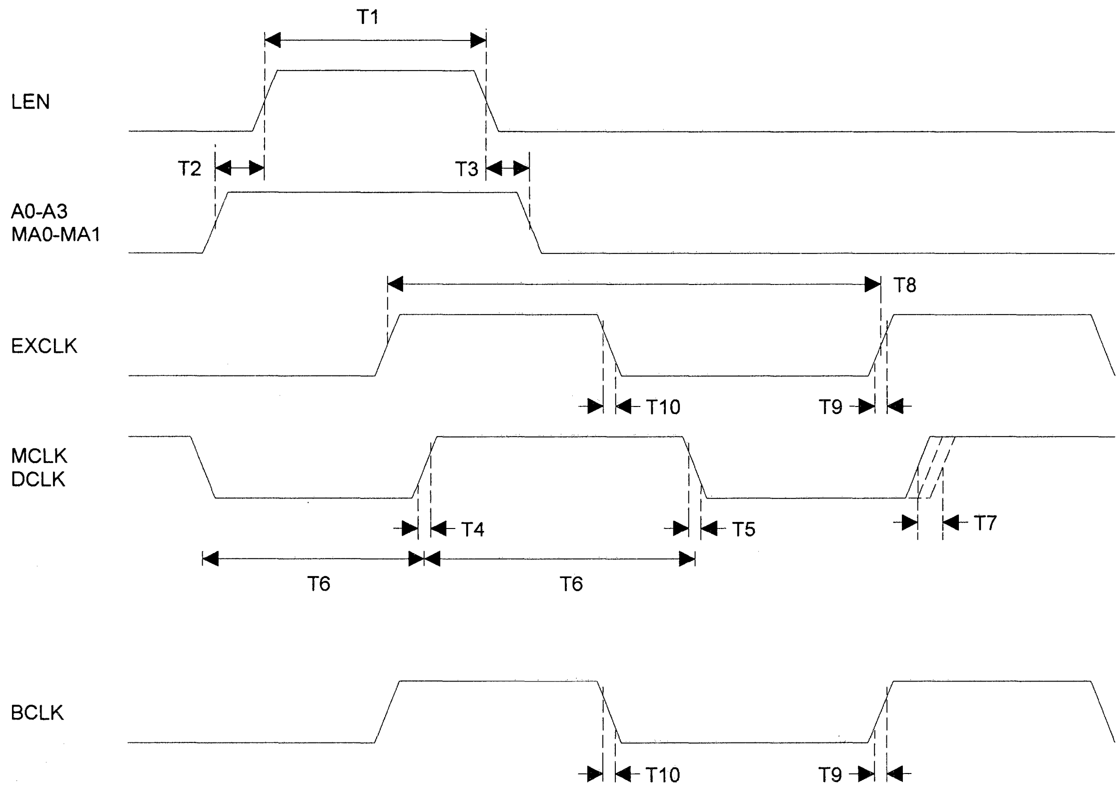
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	VIN=Vcc
I_{CC}	Operating current		35	50	mA	No load. DCLK=80MHz, MCLK=40MHz
R_{IN}	Internal pull-up resistance	15	20	25	kΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		2	3	ns	0.8V - 2.0V, 15pF
T_5	Fall time		2	3	ns	2.0V - 0.8V, 15pF
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter 1 sigma		±0.5	±2	%	
T_7	Jitter absolute		±2	±5	%	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	

TIMING DIAGRAM



Video clock address (Hex)	ST49C214-1 Frequency (MHz)	ST49C214-2 Frequency (MHz)	ST49C214-3 Frequency (MHz)	ST49C214-4 Frequency (MHz)	ST49C214-5 Frequency (MHz)
0	XTAL	30.000	25.175	20.000	50.350
1	65.028	77.250	28.325	24.000	56.644
2	EXCLK	EXCLK	85.000	32.000	65.000
3	36.000	80.000	44.900	40.000	72.000
4	25.175	31.500	40.000	50.000	80.000
5	28.322	36.000	48.000	66.667	89.800
6	24.000	75.000	50.000	80.000	63.000
7	40.000	50.000	81.150	100.000	75.000
8	44.900	40.000	25.175	54.000	25.175
9	50.350	50.000	28.325	70.000	28.322
A	16.257	32.000	37.500	90.000	31.500
B	32.514	44.900	44.900	110.000	36.000
C	56.644	25.175	40.000	25.000	40.000
D	20.000	28.322	32.500	33.333	44.900
E	41.539	65.000	50.000	40.000	50.000
F	80.000	36.000	65.000	50.000	65.000
Memory clock address (Hex)	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**
0	32.900	36.000	36.000	16.000	40.000
1	35.600	44.347	40.000	24.000	41.612
2	43.900	37.500	45.000	50.000	44.744
3	49.100	44.773	50.000	66.667	50.000

Compatible with	**ICS-236** **AV-36**	**ICS-242** **AV-42**	**ICS-231**	**ICS-244** **AV-44**	**ICS-237**
Video Controller	GD6410	WD90C30	ET4000		ET4000

Video clock address (Hex)	ST49C214-6 Frequency (MHz)	ST49C214-8 Frequency (MHz)	ST49C214-9 Frequency (MHz)	ST49C214-10 Frequency (MHz)	ST49C214-16 Frequency (MHz)
0	25.175	25.175	25.175	30.250	XTAL
1	28.322	28.322	28.322	65.000	16.257
2	40.000	40.000	40.000	85.000	EXCLK
3	65.000	32.500	EXCLK	36.000	32.514
4	44.900	50.000	50.000	25.175	25.175
5	50.000	65.000	77.000	28.322	28.322
6	130.000	38.000	36.000	34.000	24.000
7	75.000	44.900	44.889	40.000	40.000
8	25.175	31.500	130.00	44.900	XTAL
9	28.322	36.000	120.00	50.350	16.257
A	EXCLK	80.000	80.000	31.500	EXCLK
B	EXCLK	63.000	31.500	32.500	36.000
C	60.000	50.000	110.00	63.000	25.175
D	80.000	100.000	65.000	72.000	28.322
E	EXCLK	76.000	75.000	75.000	24.000
F	EXCLK	110.000	72.000	80.000	40.000
Memory clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	50.000	70.000	55.000	36.000	31.000
1	60.000	63.830	75.000	44.000	36.000
2	65.000	60.000	70.000	49.000	43.000
3	75.000	81.000	80.000	40.000	49.000

Compatible with	**ICS-253**	**ICS-263**	**ICS-256** **AV-56**	**ICS-266**	**ICS-247**
Video Controller	NCR77C22E	HT216	S3/86C911	GDS5410	GDS5320

Video clock address (Hex)	ST49C214-17 Frequency (MHz)	ST49C214-18 Frequency (MHz)	ST49C214-19 Frequency (MHz)	ST49C214-20 Frequency (MHz)	ST49C214-25* Frequency (MHz)
0	25.175	25.175	25.175	50.350	25.175
1	28.322	28.322	28.322	56.644	28.322
2	28.636	40.000	40.000	33.250	40.000
3	36.000	EXCLK	EXCLK	52.000	72.000
4	40.000	50.000	50.000	80.000	50.000
5	42.954	77.000	77.000	63.000	77.000
6	44.900	36.000	36.000	EXCLK	36.000
7	57.272	44.889	44.889	75.000	44.900
8	60.000	130.00	130.00	25.175	130.00
9	63.960	120.00	120.00	28.322	120.00
A	75.000	80.000	80.000	31.500	80.000
B	80.000	31.500	31.500	36.000	31.500
C	85.000	110.00	110.00	40.000	110.00
D	99.000	65.000	65.000	44.900	65.000
E	102.00	75.000	75.000	50.000	75.000
F	108.00	94.500	94.500	65.000	94.500
Memory clock address (Hex)	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**
0	64.000	45.000	55.000	40.000	55.000
1	40.830	38.000	75.000	33.333	65.000
2	48.000	52.000	70.000	44.000	70.000
3	60.000	50.000	80.000	50.000	80.000
4					45.000
5					40.000
6					60.000
7					50.000

Compatible with	**ICS-240**	**ICS-275** **AV-07**	**ICS-305**	**ICS-260**	**CH9294-G**
Video Controller	TI/34010/20	S3/801/805	S3/924	WEITEK W5186	S3/801/805

Video clock address (Hex)	ST49C214-26 Frequency (MHz)				ST49C214-27 Frequency (MHz)
0	25.175				75.000
1	28.322				80.000
2	36.000				85.000
3	65.000				90.000
4	44.900				95.000
5	50.000				100.00
6	80.000				105.00
7	75.000				110.00
8	56.644				115.00
9	63.000				120.00
A	72.000				125.00
B	130.00				130.00
C	90.000				135.00
D	100.00				140.00
E	110.00				145.00
F	120.00				150.00
Memory clock address (Hex)	**Frequency (MHz)**				**Frequency (MHz)**
0	50.000				40.000
1	60.000				45.000
2	65.000				50.000
3	75.000				55.000
4					60.000
5					65.000
6					70.000
7					75.000

Compatible with **ICS-277**
AV-46
Video Controller NCR77C22E+

* = The External clock input pin has been changed to MA2 to privide four additional preprogrammed memory clock selections. When Pin-3 of the ST49C214-25 is connected to ground it is downward compatible to standard ST49C214-XX. This pin contains internal pull-up resistor.

STARTECH

An EXAR Company

ST49C418

Printed August 3, 1995

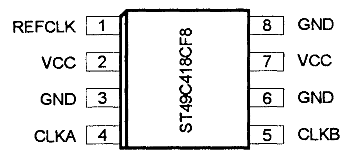
PREPROGRAMMED STEREO CODEC's CLOCK SYNTHESIZER

1

DESCRIPTION

The ST49C418 is a mask programmable monolithic analog CMOS device, designed to replace existing dual crystals/oscillators with single frequency clock input. The ST49C418 provides high speed and low jitter clock outputs for multi-media stereo codecs.
The ST49C418 interfaces to Analog Devices's AD1848 and Crystal Semiconductor's CS4231 stereo codecs. The ST49C418 provides 16.934 and 24.576 MHz clock outputs utilizing the 14.318 MHz clock input.
ST49C418 is designed in a 1.2μ process to achieve upto 50 MHz output frequency.

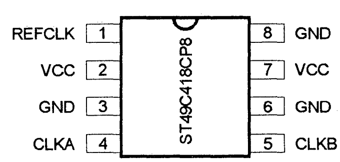
SOIC Package



FEATURES

- Mask programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package
- Programmable input/output frequencies
- TTL compatible outputs
- No external components besides decoupling capacitors

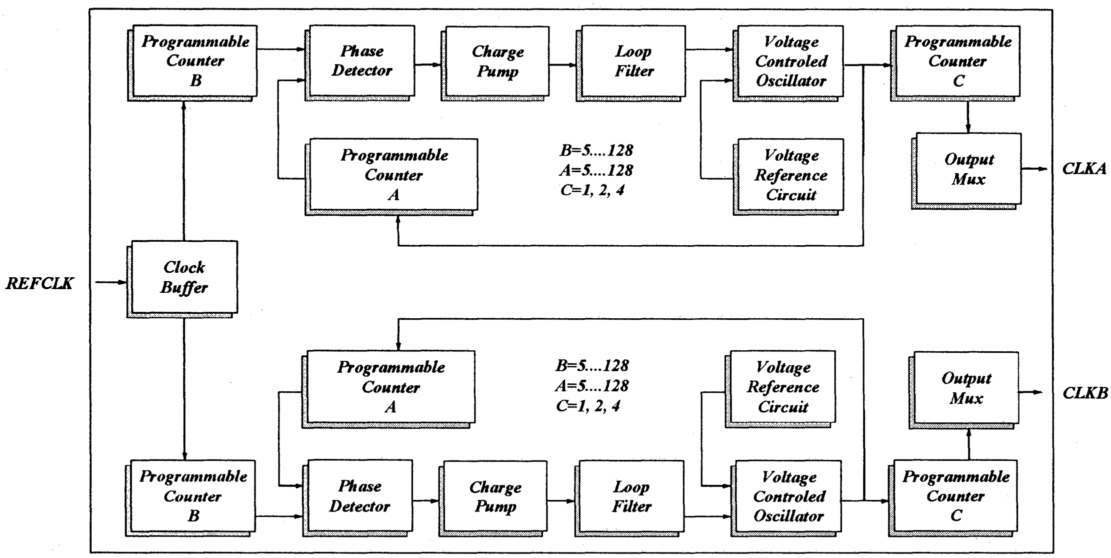
Dip Package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C418CP8	Plastic-DIP	0 ° C to +70° C
ST49C418CF8	SOIC	0° C to +70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
REFCLK	1	I	External Reference Clock input. REFCLK is used as internal phase locked loop reference clock.
VCC	2	I	Supply voltage. Single +5 volts.
GND	3	O	Supply ground.
CLKA	4	O	Programmable output clock. Programmed for 16.9344 MHz output.
CLKB	5	O	Programmable output clock. Programmed for 24.576 MHz output.
GND	6	O	Supply ground.
VCC	7	I	Supply voltage. Single +5 volts.
GND	8	O	Supply ground.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.01 to 0.047μF capacitor to REFCLK, and keep the lead length of the capacitor to REFCLK to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C418 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C418 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B X C)

where A=5, 6, 7,.........128
B=5, 6, 7,.........128
C=2

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

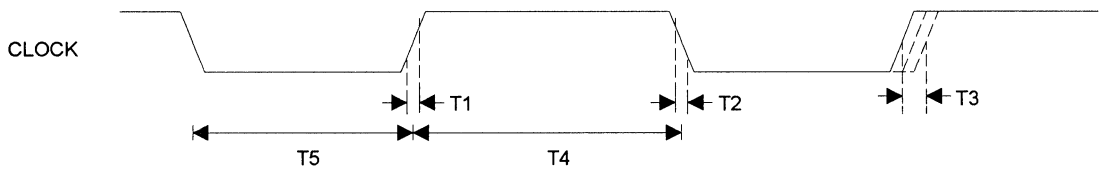
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 25 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 25 mA
I_{IH}	Input high current			1	.µA	
I_{CC}	Operating current		20	35	mA	No load.

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	CLOCK rise time		1.5	3	ns	0.5V - 2.8V, 15pF
T_2	CLOCK fall time		1.5	3	ns	2.8V - 0.5V, 15pF
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	VCC/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	
T	Input frequency	5	10	40	MHz	
T_6	CLOCK frequency change		0.01		%	

TIMING DIAGRAM



LINE DRIVERS / RECEIVERS 2

Index

STARTECH
An EXAR Company

ST26C31

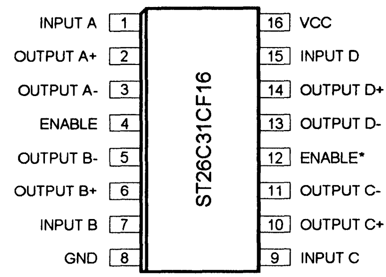
Printed August 3, 1995

QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

DESCRIPTION

The ST26C31 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST26C31 circuit.
The ST26C31 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

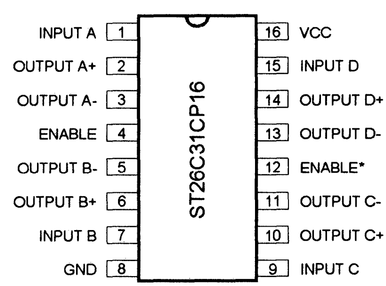
SOIC package



FEATURES

- Pin-to-pin compatible with National DS26C31C
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

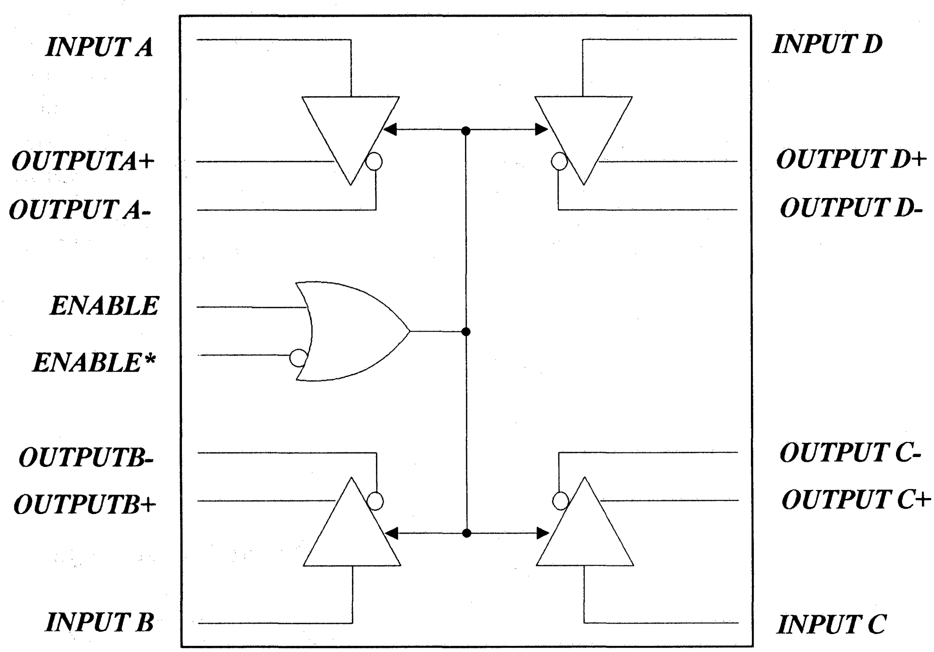
Plastic-DIP package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C31CP16	Plastic-DIP	0° C to + 70° C
ST26C31CF16	SOIC	0° C to + 70° C
ST26C31IP16	Plastic-DIP	-40° C to + 85° C
ST26C31IF16	SOIC	-40° C to + 85° C

BLOCK DIAGRAM



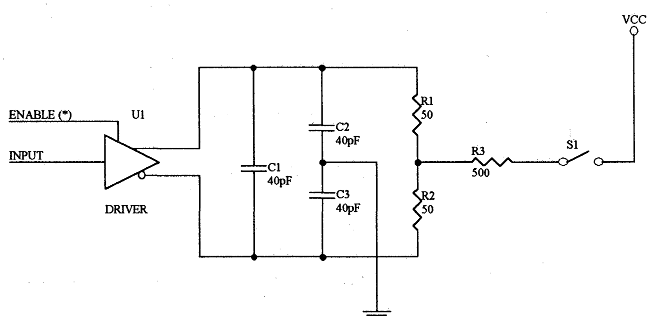
SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A	1	I	Driver A input pin.
OUTPUT A+	2	O	Driver A differential non-inverting output pin.
OUTPUT A-	3	O	Driver A differential inverting output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four drivers. All four drivers are gated with two input or gate.
OUTPUT B-	5	O	Driver B differential inverting output pin.
OUTPUT B+	6	O	Driver B differential non-inverting output pin.
INPUT B	7	I	Driver B input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverting output pin.
OUTPUT C-	11	O	Driver C differential inverting output pin.
ENABLE*	12	I	Gate control (active low). See ENABLE pin description.
OUTPUT D-	13	O	Driver D differential inverting output pin.
OUTPUT D+	14	O	Driver D differential non-inverting output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

Functional table

Enable	Enable*	Input	Differential Non-Inverting Output	Differential Inverting Output
L	H	X	Z	Z
L	L	L	L	H
L	L	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	L	H
H	H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
*T_5	Skew			2	ns	S1 open

* Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ABSOLUTE MAXIMUM RATINGS

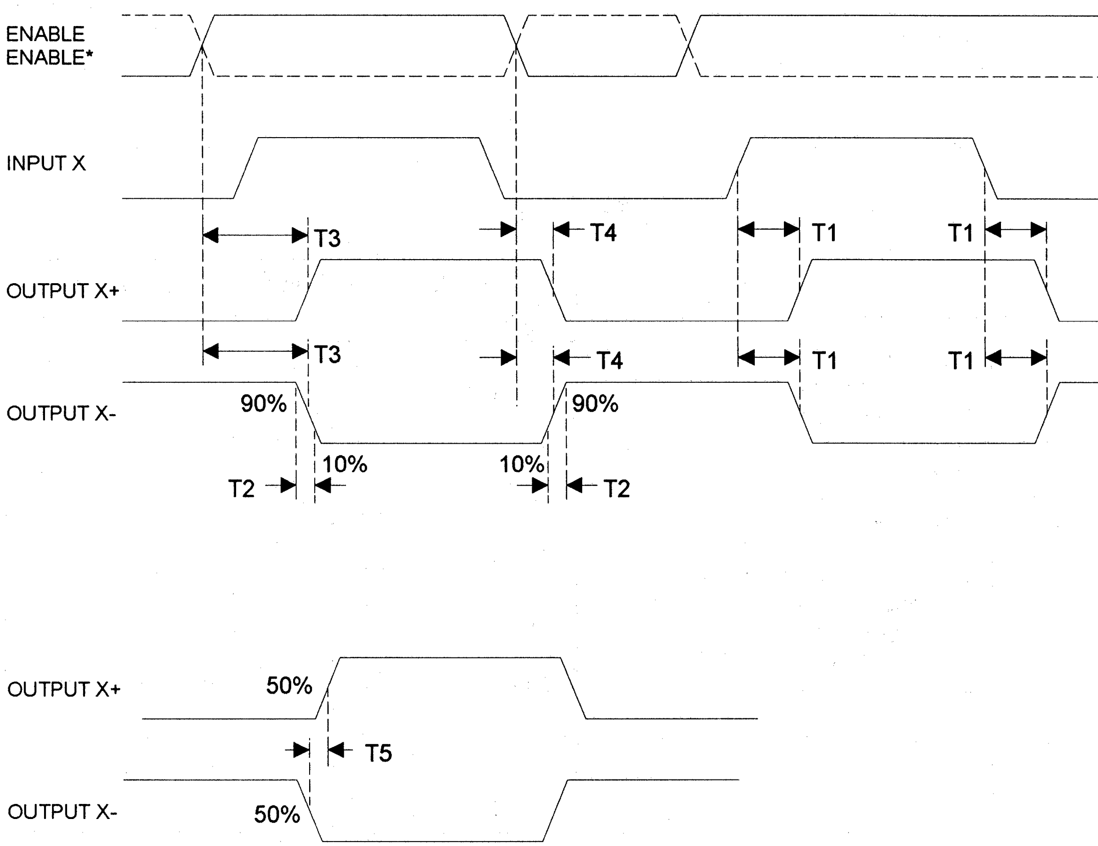
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		600		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{IH}	Input high level	2.0			V	
V_{IL}	Input low level			0.8	V	
V_{OH}	Output high level	2.5			V	
V_{OL}	Output low level			0.5	V	
V_{OS}	Differential output level	2.0			V	R_L=100Ω
V_{OC}	Common mode output voltage			3.0	V	R_L=100Ω
V_{OD}	Difference in common mode output			0.4	V	R_L=100Ω
C_{IN}	Input capacitance	7	10	15	pF	
C_{PD}	Power dissipation capacitance		100		pF	
I_{OS}	Output short current	-200		-30	mA	V_{IN}=VCC or GND
I_{OFF}	Output leakage current power off			100	µA	Vout=6V
				-100	µA	Vout=0.25V
I_{DC}	Output current			±150	mA	

DIFFERENTIAL LINE DRIVER TIMING



2631-CK-1

STARTECH

An EXAR Company

ST26C32

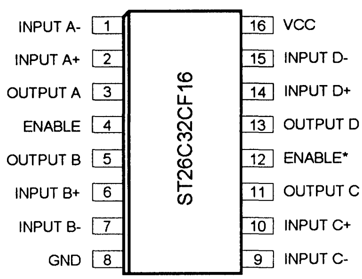
Printed August 3, 1995

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of ±7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.
The ST26C32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST26C32 is suitable for low power 5V operation.

SOIC package



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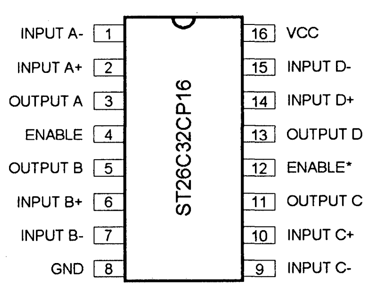
FEATURES

- Pin-to-pin compatible with National DS26C32C
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

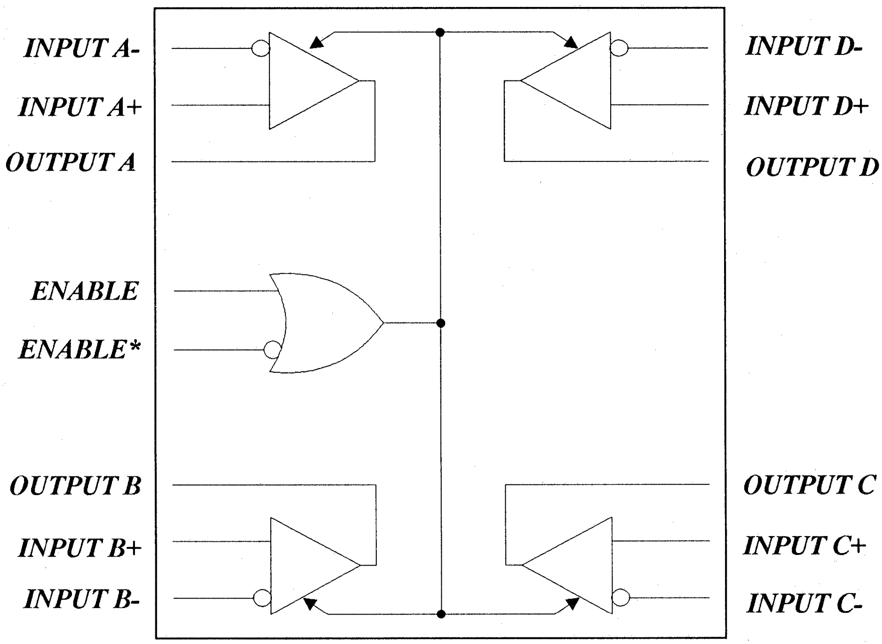
Plastic-DIP package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C32CP16	Plastic-DIP	0° C to + 70° C
ST26C32CF16	SOIC	0° C to + 70° C
ST26C32IP16	Plastic-DIP	-40° C to + 85° C
ST26C32IF16	SOIC	-40° C to + 85° C

BLOCK DIAGRAM



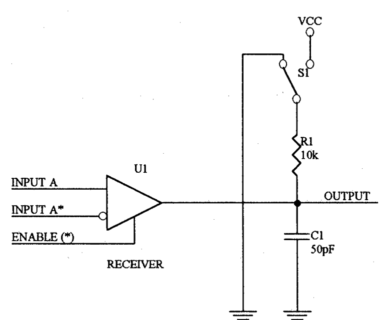
SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four receivers.
OUTPUT B	5	O	Receiver B output pin.
INPUT B+	6	I	Receiver B differential non-inverting input pin.
INPUT B-	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C-	9	I	Receiver C differential inverting input pin.
INPUT C+	10	I	Receiver C differential non-inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE *	12	I	Gate control (active low). See ENABLE description
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

Functional table

Enable	Enable*	Output	Differential Non-Inverting Input	Differential Inverting Input
L	H	Z	X	X
H	L	L	L	H
H	L	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

ABSOLUTE MAXIMUM RATINGS

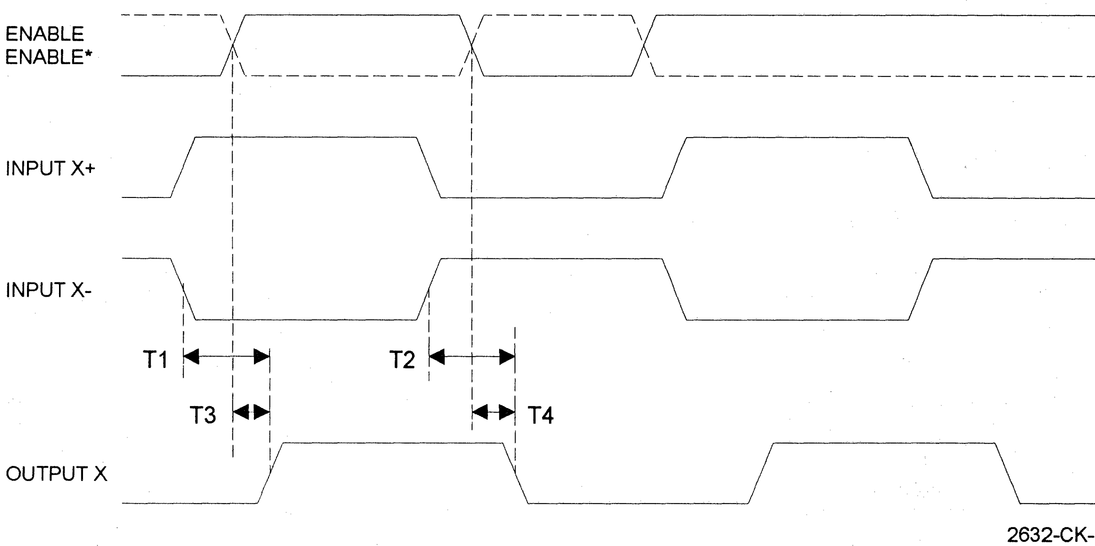
Supply range	7 Volts
Voltage at any logic pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8	4.2		V	I_{OH}= -6mA
V_{OL}	Output low level			0.4	V	I_{OH}= 6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		12		mA	V_{DIF}=+1V
I_{OZ}	Three state output leakage		±1.0	±5.0	µA	V_{OUT}=VCC or GND
I_{EN}	Enable input current		±1.0		µA	V_{IN}=VCC or GND
V_R	Input resistance	5		15	kΩ	-7V < V_{CM} < +7V

DIFFERENTIAL LINE RECEIVER TIMING



RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVERS AND DRIVERS

GENERAL DESCRIPTION

The ST31C32 is a high speed CMOS combo differential line receiver and driver designed to meet the standard RS-422, RS-423 requirements for digital and transmission over balanced lines. It provides five differential line receivers with three state control and three line drivers also with three state control.

The line driver inputs and line receiver outputs are TTL compatible to interface with standard 74LS and CMOS environments. The ST31C32 has been designed for low power 5 volts operation and is especially suited for MODEM/UART applications.

The receiver in the ST31C32 has an input sensitivity of 200mv over the common mode input voltage range of ±7V. They incorporate hysteresis for improved noise margin with slow changing input signals. Input fail-safe circuitry is also included which will cause the output of the receiver to go to a logic "1" level if the inputs are left open.

A special voltage sensing circuit is utilized in the drivers that will three-state the outputs during power down and power up. This will prevent spurious glitches from appearing on the outputs.

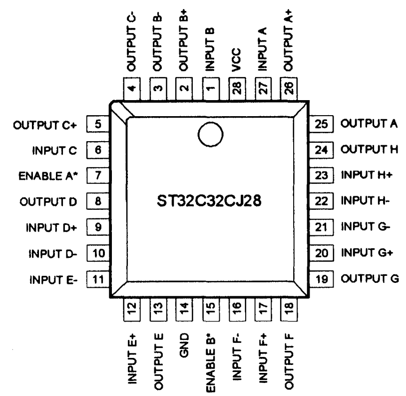
FEATURES

- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422/423 requirements
- Low propagation delays
- High speed
- Five line receivers with three state control
- Three line drivers with three state control
- 28 pin PLCC and SOIC package

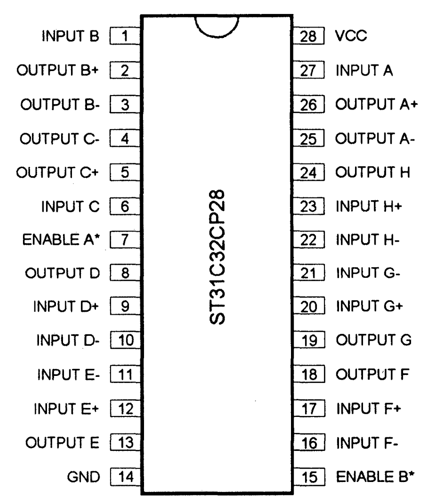
ORDERING INFORMATION

Part number	Package	Operating temperature
ST31C32CJ28	PLCC	0° C to + 70° C
ST31C32CF28	SOIC	0° C to + 70° C
ST31C32IJ28	PLCC	-40° C to + 85° C
ST31C32IF28	SOIC	-40° C to + 85° C

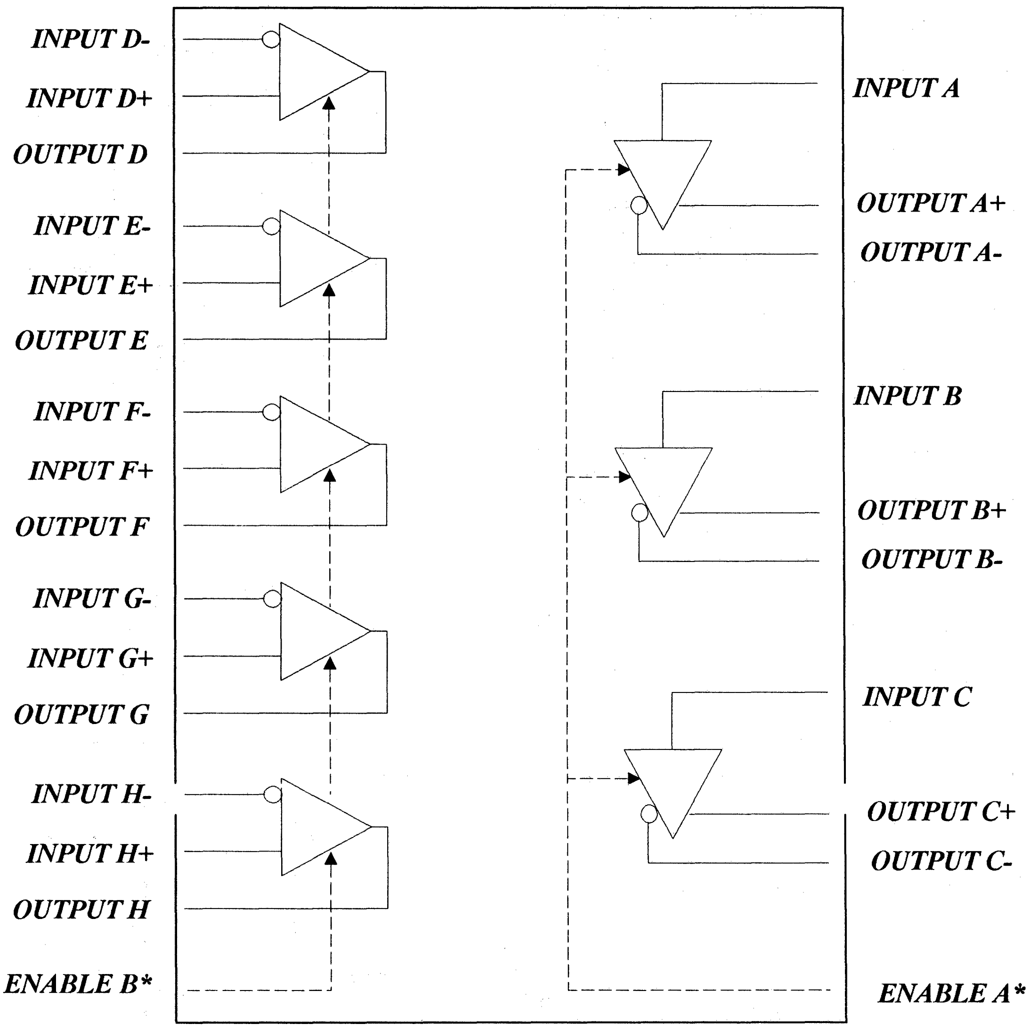
PLCC Package



DIP Package



BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT B	1	I	Line driver B input pin.
OUTPUT B+	2	O	Line driver B differential non-inverted output pin.
OUTPUT B -	3	O	Line driver B differential inverted output pin.
OUTPUT C -	4	O	Line driver C differential inverted output pin.
OUTPUT C+	5	O	Line driver C differential non-inverted output pin.
INPUT C	6	I	Line driver C input pin.
ENABLE A*	7*	I	Gate control A (active low). This pin enables/ disables the three line driver outputs.
OUTPUT D	8	O	Line receiver D output pin.
INPUT D +	9	I	Line receiver D differential non-inverted input pin.
INPUT D -	10	I	Line receiver D differential inverted input pin.
INPUT E -	11	I	Line receiver E differential inverted input pin.
INPUT E +	12	I	Line receiver E differential non-inverted input pin.
OUTPUT E	13	O	Line receiver E output pin.
GND	14	O	Signal and power ground.
ENABLE B*	15*	I	Gate control B (active low). This pin enables/ disables the five line receiver outputs.
INPUT F -	16	I	Line receiver F differential inverted input pin.
INPUT F +	17	I	Line receiver F differential non-inverted input pin.
OUTPUT F	18	O	Line receiver F output pin.
OUTPUT G	19	O	Line receiver G output pin.
INPUT G +	20	I	Line receiver G differential non-inverted input pin.

SYMBOL DESCRIPTION

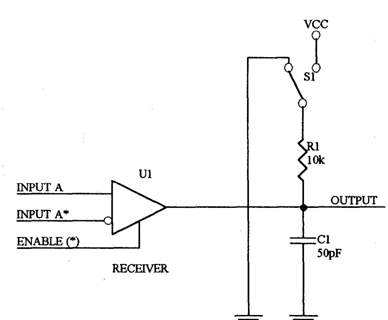
Symbol	Pin	Signal Type	Pin Description
INPUT G -	21	I	Line receiver G differential inverted input pin.
INPUT H -	22	I	Line receiver H differential inverted input pin.
INPUT H +	23	I	Line receiver H differential non-inverted input pin.
OUTPUT H	24	O	Line receiver H output pin.
OUTPUT A -	25	O	Line driver A differential inverted output pin.
OUTPUT A+	26	O	Line driver A differential non-inverted output pin.
INPUT A	27	I	Line driver A input pin.
VCC	28	I	Power supply pin.

*Has internal pull-up resistor on input

Receiver Functional table

Enable B	Differential Non-Inverting Input	Differential Inverting Input	Output
H	X	X	Z
L	L	H	L
L	H	L	H

ST31C32 RECEIVER AC TEST CIRCUIT



Driver Functional table

Enable A	Input	Differential Non-Inverted Output	Differential Inverted Output
H	X	Z	Z
L	L	L	H
L	H	H	L

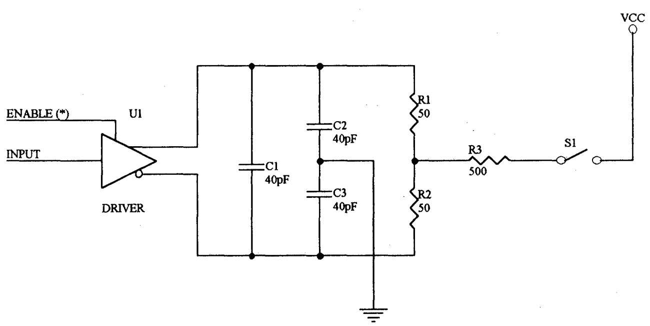
X=Don't care
Z=Three state (high impedance)

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
	Line Receiver Timing					
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V
	Line Driver Timing					
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
T_5	Skew		0.5		ns	S1 open

ST31C32 DRIVER AC TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

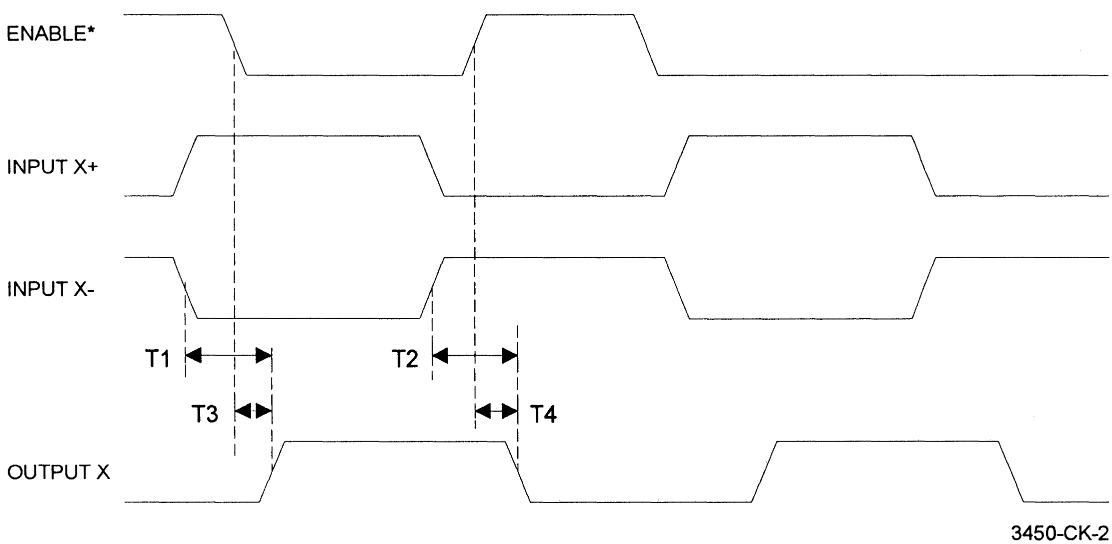
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

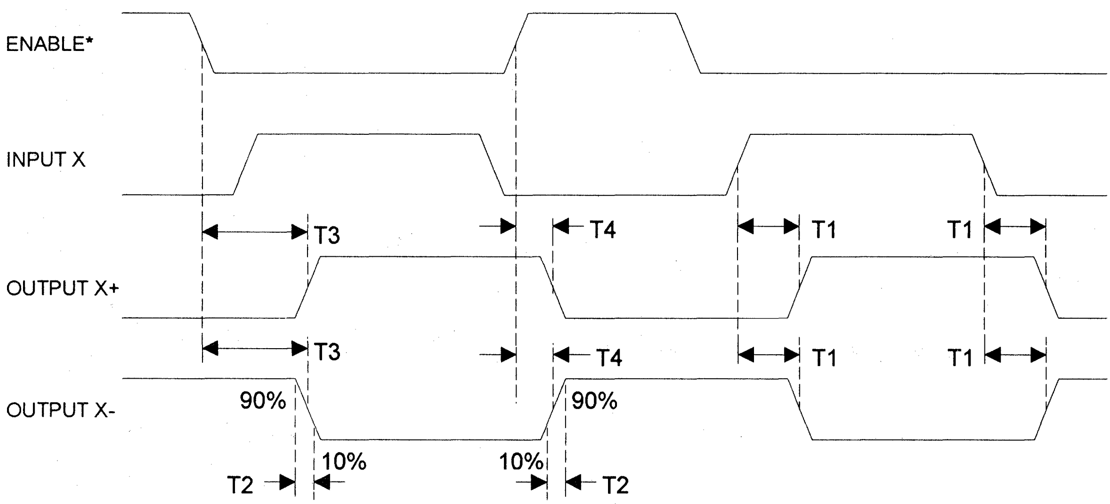
T_A=0° - 70°C, Vcc=5.0 V ± 10% unless otherwise specified.

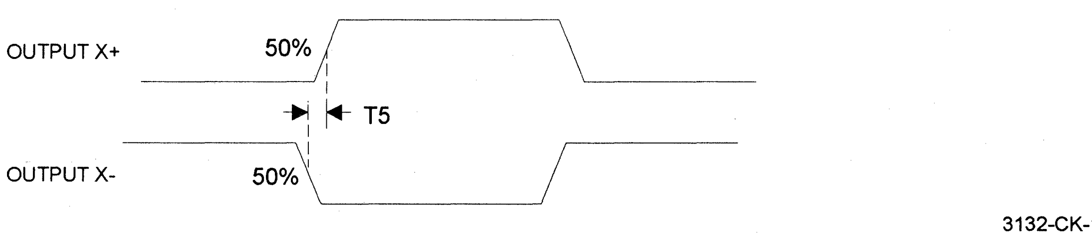
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{ROH}	Receiver output high level	3.8			V	
V_{ROL}	Receiver output low level			0.4	V	
V_{RID}	Receiver differential input level	-0.2		+0.2	V	R_L=100Ω
V_{RH}	Receiver input hysteresis		50		mV	
I_{RIN}	Receiver input current			±1.0	µA	
V_{RR}	Receiver input resistance	5		15	KΩ	
I_{CC}	Operating current		25		mA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{DOH}	Driver input high level	2.5			V	
V_{DOL}	Driver output low level			0.5	V	
V_{DOS}	Driver differential output level	2.0			V	R_L=100Ω
V_{DOC}	Driver Common mode output voltage			3.0	V	R_L=100Ω
V_{DOD}	Driver difference in common mode output			0.4	V	R_L=100Ω
I_{DIN}	Driver input current			±1.0	µA	

DIFFERENTIAL LINE RECEIVER TIMING



DIFFERENTIAL LINE DRIVER TIMING





STARTECH
An EXAR Company

ST34C50
ST34C51

Printed August 3, 1995

DUAL RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER AND DRIVER

GENERAL DESCRIPTION

The ST34C50/51 is a CMOS dual differential line receiver and driver, designed to meet the standard RS-422, RS-423 requirements and digital data transmission over balanced lines. The ST34C50/51 has an input sensitivity of 200mv over the common mode input voltage range of ± 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C50/51 circuit. The ST34C50/51 is a high speed line receiver and driver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C50/51 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C50/51 is suitable for low power 5V operation with minimum board space requirements. ST34C50/51 provides dual differential line receiver with three state control pin and dual line driver with three state control capability.

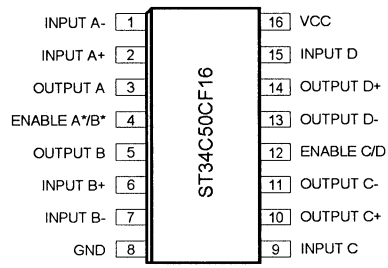
FEATURES

- Pin -to-pin compatible to Motorola MC34050 and MC34051
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422/423 requirements
- Low propagation delays
- High speed
- Dual line receiver with three state control
- Dual line driver with three state control

ORDERING INFORMATION

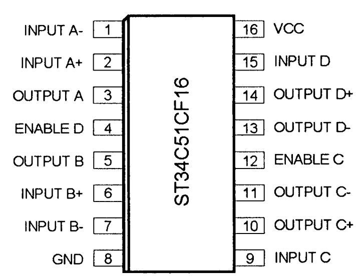
Part number	Package	Operating temperature
ST34C50CP16	Plastic-DIP	0° C to + 70° C
ST34C50CF16	SOIC	0° C to + 70° C
ST34C50IP16	Plastic-DIP	-40° C to + 85° C
ST34C50IF16	SOIC	-40° C to + 85° C
ST34C51IP16	Plastic-DIP	-40° C to + 85° C
ST34C51IF16	SOIC	-40° C to + 85° C

SOIC Package



ST34C50CF

SOIC Package



ST34C51CF

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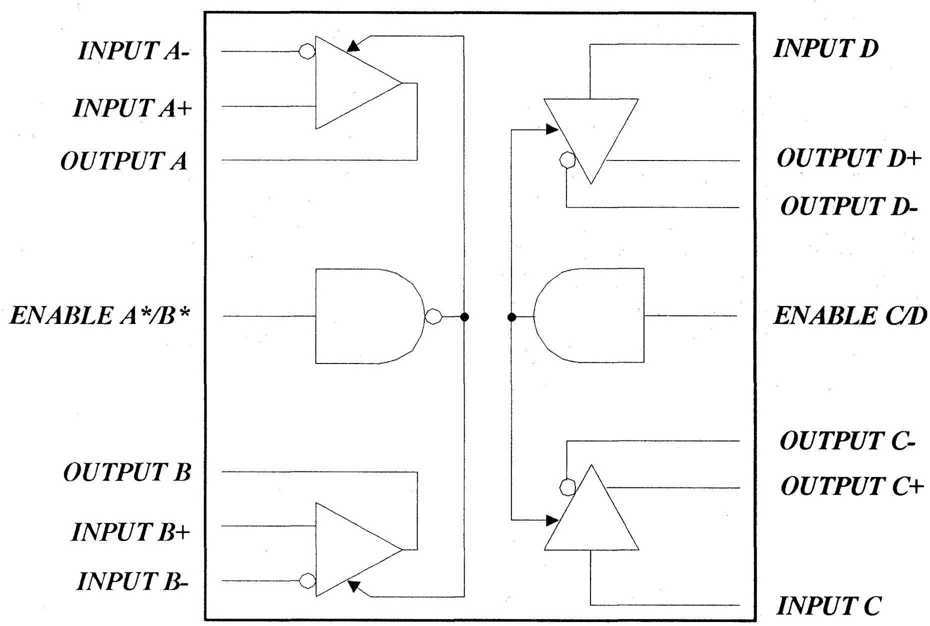
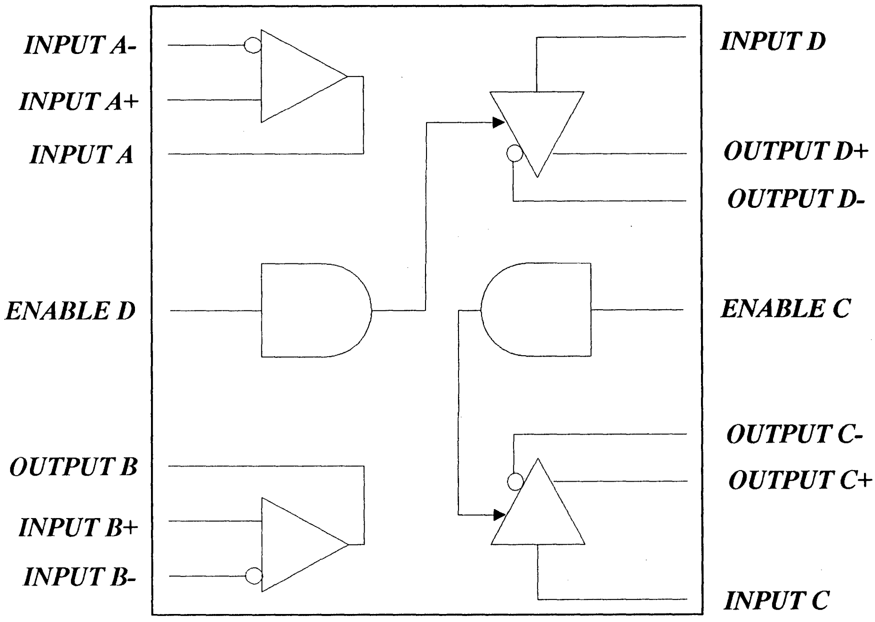
ST34C50 BLOCK DIAGRAM



ST34C51 BLOCK DIAGRAM



ST34C50
ST34C51

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active low, ST34C50 only). This pin enables/ disables the two line receiver outputs (out A and out B of ST34C50).
ENABLE D	4*	I	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver D section.
OUTPUT B	5	O	Receiver B output pin.
INPUT B +	6	I	Receiver B differential non-inverting input pin.
INPUT B -	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverted output pin.
OUTPUT C -	11	O	Driver C differential inverted output pin.
ENABLE C/D	12	I	Gate control (active high, ST34C50 only). This pin enables/ disables the two line driver outputs (output C and output D of ST34C50).
ENABLE C	12*	I	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver C section.
OUTPUT D -	13	O	Driver D differential inverted output pin.
OUTPUT D+	14	O	Driver D differential non-inverted output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

Receiver Functional table (ST34C50 only)

Enable A/B	Output	Differential Non-Inverting Input	Differential Inverting Input
H	Z	X	X
L	L	L	H
L	H	H	L

X=Don't care
Z=Three state (high impedance)
Receive sections of the ST34C51 are enabled all the time.

Driver Functional table (ST34C50 only)

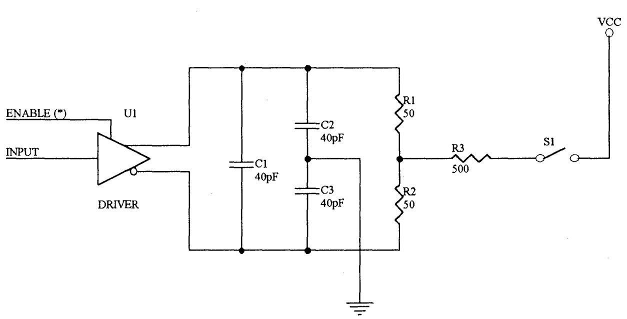
Enable C/D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

***Driver Functional table (ST34C51 only)**

Enable C or D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)
* for each section of ST34C51.

ST34C50/51 DRIVER AC TEST CIRCUIT



ST34C50
ST34C51

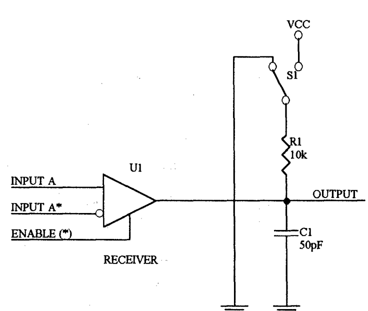
AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
	Line driver section					
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
*T_5	Skew			2	ns	S1 open
	Line receiver section					
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

* Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ST34C50/51 RECEIVER AC TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

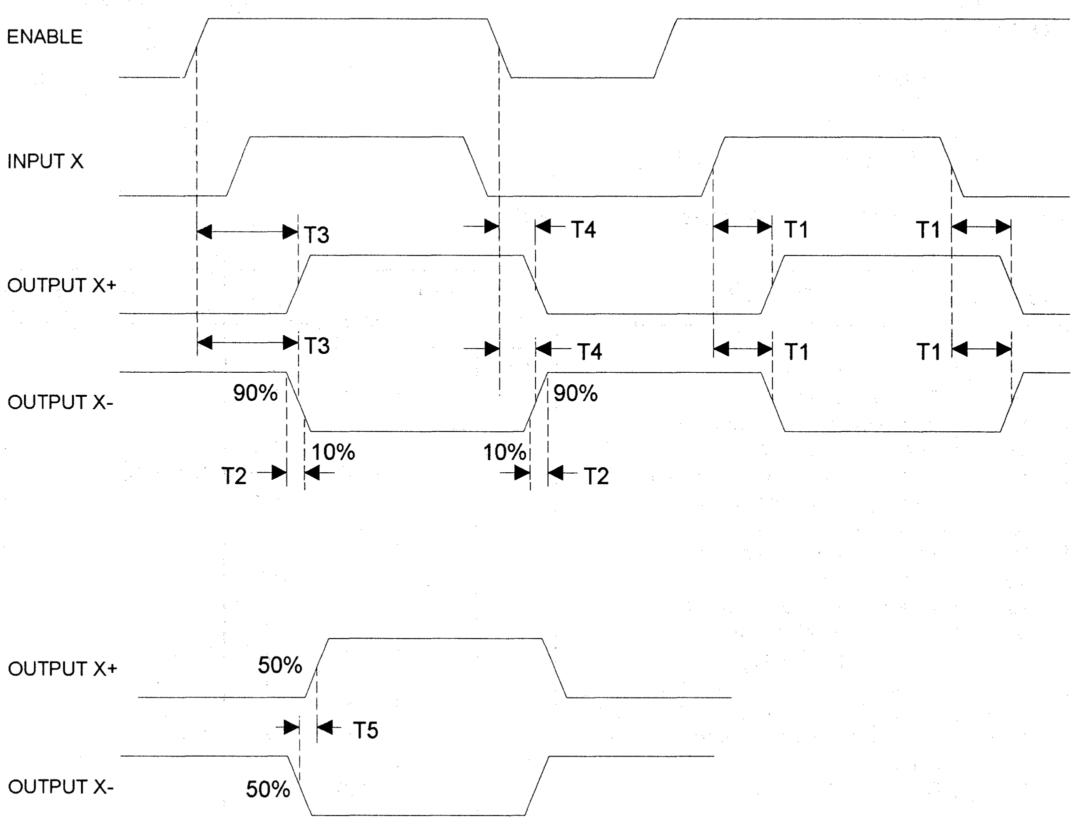
Operating supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

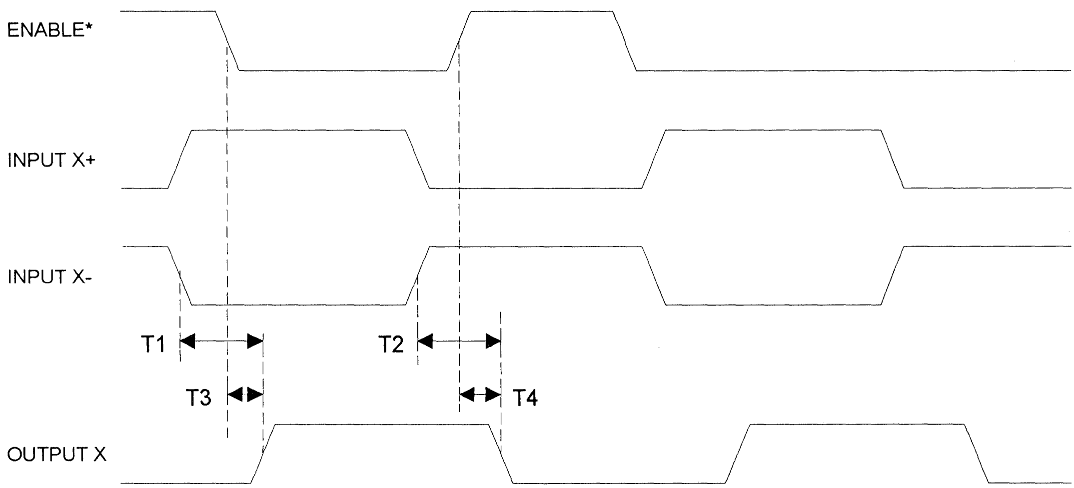
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{ROH}	Receiver output high level	3.8			V	
V_{ROL}	Receiver output low level			0.4	V	
V_{RID}	Receiver differential input level	-0.2		+0.2	V	R_L=100Ω
V_{RH}	Receiver input hysteresis		50		mV	
I_{RIN}	Receiver input current			±1.0	µA	
V_{RR}	Receiver input resistance	5		15	KΩ	
I_{CC}	Operating current		13		mA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{DOH}	Driver input high level	2.5			V	
V_{DOL}	Driver output low level			0.5	V	
V_{DOS}	Driver differential output level	2.0			V	R_L=100Ω
V_{DOC}	Driver Common mode output voltage			3.0	V	R_L=100Ω
V_{DOD}	Driver difference in common mode output			0.4	V	R_L=100Ω
I_{DIN}	Driver input current			±1.0	µA	

DIFFERENTIAL LINE DRIVER TIMING



3450-CK-1

DIFFERENTIAL LINE RECEIVER TIMING



3450-CK-2

STARTECH
An EXAR Company

ST34C86

Printed August 3, 1995

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

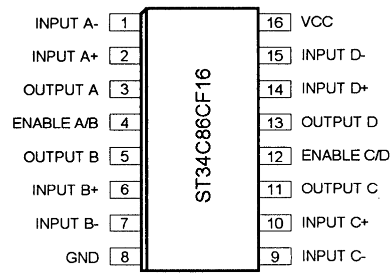
2

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of ± 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit.

The ST34C86 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

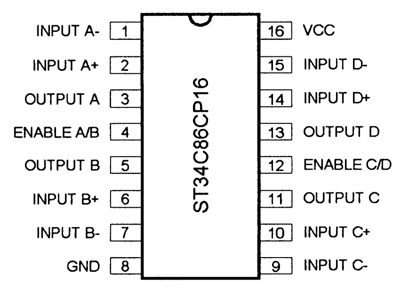
SOIC package



FEATURES

- Pin-to-pin compatible with National DS34C86
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

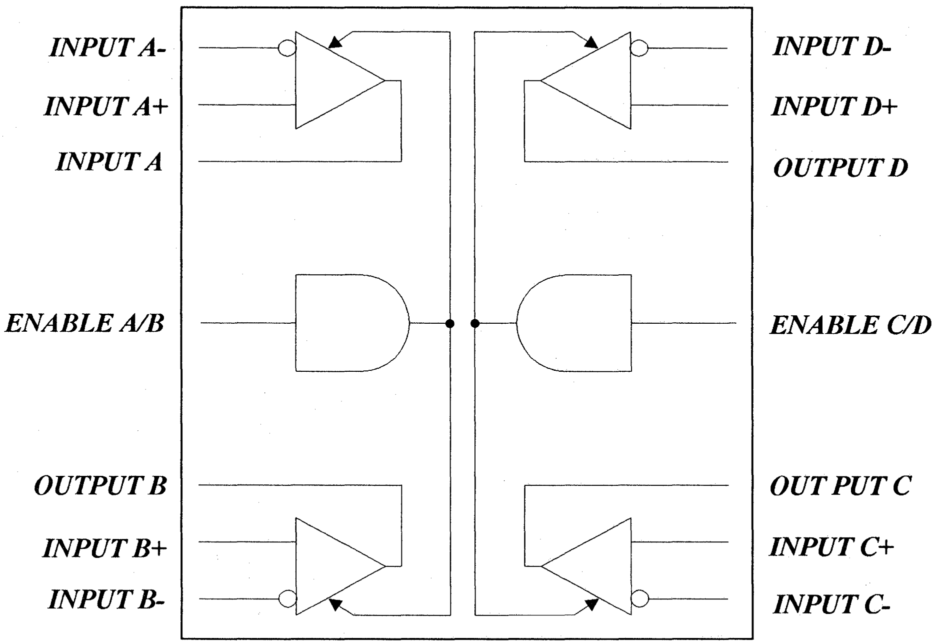
Plastic-DIP package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C86CP16	Plastic-DIP	0° C to + 70° C
ST34C86CF16	SOIC	0° C to + 70° C
ST34C86IP16	Plastic-DIP	-40° C to + 85° C
ST34C86IF16	SOIC	-40° C to + 85° C

BLOCK DIAGRAM



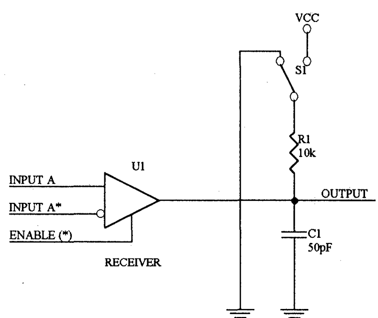
SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active high). This pin enables/disables the two line receiver outputs (out A and out B).
OUTPUT B	5	O	Receiver B output pin.
INPUT B+	6	I	Receiver B differential non-inverting input pin.
INPUT B-	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C-	9	I	Receiver C differential inverting input pin.
INPUT C+	10	I	Receiver C differential non-inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE C/D	12	I	Gate control (active high). This pin enables/disables the two line receiver outputs (output C and output D).
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

Functional table

Enable A/B C/D	Output	Differential Non-Inverting Input	Differential Inverting Input
L	Z	X	X
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

ABSOLUTE MAXIMUM RATINGS

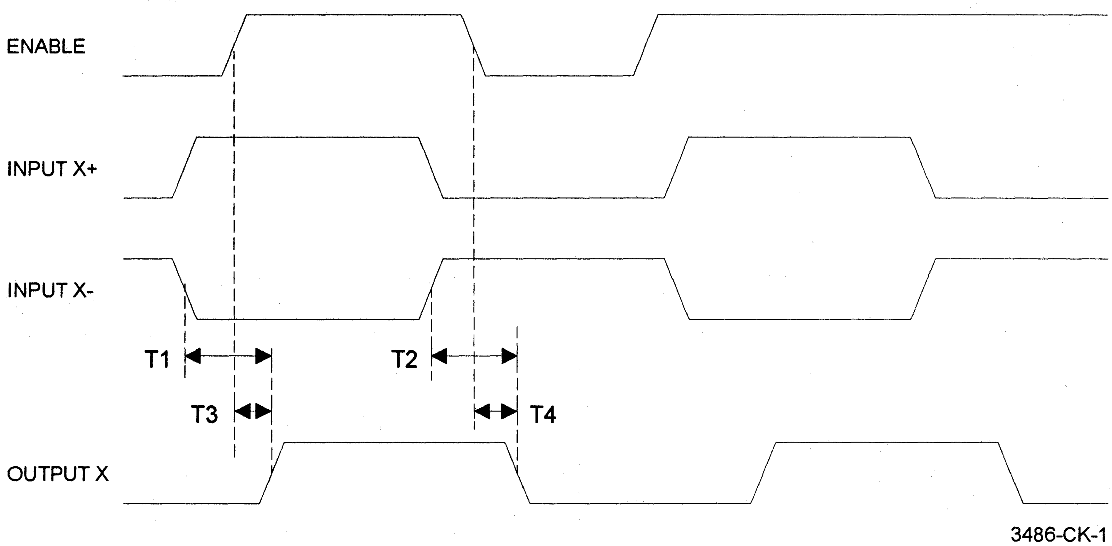
Supply range	7 Volts
Voltage at any logic pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8	4.2		V	I_{OH}= -6mA
V_{OL}	Output low level			0.4	V	I_{OH}= 6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		12		mA	V_{DIF}=+1V
I_{OZ}	Three state output leakage		±1.0	±5.0	µA	V_{OUT}=VCC or GND
I_{EN}	Enable input current		±1.0		µA	V_{IN}=VCC or GND
V_R	Input resistance	5		15	KΩ	-7V < V_{CM} < +7V

DIFFERENTIAL LINE RECEIVER TIMING



STARTECH

An EXAR Company

ST34C87

Printed August 3, 1995

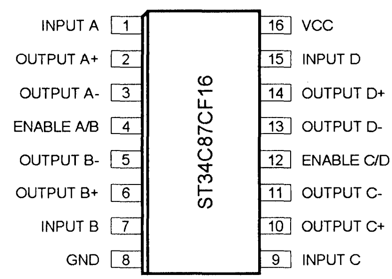
QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The ST34C87 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST34C87 circuit.

The ST34C87 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST34C87 is suitable for low power 5V operation with high input voltage protection devices.

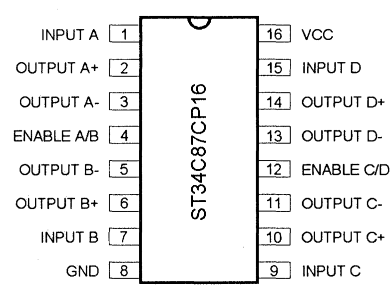
SOIC package



FEATURES

- Pin-to-pin compatible with National DS34C87
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

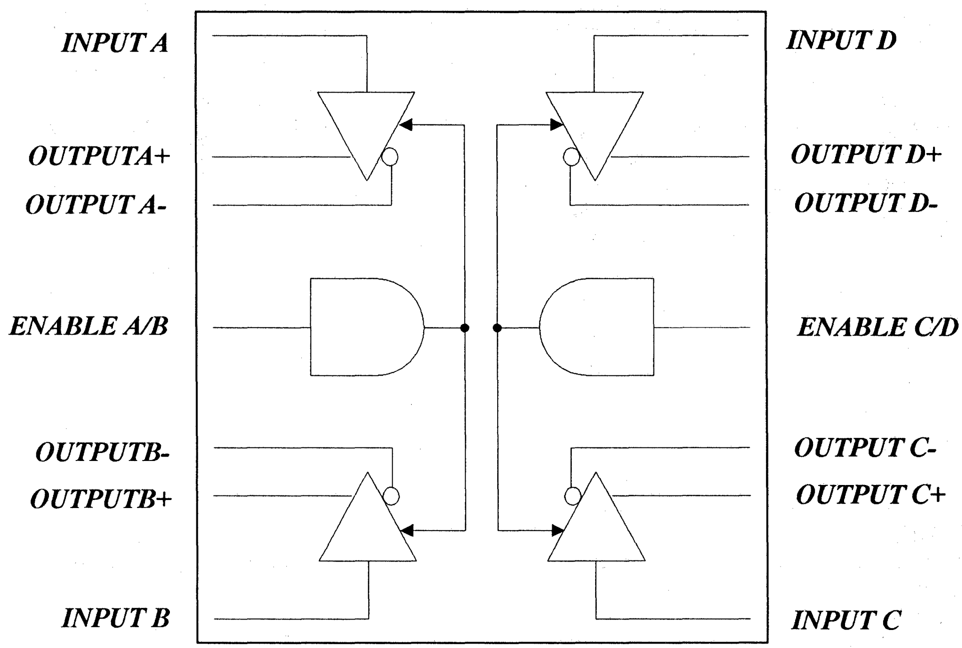
Plastic-DIP package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C87CP16	Plastic-DIP	0° C to + 70° C
ST34C87CF16	SOIC	0° C to + 70° C
ST34C87IP16	Plastic-DIP	-40° C to + 85° C
ST34C87IF16	SOIC	-40° C to + 85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

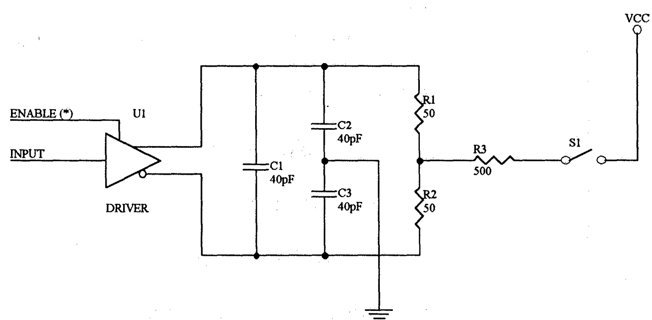
Symbol	Pin	Signal Type	Pin Description
INPUT A	1	I	Driver A input pin.
OUTPUT A+	2	O	Driver A differential non-inverting output pin.
OUTPUT A-	3	O	Driver A differential inverting output pin.
ENABLE A/B	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables two/four drivers.
OUTPUT B-	5	O	Driver B differential inverting output pin.
OUTPUT B+	6	O	Driver B differential non-inverting output pin.
INPUT B	7	I	Driver B input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverting output pin.
OUTPUT C-	11	O	Driver C differential inverting output pin.
ENABLE C/D	12	I	Gate control (active high). See ENABLE A/B pin description.
OUTPUT D-	13	O	Driver D differential inverting output pin.
OUTPUT D+	14	O	Driver D differential non-inverting output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

ST34C87

Functional table

Enable A/B C/D	Input	Differential Non-Inverting Output	Differential Inverting Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
*T_5	Skew			2	ns	S1 open

* Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ABSOLUTE MAXIMUM RATINGS

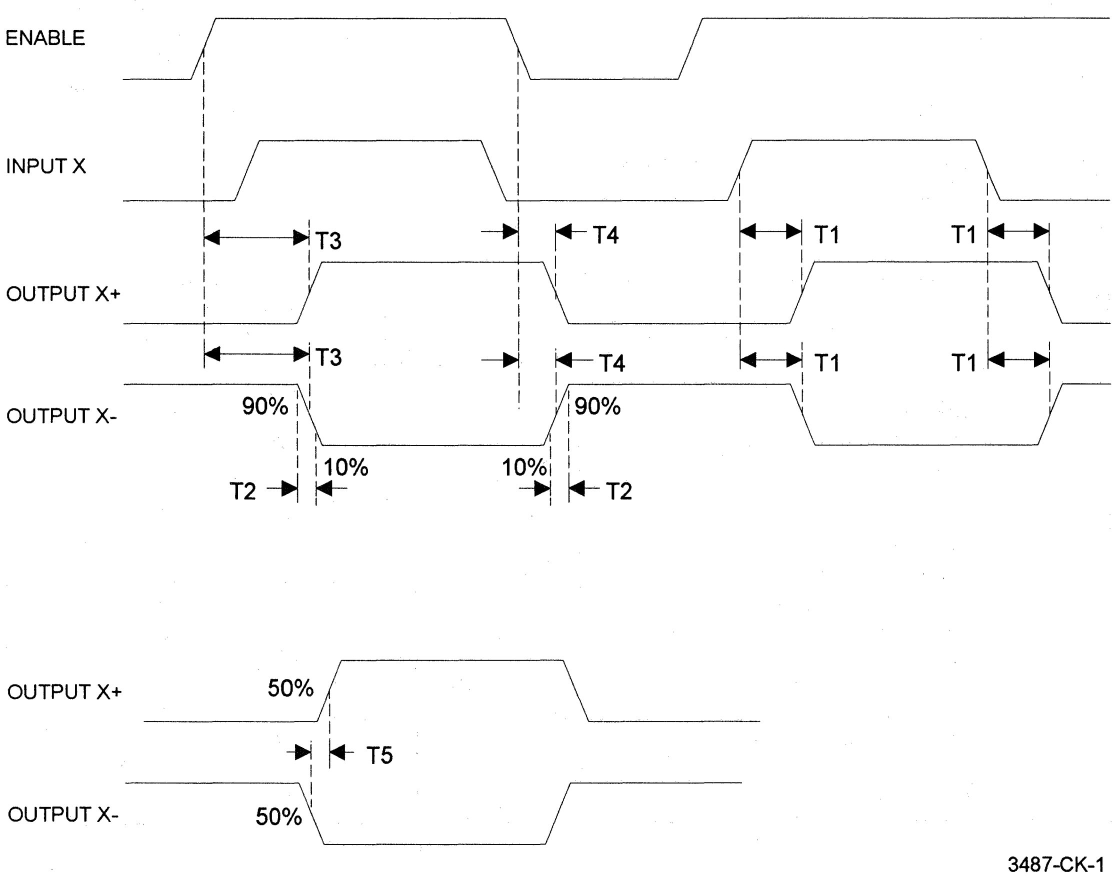
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		600		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{IH}	Input high level	2.0			V	
V_{IL}	Input low level			0.8	V	
V_{OH}	Output high level	2.5			V	
V_{OL}	Output low level			0.5	V	
V_{OS}	Differential output level	2.0			V	R_L=100Ω
V_{OC}	Common mode output voltage			3.0	V	R_L=100Ω
V_{OD}	Difference in common mode output			0.4	V	R_L=100Ω
C_{IN}	Input capacitance	7	10	15	pF	
C_{PD}	Power dissipation capacitance		100		pF	
I_{OS}	Output short current	-200		-30	mA	V_{IN}=VCC or GND
I_{OFF}	Output leakage current power off			100	µA	Vout=6V
				-100	µA	Vout=0.25V
I_{DC}	Output current			±150	mA	

DIFFERENTIAL LINE DRIVER TIMING



UARTS 3

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STARTECH
An EXAR Company

Printed August 3, 1995

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C1450/51 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.
The ST16C1450/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1450/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements.
The ST16C1450/51 provides internal loop-back capability for on board diagnostic testing.
The ST16C1450/51 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

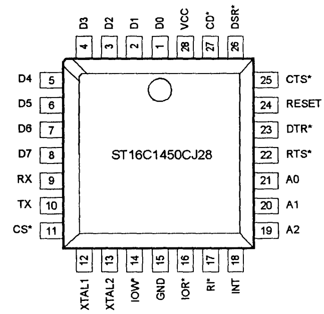
- Pin to pin and functional compatible to SSI 73M1450/2450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C450
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
- 28 Pin plastic-Dip and PLCC package
- Pin-to-pin compatible to ST16C1550/1551

ORDERING INFORMATION

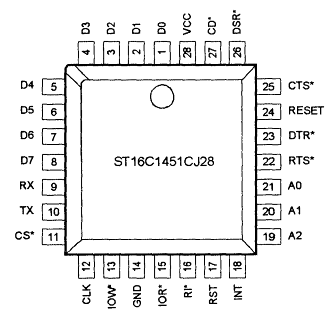
Part number	Package	Operating temperature
ST16C1450CP28	Plastic-DIP	0° C to + 70° C
ST16C1450CJ28	PLCC	0° C to + 70° C
ST16C1450CQ48	TQFP	0° C to + 70° C
ST16C1451CP28	Plastic-DIP	0° C to + 70° C
ST16C1451CJ28	PLCC	0° C to + 70° C
ST16C1451CQ48	TQFP	0° C to + 70° C

***Industrial operating range are available.**

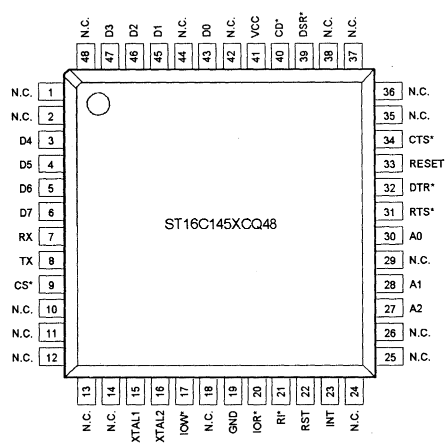
ST16C1450 PLCC Package



ST16C1451 PLCC Package

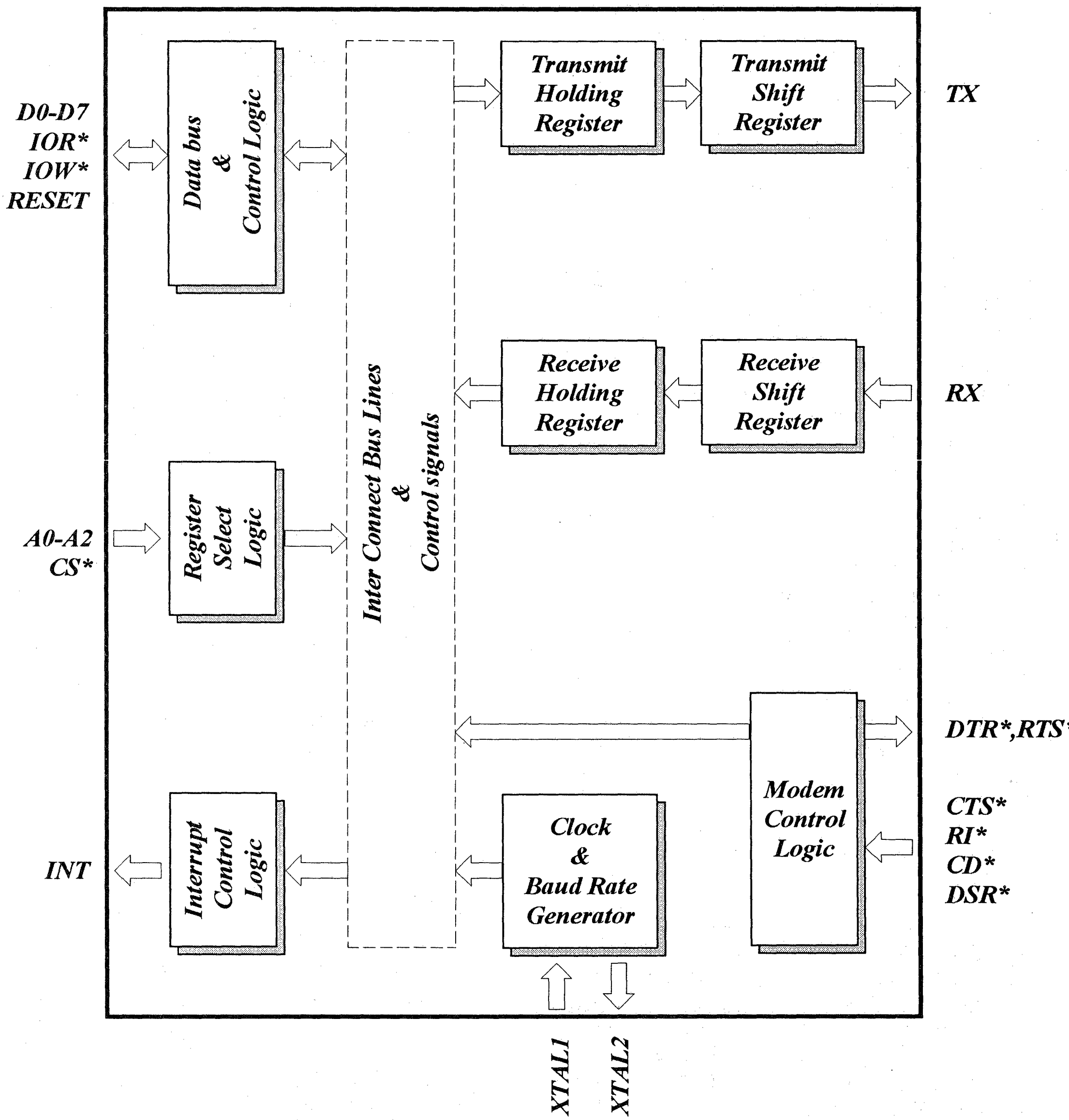


ST16C145X QFP Package

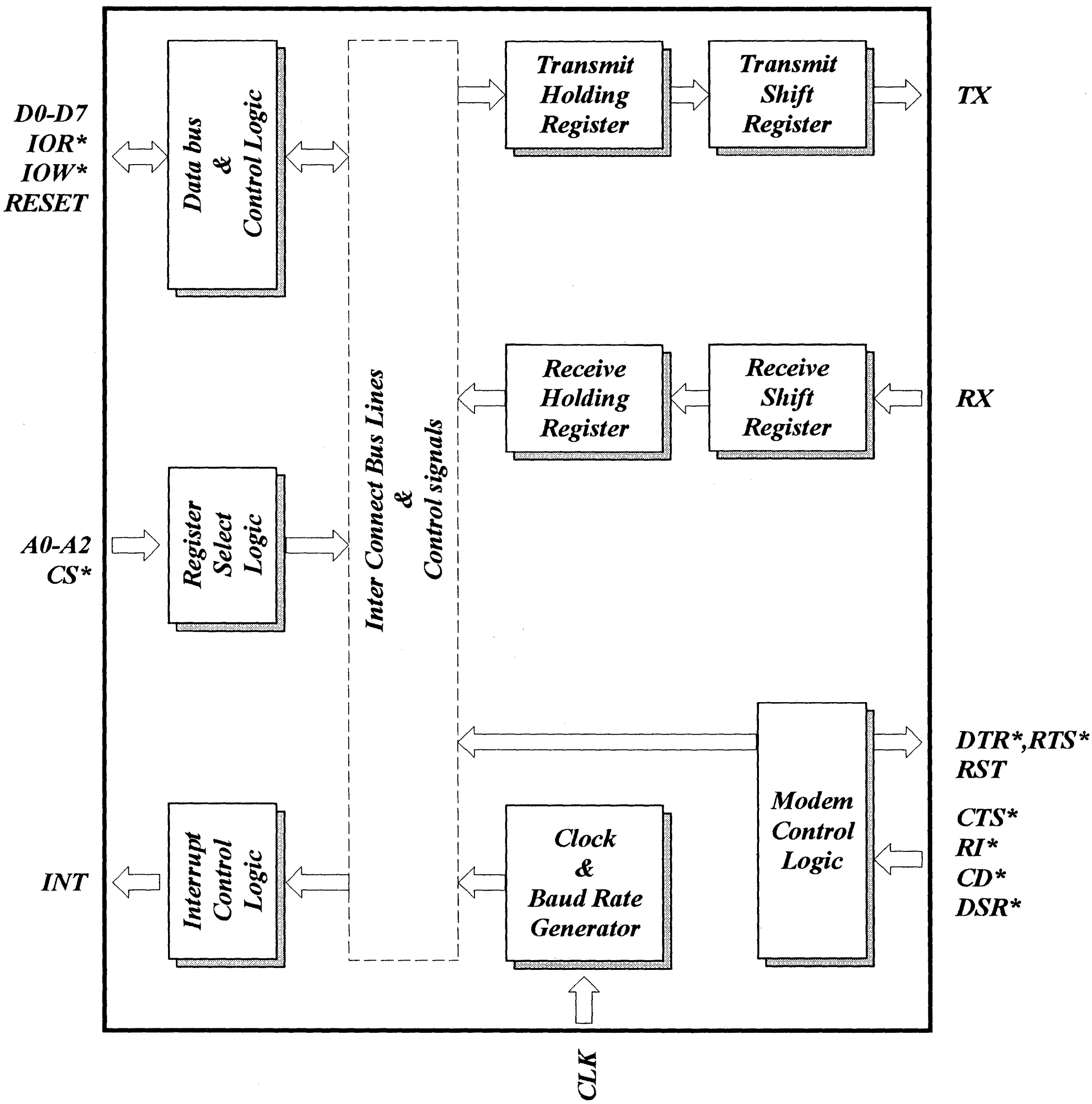


Rev. 1.0

ST16C1450 BLOCK DIAGRAM



ST16C1451 BLOCK DIAGRAM



ST16C1450
ST16C1451

SYMBOL DESCRIPTION (ST16C1450 - ST16C1451)

Symbol	Pin 28	Pin 28	Signal Type	Pin Description
D0-D7	1-8	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	9	I	Serial data input. The serial information (data) received from serial port to ST16C145X receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	10	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	11	I	Chip select (active low). A low at this pin enables the ST16C145X / CPU data transfer operation.
XTAL1	12	-	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
CLK	-	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	-	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	14	O	Signal and power ground.
IOR*	16	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C145X data bus to the CPU..
RI*	17	16	I	Ring detect indicator (active low). A low on this pin indicates

SYMBOL DESCRIPTION (ST16C1450 - ST16C1451)

Symbol	Pin 28	Pin 28	Signal Type	Pin Description
				the modem has received a ringing signal from telephone line.
RST	-	17	O	Reset output (active high). The ST16C1451 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	21-19	I	Address select line. To select internal registers.
RTS*	22	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	23	O	Data terminal read (active low). To indicate that ST16C145X is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin

ST16C1450
ST16C1451

SYMBOL DESCRIPTION (ST16C1450 - ST16C1451)

Symbol	Pin 28	Pin 28	Signal Type	Pin Description
				does not have any effect on the transmit or receive operation.
CD*	27	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	28	I	Power supply input.

All unused input pins should be tied to VCC or GND.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C1450/51 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1450/51 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT-5:
0=normal ST16C450 mode.
1=special mode. Enable power down and SOFT rest.

IER BIT 4,6-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1450/51 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1450/51 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority levels

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR bit 3-7:
Not used

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-6:
Not used. Are set to zero permanently.

MCR bit-7:
0=normal mode.
1=power down mode. XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C1450/51 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C1450/51 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.
Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1450/51 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

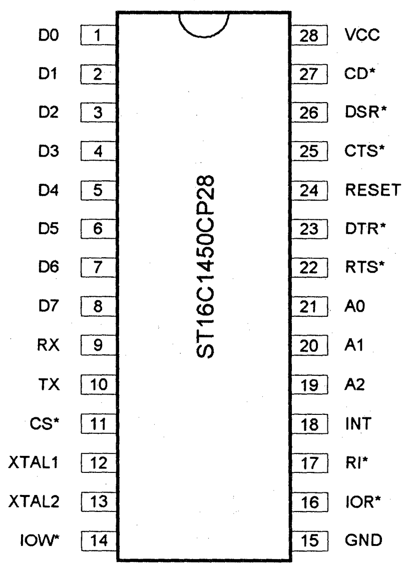
ST16C1450/51 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

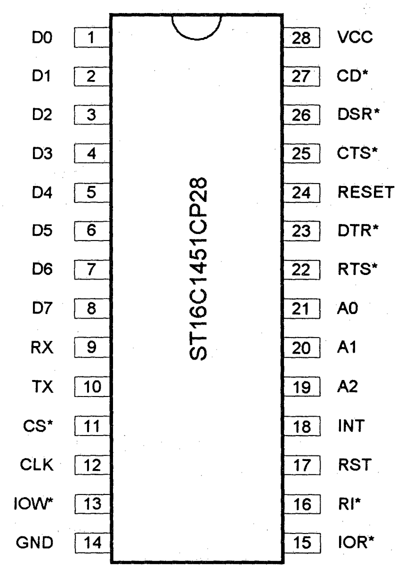
SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state mode

ST16C1450
ST16C1451

ST16C1450 Plastic-DIP Package



ST16C1451 Plastic-DIP Package



ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

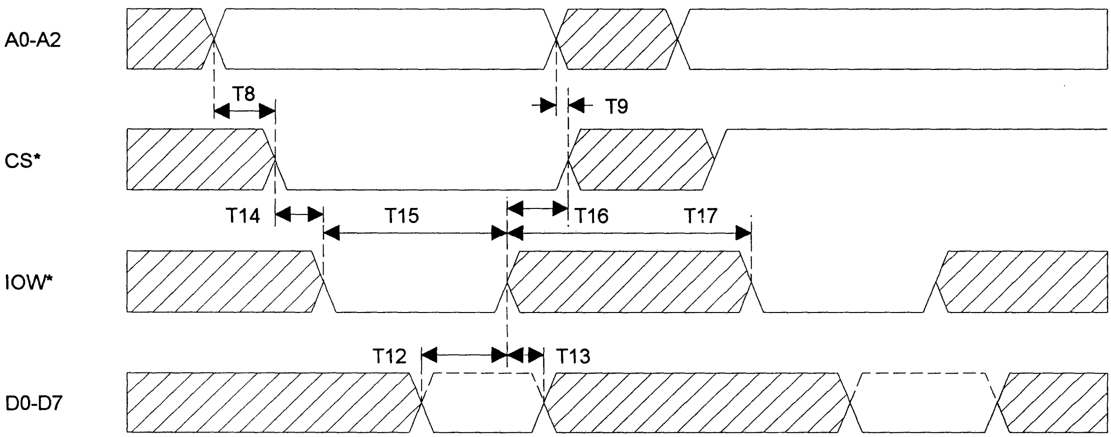
ST16C1450
ST16C1451

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

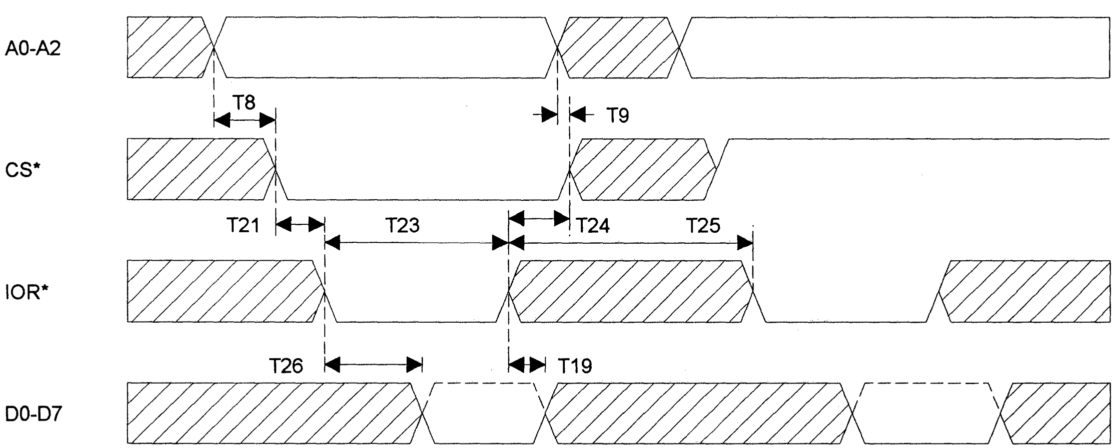
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	105			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	*	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2_{16}-1		

GENERAL WRITE TIMING



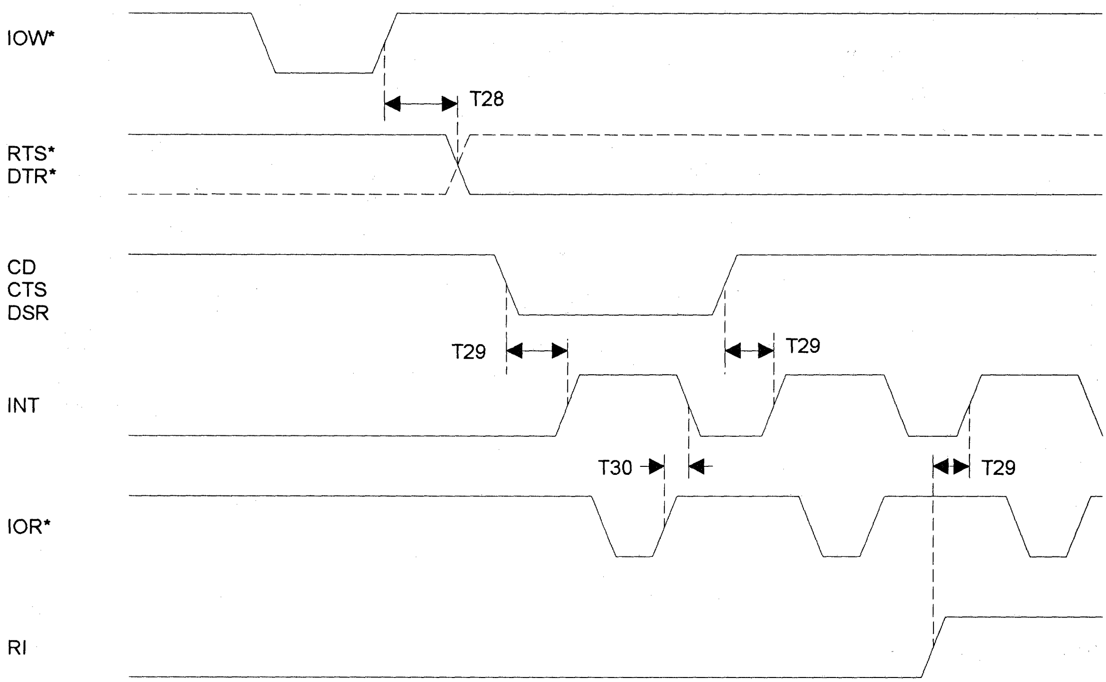
161450-WD-1

GENERAL READ TIMING



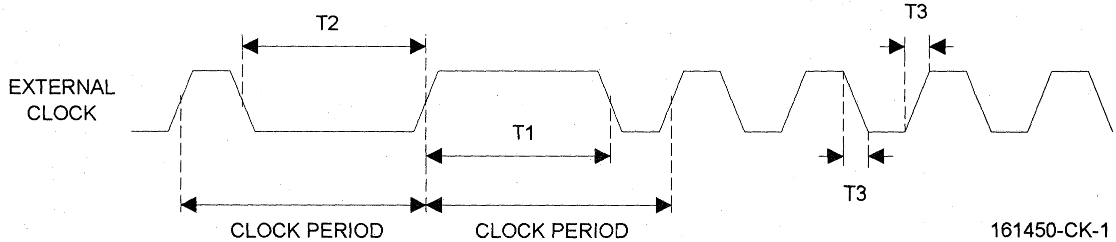
161450-RD-1

MODEM TIMING



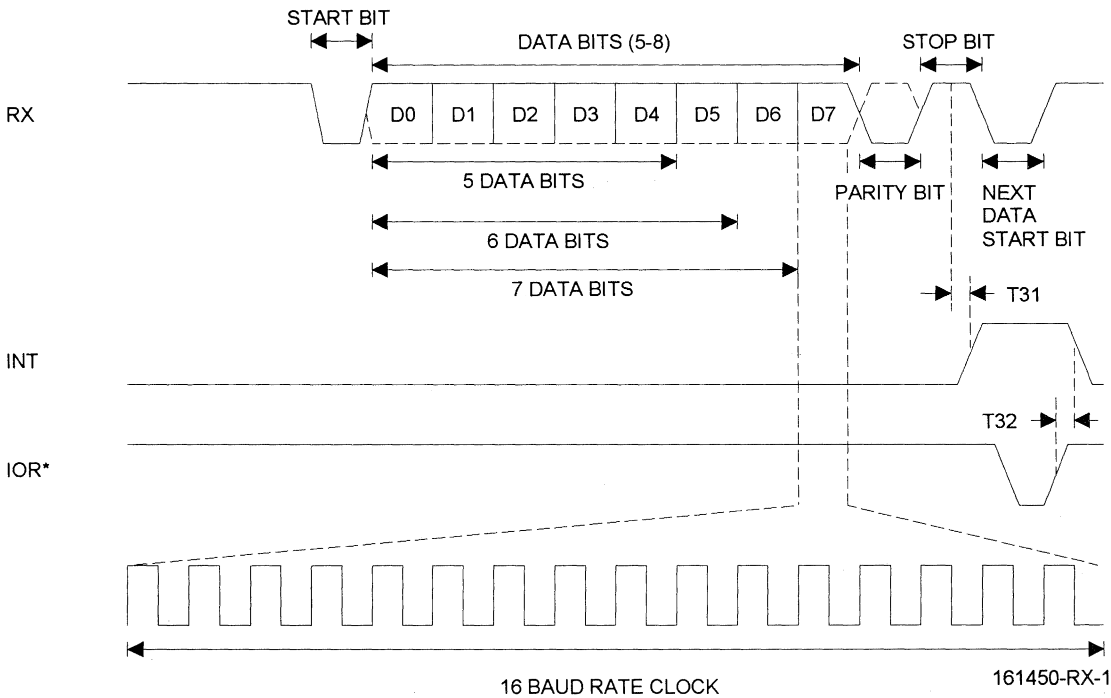
161450-MD-1

CLOCK TIMING

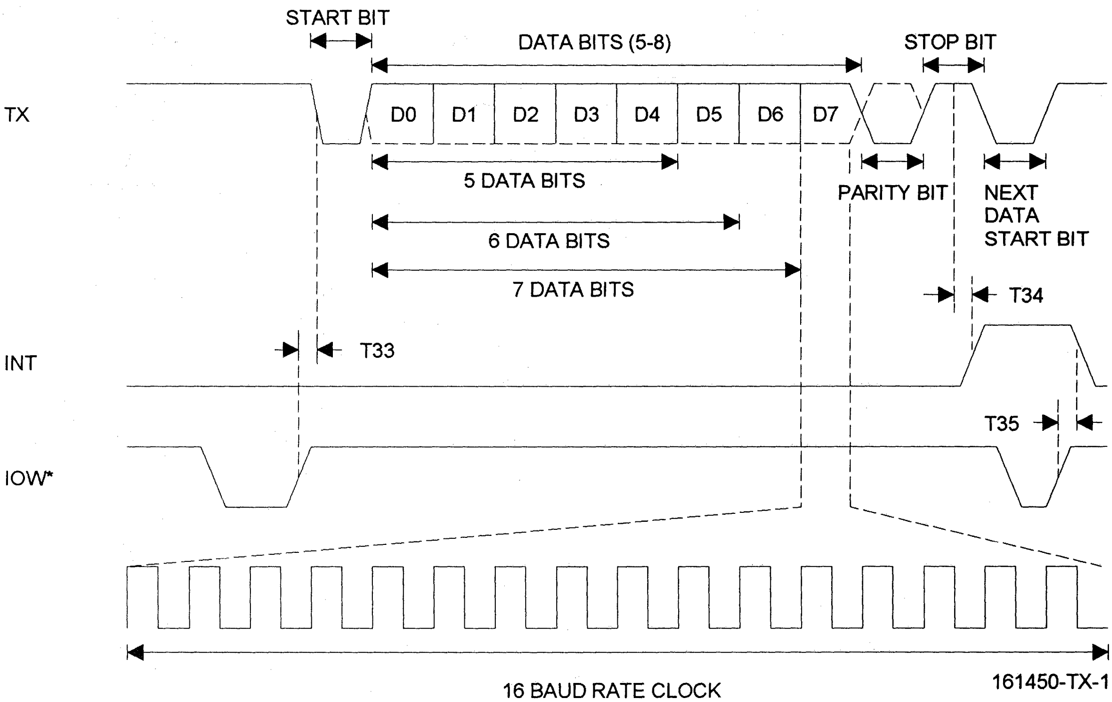


161450-CK-1

RECEIVE TIMING



TRANSMIT TIMING



STARTECH
An EXAR Company

ST16C2450

Printed August 3, 1995

DUAL UNIVERSAL ASYNCHRONOUSRECEIVER/TRANSMITTER

DESCRIPTION

The ST16C2450 is a dual universal asynchronous receiver and transmitter. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 1.5 MHz for each UART section.

The ST16C2450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C2450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2450 provides internal loop-back capability for on board diagnostic testing.

The ST16C2450 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

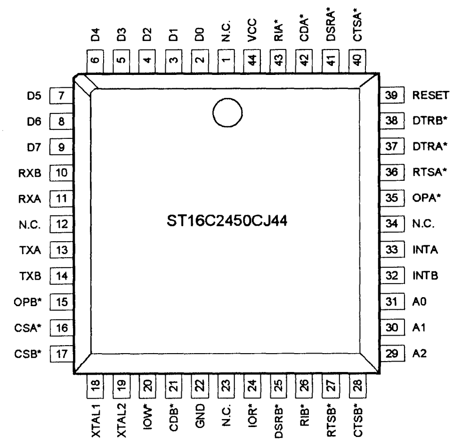
- Functional compatible to NS16450, VL16C450, WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

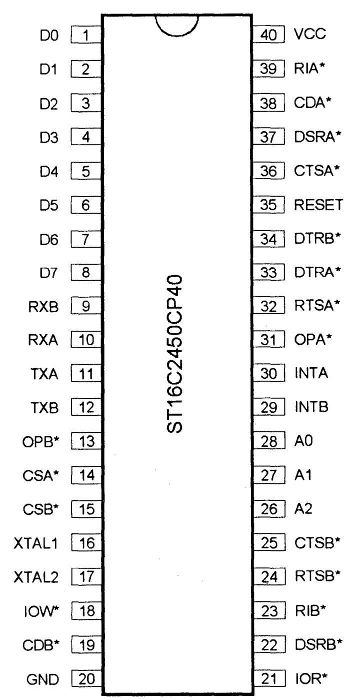
Part number	Package	Operating temperature
ST16C2450CP40	Plastic-DIP	0° C to + 70° C
ST16C2450CJ44	PLCC	0° C to + 70° C

***Industrial operating range are available**

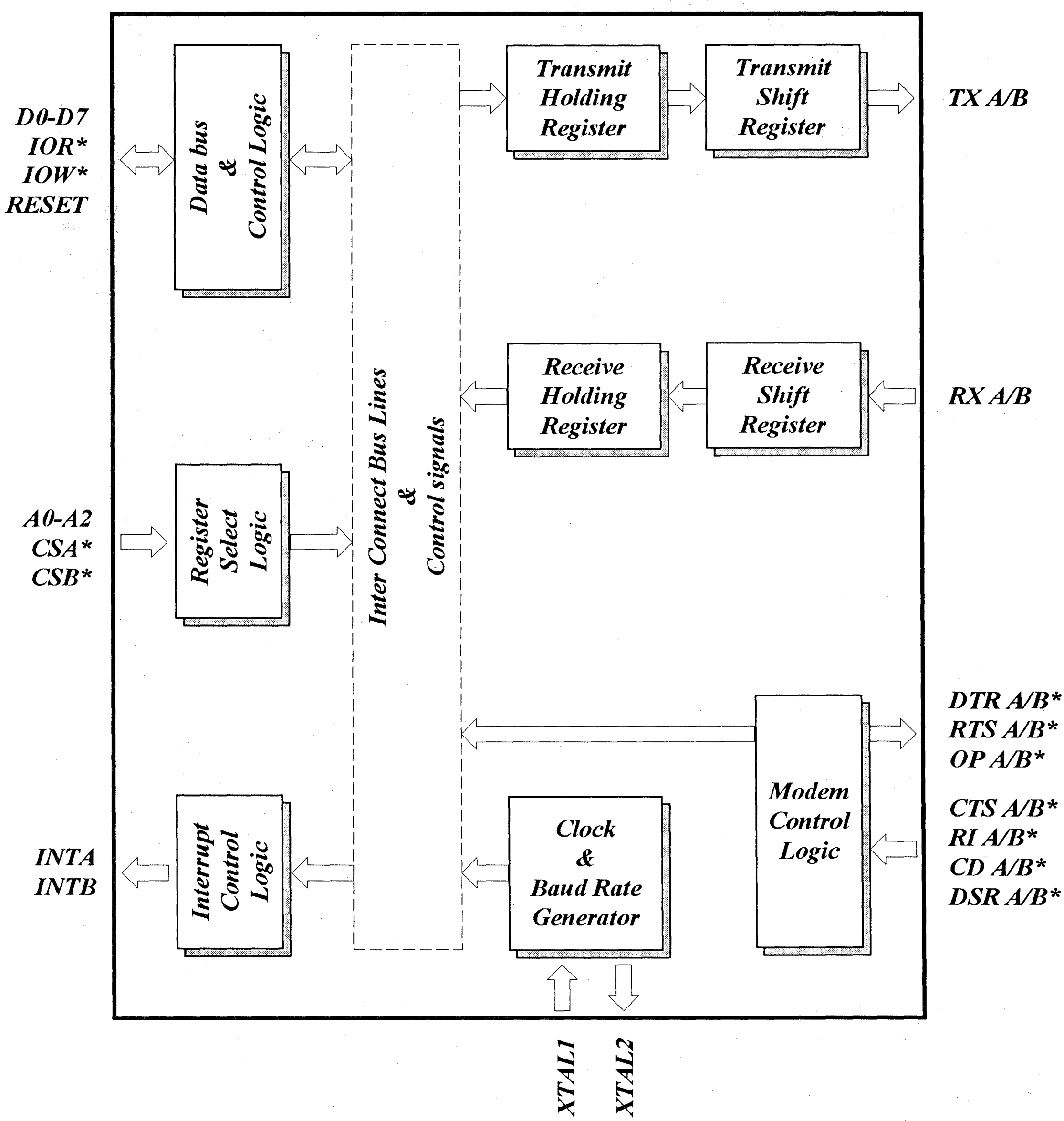
PLCC Package



Plastic-DIP Package



BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
D0-D7	1-8	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	11,10	10,9	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	13,14	O	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS* A/B	14,15	16,17	I	Chip select A/B. (active low) A low at this pin enables the ST16C2450 / CPU data transfer operation.
XTAL1	16	18	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	19	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	24	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2450 data bus to the CPU.
A0-A2	28-26	31-29	I	Address select lines. To select internal registers.
INT A/B	30,29	33,32	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
OP*A/B	31,13	35,15	O	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
RTS* A/B	32,24	36,27	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* A/B	33,34	37,38	O	Data terminal ready A/B (active low). To indicate that ST16C2450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	35	39	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS* A/B	36,25	40,28	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR* A/B	37,22	41,25	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD* A/B	38,19	42,21	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI* A/B	39,23	43,26	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
VCC	40	44	I	Power supply input.
GND	20	22	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C2450 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2/ INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS A/B

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
not used except in local loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode and OP2* output to high.
1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and OP2*/INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C2450 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2*/INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state mode

SCRATCHPAD REGISTER (SR)

ST16C2450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signal

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	15			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

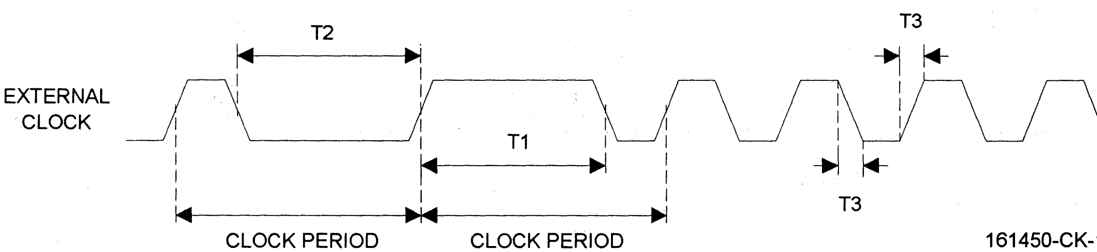
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

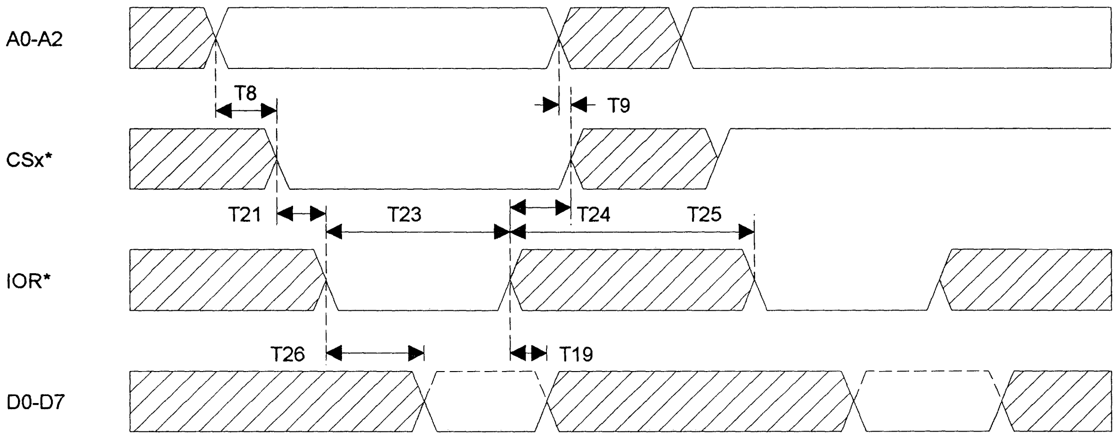
This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

CLOCK TIMING



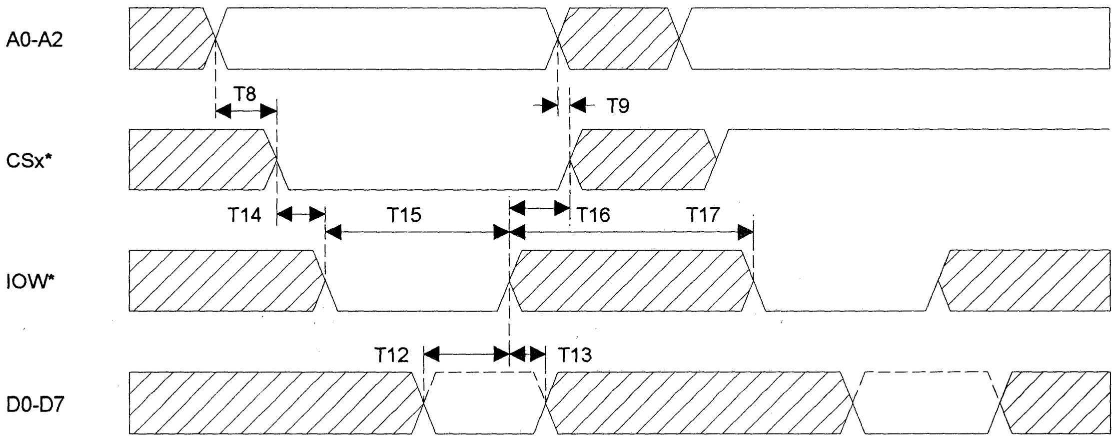
161450-CK-1

GENERAL READ TIMING



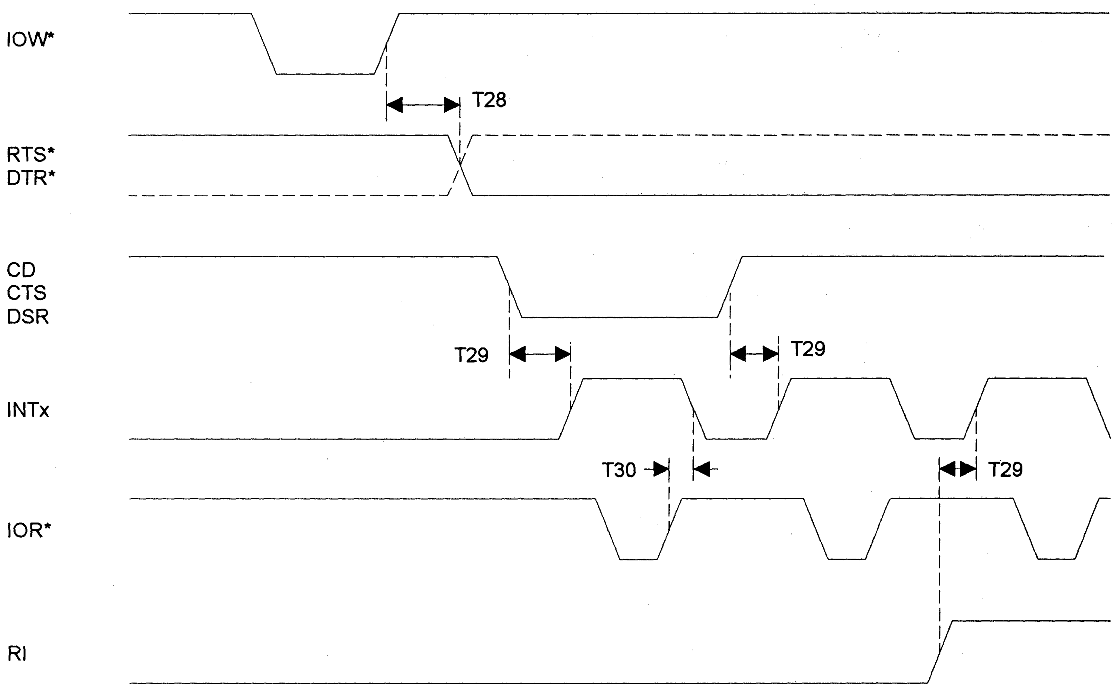
162450-RD-1

GENERAL WRITE TIMING



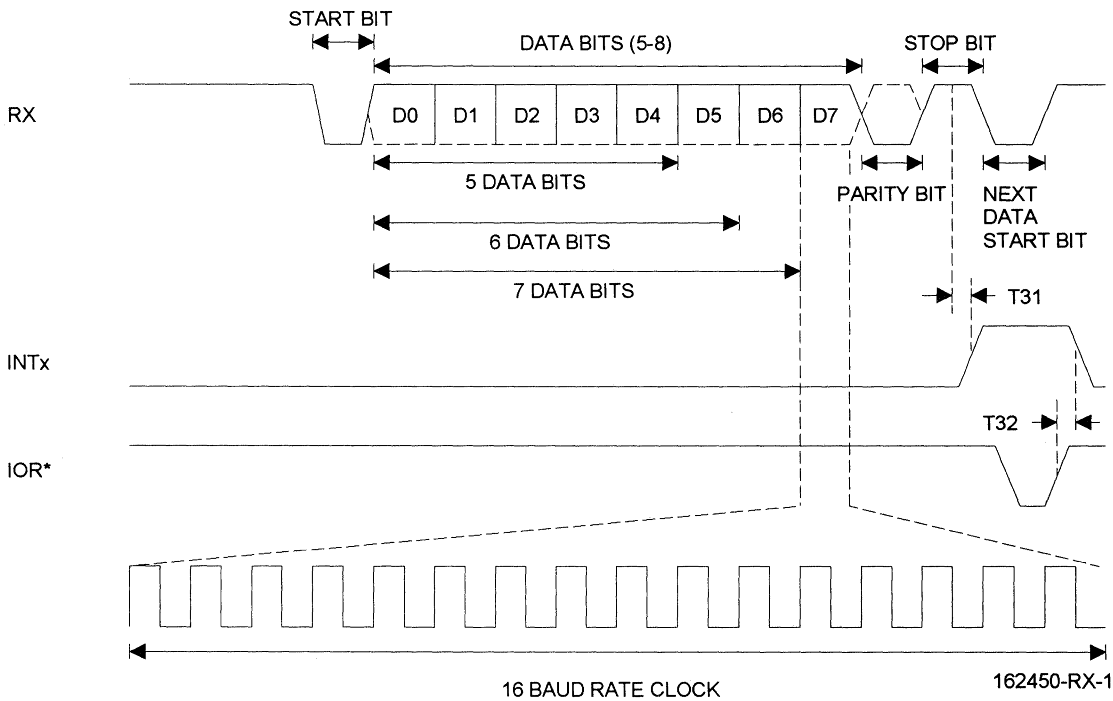
162450-WD-1

MODEM TIMING

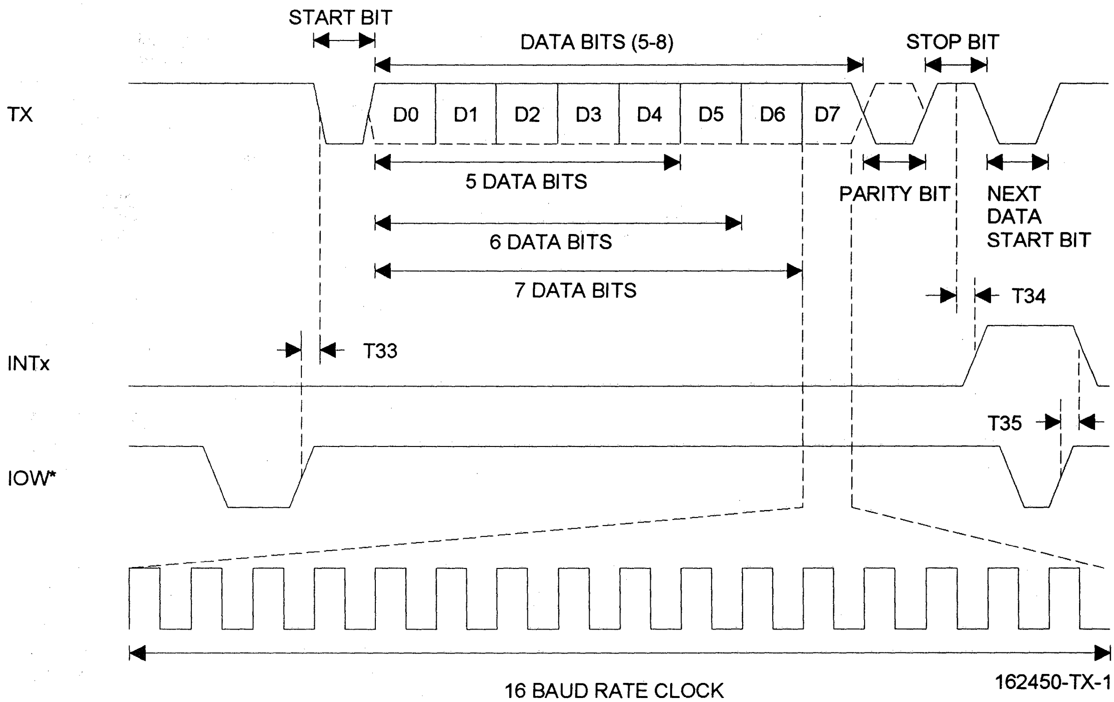


162450-MD-1

RECEIVE TIMING



TRANSMIT TIMING



STARTECH
An EXAR Company

ST16C450

Printed August 3, 1995

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

3

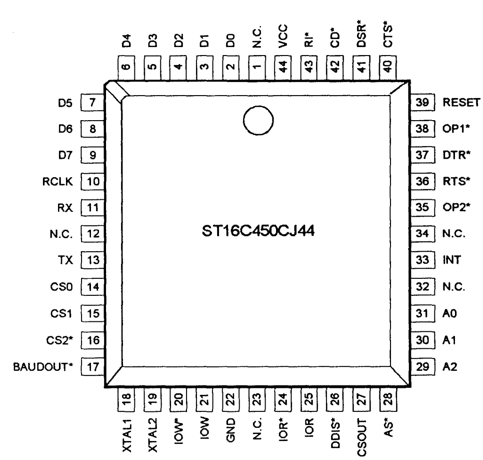
DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

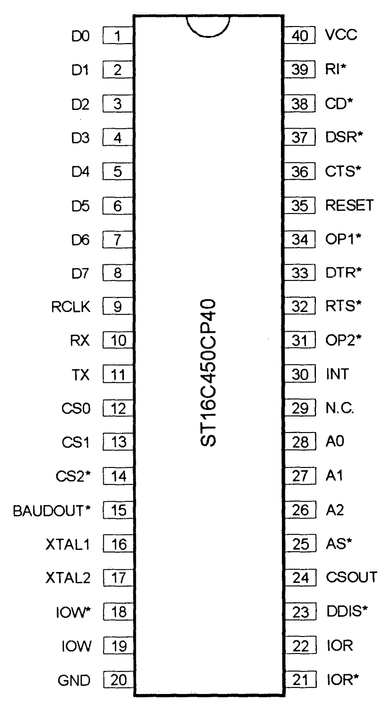
The ST16C450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C450 provides internal loop-back capability for on board diagnostic testing.

The ST16C450 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

- Pin to pin and functional compatible to NS16450,VL16C450,WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

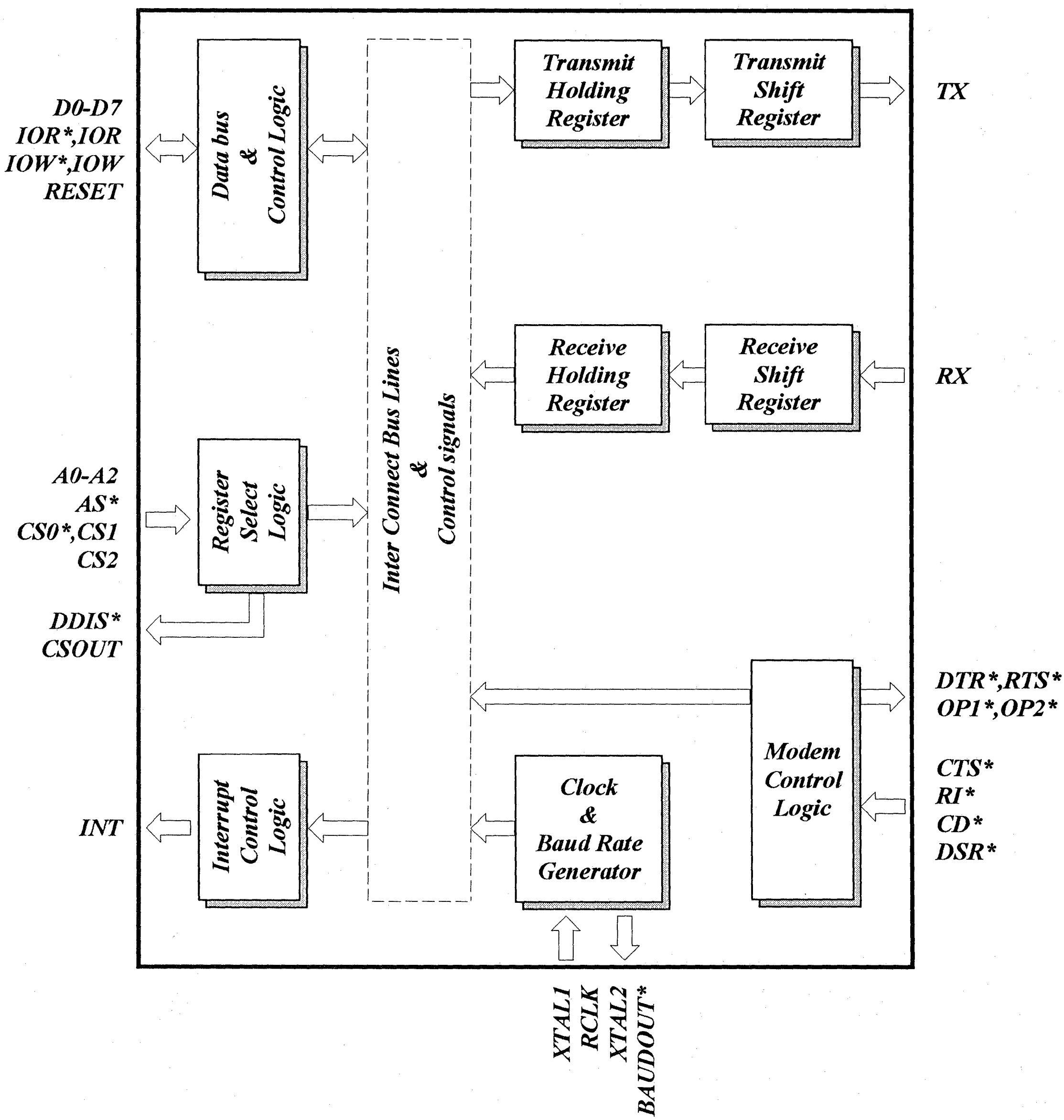
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C450CP40	Plastic-DIP	0° C to + 70° C
ST16C450CJ44	PLCC	0° C to + 70° C
ST16C450CQ48	TQFP	0° C to + 70° C

*** Industrial operating range are available.**

Rev. 1.0

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
D0-D7	1-8	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	10	I	Receive clock input. The external clock input to the ST16C450 receiver section if receiver data rate is different from transmitter data rate.
RX	10	11	I	Serial data input. The serial information (data) received from serial port to ST16C450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	13	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	14	I	Chip select 1 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS1	13	15	I	Chip select 2 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS2*	14	16	I	Chip select 3 (active low). A low at this pin (while CS0=1 and CS1=1) will enable the ST16C450 / CPU data transfer operation.
BAUDOUT*	15	17	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide the receiver clock.
XTAL1	16	18	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
XTAL2	17	19	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	20	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	21	I	Write strobe (active high). Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C450 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	22	O	Signal and power ground.
IOR*	21	24	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C450 data bus to the CPU.
IOR	22	25	I	Read strobe (active high). Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C450 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23	26	O	Drive disable (active low). This pin goes low when the CPU is reading data from the ST16C450 to disable the external transceiver or logic's.
CSOUT	24	27	O	Chip select out. A high on this pin indicates that the ST16C450 has been enabled by the chip select pin.
AS*	25	28	I	Address strobe (active low). A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	29	I	Address select line 2. To select internal registers.
A1	27	30	I	Address select line 1. To select internal registers.
A0	28	31	I	Address select line 0. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
INT	30	33	O	Interrupt output (active high). This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	35	O	General purpose output (active low). User defined output. See bit-3 modem control register (MCR bit-3).
RTS*	32	36	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	37	O	Data terminal ready (active low). To indicate that ST16C450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	38	O	General purpose output (active low). User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	35	39	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	40	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	37	41	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
CD*	38	42	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
RI*	39	43	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	44	I	Power supply input.

All unused input pins should be tied to VCC or GND.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C450 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2_{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:
0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C450 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C450 provides a temporary data register to store 8 bits of information for variable use.

SIGNAL	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
INT	Low

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

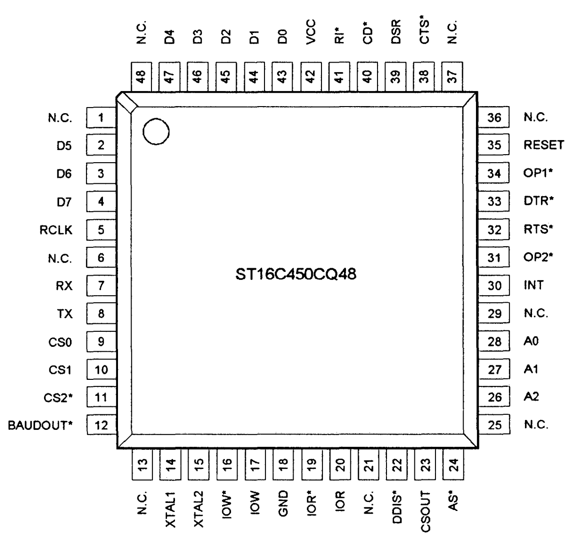
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	15			ns	
T_7	Address hold time	15			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select			10	ns	
T_{11}	IOR* to DDIS* delay			35	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	55			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	25			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data	25			ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	*	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2_{16}-1		

Note 1: Applicable only when AS* is tied low.



ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

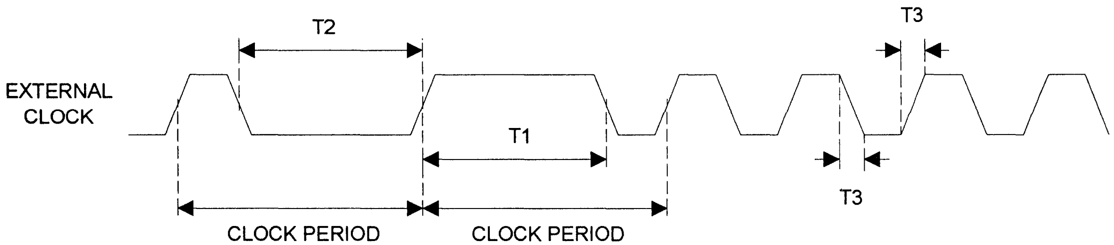
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70 C, Vcc=5.0 V ± 10% unless otherwise specified.

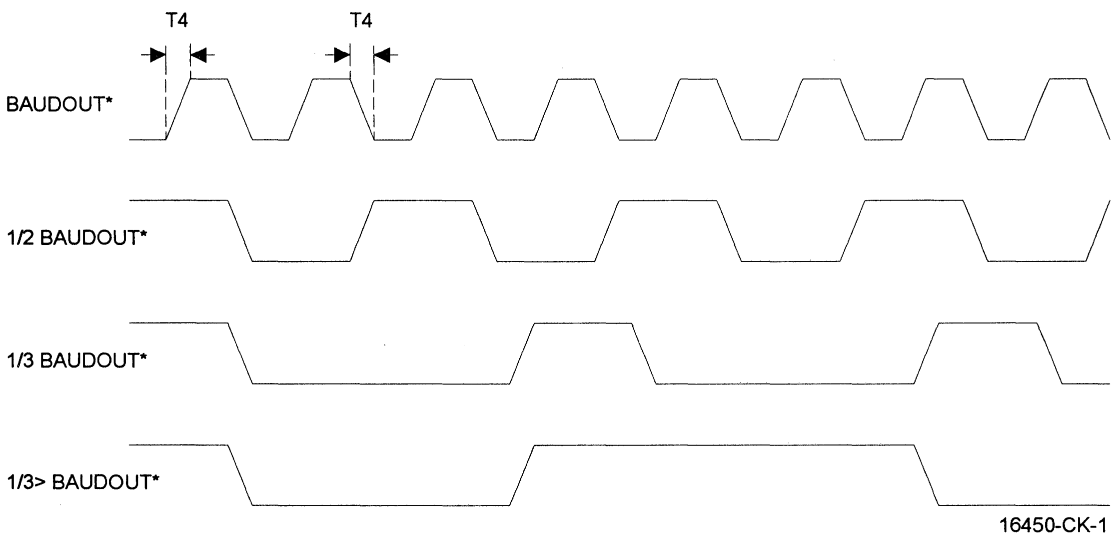
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

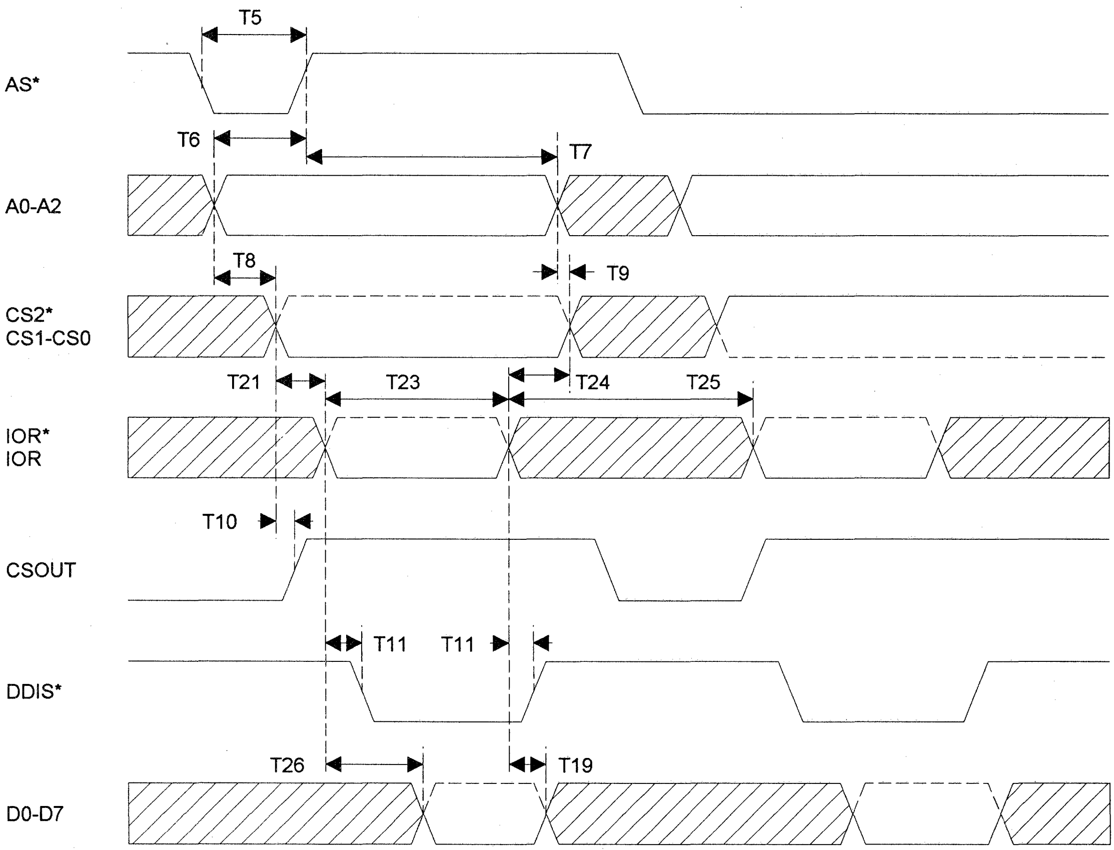
CLOCK TIMING



BAUDOUT* TIMING

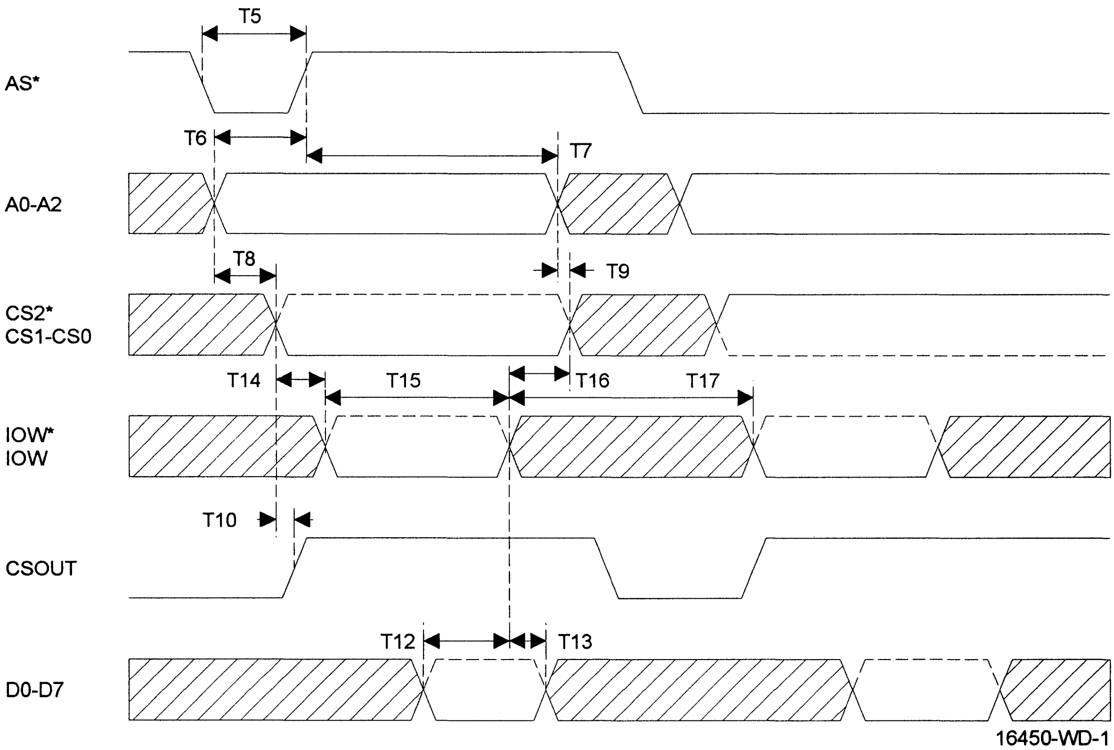


GENERAL READ TIMING

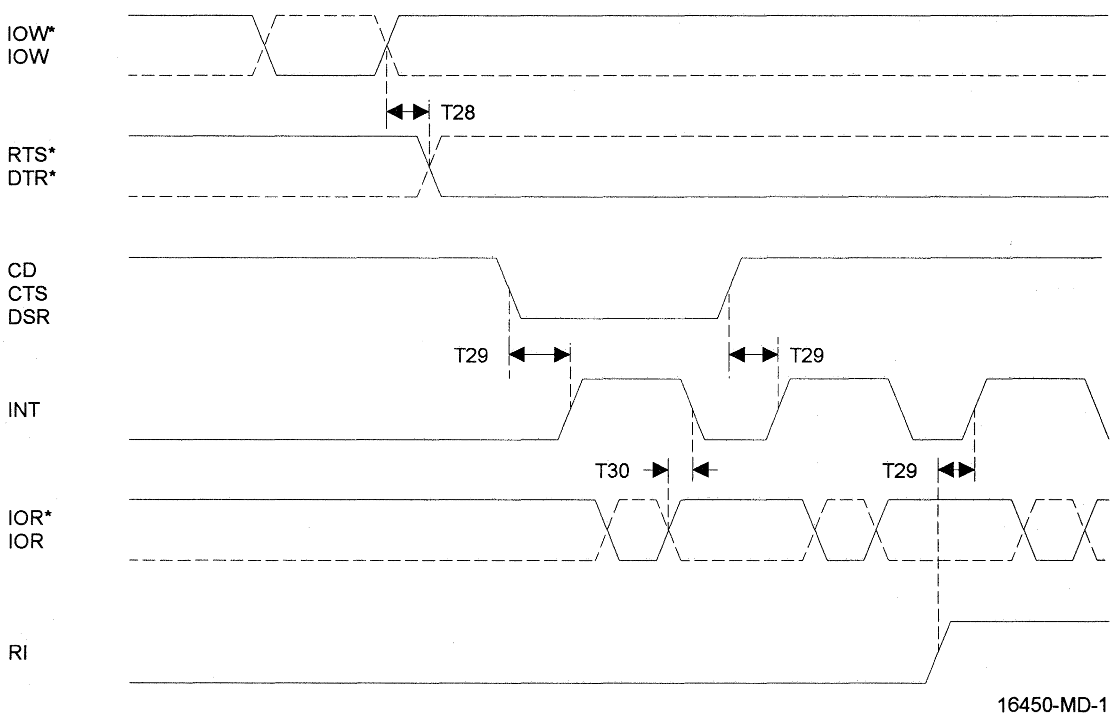


16450-RD-1

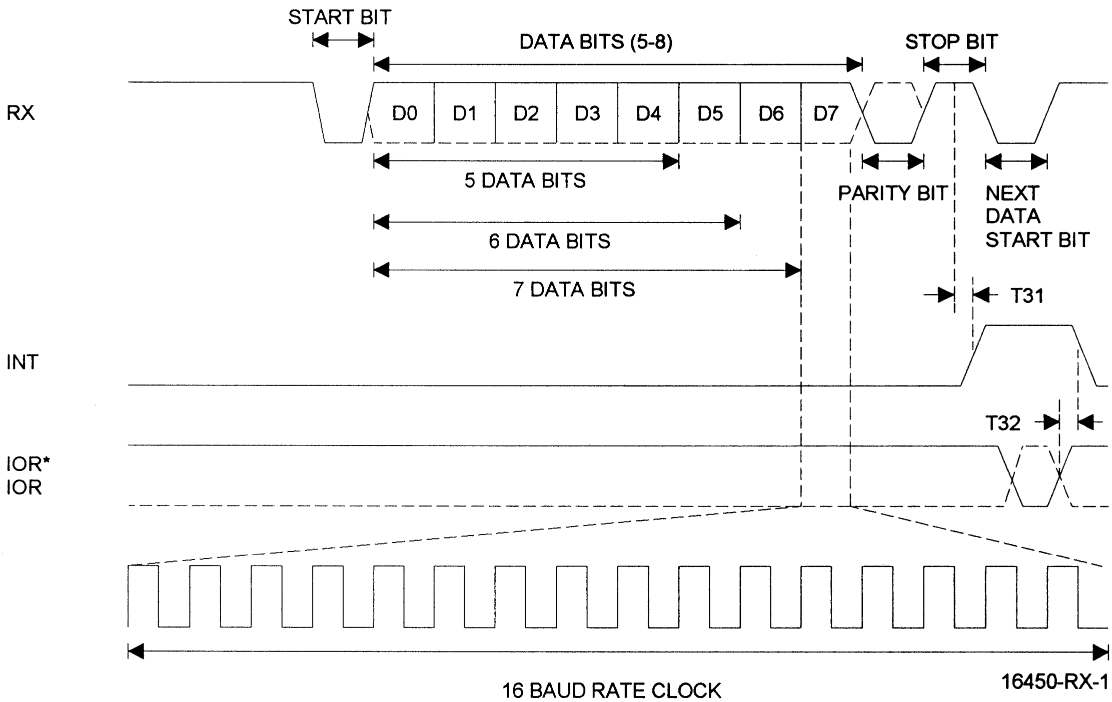
GENERAL WRITE TIMING



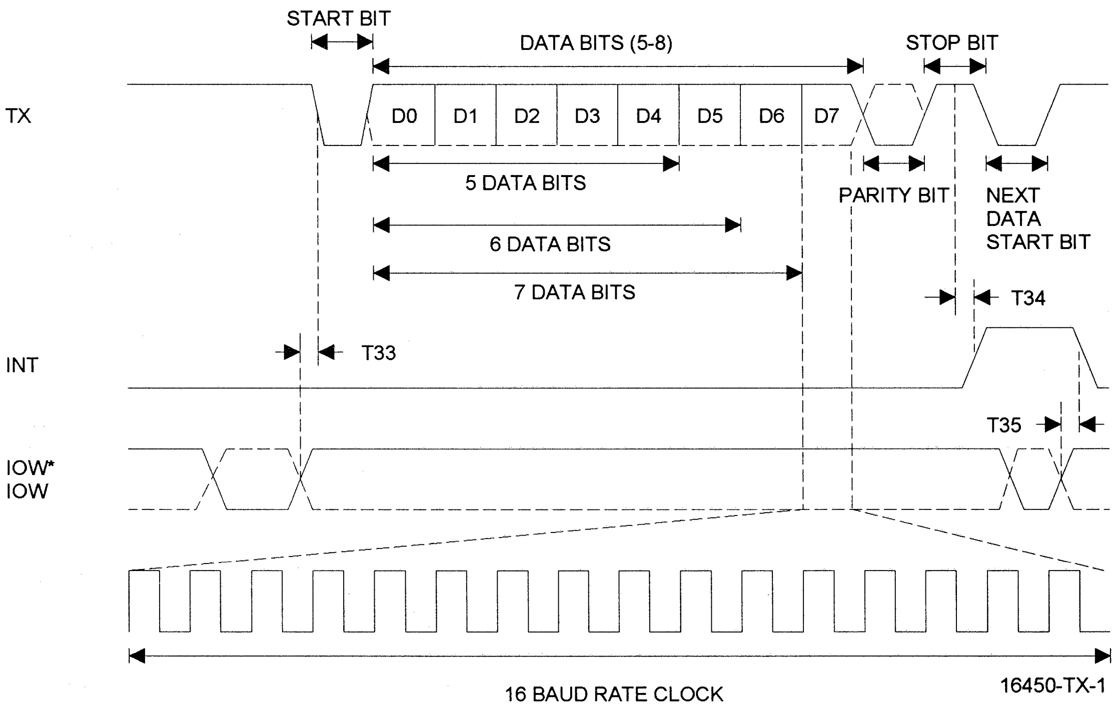
MODEM TIMING



RECEIVE TIMING



TRANSMIT TIMING



STARTECH

An EXAR Company

ST16C454

Printed August 3, 1995

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

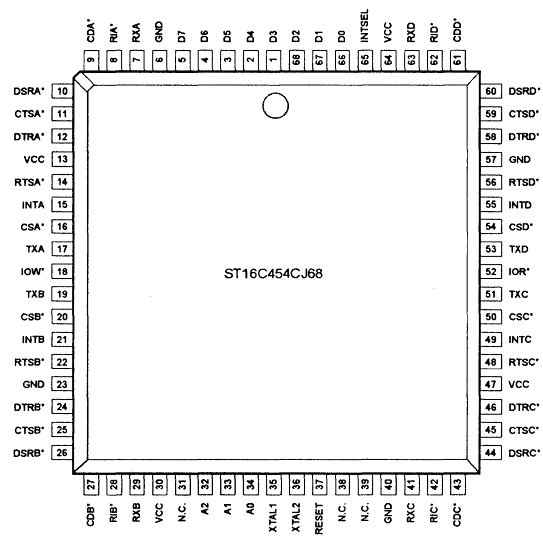
DESCRIPTION

The ST16C454 is a quad universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

The ST16C454 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C454 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C454 provides internal loop-back capability for on board diagnostic testing.

The ST16C454 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

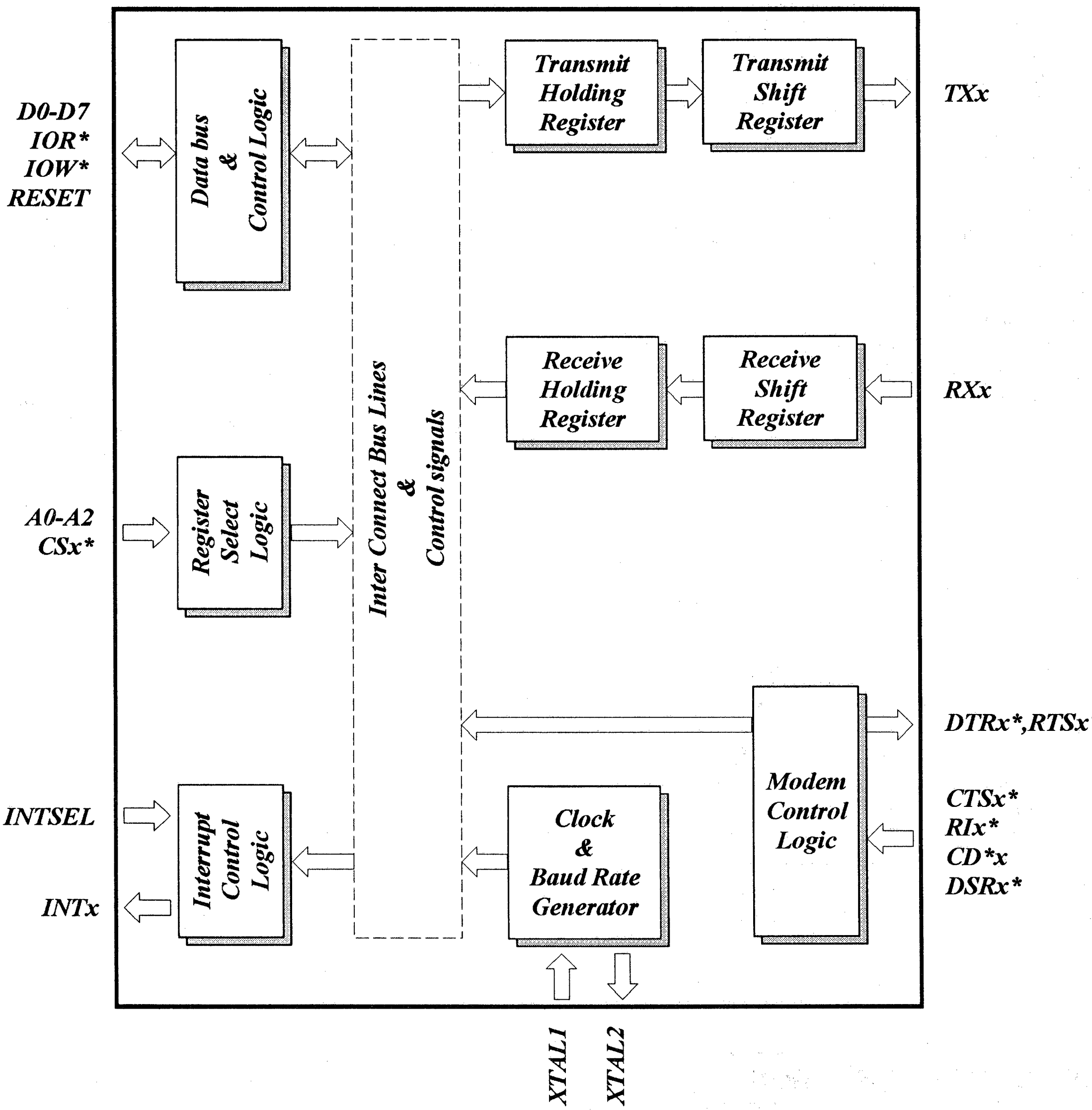
- Quad ST16C450
- Pin-to-pin compatible to ST16C554
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C454CJ68	PLCC	0° C to + 70° C
ST16C454IJ68	PLCC	-40° C to + 85° C

Rev. 1.0

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input. The serial information (data) received from serial port to ST16C454 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS* A-B CS* C-D	16,20 50,54	I	Chip select (active low). A low at this pin enables the ST16C454 / CPU data transfer operation. Each UART section of the ST16C454 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	O	Signal and power ground.
IOR*	52	I	Read strobe (active low.) A low level on this pin transfers the contents of the ST16C454 data bus to the CPU.
INTSEL	65	I	Interrupt type select. Enable /disable the interrupt three state function. Normal interrupt output can be selected by connecting this pin to VCC (MCR bit-3 does not have any effect on the interrupt output). The three state interrupt output is selected when this pin is left open or connected to

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			GND and MCR bit-3 is set to "1".
A2	32	I	Address select line 2. To select internal registers.
A1	33	I	Address select line 1. To select internal registers.
A0	34	I	Address select line 0. To select internal registers.
INT A-B INT C-D	15,21 49,55	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS* A-B RTS* C-D	14,22 48,56	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* A-B DTR* C-D	12,24 46,58	O	Data terminal ready. (active low) To indicate that ST16C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS* A-B CTS* C-D	11,25 45,59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR* A-B DSR* C-D	10,26 44,60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			does not have any effect on the transmit or receive operation.
CD* A-B CD* C-D	9,27 43,61	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI* A-B RI* C-D	8,28 42,62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13,30 47,64	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C454 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2_{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C454 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except, in internal loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C454 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C454 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C454 provides a temporary data register to store 8 bits of information for variable use.

SIGNALS	RESET STATE
TX A-D	High
RTS* A-D	High
DTR* A-D	High
INT A-D	Three state

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
MSR	BITS 4-7=input signals

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	15			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

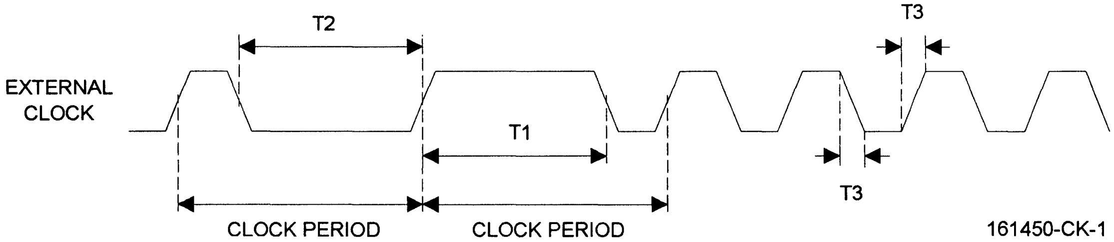
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

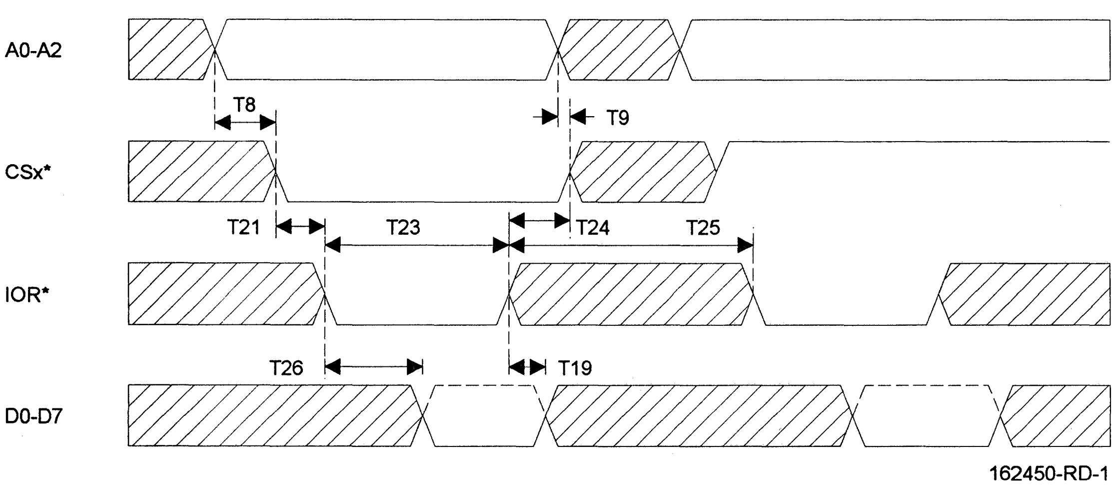
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

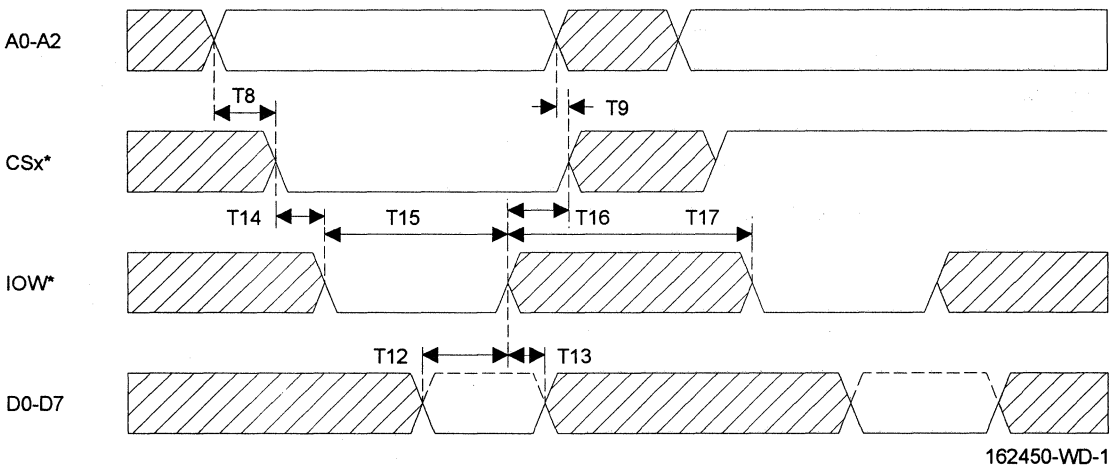
CLOCK TIMING



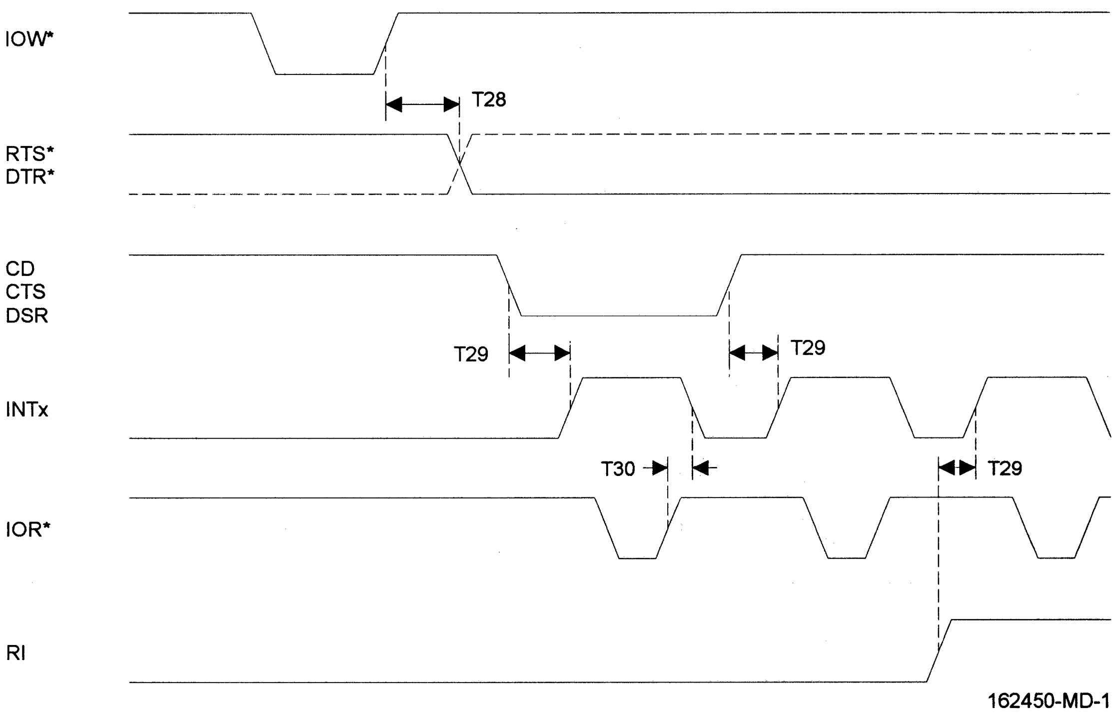
GENERAL READ TIMING



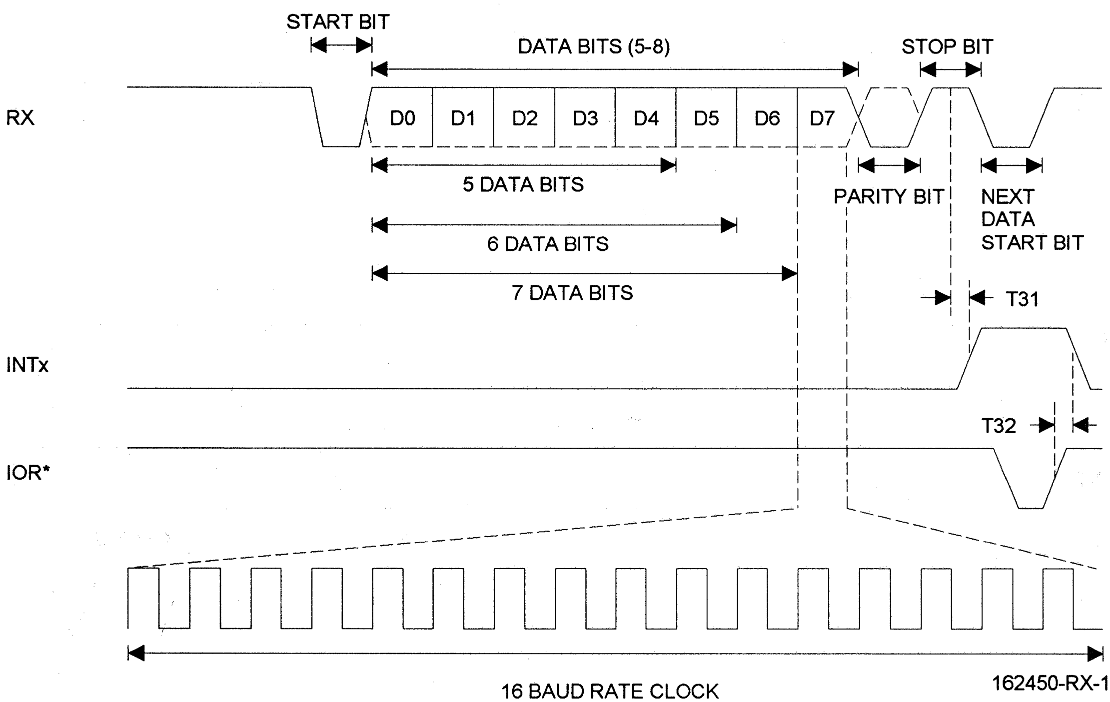
GENERAL WRITE TIMING



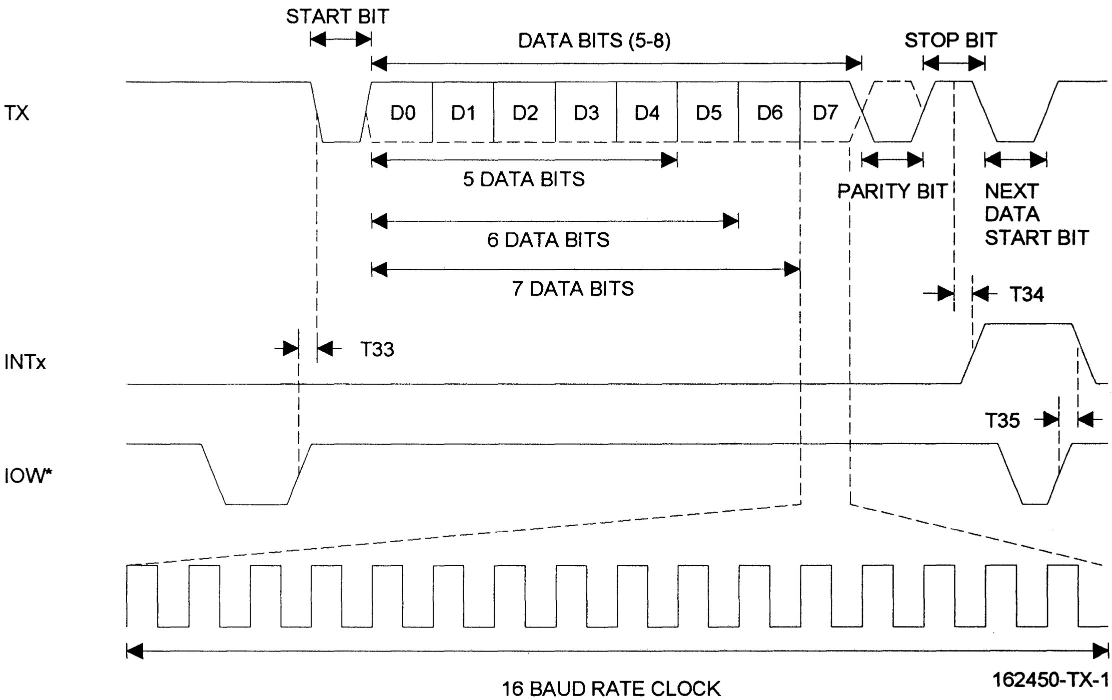
MODEM TIMING



RECEIVE TIMING



TRANSMIT TIMING



STARTECH

An EXAR Company

ST68C454

Printed August 3, 1995

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

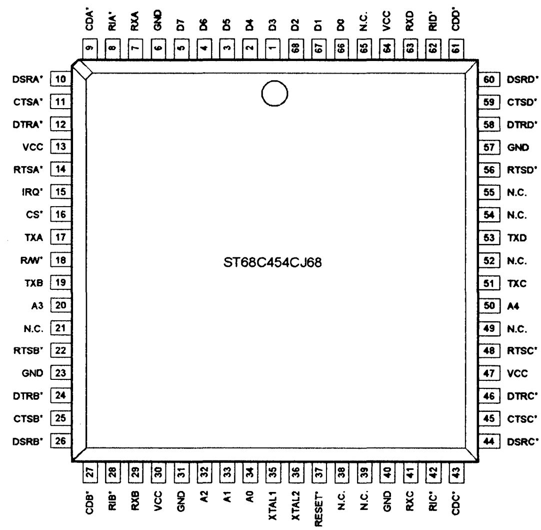
DESCRIPTION

The ST68C454 is a quad universal asynchronous receiver and transmitter with modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular micro-processors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

The ST68C454 is an improved, quad version of the NS16450 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C454 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



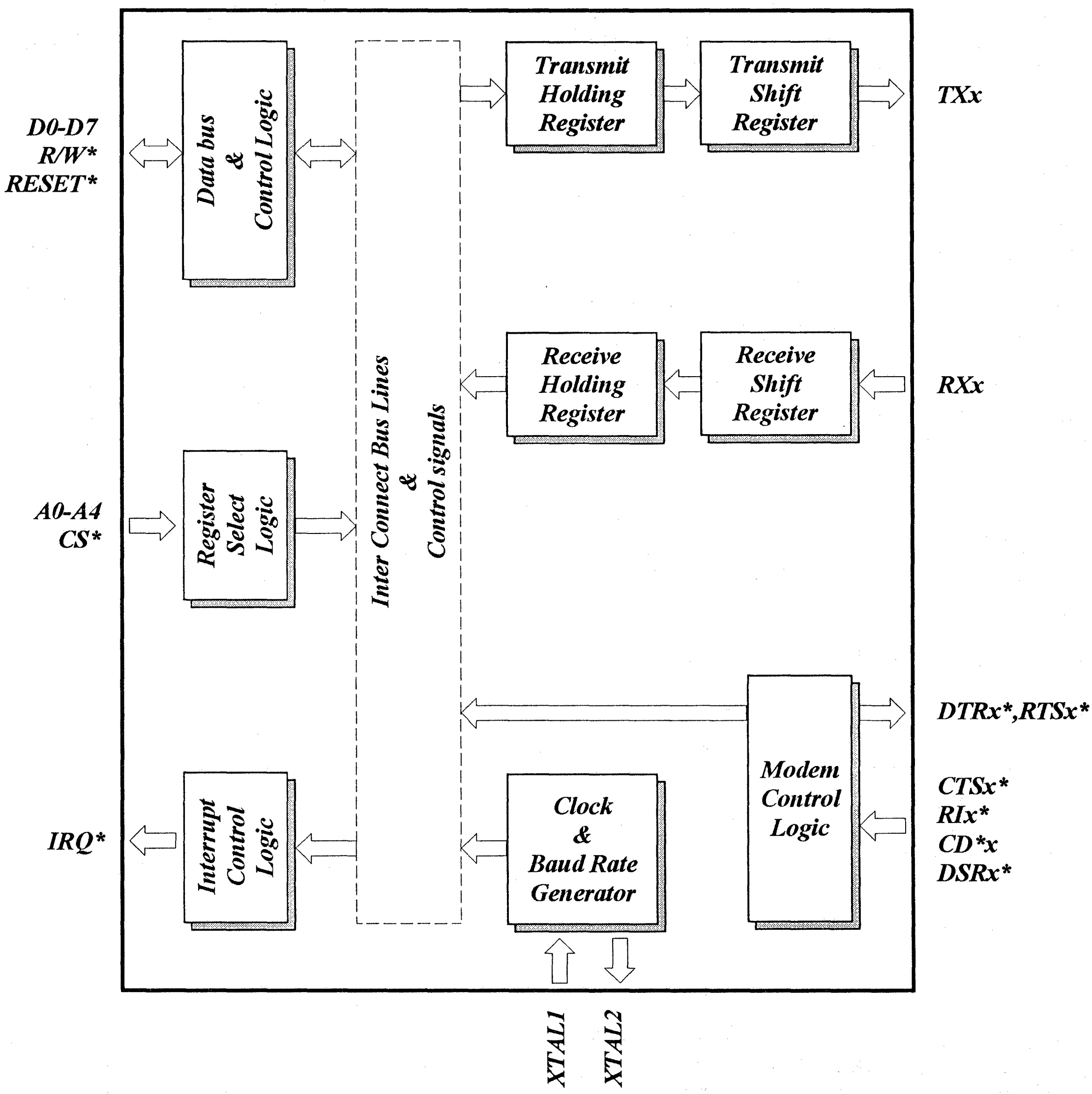
FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C450
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- 460.8 kHz transmit/receive operation with 7.372 MHz external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C454CJ68	PLCC	0° C to +70° C
ST68C454IJ68	PLCC	-40° C to +85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66	I/O	Bi-directional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B RX C/D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST68C454 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B TX C/D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	16	I	Chip select (active low). A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2. See XTAL1.
R/W*	18	I	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C454 data bus to the CPU.
CD* A/B CD* C/D	9,27 43,61	I	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23,31 40,57	O	Signal and power ground.
DSR* A/B DSR* C/D	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
RI* A/B RI* C/D	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTS* A/B RTS* C/D	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS* A/B CTS* C/D	11,25 45,59	I	Clear to send A-D. (active low) The CTS* signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmitter output.
A4	50	I	Address line 4. To select one of the four UARTS.
A3	20	I	Address line 3. To select one of the four UARTS.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
IRQ*	15	O	Interrupt output. (active low open collector) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR* A/B DTR* C/D	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that ST68C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET*	37	I	Master reset. (active low) A low on this pin will reset all the

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC	13,30		
VCC	47,64	I	Power supply input.

SERIAL PORT SELECTION GUIDE

CS*	A4	A3	UART X
1	X	X	X
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

PROGRAMMABLE BAUD RATE GENERATOR

The ST68C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2_{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D

The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the IRQ* output pin.

IER BIT-0:
0=disable the receiver ready interrupt
1=enable the receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable the modem status register interrupt
1=enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST68C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C454 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set zero.

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.

0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TX A-D) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high
1=force DTR* output to low

MCR BIT-1:
0=force RTS* output to high
1=force RTS* output to low

MCR BIT2-3:
x=not used

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS* A-D, DSR* A-D, CD* A-D, and RI* A-D) are disabled. Internally, the transmitter output is connected to the receiver input and DTR* A-D, RTS* A-D and MCR A-D bit2,3 are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST68C454 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used, set to “0”.

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed

information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST68C454 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loop-back mode. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D
ST68C454 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16xCLOCK %ERROR	DVISOR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST68C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
RTS A-D*	High
DTR A-D*	High
IRQ	Three state mode

ST68C454 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	Not used	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, VCC=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time from write or CS*	5			ns	
T_{14}	Write set up time	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	15			ns	
T_{17}	Write cycle delay	45			ns	
T_{18}	Data setup time	15			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{24}	Data hold time	0			ns	
T_{25}	Read cycle delay	25			ns	
Tr	Read cycle=T_{18}+T_{25}	105			ns	
T_{27}	Chip select pulse width	75			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			35	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	

* = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

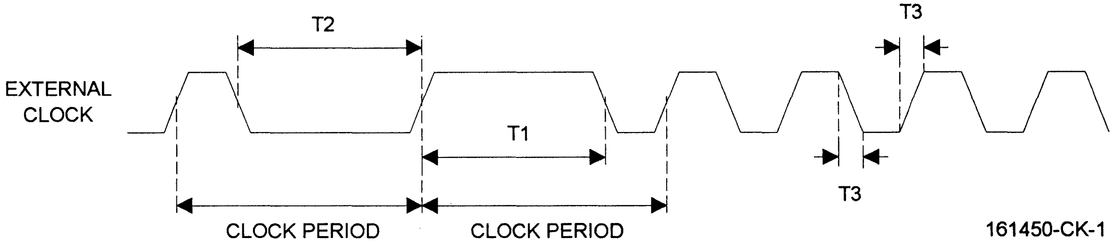
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ±10% unless otherwise specified.

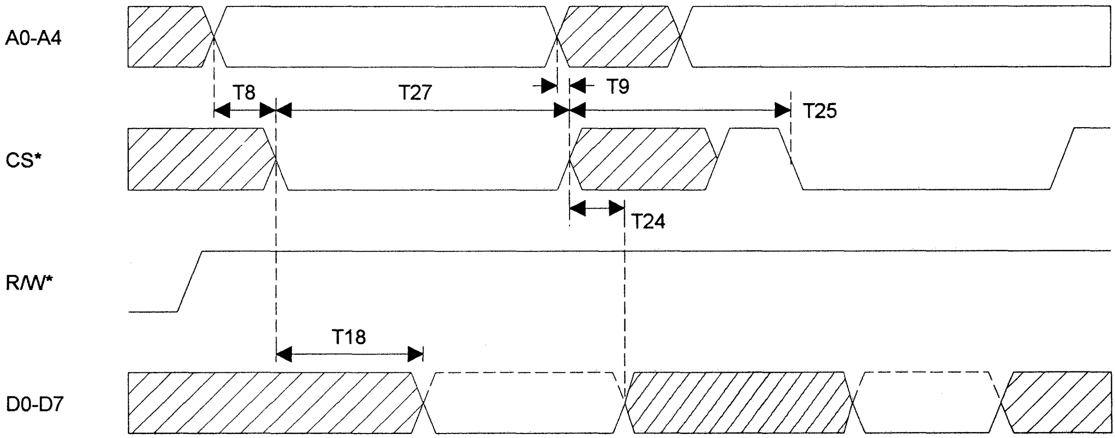
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6	12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
V_{ILCK}	Clock input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IHCK}	Clock input high level	2.4		VCC	V	Vcc=3.0 V
V_{IL}	Input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IH}	Input high level	2.0		VCC	V	Vcc=3.0 V
V_{OL}	Output low level on all outputs			0.4	V	Vcc=3.0 V, I_{OL}= 8.5 mA
V_{OH}	Output high level	2.0			V	Vcc=3.0 V, I_{OH}= -4 mA
I_{CC}	Avg power supply current		10	12	mA	Vcc=3.0 V

CLOCK TIMING



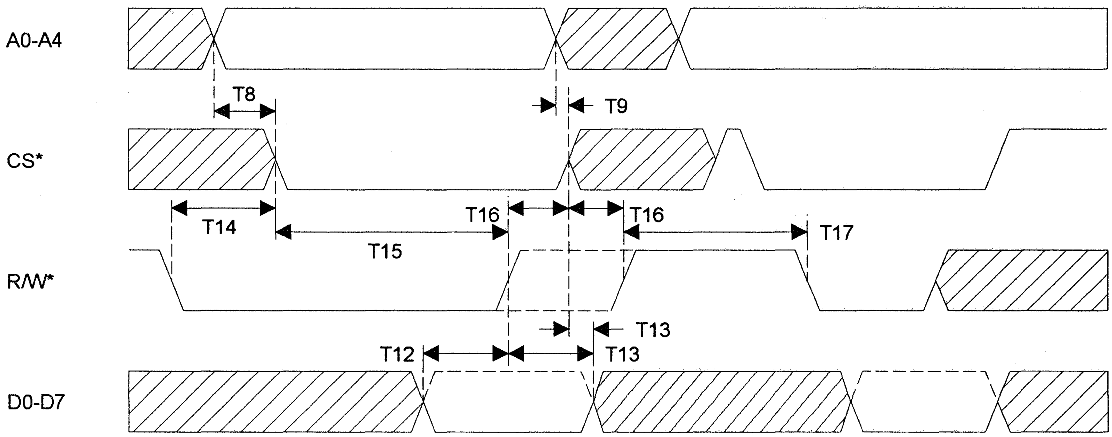
161450-CK-1

GENERAL READ TIMING



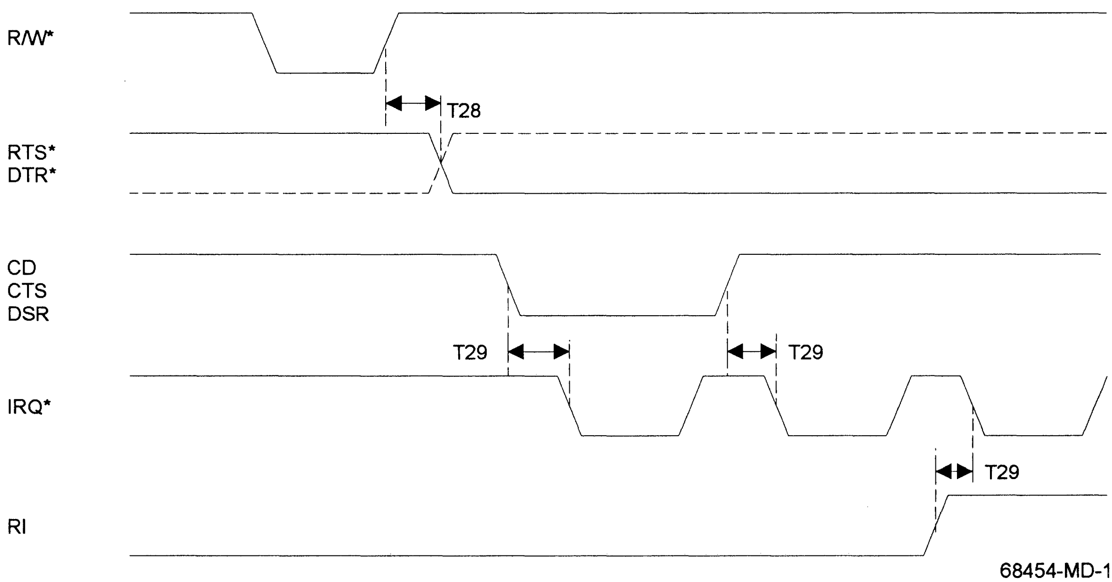
8454-RD-1

GENERAL WRITE TIMING

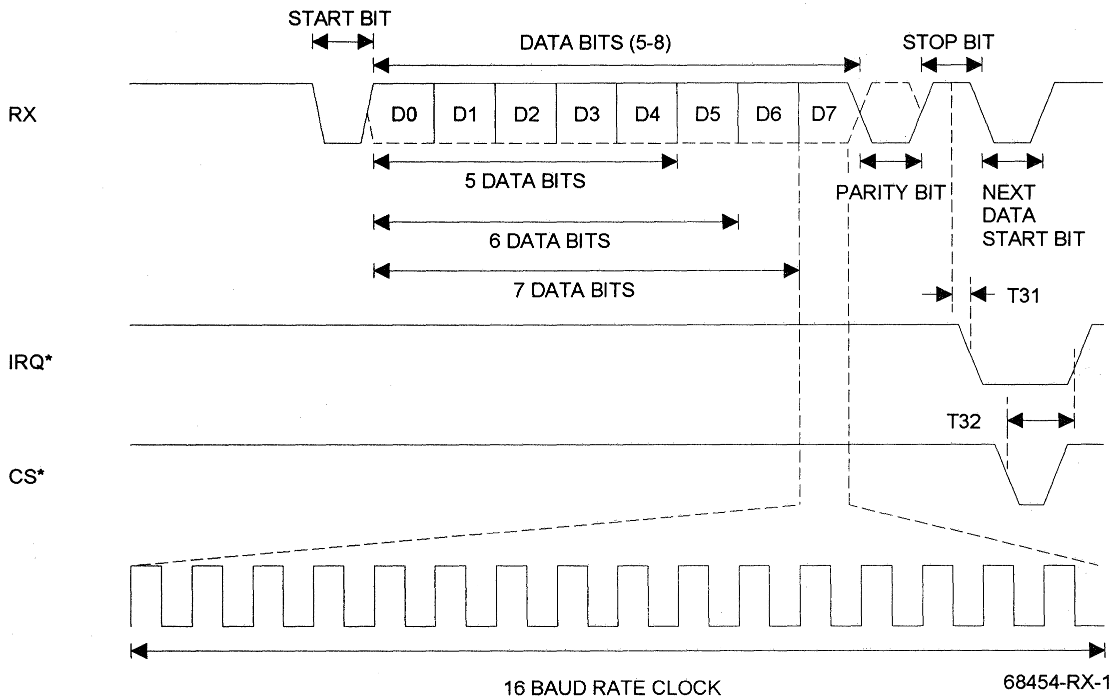


68454-WD-1

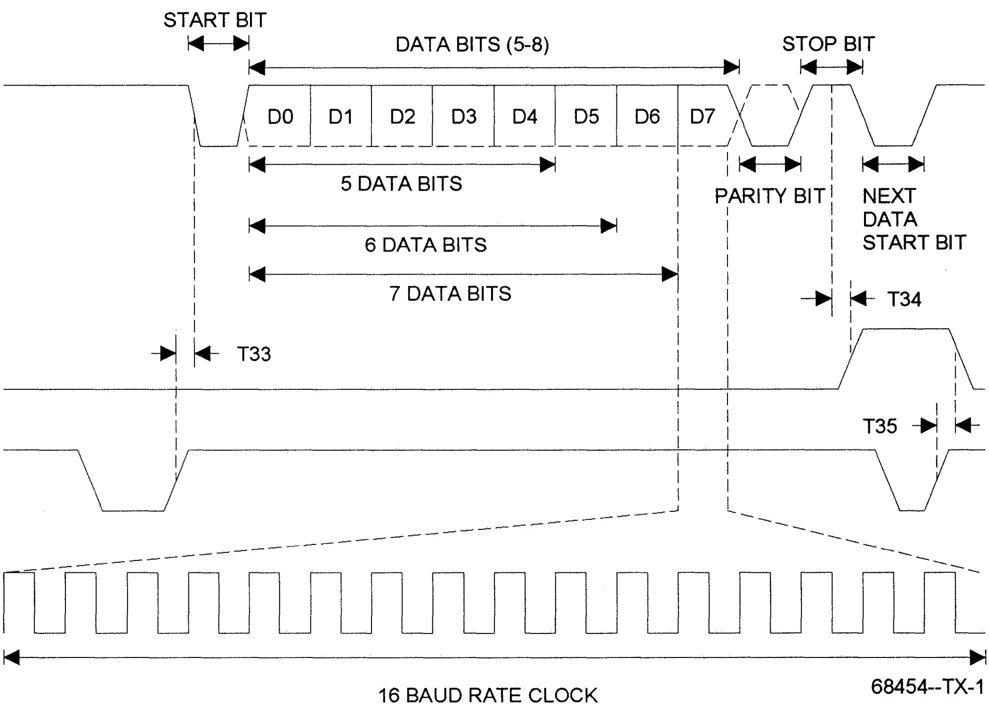
MODEM TIMING



RECEIVE TIMING



TRANSMIT TIMING



STARTECH
An EXAR Company

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UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

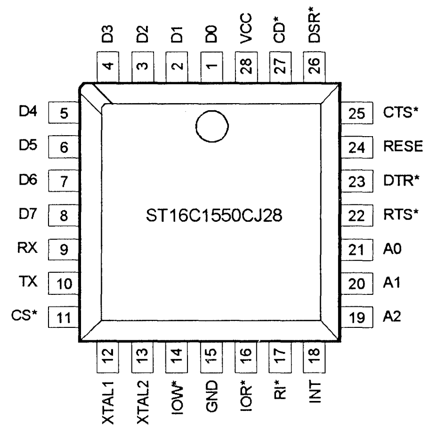
DESCRIPTION

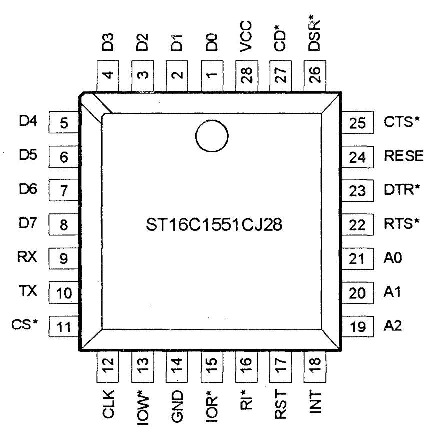
The ST16C1550/51/52 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1550/51/52 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1550/51/52 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1550/51/52 provides internal loop-back capability for on board diagnostic testing.

The ST16C1550/51/52 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package





FEATURES

- Pin to pin and functional compatible to SSI 73M1550/2550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

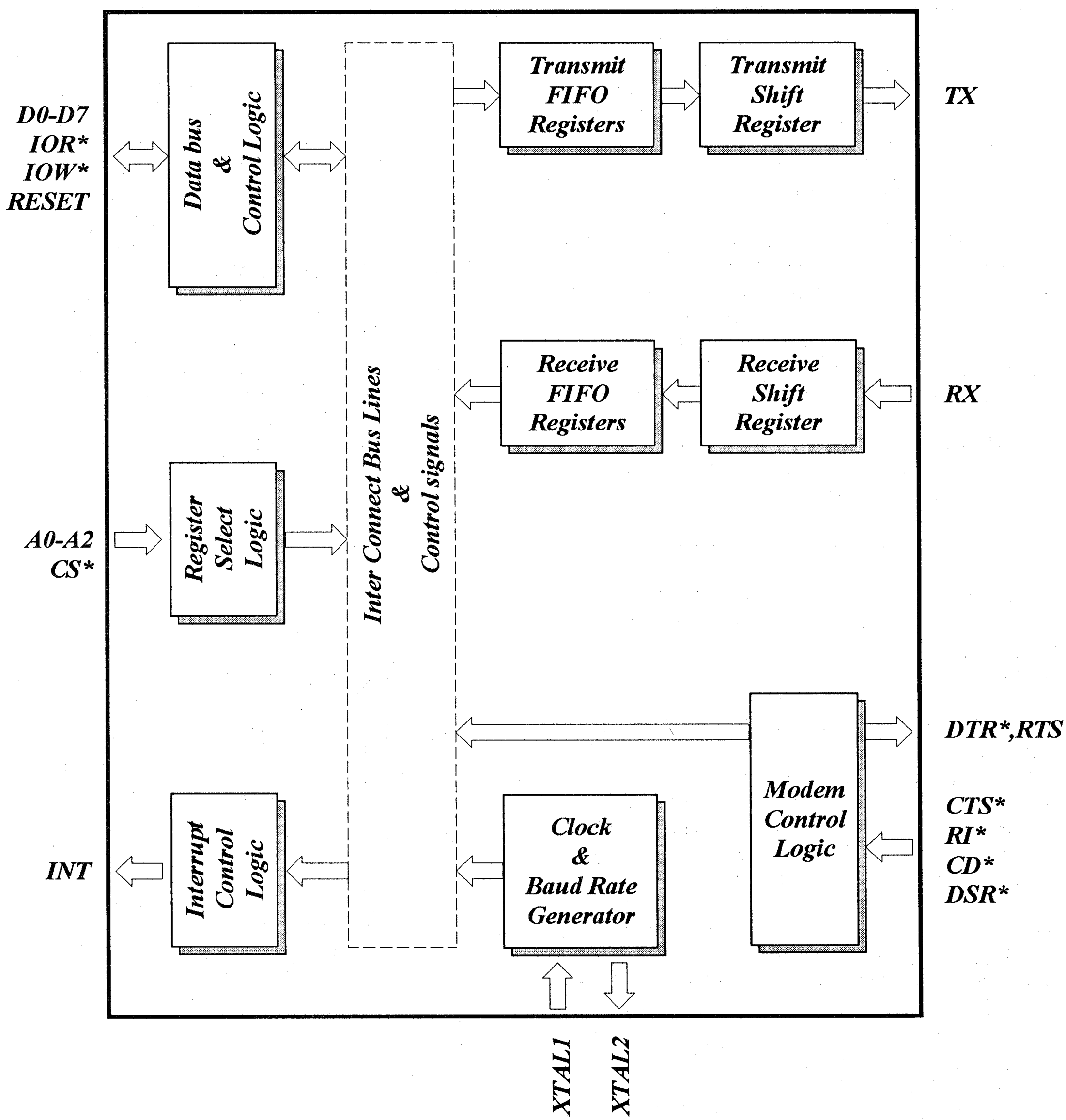
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1550CP28	Plastic-DIP	0° C to + 70° C
ST16C1550CJ28	PLCC	0° C to + 70° C
ST16C1550CQ48	TQFP	0° C to + 70° C
ST16C1551CP28	Plastic-Dip	0° C to + 70° C
ST16C1551CJ28	PLCC	0° C to + 70° C
ST16C1551CQ48	TQFP	0° C to + 70° C
ST16C1552CQ52	QFP	0° C to + 70° C

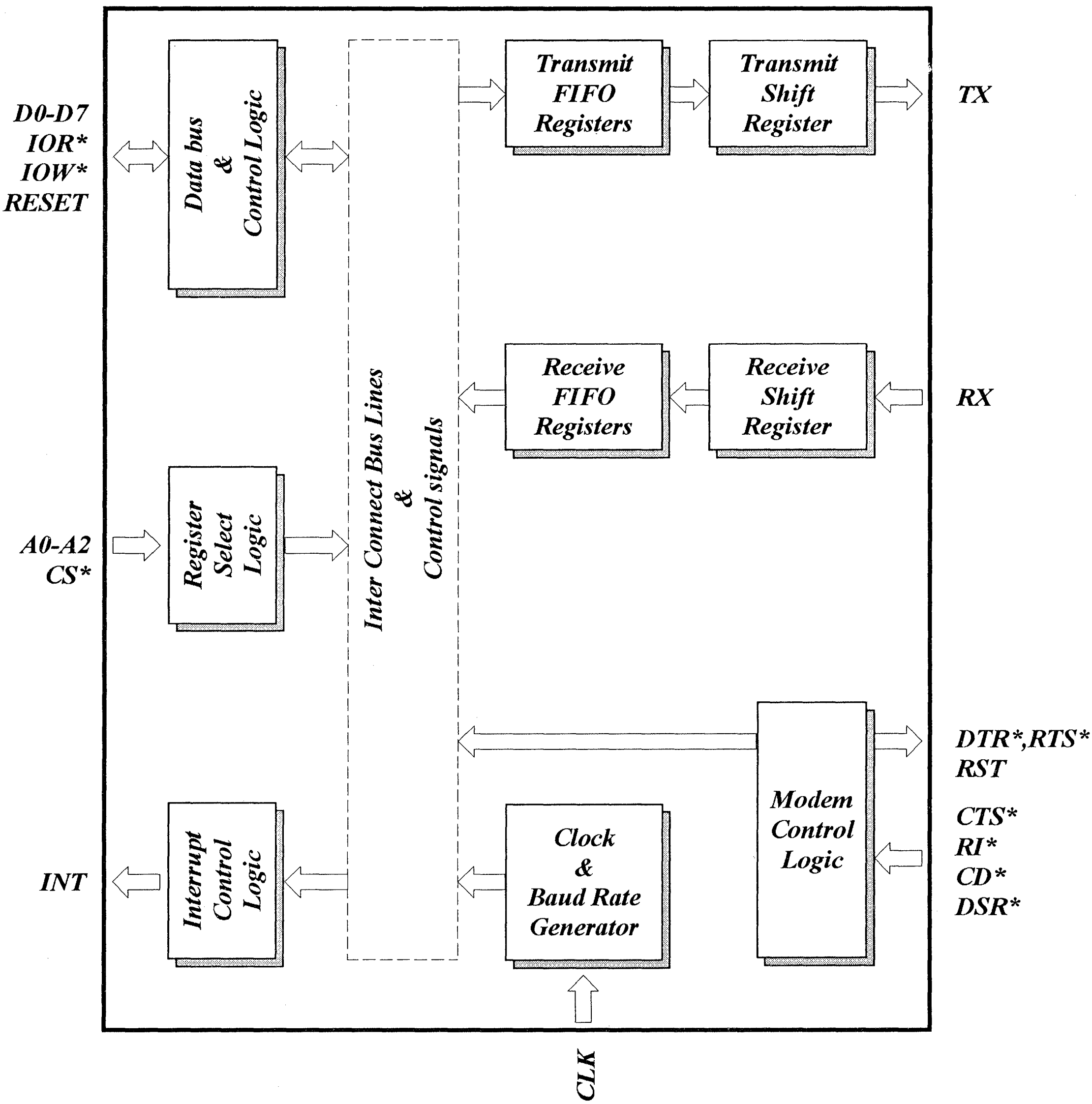
*Industrial operating range are available

Rev. 1.0

ST16C1550 BLOCK DIAGRAM



ST16C1551 BLOCK DIAGRAM



ST16C1550
ST16C1551/1552

SYMBOL DESCRIPTION (ST16C1550 - ST16C1551)

Symbol	Pin 28	Pin 28	Signal Type	Pin Description
D0-D7	1-8	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	9	I	Serial data input. The serial information (data) received from serial port to ST16C155X receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	11	I	Chip select (active low). A low at this pin enables the ST16C155X / CPU data transfer operation.
XTAL1	12	-	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
CLK	-	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	-	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	14	O	Signal and power ground.
IOR*	16	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C155X data bus to the CPU..
RI*	17	16	I	Ring detect indicator (active low). A low on this pin indicates

SYMBOL DESCRIPTION (ST16C1550 - ST16C1551)

Symbol	Pin 28	Pin 28	Signal Type	Pin Description
				the modem has received a ringing signal from telephone line.
RST	-	17	O	Reset output (active high). The ST16C1551 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	21-19	I	Address select line. To select internal registers.
RTS*	22	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	23	O	Data terminal read (active low). To indicate that ST16C155X is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin

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SYMBOL DESCRIPTION (ST16C1550 - ST16C1551)

Symbol	Pin 28	Pin 28	Signal Type	Pin Description
				does not have any effect on the transmit or receive operation.
CD*	27	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	28	I	Power supply input.

All unused input pins should be tied to VCC or GND.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0 / TX trigger (MSB)	0 / TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0 / FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C1550/51/52 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C1550/51/52 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1550/51/52 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to $2^{16}-1$. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4:
This bit is not used and set to zero.

IER BIT 5:
0=disable the ISR bits 4-5 and MCR bit-7.
1=enable the ISR bits 4-5 and MCR bit-7 function.

IER BIT 6-7:
These bits are not used and set to zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1550/51/52 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1550/51/52 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Received Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3:
This bit is used with conjunction of ISR bit 0-2:
0=normal interrupt mode
1=receive time-out indicator when priority level is set to "2" (D0=0, D1=0, and D2=1)

ISR bit-4:
This bit is the compliment of TXRDY* (ST16C550) pin when IER bit-4 is set to "1".
0=transmitter is full
1=transmitter is empty or less than full

ISR bit-5:
This bit is the compliment of RXRDY* (ST16C550) pin when IER biot-4 is set to "1".
0=receiver is empty.
1=receiver is not empty

ISR bit-6-7:
0=16C450 mode
1=16C550 mode

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
These bits are used to set the transmit trigger levels. See receive FIFO trigger table.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.

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1=force RTS* output to low.

MCR BIT-2:
0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-6:
Not used. Are set to zero permanently.

MCR bit-7:
0=normal mode.
1=power down mode. CLK, XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C1550/51/52 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C1550/51/52 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1550/51/52 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C1550
ST16C1551/1552

ST16C1550/51/52 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state

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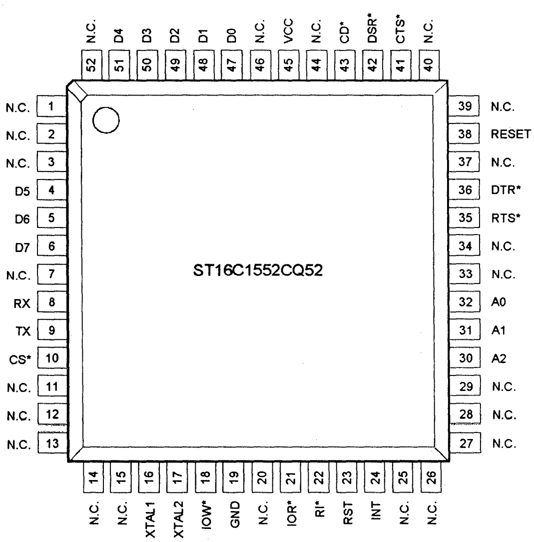
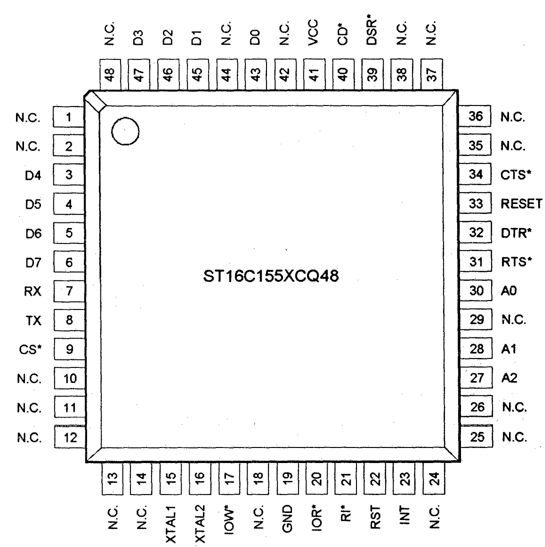


48 TQFP ST16C155X



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	

Note 1: * = Baudout* cycle

ST16C1550
ST16C1551/1552

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

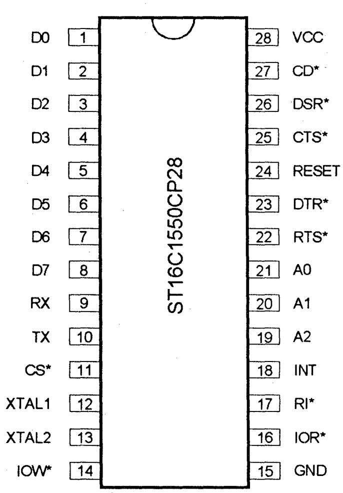
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

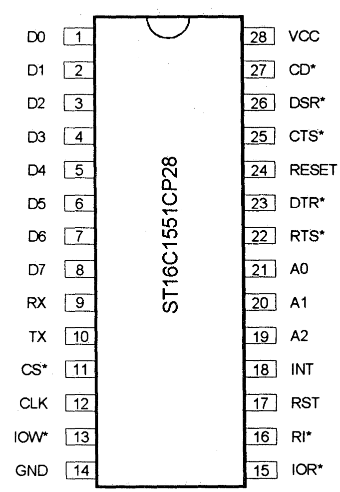
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

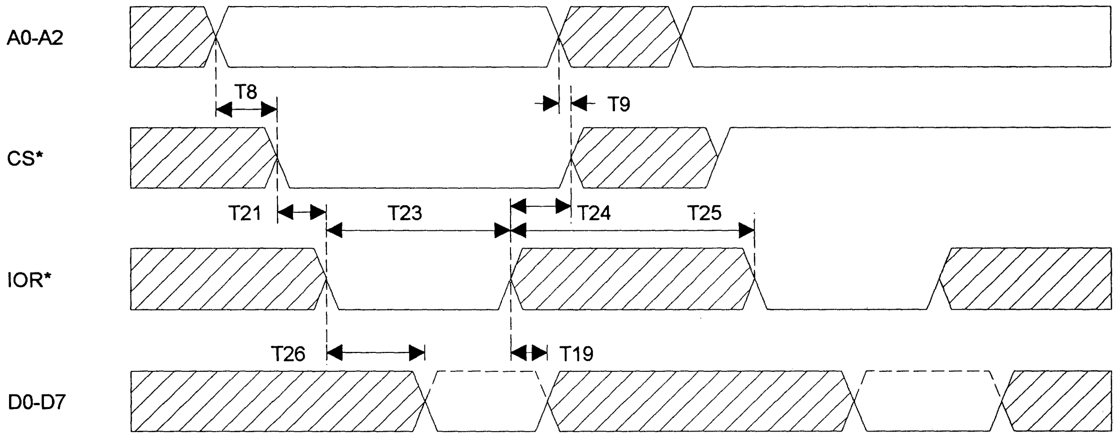
28 PIN PLASTIC-DIP ST16C1550



28 PIN PLASTIC-DIP ST16C1551

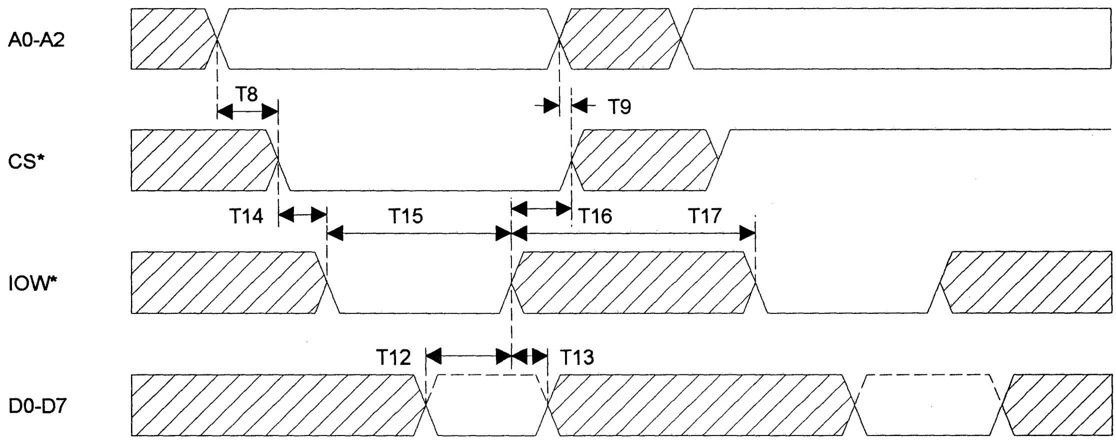


GENERAL READ TIMING



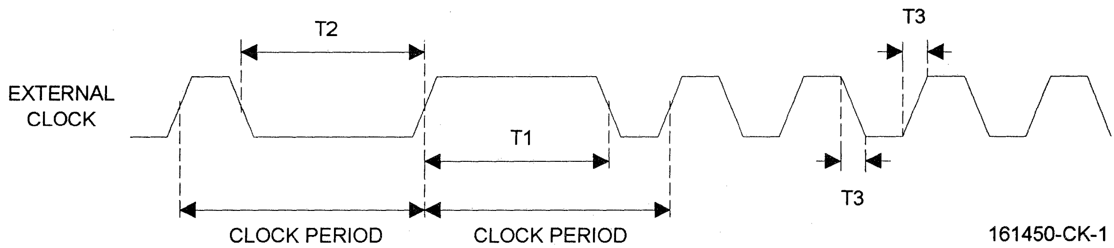
161450-RD-1

GENERAL WRITE TIMING

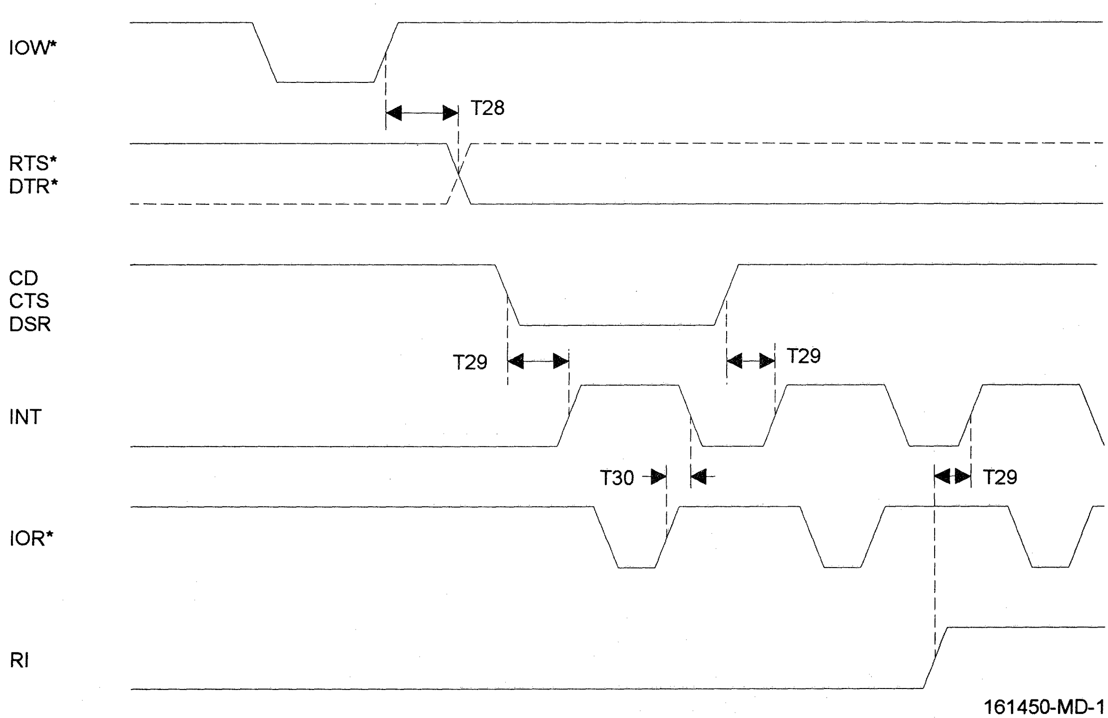


161450-WD-1

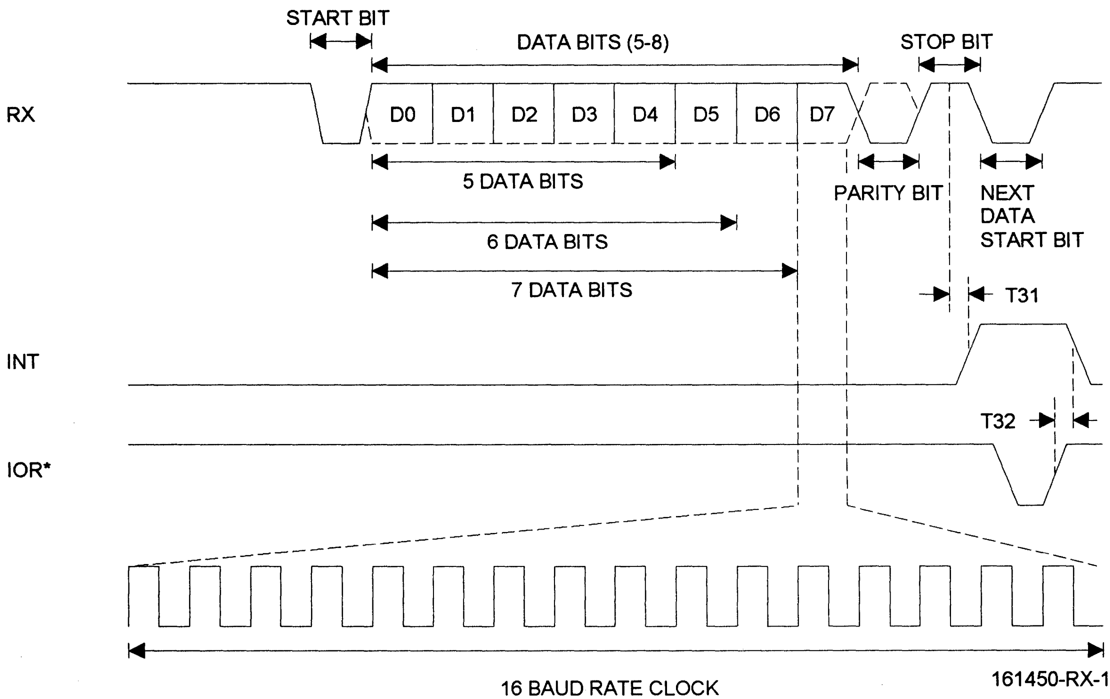
CLOCK TIMING



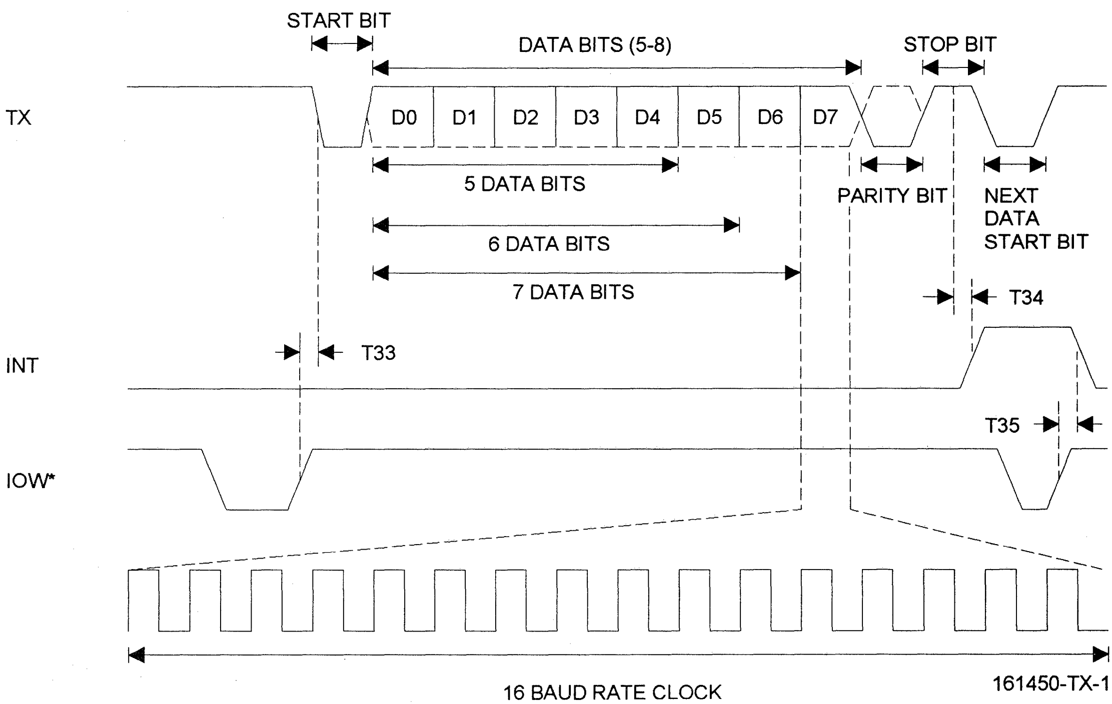
MODEM TIMING



RECEIVE TIMING



TRANSMIT TIMING



DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C2550 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 1.5 MHz for each UART.
The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C2550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2550 provides internal loop-back capability for on board diagnostic testing.
The ST16C2550 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

FEATURES

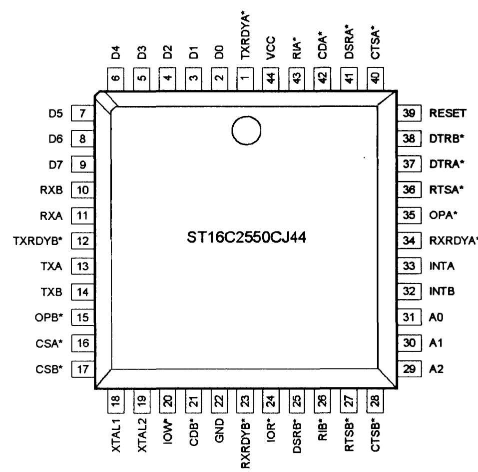
- Pin to pin and functional compatible to ST16C2450
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

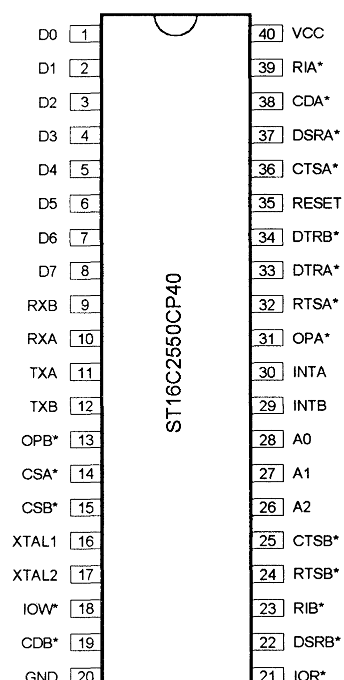
Part number	Package	Operating temperature
ST16C2550CP40	Plastic-DIP	0° C to + 70° C
ST16C2550CJ44	PLCC	0° C to + 70° C

*Industrial operating range are available

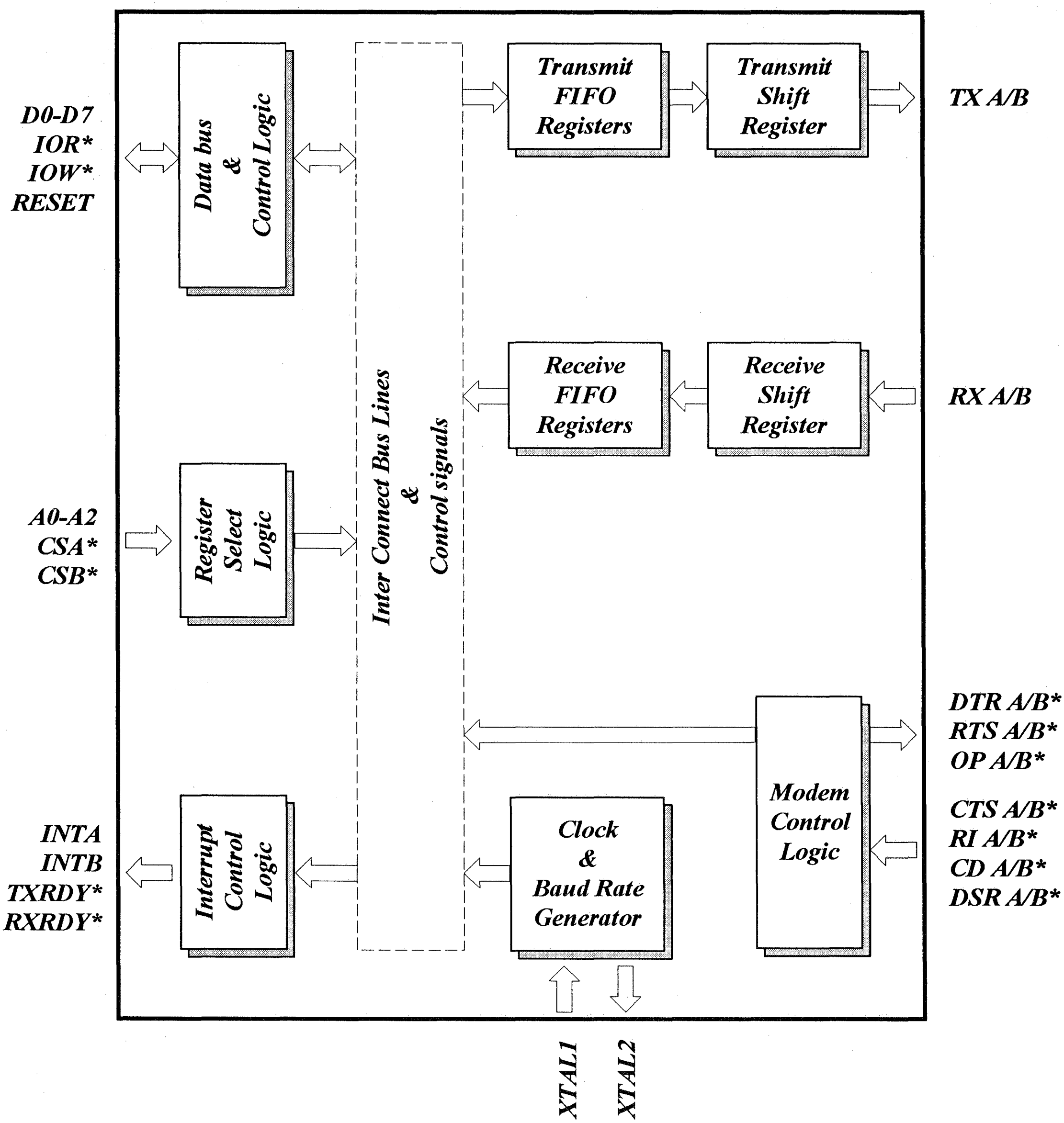
PLCC Package



Plastic-DIP Package



BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
D0-D7	1-8	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	10,9	11,10	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	13,14	O	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS* A/B	14,15	16,17	I	Chip select A/B. (active low) A low at this pin enables the ST16C2550 / CPU data transfer operation.
XTAL1	16	18	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	19	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	24	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2550 data bus to the CPU.
A0-A2	28-26	31-29	I	Address select lines. To select internal registers.
INT A/B	30,29	33,32	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
OP2* A/B	31	35,15	O	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
RTS* A/B	32,24	36,27	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* A/B	33,34	37,38	O	Data terminal ready A/B (active low). To indicate that ST16C2550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	35	39	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS* A/B	36,25	40,28	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR* A/B	37,22	41,25	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD* A/B	38,19	42,21	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI* A/B	39,23	43,26	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
VCC	40	44	I	Power supply input.
GND	20	22	O	Signal and power ground.
TXRDY* A/B	-	1,12	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.
RXRDY* A/B	-	34,23	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C2550 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2/ INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C2550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Received Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C2550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C2550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C2550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C2550 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C2550 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except in local loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode and OP2* output to high.
1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and OP2*/INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C2550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2*/INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2550 provides a temporary data register to store 8 bits of information for variable use.

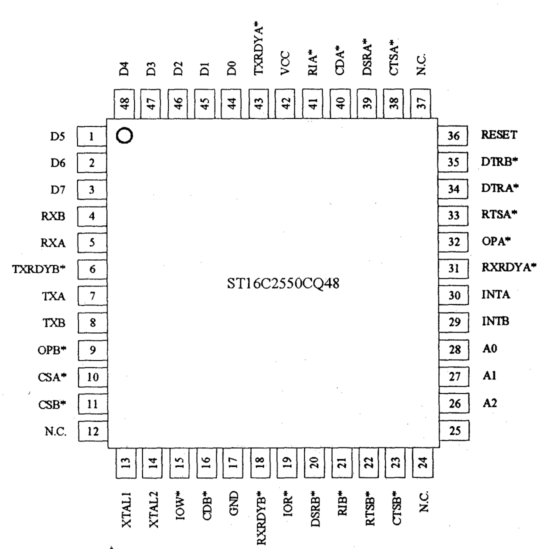
BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state mode



AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

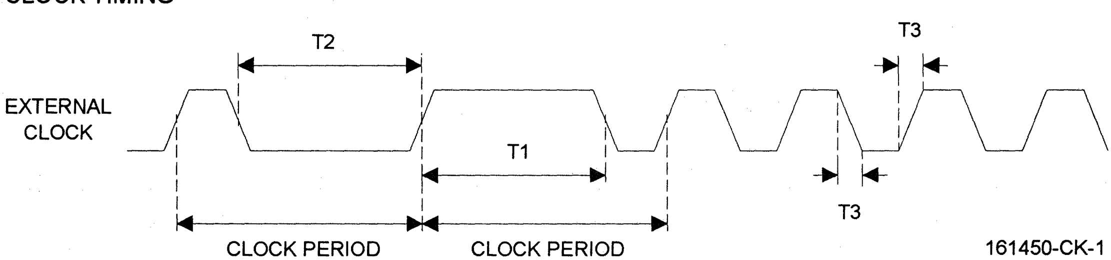
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

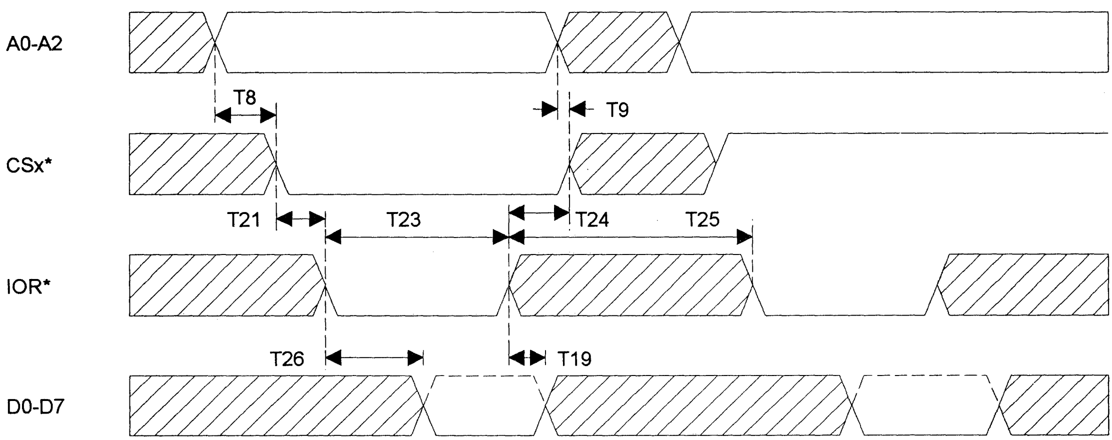
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

CLOCK TIMING

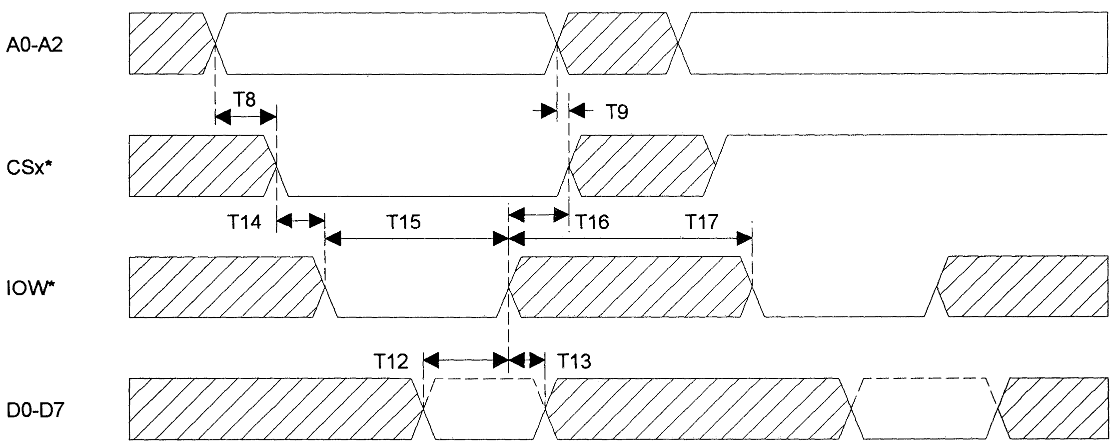


GENERAL READ TIMING



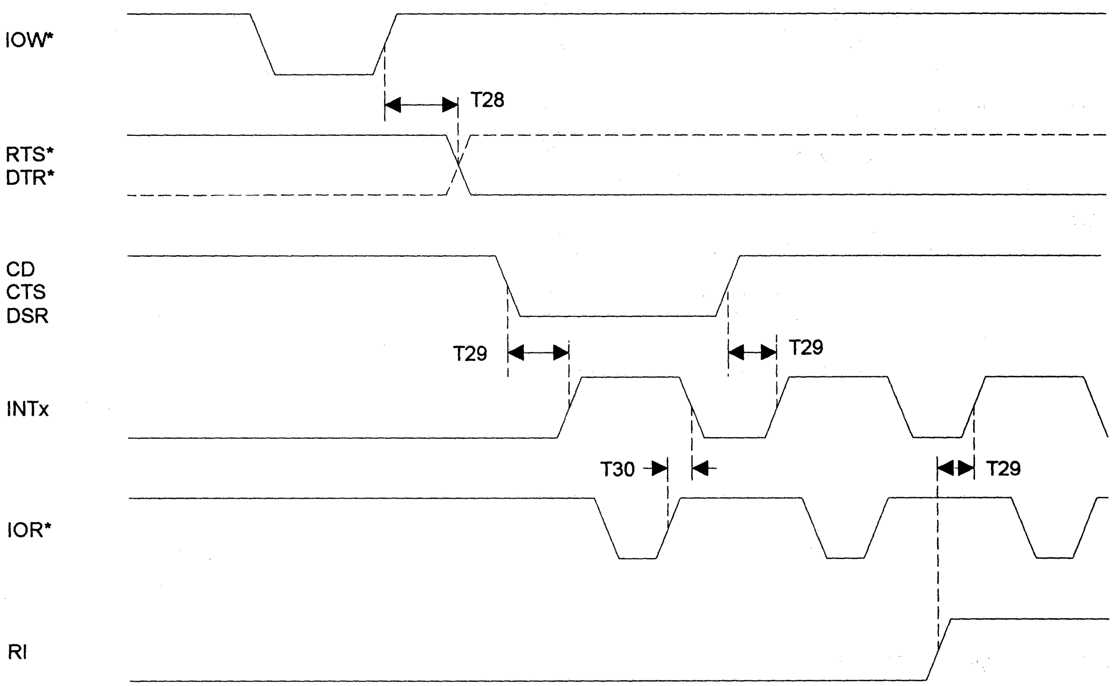
162450-RD-1

GENERAL WRITE TIMING



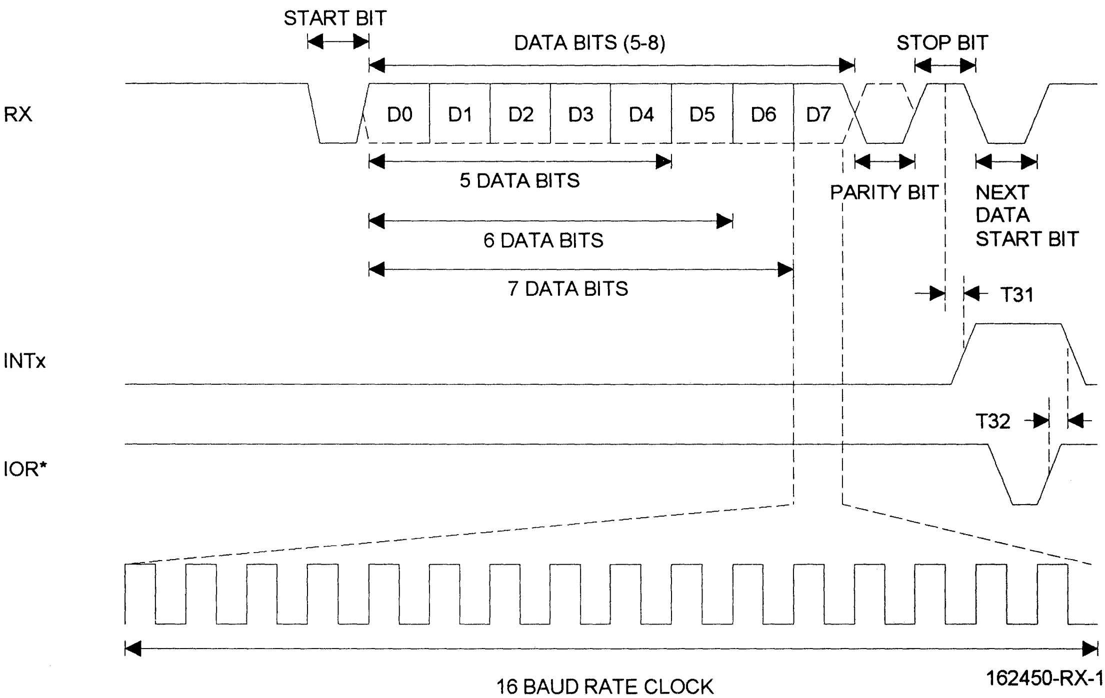
162450-WD-1

MODEM TIMING

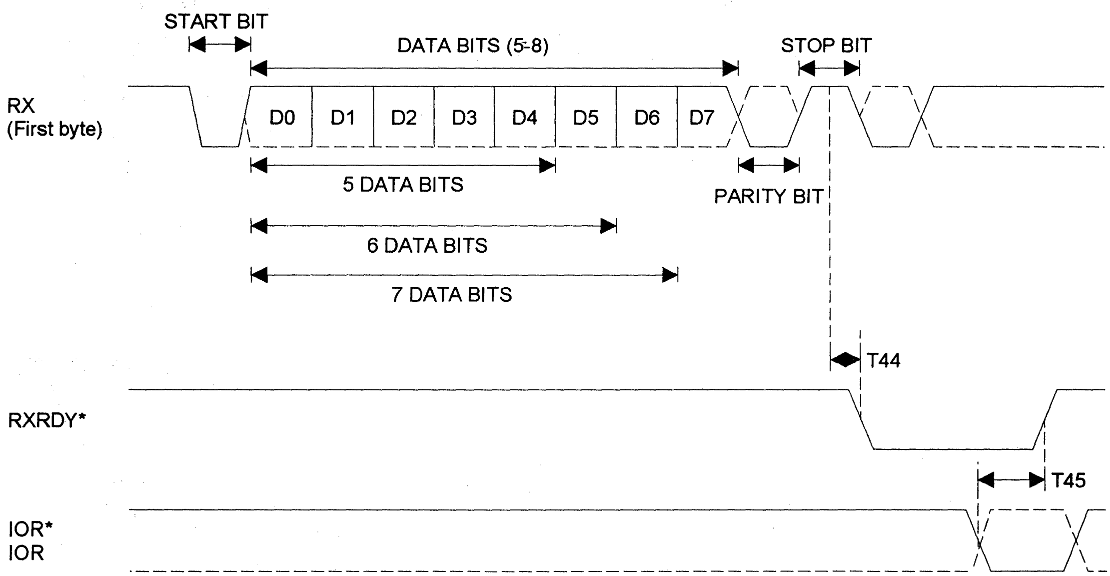


162450-MD-1

RECEIVE TIMING

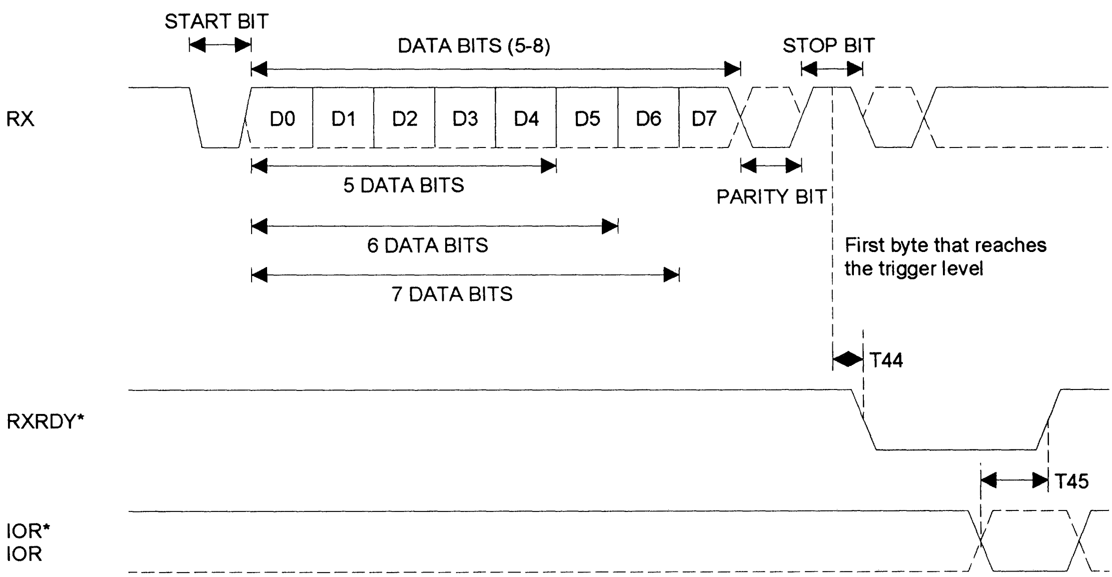


RXRDY TIMING FOR MODE "0"



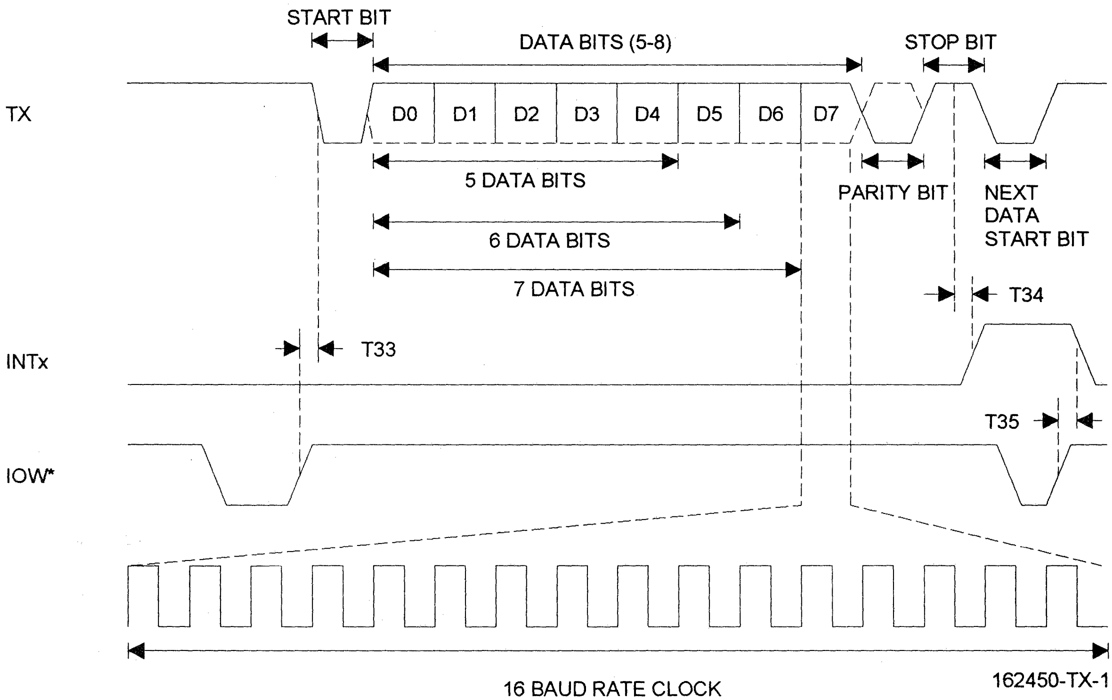
16550-RX-2

RXRDY TIMING FOR MODE "1"

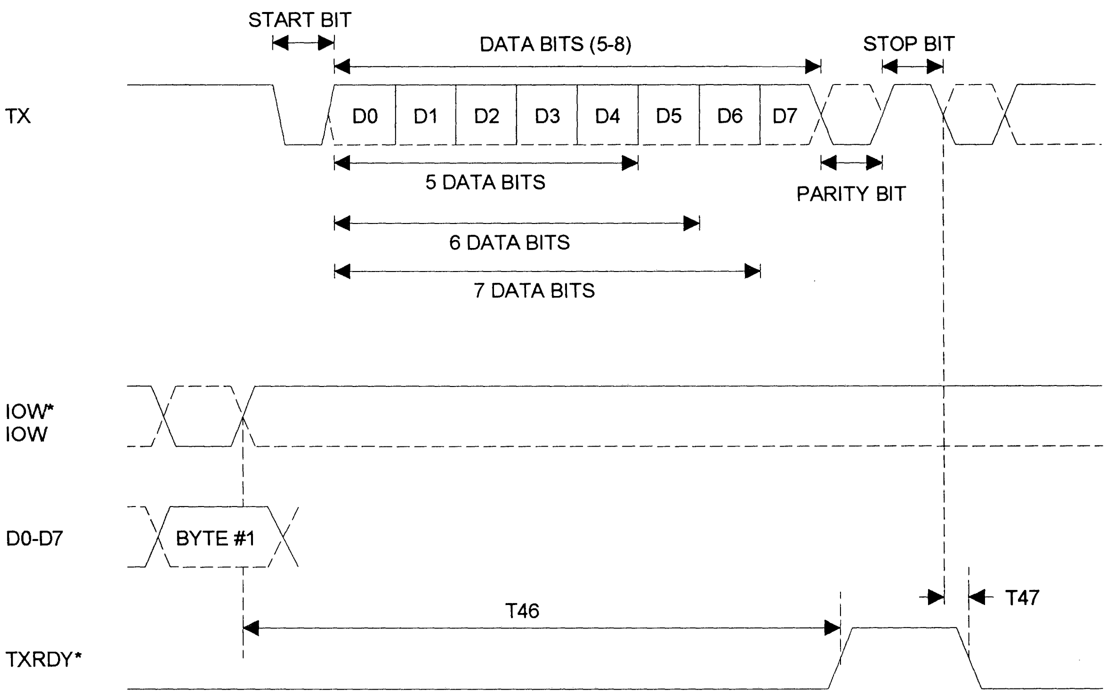


16550-RX-3

TRANSMIT TIMING

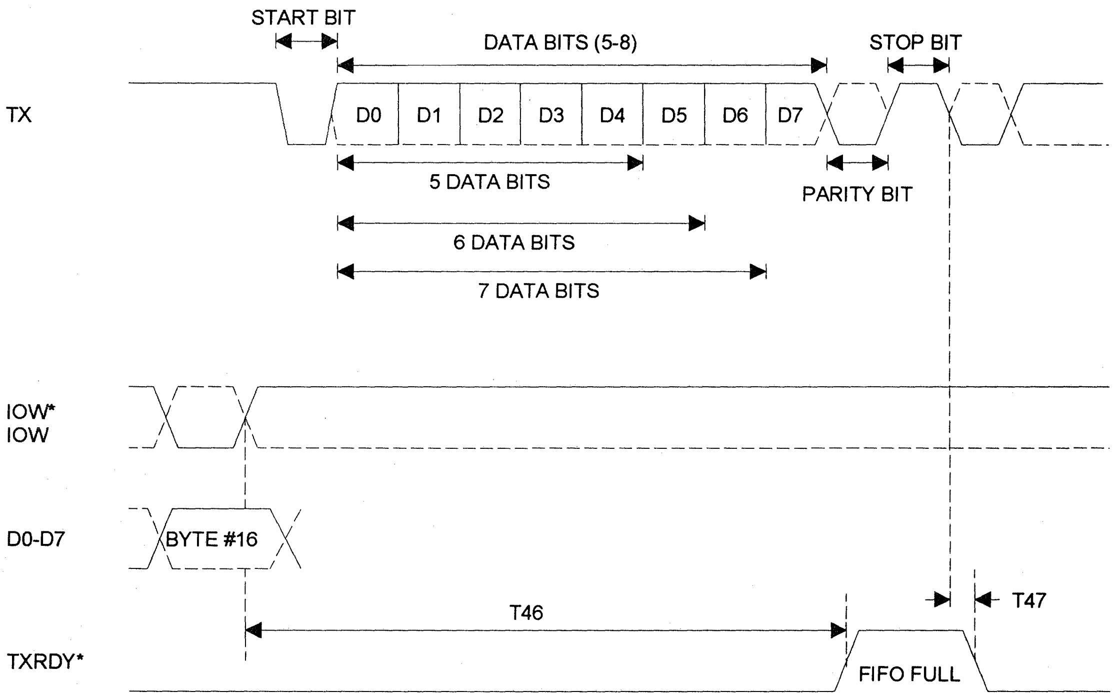


TXRDY TIMING FOR MODE "0"



16550-TX-2

TXRDY TIMING FOR MODE "1"



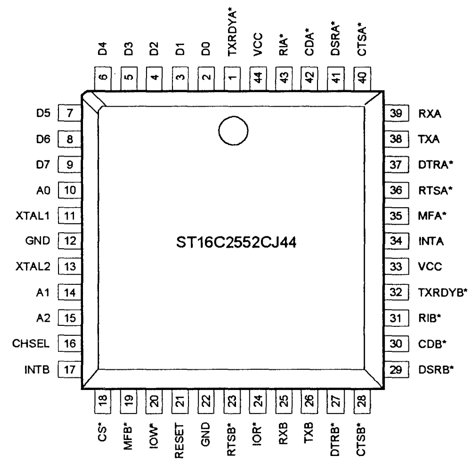
16550-TX-3

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C2552 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFOs. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 1.5 MHz for each UART.
The on board status registers of the ST16C2552 provide the error conditions, type and status of the transfer operation being performed. Complete MODEM control capability and a processor interrupt system that may be software tailored to the user's requirements are included. The ST16C2552 provides internal loop-back capability for on board diagnostic testing.
Signalling for DMA transfers is done through two pins per channel (TXRDY*, RXRDY*). The RXRDY* function is multiplexed on one pin with the OP2* and BAUDOUT functions. CPU can select these functions through the Alternate Function Register.
The ST16C2552 is fabricated in an advanced 1.2μ CMOS process to achieve low power and high speed requirements.

PLCC Package



3

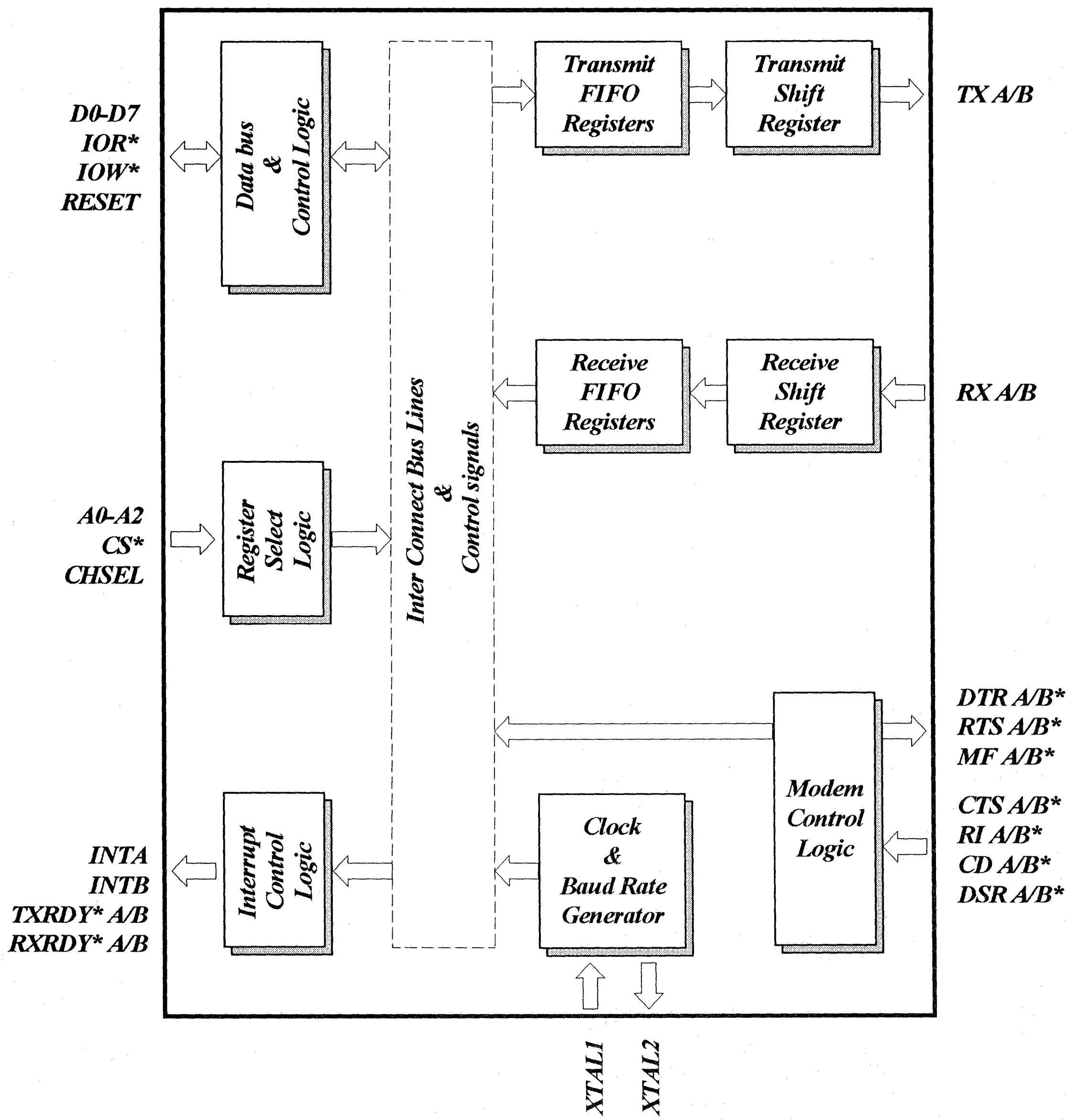
FEATURES

- Pin to pin and functional compatible to National NS16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8) bits
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Independent transmit and receive control
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2552CJ44	PLCC	0° C to + 70° C
ST16C2552IJ44	PLCC	-40° C to + 85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	39,25	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	38,26	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	18	I	Chip select. (active low) A low at this pin enables the ST16C2552 / CPU data transfer operation.
CHSEL	16	I	UART A/B select. UART A or B can be selected by changing the state of this pin when CS* is active. Low on this pin, selects the UART B and high on this pin selects UART A section.
XTAL1	11	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	O	Crystal input 2 or buffered clock output. See XTAL1. Should be left open if a clcok is connected to XTAL1.
IOW*	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	24	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2552 data bus to the CPU.
A0-A2	10,14,15	I	Address select lines. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INT A/B	34,17	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
MF* A/B	35,19	O	OP2* (interrupt enable), BAUDOUT* and RXRDY* outputs. These outputs are multiplexed via Alternate Function Register. When output enable function is selected the MF* pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled. See bit-3 modem control register (MCR bit-3). When BAUDOUT function is selected, the 16 X TX/RX Baud rate clock output is generated. RXRDY function can be selected to use to request a DMA transfer of data from the Receive data FIFO. OP2* is the default signal and it is selected immediately after master reset or power-up.
TXRDY* A/B	1,32	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the ST16C2552 is full. It can be used as a single or multi-transfer.
RTS* A/B	36,23	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* A/B	37,27	O	Data terminal ready A/B (active low). To indicate that ST16C2552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	21	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CTS* A/B	40,28	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR* A/B	41,29	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD* A/B	42,30	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI* A/B	43,31	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	33,44	I	Power supply input.
GND	12,22	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch
0	1	0	Alternate Function Register	Alternate Function Register

ST16C2552 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***
0 1 0	***AFR***	***0***	***0***	***0***	***0***	***0***	***MF* sel-1***	***MF* sel-0***	***SP write***

These registers are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

Each UART section of the ST16C2552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero if the FIFOs are not enabled. **BIT 6-7:** are set to "1" when the FIFOs are enabled.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

ALTERNATE FUNCTION REGISTER (AFR)

This is a read/write register used to select specific modes of MF* operation and to allow both UART registers sets to be written concurrently.

AFR BIT-0:
When this bit is set, CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by CPU when both channels are initialized to the same state. CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operation. Setting or clearing this bit has no effect on read operations.
The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0,1, or 2.

AFR BIT 1-2:
Combinations of these bits selects one of the MF* functions.

BIT-2	BIT-1	MF* Function
0	0	OP2*
0	1	BAUDOUT*
1	0	RXRDY*
1	1	Reserved

AFR BIT 3-7:
Not used. All these bits are set to logic zero.

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select Divisor Latch Register and Alternate Function Register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except in local loop-back mode.

MCR BIT-3:
0=force OP2* output to high.
1=force OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C2552 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
MFR	AFR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Low
TXRDY*	Low

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

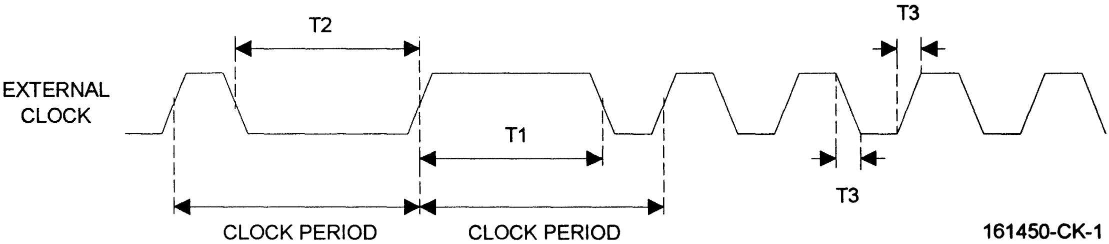
AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2_{16}-1		

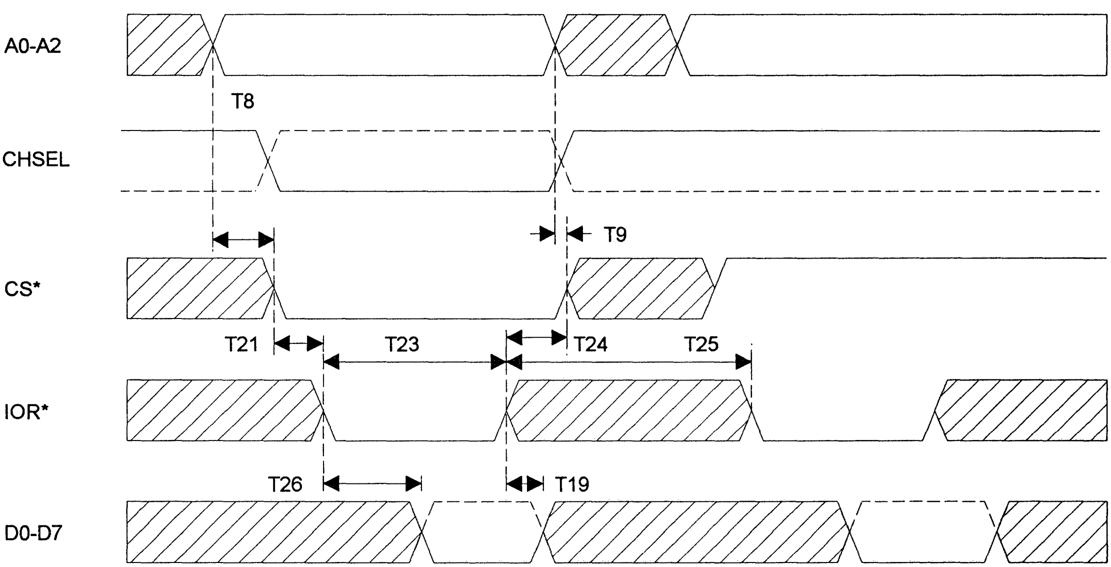
Note 1: * = Baudout* cycle

CLOCK TIMING



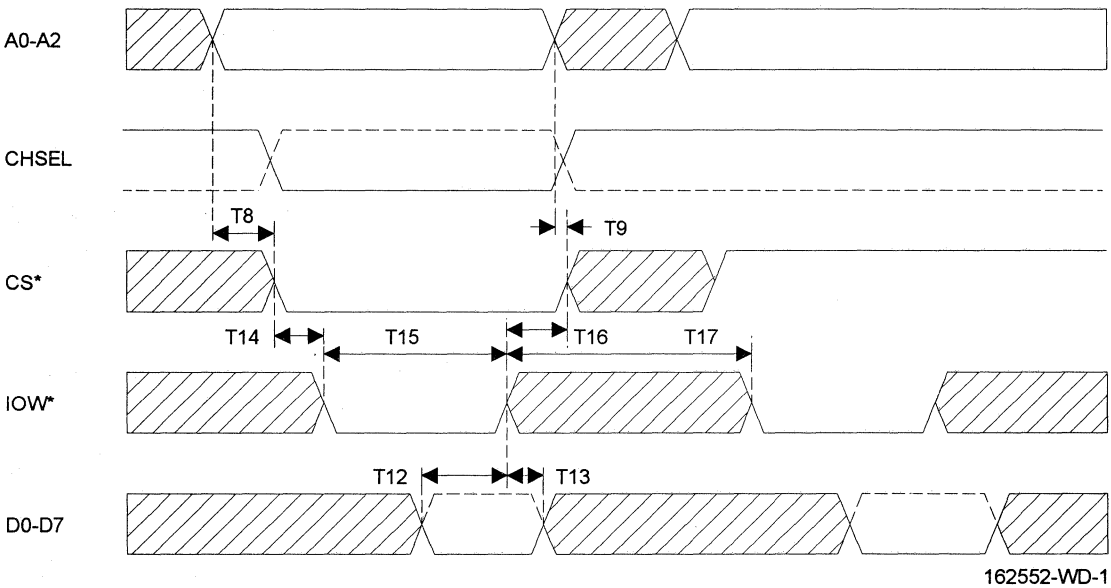
161450-CK-1

GENERAL READ TIMING

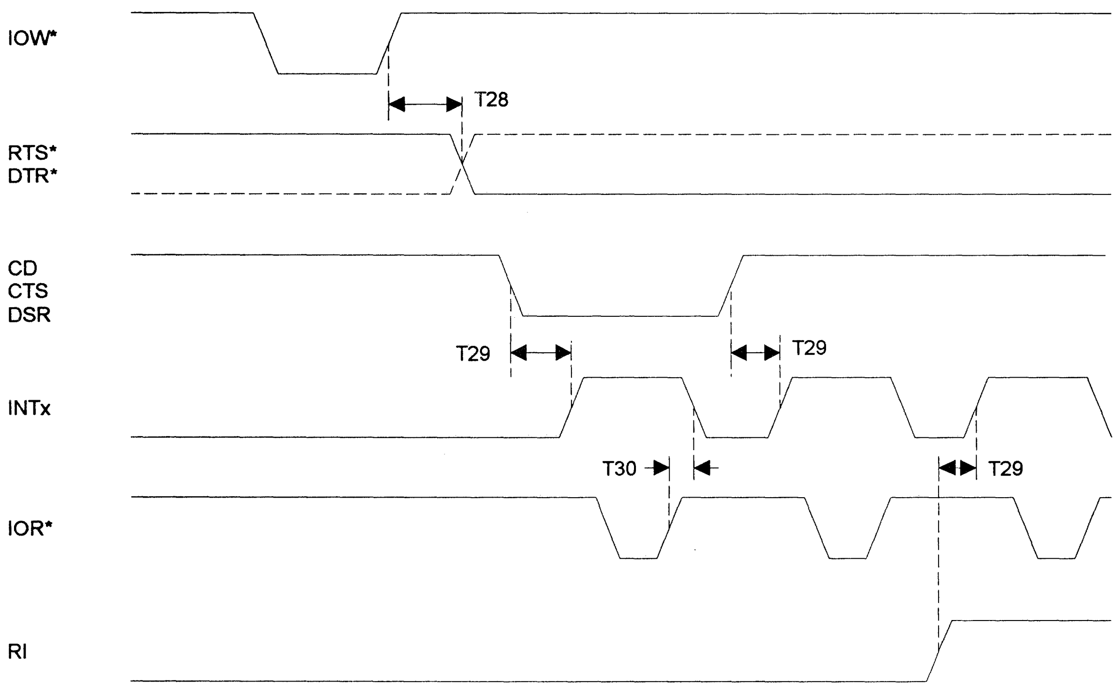


162552-RD-1

GENERAL WRITE TIMING

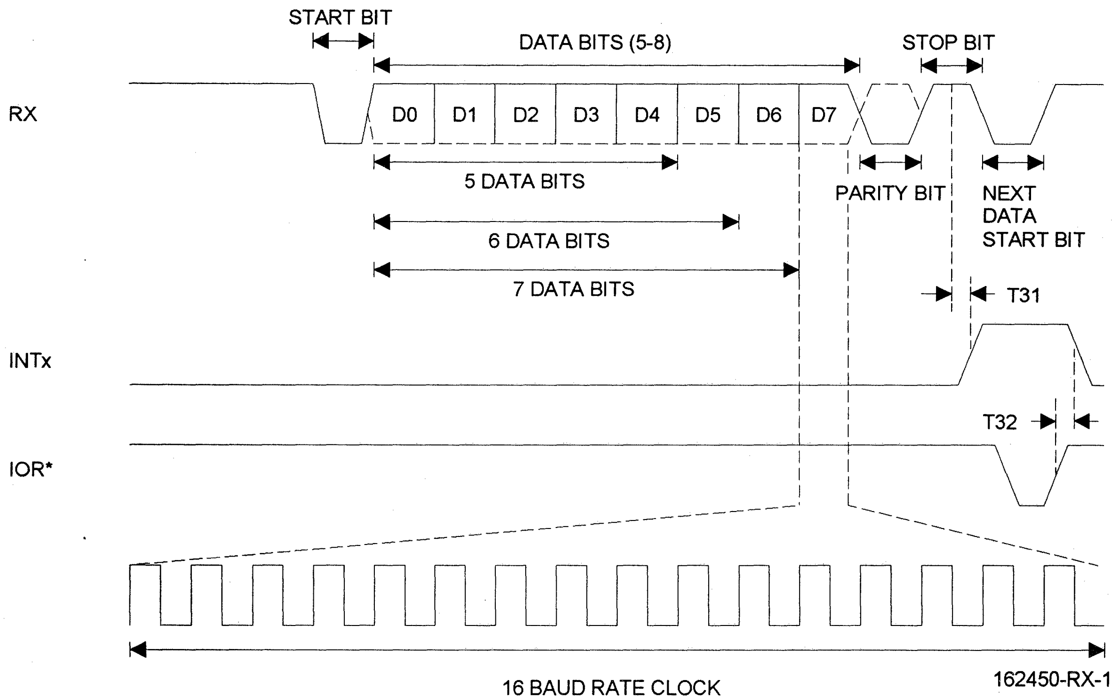


MODEM TIMING

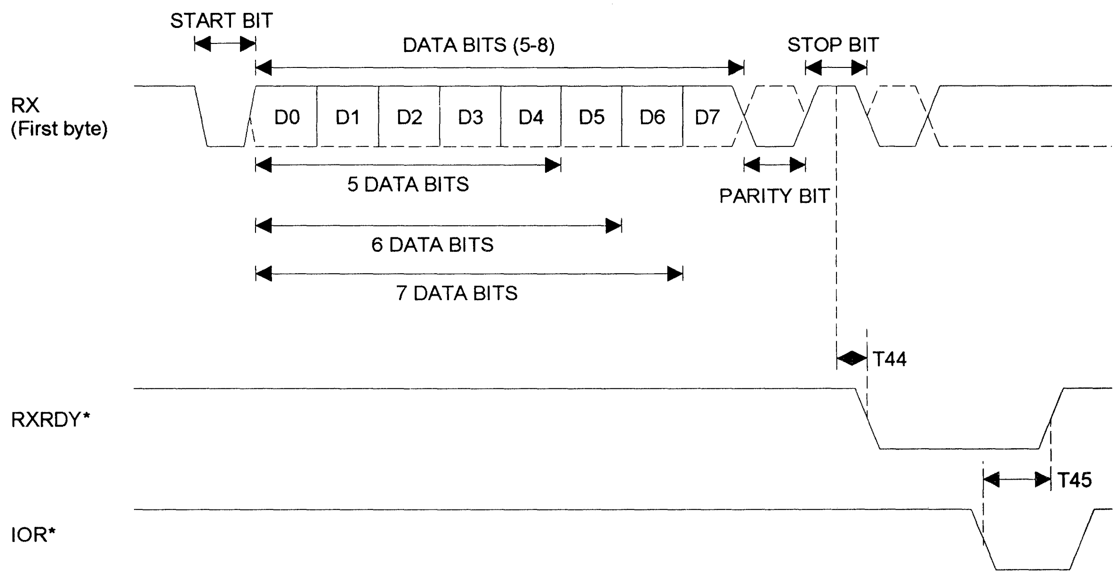


162450-MD-1

RECEIVE TIMING

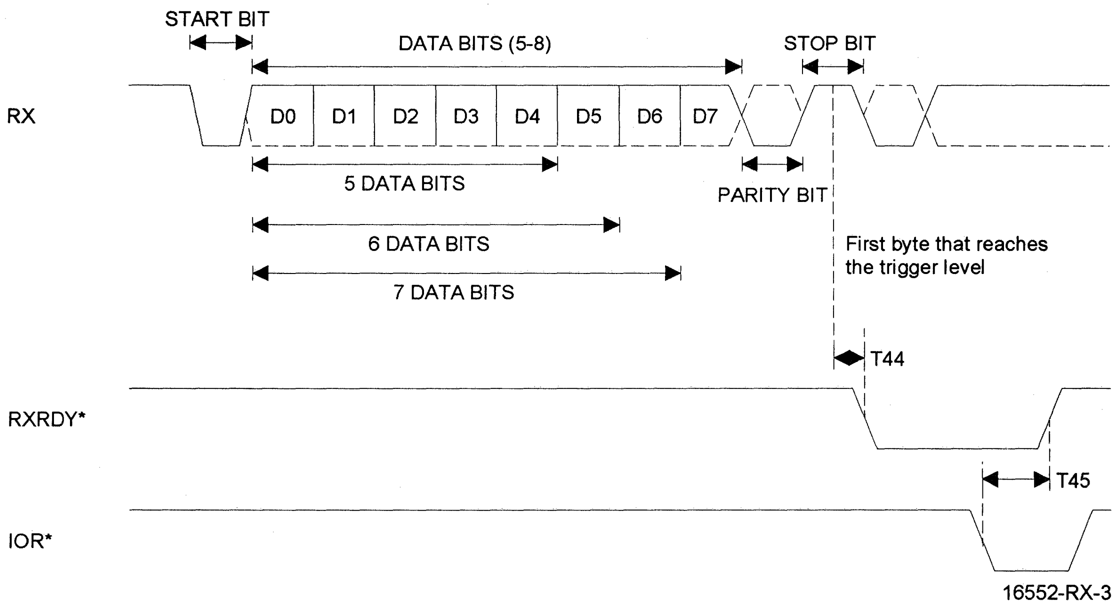


RXRDY TIMING FOR MODE "0"

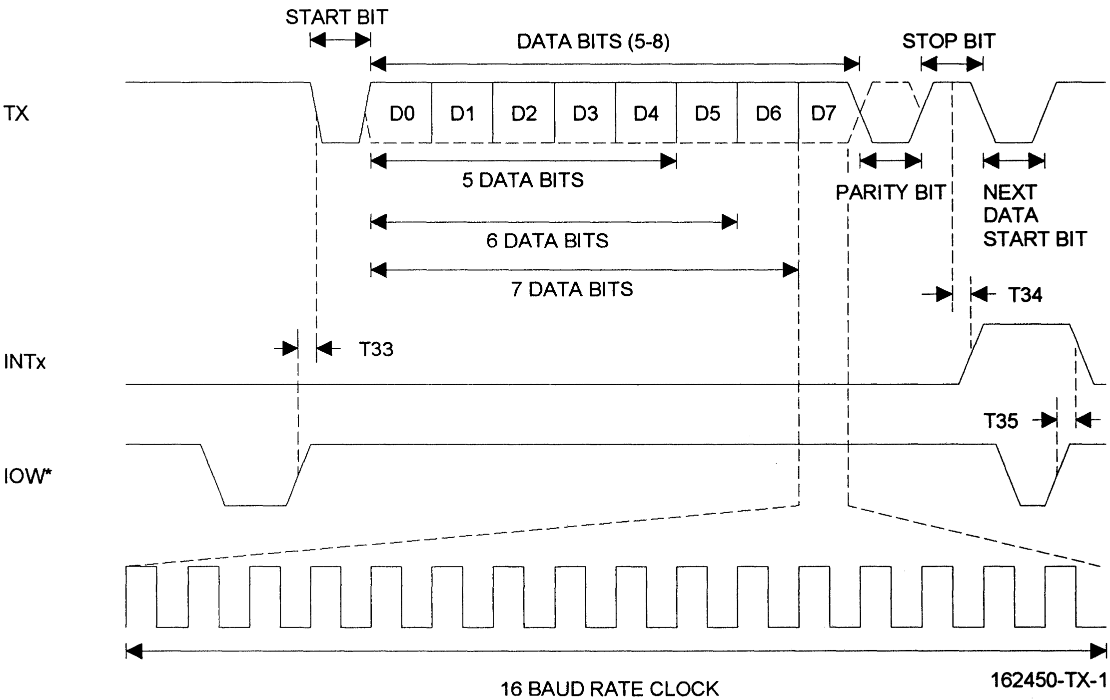


16552-RX-2

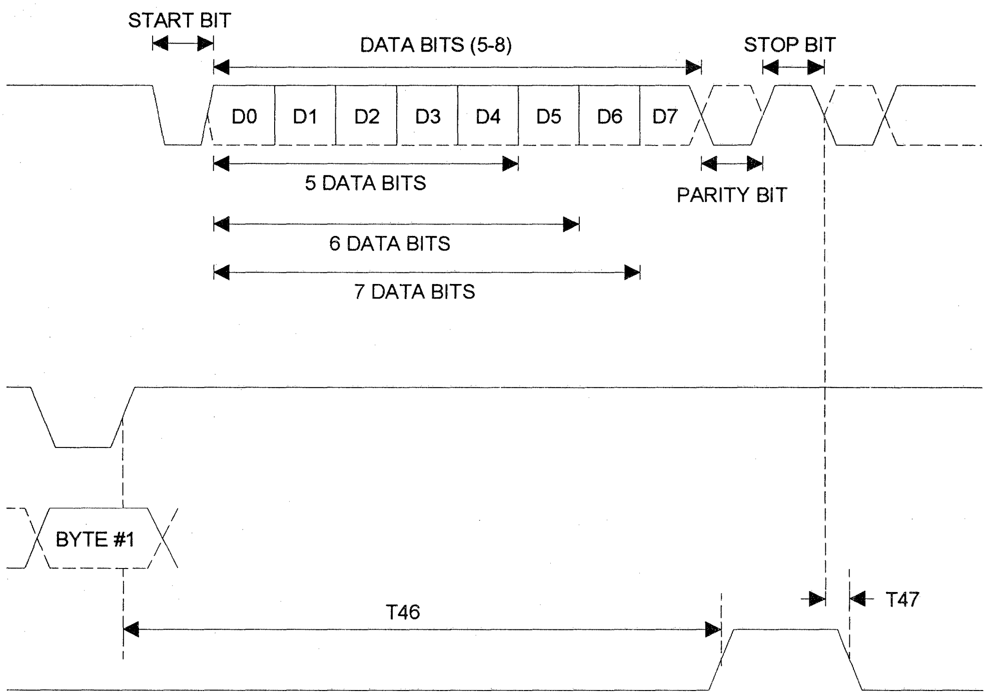
RXRDY TIMING FOR MODE "1"



TRANSMIT TIMING

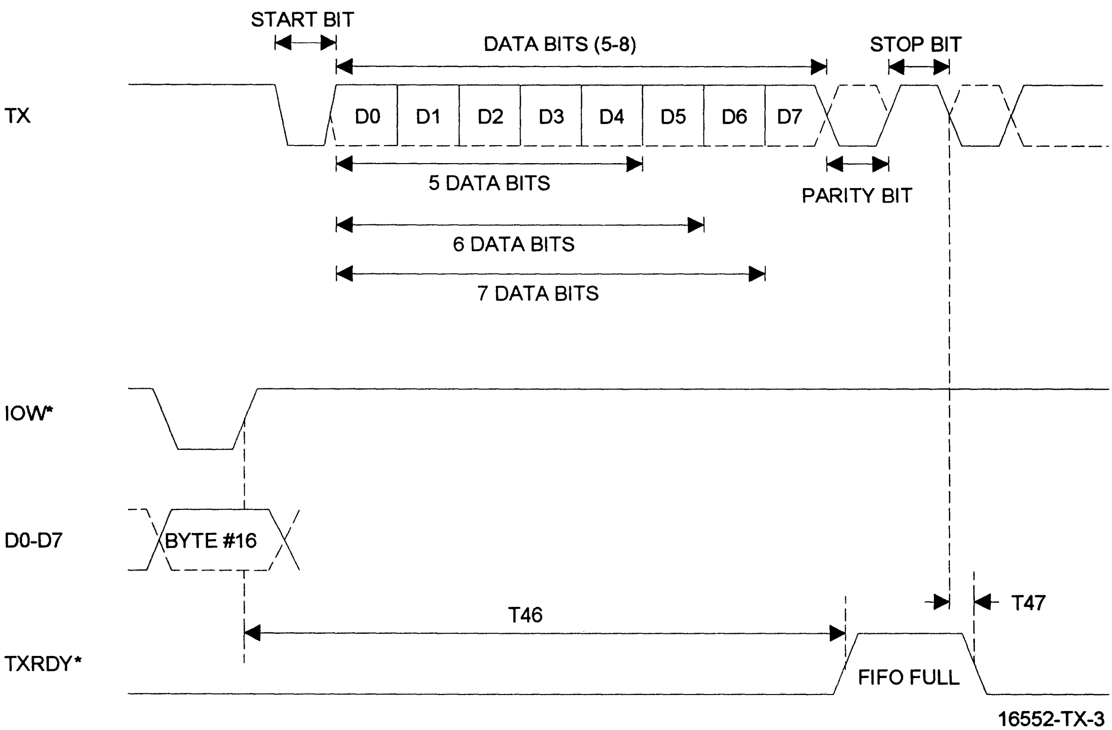


TXRDY TIMING FOR MODE "0"



16552-TX-2

TXRDY TIMING FOR MODE "1"



STARTECH

An EXAR Company

ST16C550

Printed August 3, 1995

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

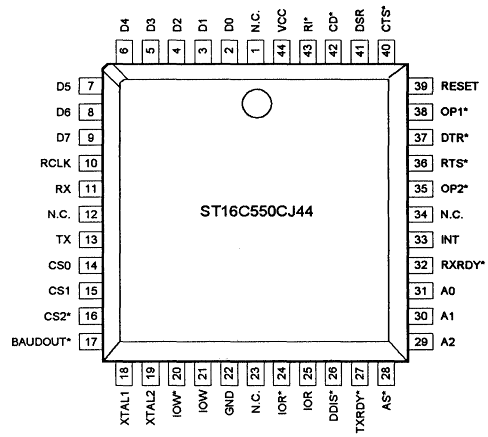
DESCRIPTION

The ST16C550 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

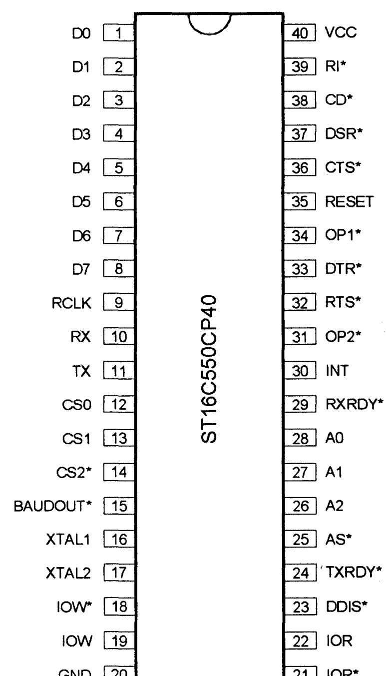
The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loop-back capability for on board diagnostic testing.

The ST16C550 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

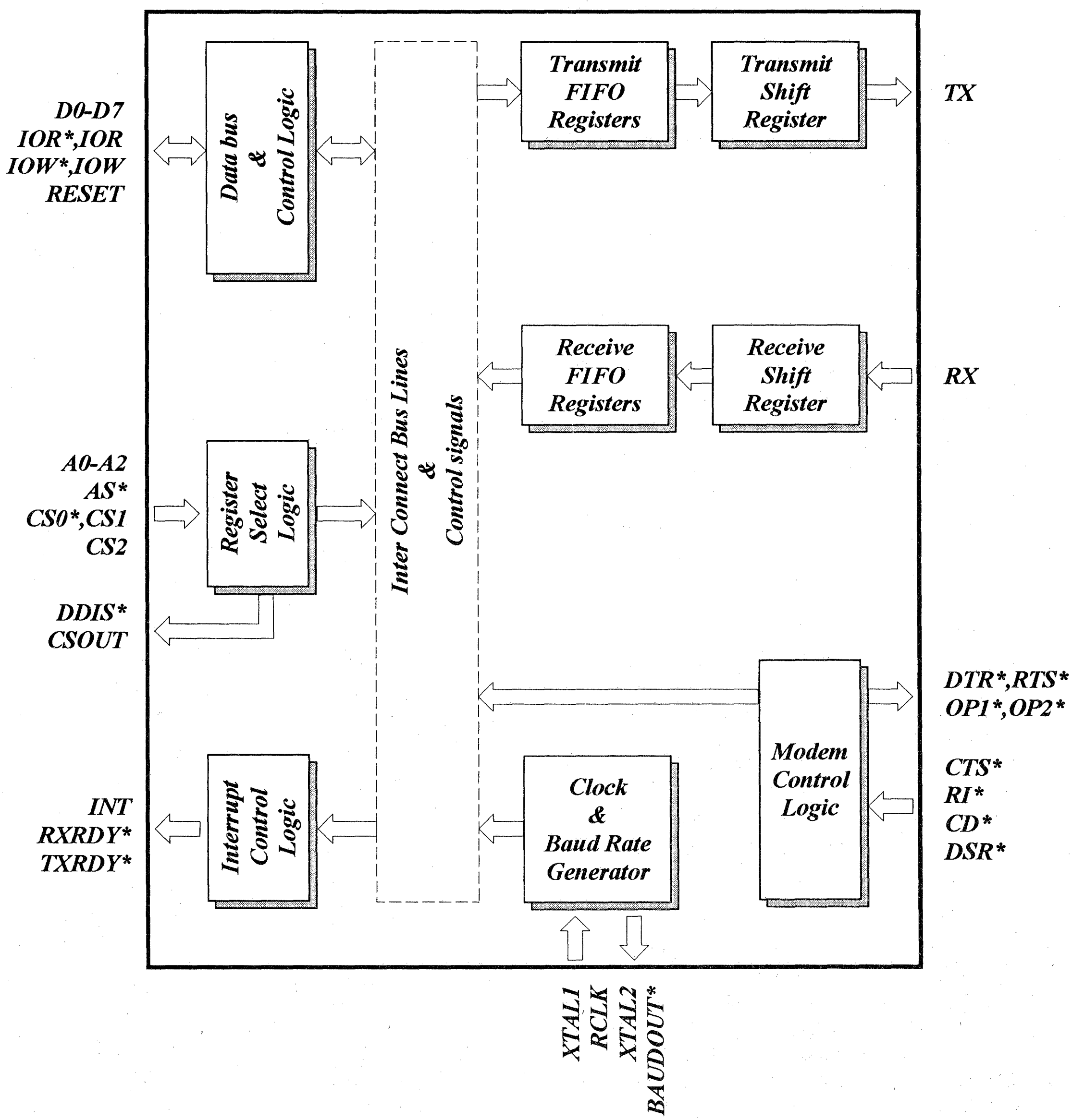
- Pin to pin and functional compatible to NS16550,VL16C550,WD16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C550CP40	Plastic-DIP	0° C to + 70° C
ST16C550CJ44	PLCC	0° C to + 70° C
ST16C550CQ52	QFP	0° C to + 70° C
ST16C550CQ48	TQFP	0° C to + 70° C

***Industrial operating range are available**

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
D0-D7	1-8	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	10	I	Receive clock input. The external clock input to the ST16C550 receiver section if receiver data rate is different from transmitter data rate.
RX	10	11	I	Serial data input. The serial information (data) received from serial port to ST16C550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	13	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	14	I	Chip select 1. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
CS1	13	15	I	Chip select 2. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
CS2*	14	16	I	Chip select 3. (active low) A low at this pin (while CS0=1 and CS1=1) will enable the ST16C550 / CPU data transfer operation.
BAUDOUT*	15	17	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide receive clock.
XTAL1	16	18	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
XTAL2	17	19	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	21	I	Write strobe. (active high) Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C550 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	22	O	Signal and power ground.
IOR*	21	24	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C550 data bus to the CPU.
IOR	22	25	I	Read strobe. (active high) Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C550 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23	26	O	Drive disable. (active low) This pin goes low when the CPU is reading data from the ST16C550 to disable the external transceiver or logic's.
TXRDY*	24	27	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.
AS*	25	28	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	29	I	Address select line 2. To select internal registers.
A1	27	30	I	Address select line 1. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
A0	28	31	I	Address select line 0. To select internal registers.
RXRDY*	29	32	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INT	30	33	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	35	O	General purpose output. (active low) User defined output. See bit-3 modem control register (MCR bit-3).
RTS*	32	36	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	37	O	Data terminal ready. (active low) To indicate that ST16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	38	O	General purpose output. (active low) User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	35	39	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	40	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
DSR*	37	41	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	38	42	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI*	39	43	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	44	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:
0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive

holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C550 has changed state since the last time it was read.
MSR BIT-2:
Indicates that the RI* input to the ST16C550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
RXRDY*	High
TXRDY*	Low
INT	Low

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select	10		25	ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load

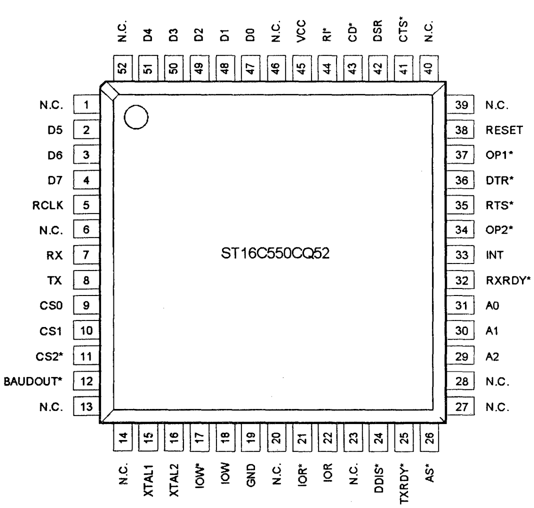
AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

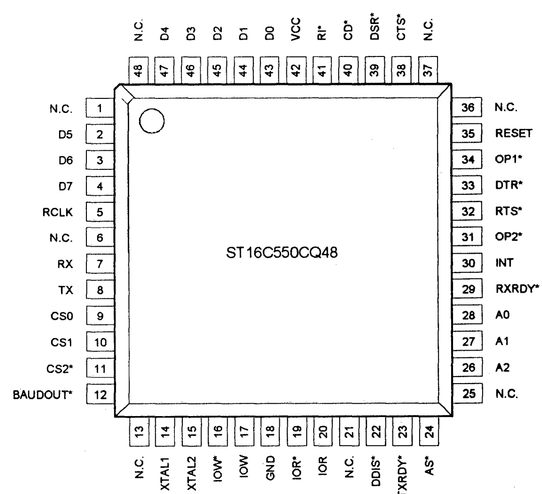
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1 RClk		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1 RCLK		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low
* = Baudout* cycle

52 Pin QFP Package



48 Pin TQFP Package



ABSOLUTE MAXIMUM RATINGS

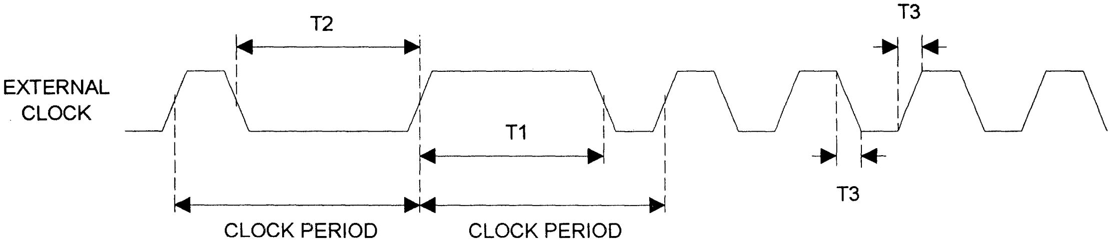
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

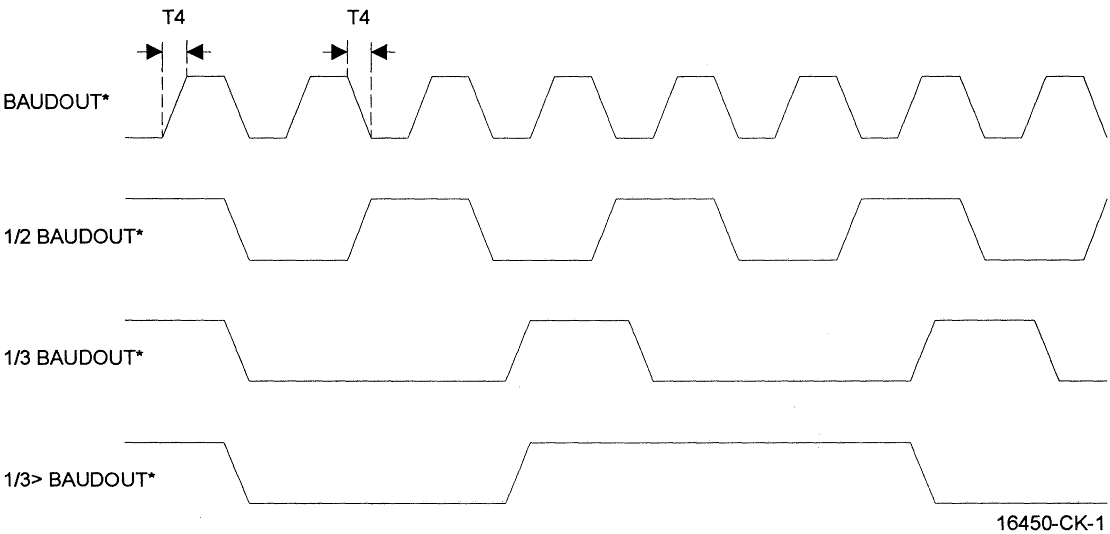
T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	Vcc=5.0 V
V_{IHCK}	Clock input high level	3.0		VCC	V	Vcc=5.0 V
V_{IL}	Input low level	-0.5		0.8	V	Vcc=5.0 V
V_{IH}	Input high level	2.2		VCC	V	Vcc=5.0 V
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{IL}	Input leakage			±10	μA	
I_{CL}	Clock leakage			±10	μA	
V_{ILCK}	Clock input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IHCK}	Clock input high level	2.4		VCC	V	Vcc=3.0 V
V_{IL}	Input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IH}	Input high level	2.0		VCC	V	Vcc=3.0 V
V_{OL}	Output low level on all outputs			0.4	V	Vcc=3.0 V, I_{OL}= 4.2 mA
V_{OH}	Output high level	2.0			V	Vcc=3.0 V, I_{OH}= -1 mA
I_{CC}	Avg power supply current		0.6	0.8	mA	Vcc=3.0 V

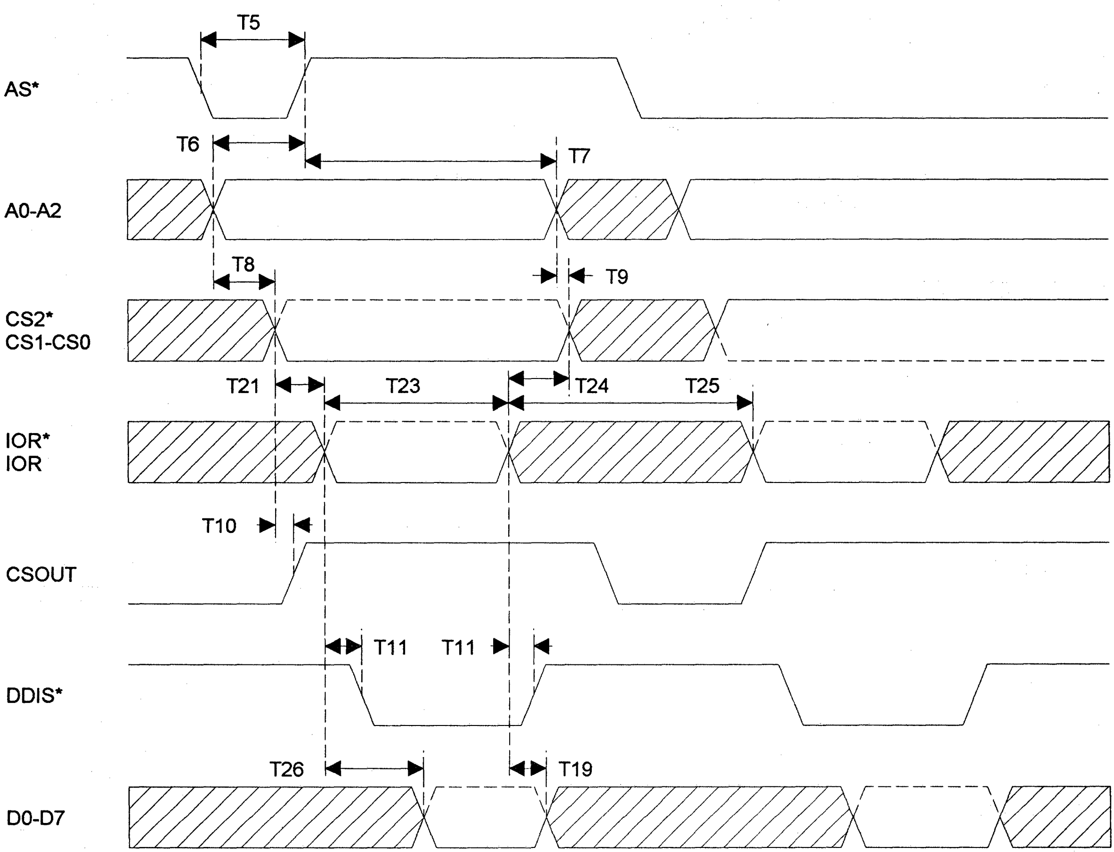
CLOCK TIMING



BAUDOUT* TIMING

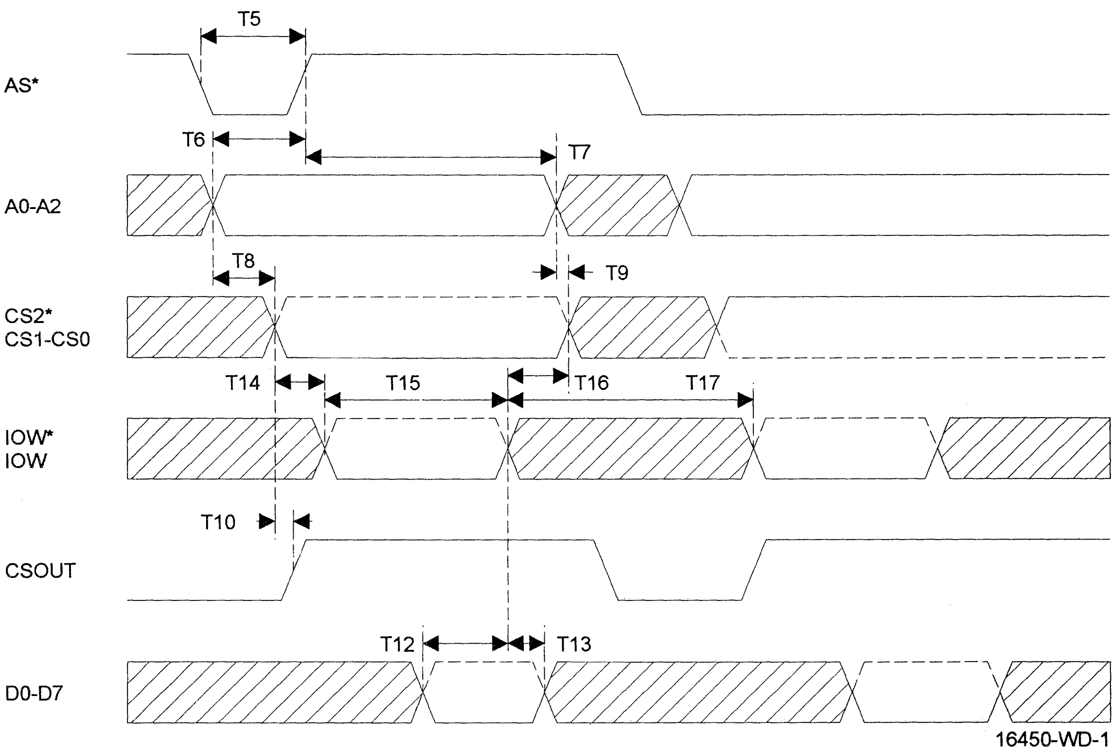


GENERAL READ TIMING

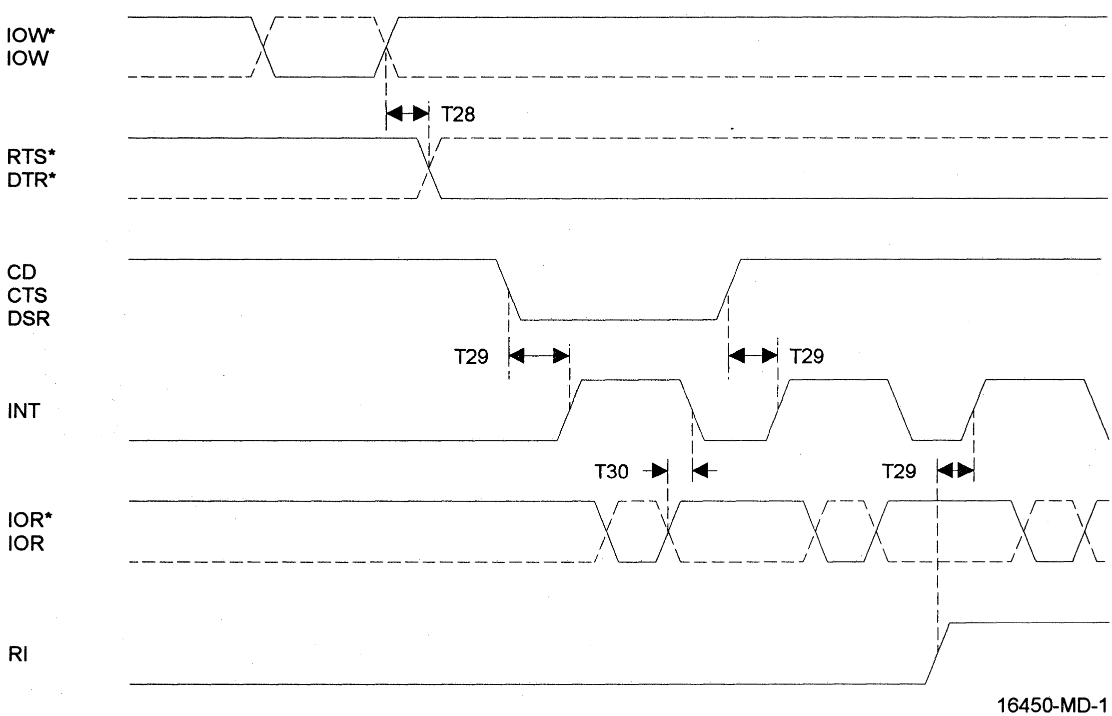


16450-RD-1

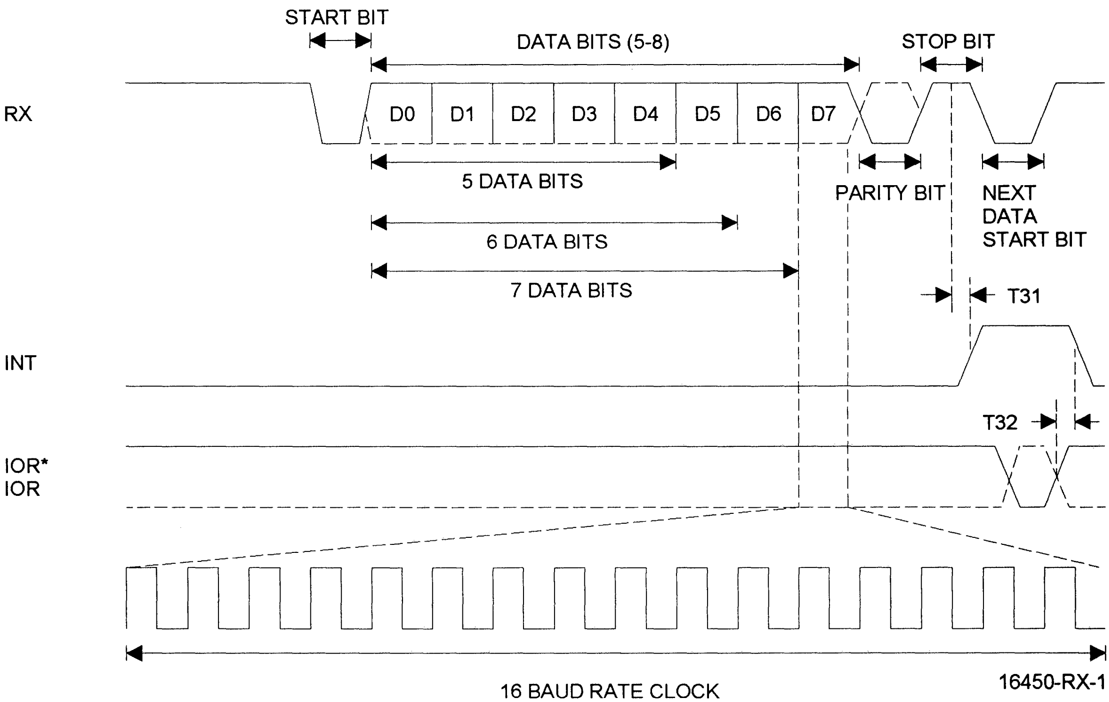
GENERAL WRITE TIMING



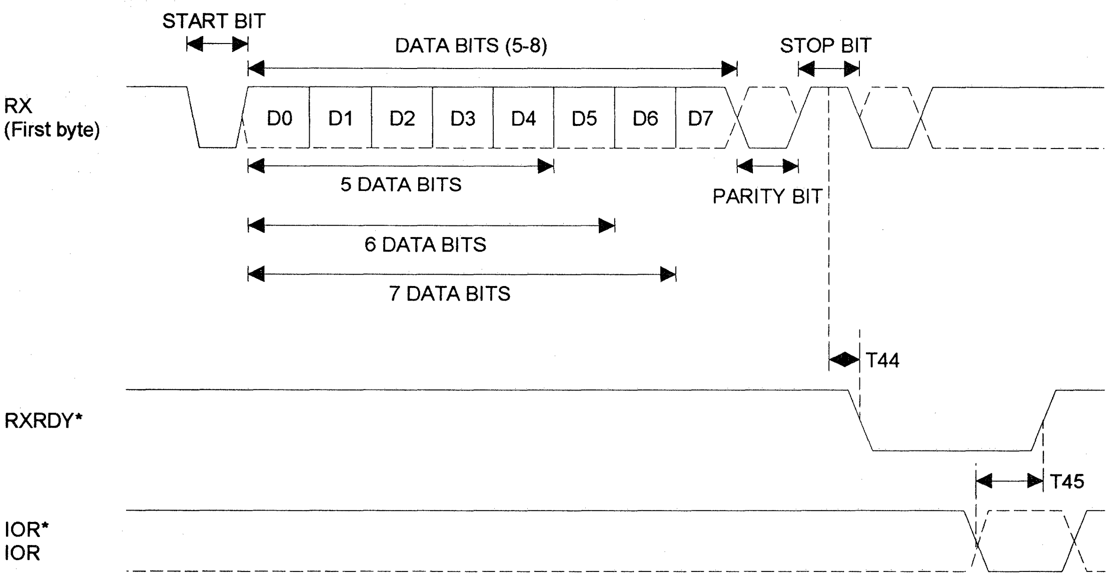
MODEM TIMING



RECEIVE TIMING

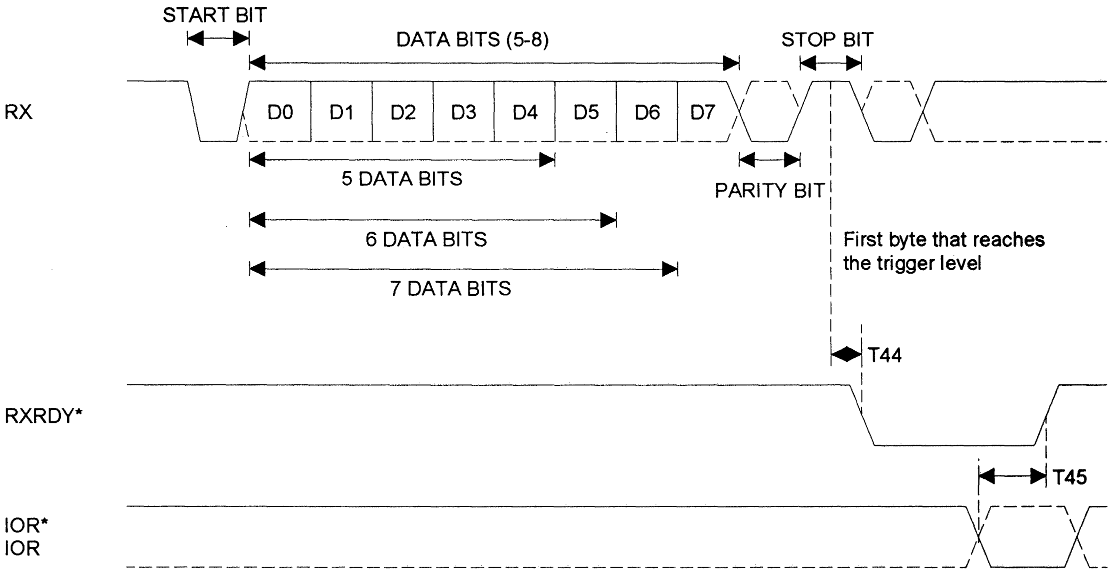


RXRDY TIMING FOR MODE "0"



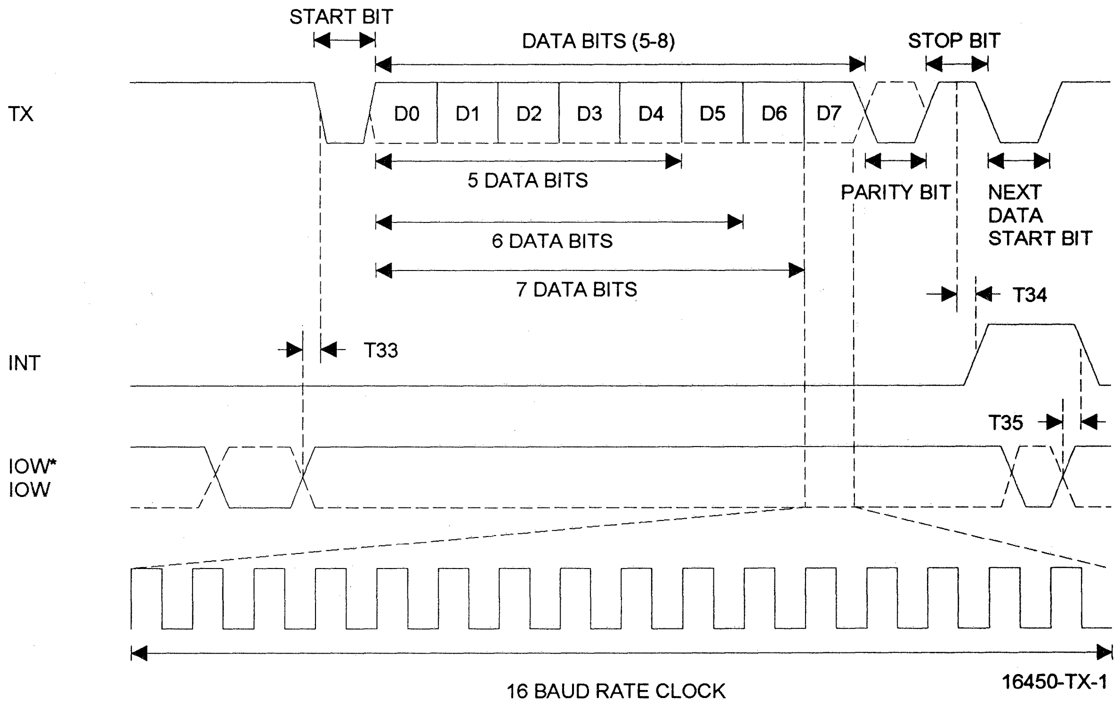
16550-RX-2

RXRDY TIMING FOR MODE "1"

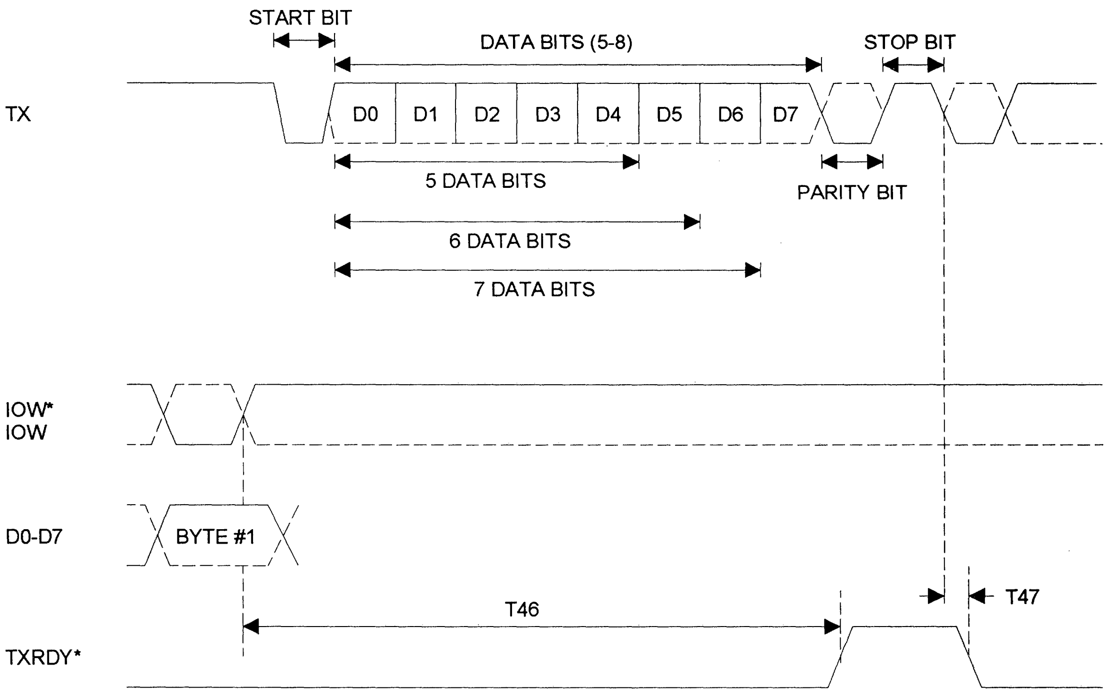


16550-RX-3

TRANSMIT TIMING

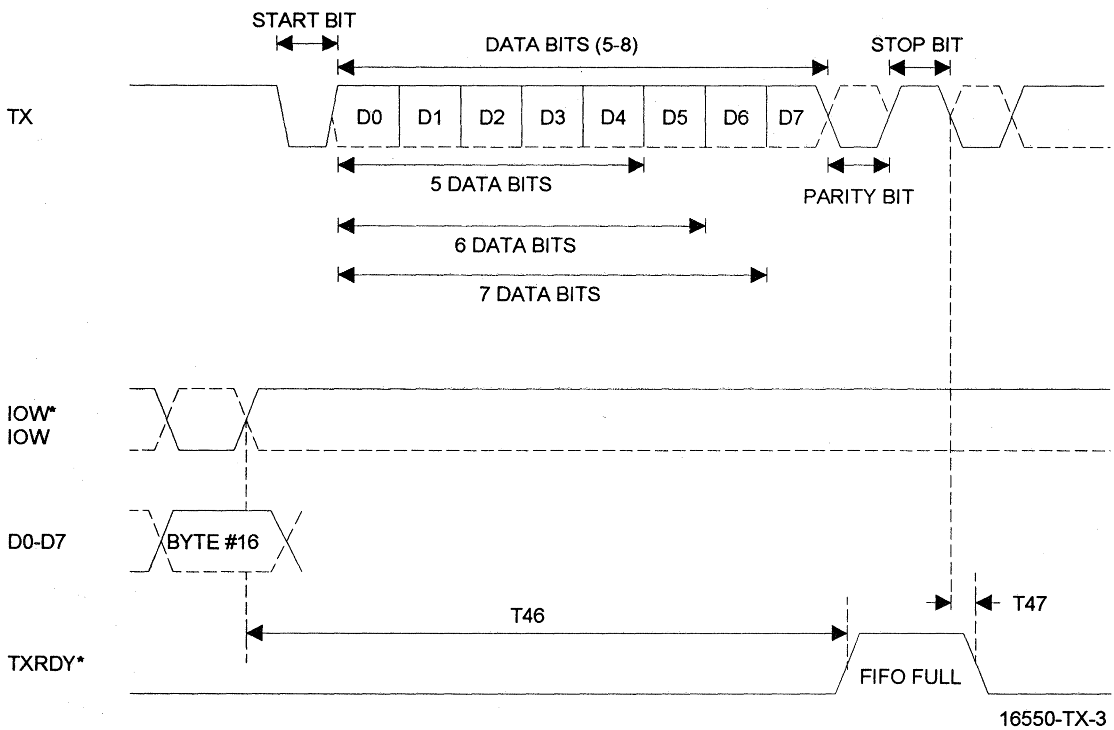


TXRDY TIMING FOR MODE "0"



16550-TX-2

TXRDY TIMING FOR MODE "1"



STARTECH

An EXAR Company

ST16C554D

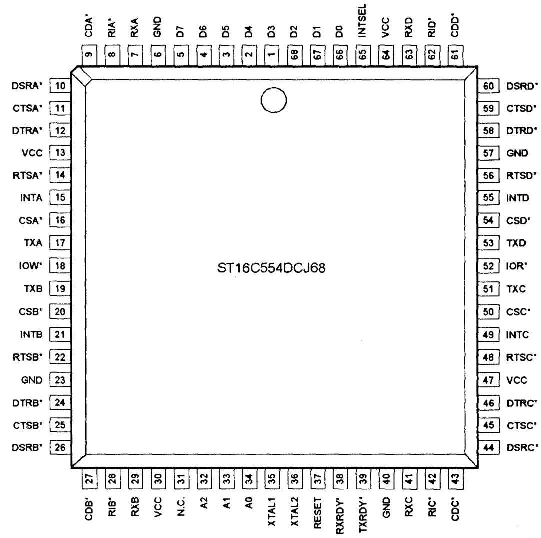
Printed August 3, 1995

QUAD ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.
The ST16C554 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C554 provides internal loop-back capability for on board diagnostic testing.
The ST16C554 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package

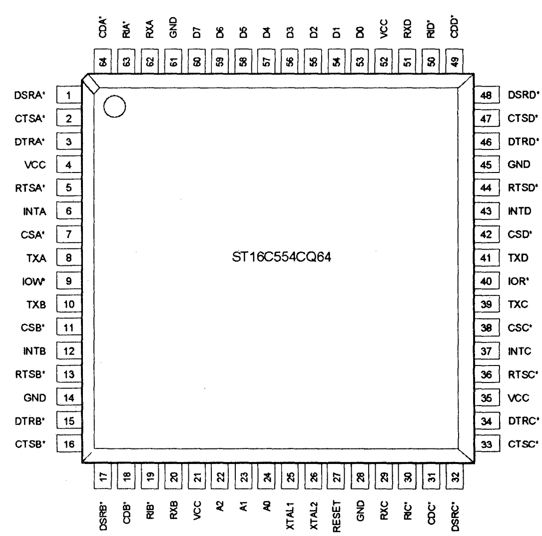


3

FEATURES

- Pin to pin and functional compatible to ST16C454
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

QFP Package

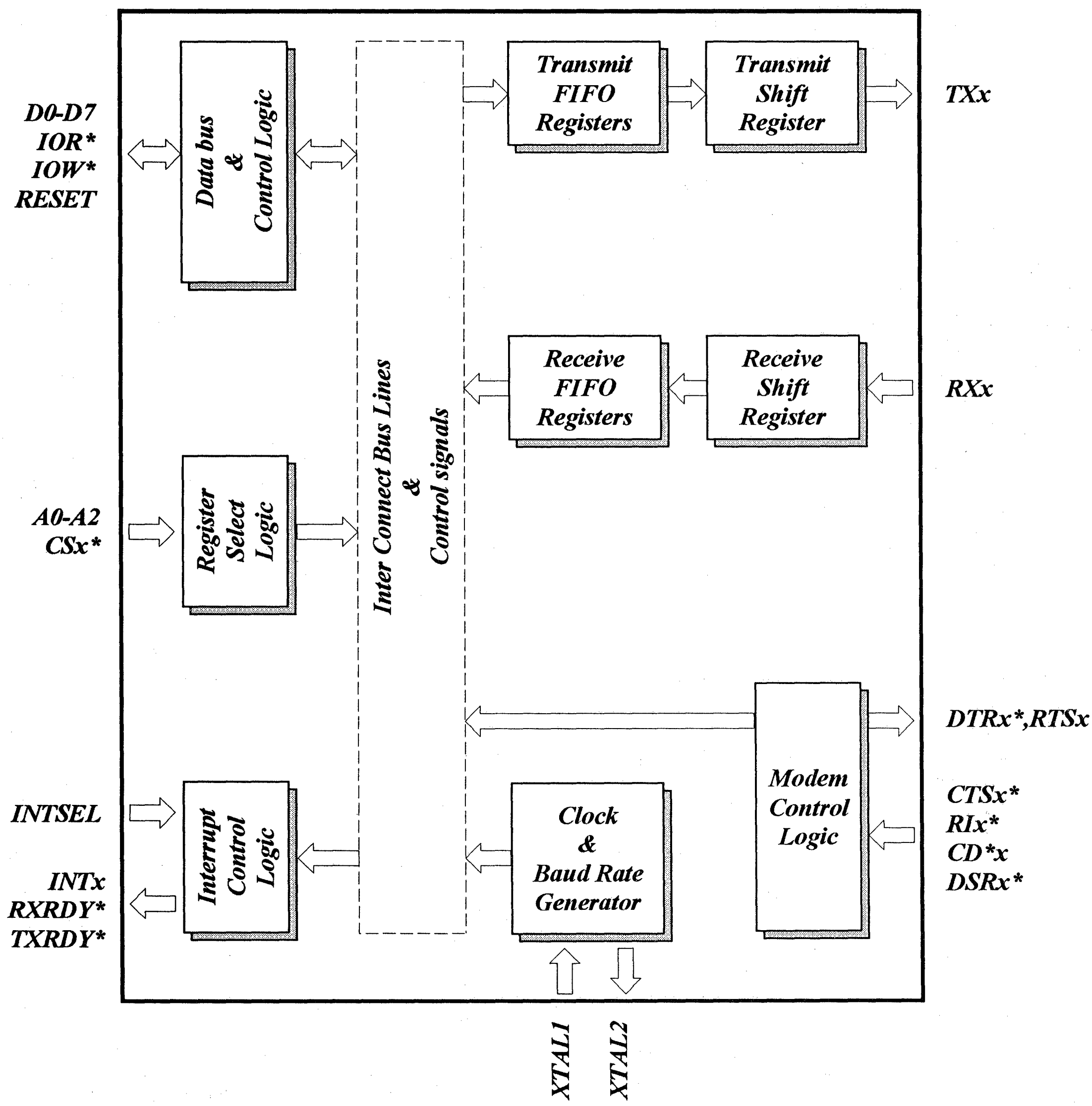


ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554CQ64	QFP	0° C to + 70° C
ST16C554DCQ64	QFP	0° C to + 70° C
ST16C554DCJ68	PLCC	0° C to + 70° C
ST16C554DIJ68	PLCC	-40° C to + 85° C

Rev. 1.0

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input. The serial information (data) received from serial port to ST16C554 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS* A-B CS* C-D	16,20 50,54	I	Chip select. (active low) A low at this pin enables the ST16C554 / CPU data transfer operation. Each UART sections of the ST16C554 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	O	Signal and power ground.
IOR*	52	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C554 data bus to the CPU.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
TXRDY*	39	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the ST16C554 is full. It can be used as a single or multi-transfer.
A2	32	I	Address select line 2. To select internal registers.
A1	33	I	Address select line 1. To select internal registers.
A0	34	I	Address select line 0. To select internal registers.
RXRDY*	38	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL	65	I	Interrupt type select. Enable /disable the interrupt three state function. Normal interrupt output can be selected by connecting this pin to VCC (MCR bit-3 does not have any effect on the interrupt output). The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is set to "1".
INT A-B INT C-D	15,21 49,55	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS* A-B RTS* C-D	14,22 48,56	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* A-B DTR* C-D	12,24 46,58	O	Data terminal ready. (active low) To indicate that ST16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS* A-B CTS* C-D	11,25 45,59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR* A-B DSR* C-D	10,26 44,60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD* A-B CD* C-D	9,27 43,61	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI* A-B RI* C-D	8,28 42,62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13,30 47,64	I	Power supply input.

ST16C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C554 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C554 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C554 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used, except in internal loop-back mode.

MCR BIT-3:
0=set the INT A-D output pin to three state mode..
1=Enable the INT A-D output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C554 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register

MSR BIT-0:
Indicates that the CTS* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX A-D	High
RTS* A-D	High
DTR* A-D	High
RXRDY*	High
TXRDY*	Low
INT A-D	Three state mode

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

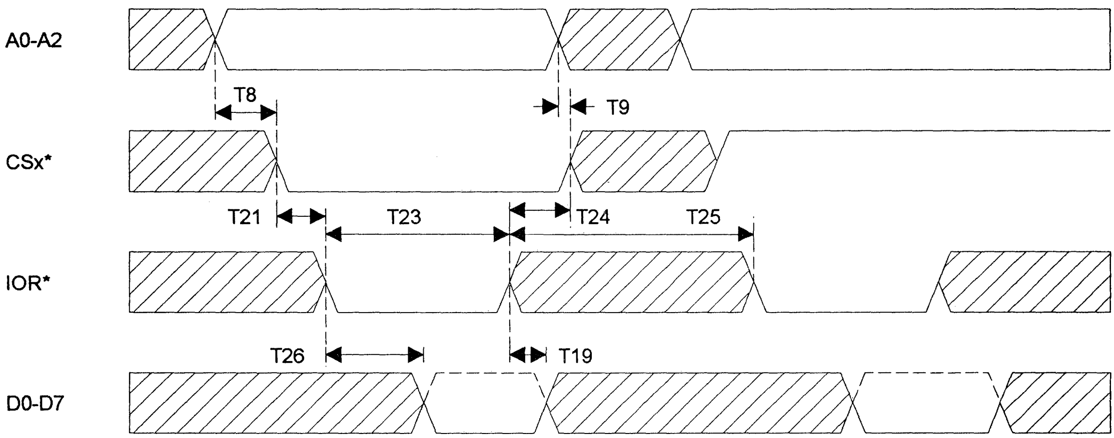
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

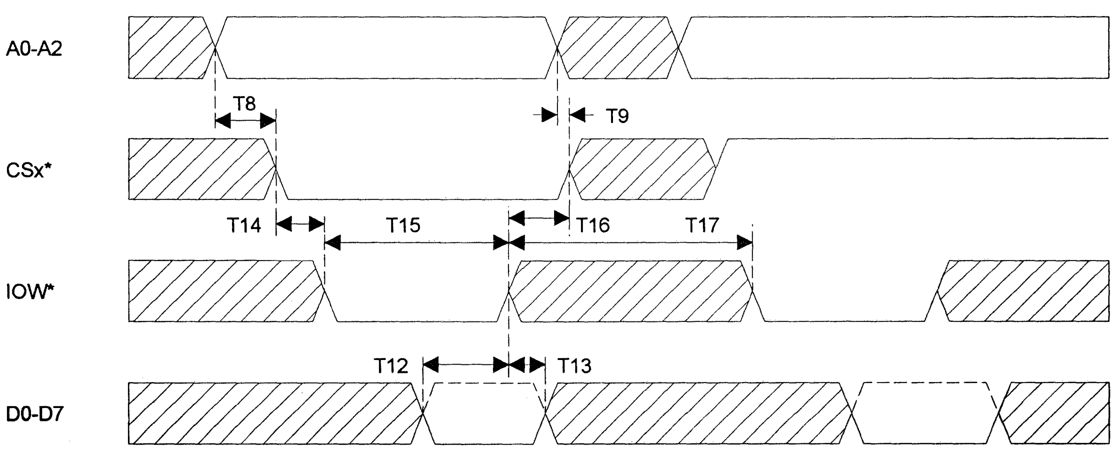
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current		6	14	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
V_{ILCK}	Clock input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IHCK}	Clock input high level	2.4		VCC	V	Vcc=3.0 V
V_{IL}	Input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IH}	Input high level	2.0		VCC	V	Vcc=3.0 V
V_{OL}	Output low level on all outputs			0.4	V	Vcc=3.0 V, I_{OL}= 8.5 mA
V_{OH}	Output high level	2.0			V	Vcc=3.0 V, I_{OH}= -4 mA
I_{CC}	Avg power supply current		10	12	mA	Vcc=3.0 V

GENERAL READ TIMING



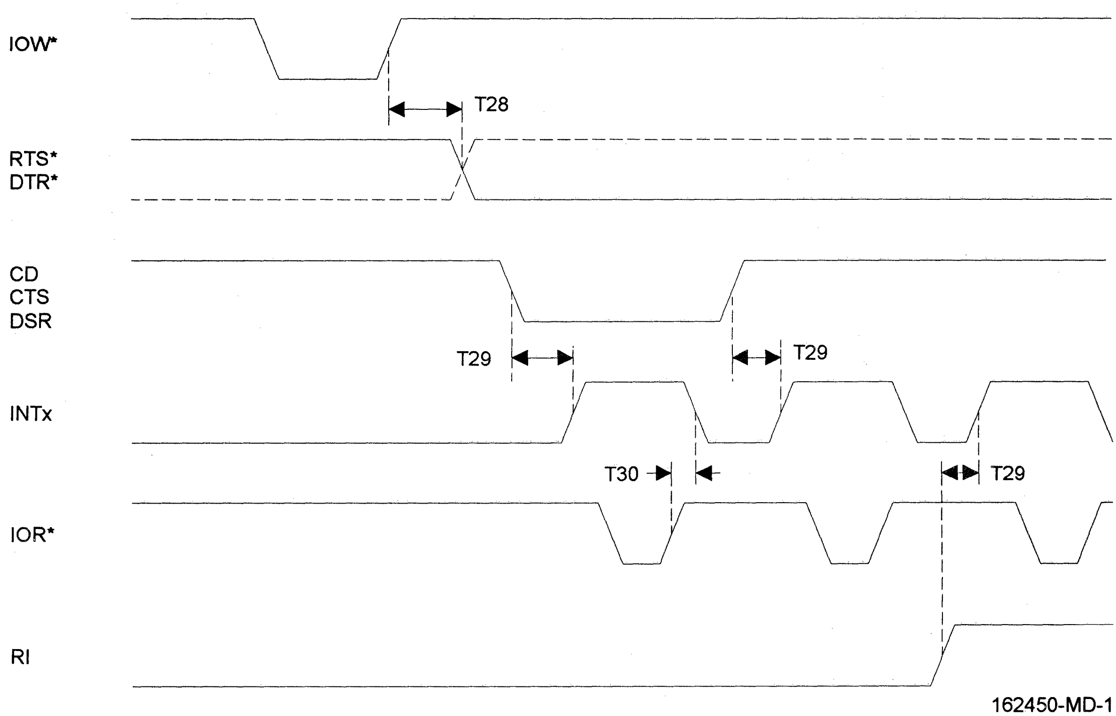
162450-RD-1

GENERAL WRITE TIMING

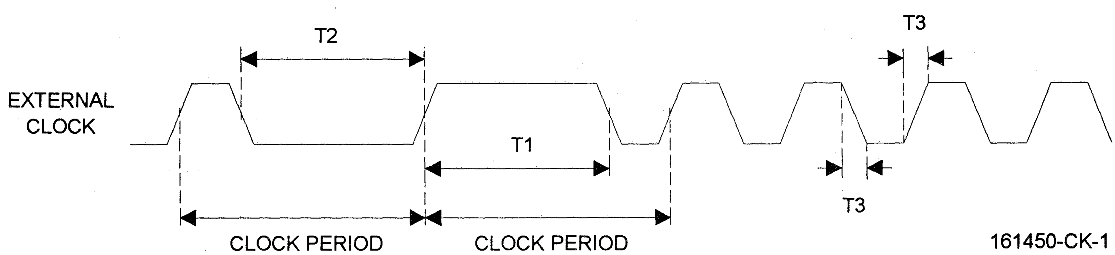


162450-WD-1

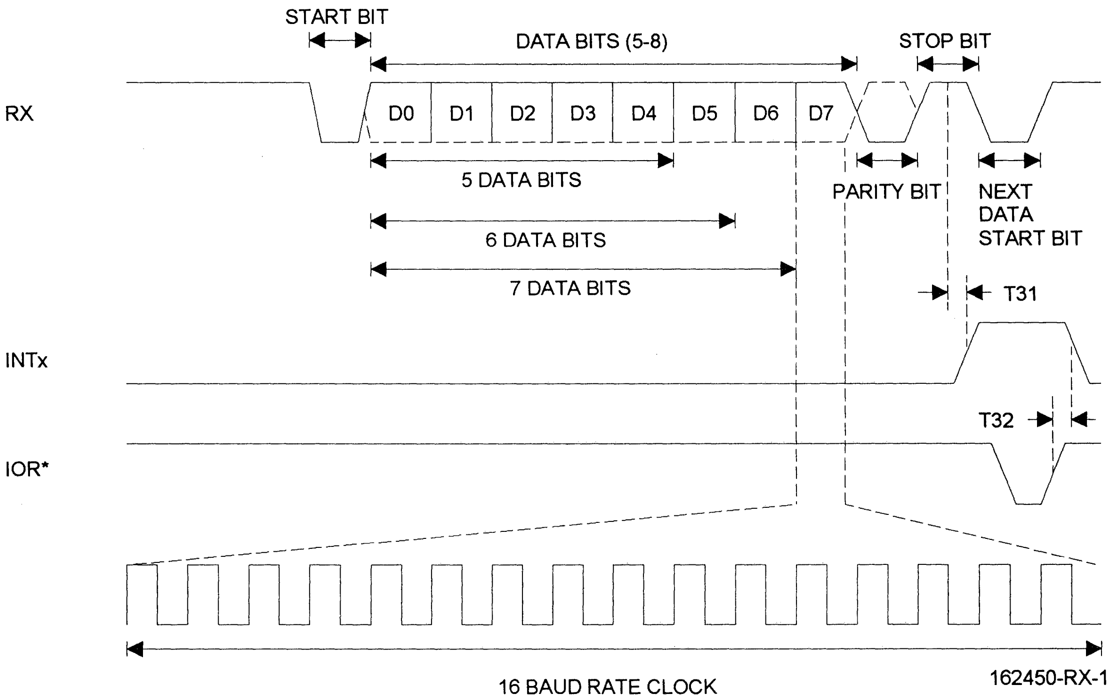
MODEM TIMING



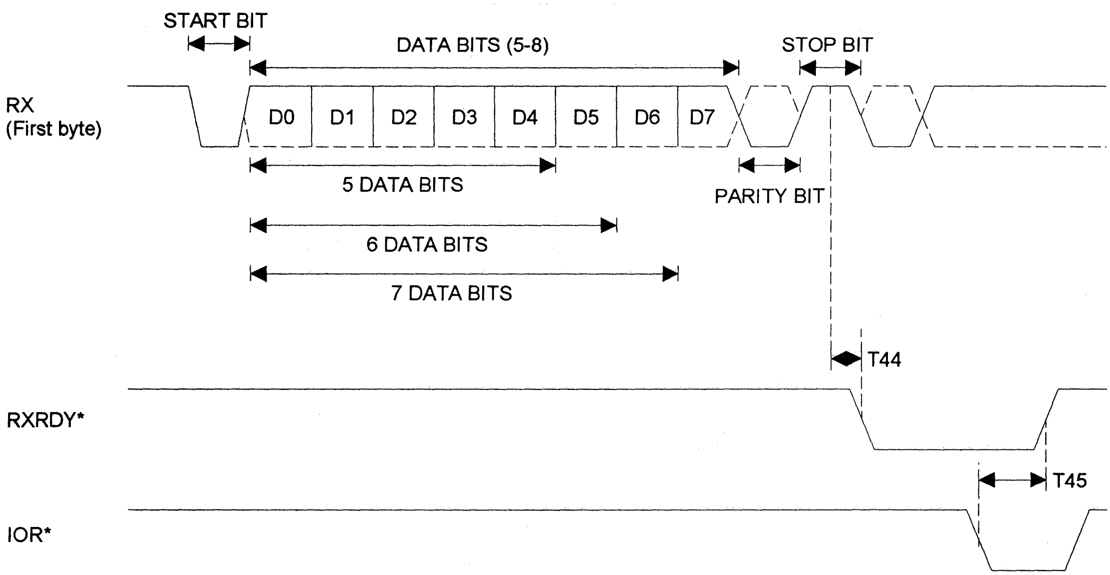
CLOCK TIMING



RECEIVE TIMING

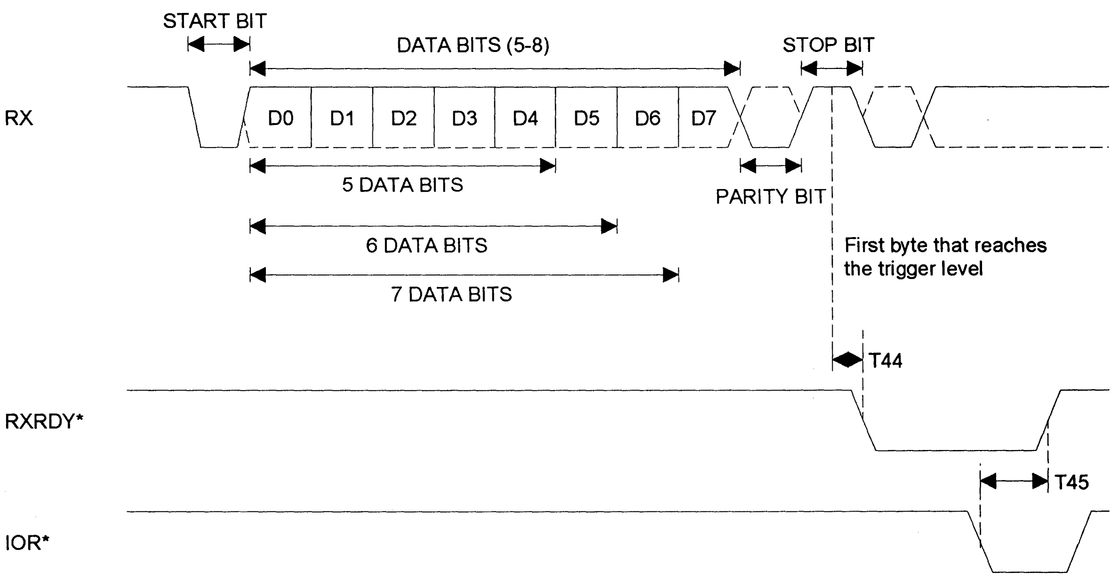


RXRDY TIMING FOR MODE "0"



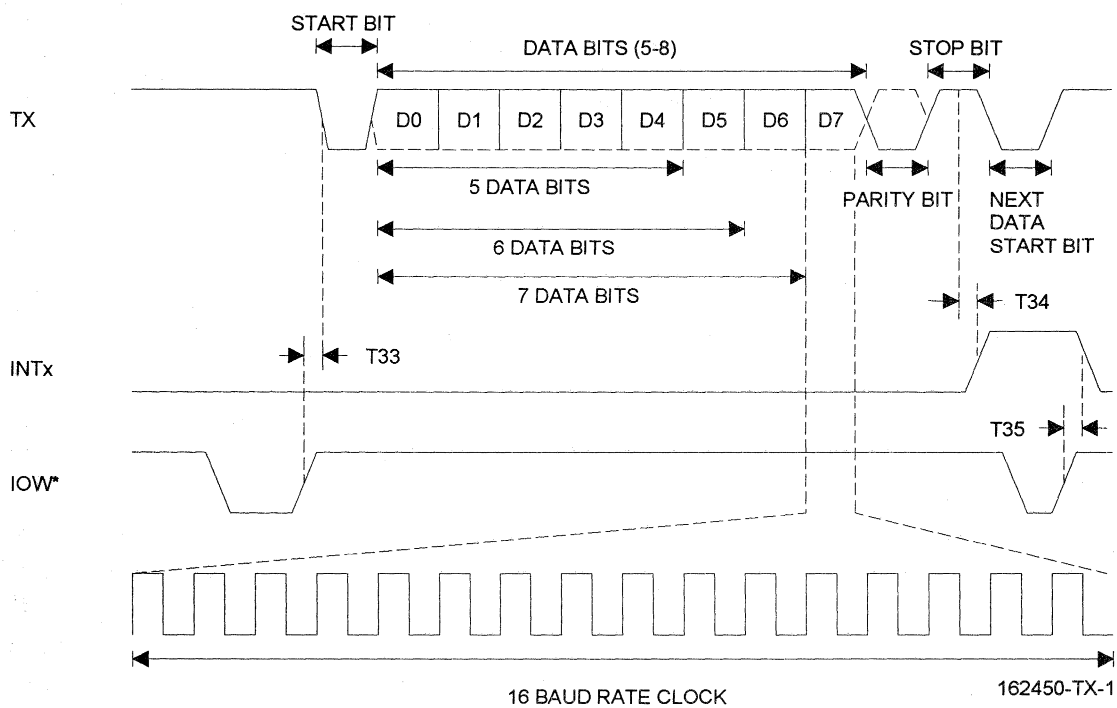
16552-RX-2

RXRDY TIMING FOR MODE "1"

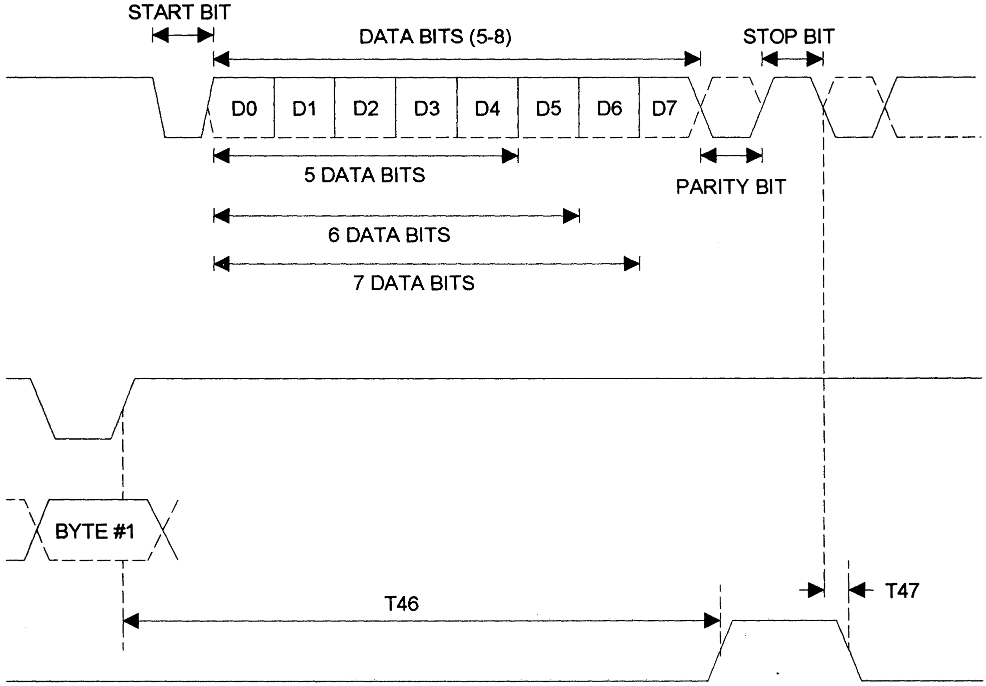


16552-RX-3

TRANSMIT TIMING

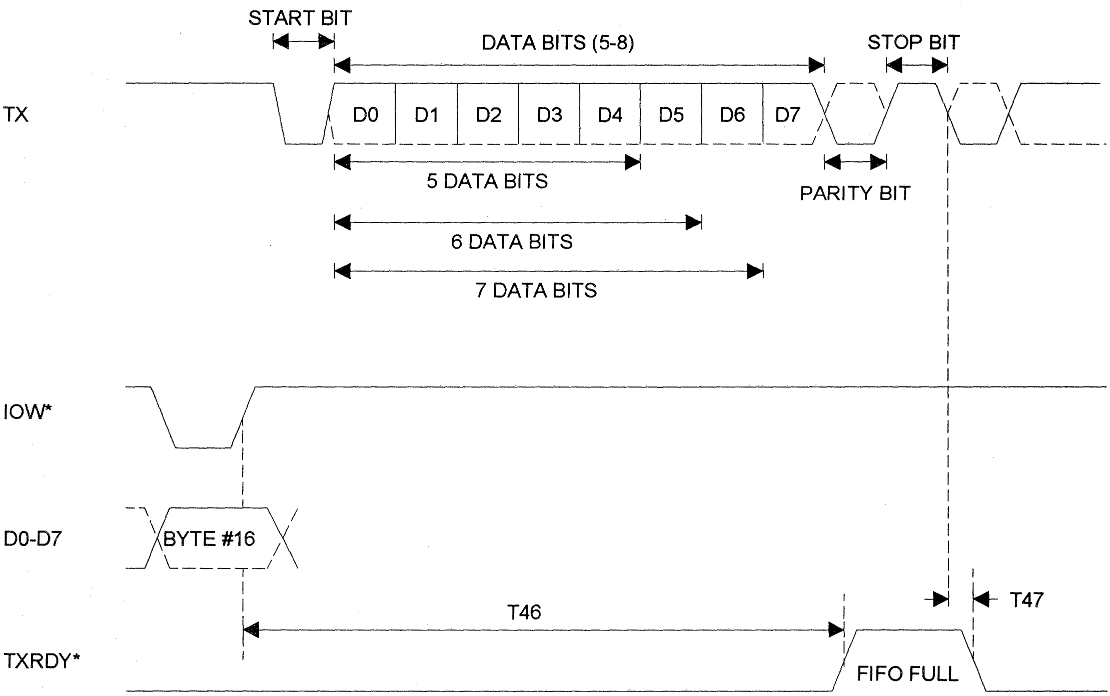


TXRDY TIMING FOR MODE "0"



16552-TX-2

TXRDY TIMING FOR MODE "1"



16552-TX-3

STARTECH

An EXAR Company

ST68C554

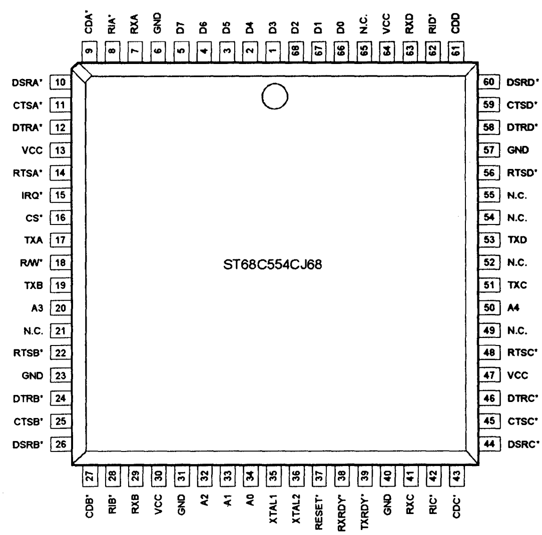
Printed August 3, 1995

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

DESCRIPTION

The ST68C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.
The ST68C554 is an improved, quad version of the NS16550 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.
The ST68C554 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



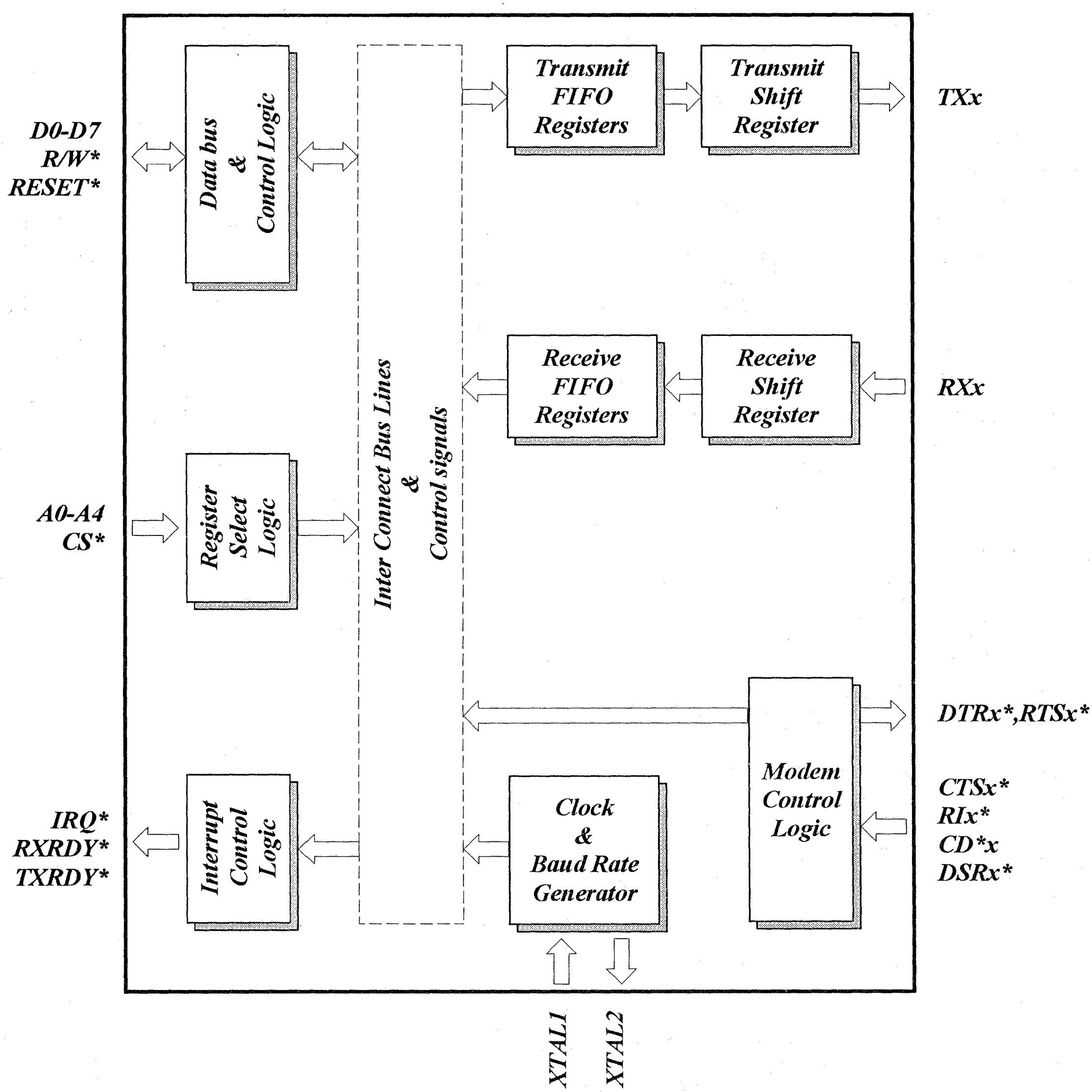
FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- 460.8 kHz transmit/receive operation with 7.372 MHz external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C554CJ68	PLCC	0° C to +70° C
ST68C554IJ68	PLCC	-40° C to +85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66	I/O	Bi-directional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B RX C/D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST68C554 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B TX C/D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	16	I	Chip select (active low). A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2. See XTAL1.
R/W*	18	I	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C554 data bus to the CPU.
CD* A/B CD* C/D	9,27 43,61	I	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23,31 40,57	O	Signal and power ground.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DSR* A/B DSR* C/D	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
RI* A/B RI* C/D	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTS* A/B RTS* C/D	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS* A/B CTS* C/D	11,25 45,59	I	Clear to send A-D. (active low) The CTS* signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmitter output.
A4	50	I	Address line 4. To select one of the four UARTS.
A3	20	I	Address line 3. To select one of the four UARTS.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
IRQ*	15	O	Interrupt output. (active low open collector) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR* A/B DTR* C/D	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			ST68C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET*	37	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.
TXRDY*	39	O	Transmit ready (active low). This pin goes high when the transmit FIFO of the ST68C554 (any one) is full. It can be used as a single or multi-transfer DMA.
RXRDY*	38	O	Receive ready (active low). This pin goes low when the receive FIFO of the ST68C554 is full. It can be used as a single or multi-transfer DMA.

SERIAL PORT SELECTION GUIDE

CS*	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST68C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The ST68C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to $2^{16}-1$. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D

The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the IRQ* output pin.

IER BIT-0:
0=disable the receiver ready interrupt
1=enable the receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable the modem status register interrupt
1=enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D

The ST68C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C554 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-5:
These bits are not used and are set zero.

ISR BIT 6-7:
0=Normal mode.
1=FIFO's are enabled.

FIFO CONTROL REGISTER (FCR)
This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST68C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST68C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST68C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST68C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.

0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TX A-D) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high
1=force DTR* output to low

MCR BIT-1:
0=force RTS* output to high
1=force RTS* output to low

MCR BIT2-3:
x=not used

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D*, DSR A-D*, CD A-D*, and RI A-D*) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D*, RTS A-D* and MCR A-D bit-2,3 are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST68C554 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A-D

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST68C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loopback mode. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D

ST68C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16xCLOCK %ERROR	DVISOR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST68C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
RTS* A-D	High
DTR* A-D	High
RXRDY*	High
TXRDY*	Low
IRQ	Three state mode

ST68C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR FIFOs	0/ FIFOs enabled	0/ enabled	0	0 priority	int priority bit-2	int priority bit-1	int status bit-0	int
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	Not used	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time from write or CS*	5			ns	
T_{14}	Write set up time	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	15			ns	
T_{17}	Write cycle delay	45			ns	
T_{18}	Data setup time	15			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{24}	Data hold time	0			ns	
T_{25}	Read cycle delay	25			ns	
Tr	Read cycle=T_{18}+T_{25}	105			ns	
T_{27}	Chip select pulse width	75			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			35	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from read (CS*) to reset RxRdy			1	µs	
T_{46}	Delay from write to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

* = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

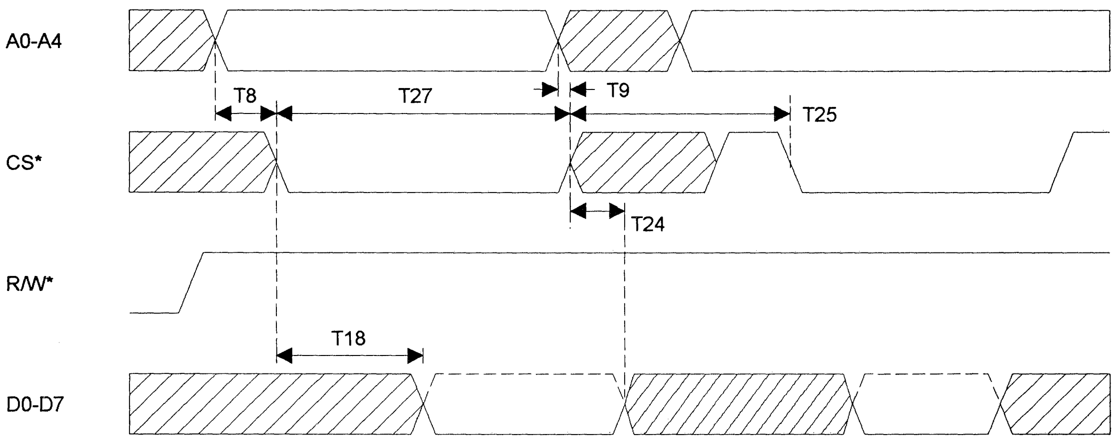
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

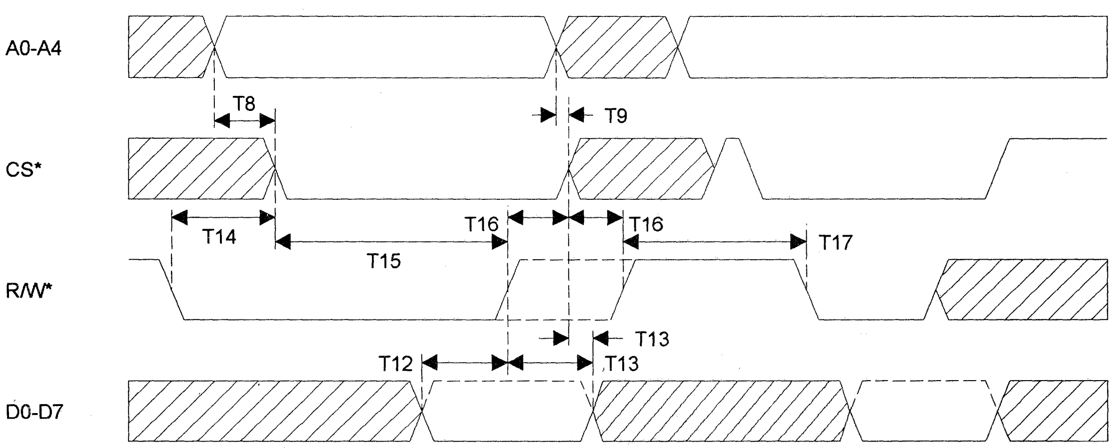
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6	12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
V_{ILCK}	Clock input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IHCK}	Clock input high level	2.4		VCC	V	Vcc=3.0 V
V_{IL}	Input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IH}	Input high level	2.0		VCC	V	Vcc=3.0 V
V_{OL}	Output low level on all outputs			0.4	V	Vcc=3.0 V, I_{OL}= 8.5 mA
V_{OH}	Output high level	2.0			V	Vcc=3.0 V, I_{OH}= -4 mA
I_{CC}	Avg power supply current		10	12	mA	Vcc=3.0 V

GENERAL READ TIMING



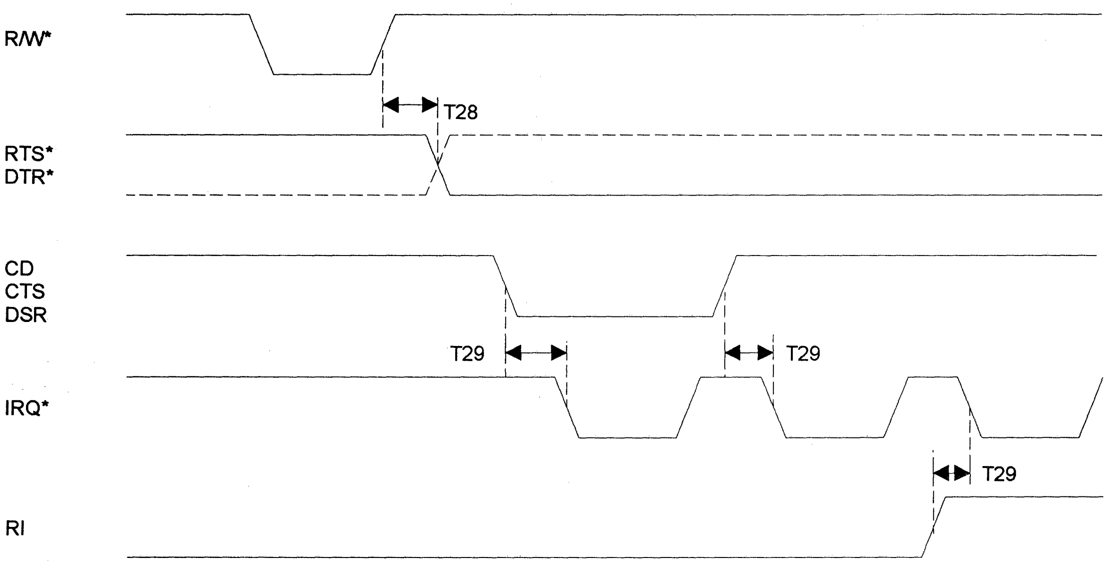
8454-RD-1

GENERAL WRITE TIMING



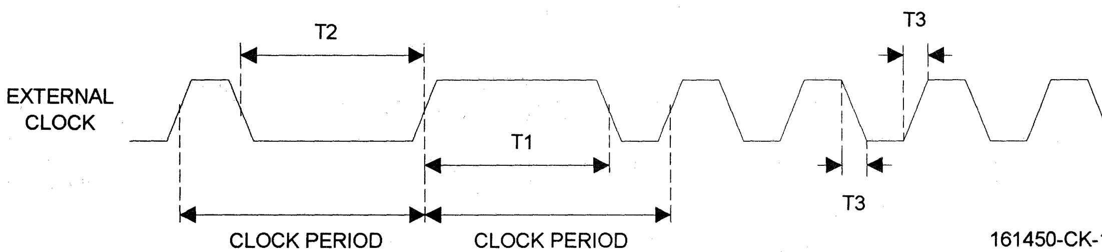
68454-WD-1

MODEM TIMING



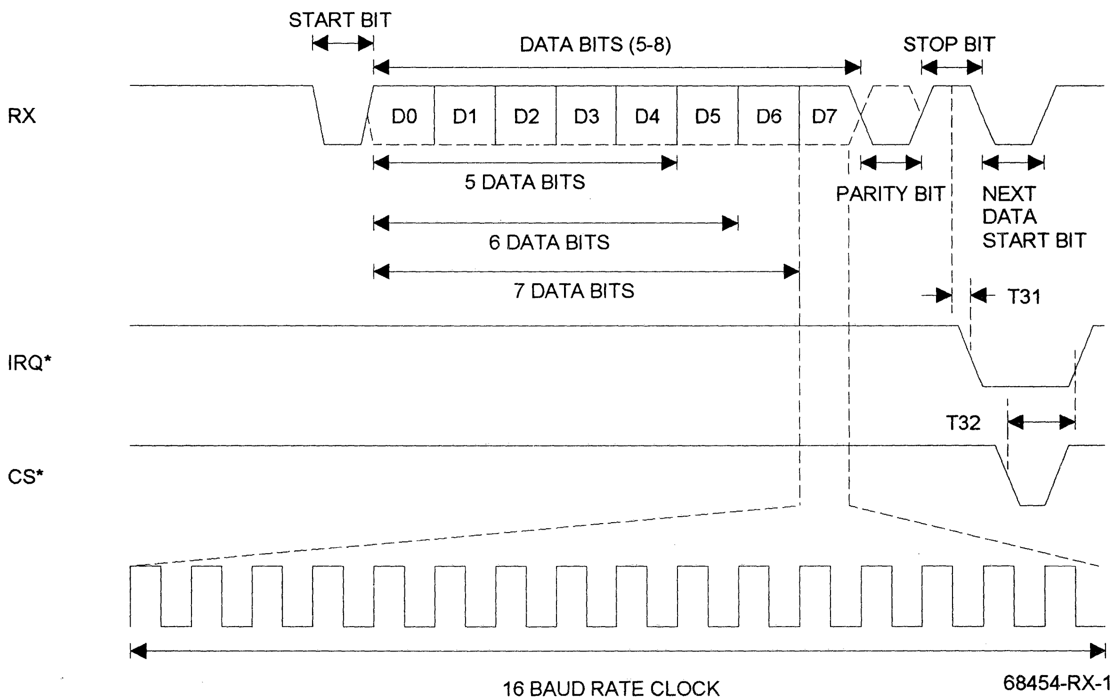
68454-MD-1

CLOCK TIMING



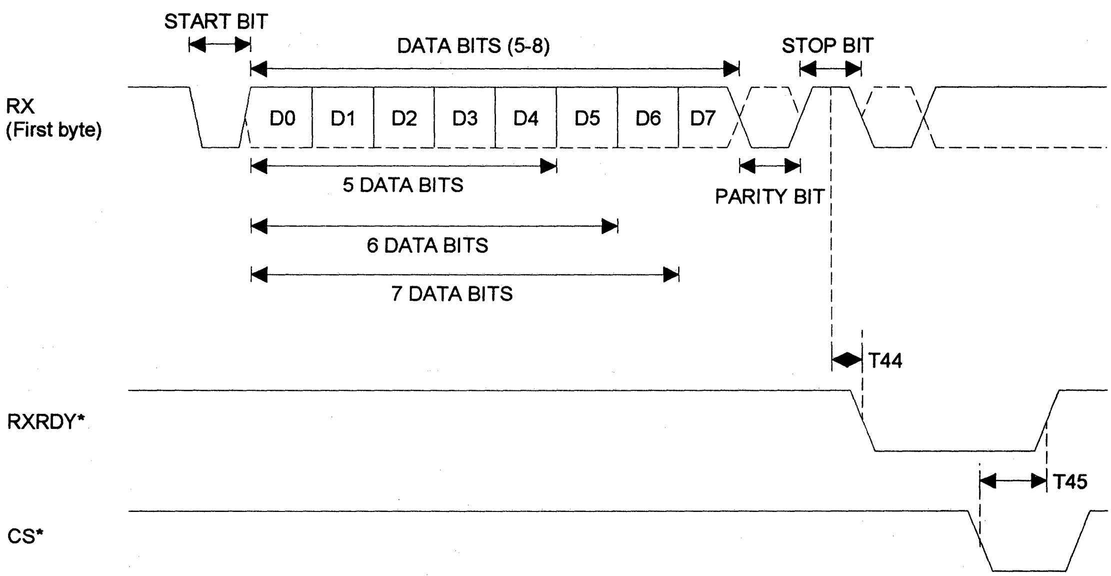
161450-CK-1

RECEIVE TIMING



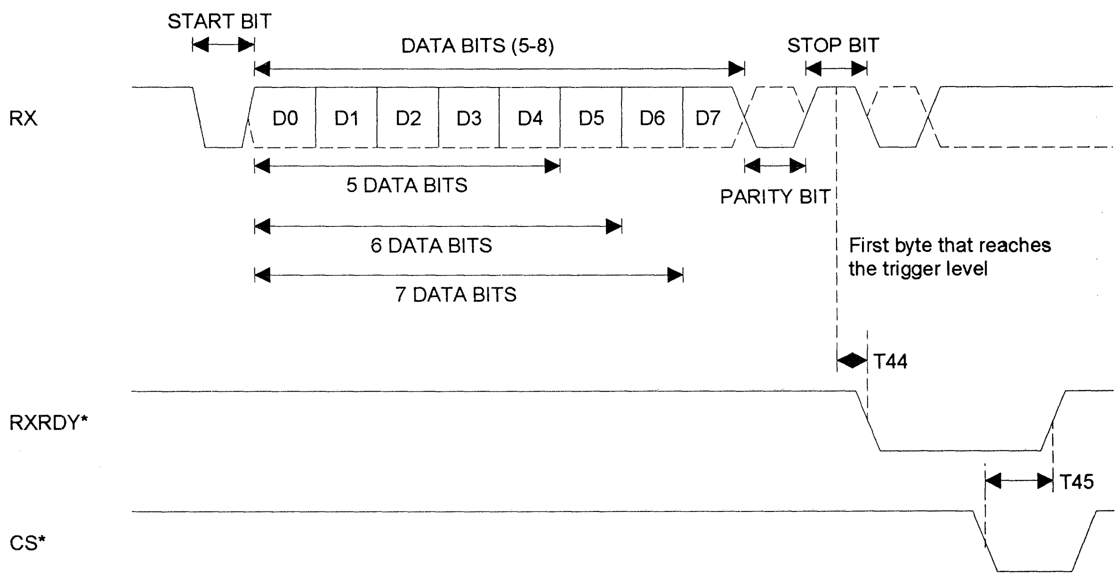
68454-RX-1

RXRDY TIMING FOR MODE "0"



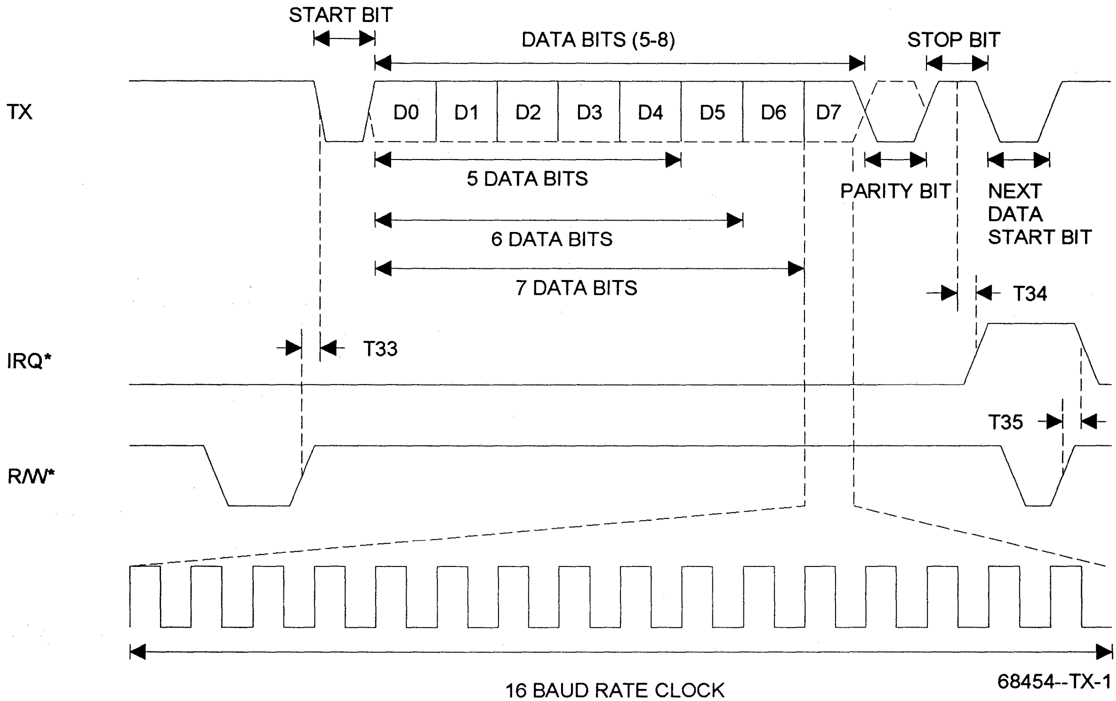
68554-RX-2

RXRDY TIMING FOR MODE "1"

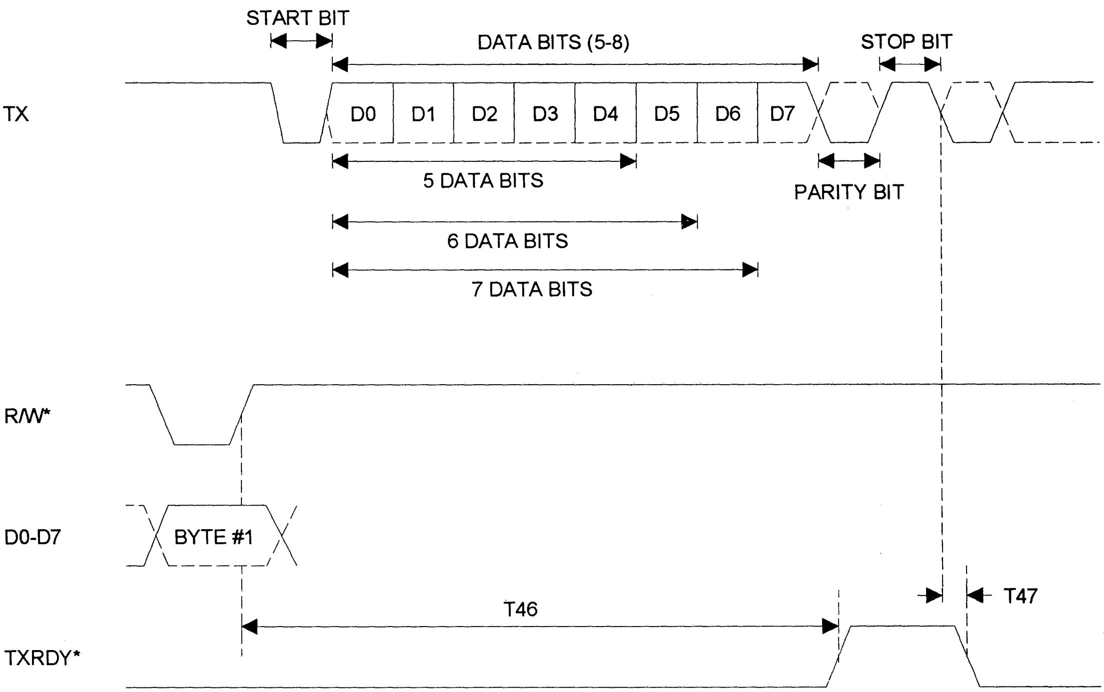


68554-RX-3

TRANSMIT TIMING

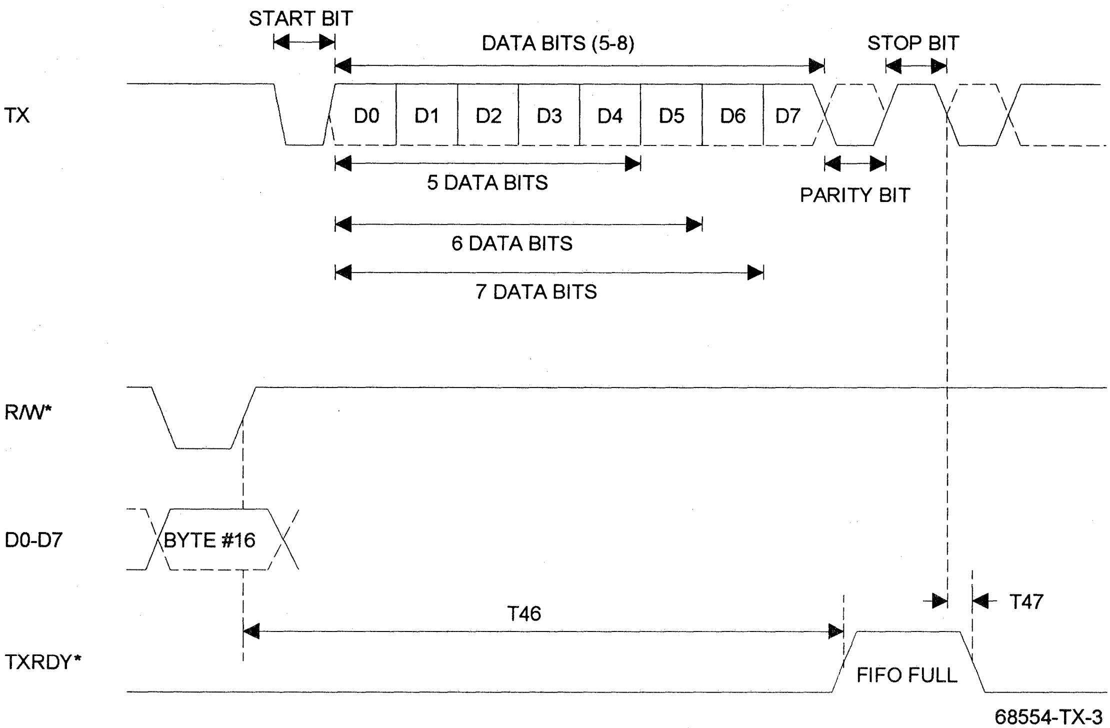


TXRDY TIMING FOR MODE "0"



68554-TX-2

TXRDY TIMING FOR MODE "1"



STARTECH

An EXAR Company

ST16C650

Printed August 3, 1995

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO's AND INFRA-RED ENCODER/DECODER

DESCRIPTION

The ST16C650 is a universal asynchronous receiver and transmitter with 32 bytes transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

The ST16C650 is an improved version of the ST16C550 UART with deeper FIFO, software/ hardware flow control. The ST16C650 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C650 provides internal loop-back capability for on board diagnostic testing. The ST16C650 provides pin selectable interface mode to function as stand alone ST16C550 or direct PC connect.

The ST16C650 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

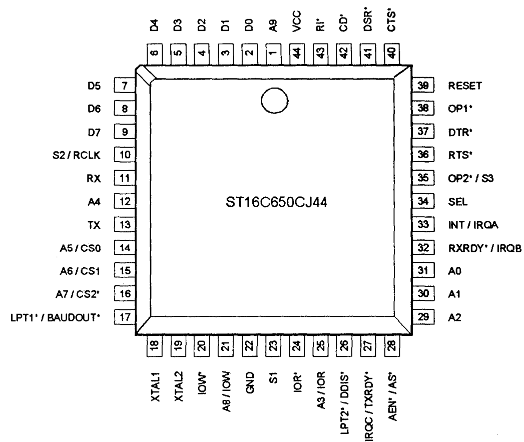
- Pin to pin and functional compatible to NS16550, VL16C550, WD16C550, ST16C550
- 32 byte transmit FIFO
- 32 byte receive FIFO with error flags
- Pin selectable interface mode
- Software/Hardware flow control
- Programmable Xon/Xoff characters
- Sleep mode (800μA stand-by)
- Low operating current (1.5mA typ.)
- Independent transmit and receive control
- 460.8 kHz transmit/receive operation
- Selectable Transmit/Receive trigger levels
- Infrared receive and transmit, input / output.

ORDERING INFORMATION

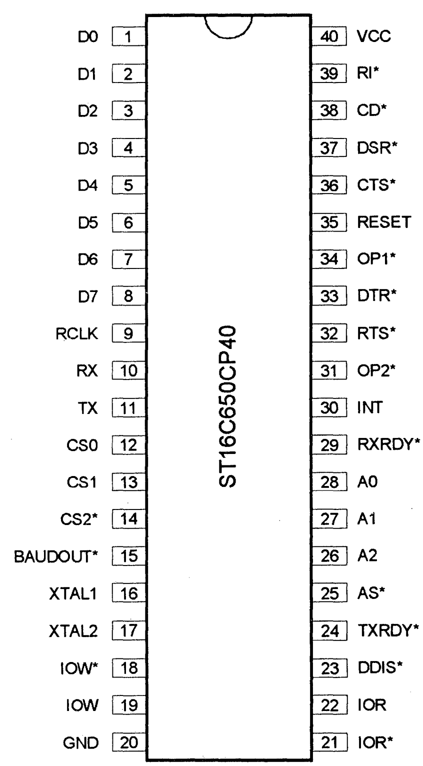
Part number	Package	Operating temperature
ST16C650CP40	Plastic-DIP	0° C to + 70° C
ST16C650CJ44	PLCC	0° C to + 70° C
ST16C650CQ52	QFP	0° C to + 70° C
ST16C650CQ48	TQFP	0° C to + 70° C

***Industrial operating range are available**

PLCC Package

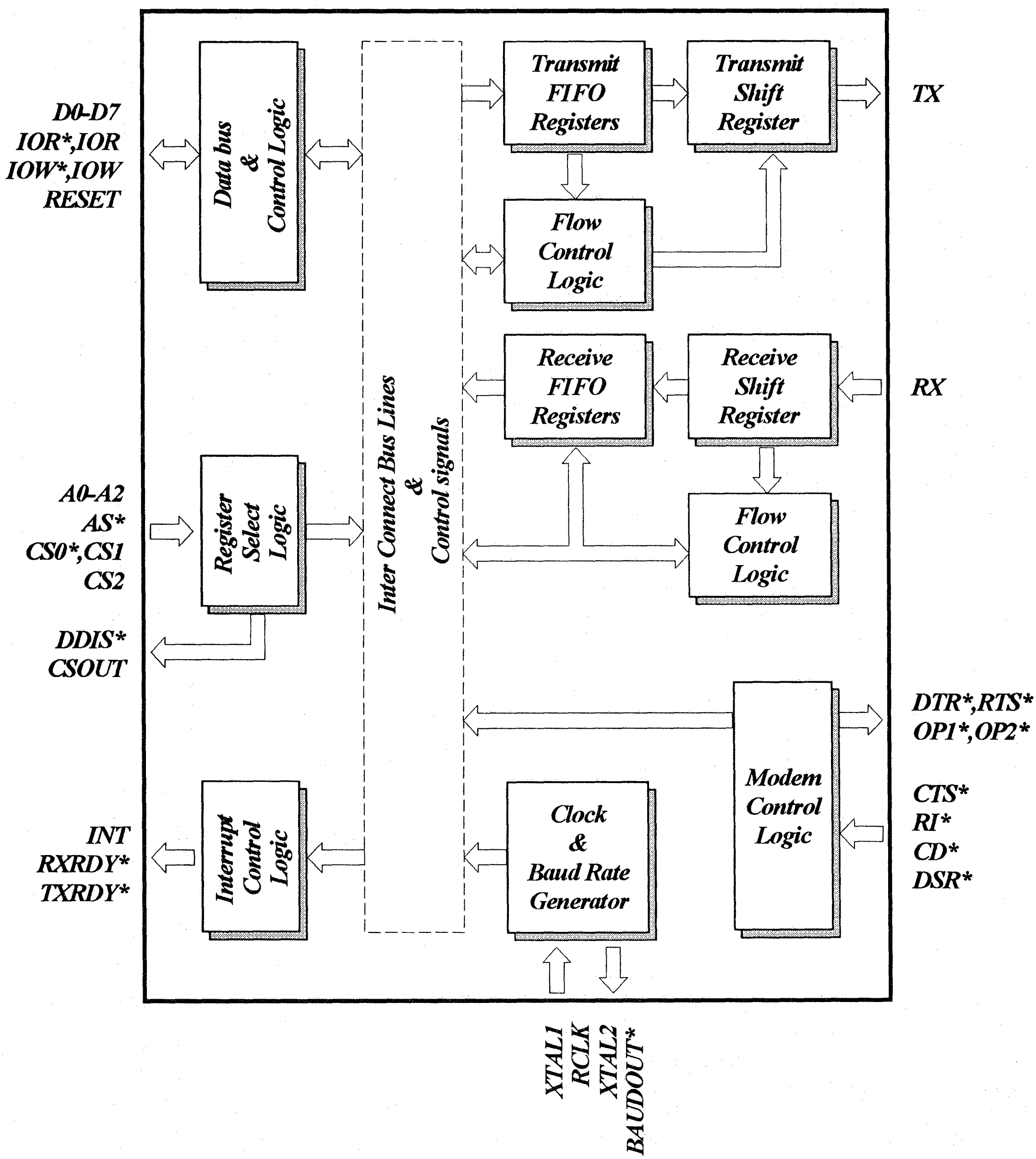


Plastic-DIP Package



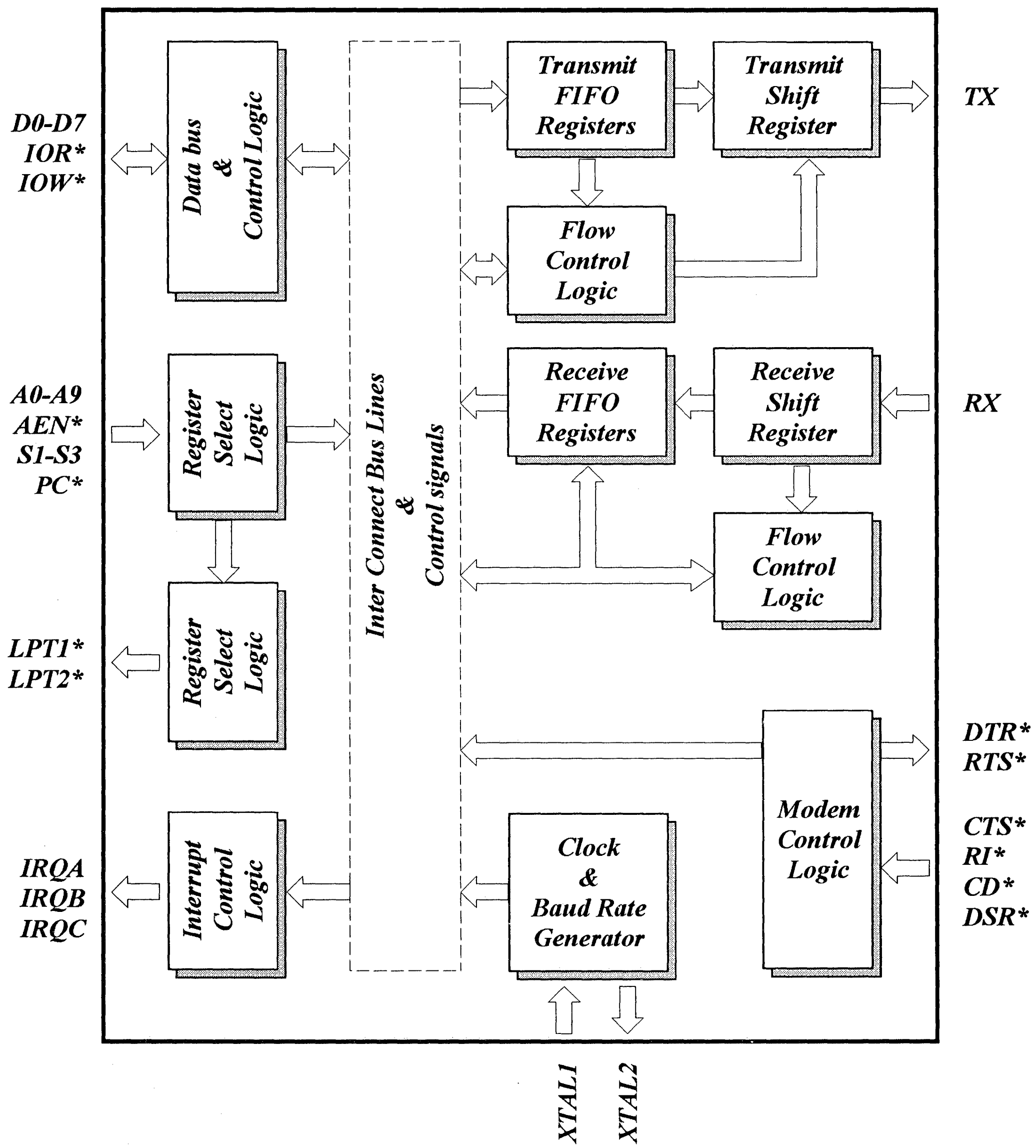
Patent pending

BLOCK DIAGRAM (Standard ST16C550 mode)



Patent pending

BLOCK DIAGRAM (Direct PC mode)



Patent pending

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
A9	-	1*	I	Address select line 9. When PC mode is selected, this pin is used as 10th address line to decode the standard COM1-4 ports.
D0-D7	1-8	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
S2/RCLK	9	10	I	Port select-2 or Receive clock input (dual function). When PC mode is selected the RCLK input is connected internally to BAUDOUT* output pin and S2 is used to select one of the ComPort addresses (Com1-4). During STD mode operation, this pin is used as external clock input to the ST16C650 receiver section.
RX	10	11	I	Serial data input. The serial information (data) received from serial port to ST16C650 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loop-back mode the RX input is disabled from external connection and connected to the TX output internally.
A4	-	12*	I	Address select line 4. When PC mode is selected, this pin is used as 5th address line to decode the standard COM1-4 ports.
TX	11	13	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loop-back mode or when the transmitter is disabled.
A5/CS0	12	14	I	Address line 5 or Chip select-1 (dual function). During the PC mode operation, this pin is used as 6th address line to decode the standard COM1-4 ports. During STD mode this pin acts as active high chip select input pin.
A6/CS1	13	15	I	Address line 6 or Chip select-2 (dual function). During the PC mode operation, this pin is used as 7th address line to decode the standard COM1-4 ports. During STD mode this pin acts as active high chip select input pin

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
A7/CS2*	14	16	I	Address line 7 or Chip select -3 (dual function). During the PC mode operation, this pin is used as 8th address line to decode the standard COM1-4 ports. During STD mode this pin acts as active low chip select input pin.
BAUD/LPT1*	15	17	O	Baud rate generator clock output or LPT1 decode address (378 Hex) (dual function). This output provides the 16X clock of the internal selected baud rate during standard mode. RCLK pin is connected externally to BAUDOUT* pin to provide receive clock when STD mode is selected. This pin internally is connected to RCLK input and address 378 Hex is decoded when PC mode is selected.
XTAL1	16	18	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	19	O	Crystal input 2 or buffered clock output. See XTAL1. External 1 MW resistor is required to connect between XTAL1 and XTAL2 pins.
IOW*	18	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
A8/IOW	19	21	I	Address 8 or Write strobe (dual function). During the PC mode operation, this pin is used as 9th address line to decode the standard COM1-4 ports. During STD mode this pin functions as Write strobe (active high). Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C650 during write operation.
GND	20	22	O	Signal and power ground.
S1	-	23*	I	Port select-1. S1 is used to select one of the ComPort addresses (Com1-4).
IOR*	21	24	I	Read strobe. (active low) A low level on this pin transfers

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
				the contents of the ST16C650 data bus to the CPU.
A3/IOR	22	25	I	Address line 3 or Read strobe (dual function). When PC mode is selected, this pin is used as 4th address line to decode the standard COM1-4 ports. During STD mode operation this pin is used as Read strobe. Same as IOR*, but it is used as active high Read strobe. Note that only an active IOR* or IOR input is required to transfer data from ST16C650 to CPU during read operation.
DDIS*/LPT2*	23	26	O	Drive disable or LPT2 decoded address (278 Hex) (dual function). (active low) This pin goes low when the CPU is reading data from the ST16C650 to disable the external transceiver or logic's during STD mode. During PC mode, LPT2 address is decoded.
IRQC/TXRDY*	24	27	O	IRQ-C Interrupt (three state) or Transmit ready (dual function). Three state interrupt output during PC mode and Transmit ready during STD mode. When STD mode is selected this pin goes high when the transmit FIFO of the ST16C650 is full. See INTA/INT description for IRQ-C operation.
AEN*/AS*	25	28	I	Address enable or Address strobe (dual function). During PC mode operation Valid COM 1-4 ports are decoded when this pin goes low. A low on this pin During STD mode latches the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	29	I	Address select line 2. To select internal registers.
A1	27	30	I	Address select line 1. To select internal registers.
A0	28	31	I	Address select line 0. To select internal registers.
IRQB/RXRDY*	29	32	O	IRQ-B Interrupt (three state) or Receive ready (dual function). Three state interrupt output during PC mode and Receive ready during STD mode. During the STD mode

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
				operation this pin goes low when the receive FIFO is full. See INTA/INT description for IRQ-B operation.
IRQA/INT	30	33	O	IRQ-A Interrupt (normal, three state or open source) or Interrupt output (triple function active high). During PC mode operation, this pin is activated when MCR Bit-3 is set to "1" and enabled by the interrupt enable register. whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected. During the STD mode operation three state mode is disabled and functions as active IRQ-A. Multiple ST16C650 interrupts can be connected to form a wired "Ored" function by setting the MCR bit-5 to "1" and connecting a 450 Ω resistor to ground.
SEL	-	34*	I	Mode select (pulled-up). PC mode is selected by tying this pin to GND and STD mode is selected when this pin is left open or tied to VCC.
S3/OP2*	31	35	I/O	Select-3 or User defined output (dual function). ComPort address select 1-4 when PC mode is selected and general purpose output when STD mode is selected. See bit-3 modem control register (MCR bit-3).
RTS*	32	36	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation it is not enabled via EFR Bit-6.
DTR*	33	37	O	Data terminal ready. (active low) To indicate that ST16C650 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	38	O	User defined output. See bit-2 of modem control register

 Patent pending

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
				(MCR bit-2).
RESET	35	39	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	40	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation if it is not enabled via EFR Bit-7.
DSR*	37	41	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	38	42	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI*	39	43	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	44	I	Power supply input.

*Have internal pull-up resistor on inputs

DESCRIPTION OF NEW FEATURES

The ST16C650 is designed to upgrade the existing 16C550 market. It provides additional features to reduce the software over-head, external glue logic, operating and stand-by current, and maintain the 16C550 software compatibility with existing software's.

After reset ST16C650 is down-ward compatible with ST16C450 and ST16C550 except it provides 32 bytes of data FIFO (when ST16C550 mode is enabled) instead of 16 bytes. All other additional features are available through special function register. The 40 pin Dip package offers the software/Hardware flow control, sleep mode, selectable transmit trigger levels, and two selectable baud rate generators. The 44 pin PLCC package offers all the above features with selectable dual foot print (direct PC connect), two additional three state interrupt lines, and one selectable open source interrupt output to "Or" other ST16C650 interrupt outputs to reduce the number of interrupt lines.

Patent pending

When direct PC mode is selected (44 pin PLCC package only), the external glue logic which is used to decode the COM-1 (3F8-3FF), COM-2 (2F8-2FF), COM-3 (3E8-3EF), and COM-4 (2E8-2EF) and select the proper interrupt lines have been implemented within the ST16C650. The ST16C650 provides Three selectable pins to select the desired ports and interrupts for automatic configurations. In addition to these addresses the ST16C650 decodes two additional addresses for LPT-1 (378-37F, printer port-1), and LPT-2 (278-27F, printer port-2) via OP2 and Baudout pins. These address decodes are used for IBM PC or compatible computers serial and parallel ports. During Direct connect mode all three interrupts functions are three state interrupts, to activate the interrupts MCR bit-3 should be set to "1".

FUNCTIONAL DESCRIPTIONS

The 32 bytes data FIFO's are enabled when user writes to the ST16C550/ST16C650 FIFO control register. With standard 16C550 parts, the user can only set receive trigger levels but not transmit trigger level. The ST16C650 provides independent trigger levels for both receiver and transmitter. To be compatible with ST16C550, 1 bytes transmit trigger level is selected after reset. Note that user can write to transmit trigger levels but activation will not take place till ST16C650 special mode is selected (EFR bit-4 is set to "1"). The ST16C650 is designed to work with high speed modems and shared network environments, that requires fast processing time. By increasing number of characters in the FIFO, networking units can handle more data within same time. Example: ST16C550 with 16 bytes of data, 115.2k and 8 bits wide word and one stop bit, will take 1.52 ms to transmit 16 bytes of data. But with 32 bytes of data buffer it will take 3.05 ms. This will gives additional time for the CPU to process other applications and reduce the interrupt servicing time.

The contents of the Xon-1,2 and Xoff 1,2 are reset to "0" values and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions.

When single Xon/Xoff characters are selected, ST16C650 compares the incoming data with these values and controls the transmission, these characters are not stacked in data buffer or FIFO. Special case is provided to detect the special character and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0-3).

Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the ST16C650 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

RTS pin will be forced to high state regardless of it's original state when receive FIFO reaches to the programmed trigger level. RTS pin resumes it original state after content of the data buffer (FIFO) drops below the next lower trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions the ST16C650 will accept additional data to fill the unused transmit and receive FIFO locations.

Special interrupt modes have been added to monitor the hardware and software flow conditions. These are the IER bits 5-7.

The ST16C650 is designed to operate with low power consumption, special sleep mode has been added to stop the clock and reduce the power consumption when it is not used (Green PC). When EFR bit-4 and IER bit-4 are enabled (set to "1"), the ST16C650 enters into sleep mode and resumes it's normal operation when a data is received or state of the modem input pins changes or it is set to transmit data. The ST16C650 stays in this mode till it is disabled.

Special care should be considered for the following interrupt conditions and handling them. After reset if transmitter interrupt is enabled, ST16C650 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS have lowest interrupt priority.

The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition next priority interrupt level will be shown. There are two interrupt conditions that have same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters are reached the programmed trigger level, in this case the ST16C650 FIFO holds equal or more characters than the trigger level. After reading block of data, user can check the LSR bit-0 for additional characters.

Note that, receive time out is functional only in ST16C550/650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Due to number of active simultaneous interrupt limitations in PC and compatibles, ST16C650 offers share interrupt out by setting MCR bit-5 to "1". If this mode is selected, it is required to connect 200-500 ohm resistor between the INTA pin to Ground. Note that other interrupts (INTB, INTC) will be inactive during this mode.

Dual baud rate generator is provided to maintain the 16C550 compatibility and provide higher data rate when it is needed. Example 14.4k to 19.2k modems requires to have 57k to 115.2k data rate and 28.8k modem requiems to have 230.4K. The 16C550 compatible parts can only offer 115.2k to maintain the software compatibility. The ST16C650 utilizes 7.32 MHz crystal/clock and provide 16C550 compatible data rate and higher. ST16C550 and ST16C650 baud rate generator tables can be selected is setting and resetting the MCR bit-7.

The ST16C650 transmit trigger level, provides additional flexibility to the user for block mode operation. In ST16C550/650 mode LSR bits 5-6 gives indication that transmitter is empty or not, but there is no mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FCR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the ST16C650 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like ST16C450 mode except it can receive and transmit 32 bytes of characters. When DMA mode "1" is activated, user takes the advantage of the block mode operation. In this mode, transmitter/receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or over receive trigger level. Note that since ST16C550 does not have transmit trigger levels, the default trigger level in the ST16C650 is set to 1 bytes (trigger level "0").

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	***0***	***0***	***LSB of Divisor Latch***	***LSB of Divisor Latch***
0	***0***	***1***	***MSB of Divisor Latch***	***MSB of Divisor Latch***
0	***1***	***0***	***Enhanced Feature Register***	***Enhanced Feature Register***
1	***0***	***0***	***Xon-1 Word***	***Xon-1 Word***
1	***0***	***1***	***Xon-2 Word***	***Xon-2 Word***
1	***1***	***0***	***Xoff-1 Word***	***Xoff-1 Word***
1	***1***	***1***	***Xoff-2 Word***	***Xoff-2 Word***

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register, Xon 1,2 and Xoff 1,2 are accessible only when LCR is set to "BF"

ST16C650 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0/ CTS interrupt	0/ RTS interrupt	0/ Xoff interrupt	0/ Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFO's enabled	0/ FIFO's enabled	0/ RTS, CTS	0/ Xoff	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	Clock select	0/ IRRT enable	INTA type select	loop back	OP2*/ IRQx enable	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***
0 1 0	***EFR***	***Auto CTS***	***Auto RTS***	***Special Char. select***	***Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7***	***Cont-3 Tx,Rx Control***	***Cont-2 Tx,Rx Control***	***Cont-1 Tx,Rx Control***	***Cont-0 Tx,Rx Control***

These registers are accessible only when LCR bit-7 is set to "1". <u>Enhanced Feature Register, Xon 1,2 and Xoff 1,2 are accessible only when LCR is set to "BF"</u>

REGISTER FUNCTIONAL DESCRIPTIONS

OPERATING MODE.

The ST16C650 provides pin selectable interface for existing 16C550 and new designs.
PC mode can be selected by tying the SEL pin to GND. When PC mode is selected the ST16C650 eliminates the external address decode logic (glue logic) for COM1-4 and jumper setting for IRQ3, IRQ4 or IRQn. The ST16C650 can be configured as follows:

S3 S2 S1	Address	ComPort	IRQ
0 0 0	3F8-3FF	COM-1	IRQB**
0 0 1	2F8-2FF	COM-2	IRQC**
0 1 0	3E8-3EF	COM-3	IRQB**
0 1 1	2E8-2EF	COM-4	IRQC**
1 0 0	3F8-3FF	COM-1	IRQA**
1 0 1	2F8-2FF	COM-2	IRQA**
1 1 0	3E8-3EF	COM-3	IRQA**
1 1 1	2E8-2EF	COM-4	IRQA**

** All interrupt outputs are inactive (three state mode) except the selected address.

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C650 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C650 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baud-out* is equal to 16X of transmission baud rate (Baud-out*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE MCR BIT-7=1	BAUD RATE MCR Bit-7=0	16 x CLOCK DIVISOR "Decimal"
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2K	24
7200	28.8K	16
9600	38.4k	12
19.2K	76.8k	6
38.4K	153.6k	3
57.6K	230.4k	2
115.2K	460.8k	1

HARDWARE FLOW CONTROL OPERATION.

When hardware flow control operation is enabled, the ST16C650 monitors the CTS* pin for transmit operation and receiver trigger level for RTS* operation. When CTS* changes state from low to high, the ST16C650 suspends the transmission operation as soon as complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as CTS* pin goes low. RTS* pin will be forced to high state when receiver FIFO reached to the programmed trigger level. RTS* will go low when Receive Holding Register is below next lower trigger level. The ST16C650 will accept additional data when transmission is suspended during hardware flow control till all locations are filled.

SOFTWARE FLOW CONTROL

When software flow control operation is enabled, the ST16C650 will compare the two sequential receive data with Xoff-1,2 programmed characters. When these characters matched correctly, the ST16C650 will halt the transmission after finishing the transmission of the complete character. The receive ready, Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After the recognition of the Xoff characters the ST16C650 will compare next two incoming characters with Xon-1,2 characters. The ST16C650 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The ST16C650 will send Xoff-1,2 characters as soon as received data passed the programmed trigger level. The ST16C650 will transmit programmed Xon-1,2 characters as soon as receive data reached to the next lower trigger level.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0= disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0= disable the transmitter empty interrupt.
1= enable the transmitter empty interrupt.

IER BIT-2:
0= disable the receiver line status interrupt.
1= enable the receiver line status interrupt.

IER BIT-3:
0= disable the modem status register interrupt.

1= enable the modem status register interrupt.

IER BIT -4:
0= disable sleep mode.
1= enable sleep mode. The ST16C650 enters into power down mode and external clock or oscillator ciruit is disabled. Any change of state on the RX, RI*, CTS*, DSR*, and CD* pins start the ST16C650. The ST16C650 will not lose the programmed bits when sleep mode is activated or deactivated. The ST16C650 will not enter in sleep mode if any interrupt is pending.

IER BIT-5:
0= disable the received Xoff interrupt.
1= enable the received Xoff interrupt. The ST16C650 issues an interrupt when Xoff characters are received and correctly matched with Xoff 1,2 words.

IER BIT-6:
0= disable the RTS interrupt.
1= enable the RTS interrupt. The ST16C650 issues interrupt when RTS pin changes state from low to high.

IER BIT-7:
0= disable the CTS interrupt.
1= enable the CTS interrupt. The ST16C650 issues interrupt when CTS pin changes state from low to high.

INTERRUPT STATUS REGISTER (ISR)

The ST16C650 provides six level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C650 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D5	D4	D3	D2	D1	D0	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS change of state

ISR BIT-0:
0= an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1= no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-5:
These bits are enabled when EFR bit-4 is set to "1". ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that CTS, RTS have been receiced or issued. Note that the ISR bit-4 will stay "1" till Xon characters are recieved.

ISR BIT 6-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C650 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0= disable the transmit and receive FIFO.
1= enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0= No change.
1= Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0= No change.
1= Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0= No change.
1= Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C650 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C650 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C650 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C650 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
These bits are used to set the trigger level for the transmit FIFO interrupt. The ST16C650 will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	FIFO trigger level
0	0	16
0	1	8
1	0	24
1	1	30

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	8
0	1	16
1	0	24
1	1	28

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0= no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0= ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0= normal operating condition.
1= forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable (DLAB).
0= normal operation.

1= Divisor latch and Enhanced Feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0= force DTR* output to high.
1= force DTR* output to low.

MCR BIT-1:
0= force RTS* output to high.
1= force RTS* output to low.
RTS* is used as hardware flow control signal when enabled via EFR bit-6. RTS* goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control. functiuons normally when hardware flow control is disabled.

MCR BIT-2:
0= set OP1* output to high.
1= set OP1* output to low.

MCR BIT-3:
0= set OP2* output to high (STD mode). Forces INTx outputs to three state mode during PC mode selection.
1= set OP2* output to low (STD mode). Sets the INTx outputs to active mode during PC mode selection

MCR BIT-4:
0= normal operating mode.
1= enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT-5:
0= Active or three state interrupt output.
1= Open source interrupt output. Required external resistor from this pin to ground. This mode is provided for share interrupts.

MCR BIT-6:
0= Standard UART receive and transmit input / output.
1= Infrared receive and transmit input / output. The TX output and RX input is converted to Infrared encoder/decoder output/input format. TX output goes low when this bit is set to "1".

MCR BIT-7:
0= Normal or divide by one clock input. Standard ST16C550 baud rates can be selected when this bit is set to "0" and 1.8432 MHz crystal is used.
1= Divide by four clock input. Standard ST16C550 baud rates can be selected when this bit is set to "1" and 7.372 MHz crystal is used.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0= no data in receive holding register or FIFO.
1= data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0= no overrun error (normal).
1= overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0= no parity error (normal).
1= parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0= no framing error (normal).
1= framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0= no break condition (normal).
1= receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
It indicates that the ST16C650 is ready to accept a new character for transmission. In addition, it causes the ST16C650 to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set.

0= transmit holding register is not empty.
1= transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load upto 32 bytes of data to the ST16C650.

LSR BIT-6:
0= transmitter holding and shift registers are full.
1= transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0= normal.
1= at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C650 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C650 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C650 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C650 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.
CTS* functions as hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as complete character is transmitted.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C650 provides a temporary data register to store 8 bits of information for variable use.

ENHANCED FEATURE REGISTER (EFR)

Enhanced Features can be Enable/Disabled via this register.

EFR BIT 0-3:
Combinations of software flow control can be selected by programming this bits.

Cont-3	Cont-2	Cont-1	Cont-0	Tx, Rx software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2 : Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2 : Xoff1 and Xoff2 Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2

EFR BIT-4:
Enhanced interrupt control bit.
0= disables the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7. Standard ST16C550 mode.
1= enables the enhanced interrupt functions.

EFR BIT-5:
0= Normal.
1= Special character detect. ST16C650 compares the incoming receive data with Xoff-2 data. Up on correct match, the received data will be transferred to FIFO and ISR Bit-4 will be set to indicate detection of special character.

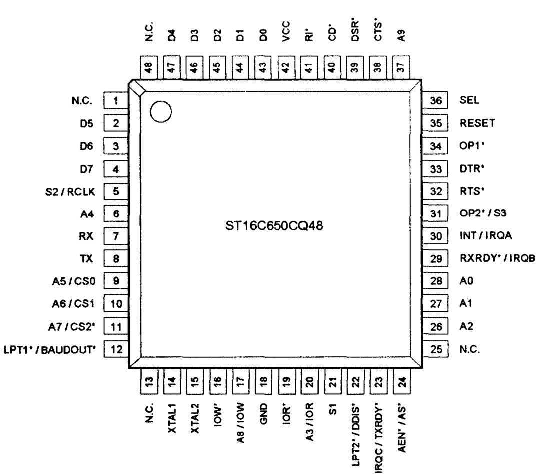
EFR BIT-6:
RTS* flow control.
0 = Normal. RTS* flow control is disabled. Standard ST16C550 mode.
1 = RTS pin goes high when receive FIFO's are reach to the programmed trigger level.

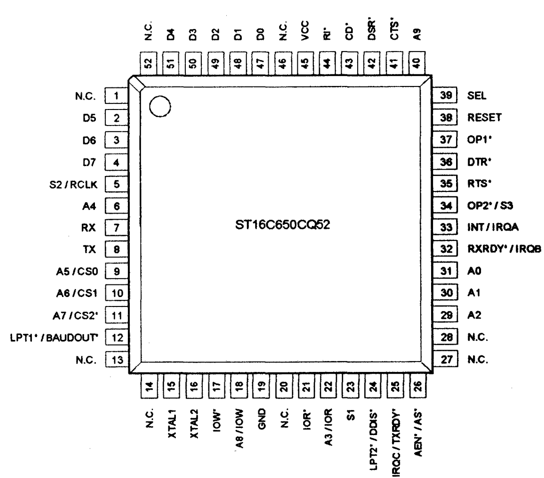
EFR Bit-7:
CTS* flow control.
0 = Normal. CTS* flow control mode is disabled. Standard ST16C550 mode.
1 = Transmission is resumed when low input signal is detected on the CTS* pin.

ST16C650 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7= input signals
FCR	FCR BITS 0-7=0
EFR	EFR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
RXRDY*	High (STD mode),/ Three state (PC mode)
TXRDY*	High (STD mode) / Three state (PC mode)
IRQn/NT	Low (STD mode) / Three state (PC mode)





Patent pending

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1 RClk		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1 RCLK		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

Note 1: Applicable only when AS* is tied low
* = Baud-out* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

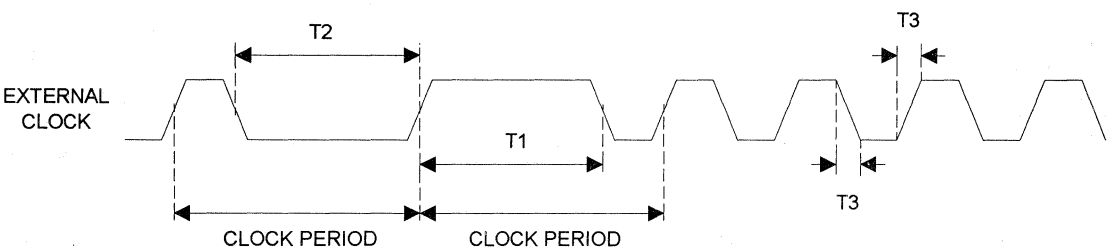
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

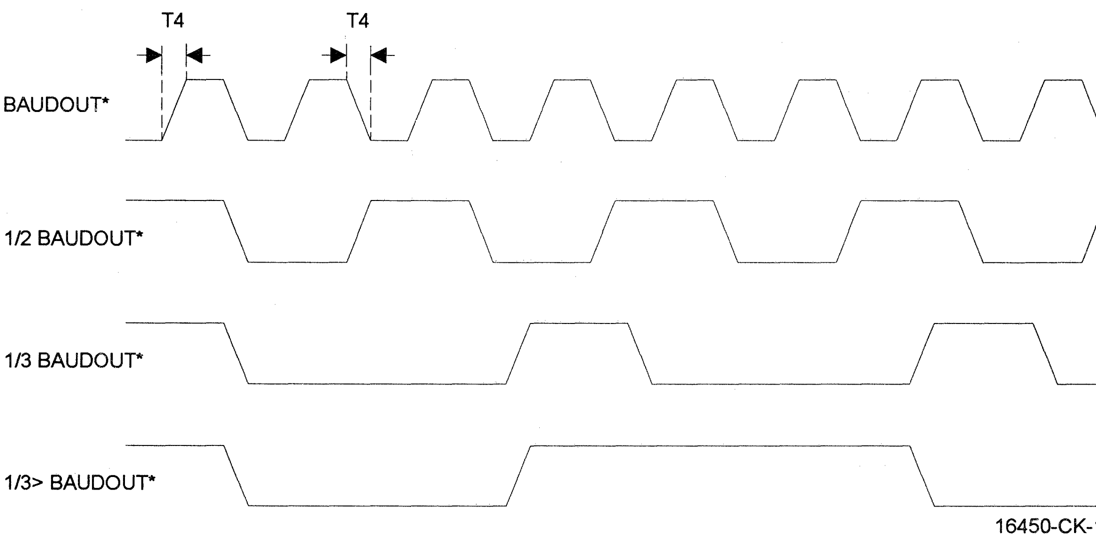
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current		1.3	2.5	mA	
V_{OP}	Operating voltage	3		5	V	
I_{SLP}	Avg sleep mode current		800	1	µA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	5		15	kΩ	*Marked pins

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

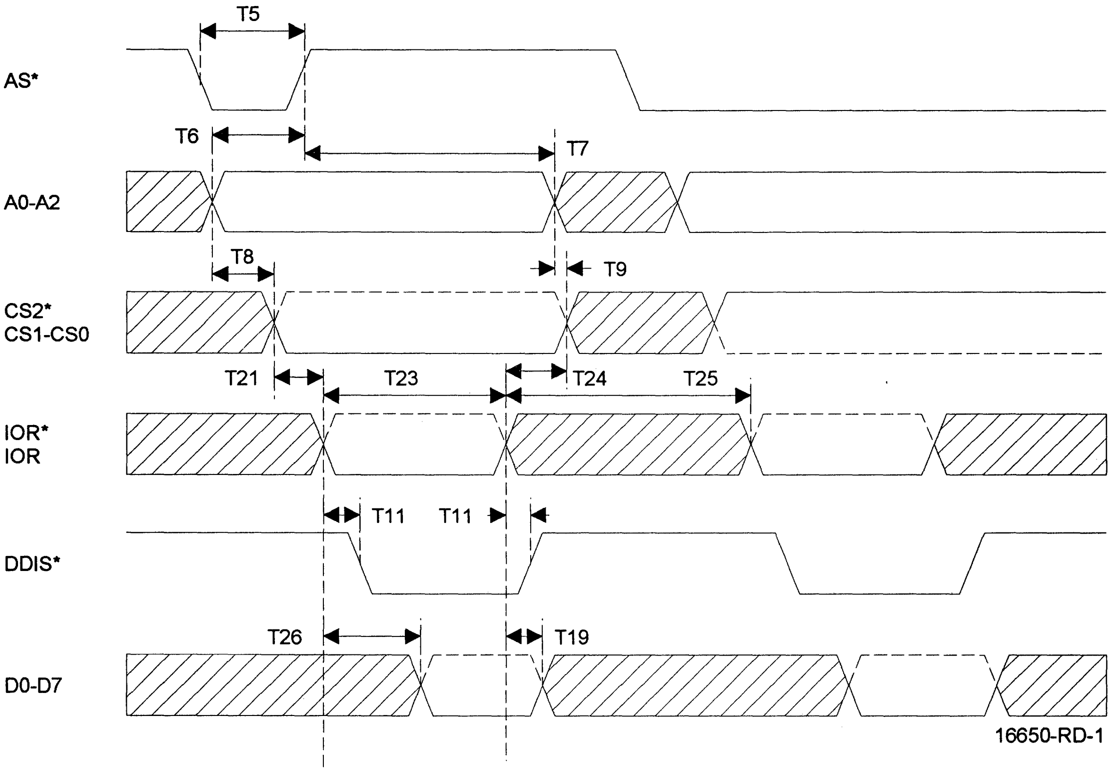
CLOCK TIMING



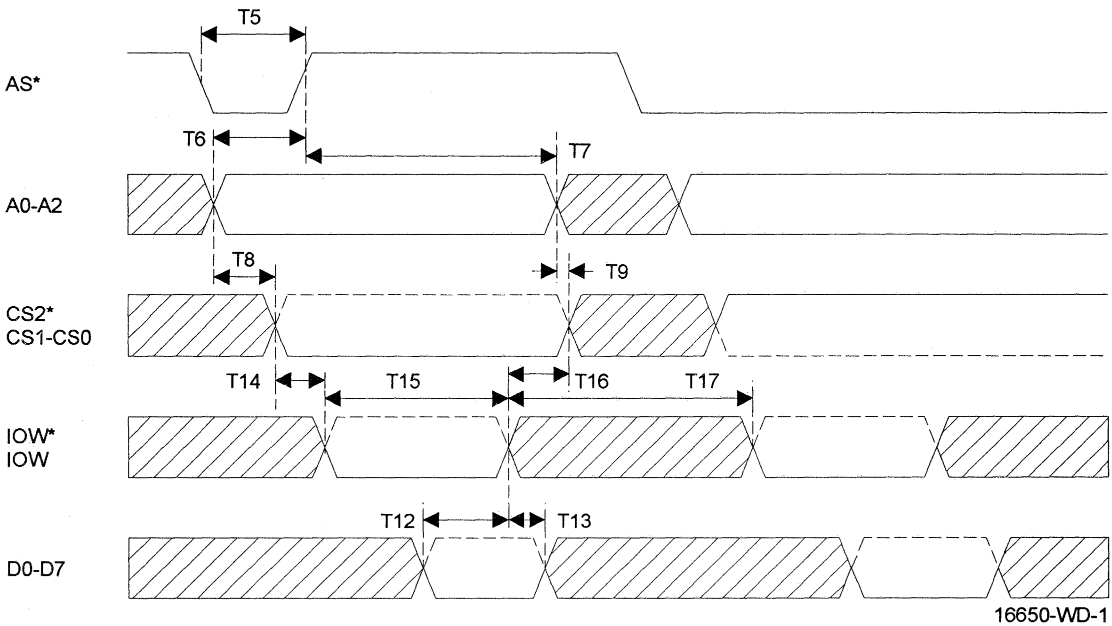
BAUDOUT* TIMING



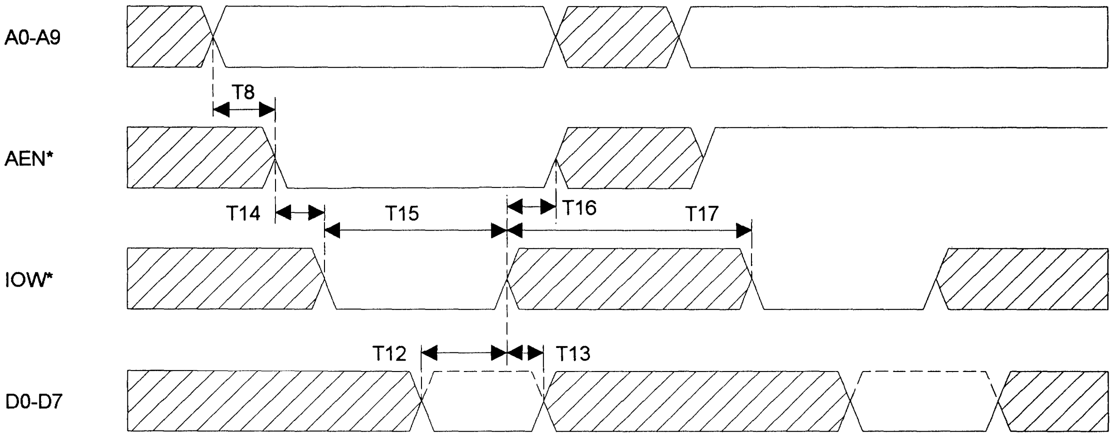
GENERAL READ TIMING



GENERAL WRITE TIMING

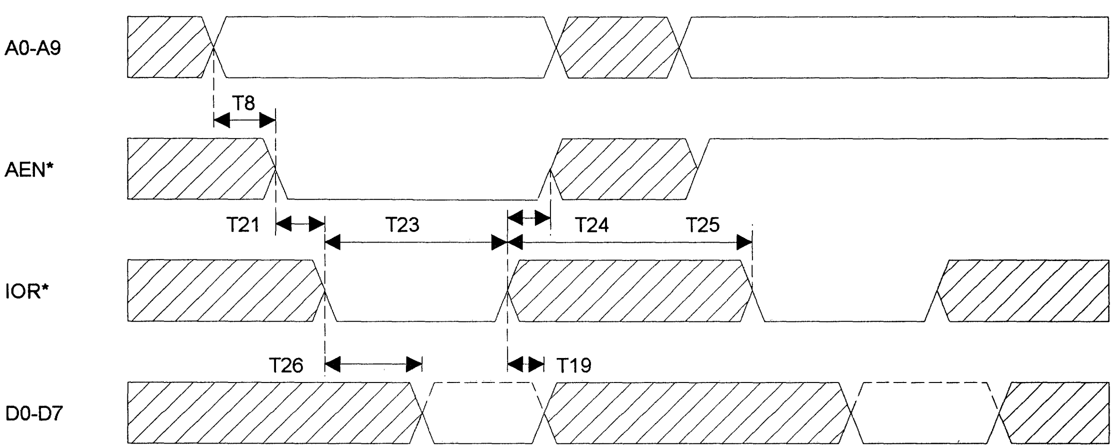


GENERAL WRITE TIMING (PC MODE)



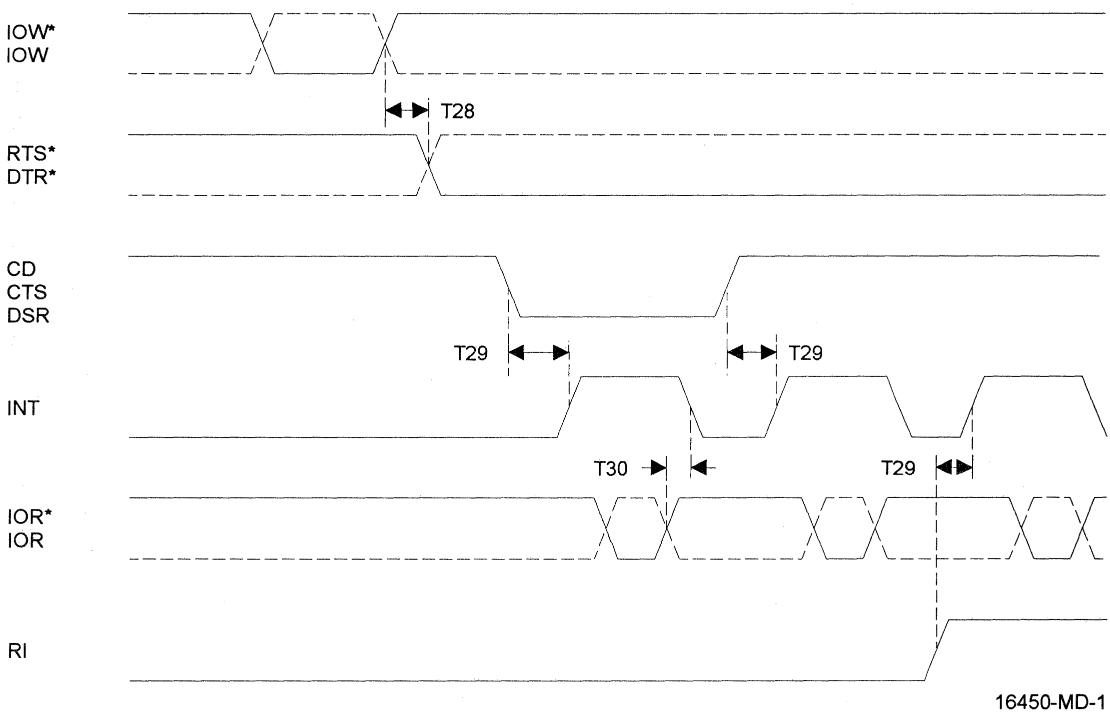
16650-WD-2

GENERAL READ TIMING (PC MODE)

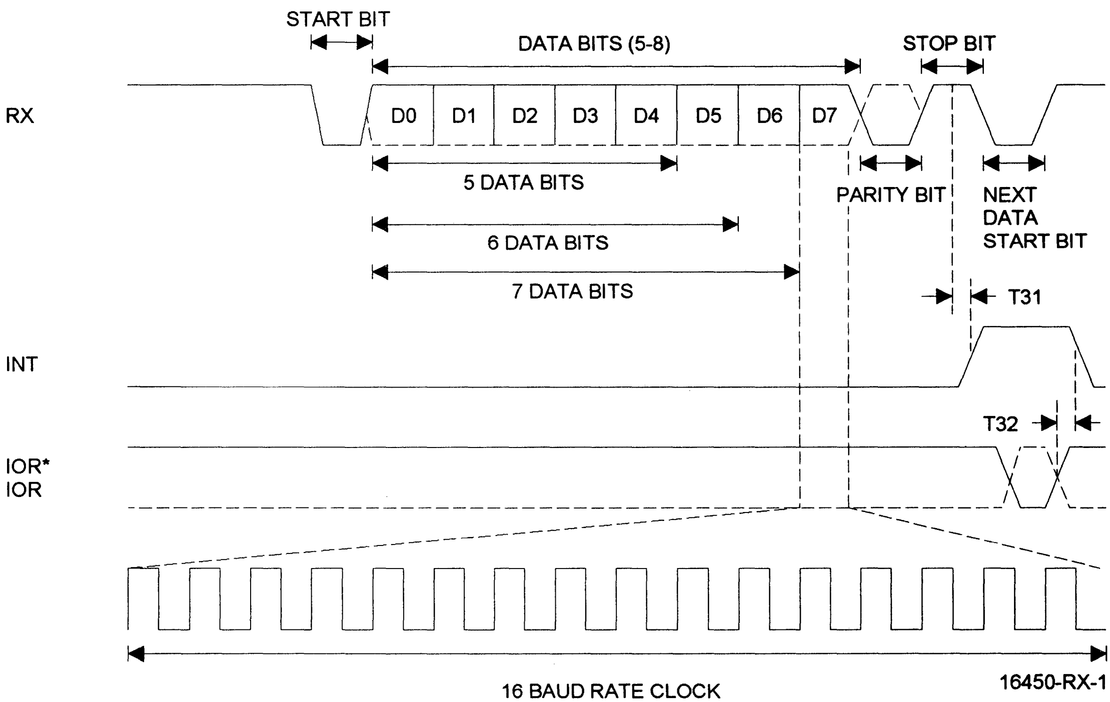


16650-RD-2

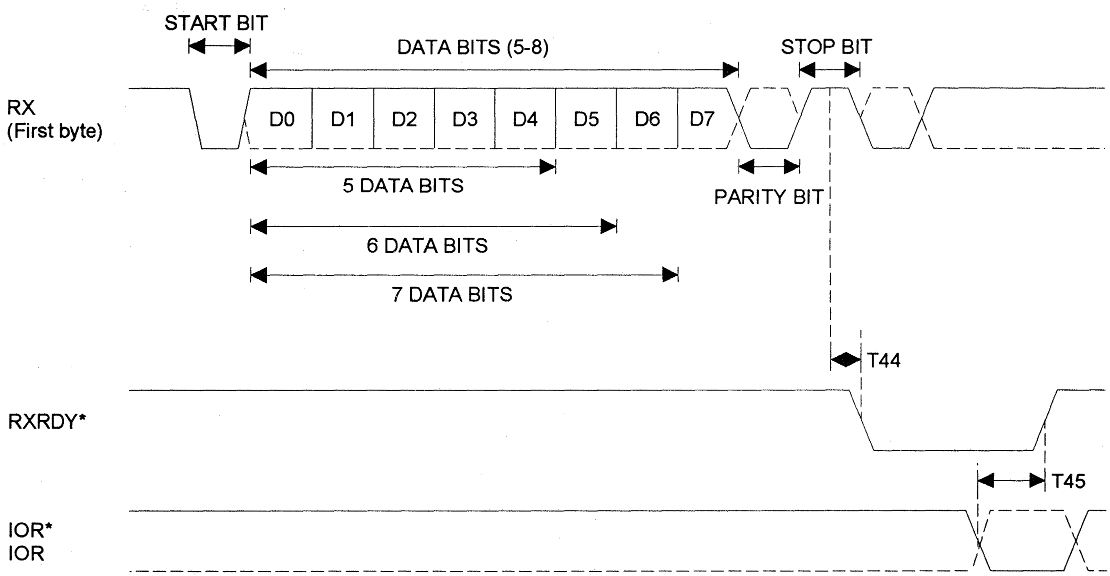
MODEM TIMING



RECEIVE TIMING

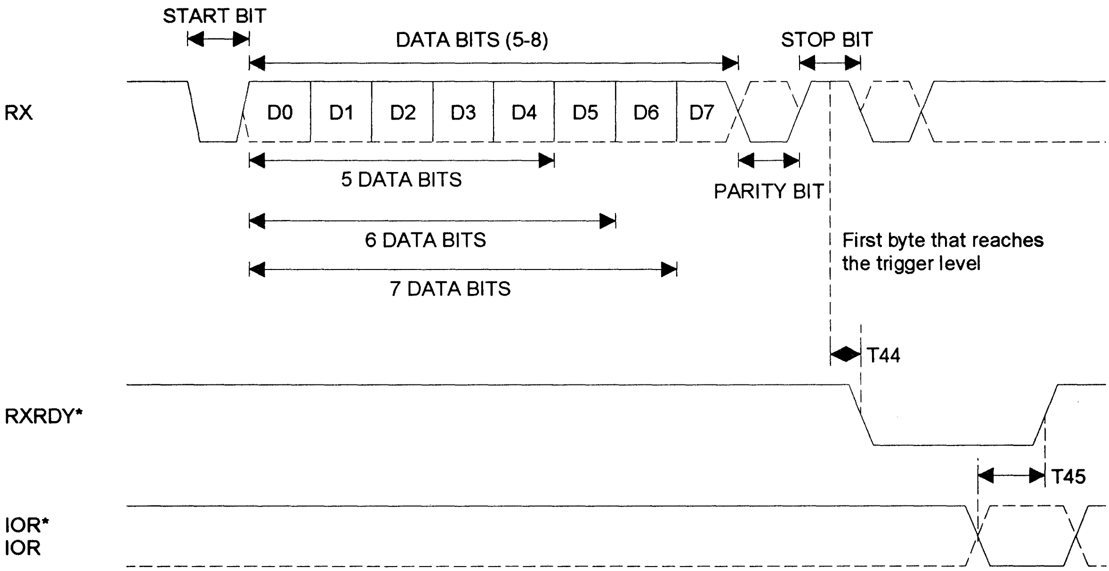


RXRDY TIMING FOR MODE "0"



16550-RX-2

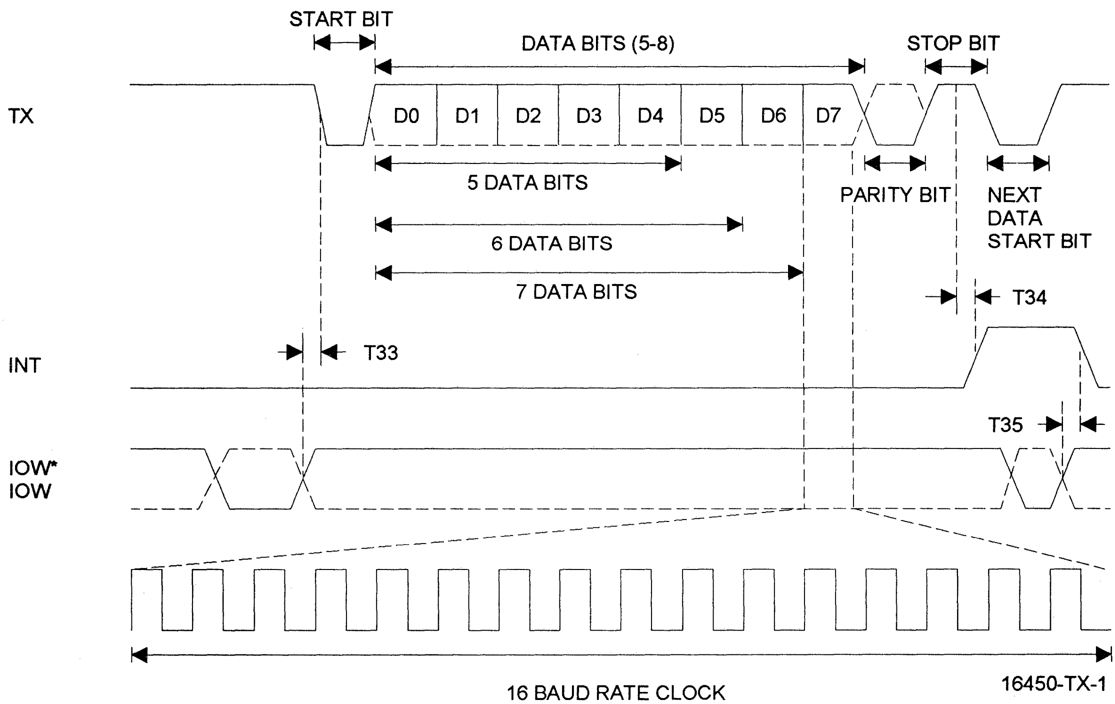
RXRDY TIMING FOR MODE "1"



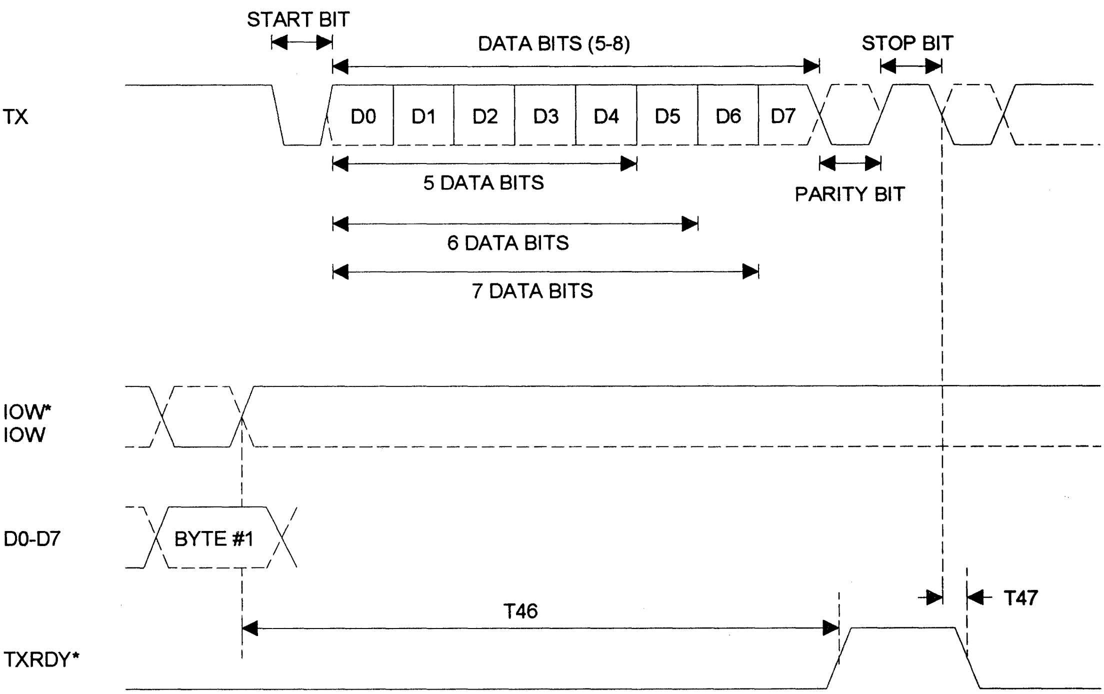
16550-RX-3

Patent pending

TRANSMIT TIMING

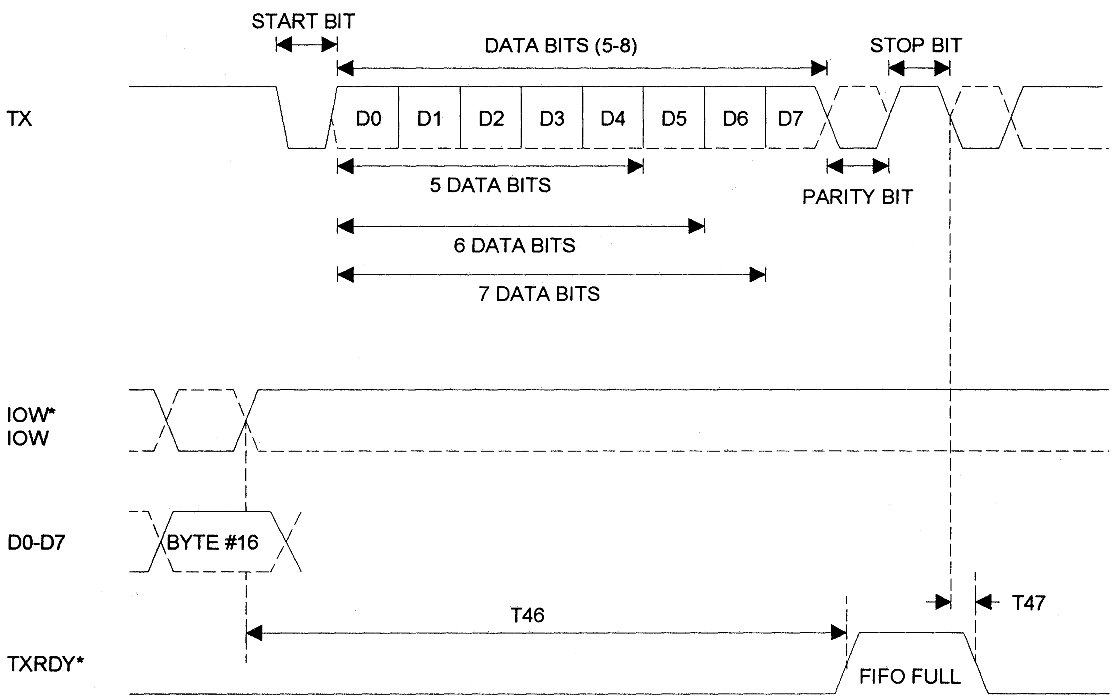


TXRDY TIMING FOR MODE "0"



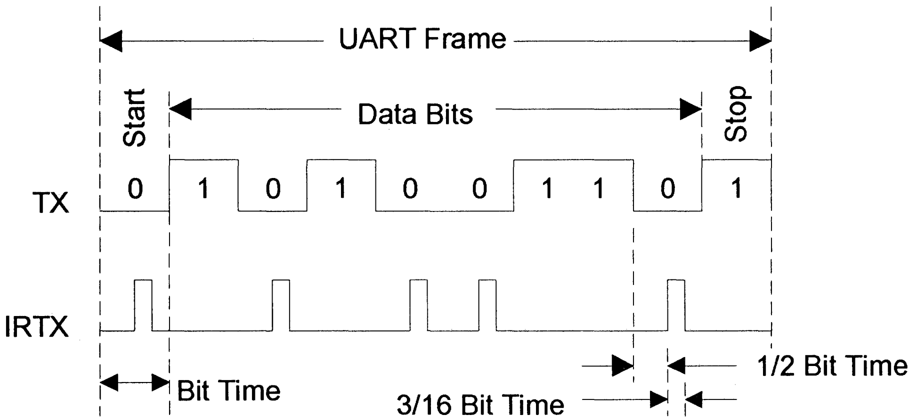
16550-TX-2

TXRDY TIMING FOR MODE "1"

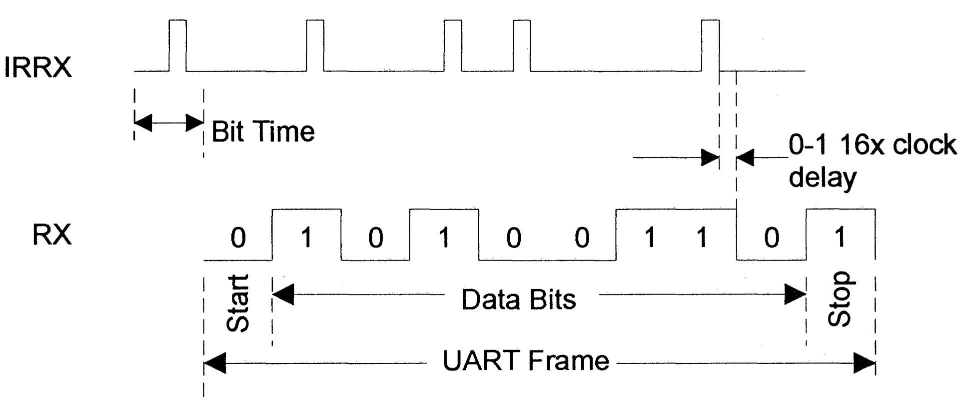


16550-TX-3

INFRARED TRANSMIT TIMING



INFRARED RECEIVE TIMING



16650-IR-1

STARTECH

An EXAR Company

Preliminary Information

ST16C654

Printed August 3, 1995

QUAD UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH 64 BYTES OF FIFO AND INFRARED ENCODER/DECODER

DESCRIPTION

The ST16C654 is a Quad universal asynchronous receiver and transmitter with 64 bytes of transmit and receive FIFO. ST16C654 provides dual foot print compatibility with ST16C554 and ST68C554. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

The ST16C654 is an improved version of the ST16C554 UART with deeper FIFO, software/ hardware flow control. The ST16C654 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C654 provides internal loop-back capability for on board diagnostic testing.

The ST16C654 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to ST16C454, ST16C554, ST16C554D, ST68C454, ST68C554
- 64 byte transmit FIFO
- 64 byte receive FIFO with error flags
- Software/Hardware flow control
- Programmable Xon/Xoff characters
- Sleep mode (800μA stand-by)
- Low operating current (1.5mA typ.)
- Independent transmit and receive control
- 460.8 kHz transmit/receive operation
- Selectable Transmit/Receive trigger levels
- Infrared receive and transmit, input / output.
- Independent MIDI interface

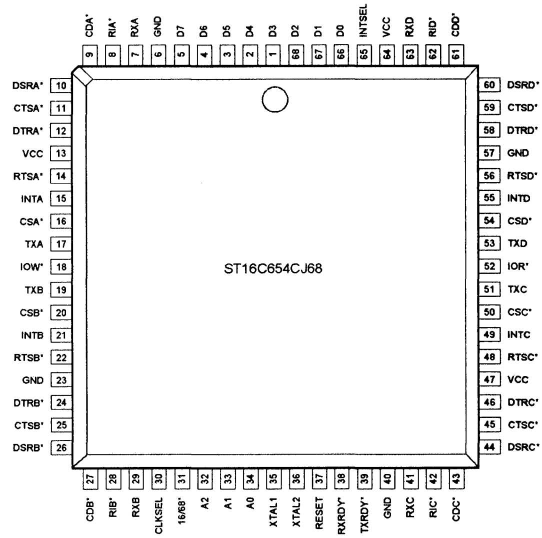
ORDERING INFORMATION

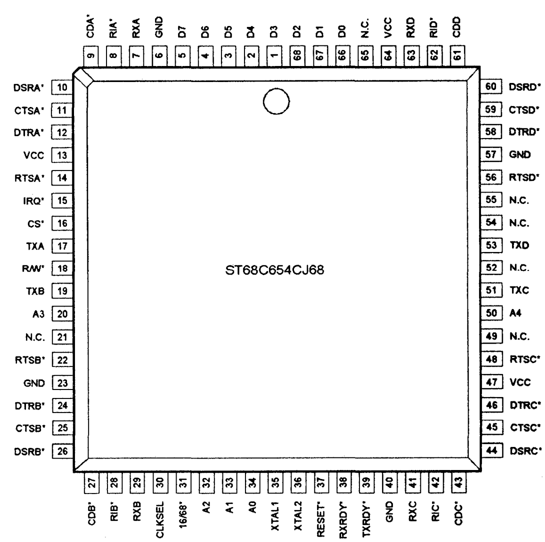
Part number	Package	Operating temperature
ST16C654CJ68	PLCC	0° C to + 70° C
ST16C654CQ64	QFP	0° C to + 70° C
ST16C654CQ100	QFP	0° C to + 70° C

*Industrial operating range are available

Rev. 1.0

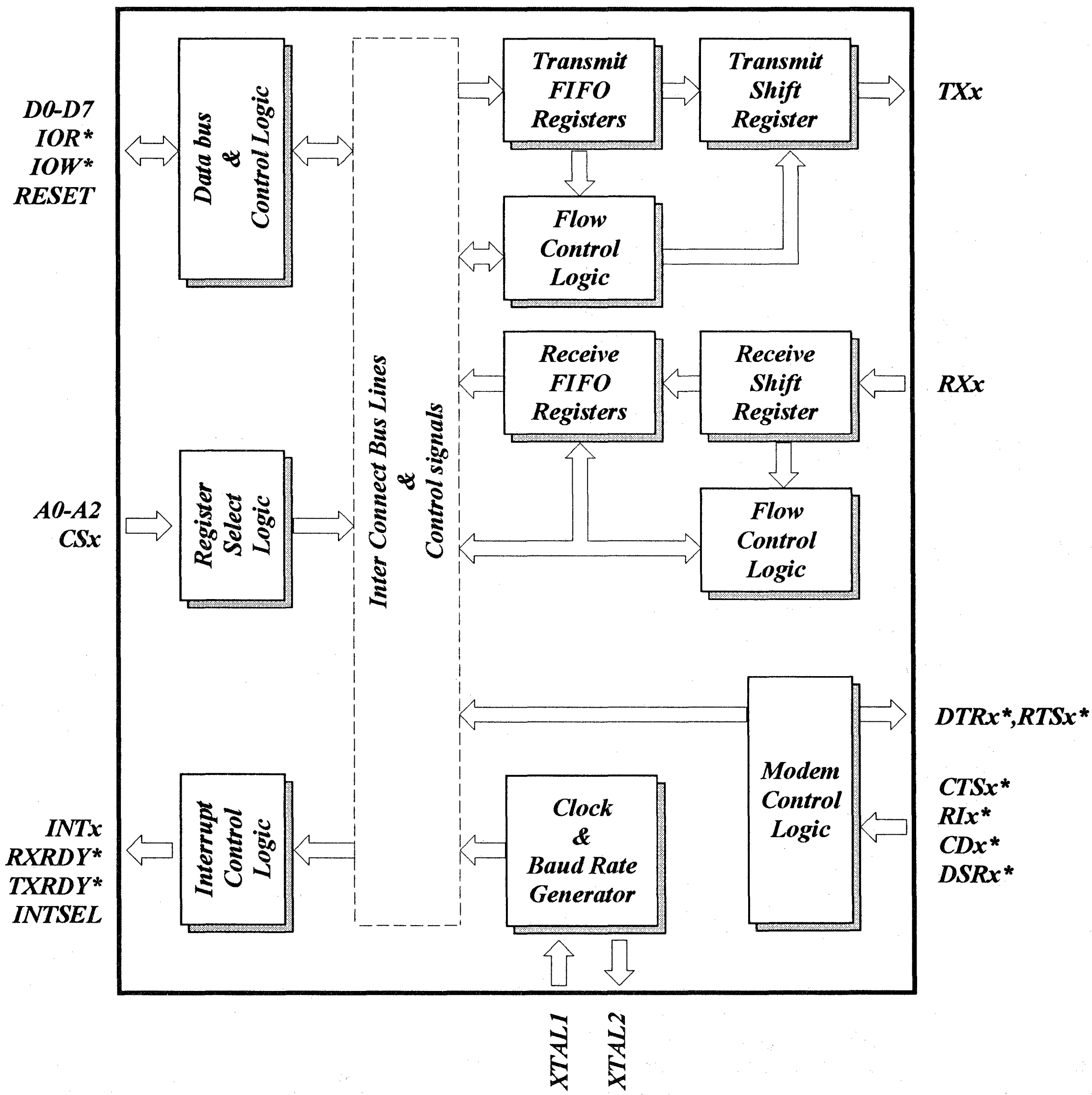
PLCC Package



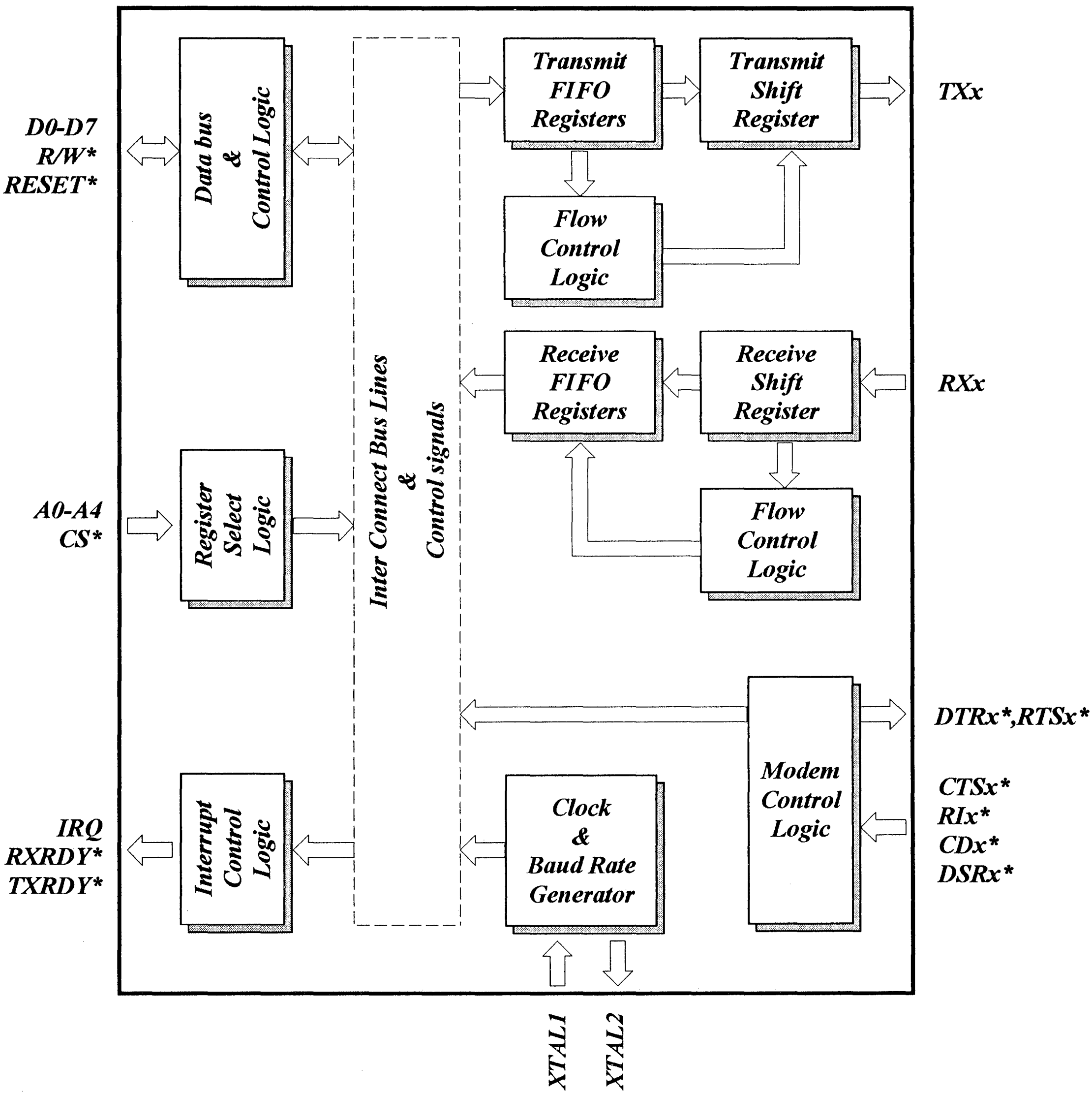


3

BLOCK DIAGRAM: ST16C654 MODE



BLOCK DIAGRAM: ST68C654 MODE



Patent pending

SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
D0-D7	66-5	88-95	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	97,34 47,85	I	Serial data input. The serial information (data) received from serial port to ST16C654 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	14,16 65,67	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
IRTX A-B IRTX C-D	- -	6,24 57,75	O	Serial IRda data output. The serial IRda data is transmitted via this pin with additional start , stop and parity bits. The IRTX will be held in mark (low) state during reset.
CS*	16	13	I	Chip select. (active low) This pin functions as chip select when 16/68* pin is connected to GND. All four UARTS will be selected when CS* is low. Each individual UART can be selected with A3-4 combinations. When 16/68* pin is connected to VCC or left open, this pin functions as CSA*.
CS* A-B CS* C-D	16,20 50,54	13,17 64,68	I	Chip select. (active low) A low at this pin enables the ST16C654 / CPU data transfer operation. Each UART sections of the ST16C654 can be accessed independently.
XTAL1	35	40	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
XTAL2	36	41	O	Crystal input 2 or buffered clock output. See XTAL1.
MIDICLK	-	42	I	Midi clock input. RXC and TXC can function as midi input / output port when an external midi clock is provided at this pin. MIDICLK can be connected to XTAL2 pin for normal operation.
CLKSEL	30	35	I	Default clock select. 1X or 1X/4 clock can be selected by connecting this pin to VCC or GND. 1X clock is selected when CLKSEL is connected to VCC and 1X/4 is selected when CLKSEL is connected to GND. The MCR bit-7 can override the default clock setup after reset when it is programmed to "1".
R/W*	18	15	I	Read/Write strobe. This pin acts as Read/Write strobe when 16/68* is connected to GND. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST16C654 selected register to CPU data bus. When 16/68* pin is connected to VCC or left open, this pin functions as IOW*.
IOW*	18	15	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	96,20 46,71	O	Signal and power ground.
IOR*	52	66	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C654 data bus to the CPU.
TXRDY*	39	45	O	Transmit ready. (active low) TXRDY* pin is the wire "OR-ed" function of all TXRDY* A-D.
TXRDY* A-B TXRDY* C-D	- -	5,25 56,81	O	Transmit ready. (active low) This pin goes when transmit FIFO of the ST16C654 is full. It can be used as a single or multi-transfer.
A3-A4	20,50	17,64	I	Address select line 3 and 4. When 16/68* pin is connected

Patent pending

SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
				to GND, combination of these pins will select individual UART's when CS* is low. When 16/68* is connected to VCC or left open, these pins function as CSB* and CSC*.
A2	32	37	I	Address select line 2. To select internal registers.
A1	33	38	I	Address select line 1. To select internal registers.
A0	34	39	I	Address select line 0. To select internal registers.
RXRDY*	38	44	O	Receive ready. (active high) RXRDY* pin is the wire "OR-ed" function of the all RXRDY* A-D.
RXRDY* A-B RXRDY* C-D	- -	100,31 50,82	O	Receive ready. (active high) This pin goes high when receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL	65	87	I	Interrupt type select. Enable /disable the interrupt three state function. Always active interrupt output can be selected by connecting this pin to VCC (MCR bit-3 does not have any effect on the interrupt output). The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is set to "1". This has no effect when 16/68* pin is connected to GND.
CSRDY*	-	76	I	FIFO ready register select. (active low) Content of the FIFORDY register can be read when this pin goes low. D0-D3 corresponds to inverted TXRDY* A-D, and D4-D7 correspond to RXRDY* A-D.
IRQ*	15	12	O	Interrupt output. (active low, open source) This pin goes low (when enabled by the interrupt enable register) when ever any of the four UART's issue interrupt. An external pull-up resistor is required to be connected to this pin. Function of the IRQ* changes to INTA when 16/68* pin is connected to VCC or left open.
INT A-B INT C-D	15,21 49,55	12,18 63,69	O	Interrupt output. (active high) This pin goes high (when

SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
				enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS* A-B RTS* C-D	14,22 48,56	11,19 62,70	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation unless hardware flow control is enabled.
DTR* A-B DTR* C-D	12,24 46,58	9,21 60,72	O	Data terminal ready. (active low) To indicate that ST16C654 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET* RESET	37	43	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time. When 16/68* is connected to GND, RESET functions as RESET*.
CTS* A-B CTS* C-D	11,25 45,59	8,22 59,73	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation unless hardware flow control is enabled
DSR* A-B DSR* C-D	10,26 44,60	7,23 58,74	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
16/68*	31	36	I	Intel or Motorola bus interface select. Functions of the IOR*,

SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
				IOW*, INT A-D, and CS* A-D are re-assigned with the state of this pin. When this pin is connected to VCC or left open, Intel bus interface is selected. When this pin is connected to GND, IOW* is re-assigned to R/W*, RESET is re-assigned to RESET*, IOR* is not used, and all INT A-D are wired "OR-ed" and used as open source IRQ output. This pin contains internal pull-up resistor.
CD* A-B	9,27	99,32		
CD* C-D	43,61	49,83	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI* A-B	8,28	98,33		
RI* C-D	42,62	48,84	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	13	10		
VCC	47,64	61,86	I	Power supply input.

DESCRIPTION OF NEW FEATURES

The ST16C654 is designed to upgrade the existing 16C550 market. It provides additional features to reduce the software over-head, external glue logic, operating and stand-by current, and maintain the 16C550 software compatibility with existing software's.

After reset ST16C654 is down-ward compatible with ST16C454 / ST68C454 and ST16C554 / ST68C554 except it provides 64 bytes of data FIFO (when ST16C550 mode is enabled) instead of 16 bytes. All other additional features are available through special function register. The ST16C654 offers the software/ Hardware flow control, sleep mode, selectable transmit trigger levels, and two selectable baud rate generators.

Separate clock input has been provided for MIDI applications. MIDICLK pin can be connected to XTAL2 pin for normal operation or an External MIDI clock oscillator for MIDI application.

Four independent Irda specified outputs are provided (100 QFP package only) for IR applications. These output are provided in parallel with regular asynchronous data output.

A separate FIFO ready register is provided to monitor the TXRDY* and RXRDY* of each individual UART's to reduce the polling time.

ST16C654 offers clock select pin for system / board designers to preset the baud rate table After reset. The CLKSEL pin selects the 1X or 1X/4 clock or internal baud rate generator. When CLKSEL is connected to the VCC pin the 1X clock is selected. 1X/4 clock is selected when CLKSEL is connected to GND.

FUNCTIONAL DESCRIPTIONS

The 64 bytes data FIFO's are enabled when user writes to the ST16C550/ST16C554 FIFO control register. With standard 16C550 parts, the user can only set receive trigger levels but not transmit trigger level. The ST16C654 provides independent trigger levels for both receiver and transmitter. To be compatible with ST16C550, 1 bytes transmit trigger level is selected after reset. The ST16C654 is designed to work with high speed modems and shared network environments, that requires fast processing time. By increasing number of characters in the FIFO, networking units can handle more data within same time. Example: ST16C550 with 16 bytes of data, 115.2k and 8 bits wide word and one stop bit, will take 1.52 ms to transmit 16 bytes of data. But with 64 bytes of data buffer it will take 6.1 ms. This will gives additional time for the CPU to process other applications and reduce the interrupt servicing time.

The contents of the Xon-1,2 and Xoff 1,2 are reset to "0" and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions. When single Xon/Xoff characters are selected, ST16C654 compares the incoming data with these values and controls the transmission, these characters are not stacked in data buffer or FIFO. When any Xon (MCR bit-5) bit is set, the ST16C654 will resume the operation after receiving any character after recognizing the Xoff character. Note that the ST16C654 will transmit Xon character(s) automatically when Xoff character(s) were send and software flow control function were disabled after wards. Special cases are provided to detect the special character and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0-3).

Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the ST16C654 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

When auto RTS* is selected, output of RTS* pin is "AND-ed" with MCR bit-1 for manual over ride capability. RTS* pin will change state when MCR bit-1 is set to "1". RTS* pin will be forced to high state when receive FIFO reaches to the programmed trigger level. RTS* pin resumes it original state after content of the data buffer (FIFO) drops below the next lower trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions the ST16C654 will accept additional data to fill the unused transmit and receive FIFO locations.

Special interrupt modes have been added to monitor the hardware and software flow conditions. These are the IER bits 5-7.

The ST16C654 is designed to operate with low power consumption, special sleep mode has been added to stop the clock and reduce the power consumption when it is not used (Green PC). When EFR bit-4 and IER bit-4 are enabled (set to "1"), the ST16C654 enters into sleep mode and resumes it's normal operation when a data is received or state of the modem input pins changes or it is set to transmit data. The ST16C654 stays in this mode till it is disabled.

Special care should be considered for the following interrupt conditions and handling them. After reset if transmitter interrupt is enabled, ST16C654 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS* have lowest interrupt priority. The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition next priority interrupt level will be shown. There are two interrupt conditions that have same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters are reached the programmed trigger level, in this case the ST16C654 FIFO holds equal or more characters than the trigger level. After reading block of data, user can check the LSR bit-0 for additional characters.

Note that, receive time out is functional only in ST16C550/650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Dual baud rate generator is provided to maintain the 16C550 compatibility and provide higher data rate when it is needed. Example 14.4k to 19.2k modems requires to have 57k to 115.2k data rate and 28.8k modem requiems to have 230.4K. The 16C550 compatible parts can only offer 115.2k to maintain the software compatibility. The ST16C654 utilizes 7.32 MHz crystal/clock and provide 16C550 compatible data rate and higher. ST16C550 and ST16C654 baud rate generator tables can be selected is setting and resetting the MCR bit-7. After hardware reset the ST16C654 will set the baud rate table according to pin state of the CLKSEL.

The ST16C654 transmit trigger level, provides additional flexibility to the user for block mode operation. In ST16C550/650 mode LSR bits 5-6 gives indication that transmitter is empty or not, but there is no mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FCR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the ST16C654 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like ST16C450 mode except it can receive and transmit 64 bytes of characters. When DMA mode "1" is activated, user takes the advantage of the block mode operation. In this mode, transmitter/receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or over receive trigger level. Note that since ST16C550 does not have transmit trigger levels, the default trigger level in the ST16C654 is set to 1 byte (trigger level "0").

SERIAL PORT SELECTION GUIDE

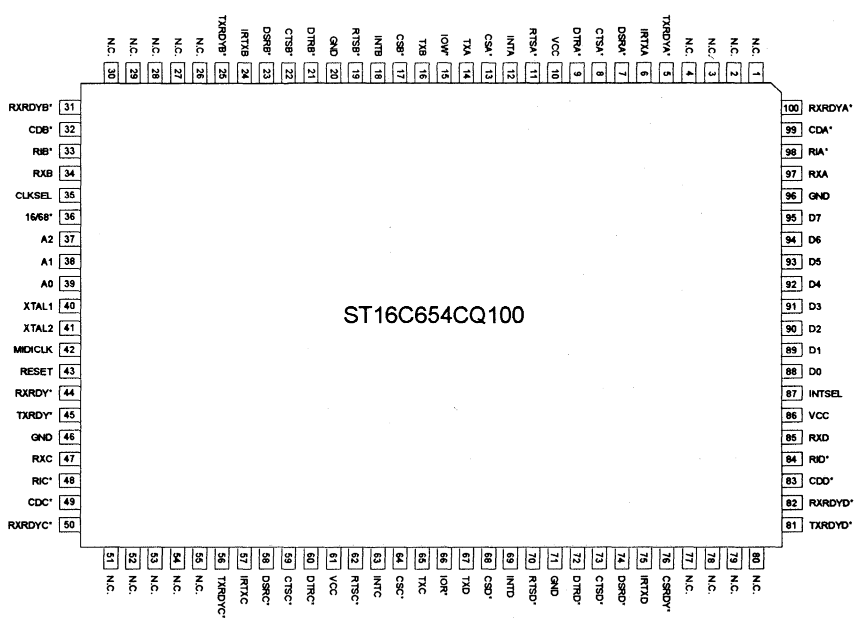
CS*	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

This table is valid when 16/68* pin is connected to GND. Otherwise each UART is selected with individual CSx pins.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	***0***	***0***	***LSB of Divisor Latch***	***LSB of Divisor Latch***
0	***0***	***1***	***MSB of Divisor Latch***	***MSB of Divisor Latch***
0	***1***	***0***	***Enhanced Feature Register***	***Enhanced Feature Register***
1	***0***	***0***	***Xon-1 Word***	***Xon-1 Word***
1	***0***	***1***	***Xon-2 Word***	***Xon-2 Word***
1	***1***	***0***	***Xoff-1 Word***	***Xoff-1 Word***
1	***1***	***1***	***Xoff-2 Word***	***Xoff-2 Word***

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register, Xon1,2 and Xoff1,2 are accessible only when LCR is set to "BF"



Patent pending

ST16C654 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0/ CTS interrupt	0/ RTS* interrupt	0/ Xoff interrupt	0/ Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFO's enabled	0/ FIFO's enabled	0/ RTS*, CTS	0/ Xoff	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	Clock select	0/ IRRT enable	0/ Xon Any	loop back	OP2*/ IRQx enable	OP1*/ no output	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DST	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPREE	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLL***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***
0 1 0	***EFR***	***Auto CTS***	***Auto RTS****	***Special Char. select***	***Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7***	***Cont-3 Tx,Rx Control***	***Cont-2 Tx,Rx Control***	***Cont-1 Tx,Rx Control***	***Cont-0 Tx,Rx Control***
X X X	FIFORdy	RxRdy D	RxRdy C	RxRdy B	RxRdy A	TxRdy D	TxRdy C	TxRdy B	TxRdy A

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1 puts the ST16C654 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C654 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE MCR BIT-7=1	BAUD RATE MCR Bit-7=0	16 x CLOCK DIVISOR "Decimal"
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2K	24
7200	28.8K	16
9600	38.4k	12
19.2K	76.8k	6
38.4K	153.6k	3
57.6K	230.4k	2
115.2K	460.8k	1

HARDWARE FLOW CONTROL OPERATION.

When hardware flow control operation is enabled, the ST16C654 monitors the CTS* pin for transmit operation and receiver trigger level for RTS* operation. When CTS* changes state from low to high, the ST16C654 suspends the transmission operation as soon as complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as CTS* pin goes low. RTS* pin will be forced to high state when receiver FIFO reached to the programmed trigger level. RTS* will go low when Receive Holding Register is below next lower trigger level. The ST16C654 will accept additional data when transmission is suspended during hardware flow control till all locations are filled.

Auto RTS* is functional only when the MCR bit-1 is set to "1". The RST* output pin can change state by setting MCR bit-1 to "0" or "1". This provides additional flexibility for manual over ride and maintain the hardware flow control functionality.

SOFTWARE FLOW CONTROL

When software flow control operation is enabled, the ST16C654 will compare the two sequential receive data with Xoff-1,2 programmed characters. When these characters matched correctly, the ST16C654 will halt the transmission after finishing the transmission of the complete character. The receive ready, Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After the recognition of the Xoff characters the ST16C654 will compare next two incoming characters with Xon-1,2 characters. The ST16C654 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The ST16C654 will send Xoff-1,2 characters as soon as received data passed the programmed trigger level. The ST16C654 will transmit programmed Xon-1,2 characters as soon as receive data reached to the next lower trigger level.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0= disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0= disable the transmitter empty interrupt.
1= enable the transmitter empty interrupt.

IER BIT-2:
0= disable the receiver line status interrupt.
1= enable the receiver line status interrupt.

IER BIT-3:
0= disable the modem status register interrupt.
1= enable the modem status register interrupt.

IER BIT -4:
0= disable sleep mode.
1= enable sleep mode. The ST16C654 enters into power down mode and external clock or oscillator circuit is disabled. Any change of state on the RX, RI*, CTS*, DSR*, and CD* pins start the ST16C654. The

ST16C654 will not lose the programmed bits when sleep mode is activated or deactivated. The ST16C654 will not enter in sleep mode if any interrupt is pending.

IER BIT-5:
0= disable the received Xoff interrupt.
1= enable the received Xoff interrupt. The ST16C654 issues an interrupt when Xoff characters are received and correctly matched with Xoff 1,2 words.

IER BIT-6:
0= disable the RTS* interrupt.
1= enable the RTS* interrupt. The ST16C654 issues interrupt when RTS* pin changes state from low to high.

IER BIT-7:
0= disable the CTS interrupt.
1= enable the CTS interrupt. The ST16C654 issues interrupt when CTS pin changes state from low to high.

INTERRUPT STATUS REGISTER (ISR)

The ST16C654 provides six level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C654 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D5	D4	D3	D2	D1	D0	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY* (Received Data Ready)
2	0	0	1	1	0	0	RXRDY* (Receive Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY* (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS* change of state

ISR BIT-0:
0= an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1= no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-5:
These bits are enabled when EFR bit-4 is set to "1".

ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that CTS, RTS* have been received or issued. Note that the ISR bit-4 will stay "1" till Xon characters are received.

ISR BIT 6-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C654 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0= disable the transmit and receive FIFO.
1= enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0= No change.
1= Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0= No change.
1= Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0= No change.
1= Changes RXRDY* and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C654 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C654 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
These bits are used to set the trigger level for the transmit FIFO interrupt. The ST16C654 will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	FIFO trigger level
0	0	8
0	1	16
1	0	32
1	1	56

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	8
0	1	16
1	0	56
1	1	60

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0= no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0= ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0= normal operating condition.
1= forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable (DLAB).
0= normal operation.
1= Divisor latch and Enhanced Feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0= force DTR* output to high.
1= force DTR* output to low.

MCR BIT-1:
0= force RTS* output to high.
1= force RTS* output to low.
RTS* is used as hardware flow control signal when enabled via EFR bit-6. RTS* goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control. functions normally when hardware flow control is disabled.

MCR BIT-2:
This bit is used in internal loop-back mode only.
0= set OP1* output to high.
1= set OP1* output to low.

MCR BIT-3:
0= set OP2* output to high (internal loopback mode). Forces INTx outputs to three state mode if INTSEL pin is left open or connected to GND. It has no effect if INTSEL pin is connected to VCC.
1= set OP2* output to low (internal loopback mode). Sets the INTx outputs to active mode if INTSEL pin is left open or connected to GND. It has no effect if INTSEL pin is connected to VCC.

MCR BIT-4:
0= normal operating mode.
1= enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT-5:
0 = Disable Xon any function, ST16C550 compatible.
1= Enable Xon any function.

MCR BIT-6:
0= Standard UART receive and transmit input / output.
1= Infrared receive and transmit input / output. The TX A-D outputs and RX A-D inputs are converted to Infrared encoder/decoder output/input format. TX output goes low when this bit is set to "1".

MCR BIT-7:
0= Normal or divide by one clock input. Standard ST16C550 baud rates can be selected when this bit is set to "0" and 1.8432 MHz crystal is used.
1= Divide by four clock input. Standard ST16C550 baud rates can be selected when this bit is set to "1" and 7.372 MHz crystal is used.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0= no data in receive holding register or FIFO.
1= data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0= no overrun error (normal).
1= overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0= no parity error (normal).
1= parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0= no framing error (normal).
1= framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0= no break condition (normal).
1= receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
It indicates that the ST16C654 is ready to accept a new character for transmission. In addition, it causes the ST16C654 to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set.

0= transmit holding register is not empty.
1= transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load upto 64 bytes of data to the ST16C654.

LSR BIT-6:
0= transmitter holding and shift registers are full.
1= transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0= normal.
1= at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C654 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C654 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C654 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C654 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS* in the MCR during local loop-back mode. It is the compliment of the CTS* input.
CTS* functions as hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as complete character is transmitted.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C654 provides a temporary data register to store 8 bits of information for variable use.

ENHANCED FEATURE REGISTER (EFR)

Enhanced Features can be Enable/Disabled via this register.

EFR BIT 0-3:
Combinations of software flow control can be selected by programming this bits.

Cont-3	Cont-2	Cont-1	Cont-0	Tx, Rx software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2 : Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2 : Xoff1 and Xoff2 Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2

EFR BIT-4:
Enhanced functions enable bit.
0= disables the IER bits 4-7, ISR bits 4-5, FCR bits 4-5 and MCR bits 5-7. After hardware reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to "0" to be compatible with ST16C550 mode.
1= enables the enhanced functions. When this bit is set to "1" all enhanced features of the ST16C654 are enabled. The content of the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7, the EFR bit-4 can be set to "0" to latch the contents of the new values, this feature is provided to prevents the existing software's to alter / overwrite the ST16C654 enhanced functions.

EFR BIT-5:
0= Normal.
1= Special character detect. ST16C654 compares the incoming receive data with Xoff-2 data. Up on correct match, the received data will be transferred to FIFO and ISR Bit-4 will be set to indicate detection of special character.

EFR BIT-6:
RTS* flow control.
0 = Normal. RTS* flow control is disabled. Standard ST16C550 mode.
1 = RTS* pin goes high when receive FIFO's are reach to the programmed trigger level.

EFR Bit-7:
CTS* flow control.
0 = Normal. CTS* flow control mode is disabled. Standard ST16C550 mode.
1 = Transmission is resumed when low input signal is detected on the CTS* pin.

FIFO READY REGISTER

This register provides the state of the transmit and receive FIFO.

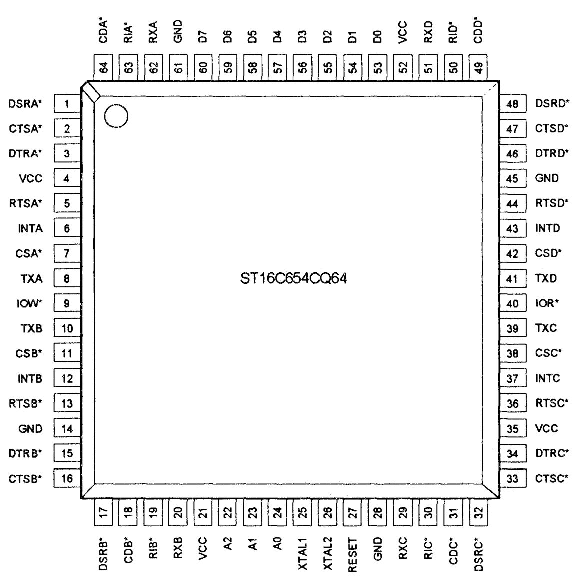
FIFORdy Bit 0-3:
0 = Transmit FIFO is full. The ST16C650 can not take any more transmit data.
1 = One or more empty location in FIFO or FIFO is below transmit trigger level.

FIFORdy Bit 4-7:
0 = Receiver is above the trigger level or timeout is occurred.
1 = Receiver is not ready.

ST16C654 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7= input signals
FCR	FCR BITS 0-7=0
EFR	EFR BITS 0-7=0

SIGNALS	RESET STATE
TX A-D	High
RTS* A-D	High
DTR* A-D	High
RXRDY* A-D	High
TXRDY* A-D	Low



Patent pending

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{RClk}		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

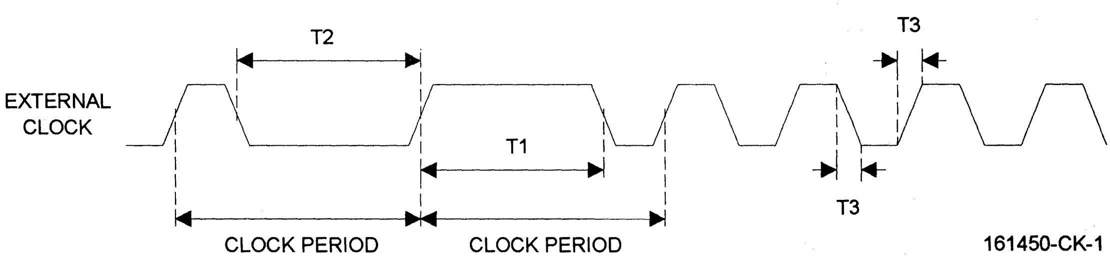
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current		1.3	2.5	mA	
V_{OP}	Operating voltage	3		5	V	
I_{SLP}	Avg sleep mode current		800	1	µA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	5		15	kΩ	*Marked pins

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

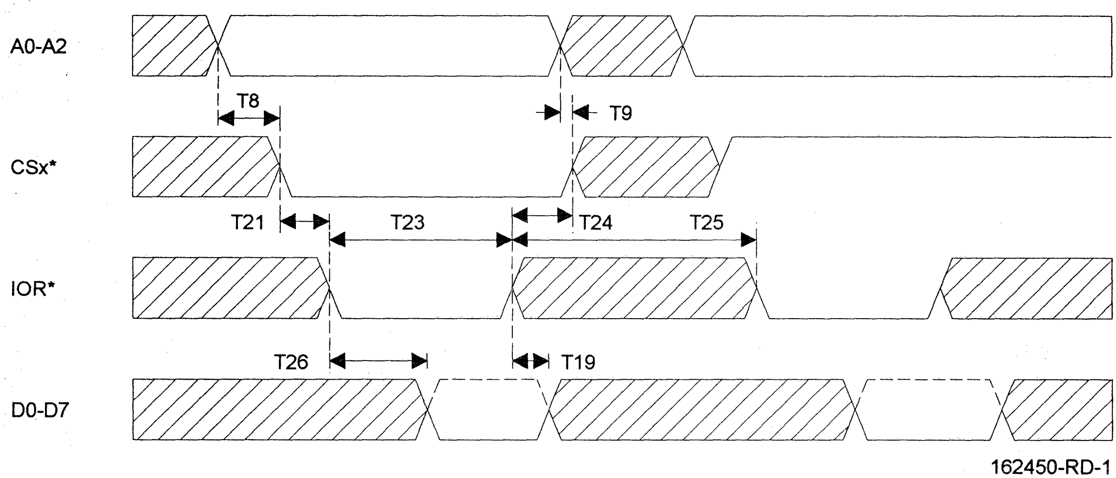
CLOCK TIMING



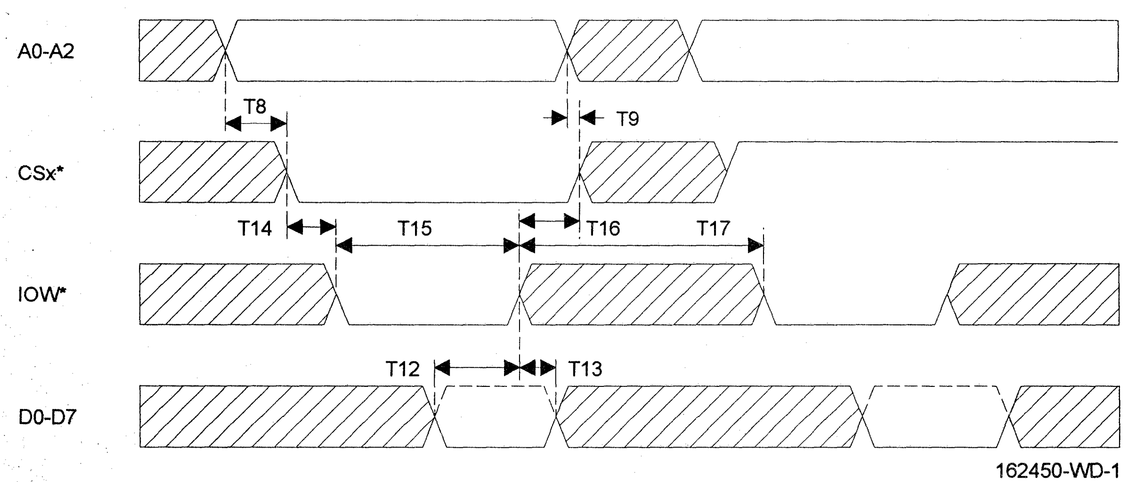
161450-CK-1

Patent pending

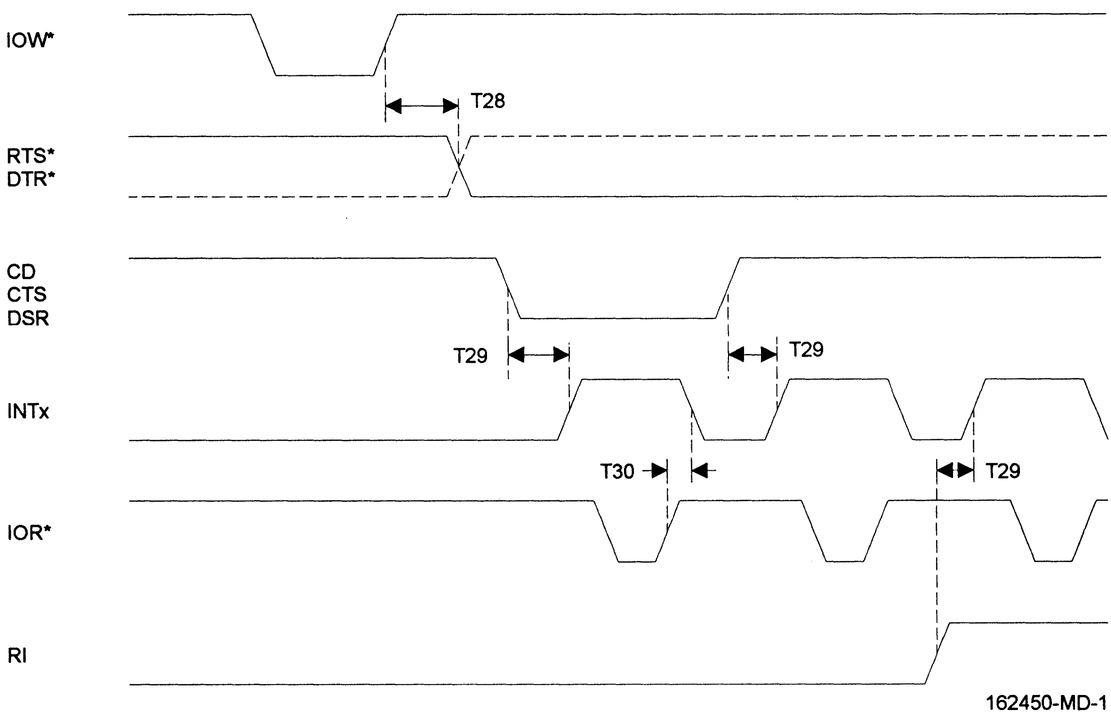
GENERAL READ TIMING



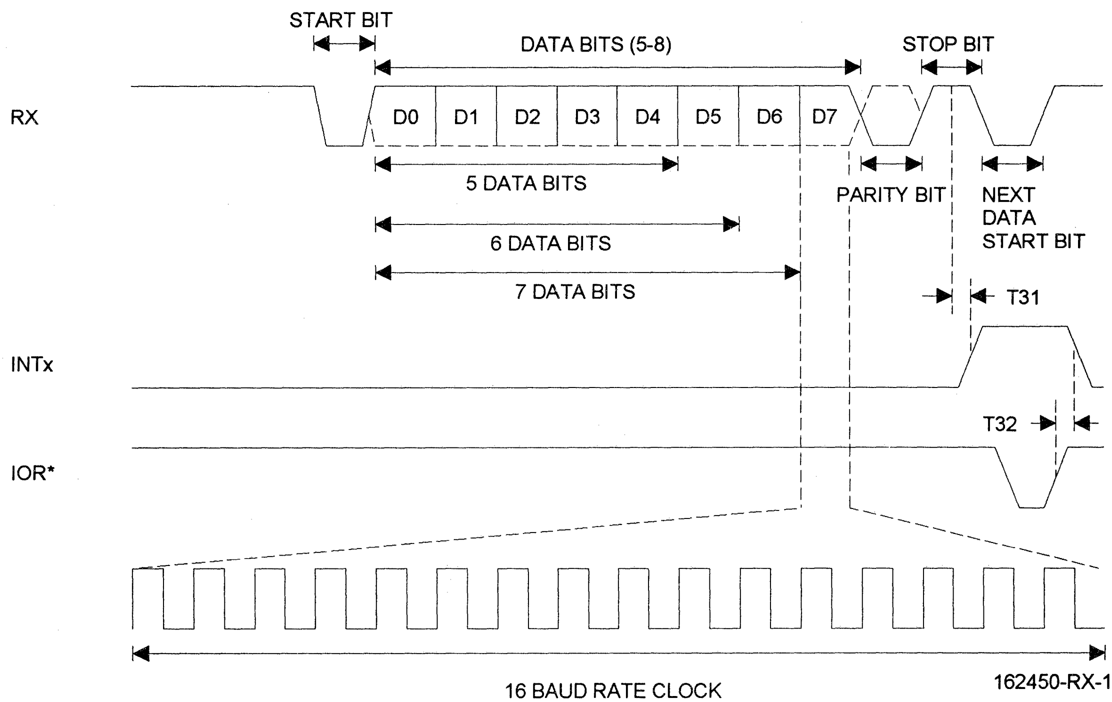
GENERAL WRITE TIMING



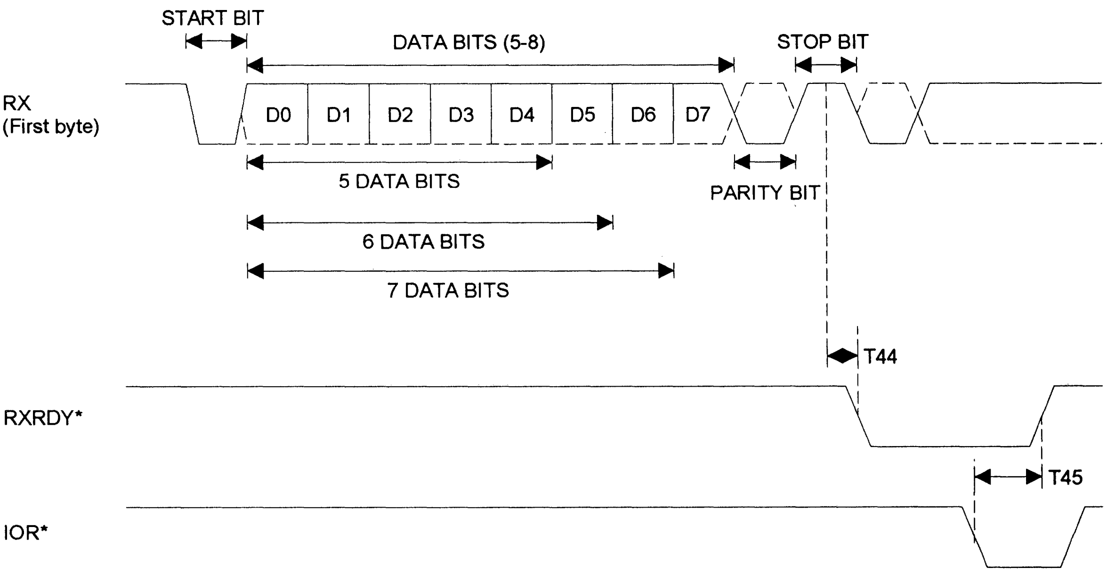
MODEM TIMING



RECEIVE TIMING



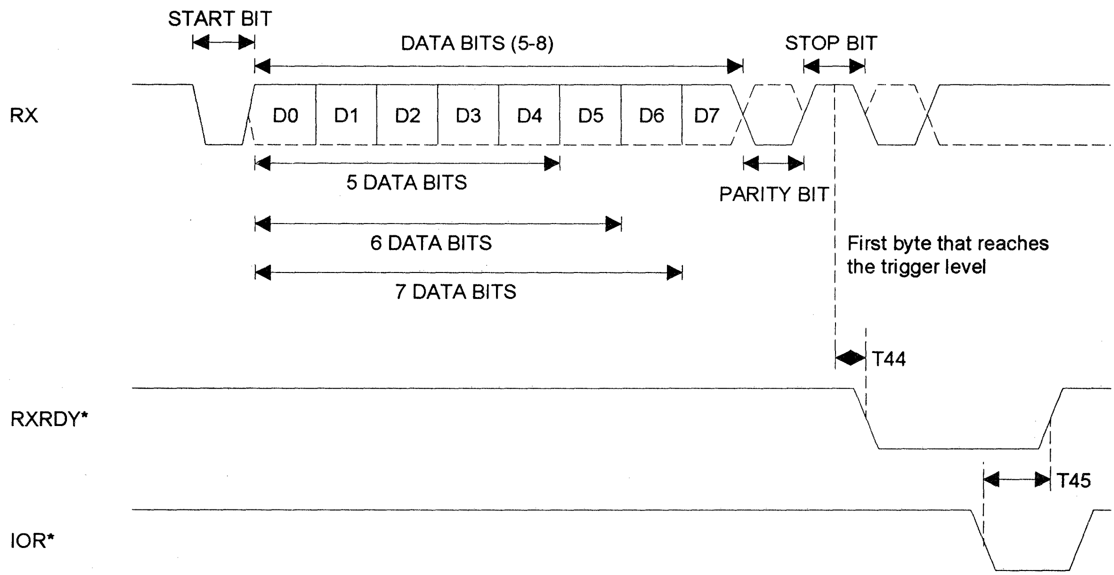
RXRDY TIMING FOR MODE "0"



16552-RX-2

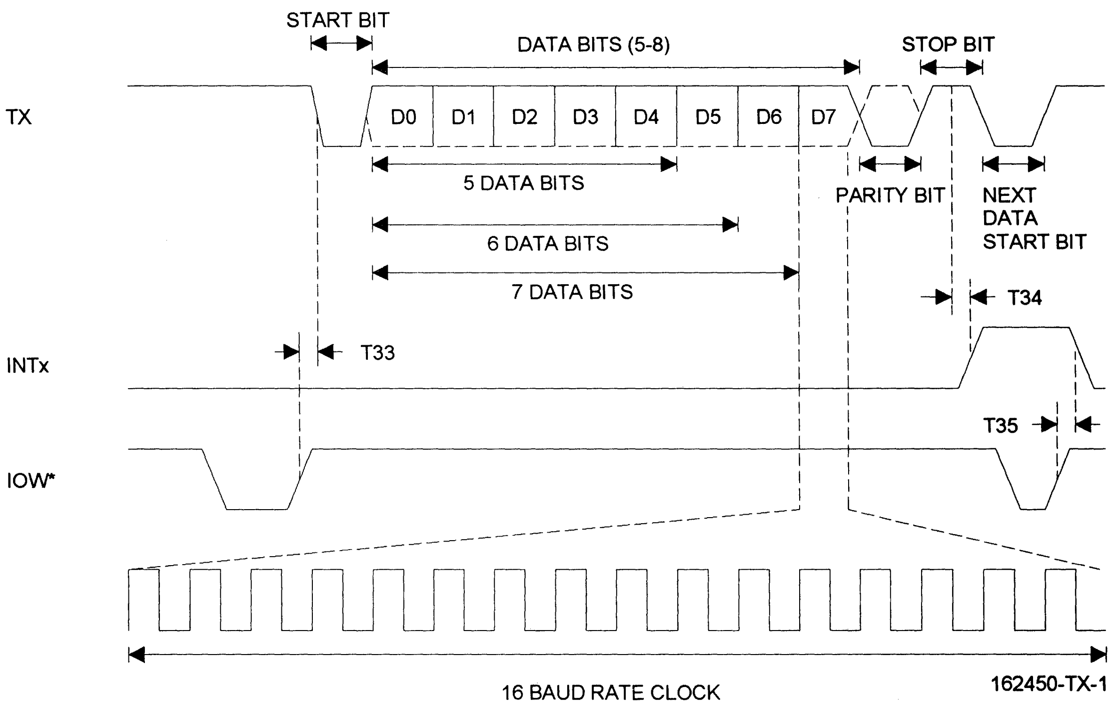
Patent pending

RXRDY TIMING FOR MODE "1"



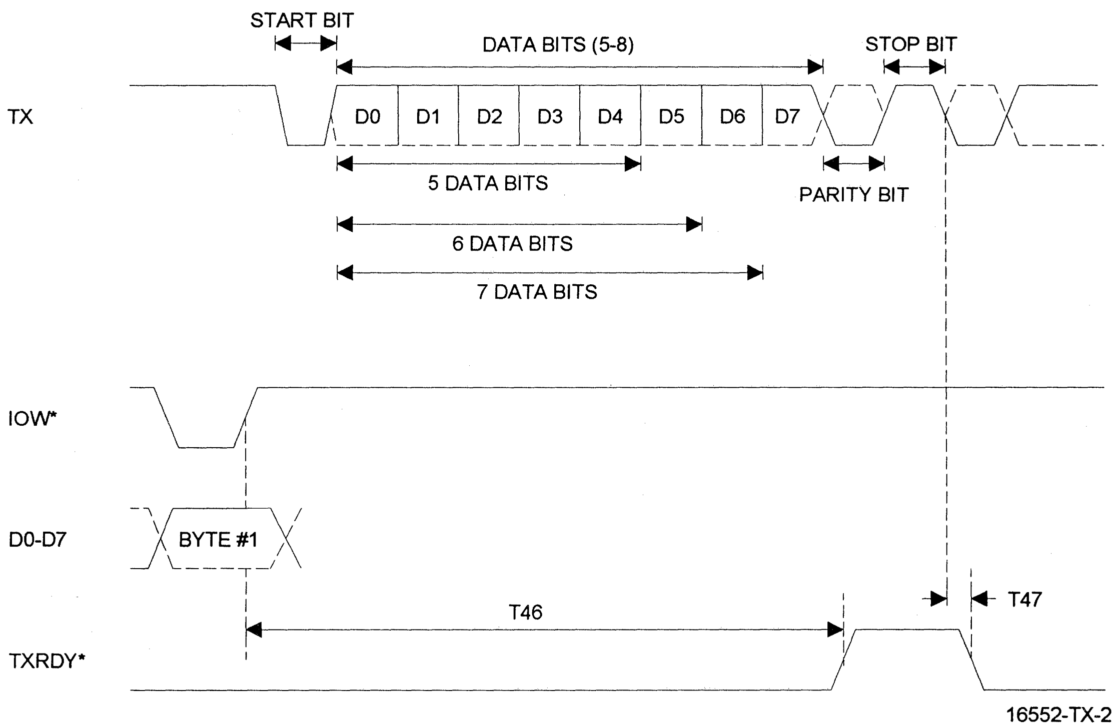
16552-RX-3

TRANSMIT TIMING

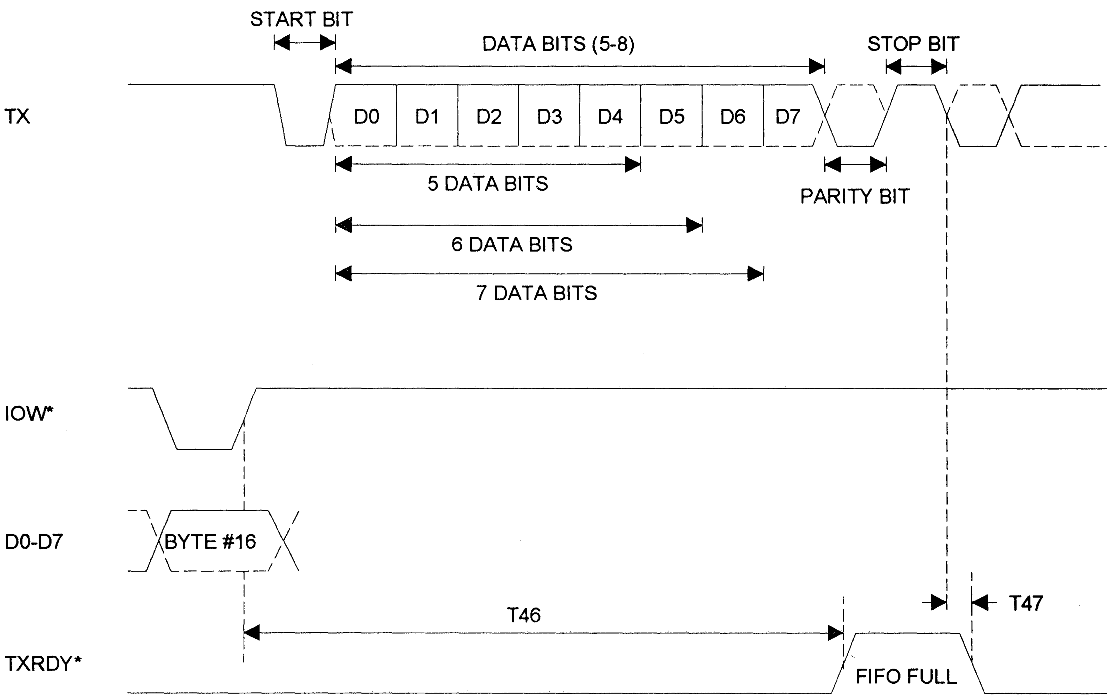


Patent pending

TXRDY TIMING FOR MODE "0"

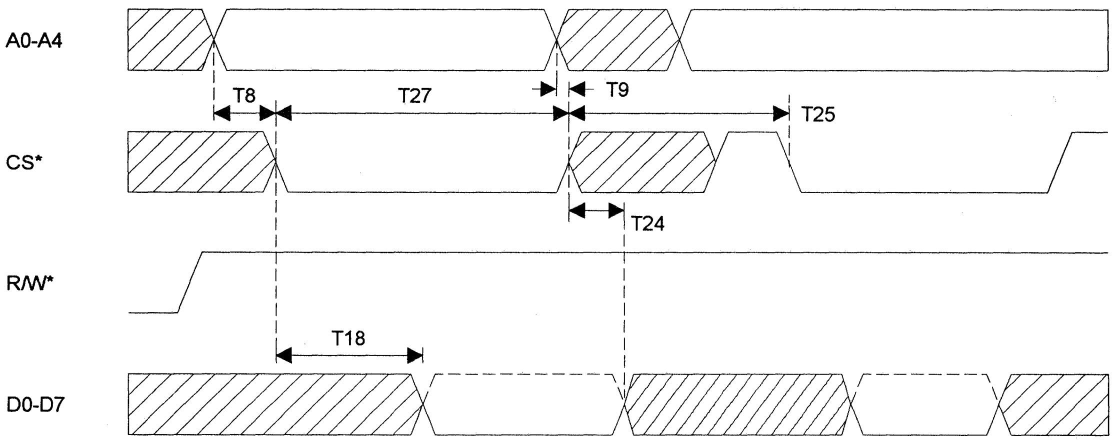


TXRDY TIMING FOR MODE "1"



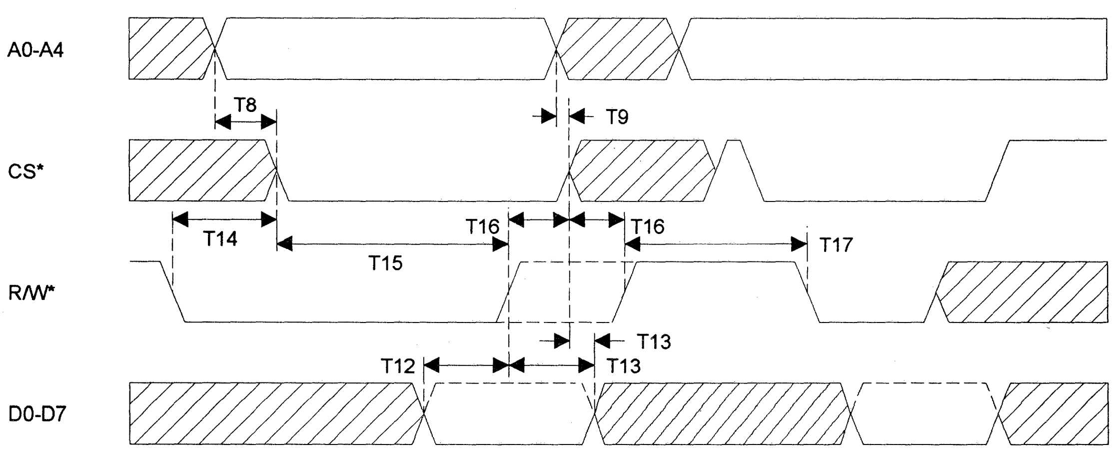
16552-TX-3

GENERAL READ TIMING



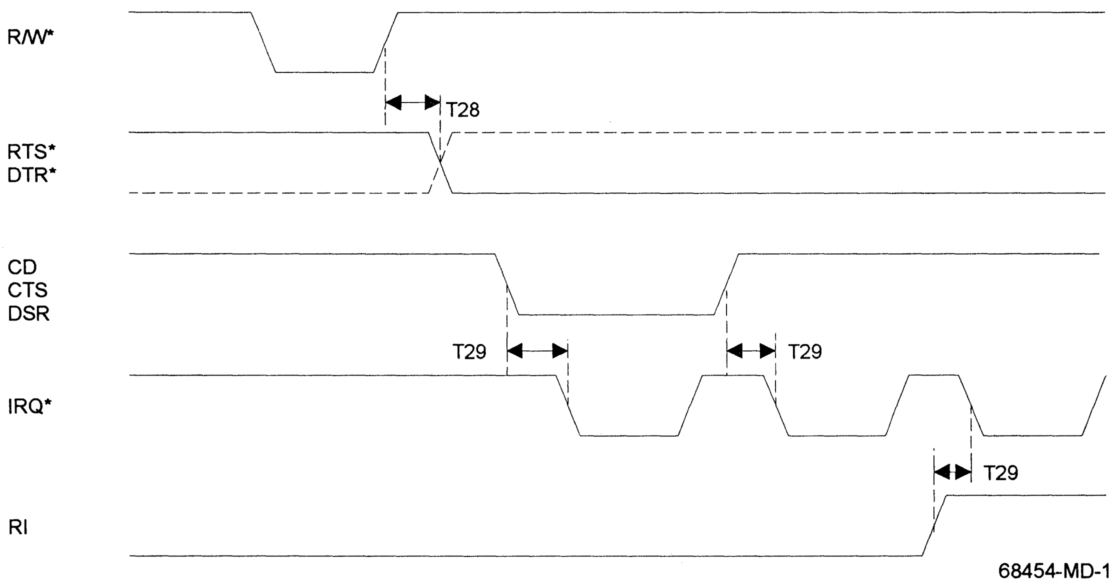
8454-RD-1

GENERAL WRITE TIMING

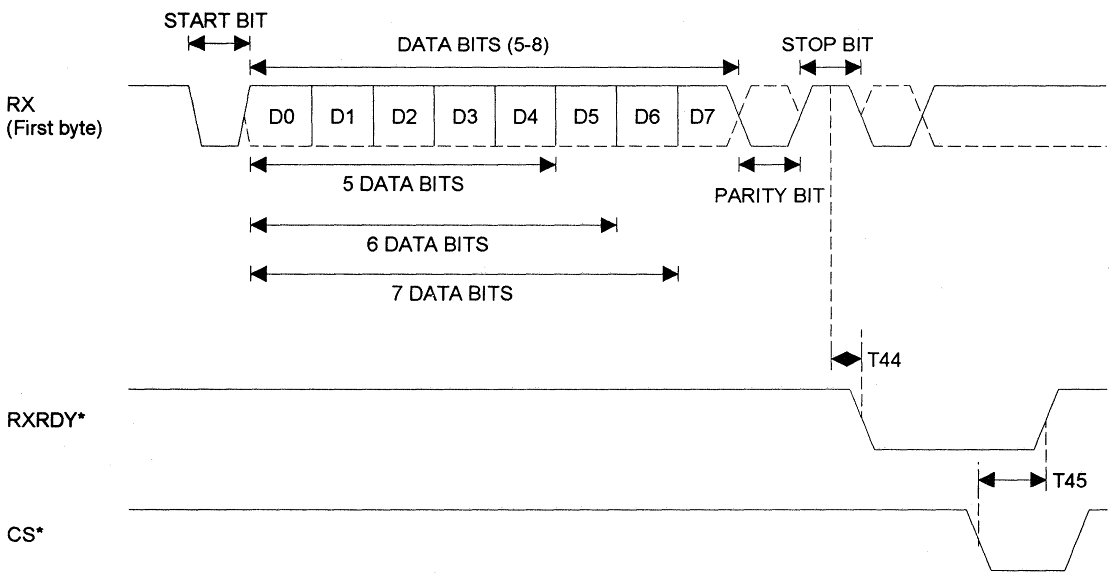


68454-WD-1

MODEM TIMING

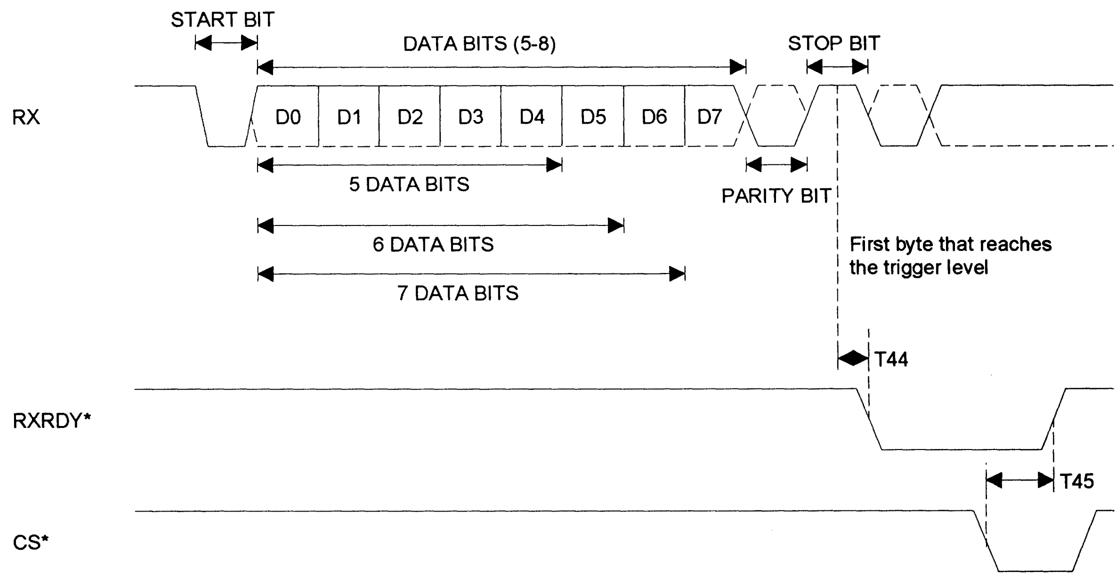


RXRDY TIMING FOR MODE "0"



68554-RX-2

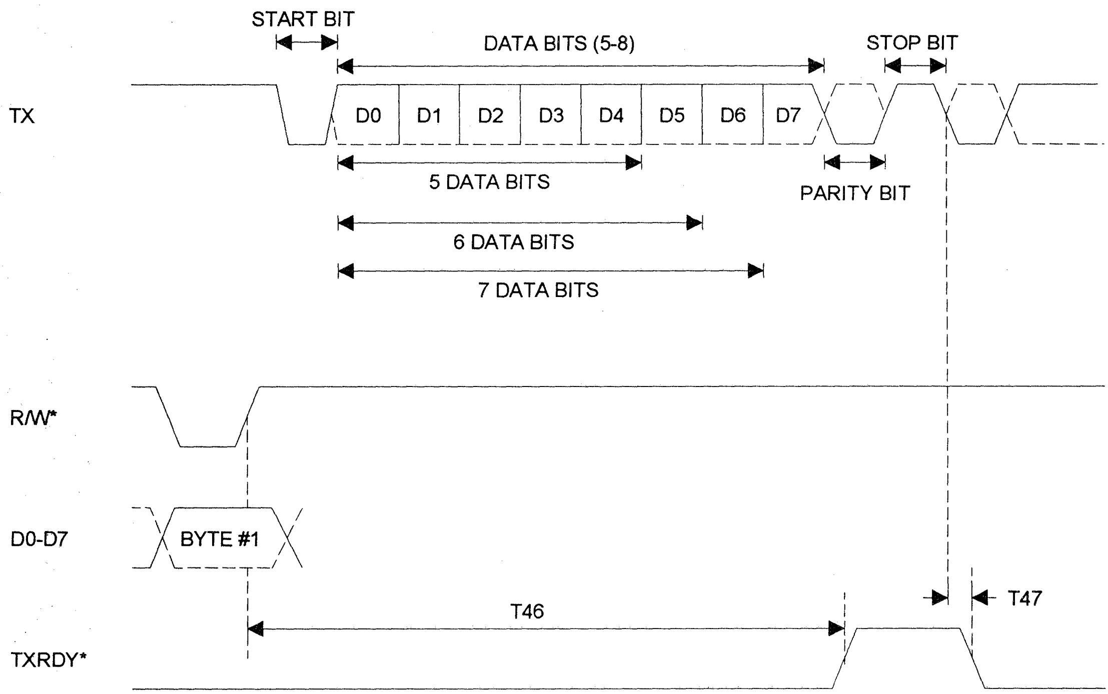
RXRDY TIMING FOR MODE "1"



68554-RX-3

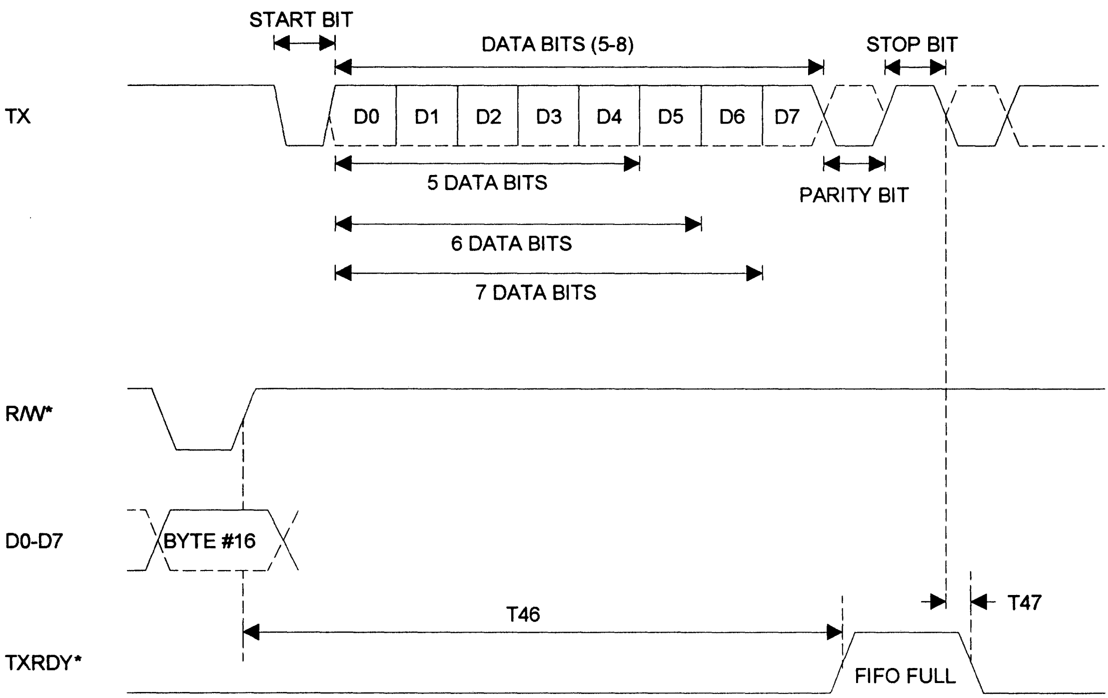
Patent pending

TXRDY TIMING FOR MODE "0"



68554-TX-2

TXRDY TIMING FOR MODE "1"



68554-TX-3

STARTECH
An EXAR Company

XR-68C681
XR-88C681

Printed August 7, 1995

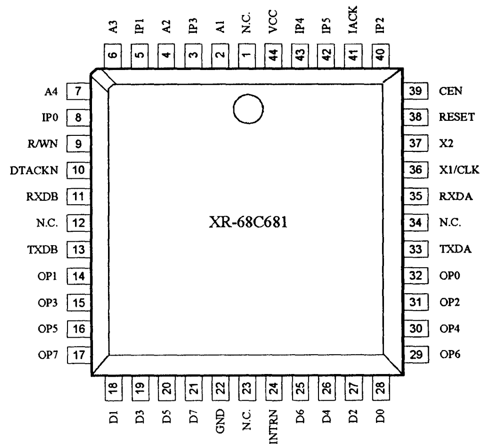
DUAL UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The XR-68C681/88C681 is a Dual Universal Asynchronous Receiver and Transmitter with 3 bytes of receive FIFO. The XR-68C681/88C681 is the improved version of the Signetics SCC2681 Dual UART with additional features.

The XR-68C681/88C681 provides independent receive and transmit operating speeds that can be selected as one of the eighteen fixed baud rates, a 16 X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock input. The XR-68C681/88C681 provides a power-down mode in which the oscillator is stopped but the register contents are stored.

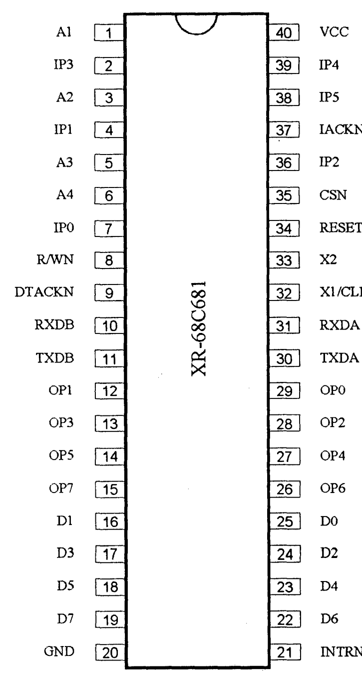
PLCC Package



FEATURES

- Pin to pin and functional compatible to SCC2681
- 3 bytes receive FIFO
- Full duplex asynchronous transmit receive operation
- Programmable character lengths (5, 6, 7, 8)
- Parity, framing, and over run error
- Programmable 16-bit timer/counter
- On-chip crystal oscillator
- TTL compatible inputs, outputs
- Single interrupt output with seven selectable interrupting conditions
- 18 fixed baud rates from 50Hz to 1M

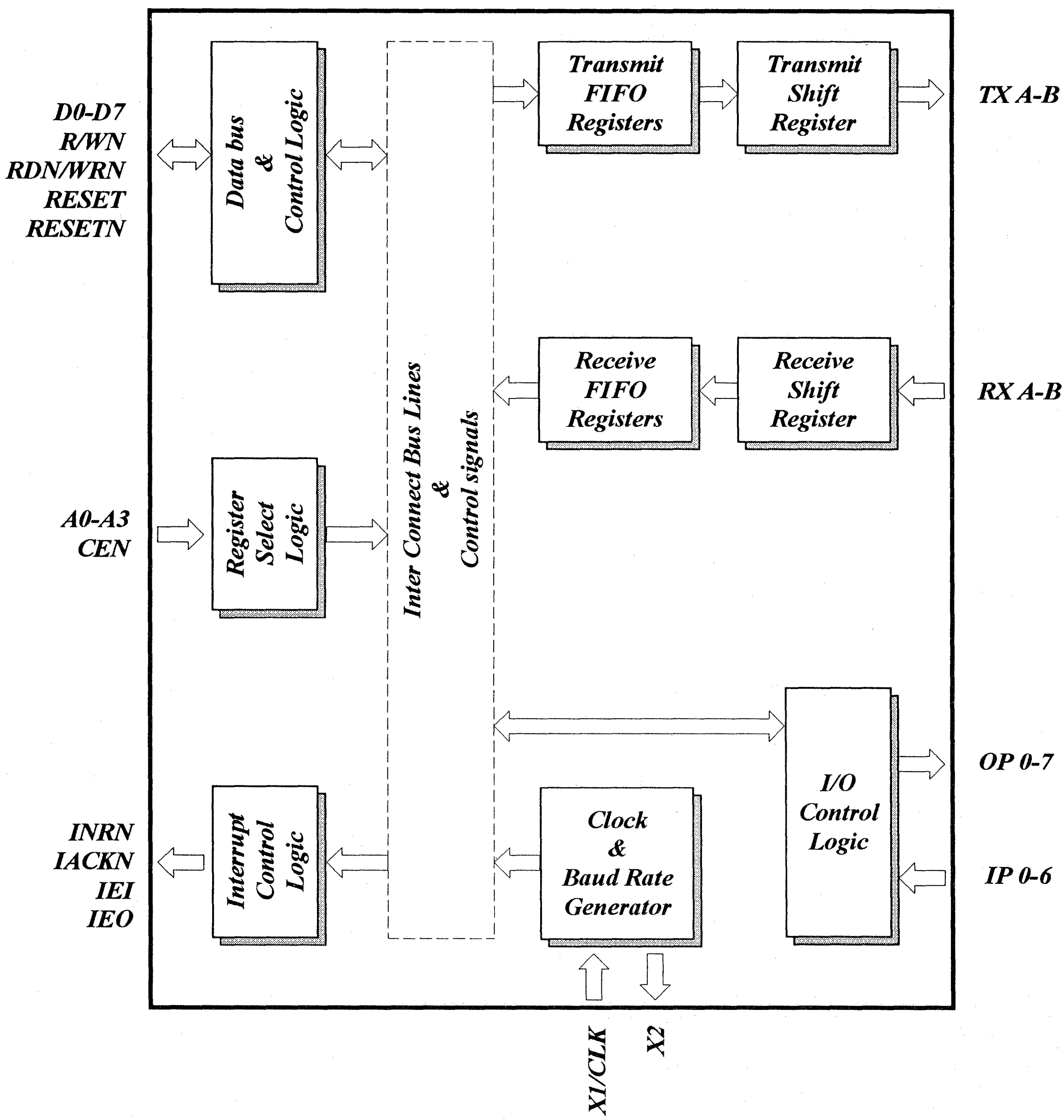
Plastic-Dip Package



ORDERING INFORMATION

Part number	Package	Operating temperature
XR-88C681CP28	Plastic-Dip	0° C to + 70° C
XR-88C681CP40	Plastic-Dip	0° C to + 70° C
XR-88C681CJ44	PLCC	0° C to + 70° C
XR-68C681CP40	Plastic-Dip	0° C to + 70° C
XR-68C681CJ44	PLCC	0° C to + 70° C

XR-68C681/88C681 BLOCK DIAGRAM



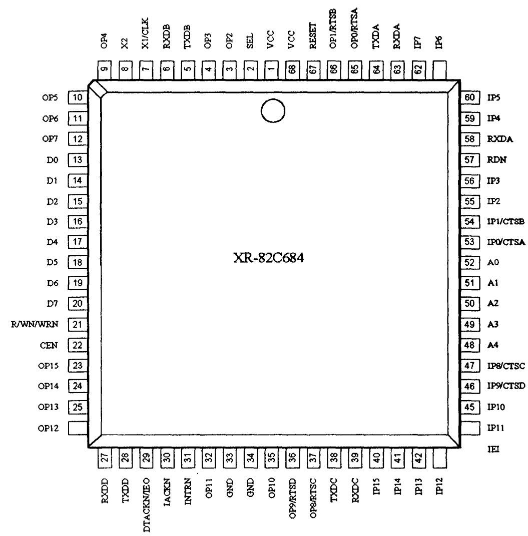
QUAD UNIVERSAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The XR-82C684 is a Quad Universal Asynchronous Receiver and Transmitter with 3 bytes of receive FIFO. The XR-82C684 is software compatible with XR-68C681/88C681 and Signetics SCC2681 Dual UART.

The XR-82C682 provides independent receive and transmit operating speeds that can be selected as one of the eighteen fixed baud rates, a 16 X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock input. The XR-82C684 provides a power-down mode in which the oscillator is stopped but the register contents are stored.

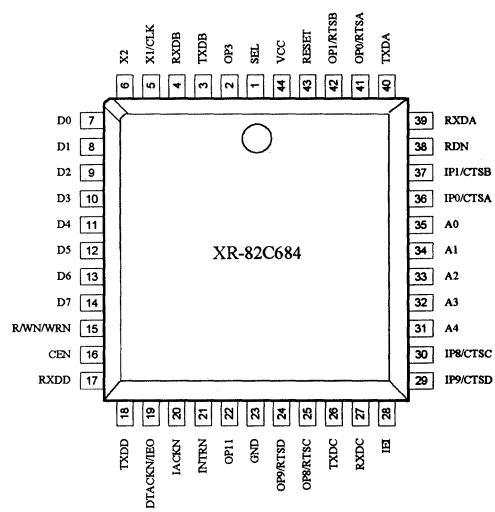
68 Pin PLCC Package



FEATURES

- Functional compatible with SCC2681
- 3 bytes receive FIFO
- Full duplex asynchronous transmit receive operation
- Programmable character lengths (5, 6, 7, 8)
- Parity, framing, and over run error
- Programmable 16-bit timer/counter
- On-chip crystal oscillator
- TTL compatible inputs, outputs
- Single interrupt output with seven selectable interrupting conditions
- 18 fixed baud rates from 50Hz to 1M

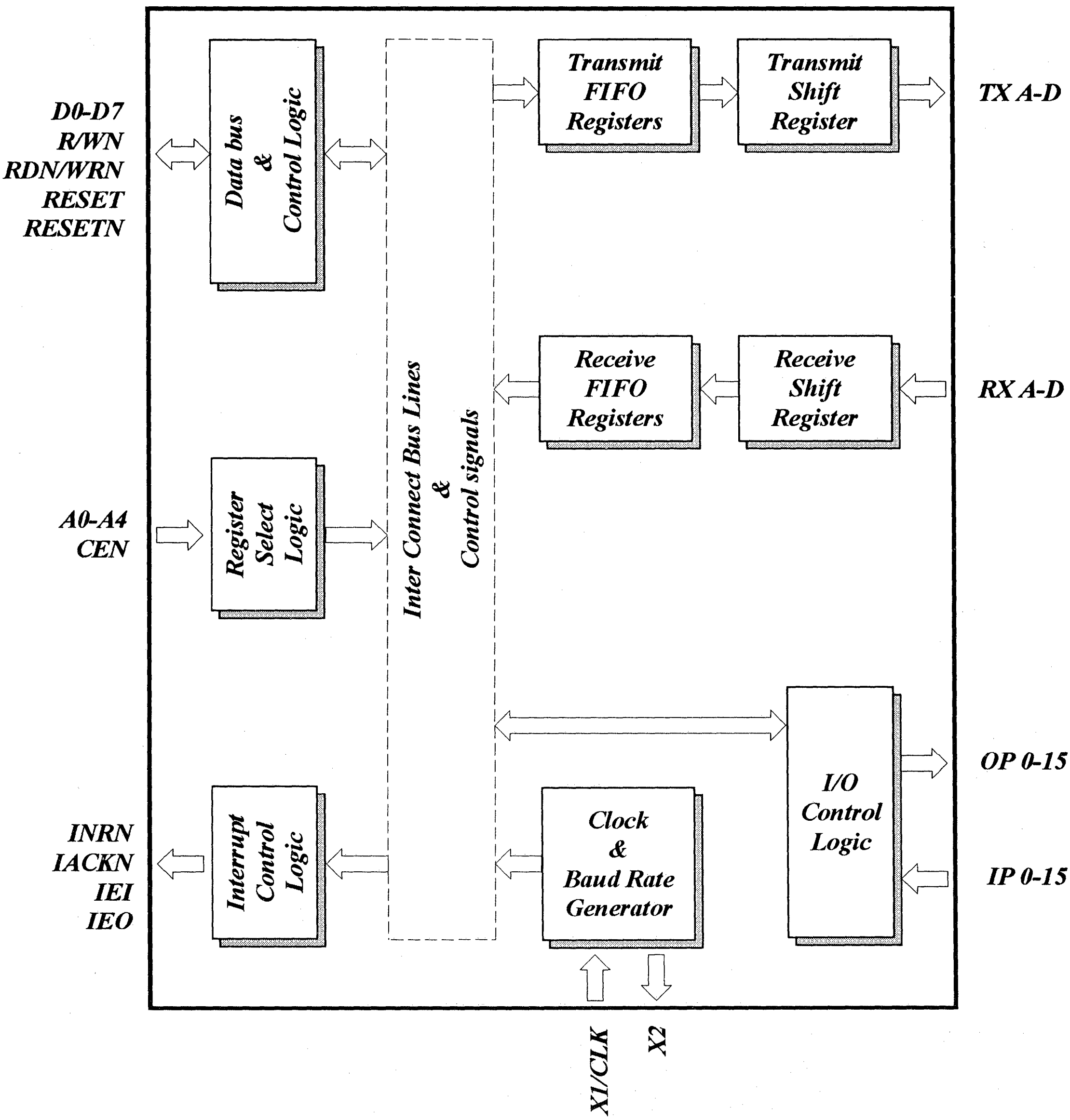
44 Pin PLCC Package



ORDERING INFORMATION

Part number	Package	Operating temperature
XR-82C684CJ44	PLCC	0° C to + 70° C
XR-82C684CJ68	PLCC	0° C to + 70° C

XR-68C681/88C681 BLOCK DIAGRAM



STARTECH

An EXAR Company

ST16C452AT
ST16C452PS

Printed August 7, 1995

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH PARALLEL PRINTER PORT

3

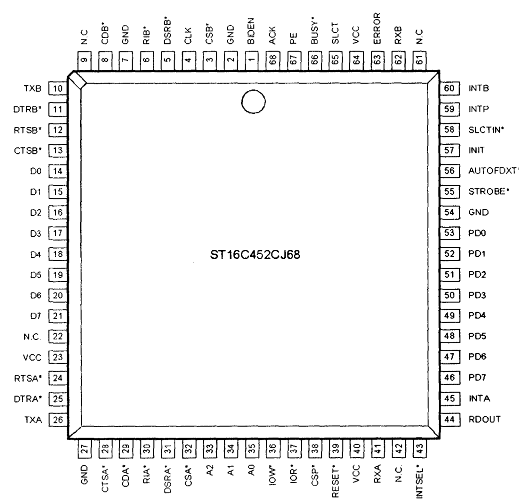
DESCRIPTION

The ST16C452 is a dual universal asynchronous receiver and transmitter with a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz. STARTECH ST16C452PS provides additional features to control the printer port direction without any additional external logic.

The ST16C452 is an improved version of the VL16C452 UART with higher operating speed and lower access time. The ST16C452 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C452 provides internal loop-back capability for on board diagnostic testing.

The ST16C452 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



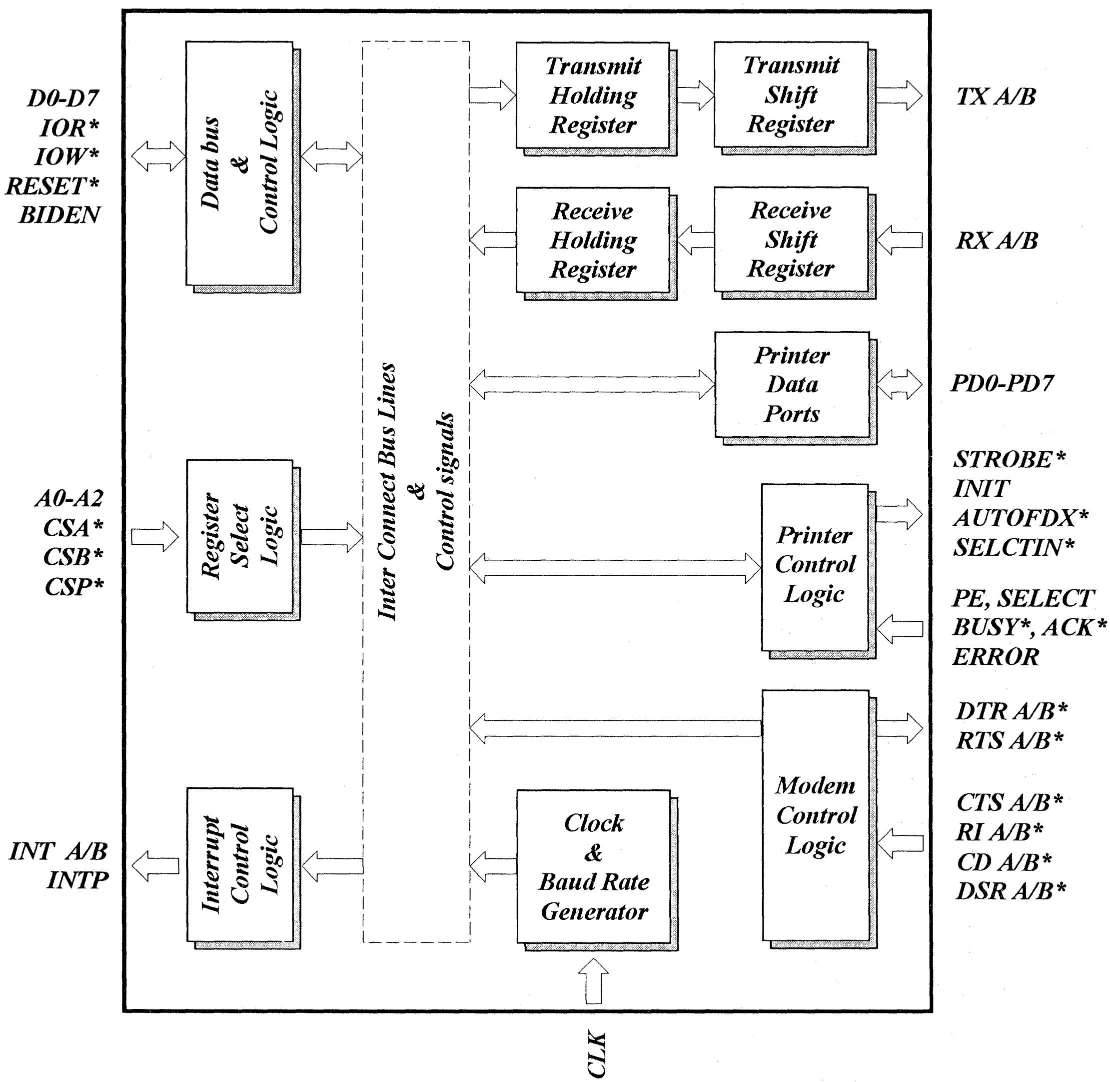
FEATURES

- Pin to pin and functional compatible to VL16C452, WD16C452
- Fully compatible with all new bi-directional PS/2 printer port registers.
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- Software compatible with INS8250, NS16C450
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C452CJ68	PLCC	0° C to + 70° C
ST16C452IJ68	PLCC	-40° C to + 85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input mode for ST16C452AT and software controlled mode (input/output) to ST16C452PS. A low sets the ST16C452 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C452 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C452 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS* A/B	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR* A/B	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI* A/B	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from

ST16C452AT
ST16C452PS

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			telephone line.
CD* A/B	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR* A/B	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS* A/B	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C452 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS* A/B	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C452 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55*	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56*	I/O	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or initialize line printer (open drain active low). When this signal is low it causes the printer to be initializes.
SLCTIN*	58*	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low it selects the printer.
ERROR*	63*	I	General purpose input or line printer error (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
PE	67*	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68*	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.

ST16C452AT
ST16C452PS

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,22 42,54,61	O	Signal and power ground. All ground pins are connected internally.
VCC	23,40,64	I	Power supply input. All power pins are connected internally.

* Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS A/B

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C452 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

ST16C452AT
ST16C452PS

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2_{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C452 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
This bit is used for internal loop-back mode, and is not used for regular operation.

MCR BIT-3:
0= sets the INT output pin to three state mode.
1= enables the INT output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2,3are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic “1”, a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C452 provides a temporary data register to store 8 bits of information for variable use.

SIGNAL	RESET STATE
TX A/B	High
RTS* A/B	High
DTR* A/B	High
INT A/B,P	Three state mode

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C452 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	BIT-0=1, ISR BITS 1-7=0
LCR	BITS 0-7=0
MCR	BITS 0-7=0
LSR	BITS 0-4=0,
LSR	BITS 5-6=1 LSR, BIT 7=0
MSR	BITS 0-3=0,
MSR	BITS 4-7=input signals

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

ST16C452XX	CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
ST16C452AT	X	0	X	Output mode
ST16C452PS	X	0	AA Hex	Input mode
ST16C452PS	X	0	55 Hex	Output mode
ST16C452AT	X	1	X	Input mode
ST16C452PS	0	1	X	Output mode
ST16C452PS	1	1	X	Input mode

PRINTER PORTREGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to “1” permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to “0” at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to “1”.

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to “1” permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

ST16C452AT
ST16C452PS

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output. I/O select register and control register bit-5 are only available for ST16C452PS parts.

ST16C452 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	low, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

ST16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR	IRQ STATE	1	1
					1= No interrupt 0= Interrupt (PS only)		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
		0=Output (PS only) 1=Input (PS only) X= AT only	0=INTP output disabled 1=INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data set up time	15			ns	
T_{13}	IOW* delay from chip select	10			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{CLK}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7-PD0 setup time	10			ns	
T_{41}	PD7-PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
N	Baud rate devisor	1		2_{16}-1		

Note 1 * = Baudout* cycle

ST16C452AT
ST16C452PS

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

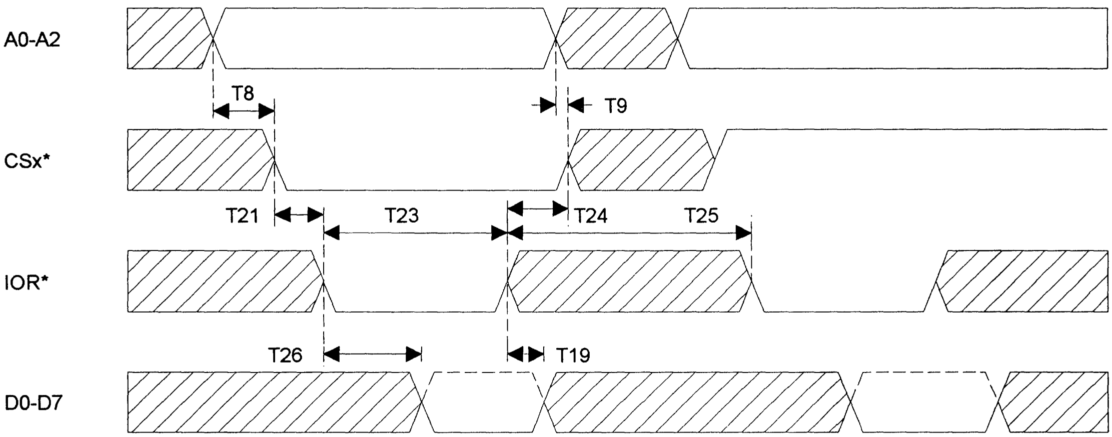
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all the outputs
I_{CC}	Avg. power supply current		12		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	4		15	kΩ	* Marked pins

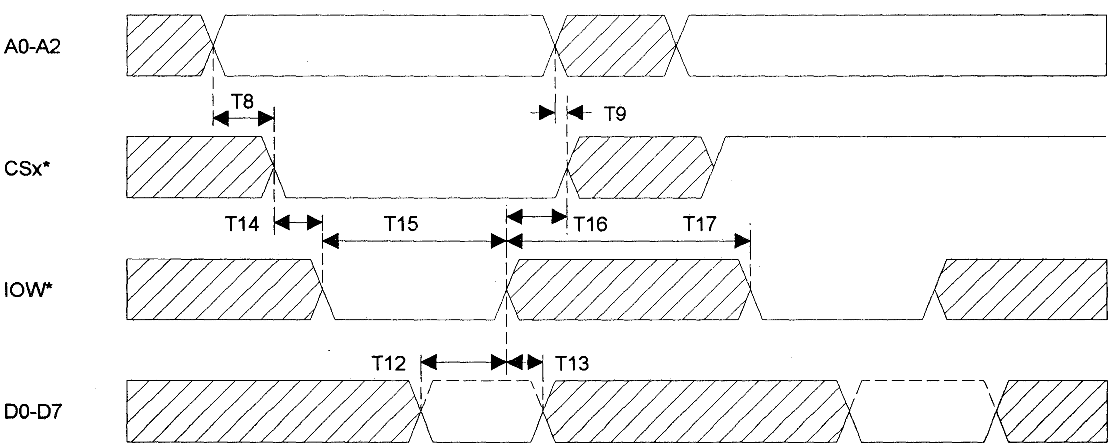
This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

GENERAL READ TIMING



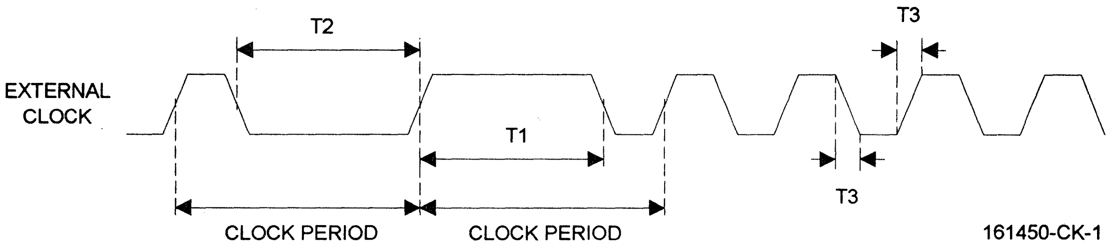
162450-RD-1

GENERAL WRITE TIMING

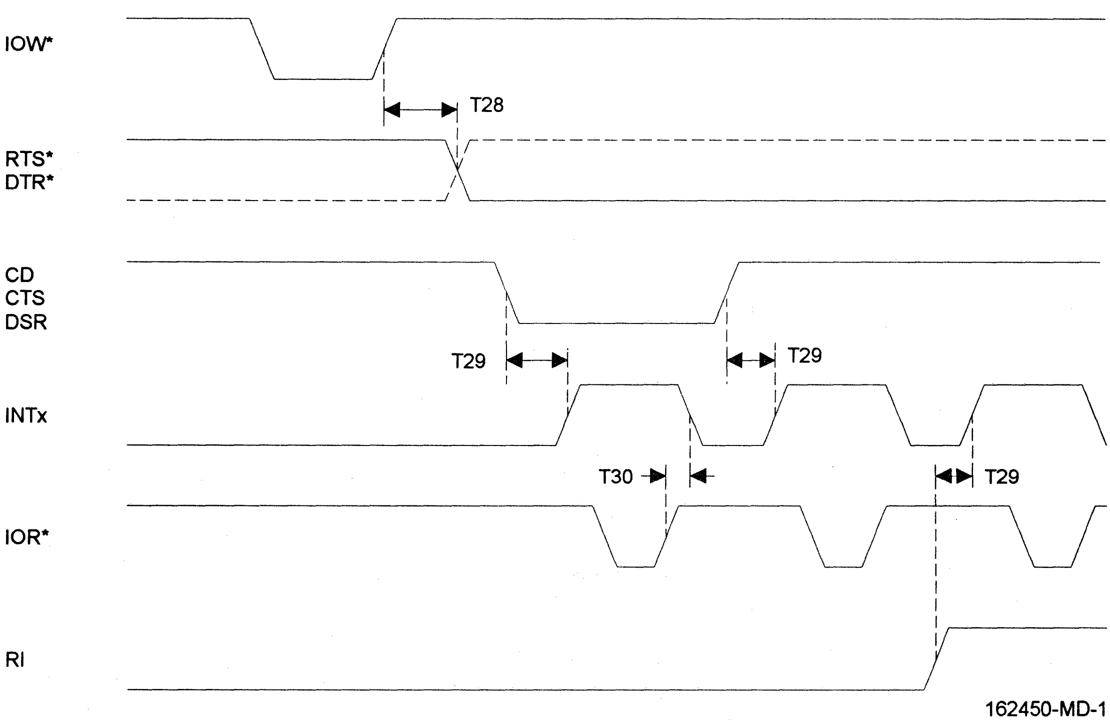


162450-WD-1

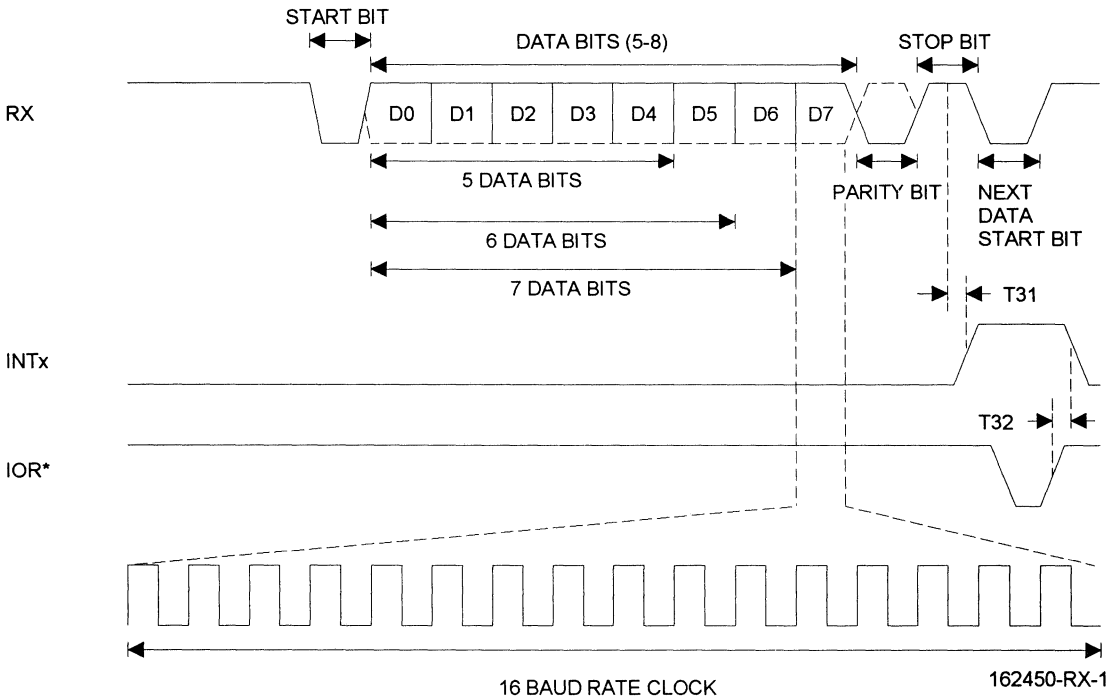
CLOCK TIMING



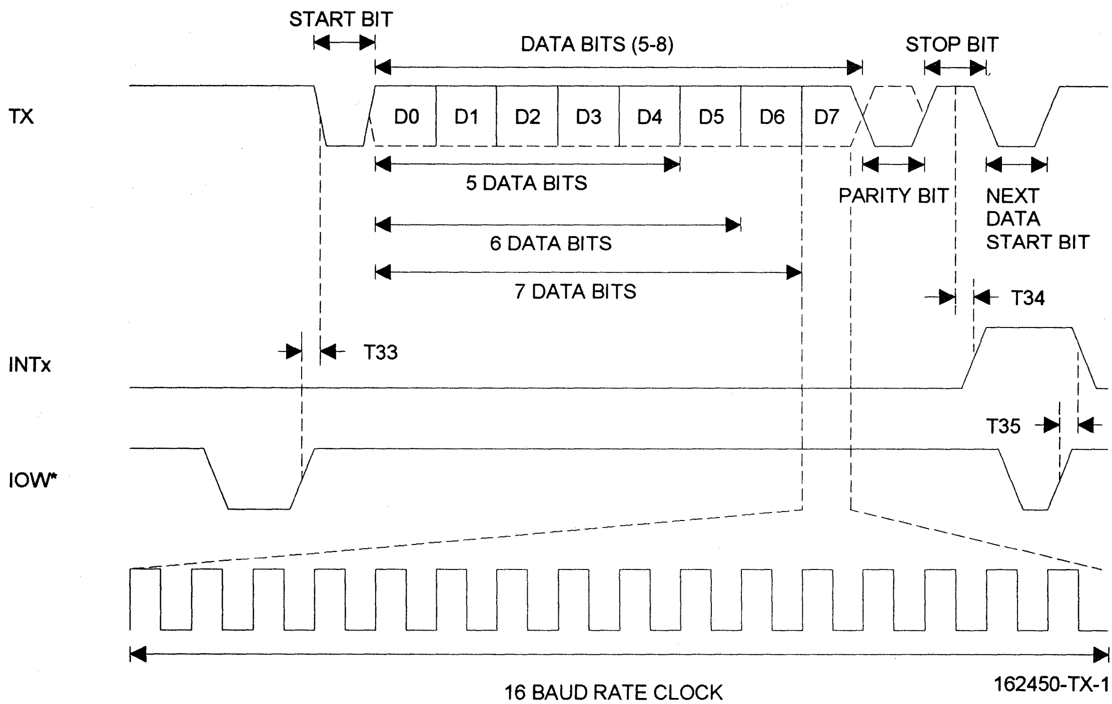
MODEM TIMING



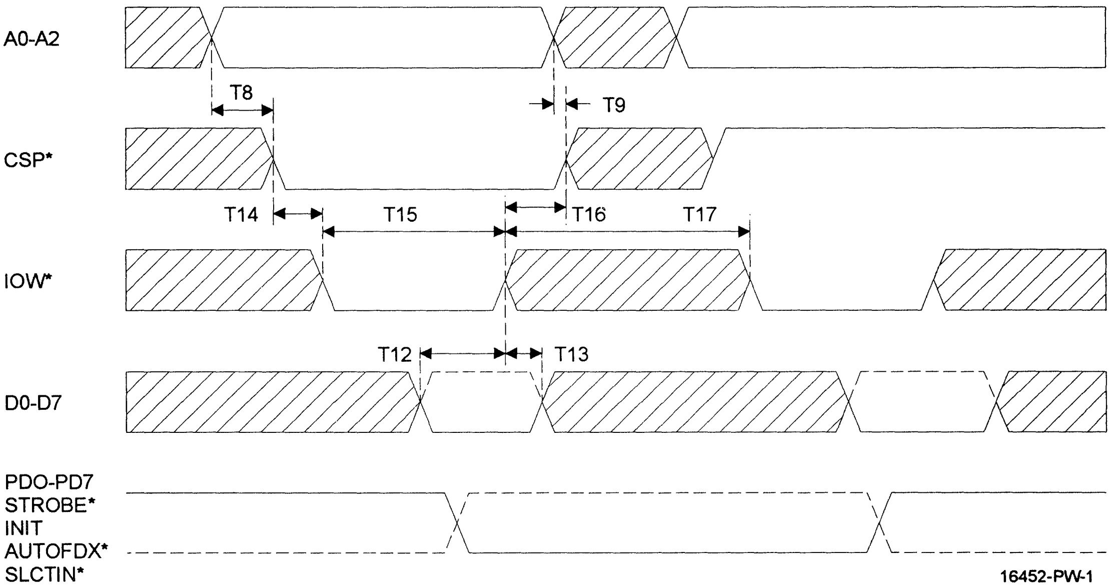
RECEIVE TIMING



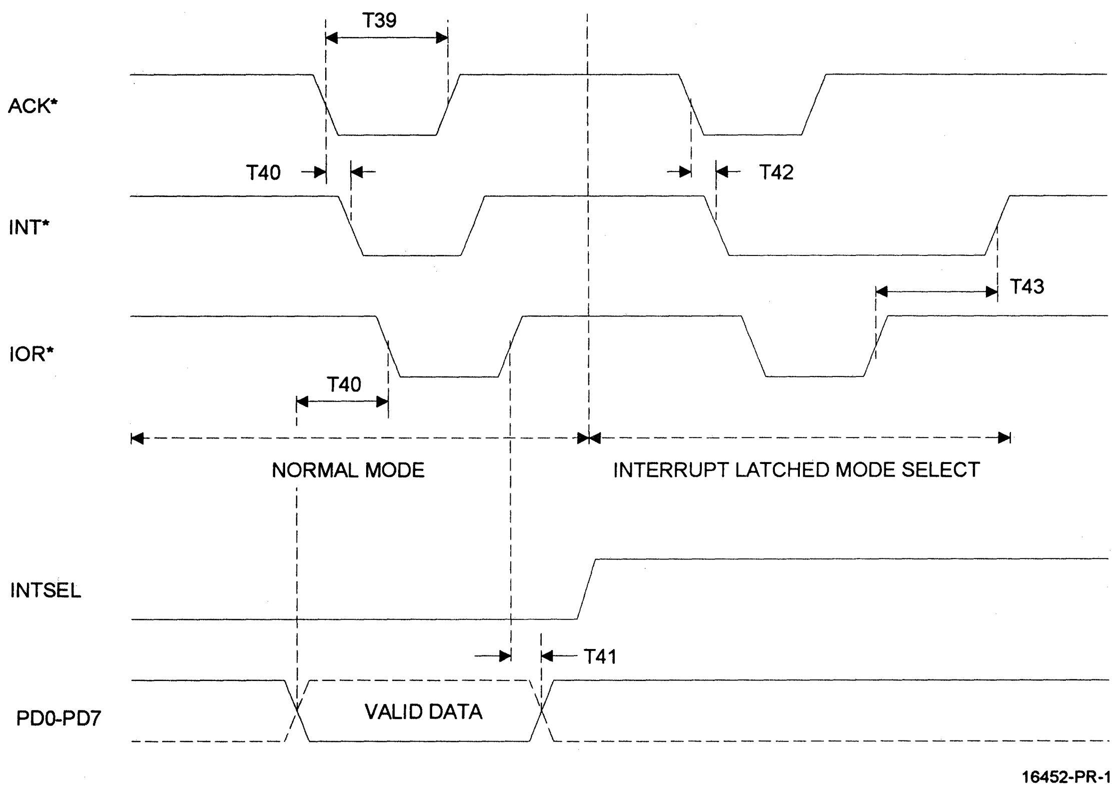
TRANSMIT TIMING



PARALLEL PORT GENERAL WRITE TIMING



GENERAL READ TIMING



UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT

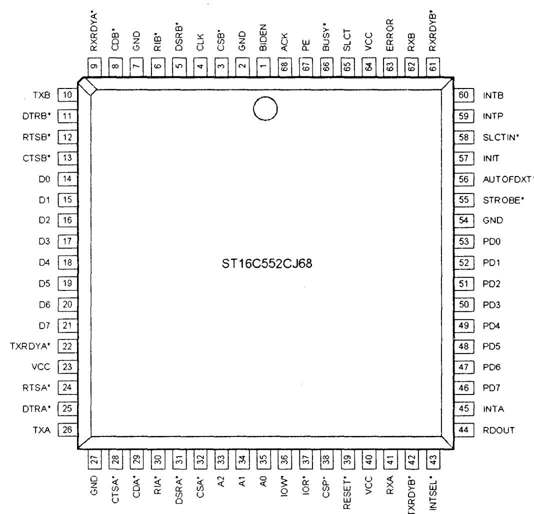
DESCRIPTION

The ST16C552 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

The ST16C552 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C552 provides internal loop-back capability for on board diagnostic testing.

The ST16C552 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



3

FEATURES

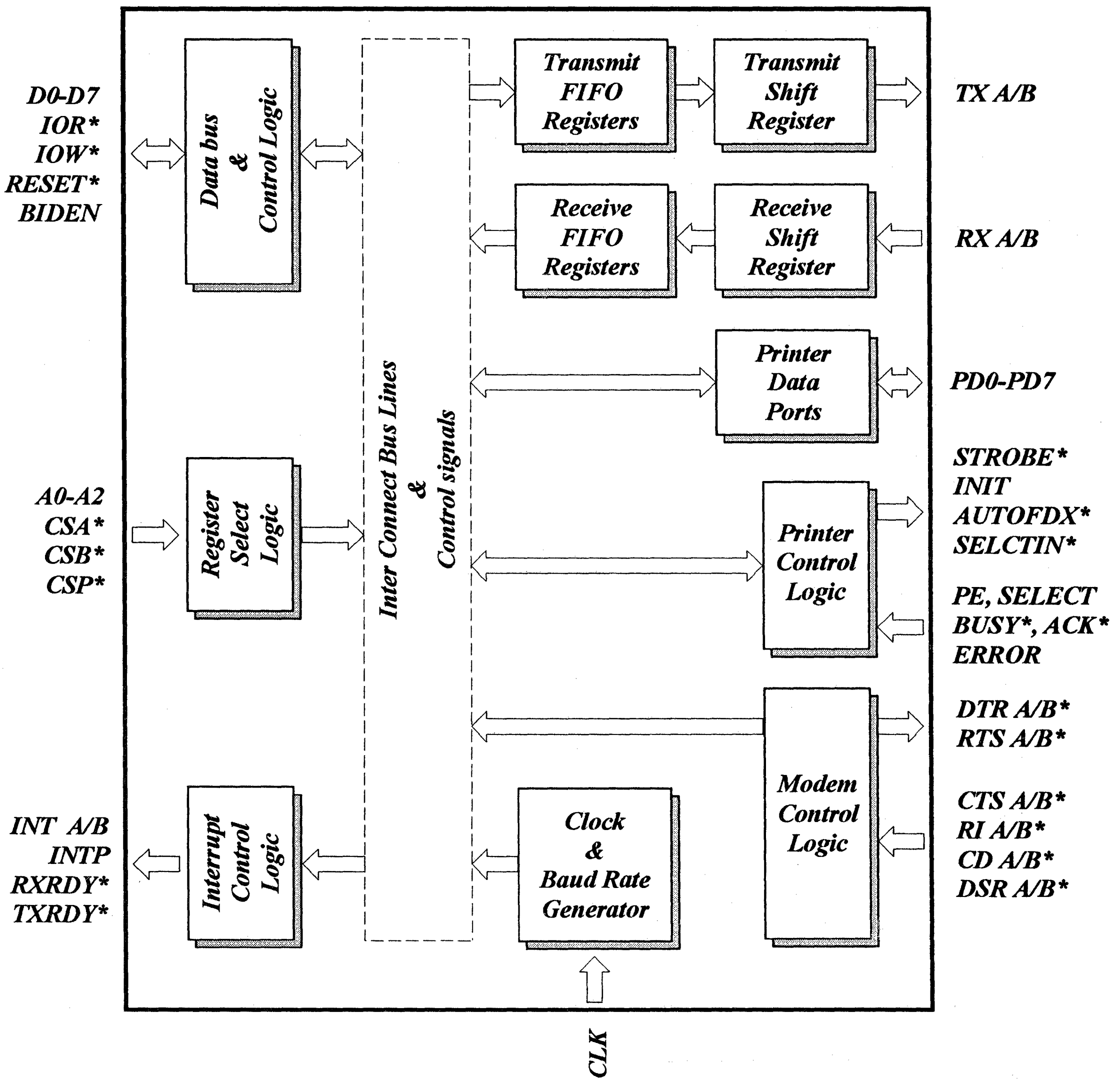
- Pin to pin and functional compatible to VL16C552, WD16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C552CJ68	PLCC	0° C to + 70° C
ST16C552IJ68	PLCC	-40° C to + 85° C

Rev. 1.0

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C552 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C552 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C552 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS* A/B	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR* A/B	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI* A/B	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD* A/B	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR* A/B	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS* A/B	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS* A/B	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY* A/B	22,42	O	Transmit ready A/B (active low). This pin goes high when the transmit FIFO of the ST16C552 is full. It can be used as

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			a single or multi-transfer.
RXRDY* A/B	9,61	O	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C552 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55*	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56*	I/O	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or initialize line printer (open drain active low). When this signal is low, it causes the printer to be initialized.
SLCTIN*	58*	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.
ERROR*	63*	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

Symbol	Pin	Signal Type	Pin Description
PE	67*	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68*	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,54 27	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

* Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C552 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C552 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

*RECEIVE TIME-OUT:
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C552 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C552 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C552 provides a temporary data register to store 8 bits of information for variable use.

ST16C552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

SIGNALS	RESET STATE
TX A/B	High
RTS* A/B	High
DTR* A/B	High
INT A/B, P	Three state mode
RXRDY* A/B	High
TXRDY* A/B	Low

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PRINTER PORT REGISTER DESCRIPTIONS

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C552 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	Low, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	X	Input mode

ST16C552 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
		0=Output 1=Input	0=INTP output disabled 1=INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1 * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

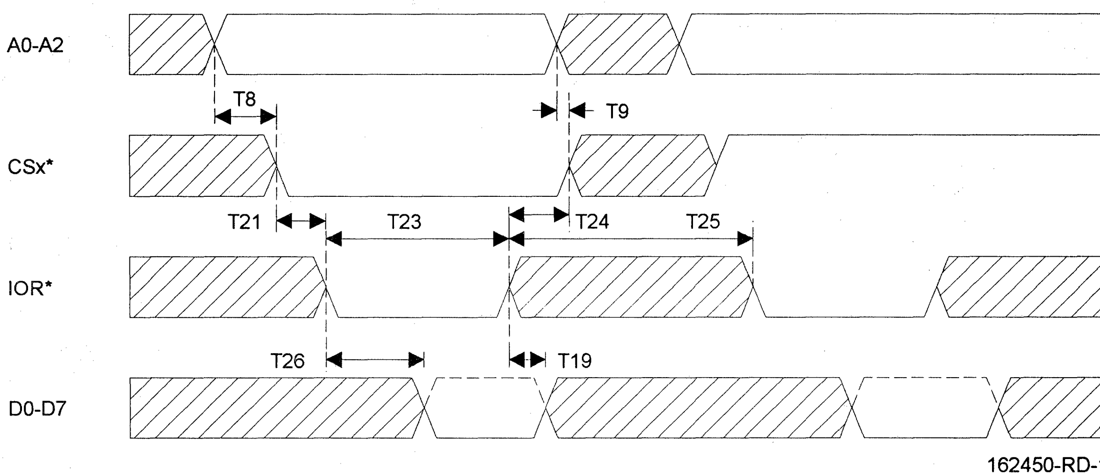
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=3.6 - 5.0 V ± 10% unless otherwise specified.

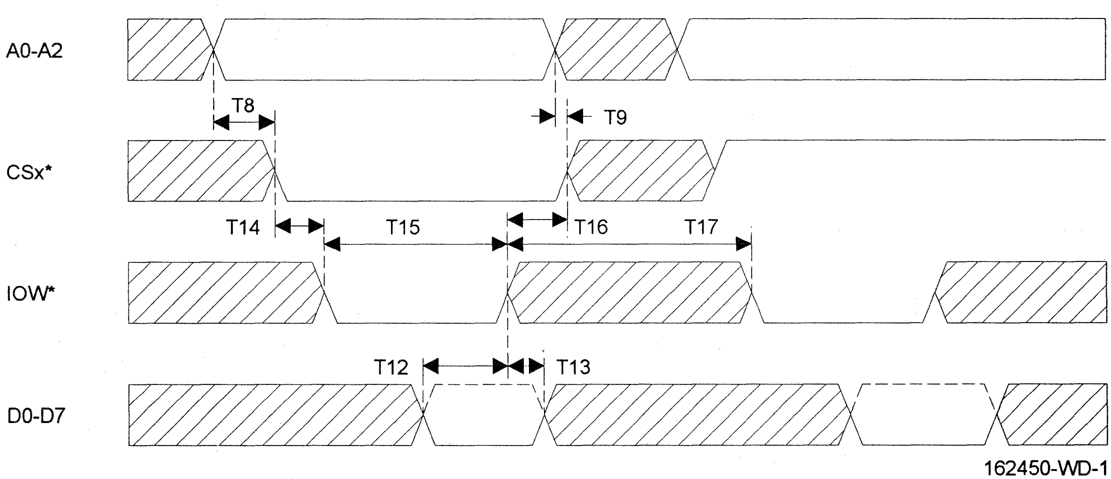
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current		2.5	4	mA	
I_{IL}	Input leakage			±10	μA	
I_{CL}	Clock leakage			±10	μA	
R_{IN}	Internal pull-up resistance	5		15	kΩ	*Marked pins

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IHCK}	Clock input high level	2.4		VCC	V	Vcc=3.0 V
V_{IL}	Input low level	-0.3		0.8	V	Vcc=3.0 V
V_{IH}	Input high level	2.0		VCC	V	Vcc=3.0 V
V_{OL}	Output low level			0.4	V	I_{OL}= 5 mA D7-D0 I_{OL}= 14 mA PD7-PD0 I_{OL}= 5 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT*
V_{OH}	Output high level	2.0			V	I_{OH}= -2.2 mA D7-D0 I_{OH}= -5 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT*
I_{CC}	Avg power supply current		1.4	1.6	mA	Vcc=3.0 V

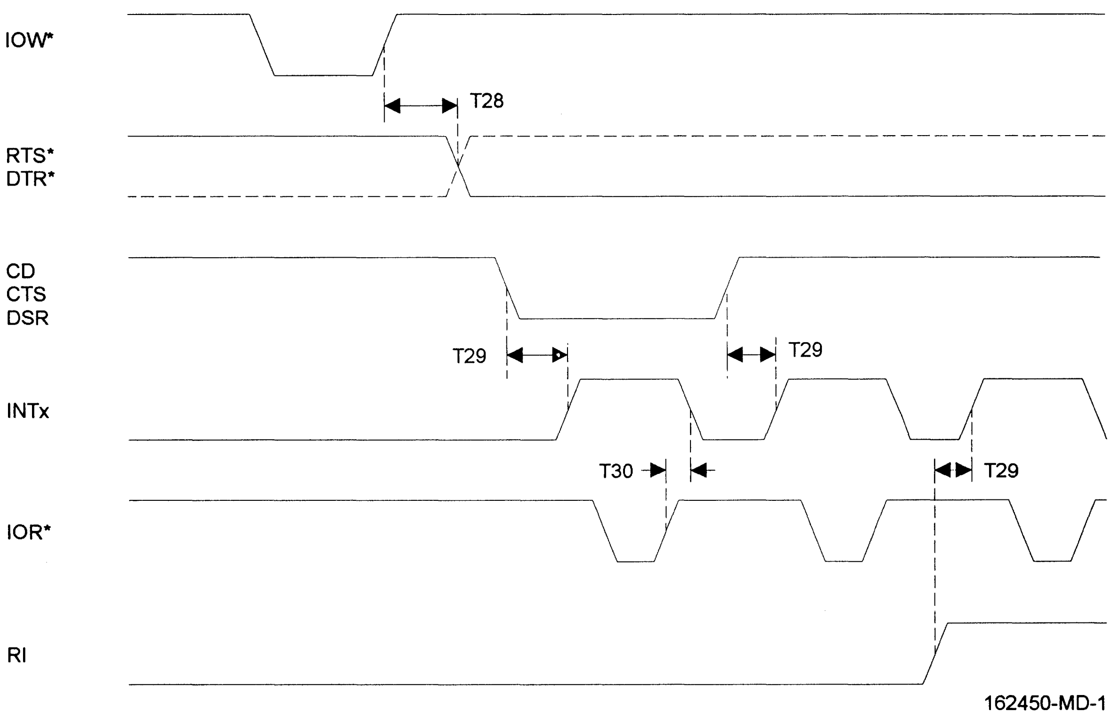
GENERAL READ TIMING



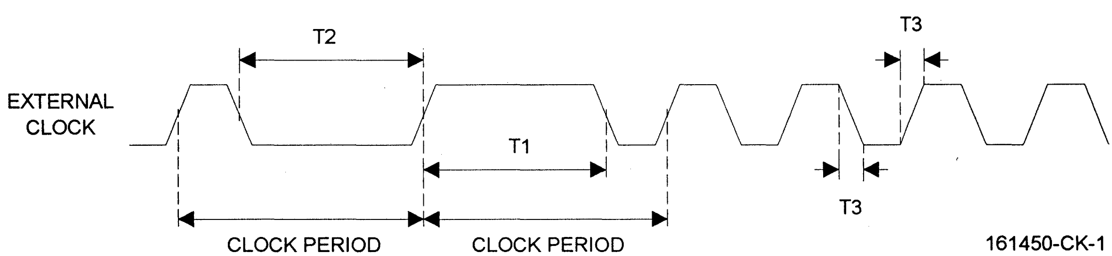
GENERAL WRITE TIMING



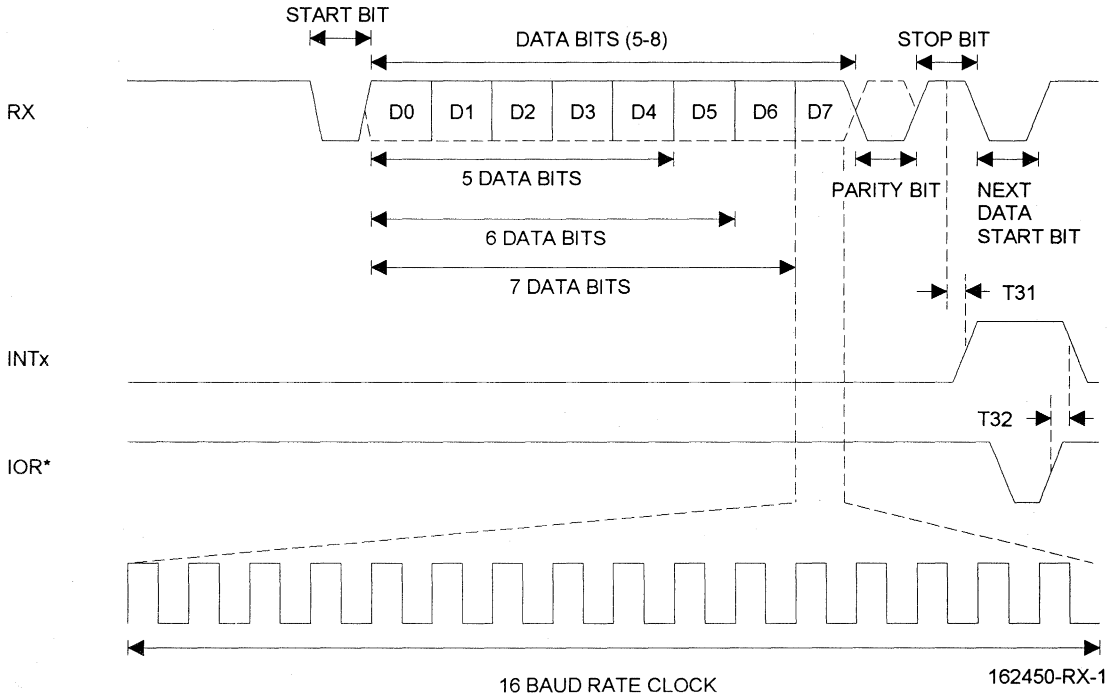
MODEM TIMING



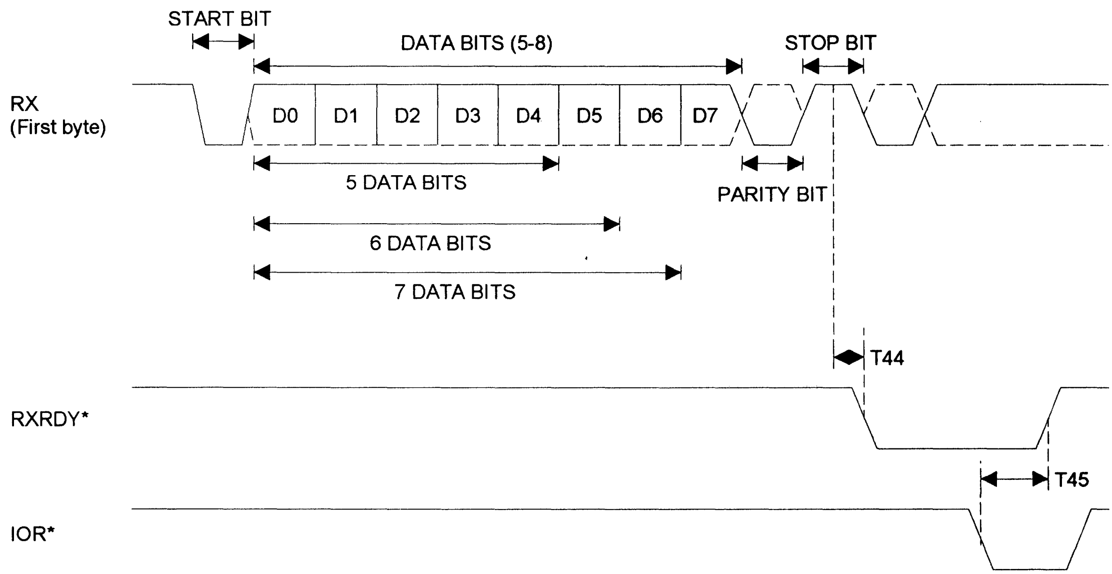
CLOCK TIMING



RECEIVE TIMING

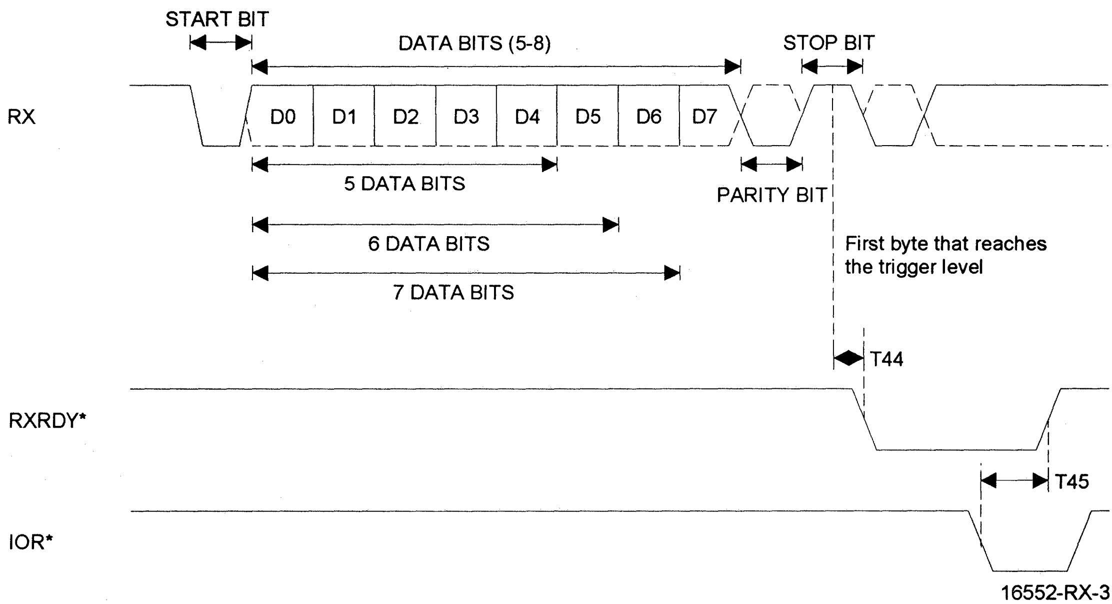


RXRDY TIMING FOR MODE "0"

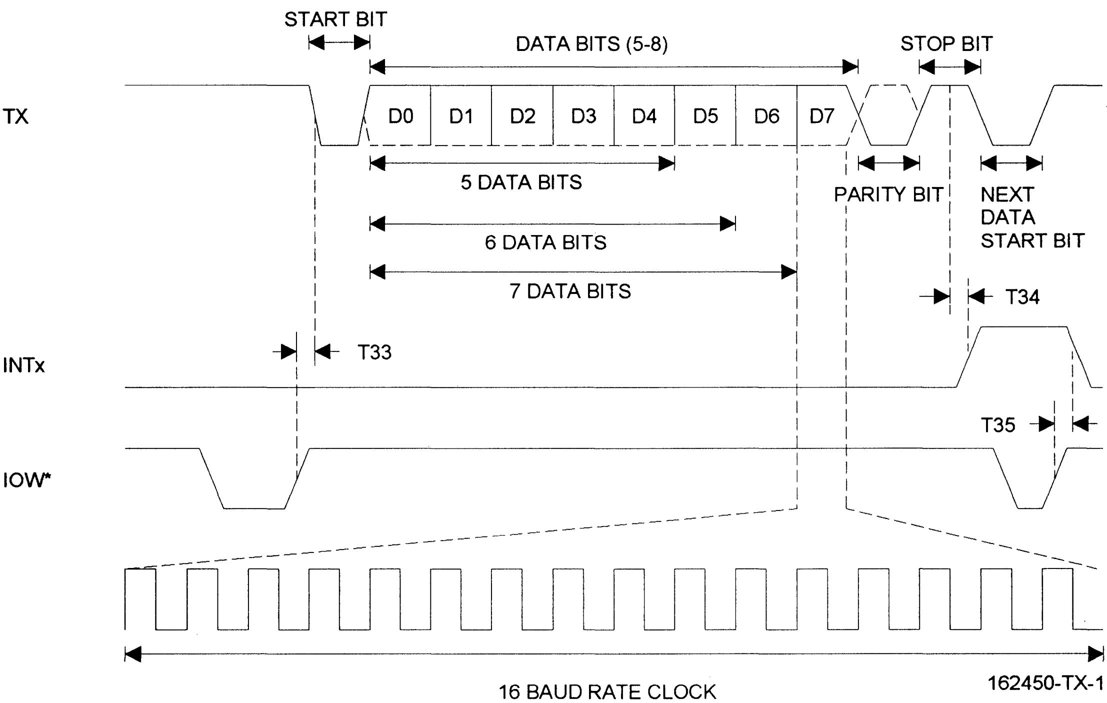


16552-RX-2

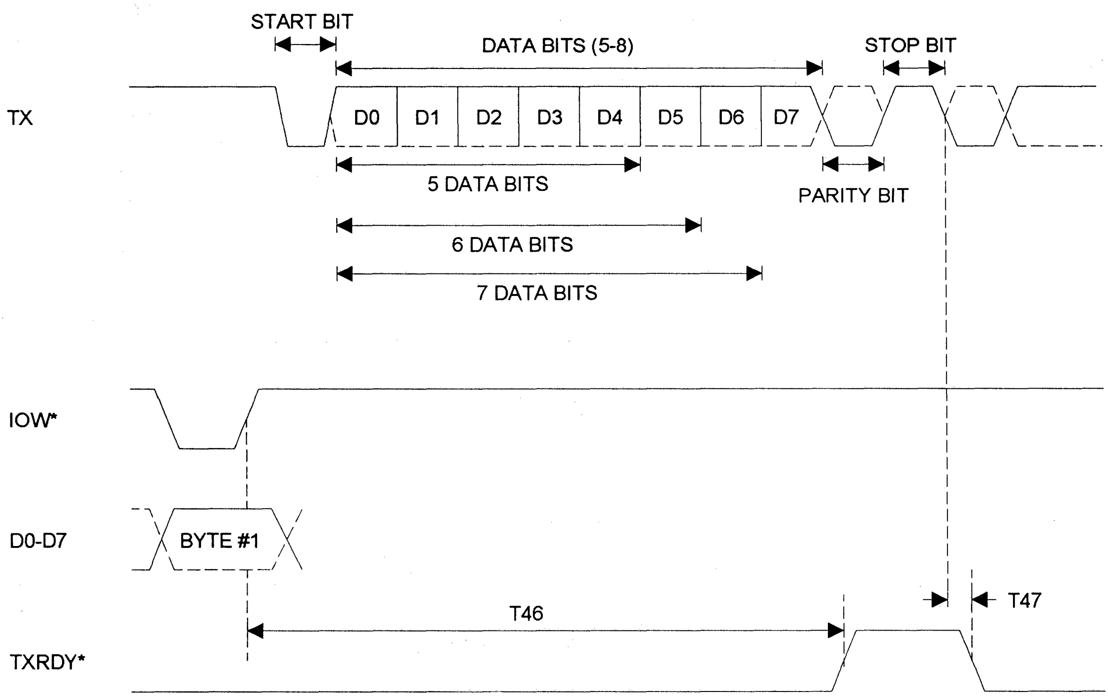
RXRDY TIMING FOR MODE "1"



TRANSMIT TIMING

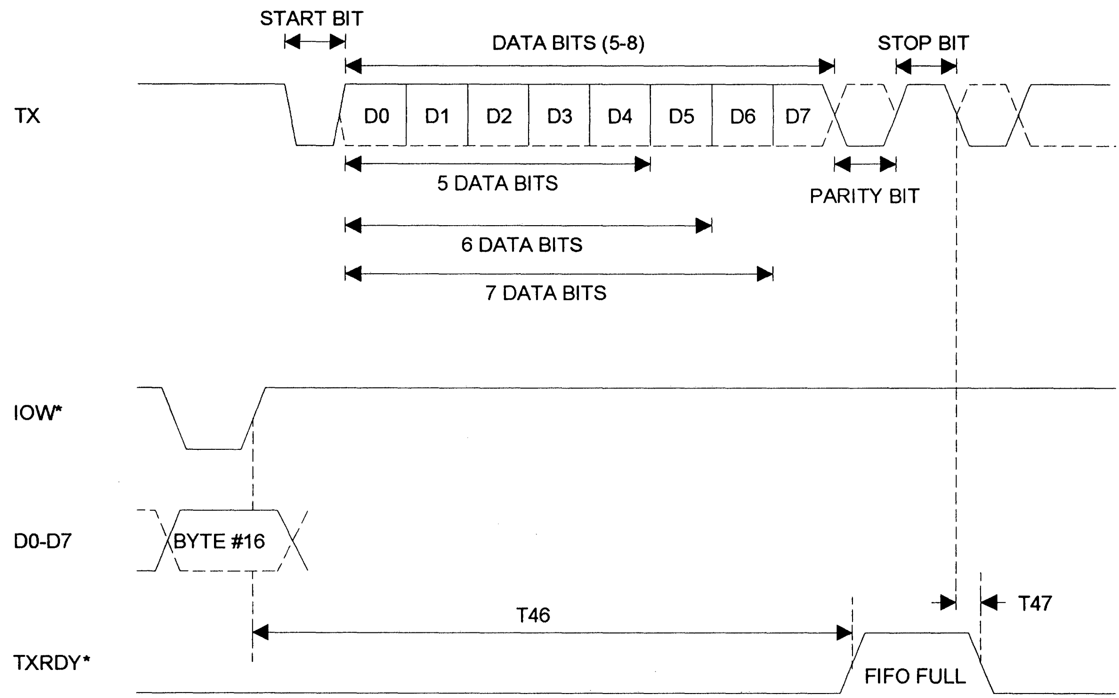


TXRDY TIMING FOR MODE "0"



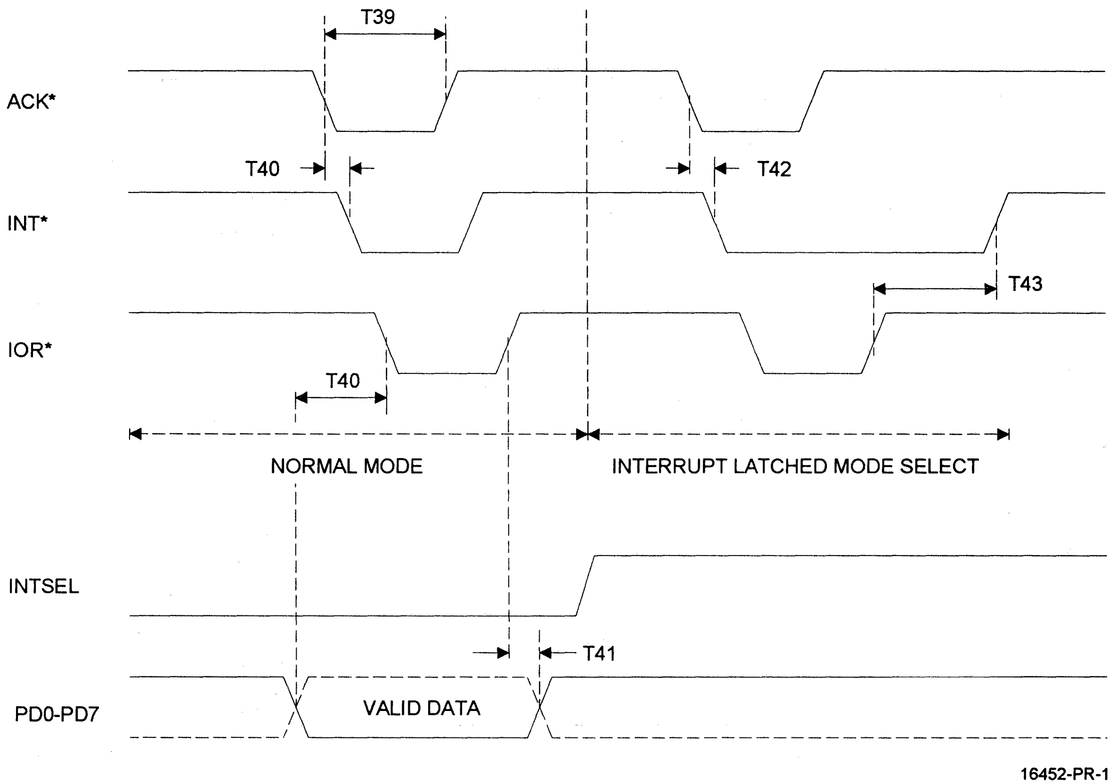
16552-TX-2

TXRDY TIMING FOR MODE "1"

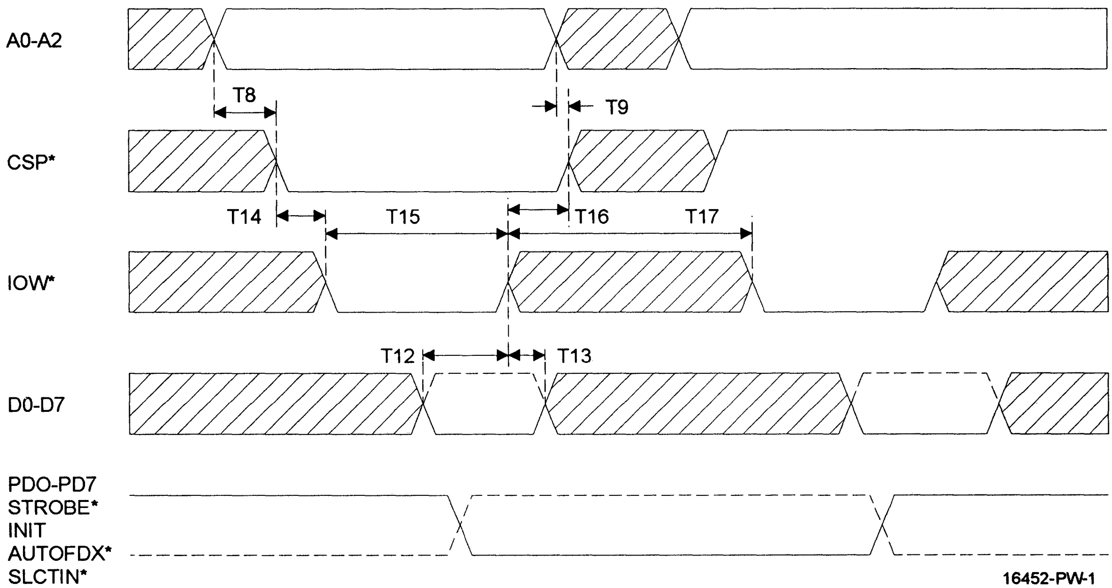


16552-TX-3

GENERAL READ TIMING



PARALLEL PORT GENERAL WRITE TIMING



STARTECH

An EXAR Company

ST16C553

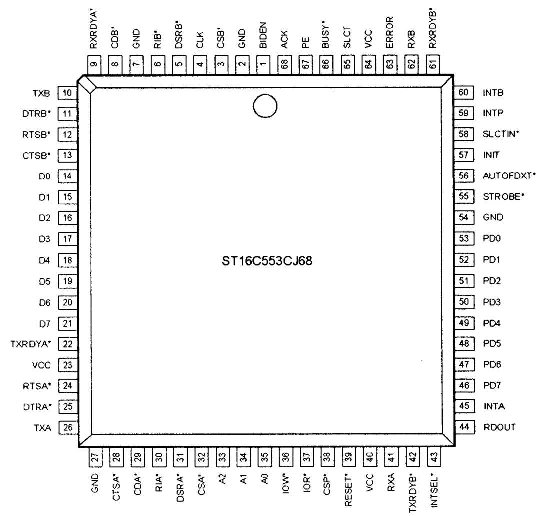
Printed August 7, 1995

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT WITH 83 BYTE FIFO

DESCRIPTION

The ST16C553 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bi-directional CENTRONICS type parallel printer port with 83 bytes of FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz. The ST16C553 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C553 provides internal loop-back capability for on board diagnostic testing. The ST16C553 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



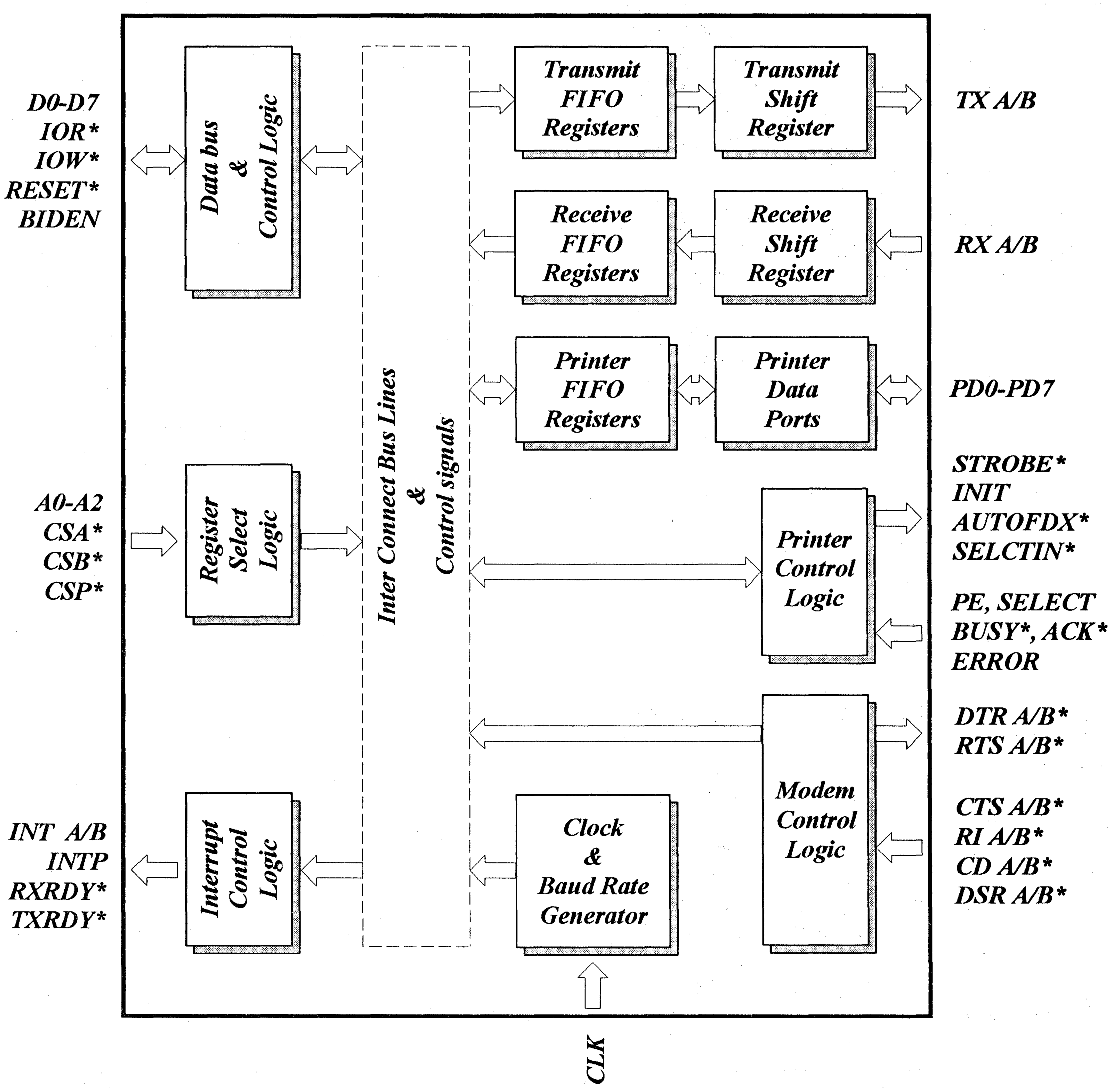
FEATURES

- Pin to pin and functional compatible to VL16C552, WD16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- 83 bytes of printer output FIFO
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C553CJ68	PLCC	0° C to + 70° C
ST16C553IJ68	PLCC	-40° C to + 85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C553 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C553 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C553 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset (active low). A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS* A/B	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR* A/B	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI* A/B	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD* A/B	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR* A/B	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C553 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS* A/B	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C553 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS* A/B	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY* A/B	22,42	O	Transmit ready A/B (active low). This pin goes high when the transmit FIFO of the ST16C553 is full. It can be used as

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			a single or multi-transfer.
RXRDY* A/B	9,61	O	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C553 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55*	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56*	I/O	General purpose I/O or automatic line feed (open drain active low). When this pin this signal is low, the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	58*	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.
ERROR*	63*	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
PE	67*	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68*	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,54	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

* Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C553 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register interrupt	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C553 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C553 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C553 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2_{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C553 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C553 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C553 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C553 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C553 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C553 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C553 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C553 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C553 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-

back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C553 provides a temporary data register to store 8 bits of information for variable use.

ST16C553 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
AFR	AFR BIT 0-7=0

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

SIGNALS	RESET STATE
TX A/B	High
RTS* A/B	High
DTR* A/B	High
INT A/B, P	Three state mode
RXRDY* A/B	High
TXRDY* A/B	Low

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYTE COUNT REGISTER

* Reading the status register will reset the INTP output.

PRINTER FUNCTIONAL DESCRIPTION

The ST16C553 parallel port is designed to operate as a normal CENTRONICS printer interface. The port contains 83 byte FIFO that may be enabled via bit-7 of the Alternate Function Register (AFR). After reset, the FIFO is disabled and the part will function identical to the ST16C552. Once the FIFO is enabled via AFR bit-7, the port will enter FIFO mode after the first byte of data is strobed to the printer and the printer responds with either an ACK* or BUSY signal.

The ST16C553 will remain in FIFO mode until the part is reset or INIT is brought low. While in FIFO mode, data transfer to the printer will be controlled by the printer without any user intervention. The printer port also contains a FIFO byte counter that maintains a count of the number of bytes remaining in the FIFO. The FIFO and the FIFO byte counter are cleared by a reset or by a change of state of the INIT pin. All FIFO related timing is derived from the clock input to pin 4 of the part.

A special parallel port write / read mode is activated when INIT is held low, either by writing a "0" to Control Register bit-2 or by forcing the INIT pin low. In this mode the FIFO read pointer is advanced by reading the parallel port instead of the ACK* or BUSY signals. The STROBE* output is forced high. This allows the user to perform write to parallel port and read from parallel port operations without strobing data to the printer.

Following an INIT, the parallel port will not be in the FIFO mode. Control Register bit-0 is used as the STROBE*, Status Register bit-7 is the inverse of the BUSY signal, and INTP* is derived from ACK*. The transition into FIFO mode will occur after the first STROBE* is generated and the printer responds with either an ACK* or BUSY. In FIFO mode, STROBE* is generated automatically and writing to Control Register bit-0 has no effect on STROBE*. Alternate Function Register bit 0-2 are used to control the delay and width of STROBE*. Handshaking between the printer and the ST16C553 may be controlled by bit-3 of the Alternate Function Register. Setting this bit to a "1" will result in the use of BUSY instead of ACK* for FIFO reading and interrupt control. INTP* will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read to Fifo Byte Count Register (FBCR) should only be performed minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL* pin. If this pin is tied high, a latched interrupt will result. In this mode, INTP* will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL* pin is tied low, INTP* will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL* pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INTP* pin may be inverted by setting Alternate Function Register bit-6 high.

The ST16C553 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INTP* output can be selected as FIFO full or FIFO empty interrupt.

PRINTER PORT REGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
This bit is set to “1” normally except when interrupt is selected as FIFO empty via AFR.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to “0” at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to “1”.

SR BIT-3:
ERROR input state.
0= ERROR input is in low state
1= ERROR input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY or FIFO full/ FIFO empty signal.

ST16C552 mode (FIFO is not enabled).
0= BUSY input is in high state
1= BUSY input is in low state

FIFO is enabled.
0= FIFO is full
1= One or more empty locations in FIFO

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled (three state mode)
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INTP* and change interrupt functions.

AFR BIT 0-2:
Timing select.
The STROBE* delay and width can be controlled by these bits.

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
1	0	0	3	2
1	0	1	5	4
1	1	0	5	4
1	1	1	9	8
0	0	0	6	4
0	0	1	10	8
0	1	0	10	8
0	1	1	18	16

AFR BIT-3:
Interrupt source.
0= ACK* input pin is selected as printer handshaking source
1= BUSY input pin is selected as printer handshaking source

AFR BIT 4-5:
Interrupt type. State of the INTP* output pin can be selected for one of the following options.

Bit-5	Bit-4	INTP* output	SR bit-0	SR bit-6
0	0	Normal mode	1	BUSY*
0	1	FIFO empty	1	FIFO empty
1	0	FIFO full	1	FIFO full
1	1	FIFO empty	0	FIFO empty

AFR BIT-6:
INTP* output polarity.
0= Normal. INTP* output follows the ACK* input
1= Inverted INTP* output

AFR BIT-7:
FIFO enable / disable function.
0= FIFO is disabled(default mode). The ST16C552 compatible mode.
1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR)

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:
FIFO byte count. Number of characters left in FIFO.

FBCR BIT-7:
FIFO state.
0= FIFO is enabled
1= FIFO is disabled

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C553 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	Low, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	X	Input mode

ST16C553 PRINTER PORT REGISTER CONFIGURATIONS

A2 A1 A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
X 0 0	PR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X 0 1	STR	BUSY*/ Alternate function	ACK	PE	SLCT	ERROR	IRQ	1	1
X 0 1	I/O	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
X 1 0	COM	1	1	1	IRQ state	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
X 1 0	CON	1	1	I/O select	IRQ mask	SLCTIN*	INIT	AUTO-FDXT	STROBE*
X 1 1	AFR	FIFO enable	INTP* polarity	IRQ type bit-1	IRQ type bit-0	INTP* source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
X 1 1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1 Rclk	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2_{16}-1		

Note 1 * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

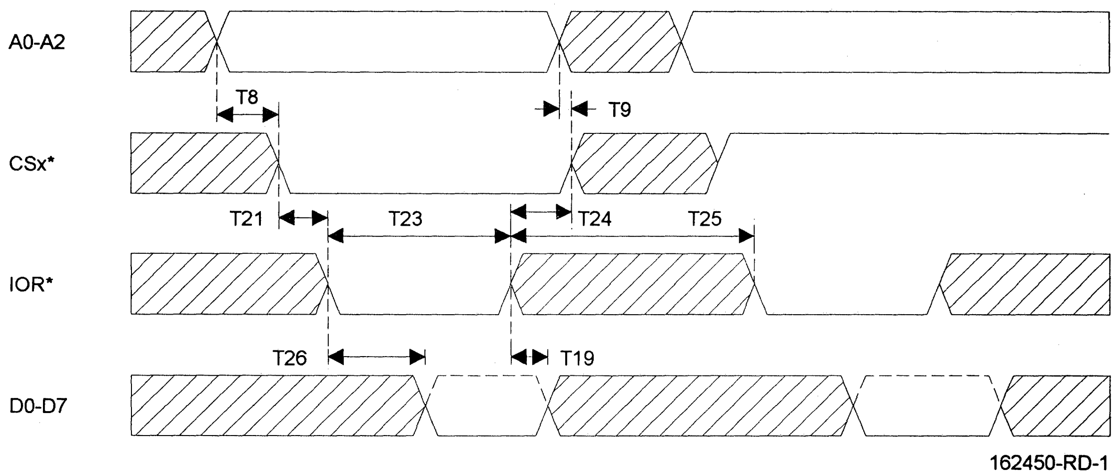
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

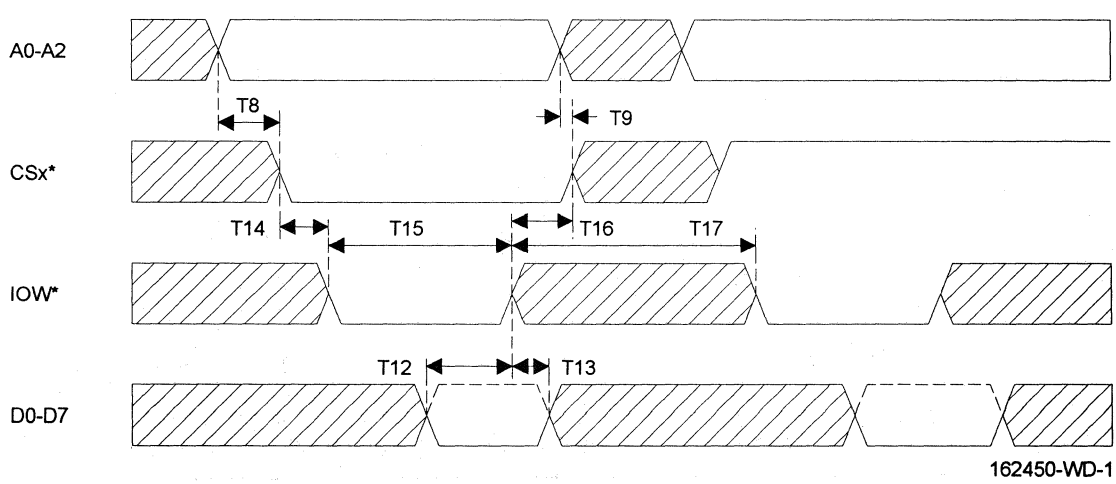
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 15mA PD7-PD0 I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -150 µA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg. power supply current		12	20	mA	
I_{IL}	Input leakage			±10	µA	Exc. pins 63, 65, 66, 67, 68
R_{IN}	Input pullup resistance			11	kΩ	Pins 63, 65, 66, 67, 68
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	4		15	kΩ	*Marked pins

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

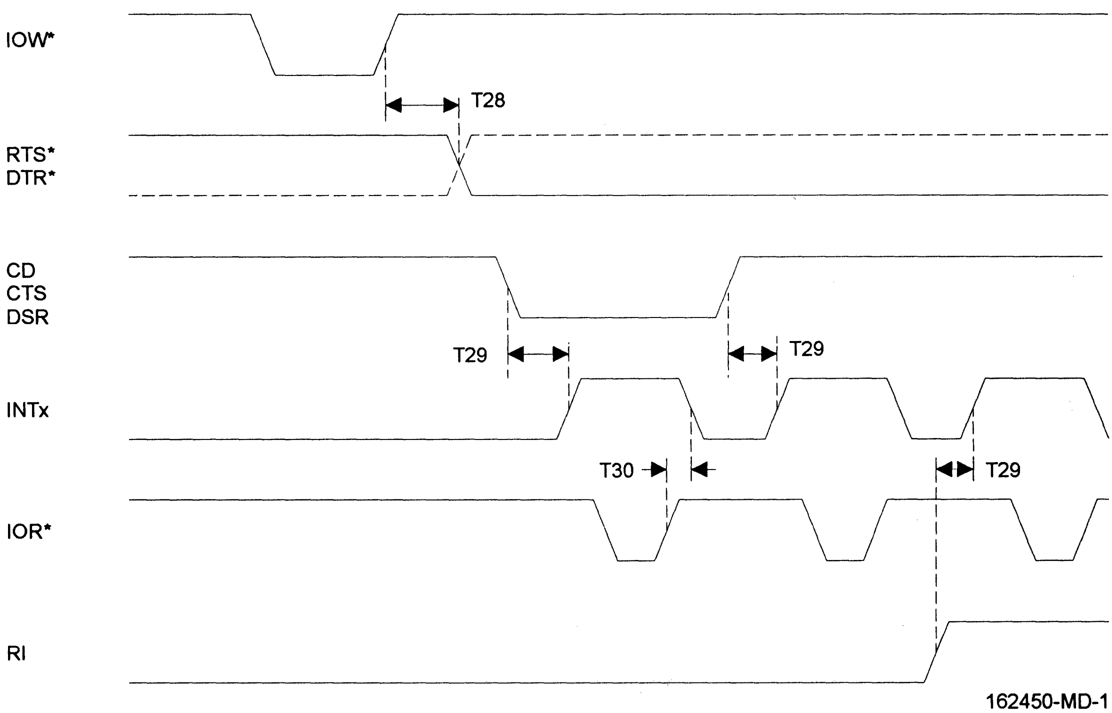
GENERAL READ TIMING



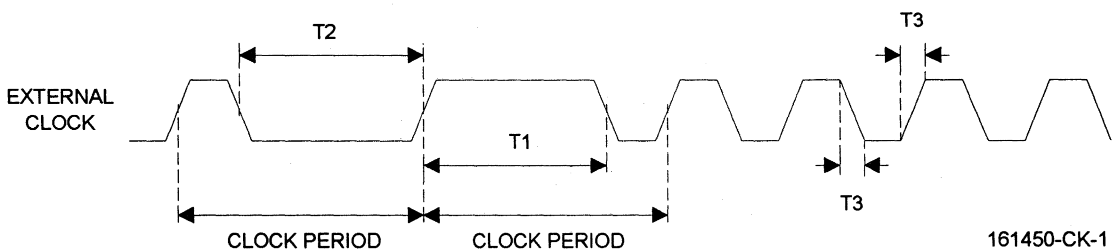
GENERAL WRITE TIMING



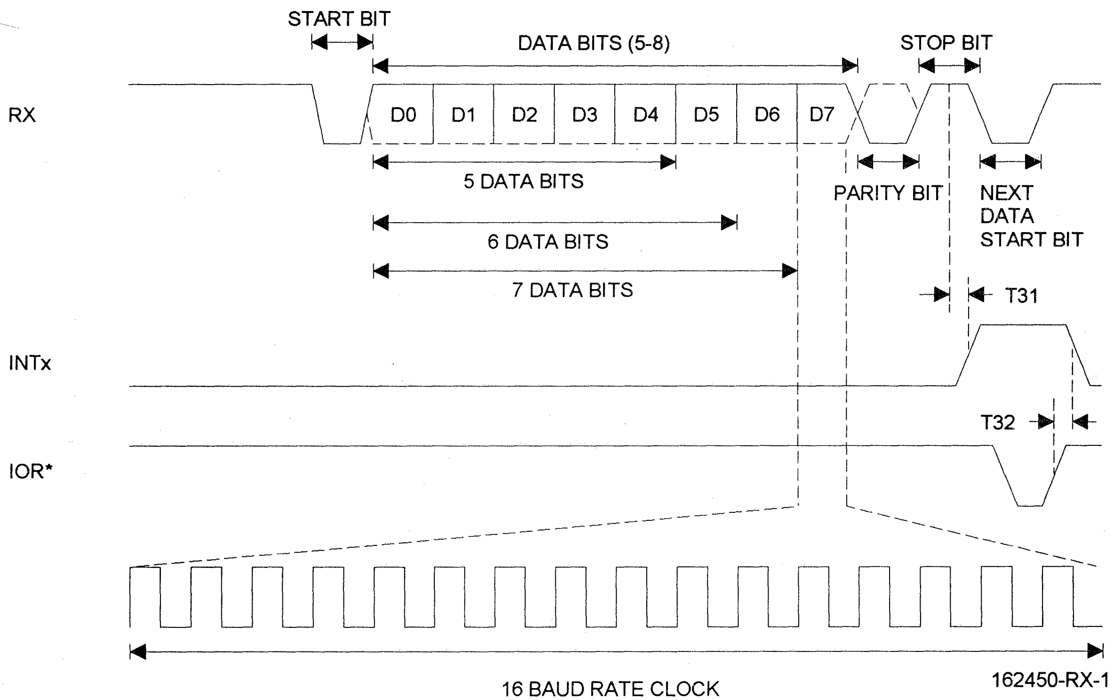
MODEM TIMING



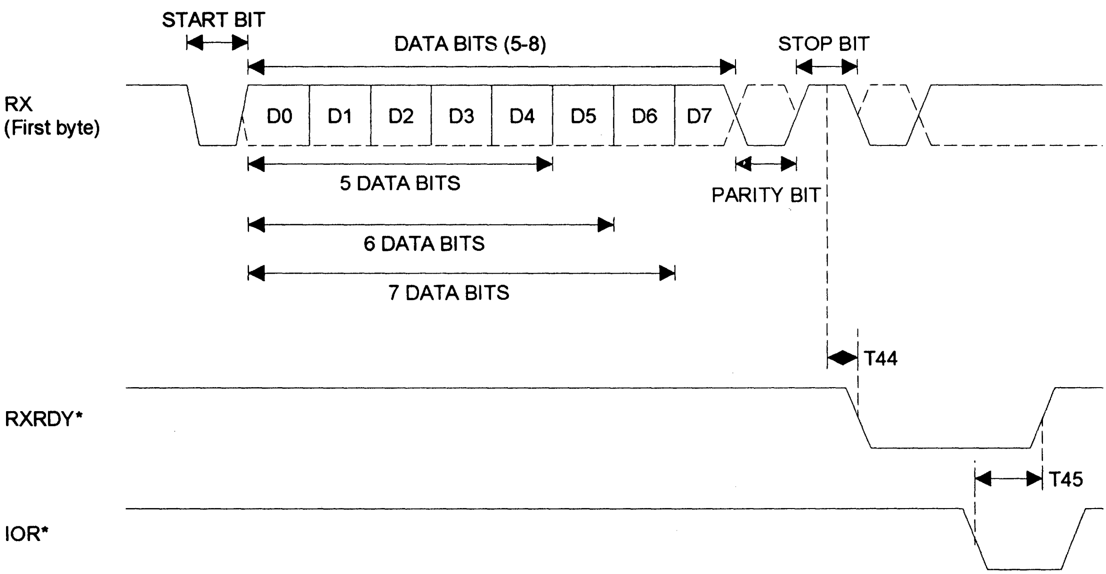
CLOCK TIMING



RECEIVE TIMING

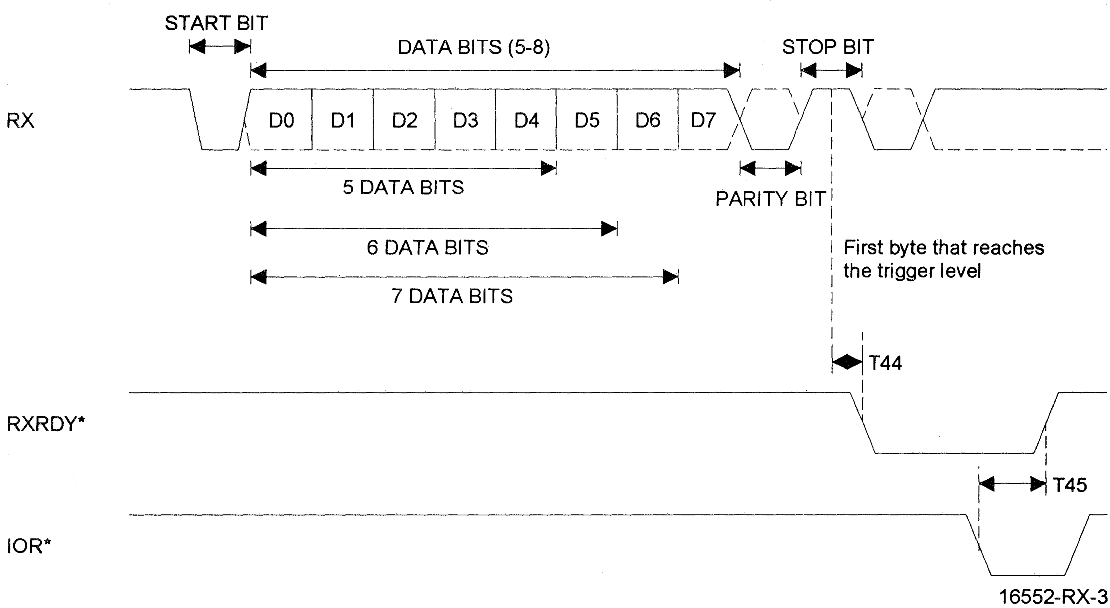


RXRDY TIMING FOR MODE "0"

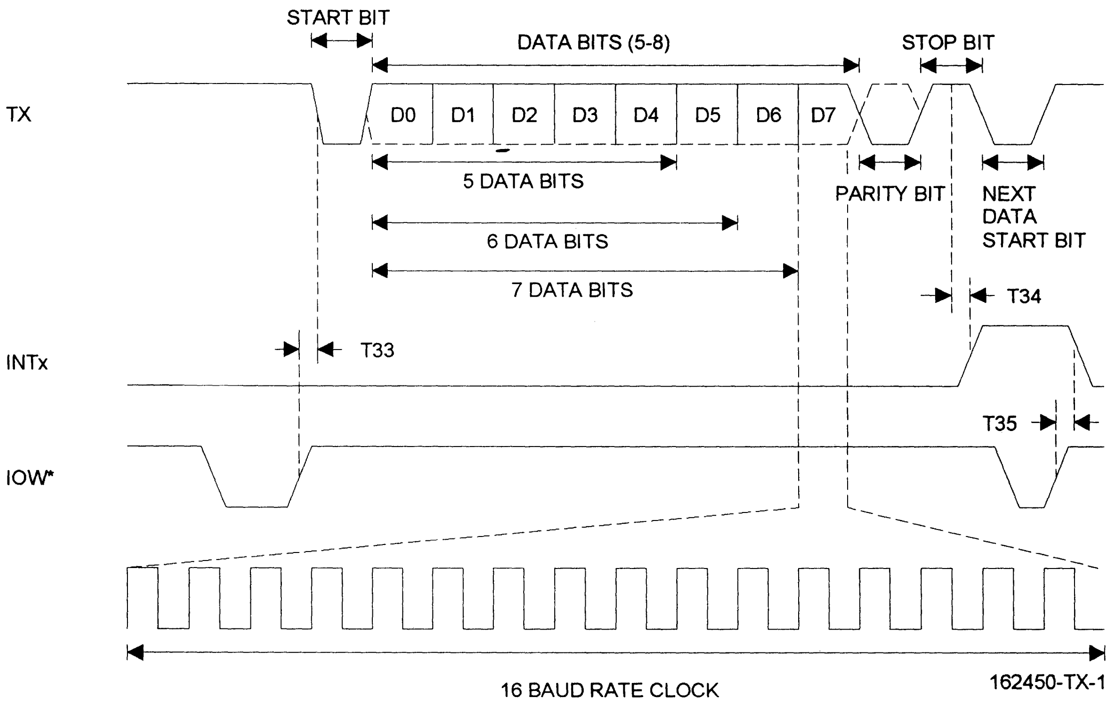


16552-RX-2

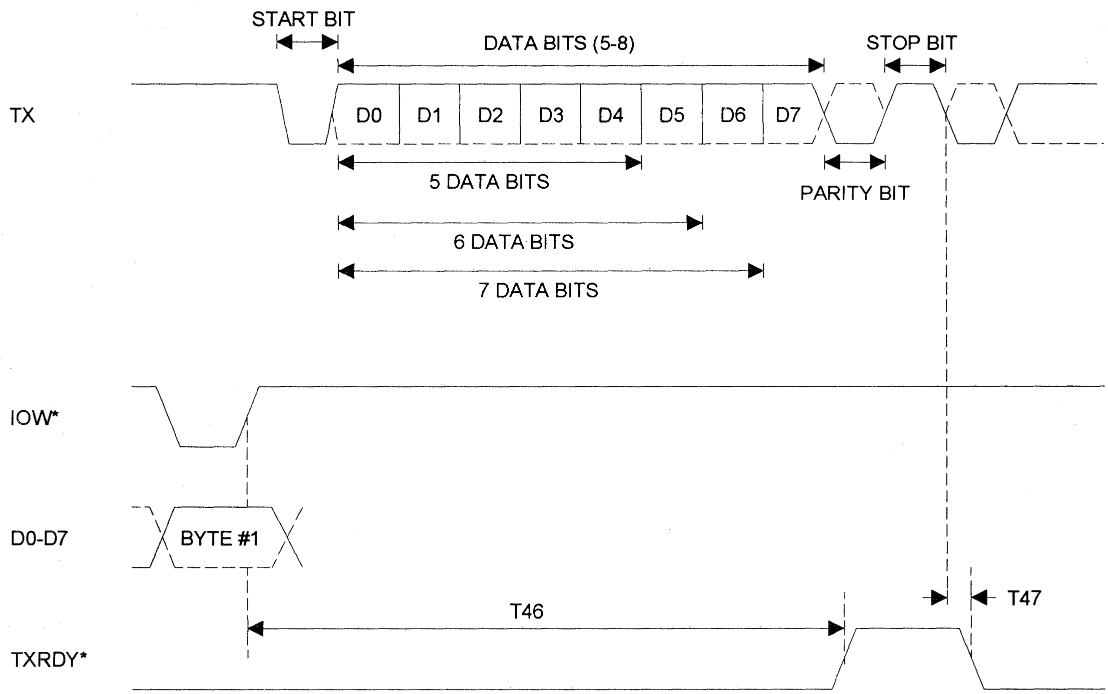
RXRDY TIMING FOR MODE "1"



TRANSMIT TIMING

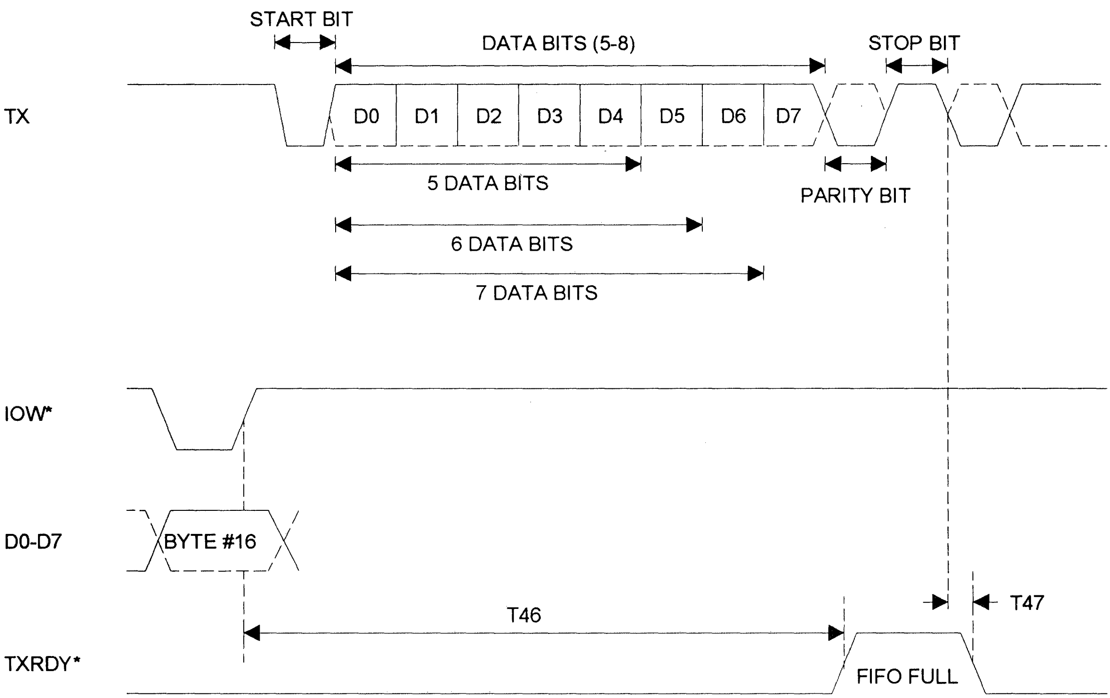


TXRDY TIMING FOR MODE "0"



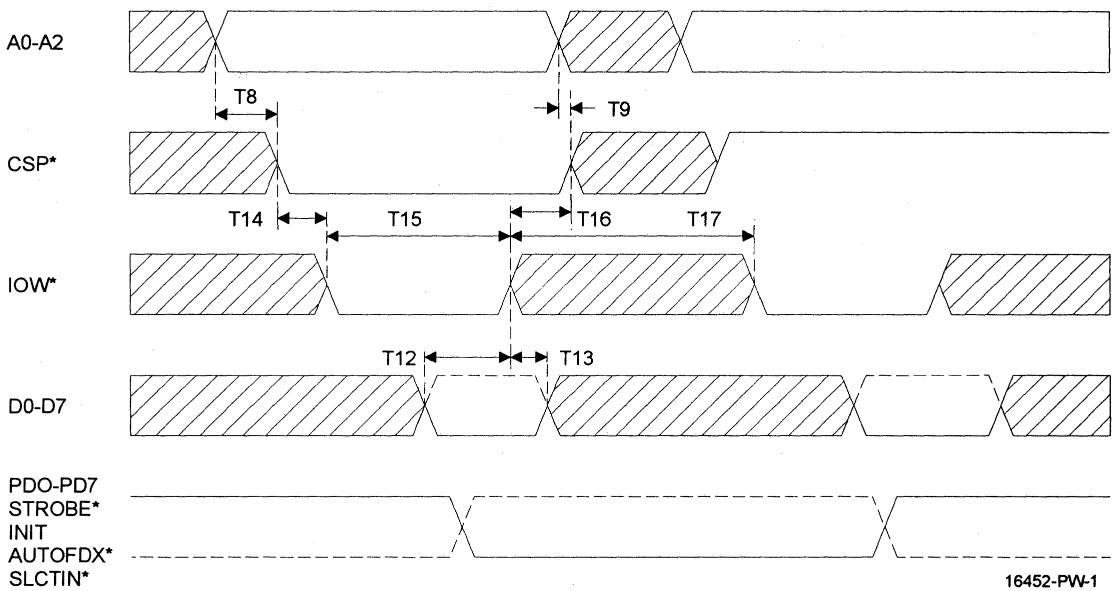
16552-TX-2

TXRDY TIMING FOR MODE "1"

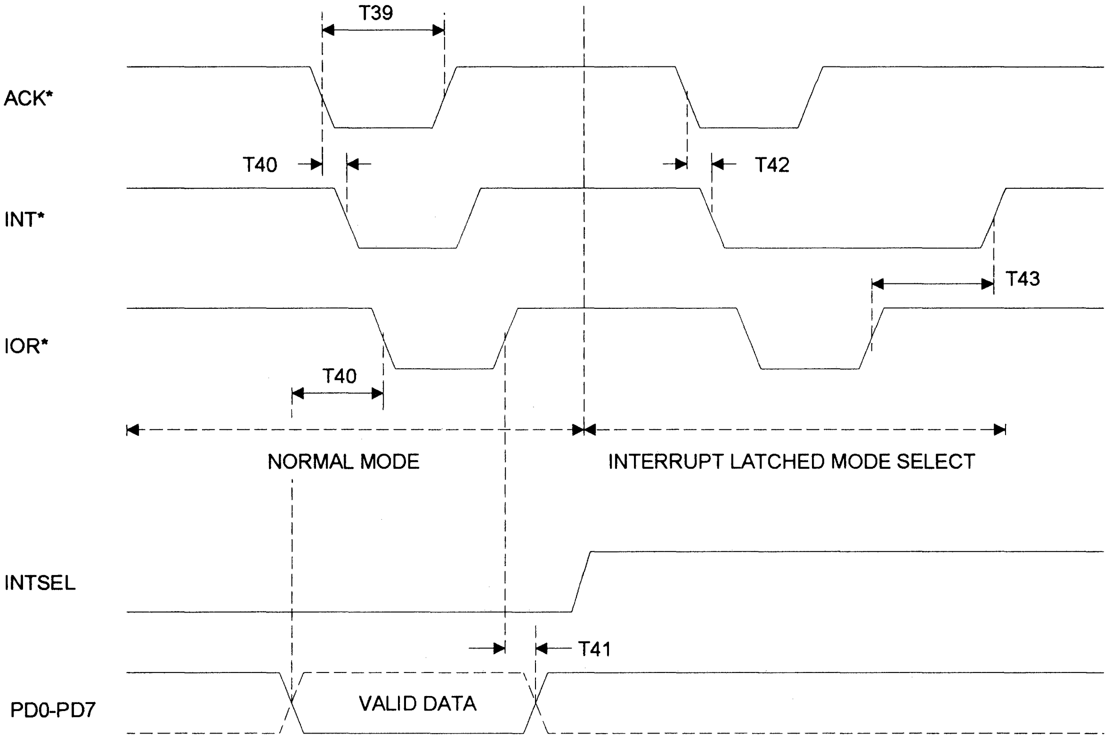


16552-TX-3

PARALLEL PORT GENERAL WRITE TIMING

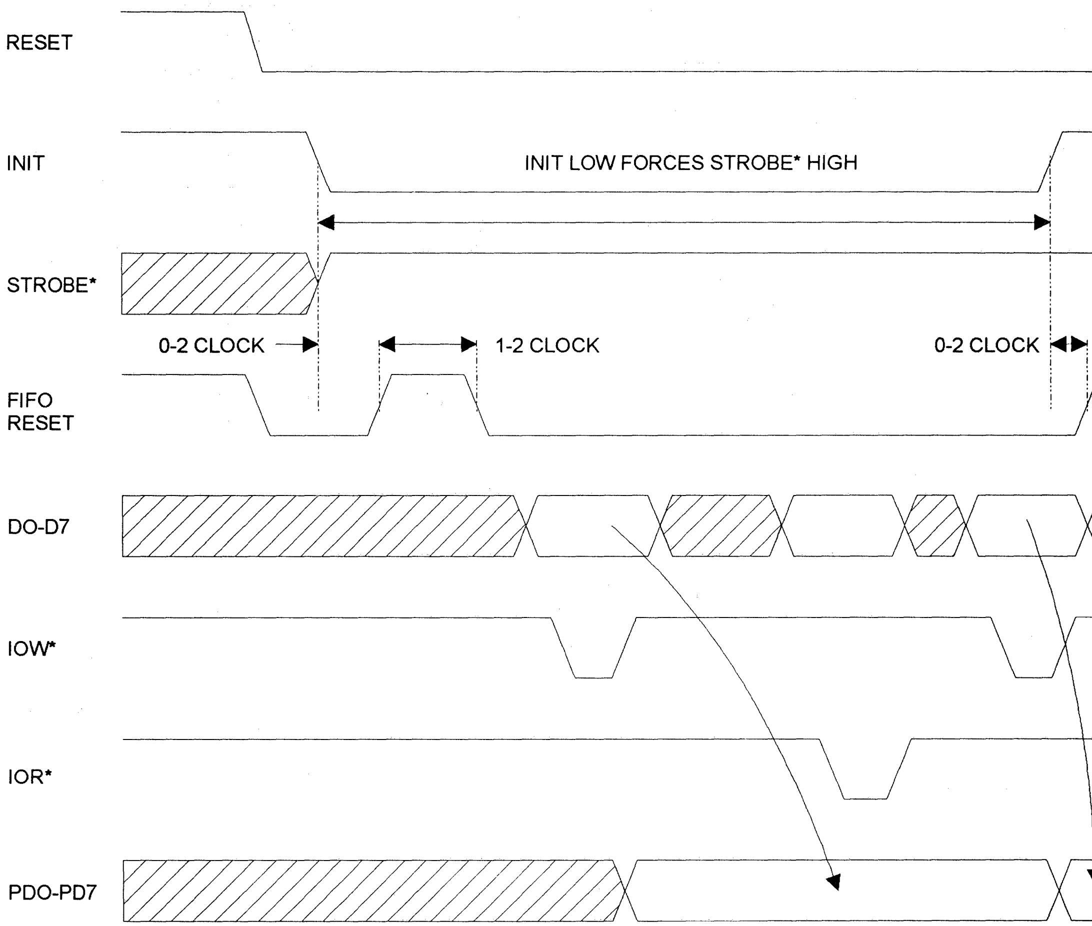


GENERAL READ TIMING



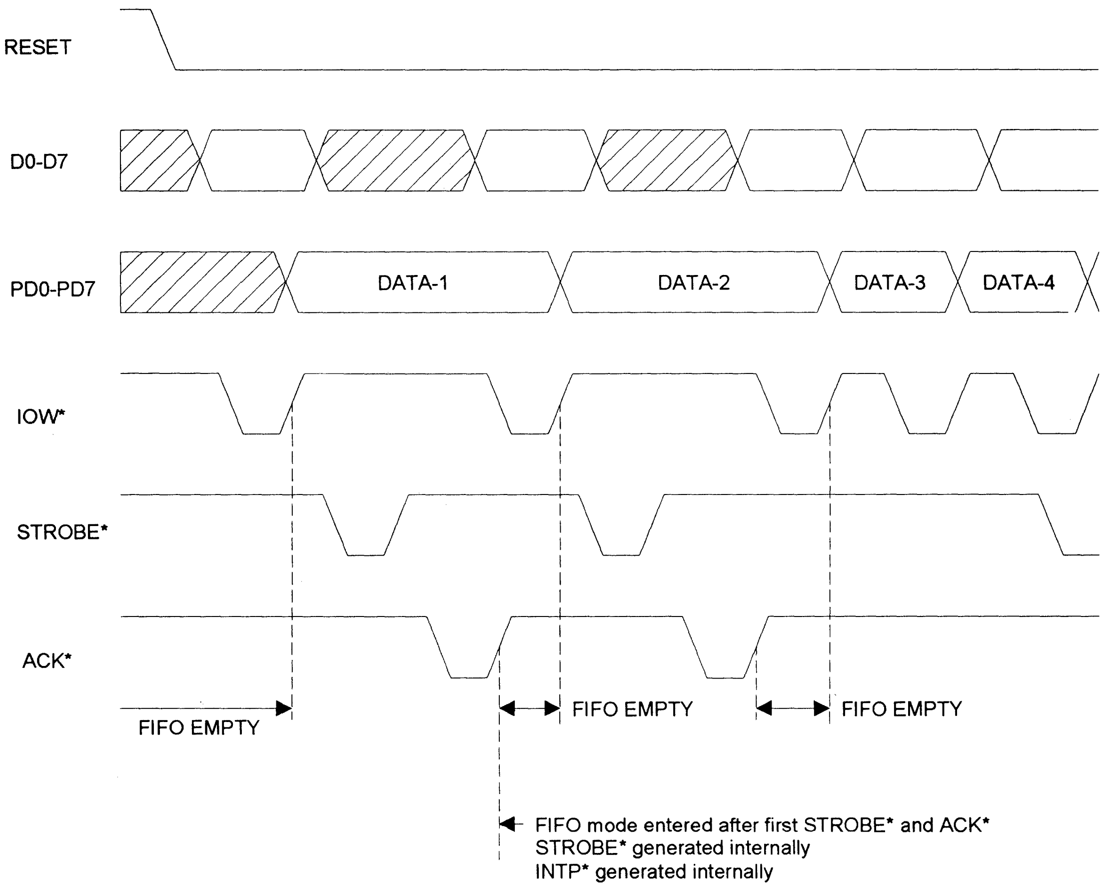
16452-PR-1

PRINTER SPECIAL MODE



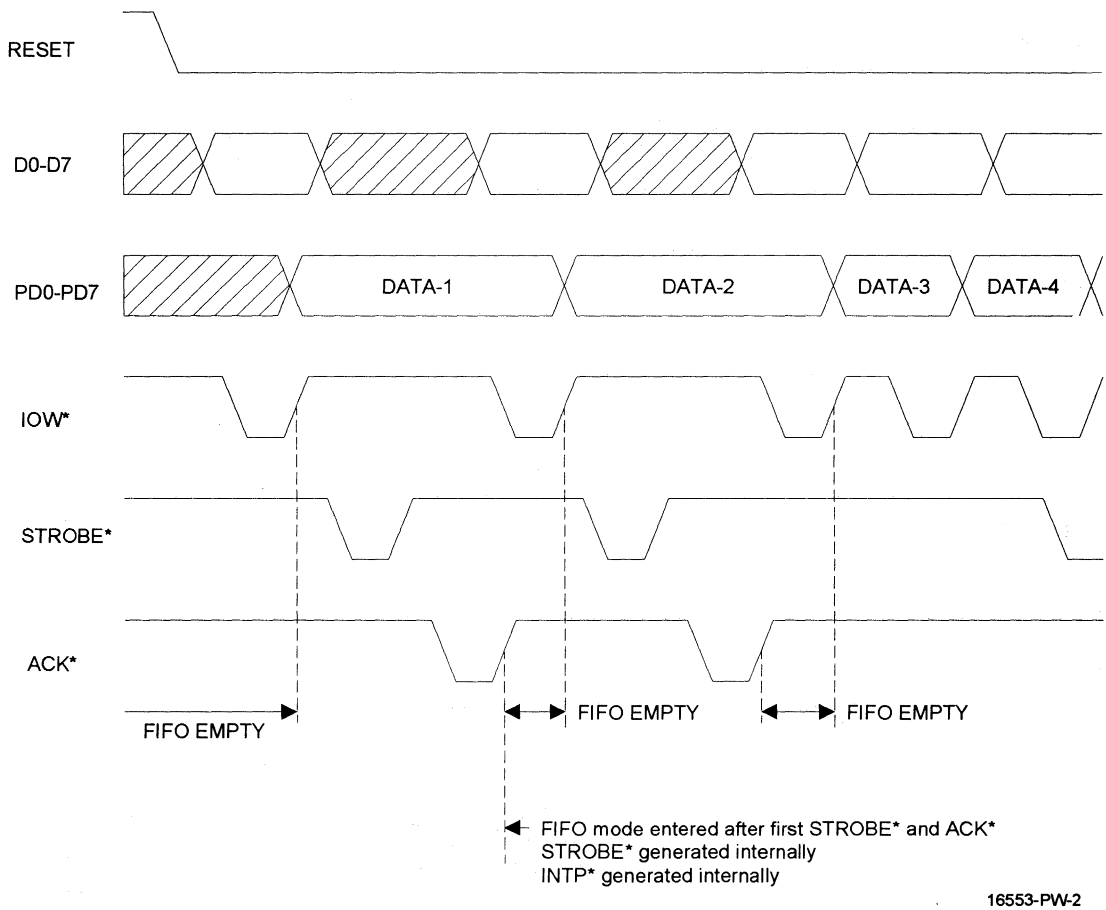
16553-PW-1

PRINTER AUTO FIFO OPERATION

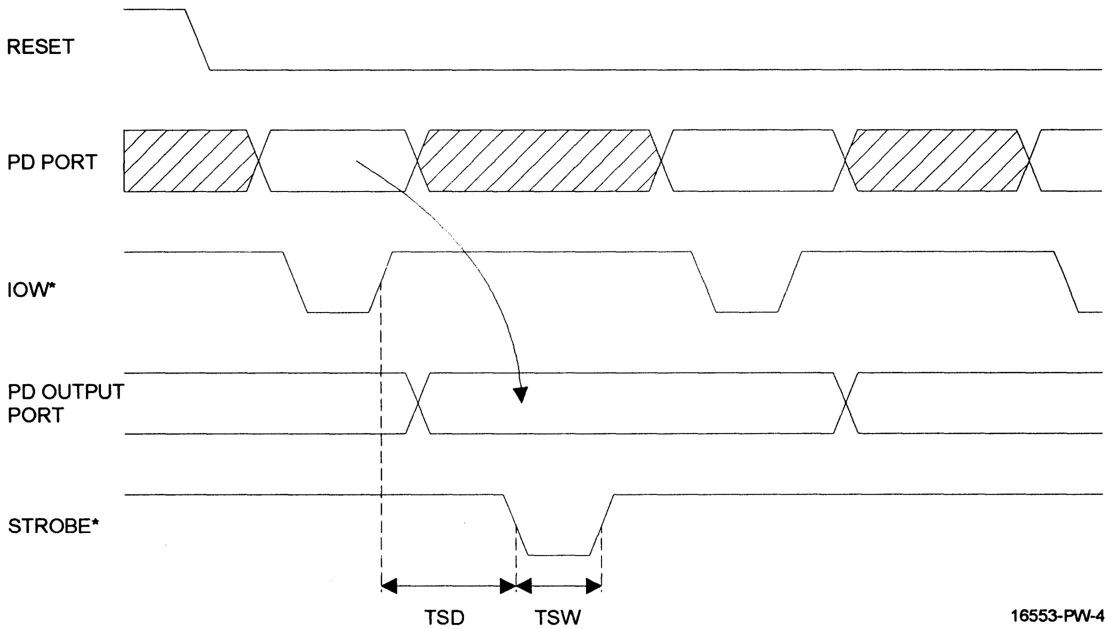


16553-PW-2

PRINTER AUTO FIFO OPERATION



PRINTER FIFO, WITH ONE BYTE IN THE FIFO



PERIPHERALS 4

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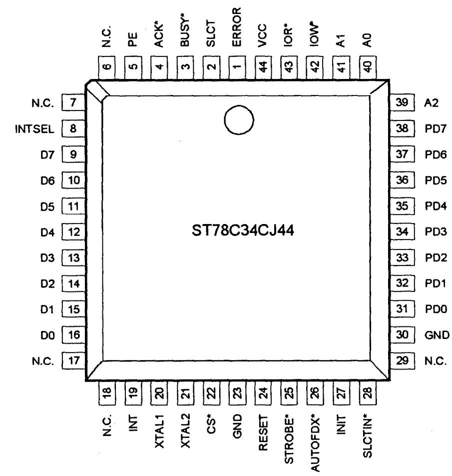
GENERAL PURPOSE PARALLEL PRINTER PORT WITH 83 BYTE FIFO

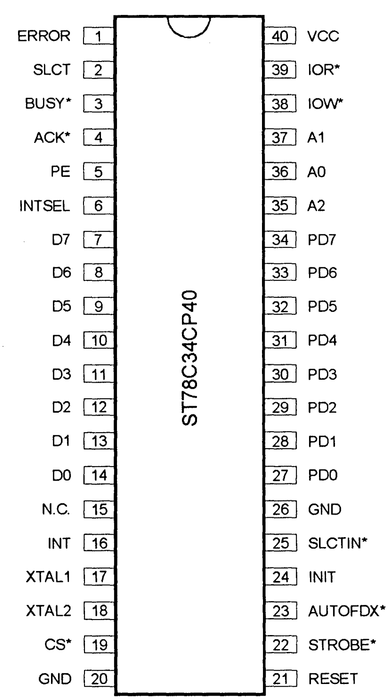
DESCRIPTION

The ST78C34 is a monolithic Bidirectional Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port.
The ST78C34 is a general purpose input/output controller with 83 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.
The ST78C34 is designed to operate as normal printer interface without any additional settings. Contents of the FIFO will be cleared after reset or setting the INIT pin to a low state. The auto FIFO operation starts after the first ACK* is received from the printer. Contents of the FIFO transfer to the printer at the printer loading speed.

PLCC Package



Plastic-DIP Package



FEATURES

- 83 bytes of printer output FIFO
- Bi-directional software parallel port
- Bi-directional I/O ports
- Register compatible to IBM XT, AT, compatible 386, 486
- Selectable interrupt polarity
- Selectable FIFO interrupts

ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C34CJ44	PLCC	0° C to + 70° C
ST78C34IJ44	PLCC	-40° C to + 85° C
ST78C34CP40	Plastic-Dip	0° C to + 70° C
ST78C34IP40	Plastic-Dip	-40° C to + 85° C

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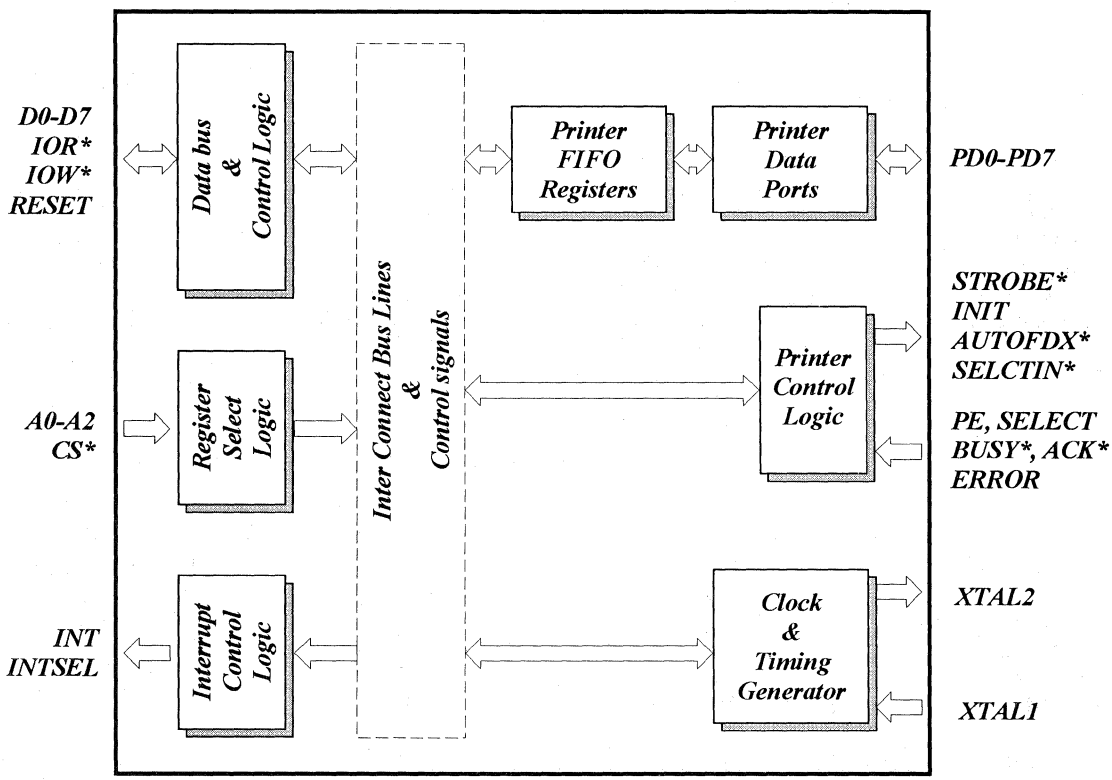
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
ERROR*	1	1	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	2	2	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	3	3	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
ACK*	4	4	I	General purpose input or line printer acknowledge (active low). An output from the printer to indicate that data has been accepted successfully.
PE	5	5	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
INTSEL	6	8	I	Interrupt select mode (pulled-up). The external ACK* can be selected as an interrupt source by connecting this pin to the VCC or left open. Connecting this pin to GND will set the interrupt to latched mode, reading the status register resets the INT output.
D0-D7	14-7	16-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus.
INT	16	19	O	Interrupt output (selectable active low or high). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INT is low and when ACK* is high INT is high if selected as active low interrupt.
XTAL1	17	20	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock oscillator circuit.
XTAL2	18	21	O	Crystal input 2 or buffered clock output. See XTAL1.

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SYMBOL DESCRIPTION

Symbol	Pin 40	Pin 44	Signal Type	Pin Description
CS*	19	22	I	Chip select (active low). A low at this pin enables the ST78C34 / CPU data transfer operation.
GND	20	23	O	Signal and power ground.
RESET	21	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers.
STROBE*	22	25	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	23	26	I/O	General purpose I/O or line printer auto feed (open drain active low). To signal the printer for continuous form feed.
INIT	24	27	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	25	28	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
GND	26	30	O	Power and signal ground.
PD0-PD7	27-34	31-38	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C34 parallel port. PD7-PD0 are latched during output mode.
A2	35	39	I	Address line A2. To select internal registers.
A0-A1	36-37	40-41	I	Address lines. To select internal registers.
IOW*	38	42	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	39	43	I	Read strobe (active low). A low level on this pin transfers the contents of the ST78C34 data bus to the CPU.
VCC	40	44	I	Power supply input.

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1		STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYTE COUNT REGISTER

* Reading the status register will reset the INT output.

PRINTER FUNCTIONAL DESCRIPTION

The ST78C34 parallel port is designed to operate as a normal CENTRONICS printer interface. The port contains 83 byte FIFO that may be enabled via bit-7 of the Alternate Function Register (AFR). After reset, the FIFO is disabled and the part will function identical to the ST16C552. Once the FIFO is enabled via AFR bit-7, the port will enter FIFO mode after the first byte of data is strobed to the printer and the printer responds with either an ACK* or BUSY signal.

The ST78C34 will remain in FIFO mode until the part is reset or INIT is brought low. While in FIFO mode, data transfer to the printer will be controlled by the printer without any user intervention. The printer port also contains a FIFO byte counter that maintains a count of the number of bytes remaining in the FIFO. The FIFO and the FIFO byte counter are cleared by a reset or by a change of state of the INIT pin. All FIFO related timing is derived from the clock input to pin 17 of the part.

A special parallel port write / read mode is activated when INIT is held low, either by writing a "0" to Control Register bit-2 or by forcing the INIT pin low. In this mode the FIFO read pointer is advanced by reading the parallel port instead of the ACK* or BUSY signals. The STROBE* output is forced high. This allows the user to perform parallel port write and read from operations without strobing data to the printer.

Following an INIT, the parallel port will not be in the FIFO mode. Control Register bit-0 is used as the STROBE*, Status Register bit-7 is the inverse of the BUSY signal, and INT is derived from ACK*. The transition into FIFO mode will occur after the first STROBE* is generated and the printer responds with either an ACK* or BUSY. In FIFO mode, STROBE* is generated automatically and writing to Control Register bit-0 has no effect on STROBE*. Alternate Function Register bit 0-2 are used to control the delay and width of STROBE*. Handshaking between the printer and the ST78C34 may be controlled by bit-3 of the Alternate Function Register. Setting this bit to a "1" will result in the use of BUSY instead of ACK* for FIFO reading and interrupt control. INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read of FIFO Byte Count Register (FBCR) should only be performed a minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL pin. If this pin is tied low, a latched interrupt will result. In this mode, INT will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL pin is tied high, INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INT pin may be inverted by setting Alternate Function Register bit-6 high.

The ST78C34 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INT output can be selected as FIFO full or FIFO empty interrupt.

REGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
This bits are set to "1" normally except when AFR bit 5-4 are both set to "1".

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR input state.
0= ERROR input is in low state
1= ERROR input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY or FIFO full signal.

0= BUSY input is in high state
1= BUSY input is in low state

FIFO is enabled.
0= FIFO is full
1= One or more empty locations in FIFO

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INT output) is disabled
1= Interrupt (INT output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INT output is disabled (three state mode)
1= INT output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INT and change interrupt functions.

AFR BIT 0-2:
Timing select.
The STROBE* delay and width can be controlled by these bits.

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
1	0	0	3	2
1	0	1	5	4
1	1	0	5	4
1	1	1	9	8
0	0	0	6	4
0	0	1	10	8
0	1	0	10	8
0	1	1	18	16

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AFR BIT-3:
Interrupt source.
0= ACK* input pin is selected as printer handshaking source
1= BUSY input pin is selected as printer handshaking source

AFR BIT 4-5:
Interrupt type. State of the INT output pin can be selected for one of the following options.

Bit-5	Bit-4	INT output	SR bit-0	SR bit-6
0	0	Normal mode	1	ACK*
0	1	FIFO empty	1	FIFO empty
1	0	FIFO full	1	FIFO full
1	1	FIFO empty	0	FIFO empty

AFR BIT-6:
INT output polarity.
0= Normal. INT output follows the ACK* input
1= Inverted INT output

AFR BIT-7:
FIFO enable / disable function.
0= FIFO is disabled(default mode).
1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR)

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:
FIFO byte count. Number of characters left in FIFO. FCRB bit-0 is the LSB bit of the counter and FCRB bit-6 is the MSB bit of the counter.

FBCR BIT-7:
FIFO state.
0= FIFO is enabled
1= FIFO is disabled

ST78C34 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	Unknown, output mode
STROBE*	High
AUTOFDXT*	High
INIT	Low
SLCTIN*	High

ST78C34 REGISTER CONFIGURATIONS

A1 A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0 0	PR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0 1	STR	BUSY*/ FIFO full*	None Latched INT	PE	SLCT	ERROR	Latched INT	1	1
1 0	COM	1	1	1	INT enable	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
1 0	CON	X	X	I/O select	INT mask	SLCTIN*	INIT	AUTO-FDXT	STROBE*
1 1	AFR	FIFO enable	INT polarity	INT type bit-1	INT type bit-0	INT source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
1 1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	

ABSOLUTE MAXIMUM RATINGS

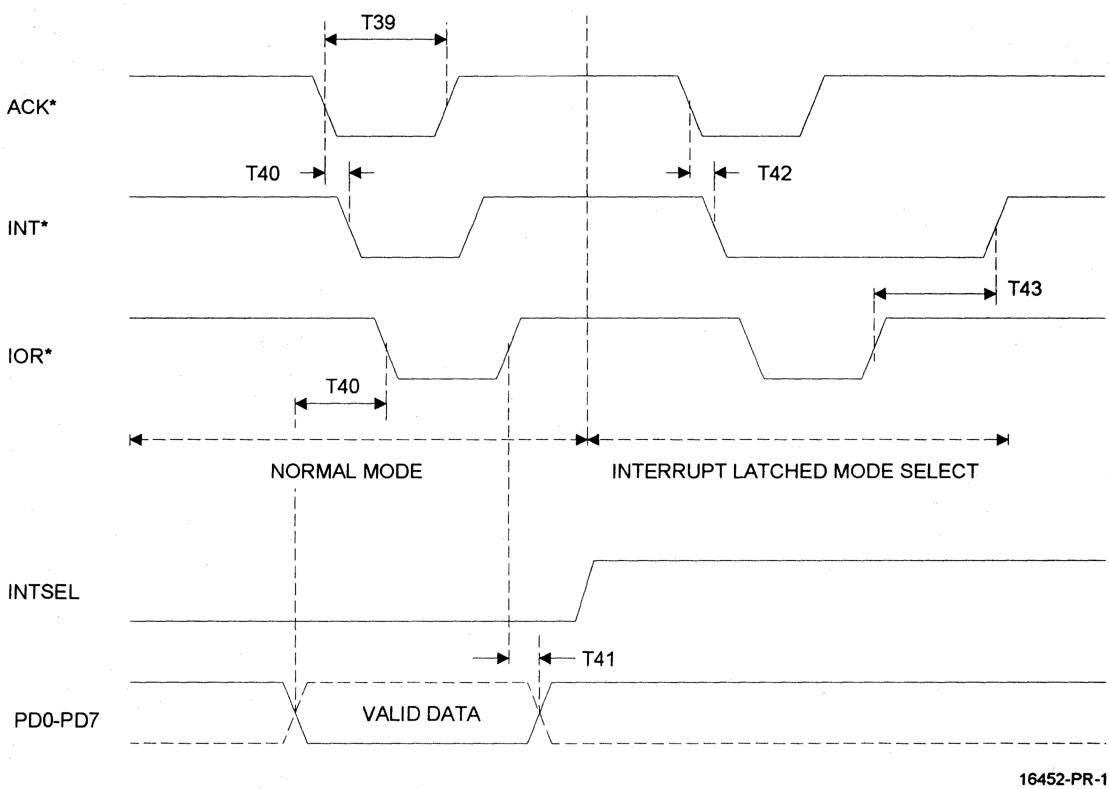
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

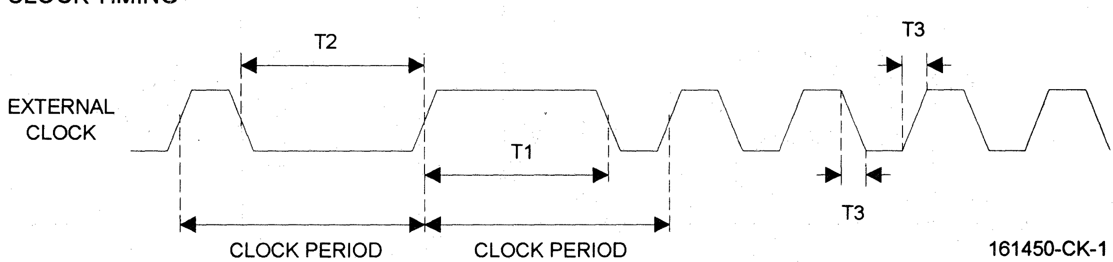
T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 15mA PD7-PD0 I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -150 µA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg. power supply current		12	20	mA	
I_{IL}	Input leakage			±10	µA	Except Pins 1-6
I_{IL}	Input leakage			-450	µA	Pins 1-6 @ Vin=0V
R_{IN}	Input pullup resistance	12		40	kΩ	Pins 1-6
I_{CL}	Clock leakage			±10	µA	

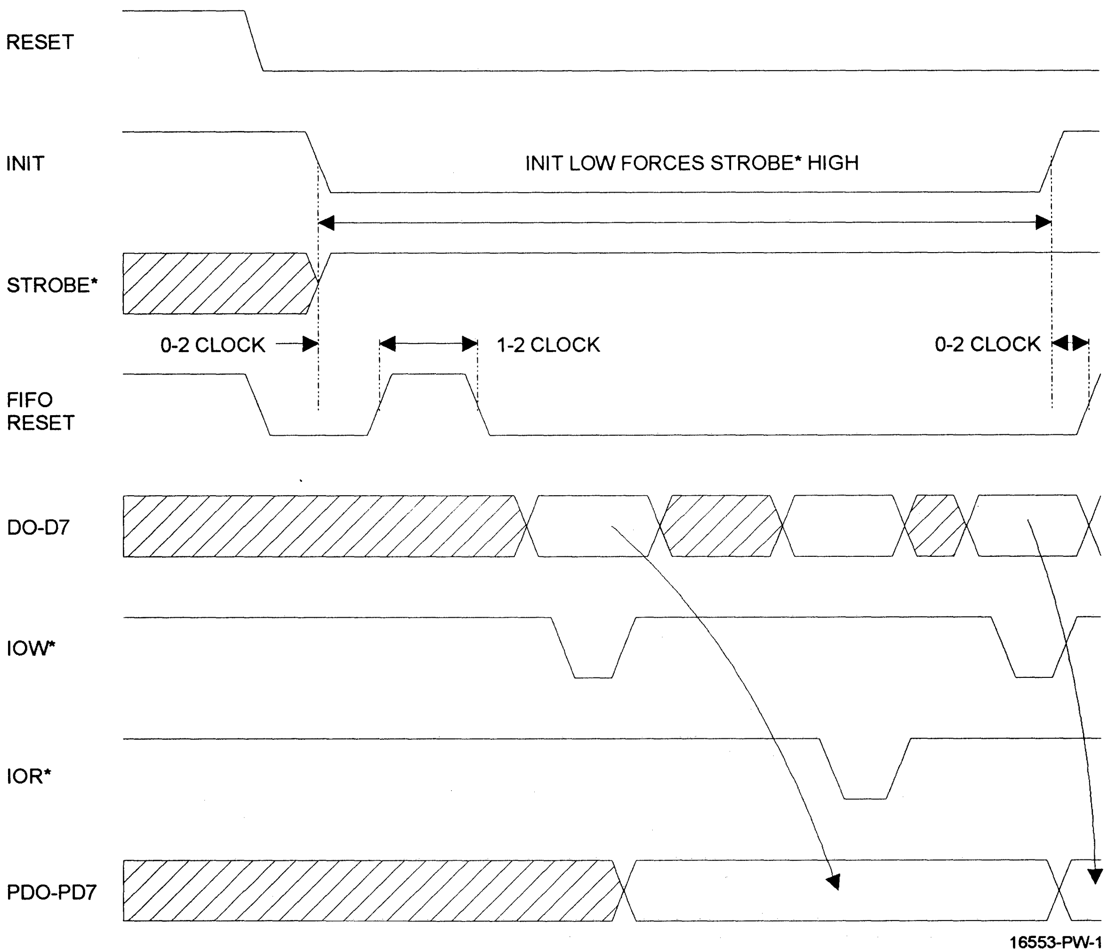
GENERAL READ TIMING



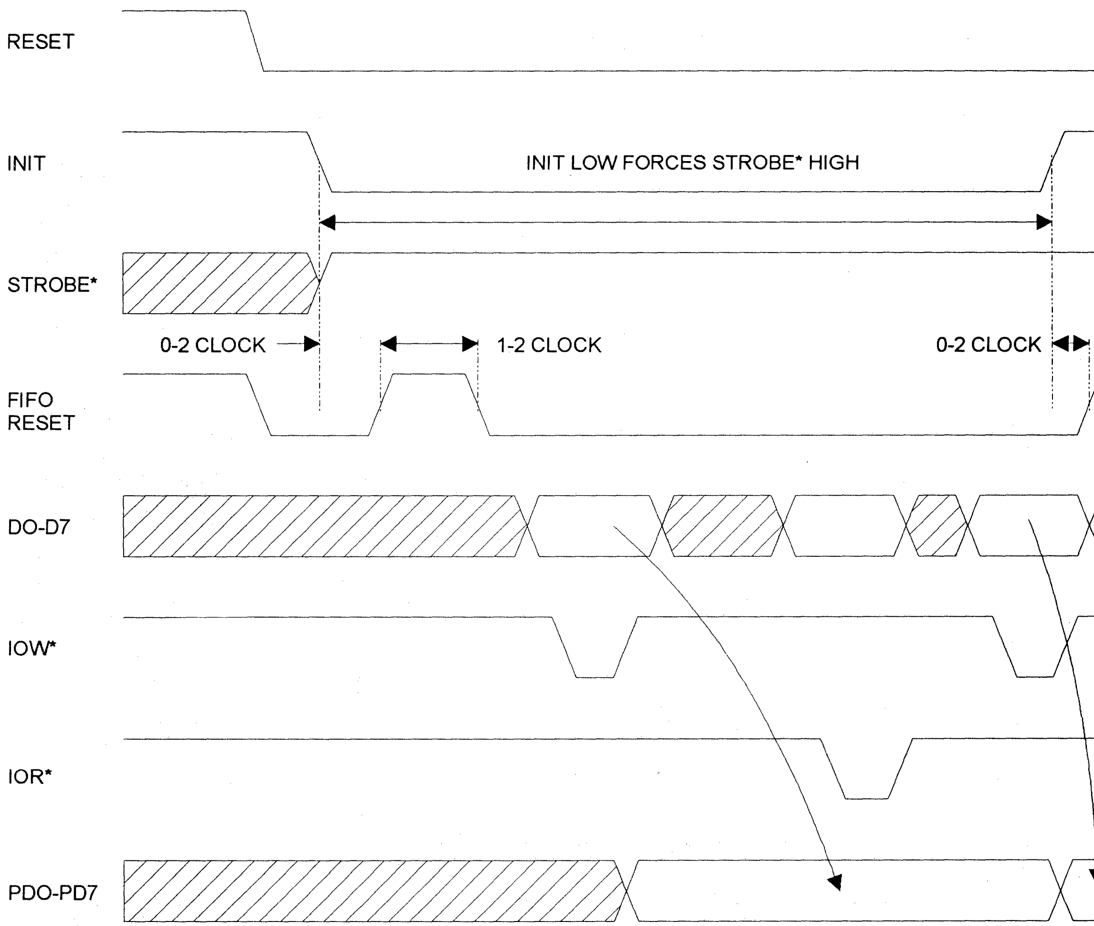
CLOCK TIMING



PRINTER SPECIAL MODE

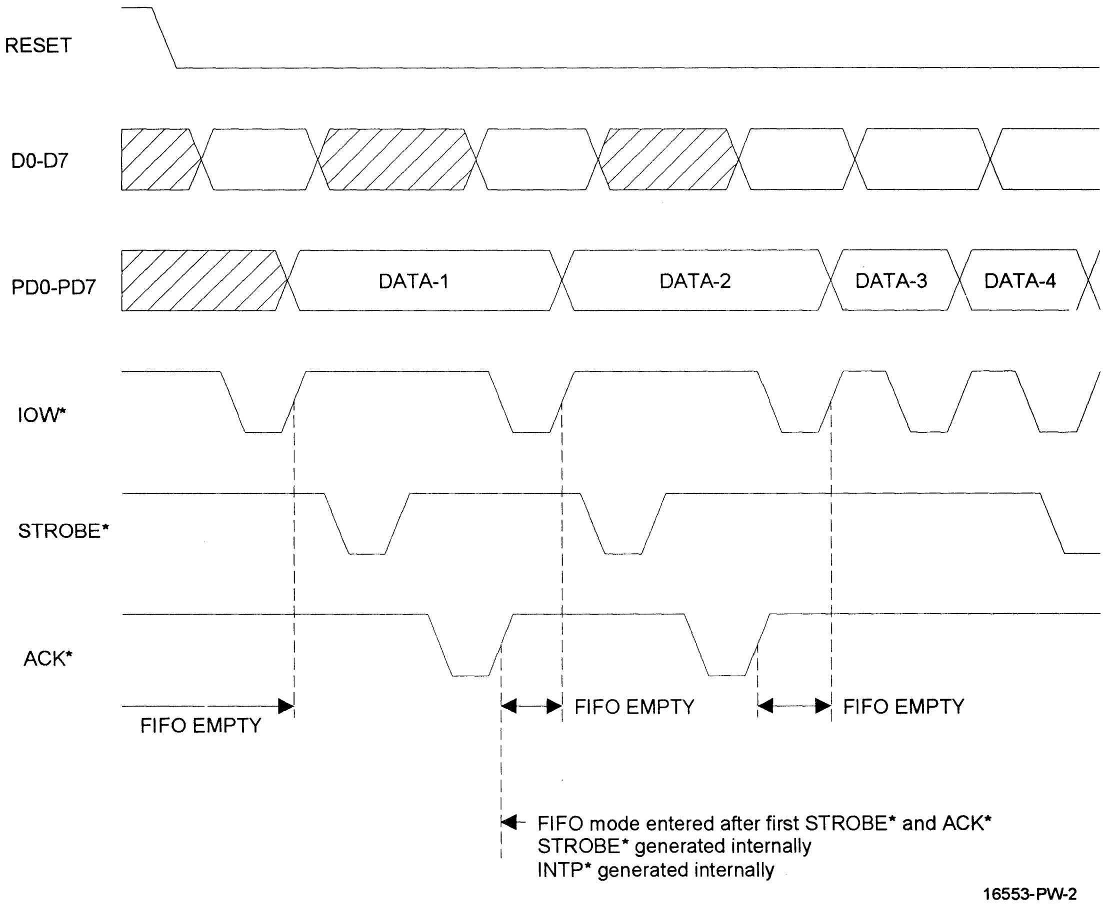


PRINTER SPECIAL MODE

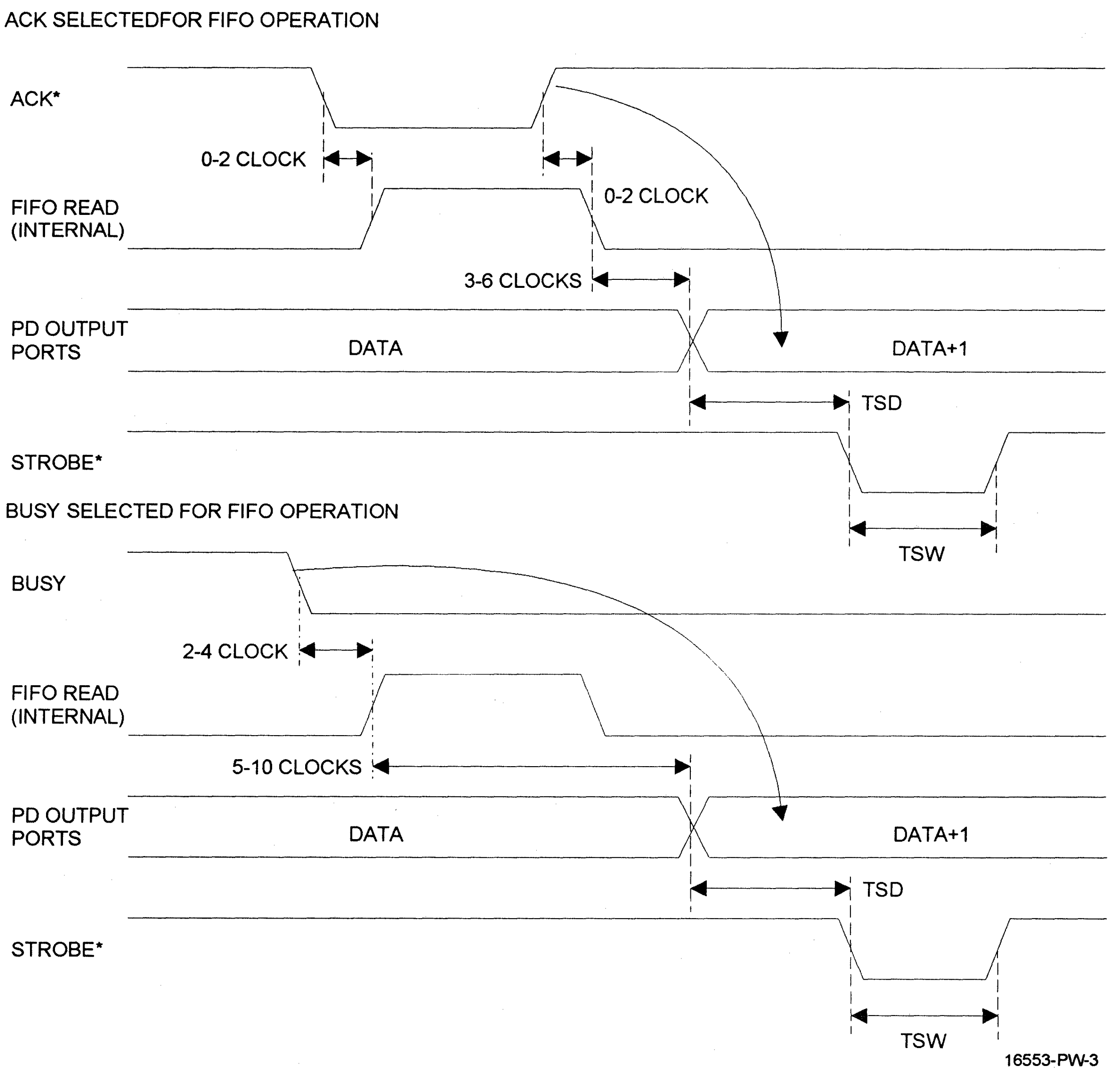


16553-PW-1

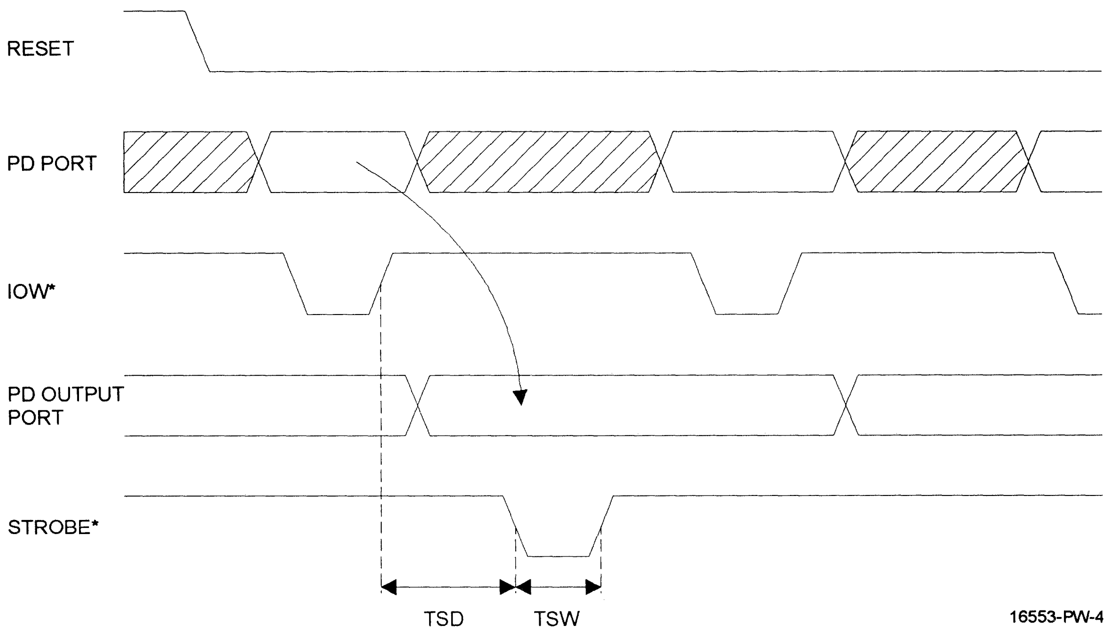
PRINTER AUTO FIFO OPERATION



PRINTER FIFO TIMING WITH MORE THAN ONE BYTE IN THE FIFO



PRINTER FIFO, WITH ONE BYTE IN THE FIFO



STARTECH

An EXAR Company

Preliminary Information

ST78C36

Printed August 3, 1995

ECP/EPP PARALLEL PRINTER PORT WITH 16 BYTE FIFO

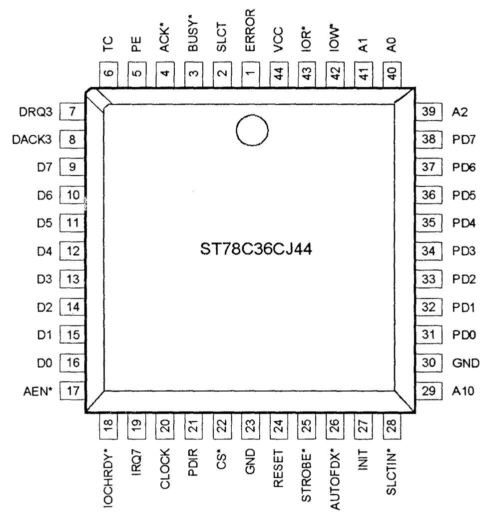
DESCRIPTION

The ST78C36 is a monolithic Parallel Port Interface for use with IBM PC compatible platforms.

Operation as a standard Centronics printer port is the default, but software may re-configure the device to support bi-directional IBM PS/2 parallel port, Enhanced Parallel Port (EPP), or the Extended Capabilities Port (ECP, as defined by Hewlett Packard and Microsoft) modes.

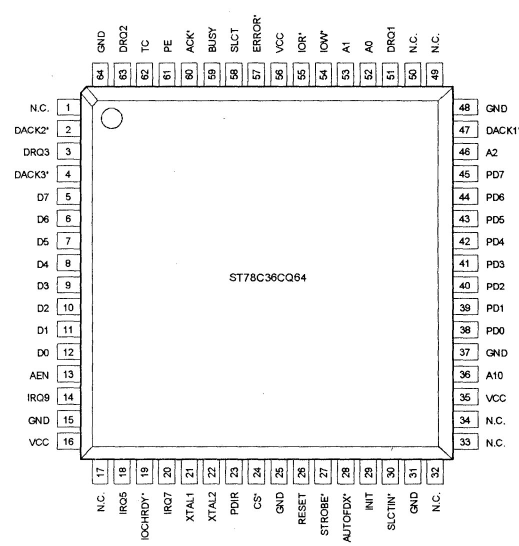
The ECP modes are supported by a 16 byte FIFO that may be accessed by programmed I/O or DMA cycles.

PLCC Package



FEATURES

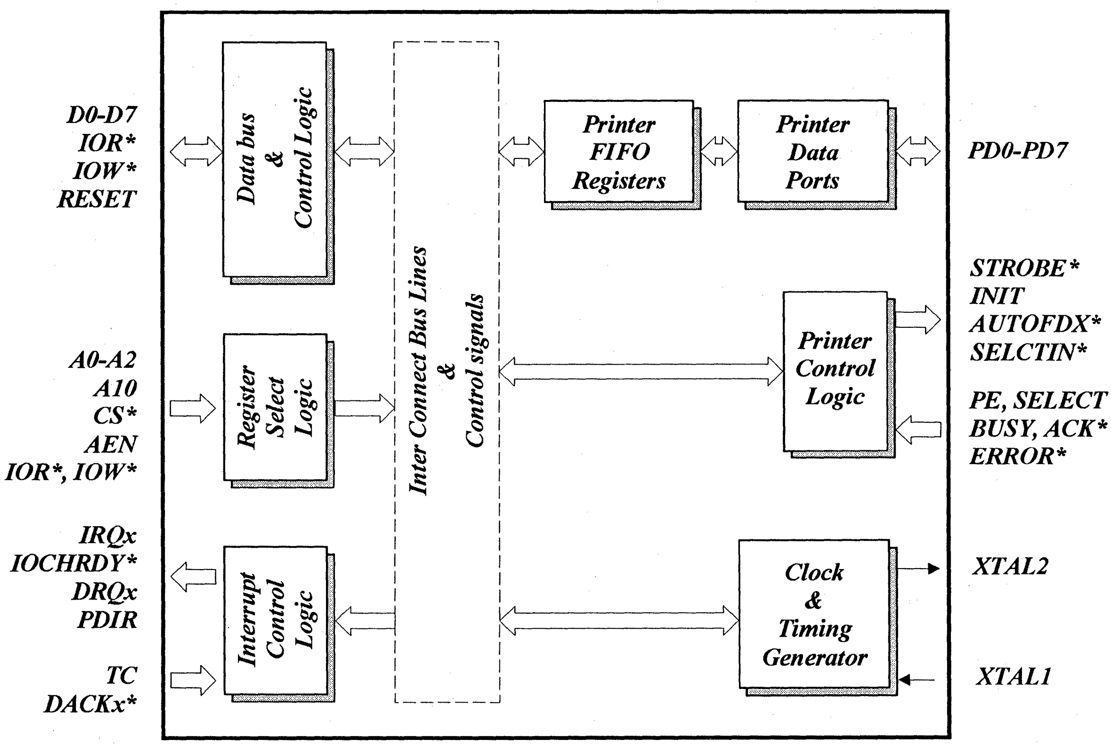
- IBM AT bus compatible
- Bi-directional port capability
- 16 byte FIFO for ECP modes
- On-chip oscillator (ST78C36CQ64)
- Software selectable Interrupt (5, 7, or 9) and 8-bit DMA channel (ST78C36CQ64)



ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C36CJ44	PLCC	0° C to + 70° C
ST78C36CQ64	TQFP	0° C to + 70° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 44	Pin 64	Signal Type	Pin Description
DACK2*	-	2	I	DMA Acknowledge for channel 2 (three stated active low).
DRQ3	7	3	O	DMA Request for channel 3 (three stated active high).
DACK3*	8	4	I	DMA Acknowledge for channel 3 (three stated active low).
D7 - D0	9-16	5-12	I/O	Data bus. Bi-directional data port.
AEN	17	13	I	DMA address enable (active high).
IRQ9*	-	14	O	Interrupt Request channel 9 (three stated active low).
IRQ5*	-	18	O	Interrupt Request channel 5 (three stated active low).
IOCHRDY	18*	19*	O	I/O Channel ready (three stated active low). This pin goes low when ST78C36 requires addition clock cycles for read and write.
IRQ7*	19	20	O	Interrupt Request channel 7 (three stated active low).
CLOCK	20	-	I	Nominal 24 MHz timing input (44-pin package).
XTAL1	-	21	I	Crystal oscillator input, nominal 24 MHz (64-pin package).
XTAL2	-	22	O	Crystal oscillator output, nominal 24 MHz (64-pin package).
PDIR	21	23	O	Printer port direction indicator (1-input, 0-output).
CS*	22	24	I	Chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
RESET	24	26	I	System RESET (active high).
STROBE*	25	27	O	Data strobe output (three stated active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFD*	26	28	O	Automatic line feed (three stated active low). When this

SYMBOL DESCRIPTION

Symbol	Pin 44	Pin 64	Signal Type	Pin Description
				signal is low the printer should automatically line feed after each line is printed.
INIT	27	29	O	Initialize line printer (three stated active low). When this signal is low, it causes the printer to be initialized.
SLCTIN*	28	30	O	Line printer select (three stated active low). When this signal is low, it selects the printer.
A10	29	36	I	Address select line 10, places the ECP control/status/data ports at 400 hex offset from CS* decoded address.
PD0 - PD7	31-38	38-45	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C36 parallel port. PD7-PD0 are latched during output mode. Output only for SPP and PPF modes, bi-directional for all other modes.
A2	39	46	I	Address select line 2.
DACK1*	-	47	I	Active low AT bus DMA ACKnowledge for channel 1.
DRQ1	-	51	O	Active high AT bus DMA ReQuest for channel 1.
A0-A1	40,41	52,53	I	Address select line 0 - 1, used for register (port) selection.
IOW*	42	54	I	Active low AT bus I/O Write strobe.
IOR*	43	55	I	Active low AT bus I/O Read strobe.
ERROR*	1	57	I	Line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	2	58	I	Line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	3	59	I	Line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
ACK*	4	60	I	Line printer acknowledge (active low). This input is pulsed

SYMBOL DESCRIPTION

Symbol	Pin 44	Pin 64	Signal Type	Pin Description
				low by the printer to indicate that data has been accepted successfully.
PE	5	61	I	Line printer paper empty (active high). An output from the printer to indicate out of paper.
TC	6	62	I	Terminal Count (active high). The ST78C36 terminates the DMA channel when a high pulse is detected.
DRQ2	-	63	O	DMA Request for channel 2 (three stated active high).
VCC	44	16,35, 56	I	Supply power (+5 Vdc).
GND	23,30	15,25, 31,37, 48, 64	O	Supply ground.

OVERVIEW

This device is designed around the Hewlett Packard/ Microsoft specification for Extended Capabilities Port Protocol with "ECR mode 100" defined as Enhanced Parallel Port (EPP) mode. The internal timing engines were designed around a 24 MHz reference, which can be supplied from an external source or by the built-in oscillator circuit (ST78C36CQ64 only) with an appropriate crystal.

At system RESET, the device defaults to standard IBM PC compatible Centronics printer mode (output only). The bi-directional PS/2, EPP, and ECP modes can only be activated by programming the ECR mode field (this requires address bit A10 = 1, which is outside the normal a three state state/ISA I/O space).

Optional capabilities of the ECP specification are set as follows:

- ECP defined interrupts are pulsed, low true (Centronics ACK* is non-pulsed, low true).
- PWord size is forced to 1 byte.
- There is 1 byte in the transmitter that does not affect the FIFO full bit (ECP modes).
- RLE compression is not supported in hardware.
- IRQ channel is selectable as 5, 7, or 9 (ST78C36CQ64 only).
- DMA channel is selectable as 1, 2, or 3 (ST78C36CQ64 only).
- FIFO THRESHOLD is set at 8 (used only for non-DMA access to the FIFO).

PORT	ADDRESS	R/W	MODE	FUNCTION
DATA	000	R/W	000-001	Data Register
ECP-AFIFO	000	W	011	ECP FIFO (Address)
DSR	001	R	All	Status Register
DCR	002	R/W	All	Control Register
EPP-APort	003	R/W	100	EPP Port (Address)
EPP-DPort	004-007	R/W	100	EPP Port (Data)
C-FIFO	400	W	010	Parallel Port Data FIFO
ECP-DFIFO	400	R/W	011	ECP FIFO (Data)
T-FIFO	400	R/W	110	Test FIFO
Cnfg-A	400	R	111	Configuration Register A
Cnfg-B	401	R-R/W	111	Configuration Register B
ECR	402	R/W	All	Extended Control Register

REGISTER DEFINITIONS

DATA REGISTER (DATA)

DATA Bit 0-7:
For host output cycles in SPP mode (ECR mode 000) or PS/2 mode (ECR mode 001), data from the host is registered at the trailing edge of IOW*. On host input cycles, data at the peripheral port is passed through to the host data bus.

ECP FIFO ADDRESS (ECP-AFIFO)

ECP-AFIFO Bit 0-7:
This port is only available for programmed I/O (non-DMA), and only has significance for host write. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set low on write.

A read from this port is the same as a read at 400.

STATUS REGISTER (DSR)

This status register is read-only except for bit-0, and all bits are latched for the duration of IOR*.

DSR Bit-0:
If EPP mode is not selected, this bit returns logic one. During EPP mode, bit-0 will return a high if the EPP 10 μsecond TimeOut elapsed during the last EPP read or write cycle (this TimeOut also aborts the EPP cycle). This status bit is cleared by exiting EPP mode or by the host writing a high to bit-0 of this register.

DSR Bit 1-2:
Reserved, logic one.

DSR Bit-3:
The true state of the ERROR* pad.

DSR Bit-4:
The true state of the SLCT pad.

DSR Bit-5:
The true state of the PE(mpty) pad.

DSR Bit-6:
The true state of the ACK* pad.

DSR Bit-7:
The complement of the BUSY pad.

CONTROL REGISTER (DCR)

DCR Bit-0:
The complement of this bit drives STROBE*, and the complement of the pad state is returned for read.

DCR Bit-1:
The complement of this bit drives AUTOFD*, and the complement of the pad state is returned for read.

DCR Bit-2:
This bit drives INIT, and the pad state is returned for read.

DCR Bit-3:
The complement of this bit drives SLCTIN*, and the complement of the pad state is returned for read.

DCR Bit-4:
Ack Interrupt Enable set to a high will generate an interrupt when ACK* is low. When either returns to a high state, this interrupt source will go in-active. This interrupt is not pulsed.

DCR Bit-5:
Peripheral port direction, OUT = 0 and IN = 1.
This bit is forced to logic zero by ECR modes 000 or 010. It can be written only in ECR mode 001, and will maintain that state if the ECR mode is changed to 011, 100, or 110. This bit must be set low for EPP mode, which allows the host to control direction with IOR* and IOW*. The final port direction also drives PDIR.

DCR Bits 6-7:
Reserved, logic zero.

EPP ADDRESS PORT (EPP-APort)
When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with SLCTIN* active. Direction is set by host read/write and will drive STROBE* low during a write if DCR bit 5 (DIR) is not set high.

EPP DATA PORT (EPP-DPort)
When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with AUTOFD* active. Direction is set by host read/write and will drive STROBE* low during a write if DCR bit 5 (DIR) is not set high.

PARALLEL PORT DATA (C-FIFO)
This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1.
Data written to this port will be automatically transferred to the peripheral with STROBE* handshaking with BUSY. This port is only defined for write, host reads will interfere with FIFO read sequencing.

ECP DATA FIFO (ECP-DFIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set high on write.
Data read from this port will undergo de-compression if the FIFO tag bit and data bit-7 are both low. The byte containing the RLE count is loaded into the RLE counter and the succeeding byte in the FIFO will be returned to the host RLE count + 1 times before the FIFO read address is incremented. If a FIFO under-run is incurred during host read, the last data byte is returned and FIFO-E remains coherent.

TEST FIFO (T-FIFO)
This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. During a read cycle from this port a FIFO under-run will return last data read and FIFO-E remains coherent.

CONFIGURATION REGISTER A (Cnfg-A)
This read-only register is available in ECR mode 111 only.

Cnfg-A Bit 0-1:
Forced to logic zero, this field is don't care for PWord = 1 byte.

Cnfg-A Bit-2:
When transmitting, there is 1 byte waiting to be transmitted that does not affect FIFO-F.

Cnfg-A Bit-3:
Reserved, logic zero.

Cnfg-A Bit 4-6:
Indicates PWord = 1 byte (8-bit implementation).

Cnfg-A Bit-7:
Indicates ECP interrupts are pulsed.

CONFIGURATION REGISTER B (Cnfg-B)
This register is available in ECR mode 111 only, and returns bits 0-5 as logic zero for the ST78C36CJ44. The ST78C36CQ64 will allow programmed selection of the Interrupt and DMA channels after a system RESET state of 001011 (bits 0-5).

Cnfg-B Bit 0-2:
With bit 2 forced low, select an 8-bit DMA channel per the following table:

IOW*	IOR*	DMA
X00	000	3
X01	001	1
X10	010	2
X11	011	3 (default)

Cnfg-B Bit 3-5:
Select an IRQ channel per the following table:

IOW*	IOR*	IRQ
000	001	7
001	001	7 (default)
010	010	9
011	001	7
100	001	7
101	001	7
110	001	7
111	111	5

Cnfg-B Bit-6:
Returns the true value of the selected IRQ pad.

Cnfg-B Bit-7:
Indicates RLE compression is not supported.

EXTENDED CONTROL REGISTER (ECR)
The Extended Control Register has a system RESET state of 00010101. The significance of the bits is defined by the ECP specification as:

ECR Bit-0:
This read-only bit returns FIFO empty status (FIFO-E) and is forced high unless PPF, ECP, or TST mode is selected.

ECR Bit-1:
This read-only bit returns FIFO full status (FIFO-F) and is forced low unless PPF, ECP, or TST mode is selected.

ECR Bit-2:
When low, this bit (ServiceIntr) enables a pulsed interrupt and enables DMA requests if bit 3 is set. If the enabled interrupt occurs, this bit is automatically returned to a high. The interrupt conditions are:

DMA	DIR	CONDITION
0	0	8 empty bytes in the FIFO.
0	1	8 filled bytes in the FIFO.
1	X	DMA Terminal Count (TC).

ECR BIT-3:
This bit disables DMA when set low. When set high, a low on ServiceIntr will enable DMA requests.

ECR Bit-4:
When low, this bit (ErrIntrEn*) enables a pulsed interrupt if ERROR* (Fault*) is low. The interrupt is only enabled in ECP mode.

ECR Bit 5-7:
This field can be set to any value if the current value is 000 or 001. If the current value is not 000 or 001, then the field can only be written to 000 or 001. The modes are defined as:

MODE	NAME	DESCRIPTION
000	SPP	Standard, output only.
001	PS2	Bi-directional parallel port.
010	PPF	FIFOed, output only.
011	ECP	ECP FIFOed port with RLE de-compression.
100	EPP	EPP mode.
101	-	reserved
110	TST	FIFO test mode.
111	CFG	Configuration register enable.

OPERATION

SPP MODE

This is ECR mode 000 (system RESET mode).
In this output-only mode the host data is registered to PD[7:0] at the trailing edge of IOW*; PDIR is driven low; STROBE*, AUTOFD*, INIT, and SLCTIN* are open-drain; and all timing is managed by the host through DSR and DCR registers.

PS2 MODE

This is ECR mode 001.
In this bi-directional mode the host output data is registered to PD[7:0] at the trailing edge of IOW*, PDIR is driven by DIR to allow peripheral data input, AUTOFD*, INIT, and SLCTIN* are totem-pole, and all timing is managed by the host through DSR and DCR registers.

PPF MODE

This is ECR mode 010.
In this output-only mode the host data is written to the FIFO with I/O writes to address 400 or by DMA writes; PDIR is driven low*; AUTOFD*, INIT, and SLCTIN* are totem-pole.
FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes STROBE* (controller) with BUSY (peripheral).

ECP MODE

This is ECR mode 011.
In this bi-directional mode the host data is written to the FIFO with I/O writes to address 000, 400 or DMA; PDIR is driven by DIR (can only be set in ECR mode 001); AUTOFD*, INIT, and SLCTIN* are totem-pole. I/O writes to address 000 will write a low into the FIFO tag bit, while I/O writes to address 400 or DMA will insert a high.

ECP FORWARD MODE (PDIR = 0)

FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes STROBE* (controller) with BUSY (peripheral). Data from the FIFO tag bit is output on AUTOFD* after being registered simultaneous with FIFO data.

4

ECP REVERSE MODE (PDIR = 1)

PD[7:0] data and BUSY are latched into the FIFO and tag bit respectively at the trailing edge of AUTOFD* if FIFO-F = 0. Timing is generated by controller logic that handshakes ACK* (peripheral) with AUTOFD* (controller).

EPP MODE

This is ECR mode 100.
In this bi-directional mode, I/O writes will latch host output data at the trailing edge of IOW*, and peripheral input data will be latched at the trailing edge of SLCTIN* or AUTOFD*. PDIR, and STROBE* are driven by the state of IOW* (DCR bits 5 and 0 must be set low); AUTOFD*, INIT, and SLCTIN* are totem-pole.

EPP mode allows buffered access between the PC bus and the peripheral with timing provided by the peripheral via BUSY handshake into IOCHRDY. I/O cycles with address 003 - 007 will immediately drive IOCHRDY low. STROBE* will go low and PD[7:0] is allowed to change (write cycles) after BUSY has been low for at least 60n second. (this delay may have elapsed prior to cycle initiation), immediately followed by a low driven on SLCTIN* for address 003 or AUTOFD* (DATASTB*) for address 004 - 007 (read and write cycles). When BUSY returns high for a minimum of 60n second, IOCHRDY and the active strobe will be driven high - allowing the host to complete the I/O transaction.

To prevent a system stall, a 10 μsecond TimeOut aborts the cycle if it expires before BUSY returns high. This TimeOut also sets bit 0 of DCR, which is cleared by disabling EPP mode or writing a high to DCR bit 0.

TST MODE
This is ECR mode 110.
This mode allows data to be transferred (read or write in any direction) between the FIFO and host at address 400 or DMA without activating the control interface (no data is transferred to/from the peripheral). PDIR is driven by DIR (can only be set in ECR mode 001); AUTOFD*, INIT, and SLCTIN* are totem-pole.

Performing I/O cycles in this mode allows software to test for the value of FIFOThreshold (FT) for both output and input directions.

CFG MODE
This is ECR mode 111.
This mode enables I/O access to the configuration registers cnfgA and cnfgB and disables I/O access to the FIFO.

IRQ
The module has four sources of interrupt which may be directed to IRQ5*, IRQ7*, IRQ9* (see cnfgB) or externally jumpered.

1) When DCR bit 4 (AIE) is high and ACK* is low the interrupt is active.

2) When ECP mode is active, if ECR bit 4 is low when ERROR transitions low or ECR bit 4 transitions low when Fault* is low an interrupt pulse of at least 200n seconds will be generated.

3) In FIFO modes (PPF, ECP, or TST) with ECR bit 3 (DMA) low, an interrupt pulse of at least 200n seconds will be generated when ECR bit 2 (SI) is set low if there are at least 8 empty bytes in the FIFO and PDIR = 0 or there are at least 8 filled bytes in the FIFO and PDIR = 1. This interrupt will automatically disable itself by setting ECR bit 2 high.

4) In FIFO modes (PPF, ECP, or TST) with (DMA request enabled), an interrupt pulse of at least 200n seconds will be generated when TC is received if PDACK* is low.
This interrupt will automatically disable itself and the DMA request by setting ECR bit 2 high.

DMA
DMA cycles occur only between the host and the FIFO data port (address 400) for PPF, ECP, or TST modes. The selected DRQ(1, 2, or 3) will be driven high if ECR bit 3 (DMA) is high and ECR bit 2 (SI) is low when {PDIR = 0 and FIFO-F = 0} or {PDIR = 1 and FIFO-E = 0} or TST mode is active.

When the selected DACK*(1, 2, or 3) is low, IOW* will transfer host data to the FIFO and IOR* will transfer FIFO data to the host.
The selected DRQ will be driven low to terminate the DMA channel when {PDIR = 0 and FIFO-F = 1} or {PDIR = 1 and FIFO-E = 1} or ECR bit 2 (SI) goes high (interrupt condition 4 above) or more than 32 consecutive DMA data cycles (read or write) have occurred.

FIFO-F and FIFO-E terminated cycles will automatically restart when their state returns low. Consecutive cycle termination will automatically restart because the counter is reset when the selected DACK* goes high. TC terminated cycles can only be restarted by the host setting ECR bit 2 (SI) low again.

RLE
The module does not support RLE compression (indicated by the "0" in cnfgB bit 7) but is required to support RLE de-compression.

The host may send compressed data to the peripheral by writing the RLE length byte (bit 7 = 0) to address 000 (NOTE: DMA cannot be used for this byte) which will place a zero into the FIFO tag bit. This must be followed immediately by the data byte being written to the FIFO at address 400. These bytes will be transferred to the peripheral in the normal manner.

De-compression takes place if PDIR = 1 when data is read from the FIFO at address 000, 400 or DMA. When a byte is read from the FIFO, bits 0-6 (length) are placed in a counter if data bit-7 and the FIFO tag bit are both low. The subsequent byte in the FIFO (data) is presented to the host count + 1 times before the FIFO read pointer is advanced.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
VILCK	Clock Input Low level	-0.5		0.6	V	
VIHCK	Clock Input High level	3.0		VCC	V	
VIL	Input Low level	-0.5		0.8	V	
VIH	Input High level	2.0		VCC	V	
VOL	Output Low level			0.4	V	Except PDIR IOL=24 mA
PDIR	IOL=4 mA					
VOH	Output High level	2.4			V	Except PDIR IOH=-12 mA
PDIR	IOH=-1 mA					
ICC	Avg. power supply current		TBD	TBD	mA	
IIL	Input leakage			10	µA	
ICL	Clock leakage			10	µA	

NOTE: Hewlett Packard / Microsoft compliance testing requires all ECP mode drivers to be push-pull and that they have an impedance controlled series resistor of at least 20 Ohms and that the typical on resistance of the combination of the driver-resistor pair is in the 45-65 Ohm range.

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
TRRQ	DRQx inactive delay from DACK*x active			100	S	
TASU	AEN setup to command active	40			S	
TAH	AEN hold from command inactive	10			S	
TCMD	Command width	150			S	
TACC	Data access from IOR* active			100	S	
TDSU	Data setup to IOW* inactive	40			S	
TDH	Data hold from command inactive	10			S	
HOST	DMA TIMING					
TPDD	PD7-0, STROBE*, AUTOFD*, INIT, SLCTIN* delay from IOW* inactive			100	S	
TIRQ	Interrupt delay from ACK*			60	S	
TPW	Interrupt pre-charge pulse at release			10	S	
TDS	PD7-0 setup to STROBE* active		600		S	
TWS	STROBE* width		600		S	
TDH	PD7-0 hold from STROBE* inactive		450		S	1
THS	STROBE* active to BUSY active (handshake)			500	S	
TDD	PD7-0 hold from BUSY inactive		80		S	1
TCD	BUSY inactive to STROBE* active (cycle delay)		680		S	
TDS	PD7-0, AUTOFD* setup to STROBE* active		0	60	S	3
T1	STROBE* inactive to BUSY inactive		0		S	
T2	BUSY inactive to STROBE* active		80	200	S	1,2
T3	STROBE* active to BUSY active		0		S	
T4	BUSY active to STROBE* inactive		80	180	S	2
TDH	PD7-0, AUTOFD* hold from BUSY active		80	180	S	1,2,3
TDS	PD7-0, BUSY setup to ACK* active		0		S	3
T1	ACK* inactive to AUTOFD* active		80	200	S	2
T2	AUTOFD* active to ACK* active		0		S	
T3	ACK* active to AUTOFD* inactive		80	200	S	1,2
T4	AUTOFD* inactive to ACK* inactive		0		S	
TDH	PD7-0 data hold from AUTOFD*		0		S	
TAS	Host address setup to IOW* active		40		S	
TAH	Host address hold from IOW* active		10		S	
TDS	Host data setup to IOW* active		0	20	S	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
TDH	Host data hold from IOW* active		0		S	
TBSY	IOW* active to IOCHRDY low		0	20	S	
TDD	IOW* active to PD7-0 valid		0	50	S	
TWPD	WAIT* active to PDIR change			10	S	
THT	IOCHRDY high to Host terminate (IOW* inactive)		10		S	
TCD	IOW* inactive to Host command active (IOW* or IOR*)		40		S	
TPDW	PDIR low to WRITE* active		0		S	
TPW	IOCHRDY pre-charge width at release			10	S	
TDWS	WAIT* active to ADDRSTB*/ DATASTB* active		60	175	S	1
TWW	WAIT* active to WRITE* change		60	155	S	1
TWDH	WAIT* active to PD7-0 change		60	140	S	1,2
TRDY	WAIT* inactive to IOCHRDY high		60	155	S	1
TWS	WAIT* inactive to ADDRSTB*/ DATASTB* inactive		60	155	S	1
TSWD	ADDRSTB*/DATASTB* inactive to WAIT* active		0		S	
TSW	ADDRSTB*/DATASTB* active to WAIT* inactive		0	10	µS	
TTO	IOW* active to WAIT* inactive (Time Out)		10	12	µS	
TAS	Host address setup to IOR* active		40		S	
TAH	Host address hold from IOR* active		10		S	
TDS	Host data setup to IOR* inactive		0	20	S	
TDH	Host data hold from IOR* inactive		0		S	
TBSY	IOR* active to IOCHRDY low		0	20	S	
TACC	ADDRSTB*/DATASTB* active to		0		S	
TDD	PD7-0 valid to D7-0 valid		0	75	S	
TWPD	WAIT* active to PDIR change PD7-0 valid		60	150	S	1
THT	IOCHRDY high to Host terminate (IOR* inactive)		10		S	
TCD	IOR* inactive to Host command active (IOW* or IOR*)		40		S	
TPW	IOCHRDY pre-charge width at release			10	S	

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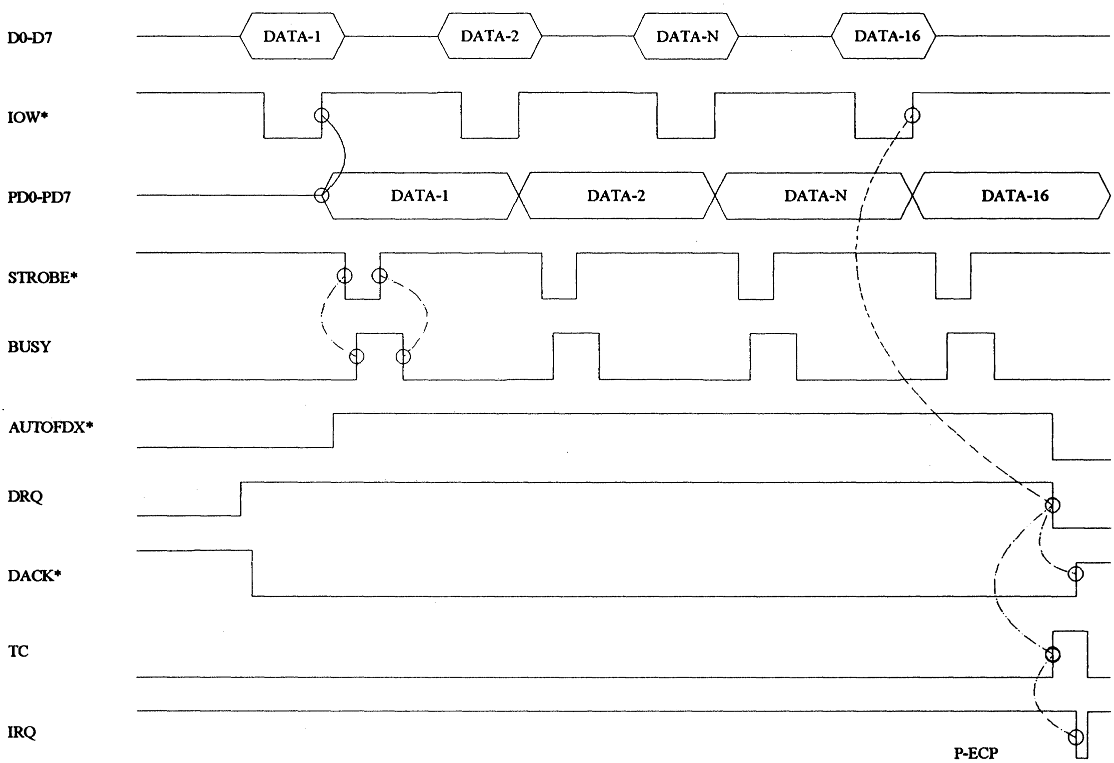
AC ELECTRICAL CHARACTERISTICS

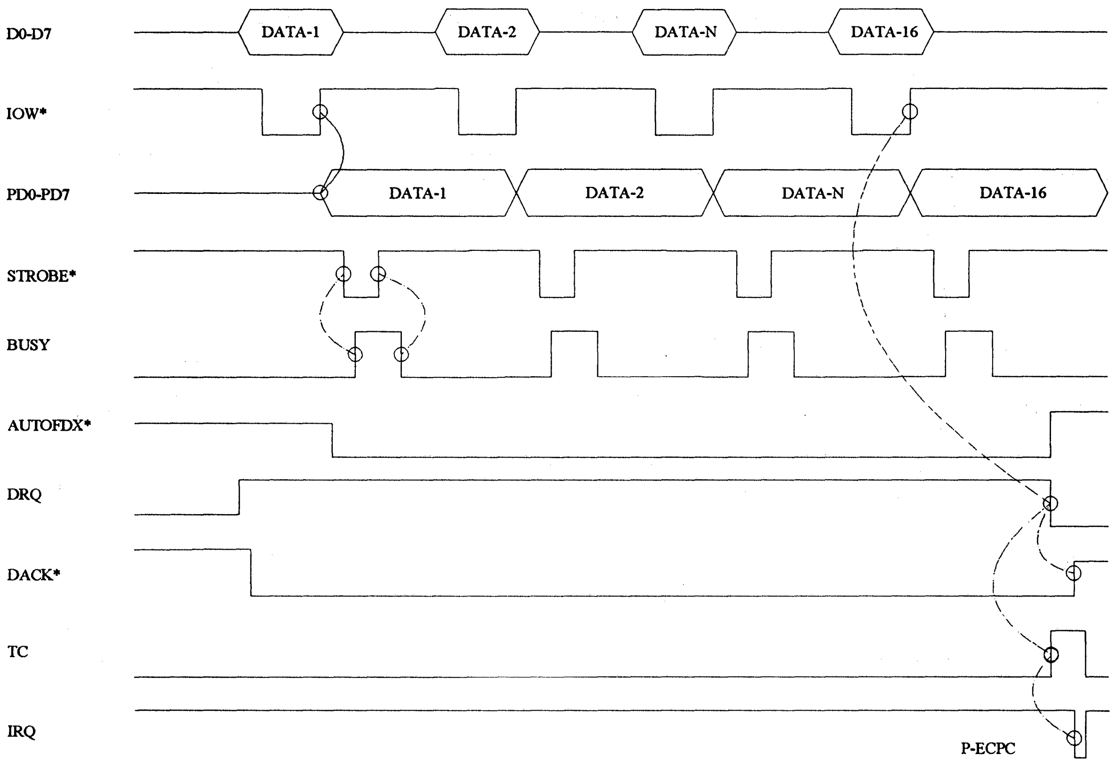
T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
TDWS	WAIT* active to ADDRSTB*/ DATASTB* active		0	175	S	
TWW	WAIT* active to WRITE* change		0	140	S	2
TWDH	WAIT* active to PD7-0 change		60	160	S	1
TRDY	WAIT* inactive to IOCHRDY high		60	160	S	1
TWS	WAIT* inactive to ADDRSTB*/ DATASTB* inactive		60	160	S	1
TSWD	ADDRSTB*/DATASTB* inactive to WAIT* active		0		S	
TSW	ADDRSTB*/DATASTB* active to WAIT* inactive		0	10	μS	
TTO	IOR* active to WAIT* inactive (Time Out)		10	12	μS	

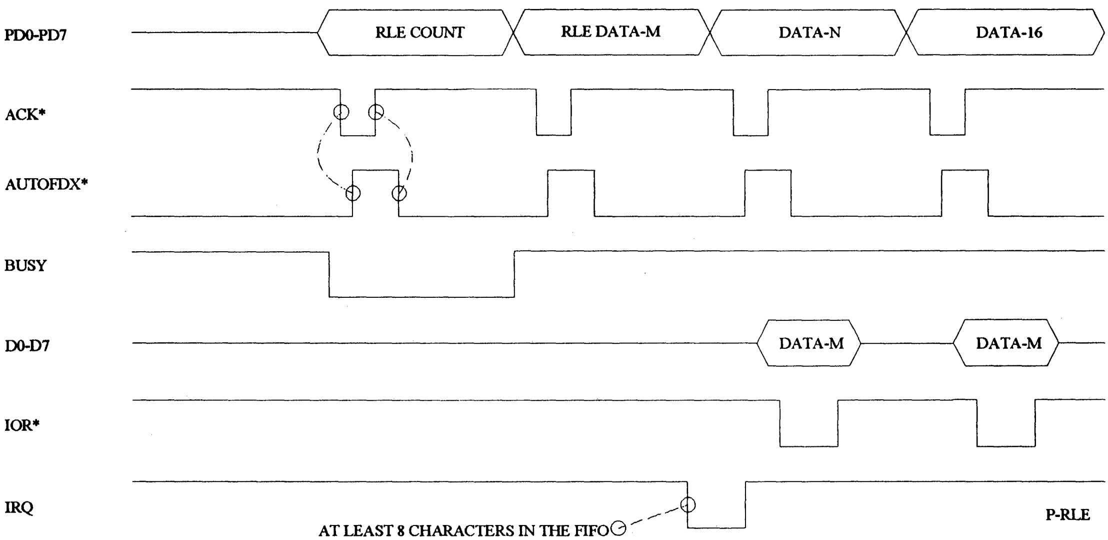
ECP MODE (MODE 011, DATA MODE OPERATION, OUTPUT DIRECTION)



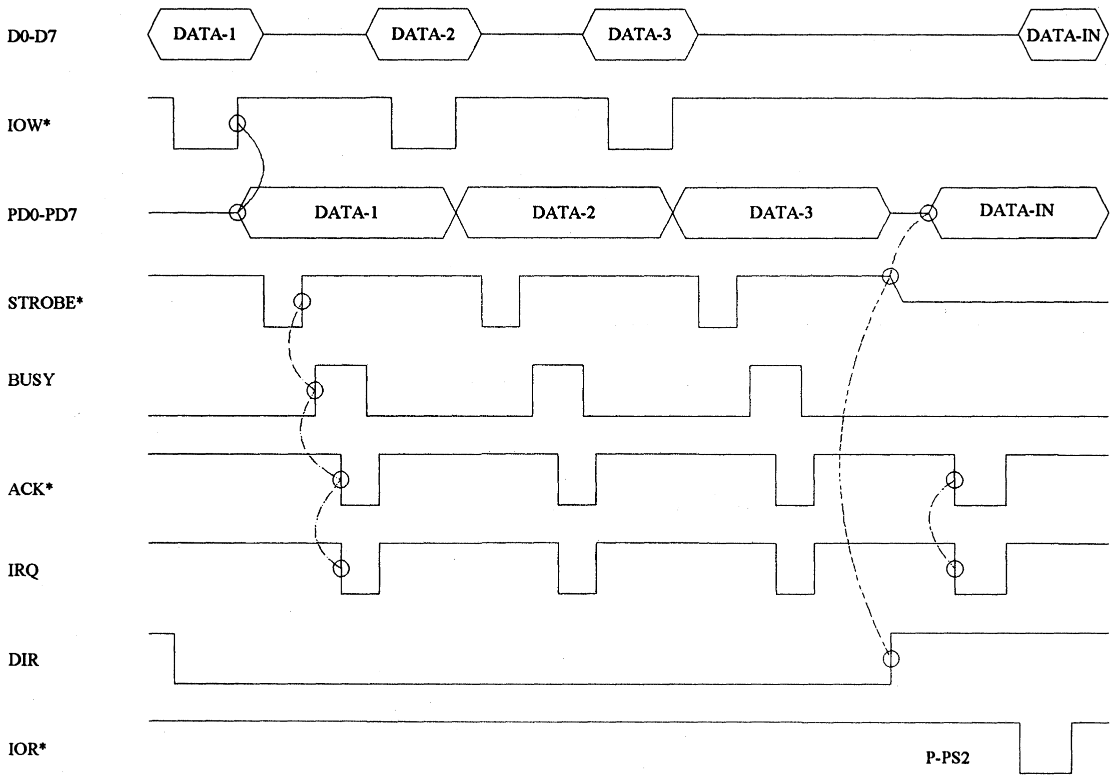
ECP MODE (MODE 011, COMMAND MODE OPERATION OUTPUT DIRECTION)



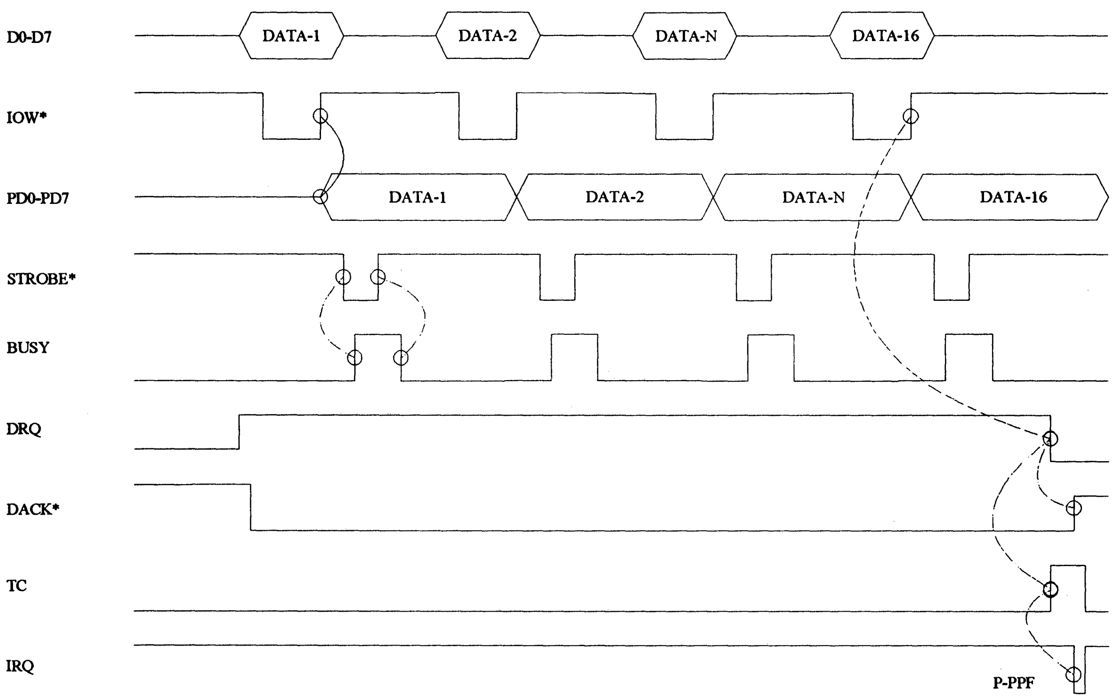
ECP MODE (MODE 011, DATA DECOMPRESSION, INPUT DIRECTION)



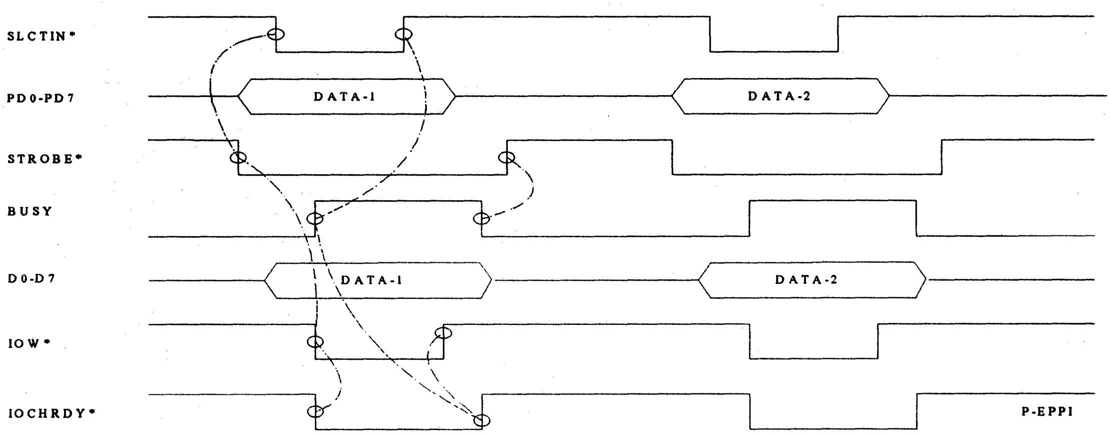
PS2 MODE (MODE 001)



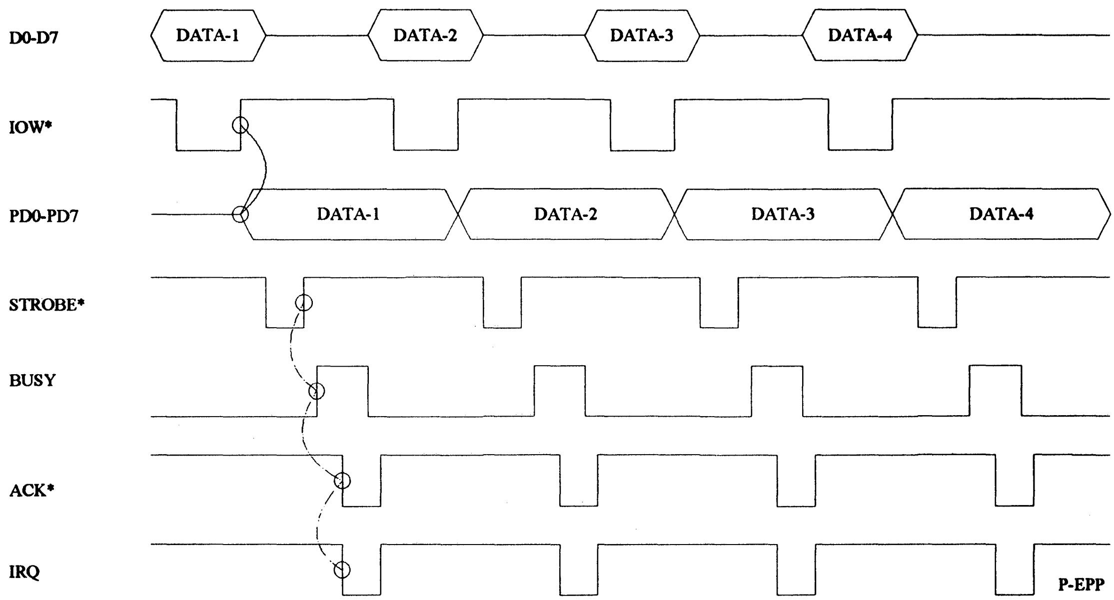
PPF MODE (MODE 000, FIFO'S ARE SET FOR OUTPUT DIRECTION ONLY)



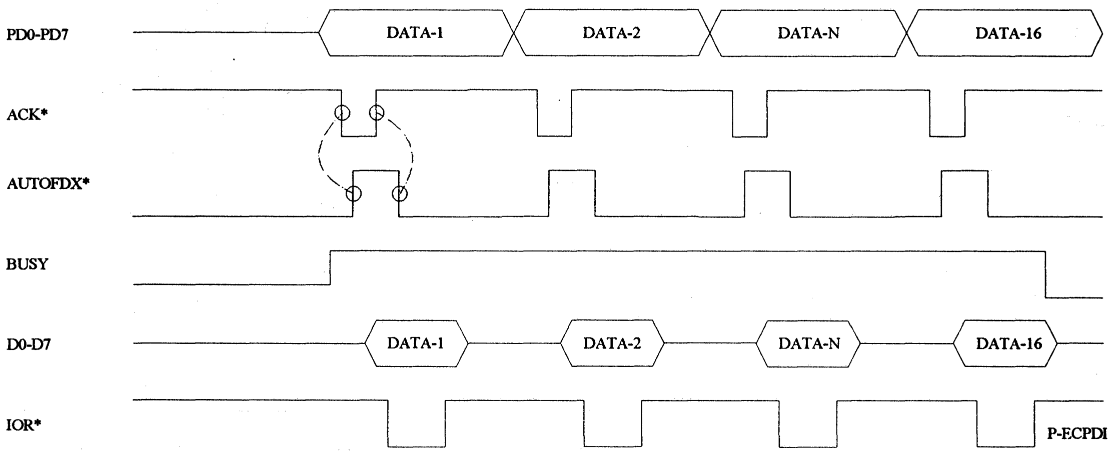
EPP MODE (MODE 100, WRITE ADDRESS, OUTMODE)



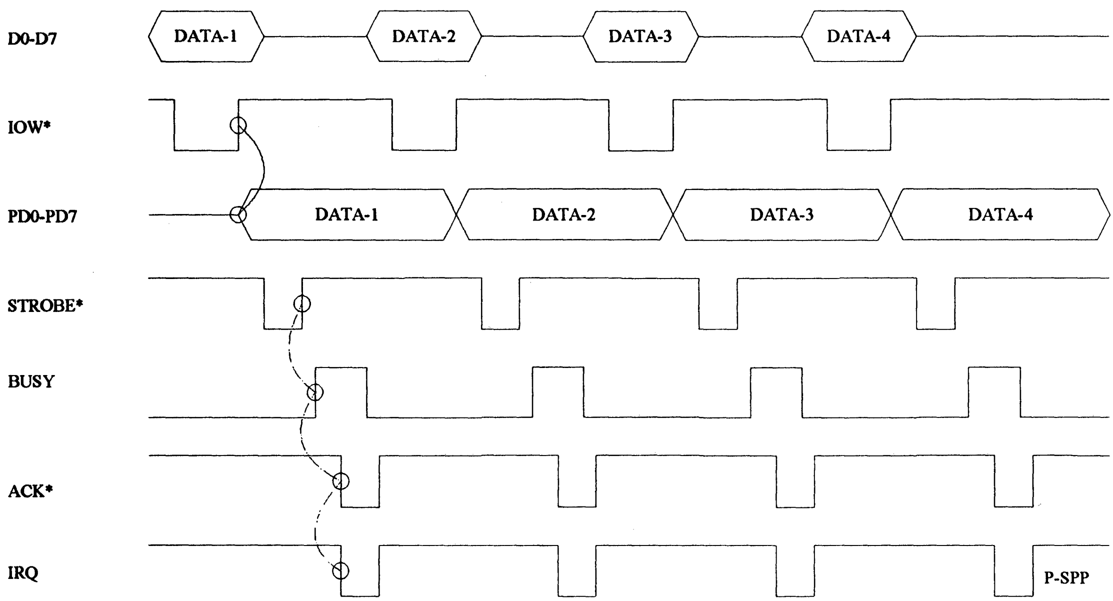
STANDARD CENTRONIC MODE (MODE 000)



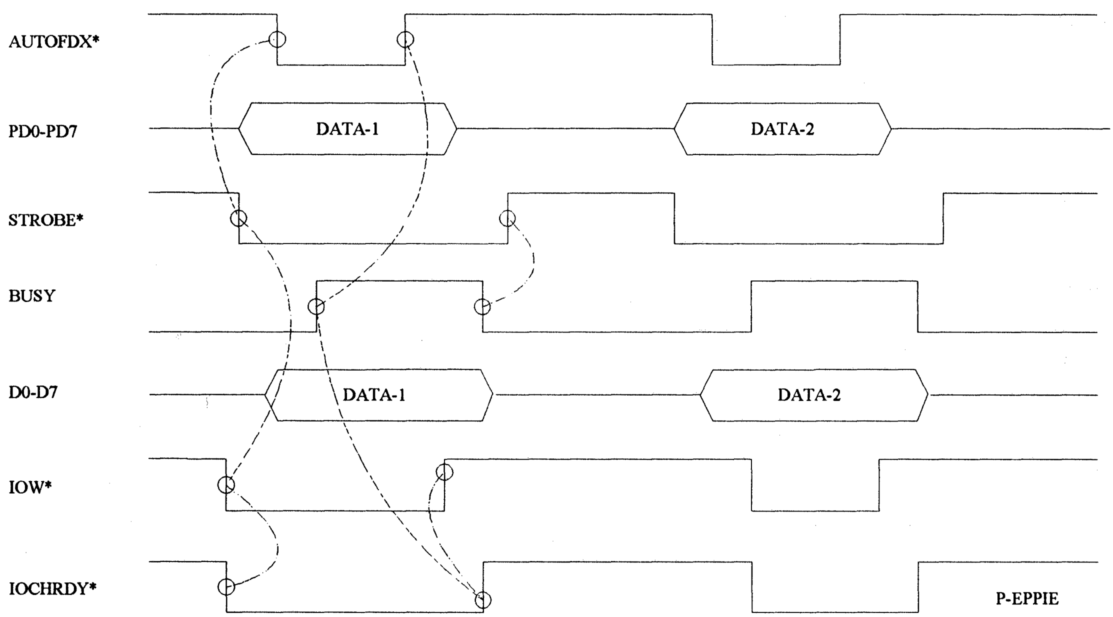
ECP MODE (MODE 011, DATA MODE OPERATION INPUT DIRECTION)



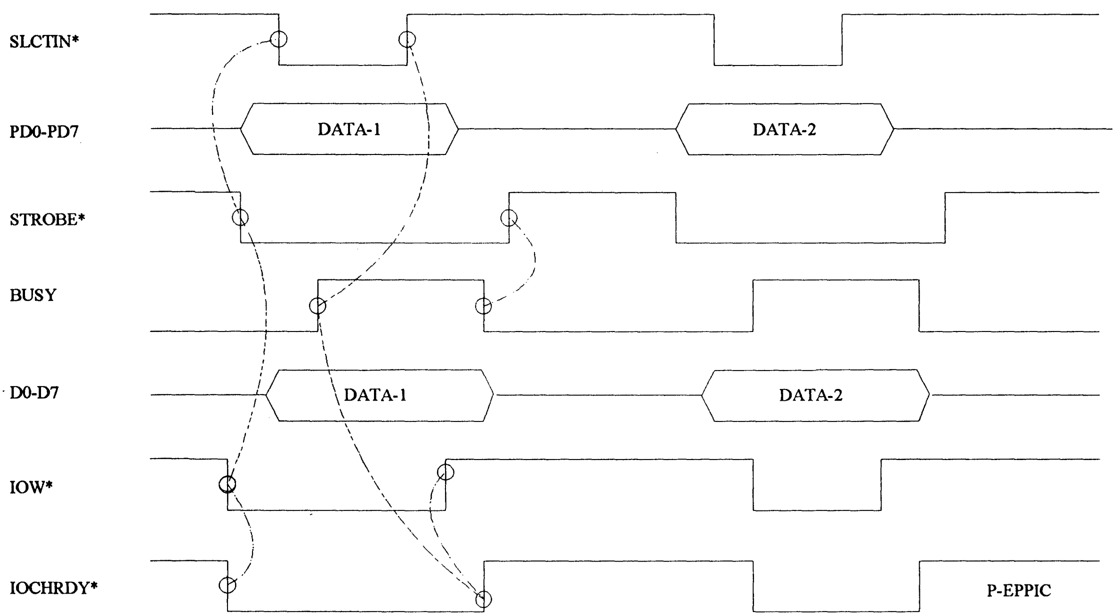
STANDARD CENTRONIC MODE (MODE 000)



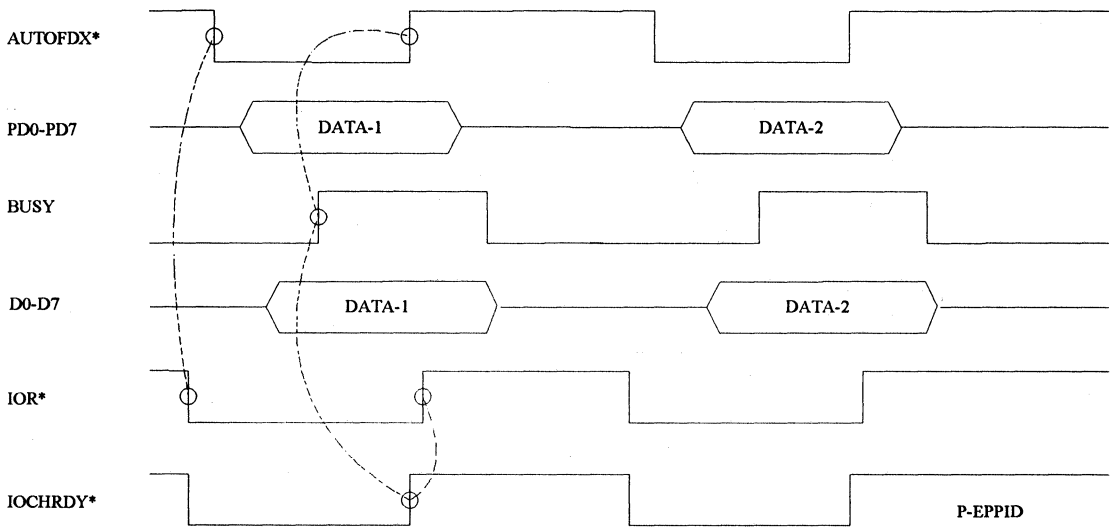
EPP MODE (MODE 100, WRITE DATA, OUTMODE)



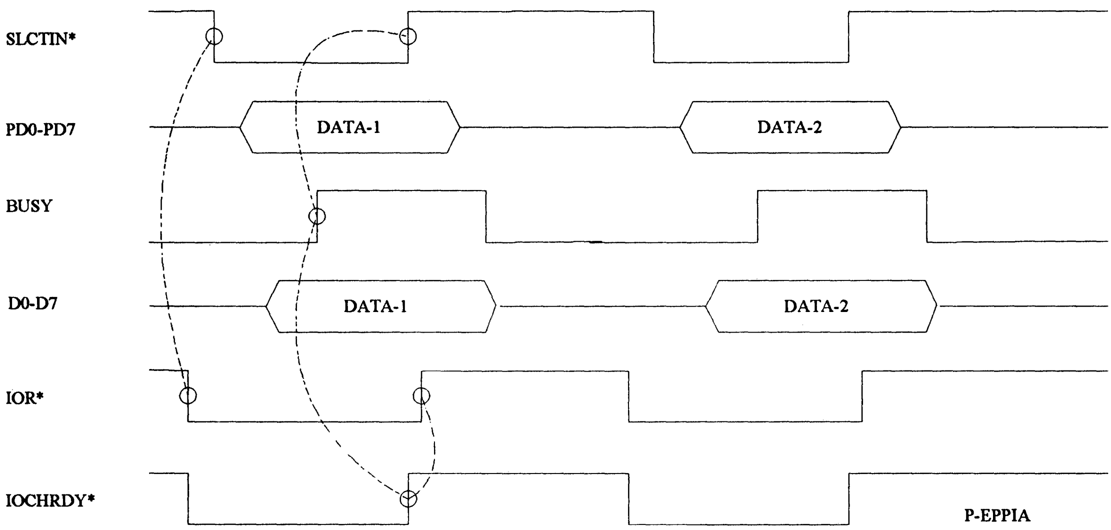
EPP MODE (MODE 100, WRITE ADDRESS, OUTMODE)



EPP MODE (MODE 100, DATA READ, INPUT MODE)



EPP MODE (MODE 100, ADDRESS READ, INPUT MODE)



STARTECH

An EXAR Company

ST84C01

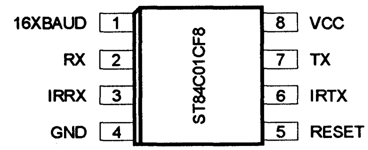
Printed August 3, 1995

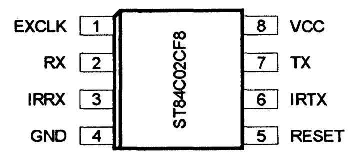
INFRARED ENCODER AND DECODER

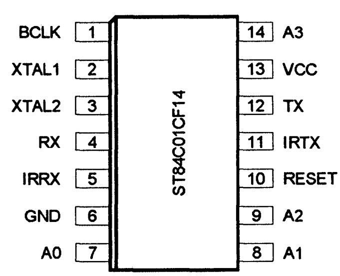
DESCRIPTION

The ST84C01/02 is a single channel Infrared encoder and decoder, designed for wireless peripheral communications. It meets the standard IrDa specification for wireless applications. The ST84C01 is offered with standard and programmable custom frequencies. The ST84C01 can interface directly to ST16C450 and ST16C550 products.
ST84C01/02 is designed in a 1.2μ process to achieve 115.2k baud transmission rate.

Plastic-DIP Package







FEATURES

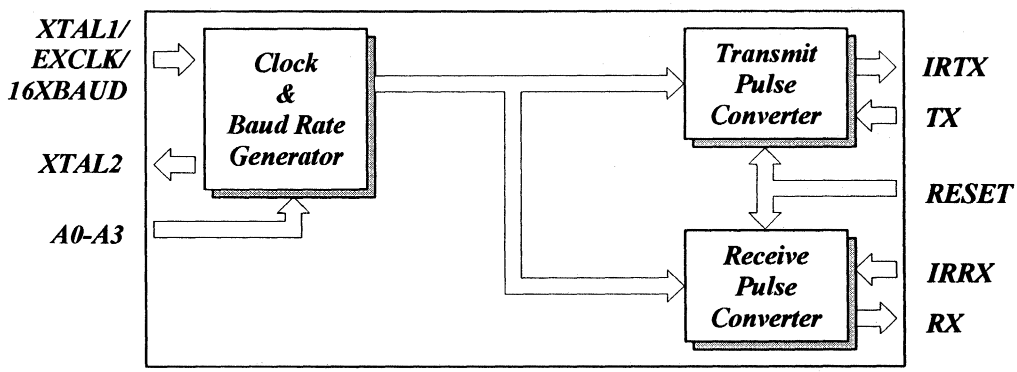
- Selectable transmit/receive bit rate
- Low power single 5V CMOS technology
- 8, 14 pin DIP or SOIC package.
- Crystal oscillator circuit on board

ORDERING INFORMATION

Part number	Package	Operating temperature
ST84C01CP8	Plastic-DIP	0 ° C to +70° C
ST84C01CF8	SOIC	0° C to +70° C
ST84C01CP14	Plastic-Dip	0° C to +70° C
ST84C01CF14	SOIC	0° C to +70° C
ST84C02CP8	Plastic-DIP	0 ° C to +70° C
ST84C02CF8	SOIC	0° C to +70° C

Rev. 1.0

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin 8	Pin 14	Signal Type	Pin Description
BCLK	-	1	O	Buffered clock output. To drive external UART clock.
XTAL1	1	2	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal reference clock. For external clock application, XTAL2 is left open or used as buffered clock output.
XTAL2	-	3	O	Crystal clock output.
RX	2	4	O	Receive data output. Standard UART data output for 8 bits wide word with 1 start and stop bits recovered from IRRX receive data.
IRRX	3	5	I	Infrared receive data input.
GND	4	6	O	Supply ground.
A0	-	7*	I	Address select 0. To select the internal preprogrammed data rates.
A1	-	8*	I	Address select 1. To select the internal preprogrammed data rates.
A2	-	9*	I	Address select 2. To select the internal preprogrammed data rates.
RESET	5	10	I	Reset input (active high). To reset internal counters, receiver and transmitter.
IRTX	6	11	O	Infrared transmit data output. Converted standard UART 8 bits wide word with 1 start and stop bit to IrDa specified pattern.
TX	7	12	I	Transmit data input. Standard UART data input for 8 bits wide word with 1 start and stop bits.
VCC	8	13	I	Positive supply input.
A3	-	14*	I	Address select 3. To select the internal preprogrammed data rates.

SYMBOL DESCRIPTION

Symbol	Pin 8	Pin 14	Signal Type	Pin Description
16XBAUD	1	-	I	16 X BAUD rate clock input (ST84C01). User selectable transmit and receive data rates. This pin can be connected to ST16C450/550 baud-out pin.

* Have internal pull-up resistors

DATA RATE SELECTION TABLE

A3	A2	A1	A0	BAUD RATE	DIVISOR
0	1	0	1	600	192
0	1	1	0	1200	96
0	1	1	1	2400	48
1	0	0	0	3600	32
1	0	0	1	4800	24
1	0	1	0	7200	16
1	0	1	1	9600	12
1	1	0	0	19.2k	6
1	1	0	1	38.4k	3
1	1	1	0	57.6k	2
1	1	1	1	115.2k	1

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0 - 70° C, VCC=5.0 V ± 10% unless otherwise specified.

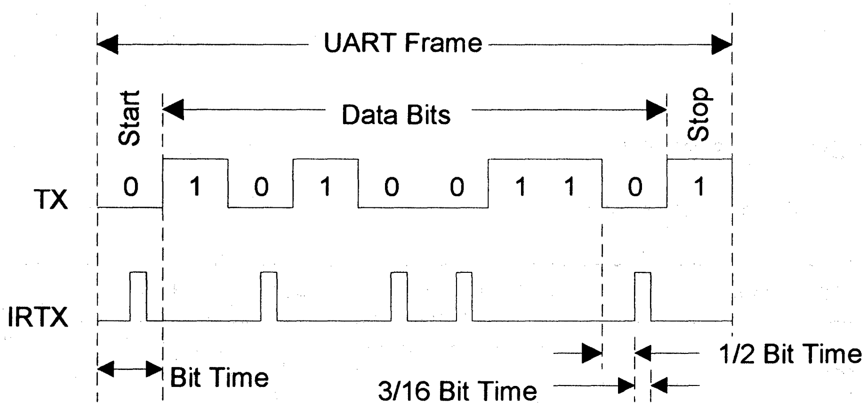
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 6.0 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 6.0 mA
I_{IL}	Input low current			-100	µA	Pin 3 only
I_{IH}	Input high current			1	µA	VIN=Vcc Pin 3
I_{CC}	Operating current		1	1.2	mA	No load.
R_{IN}	Input pull-up resistance	35	50	65	kΩ	

AC ELECTRICAL CHARACTERISTICS

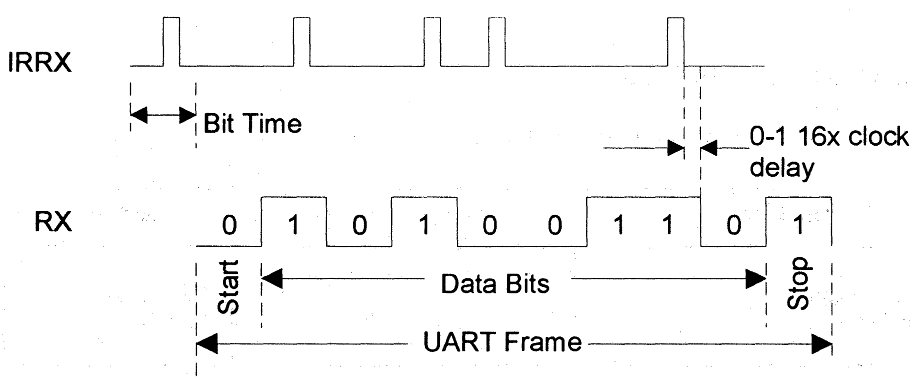
T_A=0 - 70° C, VCC=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	CLOCK rise time		1.5	2	ns	0.5V - 2.8V
T_2	CLOCK fall time		1.5	2	ns	2.8V - 0.5V

INFRARED TRANSMIT TIMING



INFRARED RECEIVE TIMING



16650-IR-1

STARTECH

An EXAR Company

ST84C72

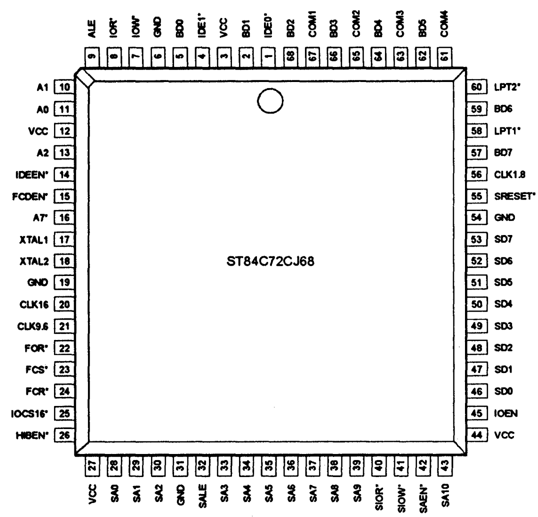
Printed August 3, 1995

IDE INTERFACE WITH I/O DECODE

DESCRIPTION

The ST84C72 is designed to replace all necessary TTL logics for 16 bit IDE interface and decode logic for floppy controller and serial / parallel I/O ports. A select pin is provided to select primary or secondary address for hard and floppy decodes. On board crystal oscillator circuit provides 16, 9, and 1.8461 MHz clock outputs for some floppy controllers and uart from 48 MHz external crystal connected to ST84C72.

PLCC package



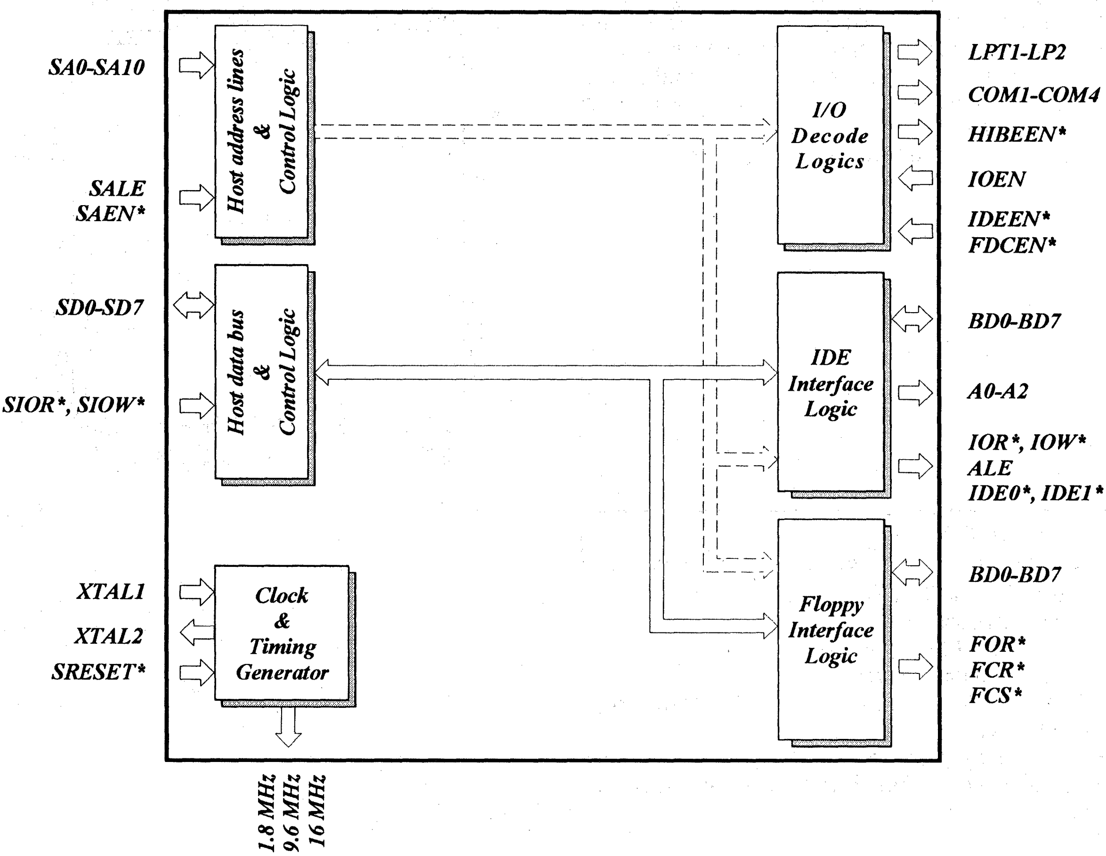
FEATURES

- Low power CMOS design
- Direct bus connect
- Replacement for more than 7 TTL parts
- High speed for new design
- Selectable I/O decode ports. (COM1-COM4, LPT1-LPT2)
- Floppy address decode
- Pin selectable primary and secondary address decodes

ORDERING INFORMATION

Part number	Package	Operating temperature
ST84C72CJ68	PLCC	0 ° C to +70 ° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
SA0-SA2	28-30	I	Host address lines A0-A2.
SA3-SA9	33-40	I	Host address lines A3-A9.
SA10	43	I	Host address line A10.
SALE	32	I	Host address latch enable (active high).
SAEN*	42	I	Host address enable (active low). All decoded addresses are valid when SAEN* is low.
SIOW*	41	I	Host I/O write signal input (active low). Buffered data bus (BD7-BD0) are gated with SIOW*, SIOR* and I/O decoded addresses to insure proper valid data time slots.
SIOR*	40	I	Host I/O read signal input (active low).Buffered data bus (B07-BD7) are gated with SIOR*, SIOW* and I/O decoded addresses to insure proper valid data time slots.
SD0-SD7	46-53	I/O	Host data bus.
SRESET*	55	I	Host system reset (internally pulled up, active low). This pin is used to set internal clock dividers to known state. For normal operation this pin should be left open or connected to VCC.
XTAL1	17	I	Crystal or external clock input. A crystal can be connected between XTAL1 and XTAL2 with some additional filters to generate 48 Mhz clock frequency for floppy controller and UART clock . This pin can be connected to VCC or GND if CLK16, CLK9.6 and CLK1.8 are not used.
XTAL2	18	O	Crystal output. This pin should be left open if external clock is used to connect to XTAL1 or clock is not used.
LPT1*	58	O	Line printer enable (active low). Primary printer enable signal. Decoded for address 378 Hex (LPT1).
LPT2*	60	O	Line printer enable (active low). Secondary printer enable signal. Decoded for address 278 Hex (LPT2).

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
COM1*	67	O	Serial communication select pin (active low). Decoded for 3F8 Hex (COM-1).
COM2*	65	O	Serial communication select pin (active low). Decoded for 2F8 Hex (COM-2).
COM3*	63	O	Serial communication select pin (active low). Decoded for 3E8 Hex (COM-3).
COM4*	61	O	Serial communication select pin (active low). Decoded for 2E8 Hex (COM-4).
CLK1.8	56	O	1.8461 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 26). This clock can substitute the standard 1.8432 Mhz serial communication clock.
IOEN	45	I	Serial and parallel port access. Connecting this pin to pin 44 (RDOUT) of the ST16C452, ST16C552, or ST16C553 enables the BD0-BD7 to access the serial and parallel ports. This pin should be tied to GND if external serial/ parallel ports are not used.
FDCEN*	15	I	Floppy controller enable/disable (internally pulled up). Floppy controller select is disabled when this pin is left open or connected to VCC. Floppy controller can be selected when this pin is connected to host SA7 pin (primary selection address 3F7, 3F5, 3F4 and 3F2 Hex) or A7* output pin of the ST84C72 (secondary selection address 377, 375, 374 and 372 Hex).
FOR*	22	O	Floppy controller address decode (372/3F2 Hex).
FCS*	23	O	Floppy controller address decode (377/3F7 Hex).
FCR*	24	O	Floppy controller address decode (374-5/3F4-5 Hex).
CLK16	20	O	16 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divided by 3).

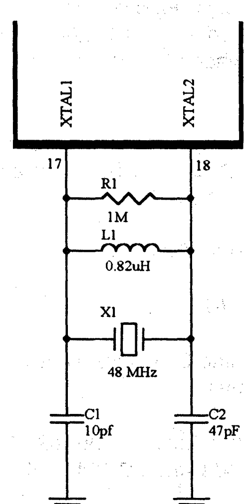
SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CLK9.6	21	O	9.6 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 5).
IOCS16*	25	I	IDE 16 bit data transfer enable (internally pulled up, active low). This pin enables the external 74LS245 bus driver (HIBEN*) when IDE port is selected and 16 bit data transfer is required.
IDEEN*	14	I	IDE Enable/Disable (internally pulled up). IDE select is disabled when this pin is left open or connected to VCC. IDE controller can be selected when this pin is connected to A7* output pin of the ST84C72 (primary selection address 3F0-3F7 and 1F0-1F7 Hex) or host address line SA7 (secondary selection address 370-377 and 170-177Hex).
IDE1*	4	O	IDE drive/register select-1 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 3F6 or 3F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE1* is enabled when I/O port address 376 or 377 Hex is accessed.
IDE0*	1	O	IDE drive/register select-0 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 1F0-1F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE0* is enabled when I/O port address 170-177 Hex is accessed.
HIBEN*	26	O	High order data bus enable. This pin enables the external 74LS245 data buffer (host SD8-SD15) when IOCS16* is active and IDE port is selected.
A0-A1	11-10	O	Buffered host addresses A0 and A1.
A2	13	O	Buffered host address A2.
A7*	16	O	Inverted host address line SA7. This pin is used to primary IDE and floppy controller.
BD3-BD0	5,2,68,66	I/O	Buffered LSB of low order host data bus (SD0-SD3). These bits are set to input mode when SIOW* is low.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
BD4-BD6	64,62,59	I/O	Buffered MSB of low order host data bus (SD4-SD6). These bits are set to input mode when SIOW* is low.
BD7	57	I/O	Buffered host data bit -7 (SD7). This bit goes to high impedance when address 3F7 or 1F7 Hex is accessed during I/O read operation. BD7 is set to input mode when SIOW* is low.
ALE	9	O	Buffered host address latch (SALE).
IOR*	8	O	Buffered host I/O read signal (HIOR*).
IOW*	7	O	Buffered host I/O write signal (HIOW*).
GND	6,19,31,54	O	Signal and power ground.
VCC	3,12,27,44	I	Power supply input.

Optional external filter.



ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 16 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -16 mA
I_{CC}	Avg power supply current			15	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

TELECOMMUNICATIONS 5

Index

STARTECH
An EXAR Company

Preliminary Information

ST88C870

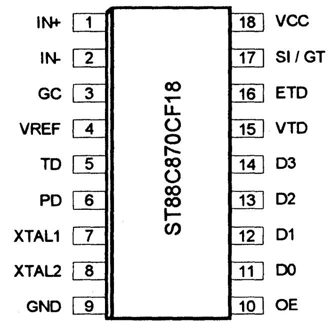
Printed August 3, 1995

INTEGRATED DTMF RECEIVER

DESCRIPTION

The ST88C870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three state bus interface.

SOIC Package



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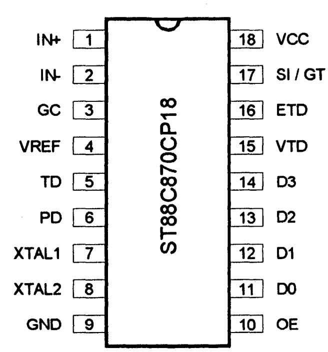
FEATURES

- complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Pin-To-Pin and functional compatible with Mitel MT8870

Plastic Dip Package



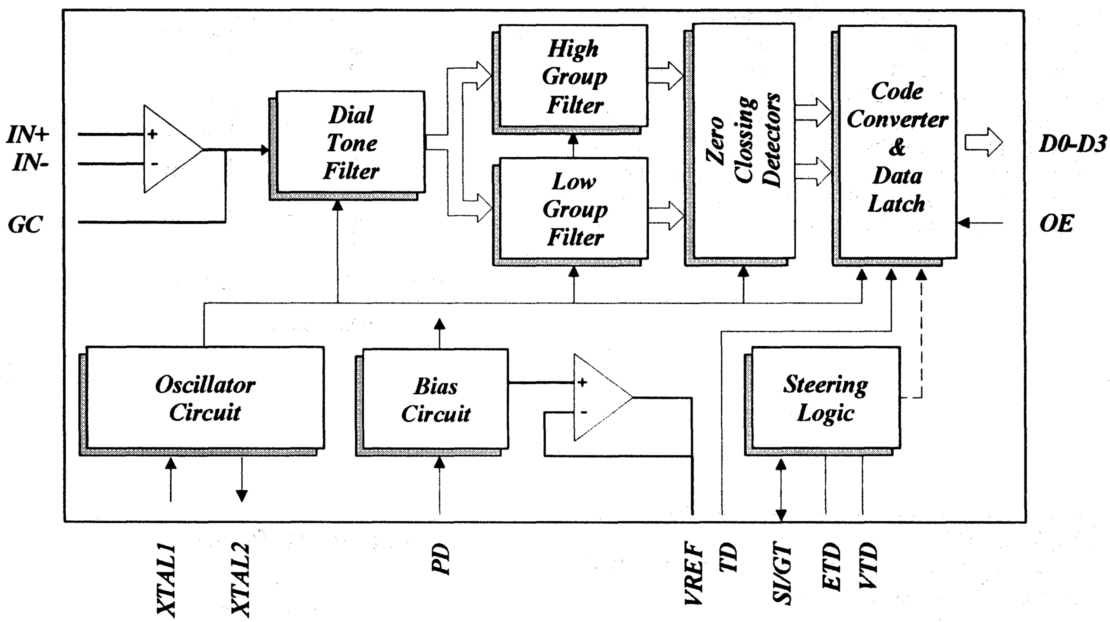
ORDERING INFORMATION

Part number	Package	Operating temperature
ST88C870CP18	Plastic-DIP	0° C to + 70° C
ST88C870CF18	SOIC	0° C to + 70° C

***Industrial operating range are available.**

Rev. 1.0

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
IN+	1	I	Non-Inverting Op-Amp input.
IN-	2	I	Inverting Op-Amp input.
GC	3	I	Gain adjustment. Op-Amp output of front end differential amplifier for connection of feedback resistor.
Vref	4	O	Reference Voltage Output, Nominally set to half supply voltage, is used to bias inputs at mid-rail
TD	5**	I	Tone disable. Logic high inhibits the detection of tones representing characters A, B, C and D.
PD	6**	I	Power Down (active high). Powers down the device and inhibits the oscillator.
XTAL1	7	I	Crystal oscillator, or External clock input pin. A 3.579545 MHz crystal connected between XTAL1 and XTAL2 completes the internal oscillator circuit.
XTAL2	8	O	Crystal oscillator output pin.
GND	9	O	Supply ground pin.
OE	10*	I	Output Enable (active high). To enable / disable the D0-D3 outputs.
D0-D3	11-14	O	Data outputs. When enabled by OE, provide the code corresponding to the last valid tone pair received. When OE is low, the data outputs are three stated.
VTD	15	O	Valid Tone detection signal. Presents a logic high when a received tone pair has been registered and the output latch updated, returns to Logic low when the voltage on SI/GT falls below Vtst.
ETD	16	O	Early Tone detection. Presents a logic high once the digital algorithm has detected a valid tone pair. Any momentary loss of signal condition will cause ETD to return to a logic low.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
SI/GT	17	I/O	Steering Input / Guard time (Output) Bidirectional. A voltage greater than Vtst detected at SI causes the device to register the detected tone pair and update the output latch. A voltage less than Vtst frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant; its state is a function of ETD and the voltage on SI.
VCC	18	I	Most positive power supply. Typically 5 Volts.

* = Internal pull-up resistor
** = Internal pull-down resistor

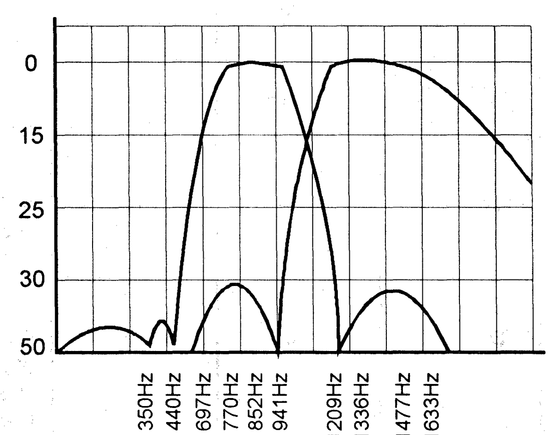
FILTER SECTION

Separation of the low group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order RC smoothing filter section which smoothes the signals prior to limiting. Limiting is performed by high gain compactors which are provided with hysteresis to prevent detection of unwanted low level signals. The outputs of the compactors provide full rail logic swings at the frequencies of the incoming DTMF signals.

DECODER SECTION

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies and noise.

When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the ETD output will go to an active state. Any subsequent loss of signal condition will cause ETD to assume an inactive state.



FUNCTIONAL DECODING TABLE:

KEY	OE	CE	ETD	D3	D2	D1	D0	FL	FH
ANY	L	X	H	Z	Z	Z	Z		
1	H	X	H	0	0	0	1	697	1209
2	H	X	H	0	0	1	0	697	1336
3	H	X	H	0	0	1	1	697	1477
4	H	X	H	0	1	0	0	770	1209
5	H	X	H	0	1	0	1	770	1336
6	H	X	H	0	1	1	0	770	1477
7	H	X	H	0	1	1	1	852	1209
8	H	X	H	1	0	0	0	852	1336
9	H	X	H	1	0	0	1	852	1477
0	H	X	H	1	0	1	0	941	1209
*	H	X	H	1	0	1	1	941	1336
#	H	X	H	1	1	0	0	941	1477
A	H	X	H	1	1	0	1	697	1633
B	H	X	H	1	1	1	0	770	1633
C	H	X	H	1	1	1	1	852	1633
D	H	X	H	0	0	0	0	941	1633
A	H	H	L	***The output code will remain the same as the previous detected code.***					
B	H	H	L						
C	H	H	L						
D	H	H	L						

STEERING CIRCUIT

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ETD. A logic high on ETD causes **Vcx** (Fig. 1,2) to rise as the capacitor discharges. Provided signal condition is maintained (ETD remains high) for the validation period (T12) **Vcx** reaches the threshold (ETD) of the steering logic to register the tone pair, latching its corresponding 4-bit code into the output latch. At this point the GT output is activated and drives **Vcx** to Vcc. GT continues to drive high as long as ETD remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag STD goes high, signaling that a received tone pair has been registered.

The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

GUARD TIME ADJUSTMENTS

In many situations not requiring selection of tone duration and interdigit pause, the simple steering circuit shown in is applicable.

Component values are chosen according to the formula:

$$T14 = T12 + T4$$
$$T16 = T13 + T5$$

$$T4 = (RpCx) \ln [VCC / (VCC-Vcx)]$$
$$T5 = (R1Cx) \ln (VCC / Vcx)$$
$$Rp = (R1R2) / (R1+R2)$$

- Decreasing T4 (T4 < T5) Fig. 2
- Decreasing T5 (T4 > T5) Fig. 1

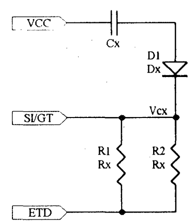


Figure 1.

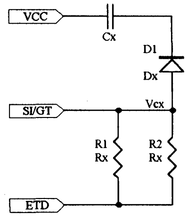


Figure 2.

The value of T12 is a device parameter and T14 is the minimum signal duration to be recognized by the receiver (see timing diagram). A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (T4) and tone absent (T5). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing T14 improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, relatively short T14 with a long T17 would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required.

POWER DOWN MODE

A logic high applied to PD will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the TD. It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code.

DIFFERENTIAL INPUT CONFIGURATION

The input arrangement of the ST88C870 provides a differential input operational amplifier as well as a bias source (Vref) which is used to bias the inputs at mid rail. Provision is made for connection of a feedback resistor to the op-amp output (GC) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in Figure 4 with the op-amp connected for unity gain and Vref biasing the input at VCC/2.

Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R3.

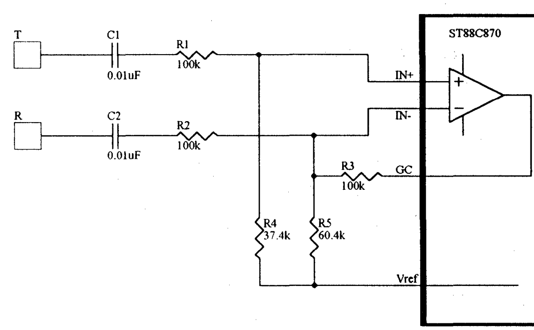


Figure 3.

R4 = (R3R5) / (R3+R5)
Voltage gain = R3 / R2

$$Z\ in = 2\sqrt{R2^2 + (1 / WC)^2}$$

CRYSTAL OSCILLATOR CIRCUIT

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 4 (Single-Ended Input Configuration). However it is possible to configure several ST88C870 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30pF capacitor to the oscillator input (XTAL1) of the next device Figure 5. Subsequent devices are connected in a similar fashion. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

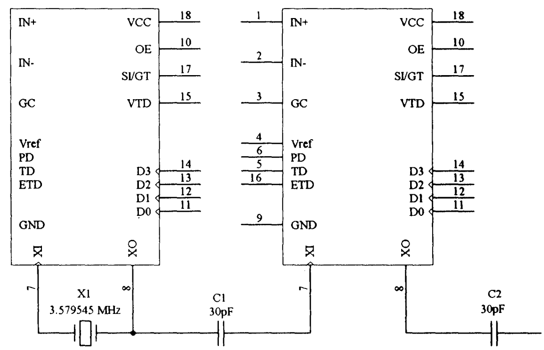
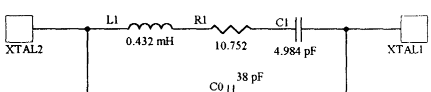


Figure 5.

CRYSTAL OSCILLATOR SPECIFICATIONS

$F = 1 / (2\pi \sqrt{(L1\ C1)}$
$L1 \approx 0.532$ mH
$C1 \approx 4.984$ pF
$R1 \approx 10.752\ \Omega$
$C0 = 38$ pF
$Q = 896$



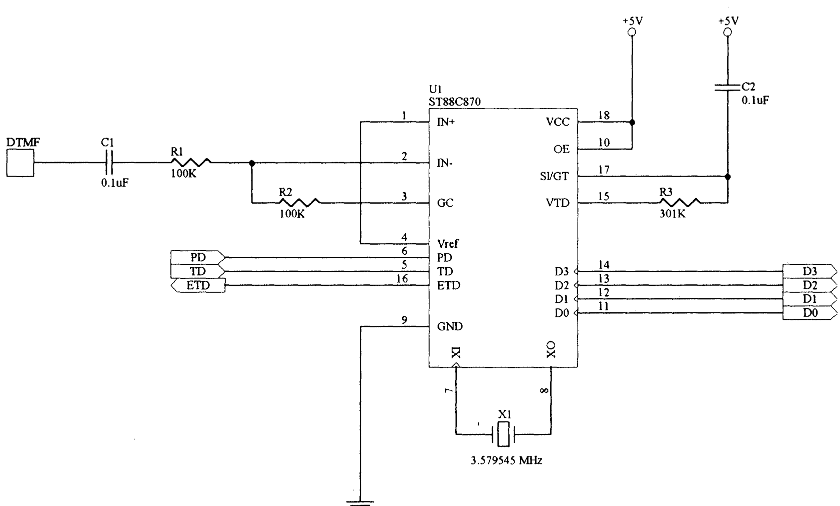


Figure 4.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

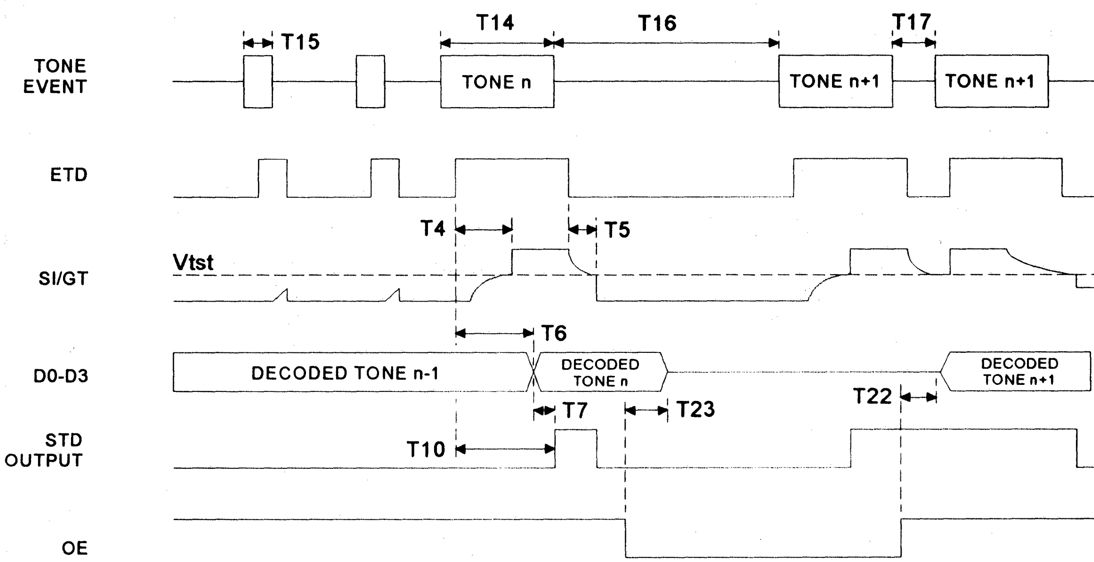
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		5	10	mA	
I_{STD}	Standby current		10	25	μA	
I_{IL}	Input leakage			±10	μA	
I_{CL}	Clock leakage			±10	μA	
R_{IIL}	Input leakage current		0.1		μA	
I_{UP}	Input pull-up current		10	20	μA	
I_{DN}	Input pull-down current		15	40	μA	
R_{IN}	Input impedance		10		MΩ	
V_{VT}	Threshold voltage	2.2	2.4	2.5	V	
V_{REF}	Vref output voltage	2.3	2.5	2.7	V	
V_R	Vref output resistance		1		kΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Input clock frequency		3.5795		MHz	
T_2	Input clock duty cycle	40	50	60	%	
T_3	Clock rise/fall time			110	ns	
T_6	Propagation delay SI to D0-D3		8	16	µs	
T_7	Propagation delay D0-D3 to STD		8	16	µs	
T_8	Power down time		20		ms	
T_9	Power up time		30		ms	
T_{10}	Propagation delay SI to STD		12	16	µs	
T_{12}	Tone present detect time	5	11	14	ms	
T_{13}	Tone absent detect time	0.5	4	8.5	ms	
T_{14}	Tone duration accept			40	ms	
T_{15}	Tone duration reject	20			ms	
T_{16}	Interdigit pause accept			40	ms	
T_{17}	Interdigit pause reject	20			ms	
T_{19}	Propagation delay		8	16	µs	
T_{21}	Output data setup time		3.4		µs	
T_{22}	Propagation delay OE to D0-D3 disable		50		ns	
T_{23}	Propagation delay OE to D0-D3 enable		300		ns	

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3.Tone duration=40 ms,tone pause=40ms.
6.Signal condition consists of nominal DTMF frequencies.
S.Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 400 Hz) ±2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.



T15
T14
T16
T17
TONE EVENT
TONE n
TONE n+1
TONE n+1
ETD
T4
T5
Vtst
SI/GT
T6
D0-D3
DECODED TONE n-1
DECODED TONE n
DECODED TONE n+1
T7
T23
T22
STD OUTPUT
T10
OE

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STARTECH

An EXAR Company

Preliminary Information

ST56CXXX

Printed August 3, 1995

ADVANCED HIGH PERFORMANCE SUPER-I/O CONTROLLER

DESCRIPTION

The ST56C5XX is an advanced high performance super-I/O controller, designed to replace the IDE controller, four Floppy controllers, two serial ST16C550 UART's with advanced Microsoft/Hewlett Packard ECP, IBM EPP printer port and game port. The ST56C5XX utilizes digital phase locked loop for the floppy controller section to eliminate the external components (except the main crystal). The ST56C5XX is optimized for mother board applications as well as controller board applications. ST56C5XX provides high ESD circuits on the printer data bus and I/O to prevent damage caused by the printer being powered when the ST56C5XX is not powered.

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FEATURES

- Licensed CMOS WD37C65C floppy controller.
- Supports vertical recording format
- 100% IBM compatible
- 48 mA drivers and schmitt Trigger inputs.
- DMA enable logic
- FDC primary and secondary address selection
- Two 16C550 serial ports
- Microsoft/Hewlett Packard Bi-directional ECP parallel port
- IBM EPP (Enhanced Printer Port)
- 16 bit IDE interface and decode logic
- Game port
- 100 pin TQFP and QFP packages
- Low power CMOS 1.2μ technology

ORDERING INFORMATION

Part number	Package	Operating temperature
ST56CXXXCQ100	QFP	0° C to + 70° C
ST56CXXXCTQ100	TQFP	0° C to + 70° C

STARTECH

An EXAR Company

Preliminary Information

ST16C554E

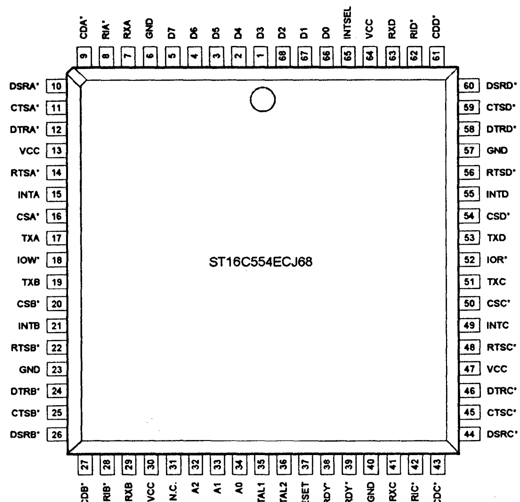
Printed August 3, 1995

QUAD ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C554E is a universal asynchronous receiver and transmitter with 64 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.
The ST16C554E is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C554E on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C554E provides internal loop-back capability for on board diagnostic testing.
The ST16C554E is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

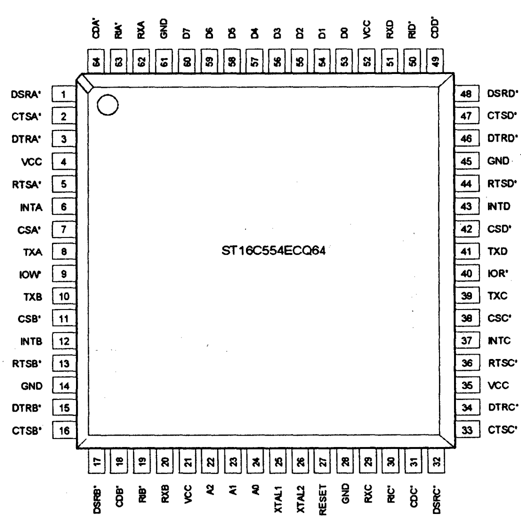
PLCC Package



FEATURES

- Pin to pin and functional compatible to ST16C554
- 64 byte transmit FIFO
- 64 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

QFP Package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554ECQ64	QFP	0° C to + 70° C
ST16C554EDCQ64	QFP	0° C to + 70° C
ST16C554EDCJ68	PLCC	0° C to + 70° C
ST16C554EDIJ68	PLCC	-40° C to + 85° C

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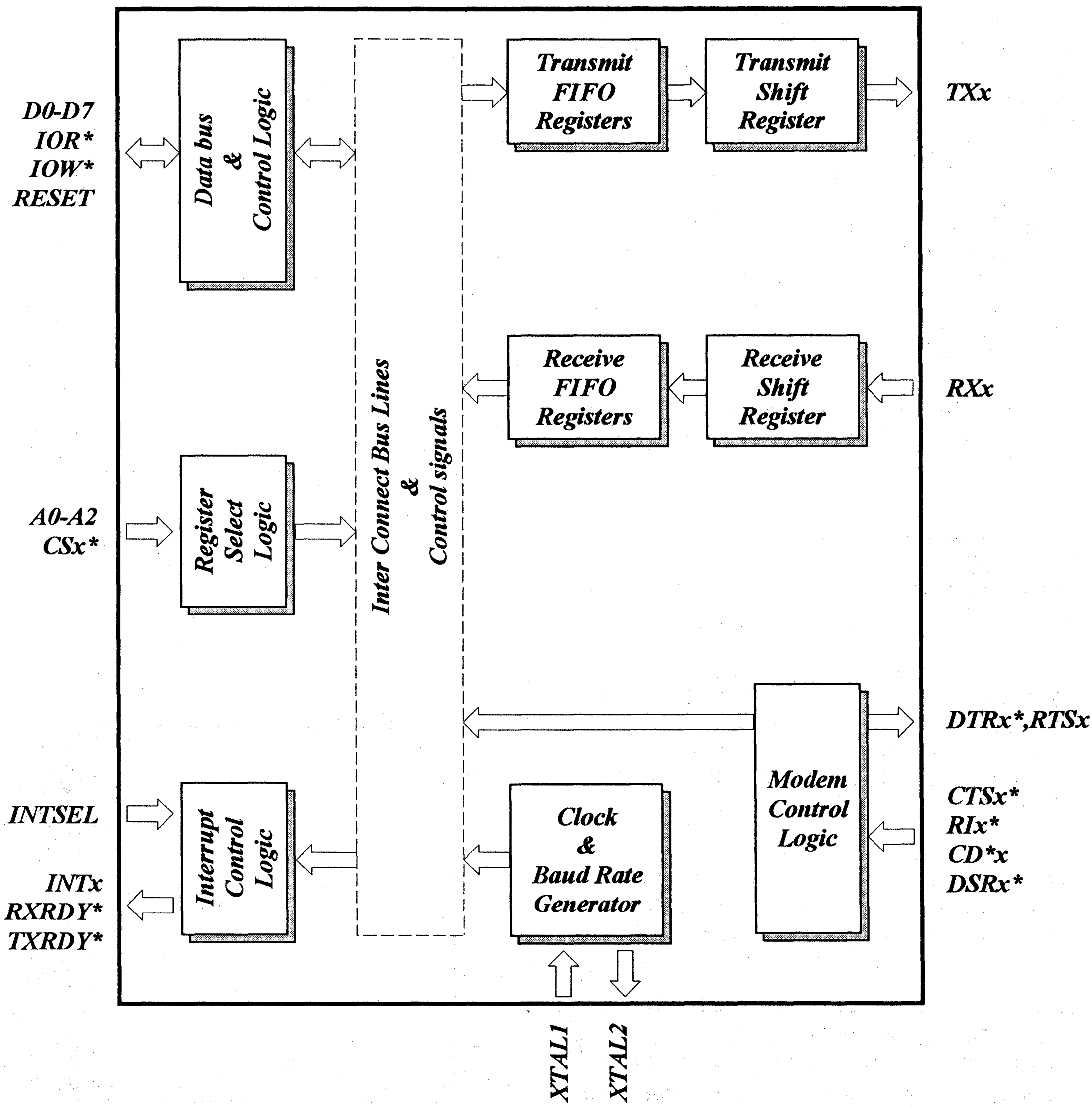
Rev. 1.0

BLOCK DIAGRAM



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CLOCK APPLICATION NOTES

GENERAL APPLICATION NOTE FOR STARTECH CLOCK FAMILY

The ST49CXXX video / memory clock chips provide 5-130 MHz clock outputs which may cause unwanted EMI problems.
To minimize problems with meeting FCC EMI requirements, consideration should be given to the following sections of the board design.

Power supply conditioning
Printed Circuit Board Layout
Video / Memory clock outputs and drive capabilities
External clock sources
Reference clock sources
Digital control / select inputs
External loop filters

Power supply considerations
Under normal conditions no external components are required for propper operation of any of the internal circuitry of the ST49CXXX. It is required to have spike free (or minimum) and stable supply source to the chips. To provide stable and clean supply voltage to STARTECH clock chips we recommend to use 0.1μF capacitors close to IC's power supply lines (VCC, AVCC and DVCC inputs). Analog and digital supply lines are separated from each other to reduce noise generated due to internal digital switching.
In most of the design cases +5V and +12V supplies are provided. A clean +5V supply can be obtained from the +12V supply by utilizing a 470Ω drop resistor and 5.1V zener diode bypassed by 0.047μF and 2.2μF Tantalum capacitors (or higher) to ground.
Trace width should be maximized from the supply source and good ground planes on top and bottom layers of the printed circuit board are recommended.

Printed Circuit Board (PCB) layout
We recommend to place all external components as close as possible to the clock chips to reduce trace length between pin and component connections. It is important to keep components not related to clock IC's (DRAM and other memory devices) far and not share the grounds. In applications utilizing a multi-layer board, GND, AGND, and DGND should be directly connected to the ground plane. If possible A full power and ground plane layout should be employed both under and around the IC package.

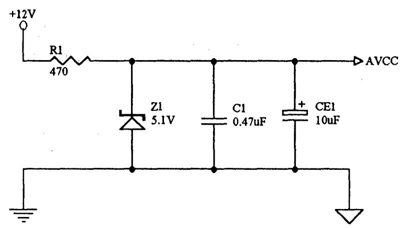
Video / Memory clock outputs and drive capabilities
Video clock is usually the highest frequency present in video graphics system board/card and consideration should be given to FCC EMI requirements.
The trace connecting DCLK and MCLK clock output pins to other components should be kept as close as possible (with optional 33Ω resistor in series) to reduce the possible emitting signals and jitter.

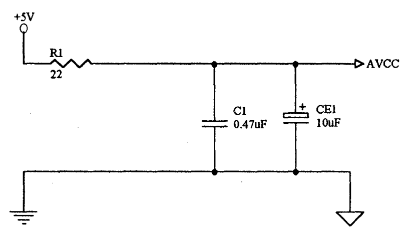
External clock sources
When an external clock source is used to bypass the internal VCO to DCLK and MCLK outputs, clock should have fast rise / fall times and minimum jitter. This signal will be connected internally to the clock output pin when it is selected / enabled. The internal VCO circuit will be locked to its internal selected frequency.

Reference clock sources
The internal oscillator circuit contains all of the passive components required for the external crystal. An appropriate parallel resonant crystal should be connected between XTAL1 and XTAL2.
The crystal leads and input pins should be maintained as close as possible, and the body of the crystal should be grounded to minimize the noise pickup. For IBM compatible applications, the 14.31818 MHz system or crystal clock is used as a reference clock to the chip.

Digital control / select inputs
The ST49CXXX provides TTL compatible address select and latch input pins to interface with CMOS or TTL / LSTTL devices. The A0-A4 and M0-M1 can also be connected to the Data bus if required.

APPLICATION NOTES





UART APPLICATION NOTES

GENERAL APPLICATION NOTE FOR STARTECH UART FAMILY

The AN-450 provides additional information to guide users to design or utilize the STARTECH product line. This document can also be used for all the STARTECH UART product lines.

GENERAL INFORMATION

STARTECH offers UART's with or without FIFO capabilities, and are marked as 45X for non FIFO families and 55X for FIFO families. All parts with sharing part numbers are foot print compatible in some extent, like ST16C450 and ST16C550, ST16C2450 and ST16C2550, etc.

This section will describe general terms for commonly used flags and registers.

OVERRUN ERROR:
The flag is set to "1" to warn the user that a serial data has been received and previous serial data has not been read from receive holding register. The new serial data will over write the previous data in the receive holding register. Note that previous serial data has been lost and user does not have an access to that data.

PARITY ERROR:
This flag is set "1" to indicate that received serial data contains mismatched parity or data bit error in the received data.

PARITY:
Four common types of parities are used in the STARTECH Uart families; Odd Parity, Even Parity, Forced Mark Parity and Forced Space Parity.

ODD PARITY:
Odd Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the total count an odd number.

Example -1: A data byte with the following pattern 11010010 will require to add a parity bit of "1" to bring the total count for "1's" to an odd number. Based on this data pattern, serial data with odd parity will be transmitted as 110100101.

Example -2: A data byte with the following pattern 10011000 will require to add a parity bit of "0" to maintain the total count of "1's" to an odd number. Based on this data pattern serial data with odd parity will be transmitted as 100110000.

EVEN PARITY:
Even Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the count an even number.

Example -3: A data byte with the following pattern 10000101 will require to add a parity bit of "1" to bring the total count for "1's" to an even number. Based on this data pattern, serial data with even parity will be transmitted as 100001011.

Example -4: A data byte with the following pattern 00001111 will require to add a parity bit of "0" to maintain the total count for "1's" to an even number. Based on this data pattern, serial data with even parity, will be transmitted as 000011110.

FORCED SPACE PARITY:
Parity bit on the serial byte is set to "0" regardless of total number of "1's" (even or odd counts).

FORCED MARK PARITY:
Parity bit on the serial byte is set to "1" regardless of total number of "1's" (even or odd counts).

FRAMING ERROR:
The flag is set to "1" to indicate that received data does not have correct start or stop bits. This can cause when the Uarts are set for 8-bits word and receiving a serial data of 7-bits word or any mismatched data patterns.

BREAK SIGNAL INDICATION:
This flag is set to "1" to warn the user that transmitter is sending continuous "0" data without stop bit (RX input is low for more that one word).

TRANSMIT/RECEIVE FIFO:
STARTECH offers 16 byte transmit FIFO and 16 byte receive FIFO for all its products with 55X part numbers. These FIFO's are static 19 X 16 bit RAM with control logic to form a ring counter. Initializing the FIFO will set the write and read pointers to the same location.

TRANSMIT EMPTY:
This flag is set "1" to indicate that, there is no character in the transmit holding and transmit shift register

TRANSMIT HOLDING EMPTY:
This flag is set "1" to indicate that, there is one or more empty locations in the transmit holding register. User has to check this bit before loading characters in the transmit holding register. In non FIFO mode, user can load one character at a time when this flag is set and 16 characters when FIFO mode is utilized.

RECEIVER DATA READY:
This bit is set "1" to indicate that, receiver has one or more character in the receive holding register. User has to check this bit prior to read receive holding register. In non FIFO mode, only one character at time can be read. In FIFO mode up to 16 characters can be read if time bit is set.

RECEIVE TIME-OUT:
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -7: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -8: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

BAUD RATE GENERATOR:
STARTECH provides a 16 bit digital divider to obtain all necessary baud rates. The 16 bit divider is broken down in to two 8-bit dividers which will be addressed as MSB divider (upper 8-bits) and LSB divider (lower 8-bits). To calculate the transmit/receive data rate it is necessary to know the provided clock rate (frequency) to STARTECH parts. STARTECH utilizes 16 clocks for each transmit bit and 16 clocks to sample the received data. Note that inorder to access these dividers, user has to enable the divisor latch access bit through the Line Control Register.

Bit rate is calculated by:
Dividing decimal number = (Clock rate) / (16 X bit rate).
To program the digital divider, dividing decimal number should be converted to hex (base 16) number and split into two 8-bits sections.

Example -5: To obtain 4800 Hz baud rate, assuming 1.8432 MHz input clock, the dividing decimal value is (input clock=1843200) / (16 X 4800) = 24

24 decimal = 0018 Hex, this value is translated to MSB = 00 Hex and LSB = 18 Hex.

BAUD RATE VERSUS BIT RATE:
The baud rate defines the width of each bit regardless of word, parity and stop bit length. Bit rate, is the rate of the transmission which each character is transmitted or received. The 2400 baud rate transmission is translated to 2400 Hz per bit for each character in a word. With 2400 baud you can transmit between 7 to 12 characters per slot.

PROGRAMMING STEPS:
The AN-450 provides the easy steps to program STARTECH Uart family. Note that all numbers are in Hex format not decimal.

Write 80 Hex to **LCR** (**L**ine **C**ontrol **R**egister) to enable baud rate generator divider latch
to set 2400 Hz baud rate:
write 00 Hex to MSB of baud rate generator (address location 1).
Write 30 Hex to LSB of baud rate generator (address location 0).

Select you word, parity and stop bit format from STARTECH Uart data sheet.
to set 8 bits, no parity and one top bit and disable the divisor access latch
write 03 Hex to **LCR** (**L**ine **C**ontrol **R**egister):

if you need to use Uarts with FIFO, select your receive trigger level from data sheet.
to enable FIFO with 14 character trigger level
write CF Hex to **FCR** (FIFO **C**ontrol **R**egister)

enable interrupt sources
write 01 Hex to **IER** (**I**nterrupt **E**nable **R**egister) to select receive interrupt.

to set RTS and DTR outputs to low and enable the interrupt output
write 0B Hex to **MCR** (**M**odem **C**ontrol **R**egister).

The STARTECH Uart is ready for transmit and receive operation.

Read **MSR** (**M**odem **S**tatus **R**egister) to check the status of **CD, RI, DSR, CTS** input pins.

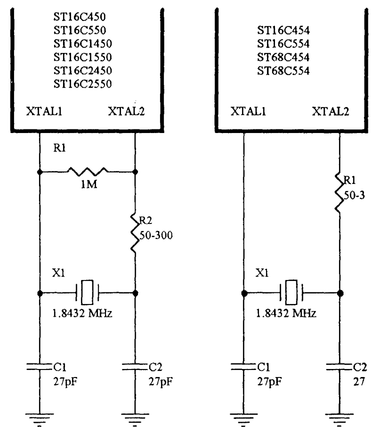
Read **LSR** (**L**ine **S**tatus **R**egister).

For polling applications (non interrupt mode) user has to monitor bit zero of this register to verify valid data in the receive holding register.

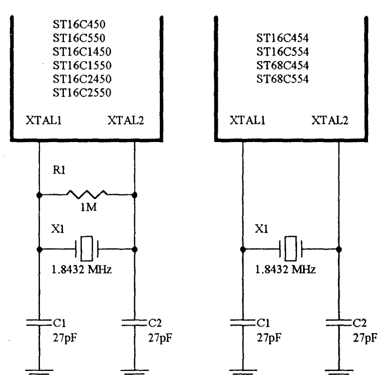
Check the Transmit Holding Empty bit before loading data in the transmit holding register,

continue the transmission.

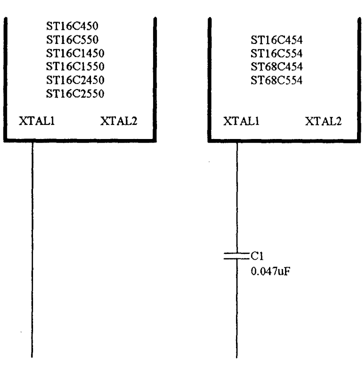
Serial Crystal Connections



Parallel Crystal Connections



External Clock Connections



C PROGRAM SAMPLE

```
; File: sample.c          Package:UART init
; This is a sample code to show how to initialize the UART series of chips
; from Startech Semiconductors.
; This also includes some basic external loop back thru' two different
; ports using the FIFO capability.
; This also includes external loop back thru a different computer

#include    <stdio.h>
#include    <string.h>
#include    <fcntl.h>

#define     TRUE                1
#define     FALSE               0

/* These are the various offsets for the registers inside the chip */
#define     RHR                 0x00  /* Receive Holding Register   */
#define     THR                 0x00  /* Receive Holding Register   */
#define     IER                 0x01  /* Interrupt Enable Register  */
#define     FCR                 0x02  /* FIFO control Register      */
#define     ISR                 0x02  /* Interrupt Status Register  */
#define     LCR                 0x03  /* Line control register      */
#define     MCR                 0x04  /* Modem Control Register     */
#define     LSR                 0x05  /* Line Status Register       */
#define     MSR                 0x06  /* Modem Status Register      */
#define     SCR                 0x07  /* Scratch pad Register       */

/* This two offsets are used for defining the baud rate      */
#define     DIVLSB              0x00  /* Divisor LSB latch address  */
#define     DIVMSB              0x01  /* Divisor MSB Latch address  */

/*\
 * Program table for baud rate
 * This represents the LSB and MSB divisor latch data
\*/
char baud_table[8][2] = {
        { 0x80, 0x01 },         /* 300  */
        { 0x60, 0x00 },         /* 1200 */
        { 0x30, 0x00 },         /* 2400 */
        { 0x0c, 0x00 },         /* 9600 */
        { 0x06, 0x00 },         /* 19K  */
        { 0x03, 0x00 },         /* 38k  */
        { 0x02, 0x00 },         /* 56k  */
        { 0x01, 0x00 }          /* 115k */
};
```

```
/* Baud Rates */
#define     _COM_300_          0
#define     _COM_1200_         1
#define     _COM_2400_         2
#define     _COM_9600_         3
#define     _COM_19K_          4
#define     _COM_38K_          5
#define     _COM_56K_          6
#define     _COM_115K_         7

/* Parity */
#define     _COM_NOPARITY_     0
#define     _COM_ODDPARITY_    1
#define     _COM_EVENPARITY_   2

/* Stopbits */
#define     _COM_STOP1_        0
#define     _COM_STOP2_        1
#define     _COM_STOP1_5_      1

/* word length */
#define     _COM_CHR5_         0
#define     _COM_CHR6_         1
#define     _COM_CHR7_         2
#define     _COM_CHR8_         3

/* word length */
#define     _COM_FIFO1_        0
#define     _COM_FIFO4_        1
#define     _COM_FIFO8_        2
#define     _COM_FIFO14_       3

/*\
 * This function checks the existence of a port.
 * It is very simple. Take the port address then write to the scratch pad
 * an the read it back. If the data read back the same as one that was
 * written then return TRUE else return FALSE.
\*/
int
check_port(com_port)
int com_port;
{

  int i;

     printf("Checking for port %4xH\n",com_port);
  /* Write 1010 1010 (0xaa) to scratch pad*/
```

```
    printf("Writing AAH in %4xH\n",com_port);
  outportb(com_port + SCR, 0xaa);

  /* read it back. If it the same then return TRUE */
  i = inportb(com_port + SCR);

    printf("Read back %2xH from %4xH\n",i,com_port);

  if( i == 0xaa)
       return TRUE;
  else
       return FALSE;

}

/*\
 * This is the work horse function which actually setups the UART.
 * It needs to know every thing.
\*/
int
init_uart(port,baud,parity,data,stop,fifo,trigger)
int port,baud,parity,data,stop,fifo,trigger;
{

  char lcr_byte;

  /* Set divisor latch */
  outportb(port+LCR, 0x80) ;

  printf("Divisor Latch is %2xH %2xH (High Low)\n",
                         baud_table[baud][1],baud_table[baud][0]);
  outportb(port+DIVLSB, baud_table[baud][0]) ;
  outportb(port+DIVMSB, baud_table[baud][1]) ;


  /* Reset to normal Programming */
  /* Program the lcr_byte for the above parameters */
  lcr_byte = 0x00;
  lcr_byte = data; /* Set the  bit0 & bit1 for word length */
  lcr_byte ;= stop << 3; /* Set the bit2 for stop bit */
  if(parity != _COM_NOPARITY_) {
     lcr_byte ;= 1 << 4;  /* Set the bit3 for parity */
     if(parity == _COM_EVENPARITY_)
       lcr_byte ;= 1 << 5; /* Set the bit4 for EVEN parity */
  }

  printf("LCR byte is %2xH\n",lcr_byte);
  /* Program LCR  */
```

```
  outportb(port+LCR, lcr_byte) ;

  if(fifo) {
   char fifo_byte;

   printf("Programming FIFOs without DMA mode\n");

   /* Have to first set the fifo enable */
   fifo_byte = 0x01;
   outportb(port+FCR,fifo_byte);

   /* Now program the FIFO */
   fifo_byte = 0x07; /* set bit0 - FIFO enable, Reset RCVR and XMIT FIFO */
   fifo_byte ;= trigger << 7; /* set bit6 and bit7 with the trigger level */

   /* Program FCR */
   outportb(port+FCR,fifo_byte);
   if(~(inportb(port + ISR) & 0xc0)) {
       printf("This port %4xH does not have FIFOs\n");
       printf("Hence did not program Enable FIFOs\n");
   }
  }

  /* Program IER */
  printf("Programming IER for interrupt on bit0 RCV holding Register\n");
  outportb(port+IER, 0x01);

  return TRUE;
}

/*\
 * This is the test mode.
 * It gets the address of the ports checks to see if they are there.
 * Note: If a driver already exists I am not sure how to temporarily remove it.
 * Well we will worry about it later.
 * Warn the use to remove any drivers that are on the ports.
 * Especially the mouse driver.
 * pass the address to the test552 routine.
\*/
int test_mode()
{
        int i,j,k; /* generic variables */
        char port1[10], port2[10];
        int pt1,pt2;  /* this are the integer port numbers */

        void test552();

        printf("WARNING: This program will not work if the ports to be tested\n");
```

```
        printf("      have drivers installed in them. e.g Mouse driver\n");
        printf("      Please remove the drivers before doing this test.\n");

        while(TRUE) {
          printf("First Port Address (In HEX) > ");
          scanf("%s",port1);
          pt1 = strtol(port1,NULL,16);
          fflush(stdin);
          /*\
           * Check if this port exists. else loop
          \*/
           if(check_port(pt1))
                break;
           printf("Error: Port %4xH does not exist. Try again\n",pt1);
        }

        while(TRUE) {
          printf("Second Port Address (In HEX) > ");
          scanf("%s",port2);
          pt2 = strtol(port2,NULL,16);
          fflush(stdin);
          /*\
           * Check if this port exists. else loop
          \*/
           if(check_port(pt2))
                break;
           printf("Error: Port %4xH does not exist. Try again\n",pt2);
        }

        /* Test 554 with the two port addresses */
        test552(pt1,pt2);

        return TRUE;

}


/*\
 * It first generates a random number for the data size to be generated.
 * Then generates a random data whose length is equal to the data size.
 * It puts it out on both the ports and polls for the interrupt to occur.
 * It reads both the ports until all characters are received OR a timeout
 * has occured. It then prints out the error Messages if any.
 * This loop is done for ever.
\*/
```

```
void test552(p1,p2)
unsigned int p1, p2;
{
  int i,j,c,w,n;
  unsigned char outbuf[20], inbuf1[20], inbuf2[20];
  unsigned char pbuf[200];
  unsigned long timeout, pass;


  printf("ST16C552 External Loop Test Beginning\n") ;
  printf("Testing ports %4x and %4x\n\n", p1, p2) ;
  printf("Programing ports for 56K,8 bit,no parity,1 stop bit,FIFO trigger level 01\n");
  printf("This program uses POLLED mode for testing\n");
  printf("Press Cntrl-C to stop the testing and quit\n");
  printf("Note: The ports will remain at the above settings after the TEST\n");

  /* Programming ports for 8 bits, no parity, 56K baud,
                                FIFO enabled at level 01 */
  /* Program first port */
  printf("Programming port %x4\n",p1);
  init_uart(p1,_COM_56K_,_COM_NOPARITY_,
          _COM_CHR8_,_COM_STOP1_,TRUE,_COM_FIFO1_);

  /* Program Second Port */
  printf("Programming port %x4\n",p2);
  init_uart(p2,_COM_56K_,_COM_NOPARITY_,
          _COM_CHR8_,_COM_STOP1_,TRUE,_COM_FIFO1_);

  printf("Starting test\n");
  for (pass = 1 ; ; pass++) {
       /* generate random size for data */
       n = rand() ;
       n += n >> 8 ;
       n &= 0x0f ;

       /* Make sure we never get a 0 as the random size data */
       if(n != 0x0f)
         n++ ;

       /* generate random data */
       for (w = 0 ; w < n ; w++) {
            c = rand() ;
            c += c >> 8 ;
            c &= 0xff ;
            c ;= 0x01 ; /* no NULLs allowed */
            outbuf[w] = c ;
       }
```

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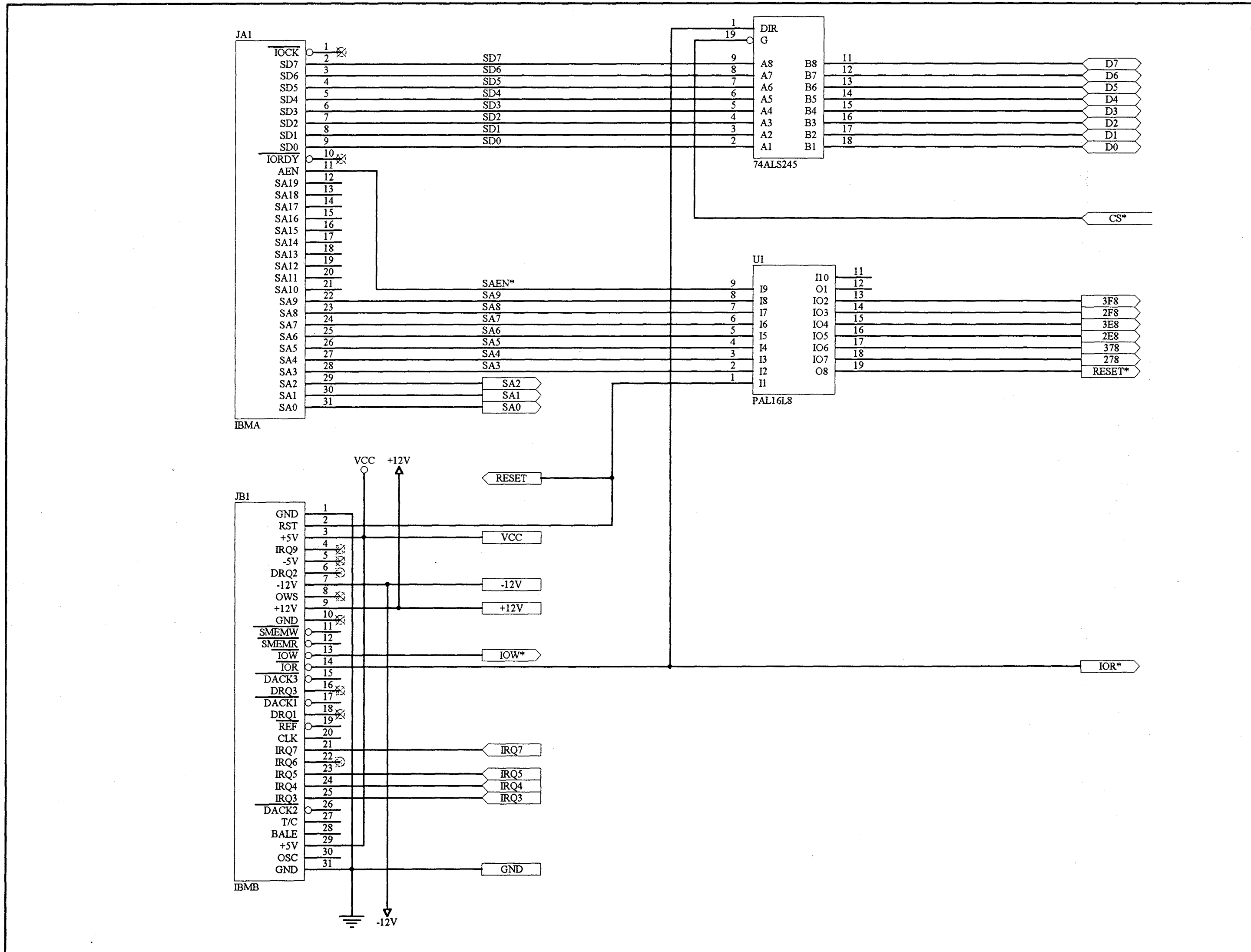
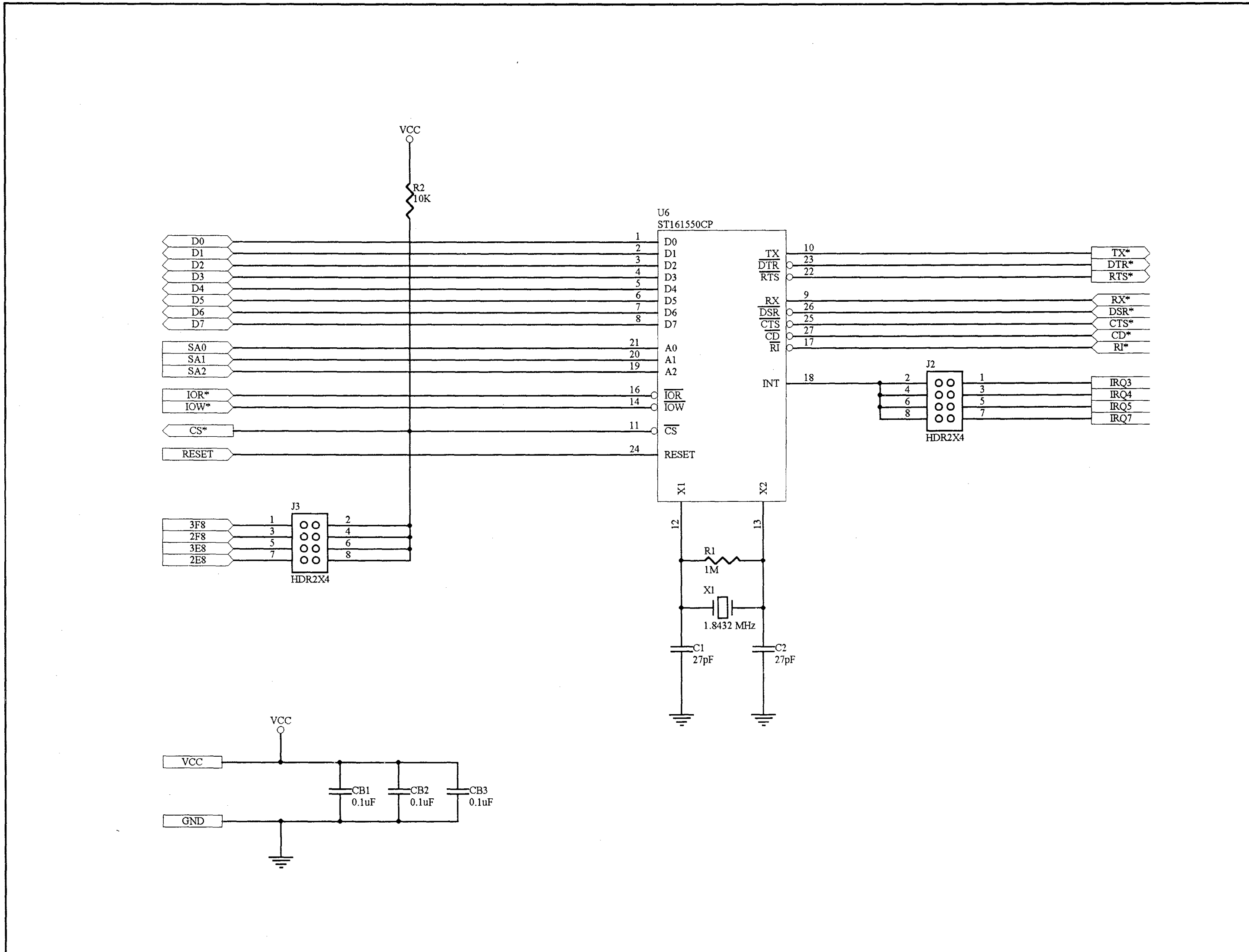
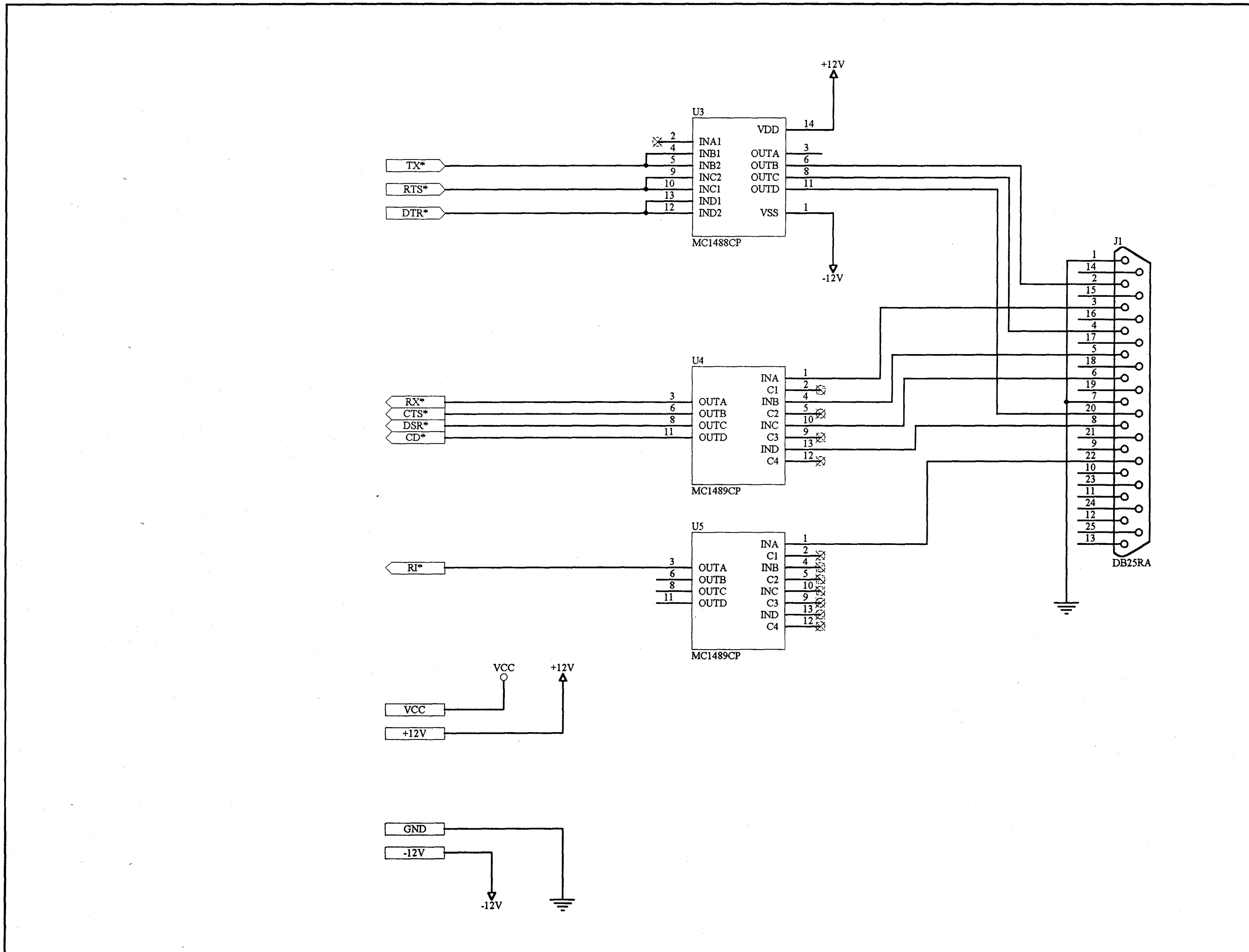
```
outbuf[w] = NULL;

printf("******** Pass %10ld Sending %d *********\015", pass, n) ;

/* Transmitt the data */
for (i = 0 ; i < n ; i++ ) {
      outportb(p1, outbuf[i]) ;
      outportb(p2, outbuf[i]) ;
}

/* loop waiting for intr pending */
for ( i = 0;;i++ ) {
      if ((~inportb(p1+ISR) & 0x01) && (~inportb(p2+ISR) & 0x01))
            break;
}

/* receive data until all has been received OR timeout */
timeout = 0x0008F ;
for (i = j = 0; ((i < 20) && (j < 20));) {
      if (inportb(p1+LSR) & 0x01) inbuf1[i++] = inportb(p1) ;
      c = rand() ;
      c += c >> 8 ;
      c &= 0x001f ;
      c++ ;
      for ( ; c != 0; c—) ;
      if (inportb(p2+LSR) & 0x01) inbuf2[j++] = inportb(p2) ;
      if (timeout— == 0) break ;
}

/* If timed out then print message else comparse data */
if(timeout == 0 )
      printf("Timed out on Ports\n");
else {
   inbuf1[i] = inbuf2[j] = NULL;
   /* compare results */
   if (strcmp(outbuf, inbuf1) ;; ( i != n)) {
         printf("\nError:%04x Sent:    ", p2) ;
         for ( w = 0; w < n; w++ )
               printf(" %02x", outbuf[w]) ;
         printf("\n%04x Received:", p1) ;
         for ( w = 0; w < i; w++ )
               printf(" %02x", inbuf1[w]) ;
         printf("\n") ;
   }
   if (strcmp(outbuf, inbuf2) ;; ( j != n )) {
         printf("\nError:%04x Sent:    ", p1);
         for ( w = 0; w < n; w++ )
               printf(" %02x", outbuf[w]) ;
```

```
                printf("\n%04x Received:", p2) ;
                for ( w = 0; w < j; w++ )
                        printf(" %02x", inbuf2[w]) ;
                printf("\n") ;
            }
        }
    }
}
```

ST16C1450/1550 APPLICATION EXAMPLE


JA1
IOCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IORDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
IBMA
SAEN*
DIR
G
A8
A7
A6
A5
A4
A3
A2
A1
B8
B7
B6
B5
B4
B3
B2
B1
74ALS245
D7
D6
D5
D4
D3
D2
D1
D0
CS*
U1
I9
I8
I7
I6
I5
I4
I3
I2
I1
I10
O1
IO2
IO3
IO4
IO5
IO6
IO7
O8
PAL16L8
3F8
2F8
3E8
2E8
378
278
RESET*
RESET
VCC
+12V
JB1
GND
RST
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
GND
SMEMW
SMEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
REF
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
BALE
+5V
OSC
GND
IBMB
VCC
-12V
+12V
IOW*
IOR*
IRQ7
IRQ5
IRQ4
IRQ3
GND
-12V


VCC
R2
10K
U6
ST161550CP
D0
D1
D2
D3
D4
D5
D6
D7
SA0
SA1
SA2
IOR*
IOW*
CS*
RESET
A0
A1
A2
IOR
IOW
CS
TX
DTR
RTS
RX
DSR
CTS
CD
RI
INT
X1
X2
TX*
DTR*
RTS*
RX*
DSR*
CTS*
CD*
RI*
J2
HDR2X4
IRQ3
IRQ4
IRQ5
IRQ7
J3
HDR2X4
3F8
2F8
3E8
2E8
R1
1M
X1
1.8432 MHz
C1
27pF
C2
27pF
VCC
GND
CB1
0.1uF
CB2
0.1uF
CB3
0.1uF


+12V
U3
VDD
INA1
INB1
INB2
INC2
INC1
IND1
IND2
OUTA
OUTB
OUTC
OUTD
VSS
MC1488CP
-12V
TX*
RTS*
DTR*
J1
DB25RA
U4
INA
C1
INB
C2
INC
C3
IND
C4
OUTA
OUTB
OUTC
OUTD
MC1489CP
RX*
CTS*
DSR*
CD*
U5
MC1489CP
RI*
VCC
+12V
VCC
+12V
GND
-12V
-12V

ST16C2450/2550 APPLICATION EXAMPLE

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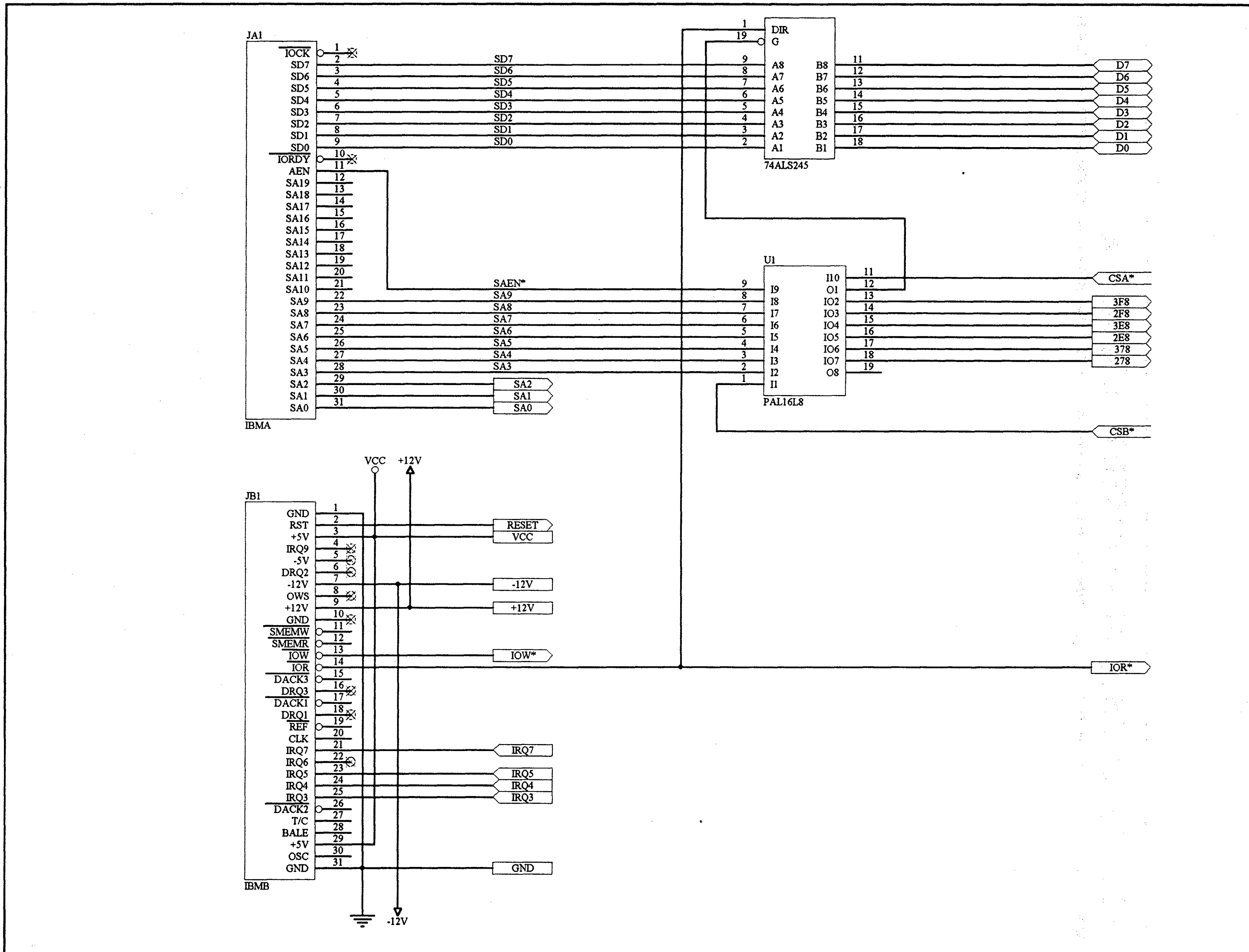
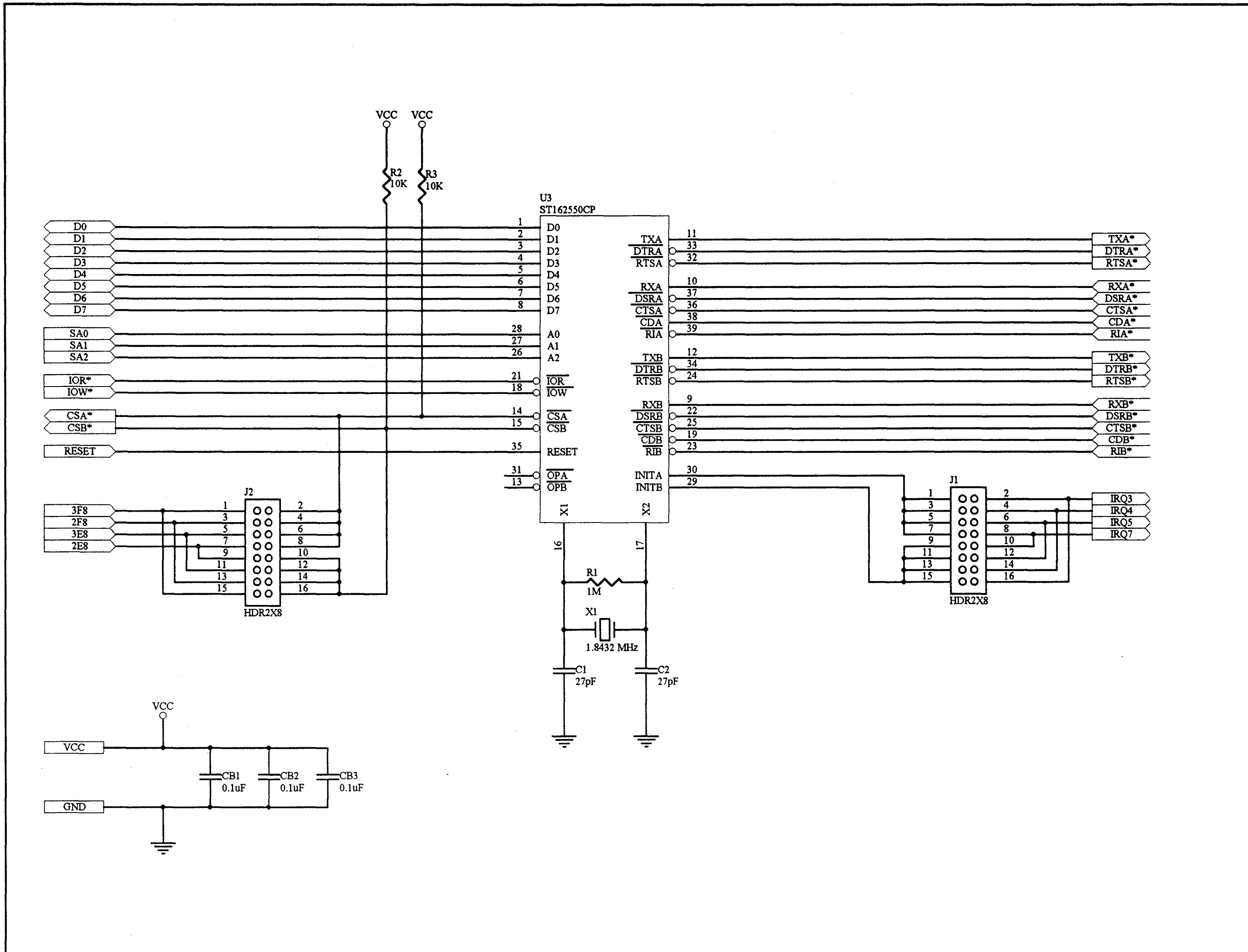
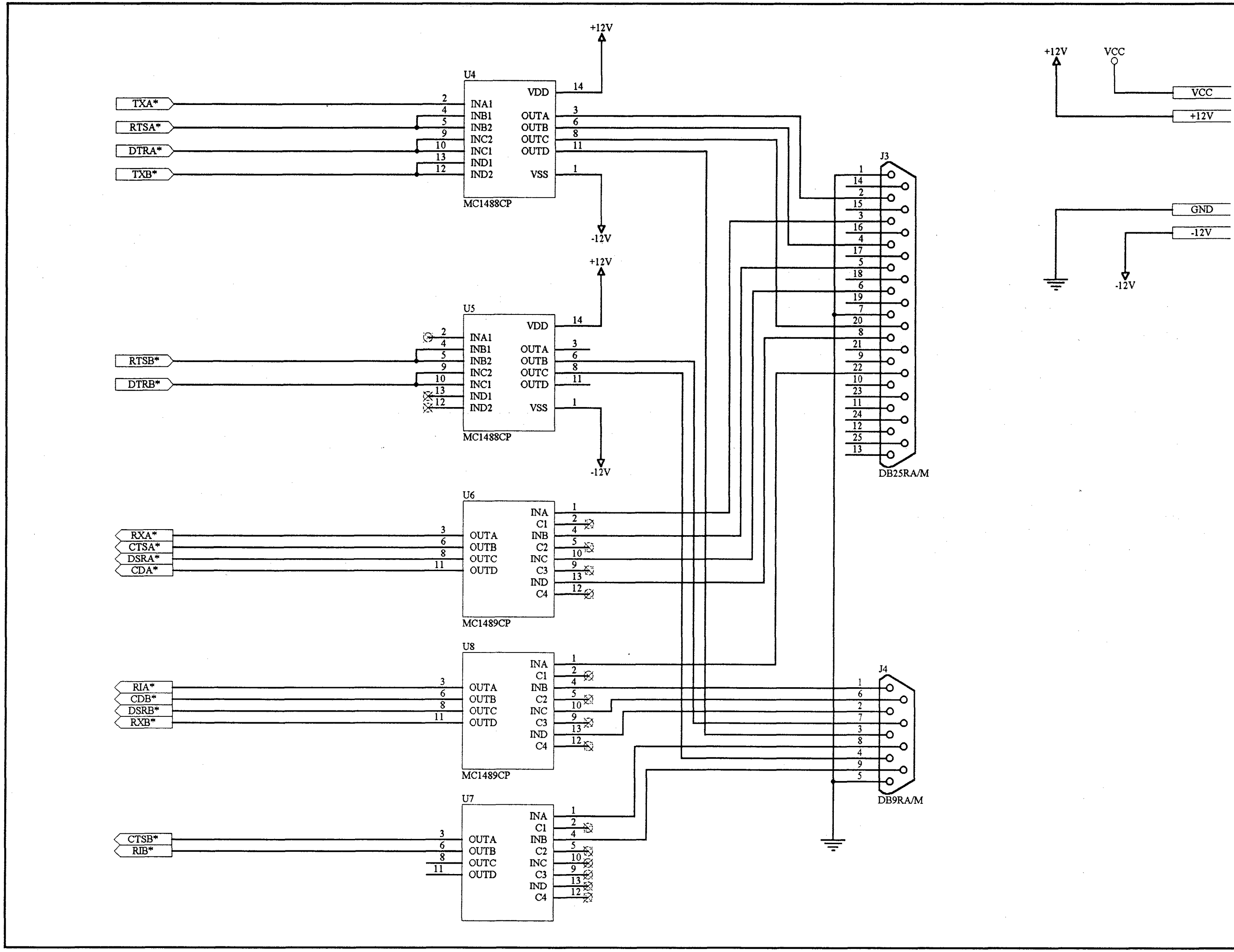
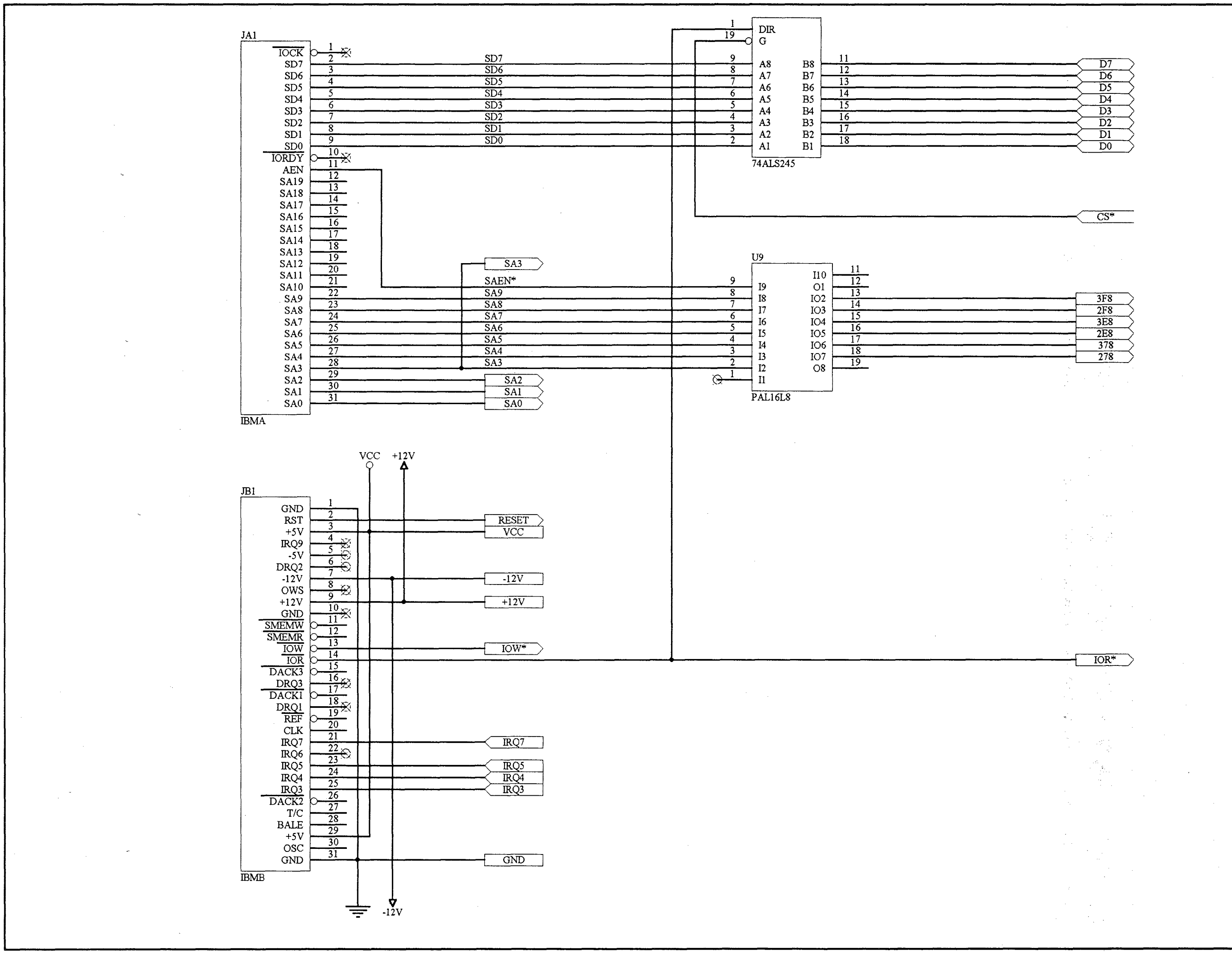
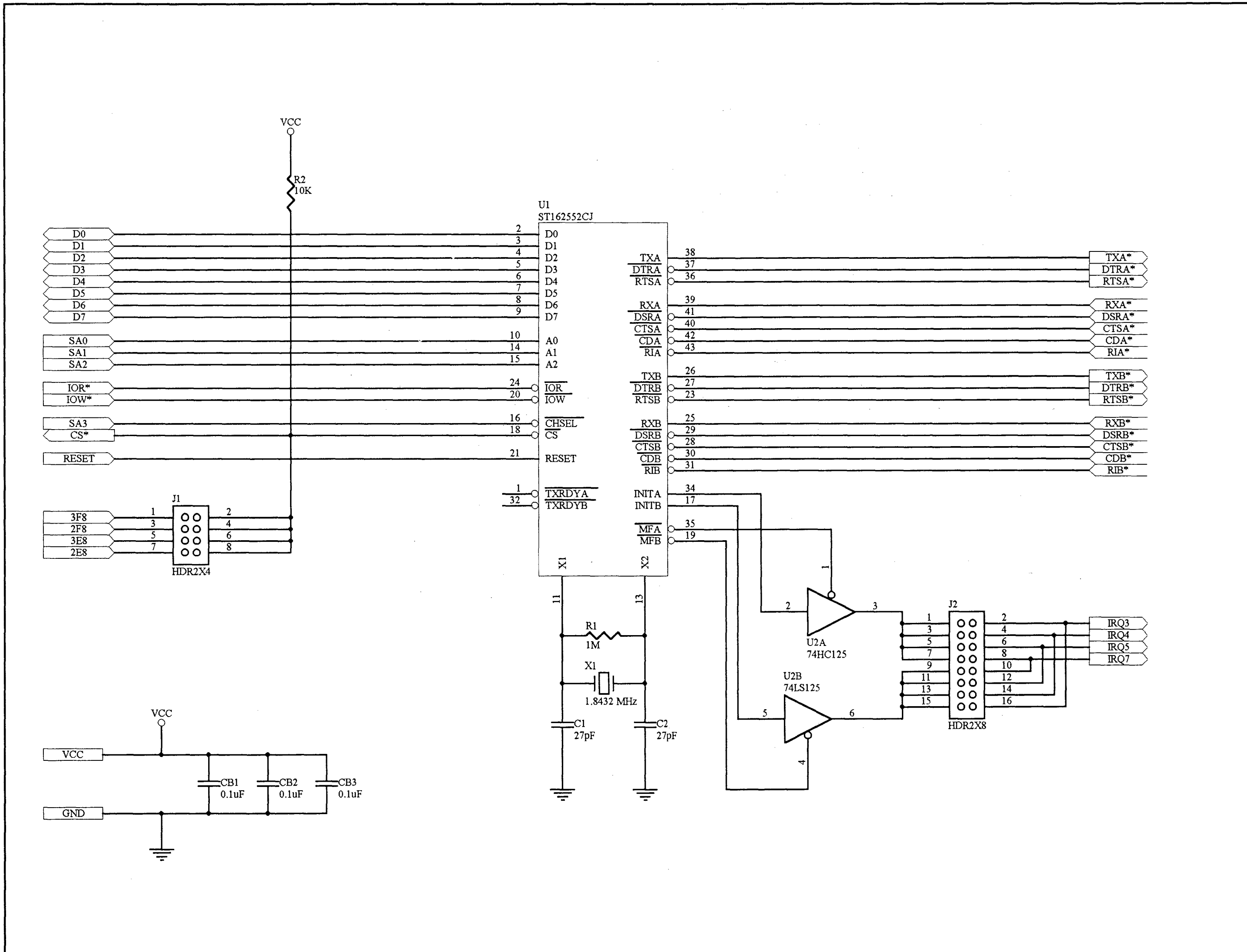

JA1
IOCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IORDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
IBMA
SAEN*
DIR
G
A8
A7
A6
A5
A4
A3
A2
A1
B8
B7
B6
B5
B4
B3
B2
B1
74ALS245
D7
D6
D5
D4
D3
D2
D1
D0
U1
I10
O1
IO2
IO3
IO4
IO5
IO6
IO7
O8
I9
I8
I7
I6
I5
I4
I3
I2
I1
PAL16L8
CSA*
3F8
2F8
3E8
2E8
378
278
CSB*
VCC
+12V
JB1
GND
RST
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
GND
SMEMW
SMEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
REF
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
BALE
+5V
OSC
GND
IBMB
RESET
VCC
-12V
+12V
IOW*
IOR*
IRQ7
IRQ5
IRQ4
IRQ3
GND
-12V

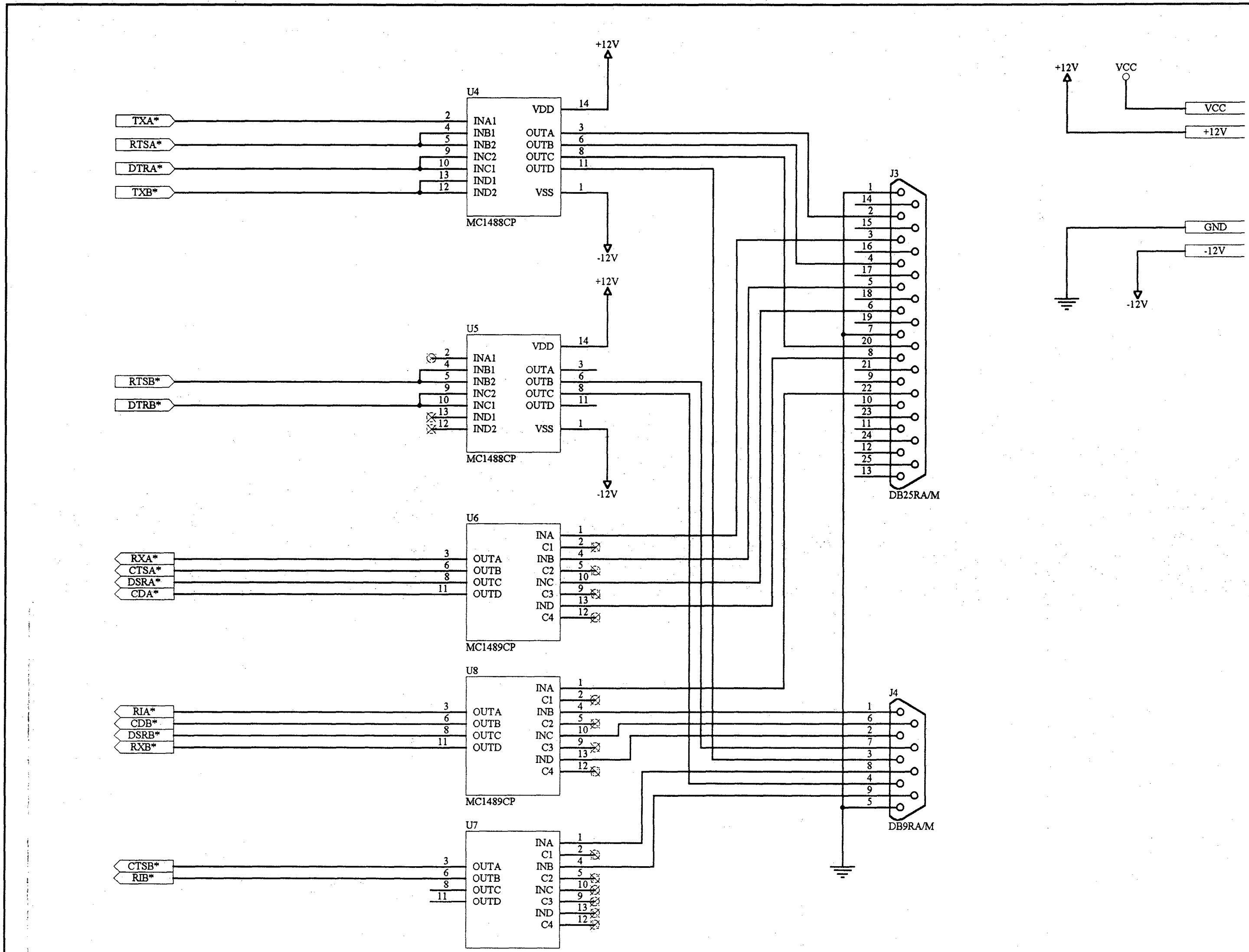

VCC
VCC
R2
10K
R3
10K
U3
ST162550CP
D0
D1
D2
D3
D4
D5
D6
D7
SA0
SA1
SA2
IOR*
IOW*
CSA*
CSB*
RESET
A0
A1
A2
IOR
IOW
CSA
CSB
OPA
OPB
X1
X2
TXA
DTRA
RTSA
RXA
DSRA
CTSA
CDA
RIA
TXB
DTRB
RTSB
RXB
DSRB
CTSB
CDB
RIB
INITA
INITB
TXA*
DTRA*
RTSA*
RXA*
DSRA*
CTSA*
CDA*
RIA*
TXB*
DTRB*
RTSB*
RXB*
DSRB*
CTSB*
CDB*
RIB*
J2
3F8
2F8
3E8
2E8
HDR2X8
J1
IRQ3
IRQ4
IRQ5
IRQ7
HDR2X8
R1
1M
X1
1.8432 MHz
C1
27pF
C2
27pF
VCC
VCC
GND
CB1
0.1uF
CB2
0.1uF
CB3
0.1uF


U4
MC1488CP
TXA*
RTSA*
DTRA*
TXB*
U5
MC1488CP
RTSB*
DTRB*
U6
MC1489CP
RXA*
CTSA*
DSRA*
CDA*
U8
MC1489CP
RIA*
CDB*
DSRB*
RXB*
U7
CTSB*
RIB*
J3
DB25RA/M
J4
DB9RA/M
+12V
-12V
VCC
GND

ST16C2552 APPLICATION EXAMPLE


JA1
IOCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IORDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
IBMA
SAEN*
DIR
G
A8
A7
A6
A5
A4
A3
A2
A1
B8
B7
B6
B5
B4
B3
B2
B1
74ALS245
D7
D6
D5
D4
D3
D2
D1
D0
CS*
U9
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
O1
IO2
IO3
IO4
IO5
IO6
IO7
O8
PAL16L8
3F8
2F8
3E8
2E8
378
278
VCC
+12V
JB1
GND
RST
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
GND
SMEMW
SMEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
REF
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
BALE
+5V
OSC
GND
IBMB
RESET
VCC
-12V
+12V
IOW*
IOR*
IRQ7
IRQ5
IRQ4
IRQ3
GND
-12V


VCC
R2
10K
U1
ST162552CJ
D0
D1
D2
D3
D4
D5
D6
D7
SA0
SA1
SA2
IOR*
IOW*
SA3
CS*
RESET
A0
A1
A2
IOR
IOW
CHSEL
CS
TXRDYA
TXRDYB
TXA
DTRA
RTSA
RXA
DSRA
CTSA
CDA
RIA
TXB
DTRB
RTSB
RXB
DSRB
CTSB
CDB
RIB
INITA
INITB
MFA
MFB
X1
X2
TXA*
DTRA*
RTSA*
RXA*
DSRA*
CTSA*
CDA*
RIA*
TXB*
DTRB*
RTSB*
RXB*
DSRB*
CTSB*
CDB*
RIB*
J1
3F8
2F8
3E8
2E8
HDR2X4
R1
1M
X1
1.8432 MHz
C1
27pF
C2
27pF
U2A
74HC125
U2B
74LS125
J2
HDR2X8
IRQ3
IRQ4
IRQ5
IRQ7
VCC
GND
CB1
0.1uF
CB2
0.1uF
CB3
0.1uF



U4
MC1488CP
TXA*
RTSA*
DTRA*
TXB*
INA1
INB1
INB2
INC2
INC1
IND1
IND2
VDD
OUTA
OUTB
OUTC
OUTD
VSS
+12V
-12V
U5
MC1488CP
RTSB*
DTRB*
U6
MC1489CP
RXA*
CTSA*
DSRA*
CDA*
INA
C1
INB
C2
INC
C3
IND
C4
U8
MC1489CP
RIA*
CDB*
DSRB*
RXB*
U7
CTSB*
RIB*
J3
DB25RA/M
J4
DB9RA/M
VCC
GND

ST16C450/550 APPLICATION EXAMPLE

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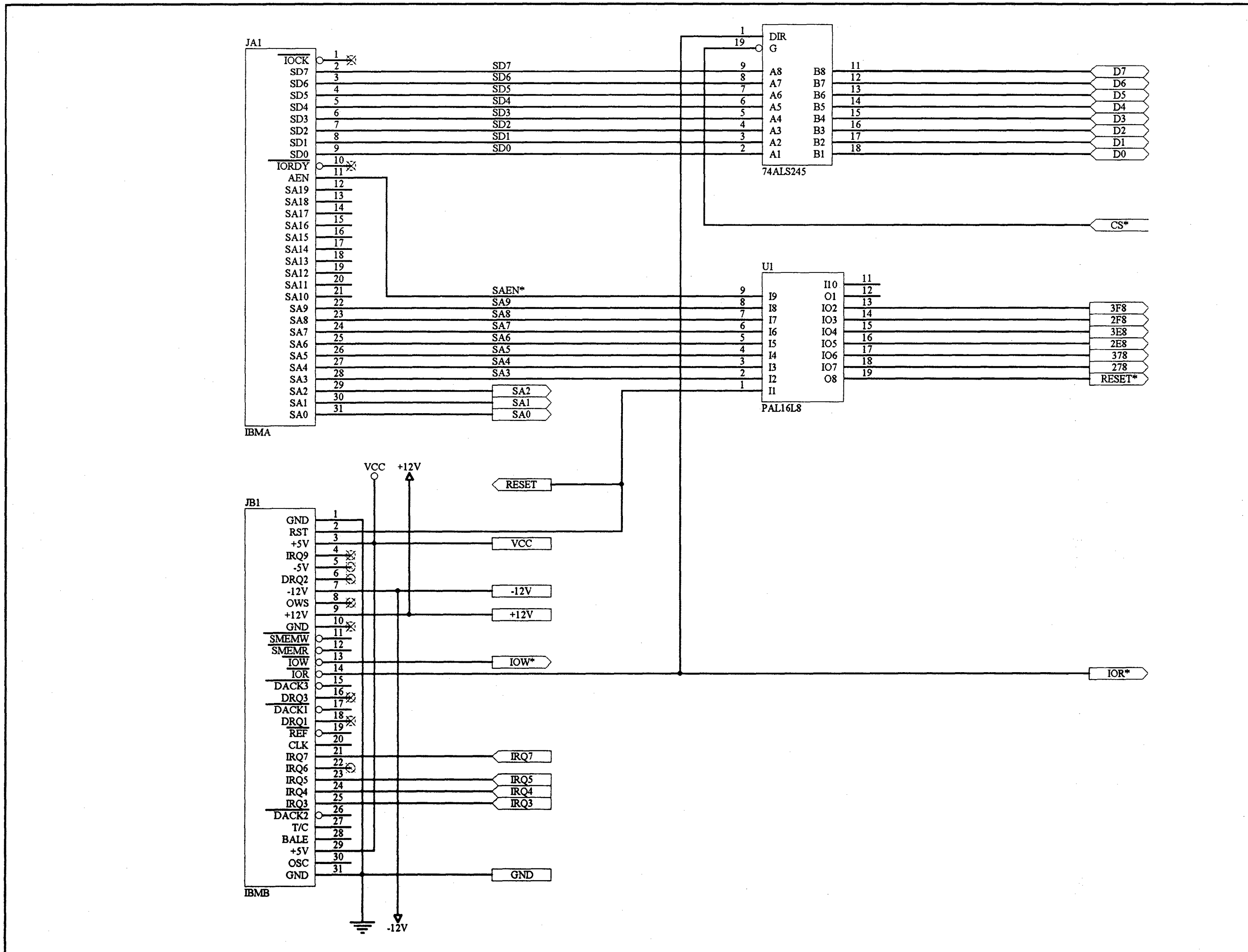
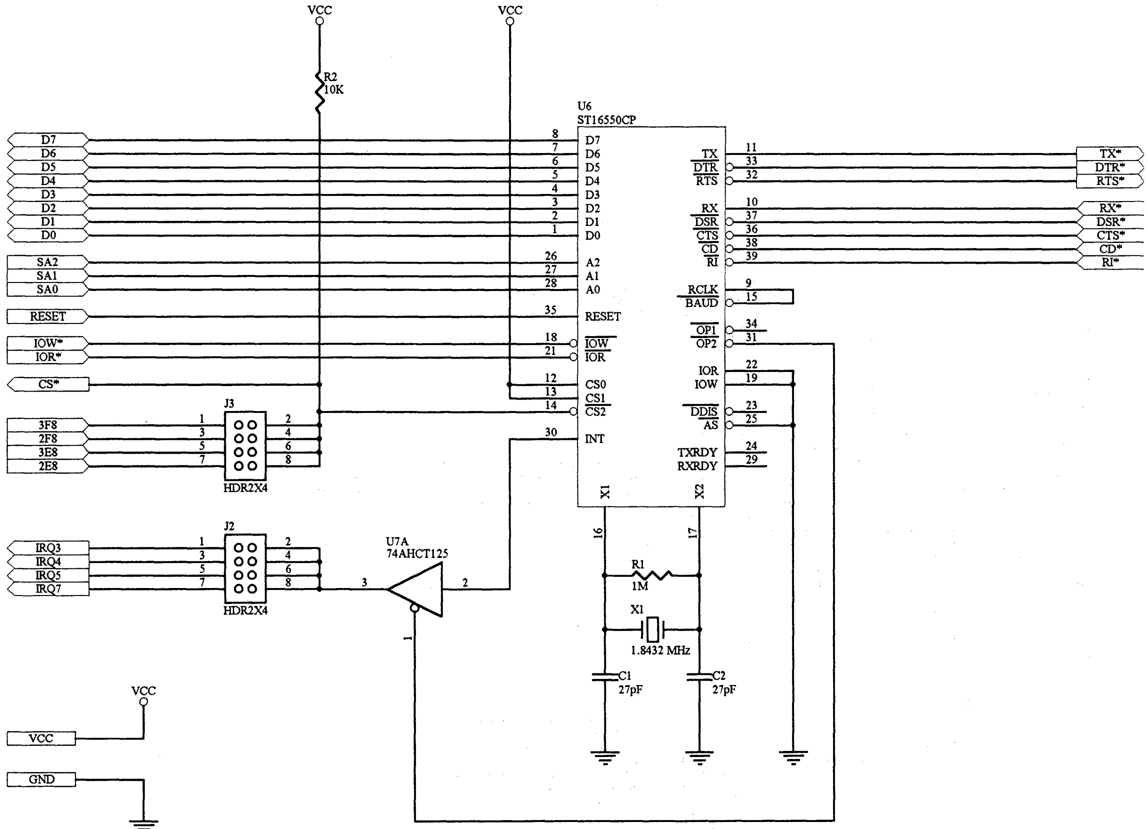
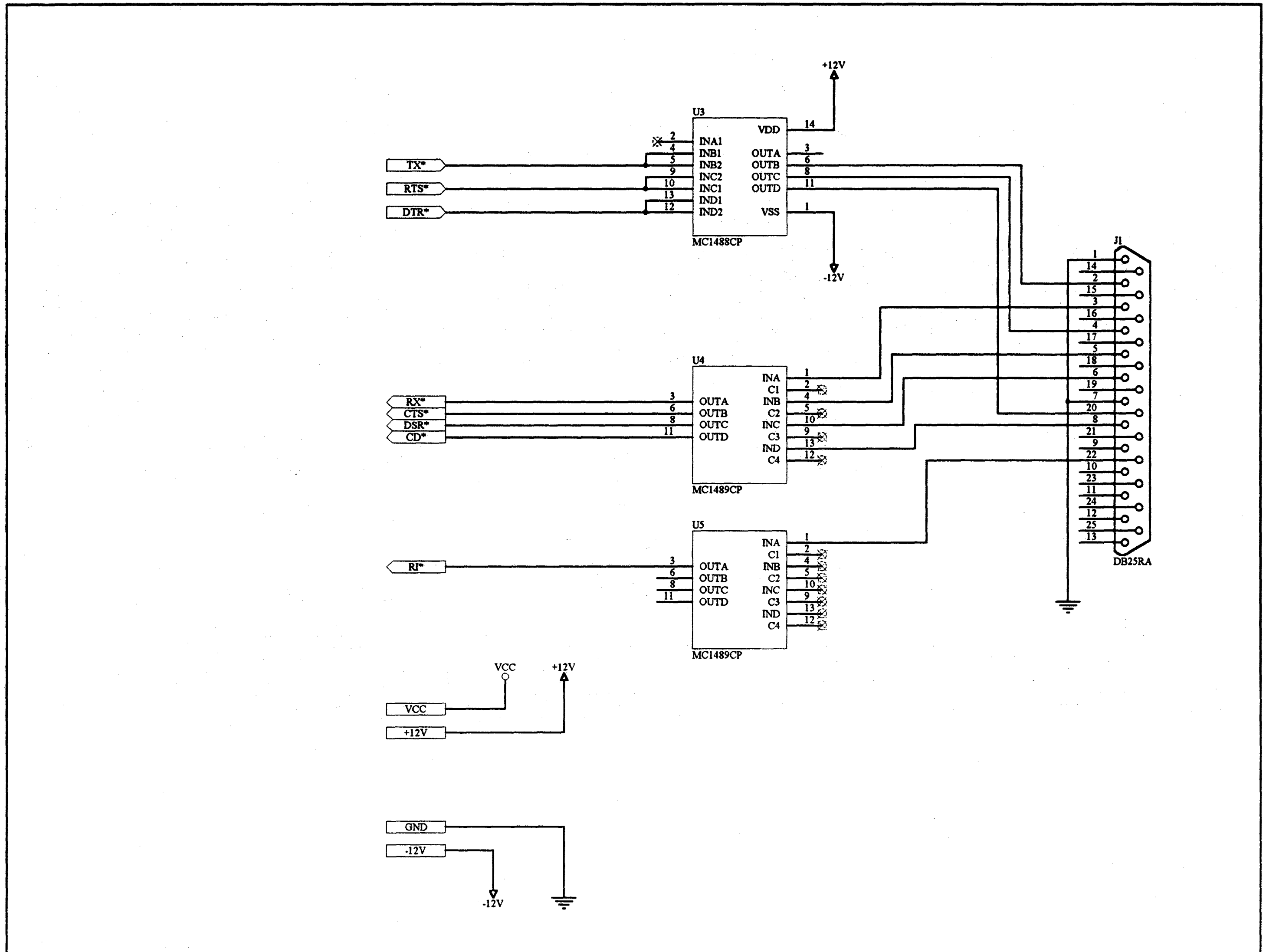

JA1
IOCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IORDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
IBMA
SAEN*
DIR
G
A8
A7
A6
A5
A4
A3
A2
A1
B8
B7
B6
B5
B4
B3
B2
B1
74ALS245
D7
D6
D5
D4
D3
D2
D1
D0
CS*
U1
I9
I8
I7
I6
I5
I4
I3
I2
I1
I10
O1
IO2
IO3
IO4
IO5
IO6
IO7
O8
PAL16L8
3F8
2F8
3E8
2E8
378
278
RESET*
VCC
+12V
RESET
JB1
GND
RST
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
GND
SMEMW
SMEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
REF
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
BALE
+5V
OSC
GND
IBMB
VCC
-12V
+12V
IOW*
IOR*
IRQ7
IRQ5
IRQ4
IRQ3
GND
-12V


VCC
R2
10K
U6
ST16550CP
D7
D6
D5
D4
D3
D2
D1
D0
SA2
SA1
SA0
RESET
IOW*
IOR*
CS*
A2
A1
A0
IOW
IOR
CS0
CS1
CS2
INT
TX
DTR
RTS
RX
DSR
CTS
CD
RI
RCLK
BAUD
OP1
OP2
IOR
IOW
DDIS
AS
TXRDY
RXRDY
X1
X2
TX*
DTR*
RTS*
RX*
DSR*
CTS*
CD*
RI*
J3
3F8
2F8
3E8
2E8
HDR2X4
J2
IRQ3
IRQ4
IRQ5
IRQ7
HDR2X4
U7A
74AHCT125
R1
1M
X1
1.8432 MHz
C1
27pF
C2
27pF
VCC
GND



U3
MC1488CP
VDD
VSS
INA1
INB1
INB2
INC2
INC1
IND1
IND2
OUTA
OUTB
OUTC
OUTD
+12V
-12V
TX*
RTS*
DTR*
U4
MC1489CP
RX*
CTS*
DSR*
CD*
INA
C1
INB
C2
INC
C3
IND
C4
U5
MC1489CP
RI*
J1
DB25RA
VCC
GND

AN454
AN554
AN654

ST16C454/554/654 APPLICATION EXAMPLE

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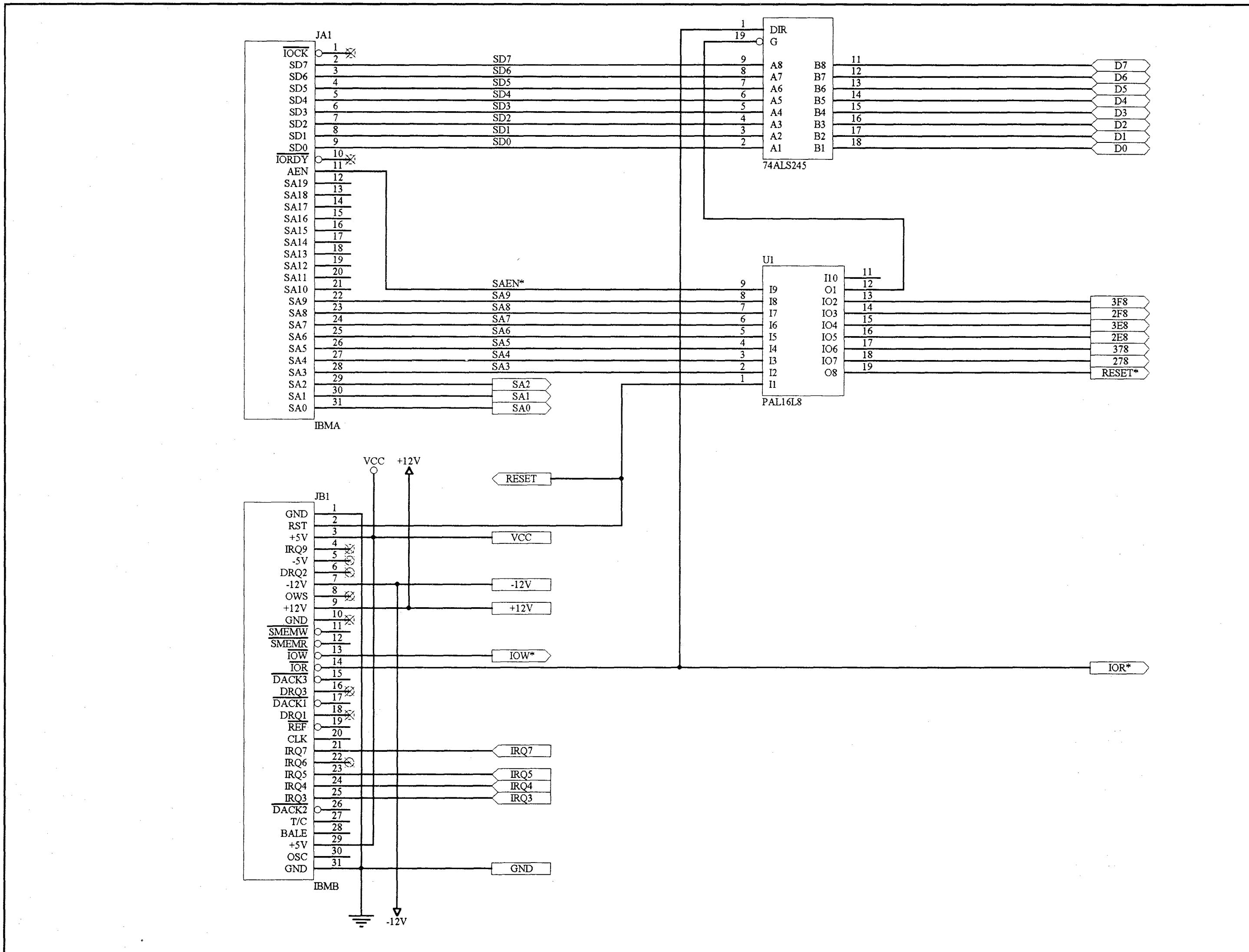
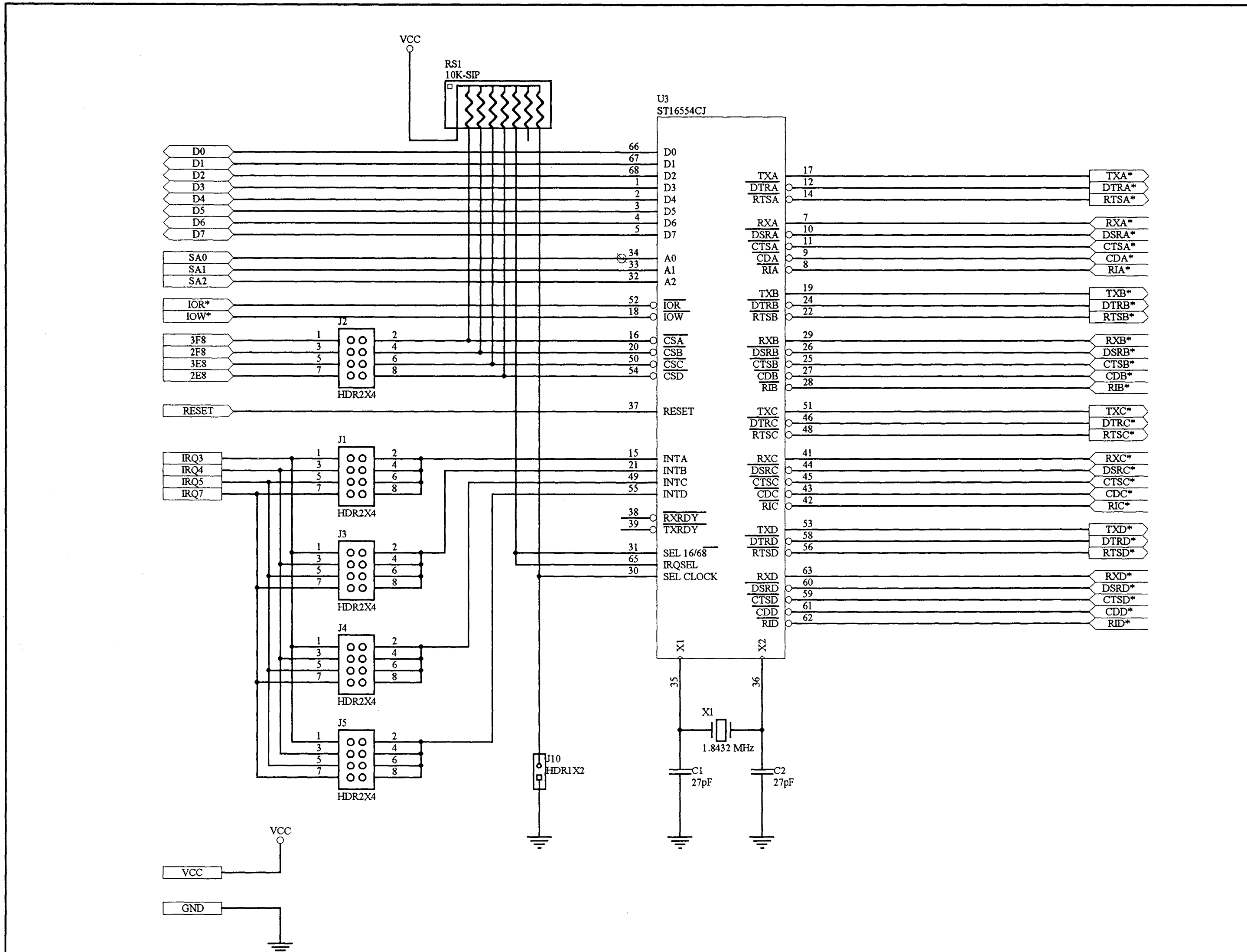
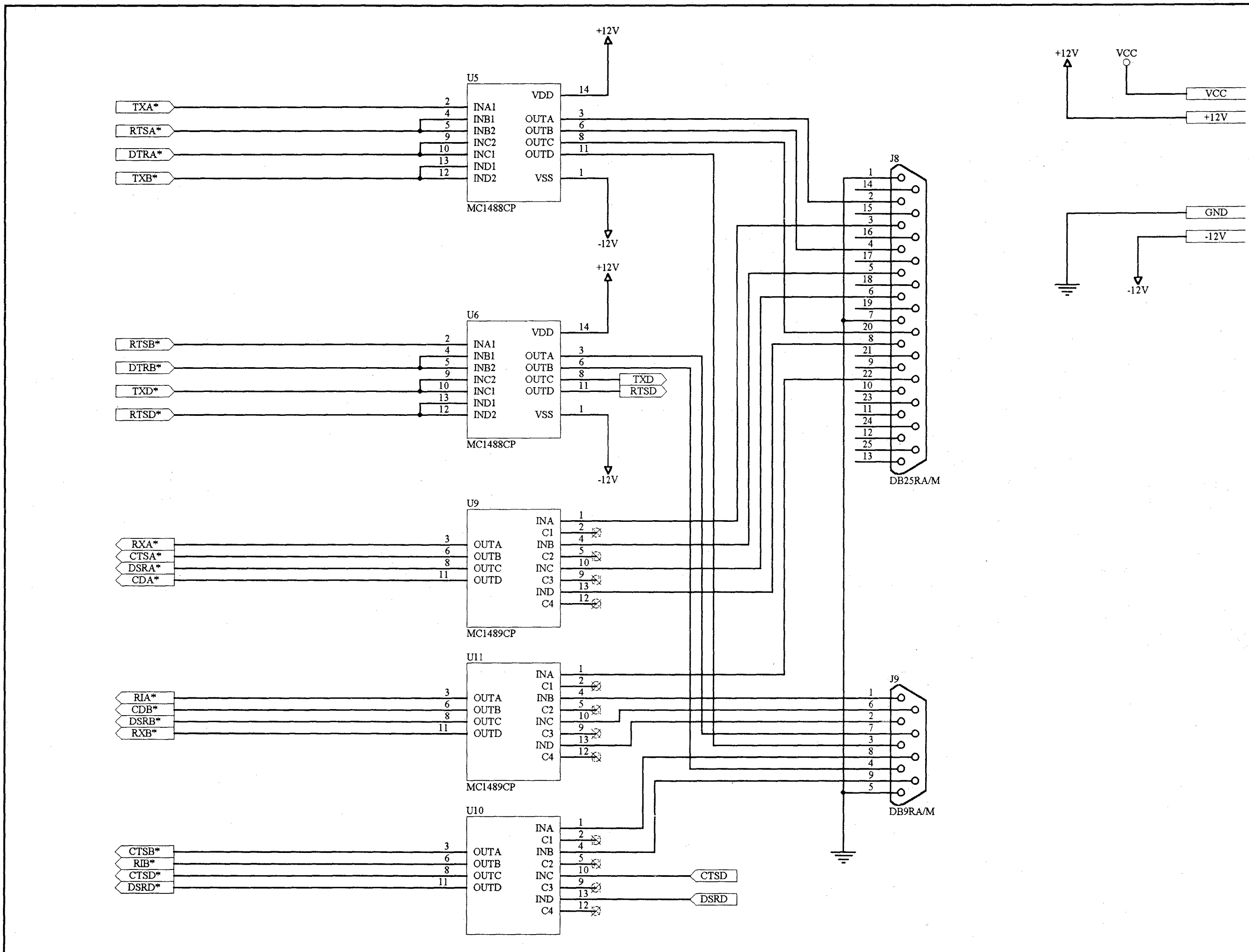
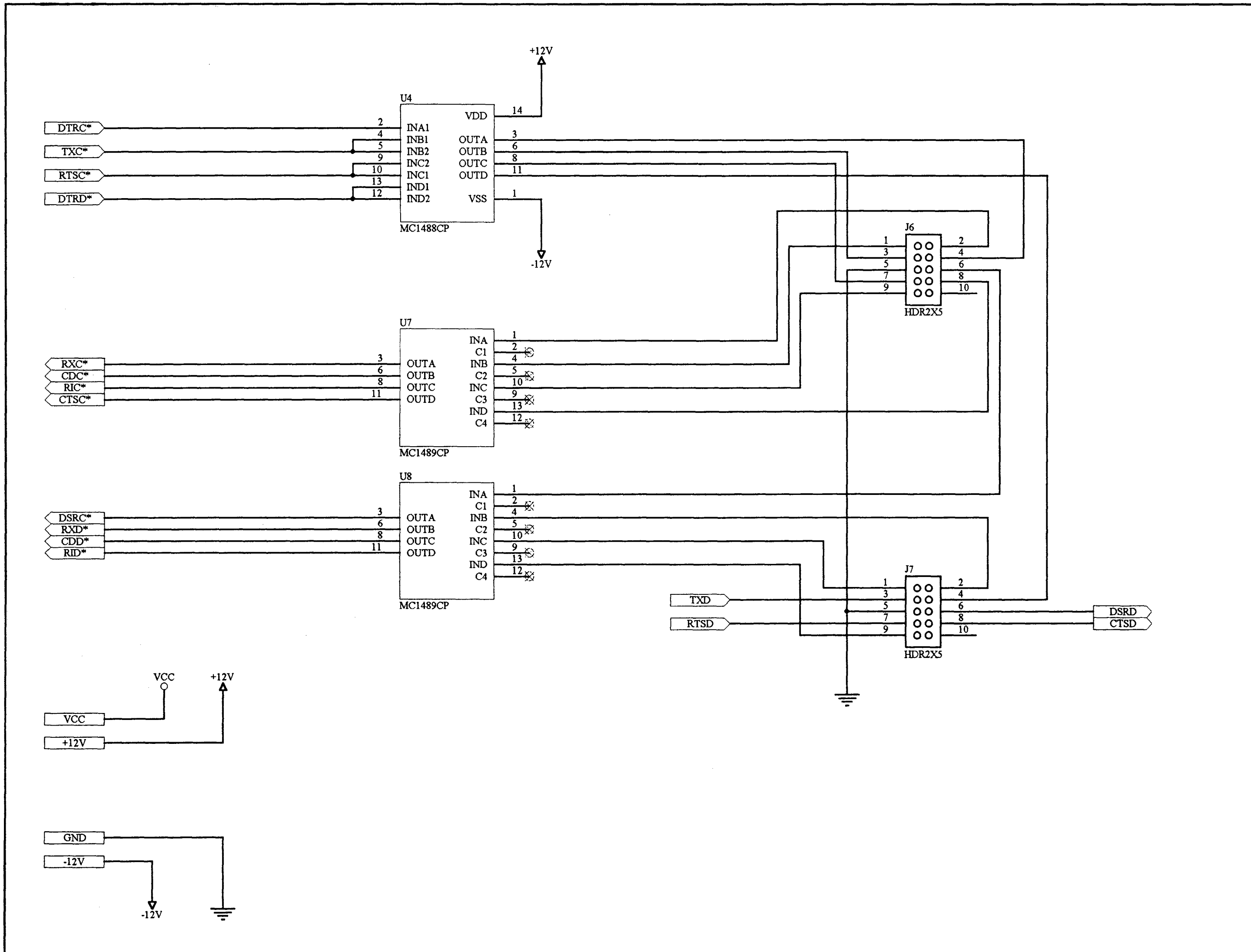
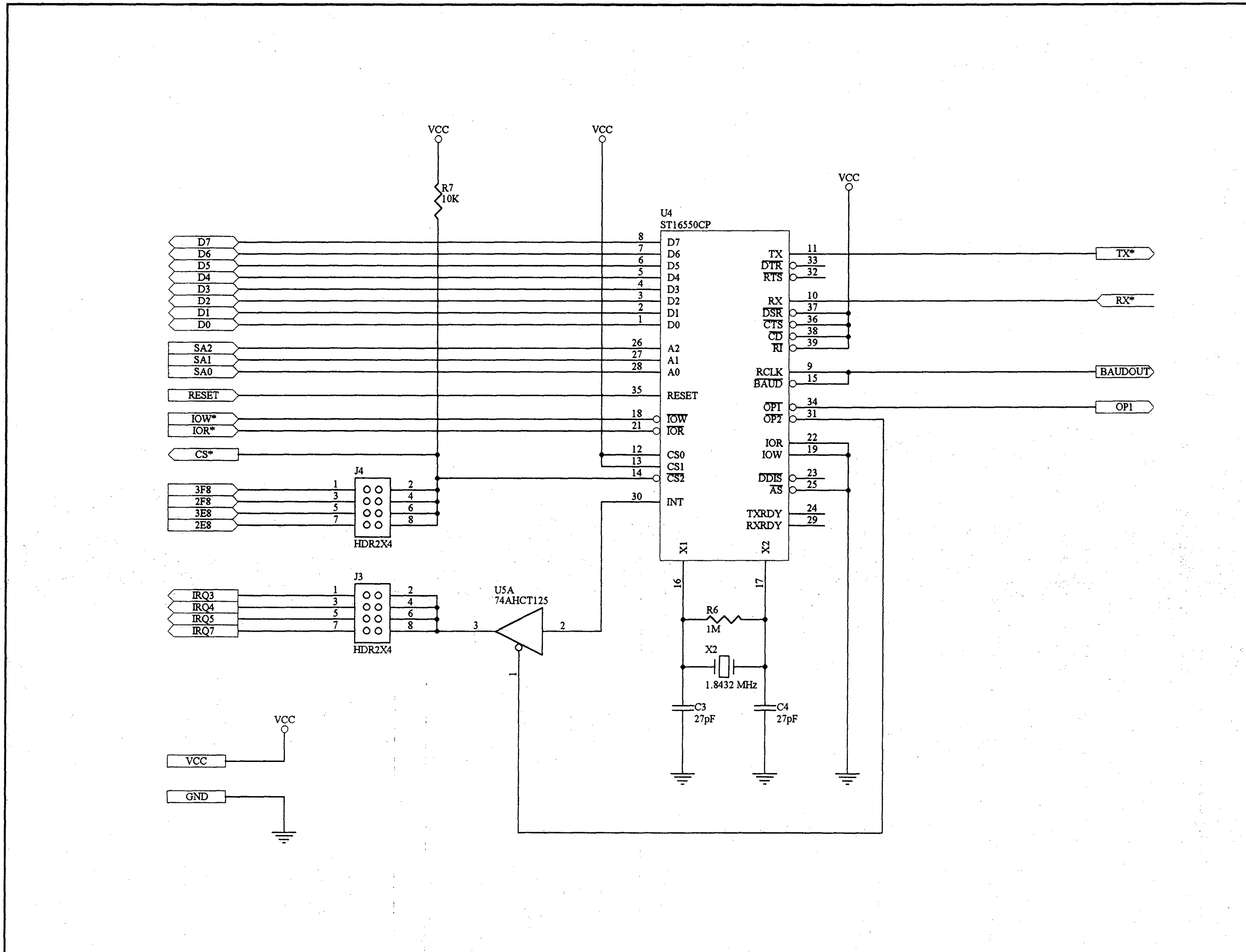

JA1
IOCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IORDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
IBMA
74ALS245
DIR
G
A8 A7 A6 A5 A4 A3 A2 A1
B8 B7 B6 B5 B4 B3 B2 B1
D7 D6 D5 D4 D3 D2 D1 D0
U1
PAL16L8
SAEN*
I1 I2 I3 I4 I5 I6 I7 I8 I9 I10
O1 IO2 IO3 IO4 IO5 IO6 IO7 O8
3F8
2F8
3E8
2E8
378
278
RESET*
RESET
VCC
+12V
JB1
GND
RST
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
GND
SMEMW
SMEMR
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
REF
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
BALE
+5V
OSC
GND
IBMB
VCC
-12V
+12V
IOW*
IOR*
IRQ7
IRQ5
IRQ4
IRQ3
GND
-12V

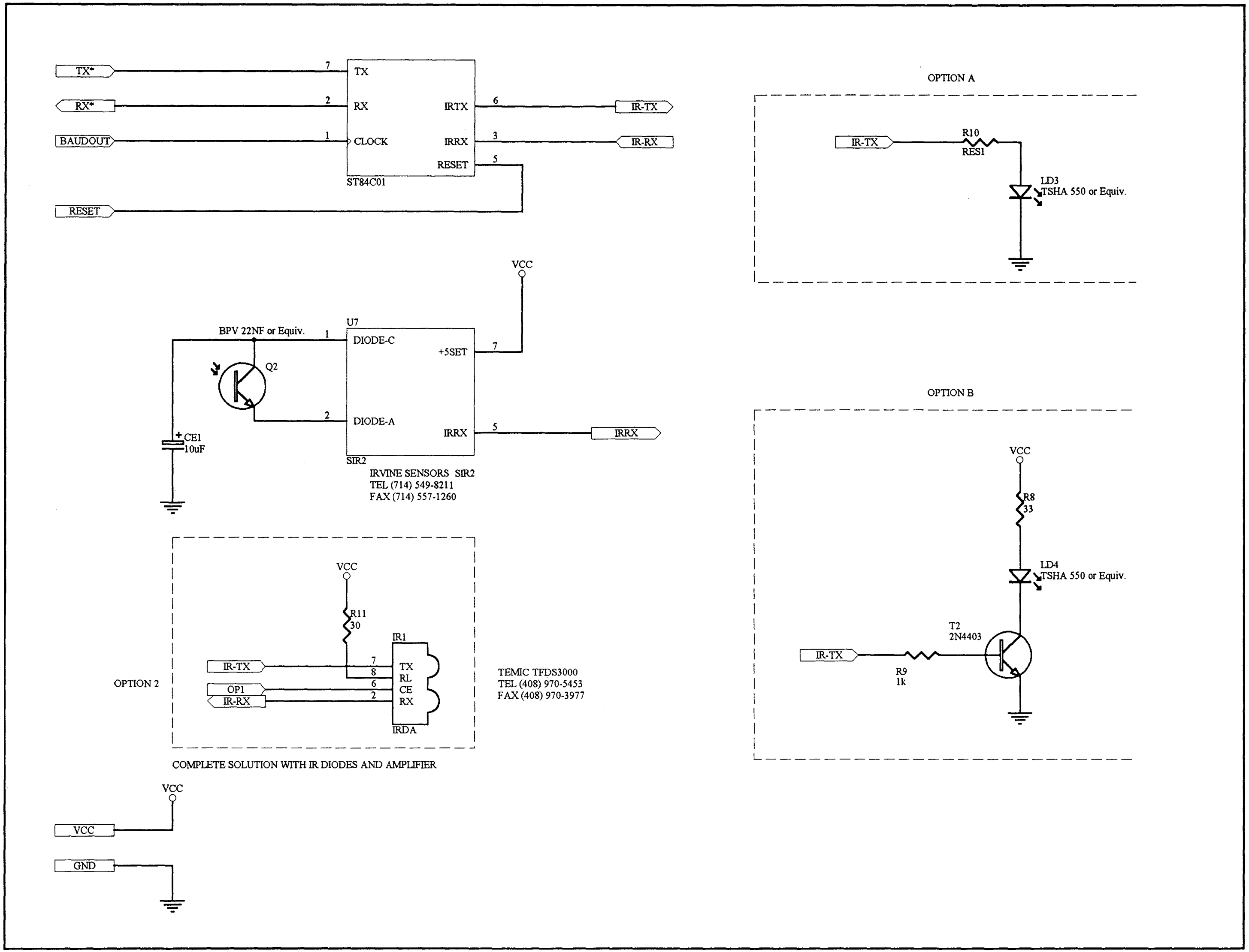

VCC
RS1
10K-SIP
U3
ST16554CJ
D0
D1
D2
D3
D4
D5
D6
D7
SA0
SA1
SA2
IOR*
IOW*
3F8
2F8
3E8
2E8
RESET
IRQ3
IRQ4
IRQ5
IRQ7
J1
J2
J3
J4
J5
HDR2X4
J10
HDR1X2
A0
A1
A2
IOR
IOW
CSA
CSB
CSC
CSD
INTA
INTB
INTC
INTD
RXRDY
TXRDY
SEL 16/68
IRQSEL
SEL CLOCK
TXA
DTRA
RTSA
RXA
DSRA
CTSA
CDA
RIA
TXB
DTRB
RTSB
RXB
DSRB
CTSB
CDB
RIB
TXC
DTRC
RTSC
RXC
DSRC
CTSC
CDC
RIC
TXD
DTRD
RTSD
RXD
DSRD
CTSD
CDD
RID
TXA*
DTRA*
RTSA*
RXA*
DSRA*
CTSA*
CDA*
RIA*
TXB*
DTRB*
RTSB*
RXB*
DSRB*
CTSB*
CDB*
RIB*
TXC*
DTRC*
RTSC*
RXC*
DSRC*
CTSC*
CDC*
RIC*
TXD*
DTRD*
RTSD*
RXD*
DSRD*
CTSD*
CDD*
RID*
X1
X2
X1
1.8432 MHz
C1
27pF
C2
27pF
VCC
GND


+12V
VCC
+12V
GND
-12V
U5
MC1488CP
VDD
INA1
INB1
INB2
INC2
INC1
IND1
IND2
OUTA
OUTB
OUTC
OUTD
VSS
TXA*
RTSA*
DTRA*
TXB*
U6
MC1488CP
RTSB*
DTRB*
TXD*
RTSD*
TXD
RTSD
J8
DB25RA/M
J9
DB9RA/M
U9
MC1489CP
RXA*
CTSA*
DSRA*
CDA*
INA
C1
INB
C2
INC
C3
IND
C4
U11
MC1489CP
RIA*
CDB*
DSRB*
RXB*
U10
CTSB*
RIB*
CTSD*
DSRD*
CTSD
DSRD


U4
MC1488CP
INA1
INB1
INB2
INC2
INC1
IND1
IND2
VDD
OUTA
OUTB
OUTC
OUTD
VSS
+12V
-12V
DTRC*
TXC*
RTSC*
DTRD*
U7
MC1489CP
RXC*
CDC*
RIC*
CTSC*
U8
MC1489CP
DSRC*
RXD*
CDD*
RID*
INA
C1
INB
C2
INC
C3
IND
C4
J6
HDR2X5
J7
HDR2X5
TXD
RTSD
DSRD
CTSD
VCC
+12V
GND
-12V

ST8401 / ST16C654 APPLICATION EXAMPLE


VCC
R7
10K
U4
ST16550CP
D7
D6
D5
D4
D3
D2
D1
D0
SA2
SA1
SA0
A2
A1
A0
RESET
IOW*
IOR*
IOW
IOR
CS*
CS0
CS1
CS2
INT
J4
3F8
2F8
3E8
2E8
HDR2X4
J3
IRQ3
IRQ4
IRQ5
IRQ7
U5A
74AHCT125
TX
DTR
RTS
RX
DSR
CTS
CD
RI
RCLK
BAUD
OP1
OP2
DDIS
AS
TXRDY
RXRDY
X1
X2
TX*
RX*
BAUDOUT
R6
1M
X2
1.8432 MHz
C3
27pF
C4
27pF
GND


TX*
RX*
BAUDOUT
RESET
TX
RX
CLOCK
IRTX
IRRX
RESET
ST84C01
IR-TX
IR-RX
OPTION A
R10
RES1
LD3
TSHA 550 or Equiv.
VCC
BPV 22NF or Equiv.
U7
DIODE-C
+5SET
Q2
DIODE-A
IRRX
CE1
10uF
SIR2
IRVINE SENSORS SIR2
TEL (714) 549-8211
FAX (714) 557-1260
OPTION B
R8
33
LD4
TSHA 550 or Equiv.
T2
2N4403
R9
1k
R11
30
IR1
TX
RL
CE
RX
IRDA
OP1
OPTION 2
TEMIC TFDS3000
TEL (408) 970-5453
FAX (408) 970-3977
COMPLETE SOLUTION WITH IR DIODES AND AMPLIFIER
VCC
GND

QUALITY / RELIABILITY 8

1.0 Quality and Reliability information

The STARTECH semiconductor quality program starts with the design of new products. Each design circuit performance is verified using simulations over voltage and temperature values beyond those of specified product operation.

The design process includes consideration of quality issues such as signal levels, power dissipation, noise generated from internal clock circuits and testability of all device functions.

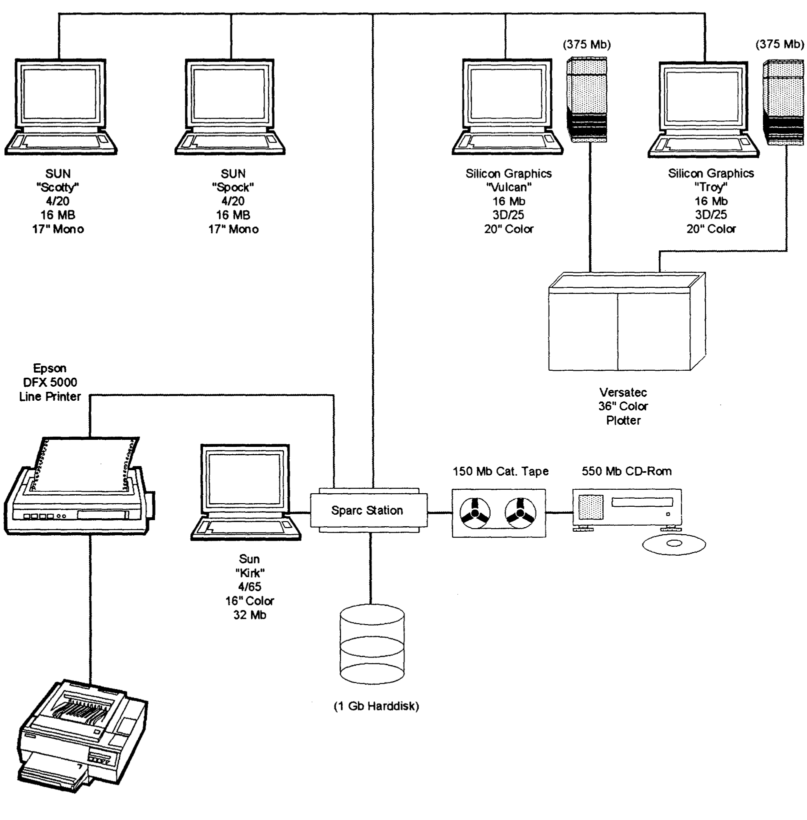
The STARTECH semiconductor document control department maintains control over all manufacturing specifications, lot travelers, procurement specifications and drawings and test programs.

All changes of design are subject to approval by the Engineering, Quality and Manufacturing managers.

STARTECH semiconductor performs a thorough internal product qualification prior to the delivery of any new product or enhanced existing products other than prototypes/samples.

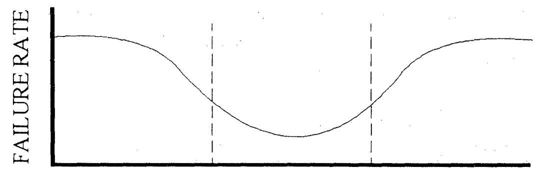
1.1 Design Tools

Schematics entry:	View Logic
Logic & Fault simulators:	Startech Advanced Logic simulator
Layout Synthesis:	Goliath (Startech Layout synthesis)
Layout Editor:	Opal
Layout Verification:	Dracula



150 samples from three different product lots are selected to perform extended temperature operation test, 85° C/ 85% R.H. / 5.5V temperature humidity bias. Same samples are used for accelerated burn-in and electro-static tests.

STARTECH semiconductor subcontracts its fabrication process to ORBIT semiconductor located in Sunnyvale, California. Packaging and final testing are also subcontracted to other vendors located locally or overseas.



1.2 Determination of the Failure Rate

In the simplest form, the failure rate prediction at a given temperature can be predicted as follows.

Failure rate= N/DH

Where:

N= number of failures
D= number of devices
H= number of hours tested

assuming that semiconductors exhibit a log normal distribution.

Acceleration Factors

The effects of temperature, voltage, time and other related functions are key when predicting life times of semiconductor devices. Understanding these effects with the use of a more accurate mathematical model, provides a better means of evaluating the change in reaction rate to changes in temperature.

$$F(T1, T2) = \exp(-Ea/k\ (1/T1 - 1/T2))$$

Where:

F= Acceleration factor
T1= Test temperature (° C+273)
T2= Desired temperature (° C+273)
k= Boltzman's constant (8.63 E-5eV / K)
Ea= Thermal activation energy (eV)

The equivalent device hours can be determined at temperature T2 can be expressed as:

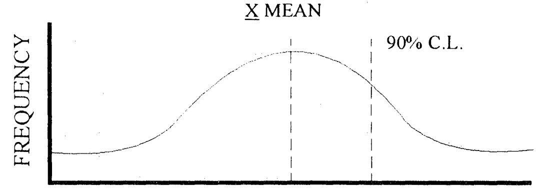
$$EDH(T2) = F(T1, T2) \times DH(T1)$$

The failure rate at T2 can be expressed as:

$$\text{Failure rate } (T2) = N/EDH(T2)$$

Where:

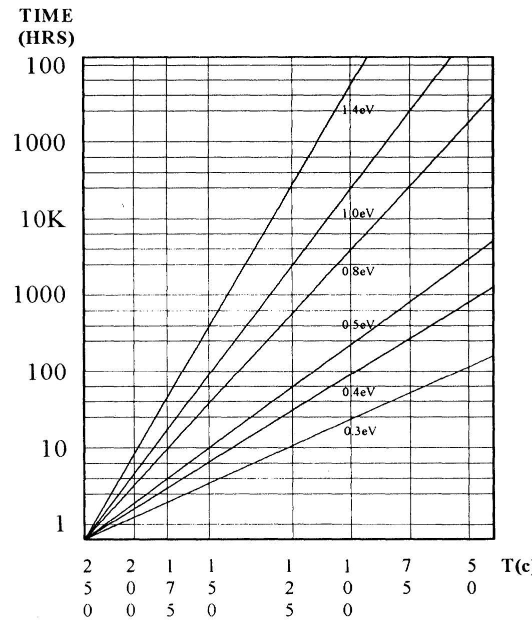
N= Number of failures
EDH= Equivalent device hours



C.L.= Confidence Level

1.3 Activation Energies for Primary Failure Mechanisms

Failure Mechanism	Ea
Contamination	1-1.4 eV
Silicon Defects	0.5 eV
Polarization	1 eV
Oxide Breakdown	0.3 eV
Aluminum Migration	0.5 eV
Trapping	1 eV



1.4 Definition and common test methods

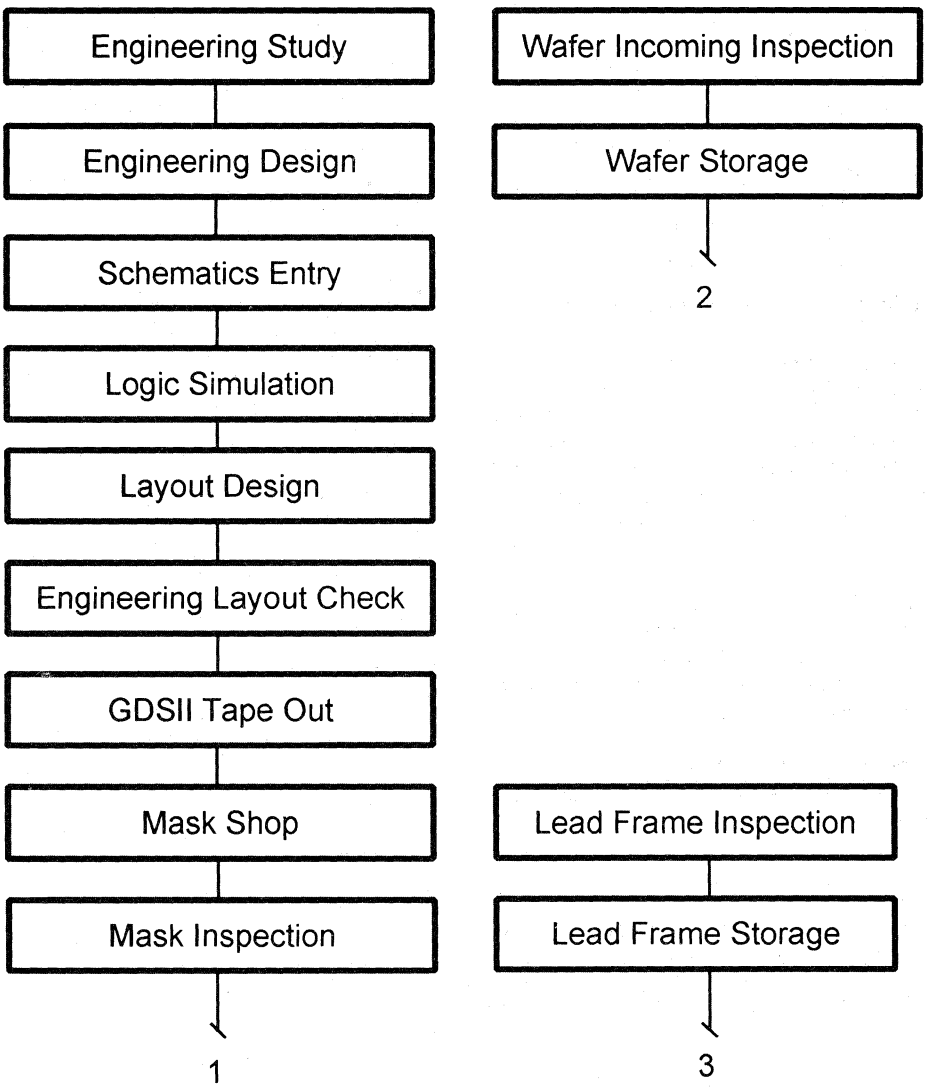
Accelerated operating life stress
Accelerated operating life stressing is performed to accelerate failure mechanisms, which are thermally activated, through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications.

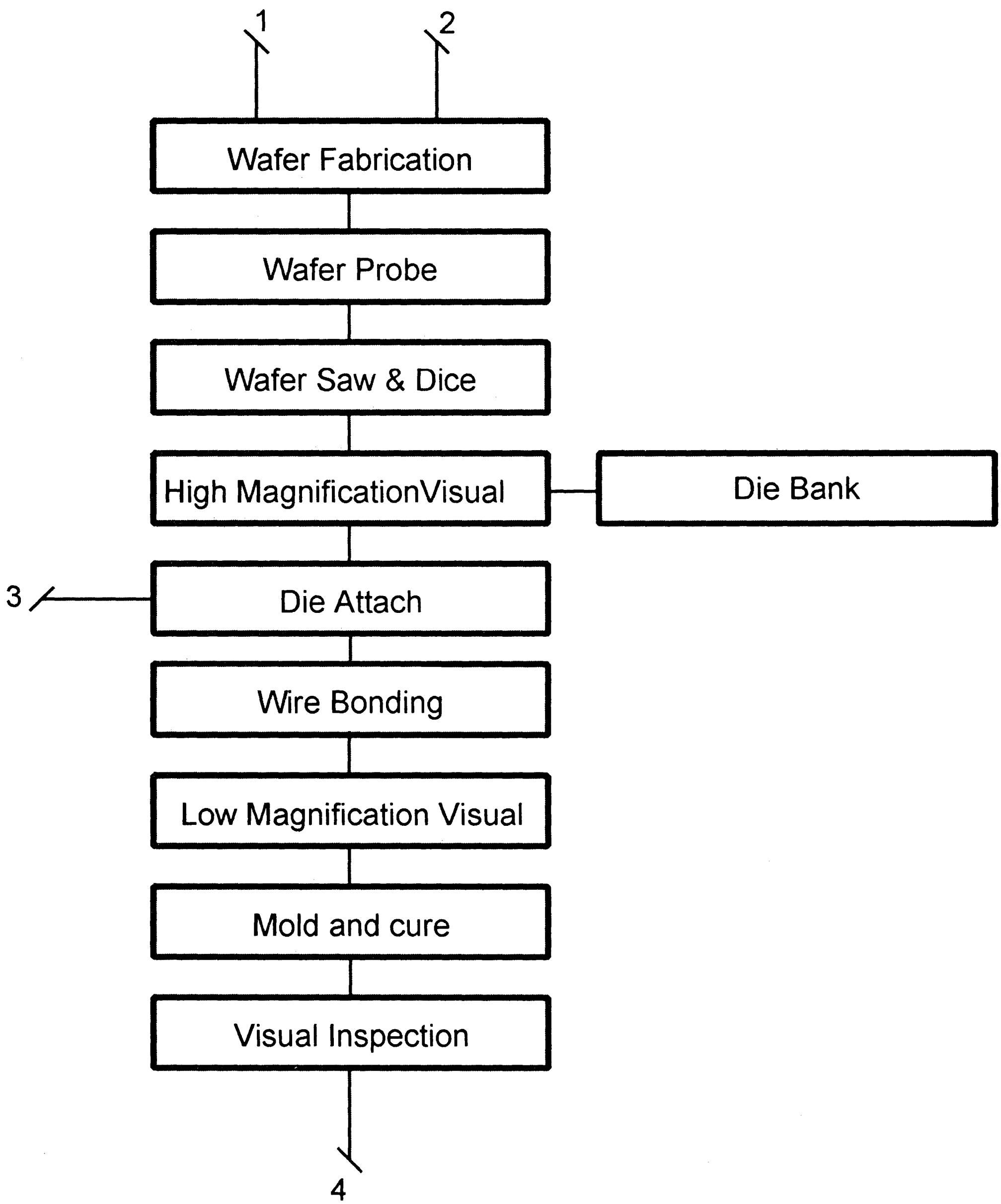
85 °C/ 85 % R.H.
85 °C/ 85 % R.H. is an environmental stress performed at a temperature of 85 °C and relative humidity of 85%. The test is designed to measure the moisture resistance of encapsulated devices.

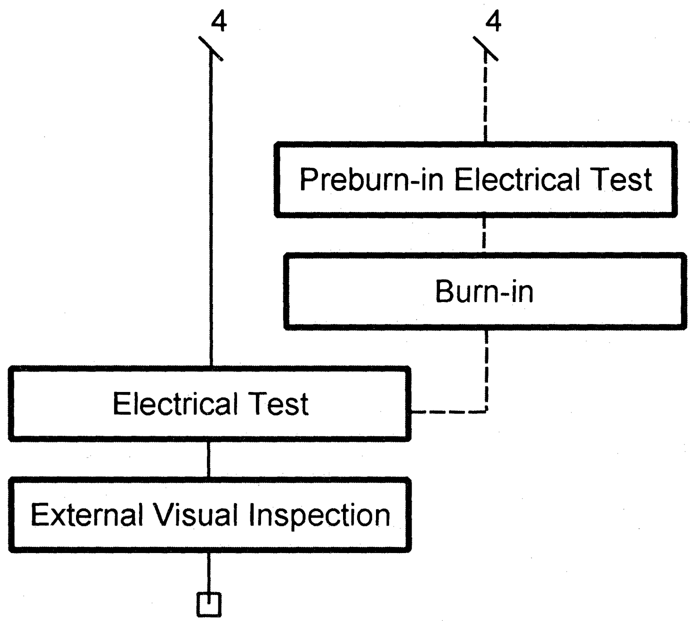
Electrostatic discharge testing
Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device.

CMOS latch-up test
CMOS latch-up test is performed to determine the sensitivity of a device input to overshoot and undershoot signals connected to device inputs.

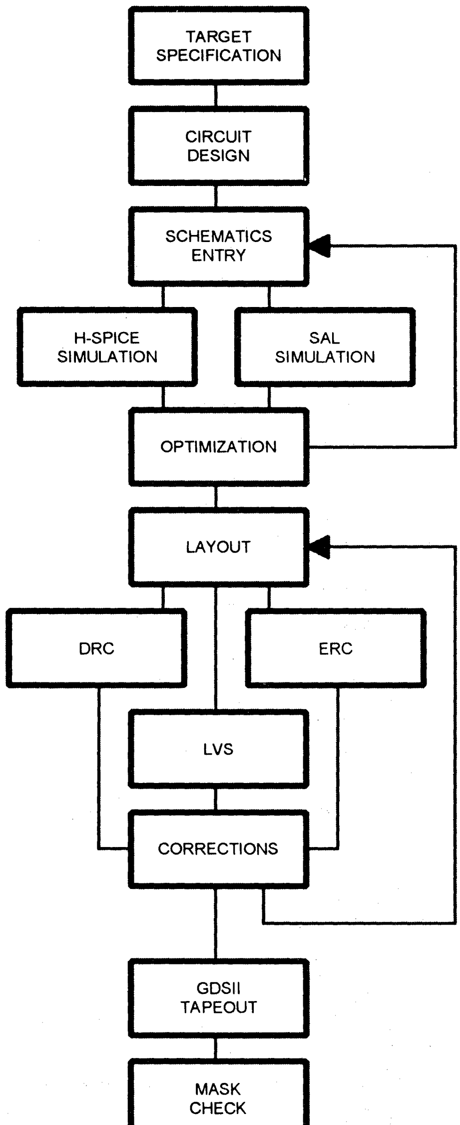
Commercial and Industrial Product Flows



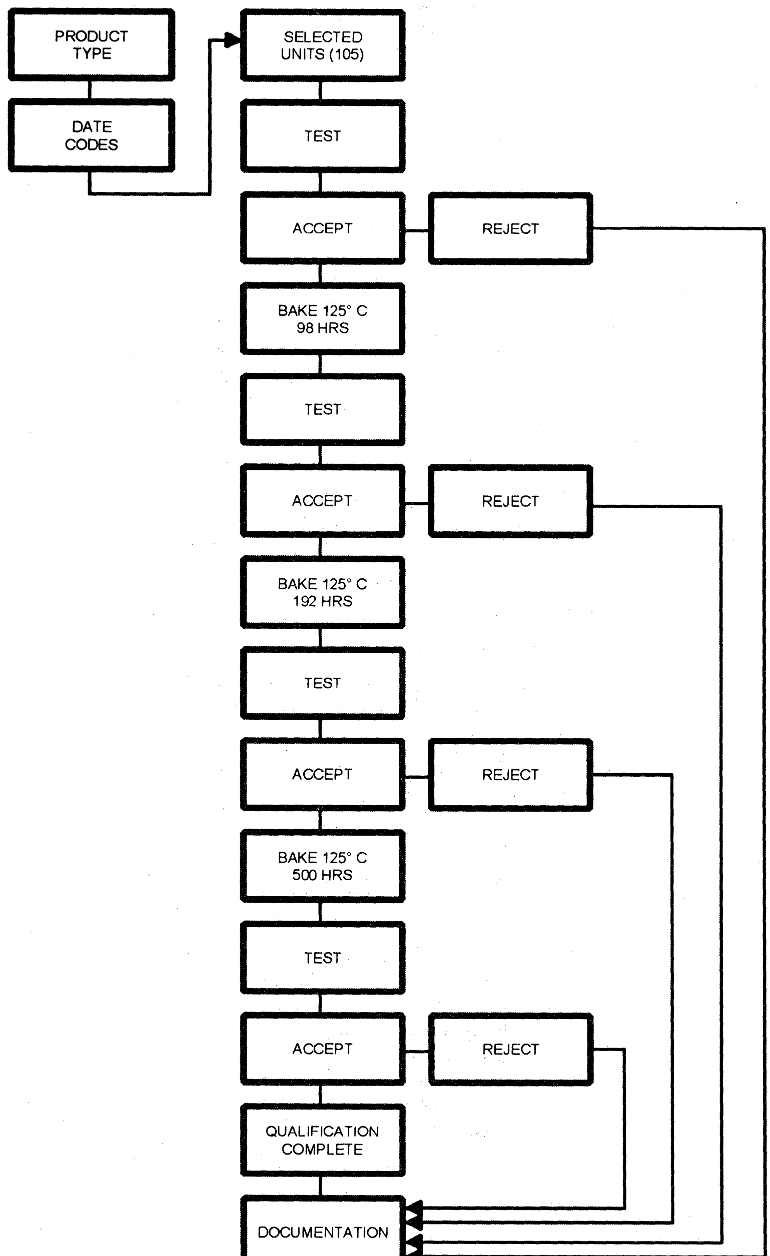

1
2
Wafer Fabrication
Wafer Probe
Wafer Saw & Dice
High MagnificationVisual
Die Bank
3
Die Attach
Wire Bonding
Low Magnification Visual
Mold and cure
Visual Inspection
4


4
4
Preburn-in Electrical Test
Burn-in
Electrical Test
External Visual Inspection

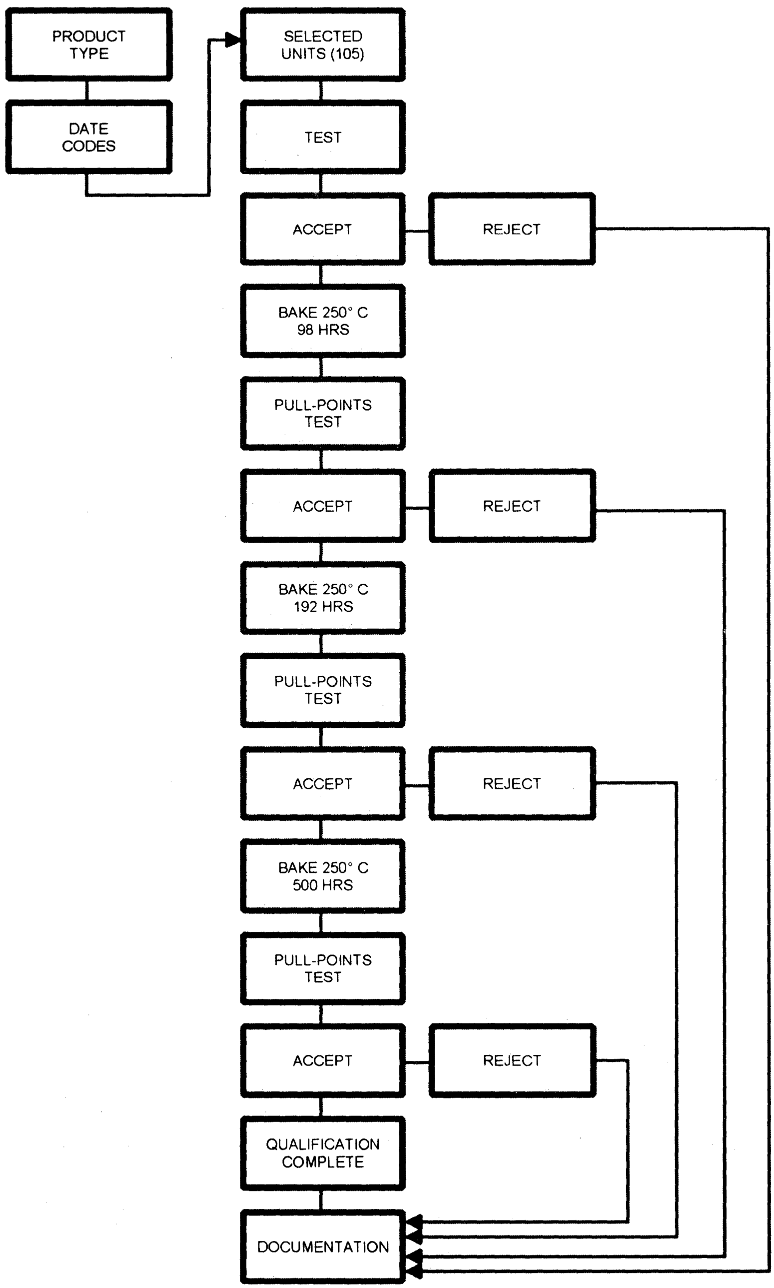
Design and Layout Flow



TEMPERATURE CYCLE FLOW



85 / 85 BIAS CYCLE FLOW



HIGH TEMPERATURE OPERATING LIFE

2.0 LONG TERM FAILURE RATE SUMMARY

2.1 Long Term Failure Rate Determination

A High temperature Operating Life test is used to estimate long term reliability. By operating the devices at accelerated temperature and voltage, hundreds of thousands of use hours can be compressed into thousands of test hours. The method used to estimate failure rates from stress data is summarized.

Method:	MIL-STD-883, method 1005.
Test:	High Temperature Operating Life Test (HTOL)
Conditions:	Dynamic Operating Conditions, VCC = 5.50 Volts, 150° C, Frequency = 2 MHz.
Duration:	Long term Failure Rate is minimum 168 hours HTOL at 150° C periodically tested to 500 hours.
Reliability:	Failure mechanisms common to semiconductor components are accelerated by temperature and voltage. In calculating failure rates, though, only temperature acceleration is included.
Acceptance criteria:	0/116

3.0 HIGH TEMPERATURE STORAGE TEST

The High Temperature Steady State Life test is used to accelerated ionic contamination problems. Static bias is used because a constant voltage gradient accelerated diffusion of ionic species. The method used to estimate failure rates from stress data is summarized.

Method:	MIL-STD-883, method 1008.
Conditions:	1000 hrs, unbiased 150° C.
Acceptance criteria:	0/116

4.0 PACKAGE STRESS TESTS

Startech Semiconductor Reliability qualifies and continuously monitors the packaging reliability to ensure exceptional resistance to environmental stress. Package reliability stress testing and failure rates are summarized.

4.1 Pressure Cooker Test "plastic package only"

Method:	JEDEC STD-22, method 102
Test:	Pressure Cooker Test (PCT)
Conditions:	15 PSIG, 121 ° C, No bias, 168 hrs, 100% RH, 2 ATM.
Purpose:	The Pressure Cooker Test is a highly accelerated packaging stress test used to ensure environmental durability of epoxy packaged parts. Passivation cracks, ionic contamination and corrosion susceptibility are all accelerated by this stress.
Failure:	Any device which fails to meet all data sheet requirements is classified as a failure.
Acceptance criteria:	0/76

5.0 Temperature Cycle Test

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes. If the materials do not expand and contact equally, large stresses can develop.

Test:	Temperature Cycle
Conditions:	MIL-STD-883C, Method 1010 test stress mechanical integrity by exposing a device to alternating temperature extremes. Weakness and thermal expansion mismatches in die interconnections, die attach, and wire bonds are often detected with this acceleration test.
Temperature:	-65° C to +150° C.
Purpose:	100 cycles minimum, periodically tested to 1000 cycles
Failure:	Any device which fails to meet all data sheet requirements is classified as a failure.
Acceptance criteria:	0/76

ESD AND LATCH-UP TEST

6.0 Latch-up Sensitive

Test:	Latch-up Sensitivity
Method:	JEDEC-STD-17
Conditions:	Current Injection = ±200mA Trigger or 2X VCC, Hot Socket = Vcc 0-7 Volts, Vcc Oscillation at Vcc = 3.5-7.0 Volts at 1 MHz, Temperature = 25° C.
Purpose:	The latch-up test is designed to test resistance of the devices to extreme voltage and current excursions. Latch-up has historically been a problem associated with CMOS devices.
Failure:	Any device which fails the Latch-up test if Latch-up occurs at less than 200mA of current.
Acceptance criteria:	0/5

6.1 Results:

All products are tested for latch-up during qualification.

Outputs:	All outputs are tested using a hot socket technique where the full voltage is applied instantly, on a voltage ramp, where voltage is increased slowly. During the hot socket technique, a maximum of 400 mA was allowed in order to protect the outputs from overstress.
Inputs:	All inputs are tested using both the hot socket technique and the voltage ramp technique.

6.2 Conclusion:

Startech Semiconductor products are very resistant to latch-up.

7.0 Electrostatic Discharge (ESD)

Test:	Electrostatic Discharge
Conditions:	MIL-STD-883C, Method 3015
Purpose:	The ESD test established the sensitive of device to electrostatic discharge of the type than can occur during ordinary handling.
Failure:	A device fails the ESD stress test is any pin combination defined in method 3015 of MIL-STD-883C is damaged after testing with a 2000 Volts discharge. Data sheet electrical testing is performed to determine if a device has been damaged.
Acceptance criteria:	0/3

7.1 Results:

All Startech Semiconductor products are tested for resistance to ESD during qualification. All pins pass ESD testing at 2000 Volts.

7.2 Conclusion:

Startech Semiconductor products are not ESD sensitive per the definition of MIL-STD-883C.

ORDERING INFORMATION 9

ORDERING INFORMATION AND PART NUMBERING GUIDE

Prefix	**Device**	**Suffix** -	**Pin Count**	**Option Code**
ST	XX C XXX	XX	XX	XX

- ST — Company ID
- XX C XXX — Part Number
- Suffix XX — Temperature
- Suffix XX — Package
- Pin Count XX — Number of the packaged pins
- Option Code XX — Options

Temperature Range

C	Commercial	0° C	To	+70° C
I	Industrial	-40° C	To	+85° C
M	Military	-55° C	To	+125° C

Package Type

P	Plastic Dip
C	Ceramic
D	Cerdip
L	Leadless Chip Carrier (LCC)
J	Plastic Leaded Chip Carrier (PLCC)
F	Flat Pack(SOIC)
Q	Quad Flat Pack
G	Pin Grid
T	Thin Shrink Small Outline Package (TSSOP)

PACKAGE MARKING INFORMATION (EXCEPT CLOCK SYNTHESIZERS AND TQFP PACKAGES)

Prefix	**Device**	**Suffix**	**Custom Marking**
ST	XX C XXX	XX	XXX

ST — Company ID
XX C XXX — Part Number
XX (first character) — Operating Temperature Range
XX (second character) — Package Type
XXX — Custom Packaged/Bonded

DATE CODE AND OPTIONS MARKING

X 9X XX - XXX

X — Revision
9X — Year
XX — Week
XXX — Custom (Special parts only)

"ST16C452" DATE CODE AND OPTIONS MARKING

X XX 9X XX

X — Revision
XX — Product type
9X — Year
XX — Week

PACKAGE MARKING INFORMATION (CLOCK SYNTHESIZERS)

Prefix ST — Company ID

Device XX C XXX — Part Number

DATE CODE AND OPTIONS MARKING

X 9X XX - XX

- REVISION — X
- YEAR — 9X
- WEEK — XX
- OPTION CODES — XX

48-TQFP PACKAGE MARKING INFORMATION

Prefix ST — Company ID

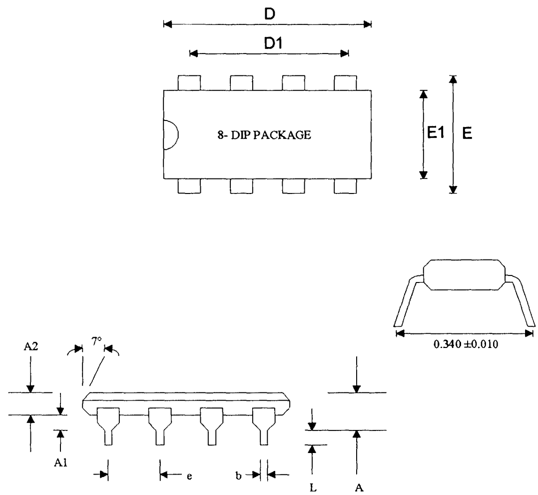
Device XX C XXX — Part Number

DATE CODE AND OPTIONS MARKING

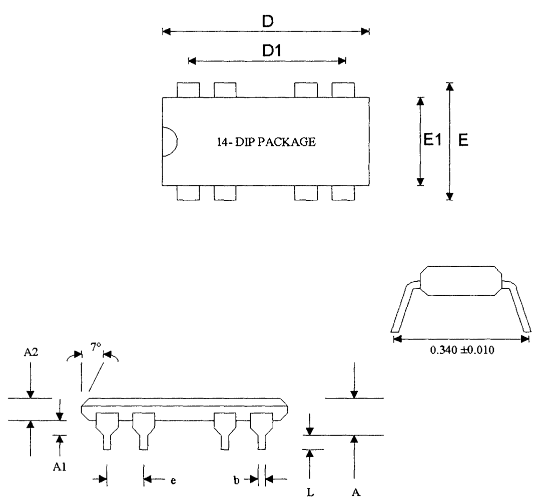
XX X 9X XX

- Operating Temperature Range — X
- Package — X
- Revision — X
- Year — 9X
- Week — XX

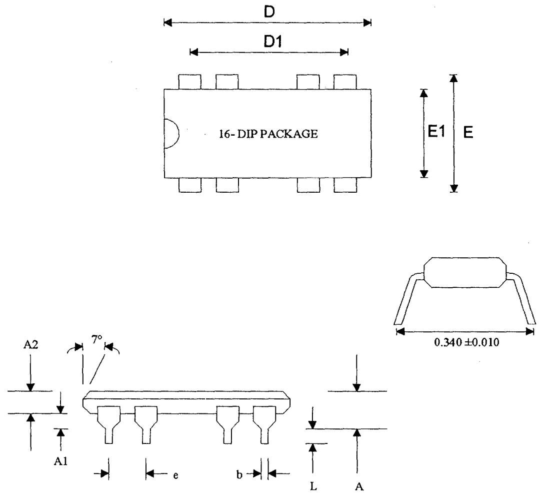
PACKAGING INFORMATION 10



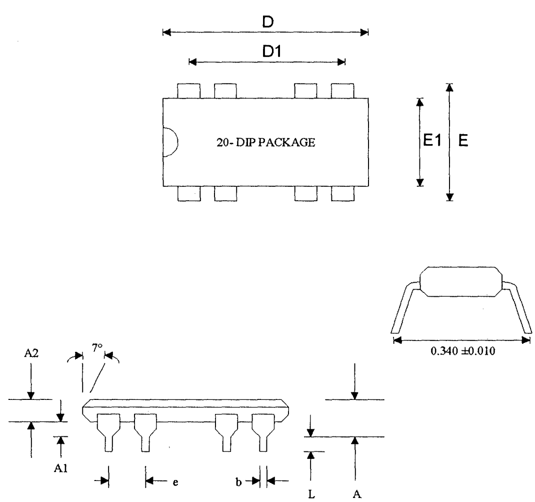
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	0.365 ±0.005
D1	0.300
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



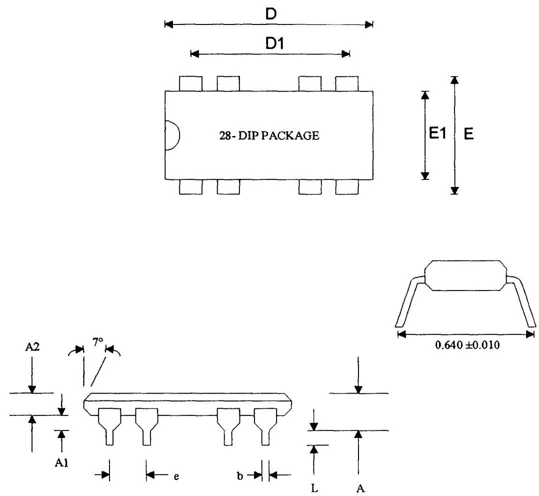
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	0.750 ±0.005
D1	0.600
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



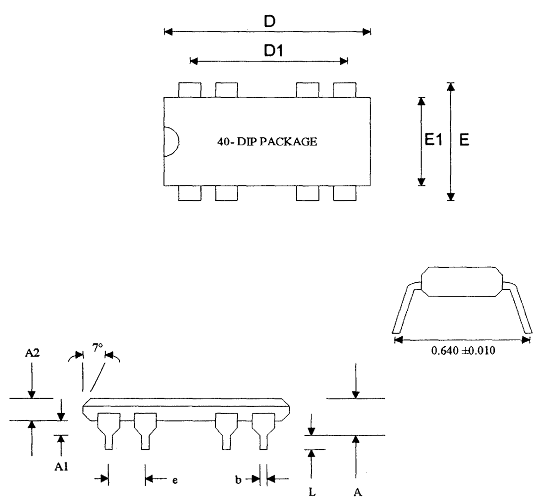
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	0.750 ±0.005
D1	0.700
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



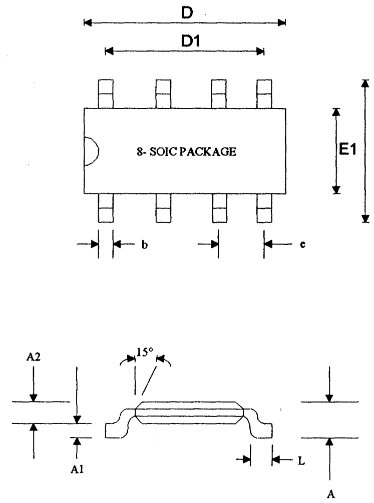
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	1.020 ±0.005
D1	0.900
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



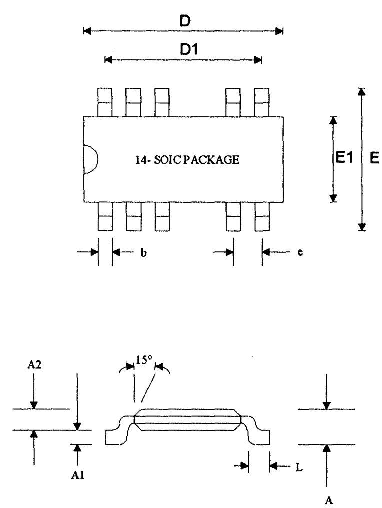
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.150 ±0.005
D	1.450 ±0.005
D1	1.300
E	0.610 ±0.010
E1	0.550 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



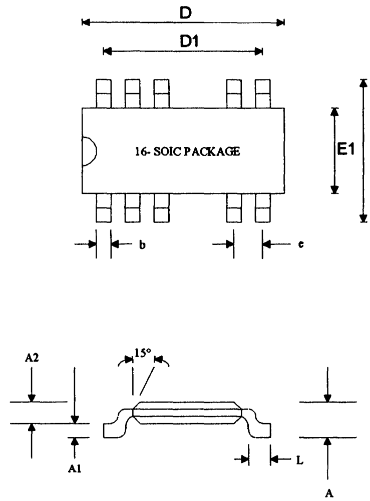
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.150 ±0.005
D	2.050 ±0.005
D1	1.900
E	0.610 ±0.010
E1	0.550 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



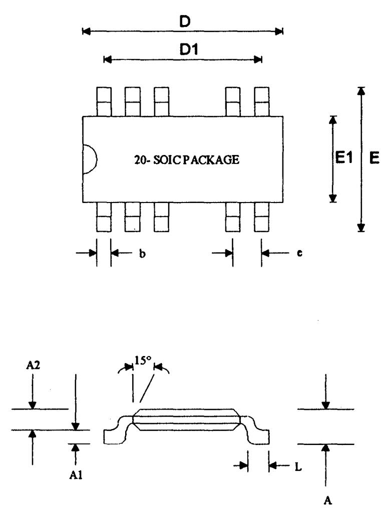
DIMENSIONS	TOLERANCE (Mil)
A	0.061 ±0.004
A1	0.004 ~ 0.010
A2	0.054 ±0.002
D	0.193 ±0.002
D1	0.150
E	0.236 ±0.008
E1	0.154 ±0.002
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



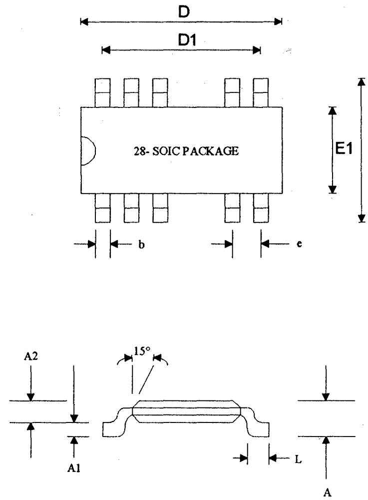
DIMENSIONS	TOLERANCE (Mil)
A	0.061 ±0.004
A1	0.004 ~ 0.010
A2	0.054 ±0.002
D	0.340 ±0.002
D1	0.300
E	0.236 ±0.008
E1	0.154 ±0.002
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



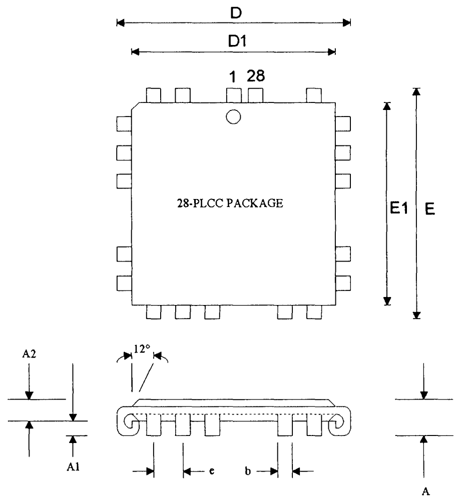
DIMENSIONS	TOLERANCE (Mil)
A	0.061 ±0.004
A1	0.004 ~ 0.010
A2	0.054 ±0.002
D	0.390 ±0.002
D1	0.350
E	0.236 ±0.008
E1	0.154 ±0.002
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



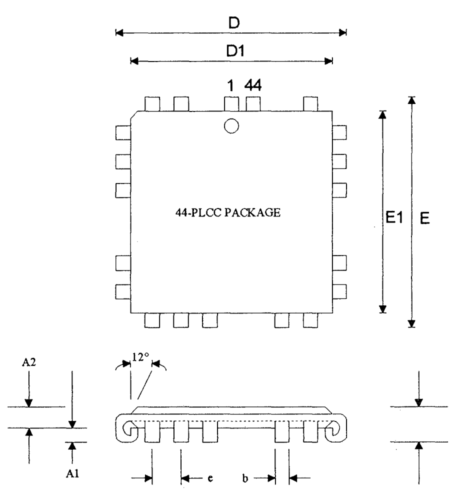
DIMENSIONS	TOLERANCE (Mil)
A	0.101 ±0.010
A1	0.006 ~ 0.008
A2	0.092 ±0.005
D	0.504 ±0.005
D1	0.450
E	0.406 ±0.010
E1	0.289 ±0.005
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



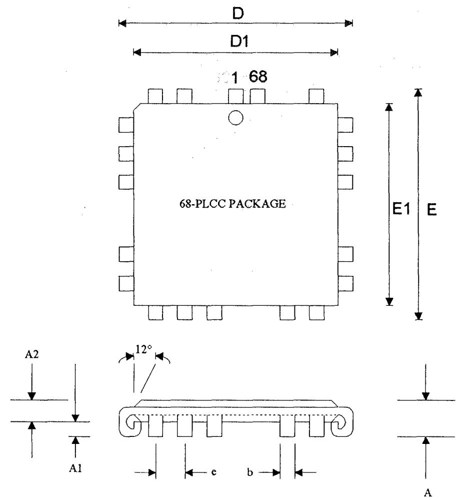
DIMENSIONS	TOLERANCE (Mil)
A	0.101 ±0.010
A1	0.006 ~ 0.008
A2	0.092 ±0.005
D	0.704 ±0.005
D1	0.650
E	0.406 ±0.010
E1	0.289 ±0.005
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



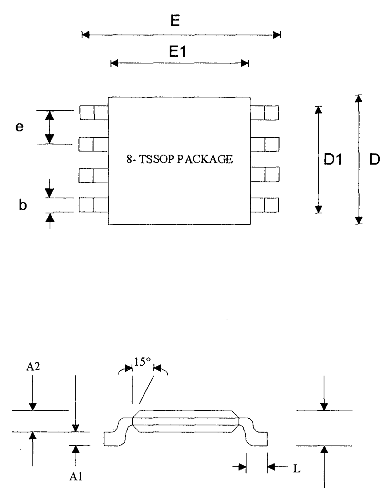
DIMENSIONS	TOLERANCE (mil)
A	0.170±0.005
A1	0.020
A2	0.150 ±0.002
D	0.490 ±0.005
D1	0.454 ±0.002
E	0.490 ±0.005
E1	0.454 ±0.002
e	0.050±0.002
b	0.030±0.005



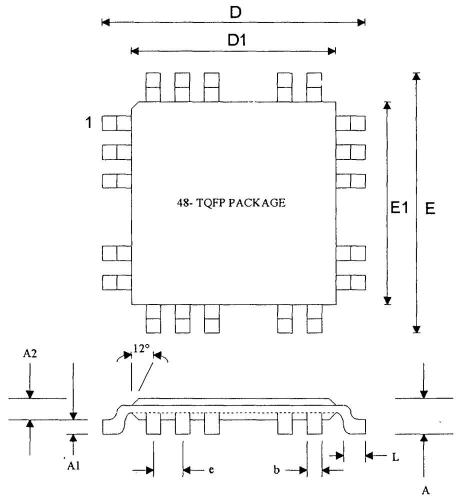
DIMENSIONS	TOLERANCE (mil)
A	0.170±0.005
A1	0.020
A2	0.150 ±0.002
D	0.690 ±0.005
D1	0.654 ±0.002
E	0.690 ±0.005
E1	0.654 ±0.002
e	0.050±0.002
b	0.030±0.005



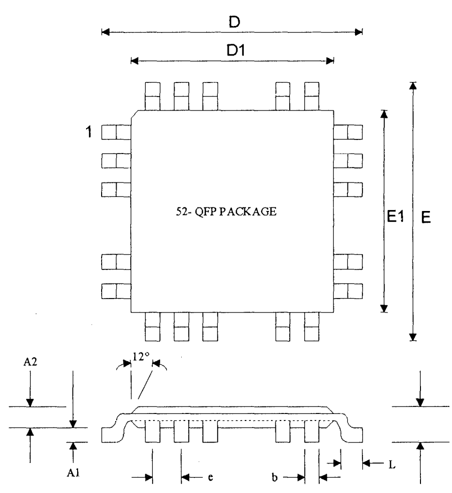
DIMENSIONS	TOLERANCE (mil)
A	0.170±0.005
A1	0.020
A2	0.150 ±0.002
D	0.990 ±0.005
D1	0.954 ±0.002
E	0.990 ±0.005
E1	0.954 ±0.002
e	0.050±0.002
b	0.030±0.005



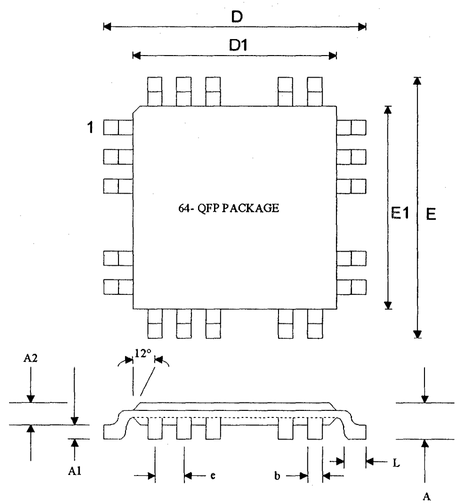
DIMENSIONS	TOLERANCE (Mil)
A	0.0390 ±0.004
A1	0.004 ± 0.002
A2	0.0323 ±0.002
D	0.118 ±0.002
D1	
E	0.250 ±0.006
E1	0.173 ±0.002
L	0.020 ±0.002
e	0.0256
b	0.17 ±0.02



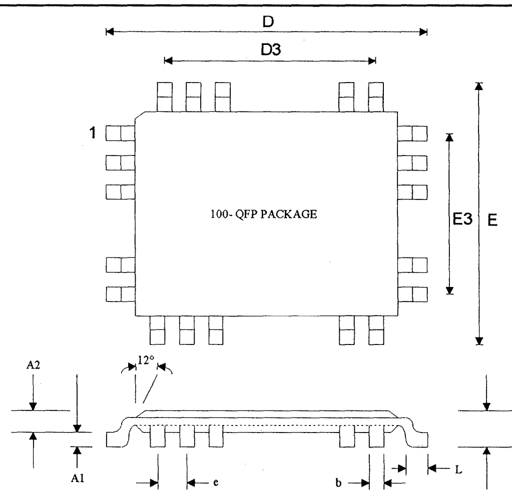
DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.05 - 0.10
A2	1.0 ±0.5
D	9.0 ±0.25
D1	7.0 ±0.10
E	9.00 ±0.25
E1	7.0 ±0.10
L	0.6 ±0.15
e	0.5
b	0.22 +0.05



DIMENSIONS	TOLERANCE (mm)
A	2.26 ±0.13
A1	0.23 ±0.07
A2	2.03 ±0.06
D	14.1 ±0.20
D1	10 ±0.10
E	14.1 ±0.20
E1	10 ±0.10
L	0.88 ±0.15
e	0.65
b	0.30 ±0.08

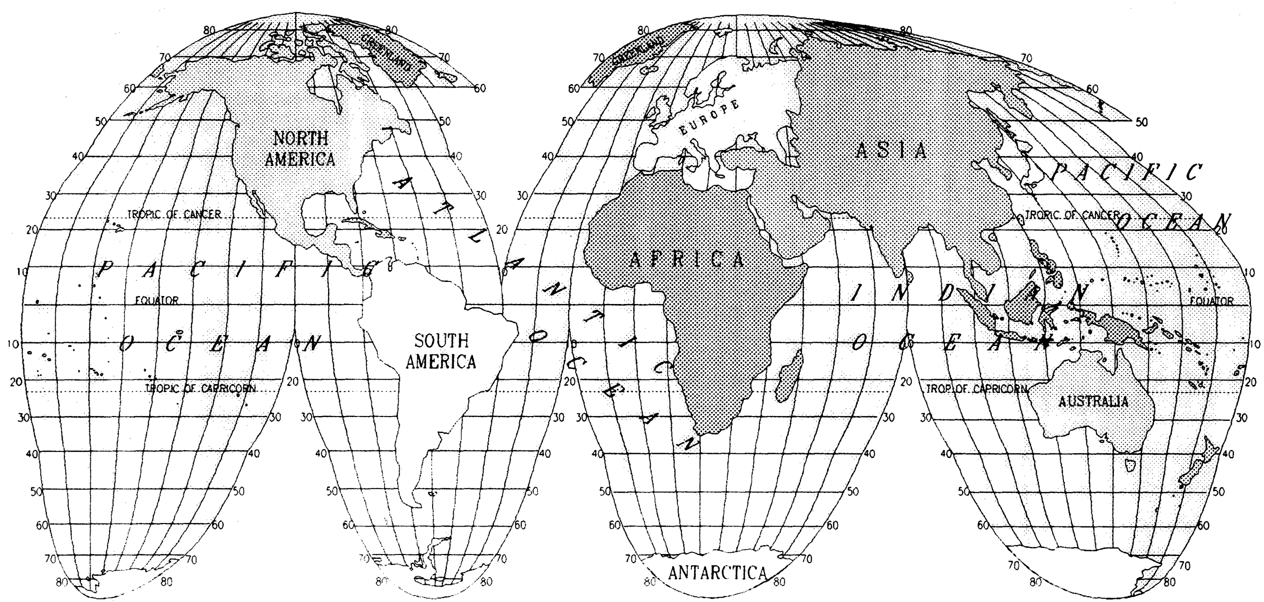


DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.15 ±0.01
A2	1.0 ±0.05
D	12.0 ±0.10
D1	10.0 ±0.10
E	12.0 ±0.10
E1	10.0 ±0.10
L	0.60 ±0.15
e	0.50
b	0.22 ±0.04



DIMENSIONS	TOLERANCE (mm)
A	3.04 ±0.30
A1	0.30 -0.03
A2	2.71 ±0.16
D	23.20 ±0.25
D3	18.85
E	17.20 ±0.25
E3	12.35
L	0.65 ~ 0.95
e	0.65
b	0.22 ~ 0.38

REPRESENTATIVES 11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