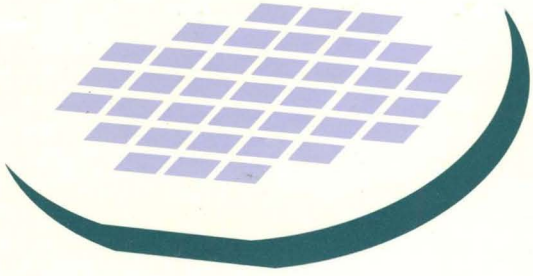

STARTECH

SEMICONDUCTOR, INC.

DATA BOOK

1994

STARTECH

Component Data

Catalog

Printed February 23, 1994

STARTECH Semiconductor Inc.
1219 BORDEAUX Dr. SUNNYVALE, CA 94089
TEL (408) 745-0801 FAX (408) 745-1269

President's Message

To our valued customer:

Startech Semiconductor was founded in 1990, with the charter to design, manufacture and market high performance data communication peripheral products in both the commercial and industrial semiconductor markets. Since then, Startech continues to follow that charter and enjoys a rapid growth.

Startech's products are marketed and distributed through a world-class network of representatives and distributors.

At Startech, we are dedicated to keeping your designs competitive with leading edge solutions. All our products are low power, high performance, CMOS ICs. Our commitment to you is to provide you with high quality and reliable ICs.

Ram K. Reddy

Introduction

President

Dear customer,

Startech Semiconductor is proud to present you with our updated January, 94 Data Book. Startech's technical staff have worked together to provide you with the most accurate, up-to-date information.

We believe that when you design our products in your systems, you have started a partnership with a company that is committed to work with the customers and deliver quality products. Startech offers to customize any of these standard products to meet your special requirements.

If you have any questions or comments, please call us directly.

Startech Semiconductor Technical Staff

Art Khachaturian
Vice President

Contents

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DIFFERENTIAL LINE DRIVERS

National Semiconductor	Startech Semiconductor
DS26C31/DS26LS31	ST26C31
DS34C86/DS34LS86	ST34C86
AMD	Startech Semiconductor
AM26LS31	ST26C31

DIFFERENTIAL LINE RECEIVERS

National Semiconductor	Startech Semiconductor
DS26C32/DS26LS32	ST26C32
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AMD	Startech Semiconductor
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Motorola Semiconductor	Startech Semiconductor
MC34050	ST34C50
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ICS2494XXX	ST49C214-XX
ICS9064	ST49C064
Avasem Corporation	Startech Semiconductor
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STEREO CLOCK GENERATOR

MicroClock Inc.	Startech Semiconductor
MK1418	ST49C418

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ST26C31	DS26C31/DS26LS31
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	AM26LS31
	National Semiconductor
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	VL16C450
	Western Digital Inc.
	WD16C450
	Texas Instruments
	TL16C450
	Exar Corporation
	XR16C450

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	Silicon Systems SSI73M550
	VLSI Technology, Inc. VL16C550
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	Integrated Circuit Systems, Inc. ICS9064
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STARTECH

ST49C064

Printed February 23, 1994

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

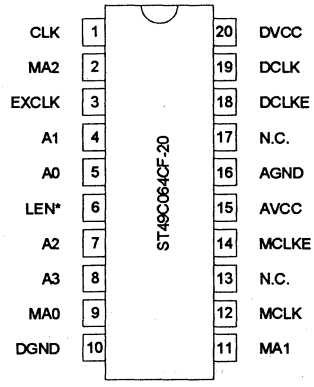
GENERAL DESCRIPTION

The ST49C064 is a monolithic analog CMOS device designed to generate dual frequency outputs from fifteen possible combinations for video Dot clock frequencies and eight memory clock frequencies for high performance video display systems. The ST49C064 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2μ process to achieve 130 MHz speed for high end frequencies.

The ST49C064 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C064 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device).

The ST49C064 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and three address lines for memory clock selection.

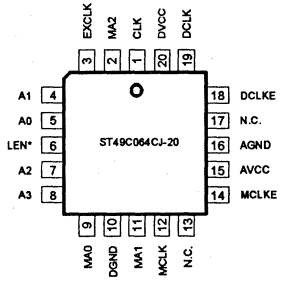
SOIC Package



FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS90C64
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip / SOIC / PLCC packages
- Compatible with Western Digital Imaging Video Graphics Array clock requirements.

PLCC Package

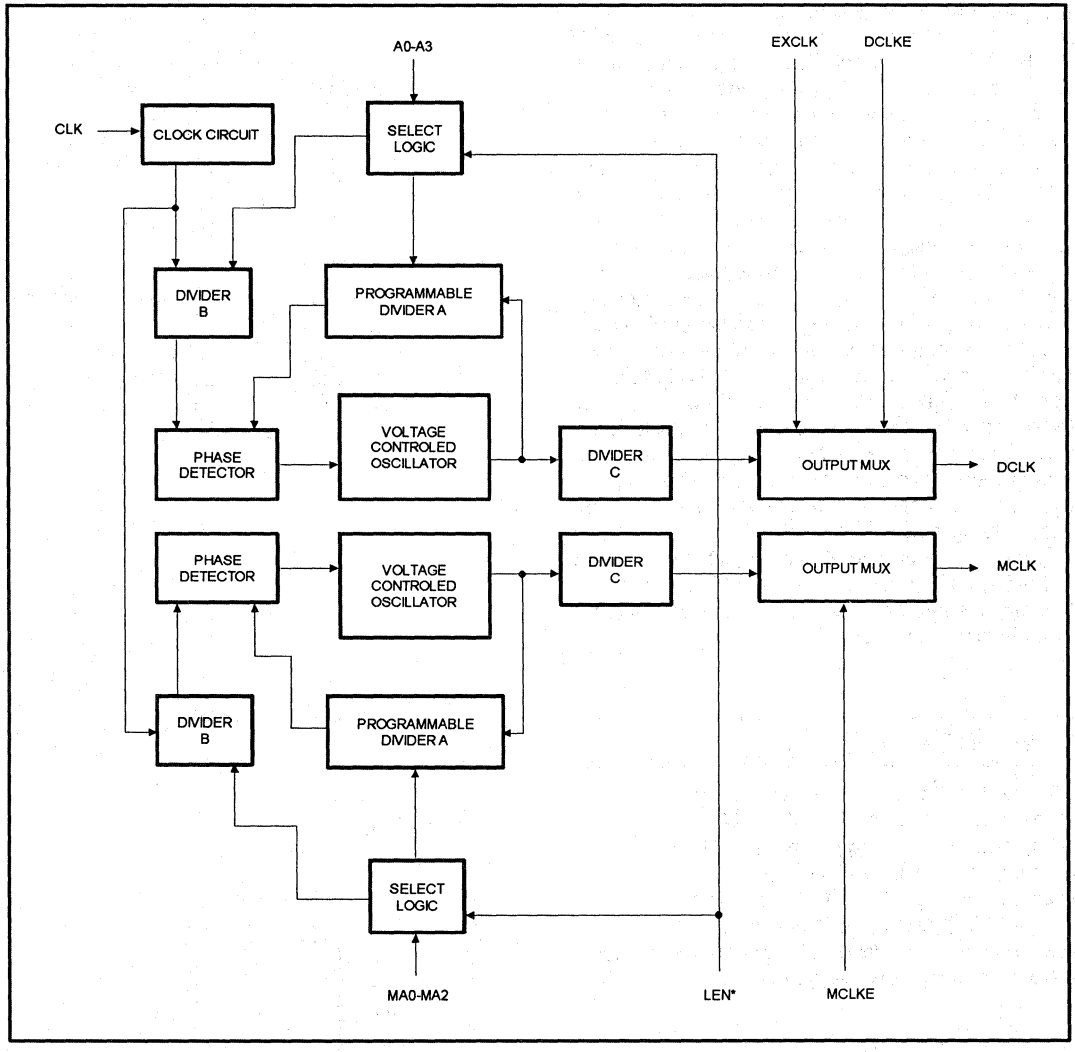


ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C064CP20-xx	Plastic-DIP	0° C to +70° C
ST49C064CF20-xx	SOIC	0° C to +70° C
ST49C064CJ20-xx	PLCC	0° C to +70° C

ST49C064

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CLK	1	I	External 14.318 MHz system reference clock input.
MA2	2*	I	Memory clock Frequency select address 3.
EXCLK	3*	I	External clock input. For additional clock frequency.
A1	4*	I	Dot clock Frequency select address 2.
A0	5*	I	Dot clock Frequency select address 1.
LEN*	6*	I	Address latch enable input (active low). To latch selected programmed clock output.
A2	7*	I	Dot clock Frequency select address 3.
A3	8*	I	Dot clock Frequency select address 4.
MA0	9*	I	Memory clock Frequency select address 1.
DGND	10	O	Digital ground.
MA1	11*	I	Memory clock Frequency select address 2.
MCLK	12	O	Programmed memory clock output frequency.
N.C.	13		No connect.
MCLKE	14*	I	MCLK output enable.
AVCC	15	I	Analog supply voltage. Single +5 volts.
AGND	16	O	Analog ground.
N.C.	17		No connect.
DCLKE	18*	I	DCLK output enable.
DCLK	19	O	Programmed video clock output frequency.
DVCC	20	I	Digital supply voltage. Single +5 volts.

* Have internal pull-up resistors on inputs

ST49C064

GENERAL INFORMATION

The ST49C064 is programmed to generate 15 different video clock frequencies using the A0-A3 inputs and 8 different memory frequencies using M0-M2 inputs. The address lines A2-A3 can be connected to video controller like Western Digital Imaging VGA controllers. Address lines A0 and A1 are latched with LEN* pin which is generated from video controllers to select proper Dot clock output. All inputs to the ST49C064 contain internal pull-up resistors including CLK and EXCLK inputs.

The EXCLK is additional input that may be internally connected to the DCLK output. The additional input is useful for supporting modes that require frequencies not provided by the ST49C064.

FREQUENCY SELECT CALCULATION

The ST49C064 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.
The accuracy of the frequencies produced by the ST49C064 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

DCLK = (Reference clock) X (A/B.C)
MCLK = (Reference clock) X (A/B.C)

where A=1,2,3,.....127,
B=1,2,3,.....127, and
C=1,2,4

For proper output frequency, the ST49C064 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask options are provided for custom applications.

* Any frequency can be in any decoding position.
* DCLK, can control selection of the internal frequencies.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	
I_{IH}	Input high current			1	µA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load. DCLK=80MHz, MCLK=40MHz
R_{in}	Internal pull-up resistance	15	20	25	kΩ	

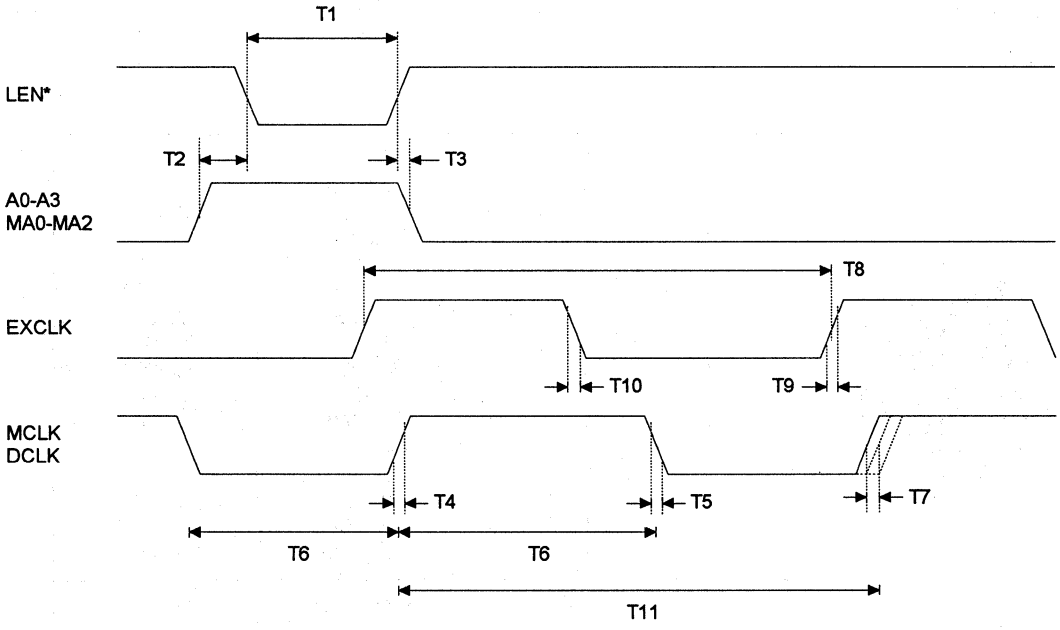
ST49C064

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1	1.5	ns	0.8V - 2.0V
T_5	Fall time		1	1.5	ns	2.0V - 0.8V
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

TIMING DIAGRAM



ST49C064

					ST49C064	ST49C064
Video clock address (Hex)	A3	A2	A1	A0	Frequency (MHz)	Frequency (MHz)
0	0	0	0	0	30.000	30.000
1	0	0	0	1	77.250	77.250
2	0	0	1	0	EXCLK	EXCLK
3	0	0	1	1	80.000	80.000
4	0	1	0	0	31.500	31.500
5	0	1	0	1	36.000	36.000
6	0	1	1	0	75.000	75.000
7	0	1	1	1	50.000	50.000
8	1	0	0	0	40.000	40.000
9	1	0	0	1	50.000	50.000
A	1	0	1	0	32.000	32.000
B	1	0	1	1	44.900	44.900
C	1	1	0	0	25.175	25.175
D	1	1	0	1	28.322	28.322
E	1	1	1	0	65.000	65.000
F	1	1	1	1	36.000	36.000
Memory clock address (Hex)		MA2	MA1	MA0	Frequency (MHz)	Frequency (MHz)
0		0	0	0	33.000	41.612
1		0	0	1	49.218	37.500
2		0	1	0	60.000	49.128
3		0	1	1	30.500	44.296
4		1	0	0	41.612	
5		1	0	1	37.500	
6		1	1	0	49.128	
7		1	1	1	44.296	

Compatible with Video Controller	ICS9064 WD90C30	AV9064 WD90C30

STARTECH

ST49C101

Printed February 23, 1994

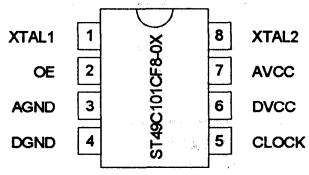
PREPROGRAMMED HIGH SPEED FREQUENCY MULTIPLIER

1

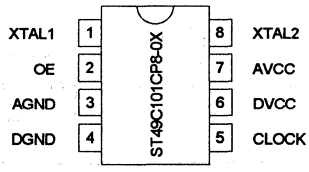
DESCRIPTION

The ST49C101 is a mask programmable monolithic analog CMOS device, designed to replace existing high frequency crystal/oscillator with single low frequency crystal. The ST49C101 provides high speed and low jitter clock output.
ST49C101 is designed in a 1.2μ process to achieve 150 MHz speed for high end frequencies.

SOIC Package



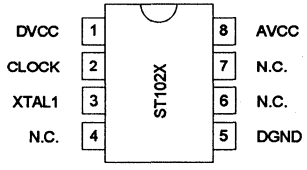
Dip Package



FEATURES

- Can replace expensive high frequency oscillator.
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package.
- Crystal oscillator circuit on board

TSSOP Package

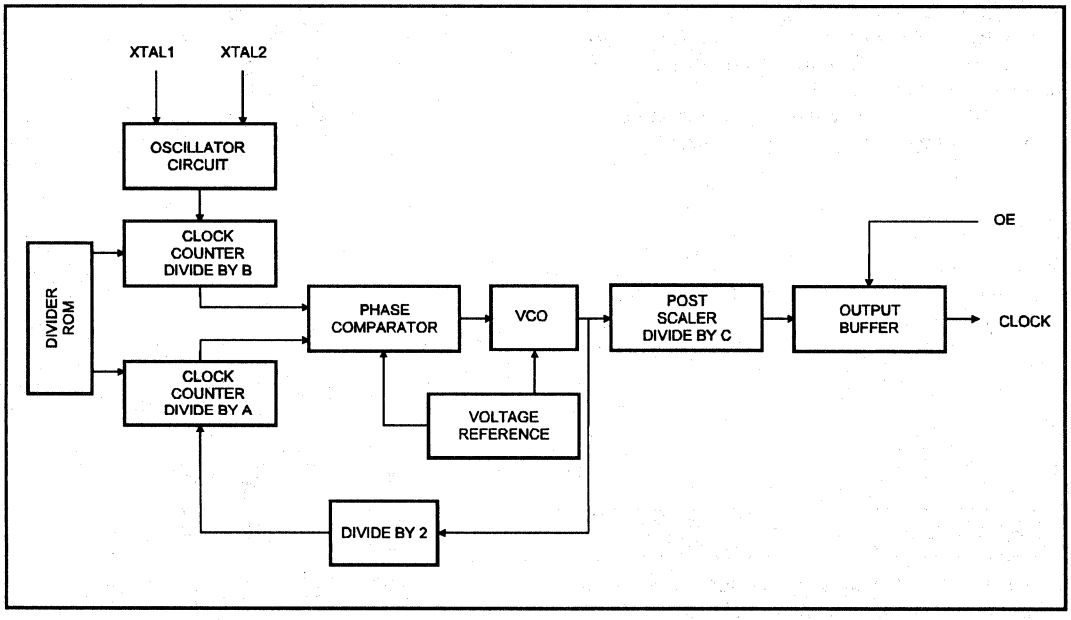


ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C101CP8	Plastic-DIP	0 ° C to +70° C
ST49C101CF8	SOIC	0° C to +70° C
ST102XCT8	TSSOP	0° C to +70° C

ST49C101

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL1	1	I	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 10.00 MHz clock, XTAL2 is left open or used as buffered clock output.
OE	2*	I	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
AGND	3	O	Analog ground.
DGND	4	O	Digital ground.
CLOCK	5	O	Programmed output clock.
DVCC	6	I	Positive supply voltage. Single +5 volts.
AVCC	7	I	Analog supply voltage. Single +5 volts.
XTAL2	8	O	Crystal output.

* Has internal pull-up resistor

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C101 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C101 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X 2A/(B.C)

where A=5, 6, 7,.....128
B=5, 6, 7,.....128
C=1,2,4

For proper output frequency, the ST49C101 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

Preprogrammed options:

ST49C101-X	Ref. frequency	Output frequency
ST49C101-01	8.33 MHz	100 MHz
ST49C101-02	10 MHz	132 MHz

ST49C101

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

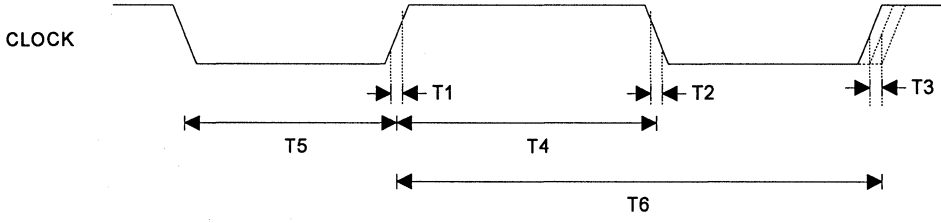
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-100	µA	Pin 2 only
I_{IH}	Input high current			1	µA	V_{IN}=Vcc Pin 2
I_{CC}	Operating current		20	30	mA	No load. CLOCK=120MHz
R_{IN}	Input pull-up resistance	50	75	100	KΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	CLOCK rise time		1	1.5	ns	Load=50Ω 0.5V - 2.8V
T_2	CLOCK fall time		1	1.5	ns	Load=50Ω 2.8V - 0.5V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	VCC/2 switch point
T_3	Jitter		±85	±100	ps	
T	Input frequency	5	10	40	MHz	
T_6	CLOCK frequency change		0.01		%	

TIMING DIAGRAM



ST49C101

STARTECH

ST49C103
ST49C104

Printed February 23, 1994

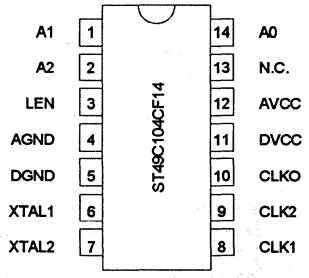
PREPROGRAMMED FREQUENCY GENERATOR

DESCRIPTION

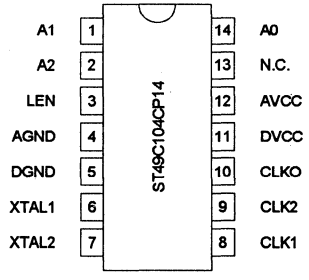
The ST49C103 and ST49C104 are mask programmable monolithic analog CMOS devices designed to generate up to 8 single frequency outputs from a single input clock. The ST49C104 will provide eight different output frequencies and the ST49C103 will provide four different output frequencies. They are designed in a 1.2μ process to achieve 130 MHz speed for high end frequencies.

The ST49C103 and ST49C104 are designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C104 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The latch enable pin is also mask programmable to be active high, active low or rising or falling edge sensitive.

SOIC Package



Plastic-DIP package



FEATURES

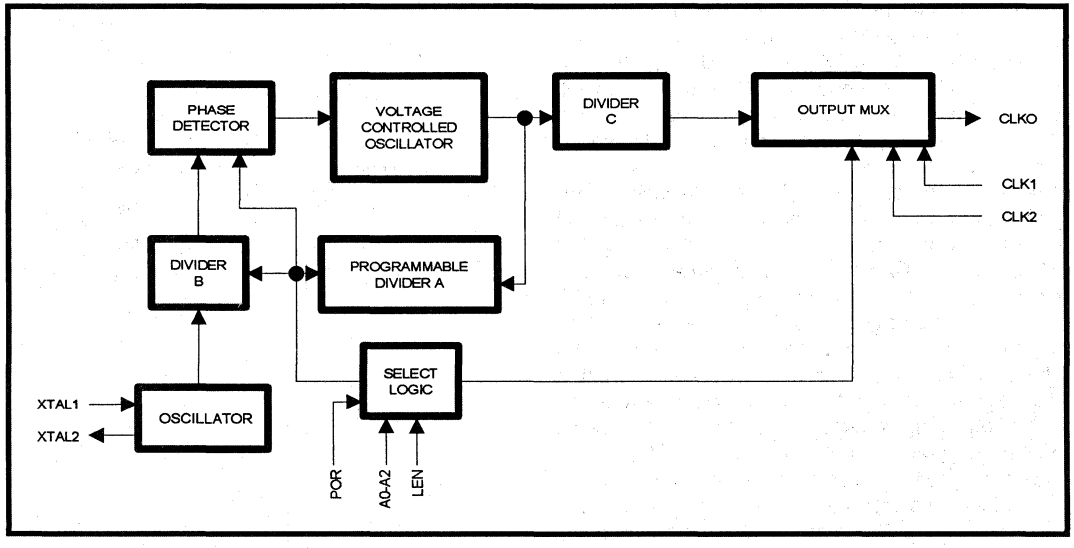
- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9103/104
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 or 14 pin DIP or SOIC package.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C103CP8	Plastic-DIP	0° C to +70° C
ST49C103CF8	SOIC	0° C to +70° C
ST49C104CP8	Plastic-DIP	0° C to +70° C
ST49C104CF8	SOIC	0° C to +70° C
ST49C104CP14	Plastic-DIP	0 ° C to +70° C
ST49C104CF14	SOIC	0° C to +70° C

ST49C103/104

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C104 14 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
LEN	3*	I	Address latch enable input. To latch selected programmed clock output.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
XTAL1	6	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	O	Crystal output.
CLK1	8	I	External clock 1 input.
CLK2	9	I	External clock 2 input / output select.
CLKO	10	O	Programmed output clock.
DVCC	11	I	Digital supply voltage. Single +5 volts.
AVCC	12	I	Analog supply voltage. Single +5 volts.
N.C.	13		
A0	14	I	Frequency select address input 1.

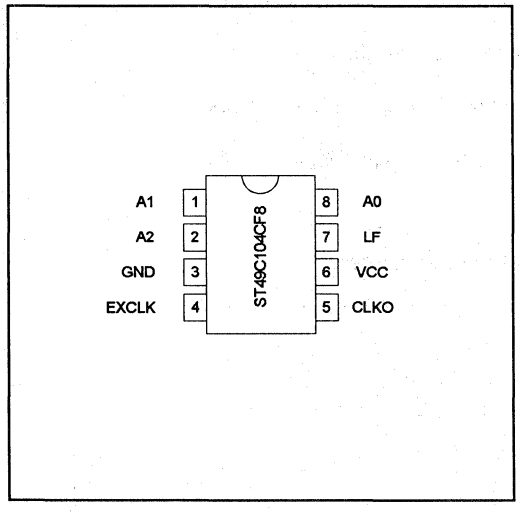
* Have internal pull-up resistors on inputs.

ST49C103/104

SYMBOL DESCRIPTION (ST49C104 8 pin package)

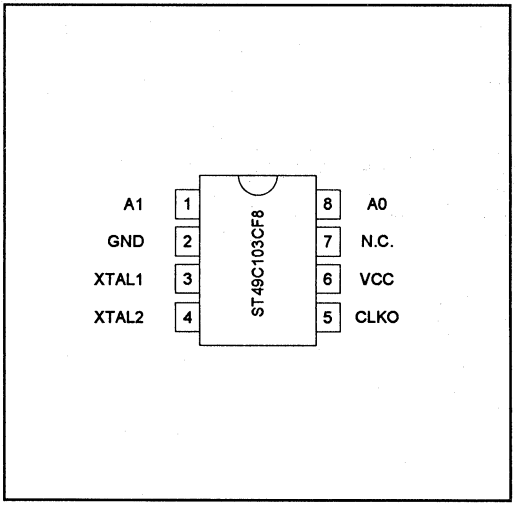
Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
GND	3	O	Digital ground.
EXCLK	4	I	External clock input. Internal phase locked loop reference clock .
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
N.C.	7		
A0	8	I	Frequency select address input 1.

* Has internal pull-up resistor on input



SYMBOL DESCRIPTION (ST49C103 8pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
GND	2	O	Digital ground.
XTAL1	3	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
N.C.	7		
A0	8	I	Frequency select address input 1.



ST49C103/104

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C104 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C104 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B.C)

where A=1,2,3,.....127
B=8, 16, 32 ,64
C=1,2,4,8

For proper output frequency, the ST49C104 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask options are provided for custom applications.

* Latch Enable can be edge triggered or level sensitive.
* Latch Enable can be active high or active low.
* Any frequency can be in any decoding position.
* CLK 1 and CLK 2 can be included in decoding table.
* CLK2 can control selection of either CLK 1 or the internal frequencies.

FEATURE	ST49C104 14-pin	ST49C104 8-pin	ST49C103 8-pin
8 output frequencies	X	X	
4 output frequencies			X
Programmable LEN pin	X	X	X
Clock input only		X	
Crystal or clock input	X		X
CLK1, CLK2 available for output mux	X		

Address latch (LEN)	State
ST49C104-1	Transparent for LEN high
ST49C104-2	Transparent for LEN low
ST49C104-3	Transparent for LEN low

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load. DCLK=80MHz
R_{IN}	Input pull-up resistance	15	20	25	KΩ	

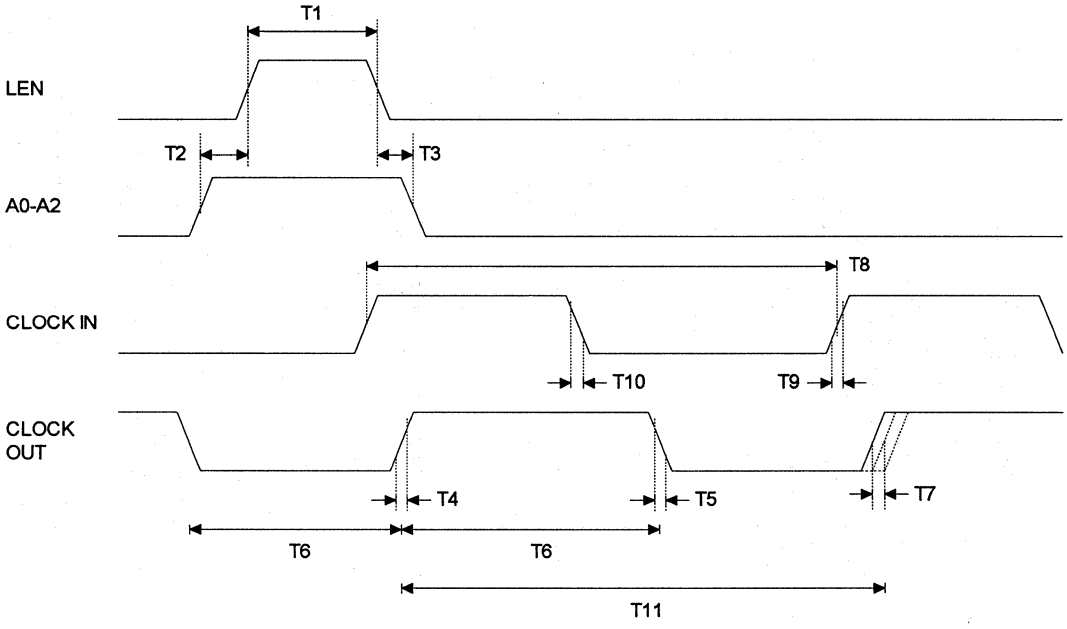
ST49C103/104

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1	1.5	ns	0.8V - 2.0V
T_5	Fall time		1	1.5	ns	2.0V - 0.8V
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

TIMING DIAGRAM



ST49C103/104

A2	A1	A0	ST49C104-1 NOMINAL	ST49C104-1 ACTUAL	ST49C104-2 NOMINAL	ST49C104-2 ACTUAL	ST49C104-3 NOMINAL	ST49C104-3 ACTUAL	ST49C104-5* NOMINAL	ST49C104-5* ACTUAL	ST49C103** NORMAL	ST49C103** ACTUAL
0	0	0	Xtal	Xtal	25.175	25.280	50.350	50.560	39.000	39.0000	32.000	32.00
0	0	1	16.257	16.331	28.322	28.412	56.664	56.824	25.000	25.000	40.00	40.00
0	1	0	Clk2	Clk2	32.514	32.663	65.028	65.326	30.750	30.750	50.00	50.00
0	1	1	32.514	32.663	36.000	35.795	72.000	71.590	26.250	26.250	1.00	1.00
1	0	0	25.175	25.056	40.000	39.822	80.000	79.640	32.000	32.000	N/A	
1	0	1	28.322	28.412	44.900	44.744	89.800	89.488	25.250	25.250	N/A	
1	1	0	24.000	23.938	50.000	50.113	75.000	75.169	31.250	31.250	N/A	
1	1	1	40.000	39.822	65.000	65.326	108.00	108.280	37.500	37.500	N/A	

A2	A1	A0	ST49C104-6** NOMINAL	ST49C104-6** ACTUAL
0	0	0	25.500	25.500
0	0	1	16.500	16.500
0	1	0	20.750	20.750
0	1	1	22.500	22.500
1	0	0	24.500	24.500
1	0	1	19.500	19.500
1	1	0	15.000	15.000
1	1	1	14.000	14.000

Input clock frequency = 14.318 MHz
* Input clock frequency = 16.0 MHz
** Input clock frequency = 8.0 MHz

STARTECH

ST49C106

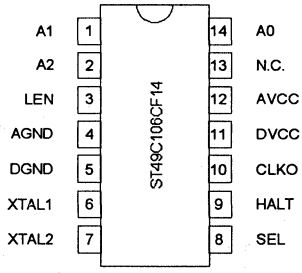
Printed February 23, 1994

PREPROGRAMMED FREQUENCY GENERATOR

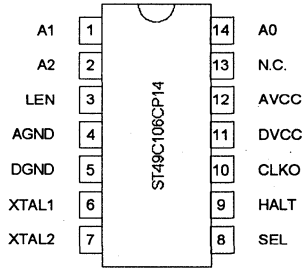
DESCRIPTION

The ST49C106 is a mask programmable monolithic analog CMOS device designed to generate up to 8 single frequency outputs from a single input clock. The ST49C106 is designed in a 1.2μ process to achieve 130 MHz speed for high end frequencies.
The ST49C106 is designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C106 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The ST49C106 contains de-glitch circuit so that full clock cycles are provided whenever the HALT pin stops or starts the output clock.

SOIC Package



Plastic-DIP package



FEATURES

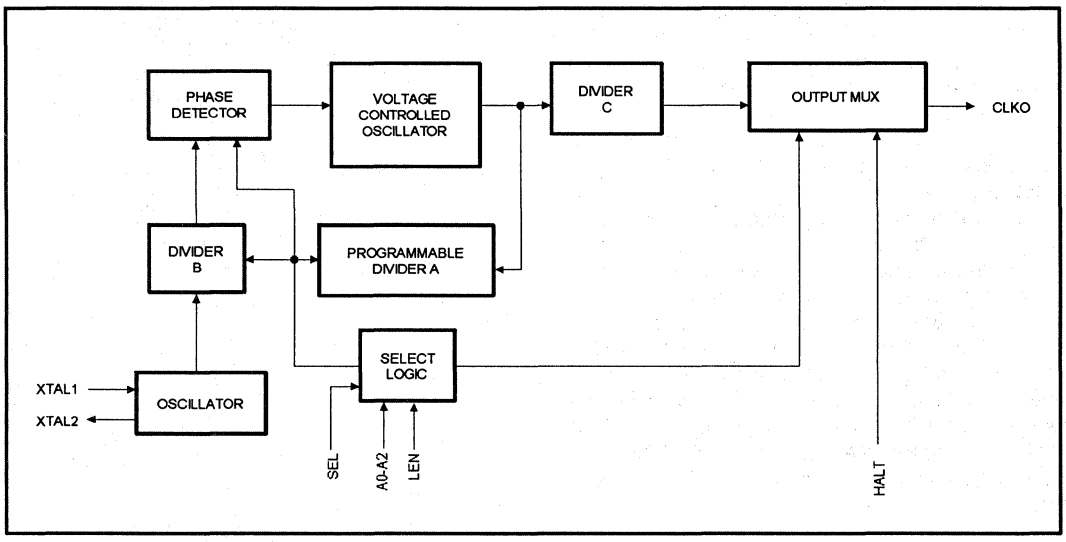
- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9106-14
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 14 pin DIP or SOIC package.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C106CP14	Plastic-DIP	0 ° C to +70° C
ST49C106CF14	SOIC	0° C to +70° C

ST49C106

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
LEN	3*	I	Address latch enable input. To latch selected programmed clock output.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
XTAL1	6	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	O	Crystal output.
SEL	8	I	Clock level select / CLK1. When HALT is asserted, SEL selects whether the clock is high or low. This level must be selected before the clock is halted. SEL pin can be used as an xternal clock input when HALT is active.
HALT	9	I	Start / Stop output clock.
CLKO	10	O	Programmed output clock.
DVCC	11	I	Digital supply voltage. Single +5 volts.
AVCC	12	I	Analog supply voltage. Single +5 volts.
A0	14	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

ST49C106

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C106 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C106 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B.C)

where A=1,2,3,.....127
B=8, 16, 32 ,64
C=1,2,4,8

For proper output frequency, the ST49C106 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load. DCLK=80MHz
R_{IN}	Input pull-up resistance	15	20	25	KΩ	

AC ELECTRICAL CHARACTERISTICS

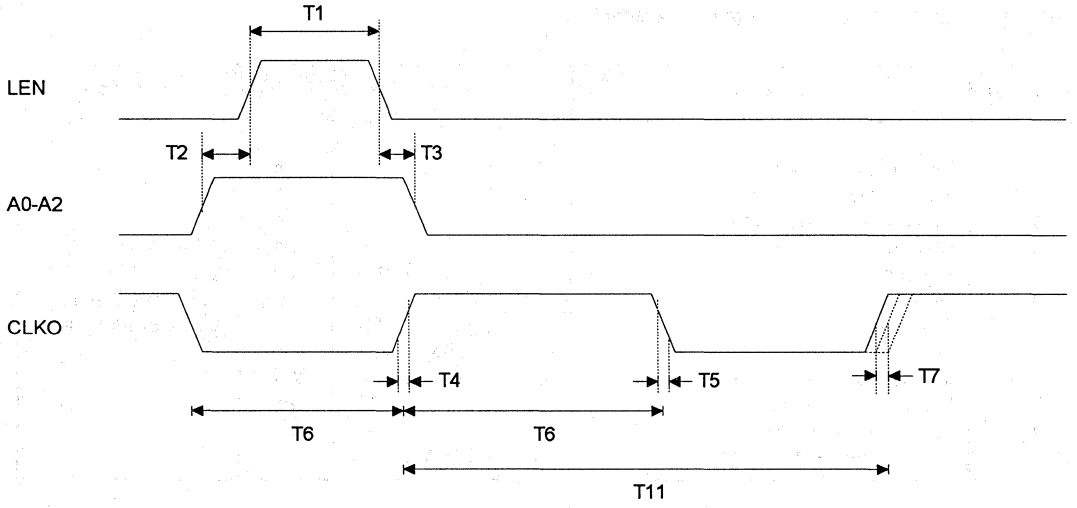
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

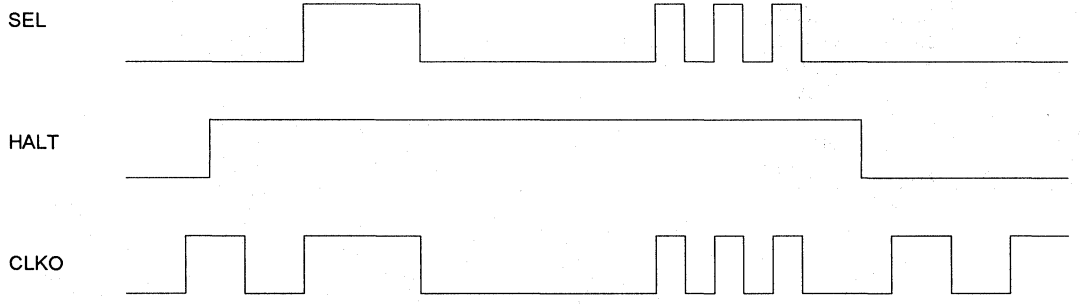
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1	1.5	ns	0.8V - 2.0V
T_5	Fall time		1	1.5	ns	2.0V - 0.8V
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

A2	A1	A0	ST49C106-5* NOMINAL	ACTUAL
0	0	0	39.000	39.000
0	0	1	25.000	25.000
0	1	0	30.750	30.750
0	1	1	26.250	26.250
1	0	0	32.000	32.000
1	0	1	25.250	25.250
1	1	0	31.250	31.250
1	1	1	37.500	37.500

ST49C106

TIMING DIAGRAM





STARTECH

ST49C107

Printed February 23, 1994

PREPROGRAMMED CPU MOTHER BOARD FREQUENCY GENERATOR

DESCRIPTION

The ST49C107 is a mask programmable monolithic analog CMOS device designed to generate two similtaneous clock. One clock, the BCLK (buffered reference clock), is a fixed output frequency. The other clock, CLOCK, 1X-CLOCK, and 2X-CLOCK can vary from 2 to 100MHz, with up to 16 single selectable preprogrammed frequencies stored in internal ROM. The ST49C107 is designed to replace existing CPU mother board clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via four address lines (two address lines for ST49C107-05).

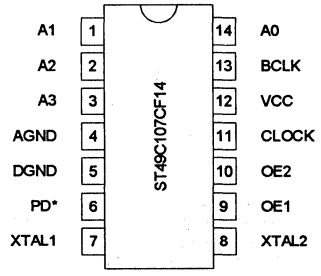
FEATURES

- Provides reference clock and synthesized clock
- 5 to 40MHz input reference frequency
- Pin-to-pin compatible to Avasem AV9107
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- Up to 16 frequencies stored internally
- 8/14 pin DIP or SOIC package.

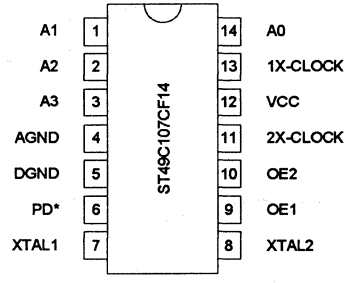
ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C107CP8	Plastic-DIP	0 ° C to +70° C
ST49C107CF8	SOIC	0° C to +70° C
ST49C107CP14	Plastic-DIP	0 ° C to +70° C
ST49C107CF14	SOIC	0° C to +70° C

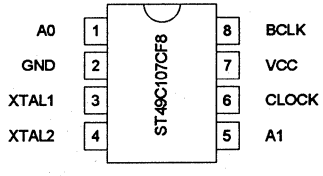
SOIC Package



ST49C107CF-03



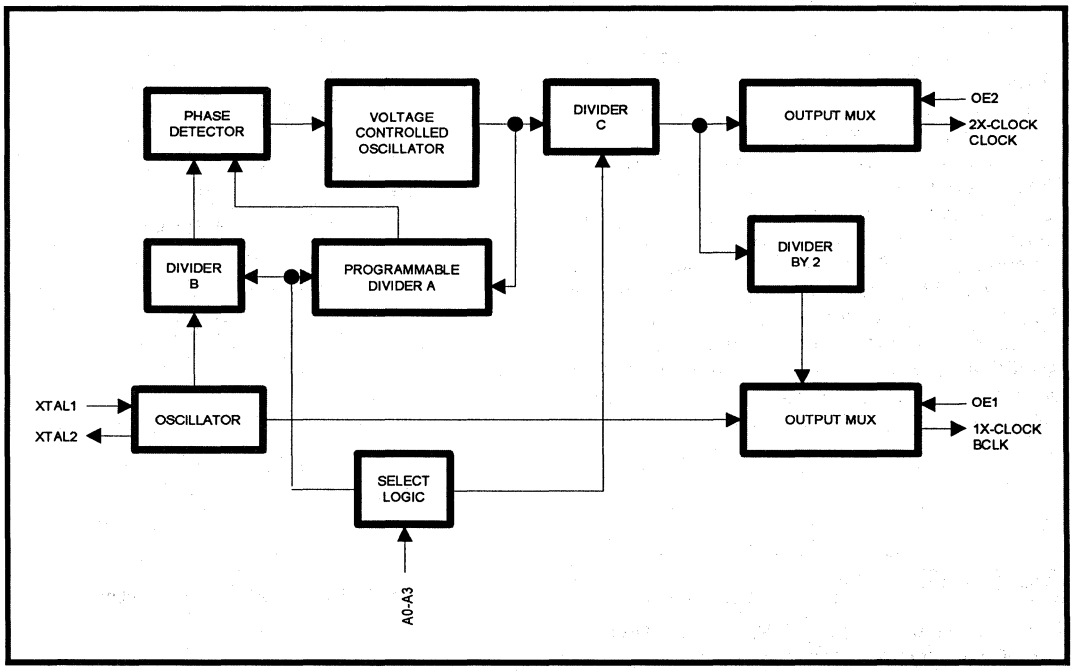
ST49C107CF-04



ST49C107CF-05

ST49C107

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C107-03 package)

Symbol	Pin	Signal Type	Pin Description
A1	1*	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
A3	3*	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6*	I	Power-Down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or EXternal Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9*	I	Buffered clock Output Enable (Active high). BCLK output is three stated when this pin is low.
OE2	10*	I	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
CLOCK	11	O	Programmed output clock.
VCC	12	I	Positive supply voltage. Single +5 volts.
BCLK	13	O	Buffered crystal clock output.
A0	14*	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

ST49C107

SYMBOL DESCRIPTION (ST49C107-04 package)

Symbol	Pin	Signal Type	Pin Description
A1	1*	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
A3	3*	I	Frequency select address input 4.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
PD	6*	I	Power-Down (Active low). Shuts off chip when low.
XTAL1	7	I	Crystal or EXternal Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O	Crystal output.
OE1	9*	I	1X-CLOCK Output Enable (Active high). 1X-CLOCK output is three stated when this pin is low.
OE2	10*	I	2X-CLOCK Output Enable (Active high). 2X-CLOCK output is three stated when this pin is low.
2X-CLOCK	11	O	Programmed output clock.
VCC	12	I	Positive supply voltage. Single +5 volts.
1X-CLOCK	13	O	2X-CLOCK Divide-by-two output.
A0	14*	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

SYMBOL DESCRIPTION (ST49C107-05 package)

Symbol	Pin	Signal Type	Pin Description
A0	1	I	Frequency select address input 1.
A1	5	I	Frequency select address input 2.
GND	2	O	Supply ground.
XTAL1	3	I	Crystal or EXternal Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLOCK	6	O	Programmed output clock.
VCC	7	I	Positive supply voltage. Single +5 volts.
BCLK	8	O	Buffered crystal clock output.

FREQUENCY TRANSITIONS

The ST49C107 is designed to provide smooth, glitch-free frequency transitions on the CLOCK, 1XCLK and 2XCLK clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C107 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C107 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B.C)

where A=5, 6, 7,.....128
B=5, 6, 7,.....128
C=1,2

For proper output frequency, the ST49C107 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

ST49C107

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-10	µA	Exc. crystal input
I_{IH}	Input high current			1	µA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load. CLOCK=80MHz
I_{SB}	Standby current		25		µA	No load.
R_{IN}	Input pull-up resistance	500	900	1300	KΩ	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	1X, 2X-CLOCK rise time		1	1.5	ns	0.8V - 2.0V
T_2	1X, 2X-CLOCK fall time		1	1.5	ns	2.0V - 0.8V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_3	Jitter		±85	±100	ps	
T	Input frequency	2		32	MHz	
T_7	Buffered clock rise time			20	ns	
T_8	Buffered clock fall time			20	ns	
T_6	1X, 2X-CLOCK frequency change		0.005		%	

CLOCK OUTPUT TABLE FOR ST49C107-03 (using 14.318 MHz input. All frequencies in MHz).

A3	A2	A1	A0	CLOCK
0	0	0	0	16.00
0	0	0	1	40.01
0	0	1	0	50.11
0	0	1	1	80.01
0	1	0	0	66.58
0	1	0	1	100.23
0	1	1	0	8.02
0	1	1	1	4.01
1	0	0	0	8.02
1	0	0	1	20.00
1	0	1	0	25.06
1	0	1	1	40.01
1	1	0	0	33.29
1	1	0	1	50.11
1	1	1	0	4.01
1	1	1	1	2.05

CLOCK OUTPUT TABLE FOR ST49C107-04 (using 14.318 MHz input. All frequencies in MHz).

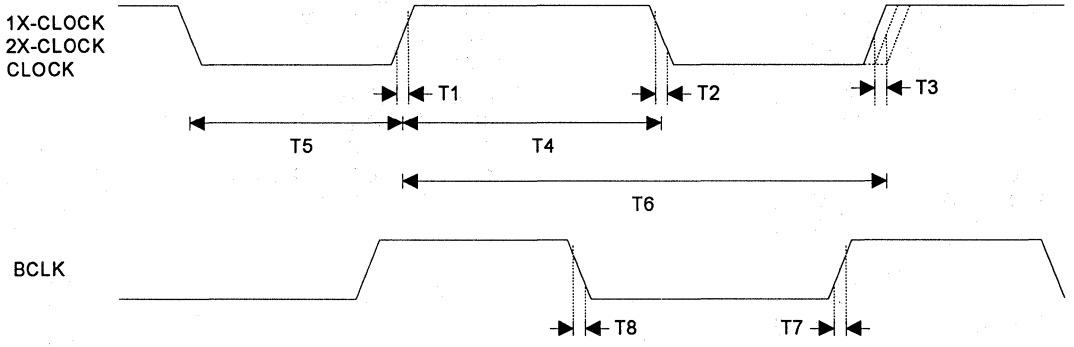
A3	A2	A1	A0	2X-CLOCK	CLOCK
0	0	0	0	80.02	40.01
0	0	0	1	66.62	33.31
0	0	1	0	50.11	25.06
0	0	1	1	40.01	20.00
0	1	0	0	100.23	50.11
0	1	0	1	33.31	16.66
0	1	1	0	32.01	16.00
0	1	1	1	25.06	12.47
1	0	0	0	64.02	32.01
1	0	0	1	2X-Input	1X-Input
1	0	1	0	3X-Input	1.5X-Input
1	0	1	1	8X-Input	4X-Input
1	1	0	0	0.5X-Input	0.25X-Input
1	1	0	1	0.25X-Input	0.125X-Input
1	1	1	0	120.00	60.00
1	1	1	1	129.96	64.98

CLOCK OUTPUT TABLE FOR ST49C107-05 (using 14.318 MHz input. All frequencies in MHz).

A1	A0	CLOCK
0	0	40.01
0	1	50.11
1	0	66.61
1	1	80.01

ST49C107

TIMING DIAGRAM



STARTECH

EVALUATION KIT AVAILABLE

ST49C155

Printed February 23, 1994

PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

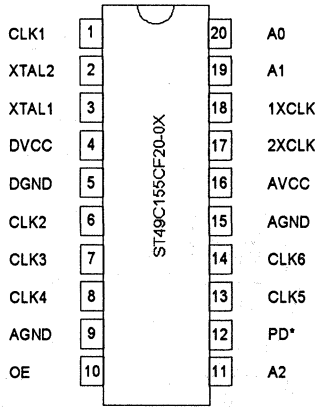
GENERAL DESCRIPTION

The ST49C155 is a monolithic analog CMOS device designed to generate eight simultaneous clock outputs for mother board applications. It is designed in a 1.2μ process to achieve 130 MHz operation with low clock jitter.

The ST49C155 may be used to replace existing BUS and I/O clocks generated from individual oscillators so that board space and number of oscillators are reduced. The high speed analog CMOS phase locked loops use the 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).

The ST49C155 is metal mask programmable to provide any custom set of CPUCLK frequencies. The programmed clock outputs are selectable via four address lines for 1XCLK / 2XCLK outputs.

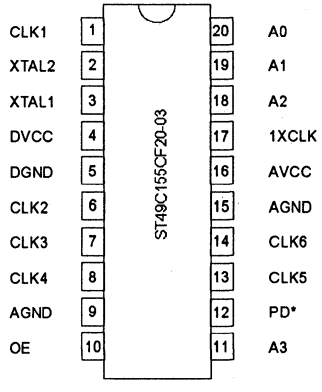
SOIC Package



FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to AV9155
- Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Skew controlled 2X and 1X clocks
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

SOIC Package

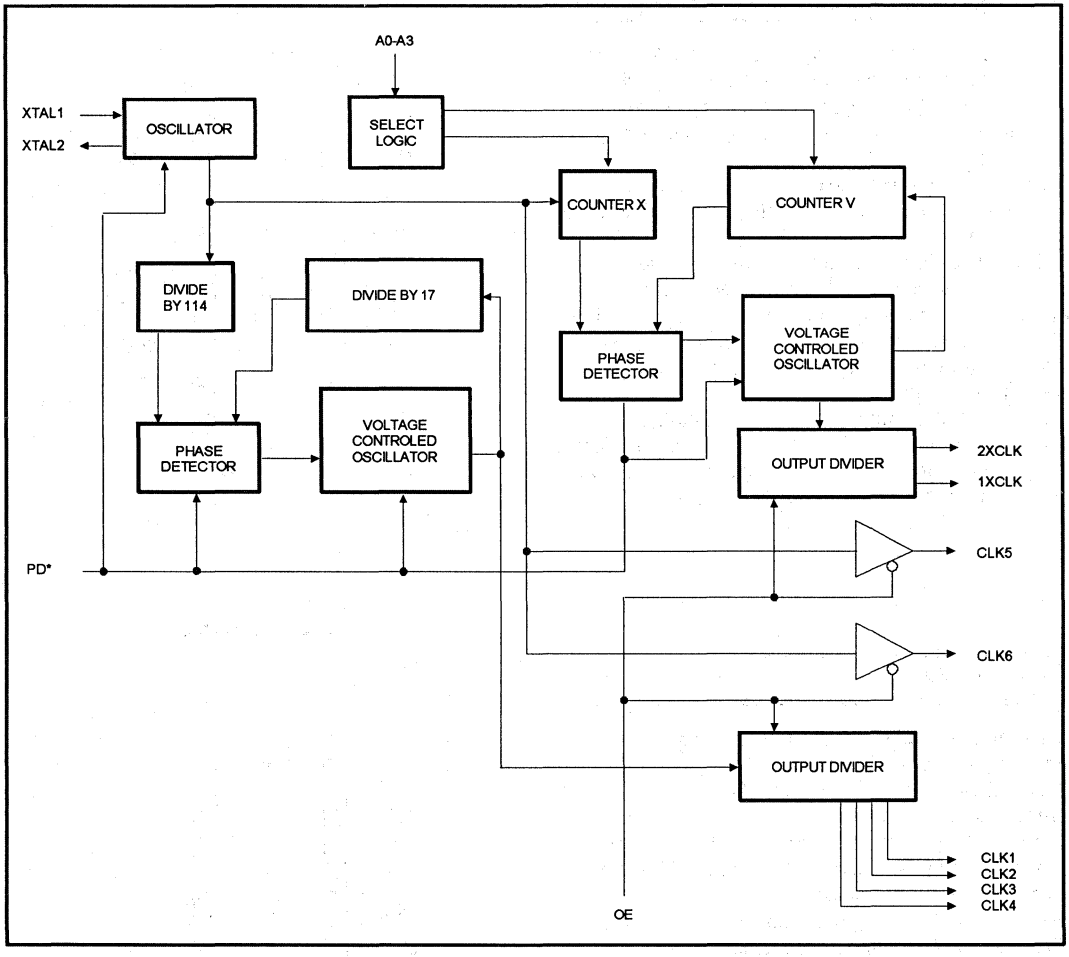


ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C155CP20-xx	Plastic-DIP	0° C to +70° C
ST49C155CF20-xx	SOIC	0° C to +70° C
ST49C155CJ20-xx	PLCC	0° C to +70° C

ST49C155

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C155-01/ -02)

Symbol	Pin	Signal Type	Pin Description
CLK1	1	O	1.8432 MHz clock output.
XTAL2	2	O	Crystal output.
XTAL1	3	I	Crystal or External clock input.
DVCC	4	I	Digital supply voltage. Single +5 volts.
DGND	5	O	Digital signal ground.
CLK2	6	O	16 MHz (ST49C155-01) or 32 MHz (ST49C155-02) clock output.
CLK3	7	O	24 MHz floppy disk clock output.
CLK4	8	O	12 MHz keyboard clock output.
AGND	9	O	Analog ground.
OE	10*	O	Output Enable (active high). Low on this pin sets all the outputs to three state mode.
A2	11	I	CPU clock frequency select address 2.
PD*	12*	I	Power down (active low). Shuts off entire chip when low.
CLK5	13	O	14.318 MHz reference clock output.
CLK6	14	O	14.318 MHz reference clock output.
AGND	15	O	Analog ground.
AVCC	16	I	Analog supply voltage. Single +5 volts.
2XCLK	17	I	2X CPU clock output.
1XCLK	18	I	1X CPU clock output.
A1	19	I	CPU clock frequency select address 1.
A0	20	I	CPU clock frequency select address 0.

*Have internal pull-up resistor on inputs

ST49C155

SYMBOL DESCRIPTION (ST49C155-03)

Symbol	Pin	Signal Type	Pin Description
CLK1	1	O	6 MHz clock output.
XTAL2	2	O	Crystal output.
XTAL1	3	I	Crystal or External clock input.
DVCC	4	I	Digital supply voltage. Single +5 volts.
DGND	5	O	Digital signal ground.
CLK2	6	O	24 MHz floppy disk clock output.
CLK3	7	O	16 MHz bus clock output.
CLK4	8	O	8 MHz keyboard clock output.
AGND	9	O	Analog ground.
OE	10*	O	Output Enable (active high). Low on this pin sets all the outputs to three state mode.
A3	11	I	CPU clock frequency select address 3.
PD*	12*	I	Power down (active low). Shuts off entire chip when low.
CLK5	13	O	14.318 MHz reference clock output.
CLK6	14	O	14.318 MHz reference clock output.
AGND	15	O	Analog signal ground.
AVCC	16	I	Analog supply voltage. Single +5 volts.
1XCLK	17	I	CPU clock output.
A2	18	I	CPU clock frequency select address 2.
A1	19	I	CPU clock frequency select address 1.
A0	20	I	CPU clock frequency select address 0.

*Have internal pull-up resistor on inputs

CPU CLOCK TABLE FOR ST49C155-01, -02 (using 14.318 MHz input. All frequencies in MHz).

A2	A1	A0	2XCLK	1XCLK
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	100	50

CPU CLOCK TABLE FOR ST49C155-03(using 14.318 MHz input. All frequencies in MHz).

A3	A2	A1	A0	1XCLK
0	0	0	0	16
0	0	0	1	40
0	0	1	0	50
0	0	1	1	80
0	1	0	0	66.66
0	1	0	1	100
0	1	1	0	8
0	1	1	1	4
1	0	0	0	8
1	0	0	1	20
1	0	1	0	25
1	0	1	1	40
1	1	0	0	33.33
1	1	0	1	50
1	1	1	0	4
1	1	1	1	2

CPU CLOCK TABLE FOR ST49C155-23(using 14.318 MHz input. All frequencies in MHz).

A2	A1	A0	2XCLK	1XCLK
0	0	0	75	37.5
0	0	1	32	16
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80	40
1	1	1	52	26

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-01 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	16	24	12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-02 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	32	24	12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-03 (MHz)

CLK1	CLK2	CLK3	CLK4
6	24	16	8

ST49C155

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-23 (MHz)

CLK1	CLK2	CLK3	CLK4
1.843	16	24	12

ACTUAL OUTPUT FREQUENCIES

CPU CLOCK TABLE FOR ST49C155-01, -02 (using 14.318 MHz input. All frequencies in MHz).

A2	A1	A0	2XCLK	1XCLK
0	0	0	7.5	3.75
0	0	1	15.51	7.76
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.41
1	1	0	80.18	40.09
1	1	1	100.23	50.11

CPU CLOCK TABLE FOR ST49C155-03(using 14.318 MHz input. All frequencies in MHz).

A3	A2	A1	A0	1XCLK
0	0	0	0	15.51
0	0	0	1	40.09
0	0	1	0	50.11
0	0	1	1	80.18
0	1	0	0	66.82
0	1	0	1	100.23
0	1	1	0	7.58
0	1	1	1	4.30
1	0	0	0	7.76
1	0	0	1	20.05
1	0	1	0	25.06
1	0	1	1	40.09
1	1	0	0	33.41
1	1	0	1	50.11
1	1	1	0	3.79
1	1	1	1	2.15

CPU CLOCK TABLE FOR ST49C155-23(using 14.318 MHz input. All frequencies in MHz).

A2	A1	A0	2XCLK	1XCLK
0	0	0	75.170	37.585
0	0	1	31.940	15.970
0	1	0	60.136	30.068
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181	40.091
1	1	1	51.903	25.952

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-01 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	16	23.71	11.86

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-02 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	32.01	24	12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-03 (MHz)

CLK1	CLK2	CLK3	CLK4
6	24	16	8

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-1	mA	Except pins 2, 10, 12
I_{IH}	Input high current			1	mA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load.
R_{IN}	Internal pull-up resistance		680		KΩ	Pins 10,12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-23 (MHz)

CLK1	CLK2	CLK3	CLK4
1.843	16	24	12

FREQUENCY TRANSITIONS

The ST49C155 is designed to provide smooth, glitch-free frequency transitions on the 1XCLK and 2XCLK clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

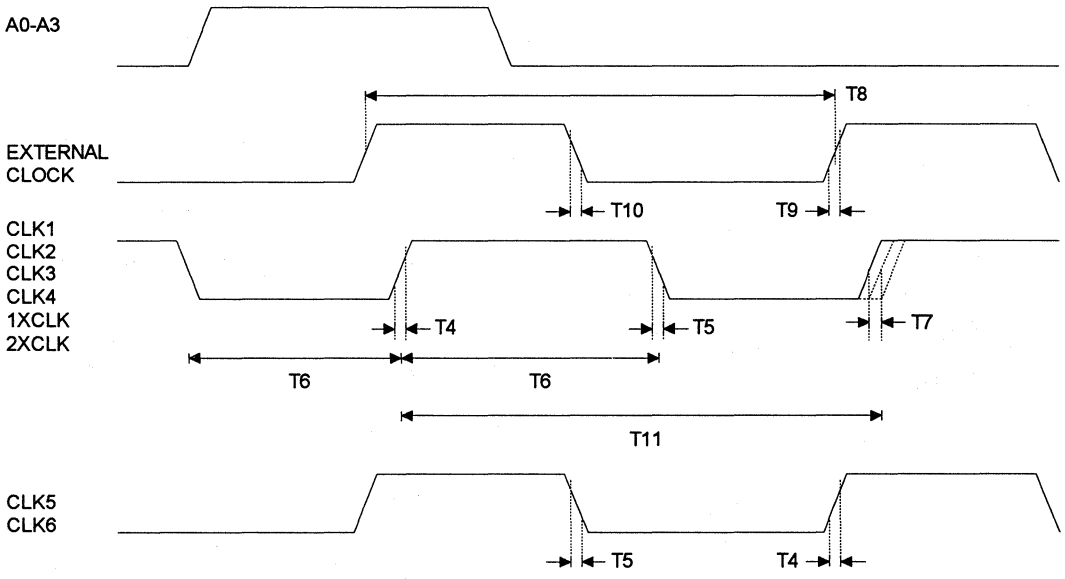
ST49C155

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_4	Rise time		1	1.5	ns	0.8V - 2.0V
T_5	Fall time		1	1.5	ns	2.0V - 0.8V
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	40	48/52	55	%	Vcc/2 switch point
T_7	Jitter		±85	±100	ps	
T_8	Input frequency		14.318		MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	

TIMING DIAGRAM



ST49C155

STARTECH

EVALUATION KIT AVAILABLE

ST49C214

Printed February 23, 1994

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

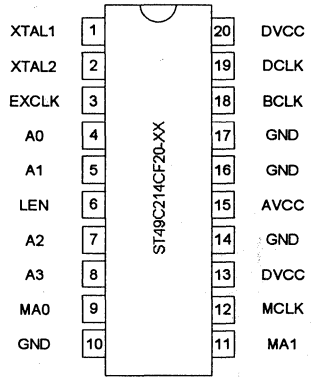
GENERAL DESCRIPTION

The ST49C214 is a monolithic analog CMOS device designed to generate dual frequency outputs from sixteen possible combinations for video Dot clock frequencies and four memory clock frequencies for high performance video display systems. The ST49C214 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2μ process to achieve 130 MHz speed for high end frequencies.

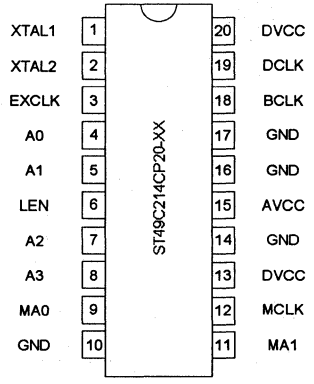
The ST49C214 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C214 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device) or external crystal connected between XTAL1 and XTAL2.

The ST49C214 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and two address lines for memory clock selection.

SOIC Package



Plastic-DIP Package



FEATURES

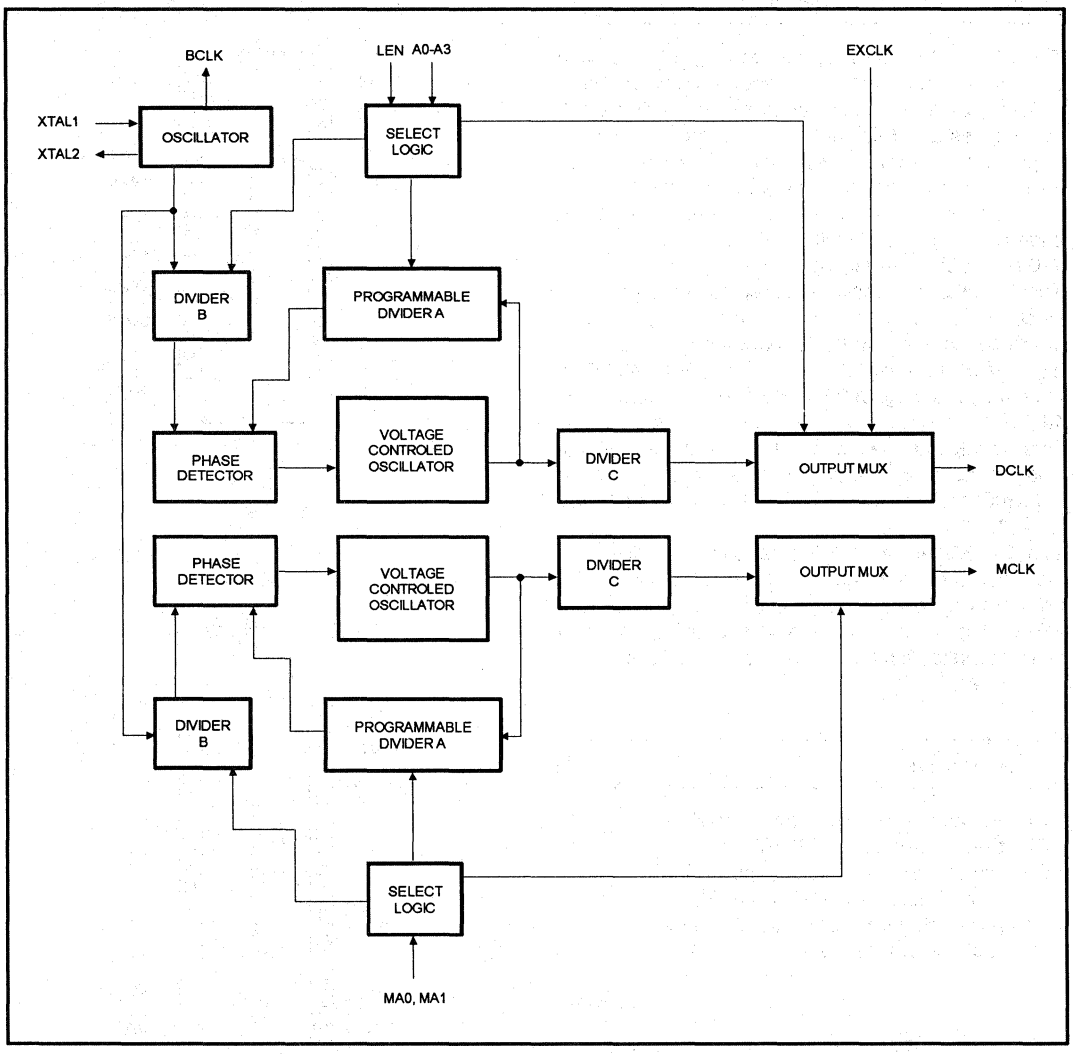
- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS2494
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C214CP20-xx	Plastic-DIP	0° C to +70° C
ST49C214CF20-xx	SOIC	0° C to +70° C
ST49C214CJ20-xx	PLCC	0° C to +70° C

ST49C214

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL1	1	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	2	O	Crystal output.
EXCLK	3*	I	External clock input.
A0	4*	I	Dot clock Frequency select address 1.
A1	5*	I	Dot clock Frequency select address 2.
LEN	6*	I	Address latch enable input (active high). To latch selected programmed clock output.
A2	7*	I	Dot clock Frequency select address 3.
A3	8*	I	Dot clock Frequency select address 4.
MA0	9*	I	Memory clock Frequency select address 1.
GND	10	O	Digital and Analog ground.
MA1	11*	I	Memory clock Frequency select address 2.
MCLK	12	O	Programmed memory clock output frequency.
DVCC	13	I	Digital supply voltage. Single +5 volts.
GND	14	O	Digital and Analog ground.
AVCC	15	I	Analog supply voltage. Single +5 volts.
GND	16	O	Digital and Analog ground.
GND	17	O	Digital and Analog ground.
BCLK	18*	O	Buffered crystal clock output frequency.
DCLK	19	O	Programmed video clock output frequency.
DVCC	20	I	Digital supply voltage. Single +5 volts.

* Have internal pull-up resistor on inputs.

ST49C214

FREQUENCY SELECT CALCULATION

The ST49C214 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.
The accuracy of the frequencies produced by the ST49C214 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

XCLK = (Reference clock) X (A/B.C)

where A=1,2,3,.....127,
B=1,2,3,.....127, AND
C=1,2,4

For proper output frequency, the ST49C214 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask option are provided for custom applications.

*Any frequency can be in any decoding position.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load. DCLK=80MHz, MCLK=40MHz
R_{IN}	Internal pull-up resistance	15	20	25	KΩ	

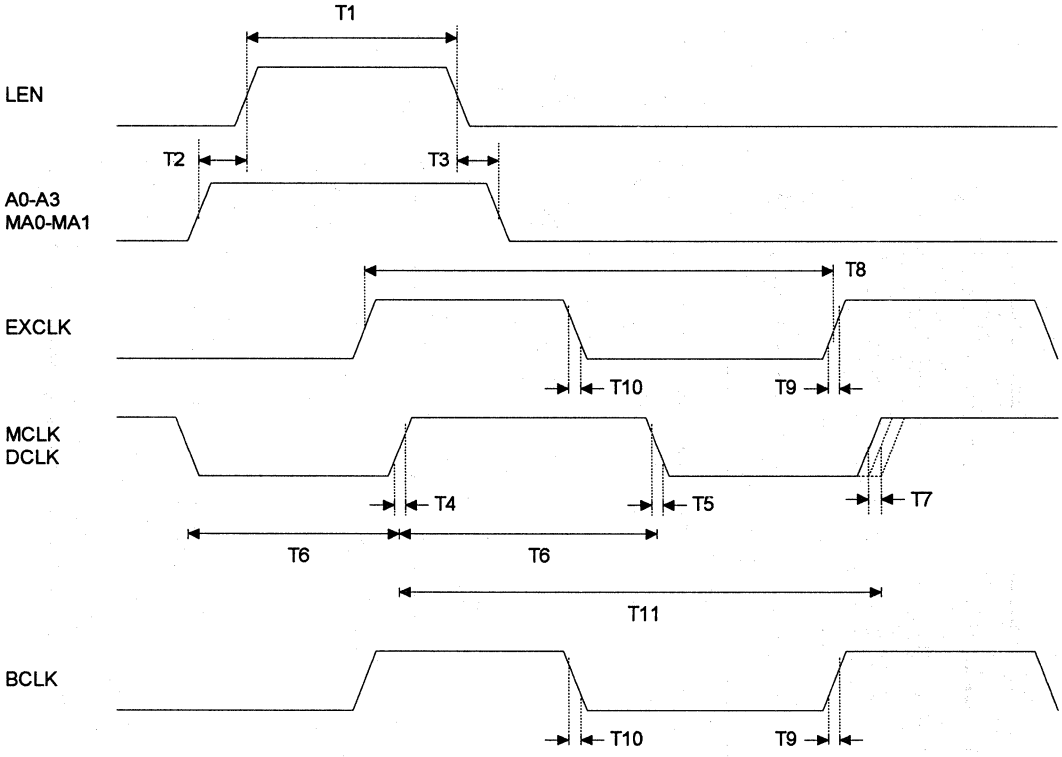
ST49C214

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1	1.5	ns	0.8V - 2.0V
T_5	Fall time		1	1.5	ns	2.0V - 0.8V
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

TIMING DIAGRAM



ST49C214

ST49C214- Frequency generator programming information

2. Please fill in the nominal frequencies required.

3. Crystal or input clock frequency _____

A3	A2	A1	A0	Nominal DCLKO	Actual DCLKO	
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			
		MA1	MA0	Nominal MCLKO	Actual MCLKO	
		0	0			
		0	1			
		1	0			
		1	1			

Video clock address (Hex)	ST49C214-1 Frequency (MHz)	ST49C214-2 Frequency (MHz)	ST49C214-3 Frequency (MHz)	ST49C214-4 Frequency (MHz)	ST49C214-5 Frequency (MHz)
0	XTAL	30.000	25.175	20.000	50.350
1	65.028	77.250	28.325	24.000	56.644
2	EXCLK	EXCLK	85.000	32.000	65.000
3	36.000	80.000	44.900	40.000	72.000
4	25.175	31.500	40.000	50.000	80.000
5	28.322	36.000	48.000	66.667	89.800
6	24.000	75.000	50.000	80.000	63.000
7	40.000	50.000	81.150	100.000	75.000
8	44.900	40.000	25.175	54.000	25.175
9	50.350	50.000	28.325	70.000	28.322
A	16.257	32.000	37.500	90.000	31.500
B	32.514	44.900	44.900	110.000	36.000
C	56.644	25.175	40.000	25.000	40.000
D	20.000	28.322	32.500	33.333	44.900
E	41.539	65.000	50.000	40.000	50.000
F	80.000	36.000	65.000	50.000	65.000
Memory clock address (Hex)	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**
0	32.900	36.000	36.000	16.000	40.000
1	35.600	44.347	40.000	24.000	41.612
2	43.900	37.500	45.000	50.000	44.744
3	49.100	44.773	50.000	66.667	50.000

Compatible with Video Controller	**ICS-236** GD6410	**ICS-242** WD90C30	**ICS-231** ET4000	**ICS-244**	**ICS-237** ET4000

ST49C214

Video clock address (Hex)	ST49C214-6 Frequency (MHz)	ST49C214-8 Frequency (MHz)	ST49C214-9 Frequency (MHz)	ST49C214-10 Frequency (MHz)	ST49C214-16 Frequency (MHz)
0	25.175	25.175	25.175	30.250	XTAL
1	28.322	28.322	28.322	65.000	16.257
2	40.000	40.000	40.000	85.000	EXCLK
3	65.000	32.500	EXCLK	36.000	32.514
4	44.900	50.000	50.000	25.175	25.175
5	50.000	65.000	77.000	28.322	28.322
6	130.000	38.000	36.000	34.000	24.000
7	75.000	44.900	44.889	40.000	40.000
8	25.175	31.500	130.00	44.900	XTAL
9	28.322	36.000	120.00	50.350	16.257
A	EXCLK	80.000	80.000	31.500	EXCLK
B	EXCLK	63.000	31.500	32.500	36.000
C	60.000	50.000	110.00	63.000	25.175
D	80.000	100.000	65.000	72.000	28.322
E	EXCLK	76.000	75.000	75.000	24.000
F	EXCLK	110.000	72.000	80.000	40.000
Memory clock address (Hex)	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**
0	50.000	70.000	55.000	36.000	31.000
1	60.000	63.830	75.000	44.000	36.000
2	65.000	60.000	70.000	49.000	43.000
3	75.000	81.000	80.000	40.000	49.000

Compatible with	**ICS-253**		**ICS-256**	**ICS-266**	**ICS-247**
Video Controller	NCR77C22E	HT216	S3/86C911	GDS5410	GDS5320

Video clock address (Hex)	ST49C214-17 Frequency (MHz)	ST49C214-18 Frequency (MHz)	ST49C214-19 Frequency (MHz)	ST49C214-20 Frequency (MHz)	ST49C214-25* Frequency (MHz)
0	25.175	25.175	25.175	50.350	25.175
1	28.322	28.322	28.322	56.644	28.322
2	28.636	40.000	40.000	33.250	40.000
3	36.000	EXCLK	EXCLK	52.000	72.000
4	40.000	50.000	50.000	80.000	50.000
5	42.954	77.000	77.000	63.000	77.000
6	44.900	36.000	36.000	EXCLK	36.000
7	57.272	44.889	44.889	75.000	44.900
8	60.000	130.00	130.00	25.175	130.00
9	63.960	120.00	120.00	28.322	120.00
A	75.000	80.000	80.000	31.500	80.000
B	80.000	31.500	31.500	36.000	31.500
C	85.000	110.00	110.00	40.000	110.00
D	99.000	65.000	65.000	44.900	65.000
E	102.00	75.000	75.000	50.000	75.000
F	108.00	94.500	94.500	65.000	94.500
Memory clock address (Hex)	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**	**Frequency (MHz)**
0	64.000	45.000	55.000	40.000	55.000
1	40.830	38.000	75.000	33.333	65.000
2	48.000	52.000	70.000	44.000	70.000
3	60.000	50.000	80.000	50.000	80.000
4					45.000
5					40.000
6					60.000
7					50.000

Compatible with Video Controller	**ICS-240** TI/34010/20	**ICS-275** S3/801/805	**ICS-305** S3/924	**ICS-260** WEITEK W5186	**CH9294-G** S3/801/805

*= The External clock input pin has been changed to MA2 to privide four additional preprogrammed memory clock selections. When Pin-3 of the ST49C214-25 is connected to ground it is downward compatible to standard ST49C214-XX. This pin contains internal pull-up resistor.

ST49C214

STARTECH

ST49C418

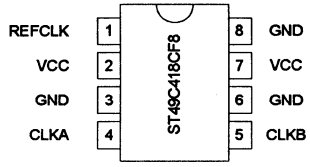
Printed February 23, 1994

PREPROGRAMMED STEREO CODEC's CLOCK SYNTHESIZER

DESCRIPTION

The ST49C418 is a mask programmable monolithic analog CMOS device, designed to replace existing dual crystals/oscillators with single frequency clock input. The ST49C418 provides high speed and low jitter clock outputs for multi-media stereo codecs.
The ST49C418 interfaces to Analog Devices's AD1848 and Crystal Semiconductor's CS4231 stereo codecs. The ST49C418 provides 16.934 and 24.576 MHz clock outputs utilizing the 14.318 MHz clock input.
ST49C418 is designed in a 1.2µ process to achieve 150 MHz speed for high end frequencies.

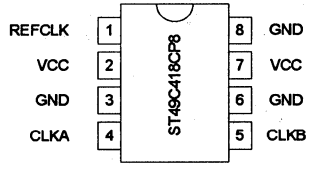
SOIC Package



FEATURES

- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package
- Programmable input/output frequencies
- TTL compatible outputs
- No external components besides de-coupling capacitors

Dip Package

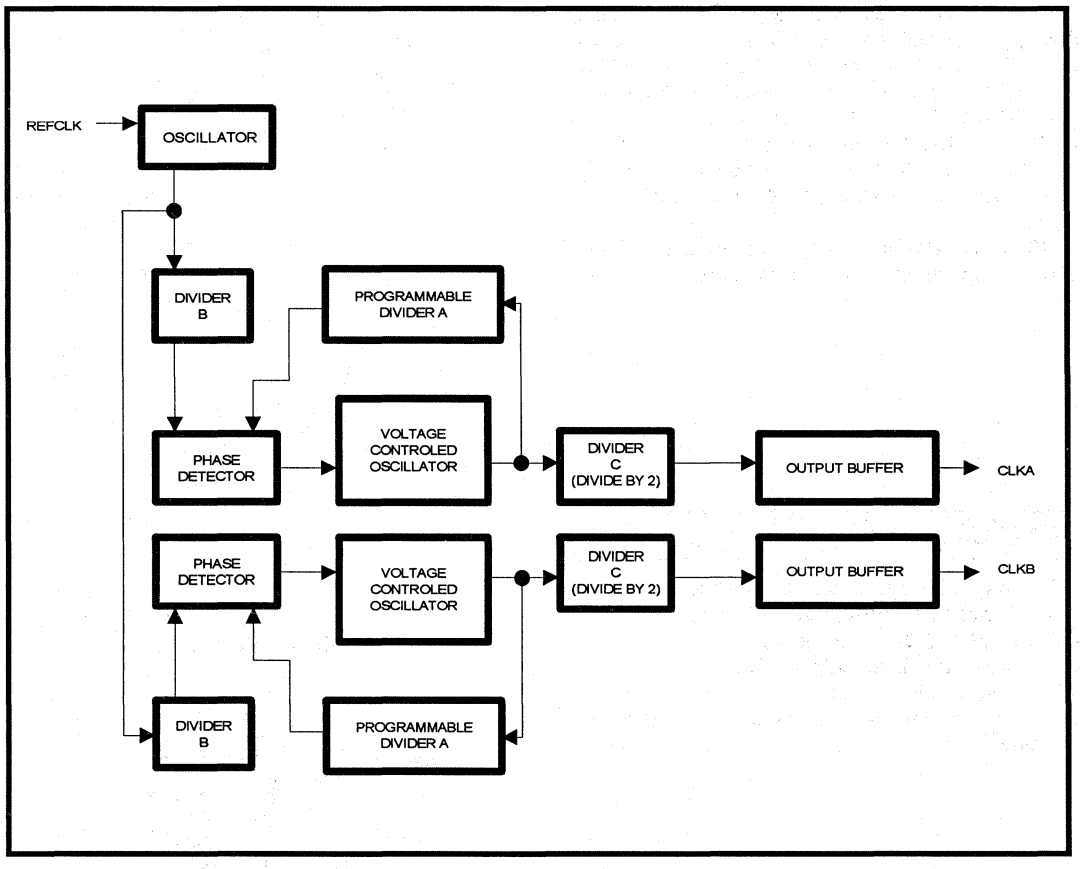


ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C418CP8	Plastic-DIP	0 ° C to +70° C
ST49C418CF8	SOIC	0° C to +70° C

ST49C418

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
REFCLK	1	I	External Reference Clock input. REFCLK is used as internal phase locked loop reference clock.
VCC	2	I	Supply voltage. Single +5 volts.
GND	3	O	Supply ground.
CLKA	4	O	Programmable output clock. Programmed for 16.9344 MHz output.
CLKB	5	O	Programmable output clock. Programmed for 24.576 MHz output.
GND	6	O	Supply ground.
VCC	7	I	Supply voltage. Single +5 volts.
GND	8	O	Supply ground.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.01 to 0.047µF capacitor to REFCLK, and keep the lead length of the capacitor to REFCLK to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C418 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C418 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B.C)

where A=5, 6, 7,.....128
B=5, 6, 7,.....128
C=2

For proper output frequency, the ST49C418 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

ST49C418

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

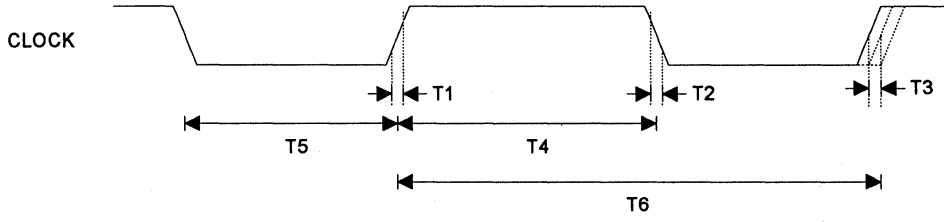
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 25 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 25 mA
I_{IH}	Input high current			1	µA	
I_{CC}	Operating current		20	25	mA	No load.

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	CLOCK rise time		1	1.5	ns	0.5V - 2.8V
T_2	CLOCK fall time		1	1.5	ns	2.8V - 0.5V
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	VCC/2 switch point
T_3	Jitter		±85	±100	ps	
T	Input frequency	5	10	40	MHz	
T_6	CLOCK frequency change		0.01		%	

TIMING DIAGRAM



ST49C418

LINE DRIVERS / RECEIVERS 2

Index

STARTECH

ST26C31

Printed February 23, 1994

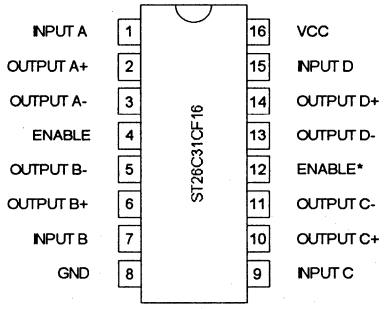
QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

DESCRIPTION

The ST26C31 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST26C31 circuit.

The ST26C31 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

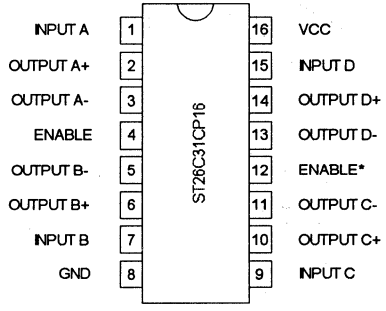
SOIC package



FEATURES

- Pin-to-pin compatible with National DS26C31C
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

Plastic-DIP package

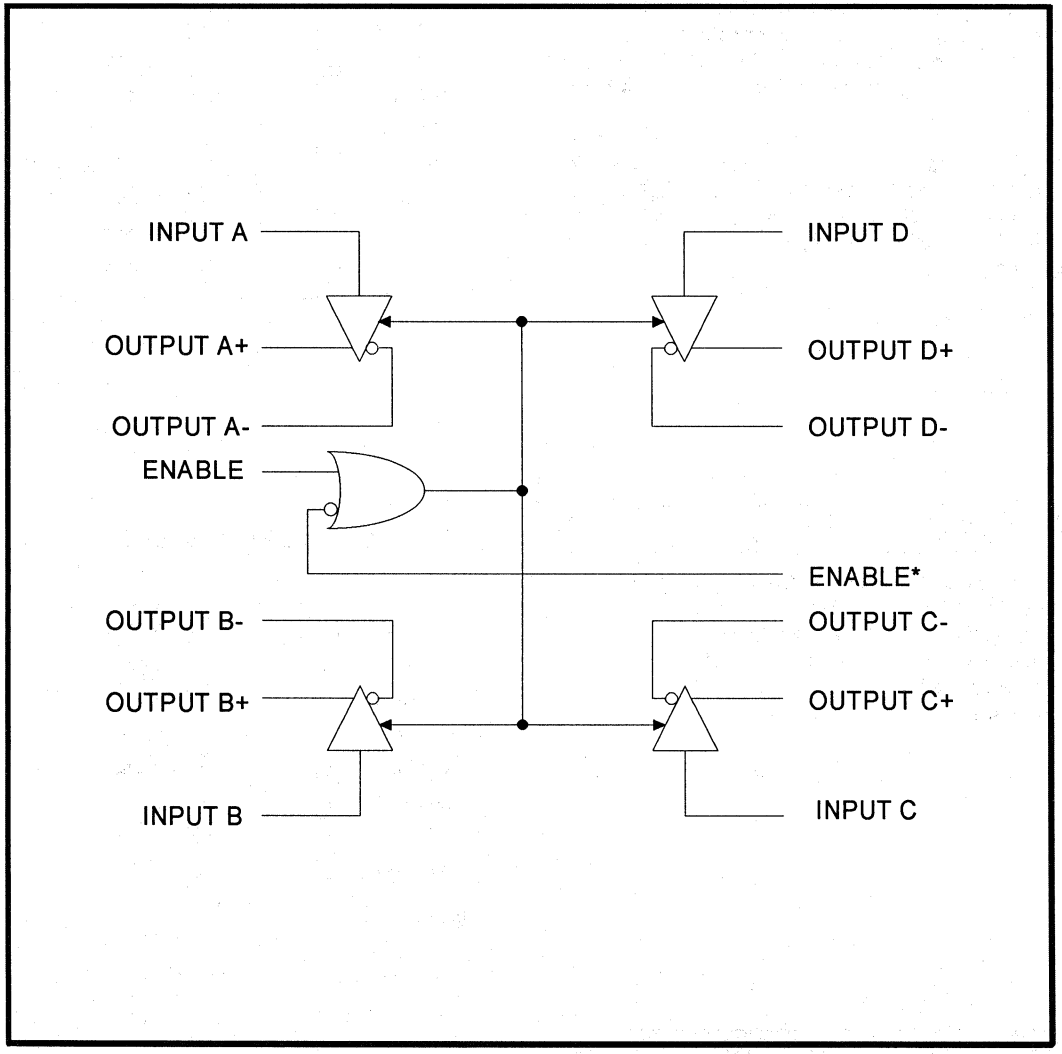


ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C31CP16	Plastic-DIP	0° C to + 70° C
ST26C31CF16	SOIC	0° C to + 70° C

ST26C31

BLOCK DIAGRAM



SYMBOL DESCRIPTION

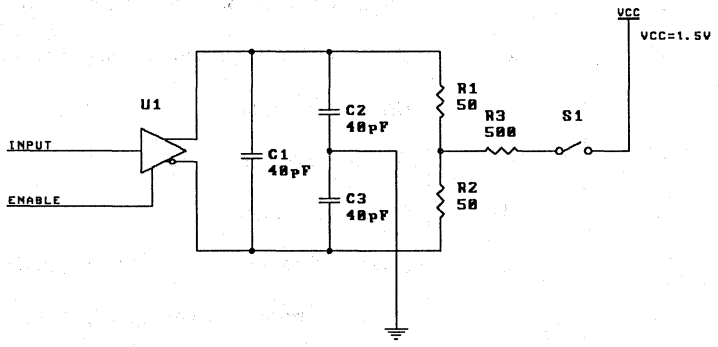
Symbol	Pin	Signal Type	Pin Description
INPUT A	1	I	Driver A input pin.
OUTPUT A+	2	O	Driver A differential non-inverting output pin.
OUTPUT A-	3	O	Driver A differential inverting output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four drivers. All four drivers are gated with two input or gate.
OUTPUT B-	5	O	Driver B differential inverting output pin.
OUTPUT B+	6	O	Driver B differential non-inverting output pin.
INPUT B	7	I	Driver B input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverting output pin.
OUTPUT C-	11	O	Driver C differential inverting output pin.
ENABLE*	12	I	Gate control (active low). See ENABLE pin description.
OUTPUT D-	13	O	Driver D differential inverting output pin.
OUTPUT D+	14	O	Driver D differential non-inverting output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

ST26C31

Functional table

Enable	Enable*	Input	Differential Non-Inverting Output	Differential Inverting Output
L	H	X	Z	Z
L	L	L	L	H
L	L	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	L	H
H	H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
*T_5	Skew			2	ns	S1 open

* Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

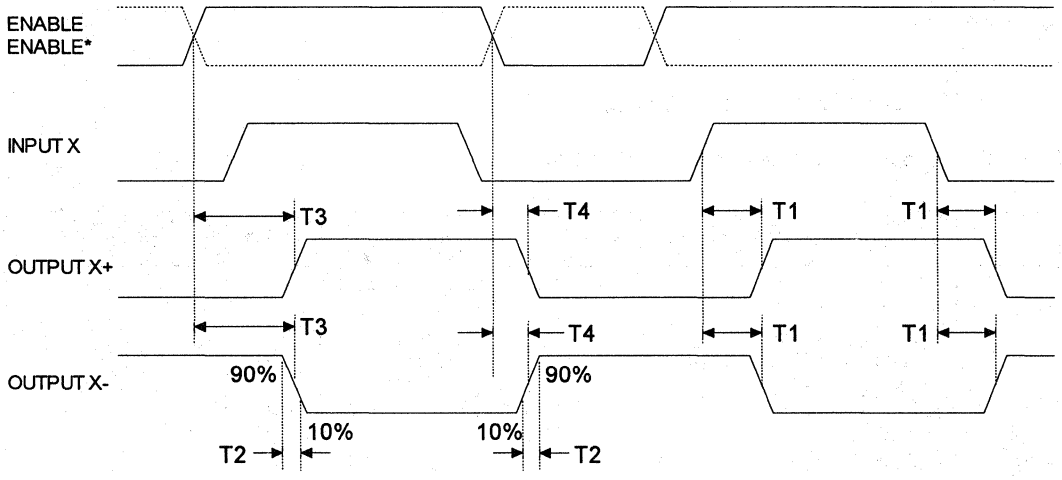
DC ELECTRICAL CHARACTERISTICS

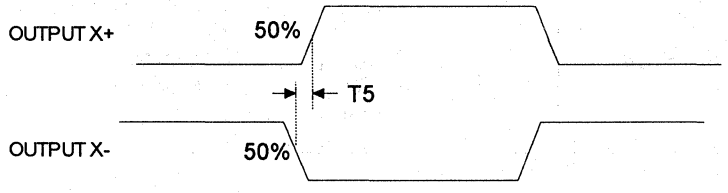
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{IH}	Input high level	2.0			V	
V_{IL}	Input low level			0.8	V	
V_{OH}	Output high level	2.5			V	
V_{OL}	Output low level			0.5	V	
V_{OS}	Differential output level	2.0			V	R_L=100Ω
V_{OC}	Common mode output voltage			3.0	V	R_L=100Ω
V_{OD}	Difference in common mode output			0.4	V	R_L=100Ω
C_{IN}	Input capacitance	7	10	15	pF	
C_{PD}	Power dissipation capacitance		100		pF	
I_{OS}	Output short current	-30		-150	mA	V_{IN}=VCC or GND
I_{OFF}	Output leakage current power off			100	µA	Vout=6V
				-100	µA	Vout=0.25V
I_{DC}	Output current			±150	mA	

ST26C31

DIFFERENTIAL LINE DRIVER TIMING





STARTECH

ST26C32

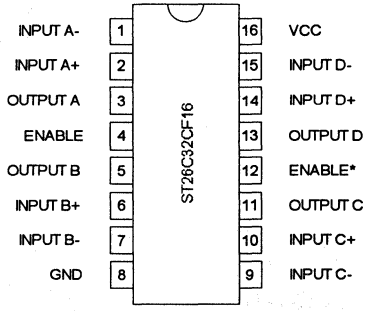
Printed February 23, 1994

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of ±7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.
The ST26C32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST26C32 is suitable for low power 5V operation.

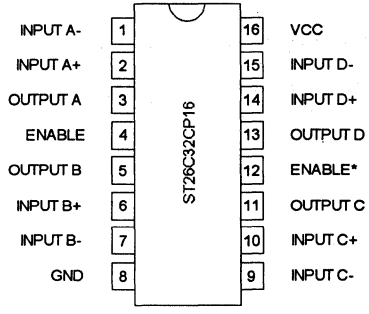
SOIC package



FEATURES

- Pin-to-pin compatible with National DS26C32C
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

Plastic-DIP package

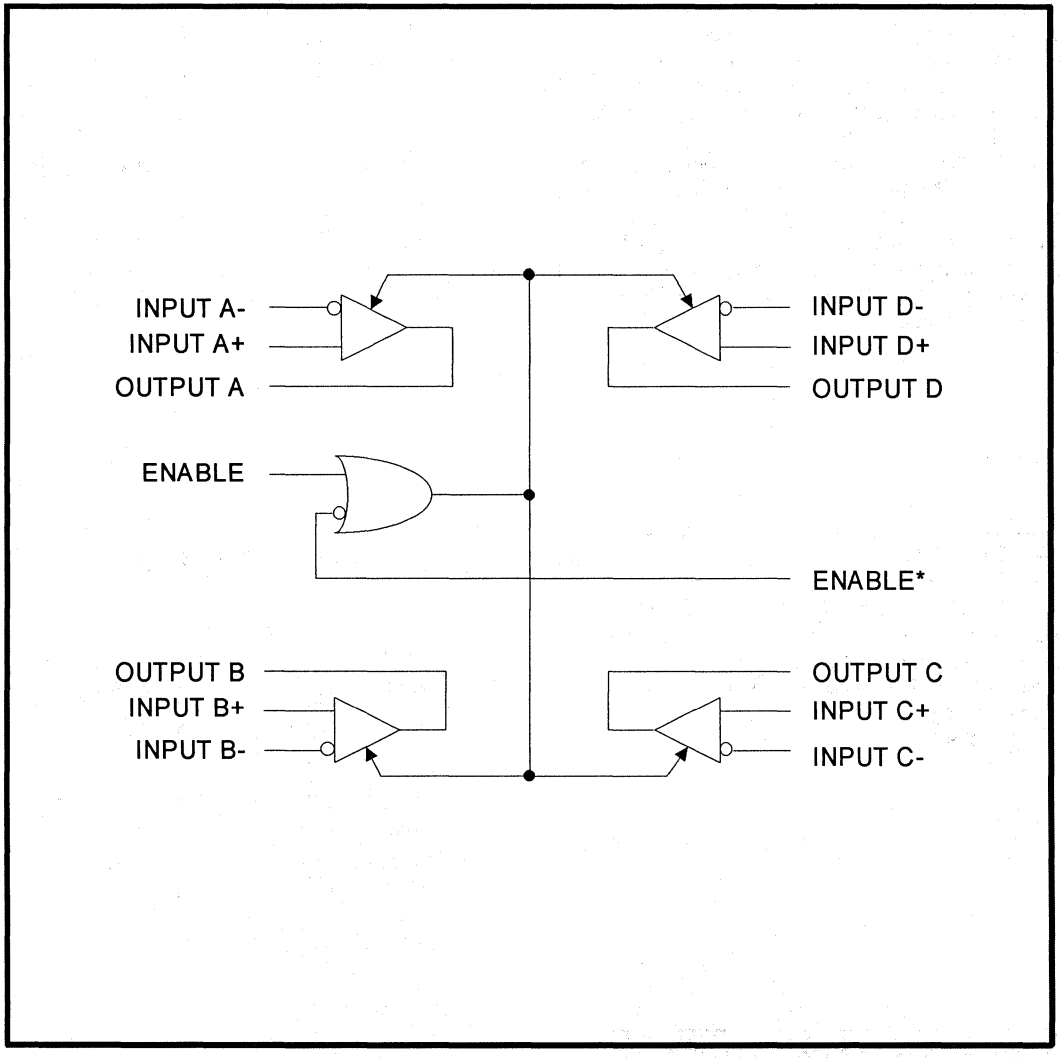


ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C32CP16	Plastic-DIP	0° C to + 70° C
ST26C32CF16	SOIC	0° C to + 70° C

ST26C32

BLOCK DIAGRAM



SYMBOL DESCRIPTION

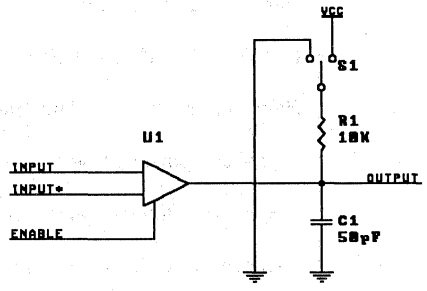
Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four receivers.
OUTPUT B	5	O	Receiver B output pin.
INPUT B+	6	I	Receiver B differential non-inverting input pin.
INPUT B-	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C-	9	I	Receiver C differential inverting input pin.
INPUT C+	10	I	Receiver C differential non-inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE *	12	I	Gate control (active low). See ENABLE description
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

ST26C32

Functional table

Enable	Enable*	Output	Differential Non-Inverting Input	Differential Inverting Input
L	H	Z	X	X
H	L	L	L	H
H	L	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any logic pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

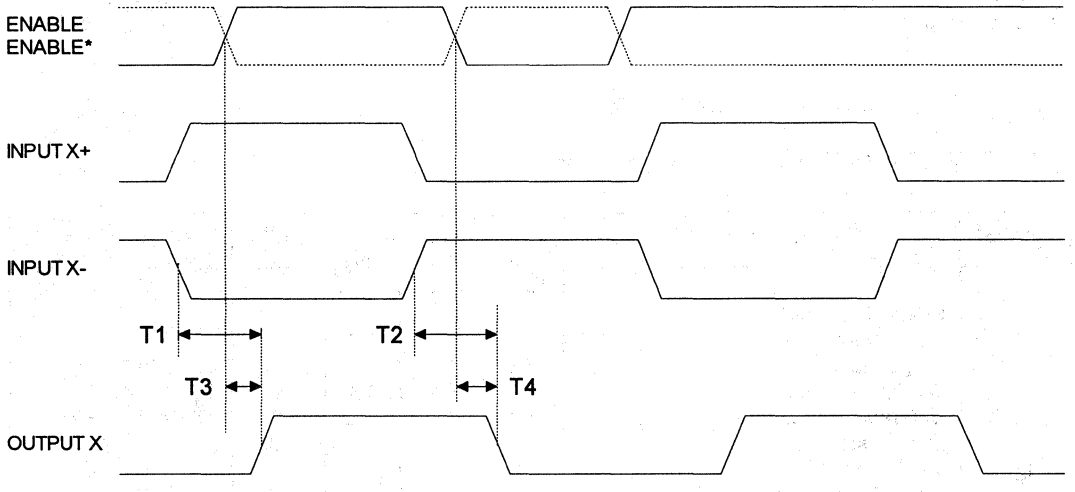
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8	4.2		V	I_{OH}= -6mA
V_{OL}	Output low level		0.2	0.4	V	I_{OH}= 6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	mA	
I_{CC}	Operating current		200		µA	V_{DIF}=+1V
I_{OZ}	Three state output leakage		±1.0	±5.0	µA	V_{OUT}=VCC or GND
I_{EN}	Enable input current		±1.0		mA	V_{IN}=VCC or GND
V_R	Input resistance		10		KΩ	-7V < V_{CM} < +7V

ST26C32

DIFFERENTIAL LINE RECEIVER TIMING



STARTECH

ST34C50
ST34C51

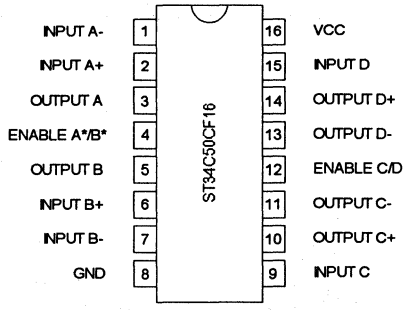
Printed February 23, 1994

DUAL RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER AND DRIVER

GENERAL DESCRIPTION

The ST34C50/51 is a CMOS dual differential line receiver and driver, designed to meet the standard RS-422, RS-423 requirements and digital data transmission over balanced lines. The ST34C50/51 has an input sensitivity of 200mv over the common mode input voltage range of ± 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C50/51 circuit. The ST34C50/51 is a high speed line receiver and driver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C50/51 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C50/51 is suitable for low power 5V operation with minimum board space requirements. ST34C50/51 provides dual differential line receiver with three state control pin and dual line driver with three state control capability.

SOIC Package

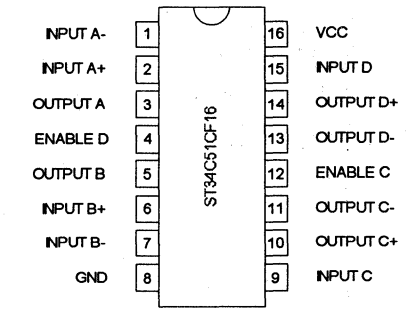


ST34C50CF / ST34C50CP

FEATURES

- Pin -to-pin compatible to Motorola MC34050 and MC34051
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422/423 requirements
- Low propagation delays
- High speed
- Dual line receiver with three state control
- Dual line driver with three state control

SOIC Package



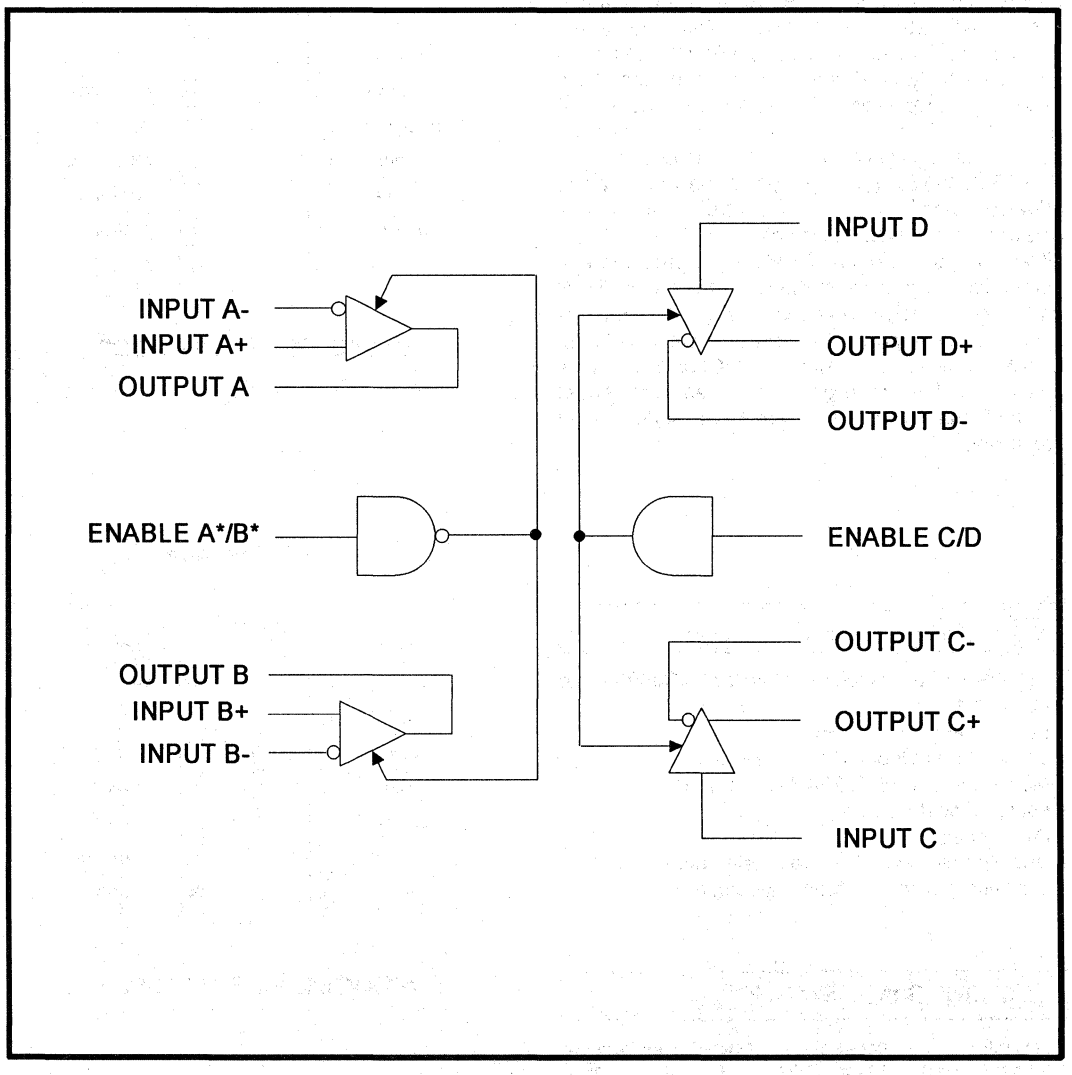
ST34C51CF / ST34C51CP

ORDERING INFORMATION

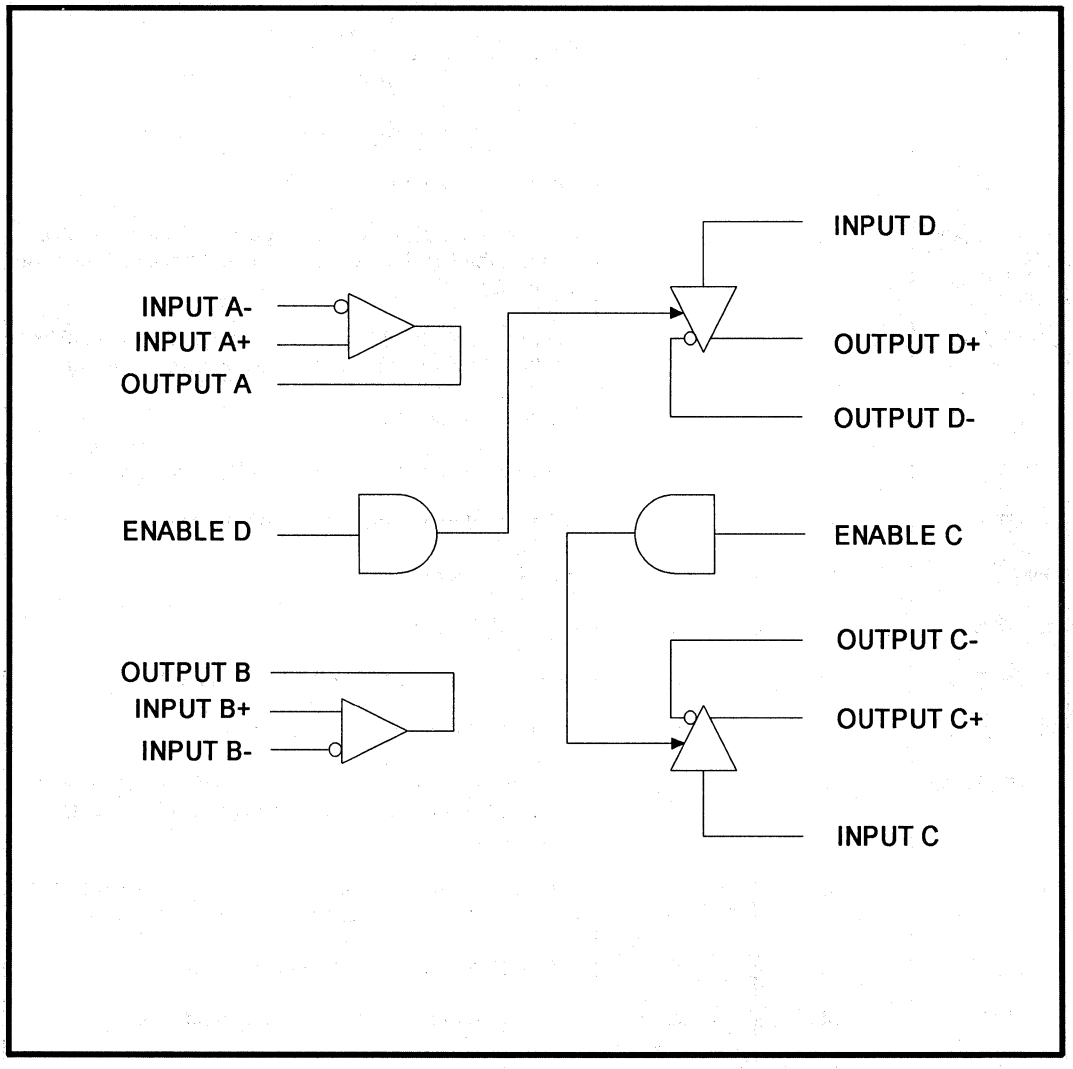
Part number	Package	Operating temperature
ST34C50CP16	Plastic-DIP	0° C to + 70° C
ST34C50CF16	SOIC	0° C to + 70° C
ST34C51CP16	Plastic-DIP	0° C to + 70° C
ST34C51CF16	SOIC	0° C to + 70° C

ST34C50
ST34C51

ST34C50 BLOCK DIAGRAM



ST34C51 BLOCK DIAGRAM



ST34C50
ST34C51

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active low, ST34C50 only). This pin enables/ disables the two line receiver outputs (out A and out B of ST34C50).
ENABLE D	4*	I	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver D section.
OUTPUT B	5	O	Receiver B output pin.
INPUT B +	6	I	Receiver B differential non-inverting input pin.
INPUT B -	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverted output pin.
OUTPUT C -	11	O	Driver C differential inverted output pin.
ENABLE C/D	12	I	Gate control (active high, ST34C50 only). This pin enables/ disables the two line driver outputs (output C and output D of ST34C50).
ENABLE C	12*	I	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver C section.
OUTPUT D -	13	O	Driver D differential inverted output pin.
OUTPUT D+	14	O	Driver D differential non-inverted output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

Receiver Functional table (ST34C50 only)

Enable A/B	Output	Differential Non-Inverting Input	Differential Inverting Input
H	Z	X	X
L	L	L	H
L	H	H	L

X=Don't care
Z=Three state (high impedance)
Receive sections of the ST34C51 are enabled all the time.

Driver Functional table (ST34C50 only)

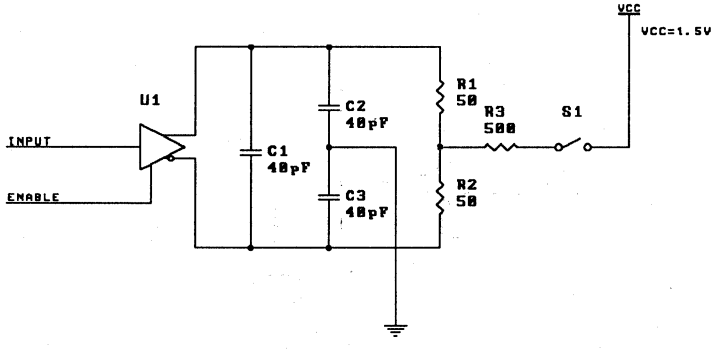
Enable C/D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

***Driver Functional table (ST34C51 only)**

Enable C or D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)
* for each section of ST34C51.

ST34C50/51 DRIVER AC TEST CIRCUIT



ST34C50
ST34C51

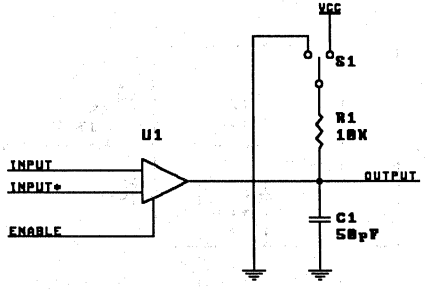
AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
	Line driver section					
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
*T_5	Skew			2	ns	S1 open
	Line receiver section					
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

* Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ST34C50/51 RECEIVER AC TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

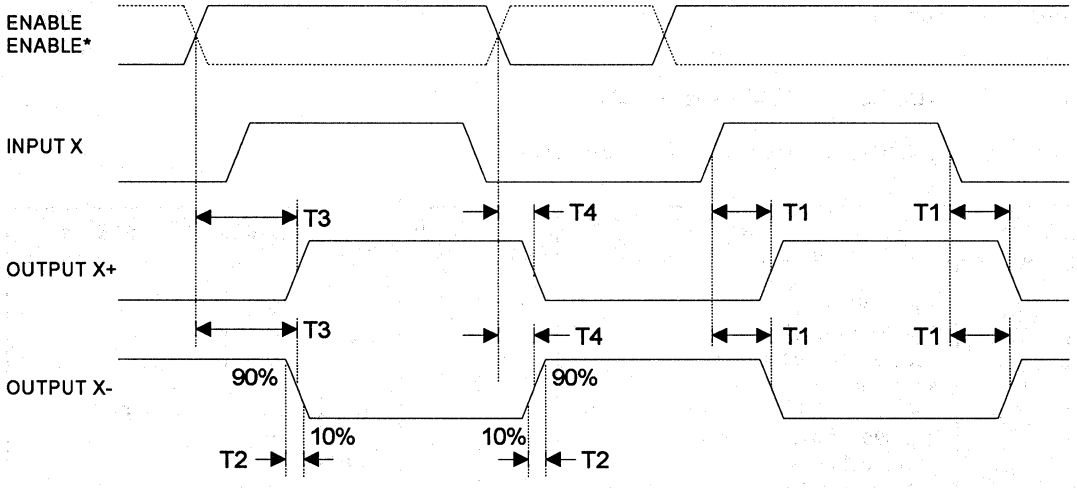
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

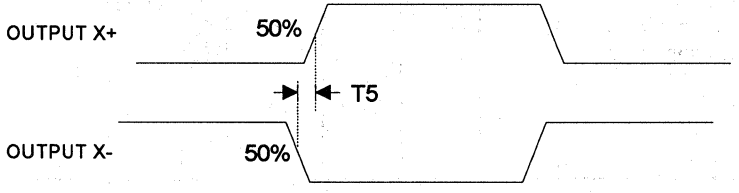
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

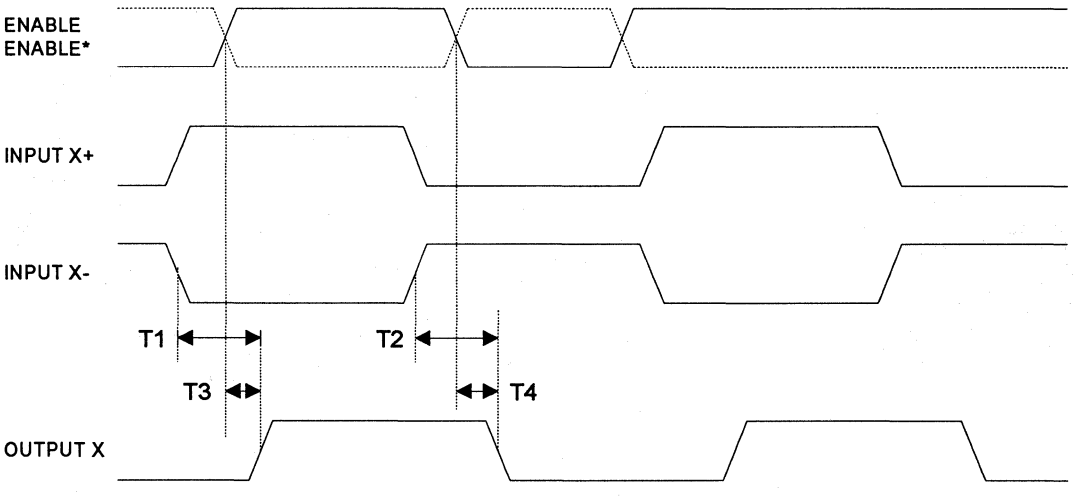
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{ROH}	Receiver output high level	3.8			V	
V_{ROL}	Receiver output low level			0.4	V	
V_{RID}	Receiver differential input level	-0.2		+0.2	V	R_L=100 Ω
V_{RH}	Receiver input hysteresis		50		mV	
I_{RIN}	Receiver input current			±1.0	mA	
V_{RR}	Receiver input resistance		10		KΩ	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{DOH}	Driver input high level	2.5			V	
V_{DOL}	Driver output low level			0.5	V	
V_{DOS}	Driver differential output level	2.0			V	R_L=100 Ω
V_{DOC}	Driver Common mode output voltage			3.0	V	R_L=100 Ω
V_{DOD}	Driver difference in common mode output			0.4	V	R_L=100 Ω
I_{DIN}	Driver input current			±1.0	µA	

DIFFERENTIAL LINE DRIVER TIMING





DIFFERENTIAL LINE RECEIVER TIMING



ST34C50
ST34C51

STARTECH

ST34C86

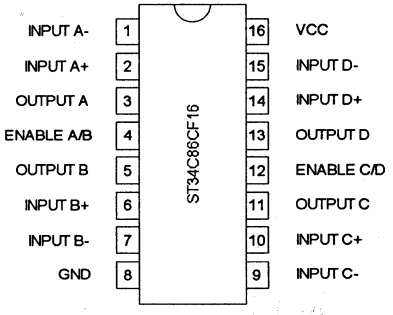
Printed February 23, 1994

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of ± 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit.
The ST34C86 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

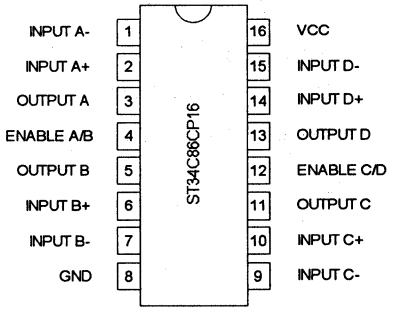
SOIC package



FEATURES

- Pin-to-pin compatible with National DS34C86
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

Plastic-DIP package

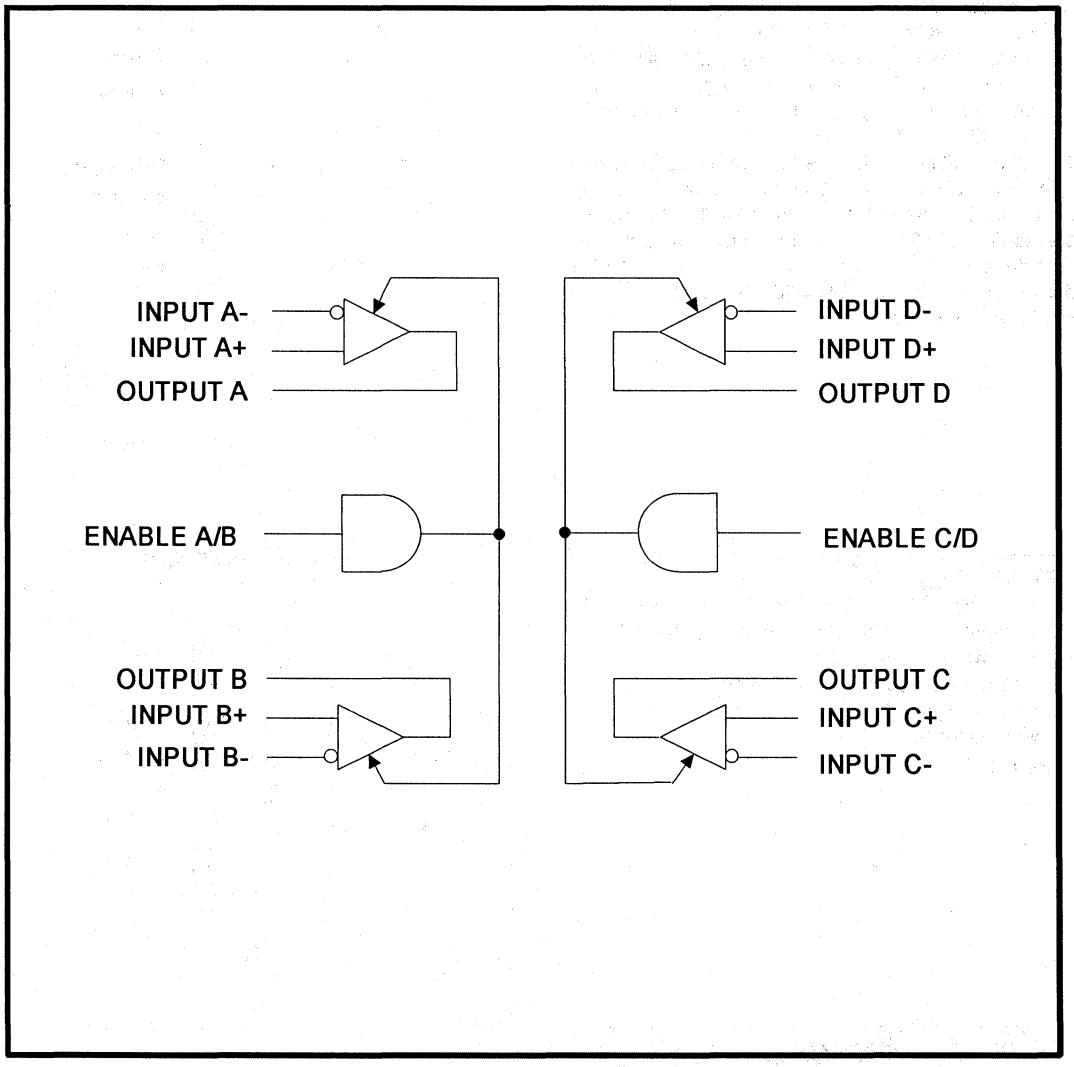


ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C86CP16	Plastic-DIP	0° C to + 70° C
ST34C86CF16	SOIC	0° C to + 70° C

ST34C86

BLOCK DIAGRAM



SYMBOL DESCRIPTION

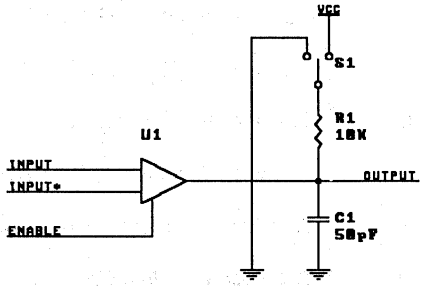
Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active high). This pin enables/disables the two line receiver outputs (out A and out B).
OUTPUT B	5	O	Receiver B output pin.
INPUT B+	6	I	Receiver B differential non-inverting input pin.
INPUT B-	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C-	9	I	Receiver C differential inverting input pin.
INPUT C+	10	I	Receiver C differential non-inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE C/D	12	I	Gate control (active high). This pin enables/disables the two line receiver outputs (output C and output D).
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

ST34C86

Functional table

Enable A/B C/D	Output	Differential Non-Inverting Input	Differential Inverting Input
L	Z	X	X
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any logic pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

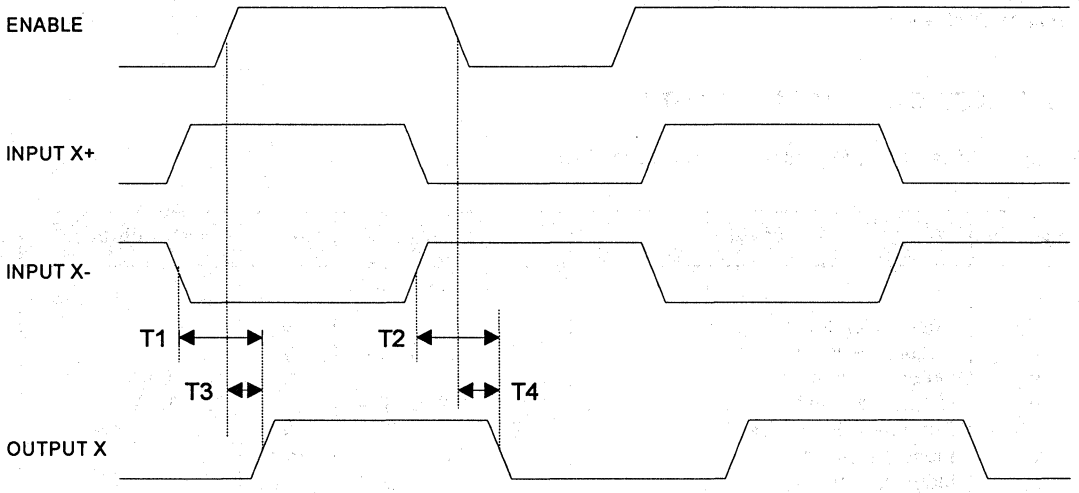
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8	4.2		V	I_{OH}= -6mA
V_{OL}	Output low level		0.2	0.4	V	I_{OH}= 6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	mA	
I_{CC}	Operating current		200		µA	V_{DIF}=+1V
I_{OZ}	Three state output leakage		±1.0	±5.0	µA	V_{OUT}=VCC or GND
I_{EN}	Enable input current		±1.0		mA	V_{IN}=VCC or GND
V_R	Input resistance		10		KΩ	-7V < V_{CM} < +7V

ST34C86

ST34C86

DIFFERENTIAL LINE RECEIVER TIMING



STARTECH

ST34C87

Printed February 23, 199

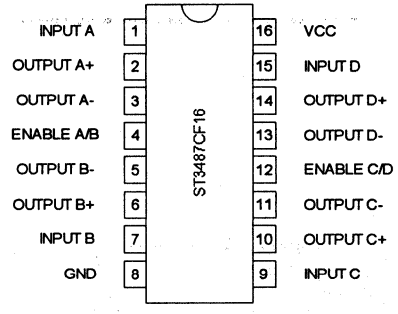
QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The ST34C87 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST34C87 circuit.

The ST34C87 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST34C87 is suitable for low power 5V operation with high input voltage protection devices.

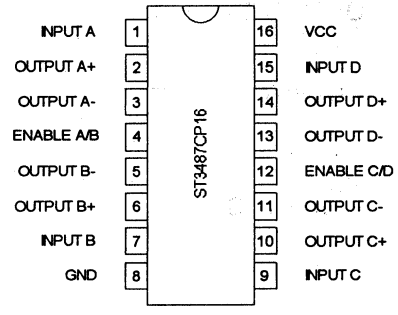
SOIC package



FEATURES

- Pin-to-pin compatible with National DS34C87
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

Plastic-DIP package

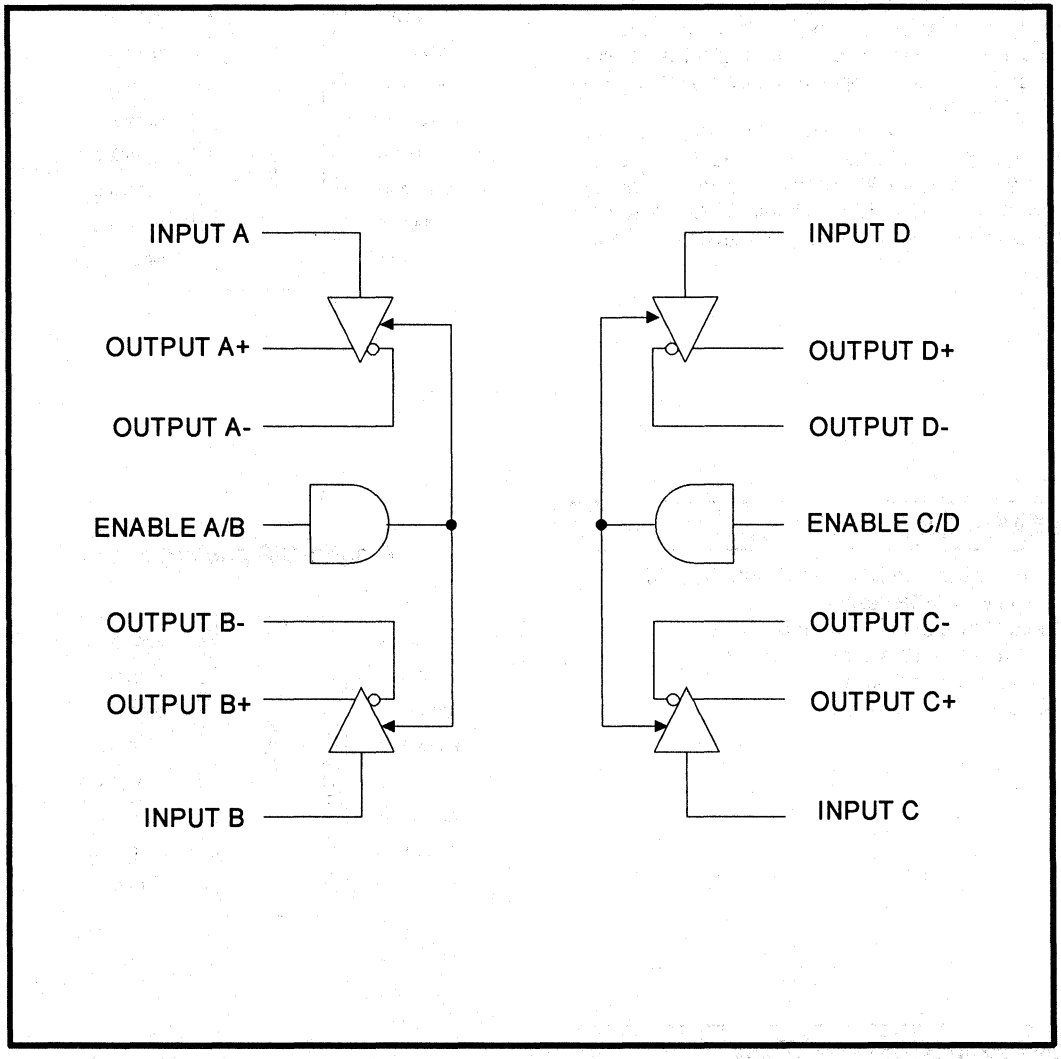


ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C87CP16	Plastic-DIP	0° C to + 70° C
ST34C87CF16	SOIC	0° C to + 70° C

ST34C87

BLOCK DIAGRAM



SYMBOL DESCRIPTION

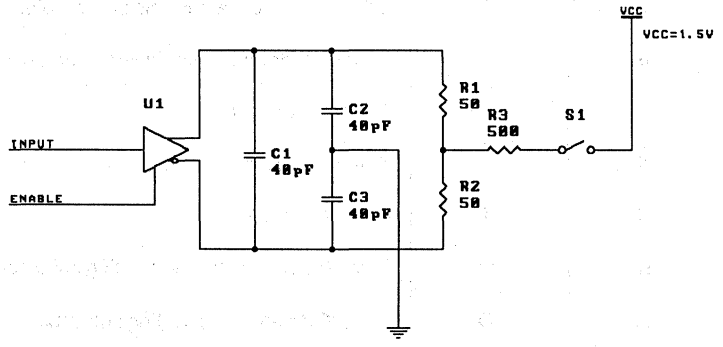
Symbol	Pin	Signal Type	Pin Description
INPUT A	1	I	Driver A input pin.
OUTPUT A+	2	O	Driver A differential non-inverting output pin.
OUTPUT A-	3	O	Driver A differential inverting output pin.
ENABLE A/B	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables two/four drivers.
OUTPUT B-	5	O	Driver B differential inverting output pin.
OUTPUT B+	6	O	Driver B differential non-inverting output pin.
INPUT B	7	I	Driver B input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverting output pin.
OUTPUT C-	11	O	Driver C differential inverting output pin.
ENABLE C/D	12	I	Gate control (active high). See ENABLE A/B pin description.
OUTPUT D-	13	O	Driver D differential inverting output pin.
OUTPUT D+	14	O	Driver D differential non-inverting output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

ST34C87

Functional table

Enable A/B C/D	Input	Differential Non-Inverting Output	Differential Inverting Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
*T_5	Skew			2	ns	S1 open

* Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

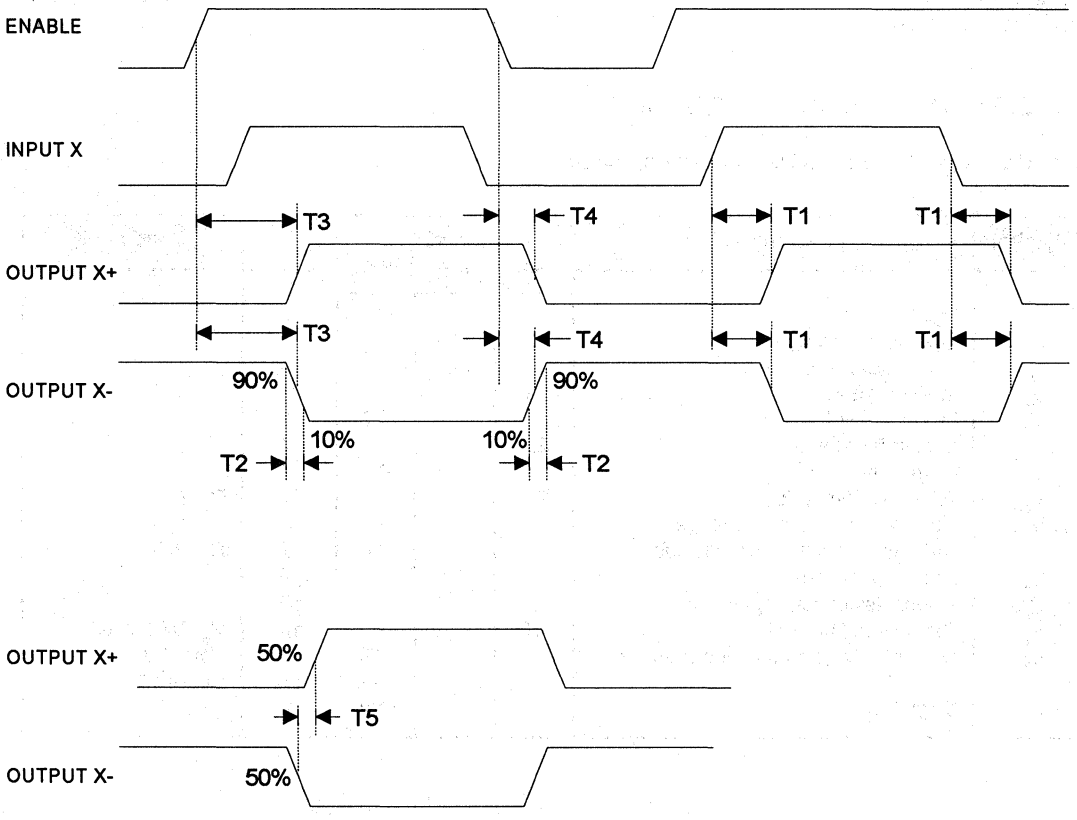
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{IH}	Input high level	2.0			V	
V_{IL}	Input low level			0.8	V	
V_{OH}	Output high level	2.5			V	
V_{OL}	Output low level			0.5	V	
V_{OS}	Differential output level	2.0			V	R_L=100Ω
V_{OC}	Common mode output voltage			3.0	V	R_L=100Ω
V_{OD}	Difference in common mode output			0.4	V	R_L=100Ω
C_{IN}	Input capacitance	7	10	15	pF	
C_{PD}	Power dissipation capacitance		100		pF	
I_{OS}	Output short current	-30		-150	mA	V_{IN}=VCC or GND
I_{OFF}	Output leakage current power off			100	µA	Vout=6V
				-100	µA	Vout=0.25V
I_{DC}	Output current			±150	mA	

ST34C87

DIFFERENTIAL LINE DRIVER TIMING



STARTECH

ST31C32

Printed February 23, 1994

RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVERS AND DRIVERS

GENERAL DESCRIPTION

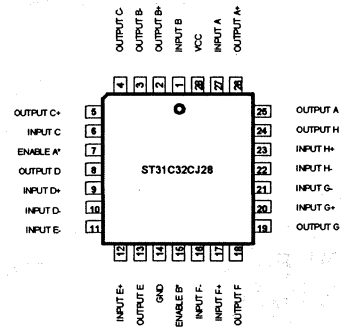
The ST31C32 is a high speed CMOS combo differential line receiver and driver designed to meet the standard RS-422, RS-423 requirements for digital and transmission over balanced lines. It provides five differential line receivers with three state control and three line drivers also with three state control.

The line driver inputs and line receiver outputs are TTL compatible to interface with standard 74LS and CMOS environments. The ST31C32 has been designed for low power 5 volts operation and is especially suited for MODEM/UART applications.

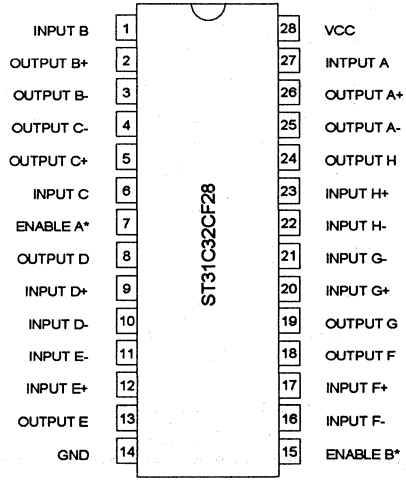
The receiver in the ST31C32 has an input sensitivity of 200mv over the common mode input voltage range of ± 7V. They incorporate hysteresis for improved noise margin with slow changing input signals. Input fail-safe circuitry is also included which will cause the output of the receiver to go to a logic "1" level if the inputs are left open.

A special voltage sensing circuit is utilized in the drivers that will three-state the outputs during power down and power up. This will prevent spurious glitches from appearing on the outputs.

PLCC Package



SOIC Package



FEATURES

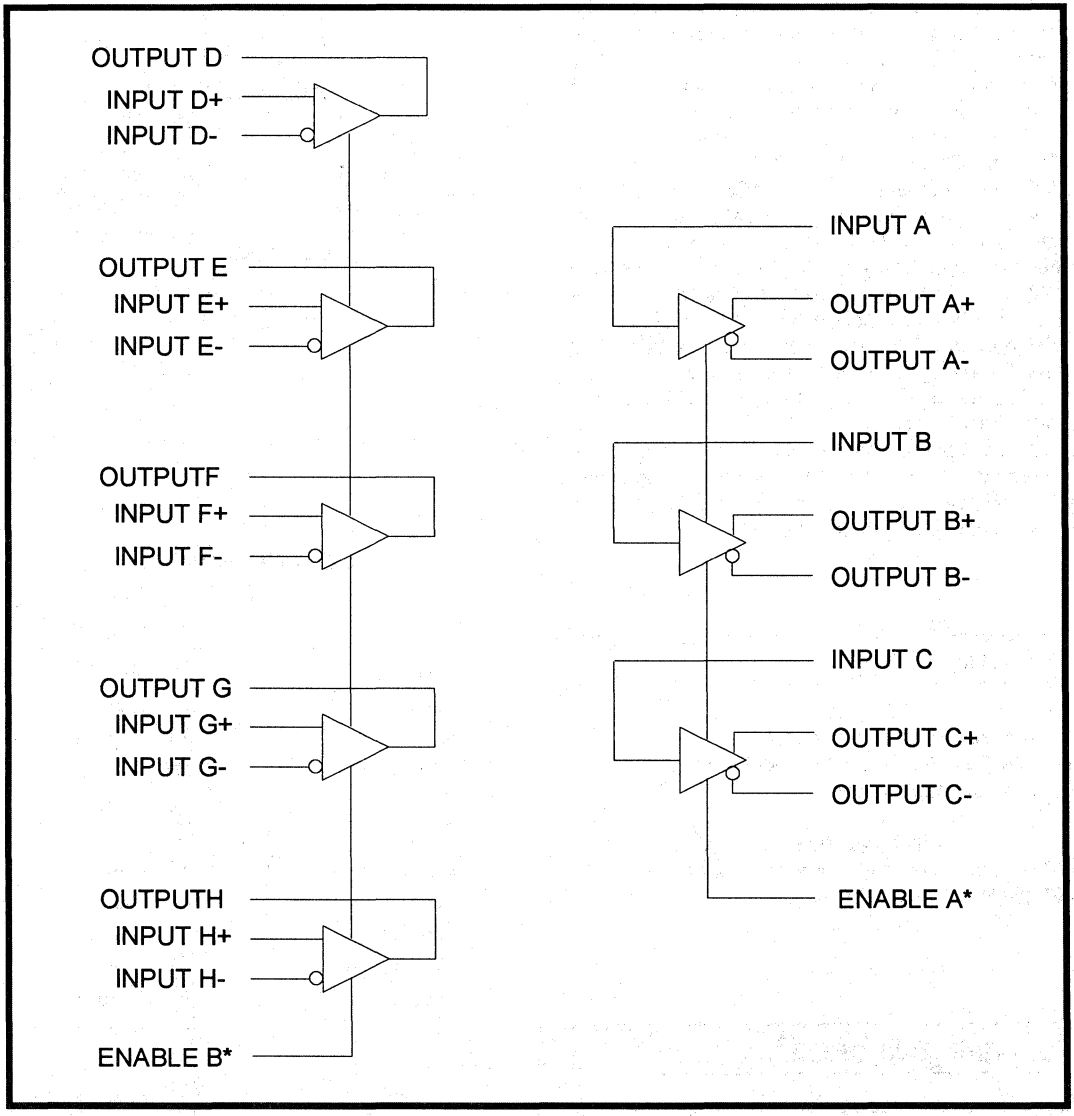
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422/423 requirements
- Low propagation delays
- High speed
- Five line receivers with three state control
- Three line drivers with three state control
- 28 pin PLCC and SOiC package

ORDERING INFORMATION

Part number	Package	Operating temperature
ST31C32CJ28	PLCC	0° C to + 70° C
ST31C32CF28	SOIC	0° C to + 70° C

ST31C32

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT B	1	I	Line driver B input pin.
OUTPUT B+	2	O	Line driver B differential non-inverted output pin.
OUTPUT B -	3	O	Line driver B differential inverted output pin.
OUTPUT C -	4	O	Line driver C differential inverted output pin.
OUTPUT C+	5	O	Line driver C differential non-inverted output pin.
INPUT C	6	I	Line driver C input pin.
ENABLE A*	7*	I	Gate control A (active low). This pin enables/ disables the three line driver outputs.
OUTPUT D	8	O	Line receiver D output pin.
INPUT D +	9	I	Line receiver D differential non-inverted input pin.
INPUT D -	10	I	Line receiver D differential inverted input pin.
INPUT E -	11	I	Line receiver E differential inverted input pin.
INPUT E +	12	I	Line receiver E differential non-inverted input pin.
OUTPUT E	13	O	Line receiver E output pin.
GND	14	O	Signal and power ground.
ENABLE B*	15*	I	Gate control B (active low). This pin enables/ disables the five line receiver outputs.
INPUT F -	16	I	Line receiver F differential inverted input pin.
INPUT F +	17	I	Line receiver F differential non-inverted input pin.
OUTPUT F	18	O	Line receiver F output pin.
OUTPUT G	19	O	Line receiver G output pin.
INPUT G +	20	I	Line receiver G differential non-inverted input pin.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT G -	21	I	Line receiver G differential inverted input pin.
INPUT H -	22	I	Line receiver H differential inverted input pin.
INPUT H +	23	I	Line receiver H differential non-inverted input pin.
OUTPUT H	24	O	Line receiver H output pin.
OUTPUT A -	25	O	Line driver A differential inverted output pin.
OUTPUT A+	26	O	Line driver A differential non-inverted output pin.
INPUT A	27	I	Line driver A input pin.
VCC	28	I	Power supply pin.

*Has internal pull-up resistor on input

Receiver Functional table

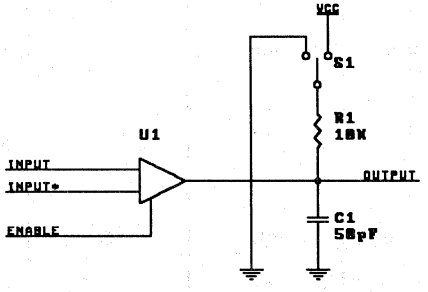
Enable B	Differential Non-Inverting Input	Differential Inverting Input	Output
H	X	X	Z
L	L	H	L
L	H	L	H

Driver Functional table

Enable A	Input	Differential Non-Inverted Output	Differential Inverted Output
H	X	Z	Z
L	L	L	H
L	H	H	L

X=Don't care
Z=Three state (high impedance)

ST31C32 RECEIVER AC TEST CIRCUIT

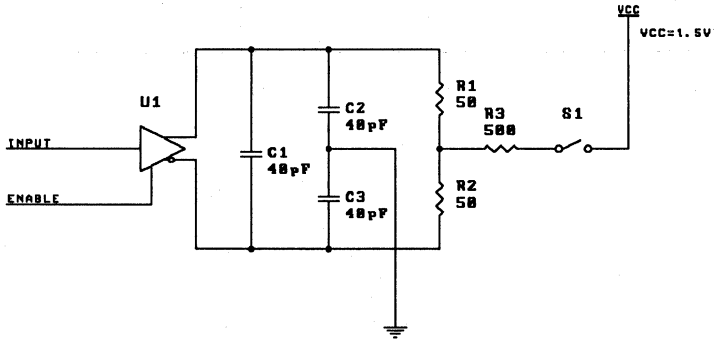


AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
	Line Receiver Timing					
T_1	Propagation delay, input to output		8	10	ns	S1=VCC
T_2	Propagation delay, input to putput		18	20	ns	S1=GND
T_3	Output enable time		18	20	ns	V_{DIF}=2.5V
T_4	Output disable time		18	20	ns	V_{DIF}=2.5V
	Line Driver Timing					
T_1	Propagation delay, input to output		8	10	ns	S1 open
T_2	Differential output rise and fall time		8	10	ns	S1 open
T_3	Output enable time		18	20	ns	S1 close
T_4	Output disable time		18	20	ns	S1 close
T_5	Skew		0.5		ns	S1 open

ST31C32 DRIVER AC TEST CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

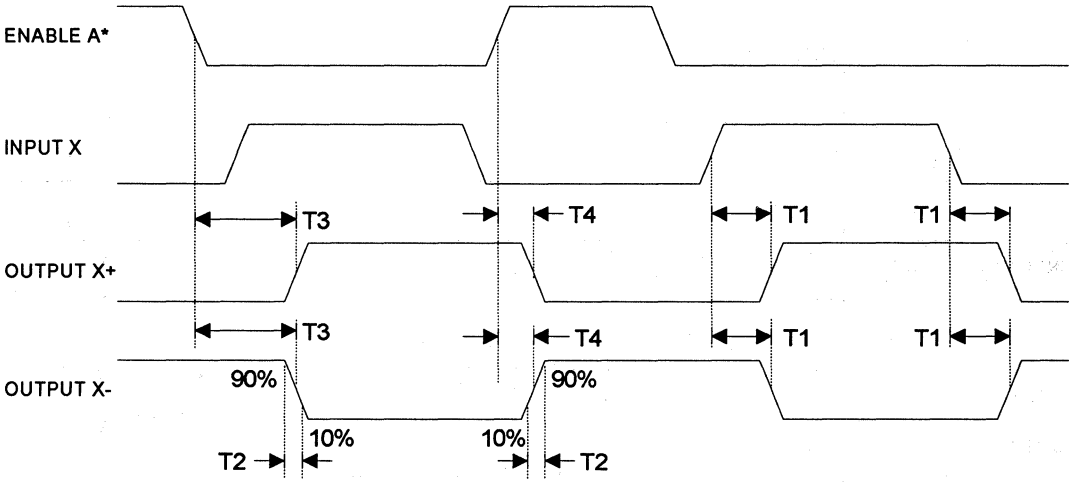
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

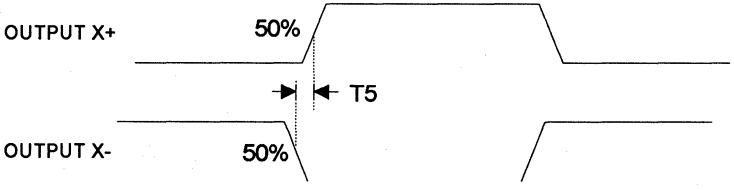
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{ROH}	Receiver output high level	3.8			V	
V_{ROL}	Receiver output low level			0.4	V	
V_{RID}	Receiver differential input level	-0.2		+0.2	V	R_L=100 Ω
V_{RH}	Receiver input hysteresis		50		mV	
I_{RIN}	Receiver input current			±1.0	mA	
V_{RR}	Receiver input resistance		10		KΩ	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{DOH}	Driver input high level	2.5			V	
V_{DOL}	Driver output low level			0.5	V	
V_{DOS}	Driver differential output level	2.0			V	R_L=100 Ω
V_{DOC}	Driver Common mode output voltage			3.0	V	R_L=100 Ω
V_{DOD}	Driver difference in common mode output			0.4	V	R_L=100 Ω
I_{DIN}	Driver input current			±1.0	mA	

DIFFERENTIAL LINE DRIVER TIMING





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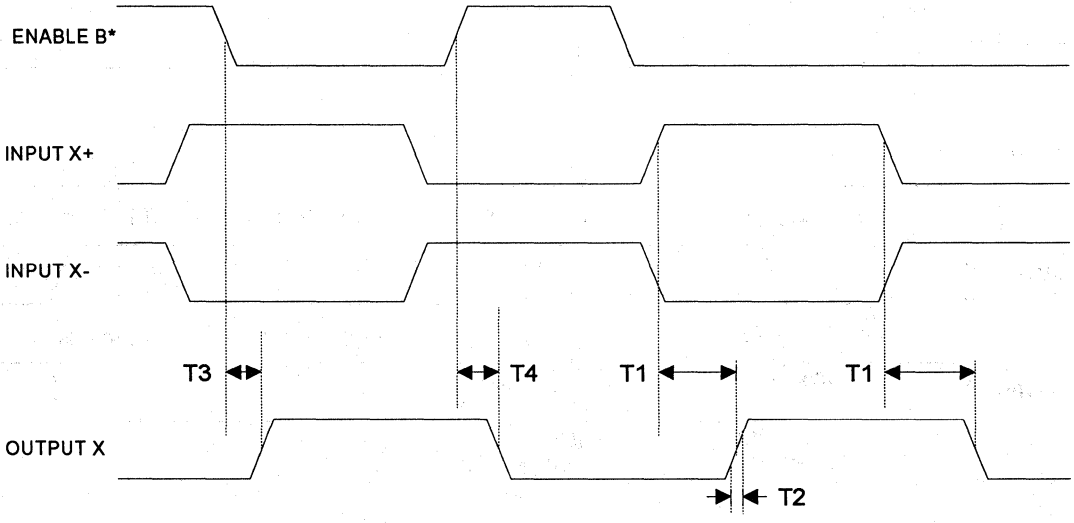
DIFFERENTIAL LINE RECEIVER TIMING



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STARTECH

ST16C450

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

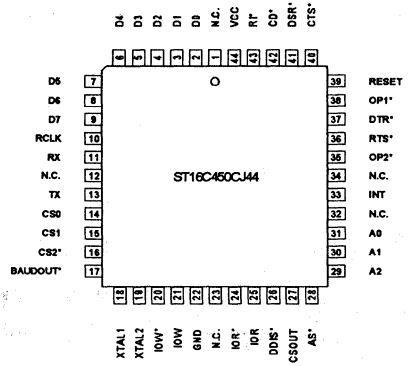
DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

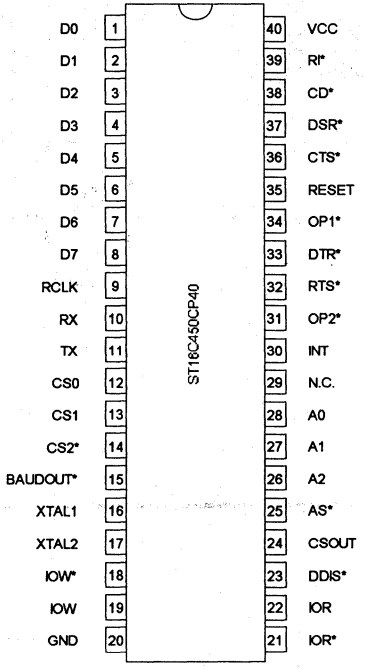
The ST16C450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C450 provides internal loop-back capability for on board diagnostic testing.

The ST16C450 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

- Pin to pin and functional compatible to NS16450,VL16C450,WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

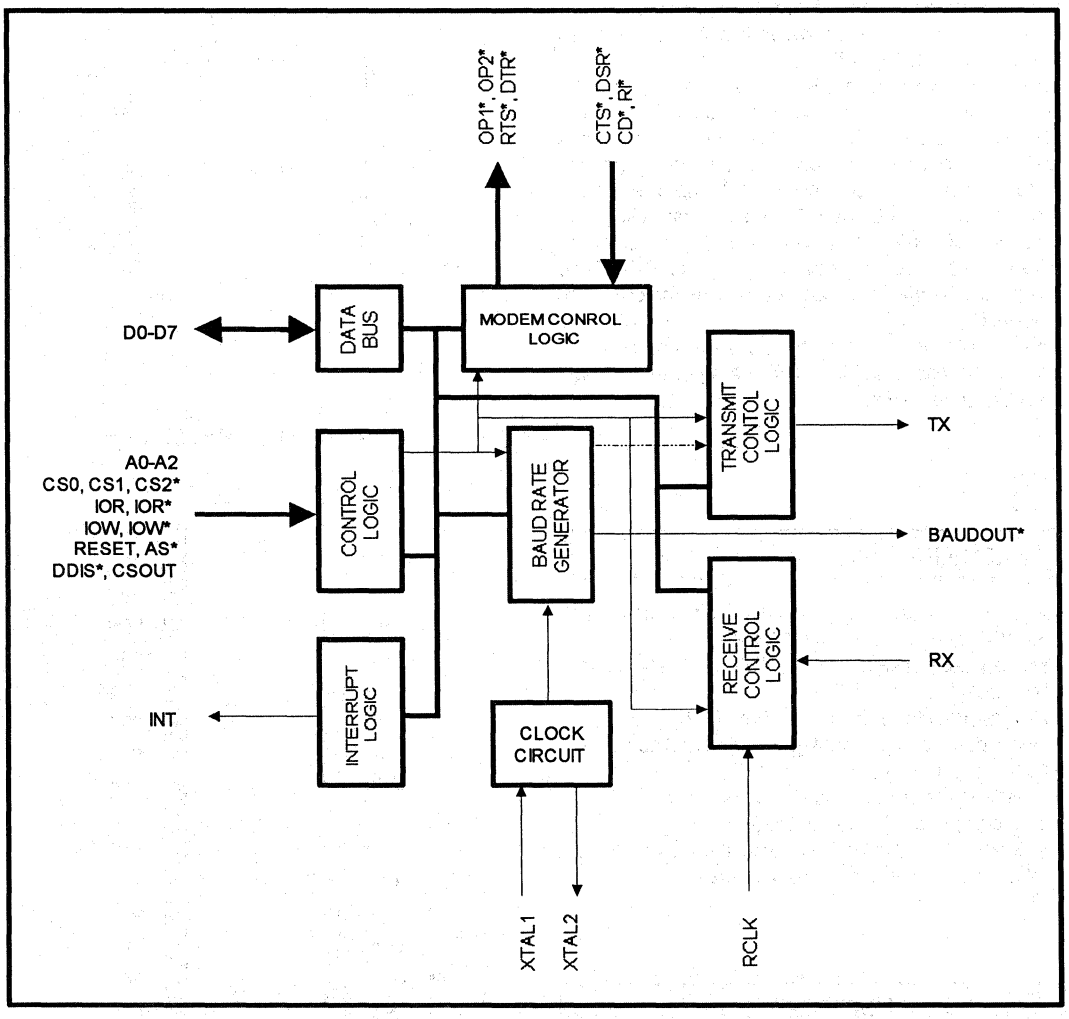
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C450CP40	Plastic-DIP	0° C to + 70° C
ST16C450CJ44	PLCC	0° C to + 70° C
ST16C450CQ48	TQFP	0° C to + 70° C

*** Industrial operating range are available.**

ST16C450

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the ST16C450 receiver section if receiver data rate is different from transmitter data rate.
RX	10	I	Serial data input. The serial information (data) received from serial port to ST16C450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS1	13	I	Chip select 2 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS2*	14	I	Chip select 3 (active low). A low at this pin (while CS0=1 and CS1=1) will enable the ST16C450 / CPU data transfer operation.
BAUDOUT*	15	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide the receiver clock.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	Write strobe (active high). Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C450 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	O	Signal and power ground.
IOR*	21	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C450 data bus to the CPU.
IOR	22	I	Read strobe (active high). Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C450 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23	O	Drive disable (active low). This pin goes low when the CPU is reading data from the ST16C450 to disable the external transceiver or logic's.
CSOUT	24	O	Chip select out. A high on this pin indicates that the ST16C450 has been enabled by the chip select pin.
AS*	25	I	Address strobe (active low). A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	I	Address select line 2. To select internal registers.
A1	27	I	Address select line 1. To select internal registers.
A0	28	I	Address select line 0. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
N/C	29		No connection.
INT	30	O	Interrupt output (active high). This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	O	General purpose output (active low). User defined output. See bit-3 modem control register (MCR bit-3).
RTS*	32	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	O	Data terminal ready (active low). To indicate that ST16C450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	O	General purpose output (active low). User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	35	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	37	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD*	38	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
RI*	39	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

All unused input pins should be tied to VCC or GND.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C450 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

ST16C450

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:
0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts

are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C450 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNAL	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
INT	Low

ST16C450

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

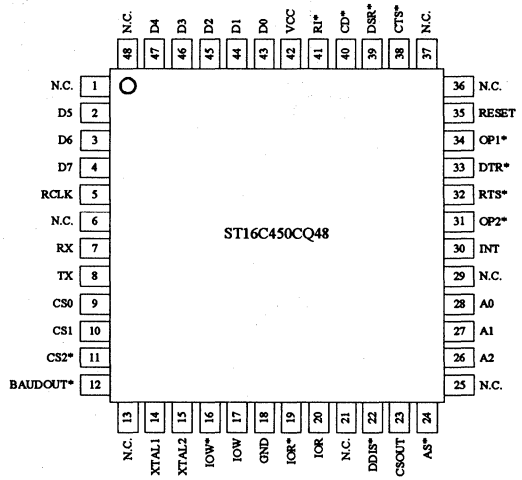
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	Note: 2
T_2	Clock low pulse duration	50			ns	Note: 2
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	15			ns	
T_7	Address hold time	15			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select			10	ns	
T_{11}	IOR* to DDIS* delay			35	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	55			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	25			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data	25			ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	*	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low.
Note 2: 1.8432 Mhz crystal or External clock.
* = Baudout* cycle



ST16C450

ST16C450

ABSOLUTE MAXIMUM RATINGS

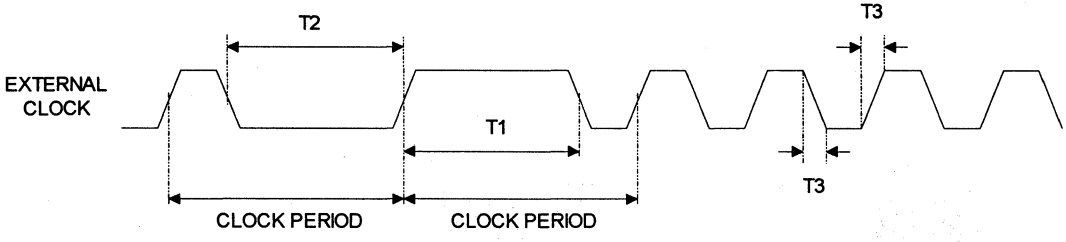
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

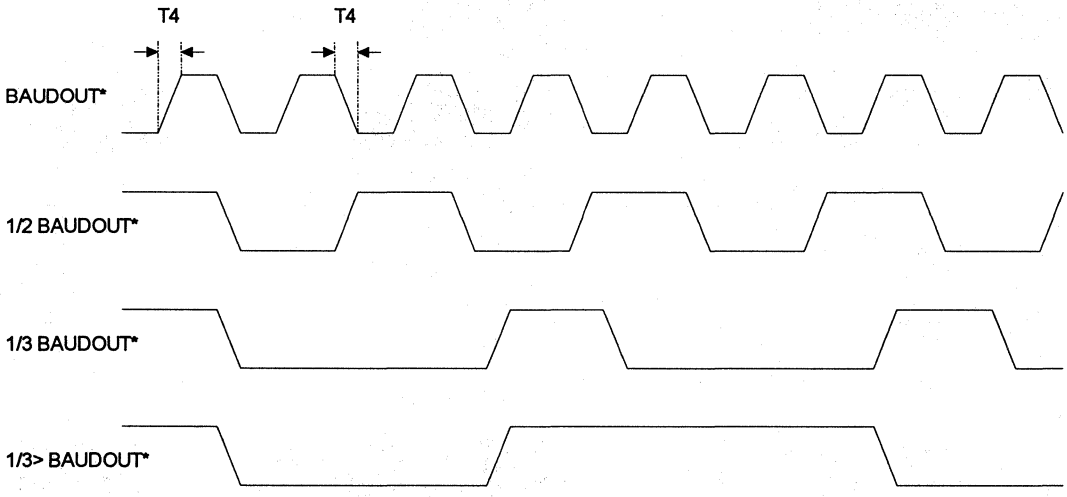
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

CLOCK TIMING



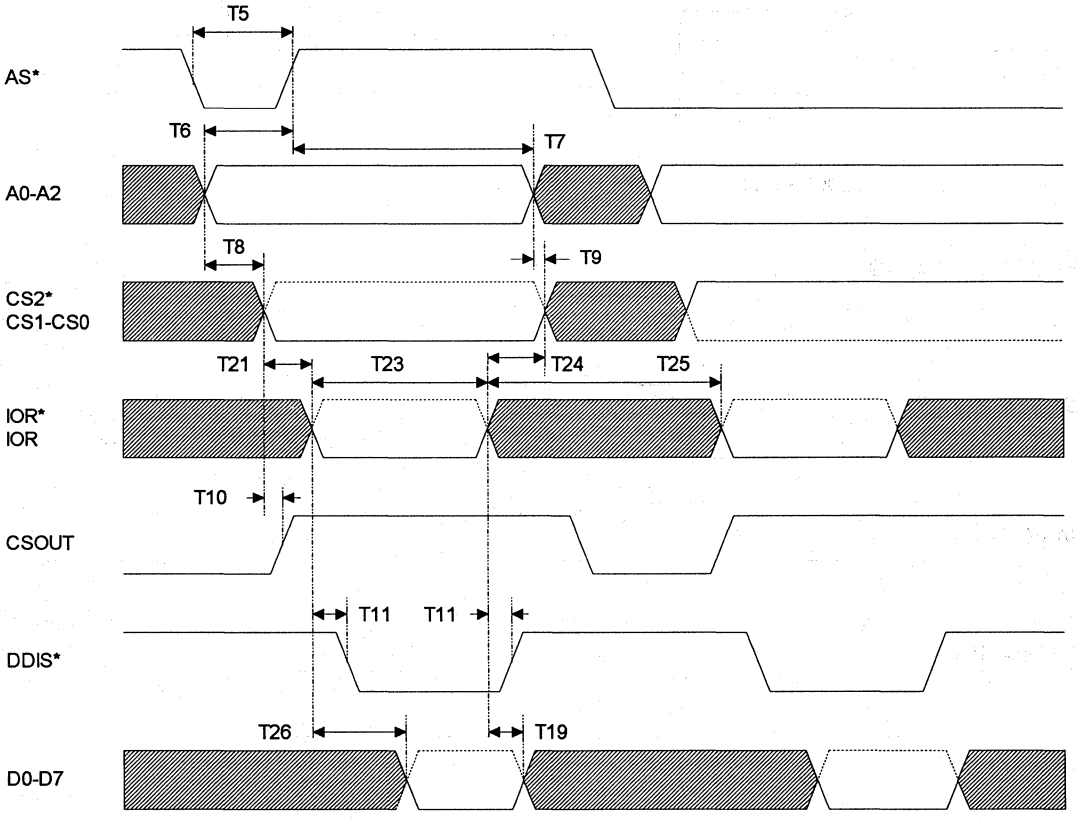
BAUDOUT* TIMING



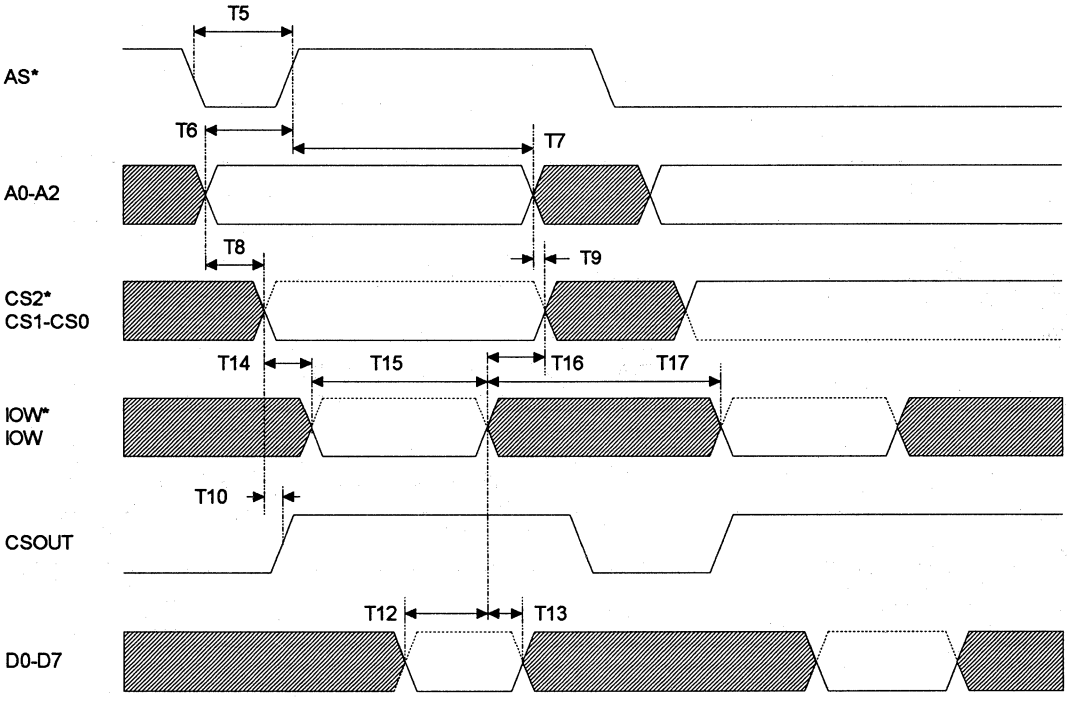
ST16C450

ST16C450

GENERAL READ TIMING

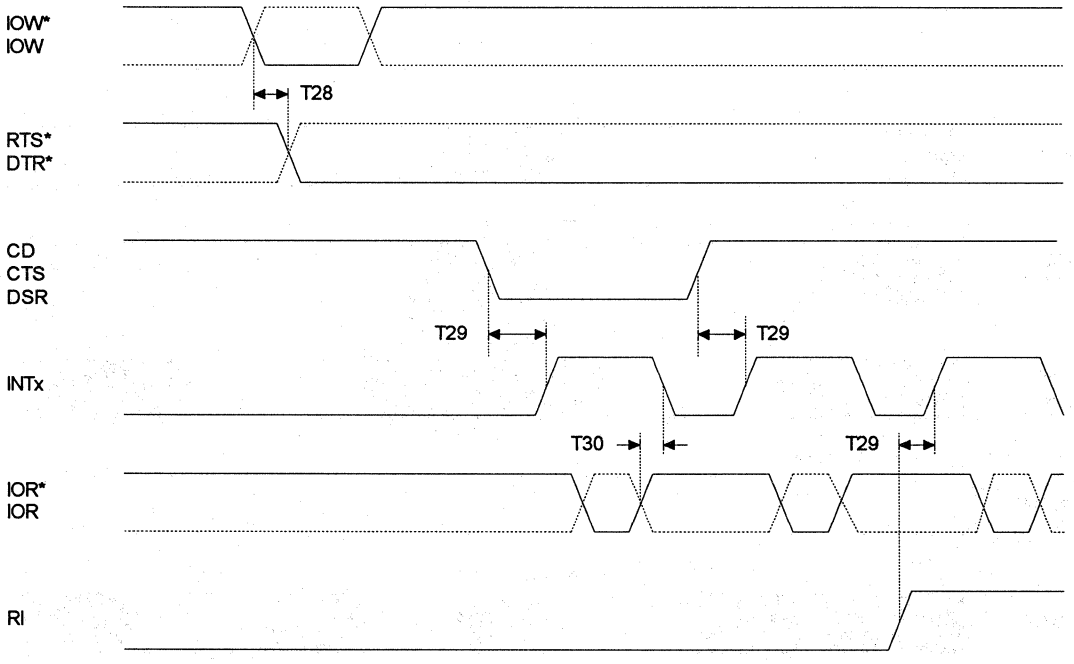


GENERAL WRITE TIMING

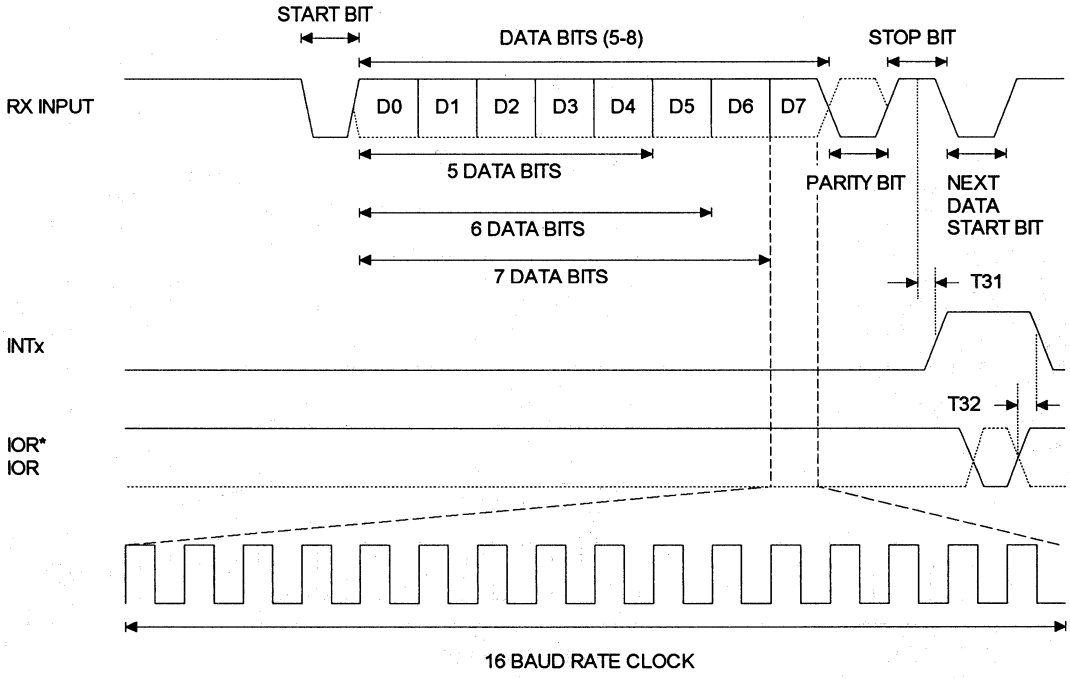


ST16C450

MODEM TIMING

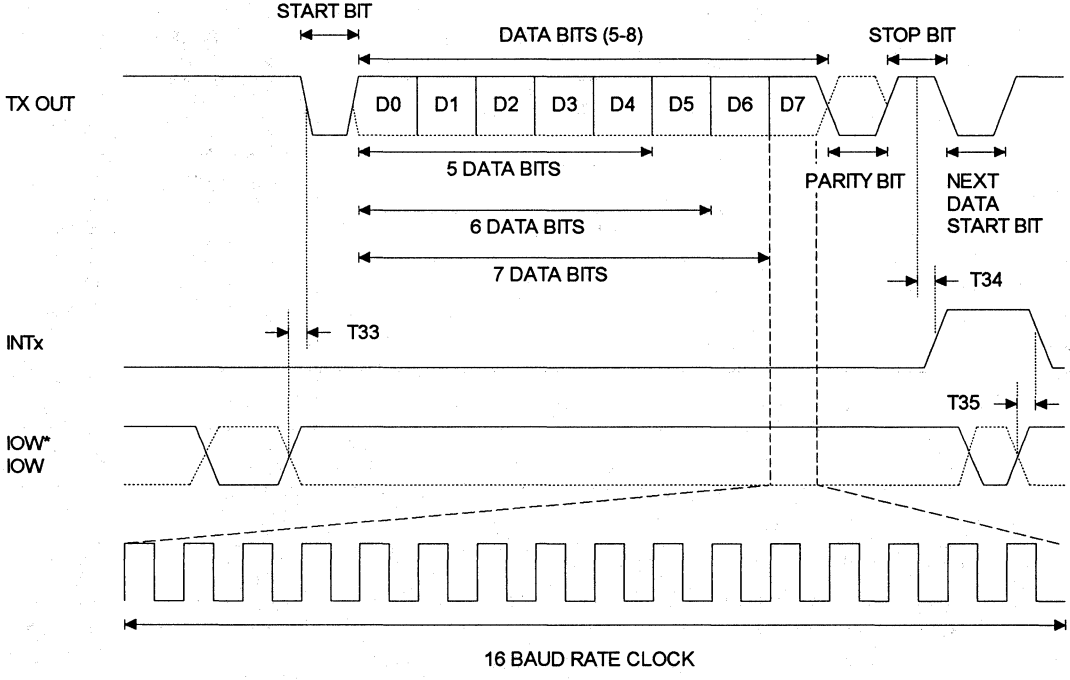


RECEIVE TIMING



ST16C450

TRANSMIT TIMING



STARTECH

ST16C1450
ST16C1451

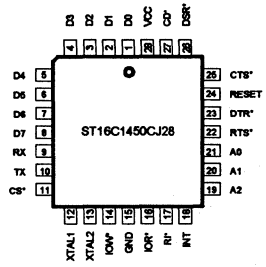
Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C1450/51 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.
The ST16C1450/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1450/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1450/51 provides internal loop-back capability for on board diagnostic testing.
The ST16C1450/51 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package

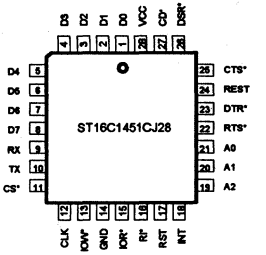


ST16C1450

FEATURES

- Pin to pin and functional compatible to SSI 73M1550/2550
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
- 28 Pin plastic-Dip and PLCC package
- Pin-to-pin compatible to ST16C1550/1551

PLCC Package



ST16C1451

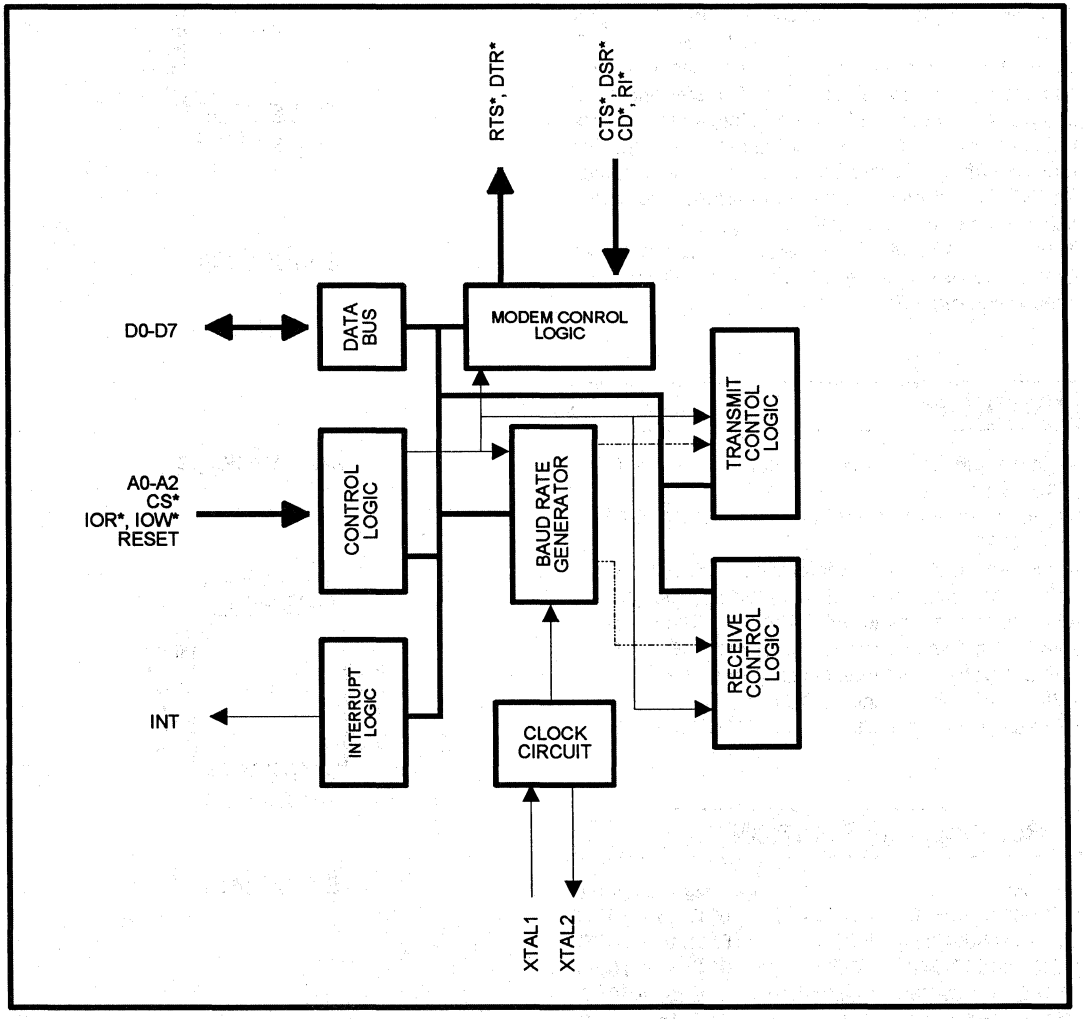
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1450CP28	Plastic-DIP	0° C to + 70° C
ST16C1450CJ28	PLCC	0° C to + 70° C
ST16C1450CQ48	TQFP	0° C to + 70° C
ST16C1451CP28	Plastic-DIP	0° C to + 70° C
ST16C1451CJ28	PLCC	0° C to + 70° C
ST16C1451CQ48	TQFP	0° C to + 70° C

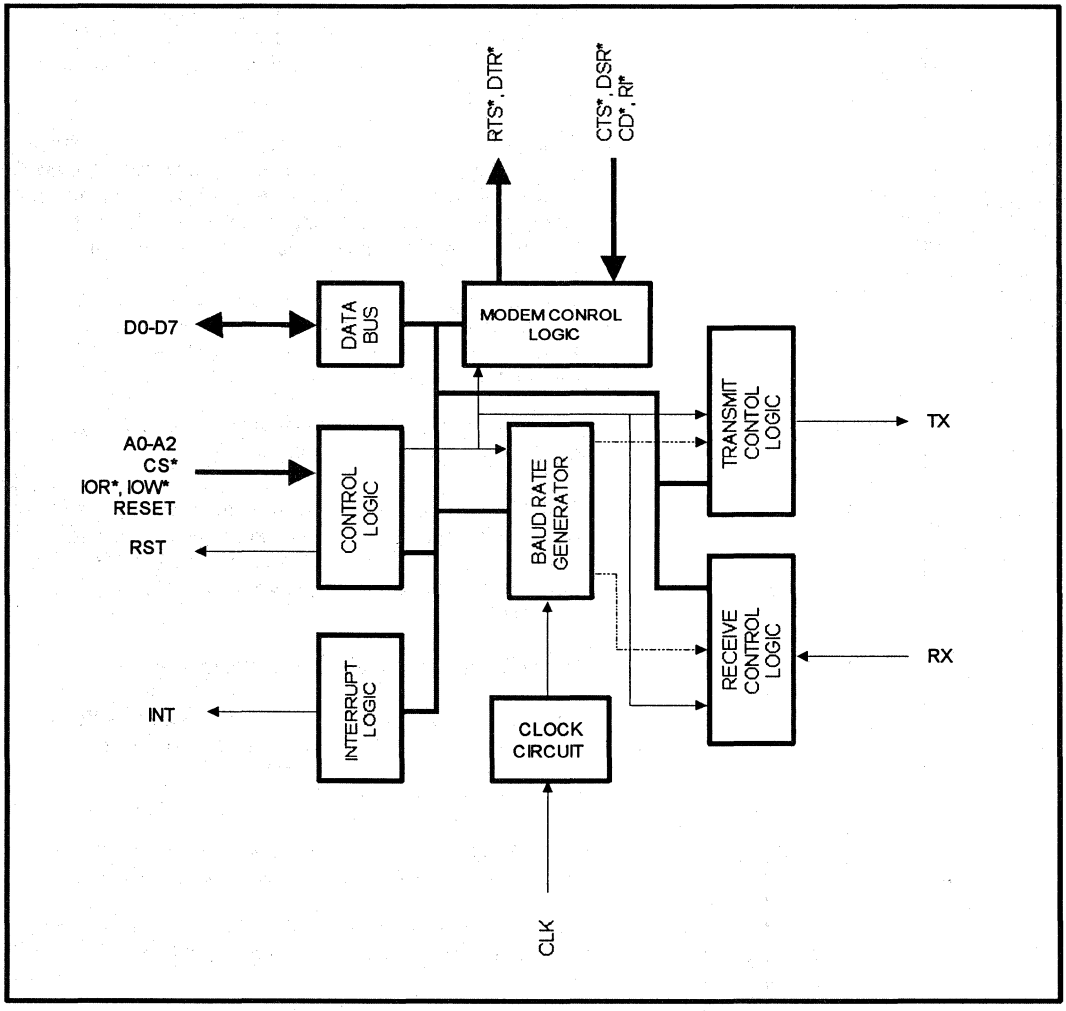
***Industrial operating range are available.**

ST16C1450
ST16C1451

ST16C1450 BLOCK DIAGRAM



ST16C1451 BLOCK DIAGRAM



ST16C1450
ST16C1451

ST16C1450 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1450 / CPU data transfer operation.
XTAL1	12	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	O	Signal and power ground.
IOR*	16	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1450 data bus to the CPU..
RI*	17	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
INT	18	O	Interrupt output. (three state / active high) This pin goes high

ST16C1450 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			(when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1450
ST16C1451

ST16C1451 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1451 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1451 / CPU data transfer operation.
CLK	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
IOW*	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	14	O	Signal and power ground.
IOR*	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1451 data bus to the CPU.
RI*	16	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
RST	17	O	Reset output (active high). The ST16C1451 provides a buffered reset output which is gated internally with MCR bit-2.

ST16C1451 SYMBOL DESCRIPTION

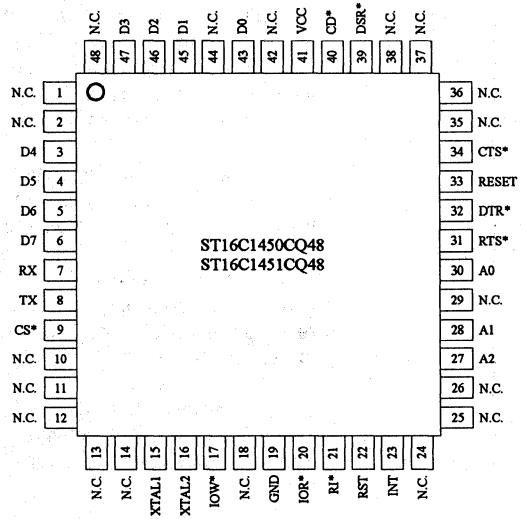
Symbol	Pin	Signal Type	Pin Description
INT	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1451 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1450
ST16C1451

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

All unused input pins should be tied to VCC or GND.



ST16C1450 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

ST16C1450
ST16C1451

ST16C1451 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1450/51 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT-5:
0=normal ST16C450 mode.
1=special mode. Enable power down and SOFT rest.

IER BIT 4,6-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1450/51 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1450/51 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority levels

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR bit 3-7:
Not used

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-6:
Not used. Are set to zero permanently.

MCR bit-7:
0=normal mode.
1=power down mode. XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C1450/51 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used.

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MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C1450/51 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.
Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1450/51 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

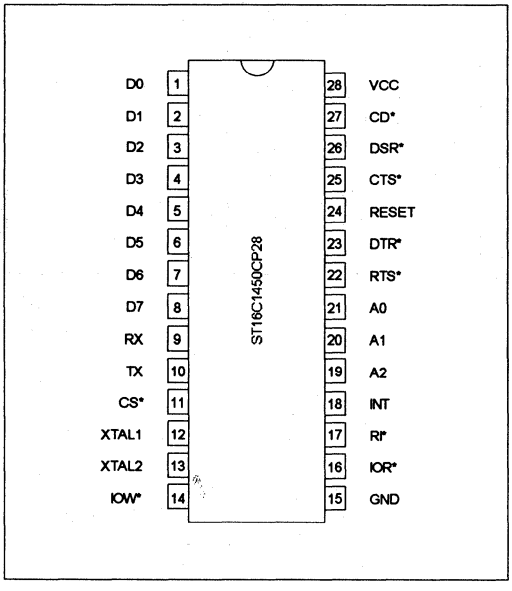
BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C1450/51 EXTERNAL RESET CONDITION

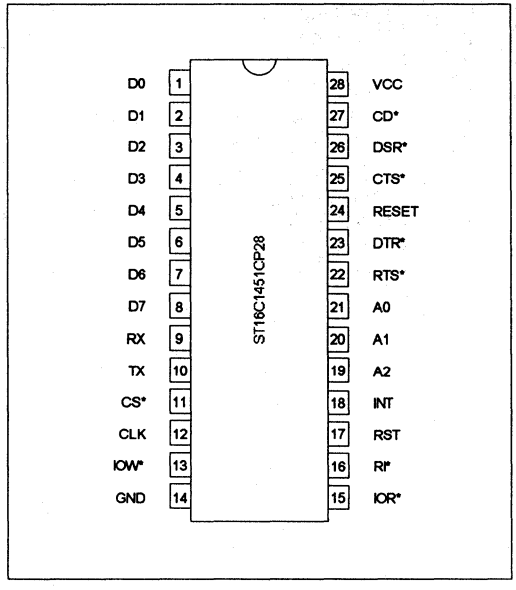
REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state mode

ST16C1450 Plastic-DIP Package



ST16C1451 Plastic-DIP Package



ST16C1450
ST16C1451

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	Note: 1
T_2	Clock low pulse duration	50			ns	Note: 1
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	105			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	*	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: 1.8432 MHz crystal or External clock
* = Baudout* cycle

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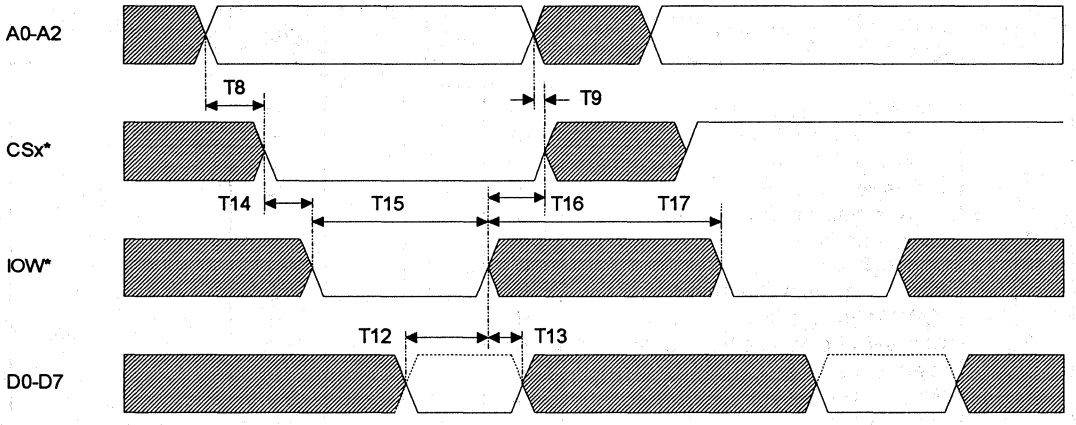
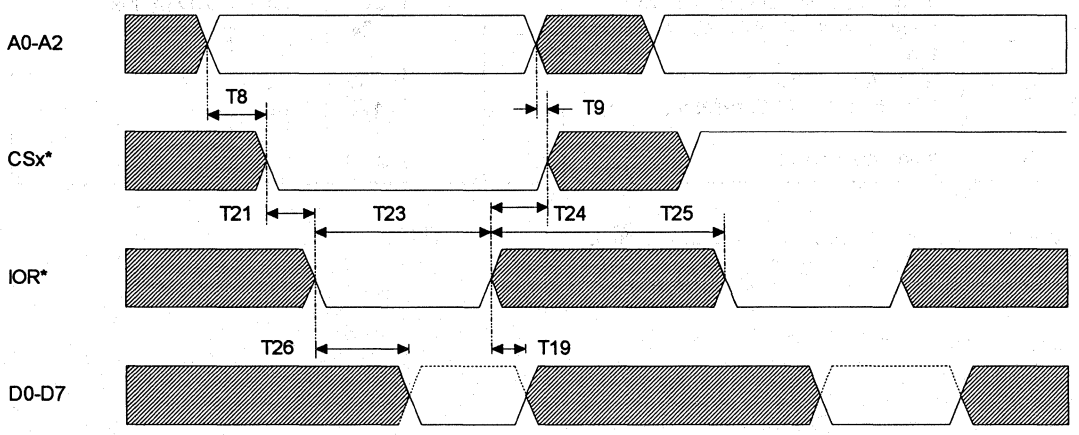
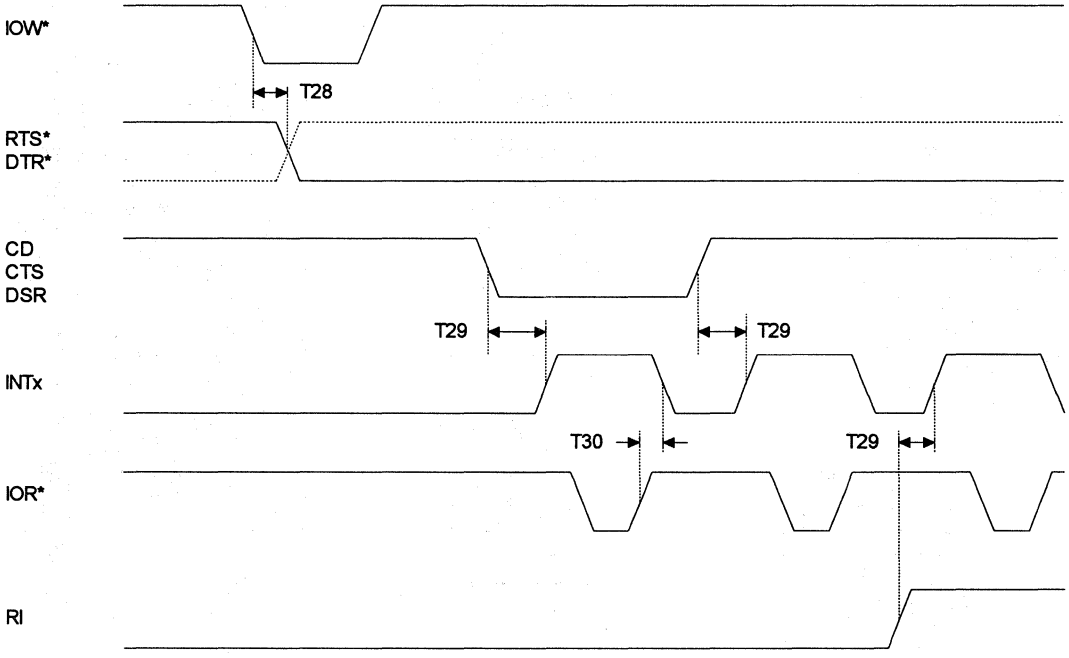
GENERAL WRITE TIMING



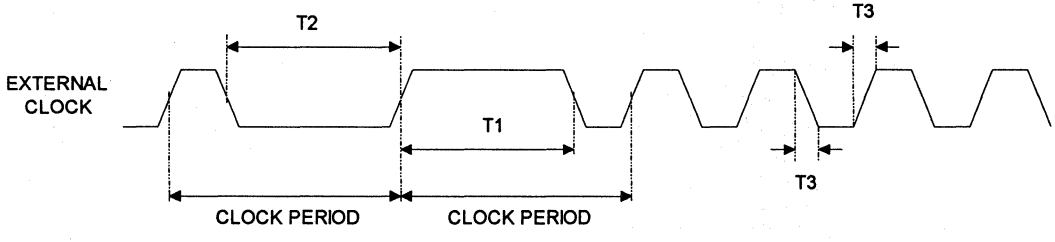
GENERAL READ TIMING



MODEM TIMING



CLOCK TIMING



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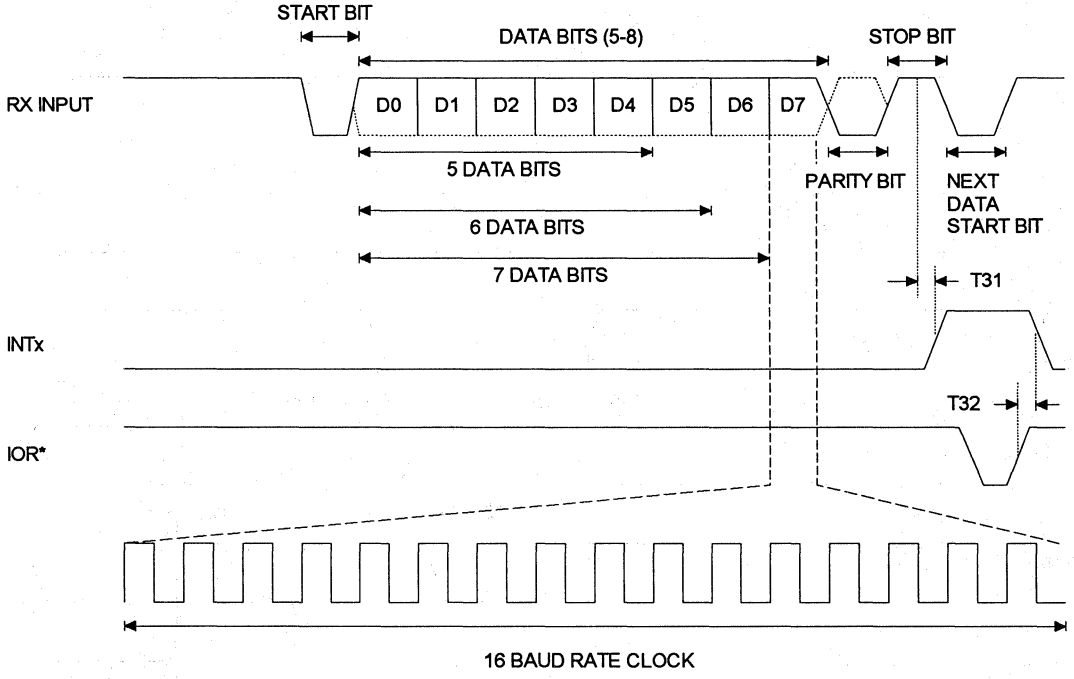
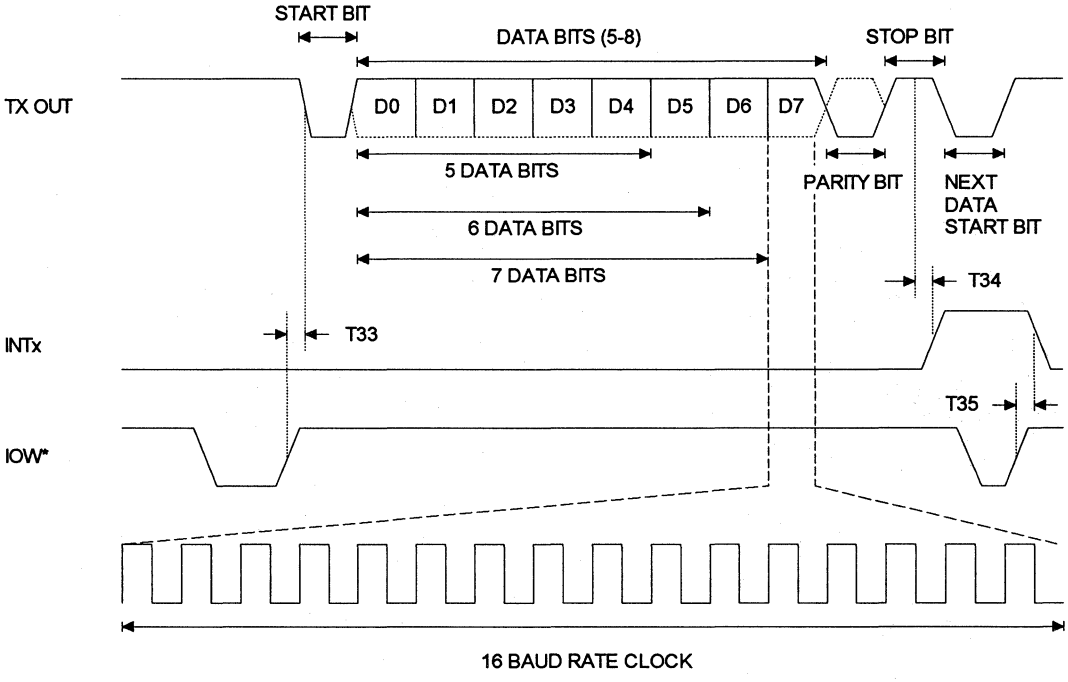
RECEIVE TIMING



TRANSMIT TIMING



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STARTECH

ST16C2450

Printed February 23, 1994

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

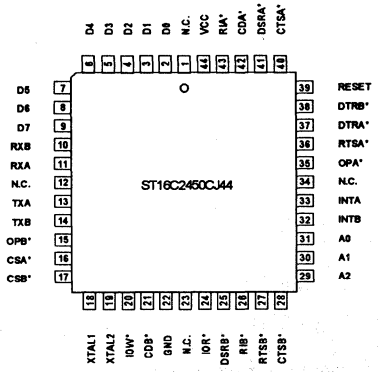
DESCRIPTION

The ST16C2450 is a dual universal asynchronous receiver and transmitter. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART section.

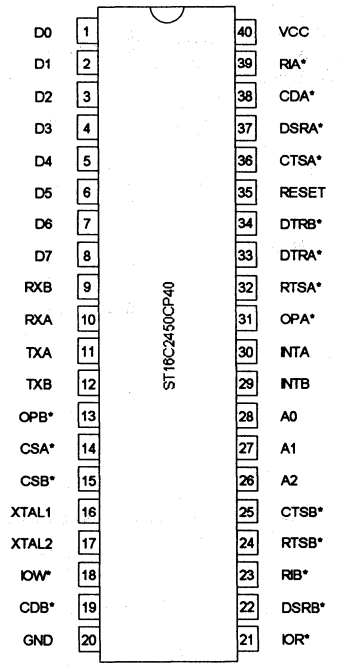
The ST16C2450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C2450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2450 provides internal loop-back capability for on board diagnostic testing.

The ST16C2450 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

- Functional compatible to NS16450, VL16C450, WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

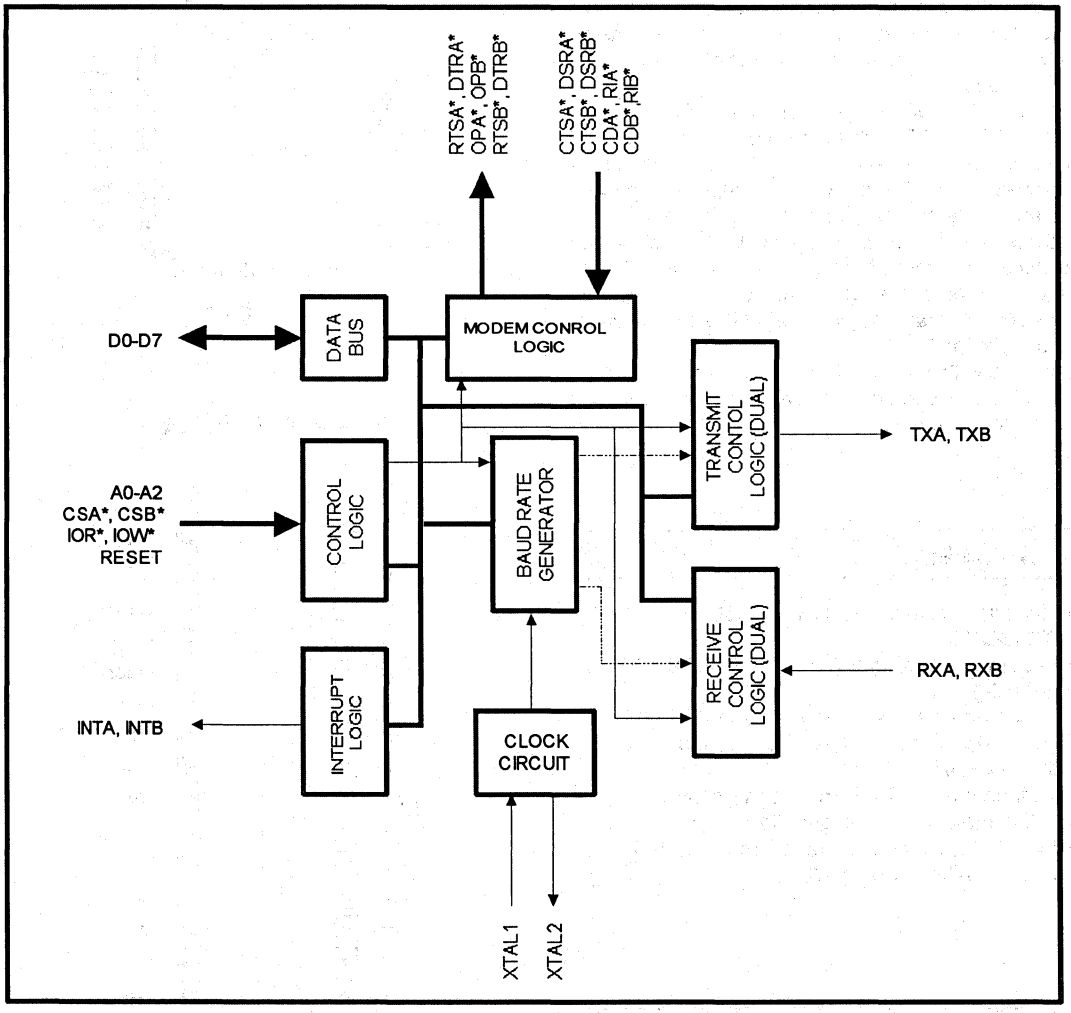
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2450CP40	Plastic-DIP	0° C to + 70° C
ST16C2450CJ44	PLCC	0° C to + 70° C

***Industrial operating range are available**

ST16C2450

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	10,9	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A/B*	14,15	I	Chip select A/B. (active low) A low at this pin enables the ST16C2450 / CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2450 data bus to the CPU.
A0-A2	28-26	I	Address select lines. To select internal registers.
INT A/B	30,29	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
OPA/B*	31,13	O	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
RTS A/B*	32,24	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A/B*	33,34	O	Data terminal ready A/B (active low). To indicate that ST16C2450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A/B*	36,25	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A/B*	37,22	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B*	38,19	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI A/B*	39,23	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
VCC	40	I	Power supply input.
GND	20	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

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ST16C2450 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2/ INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS A/B

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ST16C2450

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
not used except in local loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode and OP2* output to high.
1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and OP2*/INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C2450 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2450 has changed state since the last time it was read.

ST16C2450

MSR BIT-1:
Indicates that the DSR* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2*/INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state mode

SCRATCHPAD REGISTER (SR)

ST16C2450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signal

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	15			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C2450

ABSOLUTE MAXIMUM RATINGS

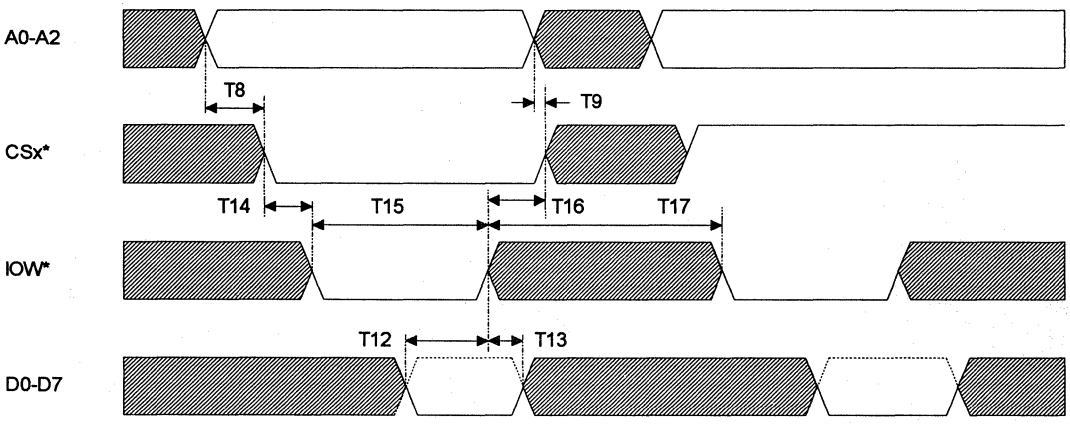
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

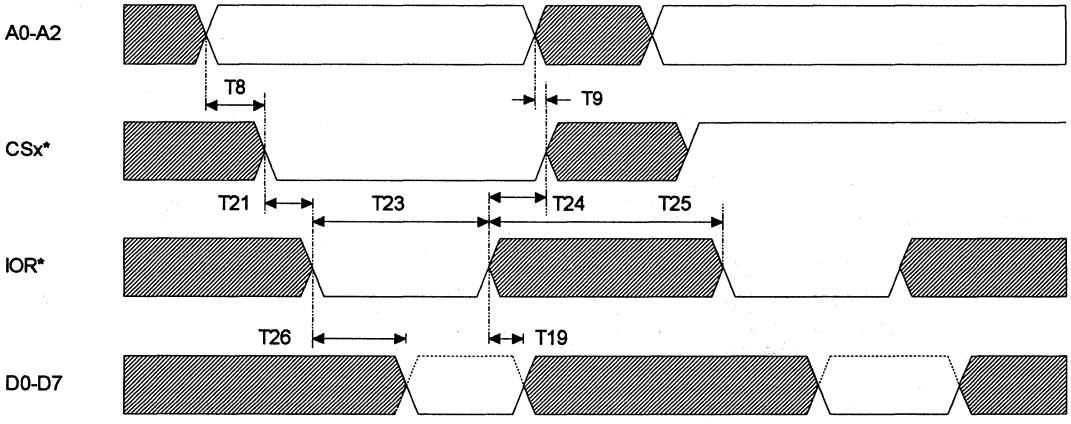
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING



GENERAL READ TIMING



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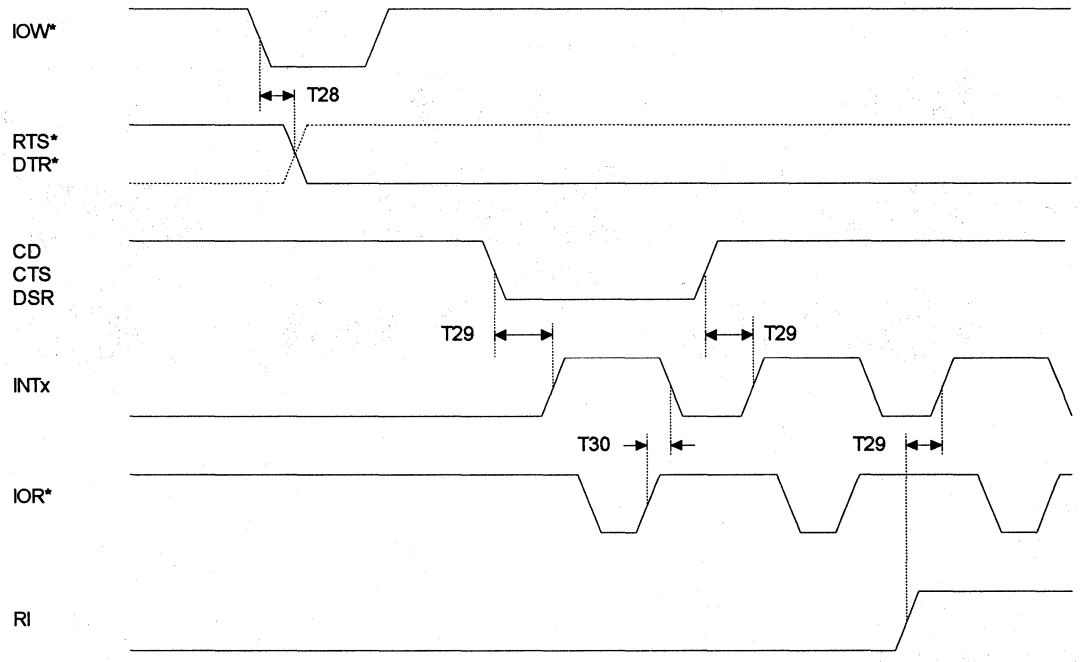
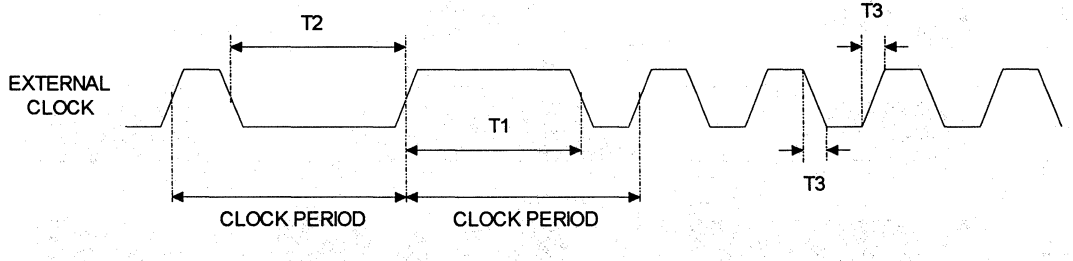
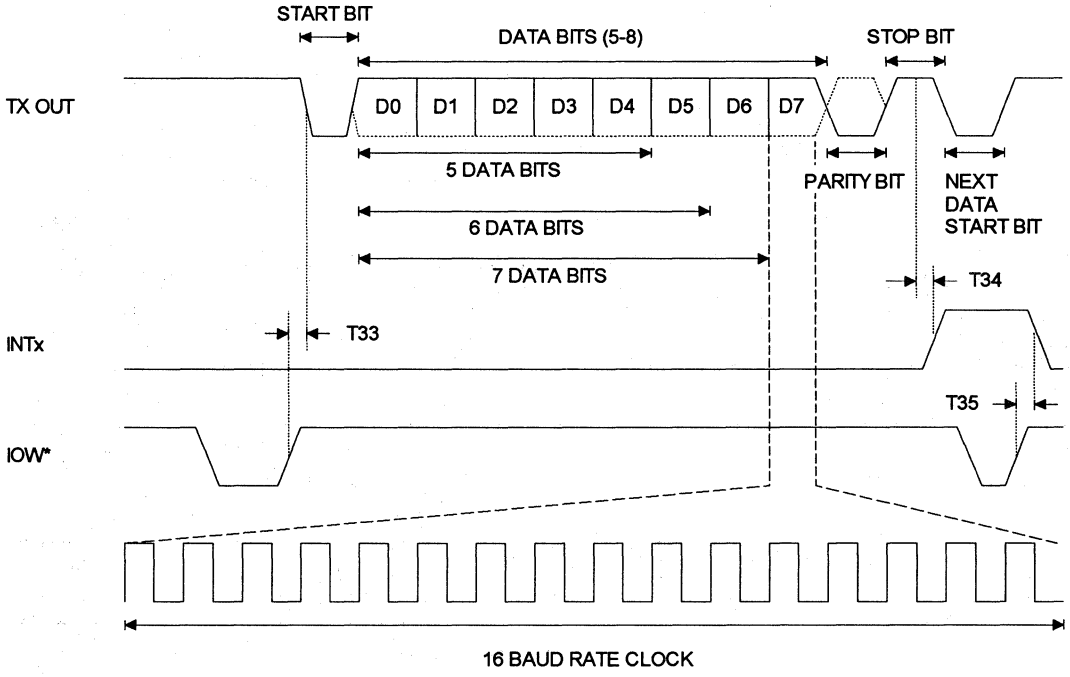
MODEM TIMING



CLOCK TIMING



TRANSMIT TIMING



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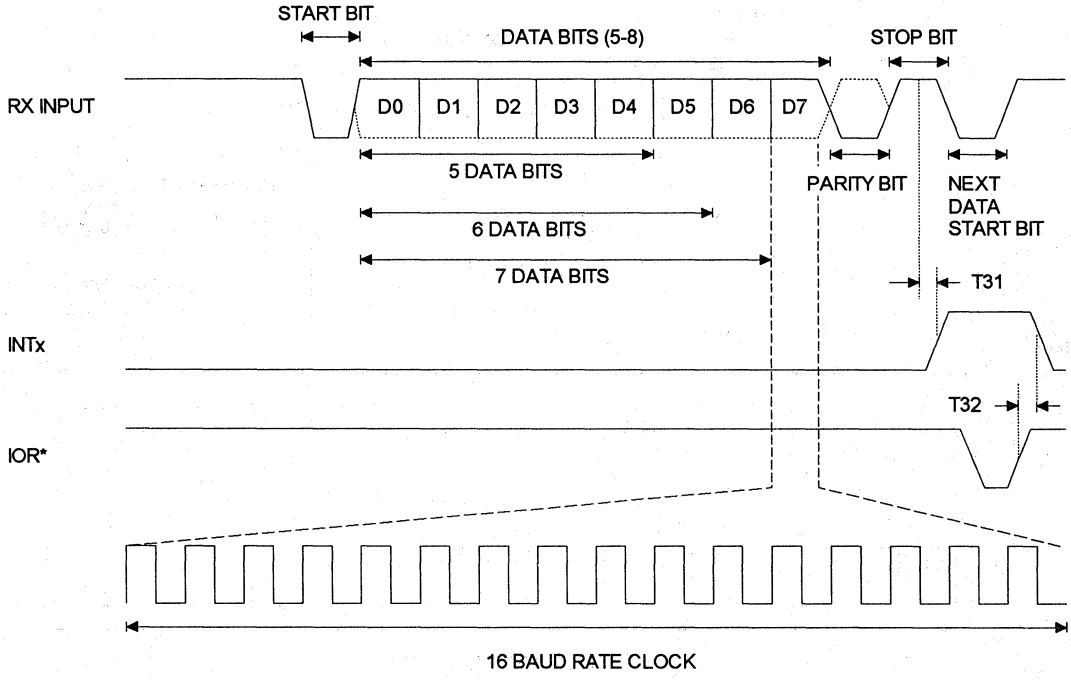
RECEIVE TIMING



STARTECH

ST16C454

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

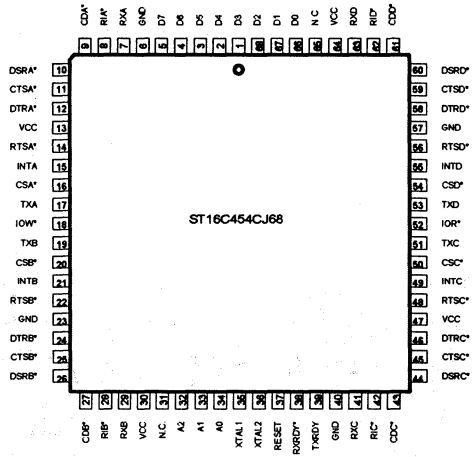
DESCRIPTION

The ST16C454 is a quad universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C454 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C454 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C454 provides internal loop-back capability for on board diagnostic testing.

The ST16C454 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



3

FEATURES

- Quad ST16C450
- Pin-to-pin compatible to ST16C554
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C454CJ68	PLCC	0° C to + 70° C
ST16C454IJ68	PLCC	-40° C to + 85° C

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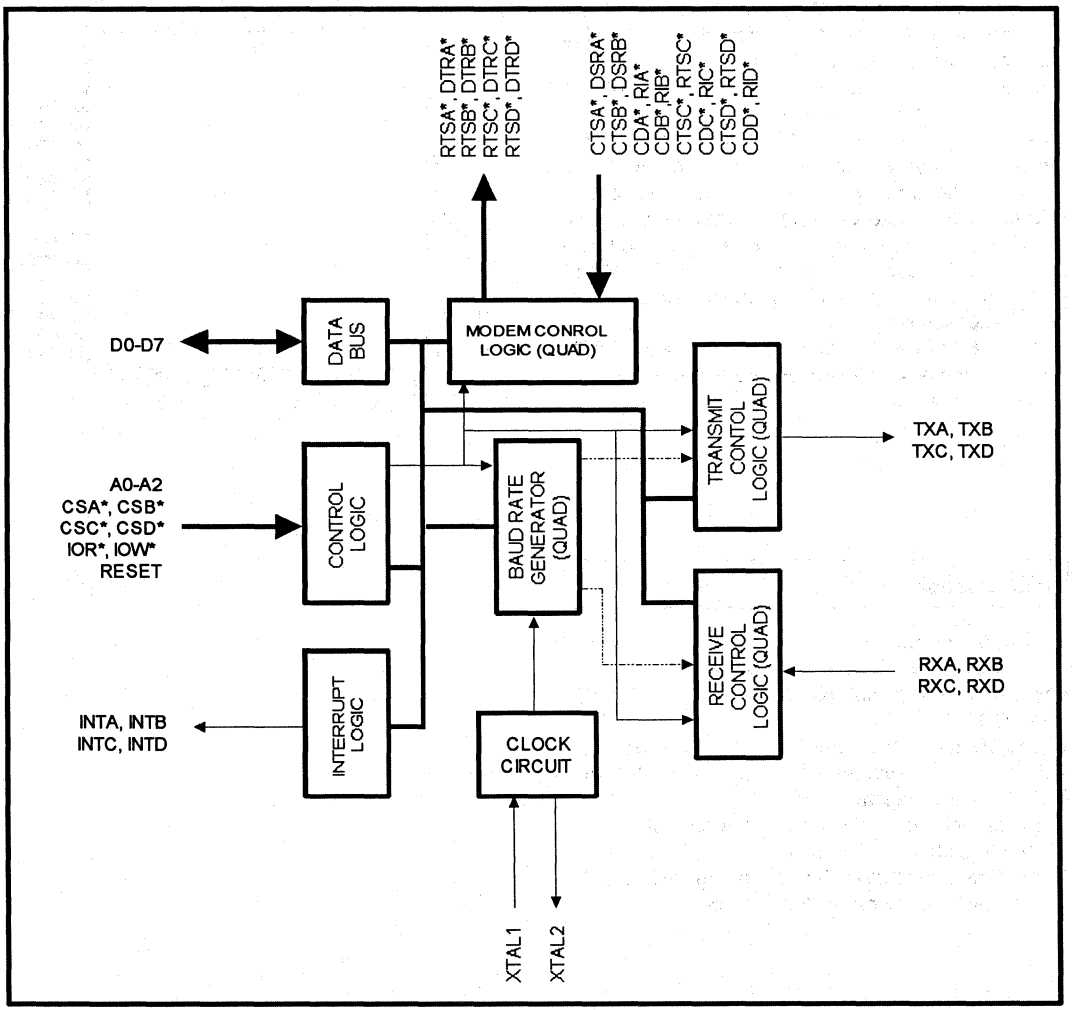
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input. The serial information (data) received from serial port to ST16C454 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A-B* CS C-D*	16,20 50,54	I	Chip select (active low). A low at this pin enables the ST16C454 / CPU data transfer operation. Each UART section of the ST16C454 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	O	Signal and power ground.
IOR*	52	I	Read strobe (active low.) A low level on this pin transfers the contents of the ST16C454 data bus to the CPU.
RXRDY*	38	O	Receive data ready (active low). This pin is the inverted output of internally "or-ed" four received data (LSR Bit-0) bits. Goes low when one of the UART's contains data in the receive holding register.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
TXRDY	39	O	Transmit ready (active high). This pin is the output of internally "or-ed" four transmit empty signals (LSR Bit-6). This pin stays low when all four transmitters are empty.
A2	32	I	Address select line 2. To select internal registers.
A1	33	I	Address select line 1. To select internal registers.
A0	34	I	Address select line 0. To select internal registers.
INT A-B INT C-D	15,21 49,55	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS A-B* RTS C-D*	14,22 48,56	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A-B* DTR C-D*	12,24 46,58	O	Data terminal ready. (active low) To indicate that ST16C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A-B* CTS C-D*	11,25 45,59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DSR A-B*	10,26		
DSR C-D*	44,60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A-B*	9,27		
CD C-D*	43,61	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI A-B*	8,28		
RI C-D*	42,62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	13,30		
VCC	47,64	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

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ST16C454 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C454 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

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ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except, in internal loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C454 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C454 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C454 has changed state since the last time it was read.

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MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C454 provides a temporary data register to store 8 bits of information for variable use.

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state
RxRdy*	High
TxRdy	Low

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
MSR	BITS 4-7=input signals

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	15			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

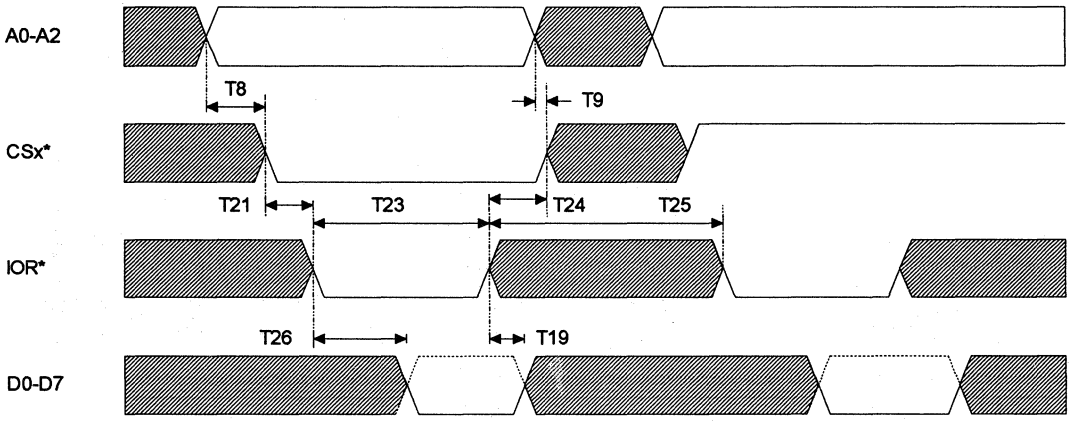
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

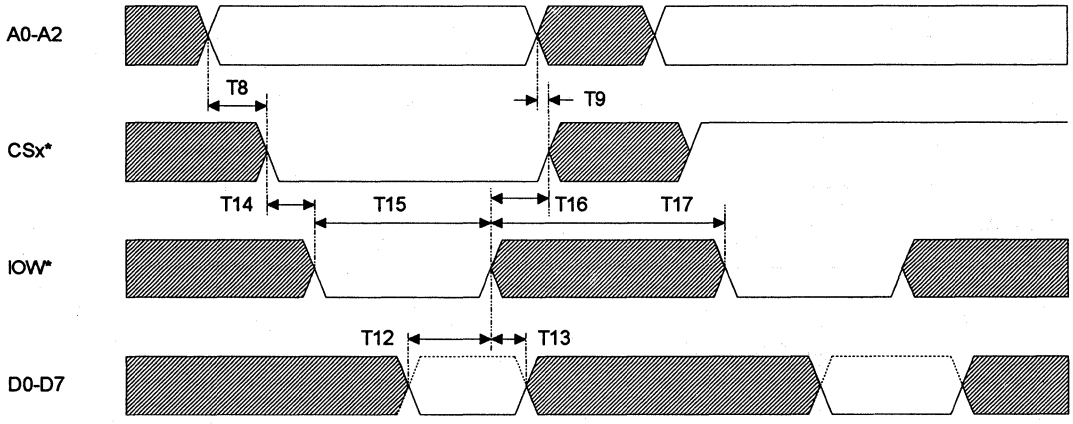
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL READ TIMING



GENERAL WRITE TIMING



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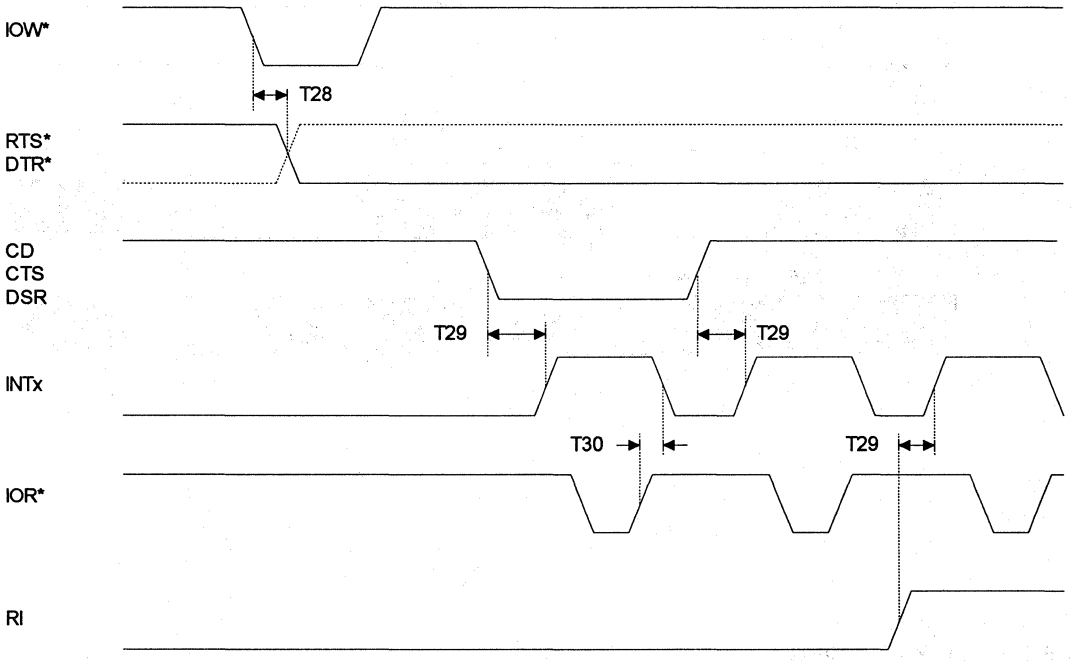
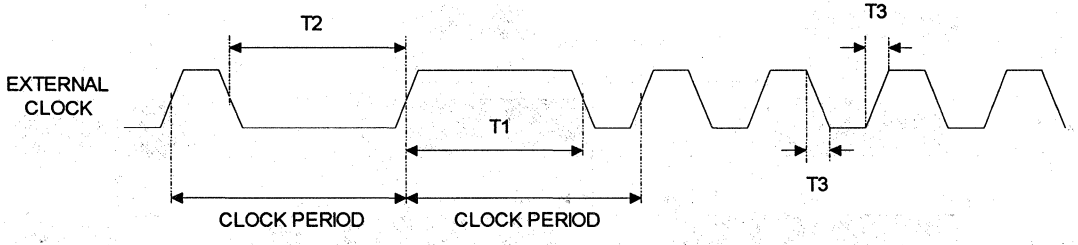
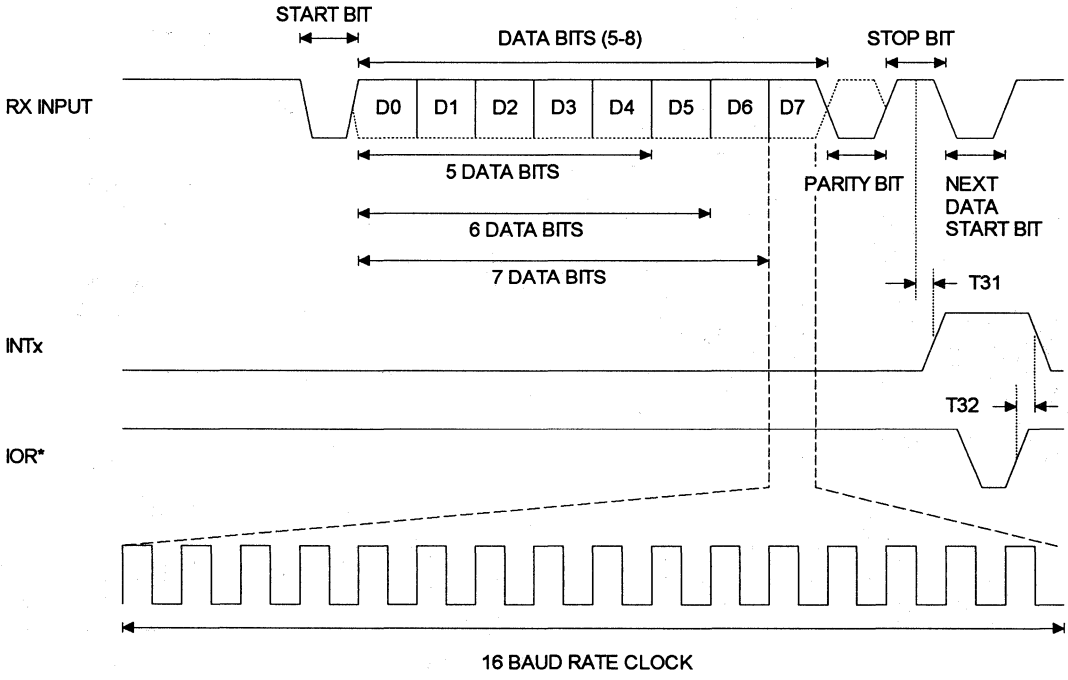
MODEM TIMING



CLOCK TIMING



RECEIVE TIMING



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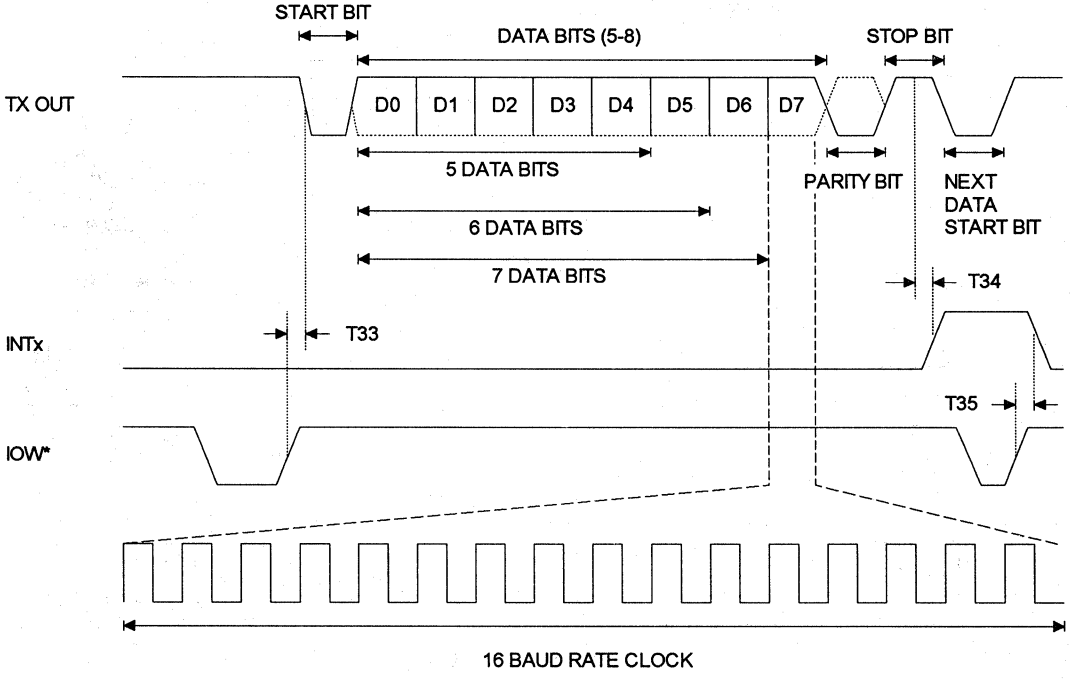
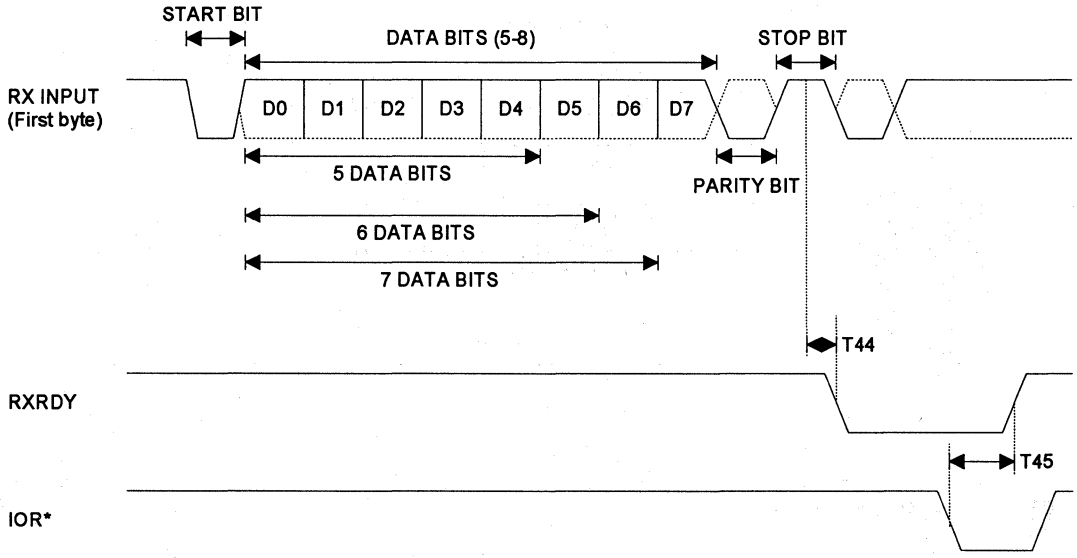
TRANSMIT TIMING



RXRDY TIMING



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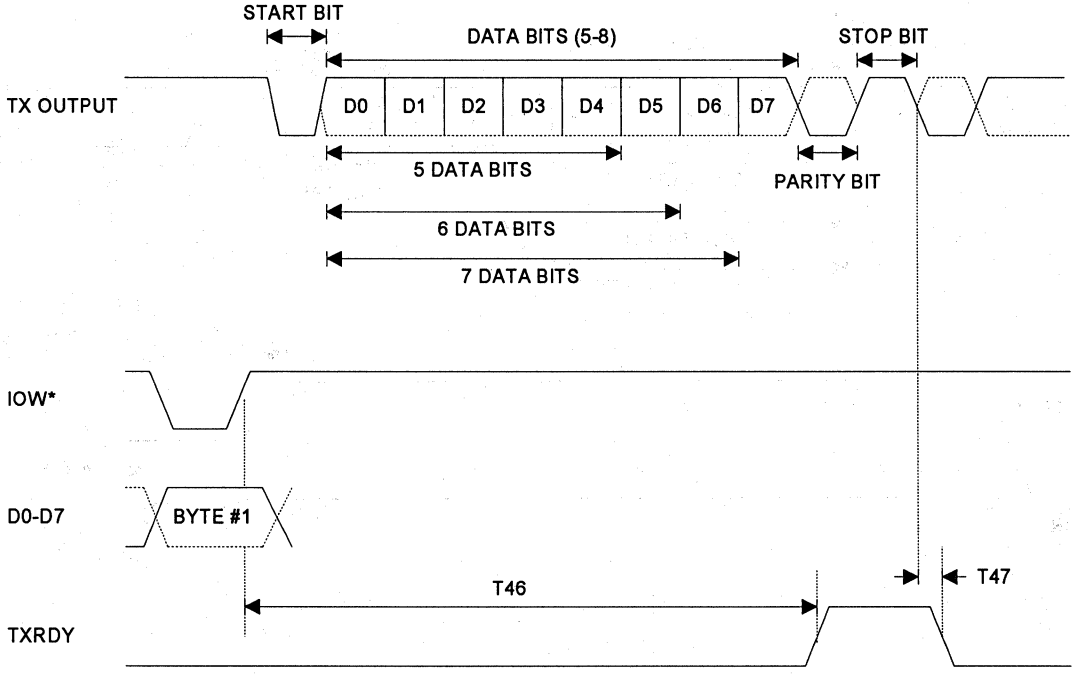
TXRDY TIMING



STARTECH

ST68C454

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

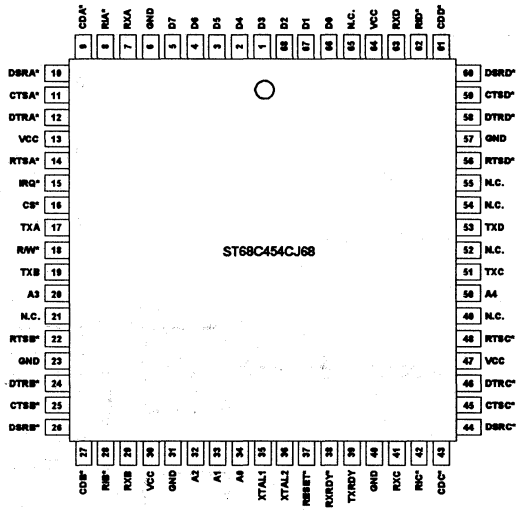
DESCRIPTION

The ST68C454 is a quad universal asynchronous receiver and transmitter with modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST68C454 is an improved, quad version of the NS16450 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C454 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C450
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C454CJ68	PLCC	0° C to +70° C
ST68C454IJ68	PLCC	-40° C to +85° C

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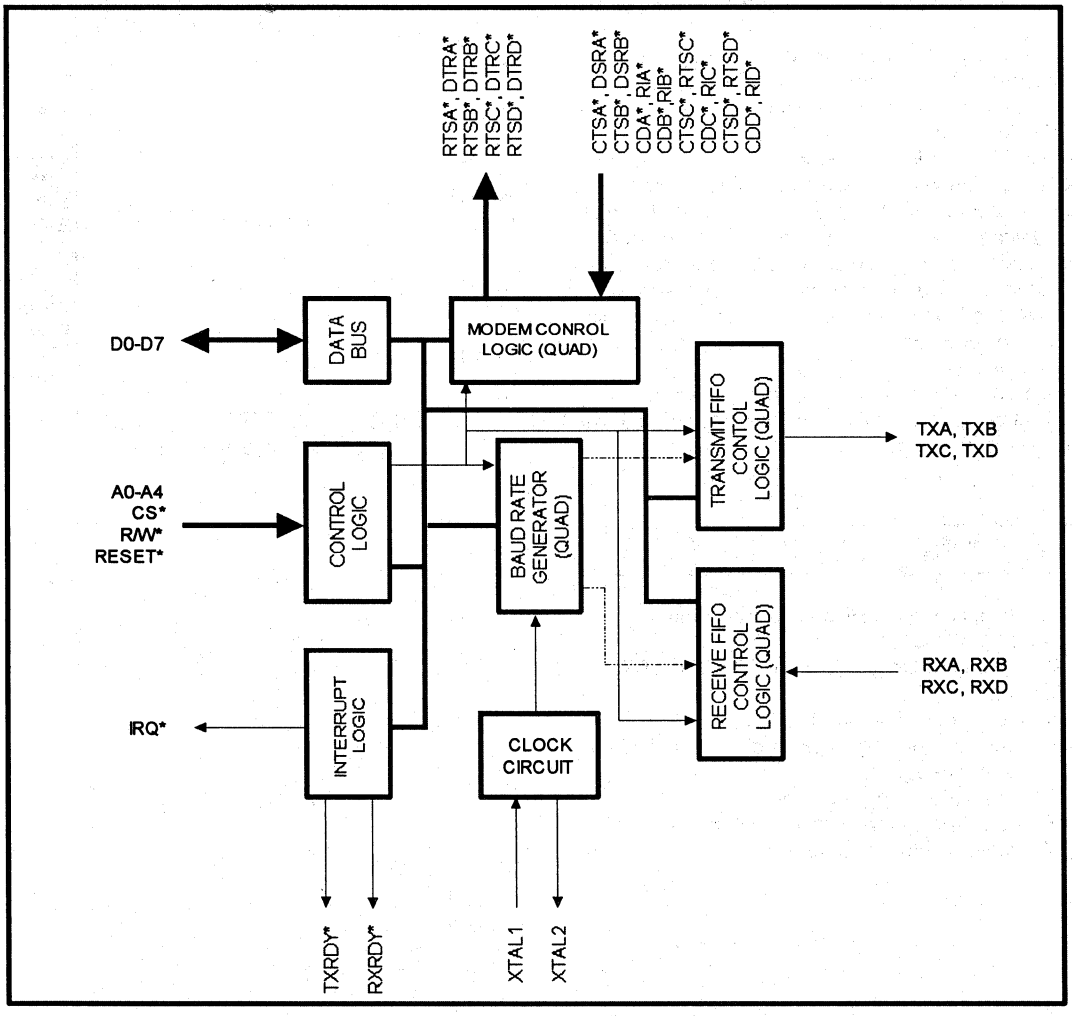
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66	I/O	Bi-directional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B RX C/D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST68C454 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B TX C/D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	16	I	Chip select (active low). A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	I	Crystal input 2. See XTAL1.
R/W*	18	I	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C454 data bus to the CPU.
CD A/B* CD C/D*	9,27 43,61	I	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23,31 40,57	O	Signal and power ground.
DSR A/B* DSR C/D*	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
RI A/B* RI C/D*	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTS A/B* RTS C/D*	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS A/B* CTS C/D*	11,25 45,59	I	Clear to send A-D. (active low) The CTS* signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmitter output.
RXRDY*	38	O	Receive data ready (active low). This pin is the inverted output of internally "or-ed" four received data (LSR Bit-0) bits. Goes low when one of the UART's contains data in the receive holding register.
TXRDY	39	O	Transmit ready (active high). This pin is the output of internally "or-ed" four transmit empty signals (LSR Bit-6). This pin stays low when all four transmitters are empty.
A4	50	I	Address line 4. To select one of the four UARTS.
A3	20	I	Address line 3. To select one of the four UARTS.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
IRQ*	15	O	Interrupt output. (active low open collector) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DTR A/B* DTR C/D*	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that ST68C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET*	37	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.

SERIAL PORT SELECTION GUIDE

CS*	A4	A3	UART X
1	X	X	X
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

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PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

PROGRAMMABLE BAUD RATE GENERATOR

The ST68C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D

The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the IRQ* output pin.

IER BIT-0:
0=disable the receiver ready interrupt
1=enable the receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable the modem status register interrupt
1=enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST68C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C454 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set zero.

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.

0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

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LCR BIT-6:
Break control bit.
1=forces the transmitter output (TX A-D) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high
1=force DTR* output to low

MCR BIT-1:
0=force RTS* output to high
1=force RTS* output to low

MCR BIT2-3:
x=not used

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D*, DSR A-D*, CD A-D*, and RI A-D*) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D*, RTS A-D* and MCR A-D bit2,3 are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST68C454 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used, set to "0".

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed

information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST68C454 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loop-back mode. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D
ST68C454 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16xCLOCK %ERROR	DVISOR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST68C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
RTS A-D*	High
DTR A-D*	High
IRQ	Three state mode
RXRDY*	High
TXRDY	Low

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ST68C454 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	Not used	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time from write or CS*	15			ns	
T_{14}	Write set up time	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	15			ns	
T_{17}	Write cycle delay	45			ns	
T_{18}	Data setup time	15			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{24}	Data hold time	0			ns	
T_{25}	Read cycle delay	25			ns	
Tr	Read cycle=T_{18}+T_{25}	105			ns	
T_{27}	Chip select pulse width	75			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			35	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from Read to reset RxRdy			1	µs	
T_{46}	Delay from Write to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

* = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

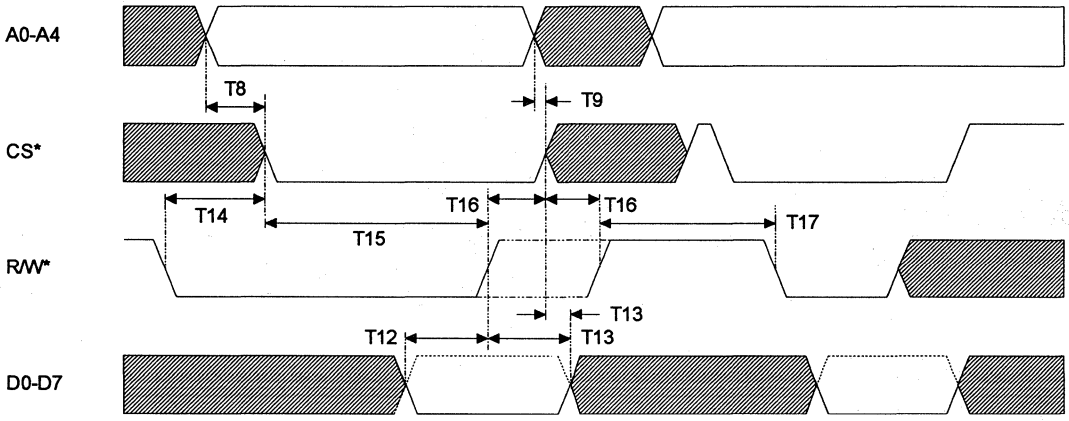
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

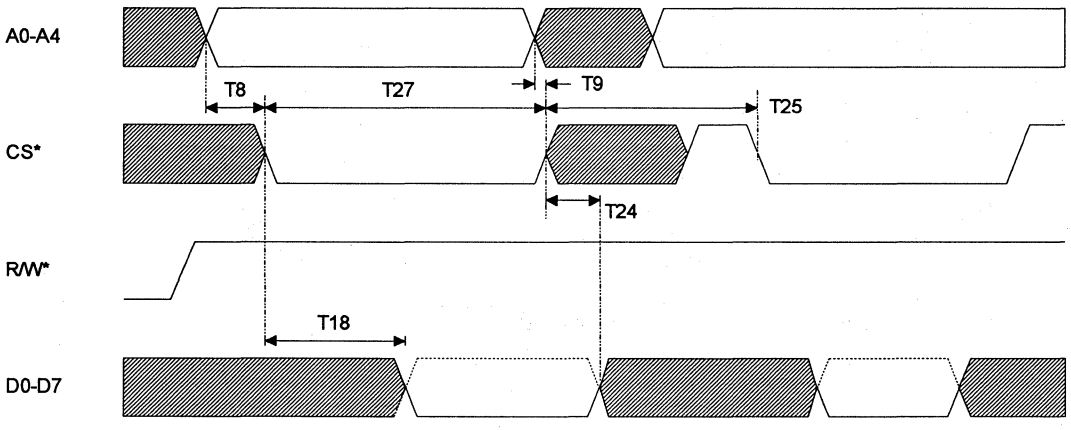
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING



GENERAL READ TIMING



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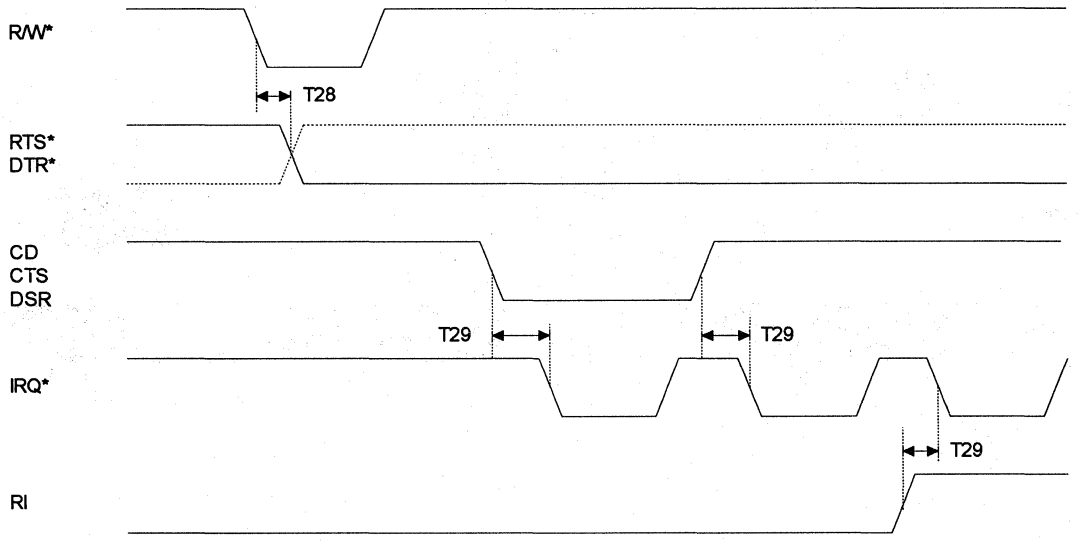
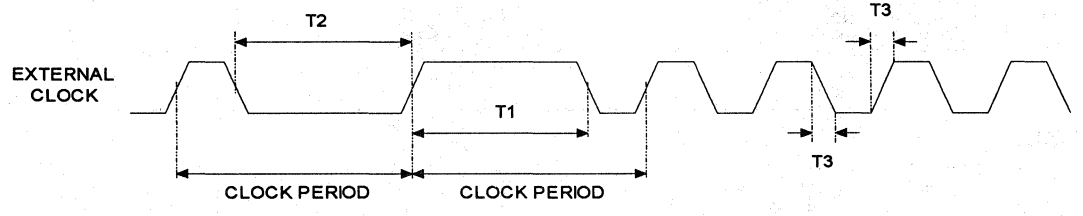
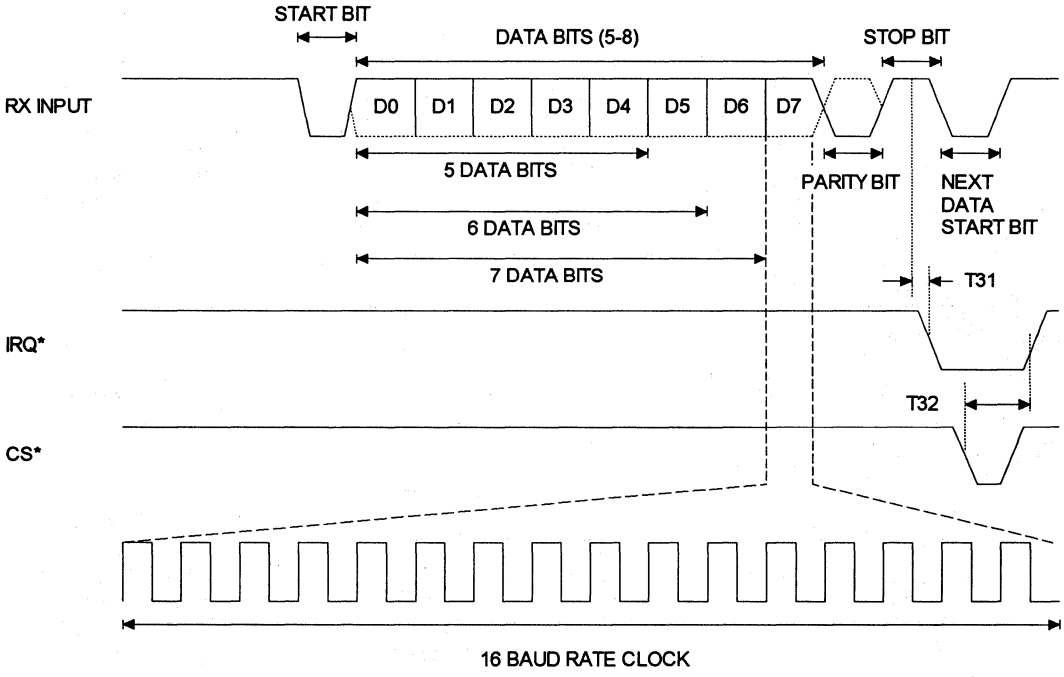
MODEM TIMING



CLOCK TIMING



RECEIVE TIMING



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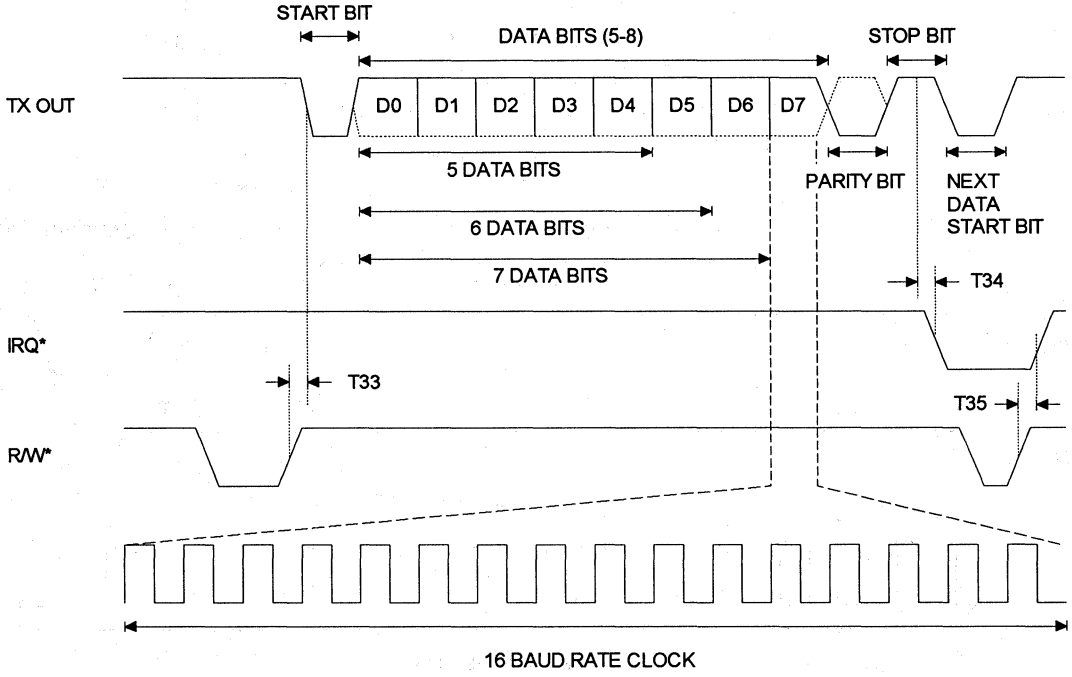
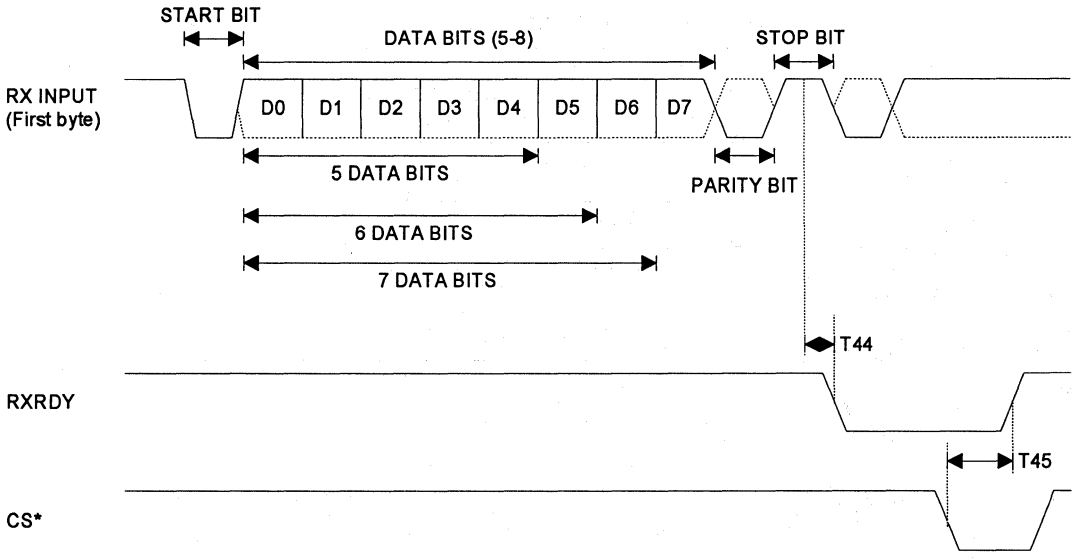
TRANSMIT TIMING



RXRDY TIMING



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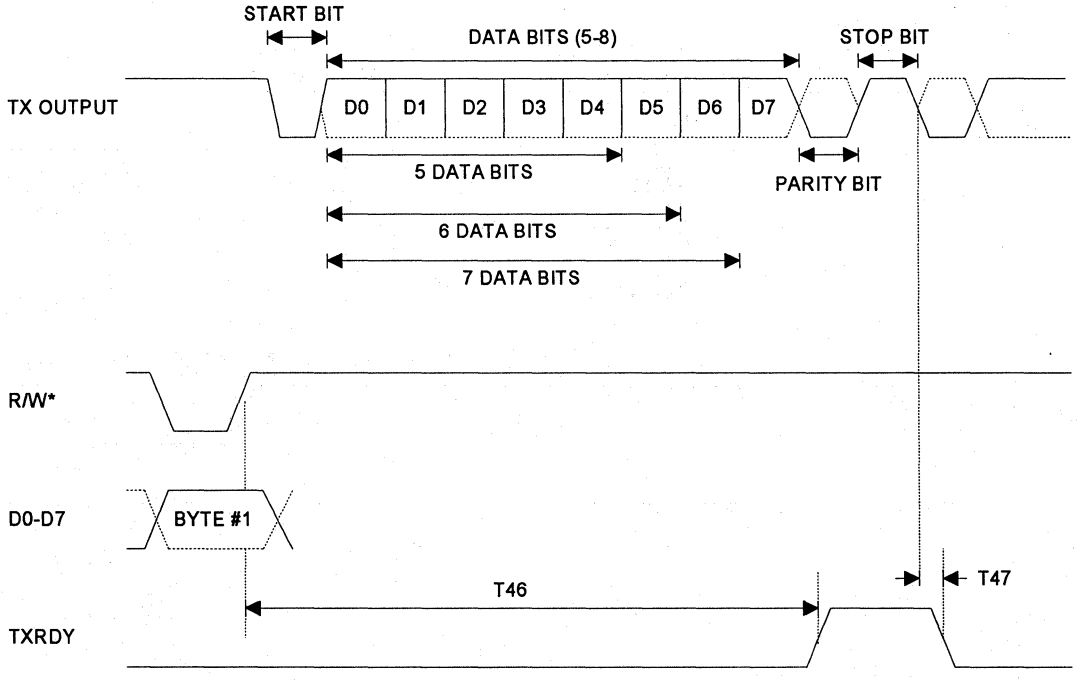
TXRDY TIMING



STARTECH

ST16C550

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

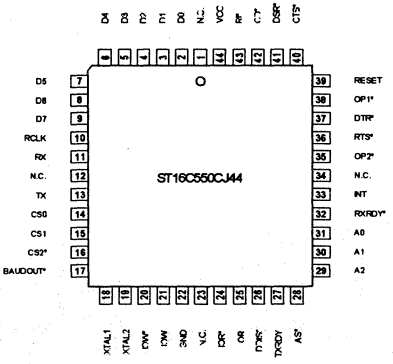
DESCRIPTION

The ST16C550 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

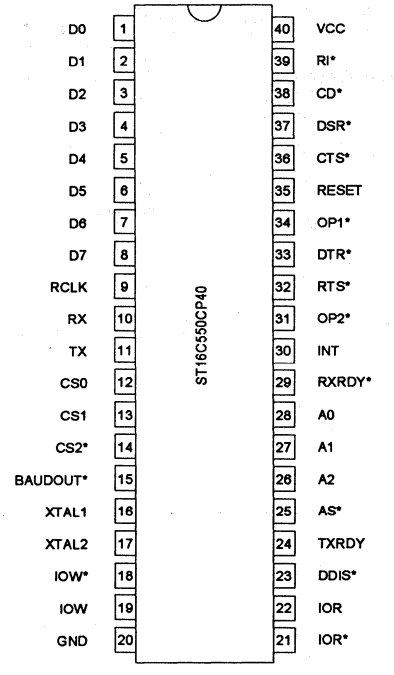
The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loop-back capability for on board diagnostic testing.

The ST16C550 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

- Pin to pin and functional compatible to NS16550,VL16C550,WD16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C450
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C550CP40	Plastic-DIP	0° C to + 70° C
ST16C550CJ44	PLCC	0° C to + 70° C
ST16C550CQ52	QFP	0° C to + 70° C
ST16C550CQ48	TQFP	0° C to + 70° C

***Industrial operating range are available**

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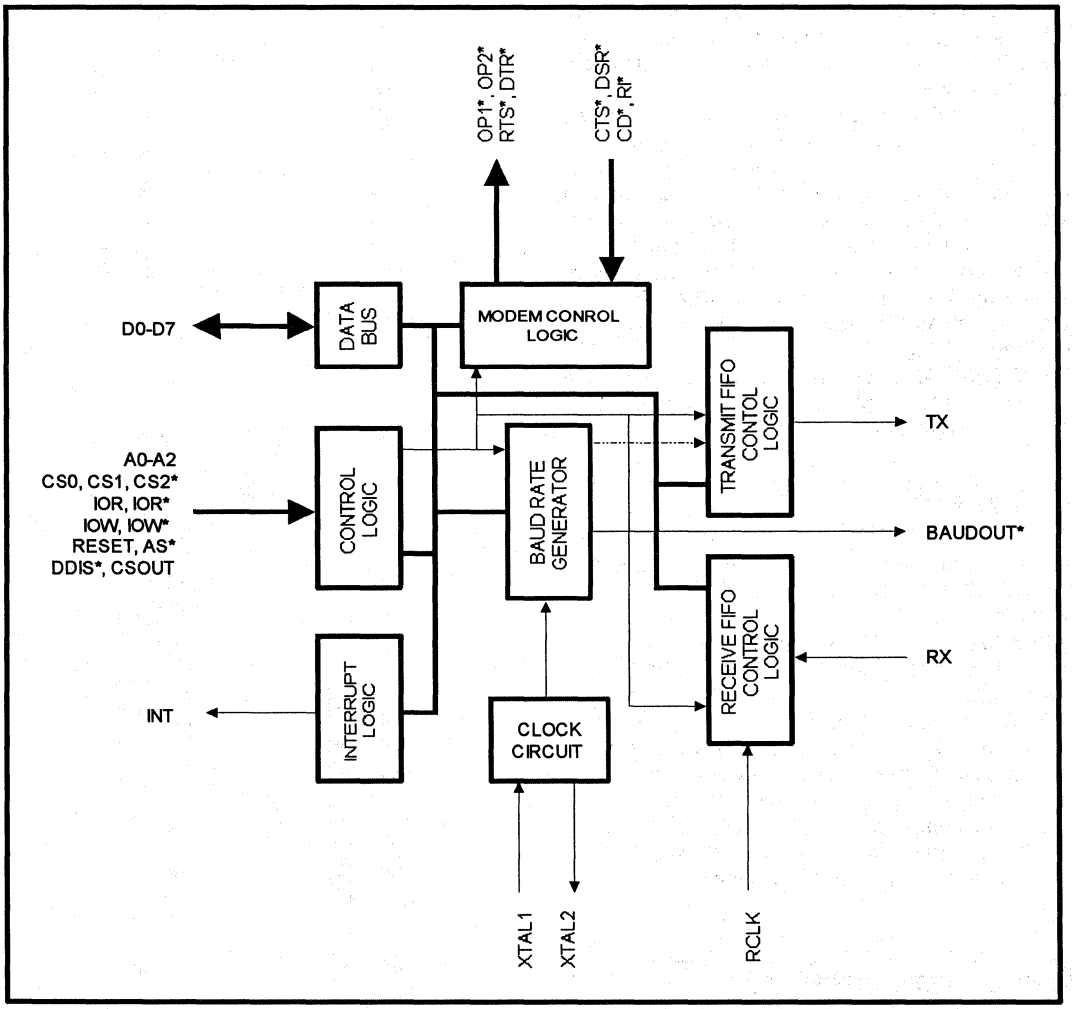
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the ST16C550 receiver section if receiver data rate is different from transmitter data rate.
RX	10	I	Serial data input. The serial information (data) received from serial port to ST16C550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
CS2*	14	I	Chip select 3. (active low) A low at this pin (while CS0=1 and CS1=1) will enable the ST16C550 / CPU data transfer operation.
BAUDOUT*	15	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide receive clock.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	Write strobe. (active high) Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C550 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	O	Signal and power ground.
IOR*	21	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C550 data bus to the CPU.
IOR	22	I	Read strobe. (active high) Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C550 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23	O	Drive disable. (active low) This pin goes low when the CPU is reading data from the ST16C550 to disable the external transceiver or logic's.
TXRDY	24	O	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.
AS*	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	I	Address select line 2. To select internal registers.
A1	27	I	Address select line 1. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A0	28	I	Address select line 0. To select internal registers.
RXRDY*	29	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register (MCR bit-3).
RTS*	32	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	O	Data terminal ready. (active low) To indicate that ST16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DSR*	37	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	38	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI*	39	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example-A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

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1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:
0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive

holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
RXRDY*	High
TXRDY	Low
INT	Low

ST16C550

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select	10		25	ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load

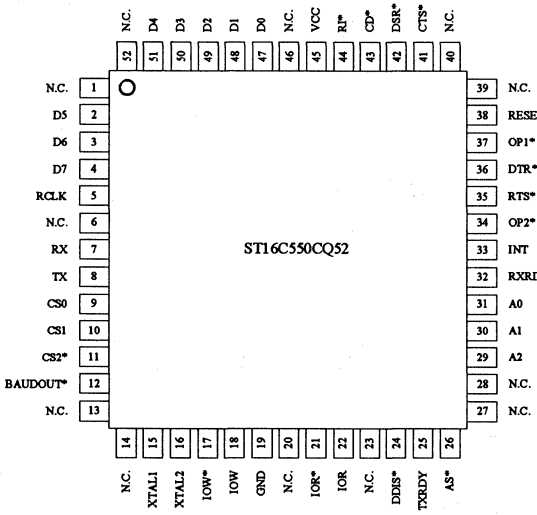
AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

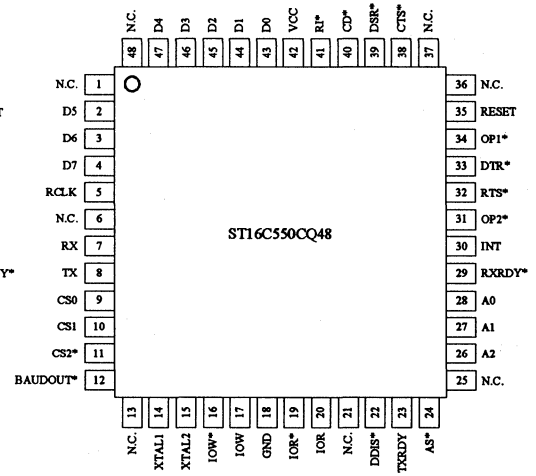
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{RClk}		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low
* = Baudout* cycle

52 Pin QFP Package



48 Pin TQFP Package



ST16C550

ABSOLUTE MAXIMUM RATINGS

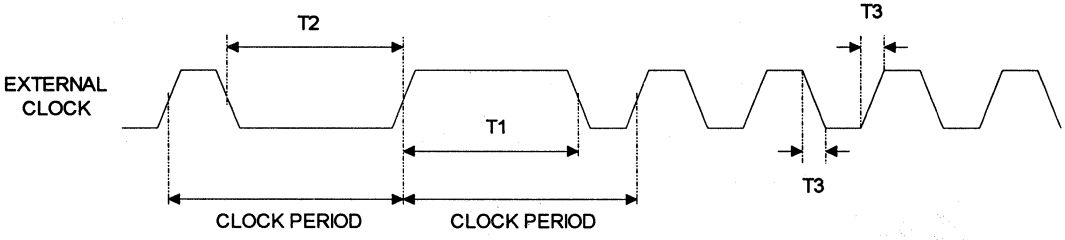
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

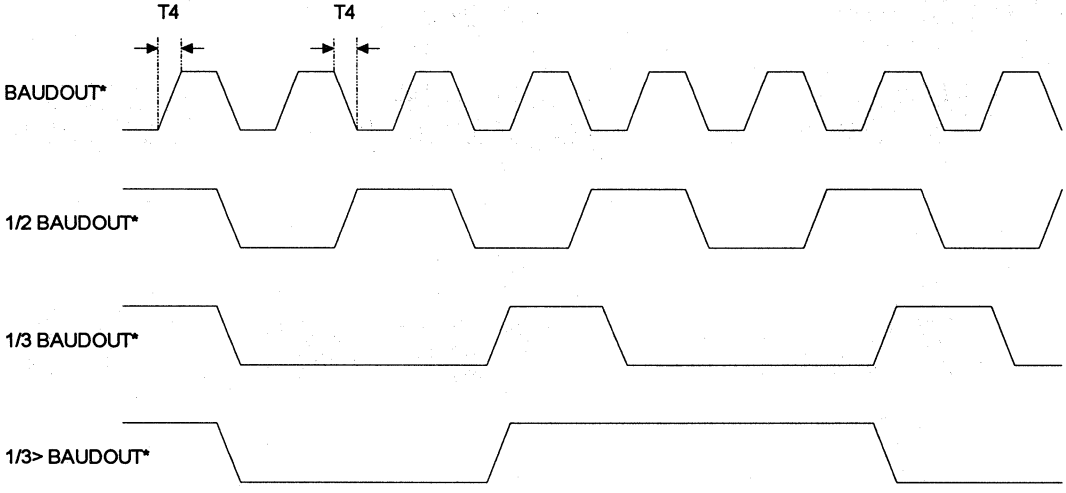
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

CLOCK TIMING

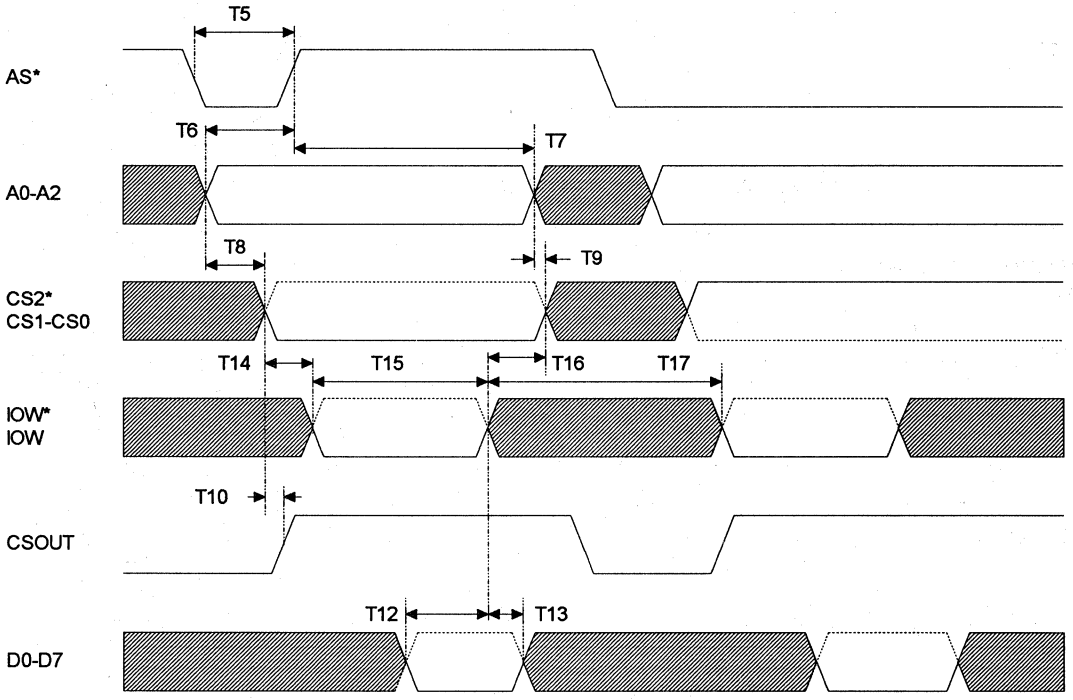


BAUDOUT* TIMING

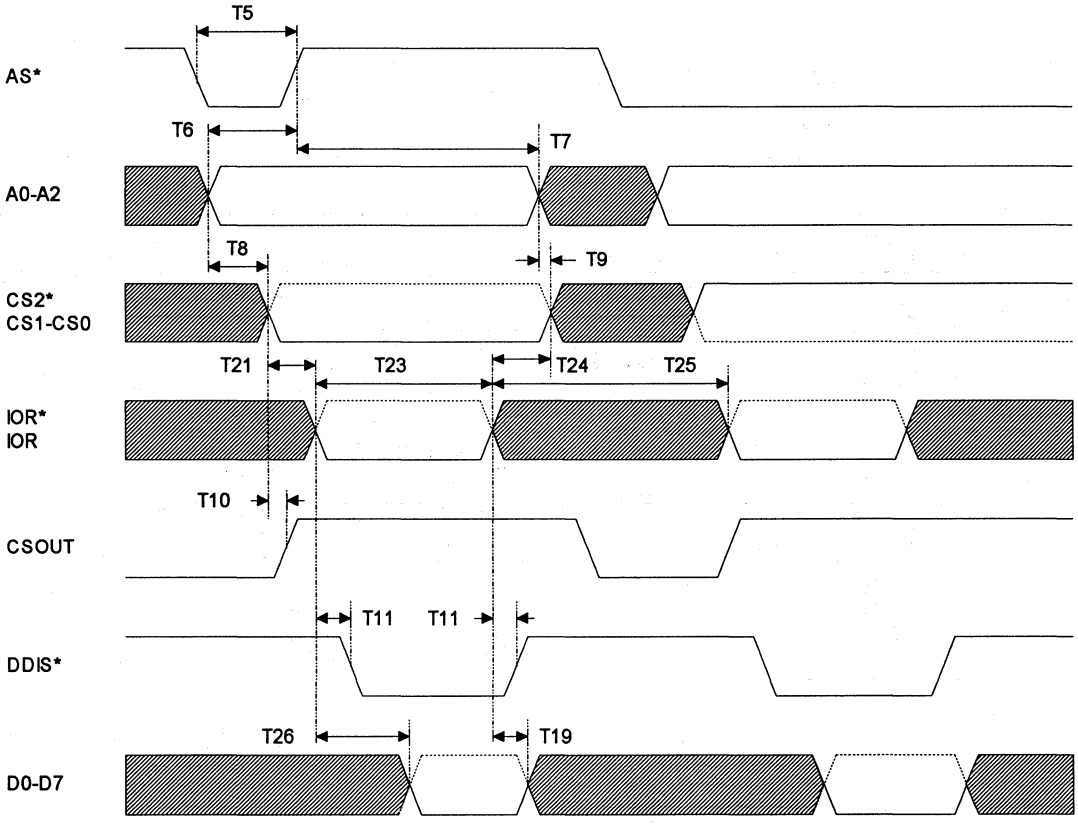


ST16C550

GENERAL WRITE TIMING

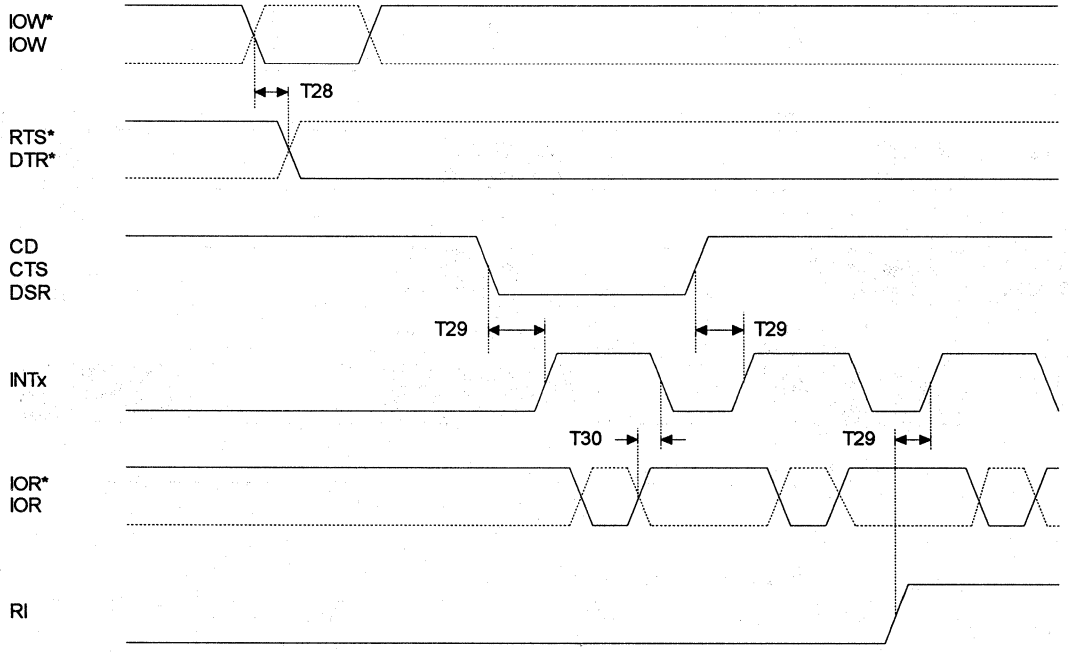


GENERAL READ TIMING

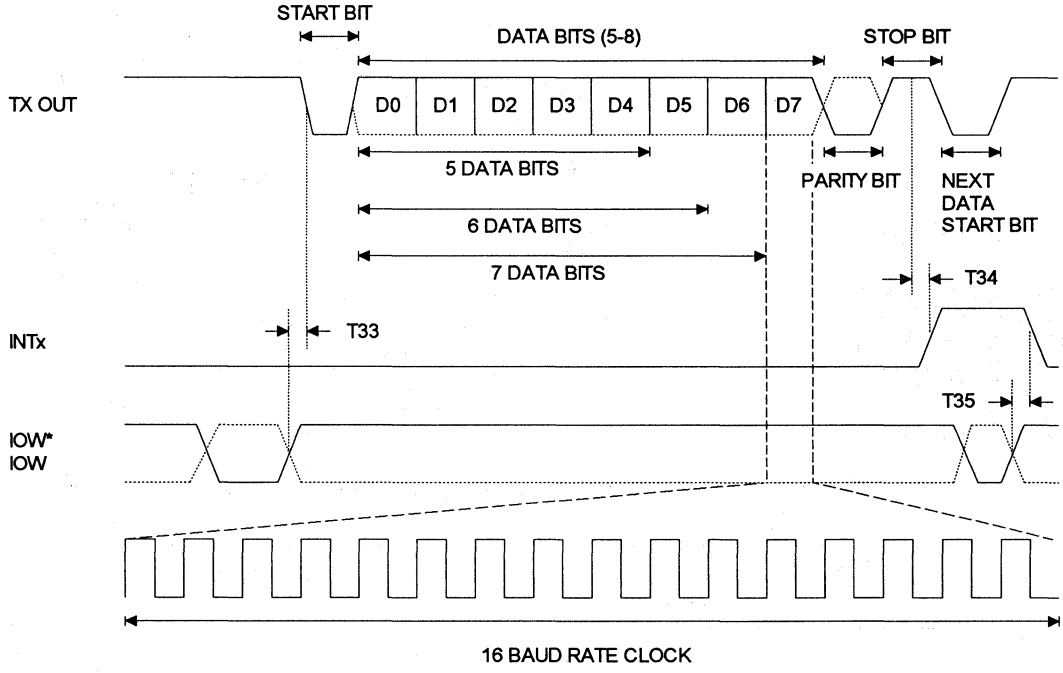


ST16C550

MODEM TIMING

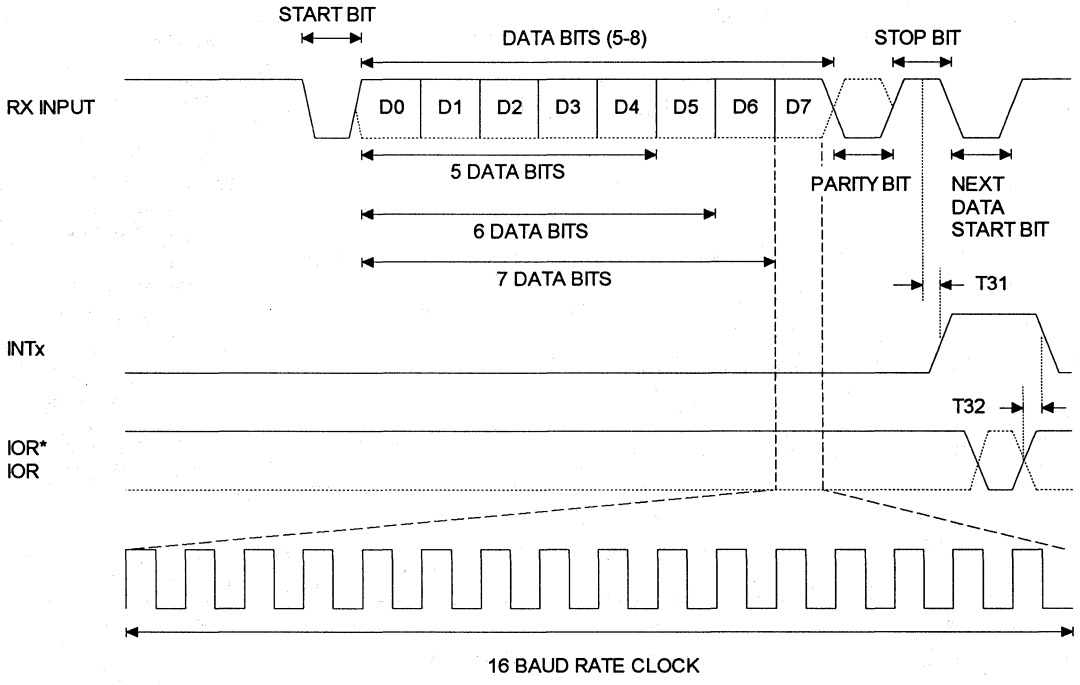


TRANSMIT TIMING

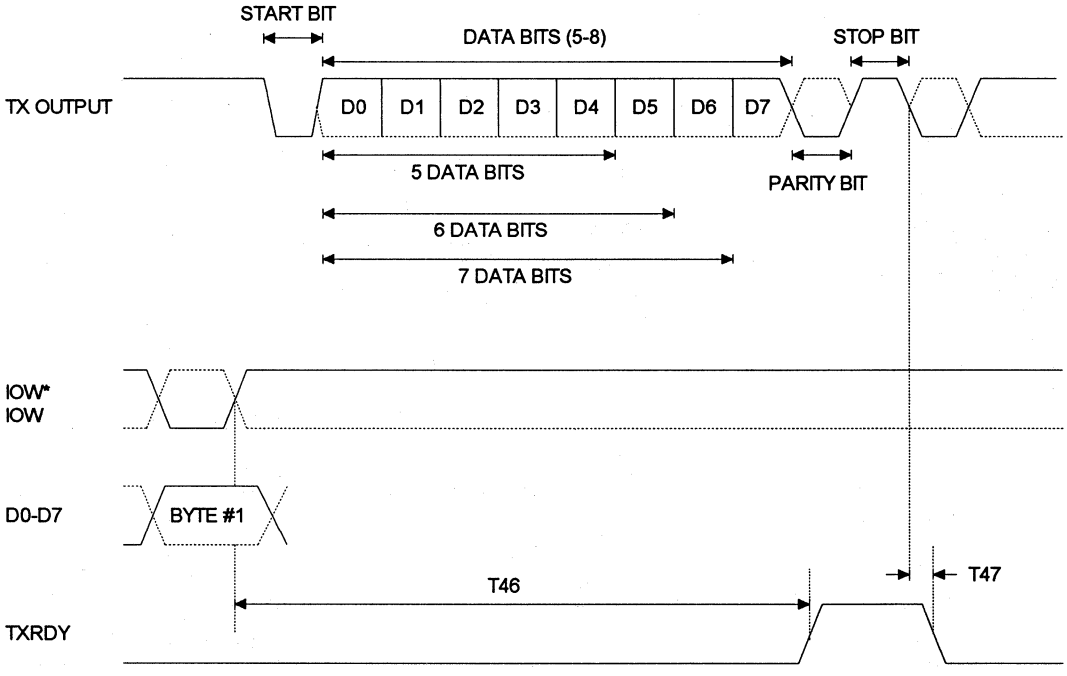


ST16C550

RECEIVE TIMING

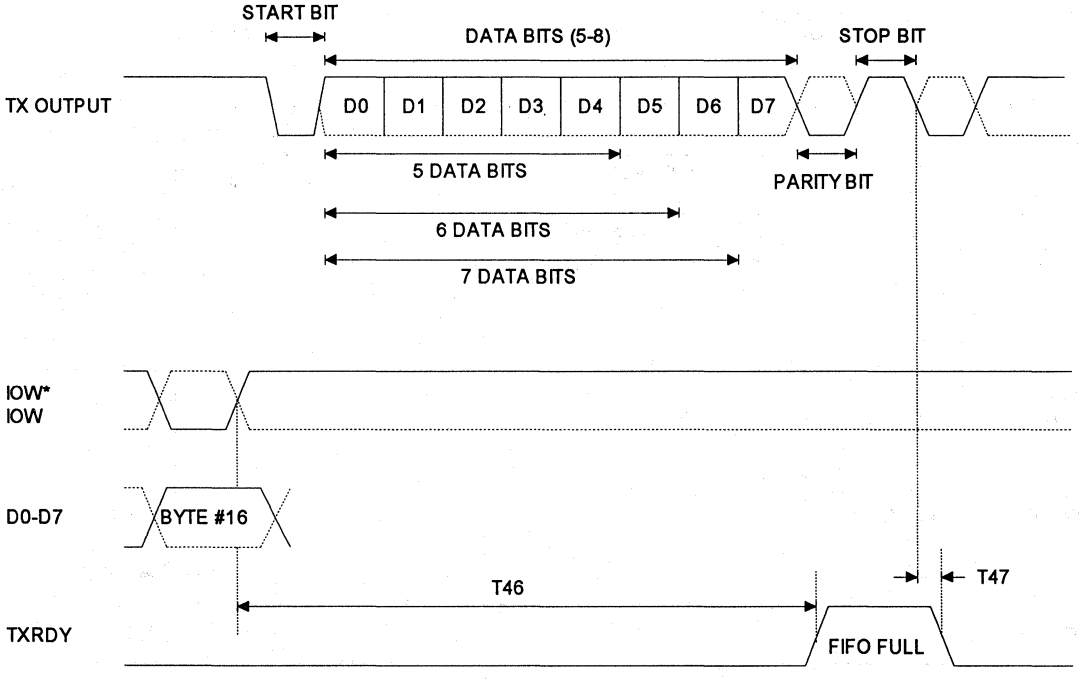


TXRDY TIMING FOR MODE "0"

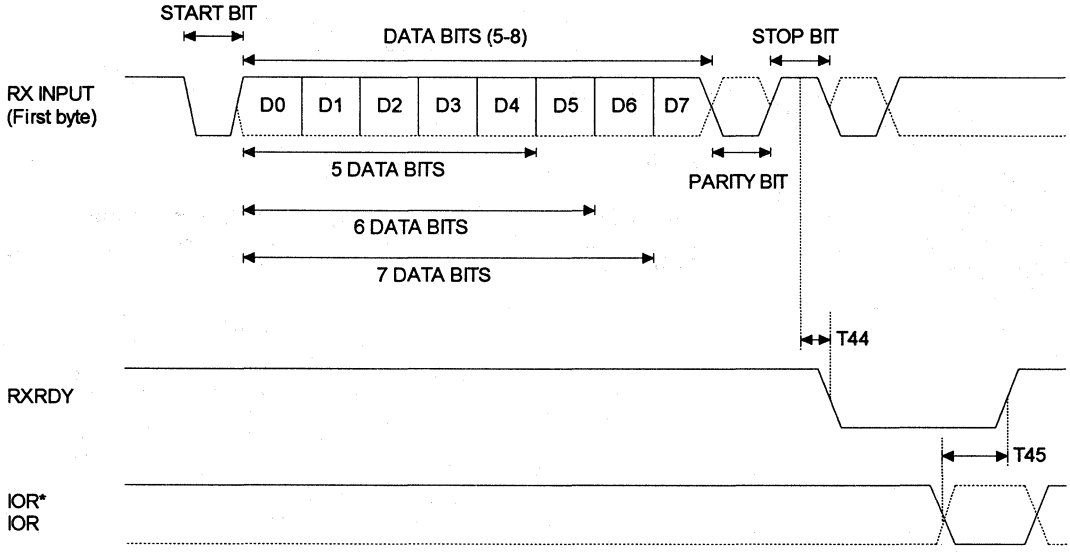


ST16C550

TXRDY TIMING FOR MODE "1"

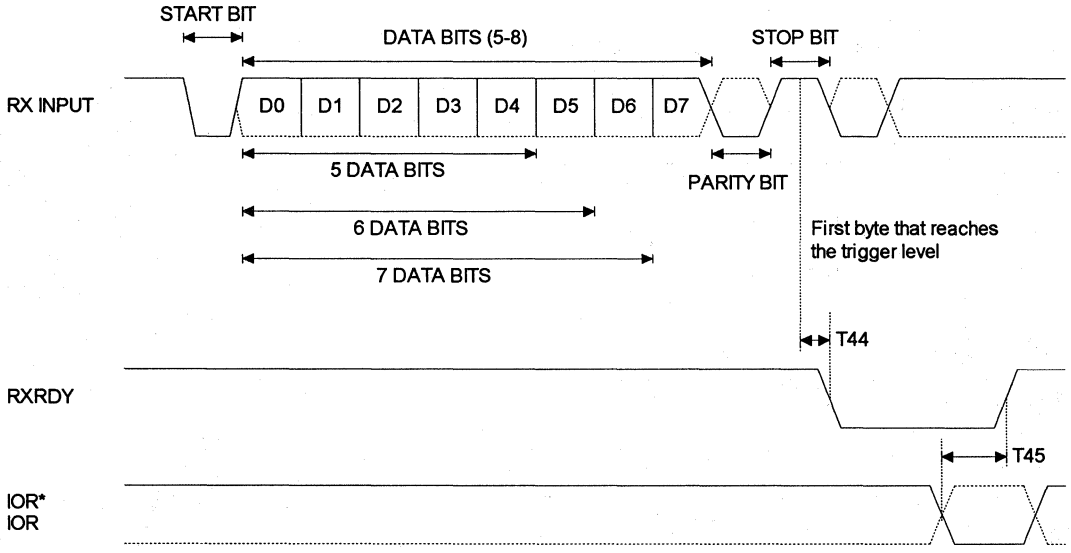


RXRDY TIMING FOR MODE "0"



ST16C550

RXRDY TIMING FOR MODE "1"



STARTECH

ST16C1550
ST16C1551/1552

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C1550/51/52 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1550/51/52 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1550/51/52 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1550/51/52 provides internal loop-back capability for on board diagnostic testing.

The ST16C1550/51/52 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

FEATURES

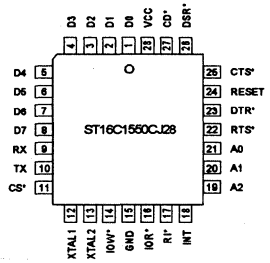
- Pin to pin and functional compatible to SSI 73M1550/2550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

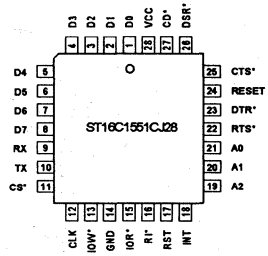
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1550CP28	Plastic-DIP	0° C to + 70° C
ST16C1550CJ28	PLCC	0° C to + 70° C
ST16C1550CQ48	TQFP	0° C to + 70° C
ST16C1551CP28	Plastic-Dip	0° C to + 70° C
ST16C1551CJ28	PLCC	0° C to + 70° C
ST16C1551CQ48	TQFP	0° C to + 70° C
ST16C1552CQ52	QFP	0° C to + 70° C

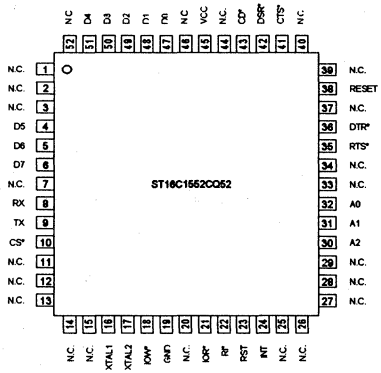
***Industrial operating range are available**

PLCC Package





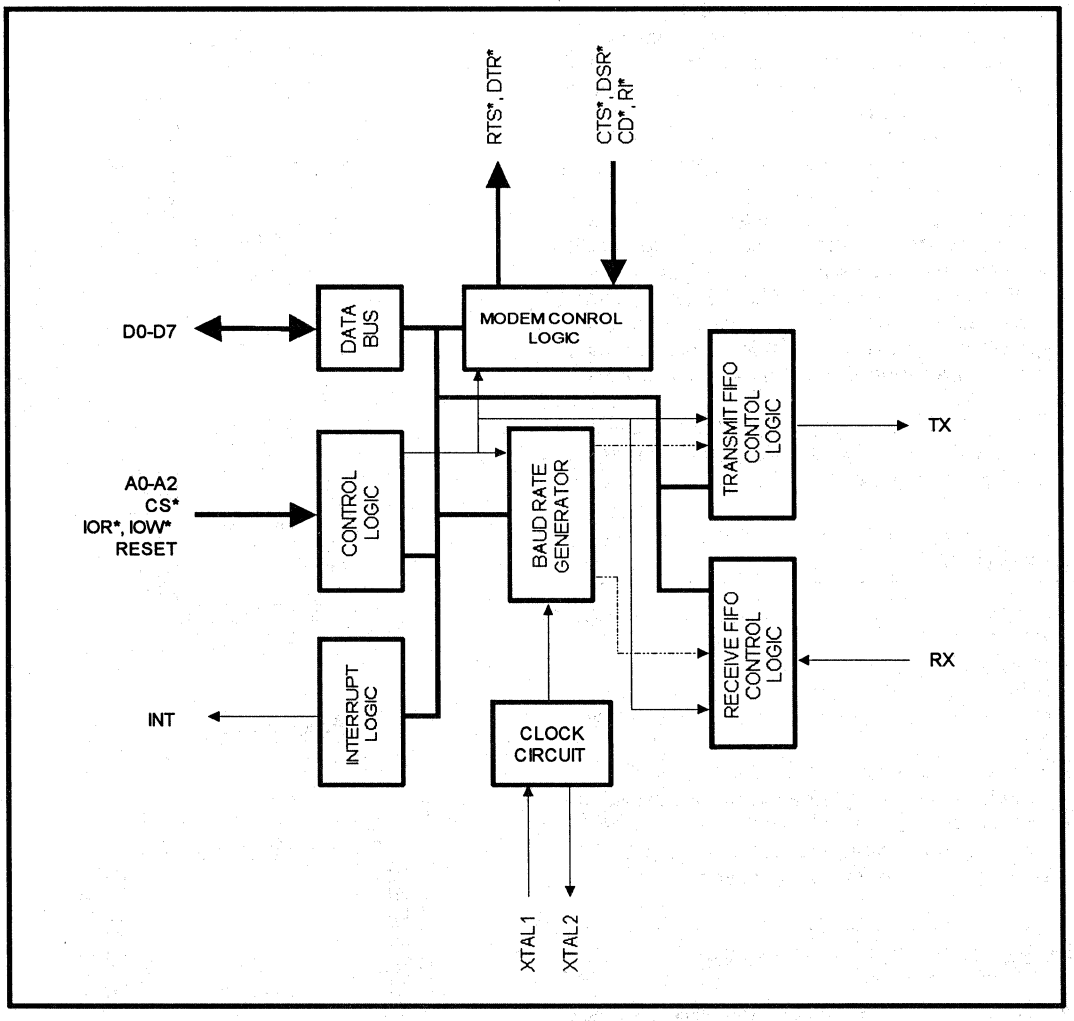
QFP Package



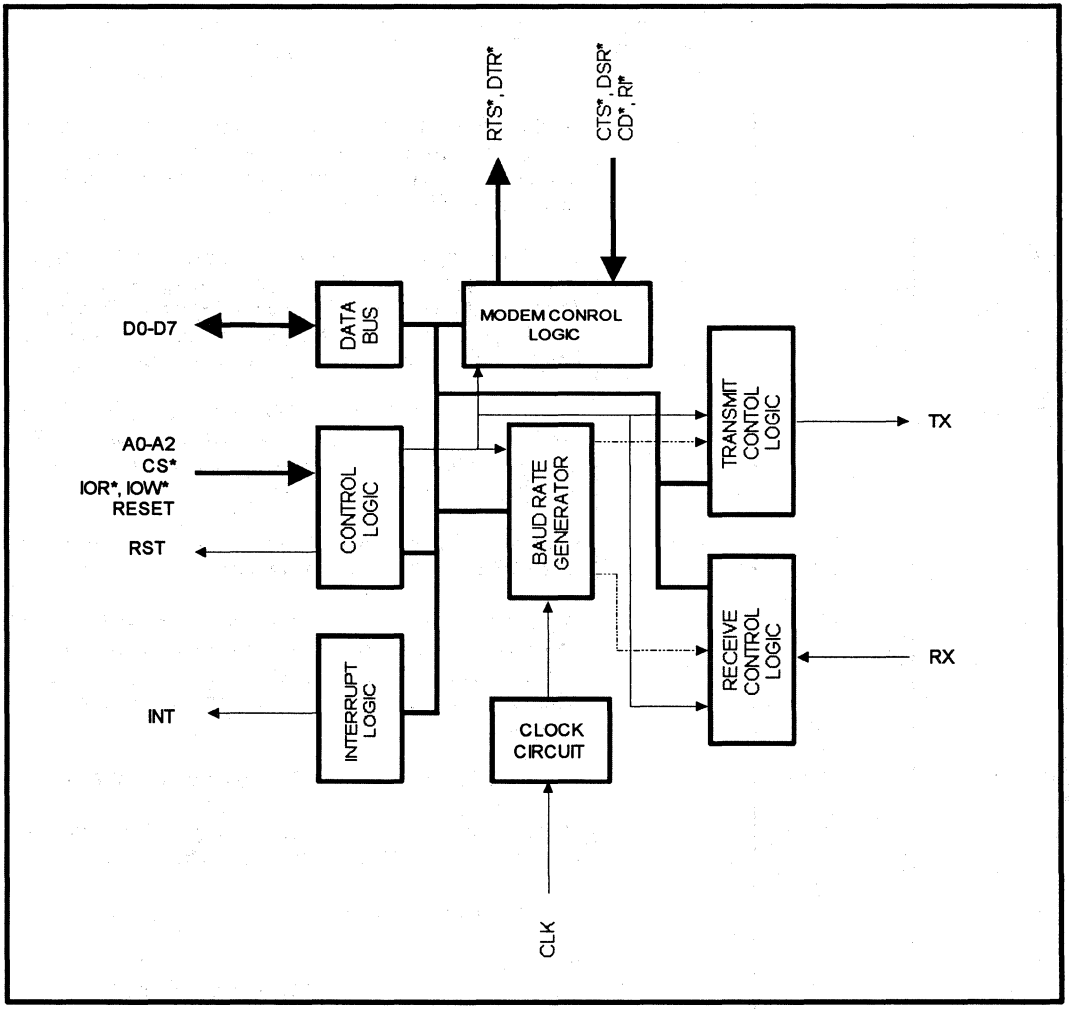
3

ST16C1550
ST16C1551/1552

ST16C1550 BLOCK DIAGRAM



ST16C1551 BLOCK DIAGRAM



ST16C1550
ST16C1551/1552

ST16C1550 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1550 / CPU data transfer operation.
XTAL1	12	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	O	Signal and power ground.
IOR*	16	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1550 data bus to the CPU..
RI*	17	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
INT	18	O	Interrupt output. (three state / active high) This pin goes high

ST16C1550 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			(when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1550
ST16C1551/1552

ST16C1551 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1551 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1551 / CPU data transfer operation.
CLK	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
IOW*	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	14	O	Signal and power ground.
IOR*	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1551 data bus to the CPU..
RI*	16	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
RST	17	O	Reset output (active high). The ST16C1551 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	O	Interrupt output. (three state / active high) This pin goes high

ST16C1551 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			(when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1551 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

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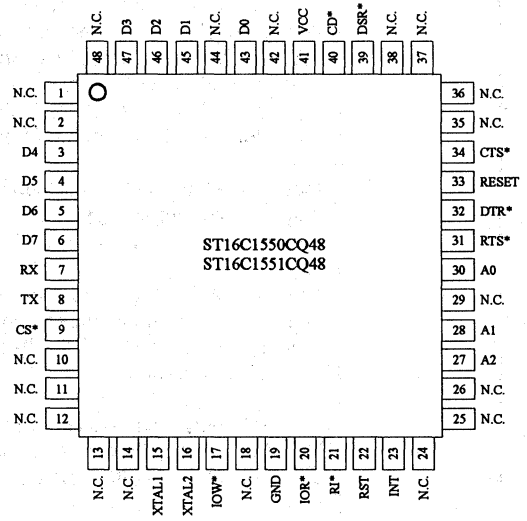
PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch



ST16C1550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0 / TX trigger (MSB)	0 / TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0 / FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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ST16C1551 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0 / special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0 / FIFOs enabled	0 / FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C1550/51/52 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C1550/51/52 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1550/51/52 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

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IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1550/51/52 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1550/51/52 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Received Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example-A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3:
This bit is used with conjunction of ISR bit 0-2:
0=normal interrupt mode
1=receive time-out indicator when priority level is set to "2" (D0=0, D1=0, and D2=1)

ISR bit-4:
This bit is the compliment of TXRDY* (ST16C550) pin.
0=transmitter is full
1=transmitter is empty or less than full

ISR bit-5:
This bit is the compliment of RXRDY* (ST16C550) pin.

0=receiver is empty.
1=receiver is not empty

ISR bit-6-7:
0=16C450 mode
1=16C550 mode

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
These bits are used to set the transmit trigger levels. See receive FIFO trigger table.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

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LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.

In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-6:
Not used. Are set to zero permanently.

MCR bit-7:
0=normal mode.
1=power down mode. CLK, XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C1550/51/52 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C1550/51/52 has changed from a low to a high state.

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MSR BIT-3:
Indicates that the CD* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1550/51/52 provides a temporary data register to store 8 bits of information for variable use.

SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C1550/51/52 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	

Note 1: * = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

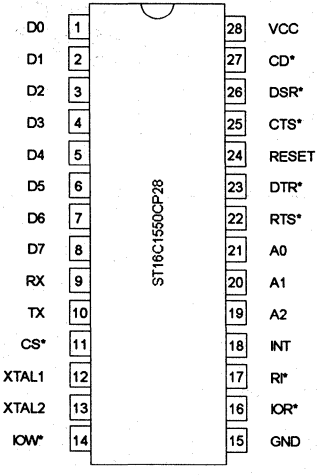
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

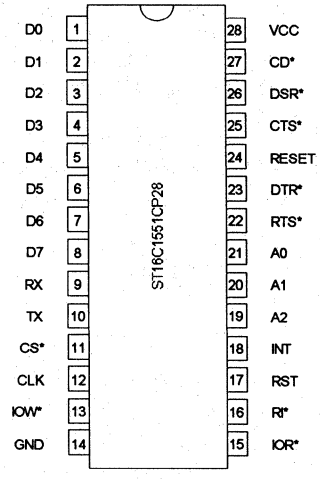
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

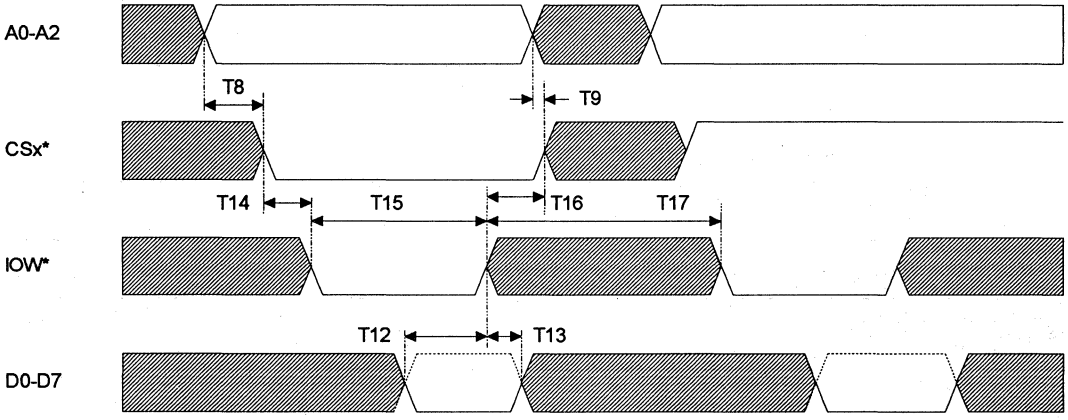
28 PIN PLASTIC-DIP ST16C1550



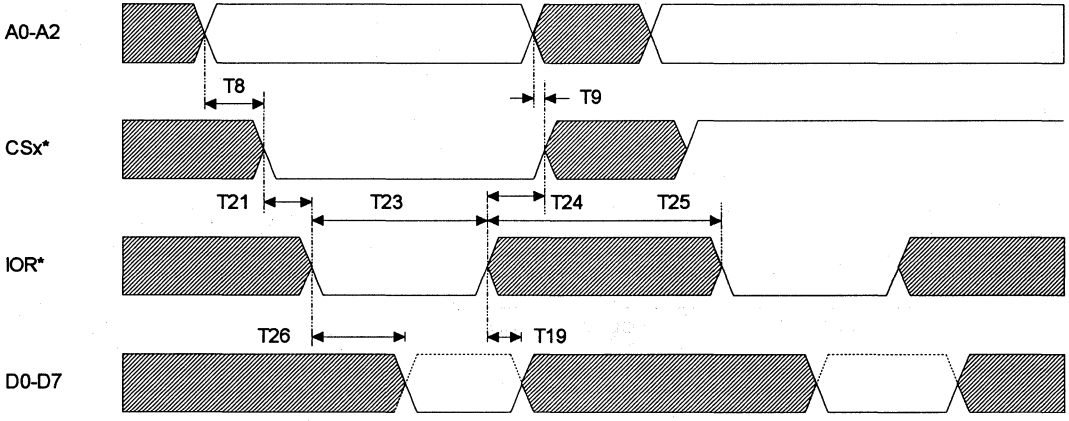
28 PIN PLASTIC-DIP ST16C1551



GENERAL WRITE TIMING

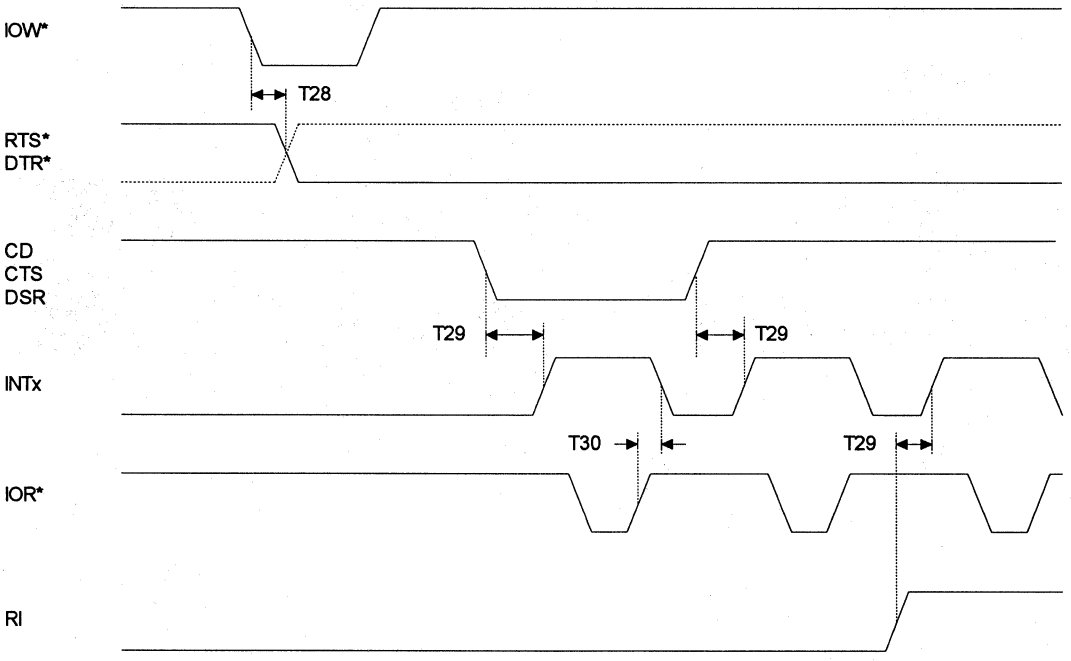


GENERAL READ TIMING

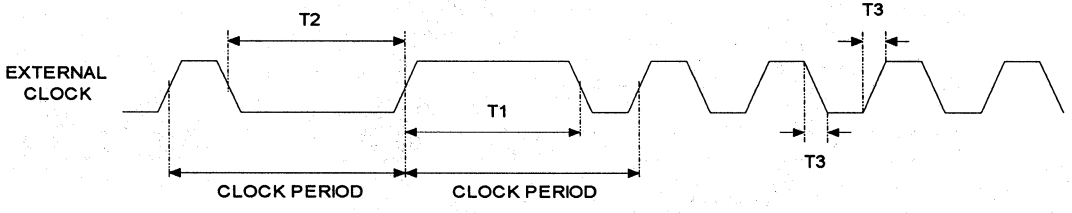


ST16C1550
ST16C1551/1552

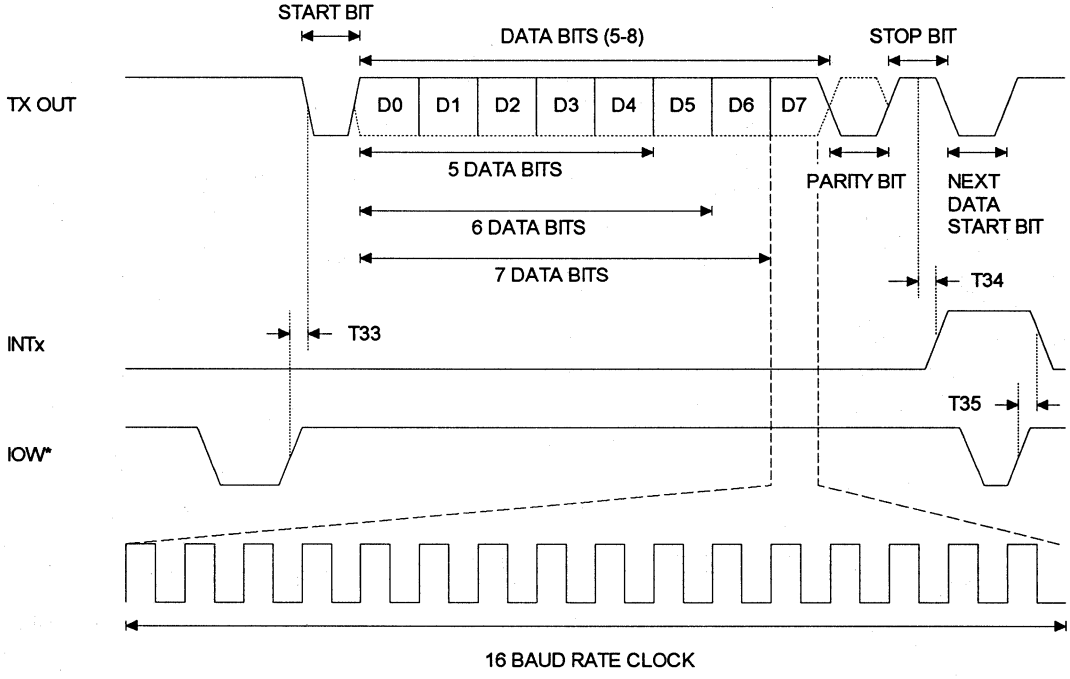
MODEM TIMING



CLOCK TIMING

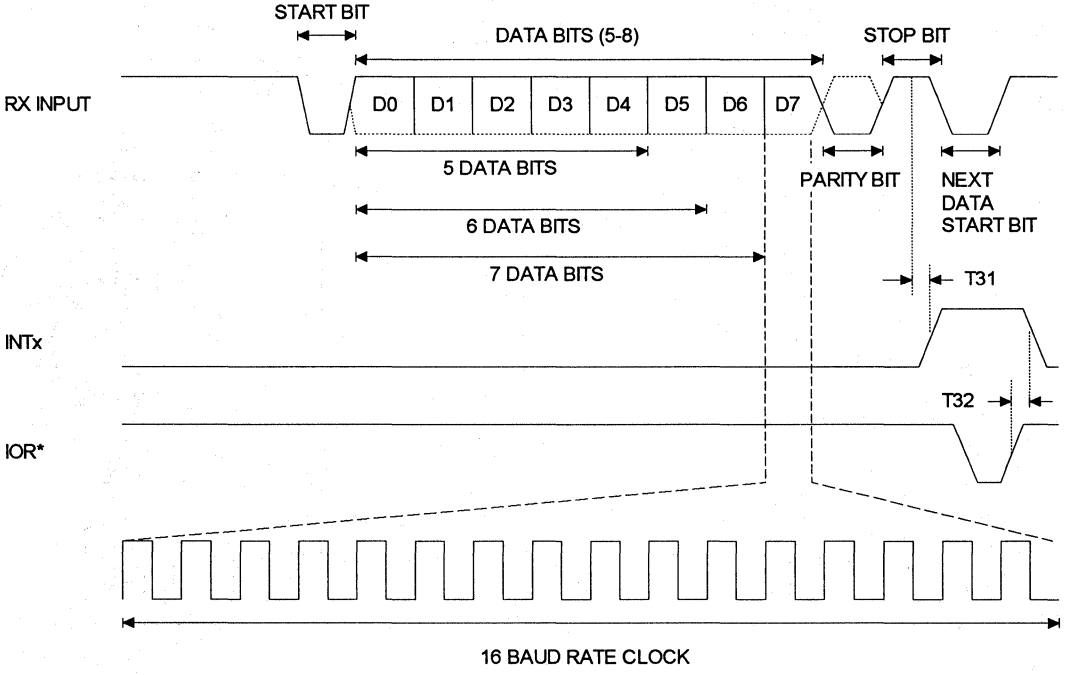


TRANSMIT TIMING



ST16C1550
ST16C1551/1552

RECEIVE TIMING



STARTECH

ST16C2550

Printed February 23, 1994

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

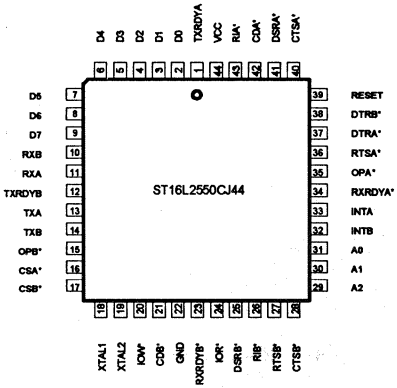
DESCRIPTION

The ST16C2550 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART.

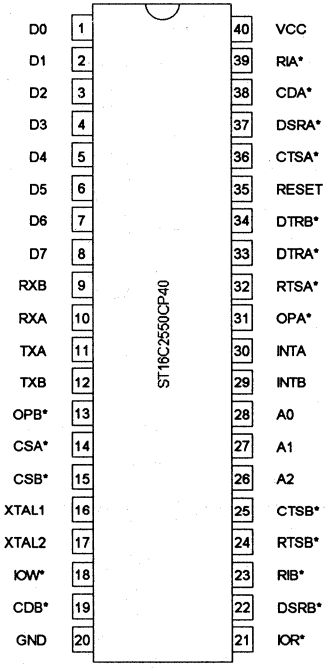
The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C2550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2550 provides internal loop-back capability for on board diagnostic testing.

The ST16C2550 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

- Pin to pin and functional compatible to ST16C2450
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

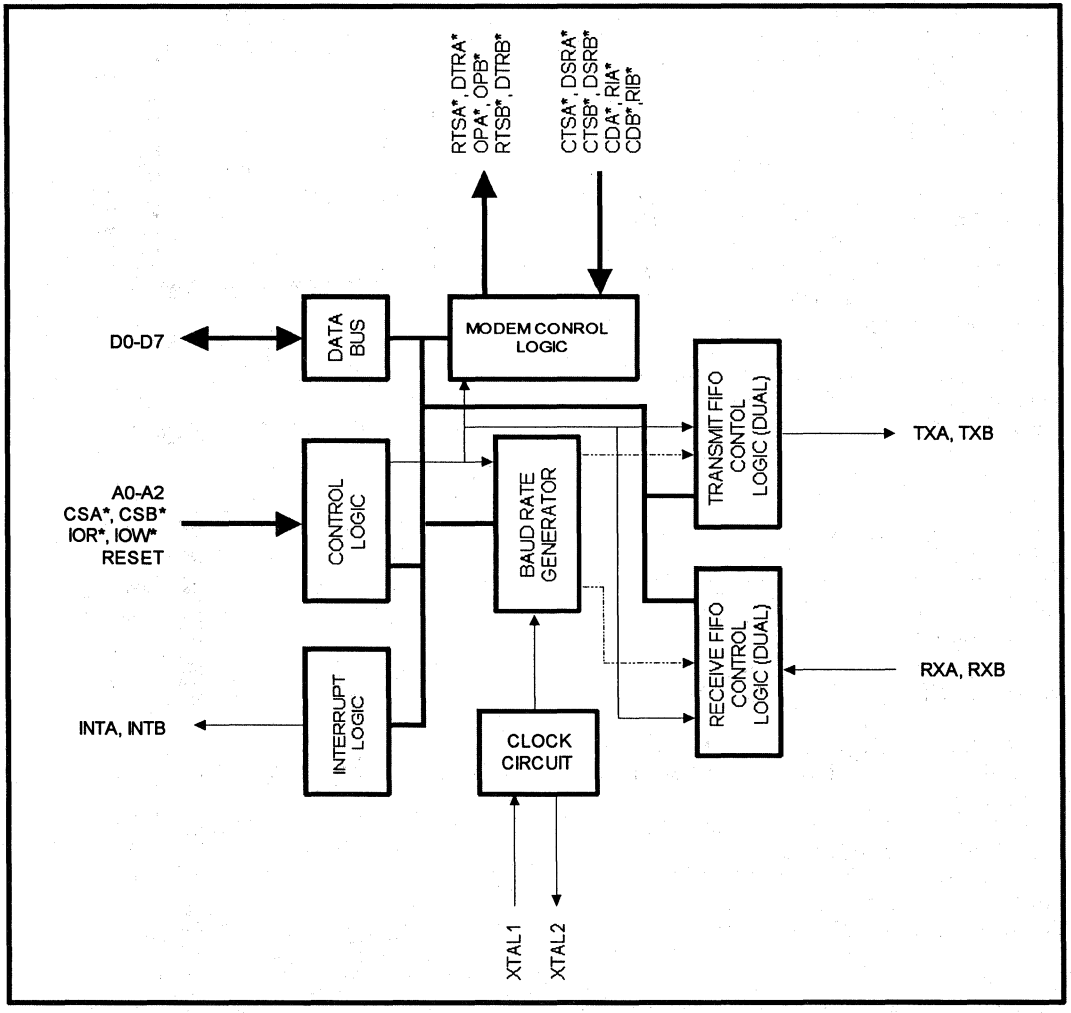
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2550CP40	Plastic-DIP	0° C to + 70° C
ST16C2550CJ44	PLCC	0° C to + 70° C

***Industrial operating range are available**

ST16C2550

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	10,9	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	O	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A/B*	14,15	I	Chip select A/B. (active low) A low at this pin enables the ST16C2550 / CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2550 data bus to the CPU.
A0-A2	28-26	I	Address select lines. To select internal registers.
INT A/B	30,29	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
OP2 A/B*	31	O	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
RTS A/B*	32,24	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A/B*	33,34	O	Data terminal ready A/B (active low). To indicate that ST16C2550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A/B*	36,25	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A/B*	37,22	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B*	38,19	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI A/B*	39,23	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
VCC	40	I	Power supply input.
GND	20	O	Signal and power ground.
TXRDY A/B	1,12**	O	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.
RXRDY A/B*	34,23**	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.

** Available on the PLCC package only.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

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ST16C2550 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2/ INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C2550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

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IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Received Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C2550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C2550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C2550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C2550 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C2550 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

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LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except in local loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode and OP2* output to high.
1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and OP2*/INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C2550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2during local loop-back mode. It is the compliment of the RI* input.

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MSR BIT-7:
This bit is equivalent to OP2*/INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state mode

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C2550

ABSOLUTE MAXIMUM RATINGS

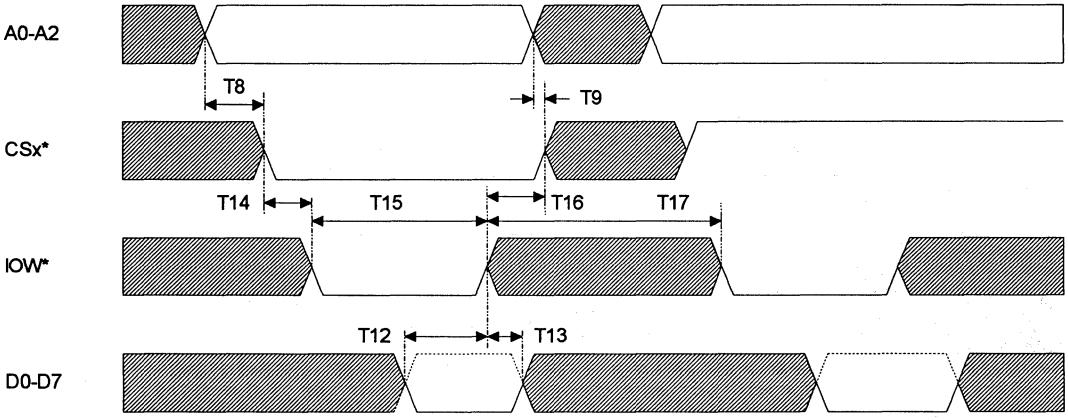
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

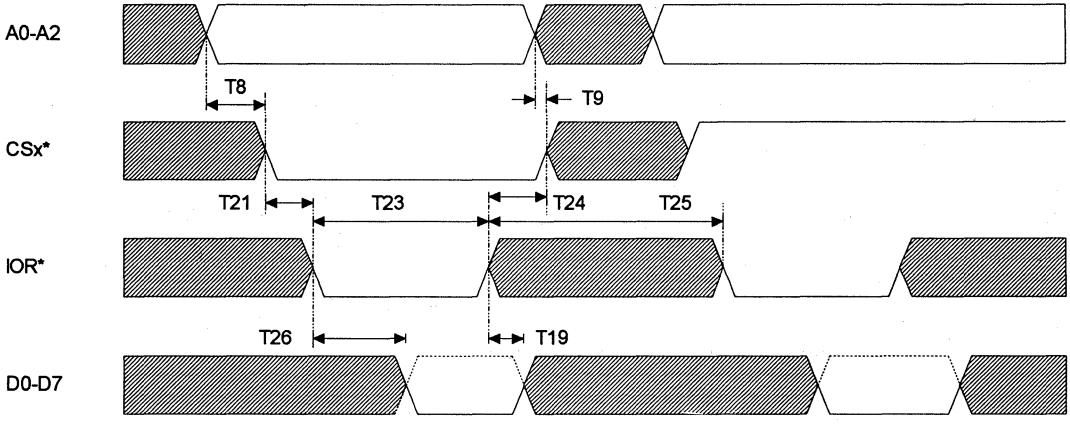
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING



GENERAL READ TIMING



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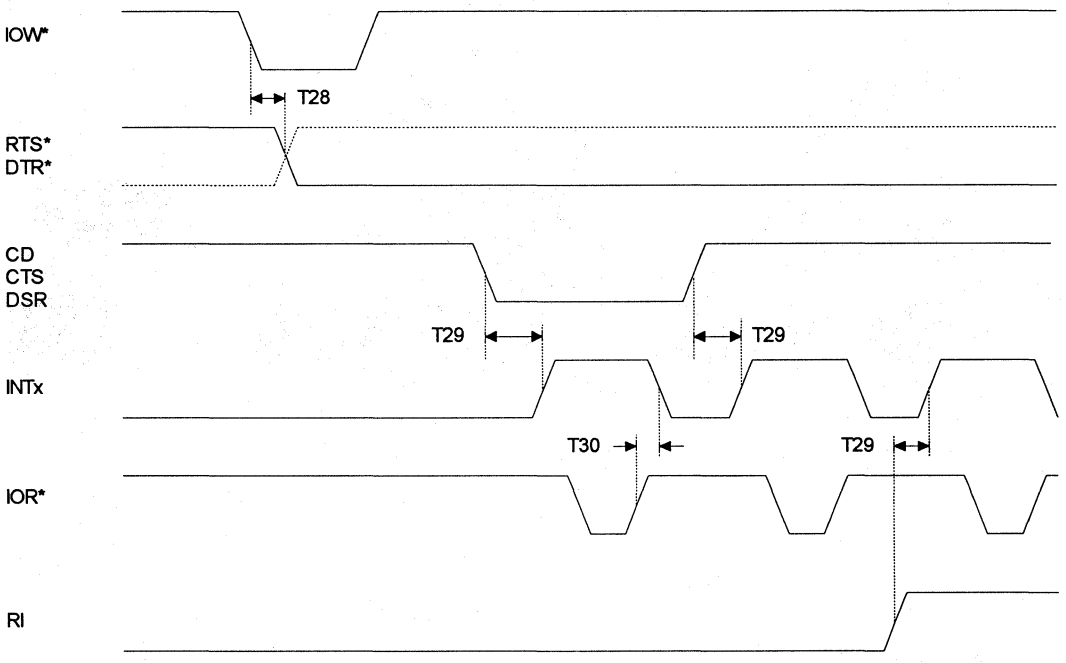
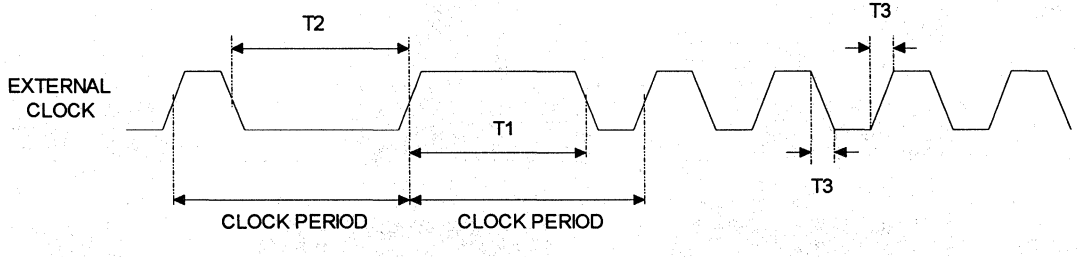
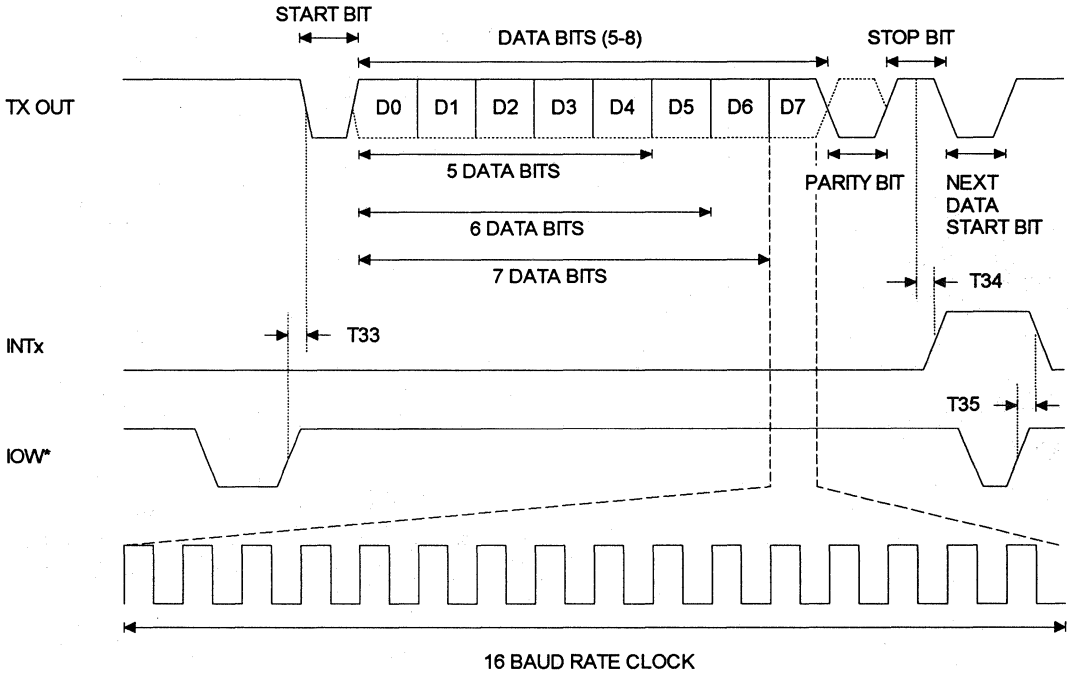
MODEM TIMING



CLOCK TIMING



TRANSMIT TIMING



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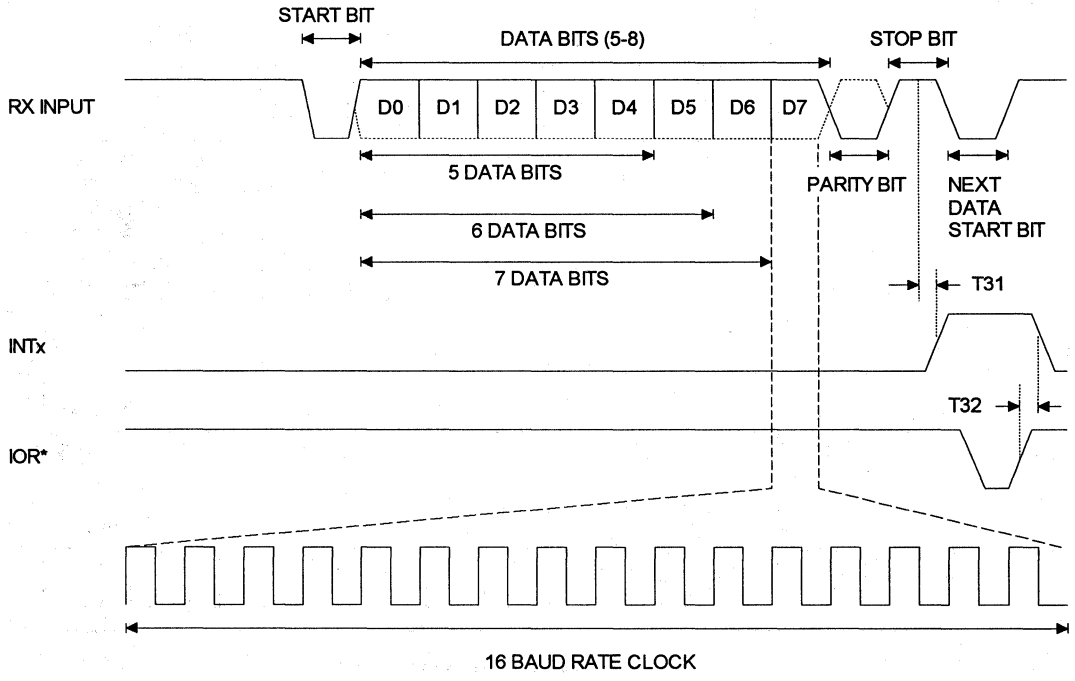
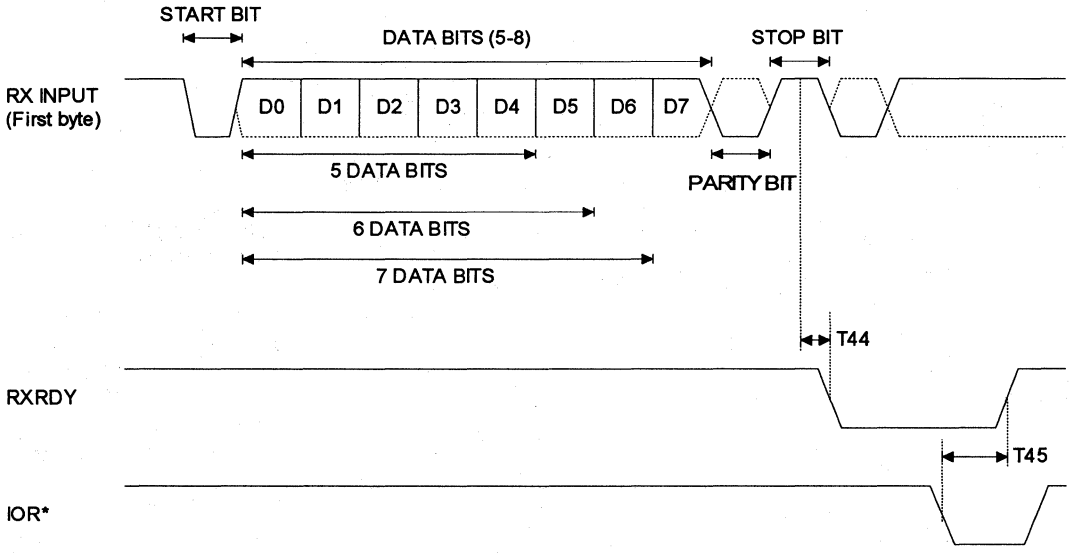
RECEIVE TIMING



RXRDY TIMING FOR MODE "0"



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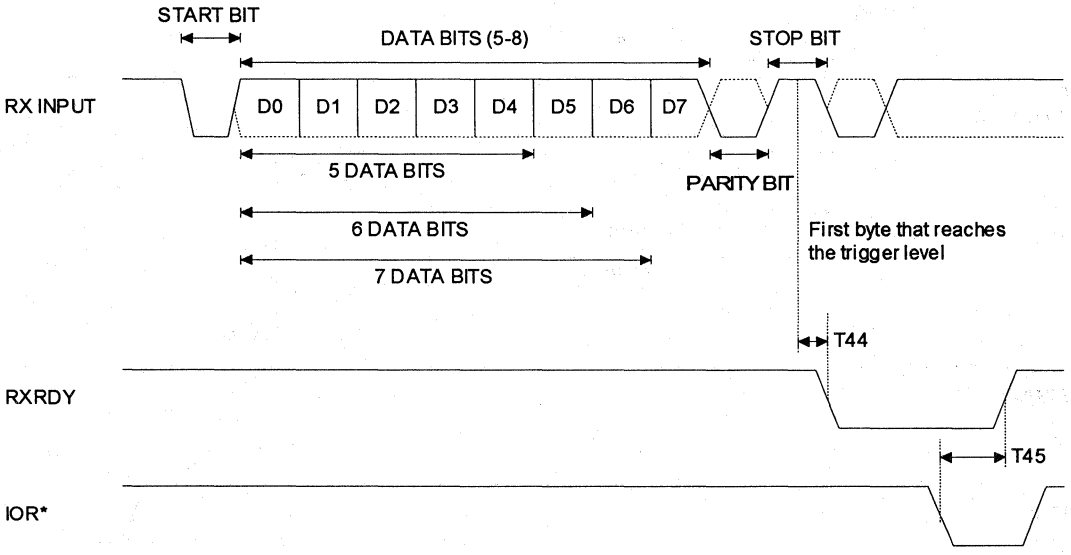
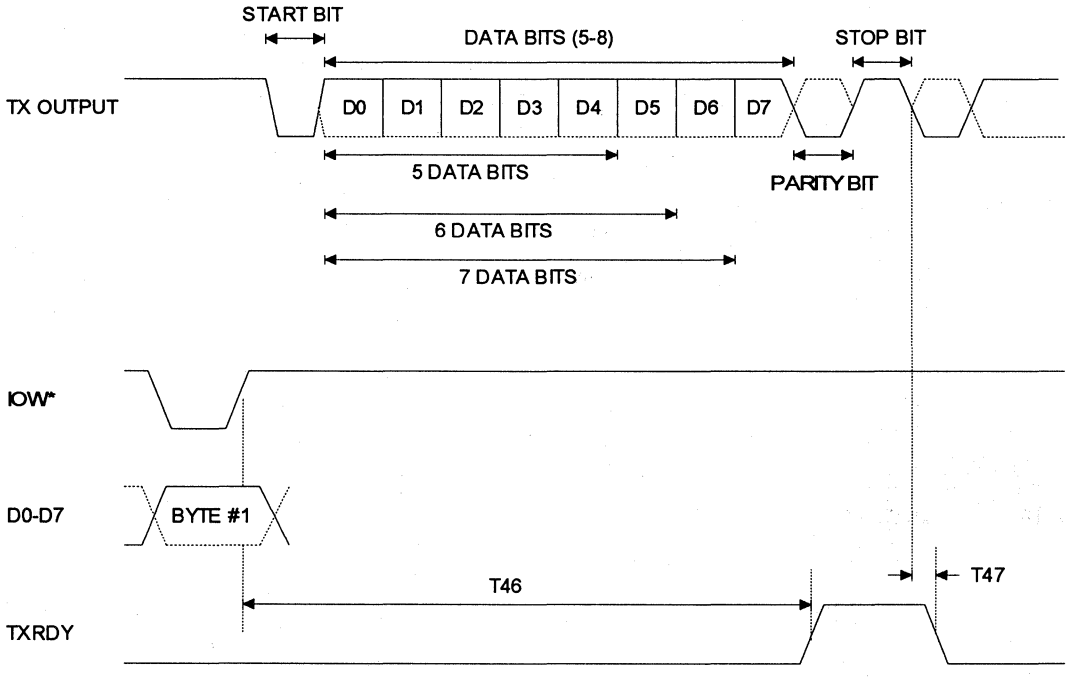
RXRDY TIMING FOR MODE "1"



TXRDY TIMING FOR MODE "0"



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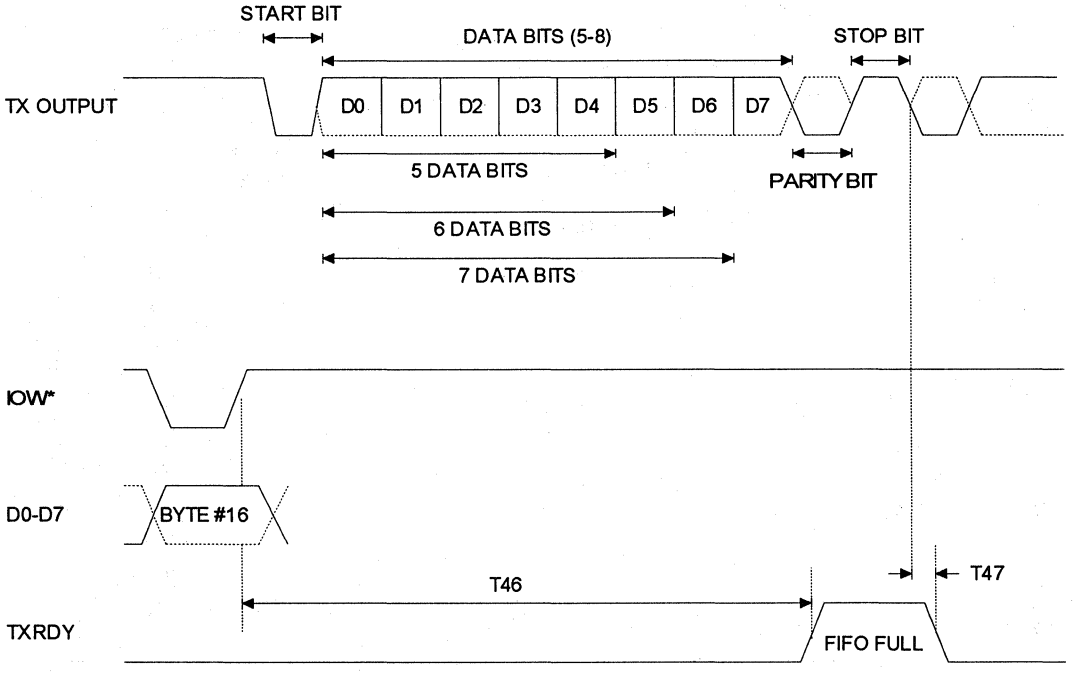
TXRDY TIMING FOR MODE "1"



STARTECH

ST16C2552

Printed February 23, 199

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

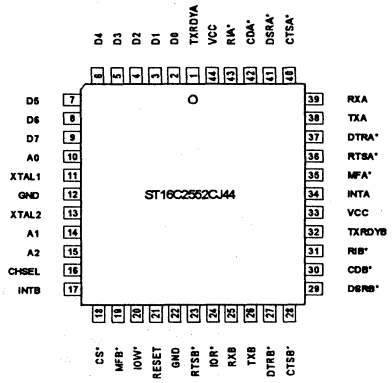
The ST16C2552 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFOs. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART.

The on board status registers of the ST16C2552 provide the error conditions, type and status of the transfer operation being performed. Complete MODEM control capability and a processor interrupt system that may be software tailored to the user's requirements are included. The ST16C2552 provides internal loop-back capability for on board diagnostic testing.

Signalling for DMA transfers is done through two pins per channel (TXRDY, RXRDY*). The RXRDY* function is multiplexed on one pin with the OP2* and BAUDOUT functions. CPU can select these functions through the Alternate Function Register.

The ST16C2552 is fabricated in an advanced 1.2µ CMOS process to achieve low power and high speed requirements.

PLCC Package



FEATURES

- Pin to pin and functional compatible to National NS16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8) bits
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Independent transmit and receive control
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2552CJ44	PLCC	0° C to + 70° C
ST16C2552IJ44	PLCC	-40° C to + 85° C

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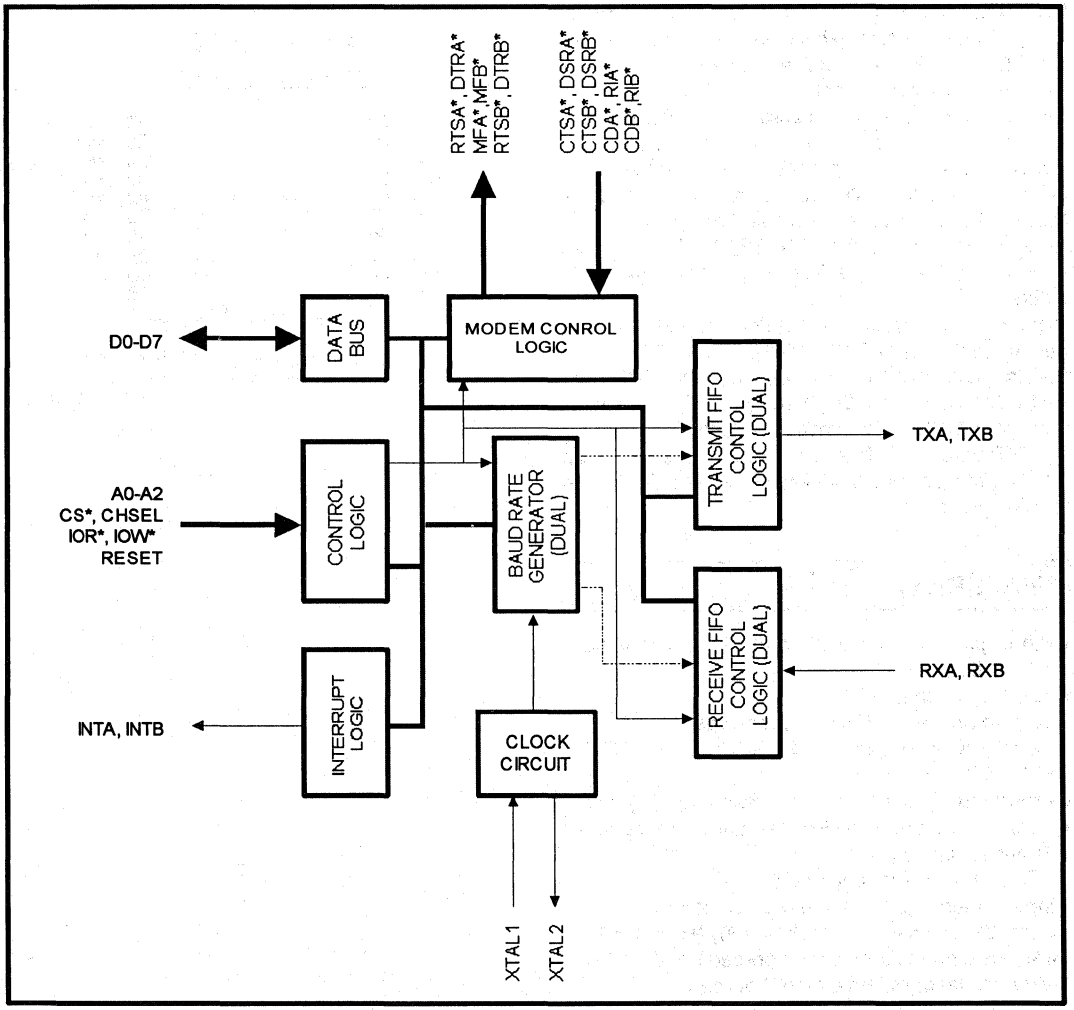
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	39,25	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	38,26	O	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	18	I	Chip select. (active low) A low at this pin enables the ST16C2552 / CPU data transfer operation.
CHSEL	16	I	UART A/B select. UART A or B can be selected by changing the state of this pin when CS* is active. Low on this pin, selects the UART B and high on this pin selects UART A section.
XTAL1	11	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	I	Crystal input 2 or buffered clock output. See XTAL1. Should be left open if a clcok is connected to XTAL1.
IOW*	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	24	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2552 data bus to the CPU.
A0-A2	10,14,15	I	Address select lines. To select internal registers.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INT A/B	34,17	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
MF A/B*	35,19	O	OP2* (interrupt enable), BAUDOUT* and RXRDY* outputs. These outputs are multiplexed via Alternate Function Register. When output enable function is selected the MF* pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled. See bit-3 modem control register (MCR bit-3). When BAUDOUT function is selected, the 16 X TX/RX Baud rate clock output is generated. RXRDY function can be selected to use to request a DMA transfer of data from the Receive data FIFO. OP2* is the default signal and it is selected immediately after master reset or power-up.
TXRDY A/B	1,32	O	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C2552 is full. It can be used as a single or multi-transfer.
RTS A/B*	36,23	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A/B*	37,27	O	Data terminal ready A/B (active low). To indicate that ST16C2552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	21	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CTS A/B*	40,28	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A/B*	41,29	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B*	42,30	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI A/B*	43,31	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	33,44	I	Power supply input.
GND	12,22	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch
0	1	0	Alternate Function Register	Alternate Function Register

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ST16C2552 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***
0 1 0	***AFR***	***0***	***0***	***0***	***0***	***0***	***MF* sel-1***	***MF* sel-0***	***SP write***

These registers are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

Each UART section of the ST16C2552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

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IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero if the FIFOs are not enabled. **BIT 6-7:** are set to "1" when the FIFOs are enabled.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

ALTERNATE FUNCTION REGISTER (AFR)

This is a read/write register used to select specific modes of MF* operation and to allow both UART registers sets to be written concurrently.

AFR BIT-0:
When this bit is set, CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by CPU when both channels are initialized to the same state. CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operation. Setting or clearing this bit has no effect on read operations.
The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0,1, or 2.

AFR BIT 1-2:
Combinations of these bits selects one of the MF* functions.

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BIT-2	BIT-1	MF* Function
0	0	OP2*
0	1	BAUDOUT*
1	0	RXRDY*
1	1	Reserved

AFR BIT 3-7:
Not used. All these bits are set to logic zero.

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select Divisor Latch Register and Alternate Function Register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except in local loop-back mode.

MCR BIT-3:
0=force OP2* output to high.
1=force OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C2552 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

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MSR BIT-0:
Indicates that the CTS* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
MFR	AFR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Low
TxRdy	Low

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

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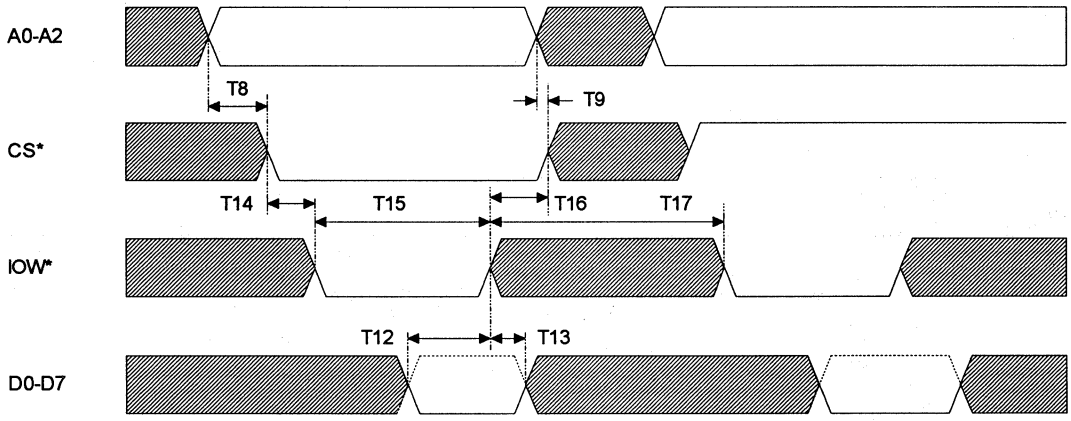
AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

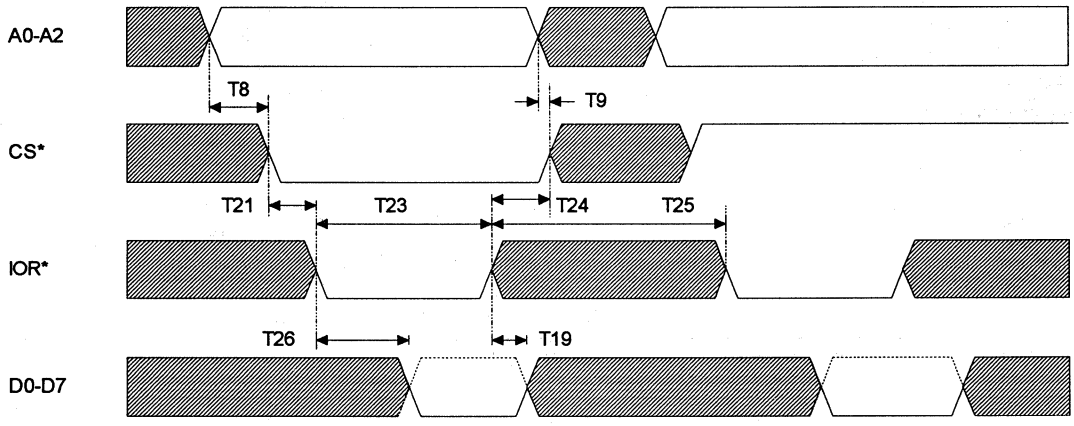
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

GENERAL WRITE TIMING

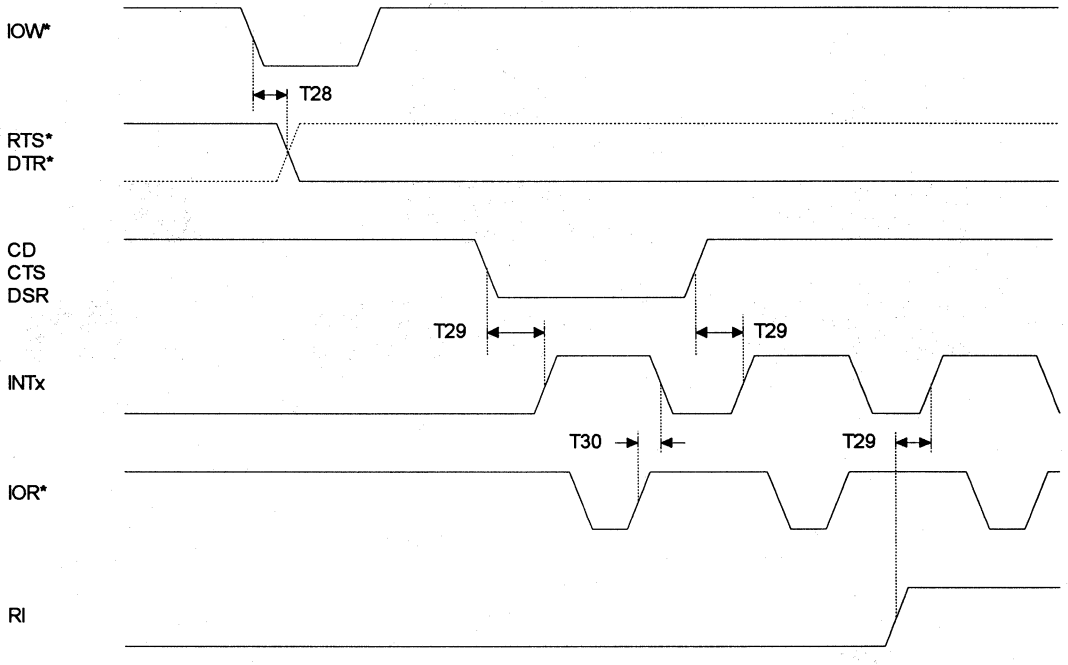


GENERAL READ TIMING

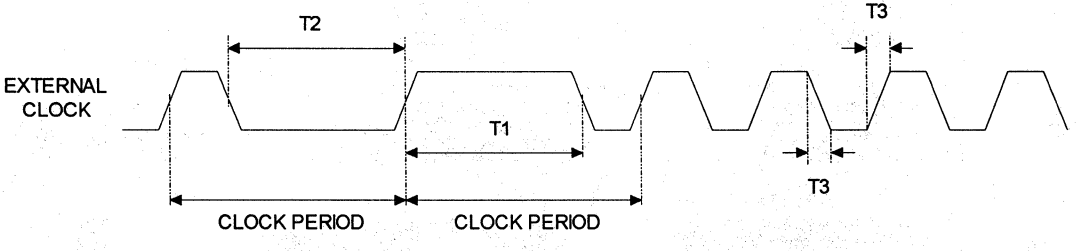


ST16C2552

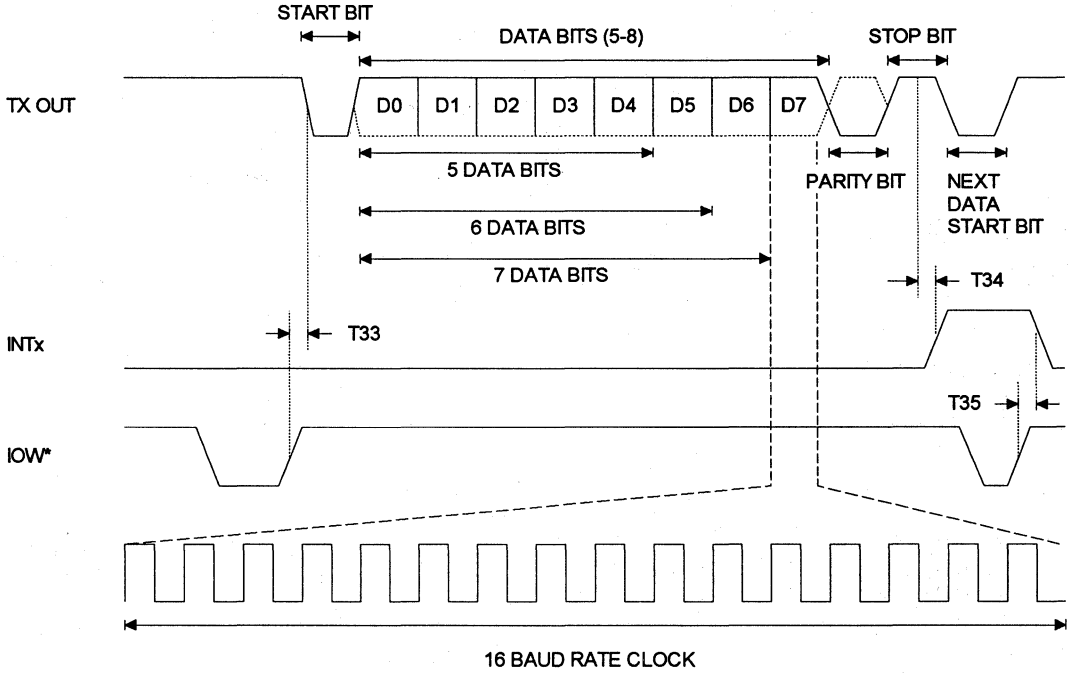
MODEM TIMING



CLOCK TIMING



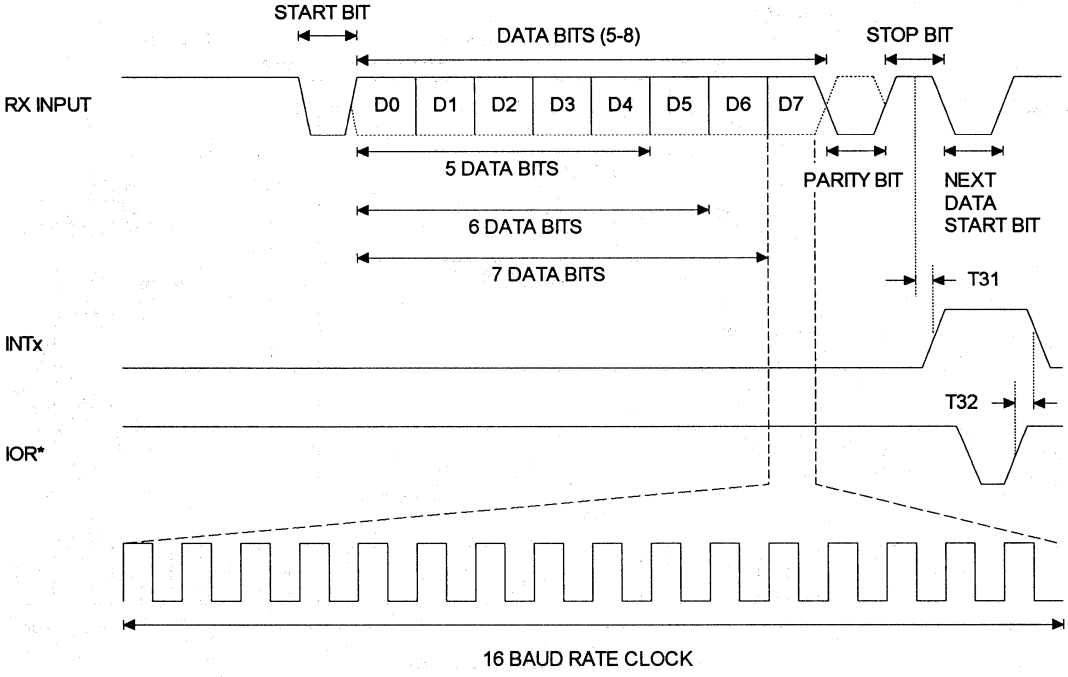
TRANSMIT TIMING



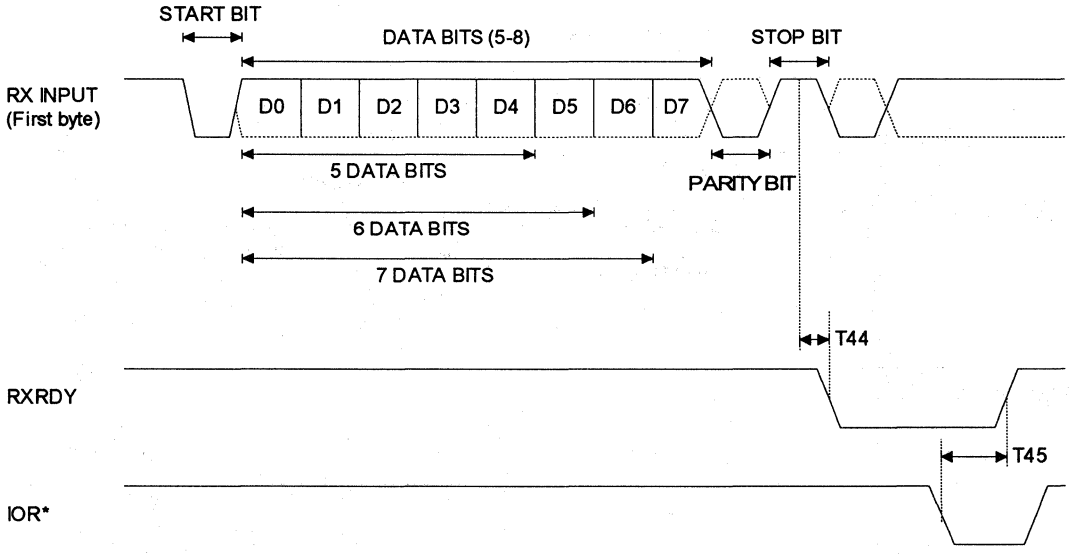
ST16C2552

ST16C2552

RECEIVE TIMING

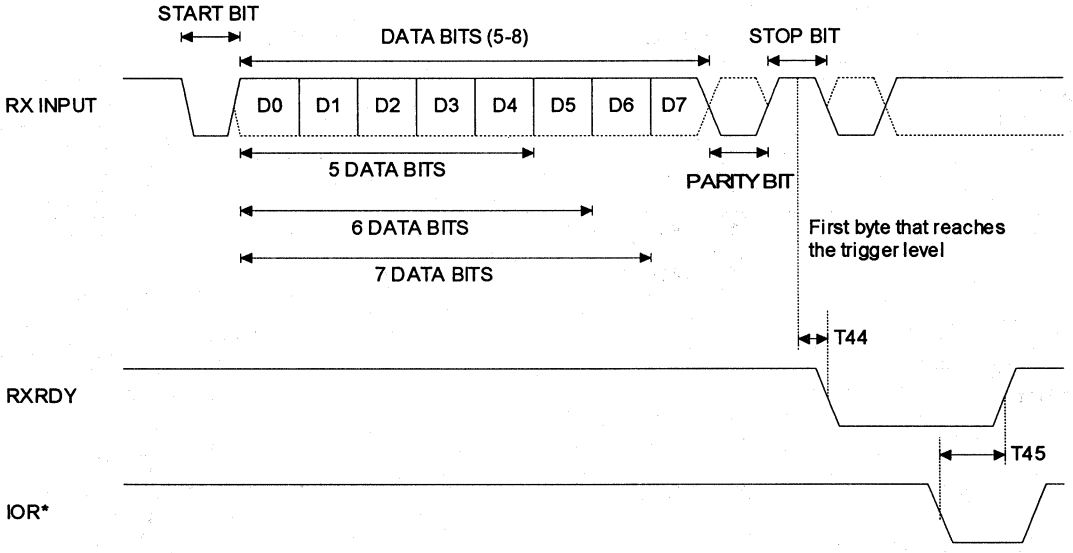


RXRDY TIMING FOR MODE "0"

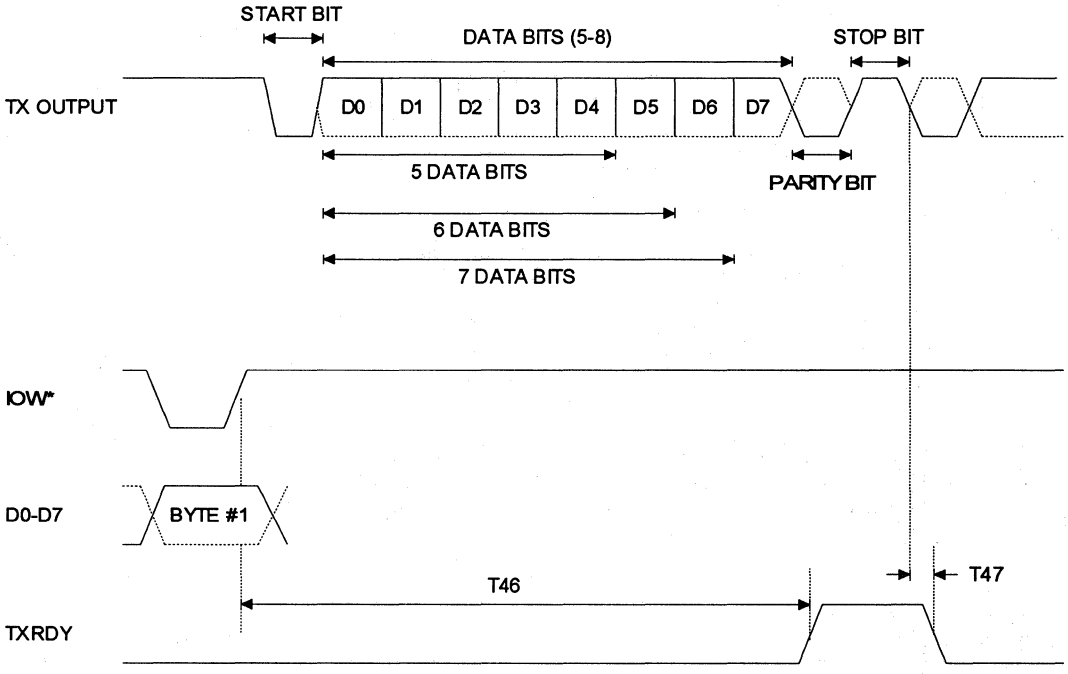


ST16C2552

RXRDY TIMING FOR MODE "1"

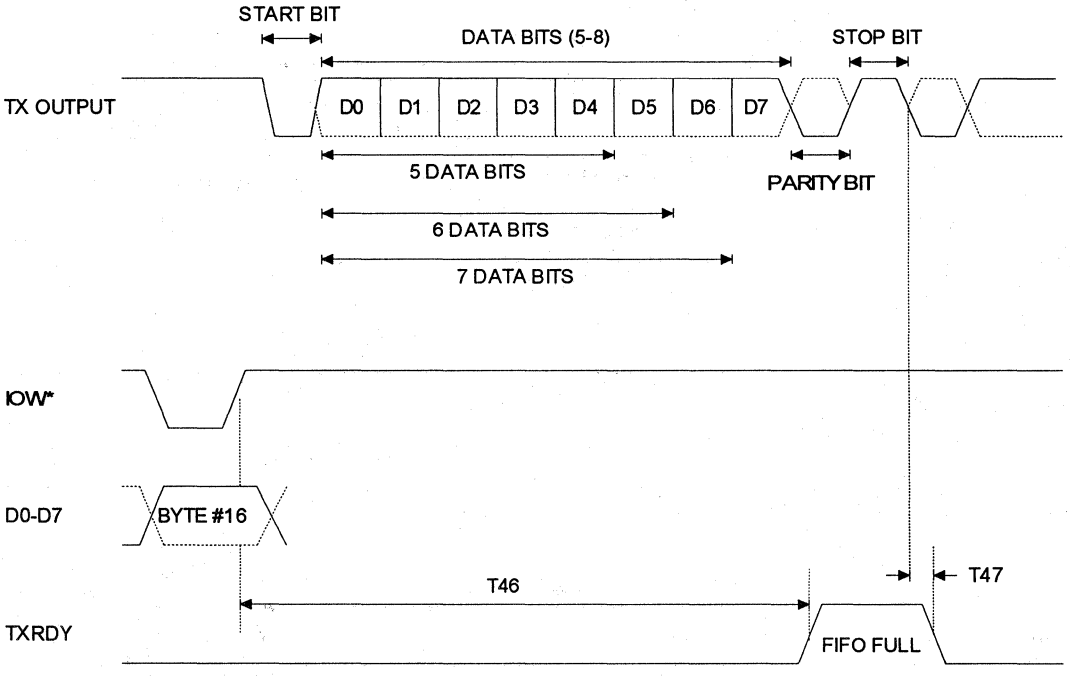


TXRDY TIMING FOR MODE "0"



ST16C2552

TXRDY TIMING FOR MODE "1"



STARTECH

EVALUATION KIT AVAILABLE

ST16C554
ST16C554D

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

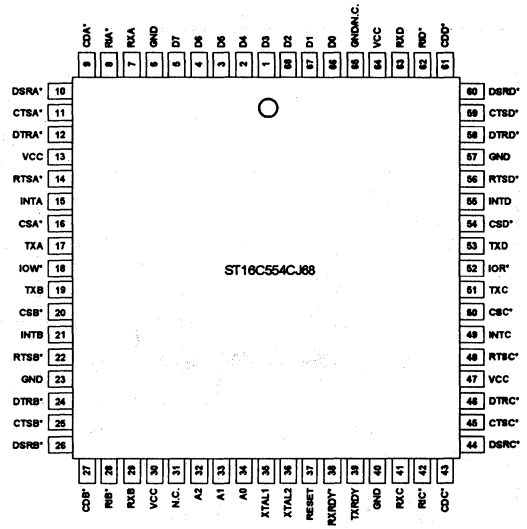
DESCRIPTION

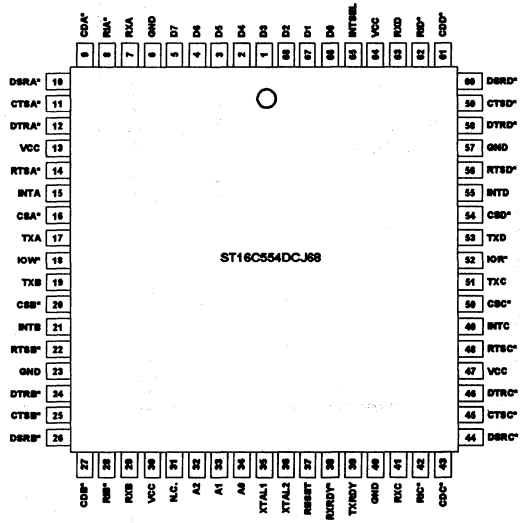
The ST16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C554 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C554 provides internal loop-back capability for on board diagnostic testing.

The ST16C554 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package





FEATURES

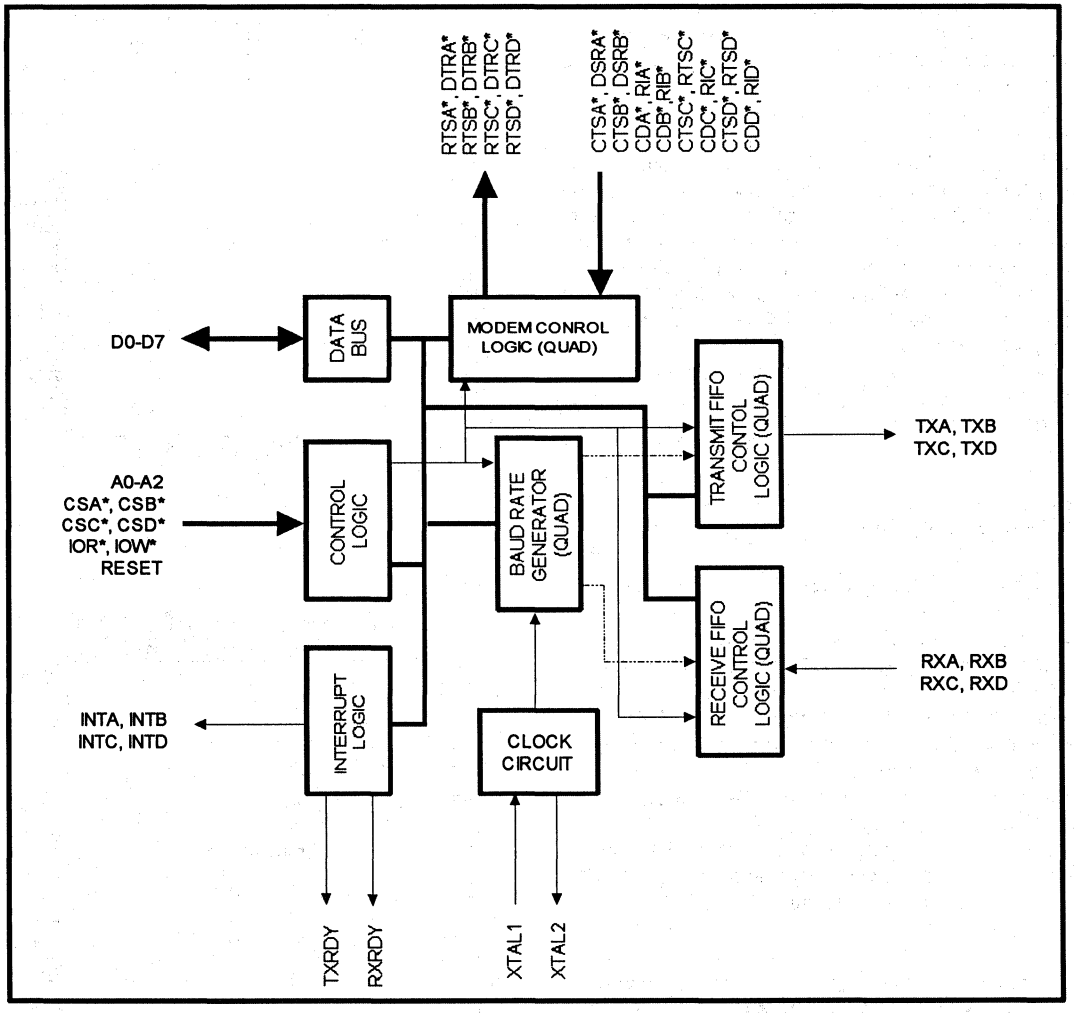
- Pin to pin and functional compatible to ST16C454
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554CJ68	PLCC	0° C to + 70° C
ST16C554IJ68	PLCC	-40° C to + 85° C
ST16C554DCJ68	PLCC	0° C to + 70° C
ST16C554DIJ68	PLCC	-40° C to + 85° C

ST16C554
ST16C554D

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input. The serial information (data) received from serial port to ST16C554 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A-B* CS C-D*	16,20 50,54	I	Chip select. (active low) A low at this pin enables the ST16C554 / CPU data transfer operation. Each UART sections of the ST16C554 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	O	Signal and power ground.
IOR*	52	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C554 data bus to the CPU.

ST16C554
ST16C554D

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
TXRDY	39	O	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C554 is full. It can be used as a single or multi-transfer.
A2	32	I	Address select line 2. To select internal registers.
A1	33	I	Address select line 1. To select internal registers.
A0	34	I	Address select line 0. To select internal registers.
RXRDY*	38	O	Receive ready. (active high) This pin goes high when the receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL	**65****	I	**Interrupt type select. Enable /disable the interrupt three state function. Normal interrupt output can be selected by connecting this pin to VCC (MCR bit-3 does not have any effect on the interrupt output). The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is set to "1".**
INT A-B INT C-D	15,21 49,55	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS A-B* RTS C-D*	14,22 48,56	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A-B* DTR C-D*	12,24 46,58	O	Data terminal ready. (active low) To indicate that ST16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low.

** ST16C554D PARTS ONLY

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A-B* CTS C-D*	11,25 45,59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A-B* DSR C-D*	10,26 44,60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A-B* CD C-D*	9,27 43,61	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI A-B* RI C-D*	8,28 42,62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13,30 47,64	I	Power supply input.

ST16C554
ST16C554D

ST16C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

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A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C554 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C554 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example-A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C554 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

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BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used, except in internal loop-back mode.

MCR BIT-3:
0=set the INT A-D output pin to three state mode..
1=Enable the INT A-D output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C554 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register

MSR BIT-0:
Indicates that the CTS* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C554 has changed from a low to a high state.

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MSR BIT-3:
Indicates that the CD* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
RTS*	High
DTR*	High
RXRDY*	High
TXRDY	Low
INT	Three state mode

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

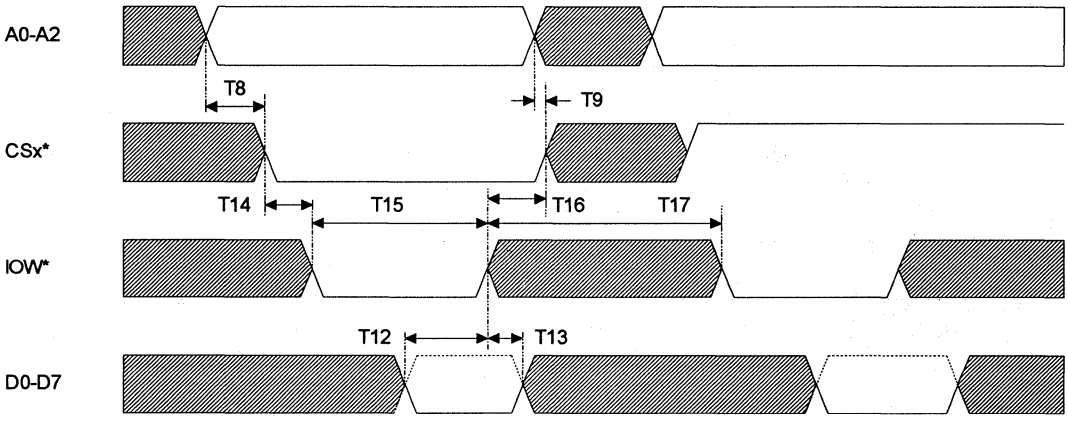
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

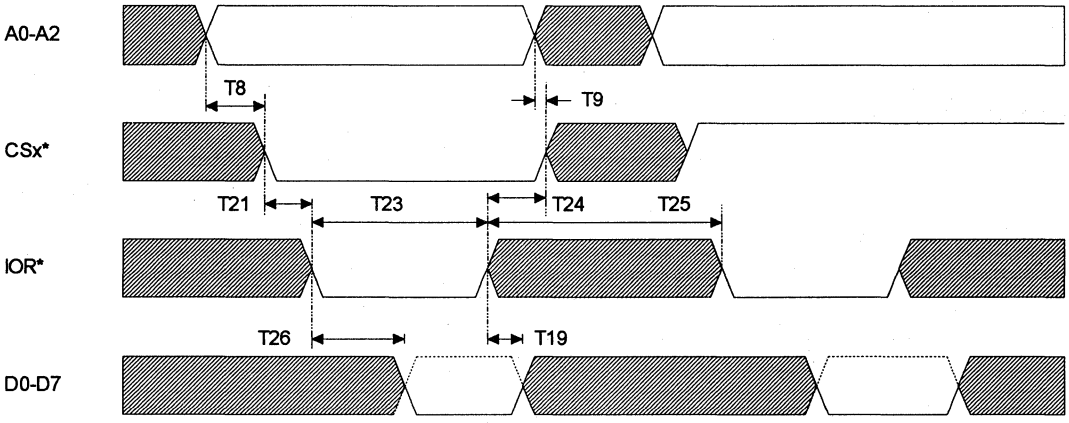
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING



GENERAL READ TIMING



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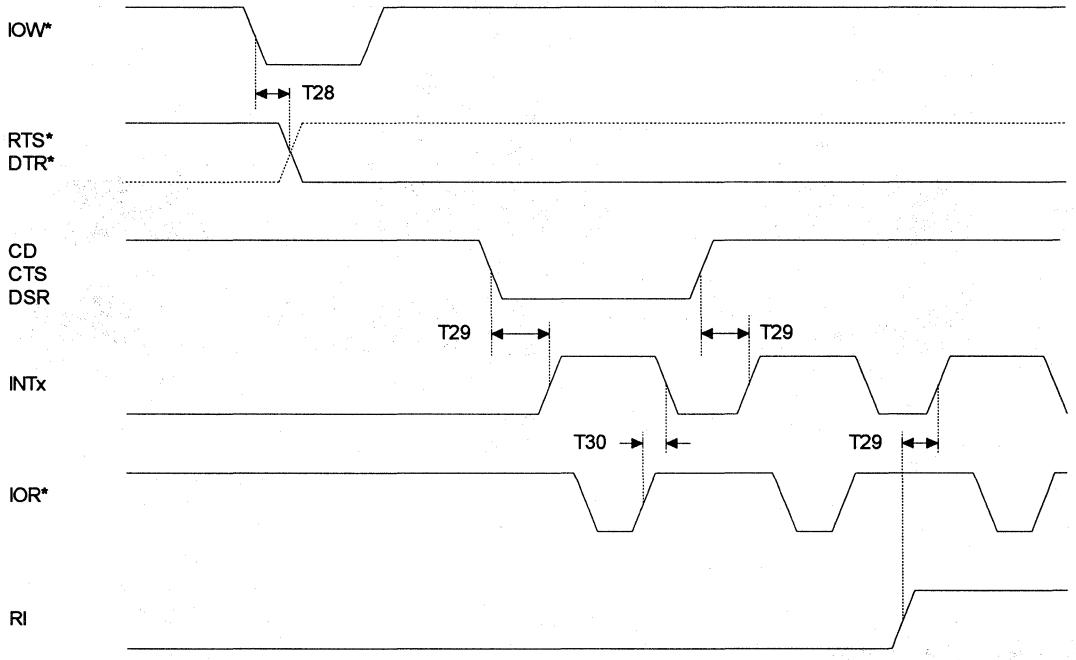
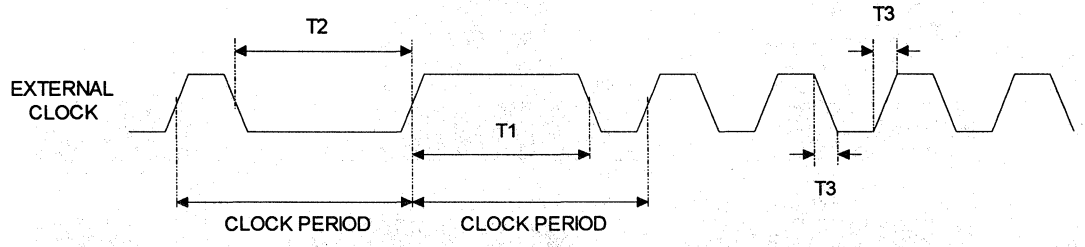
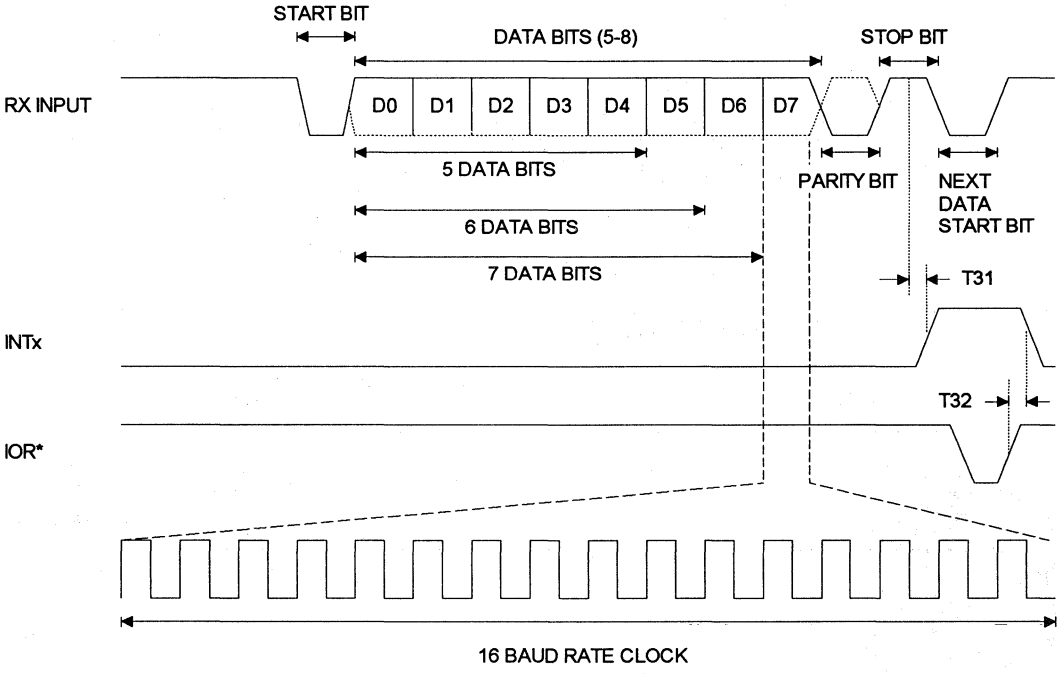
MODEM TIMING



CLOCK TIMING



RECEIVE TIMING



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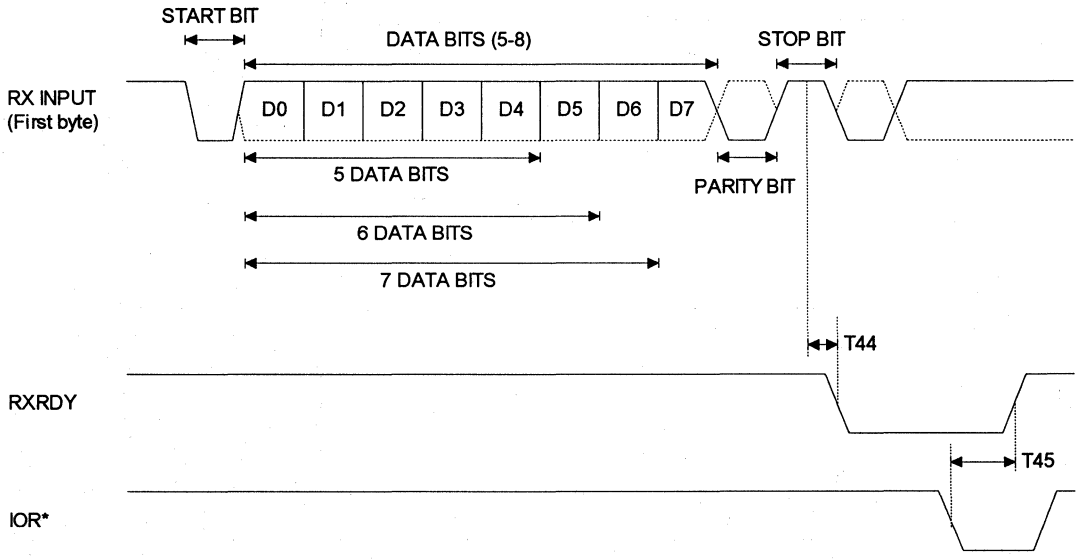
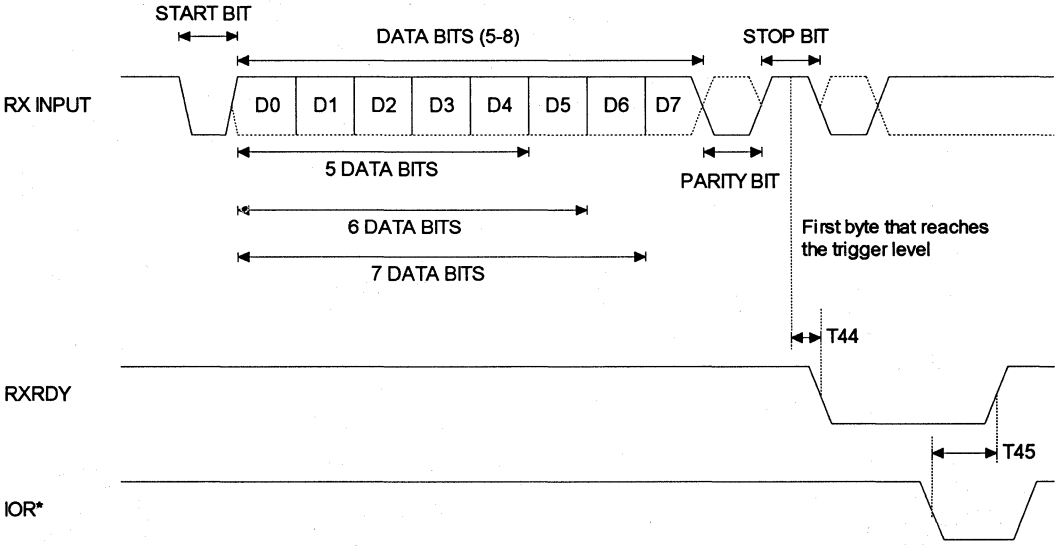
RXRDY TIMING FOR MODE "0"



RXRDY TIMING FOR MODE "1"



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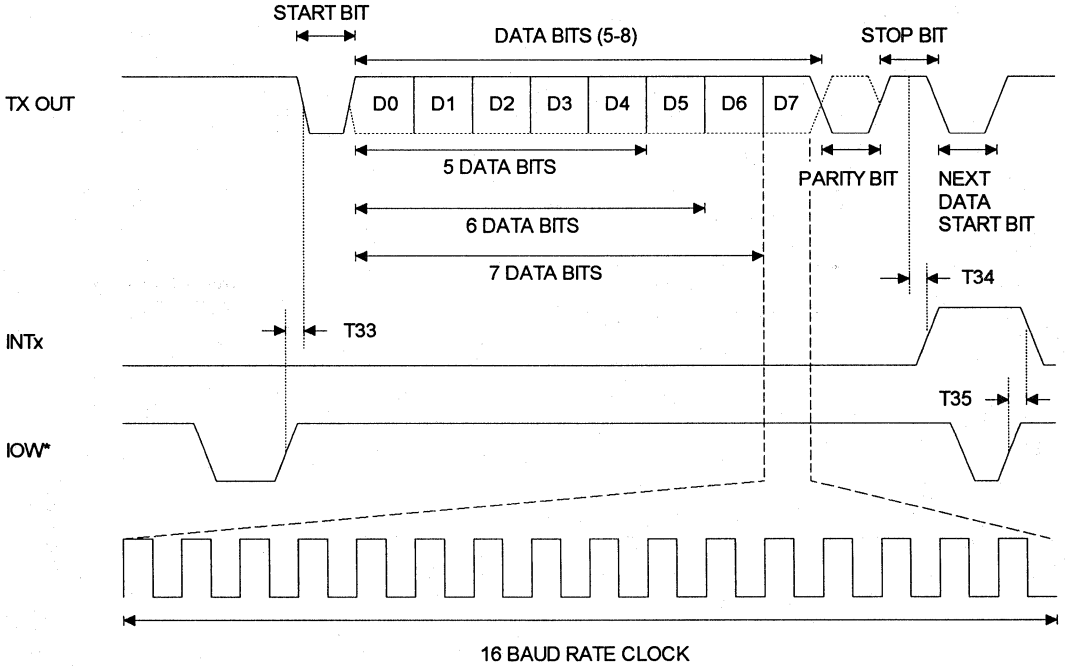
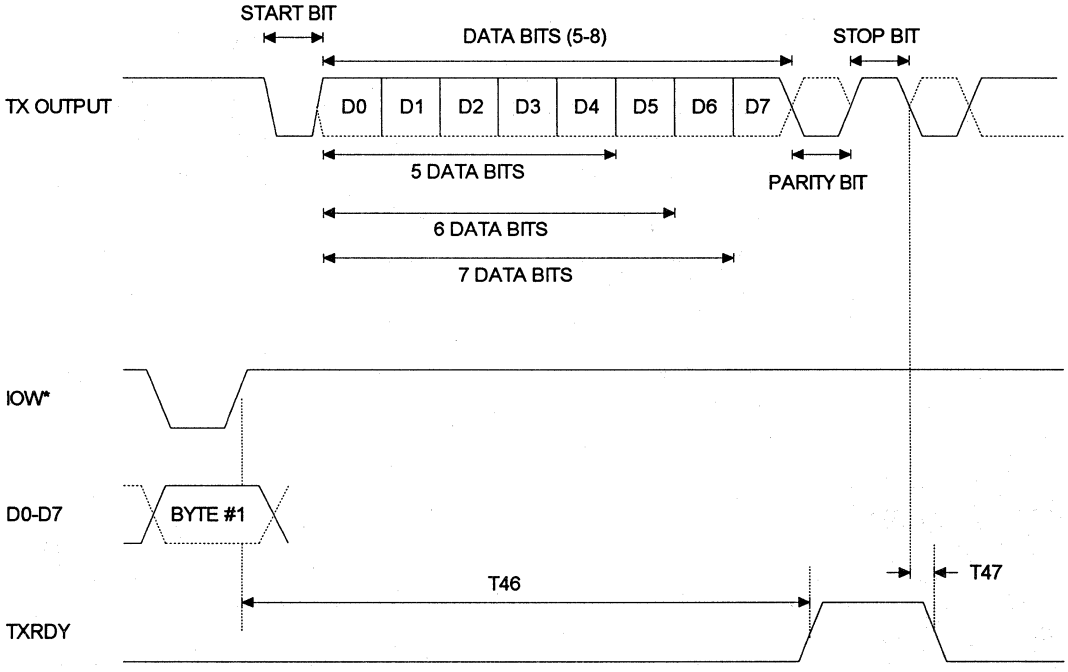
TRANSMIT TIMING



TXRDY TIMING FOR MODE "0"



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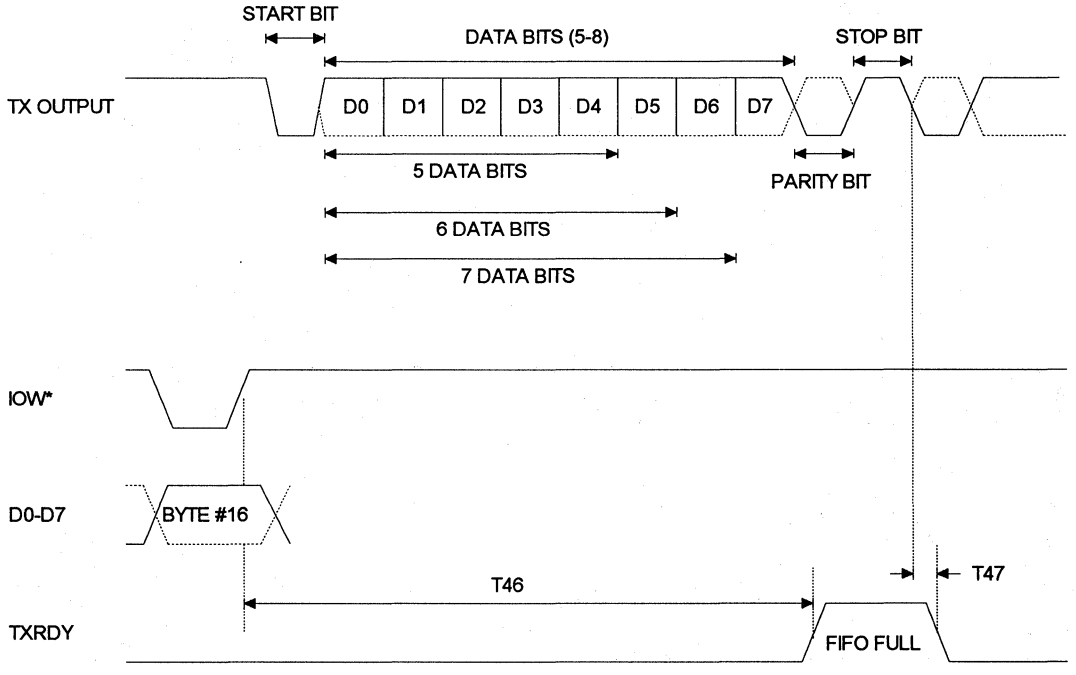
TXRDY TIMING FOR MODE "1"



STARTECH

ST68C554

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

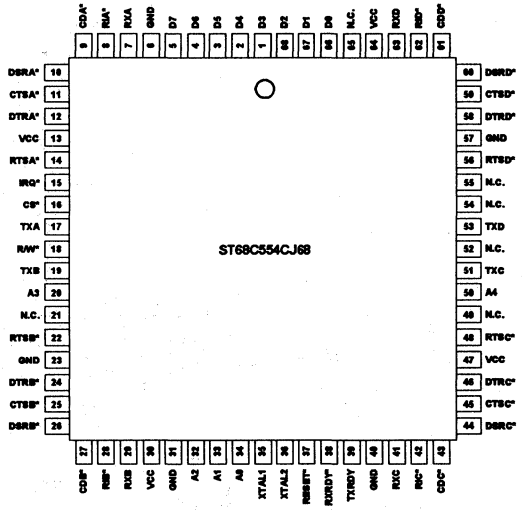
DESCRIPTION

The ST68C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST68C554 is an improved, quad version of the NS16550 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C554 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C554CJ68	PLCC	0° C to +70° C
ST68C554IJ68	PLCC	-40° C to +85° C

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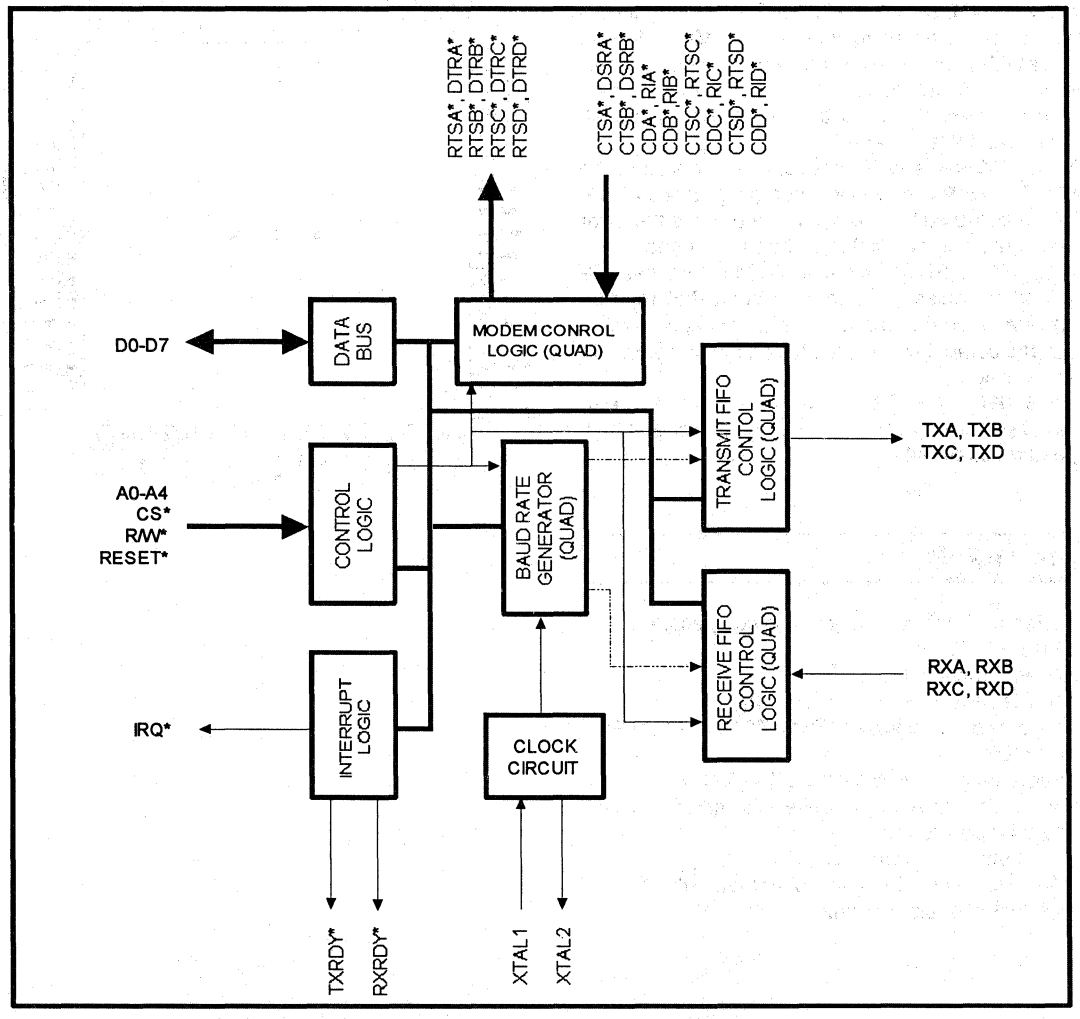
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66	I/O	Bi-directional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B RX C/D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST68C554 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B TX C/D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	16	I	Chip select (active low). A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	I	Crystal input 2. See XTAL1.
R/W*	18	I	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C554 data bus to the CPU.
CD A/B* CD C/D*	9,27 43,61	I	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23,31 40,57	O	Signal and power ground.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DSR A/B* DSR C/D*	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
RI A/B* RI C/D*	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTS A/B* RTS C/D*	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS A/B* CTS C/D*	11,25 45,59	I	Clear to send A-D. (active low) The CTS* signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmitter output.
A4	50	I	Address line 4. To select one of the four UARTS.
A3	20	I	Address line 3. To select one of the four UARTS.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
IRQ*	15	O	Interrupt output. (active low open collector) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR A/B* DTR C/D*	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			ST68C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET*	37	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.
TXRDY	39	O	Transmit ready (active high). This pin goes high when the transmit FIFO of the ST68C554 (any one) is full. It can be used as a single or multi-transfer DMA.
RXRDY*	38	O	Receive ready (active low). This pin goes low when the receive FIFO of the ST68C554 is full. It can be used as a single or multi-transfer DMA.

SERIAL PORT SELECTION GUIDE

CS*	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

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PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST68C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR
The ST68C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D
The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the IRQ* output pin.

IER BIT-0:
0=disable the receiver ready interrupt
1=enable the receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable the modem status register interrupt
1=enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST68C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C554 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example-A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

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ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-5:
These bits are not used and are set zero.

ISR BIT 6-7:
0=Normal mode.
1=FIFO's are enabled.

FIFO CONTROL REGISTER (FCR)
This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST68C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST68C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST68C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST68C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.

0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TX A-D) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high
1=force DTR* output to low

MCR BIT-1:
0=force RTS* output to high
1=force RTS* output to low

MCR BIT2-3:
x=not used

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D*, DSR A-D*, CD A-D*, and RI A-D*) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D*, RTS A-D* and MCR A-D bit-2,3 are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

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LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST68C554 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST68C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loopback mode. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D
ST68C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16xCLOCK %ERROR	DVISOR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST68C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
RTS A-D*	High
DTR A-D*	High
RxRdy*	High
TxRdy	Low
IRQ	Three state mode

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ST68C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR FIFOs	0/ FIFOs enabled	0/ enabled	0	0 priority	int priority bit-2	int priority bit-1	int status bit-0	int
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	Not used	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time from write or CS*	15			ns	
T_{14}	Write set up time	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	15			ns	
T_{17}	Write cycle delay	45			ns	
T_{18}	Data setup time	15			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{24}	Data hold time	0			ns	
T_{25}	Read cycle delay	25			ns	
Tr	Read cycle=T_{18}+T_{25}	105			ns	
T_{27}	Chip select pulse width	75			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			35	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from read (CS*) to reset RxRdy			1	µs	
T_{46}	Delay from write to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

* = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

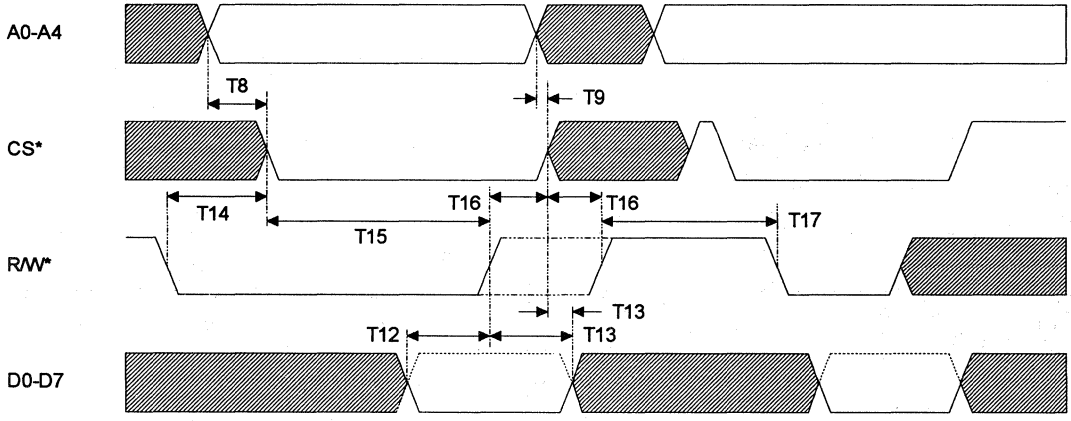
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

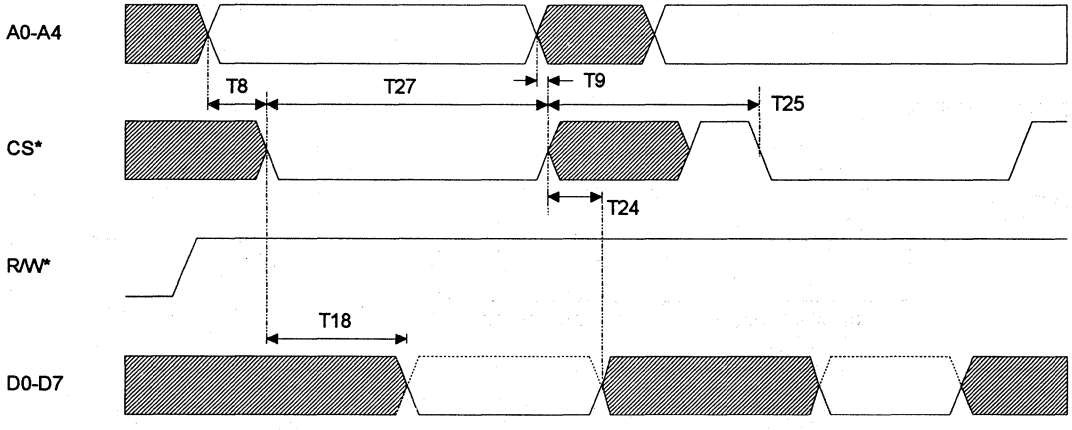
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg. power supply current		6		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING



GENERAL READ TIMING



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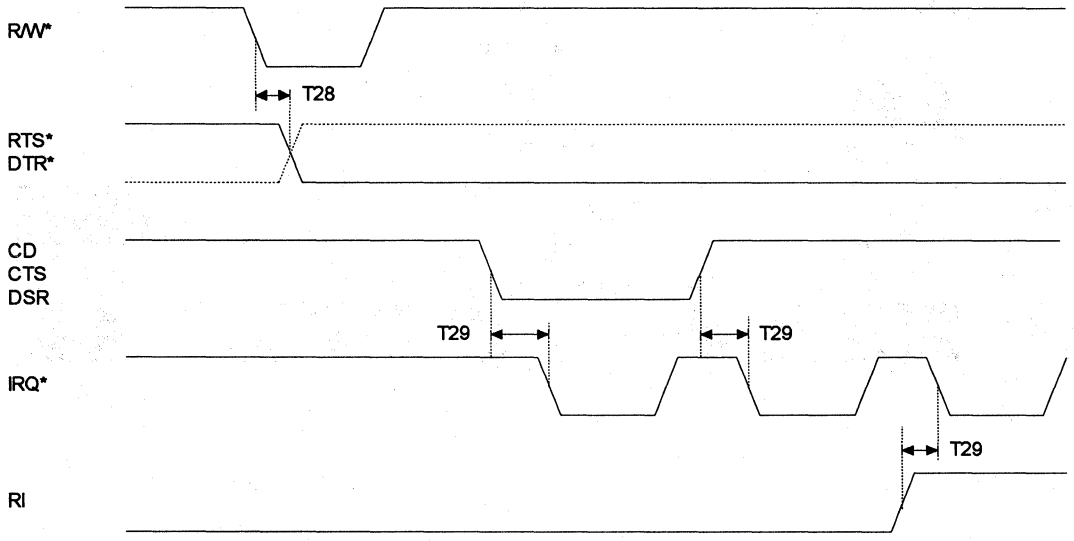
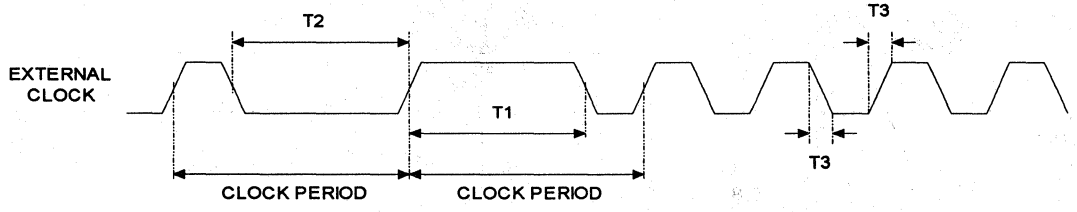
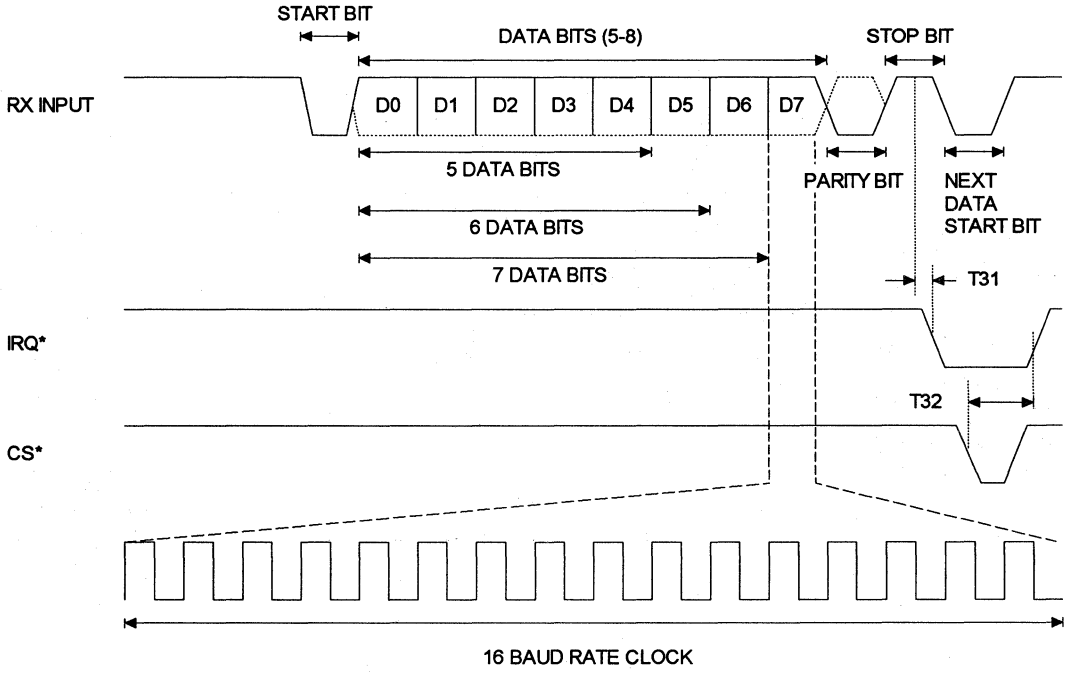
MODEM TIMING



CLOCK TIMING



RECEIVE TIMING



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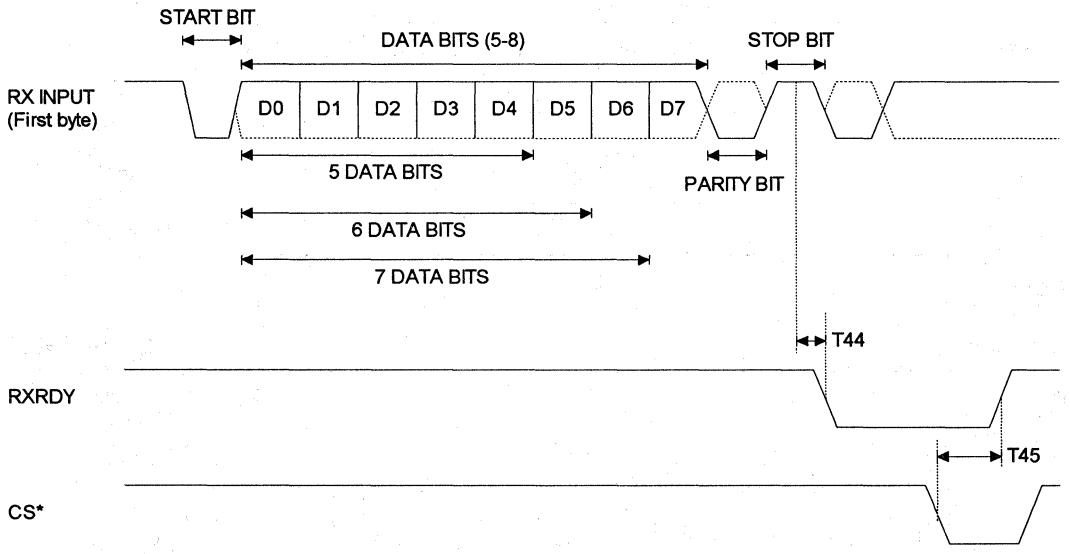
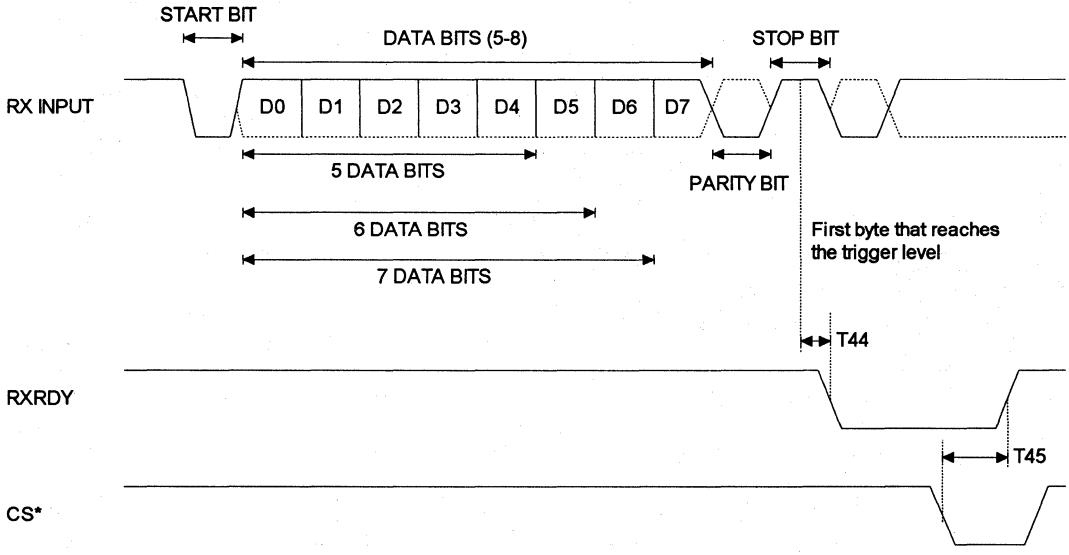
RXRDY TIMING FOR MODE "0"



RXRDY TIMING FOR MODE "1"



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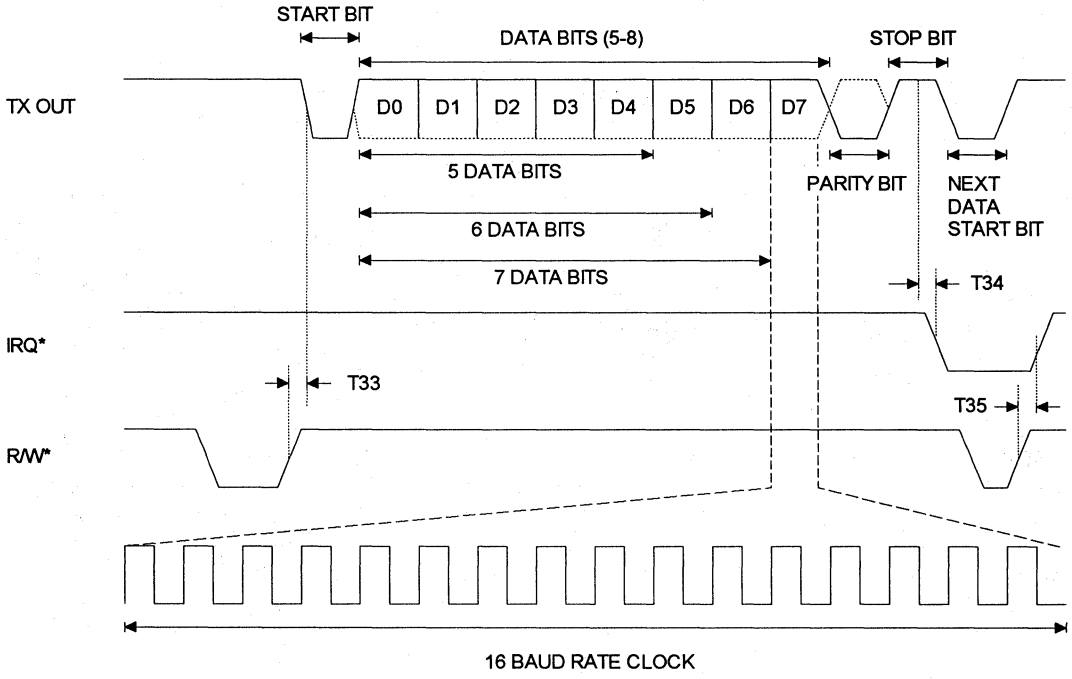
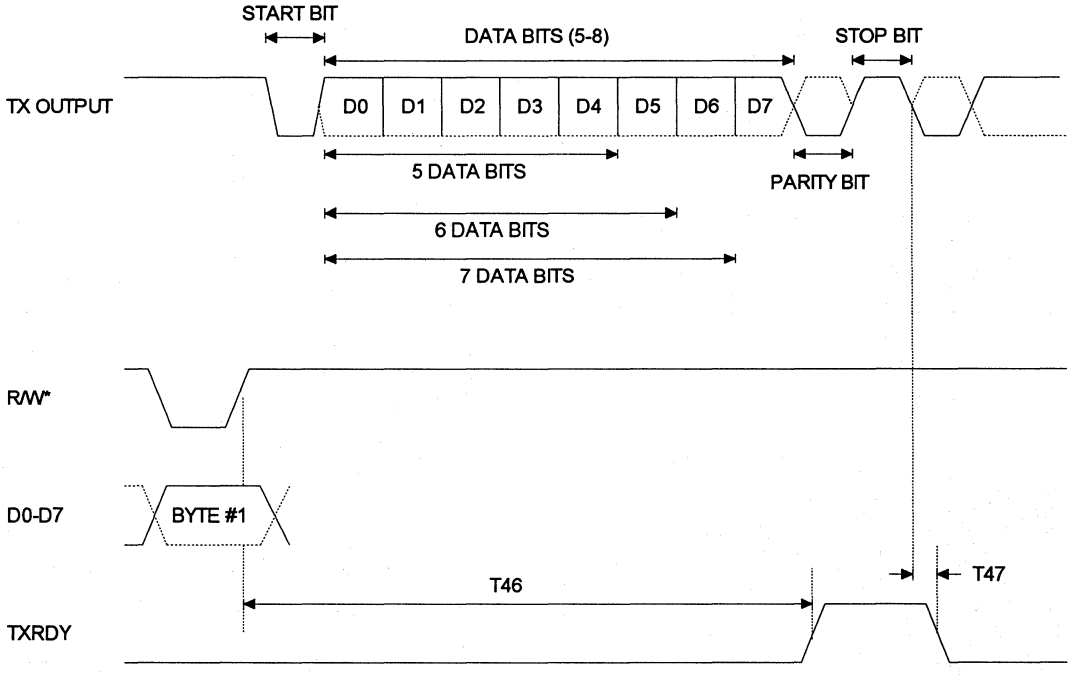
TRANSMIT TIMING

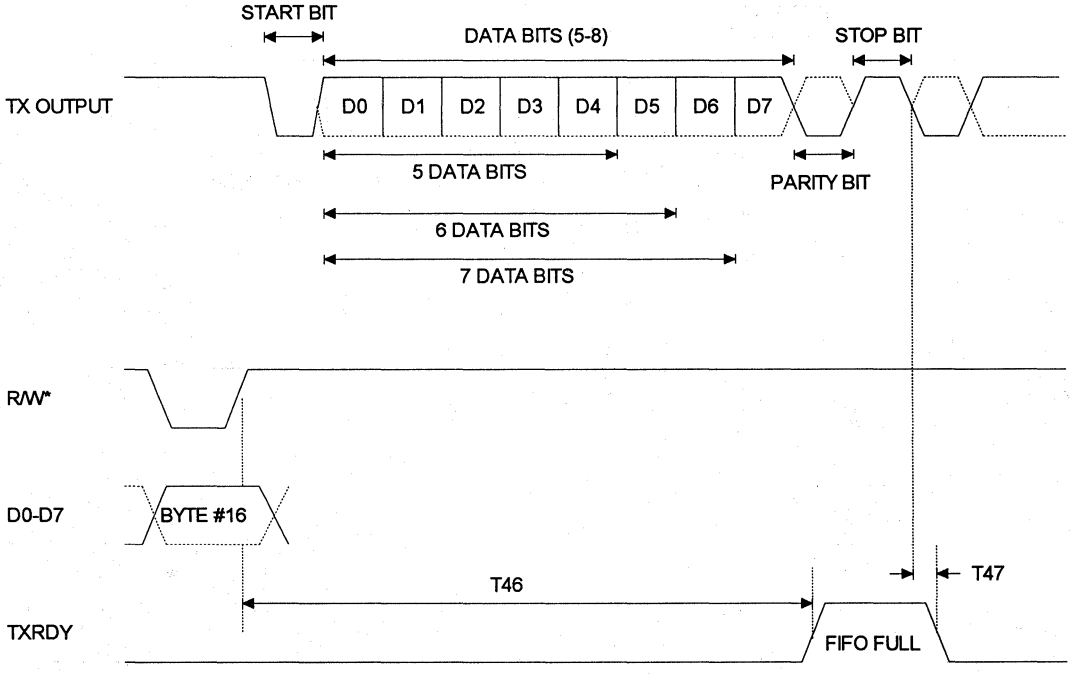


TXRDY TIMING FOR MODE "0"



ST68C554

TXRDY TIMING FOR MODE "1"



STARTECH

EVALUATION KIT AVAILABLE

ST16C452AT
ST16C452PS

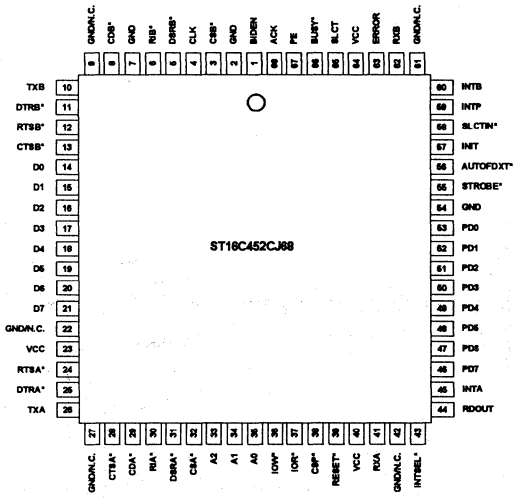
Printed February 23, 199

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

The ST16C452 is a dual universal asynchronous receiver and transmitter with a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.
STARTECH ST16C452PS provides additional features to control the printer port direction without any additional external logic.
The ST16C452 is an improved version of the VL16C452 UART with higher operating speed and lower access time. The ST16C452 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C452 provides internal loop-back capability for on board diagnostic testing.
The ST16C452 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Pin to pin and functional compatible to VL16C452, WD16C452
- Fully compatible with all new bi-directional PS/2 printer port registers.
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- Software compatible with INS8250, NS16C450
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C452CJ68	PLCC	0° C to + 70° C
ST16C452IJ68	PLCC	-40° C to + 85° C

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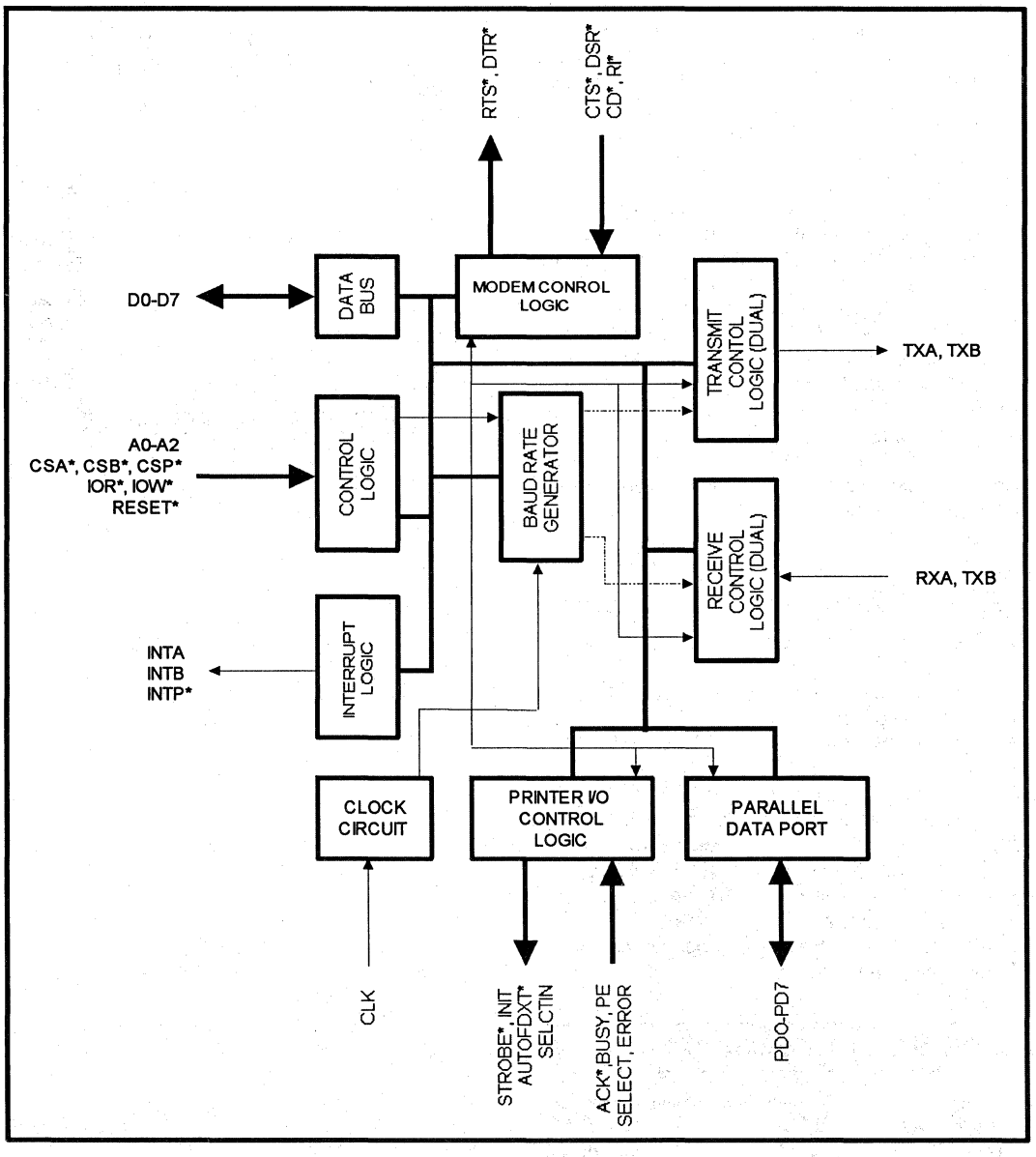
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input mode for ST16C452AT and software controlled mode (input/output) to ST16C452PS. Allow sets the ST16C452 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C452 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C452 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			telephone line.
CD A/B*	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR A/B*	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B*	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C452 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C452 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55*	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56*	I/O	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or initialize line printer (open drain active low). When this signal is low it causes the printer to be initializes.
SLCTIN*	58*	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low it selects the printer.
ERROR*	63*	I	General purpose input or line printer error (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
PE	67*	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68*	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,22 42,54,61	O	Signal and power ground. All ground pins are connected internally.
VCC	23,40,64	I	Power supply input. All power pins are connected internally.

* Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS A/B

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C452 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C452 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

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MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
This bit is used for internal loop-back mode, and is not used for regular operation.

MCR BIT-3:
0= sets the INT output pin to three state mode.
1= enables the INT output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2,3are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to MCR bit-3 during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C452 provides a temporary data register to store 8 bits of information for variable use.

SIGNAL	RESET STATE
TX	High
RTS*	High
DTR*	High
INT	Three state mode

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C452 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	BIT-0=1, ISR BITS 1-7=0
LCR	BITS 0-7=0
MCR	BITS 0-7=0
LSR	BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	BITS 0-3=0, MSR BITS 4-7=input signals

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PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

ST16C452XX	CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
ST16C452AT	X	0	X	Output mode
ST16C452PS	X	0	AA Hex	Input mode
ST16C452PS	X	0	55 Hex	Output mode
ST16C452AT	X	1	X	Input mode
ST16C452PS	0	1	X	Output mode
ST16C452PS	1	1	X	Input mode

PRINTER PORTREGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

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CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output. I/O select register and control register bit-5 are only available for ST16C452PS parts.

ST16C452 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	High, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

ST16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt (PS only)		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
	0=Output (PS only) 1=Input (PS only) X= AT only		0=INTP output disabled 1=INTP output enabled				

ST16C452AT
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AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data set up time	15			ns	
T_{13}	IOW* delay from chip select	10			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{CLK}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7-PD0 setup time	10			ns	
T_{41}	PD7-PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1 * = Baudout* cycle

ST16C452AT
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ABSOLUTE MAXIMUM RATINGS

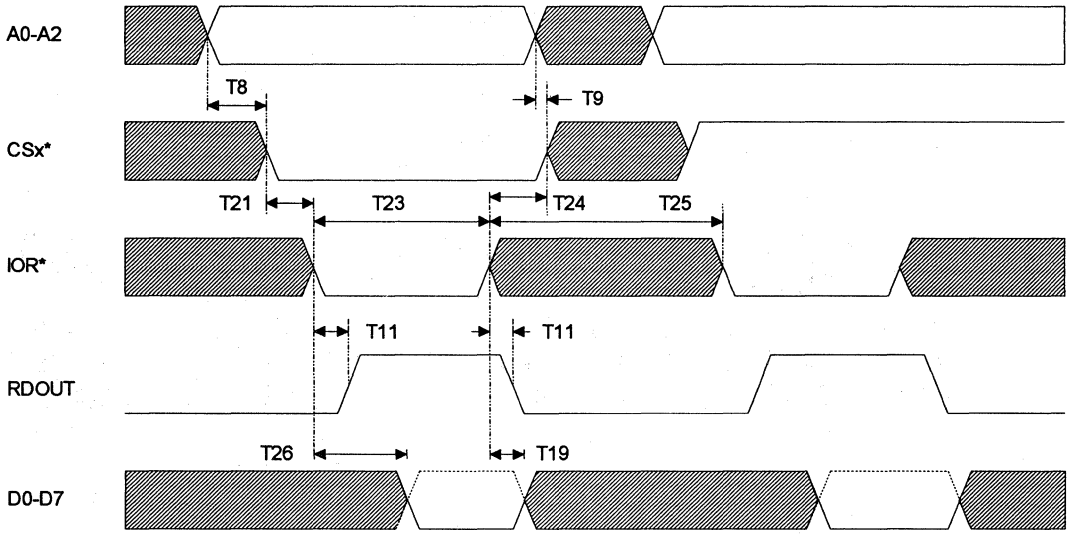
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

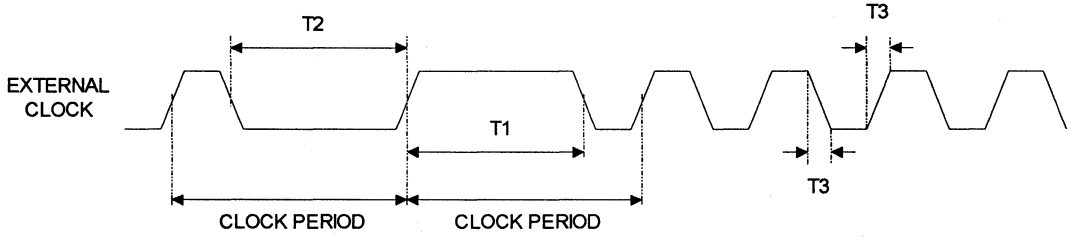
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all the outputs
I_{CC}	Avg. power supply current		12		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	4		15	kΩ	* Marked pins

GENERAL READ TIMING



CLOCK TIMING



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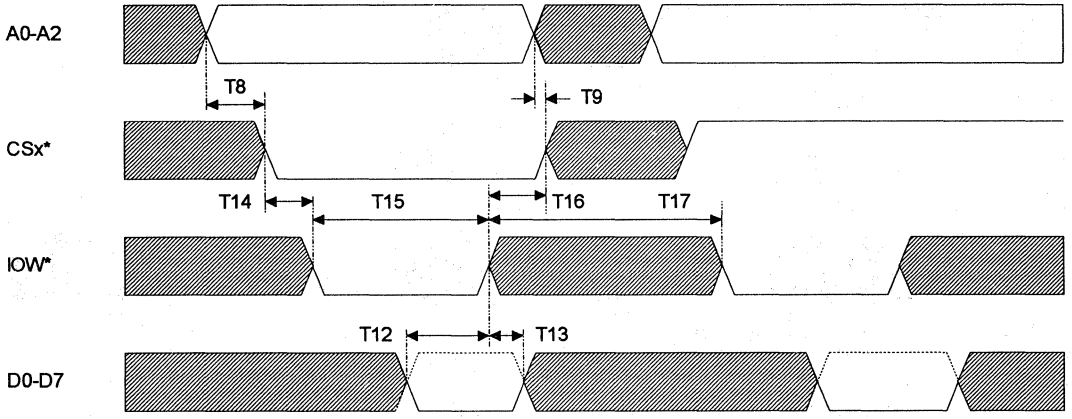
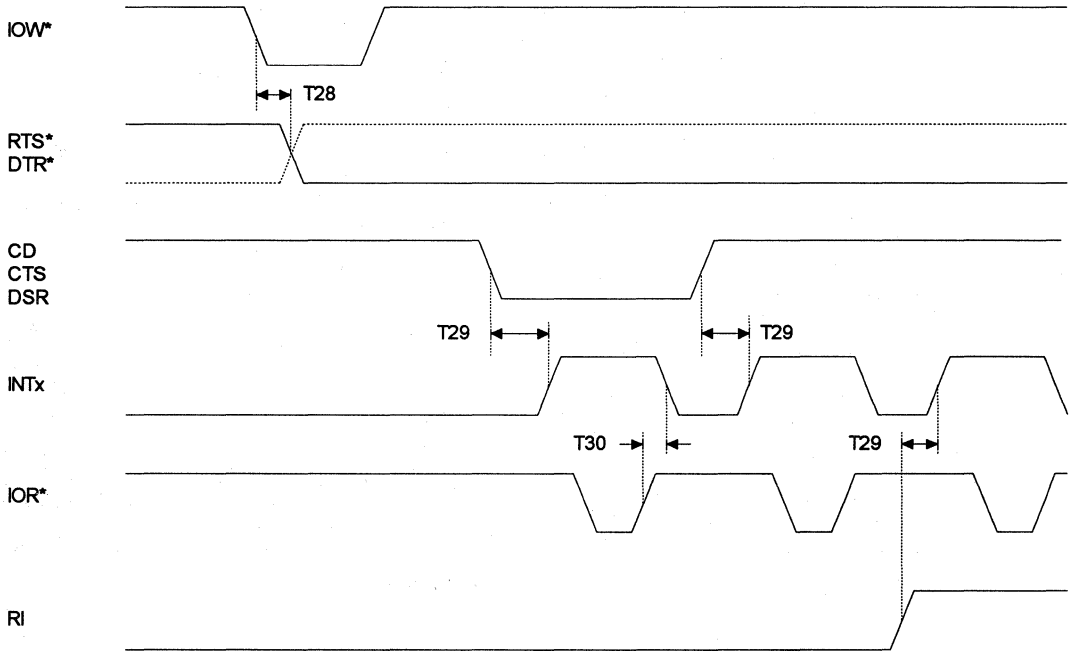
GENERAL WRITE TIMING



MODEM TIMING



ST16C452AT
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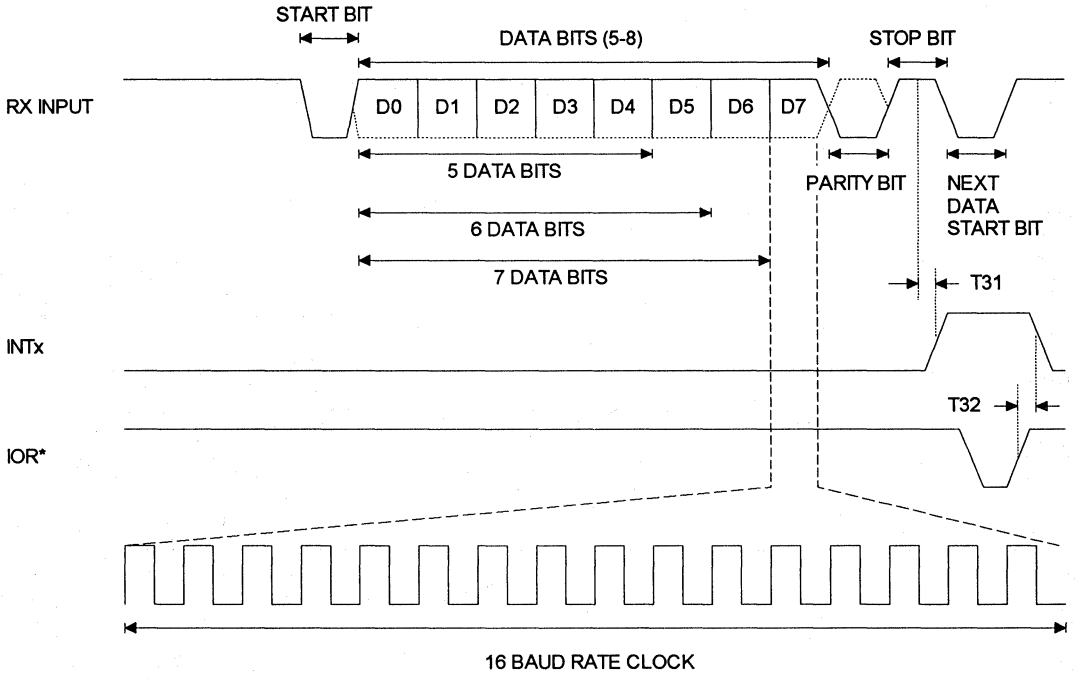
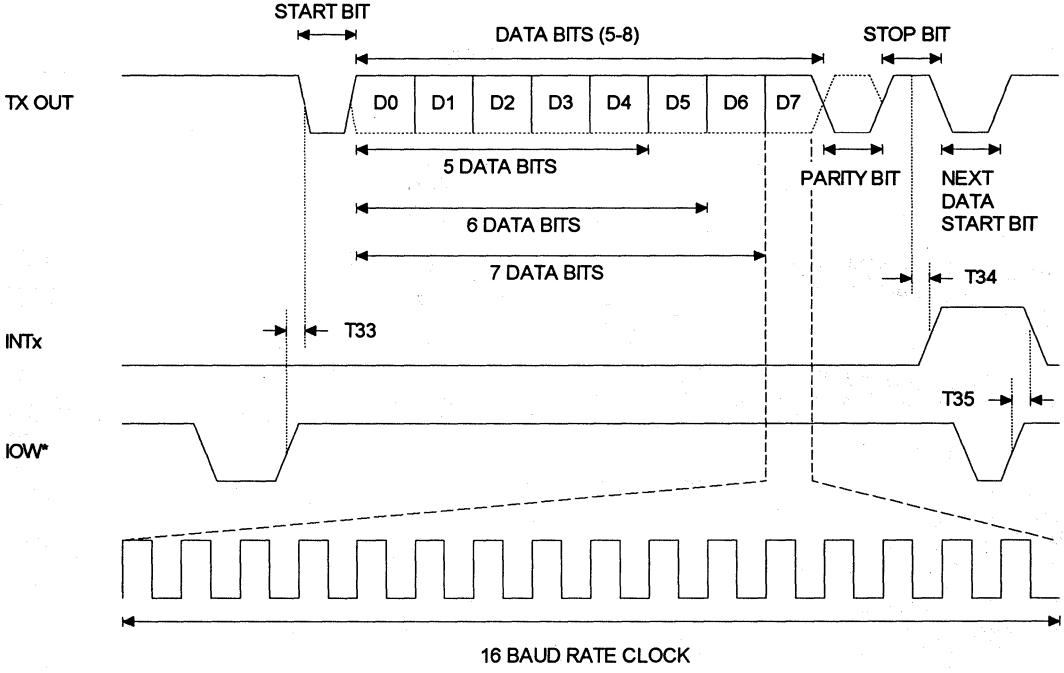
RECEIVE TIMING



TRANSMIT TIMING



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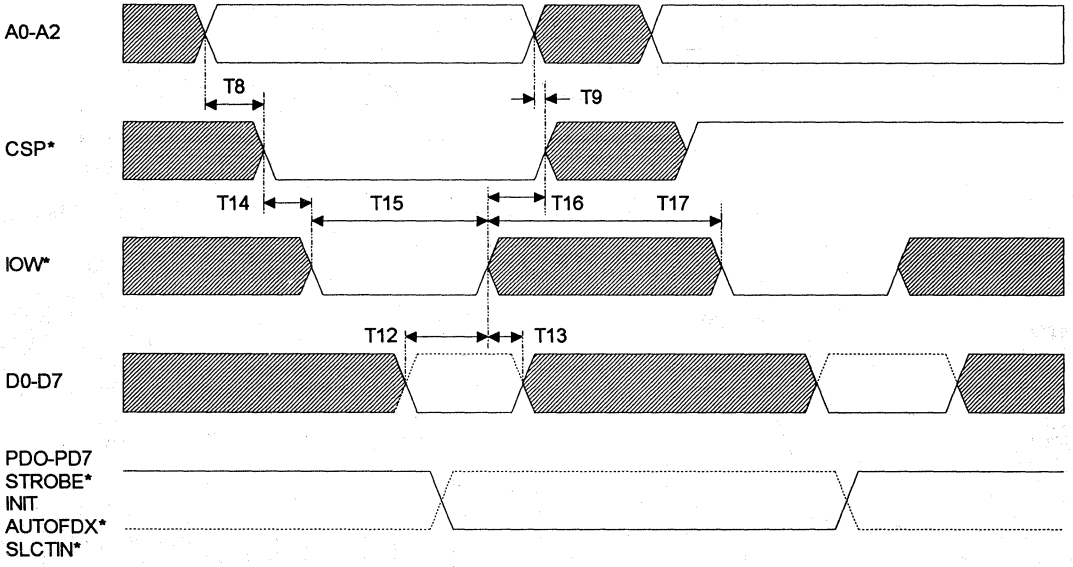
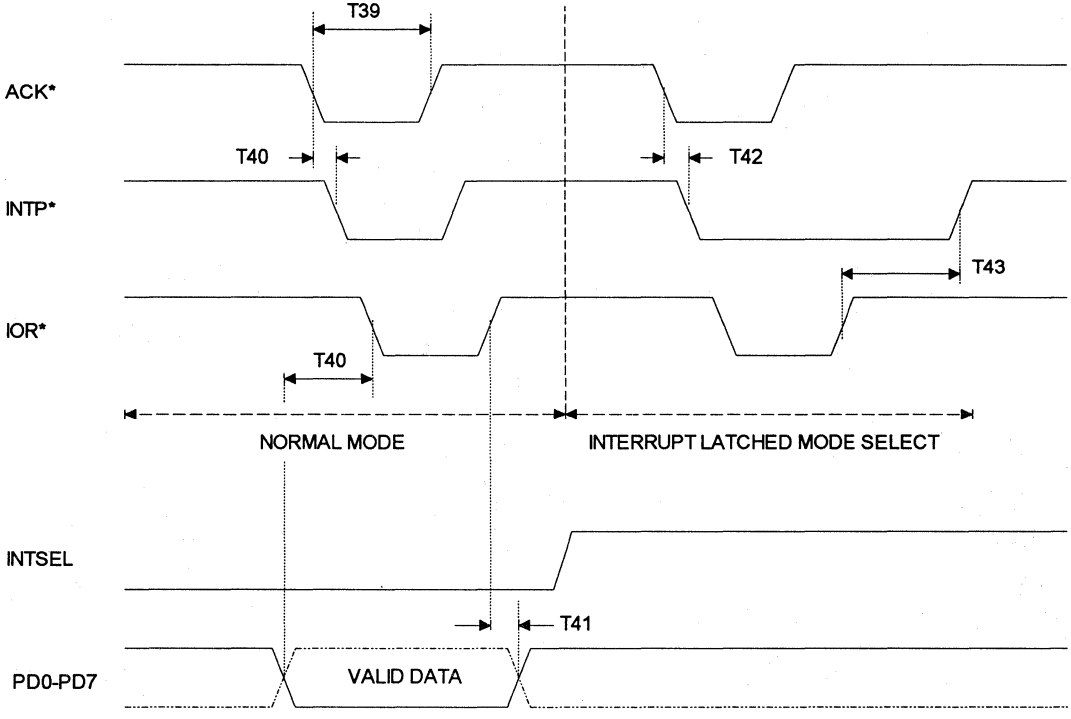
PARALLEL PORT GENERAL WRITE TIMING



PARALLEL PORT READ TIMING



ST16C452AT
ST16C452PS

STARTECH

EVALUATION KIT AVAILABLE

ST16C552

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT

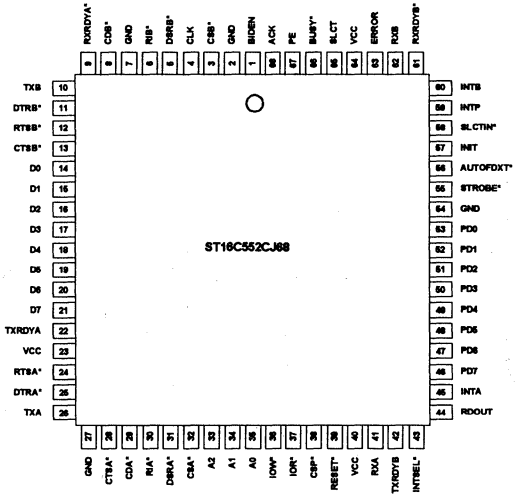
DESCRIPTION

The ST16C552 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C552 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C552 provides internal loopback capability for on board diagnostic testing.

The ST16C552 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Pin to pin and functional compatible to VL16C552, WD16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C552CJ68	PLCC	0° C to + 70° C
ST16C552IJ68	PLCC	-40° C to + 85° C

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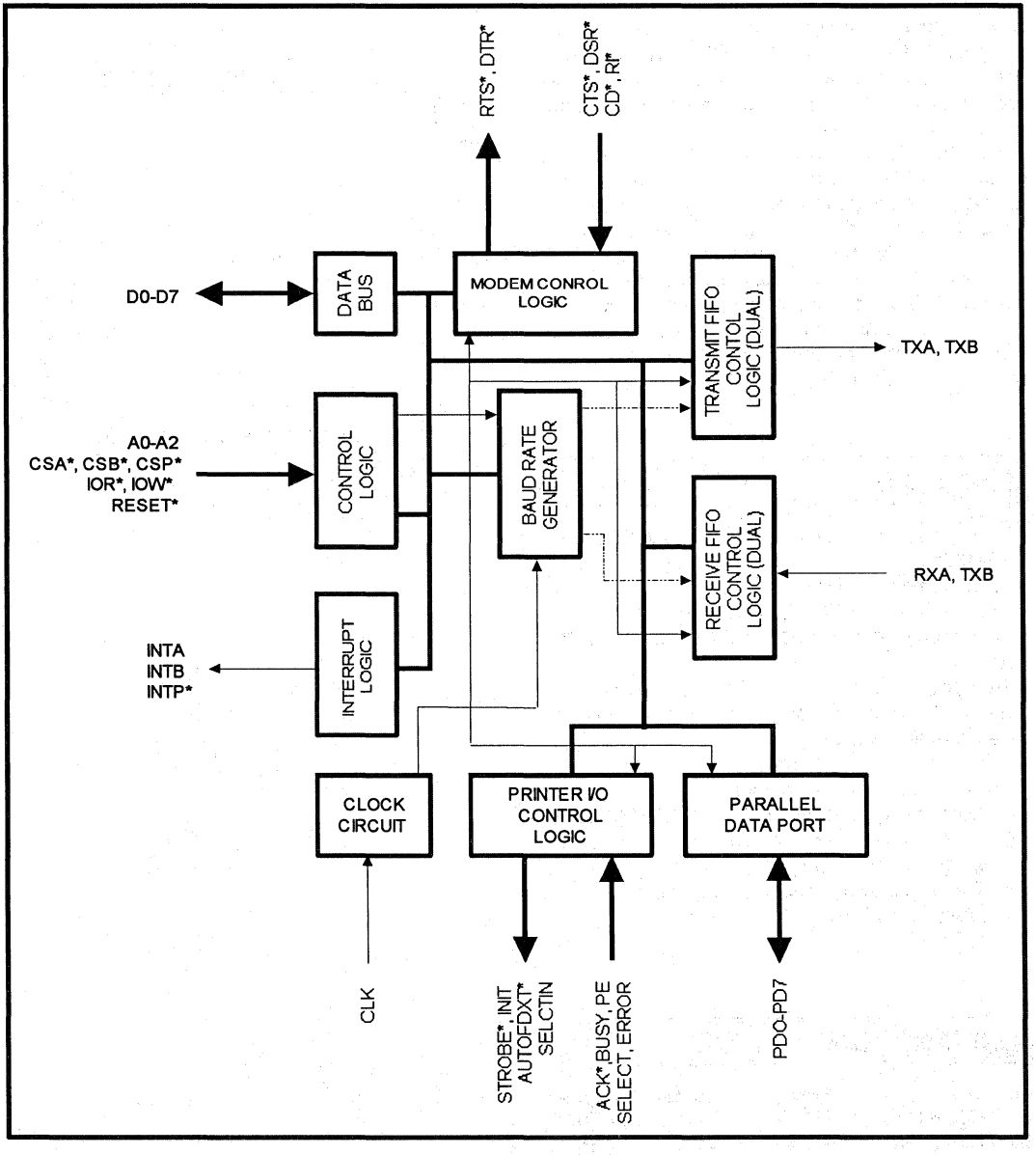
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C552 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C552 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C552 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD A/B*	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR A/B*	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B*	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY A/B	22,42	O	Transmit ready A/B (active high). This pin goes high when the transmit FIFO of the ST16C552 is full. It can be used as

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			a single or multi-transfer.
RXRDY A/B*	9,61	O	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C552 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55*	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56*	I/O	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or initialize line printer (open drain active low). When this signal is low, it causes the printer to be initialized.
SLCTIN*	58*	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.
ERROR*	63*	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

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Symbol	Pin	Signal Type	Pin Description
PE	67*	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68*	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,54 27	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

* Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C552 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C552 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C552 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

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1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

ST16C552

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C552 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C552 provides a temporary data register to store 8 bits of information for variable use.

ST16C552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

SIGNALS	RESET STATE
TX	High
RTS*	High
DTR*	High
INT	Three state mode
RXRDY*	High
TXRDY	Low

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

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PRINTER PORT REGISTER DESCRIPTIONS

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C552 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	High, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	X	Input mode

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ST16C552 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
	0=Output 1=Input		0=INTP output disabled 1=INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1 * = Baudout* cycle

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ABSOLUTE MAXIMUM RATINGS

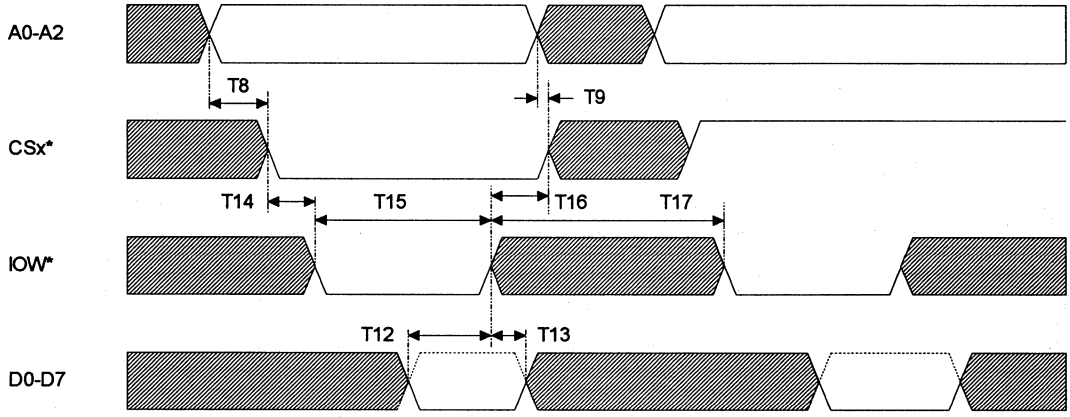
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

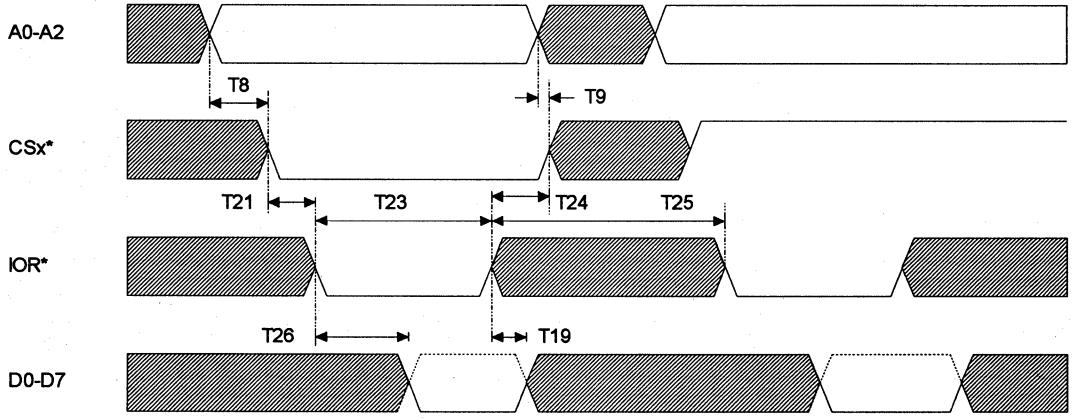
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current		12		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	4		15	kΩ	*Marked pins

GENERAL WRITE TIMING



GENERAL READ TIMING



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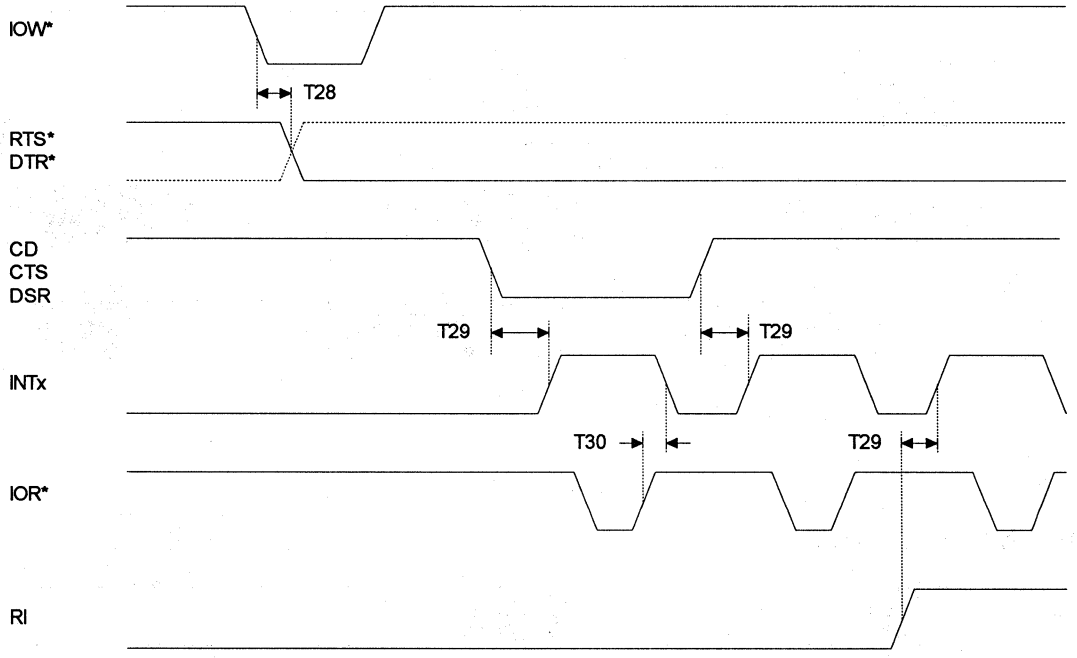
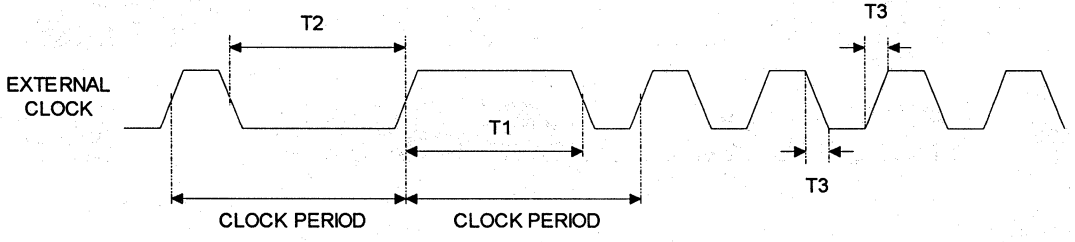
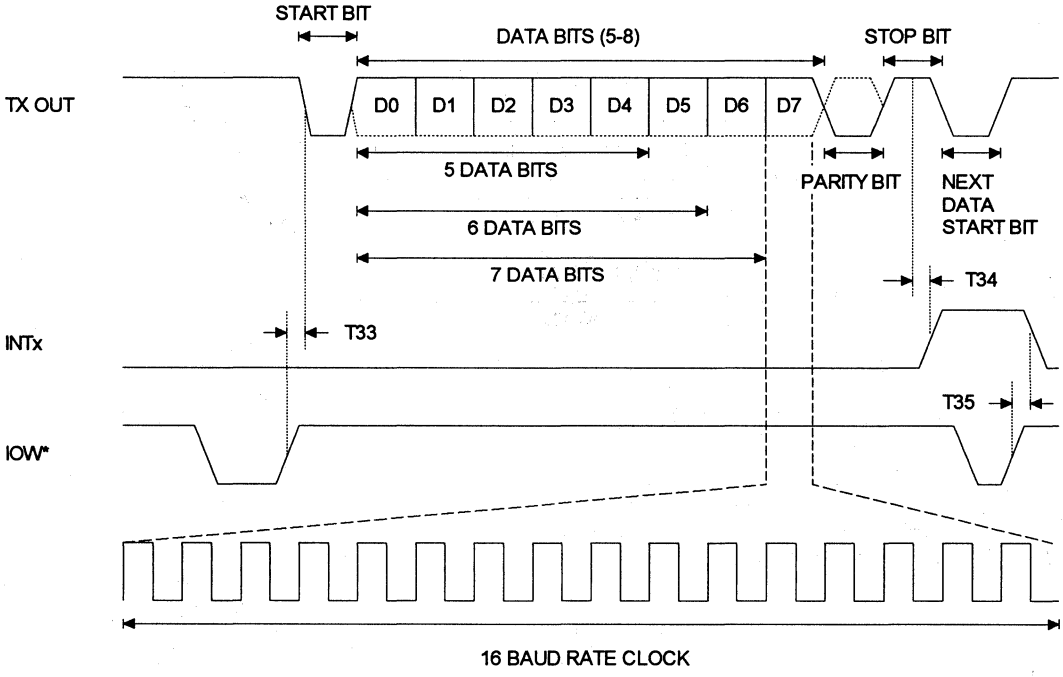
MODEM TIMING



CLOCK TIMING



TRANSMIT TIMING



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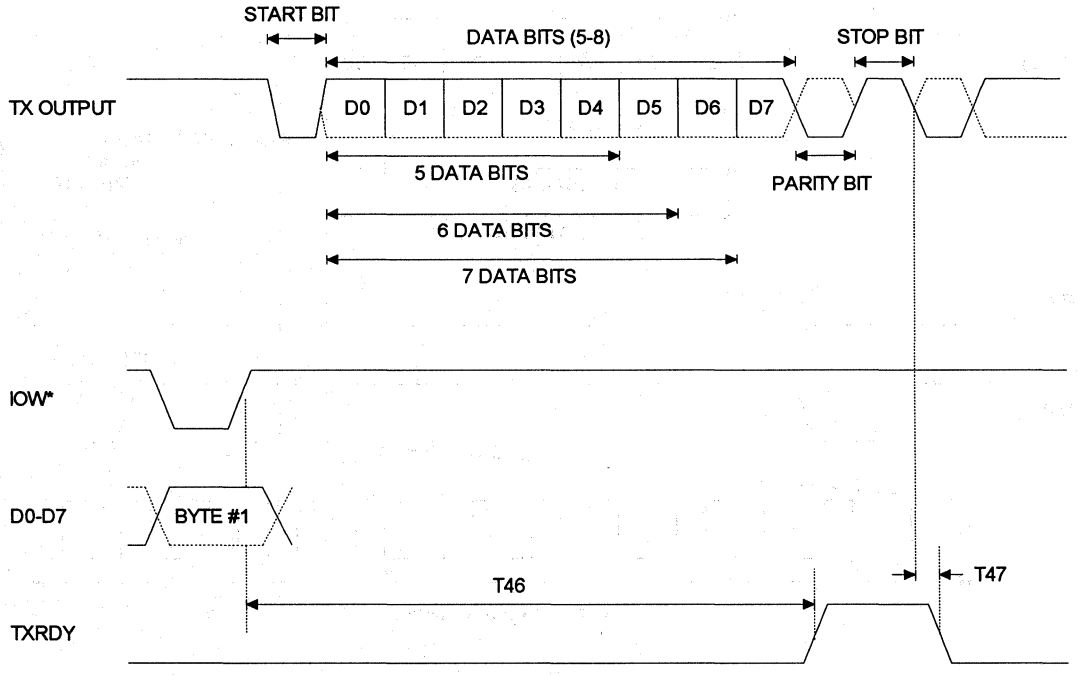
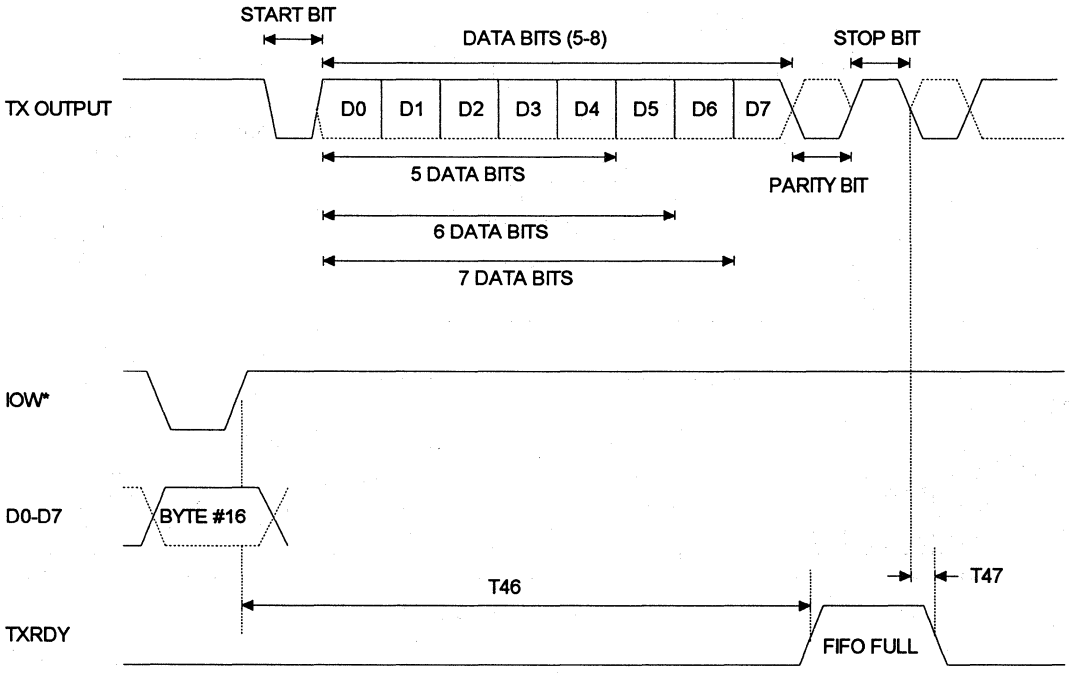
TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"



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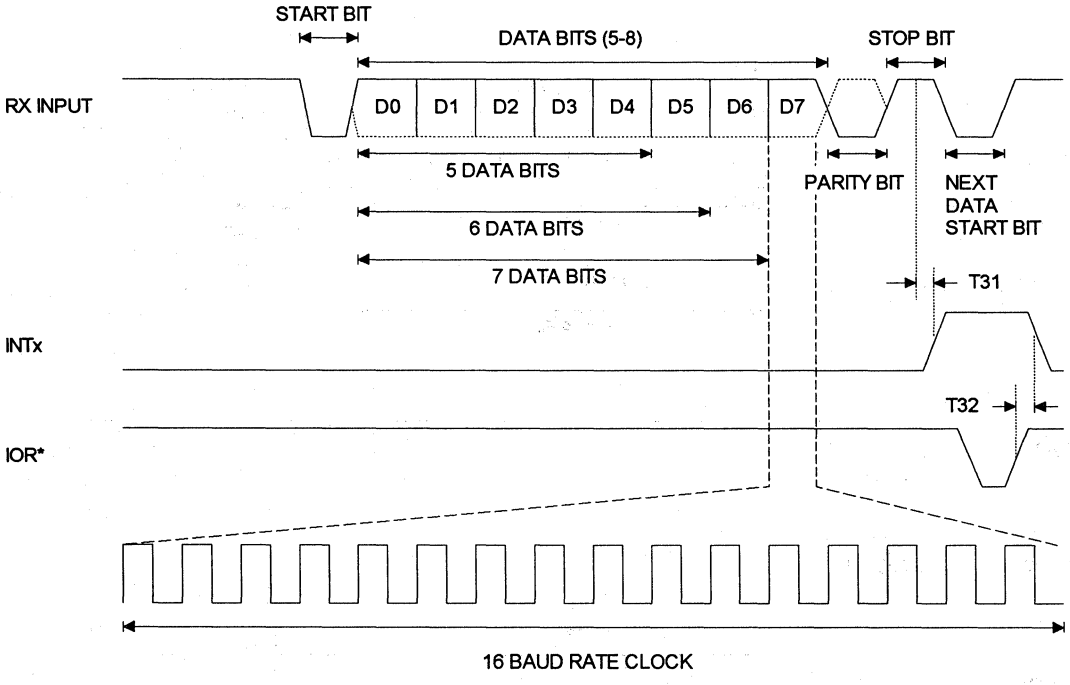
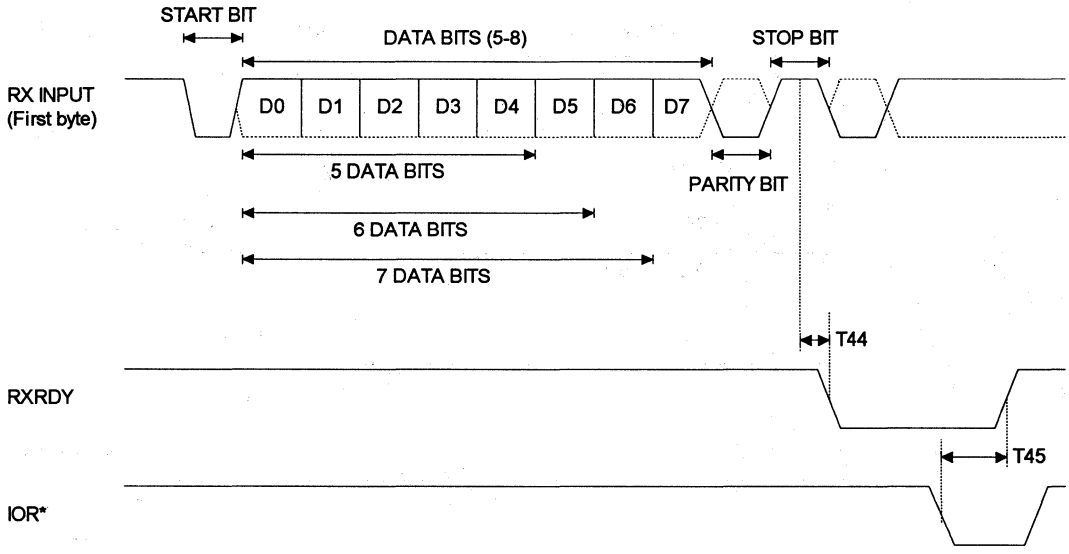
RECEIVE TIMING



RXRDY TIMING FOR MODE "0"



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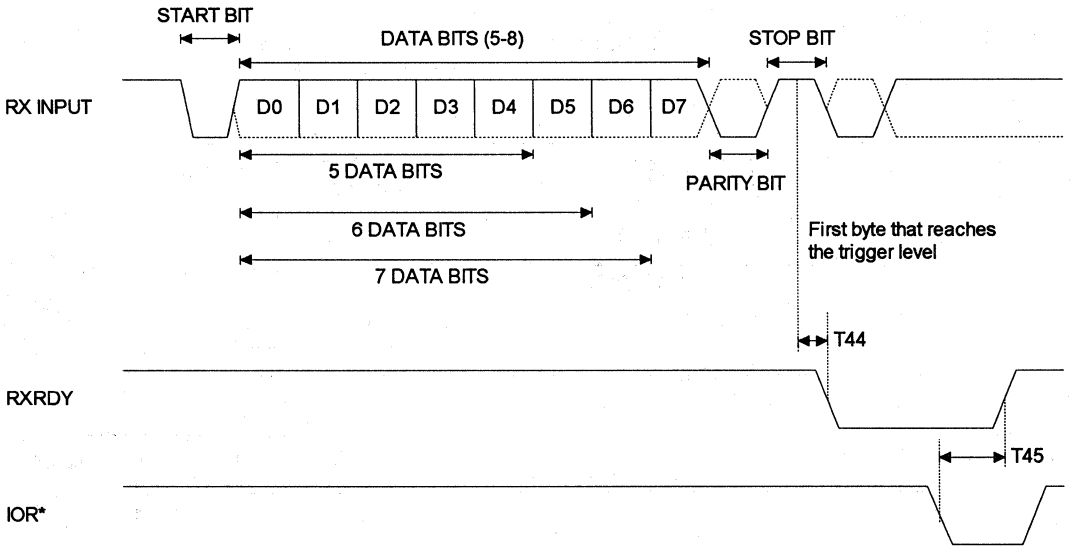
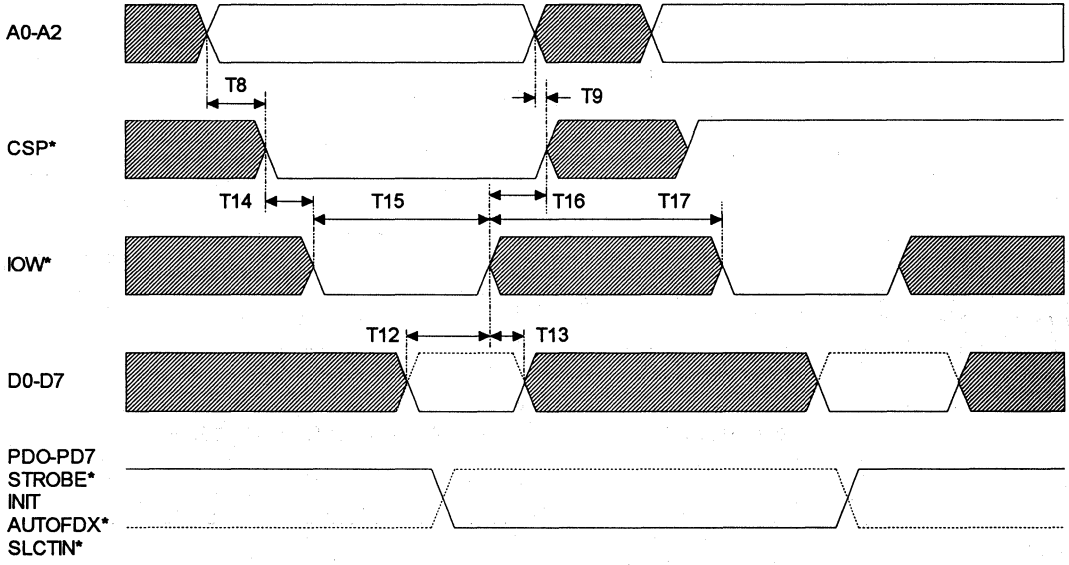
RXRDY TIMING FOR MODE "1"



PARALLEL PORT GENERAL WRITE TIMING



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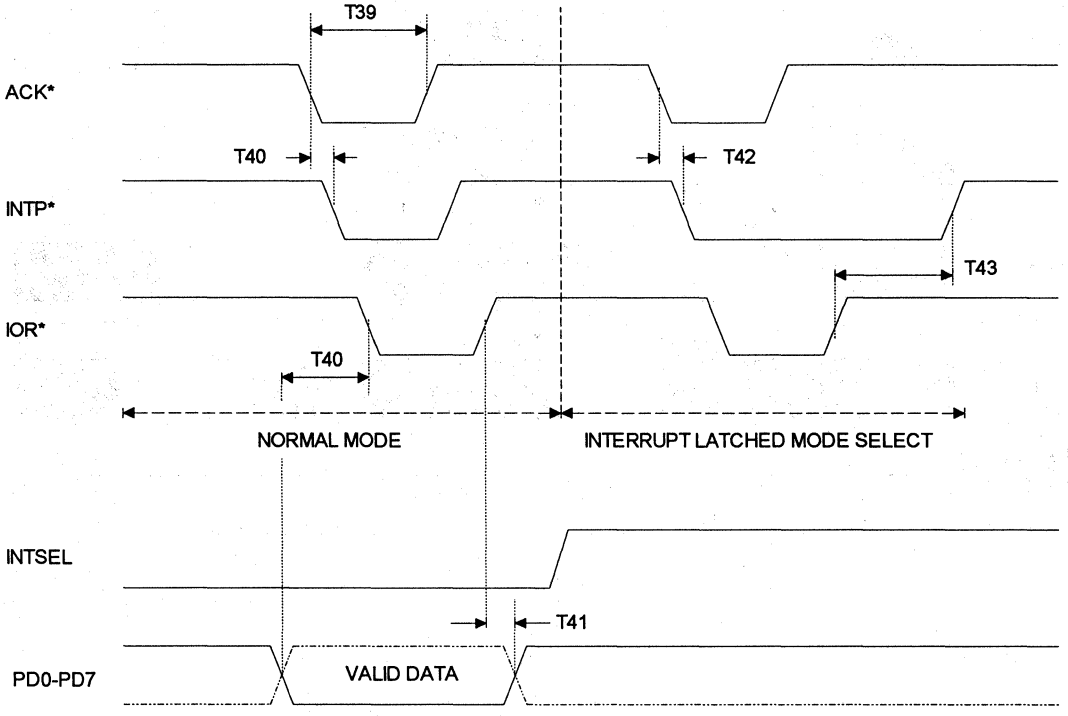
PARALLEL PORT READ TIMING



STARTECH

EVALUATION KIT AVAILABLE

ST16C553

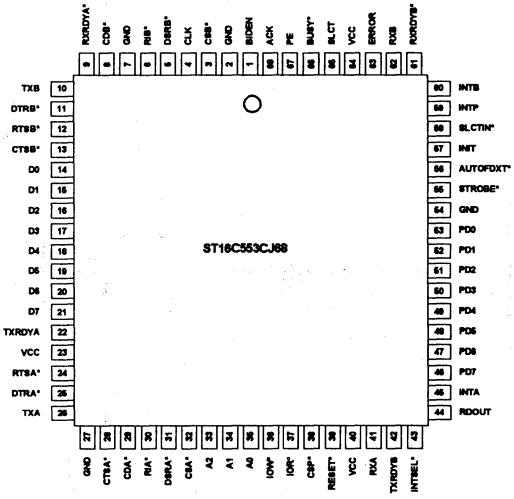
Printed February 23, 199

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT WITH 83 BYTE FIFO

DESCRIPTION

The ST16C553 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bi-directional CENTRONICS type parallel printer port with 83 bytes of FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The ST16C553 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C553 provides internal loopback capability for on board diagnostic testing.
The ST16C553 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Pin to pin and functional compatible to VL16C552, WD16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- 83 bytes of printer output FIFO
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C553CJ68	PLCC	0° C to + 70° C
ST16C553IJ68	PLCC	-40° C to + 85° C

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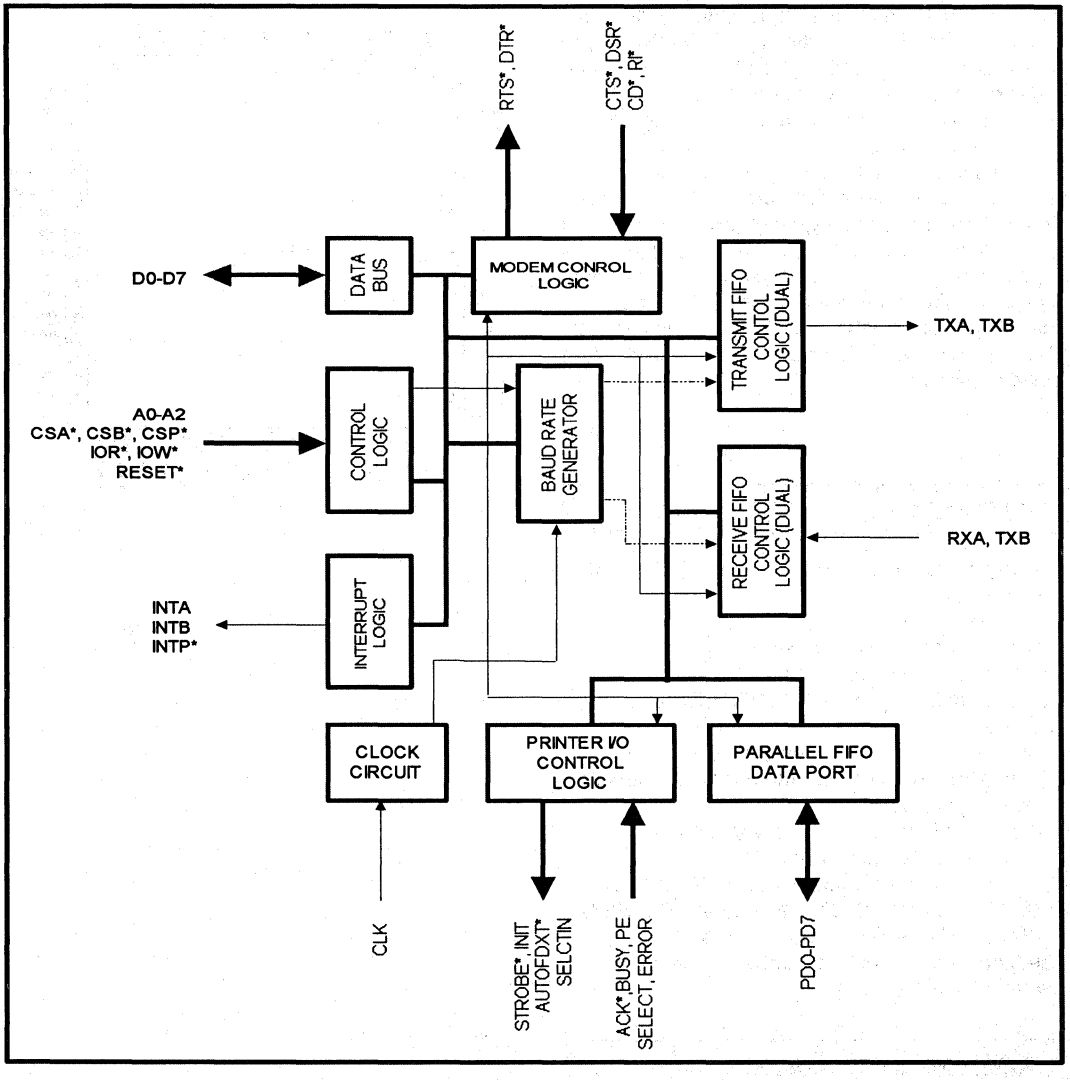
ST16C553

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C553 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C553 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C553 to en/disable the external transceiver or logic's.
RESET*	39	I	Master reset (active low). A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD A/B*	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR A/B*	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C553 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B*	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C553 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY A/B	22,42	O	Transmit ready A/B (active high). This pin goes high when the transmit FIFO of the ST16C553 is full. It can be used as

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			a single or multi-transfer.
RXRDY A/B*	9,61	O	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C553 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55*	I/O	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
AUTOFDXT*	56*	I/O	General purpose I/O or automatic line feed (open drain active low). When this pin this signal is low, the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	58*	I/O	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.
ERROR*	63*	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
PE	67*	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68*	I	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,54	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

* Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C553 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register interrupt	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0 0 1	***DLM***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C553 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C553 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C553 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2^{16} -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C553 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C553 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

***RECEIVE TIME-OUT:**
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C553 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.

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1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C553 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C553 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C553 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C553 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

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LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C553 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C553 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-

ΓER FUNCTIONAL DESCRIPTION

Γ16C553 parallel port is designed to operate as nal CENTRONICS printer interface. The port ins 83 byte FIFO that may be enabled via bit-7 ; Alternate Function Register (AFR). After reset, IFO is disabled and the part will function identical ə ST16C552. Once the FIFO is enabled via AFR , the port will enter FIFO mode after the first byte ata is strobed to the printer and the printer re- nds with either an ACK* or BUSY signal.

; ST16C553 will remain in FIFO mode until the part eset or INIT is brought low. While in FIFO mode, a transfer to the printer will be controlled by the nter without any user intervention. The printer port o contains a FIFO byte counter that maintains a nt of the number of bytes remaining in the FIFO. e FIFO and the FIFO byte counter are cleared by a et or by a change of state of the INIT pin. All FIFO ated timing is derived from the clock input to pin 4 he part.

pecial parallel port write / read mode is activated n INIT is held low, either by writing a "0" to Control ister bit-2 or by forcing the INIT pin low. In this le the FIFO read pointer is advanced by reading arallel port instead of the ACK* or BUSY signals. STROBE* output is forced high. This allows the to perform write to parallel port and read from el port operations without strobing data to the r.

ing an INIT, the parallel port will not be in the node. Control Register bit-0 is used as the E*, Status Register bit-7 is the inverse of the ignal, and INTP* is derived from ACK*. The n into FIFO mode will occur after the first * is generated and the printer responds with ACK* or BUSY. In FIFO mode, STROBE* is automatically and writing to Control Regis- s no effect on STROBE*. Alternate Func- r bit 0-2 are used to control the delay and ROBE*. Handshaking between the printer 6C553 may be controlled by bit-3 of the ction Register. Setting this bit to a "1" will se of BUSY instead of ACK* for FIFO reading and interrupt control. INTP* will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read to Fifo Byte Count Register (FBCR) should only be performed minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL* pin. If this pin is tied high, a latched interrupt will result. In this mode, INTP* will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL* pin is tied low, INTP* will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL* pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INTP* pin may be inverted by setting Alternate Function Register bit-6 high.

The ST16C553 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INTP* output can be selected as FIFO full or FIFO empty interrupt.

back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C553 provides a temporary data register to store 8 bits of information for variable use.

ST16C553 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
AFR	AFR BIT 0-7=0

BAUD RATE GENERATOR TABLE (1.8432 MHz CLOCK

BAUD RATE	16 x CLOCK DIVISOR
50	2304
110	1047
150	768
300	384
600	192
1200	96
2400	48
4800	24
7200	16
9600	12
19.2K	6
38.4K	3
56K	2
115.2K	1

SIGNALS	RESET STATE
TX	High
RTS*	High
DTR*	High
INT	Three state mode
RXRDY*	High
TXRDY	Low

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGIS
0	1	I/O SELECT REGISTER	STATUS RE
1	0	CONTROL REGISTER	COMMANI
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYT

* Reading the status register will reset the INTP output.

PRINTER PORT REGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
This bit is set to "1" normally except when interrupt is selected as FIFO empty via AFR.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR input state.
0= ERROR input is in low state
1= ERROR input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY or FIFO full/ FIFO empty signal.

ST16C552 mode (FIFO is not enabled).
0= BUSY input is in high state
1= BUSY input is in low state

FIFO is enabled.
0= FIFO is full
1= One or more empty locations in FIFO

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

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COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled (three state mode)
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INTP* and change interrupt functions.

AFR BIT 0-2:
Timing select.
The STROBE* delay and width can be controlled by these bits.

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
1	0	0	3	2
1	0	1	5	4
1	1	0	5	4
1	1	1	9	8
0	0	0	6	4
0	0	1	10	8
0	1	0	10	8
0	1	1	18	16

AFR BIT-3:
Interrupt source.
0= ACK* input pin is selected as printer handshaking source
1= BUSY input pin is selected as printer handshaking source

AFR BIT 4-5:
Interrupt type. State of the INTP* output pin can be selected for one of the following options.

Bit-5	Bit-4	INTP* output	SR bit-0	SR bit-6
0	0	Normal mode	1	BUSY*
0	1	FIFO empty	1	FIFO empty
1	0	FIFO full	1	FIFO full
1	1	FIFO empty	0	FIFO empty

AFR BIT-6:
INTP* output polarity.
0= Normal. INTP* output follows the ACK* input
1= Inverted INTP* output

AFR BIT-7:
FIFO enable / disable function.
0= FIFO is disabled(default mode). The ST16C552 compatible mode.
1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR)

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:
FIFO byte count. Number of characters left in FIFO.

FBCR BIT-7:
FIFO state.
0= FIFO is enabled
1= FIFO is disabled

I/O SELECT REGISTER

Software controlled I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C553 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	High, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	X	Input mode

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ST16C553 PRINTER PORT REGISTER CONFIGURATIONS

A2 A1 A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
X 0 0	PR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X 0 1	STR	BUSY*/ Alternate function	ACK	PE	SLCT	ERROR	IRQ	1	1
X 0 1	I/O	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
X 1 0	COM	1	1	1	IRQ state	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
X 1 0	CON	1	1	I/O select	IRQ mask	SLCTIN*	INIT	AUTO-FDXT	STROBE*
X 1 1	AFR	FIFO enable	INTP* polarity	IRQ type bit-1	IRQ type bit-0	INTP* source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
X 1 1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to DDIS* delay			25	ns	100 pF load
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rck}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	

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AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1 * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 15mA PD7-PD0 I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -150 µA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg. power supply current		12	20	mA	
I_{IL}	Input leakage			±10	µA	Exc. pins 63, 65, 66, 67, 68
R_{IN}	Input pullup resistance			11	KΩ	Pins 63, 65, 66, 67, 68
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	4		15	kΩ	*Marked pins

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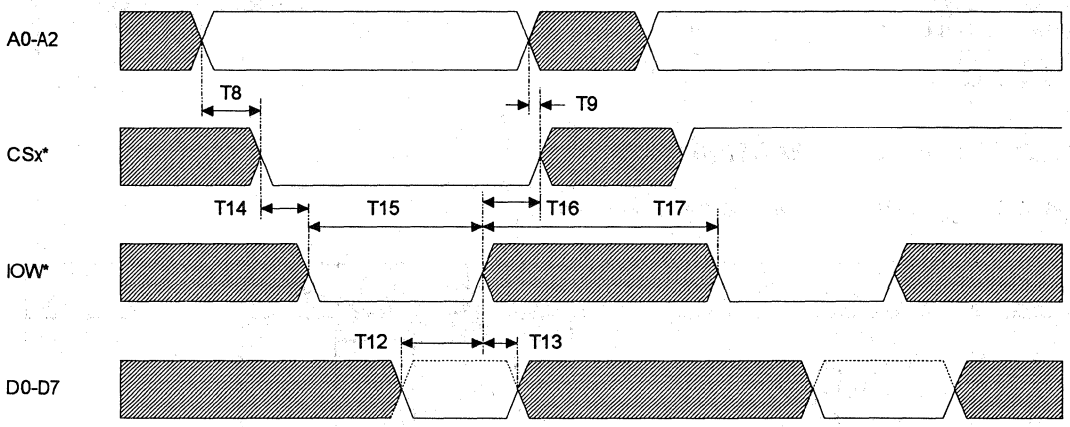
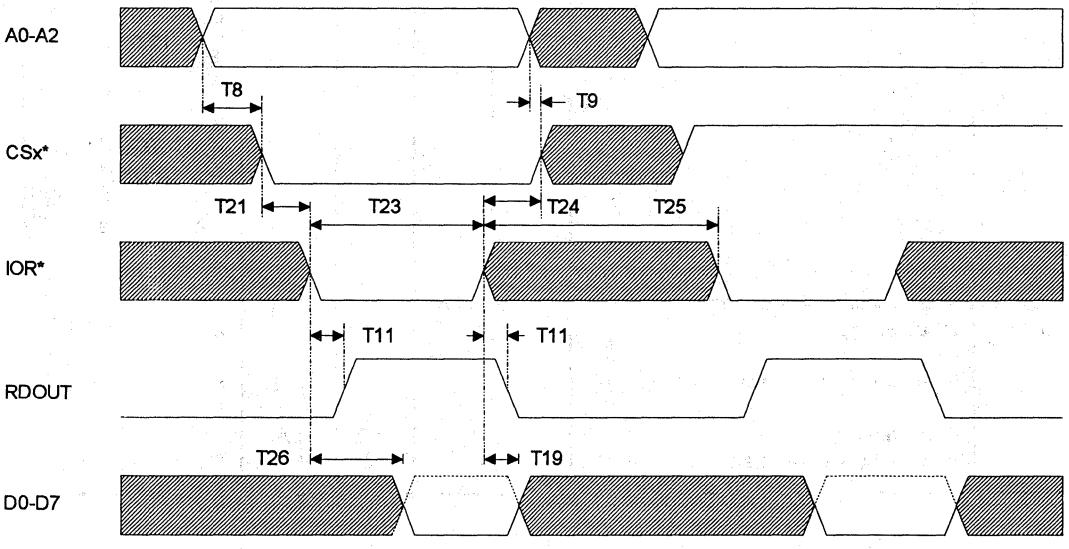
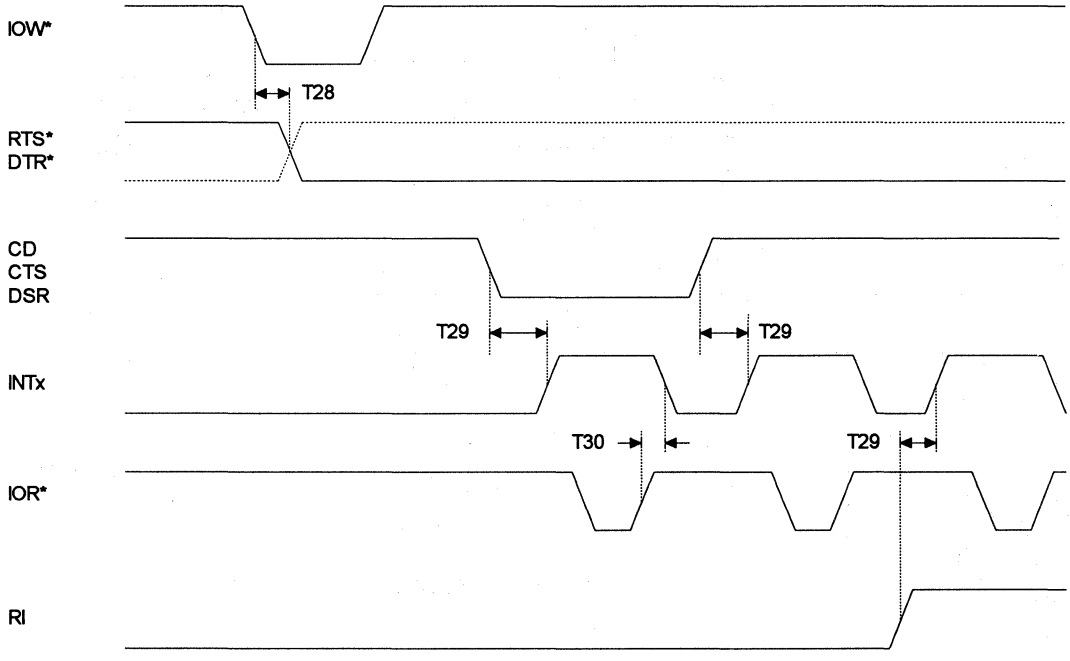
GENERAL WRITE TIMING



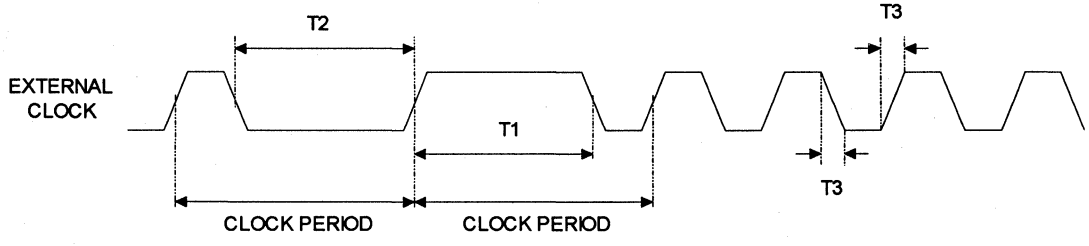
GENERAL READ TIMING



MODEM TIMING



CLOCK TIMING



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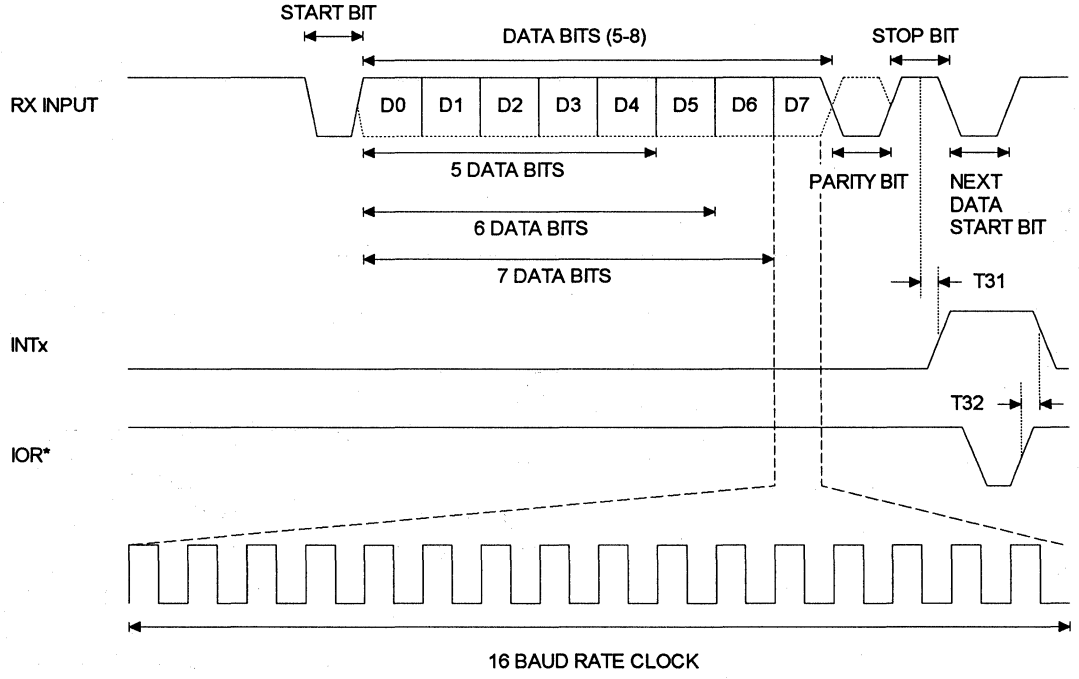
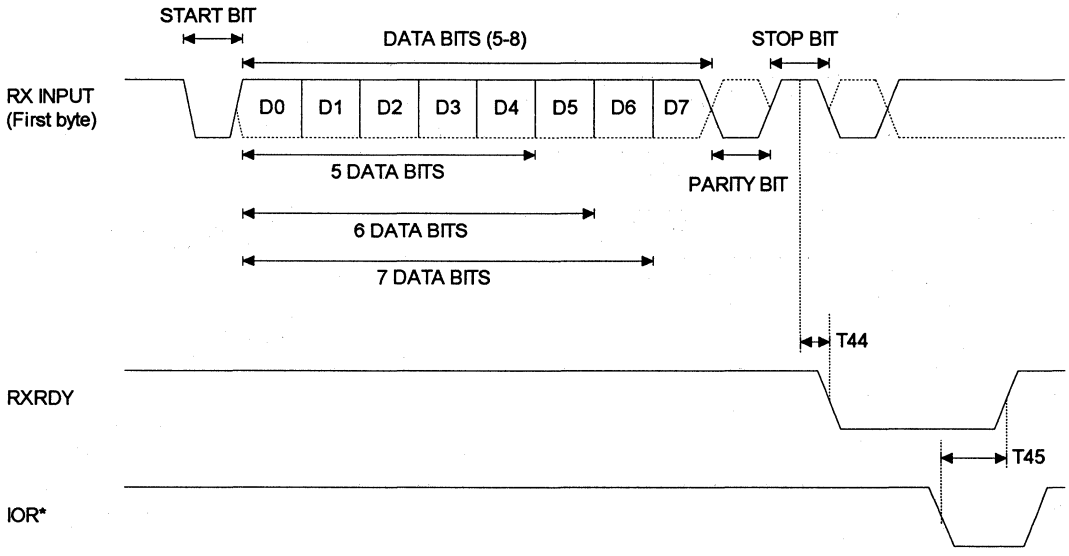
RECEIVE TIMING



RXRDY TIMING FOR MODE "0"



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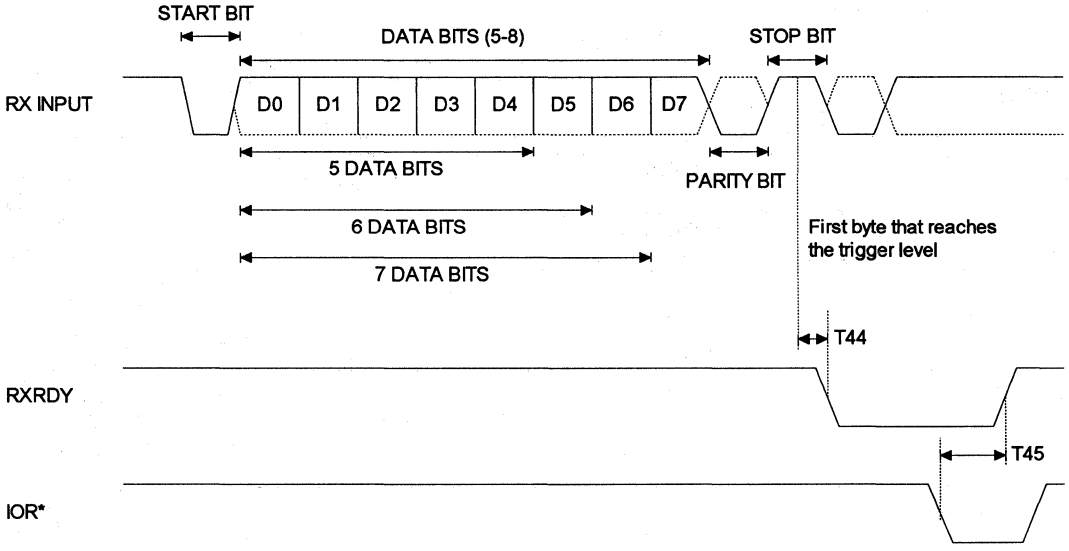
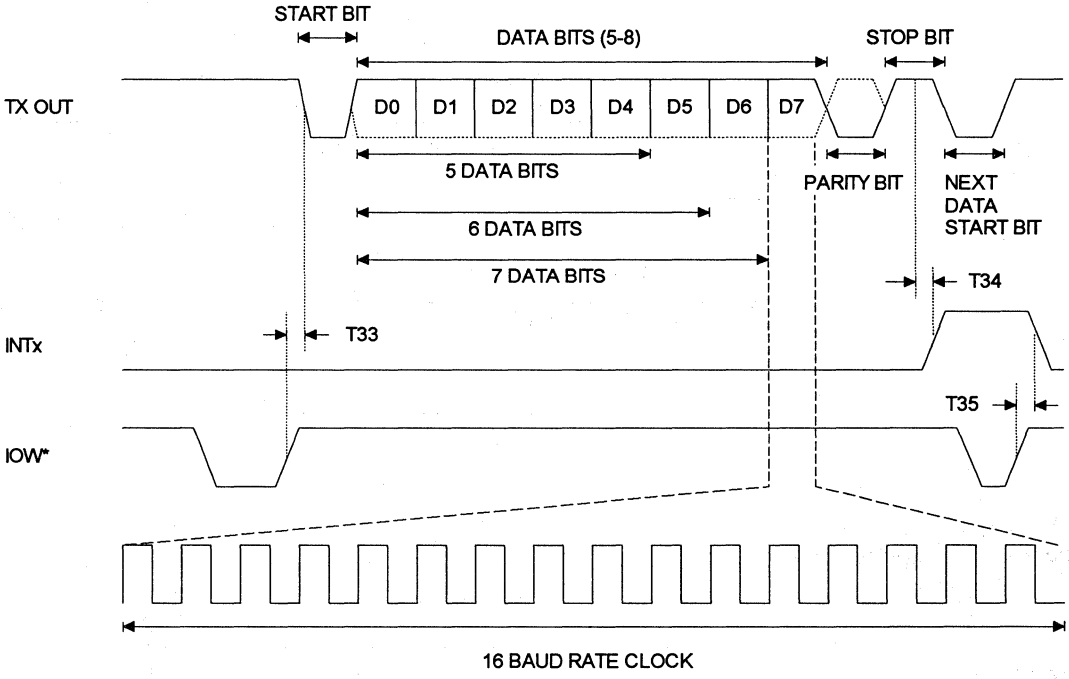
RXRDY TIMING FOR MODE "1"



TRANSMIT TIMING



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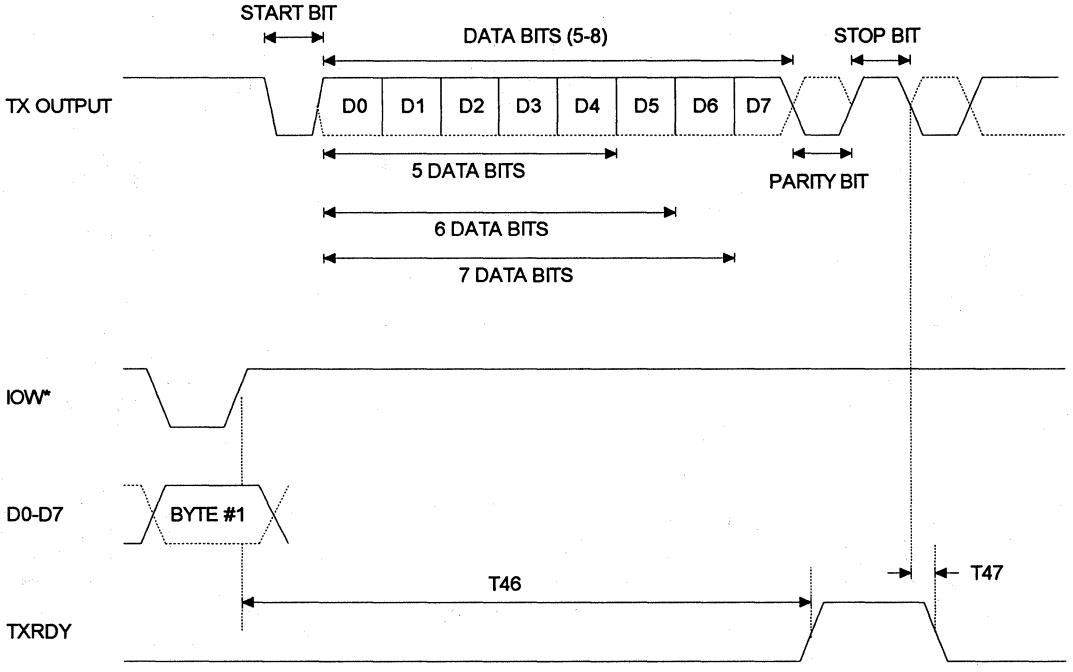
TXRDY TIMING FOR MODE "0"



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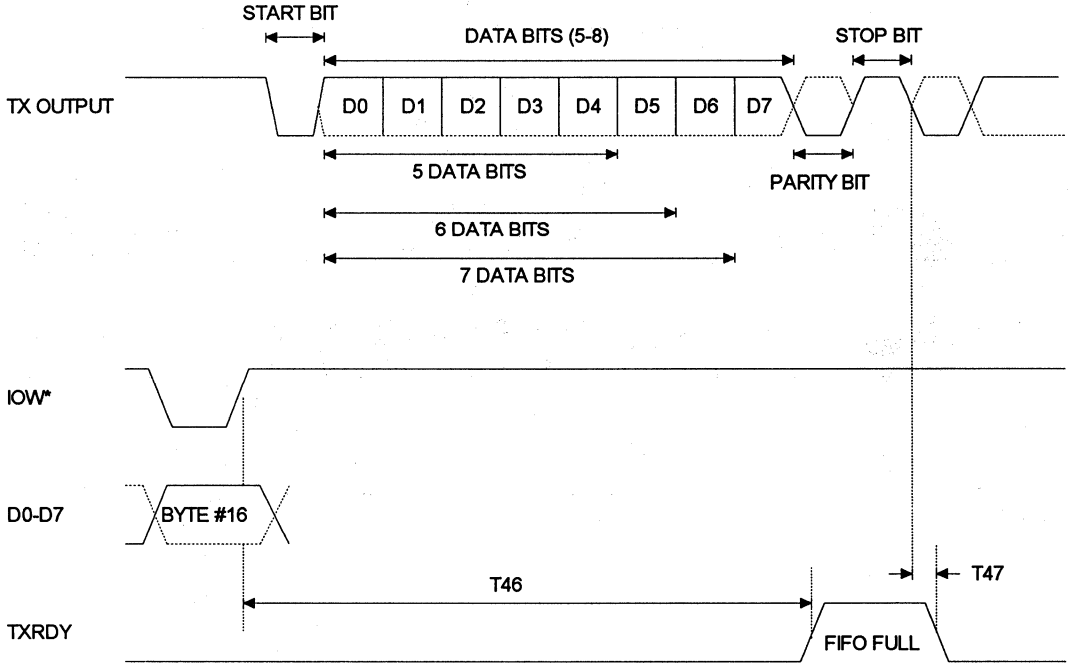
TXRDY TIMING FOR MODE "1"



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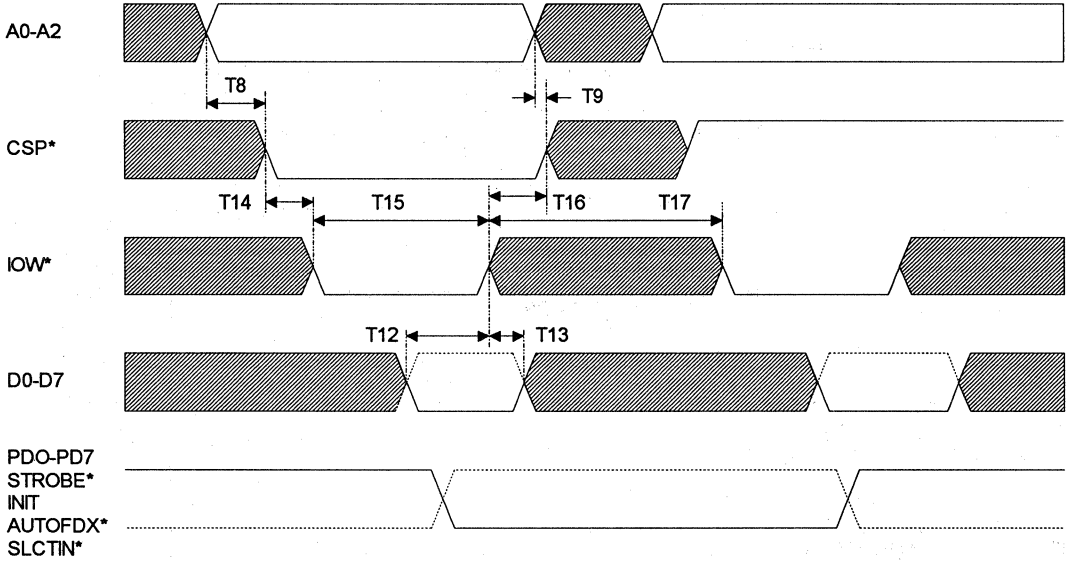
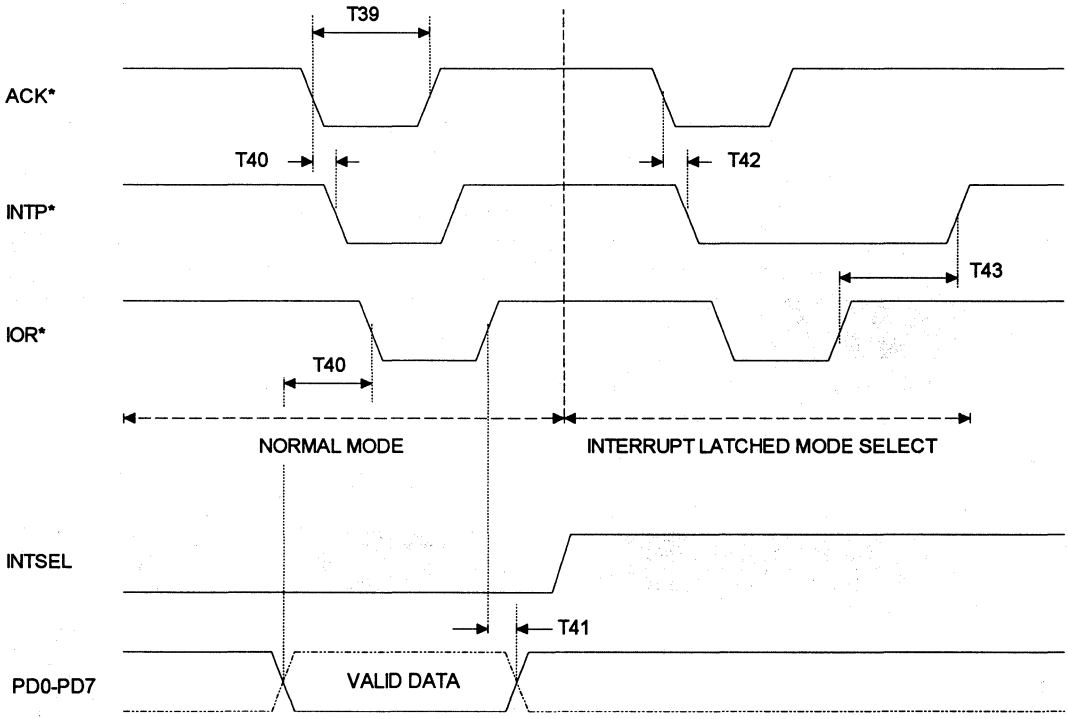
PARALLEL PORT GENERAL WRITE TIMING



PARALLEL PORT READ TIMING



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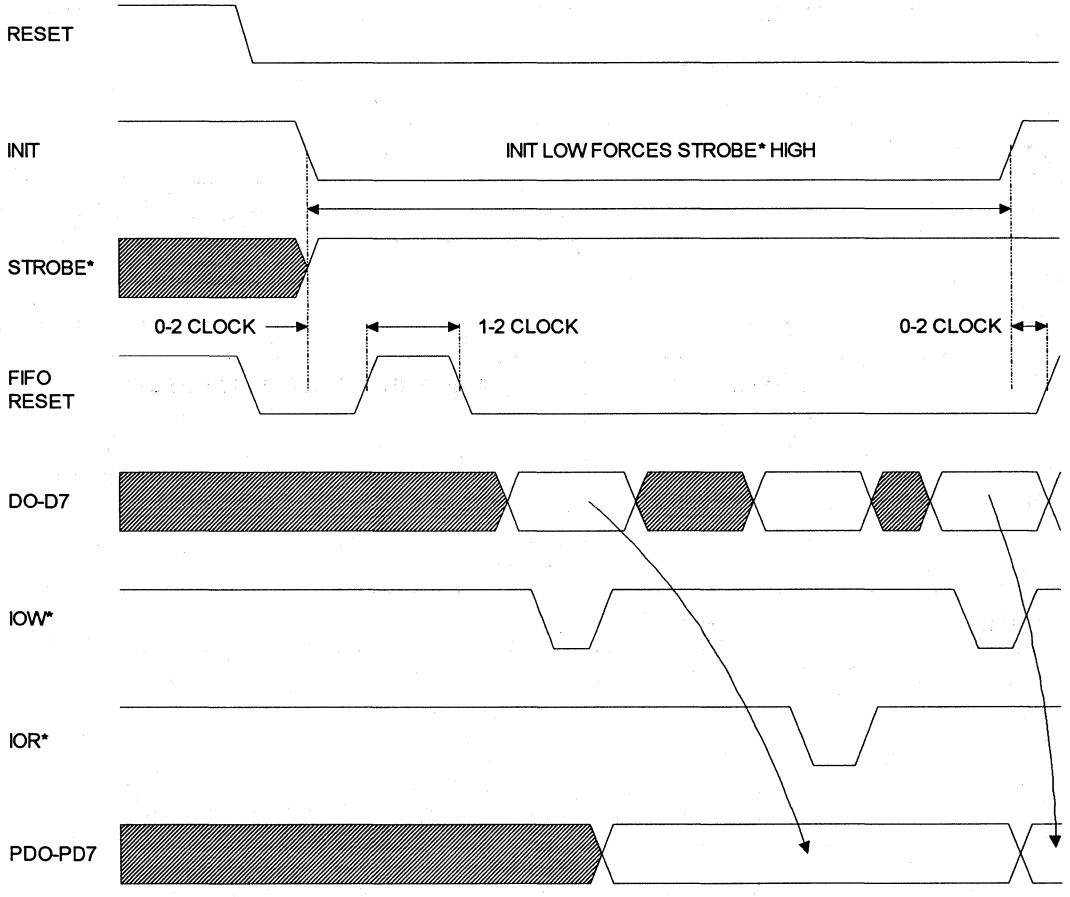
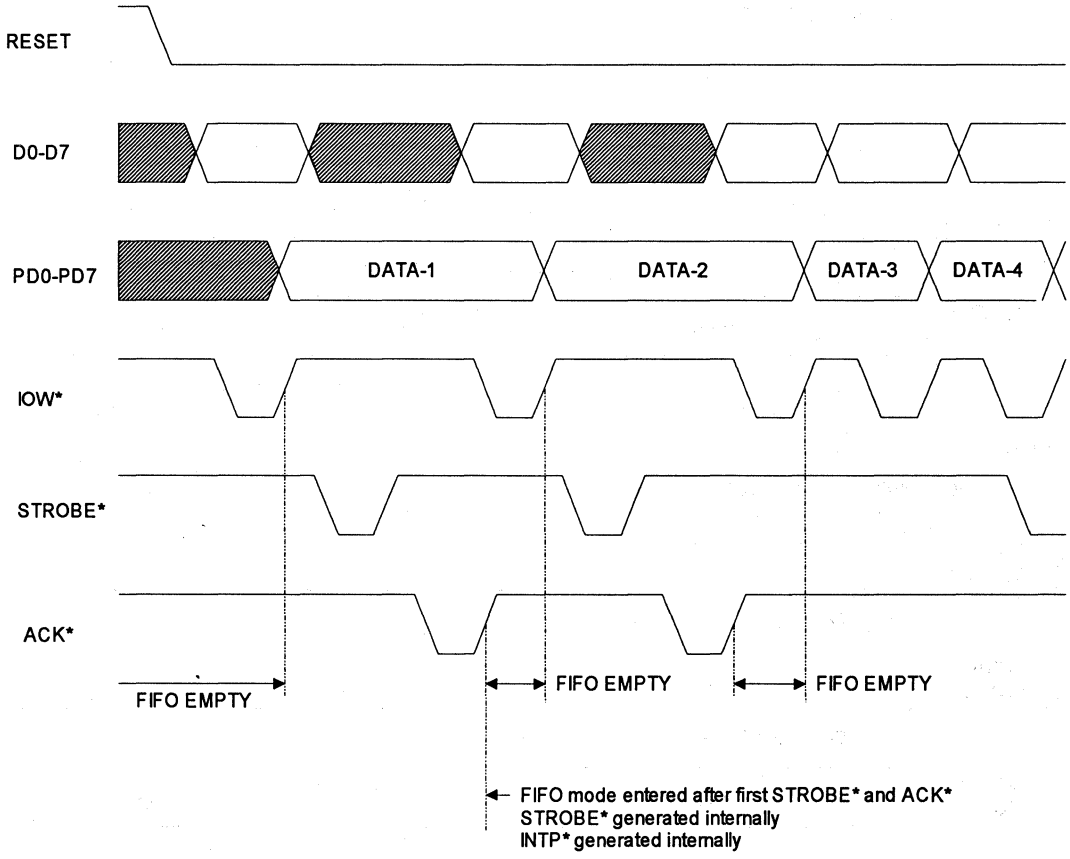
ST16C553 PRINTER SPECIAL MODE



ST16C553 PRINTER AUTO FIFO OPERATION



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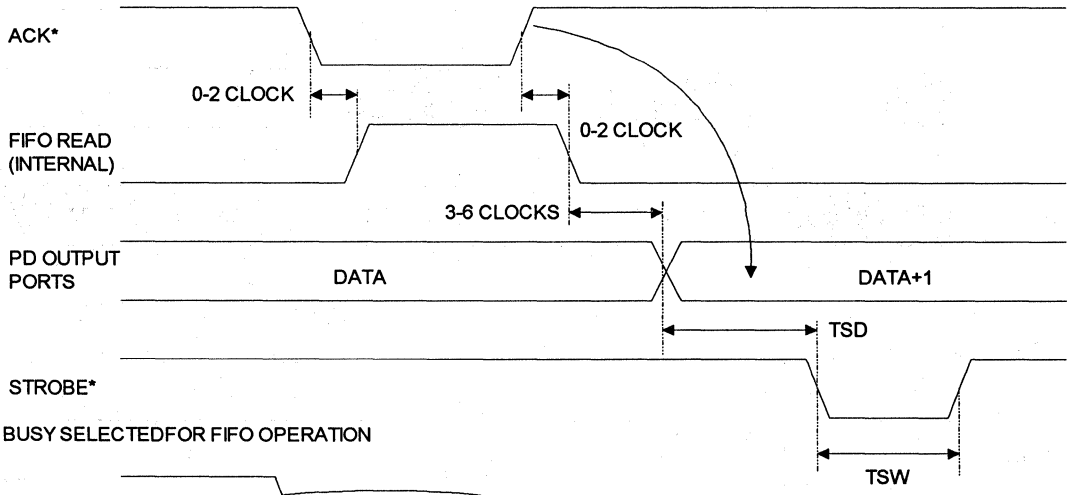
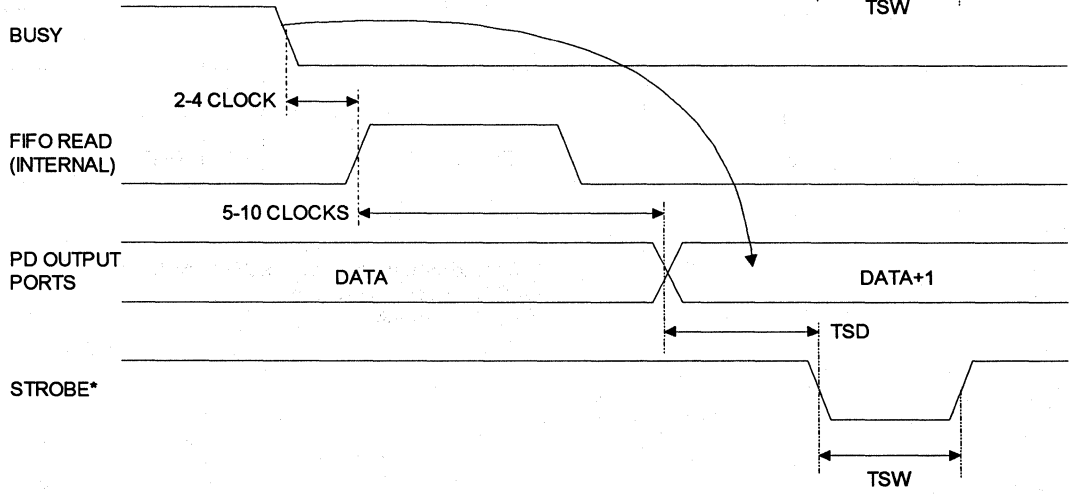
ST16C553 PRINTER FIFO TIMING WITH MORE THAN ONE BYTE IN THE FIFO

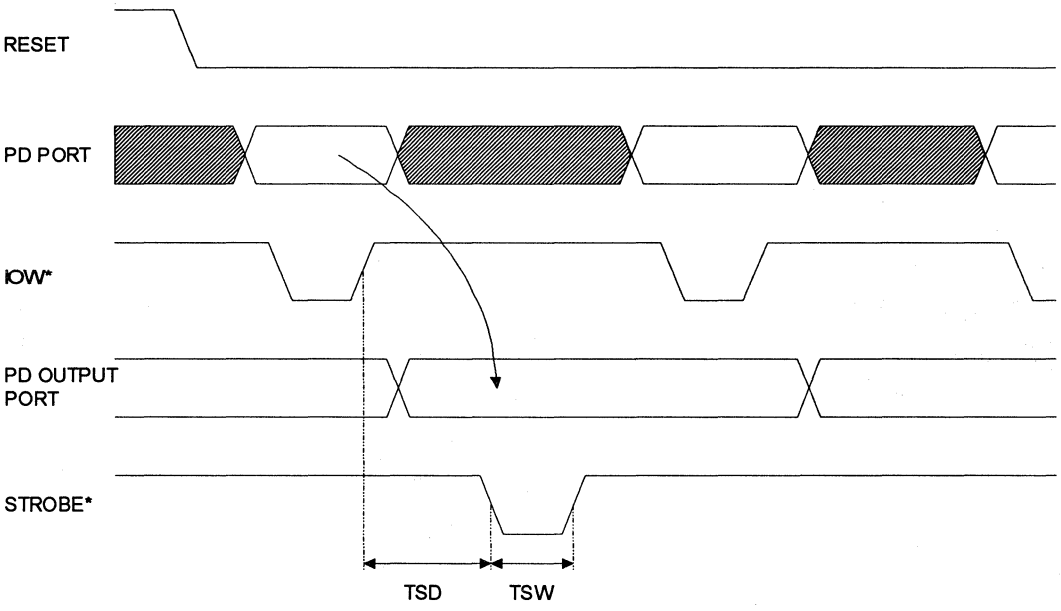
ACK SELECTEDFOR FIFO OPERATION



BUSY SELECTEDFOR FIFO OPERATION



ST16C553 PRINTER FIFO, WITH ONE BYTE IN THE FIFO



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PERIPHERALS 4

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STARTECH

ST78C34

Printed February 23, 1994

GENERAL PURPOSE PARALLEL PRINTER PORT WITH 83 BYTE FIFO

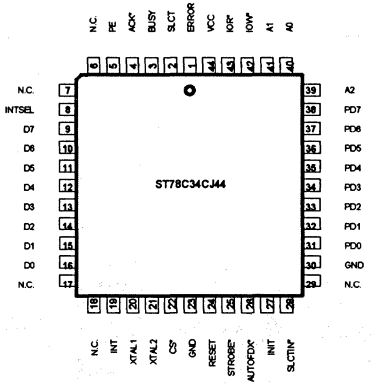
DESCRIPTION

The ST78C34 is a monolithic Bidirectional Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port.

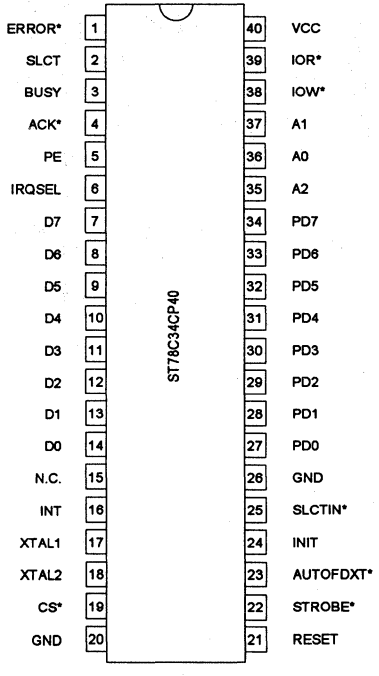
The ST78C34 is a general purpose input/output controller with 83 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.

The ST78C34 is designed to operate as normal printer interface without any additional settings. Contents of the FIFO will be cleared after reset or setting the INIT pin to a low state. The auto FIFO operation starts after the first ACK* is received from the printer. Contents of the FIFO transfer to the printer at the printer loading speed.

PLCC Package



Plastic-DIP Package



FEATURES

- 83 bytes of printer output FIFO
- Bi-directional software parallel port
- Bi-directional I/O ports
- Pin-to-pin compatible to ST78C35
- Register compatible to IBM XT, AT, compatible 386, 486
- Selectable interrupt polarity
- Selectable FIFO interrupts

ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C34CJ44	PLCC	0° C to + 70° C
ST78C34IJ44	PLCC	-40° C to + 85° C
ST78C34CP40	Plastic-Dip	0° C to + 70° C
ST78C34IP40	Plastic-Dip	-40° C to + 85° C

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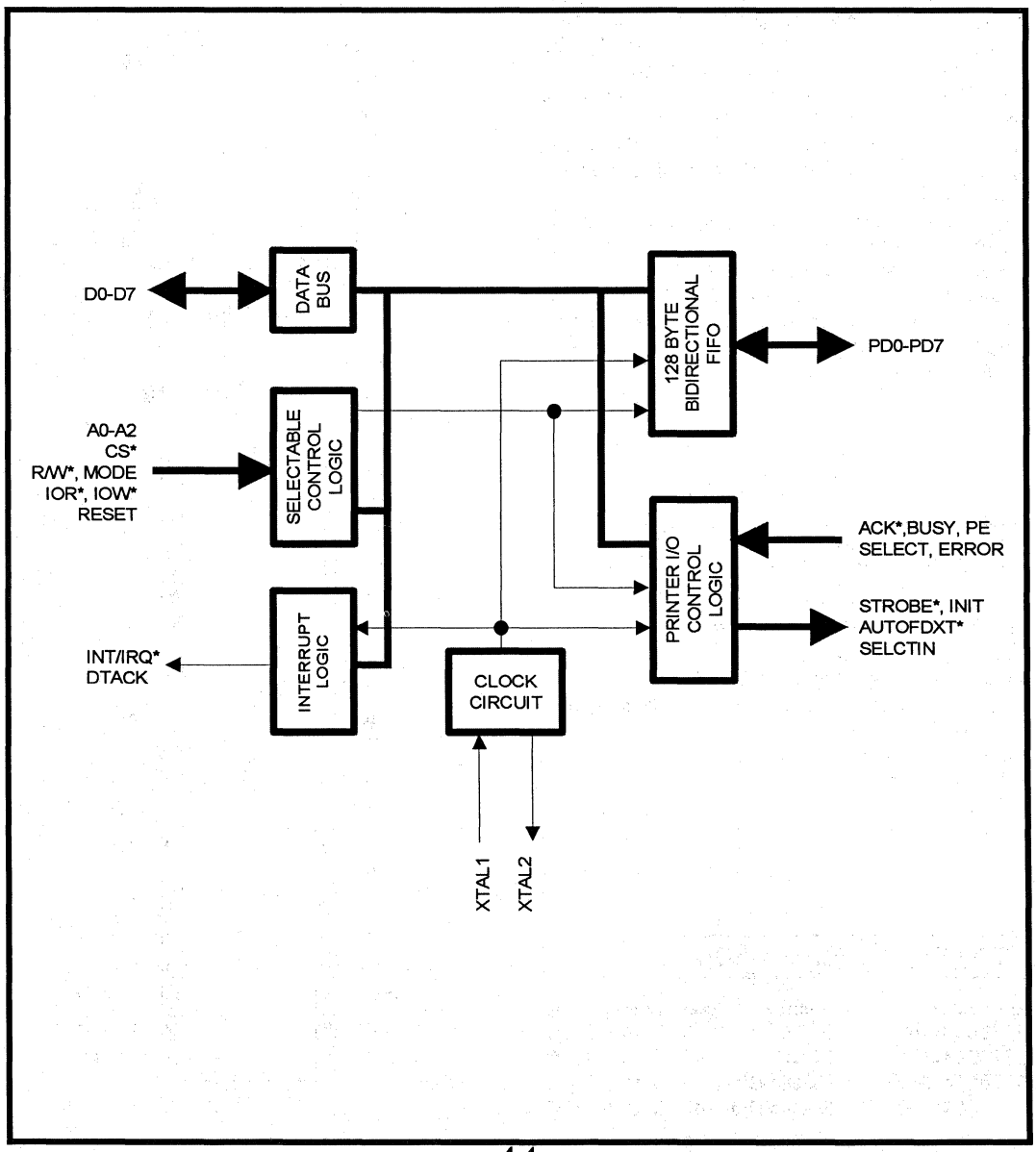
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
ERROR*	1	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	2	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	3	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
ACK*	4	I	General purpose input or line printer acknowledge (active low). An output from the printer to indicate that data has been accepted successfully.
PE	5	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
INTSEL	6	I	Interrupt select mode (pulled-up). The external ACK* can be selected as an interrupt source by connecting this pin to the VCC or left open. Connecting this pin to GND will set the interrupt to latched mode, reading the status register resets the INT output.
D0-D7	14-7	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus.
N.C.	15		No connect. Should be left open for future expansion.
INT	16	O	Interrupt output (selectable active low or high). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INT is low and when ACK* is high INT is high if selected as active low interrupt.
XTAL1	17	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock oscillator circuit.

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Symbol	Pin	Signal Type	Pin Description
XTAL2	18	O	Crystal input 2 or buffered clock output. See XTAL1.
CS*	19	I	Chip select (active low). A low at this pin enables the ST78C34 / CPU data transfer operation.
GND	20	O	Signal and power ground.
RESET	21	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers.
STROBE*	22	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	23	I/O	General purpose I/O or line printer auto feed (open drain active low). To signal the printer for continuous form feed.
INIT	24	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	25	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
GND	26	O	Power and signal ground.
PD7-PD0	34-27	I/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C34 parallel port. PD7-PD0 are latched during output mode.
A2	35		Address line A2. To select internal registers.
A0-A1	36-37	I	Address lines. To select internal registers.
IOW*	38	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	39	I	Read strobe (active low). A low level on this pin transfers the contents of the ST78C34 data bus to the CPU.
VCC	40	I	Power supply input.

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1		STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYTE COUNT REGISTER

* Reading the status register will reset the INT output.

PRINTER FUNCTIONAL DESCRIPTION

The ST78C34 parallel port is designed to operate as a normal CENTRONICS printer interface. The port contains 83 byte FIFO that may be enabled via bit-7 of the Alternate Function Register (AFR). After reset, the FIFO is disabled and the part will function identical to the ST16C552. Once the FIFO is enabled via AFR bit-7, the port will enter FIFO mode after the first byte of data is strobed to the printer and the printer responds with either an ACK* or BUSY signal.

The ST78C34 will remain in FIFO mode until the part is reset or INIT is brought low. While in FIFO mode, data transfer to the printer will be controlled by the printer without any user intervention. The printer port also contains a FIFO byte counter that maintains a count of the number of bytes remaining in the FIFO. The FIFO and the FIFO byte counter are cleared by a reset or by a change of state of the INIT pin. All FIFO related timing is derived from the clock input to pin 17 of the part.

A special parallel port write / read mode is activated when INIT is held low, either by writing a "0" to Control Register bit-2 or by forcing the INIT pin low. In this mode the FIFO read pointer is advanced by reading the parallel port instead of the ACK* or BUSY signals. The STROBE* output is forced high. This allows the user to perform parallel port write and read from operations without strobing data to the printer.

Following an INIT, the parallel port will not be in the FIFO mode. Control Register bit-0 is used as the STROBE*, Status Register bit-7 is the inverse of the BUSY signal, and INT is derived from ACK*. The transition into FIFO mode will occur after the first STROBE* is generated and the printer responds with either an ACK* or BUSY. In FIFO mode, STROBE* is generated automatically and writing to Control Register bit-0 has no effect on STROBE*. Alternate Function Register bit 0-2 are used to control the delay and width of STROBE*. Handshaking between the printer and the ST78C34 may be controlled by bit-3 of the Alternate Function Register. Setting this bit to a "1" will result in the use of BUSY instead of ACK* for FIFO reading and interrupt control. INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read of FIFO Byte Count Register (FBCR) should only be performed a minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data

ST78C34

will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL pin. If this pin is tied low, a latched interrupt will result. In this mode, INT will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL pin is tied high, INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INT pin may be inverted by setting Alternate Function Register bit-6 high.

The ST78C34 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INT output can be selected as FIFO full or FIFO empty interrupt.

REGISTER DESCRIPTIONS

PORT REGISTER
Bi-directional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bi-directional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
This bits are set to "1" normally except when AFR bit 5-4 are both set to "1".

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR input state.
0= ERROR input is in low state
1= ERROR input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY or FIFO full signal.

0= BUSY input is in high state
1= BUSY input is in low state

FIFO is enabled.
0= FIFO is full
1= One or more empty locations in FIFO

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

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COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INT output) is disabled
1= Interrupt (INT output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INT output is disabled (three state mode)
1= INT output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INT and change interrupt functions.

AFR BIT 0-2:
Timing select.
The STROBE* delay and width can be controlled by these bits.

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
1	0	0	3	2
1	0	1	5	4
1	1	0	5	4
1	1	1	9	8
0	0	0	6	4
0	0	1	10	8
0	1	0	10	8
0	1	1	18	16

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AFR BIT-3:
Interrupt source.
0= ACK* input pin is selected as printer handshaking source
1= BUSY input pin is selected as printer handshaking source

AFR BIT 4-5:
Interrupt type. State of the INT output pin can be selected for one of the following options.

Bit-5	Bit-4	INT output	SR bit-0	SR bit-6
0	0	Normal mode	1	ACK*
0	1	FIFO empty	1	FIFO empty
1	0	FIFO full	1	FIFO full
1	1	FIFO empty	0	FIFO empty

AFR BIT-6:
INT output polarity.
0= Normal. INT output follows the ACK* input
1= Inverted INT output

AFR BIT-7:
FIFO enable / disable function.
0= FIFO is disabled(default mode).
1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR)

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:
FIFO byte count. Number of characters left in FIFO. FCRB bit-0 is the LSB bit of the counter and FCRB bit-6 is the MSB bit of the counter.

FBCR BIT-7:
FIFO state.
0= FIFO is enabled
1= FIFO is disabled

ST78C34 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	Unknown, output mode
STROBE*	High
AUTOFDXT*	High
INIT	Low
SLCTIN*	High

ST78C34 REGISTER CONFIGURATIONS

A1	A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0	0	PR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0	1	STR	BUSY*/ FIFO full*	None Latched INT	PE	SLCT	ERROR	Latched INT	1	1
1	0	COM	1	1	1	INT enable	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
1	0	CON	X	X	I/O select	INT mask	SLCTIN*	INIT	AUTO-FDXT	STROBE*
1	1	AFR	FIFO enable	INT polarity	INT type bit-1	INT type bit-0	INT source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
1	1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

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AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 15mA PD7-PD0 I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -150 µA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg. power supply current		12	20	mA	
I_{IL}	Input leakage			±10	µA	Except Pins 1-6
I_{IL}	Input leakage			-450	µA	Pins 1-6 @ Vin=0V
R_{IN}	Input pullup resistance	12		40	KΩ	Pins 1-6
I_{CL}	Clock leakage			±10	µA	

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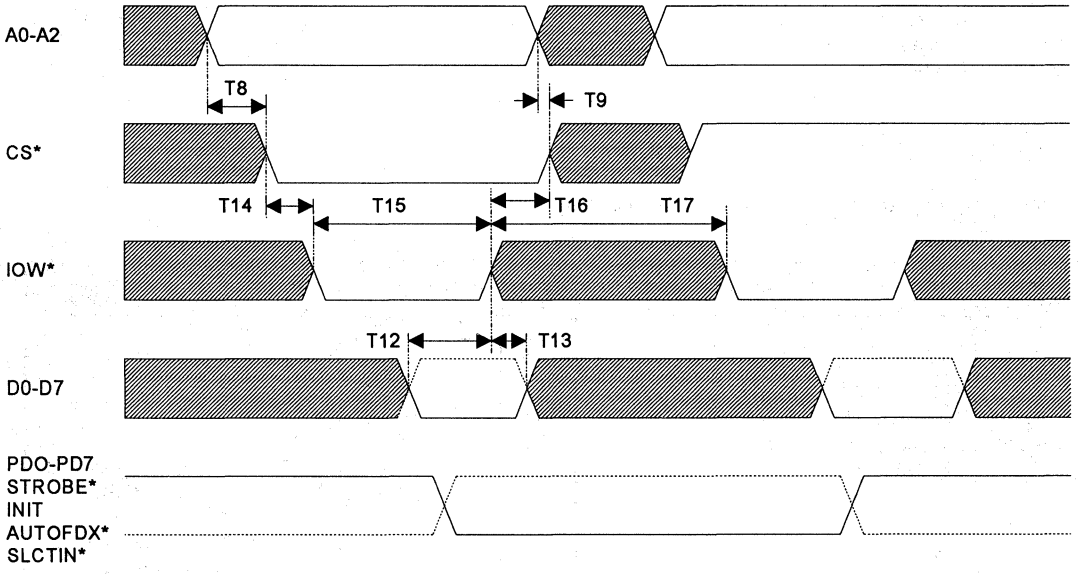
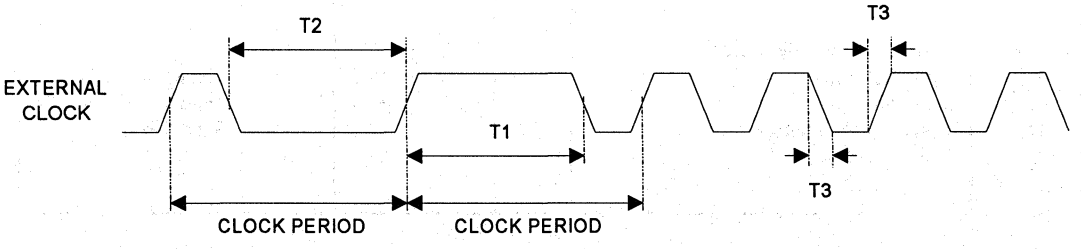
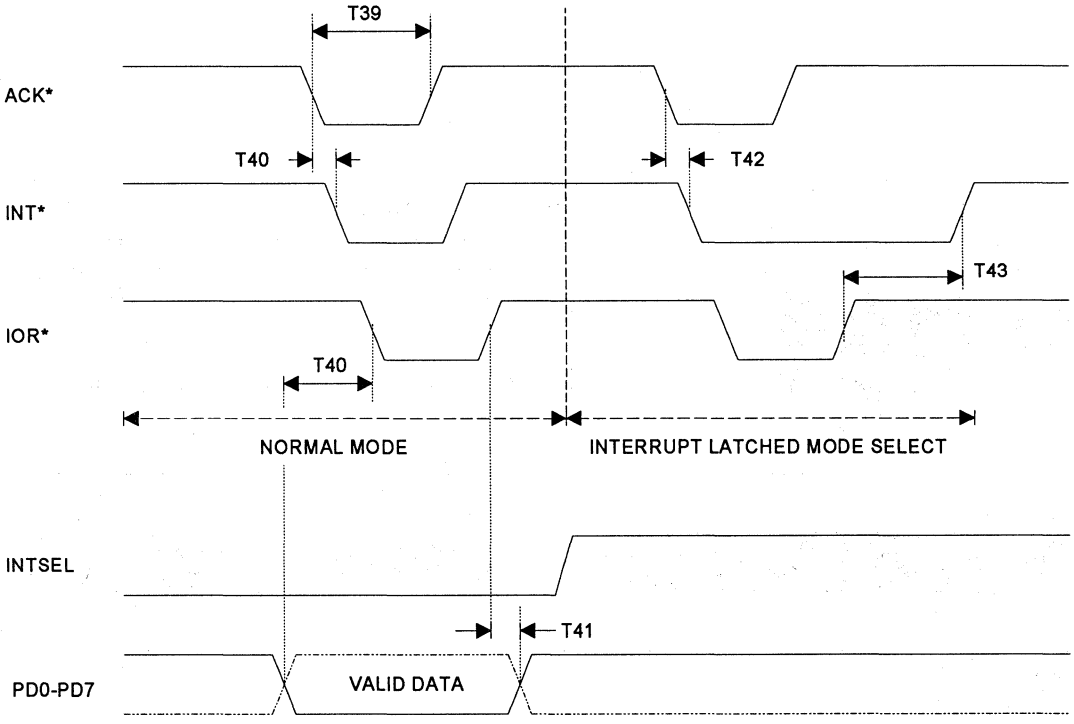
GENERAL WRITE TIMING



CLOCK TIMING



GENERAL READ TIMING



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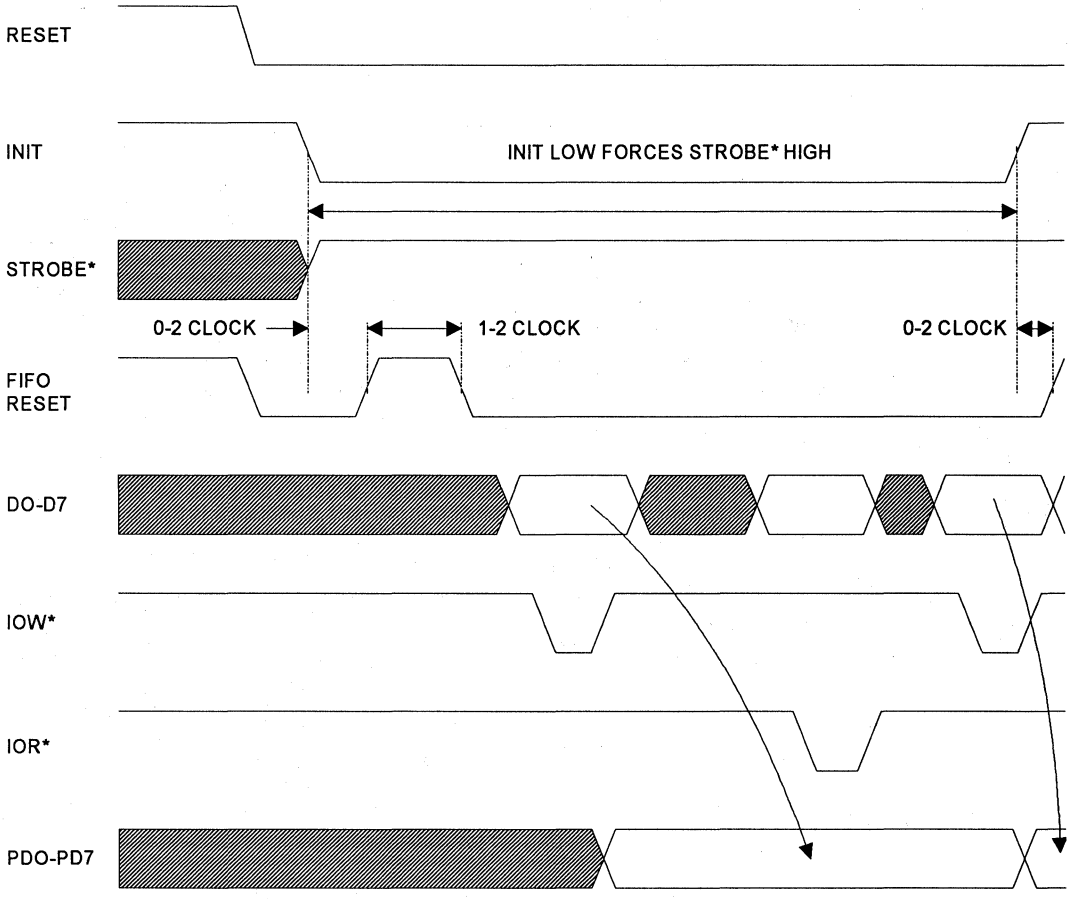
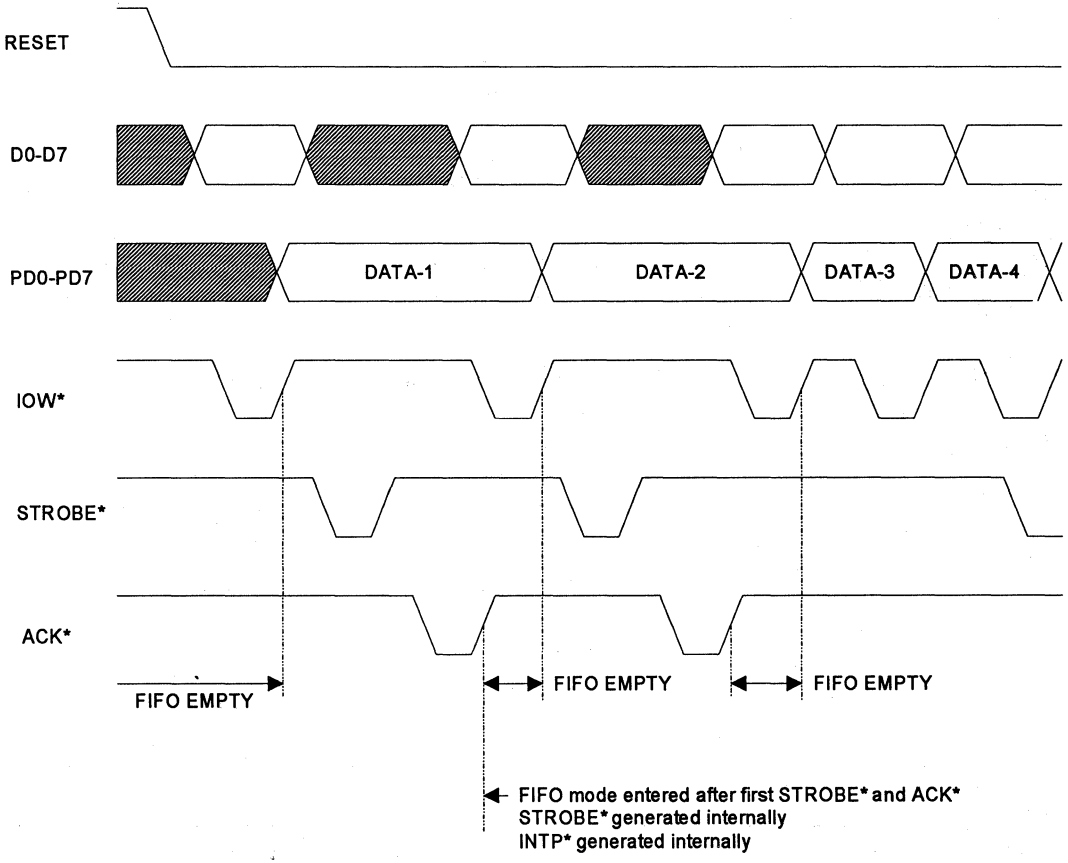
ST78C34 SPECIAL MODE



ST78C34

ST78C34 AUTO FIFO OPERATION



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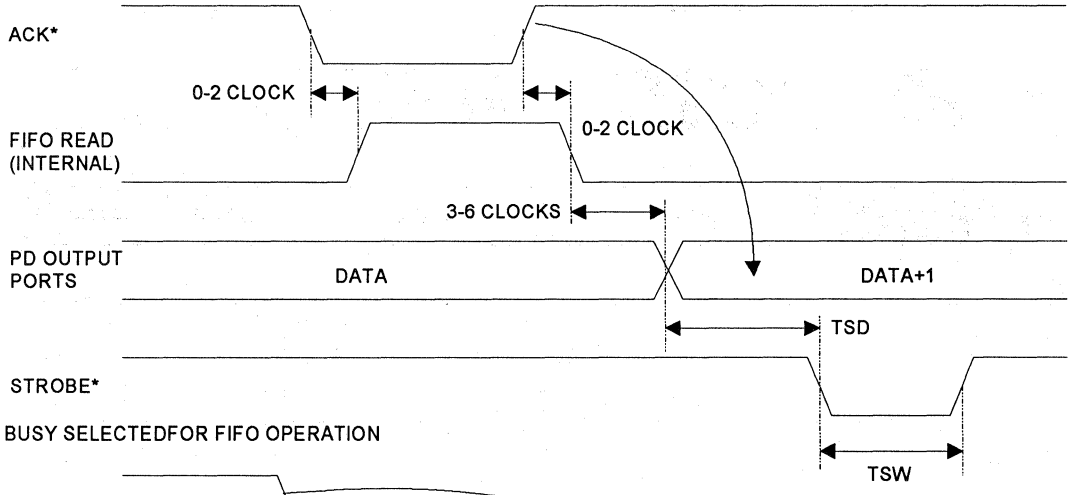
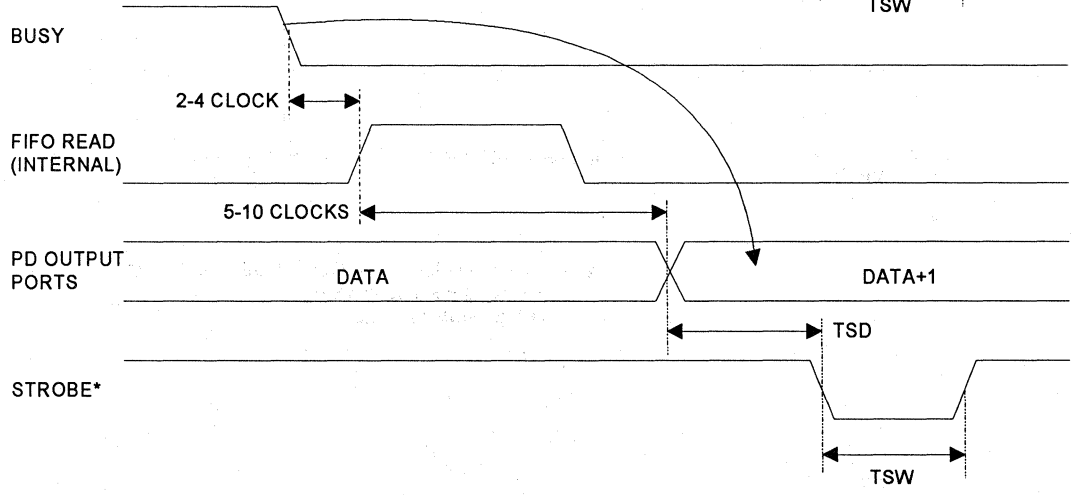
ST78C34 FIFO TIMING WITH MORE THAN ONE BYTE IN THE FIFO

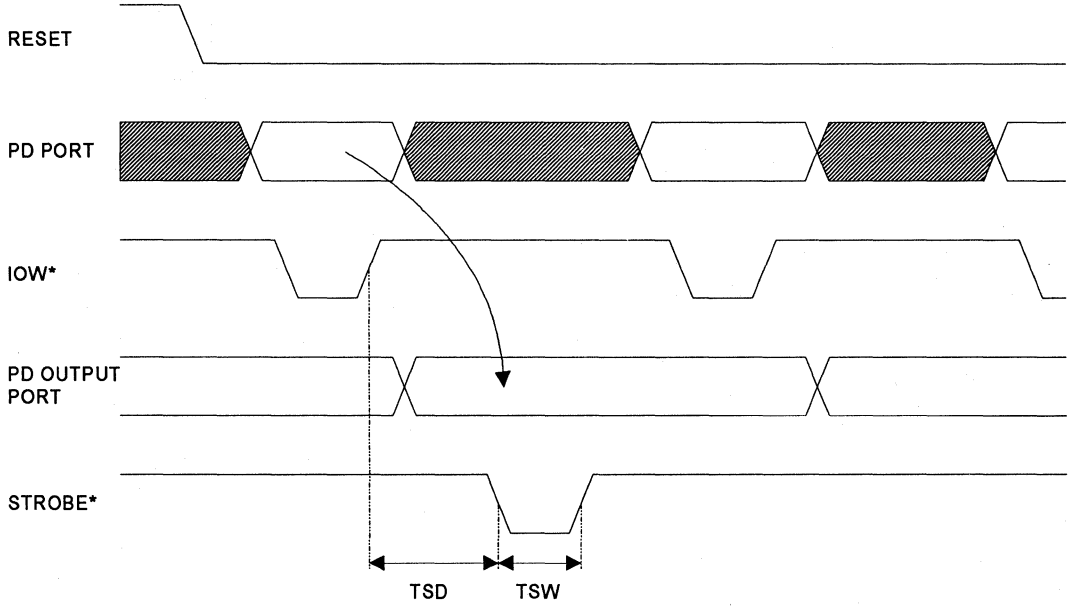
ACK SELECTEDFOR FIFO OPERATION



BUSY SELECTEDFOR FIFO OPERATION



ST78C34 FIFO TIMING, WITH ONE BYTE IN THE FIFO



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STARTECH

IDE INTERFACE WITH I/O DECODE

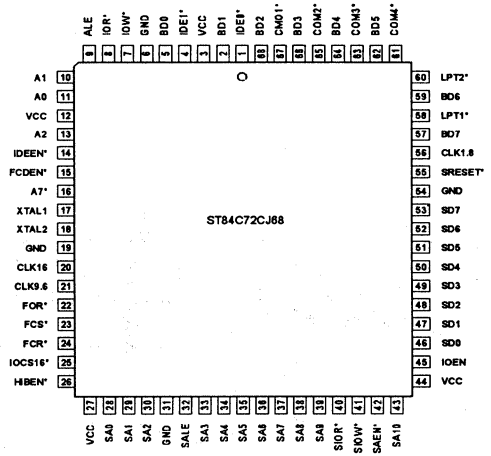
ST84C72

Printed February 23, 1994

DESCRIPTION

The ST84C72 is designed to replace all necessary TTL logics for 16 bit IDE interface and decode logic for floppy controller and serial / parallel I/O ports. A select pin is provided to select primary or secondary address for hard and floppy decodes. On board crystal oscillator circuit provides 16, 9, and 1.8461 MHz clock outputs for some floppy controllers and uart from 48 MHz external crystal connected to ST84C72.

PLCC package



FEATURES

- Low power CMOS design
- Direct bus connect
- Replacement for more than 7 TTL parts
- High speed for new design
- Selectable I/O decode ports. (COM1-COM4, LPT1-LPT2)
- Floppy address decode
- Pin selectable primary and secondary address decodes

ORDERING INFORMATION

Part number	Package	Operating temperature
ST84C72CJ68	PLCC	0 ° C to +70 ° C

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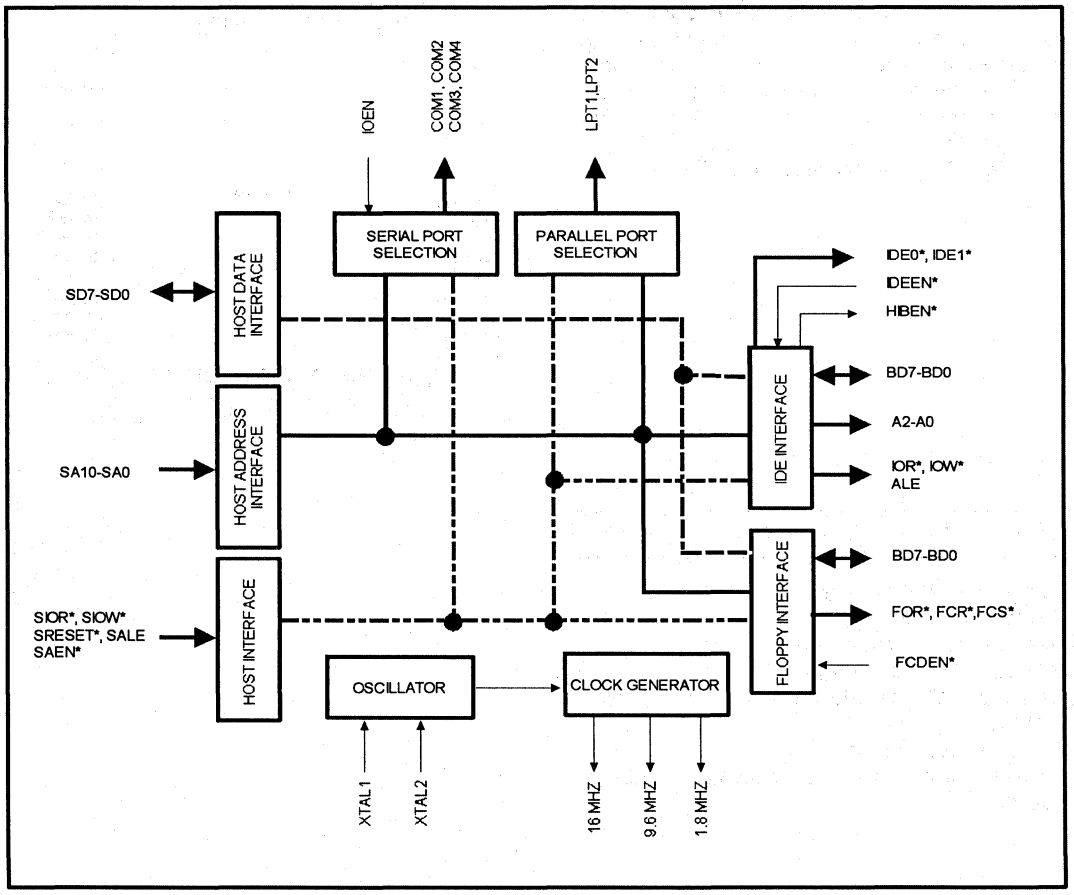
ST84C72

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
SA0-SA2	28-30	I	Host address lines A0-A2.
SA3-SA9	33-40	I	Host address lines A3-A9.
SA10	43	I	Host address line A10.
SALE	32	I	Host address latch enable (active high).
SAEN*	42	I	Host address enable (active low). All decoded addresses are valid when SAEN* is low.
SIOW*	41	I	Host I/O write signal input (active low). Buffered data bus (BD7-BD0) are gated with SIOW*, SIOR* and I/O decoded addresses to insure proper valid data time slots.
SIOR*	40	I	Host I/O read signal input (active low).Buffered data bus (B07-BD7) are gated with SIOR*, SIOW* and I/O decoded addresses to insure proper valid data time slots.
SD0-SD7	46-53	I/O	Host data bus.
SRESET*	55	I	Host system reset (internally pulled up, active low). This pin is used to set internal clock dividers to known state. For normal operation this pin should be left open or connected to VCC.
XTAL1	17	I	Crystal or external clock input. A crystal can be connected between XTAL1 and XTAL2 with some additional filters to generate 48 Mhz clock frequency for floppy controller and UART clock . This pin can be connected to VCC or GND if CLK16, CLK9.6 and CLK1.8 are not used.
XTAL2	18	O	Crystal output. This pin should be left open if external clock is used to connect to XTAL1 or clock is not used.
LPT1*	58	O	Line printer enable (active low). Primary printer enable signal. Decoded for address 378 Hex (LPT1).
LPT2*	60	O	Line printer enable (active low). Secondary printer enable signal. Decoded for address 278 Hex (LPT2).

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
COM1*	67	O	Serial communication select pin (active low). Decoded for 3F8 Hex (COM-1).
COM2*	65	O	Serial communication select pin (active low). Decoded for 2F8 Hex (COM-2).
COM3*	63	O	Serial communication select pin (active low). Decoded for 3E8 Hex (COM-3).
COM4*	61	O	Serial communication select pin (active low). Decoded for 2E8 Hex (COM-4).
CLK1.8	56	O	1.8461 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 26). This clock can substitute the standard 1.8432 Mhz serial communication clock.
IOEN	45	I	Serial and parallel port access. Connecting this pin to pin 44 (RDOUT) of the ST16C452, ST16C552, or ST16C553 enables the BD0-BD7 to access the serial and parallel ports. This pin should be tied to GND if external serial/ parallel ports are not used.
FDCEN*	15	I	Floppy controller enable/disable (internally pulled up). Floppy controller select is disabled when this pin is left open or connected to VCC. Floppy controller can be selected when this pin is connected to host SA7 pin (primary selection address 3F7, 3F5, 3F4 and 3F2 Hex) or A7* output pin of the ST84C72 (secondary selection address 377, 375, 374 and 372 Hex).
FOR*	22	O	Floppy controller address decode (372/3F2 Hex).
FCS*	23	O	Floppy controller address decode (377/3F7 Hex).
FCR*	24	O	Floppy controller address decode (374-5/3F4-5 Hex).
CLK16	20	O	16 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divided by 3).

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CLK9.6	21	O	9.6 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 5).
IOCS16*	25	I	IDE 16 bit data transfer enable (internally pulled up, active low). This pin enables the external 74LS245 bus driver (HIBEN*) when IDE port is selected and 16 bit data transfer is required.
IDEEN*	14	I	IDE Enable/Disable (internally pulled up). IDE select is disabled when this pin is left open or connected to VCC. IDE controller can be selected when this pin is connected to host SA7 pin (primary selection address 3F0-3F7 and 1F0-1F7 Hex) or A7* output pin of the ST84C72 (secondary selection address 370-377 and 170-177Hex).
IDE1*	4	O	IDE drive/register select-1 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 3F6 or 3F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE1* is enabled when I/O port address 376 or 377 Hex is accessed.
IDE0*	1	O	IDE drive/register select-0 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 1F0-1F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE0* is enabled when I/O port address 170-177 Hex is accessed.
HIBEN*	26	O	High order data bus enable. This pin enables the external 74LS245 data buffer (host SD8-SD15) when IOCS16* is active and IDE port is selected.
A0-A1	11-10	O	Buffered host addresses A0 and A1.
A2	13	O	Buffered host address A2.
A7*	16	O	Inverted host address line SA7. This pin is used to select secondary IDE and floppy controller.
BD3-BD0	5,2,68,66	I/O	Buffered LSB of low order host data bus (SD0-SD3). These bits are set to input mode when SIOW* is low.

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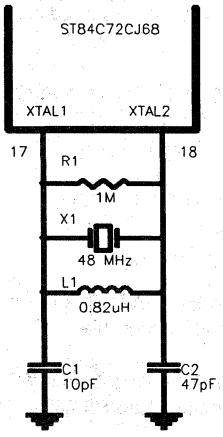
SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
BD4-BD6	64,62,59	I/O	Buffered MSB of low order host data bus (SD4-SD6). These bits are set to input mode when SIOW* is low.
BD7	57	I/O	Buffered host data bit -7 (SD7). This bit goes to high impedance when address 3F7 or 1F7 Hex is accessed during I/O read operation. BD7 is set to input mode when SIOW* is low.
ALE	9	O	Buffered host address latch (SALE).
IOR*	8	O	Buffered host I/O read signal (HIOR*).
IOW*	7	O	Buffered host I/O write signal (HIOW*).
GND	6,19,31,54	O	Signal and power ground.
VCC	3,12,27,44	I	Power supply input.

Optional external filter.



ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{cc}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			15	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST84C72

STARTECH

ST37C65

Printed February 28, 1994

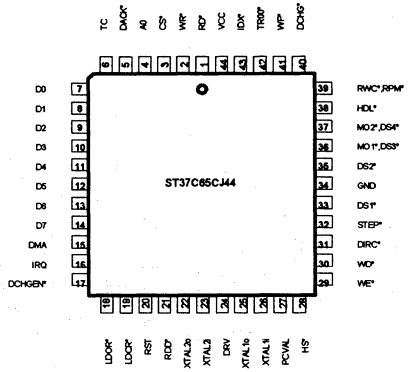
FLOPPY DISK SUBSYSTEM CONTROLLER

DESCRIPTION

The ST37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "super-chip" integrates the following functions: formatter / controller, data separation, write precompensation, data rate selection (to a maximum of 1Mbit per second), and clock generation. It also provides interface drivers and receivers for the floppy drive.

The ST37C65 is functionally compatible pin-for-pin with the WD37C65C. In addition the ST37C65 Supports a power down mode for laptop and portable systems.

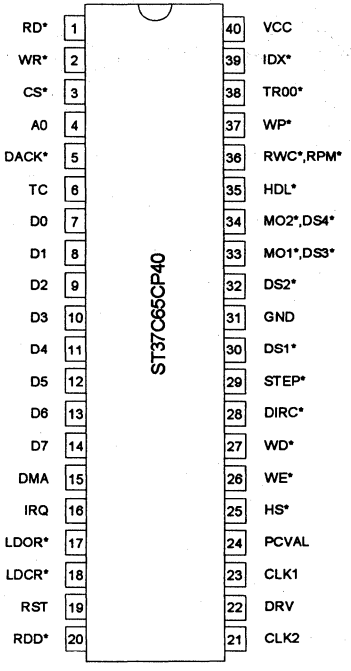
PLCC Package



FEATURES

- IBM* PC AT* compatible format (single and double density)
- BIOS compatible, supports dual speed spindle drives
- Address mark detection circuitry (internal to floppy disk controller)
- Multi-sector and multi-track transfer capability
- Direct floppy disk drive interface (no buffers needed)
- 48 mA sink output drivers
- Automatic write pre-compensation Disable option, Pin selectable inner track values of 125 or 187 nanoseconds
- Integrated high-performance DPLL data separator, industry standard error rates of <10E-9
- Data rates of 125, 250, 300, 500 Kbits/second and 1 Mbit/second
- User programmable track stepping rate and head load/unload times
- Supports four floppy drives

DIP Package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST37C65CJ44	PLCC	0° C to + 70° C
ST37C65CP40	Plastic-Dip	0° C to + 70° C

4

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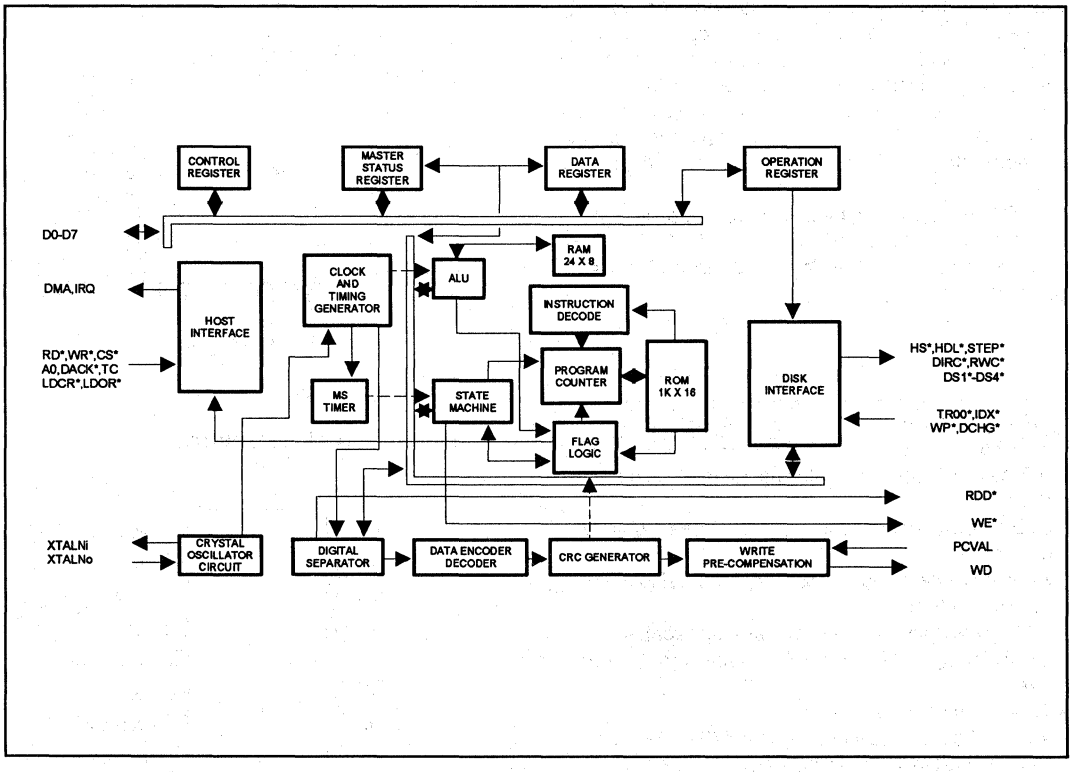
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
RD*	1	I	Read signal (active low). Control signal for transfer of data or status onto the data bus by the ST37C65.
WR*	2	I	Write signal (active low). Control signal for latching data from the bus into the ST37C65 buffer register.
CS*	3	I	Chip select (active low). Selected when low allowing RD* or WR* operation from the host.
A0	4	I	Address line 1. Address line selecting data or status information.
DACK*	5	I	DMA ACKNOWLEDGE (active low). Used by DMA controller to transfer data from the ST37C65 onto the bus. AT/EISA mode, this signal is qualified by DMAEN from the Operation Register.
TC	6	I	Terminal Count (active high). This signal indicates to ST37C65 that data transfer is complete. If DMA operation mode is selected for command execution, TC will be qualified by DACK*, but not in the programmed I/O execution. In AT/EISA or Special mode, qualification by DACK* requires the Operation Register signal DMAEN to be logically true. Note also AT/EISA mode, TC will be qualified by DACK*, whether in DMA or non-DMA host operation. Programmed I/O in AT/EISA mode will cause an abnormal termination error at the completion of a command.
DB0-DB7	7-14	I/O	Data bus. 8 bit, bi-directional, three state, data bus. DB0 id the least significant bit and DB7 is the most significant bit.
DMA	15	O	Direct Memory Access (three state, active high). DMA request for byte transfers of data. In Special or AT/EISA mode, this pin is three stated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base mode.
IRQ	16	O	Interrupt (three state, active high). Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in Base

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			mode. In Special AT/EISA mode, this pin is three stated, enabled by DMAEN signal from the Operation Register.
DCHGEN*	17	I	Disk Change Enable (active low). This input must be at logic "0" to enable DCHG* input status at pin 40 to be placed on bit-7 of the data bus during RD* of LDCR*. It has internal pull-up.
LDOR*	18	I	Load Operations Register (active low). Address decode which enables the loading of the Operation Register. Internally gated with WR* creates the strobe which latches the data bus into the Operations Register.
LDCR*	19	I	Load Control Register (active low). Address decode which enablesloading of the Control Register. Internally gated with WR* create the strobe which latches the two LSBs from the data bus into the Control Register.
RST	20	I	Reset (active high). Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
RDD*	21	I	Read Disk Data. This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of encoded data.
*CLK2	21	I	Clock-2. TTL level clock input used for non-standard data rates; is 9.6 MHz for 300 kb/s, and can only be selected from the Control Register.
XTAL2o	22	O	Crystal oscillator drive output. A crystal oscillator is connected from this pin to XTAL2i pin. This pin should be left floating if TTL inputs used at pin XTAL2i.
XTAL2i	23	I	Crystal oscillator or External clock input pin. Used for non-standard data rates.
DRV	24	I	Drive Type. This input indicates to the device that a two speed spindle motor is used if logic is "0". In that case, the second clock input will never be selected and must be grounded.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
*CLK1	23	I	Clock1. TTL level clock input is used to generate all internal timing for standard data rates. Frequency must be 16 MHz ±0.1% or 32 MHz ±0.1%, and may have 40/60 or 60/40 duty cycle.
XTAL1o	25	O	Crystal oscillator drive output. A crystal oscillator is connected from this pin to XTAL1i pin. This pin should be left floating if TTL inputs used at pin XTAL1i.
XTAL1i	26	I	Crystal oscillator or External clock input pin. Requires 16 MHz or 32 MHz crystal. This oscillator is used for all standard data rates, and may be driven with TTL level signal.
PCVAL	27	I	Pre-Compensation Value. This pin determines the amount of write pre-compensation used on the inner tracks of the diskette. Logic "1" = 125 ns, logic "0" = 187 ns. If the data defeat option is used, PCVAL is unimportant and pre-compensation is disabled.
HS*	28	O	Head Select (active low). High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic "1" = side 0.
WE*	29	O	Write Enable (active low). The output becomes true, just prior to writing on the diskette. This allows current to flow through the write head.
WD*	30	O	Write Data. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
DIRC*	31	O	Direction (active low). DIRC* determines the direction of the head stepper motor. Logic "1" = outward motion.
STEP*	32	O	Step Pulse (active low). STEP* output issues an active low pulse for each track to track movement of the hrad.
DS1*	33	O	Drive Select-1 (active low). It enables the interface to this disk drive. This signal comes from the Operation Register. In Base mode, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			syntax.
GND	34	O	Supply ground.
DS2*	35	O	Drive Select-2 (active low). It enables the interface to this disk drive. This signal comes from the Operation Register. In Base mode, or Special mode, this output is #2 of the four decoded Unit Selects, as specified in the device command syntax.
MO1*, DS3*	36	O	Motor On enable for disk drive #1 (active low). This signal comes from the Operation Register. In Base mode, or Special mode, this output is #3 of the four decoded Unit Selects, as specified in the device command syntax.
MO2*, DS4*	37	O	Motor On enable for disk drive #2 (active low). This signal comes from the Operation Register. In Base mode, or Special mode, this output is #4 of the four decoded Unit Selects, as specified in the device command syntax.
HDL*	38	O	Head Load (active low). When HDL* is low, causes the head to be loaded againt the media in the selected drive.
RWC*, RPM*	39	O	Readuced Write Current / Revolutions Per Minute (active low). When low, causes a Reduced Write Current when bit density is increased toward the inner tracks, becoming active when tracks >28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write pre-compensation is necessary. In the AT/EISA mode, this signal will be active when CR0=1.
DCHG*	40	I	Disk Change (active low). This input senses status from the drive. Active low indicates that drive door is open or that the diskette has possibly changed since the last drive selection. It has internal pull-up.
WP*	41	I	Write Protected (active low). This input senses status from disk drive, indicating active low when a diskette is Write Protected.
TR00*	42	I	Track Zero (active low). This input senses status from disk

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			drive, indicating active low when the head is positioned over the outermost track, Track 00.
IDX*	43	I	Index (active low) This input senses status from disk drive, indicating active low when the head is positioned over the begining of a track marked by an index hole.
VCC	44	I	Positive supply input.

* 40 Pin package only

FUNCTIONAL DESCRIPTION

ST37C65 includes data separation designed to address high performance error rate on floppy disk drives. It contains all the necessary Logic to achieve classical 2nd order, type 2, phase locked-loop performance. Write pre-compensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with 48 mA drivers which meet the ANSI specification.

The host interface supports an 8 or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers. Output drive capability is 20 LS-TTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC, PC AT and EISA applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the ST37C65, these functions are latched into registers addressed within the I/O mapping of the system. The ST37C65 has eight internal registers. The eight bit main status register contains status information about the ST37C65 and may be accessed any time. Another four status registers under system control also give various status and error information. The. Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the ST37C65.

CLOCK GENERATION

SCLK - Sampling Clock, WCLK- Write Clock, and MCLK - Master Clock, are included in the ST37C65. XTAL oscillator circuits provide the necessary signals for internal liming when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the ST37C65. The first at 32 MHz that handles all standard data rates (1Mb/sec, 500, 250, and 125 kb/sec or 16 MHz to handle 500, 250, and 125 Kb/sec.). The second oscillator is at 9.6 MHz to support the 300 kb/sec data rate used in PC AT designs.
Some AT compatibles use two-speed disk drives. If a two speed disk drive is used, the DRV input should be grounded along with the CLK2 input.

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ARCHITECTURE

The ST37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "super-chip" integrates formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or AT/EISA modes IRQ and DMA request are three-stated and qualified by DMA enable which is provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LS-TTL loading. Inputs are Schmitt Trigger receivers and can be hooked up to a bus or back plane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU waits for 12μs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of The command word may be written into the ST37C65. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the ST37C65. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register.

Note that this reading of the Main Status Register before each byte transfer to the ST37C65 is required only in the Command and Result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12μs.

During the Execution phase, the Main Status Register need not be read. If the ST37C65 is in the non-DMA Mode, then the receipt of each data byte (ST37C65 is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal (RD*=0) clears the interrupt and sends the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the WR* signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the ST37C65 is in the DMA mode, no interrupt signals are generated during the Execution phase. The ST37C65 generates DMA's (DMA Requests) when each byte of data is available The DMA Controller responds to this request with both DACK*= 0 (DMA Acknowledge) and an RD*=0 (Read signal). When the DMA Acknowledge signal goes low (DACK*= 0), the DMA Request is cleared DMA= 0) If a Write Command has been issued, then a WR* signal will appear instead of RD*. After the Execution phase has been completed (Terminal Count has occurred) The EOT sector read/written, then an Interrupt will occur (IRQ=1) this signifies the begining of the result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (IRQ=0). Note that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the ST37C65 will successfully complete commands, but will at ways give abnormal termination error status since TC is qualified by an inactive DACK*. The RD* or WD* signals should be asserted while DACK* is true The CS* signal is used in conjunction with RD* and WR* as gating function during programmed I/O operations. CS* has no effect during DMA operations. It the non-DMA mode is chosen, the DACK signal should be pulled up to VCC.

Note that during the Result phase all bytes shown in the Command Table must be read.

The Read Data Command, for example has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The ST37C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during

the Result phase. The ST37C65 contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the ST37C65 to form the command phase, and are read out of the ST37C65 in the result phase, must occur in the order shown in the Command table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the command phase is sent to the ST37C65, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the ST37C65 is ready for a new command.

CONTROL REGISTER

The Control Register is a write only register that is used to set the data transfer rate and disable write precompensation. It provides support logic that latches the two LSBs of the data bus upon receiving LDCR* and WR*. CS* should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switch over is internally "deglitched", allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64 times the desired MFM data rate. This implies a maximum data rate of 250 kb/s for a frequency of 16 MHz or a maximum data rate of 500 kb/s for a frequency of 32 MHz, unless the Control Register is used. Switching of this clock must be "glitchess" or the device will need to be reset. Table 1 and Table 2 present the Control Register configuration for 16 MHz and 32 MHz frequencies, respectively.

ST37C65 optionally supports 150 kbits FM data transfer rate. The Control Register configuration is shown in Table 3. The 150 kb/s data rate can be selected by using a 9.6 MHz XTAL or TTL level clock input on pin 26 (44-pin PLCC) or pin 23 (40-pin DIP). Only two data transfer rates can be selected with this configuration 150 kb/s FM and 300 kb/s MFM.

TABLE 1. CONTROL REGISTER CONFIGURATION 16 MHz

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	500 k	MFM	1
0	0	X	250 k	FM	1
0	1	0	250 k	MFM	0
0	1	1	300 k	MFM (9.6 MHz)	0
1	0	X	250 k	MFM, RST Default	1
1	0	X	125 k	FM, RST Default	1
1	1	X	125 k	FM	0

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TABLE 2. CONTROL REGISTER CONFIGURATION 32 MHz

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	1 M	MFM	1
0	0	X	500 k	FM	1
0	1	0	500 k	MFM	0
0	1	1	300 k	MFM (9.6 MHz)	0
1	0	X	500 k	MFM, RST Default	1
1	0	X	250 k	FM, RST Default	1
1	1	X	250 k	FM	0

TABLE 2. CONTROL REGISTER CONFIGURATION - OPTIONS

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	300 k	MFM	1
0	0	X	150 k	FM	1

In AT/EISA mode, write pre-compensation can be disabled by a logic high on bit-2 of the Control Register. (see table 4.)

TABLE 4. CONTROL REGISTER CONFIGURATION - AT/EISA MODE

BIT	SIGNAL NAME AND FUNCTION	RESET	CLOCK QUALIFIER
0	Data rate	0	None
1	Data rate	0	None
2	No Write Pre-compensation	0	None
3-7	Reserved	None	None

MASTER STATUS REGISTER

The Master Status Register is an eight-bit, read/write register that contains the status information of the FDC. It can be accessed at any time. The ST37C65 provides a write only register, called Master Status Register 1 (MSR1) which is used only to select power down mode. In power down mode the XTAL oscillator, controller circuitry and all linear circuitry are turned off so that the controller draws very low current. Normal operation is restored by asserting reset to the ST37C65 (see Master Status Register 1).

Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and ST37C65. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD* or WR* during a Command or Result phase and the setting of DIO and RQM is 12µs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24µs. If 1 Mb/s is selected, the delay is 6µs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12µs. The maximum time from

the trailing edge of the last RD* in the result phase to when DB4 (FDC busy) goes low is 12μs.

MASTER STATUS REGISTER 1
(MSR1 - Write Only)
The ST37C65 will enter power down mode, when bit of MSR1 is set to logical "1" and the following conditions are met:

1.The RST pin to the FDC is inactive.
2.Bit 2 in the Operations Register is "SRST= 1".
3.The ST37C65 is a waiting a command from the host

The ST37C65 can also be programmed with external logic to automatically enter power down mode a few msec. after the beginning of idle mode.

Normal operation is restored when the RST pin to the FDC is active and the FDC is reset. This in turn resets bit of MSR1 register to logic 0.

TABLE 5. AT/EISA MODE. MASTER STATUS REGISTER 1 CONFIGURATION

BIT	SIGNAL NAME AND FUNCTION	RESET	CLOCK QUALIFIER
0	Power down mode (PDM)	0	None
1-7	Reserved	None	None

TABLE 6. MASTER STATUS REGISTER BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	FDD 0 busy	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D1	FDD 1 busy	D1B	FDD number is 1 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D2	FDD 2 busy	D2B	FDD number is 2 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D3	FDD 3 busy	D3B	FDD number is 3 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D4	FDC busy	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
D5	Execution mode	EXM	This bit is set only during execution phase in non-DMA mode. When D5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.

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BIT	NAME	SYMBOL	DESCRIPTION
D6	Data input	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, then transfer is from the processor to Data Register.
D7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking function of "ready" and "direction" to the processor.

TABLE 7. STATUS REGISTER 0 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Unit select 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.
D1	Unit select 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D2	Head select	HS	This flag is used to indicate the state of the head at interrupt.
D3	Not ready	NR	Since drive Ready is always presumed true, this will always be a logic "0" (low).
D4	Equipment check	EC	If the Track "0" signal fails to occur after 77 step pulses per Recalibrate Command, then this flag is set.
D5	Seek end	SE	When the FDC completes the SEEK command, this flag is set to "1" (high).
D6	Interrupt code	IC	See D7.
D7	Interrupt code	IC	D7 = 1 and D6 = 0, invalid command issue. Command which was issued was never started.D7 = 0 and D6 = 0, normal termination of command was completed and properly executed. D7 = 0 and D6 = 1, abnormal termination of command, (AT). Execution of command was started but was not successfully completed.

TABLE 8. STATUS REGISTER 1 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Missing address mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.
D1	Not writeable	NW	During execution of Write Data, Write Deleted Data or Format a Track commands, if the FDC detectes a WP* signal from the FDD, then this flag is set.
D2	No data	ND	During execution of Read Data, Write Deleted Data, or Scan command, if the FDC cannot find the sector specified in the IDR (Internal Data Register), this flag is set. During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the Read a Track command, if the starting sector cannot be found, then this flag is set.
D3	Not used		This bit is always set to "0".
D4	Overrun	OR	If the FDC is set not serviced by the host system during data transfers within a certain time interval, this flag is set.
D5	Data error	DE	When the FDC detects a CRC (Cyclic Redundancy Check) error in either the ID field or the data field, this flag is set.
D6	Not used		This bit is always set to "0".
D7	End od cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.

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TABLE 9. STATUS REGISTER 2 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Missing address	MD	Missing address mark in data field. When data is read from the medium, if FDC cannot find a Data Address Mark of Deleted Data Address Mark, then this flag is set.
D1	Bad cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D2	Scan not	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D3	Scan equal	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D4	Wrong cylinder	WC	This bit is related to the ND bit, and when contents of cylinder on the medium is different from that stored in the IDR, this flag is set.
D5	Data error	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D6	Control mark	CM	During execution of the Read Data or Scan Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D7	Not used		This bit is always set to "0".

TABLE 10. STATUS REGISTER 3 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Unit select 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.
D1	Unit select 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D2	Head select	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D3	Write protected	WP*	This bit is used by the ST37C65 to indicate the status of the Write Protected (WP*) signal from FDD.
D4	Track 0	T0	This bit is used to indicated the status of the Track 0 signal from the FDD.
D5	Ready	RY	This bit will always be a logic "1". Drive is presumed to be ready.
D6	Write protected	WP*	This bit is used to indicate the status of the Write Protected (WP*) signal from FDD.
D7	Not used		This bit is always set to "0".

DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out A0, or written into, the Data Register in order to program or obtain the results after a particular command.The relationship between the Master Status Register and the Data Register and the signals RD*, WR*, and A0 are shown in Table 11.

Table 11. MASTER STATUS AND DATA REGISTER

A0	RD*	WR*	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

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OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving LDOR* and WR*. CS* should not be active when this happens. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to selected the desired disk drive. Table 12 represents the Operations Register.

TABLE 12. OPERATIONS REGISTER

OR0	DSEL	Drive Select, if low and MOEN1 = 1, then DS1* is active. If high and MOEN2 = 1, then DS2* is active, but only in the AT/IEISA mode.
OR1	(X)	This must be a logic 0 for DS1* and DS2* to become active.
OR2	SRST*	Soft reset, active low.
OR3	DMAEN	DMA enable, active in Special and AT/EISA modes. Qualifies DMA and IRQ outputs and DACK* input.
OR4	MOEN1	Motor On enable, inverted output M01* is active only in AT/IEISA mode.
OR5	MOEN2	Motor On enable, inverted output M02* Is active only in AT/EISA mode.
OR6	(X)	Has no defined function. A spare.
OR7	(MSEL)	Mode Select. During a soft reset condition, may be used to select between Special mode (1) and AT/IEISA mode (0).

BASE, SPECIAL, AND AT/EISA MODES

Base, Special, PC AT and EISA modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

Base Mode

After a hardware reset, RST active, the ST37C65 will be held in soft reset, SRST* active, with the normally driven signals, DMA request and IRQ request outputs three-stated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying DMAEN and no soft resets. The Drive Select outputs, DS1* to DS4*, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin RWC* represents Reduce Write Current and is indicative of when write pre-compensation is necessary.

Special Mode

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, SRST*. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing SRST* to be active. Then a read of the Control Register address, LDCR* and places the device in Special mode. The DS1*

through DS4* is again offered in this mode, as is RWC*.

AT/EISA Modes

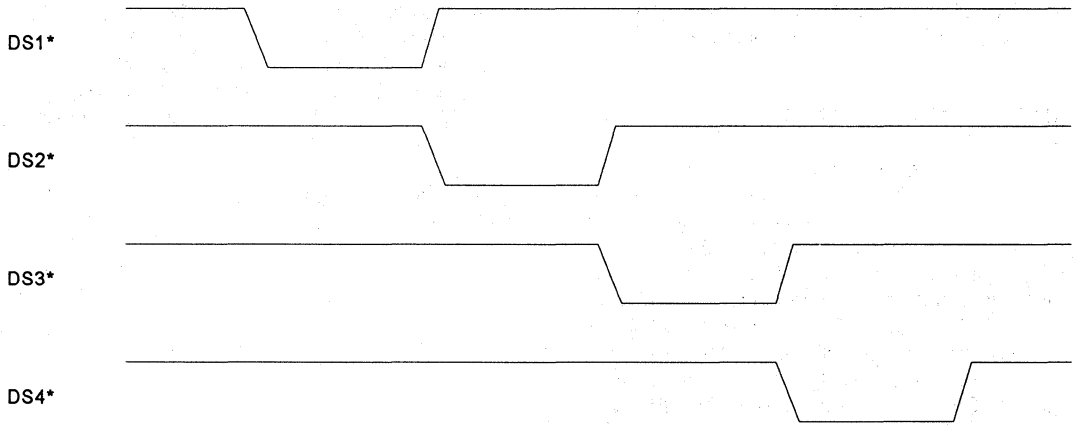
For AT/EISA compatibility, users write to the Operations Register, LDOR* and WR*; this action, performed after a hardware reset, or in the Base mode, initiates AT/EISA mode. AT/EISA mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing SRST* to be active. Then a read of the Control Register address sets the device into AT/EISA mode. The DS* outputs are replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and SRST* are supported and compatible with the current BIOS. RWC* pin function is now RPM* so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low. It can also be used to reduce write current when a slower data rate is selected for a given drive.

POLLING ROUTINE

After any reset the ST37C65, (a hard RST or soft SRST*), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the ST37C65 polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special, AT/EISA modes, if DMAEN is not valid 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the ST37C65 occurs continuously between Each drive is polled every 1.024ms, except during the READ/WRITE commands. For mini- floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3. Note that in the AT/EISA mode, the user will not see the polling at the Drive Select signals. Figure 4 illustrates the Drive Select Polling Timing.

FIGURE 4.

DRIVE SELECT POLLING TIMING



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DEVICE RESETS

The ST37C65 supports both hardware reset (RST pin 19) and a software reset (SRST*) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and selects 250kb MFM (or 125kb FM code dependent) as the data rate (16 MHz input clock) The default data rate for a 32 MHz input clock is 500kb MFM. SRST* will reset the micro controller as did the RST, but will not affect the current data rate selection or the mode RST, when active, will disable the current driver outputs to the disk drive. RST and SRST* will not affect the values set for the internal timers HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the ST37C65 system. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

WRITE PRE-COMPENSATION

The ST37C65 maintains the standard first level algorithm to determine when write pre compensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz or 32 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexed gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24)=1, all data will be pre-compensated by ±125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write pre-compensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ±187ns pre-compensation will be generated. For frequencies other then 16MHz or 32MHz on the CLK1 pin, the pre-compensation values will be two and three clock cycles respectively. When the non-standard 300 kb/s data rate using CLK2 is chosen, the MFM pre-compensation will always be two clock cycles For 9.6 MHz, this is ±208ns. In this case, the PCVAL function is disabled. Write pre-compensation can be disabled by bit-2 of the Control Register for the AT/EISA. The PCVAL input to ST37C65 is ignored if there is no write pre-compensation.

CLOCK GENERATION

This logical block provides all the clocks needed by the ST37C65. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK). SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

MCLK is used by microsequencer. MCLK and MCLK* clock all latches in a two-phase scheme. One micro-instruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 13 presents the Clock Data Rate.

In power down mode the XTAL oscillator and the clok circuitry are turned off.

TABLE 13. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK
1Mb/s	MFM	32.0 MHz	8.0 MHz	2.0 MHz
500 kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
500 kb/s	FM	16.0 MHz	8.0 MHz	1.0 MHz
250 kb/s	FM	8.0 MHz	4.0 MHz	500 kHz
250 kb/s	MFM	8.0 MHz	2.0 MHz	500 kHz
125 kb/s	FM	4.0 MHz	2.0 MHz	250 kHz
300 kb/s	MFM	9.6 MHz	2.4 MHz	600 kHz

COMMAND PARAMETERS

The ST37C65 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command phase, Execution phase, and the Result phase.

- Command phase
  The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

- Execution phase
  The FDC performs the operation it was instructed to do.

- Result phase
  After completion of the operation, status and other housekeeping information are made available to the processor.

Table 14 lists the 15 ST37C65 commands.

TABLE 14. ST37C65 COMMANDS

- Read Data
- Read Deleted Data
- Write Data
- Write Deleted Data
- Read a Track
- Read ID
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek

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TABLE 15. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

TABLE 16. READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

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TABLE 17. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	0	0	0	1	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

TABLE 18. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	0	0	1	0	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				C					Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
EXECUTION										Data transfer between FDD and main system.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

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TABLE 19. READ TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	0	0	0	1	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system. FDD reads all data fiels from index hole to EOT.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

TABLE 20. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	MF	0	0	1	0	1	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first corrected ID information on the cylinder is stored in Data Register.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information read during Execution Phase from floppy disk.
	R				H					
	R				R					
	R				N					

TABLE 21. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	MF	0	0	1	1	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				N					Bytes/Sector.
	W				SC					Sectors/Track.
	W				GPL					Gap 3.
	W				D					Filler Byte.
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					In this case, the ID information has no meaning.
	R				H					
	R				R					
	R				N					

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TABLE 22. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				C					Sector ID informatiom prior to command execution.
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
EXECUTION										Data compared between the FDD and main system.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

TABLE 23. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	1		1	0	0	1	Command code.
	W	X	X	X	X		X	HS	US1	US0	
	W					C					Sector ID informatiom prior to command execution.
	W					H					
	W					R					
	W					N					
	W					EOT					
	W					GPL					
	W					DTL					
EXECUTION											Data compared between FDD and main system.
RESULTS	R					ST0					Status information after command execution.
	R					ST1					
	R					ST2					
	R					C					Sector ID information after command execution.
	R					H					
	R					R					
	R					N					

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TABLE 24. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				C					Sector ID informatiom prior to command execution.
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
EXECUTION										Data compared between FDD and main system.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

TABLE 25. RECALIBRATE

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	1	1	1	Command code.
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 26. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	1	0	0	0	Command code.
	W	X	X	X	X	X	0	US1	US0	
RESULTS	R				ST0					Status information about the FDC at the end of seek operation.
	R				PCN					

TABLE 27. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	0	1	1	Command code.
	W	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT	
	W	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND	

TABLE 28. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	1	0	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R				ST3					Status information about FDC.

TABLE 29. SEEK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	1	1	1	1	Command code.
	W	X	X	X	X	X	0	US1	US0	
	W				NCN					
EXECUTION										Head is positioned over proper cylinder on the diskette.

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TABLE 30. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
A0	Address line 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	Cylinder Number	C stands for the current/selected cylinder (track) number 0 through 255 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D7 - D0	Data Bus	8-bits Data Bus, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the Data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in the ID field.
HLT	Head Load Time	HLT stands for the Head Load Time in FDD (2 to 254 ms in 2 ms increments).
HS	Head Select	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	Head Unload Time	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MultiTrack	If MT is high, a MUTITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the NUMBER of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	Non-DMA Mode	ND stands for operation in the NON-DMA MODE.

TABLE 30. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
PCN	Present Cylinder	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head ar present time.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either READ or WRITE signal.
SC	Sector	SC indicates the number of sectores per cylinder.
SK	Skip	SK stands for SKIP Deleted Data Address Mark.
SRT	Step Rate Time	SRT stabds for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives. In 2's complement format, F (hex)=1 ms, E (hex)=2 ms, etc.
ST0-3	Status 0-3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, If STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectore are read and compared.
US0-1	Unit Select 0-1	US stands for a selected drive; binary encoded, 1 of 4.

COMMAND DESCRIPTIONS

Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time Idefined in Ihe Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read of the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the dala bus. After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next seclor is read and output on the data bus. This continuous read function is called a "Multi- sector Read Operation" The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time thal the DACK* for the last byte of data is

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sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes sector). Table 31 lists the Transfer Capacity.

TABLE 31. TRANSFER CAPACITY

Multi-Track MT	MFM/ FM MF	Bytes/ Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3328	26 at side 0
0	1	01	(256) (26) = 6656	or 26 at side 1
1	0	00	(128) (52) = 6656	26 at side 1
1	1	01	(256) (52) = 13312	26 at side 1
0	0	01	(256) (15) = 3840	15 at side 0
0	1	02	(512) (15) = 7680	or 15 at side 1
1	0	01	(256) (30) = 7680	15 at side 1
1	1	02	(512) (30) = 15360	15 at side 1
0	0	02	(512) (8) = 4096	8 at side 0
0	1	03	(1024) (8) = 8192	8 at side 1
1	0	02	(512) (16) = 8192	8 at side 1
1	1	03	(1024) (16) = 16384	8 at side 1

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette. When N=0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexidecimal.

At the completion of the Read Dala command, the head is not unloaded until after Head Unload Time

Interval (specified in the Specity command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 lo 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 6 and set to 0 and 1) respectively.

If Ihe FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit OS in the first Command Word) is not set (SK=0) then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command after reading all the data in the sector. If SK=1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK=1.

During disk data transfers between the FDC and the processor via the data bus, the FDC must be serviced by the processor every 27μs in the FM mode, and every 19μs in the MFM mode or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 32 shows the values for C, H, A, and N, when the processor terminates the command.

TABLE 32. C, H, R, AND N VALUES

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=1	NC
0	1	Less that EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=1	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=1	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=1	NC

Note: NC (No Change): The same value as the one at the begininning of command execution.

Write Datas

A set of nine bytes is required to set the FDC into the Wide Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent complete the data field. If the Terminal Counl signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Wrile Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data

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command for details

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N= 0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data
This command is the same as the Write Data command except a Deleted Data Address mark Is written at the beginning of the data field instead of the normal Data address mark.

Read Deteted Data.
This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK=0) it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK=1, then the FDC skips the sector with the Data Address mark and reads the next sector

Read A Track
This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts leading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to o and 1 respectively.)

Read ID
The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track
The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed inlo N (number ot bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the ST37C65 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after

each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 33 shows the relationship between N, SC, and GPL for various sector sizes.

TABLE 33. N, SC AND GPL RELATIONSHIP

FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2,3
8" STANDARD FLOPPY					
FM MODE					
	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5 1/4" MINI-FLOPPY					
FM MODE					
	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM MODE					
	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3 1/2" SONY MICRO-FLOPPY					
FM MODE					
	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM MODE					
	256	01	0F	0E	36
	256	02	09	1B	54
	1024	03	05	35	74

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. Ones complement arithmetic is used for comparison (FF=largest number, 00=smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP -8R), and the scan operation is continued. The scan operation continues until one of the following conditions occur the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Regisler 2 is a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and the to terminale the command. Table 34 shows the status of bits SH and SN under various conditions of Scan.

TABLE 34. STATUS OF BITS SH AND SN

STATUS REGISTER 2 COMMAND	BIT-2	BIT-3	COMMENTS
Scan Equal	0	1	DFDD = Dprocessor
	1	0	DFDD ≠ Dprocessor
	0	1	DFDD = Dprocessor
Scan Low or Equal	0	0	DFDD < Dprocessor
	1	0	DFDD > Dprocessor
	0	1	DFDD = Dprocessor
Scan High or Equal	0	0	DFDD > Dprocessor
	1	0	DFDD < Dprocessor

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If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK=0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command If SK=1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK=1), the FDC sets the CM (Conlrol mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors=01, or alternate sectors=02) sectors are read or the MT (Multitrack) is programmed it is necessary to remember that the last sector on tbe track must be read. For example, if STP=02, MT=0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sertor 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27μs (FM mode) or 13μs (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if lhere is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, lhe SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated At this point FDC interrupt goes high. Bits D0B-D3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operalions may be done on up to four drives at once. No other command can be issued as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be shorter than that set in the Specify command by as much as 1ms.

Recalibrate

Tne function of this command is to retract the Read/Write nead within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated If the Track 0 signal is still low after 255 step pulses have been issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also

applies to the Recalibrate command.

Sense Interrupt Status
An Interrupt signal is generated by the FDC for one of the following reasons:

1 Upon entering the Result phase of
- Read Data command
- Read A Track command
- Read ID command
- Read Deleted Data command
- Write Data command
- Format A Cylinder command
- Write Deleted Data command
- Scan commands

2 Ready Line of FDD changes state
3 End of Seek or Recalibrate command
4 During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor During an Execution phase in non-DMA mode, DBS in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands.

The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued. resets the Interrupt signal and via bits 5, 6, and 7 ot Status Register 0 identifies the cause of the interrupt.

TABLE 35. INTERRUPT CAUSE

BIT-5	BIT-6	BIT-7	CAUSE
0	1	1	Ready line changed state, either polarity.
1	0	0	Normal Termination of Seek or Recalibrate command.
1	1	0	Abnormal Termination of Seek or Recalibrate command.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the ST37C65 will Set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 7.

The Specify command sets the initial values for each of the three internal timers: The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state This timer is programmable from 16 to 240ms in increments of 16ms (01=16ms, 02=120ms, 0F=240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F=1ms, E=2ms, D=3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/ Write operation starts. This timer is programmable from 2 to 254ms in increments of 2ms (01=2ms, 02=4ms, 03=6ms . . . 7F=254ms).

The time intervals mentioned above are a dirert lunction of tne clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2. If the clock was increased to 32MHz, then all time in tervals are decreased by half.
The choice ot DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-OMA mode is selected; and when ND = 0, the DMA mode is selected.

Sense Drive Status
This command may be used by the processor to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid
If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set

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to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the ST37C65 is in the Result phase and the contents of Status Register 0 (STD) must be read When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

FIGURE 8. ST37C65 FM MODE FORMAT

GAP (4a) 40x FF	SYNC 6x 00	IAM FC	GAP (1) 26x FF	SYNC 6x 00	IDAM FE	C Y L	H D	S E C	N O	C R C	GAP (2) 11x FF	SYNC 6x 00	DATA AM FB or F8	DATA	C R C	GAP (3)	GAP (4b)

FIGURE 9. ST37C65 MFM MODE FORMAT

GAP (4a) 80x FF	SYNC 12x 00	IAM 3x C2 FC	GAP (1) 50x 4E	SYNC 12x 00	IDAM 3x A1 FE	C Y L	H D	S E C	N O	C R C	GAP (2) 22x 4E	SYNC 12x 00	DATA AM 3x A1 FB F8	DATA	C R C	GAP (3)	GAP (4b)

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	13.5			ns	
T_2	Clock low pulse duration	13.5			ns	
T_3	Clock rise/fall time			2	ns	
T_4	A0, CS*, DACK* set up time to RD* low	0			ns	
T_5	RD* width	90			ns	
T_6	A0, CS*, DACK* hold time to RD* high	0			ns	
T_8	Data access time from RD* low			90	ns	
T_9	Data bus to float delay from RD* high	10		65	ns	
T_{10}	IRQ reset delay time from RD* high			T_{18}	ns	+150ns
T_{11}	A0, CS*, DACK*, LDCR*, LDOR* set up time to WR* low	0			ns	
T_{12}	WR* width	60			ns	
T_{13}	A0, CS*, DACK*, LDCR*, LDOR* hold time from WR* high	0			ns	
T_{15}	Data set up time to WR* high	80			ns	
T_{16}	Data hold time from WR* high	0			ns	
T_{17}	IRQ reset delay time from WR* high			T_{18}	ns	+150ns
T_{18}	DMA cycle time	52			T_{18}	
T_{19}	DACK* delay time from DMA high	0			ns	
T_{20}	DMA reset delay time from DACK* low			140	ns	
T_{21}	DACK* width	90			ns	
T_{22}	RD* or WR* response from DMA high			48	T_{18}	
T_{23}	RD* delay from DMA	0			ns	
T_{24}	WR* delay from DMA	0			ns	
T_{28}	TC delay from last DMA or IRQ, RD*	0		192	T_{18}	
T_{29}	TC delay from last DMA or IRQ, WR*	0		384	T_{18}	
T_{30}	TC width	60			ns	
T_{31}	Reset width - TTL driven CLK1	60			ns	
T_{32}	Chip access delay from RST low	32			T_{18}	
T_{33}	DIRC* hold & set up to STEP* low	4			T_{18}	
T_{34}	STEP* active time low	24			T_{18}	
T_{35}	DIRC* hold time after STEP*	96			T_{18}	
T_{36}	STEP* cycle time	132			T_{18}	
T_{37}	DSX* hold time from STEP* low	20			T_{18}	
T_{38}	IDX* index pulse width	2			T_{18}	
T_{39}	RDD* active time low	40			ns	
T_{40}	WD* write data width low		1/2		WCLK	

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ABSOLUTE MAXIMUM RATINGS

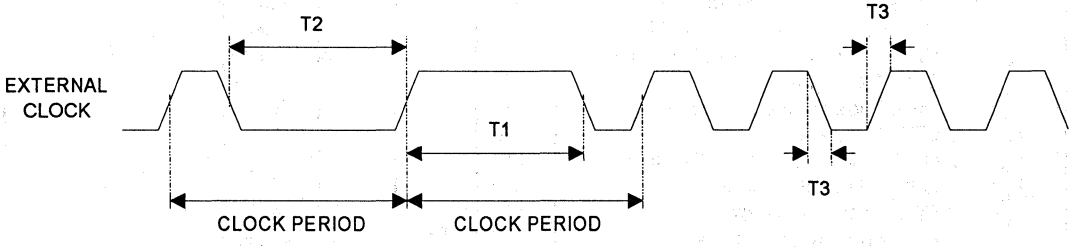
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

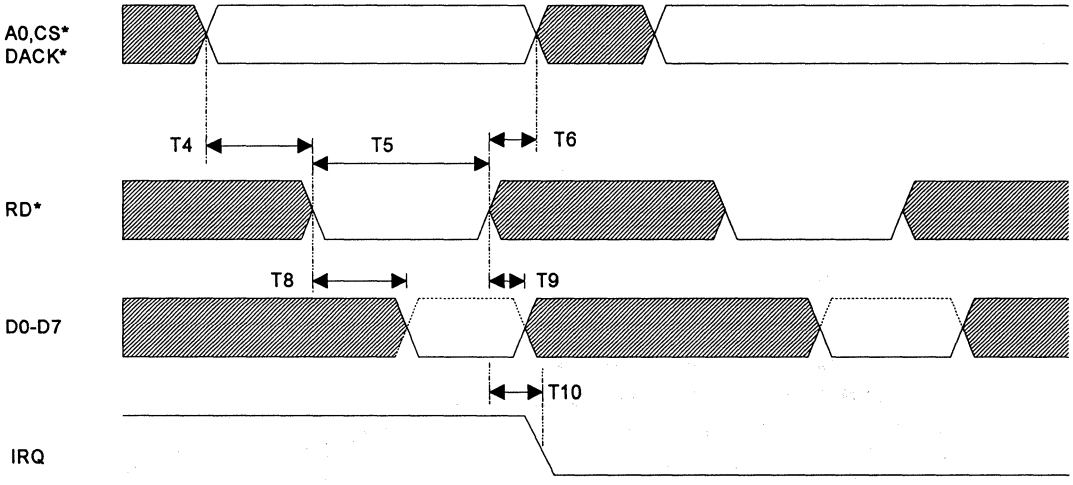
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level for Dx, IRQ, DMA			0.4	V	I_{OL}= 24 mA
V_{OH}	Output high level for Dx, IRQ, DMA	2.8			V	I_{OH}= -5 mA
V_{OLHC}	Output low-high current open drain			0.4	V	I_{OL}= 24 mA
I_{CC}	Avg. power supply current		5		mA	
I_{CCC}	Power down current		100		µA	
I_{IL}	Input leakage			±10	µA	
V_{ILT}	Input low trashold - "Schmitt"	0.8		1.1	V	
V_{IHT}	Input high trashold - "Schmitt"	1.7		2.0	V	
V_{HYS}	Schmitt trigger hysterisis	0.45			V	

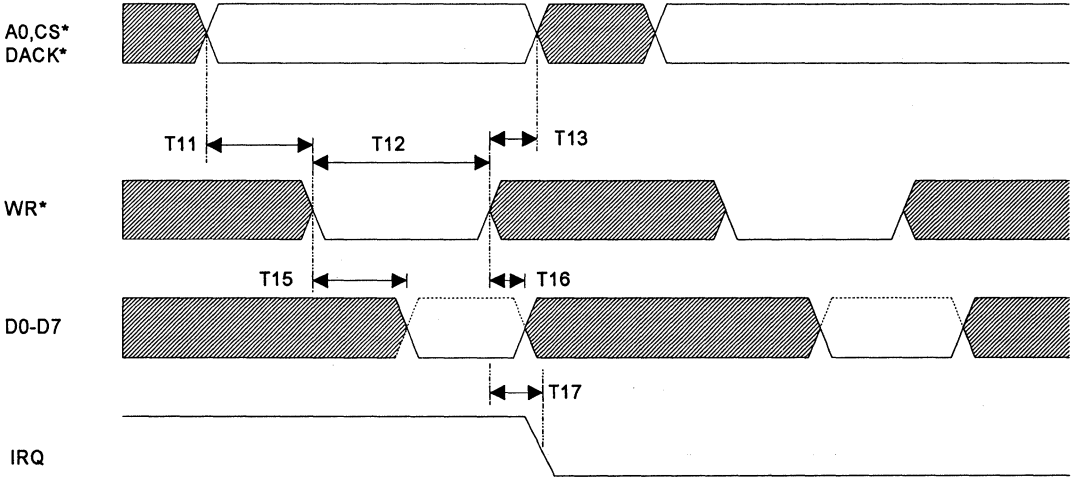
CLOCK TIMING



GENERAL READ TIMING



GENERAL WRITE TIMING



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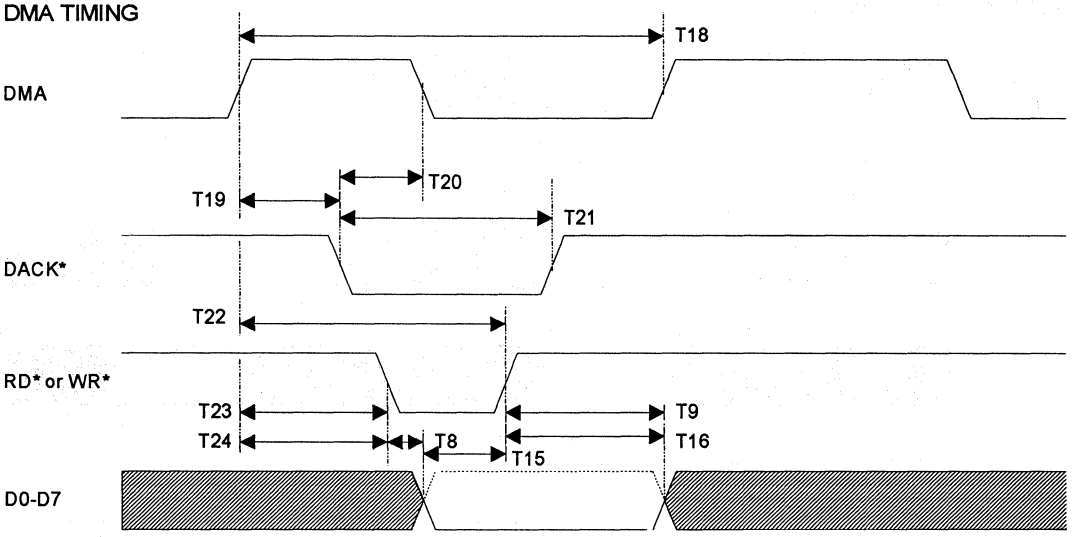
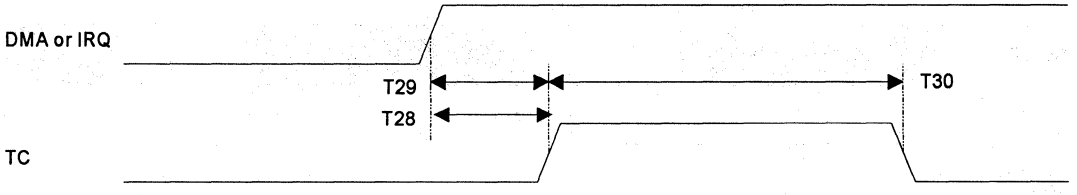
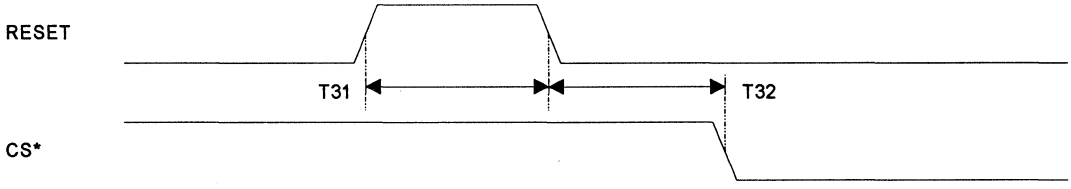
DMA TIMING



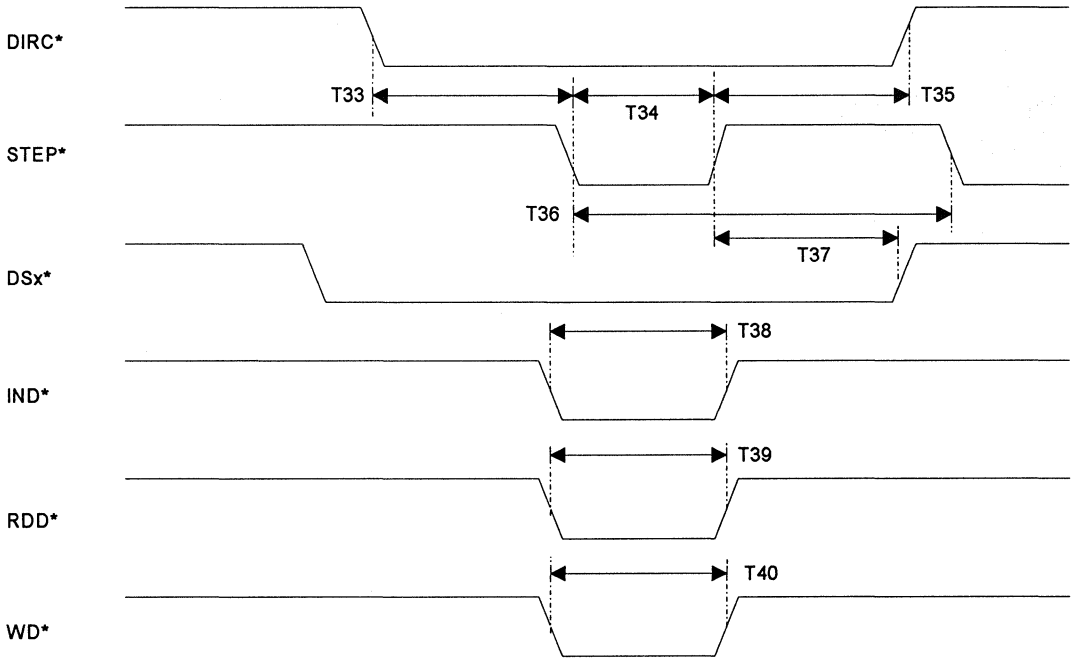
TERMINAL COUNT TIMING



RESET TIMING



DISK DRIVE TIMING



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3.0 VOLT PRODUCTS

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STARTECH

ST16C450

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

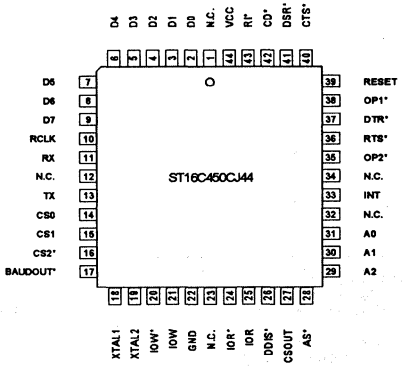
DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C450 provides internal loop-back capability for on board diagnostic testing.

The ST16C450 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



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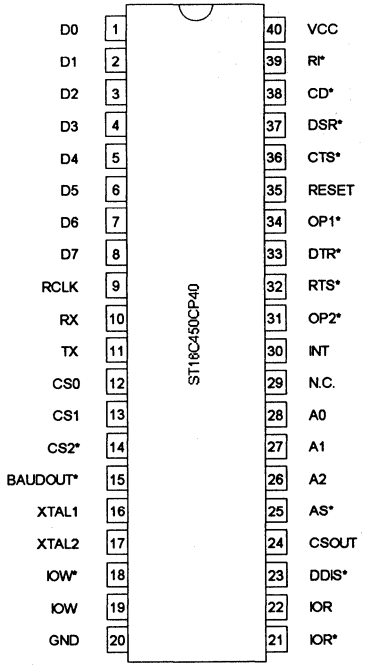
Plastic-DIP Package



FEATURES

- Pin to pin and functional compatible to NS16450,VL16C450,WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C450CP40	Plastic-DIP	0° C to + 70° C
ST16C450CJ44	PLCC	0° C to + 70° C
ST16C450CQ48	TQFP	0° C to + 70° C

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	Note: 2
T_2	Clock low pulse duration	50			ns	Note: 2
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	40			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	15			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select			25	ns	
T_{11}	IOR* to DDIS* delay			50	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	55			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	25			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data	25			ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	*	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

ST16C450

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low.
Note 2: 1.8432 Mhz crystal or External clock.
* = Baudout* cycle

STARTECH

ST16C1450
ST16C1451

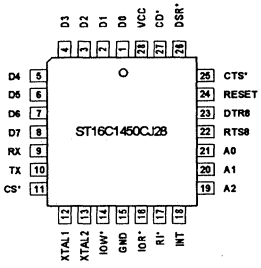
Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C1450/51 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.
The ST16C1450/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1450/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1450/51 provides internal loop-back capability for on board diagnostic testing.
The ST16C1450/51 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



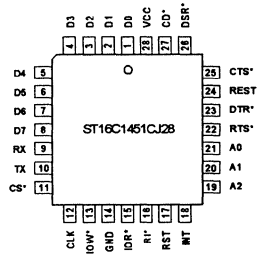
ST16C1450

5

FEATURES

- Pin to pin and functional compatible to SSI 73M1550/2550
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
- Operating supply from 2.7V to 5.25V
- Pin-to-pin compatible to ST16C1550/1551

PLCC Package



ST16C1451

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1450CP28	Plastic-DIP	0° C to + 70° C
ST16C1450CJ28	PLCC	0° C to + 70° C
ST16C1451CP28	Plastic-DIP	0° C to + 70° C
ST16C1451CJ28	PLCC	0° C to + 70° C
ST16C1450CQ48	TQFP	0° C to + 70° C
ST16C1451CQ48	TQFP	0° C to + 70° C

ST16C1450
ST16C1451

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	Note: 1
T_2	Clock low pulse duration	50			ns	Note: 1
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	35			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	105			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	*	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: 1.8432 MHz crystal or External clock
* = Baudout* cycle

ST16C1450
ST16C1451

STARTECH

ST16C2450

Printed February 23, 1994

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

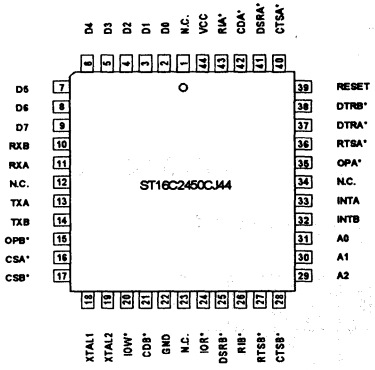
DESCRIPTION

The ST16C2450 is a dual universal asynchronous receiver and transmitter. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART section.

The ST16C2450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C2450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2450 provides internal loop-back capability for on board diagnostic testing.

The ST16C2450 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



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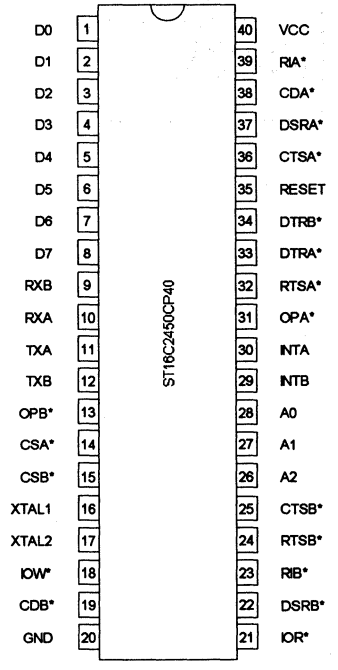
Plastic-DIP Package



FEATURES

- Functional compatible to NS16450, VL16C450, WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2450CP40	Plastic-DIP	0° C to + 70° C
ST16C2450CJ44	PLCC	0° C to + 70° C

ST16C2450

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	15			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C2450

STARTECH

ST16C454

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

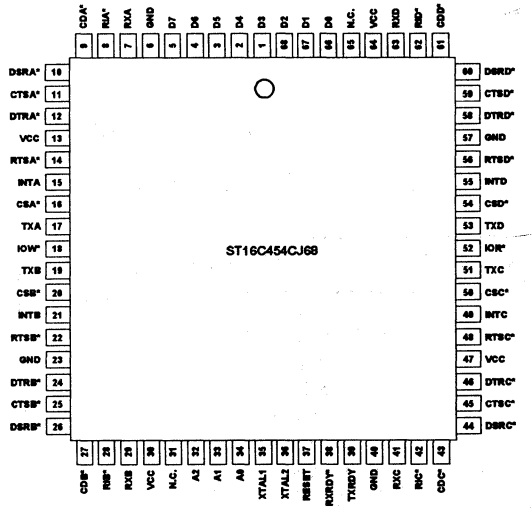
DESCRIPTION

The ST16C454 is a quad universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C454 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C454 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C454 provides internal loop-back capability for on board diagnostic testing.

The ST16C454 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Quad ST16C450
- Pin-to-pin compatible to ST16C554
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C454CJ68	PLCC	0° C to + 70° C

ST16C454

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	15			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C454

STARTECH

ST68C454

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

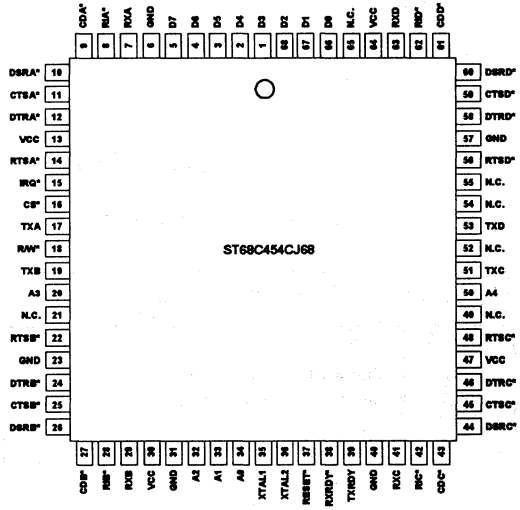
DESCRIPTION

The ST68C454 is a quad universal asynchronous receiver and transmitter with modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST68C454 is an improved, quad version of the NS16450 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C454 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C450
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C454CJ68	PLCC	0° C to +70° C
ST68C454IJ68	PLCC	-40° C to +85° C

ST68C454

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 2 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time from write or CS*	15			ns	
T_{14}	Write set up time	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	15			ns	
T_{17}	Write cycle delay	45			ns	
T_{18}	Data setup time	15			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{24}	Data hold time	0			ns	
T_{25}	Read cycle delay	25			ns	
Tr	Read cycle=T_{18}+T_{25}	105			ns	
T_{27}	Chip select pulse width	75			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			35	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from Read to reset RxRdy			1	µs	
T_{46}	Delay from Write to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

* = Baudout* cycle

ST68C454

STARTECH

ST16C550

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C550 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loop-back capability for on board diagnostic testing.

The ST16C550 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

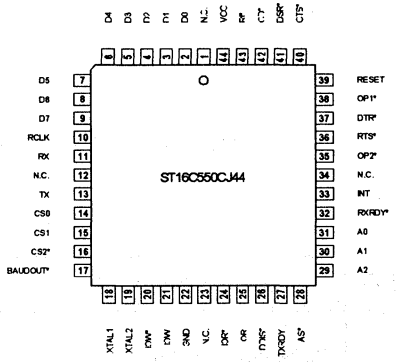
FEATURES

- Pin to pin and functional compatible to NS16550,VL16C550,WD16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C450
- Operating supply from 2.7V to 5.25V

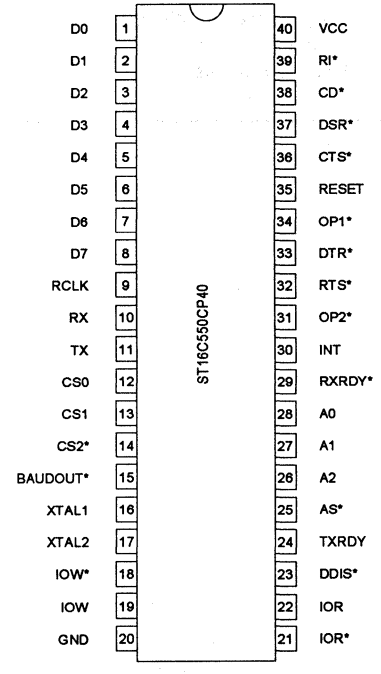
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C550CP40	Plastic-DIP	0° C to + 70° C
ST16C550CJ44	PLCC	0° C to + 70° C
ST16C550CQ52	QFP	0° C to + 70° C
ST16C550CQ48	TQFP	0° C to + 70° C

PLCC Package



Plastic-DIP Package



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ST16C550

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	40			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select	10		25	ns	
T_{11}	IOR* to DDIS* delay			50	ns	100 pF load
T_{12}	Data setup time	15			ns	Note: 1
T_{13}	Data hold time	15			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	10			ns	Note: 1
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load

ST16C550

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{RClk}		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low
* = Baudout* cycle

STARTECH

ST16C1550
ST16C1551/1552

Printed February 23, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C1550/51/52 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1550/51/52 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1550/51/52 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1550/51/52 provides internal loop-back capability for on board diagnostic testing.

The ST16C1550/51/52 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

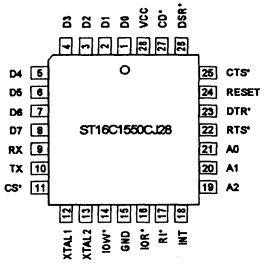
FEATURES

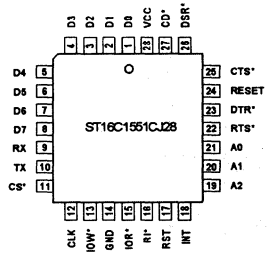
- Pin to pin and functional compatible to SSI 73M1550/2550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

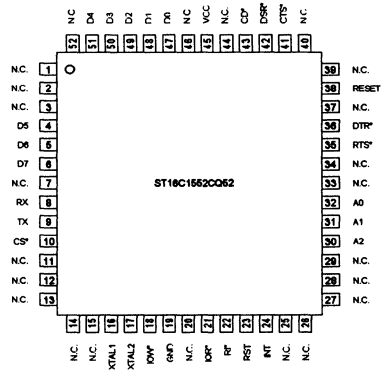
Part number	Package	Operating temperature
ST16C1550CP28	Plastic-DIP	0° C to + 70° C
ST16C1550CJ28	PLCC	0° C to + 70° C
ST16C1550CQ48	TQFP	0° C to + 70° C
ST16C1551CP28	Plastic-Dip	0° C to + 70° C
ST16C1551CJ28	PLCC	0° C to + 70° C
ST16C1551CQ48	TQFP	0° C to + 70° C
ST16C1552CQ52	QFP	0° C to + 70° C

PLCC Package





QFP Package



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ST16C1550
ST16C1551/1552

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	

Note 1: * = Baudout* cycle

ST16C1550
ST16C1551/1552

STARTECH

ST16C2550

Printed February 23, 1994

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

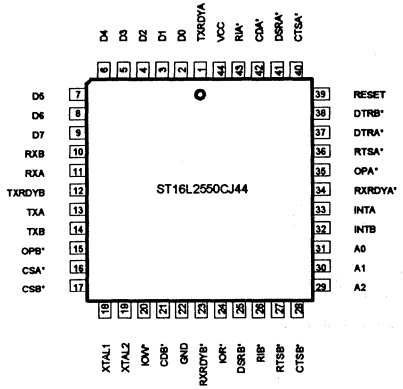
DESCRIPTION

The ST16C2550 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART.

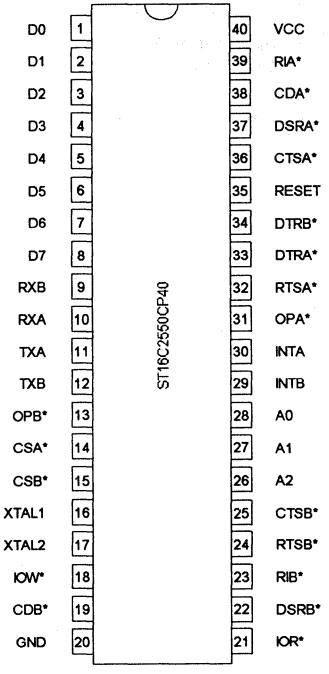
The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C2550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2550 provides internal loop-back capability for on board diagnostic testing.

The ST16C2550 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

- Pin to pin and functional compatible to ST16C2450
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2550CP40	Plastic-DIP	0° C to + 70° C
ST16C2550CJ44	PLCC	0° C to + 70° C

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ST16C2550

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C2550

STARTECH

ST16C2552

Printed February 23, 199

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

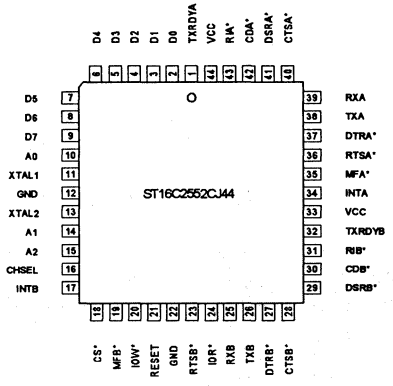
The ST16C2552 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFOs. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART.

The on board status registers of the ST16C2552 provide the error conditions, type and status of the transfer operation being performed. Complete MODEM control capability and a processor interrupt system that may be software tailored to the user's requirements are included. The ST16C2552 provides internal loop-back capability for on board diagnostic testing.

Signalling for DMA transfers is done through two pins per channel (TXRDY, RXRDY*). The RXRDY* function is multiplexed on one pin with the OP2* and BAUDOUT functions. CPU can select these functions through the Alternate Function Register.

The ST16C2552 is fabricated in an advanced 1.2µ CMOS process to achieve low power and high speed requirements.

PLCC Package



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FEATURES

- Pin to pin and functional compatible to National NS16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8) bits
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Independent transmit and receive control
- Software compatible with INS8250, NS16C550
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2552CJ44	PLCC	0° C to + 70° C
ST16C2552IJ44	PLCC	-40° C to + 85° C

ST16C2552

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time			45	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C2552

STARTECH

ST16C554
ST16C554D

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

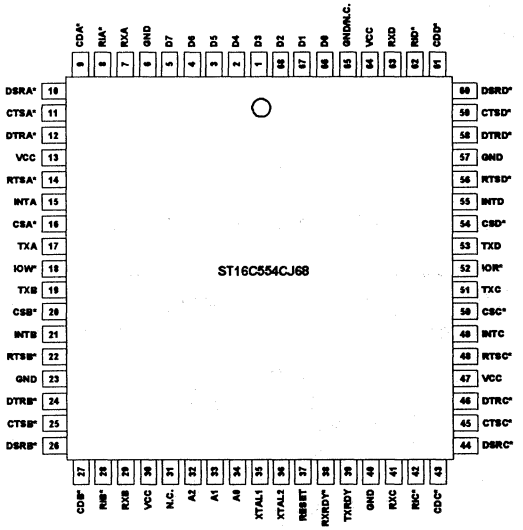
DESCRIPTION

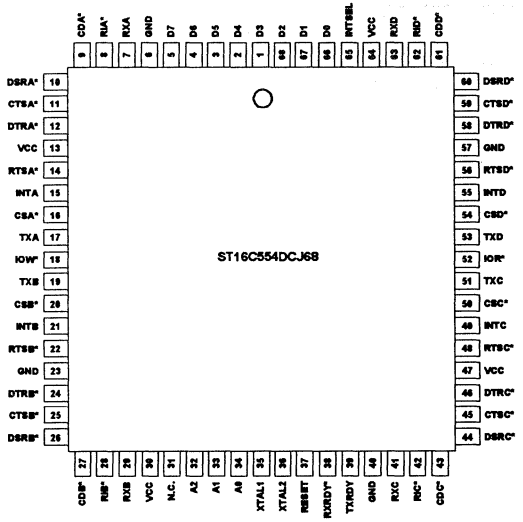
The ST16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C554 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C554 provides internal loop-back capability for on board diagnostic testing.

The ST16C554 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package





FEATURES

- Pin to pin and functional compatible to ST16C454
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554CJ68	PLCC	0° C to + 70° C
ST16C554DCJ68	PLCC	0° C to + 70° C

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ST16C554
ST16C554D

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 2 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{19}	Data hold time	15		25	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
Tr	Read cycle=T_{23}+T_{25}	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: * = Baudout* cycle

ST16C554
ST16C554D

STARTECH

ST68C554

Printed February 23, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

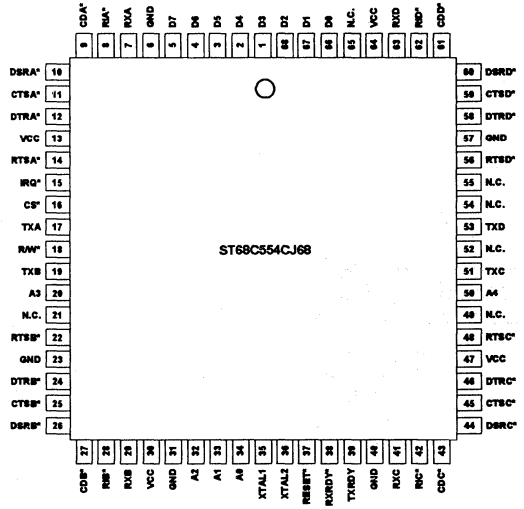
DESCRIPTION

The ST68C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST68C554 is an improved, quad version of the NS16550 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C554 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Operating supply from 2.7V to 5.25V

ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C554CJ68	PLCC	0° C to +70° C
ST68C554IJ68	PLCC	-40° C to +85° C

ST68C554

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 3.3V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.4	V	
V_{IHCK}	Clock input high level	2.2		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.0		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 2 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -2 mA
I_{CC}	Avg. power supply current		3		mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=2.7V to 5.25V unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	50			ns	
T_2	Clock low pulse duration	50			ns	External clock
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	5			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time from write or CS*	15			ns	
T_{14}	Write set up time	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	15			ns	
T_{17}	Write cycle delay	45			ns	
T_{18}	Data setup time	15			ns	
Tw	Write cycle=T_{15}+T_{17}	105			ns	
T_{24}	Data hold time	0			ns	
T_{25}	Read cycle delay	25			ns	
Tr	Read cycle=T_{18}+T_{25}	105			ns	
T_{27}	Chip select pulse width	75			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			35	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from read (CS*) to reset RxRdy			1	µs	
T_{46}	Delay from write to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

* = Baudout* cycle

ST68C554

PRODUCTS PREVIEW 6

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STARTECH

ST78C35

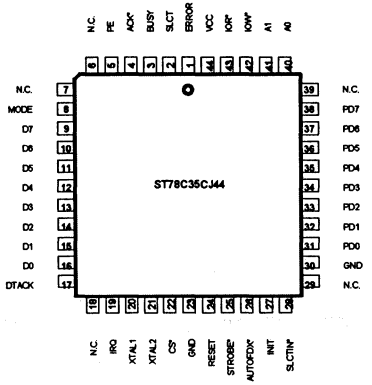
Printed February 23, 1994

GENERAL PURPOSE INPUT/OUTPUT PORT WITH 128 BYTE FIFO

DESCRIPTION

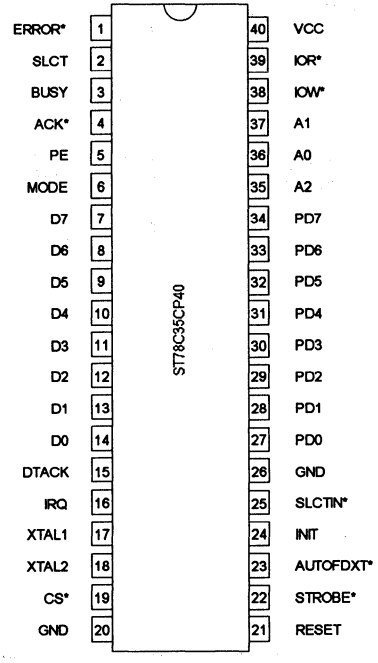
The ST78C35 is a monolithic Bidirectional Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port.
The ST78C35 is a general purpose input/output controller with 128 byte internal FIFO. FIFO operation can be enabled or disabled and configured for either direction. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.
The ST78C35 is designed to operate as normal printer interface without any additional settings. Contents of the FIFO will be cleared after reset or setting the INIT pin to a low state. The auto FIFO operation starts after the first ACK* is received from the printer. Contents of the FIFO transfer to the printer at the printer loading speed. The ST78C35 FIFO can operate as input or output by setting the port direction.

PLCC Package



5

Plastic-DIP Package



FEATURES

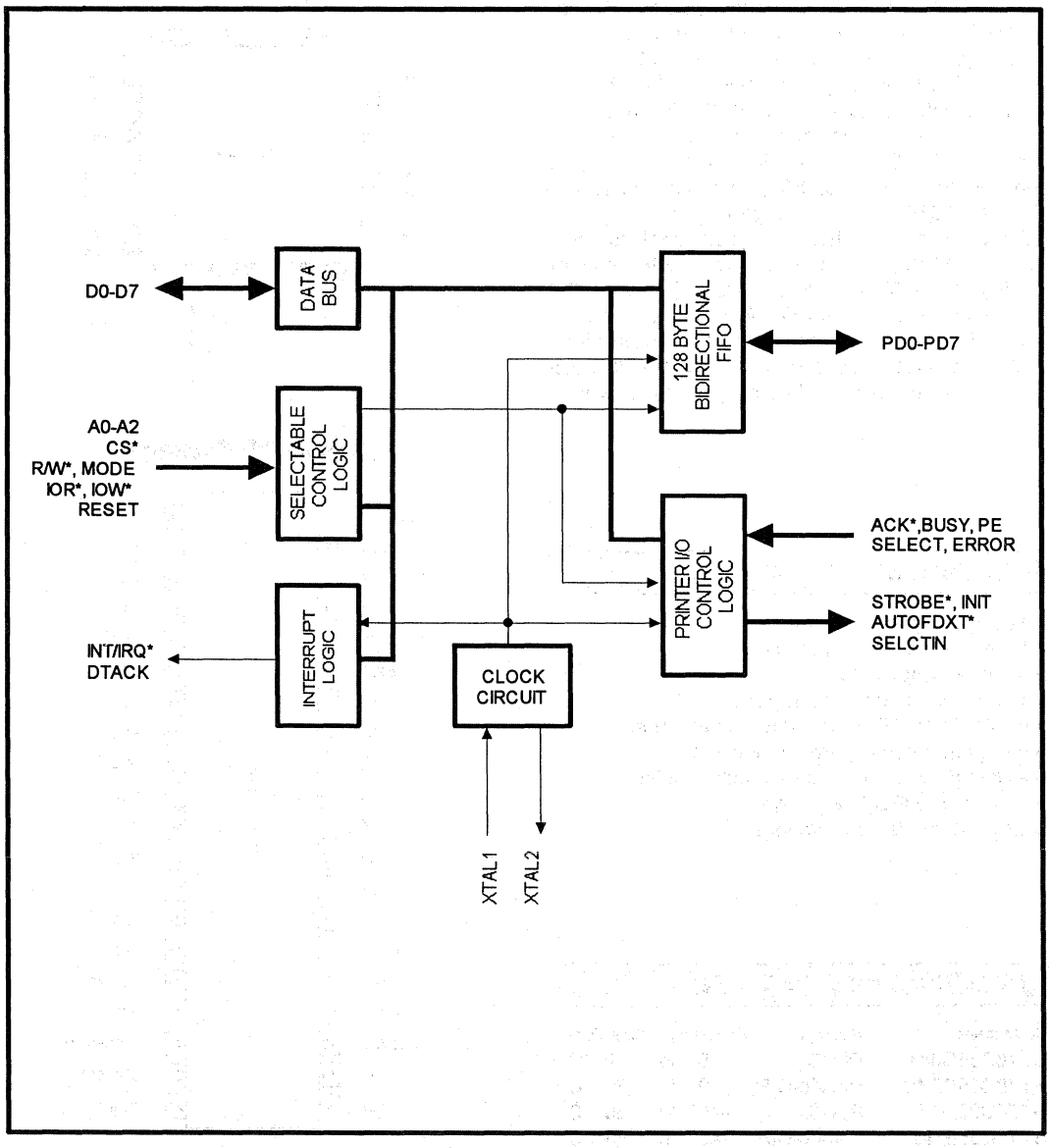
- 128 Byte input/output FIFO
- 5 General purpose input ports
- 8 Bidirectional ports
- 4 Open drain input/output ports
- Replaces all TTL logic for IBM printer port
- IBM printer port register compatible
- 4 User programmable strobe pulse widths
- Selectable FIFO trigger level
- Intel / Motorola bus compatible

ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C35CJ44	PLCC	0° to + 70° C
ST78C35CP40	Plastic-DIP	0° to + 70° C
ST78C35IJ44	PLCC	-40° to + 85° C
ST78C35IP40	Plastic-DIP	-40° to + 85° C

ST78C35

BLOCK DIAGRAM



ST78C35

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
ERROR	1	I	General purpose input or CENTRONICS ERROR input pin.
SLCT	2	I	General purpose input or CENTRONICS SLCT input pin.
BUSY	3	I	General purpose input or CENTRONICS BUSY input pin.
ACK*	4	I	General purpose input or CENTRONICS ACK* input pin.
PE	5	I	General purpose input or CENTRONICS PE input pin.
MODE	8	I	Intel / Motorola Bus select. ST78C35 is set to Intel bus format when this pin is connected to VCC and Motorola bus format when this pin is connected to GND.
D7-0	9-16	I/O	Data bus.
DTACK	17	O	Data acknowledge output. This pin goes low when data has been accepted by ST78C35.
IRQ	19	O	Interrupt output. Three state output when not enabled. Polarity of this pin can be selected via setup register bit-7.
XTAL1	20	I	Crystal or External clock input. Crystal connection between XTAL1 and XTAL2 input/output pins.
XTAL2	21	O	Crystal output pin.
CS*	22	I	Chip select input. Read and write operation to ST78C35 is active when this pin is low.
GND	23	O	Supply ground pin.
RESET	24	I	Reset input pin. Polarity of this pin changes when ST78C35 is configured for Intel or Motorola bus format. This pin is active high when Intel format is selected and active low when Motorola bus format is selected.
STROBE*	25	O	General purpose open drain output or CENTRONICS STROBE* output pin.

* 44-pin PLCC package

ST78C35

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
AUTOFDX*	26	O	General purpose open drain output or CENTRONICS AUTOFDX* output pin.
INIT	27	O	General purpose open drain output or CENTRONICS INIT output pin.
SLCTIN*	28	O	General purpose open drain output or CENTRONICS SLCTIN* output pin.
GND	30	O	Supply ground pin.
PD7-PD0	38-31	I/O	General purpose input/output ports or CENTRONICS DATA port.
A2	39	I	ST78C35 A2 address line.
A0	40	I	ST78C35 A0 address line.
A1	41	I	ST78C35 A1 address line.
IOW*	42	I	Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. This pin is used as R/W* in Motorola bus format.
IOR*	43	I	Read strobe. A low on this pin will read contents of addressed register.
VCC	44	I	Power supply input pin.

PORT REGISTER
Bidirectional I/O or printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER
The state of the four open drain output pins (STROBE*, AUTOFDXT*, INIT, SLCTIN*), and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDX* input pin.
0= AUTOFDX* pin is in high state
1= AUTOFDX* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt is disabled
1= Interrupt is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.
Writing to this register will set the state of the four open drain output pins (STROBE*, AUTOFDXT*, INIT, SLCTIN), and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDX* output control bit.
0= AUTOFDX* output is set to high state
1= AUTOFDX* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

ST78C35

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= IRQ output pin is disabled. Set to three state
1= IRQ output pin is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

SETUP REGISTER
This register sets the ST78C35 operating conditions.

STR BIT-0:
FIFO select bit.
0=FIFO disable (default)
1=FIFO enabled (128 bytes)

STR BIT1-2:
Interrupt source select bits.

STR-2	STR-1	CONDITIONS
0	0	Single character interrupt (ACK*)
0	1	FIFO empty interrupt
1	0	Programmable trigger level interrupt
1	1	FIFO full interrupt

STR BIT3-4:
Strobe width select bits.

STR-4	STR-3	CONDITIONS
0	0	Strobe width=1µs
0	1	Strobe width=2µs
1	0	Strobe width=5µs
1	1	Strobe width=10µs

STR BIT-6:
Interrupt vector select bit.
0=Normal interrupt output. Contents of the interrupt register is read when Address 01 Hex is read.
1=Interrupt vector source selected. Contents of the interrupt vector register is read when Address 01 Hex is read.

STR BIT-7:
Interrupt polarity select bit.
0=Interrupt output pin is active low.
1=Interrupt output pin is active high.

FIFO STATUS REGISTER
This register provides the FIFO enable/disable and FIFO counter location.

FSR bit-0:
0=FIFO disabled
1=FIFO enabled

FSR1-7:
In Use FIFO locations in Hex format.

FIFO INTERRUPT TRIGGER REGISTER
User selectable software control FIFO trigger level interrupt select register.

FIT BIT-0:
0=Normal. Interrupt selected from setup register
1=FIFO trigger level. ST78C35 interrupt output is set when FIFO count reached to FIFO trigger level.

FIT BIT1-7:

FIFO trigger select level in Hex format.

USER DEFINED INTERRUPT VECTOR REGISTER
ST78C35 provides user defined interrupt service jump routine.

IVR BIT0-7:

PRINTER PORT PROGRAMMING TABLE:

A2	A1	A0	IOW*	IOR*
0	0	0	PORT REGISTER	PORT REGISTER
0	0	1		STATUS REGISTER
0	1	0	CONTROL REGISTER	COMMAND REGISTER
0	1	1	SETUP REGISTER	SETUP REGISTER
1	0	0	FIFO INTERRUPT TRIGGER REGISTER	FIFO STATUS REGISTER
1	0	1	INTERRUPT VECTOR REGISTER	INTERRUPT VECTOR REGISTER

ST78C35

ST78C35 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDX*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDX*	STROBE*
	0=Output 1=Input		0=IRQ output disabled (three state) 1=IRQ output enabled				

SETUP REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
IRQ POLARITY	INTERRUPT VECTOR	STROBE	STROBE WIDTH SEL.	INTERRUPT WIDTH SEL.	INTERRUPT SOURCE	FIFO SOURCE	EN/DIS

FIFO INTERRUPT TRIGGER REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
FIFO TRIGGER-6	FIFO TRIGGER-5	FIFO TRIGGER-4	FIFO TRIGGER-3	FIFO TRIGGER-2	FIFO TRIGGER-1	FIFO TRIGGER-0	INTERRUPT TYPE

FIFO STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
FIFO COUNT-6	FIFO COUNT-5	FIFO COUNT-4	FIFO COUNT-3	FIFO COUNT-2	FIFO COUNT-1	FIFO COUNT-0	FIFO STATUS

INTERRUPT VECTOR REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
INTERRUPT VECTOR-7	INTERRUPT VECTOR-6	INTERRUPT VECTOR-5	INTERRUPT VECTOR-4	INTERRUPT VECTOR-3	INTERRUPT VECTOR-2	INTERRUPT VECTOR-1	INTERRUPT VECTOR-0

ST78C35

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.3		0.6	V	
V_{IHCK}	Clock input high level	3.0		Vcc	V	
V_{IL}	Input low level	-0.3		0.8	V	
V_{IH}	Input high level	2.2		Vcc	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*, STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all other outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST78C35

ST78C35

STARTECH

ST78C36

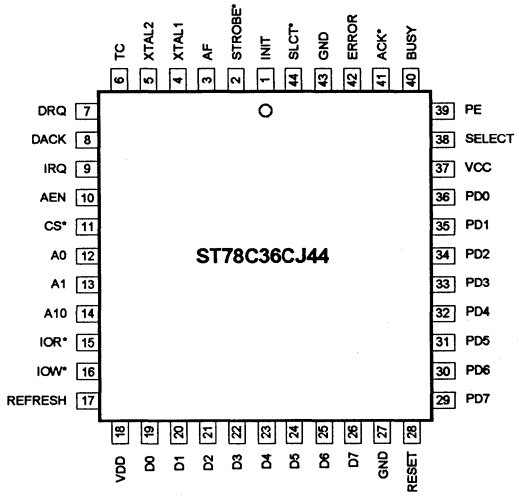
Printed February 23, 1994

ECP/EPP PARALLEL PRINTER PORT WITH 16 BYTE FIFO

DESCRIPTION

The ST78C36 is a monolithic Bidirectional ECP/EPP Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port, MicroSoft/HP ECP, IBM EPP smart printer port. The ST78C36 is a general purpose input/output controller with 16 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.
The ST78C36 is designed to operate as normal printer interface without any additional settings.

PLCC Package



FEATURES

- 16 bytes of printer output FIFO
- Bi-directional parallel port
- Bi-directional I/O ports
- Register compatible to IBM XT, AT, compatible 386, 486
- MicroSoft ECP compatible.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C36CJ44	PLCC	0° C to + 70° C
ST78C36IJ44	PLCC	-40° C to + 85° C
ST78C36CQ48	TQFP	0° C to + 70° C

ST78C36

STARTECH

ST56C5XX

Printed February 23, 1994

ADVANCED HIGH PERFORMANCE SUPER-I/O CONTROLLER

DESCRIPTION

The ST56C5XX is an advanced high performance super-I/O controller, designed to replace the IDE controller, four Floppy controllers, two serial ST16C550 UART's with advanced Microsoft/Hewlett Packard ECP, IBM EPP printer port and game port. The ST56C5XX utilizes digital phase locked loop for the floppy controller section to eliminate the external components (except the main crystal). The ST56C5XX is optimized for mother board applications as well as controller board applications. ST56C5XX provides high ESD circuits on the printer data bus and I/O to prevent damage caused by the printer being powered when the ST56C5XX is not powered.

FEATURES

- Licensed CMOS WD37C65C floppy controller.
- Supports vertical recording format
- 100% IBM compatible
- 48 mA drivers and schmitt Trigger inputs.
- DMA enable logic
- FDC primary and secondary address selection
- Two 16C550 serial ports
- Microsoft/Hewlett Packard Bi-directional ECP parallel port
- IBM EPP (Enhanced Printer Port)
- 16 bit IDE interface and decode logic
- Game port
- 100 pin TQFP and QFP packages
- Low power CMOS 1.2μ technology

ORDERING INFORMATION

Part number	Package	Operating temperature
ST56C5XXCQ100	QFP	0° C to + 70° C
ST56C5XXCTQ100	TQFP	0° C to + 70° C

APPLICATION NOTES 7

GENERAL APPLICATION NOTE FOR STARTECH UART FAMILY

The AN-450 provides additional information to guide users to design or utilize the STARTECH product line. This document can also be used for all the STARTECH UART product lines.

GENERAL INFORMATION

STARTECH offers UART's with or without FIFO capabilities, and are marked as 45X for non FIFO families and 55X for FIFO families. All parts with sharing part numbers are foot print compatible in some extent, like ST16C450 and ST16C550, ST16C2450 and ST16C2550, etc.

This section will describe general terms for commonly used flags and registers.

OVERRUN ERROR:
The flag is set to "1" to warn the user that a serial data has been received and previous serial data has not been read from receive holding register. The new serial data will over write the previous data in the receive holding register. Note that previous serial data has been lost and user does not have an access to that data.

PARITY ERROR:
This flag is set "1" to indicate that received serial data contains mismatched parity or data bit error in the received data.

PARITY:
Four common types of parities are used in the STARTECH Uart families; Odd Parity, Even Parity, Forced Mark Parity and Forced Space Parity.

ODD PARITY:
Odd Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the total count an odd number.

Example -1: A data byte with the following pattern 11010010 will require to add a parity bit of "1" to bring the total count for "1's" to an odd number. Based on this data pattern, serial data with odd parity will be transmitted as 110100101.

Example -2: A data byte with the following pattern 10011000 will require to add a parity bit of "0" to maintain the total count of "1's" to an odd number. Based on this data pattern, serial data with odd parity will be transmitted as 100110000.

EVEN PARITY:
Even Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the count an even number.

Example -3: A data byte with the following pattern 10000101 will require to add a parity bit of "1" to bring the total count for "1's" to an even number. Based on this data pattern, serial data with even parity will be transmitted as 100001011.

Example -4: A data byte with the following pattern 00001111 will require to add a parity bit of "0" to maintain the total count for "1's" to an even number. Based on this data pattern, serial data with even parity, will be transmitted as 000011110.

FORCED SPACE PARITY:
Parity bit on the serial byte is set to "0" regardless of total number of "1's" (even or odd counts).

FORCED MARK PARITY:
Parity bit on the serial byte is set to "1" regardless of total number of "1's" (even or odd counts).

FRAMING ERROR:
The flag is set to "1" to indicate that received data does not have correct start or stop bits. This can cause when the Uarts are set for 8-bits word and receiving a serial data of 7-bits word or any mismatched data patterns.

BREAK SIGNAL INDICATION:
This flag is set to "1" to warn the user that transmitter is sending continuous "0" data without stop bit (RX input is low for more that one word).

TRANSMIT/RECEIVE FIFO:
STARTECH offers 16 byte transmit FIFO and 16 byte receive FIFO for all its products with 55X part numbers. These FIFO's are static 19 X 16 bit RAM with control logic to form a ring counter. Initializing the FIFO will set the write and read pointers to the same location.

TRANSMIT EMPTY:
This flag is set "1" to indicate that, there is no character in the transmit holding and transmit shift register

APPLICATION NOTES

TRANSMIT HOLDING EMPTY:
This flag is set "1" to indicate that, there is one or more empty locations in the transmit holding register. User has to check this bit before loading characters in the transmit holding register. In non FIFO mode, user can load one character at a time when this flag is set and 16 characters when FIFO mode is utilized.

RECEIVER DATA READY:
This bit is set "1" to indicate that, receiver has one or more character in the receive holding register. User has to check this bit prior to read receive holding register. In non FIFO mode, only one character at time can be read. In FIFO mode up to 16 characters can be read if time bit is set.

RECEIVE TIME-OUT:
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -7: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -8: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

BAUD RATE GENERATOR:
STARTECH provides a 16 bit digital divider to obtain all necessary baud rates. The 16 bit divider is broken down in to two 8-bit dividers which will be addressed as MSB divider (upper 8-bits) and LSB divider (lower 8-bits). To calculate the transmit/receive data rate it is necessary to know the provided clock rate (frequency) to STARTECH parts. STARTECH utilizes 16 clocks for each transmit bit and 16 clocks to sample the received data. Note that inorder to access these dividers, user has to enable the divisor latch access bit through the Line Control Register.

Bit rate is calculated by:
Dividing decimal number = (Clock rate) / (16 X bit rate).
To program the digital divider, dividing decimal number should be converted to hex (base 16) number and split into two 8-bits sections.

Example -5: To obtain 4800 Hz baud rate, assuming 1.8432 MHz input clock, the dividing decimal value is (input clock=1843200) / (16 X 4800) = 24

24 decimal = 0018 Hex, this value is translated to MSB = 00 Hex and LSB = 18 Hex.

BAUD RATE VERSUS BIT RATE:
The baud rate defines the width of each bit regardless of word, parity and stop bit length. Bit rate, is the rate of the transmission which each character is transmitted or received. The 2400 baud rate transmission is translated to 2400 Hz per bit for each character in a word. With 2400 baud you can transmit between 7 to 12 characters per slot.

PROGRAMMING STEPS:
The AN-450 provides the easy steps to program STARTECH Uart family. Note that all numbers are in Hex format not decimal.

Write 80 Hex to **LCR** (Line **C**ontrol **R**egister) to enable baud rate generator divider latch
to set 2400 Hz baud rate:
write 00 Hex to MSB of baud rate generator (address location 1).
Write 30 Hex to LSB of baud rate generator (address location 0).

Select you word, parity and stop bit format from STARTECH Uart data sheet.
to set 8 bits, no parity and one top bit and disable the divisor access latch
write 03 Hex to **LCR** (Line **C**ontrol **R**egister):

if you need to use Uarts with FIFO, select your receive trigger level from data sheet.
to enable FIFO with 14 character trigger level
write CF Hex to **FCR** (FIFO **C**ontrol **R**egister)

enable interrupt sources
write 01 Hex to **IER** (Interrupt Enable Register) to select receive interrupt.

to set RTS and DTR outputs to low and enable the interrupt output
write 0B Hex to **MCR** (Modem Control Register).

The STARTECH Uart is ready for transmit and receive operation.

Read **MSR** (Modem Status Register) to check the status of **CD, RI, DSR, CTS** input pins.

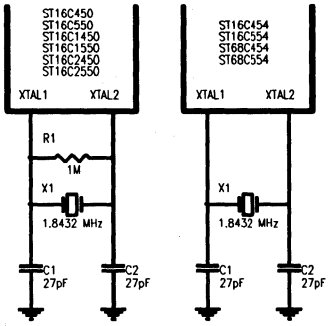
Read **LSR** (Line Status Register).

For polling applications (non interrupt mode) user has to monitor bit zero of this register to verify valid data in the receive holding register.

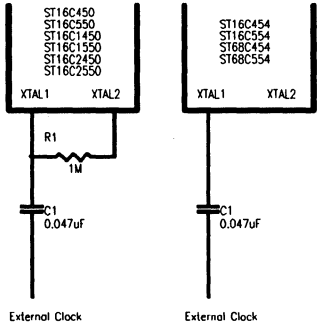
Check the Transmit Holding Empty bit before loading data in the transmit holding register,

continue the transmission.

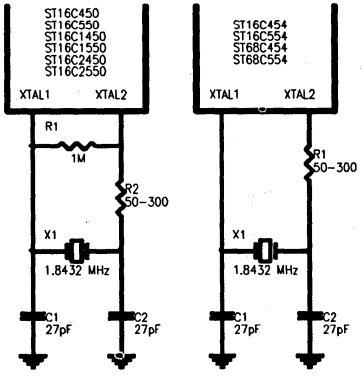
Parallel Crystal Connections



External Clock Connections



Serial Crystal Connections



APPLICATION NOTES

C PROGRAM SAMPLE

```
; File: sample.c          Package:UART init
; This is a sample code to show how to initialize the UART series of chips
; from Startech Semiconductors.
; This also includes some basic external loop back thru' two different
; ports using the FIFO capability.
; This also includes external loop back thru a different computer

#include    <stdio.h>
#include    <string.h>
#include    <fcntl.h>

#define     TRUE                1
#define     FALSE               0

/* These are the various offsets for the registers inside the chip */
#define     RHR                 0x00  /* Receive Holding Register    */
#define     THR                 0x00  /* Receive Holding Register    */
#define     IER                 0x01  /* Interrupt Enable Register   */
#define     FCR                 0x02  /* FIFO control Register       */
#define     ISR                 0x02  /* Interrupt Status Register   */
#define     LCR                 0x03  /* Line control register       */
#define     MCR                 0x04  /* Modem Control Register      */
#define     LSR                 0x05  /* Line Status Register        */
#define     MSR                 0x06  /* Modem Status Register       */
#define     SCR                 0x07  /* Scratch pad Register        */

/* This two offsets are used for defining the baud rate      */
#define     DIVLSB              0x00  /* Divisor LSB latch address   */
#define     DIVMSB              0x01  /* Divisor MSB Latch address   */

/*\
 * Program table for baud rate
 * This represents the LSB and MSB divisor latch data
\*/
char baud_table[8][2] = {
        { 0x80, 0x01 },             /* 300  */
        { 0x60, 0x00 },             /* 1200 */
        { 0x30, 0x00 },             /* 2400 */
        { 0x0c, 0x00 },             /* 9600 */
        { 0x06, 0x00 },             /* 19K  */
        { 0x03, 0x00 },             /* 38k  */
        { 0x02, 0x00 },             /* 56k  */
        { 0x01, 0x00 }              /* 115k */
};
```

```
/* Baud Rates */
#define     _COM_300_           0
#define     _COM_1200_          1
#define     _COM_2400_          2
#define     _COM_9600_          3
#define     _COM_19K_           4
#define     _COM_38K_           5
#define     _COM_56K_           6
#define     _COM_115K_          7

/* Parity */
#define     _COM_NOPARITY_      0
#define     _COM_ODDPARITY_     1
#define     _COM_EVENPARITY_    2

/* Stopbits */
#define     _COM_STOP1_         0
#define     _COM_STOP2_         1
#define     _COM_STOP1_5_       1

/* word length */
#define     _COM_CHR5_          0
#define     _COM_CHR6_          1
#define     _COM_CHR7_          2
#define     _COM_CHR8_          3

/* word length */
#define     _COM_FIFO1_         0
#define     _COM_FIFO4_         1
#define     _COM_FIFO8_         2
#define     _COM_FIFO14_        3

/*\
 * This function checks the existence of a port.
 * It is very simple. Take the port address then write to the scratch pad
 * an the read it back. If the data read back the same as one that was
 * written then return TRUE else return FALSE.
\*/
int
check_port(com_port)
int com_port;
{

  int i;

     printf("Checking for port %4xH\n",com_port);
  /* Write 1010 1010 (0xaa) to scratch pad*/
```

```
    printf("Writing AAH in %4xH\n",com_port);
  outportb(com_port + SCR, 0xaa);

  /* read it back. If it the same then return TRUE */
  i = inportb(com_port + SCR);

    printf("Read back %2xH from %4xH\n",i,com_port);

  if( i == 0xaa)
      return TRUE;
  else
      return FALSE;

}

/*\
 * This is the work horse function which actually setups the UART.
 * It needs to know every thing.
\*/
int
init_uart(port,baud,parity,data,stop,fifo,trigger)
int port,baud,parity,data,stop,fifo,trigger;
{

  char lcr_byte;

  /* Set divisor latch */
  outportb(port+LCR, 0x80) ;

  printf("Divisor Latch is %2xH %2xH (High Low)\n",
                        baud_table[baud][1],baud_table[baud][0]);
  outportb(port+DIVLSB, baud_table[baud][0]) ;
  outportb(port+DIVMSB, baud_table[baud][1]) ;


  /* Reset to normal Programming */
  /* Program the lcr_byte for the above parameters */
  lcr_byte = 0x00;
  lcr_byte = data; /* Set the  bit0 & bit1 for word length */
  lcr_byte ;= stop << 3; /* Set the bit2 for stop bit */
  if(parity != _COM_NOPARITY_) {
    lcr_byte ;= 1 << 4;  /* Set the bit3 for parity */
    if(parity == _COM_EVENPARITY_)
      lcr_byte ;= 1 << 5; /* Set the bit4 for EVEN parity */
  }

  printf("LCR byte is %2xH\n",lcr_byte);
  /* Program LCR  */
```

```
  outportb(port+LCR, lcr_byte) ;

  if(fifo) {
    char fifo_byte;

    printf("Programming FIFOs without DMA mode\n");

    /* Have to first set the fifo enable */
    fifo_byte = 0x01;
    outportb(port+FCR,fifo_byte);

    /* Now program the FIFO */
    fifo_byte = 0x07; /* set bit0 - FIFO enable, Reset RCVR and XMIT FIFO */
    fifo_byte ;= trigger << 7; /* set bit6 and bit7 with the trigger level */

    /* Program FCR */
    outportb(port+FCR,fifo_byte);
    if(~(inportb(port + ISR) & 0xc0)) {
        printf("This port %4xH does not have FIFOs\n");
        printf("Hence did not program Enable FIFOs\n");
    }
  }

  /* Program IER */
  printf("Programming IER for interrupt on bit0 RCV holding Register\n");
  outportb(port+IER, 0x01);

  return TRUE;
}

/*\
 * This is the test mode.
 * It gets the address of the ports checks to see if they are there.
 * Note: If a driver already exists I am not sure how to temporarily remove it.
 * Well we will worry about it later.
 * Warn the use to remove any drivers that are on the ports.
 * Especially the mouse driver.
 * pass the address to the test552 routine.
\*/
int test_mode()
{
        int i,j,k; /* generic variables */
        char port1[10], port2[10];
        int pt1,pt2;  /* this are the integer port numbers */

        void test552();

        printf("WARNING: This program will not work if the ports to be tested\n");
```

```
        printf("       have drivers installed in them. e.g Mouse driver\n");
        printf("       Please remove the drivers before doing this test.\n");

        while(TRUE) {
          printf("First Port Address (In HEX) > ");
          scanf("%s",port1);
          pt1 = strtol(port1,NULL,16);
          fflush(stdin);
          /*\
           * Check if this port exists. else loop
          \*/
           if(check_port(pt1))
               break;
           printf("Error: Port %4xH does not exist. Try again\n",pt1);
        }


        while(TRUE) {
          printf("Second Port Address (In HEX) > ");
          scanf("%s",port2);
          pt2 = strtol(port2,NULL,16);
          fflush(stdin);
          /*\
           * Check if this port exists. else loop
          \*/
           if(check_port(pt2))
               break;
           printf("Error: Port %4xH does not exist. Try again\n",pt2);
        }

        /* Test 554 with the two port addresses */
        test552(pt1,pt2);

        return TRUE;

}


/*\
 * It first generates a random number for the data size to be generated.
 * Then generates a random data whose length is equal to the data size.
 * It puts it out on both the ports and polls for the interrupt to occur.
 * It reads both the ports until all characters are received OR a timeout
 * has occured. It then prints out the error Messages if any.
 * This loop is done for ever.
\*/
```

```
void test552(p1,p2)
unsigned int p1, p2;
{
  int i,j,c,w,n;
  unsigned char outbuf[20], inbuf1[20], inbuf2[20];
  unsigned char pbuf[200];
  unsigned long timeout, pass;


  printf("ST16C552 External Loop Test Beginning\n") ;
  printf("Testing ports %4x and %4x\n\n", p1, p2) ;
  printf("Programing ports for 56K,8 bit,no parity,1 stop bit,FIFO trigger level 01\n");
  printf("This program uses POLLED mode for testing\n");
  printf("Press Cntrl-C to stop the testing and quit\n");
  printf("Note: The ports will remain at the above settings after the TEST\n");

  /* Programming ports for 8 bits, no parity, 56K baud,
                          FIFO enabled at level 01 */
  /* Program first port */
  printf("Programming port %x4\n",p1);
  init_uart(p1,_COM_56K_,_COM_NOPARITY_,
        _COM_CHR8_,_COM_STOP1_,TRUE,_COM_FIFO1_);

  /* Program Second Port */
  printf("Programming port %x4\n",p2);
  init_uart(p2,_COM_56K_,_COM_NOPARITY_,
        _COM_CHR8_,_COM_STOP1_,TRUE,_COM_FIFO1_);

  printf("Starting test\n");
  for (pass = 1 ; ; pass++) {
      /* generate random size for data */
      n = rand() ;
      n += n >> 8 ;
      n &= 0x0f ;

      /* Make sure we never get a 0 as the random size data */
      if(n != 0x0f)
        n++ ;

      /* generate random data */
      for (w = 0 ; w < n ; w++) {
          c = rand() ;
          c += c >> 8 ;
          c &= 0xff ;
          c ;= 0x01 ; /* no NULLs allowed */
          outbuf[w] = c ;
      }
```

```
outbuf[w] = NULL;

printf("******** Pass %10ld Sending %d *********\015", pass, n) ;

/* Transmitt the data */
for (i = 0 ; i < n ; i++ ) {
      outportb(p1, outbuf[i]) ;
      outportb(p2, outbuf[i]) ;
}

/* loop waiting for intr pending */
for ( i = 0;;i++ ) {
      if ((~inportb(p1+ISR) & 0x01) && (~inportb(p2+ISR) & 0x01))
            break;
}

/* receive data until all has been received OR timeout */
timeout = 0x0008F ;
for (i = j = 0; ((i < 20) && (j < 20));) {
      if (inportb(p1+LSR) & 0x01) inbuf1[i++] = inportb(p1) ;
      c = rand() ;
      c += c >> 8 ;
      c &= 0x001f ;
      c++ ;
      for ( ; c != 0; c—) ;
      if (inportb(p2+LSR) & 0x01) inbuf2[j++] = inportb(p2) ;
      if (timeout— == 0) break ;
}

/* If timed out then print message else comparse data */
if(timeout == 0 )
      printf("Timed out on Ports\n");
else {
  inbuf1[i] = inbuf2[j] = NULL;
  /* compare results */
  if (strcmp(outbuf, inbuf1) ;; ( i != n)) {
        printf("\nError:%04x Sent:    ", p2) ;
        for ( w = 0; w < n; w++ )
              printf(" %02x", outbuf[w]) ;
        printf("\n%04x Received:", p1) ;
        for ( w = 0; w < i; w++ )
              printf(" %02x", inbuf1[w]) ;
        printf("\n") ;
  }
  if (strcmp(outbuf, inbuf2) ;; ( j != n )) {
        printf("\nError:%04x Sent:    ", p1);
        for ( w = 0; w < n; w++ )
              printf(" %02x", outbuf[w]) ;
```

```
                printf("\n%04x Received:", p2) ;
                for ( w = 0; w < j; w++ )
                        printf(" %02x", inbuf2[w]) ;
                printf("\n") ;
            }
        }
    }
}
```

APPLICATION NOTES

GENERAL APPLICATION NOTE FOR STARTECH CLOCK FAMILY

The ST49CXXX video / memory clock chips provide 5-130 MHz clock outputs which may cause unwanted EMI problems.
To minimize problems with meeting FCC EMI requirements, consideration should be given to the following sections of the board design.

Power supply conditioning
Printed Circuit Board Layout
Video / Memory clock outputs and drive capabilities
External clock sources
Reference clock sources
Digital control / select inputs
External loop filters

Power supply considerations
Some of the ST49CXXX clock chip contained internal loop filters for VCO circuits and some utilize external components. In both cases it is required to have spike free (or minimum) and stable supply source to the chips. To provide stable and clean supply voltage to STARTECH clock chips we recommend to use 0.1μF capacitors close to IC's power supply lines (VCC, AVCC and DVCC inputs). Analog and digital supply lines are separated from each other to reduce noise generated due to internal digital switching.
In most of the design cases +5V and +12V supplies are provided. A clean +5V supply can be obtained from the +12V supply by utilizing a 470Ω drop resistor and 5.1V zener diode bypassed by 0.047μF and 2.2μF Tantalum capacitors (or higher) to ground.
Trace width should be maximized from the supply source and good ground planes on top and bottom layers of the printed circuit board are recommended.

Printed Circuit Board (PCB) layout
We recommend to place all external components as close as possible to the clock chips to reduce trace length between pin and component connections. It is important to keep components not related to clock IC's (DRAM and other memory devices) far and not share the grounds. In applications utilizing a multi-layer board, GND, AGND, and DGND should be directly connected to the ground plane.

Video / Memory clock outputs and drive capabilities
Video clock is usually the highest frequency present in video graphics system board/card and consideration should be given to FCC EMI requirements.
The trace connecting DCLK and MCLK clock output pins to other components should be kept as close as possible and ferrite beads should be used (with optional 33Ω resistor in series with ferrite beads) to reduce the possible emitting signals and jitter.

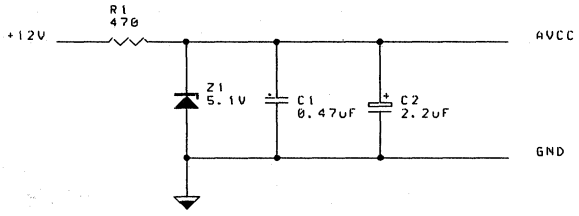
External clock sources
When an external clock source is used to bypass the internal VCO to DCLK and MCLK outputs, clock should have fast rise / fall times and minimum jitter. This signal will be connected internally to the clock output pin when it is selected / enabled. The internal VCO circuit will be locked to its internal selected frequency.

Reference clock sources
The internal oscillator circuit contains all of the passive components required for the external crystal. An appropriate parallel resonant crystal should be connected between XTAL1 and XTAL2.
The crystal leads and input pins should be maintained as close as possible, and the body of the crystal should be grounded to minimize the noise pickup. For IBM compatible applications, the 14.31818 MHz system or crystal clock is used as a reference clock to the chip.

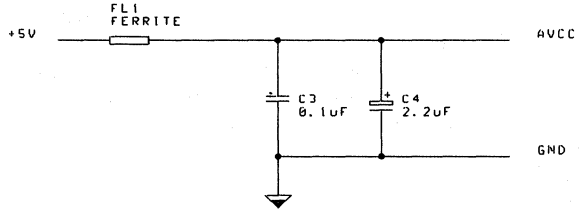
Digital control / select inputs
The ST49CXXX provides TTL compatible address select and latch input pins to interface with CMOS or TTL / LSTTL devices. The A0-A4 and M0-M1 can also be connected to the Data bus if required.

APPLICATION NOTES

EXAMPLE-1:
SUPPLY CONNECTION FROM +12V SUPPLY



EXAMPLE-2:
SUPPLY CONNECTION FROM +5V SUPPLY



QUALITY/RELIABILITY 8

QUALITY AND RELIABILITY

1.0 Quality and Reliability information

The STARTECH semiconductor quality program starts with the design of new products. Each design circuit performance is verified using simulations over voltage and temperature values beyond those of specified product operation.

The design process includes consideration of quality issues such as signal levels, power dissipation, noise generated from internal clock circuits and testability of all device functions.

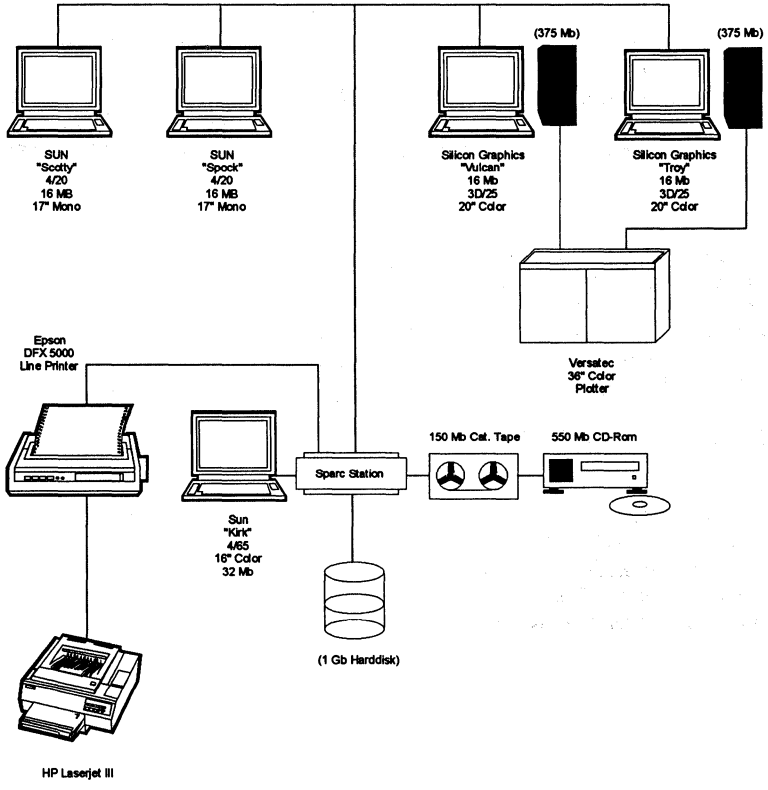
The STARTECH semiconductor document control department maintains control over all manufacturing specifications, lot travelers, procurement specifications and drawings and test programs.

All changes of design are subject to approval by the Engineering, Quality and Manufacturing managers.

STARTECH semiconductor performs a thorough internal product qualification prior to the delivery of any new product or enhanced existing products other than prototypes/samples.

1.1 Design Tools

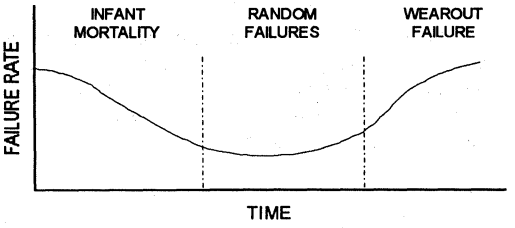
Schematics entry:	View Logic
Logic & Fault simulators:	Startech Advanced Logic simulator
Layout Synthesis:	Goliath (Startech Layout synthesis)
Layout Editor:	Opal
Layout Verification:	Dracula



QUALITY / RELIABILITY

150 samples from three different product lots are selected to perform extended temperature operation test, 85° C/ 85% R.H. / 5.5V temperature humidity bias. Same samples are used for accelerated burn-in and electro-static tests.

STARTECH semiconductor subcontracts its fabrication process to ORBIT semiconductor located in Sunnyvale, California. Packaging and final testing are also subcontracted to other vendors located locally or overseas.



1.2 Determination of the Failure Rate

In the simplest form, the failure rate prediction at a given temperature can be predicted as follows.

Failure rate= N/DH

Where:

N= number of failures
D= number of devices
H= number of hours tested

assuming that semiconductors exhibit a log normal distribution.

Acceleration Factors

The effects of temperature, voltage, time and other related functions are key when predicting life times of semiconductor devices. Understanding these effects with the use of a more accurate mathematical model, provides a better means of evaluating the change in reaction rate to changes in temperature.

$$F(T1, T2)= \exp (-Ea/k (1/T1- 1/T2))$$

Where:

F= Acceleration factor
T1= Test temperature (° C+273)
T2= Desired temperature (° C+273)
k= Boltzman's constant (8.63 E-5eV / K)
Ea= Thermal activation energy (eV)

The equivalent device hours can be determined at temperature T2 can be expressed as:

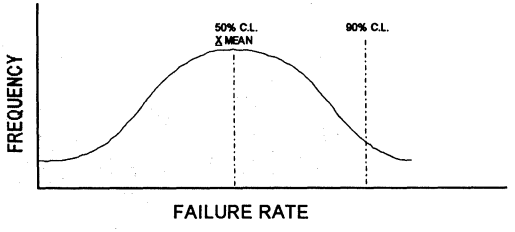
$$EDH (T2) = F (T1, T2) \times DH (T1)$$

The failure rate at T2 can be expressed as:

$$\text{Failure rate } (T2)= N/EDH (T2)$$

Where:

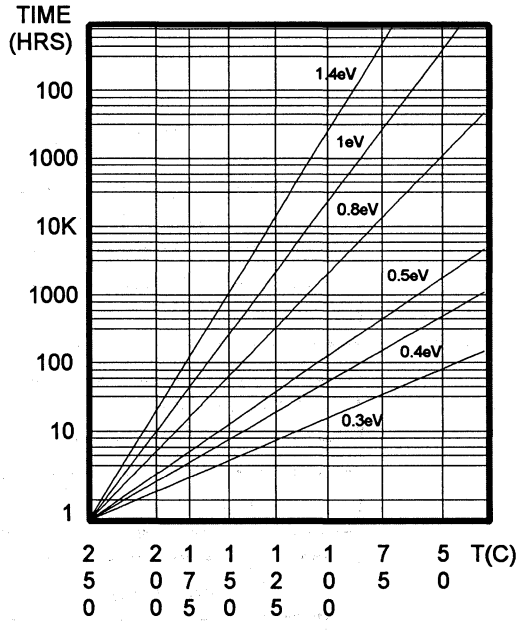
N= Number of failures
EDH= Equivalent device hours



C.L.=Confidence Level

1.3 Activation Energies for Primary Failure Mechanisms

Failure Mechanism	Ea
Contamination	1-1.4 eV
Silicon Defects	0.5 eV
Polarization	1 eV
Oxide Breakdown	0.3 eV
Aluminum Migration	0.5 eV
Trapping	1 eV



1.4 Definition and common test methods

Accelerated operating life stress
Accelerated operating life stressing is performed to accelerate failure mechanisms, which are thermally activated, through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications.

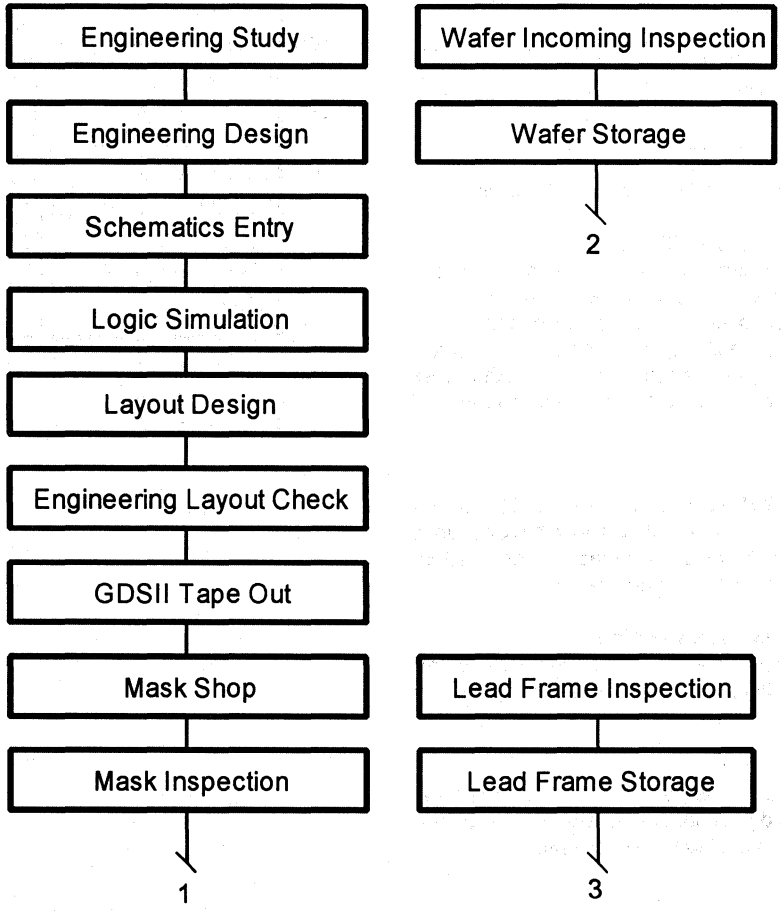
85 °C/ 85 % R.H.
85 °C/ 85 % R.H. is an environmental stress performed at a temperature of 85 °C and relative humidity of 85%. The test is designed to measure the moisture resistance of encapsulated devices.

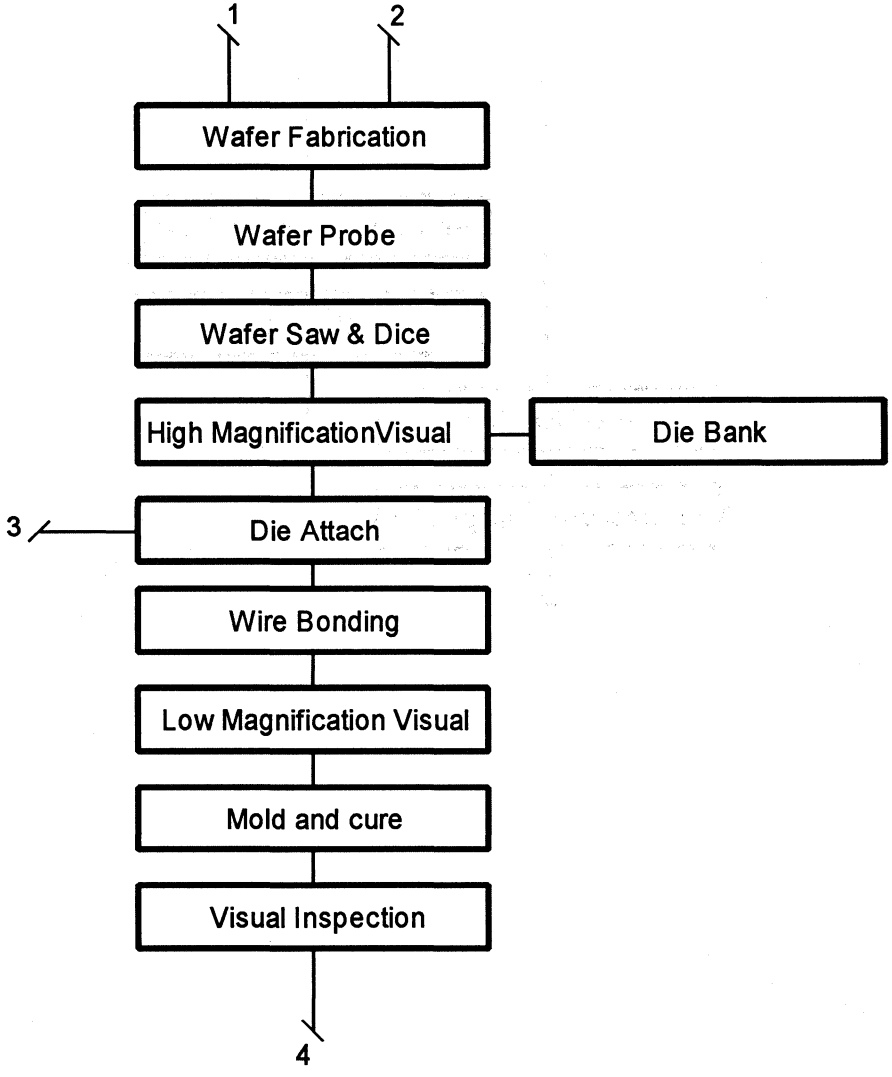
Electrostatic discharge testing
Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device.

CMOS latch-up test
CMOS latch-up test is performed to determine the sensitivity of a device input to overshoot and undershoot signals connected to device inputs.

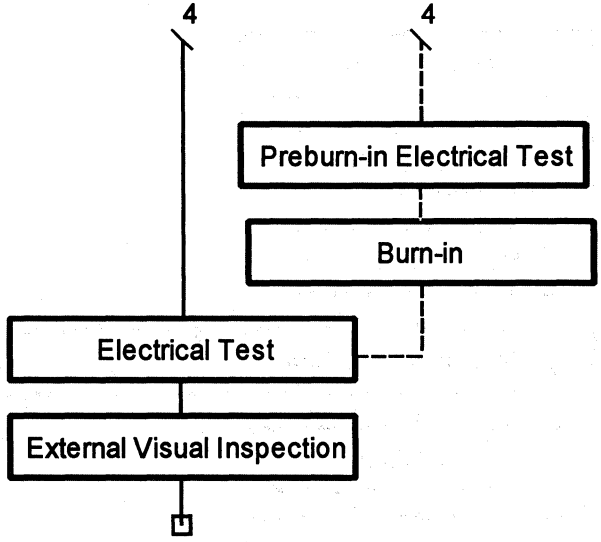
QUALITY / RELIABILITY

Commercial and Industrial Product Flows

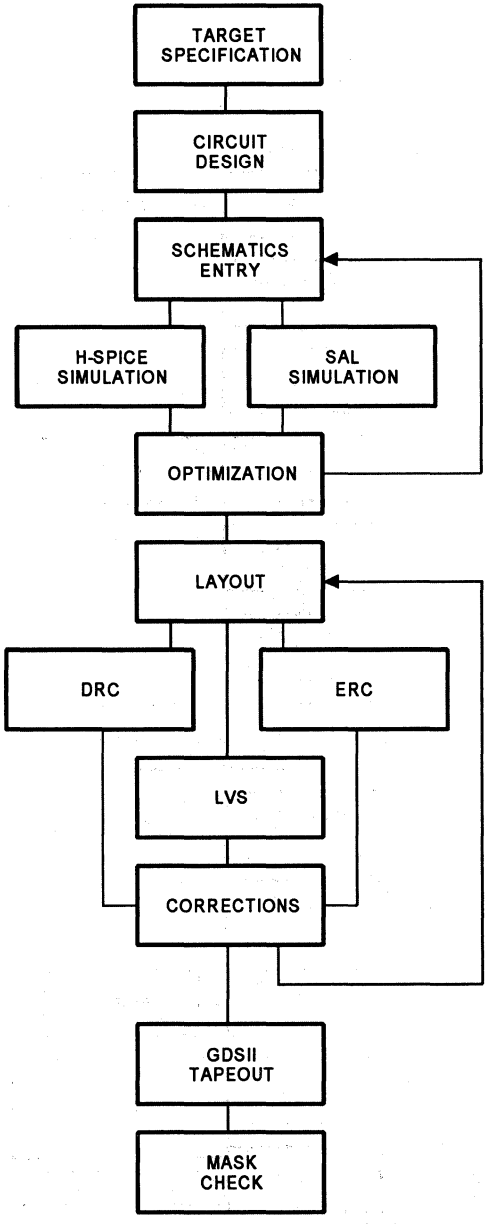



1
2
Wafer Fabrication
Wafer Probe
Wafer Saw & Dice
High MagnificationVisual
Die Bank
3
Die Attach
Wire Bonding
Low Magnification Visual
Mold and cure
Visual Inspection
4

QUALITY / RELIABILITY

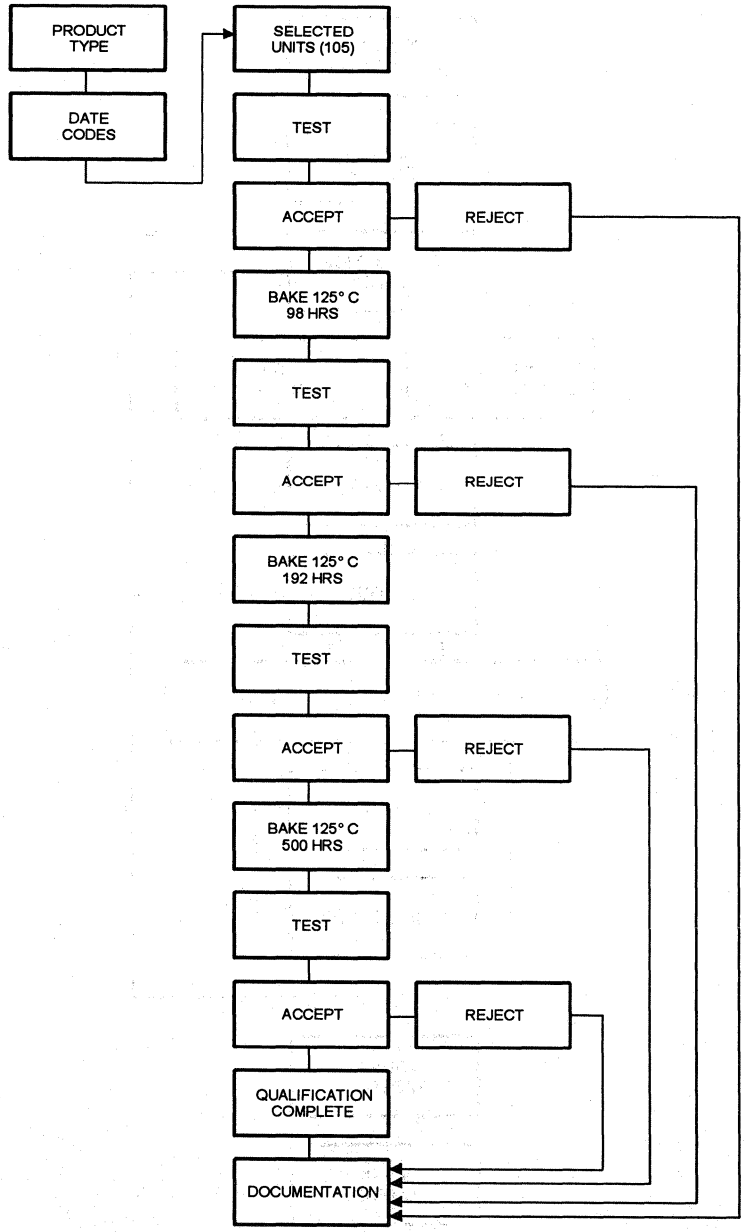


Design and Layout Flow

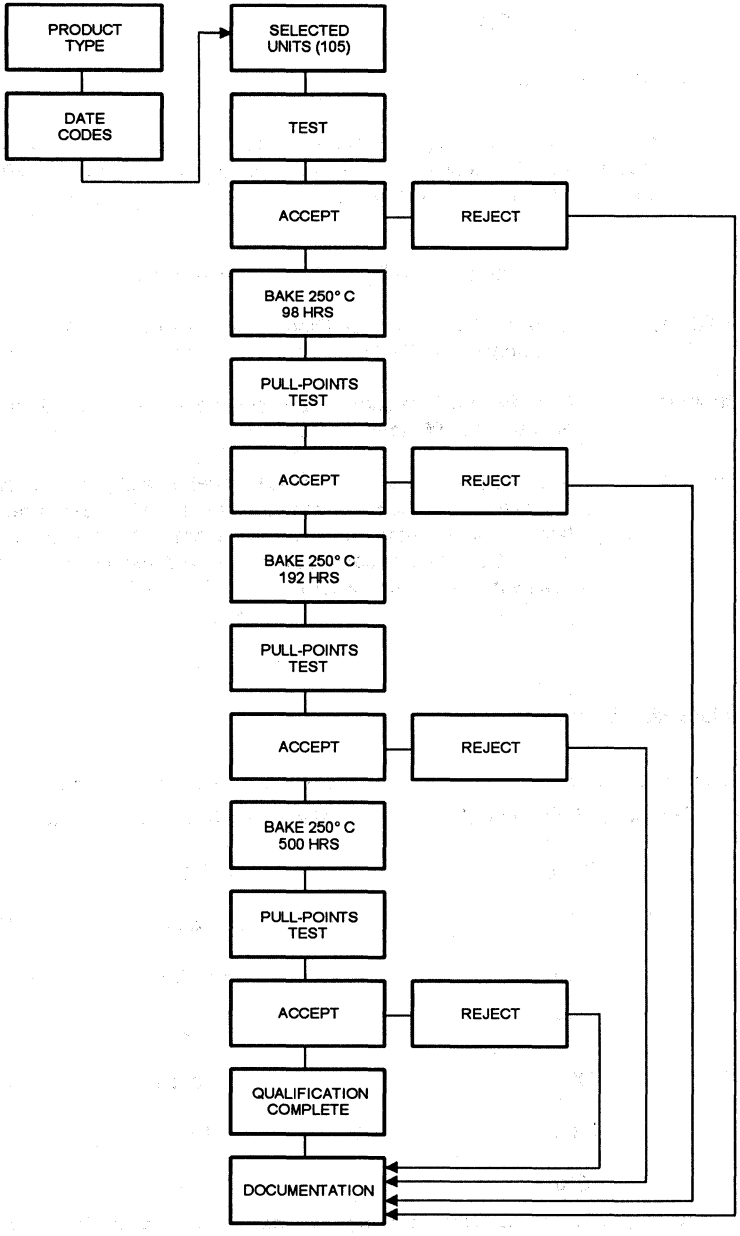


QUALITY / RELIABILITY

TEMPERATURE CYCLE FLOW



85 / 85 BIAS CYCLE FLOW



QUALITY / RELIABILITY

HIGH TEMPERATURE OPERATING LIFE

2.0 EARLY FAILURE RATE SUMMARY

2.1 Early Failure rate Determination

High temperature operating life testing for as log as 96 hours, is used to estimate device early failure rate. Using our standard failure rate assumption, the early failure rate period extends through the first 2000 hours of device operation. Afterwards, the device reliability is characterized by the long term failure rate.

Test:	High Temperature Operating Life Test (HTOL)
Conditions:	Dynamic Operating Conditions, Vcc = 5.25 Volts, 150 ° C or 125 ° C, Frequency = 2 MHz.
Duration:	Early Failure Rate samples are tested between 48 and 96 hours HTOL at 150 ° C or 96 hours at 125 ° C.
Failure:	A failure is any device that fails to meet data sheet electrical requirements following the HTOL test. Failure analysis is performed on every failure to identify the specific mechanism and determine a corrective action. Corrective actions are implemented and audited under the total quality management system.

2.2 Early Failure Rate Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450	1000	0	None	0
ST16C550	1500	2	Leakage	1333
ST16C452	1500	1	Functional	666
ST16C552	2000	0	None	0
ST16C554	2000	1	Leakage	500
ST26C31	1000	0	None	0
ST26C32	1000	0	None	0

3.0 LONG TERM FAILURE RATE SUMMARY

3.1 Long Term Failure Rate Determination

A High temperature Operating Life test is used to estimate long term reliability. By operating the devices at accelerated temperature and voltage, hundreds of thousands of use hours can be compressed into thousands of test hours. The method used to estimate failure rates from stress data is summarized.

Test:	High Temperature Operating Life Test (HTOL)
Conditions:	Dynamic Operating Conditions, Vcc = 5.25 Volts, 150 ° C, Frequency = 2 MHz.
Duration:	Long term Failure Rate is minimum 168 hours HTOL at 150 ° C periodically tested to 2000 hours.
Reliability:	Failure mechanisms common to semiconductor components are accelerated by temperature and voltage. In calculating failure rates, though, only temperature acceleration is included.

3.2 Long term Failure Rate Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450	5000	1	Functional	200
ST16C550	8000	1	Leakage	125
ST16C452	7500	0	None	0
ST16C552	5000	0	None	0
ST16C554	7000	1	Functional	143
ST26C31	1000	0	None	0
ST26C32	1000	0	None	0

QUALITY / RELIABILITY

4.0 HIGH TEMPERATURE STEADY STATE LIFE TEST

The High Temperature Steady State Life test is used to accelerated ionic contamination problems. Static bias is used because a constant voltage gradient accelerated diffusion of ionic species. The method used to estimate failure rates from stress data is summarized.

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450	3000	1	Functional	333
ST16C550	3000	0	None	0
ST16C452	4500	1	Functional	222
ST16C552	1000	0	None	0
ST16C554	1000	0	None	0
ST26C31	1000	0	None	0
ST26C32	1000	0	None	0

5.0 PACKAGE STRESS TESTS

Startech Semiconductor Reliability qualifies and continuously monitors the packaging reliability to ensure exceptional resistance to environmental stress. Package reliability stress testing and failure rates are summarized.

5.1 Pressure Cooker Test

Test:	Pressure Cooker Test (PCT)
Conditions:	15 PSIG, 120 ° C, No bias, 295 hours minimum time
Purpose:	The Pressure Cooker Test is a highly accelerated packaging stress test used to ensure environmental durability of epoxy packaged parts. Passivation cracks, ionic contamination and corrosion susceptibility are all accelerated by this stress.
Failure:	Any device which fails to meet all data sheet requirements is classified as a failure.

5.2 Pressure Cooker Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450CP40	5000	1	Functional	200
ST16C450CJ44	5000	0	None	0
ST16C550CP40	5000	0	None	0
ST16C550CJ44	5000	1	Leakage	200
ST16C452CP68	5000	1	Functional	200
ST16C552CP68	5000	1	Functional	200
ST16C554CP68	5000	0	None	0
ST26C31CP16	1000	0	None	0
ST26C32CP16	1000	0	None	0

5.2 Highly Accelerated Stress Test

Test: High Accelerated Stress Test (HAST)

Conditions: 18.6 PSIG, 125 ° C, 85% RH, 5.5 Volts bias, minimum test time, 96 hours.

Purpose: HAST is an accelerated biased humidity test that literature, and tests run at Startech, has shown provides an acceleration 10-15X over 85 ° C/ 85%. This test provides the factory with rapid feedback regarding the quality of the epoxy package process.

Failure: A failure is defined as a device which fails to pass the standard data sheet test program.

QUALITY / RELIABILITY

5.4 Accelerated Stress Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450CP40	5000	0	None	0
ST16C450CJ44	5000	0	None	0
ST16C550CP40	5000	0	None	0
ST16C550CJ44	5000	0	None	0
ST16C452CP68	5000	0	None	0
ST16C552CP68	5000	0	None	0
ST16C554CP68	5000	0	None	0
ST26C31CP16	1000	0	None	0
ST26C32CP16	1000	0	None	0

5.5 Temperature Cycle Test

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes. If the materials do not expand and contact equally, large stresses can develop.

Test:	Temperature Cycle
Conditions:	MIL-STD-883C, Method test stress mechanical integrity by exposing a device to alternating temperature extremes. Weakness and thermal expansion mismatches in die interconnections, die attach, and wire bonds are often detected with this acceleration test.
Purpose:	100 cycles minimum, periodically tested to 1000 cycles
Failure:	Any device which fails to meet all data sheet requirements is classified as a failure.

5.6 Temperature Cycle Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450CP40	5000	0	None	0
ST16C450CJ44	5000	0	None	0
ST16C550CP40	5000	0	None	0
ST16C550CJ44	5000	2	Leakage Functional	400
ST16C452CP68	5000	0	None	0
ST16C552CP68	5000	0	None	0
ST16C554CP68	5000	0	None	0
ST26C31CP16	1000	0	None	0
ST26C32CP16	1000	0	None	0

QUALITY / RELIABILITY

ESD AND LATCH-UP TEST

6.0 Latch-up Sensitive

Test:	Latch-up Sensitivity
Conditions:	Current Injection = 200mA Trigger, Hot Socket = Vcc 0-7 Volts, Vcc Oscillation at Vcc = 3.5-7.0 Volts at 1 MHz, Temperature = 150 ° C.
Purpose:	The latch-up test is designed to test resistance of the devices to extreme voltage and current excursions. Latch-up has historically been a problem associated with CMOS devices.
Failure:	Any device which fails the Latch-up test if Latch-up occurs at less than 200mA of current.

6.1 Results:

All products are tested for latch-up during qualification.

Outputs:	All outputs are tested using a hot socket technique where the full voltage is applied instantly, on a voltage ramp, where voltage is increased slowly. During the hot socket technique, a maximum of 400 mA was allowed in order to protect the outputs from overstress.
Inputs:	All inputs are tested using both the hot socket technique and the voltage ramp technique.

6.2 Conclusion:

Startech Semiconductor products are very resistant to latch-up.

7.0 Electrostatic Discharge (ESD)

Test:	Electrostatic Discharge
Conditions:	MIL-STD-883C, Method 3015
Purpose:	The ESD test established the sensitive of device to electrostatic discharge of the type than can occur during ordinary handling.
Failure:	A device fails the ESD stress test is any pin combination defined in method 3015 of MIL-STD-883C is damaged after testing with a 2000 Volts discharge. Data sheet electrical testing is performed to determine if a device has been damaged.

7.1 Results:

All Startech Semiconductor products are tested for resistance to ESD during qualification. All pins pass ESD testing at 2000 Volts.

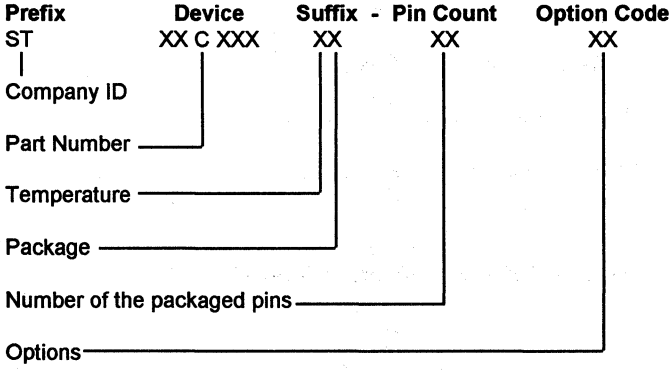
7.2 Conclusion:

Startech Semiconductor products are not ESD sensitive per the definition of MIL-STD-883C.

QUALITY / RELIABILITY

ORDERING INFORMATION 9

ORDERING INFORMATION AND PART NUMBERING GUIDE



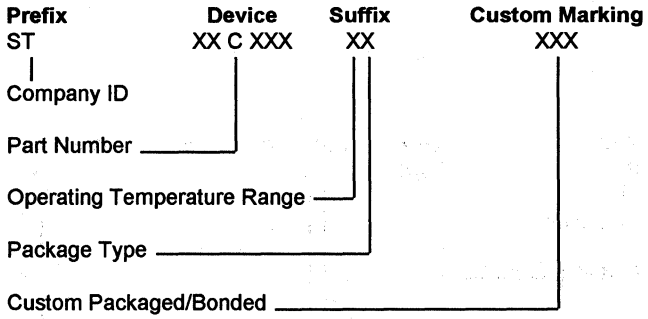
Temperature Range

C	Commercial	0° C	To	+70° C
I	Industrial	-40° C	To	+85° C
M	Military	-55° C	To	+125° C

Package Type

P Plastic Dip
C Ceramic
D Cerdip
L Leadless Chip Carrier (LCC)
J Plastic Leaded Chip Carrier (PLCC)
F Flat Pack(SOIC)
Q Quad Flat Pack
G Pin Grid
T Thin Shrink Small Outline Package (TSSOP)

PACKAGE MARKING INFORMATION (EXCEPT CLOCK SYNTHESIZERS AND TQFP PACKAGES)



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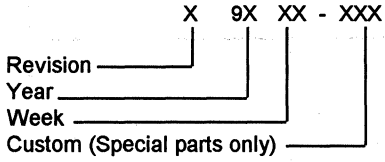

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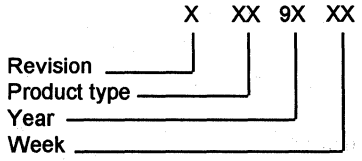
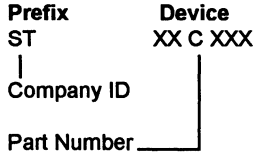


PACKAGE MARKING INFORMATION (CLOCK SYNTHESIZERS)



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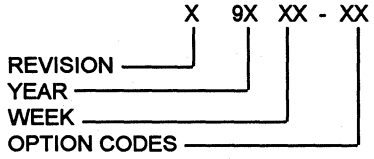
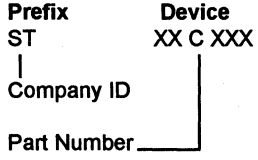


48-TQFP PACKAGE MARKING INFORMATION



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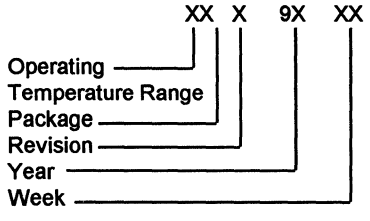
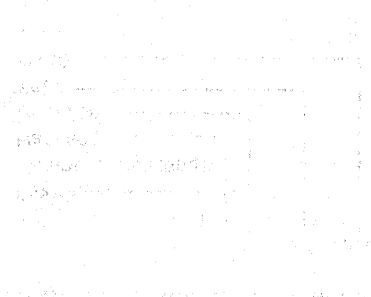
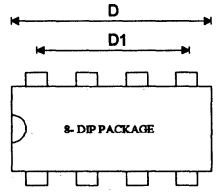
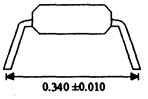
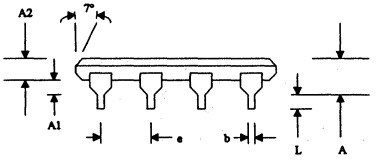




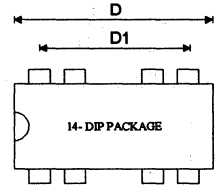
PACKAGING INFORMATION

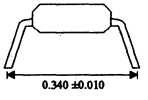


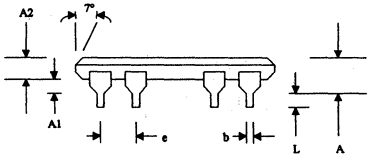




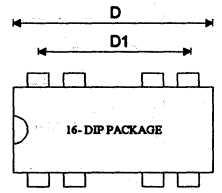
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	0.365 ±0.005
D1	0.300
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02

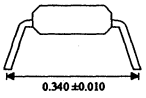


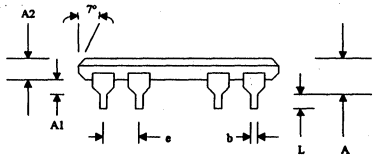




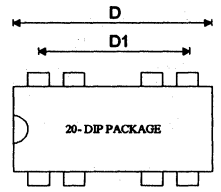
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	0.750 ±0.005
D1	0.600
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02

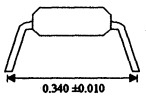


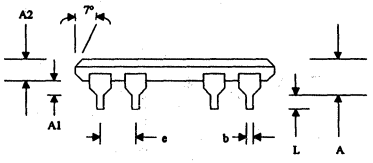




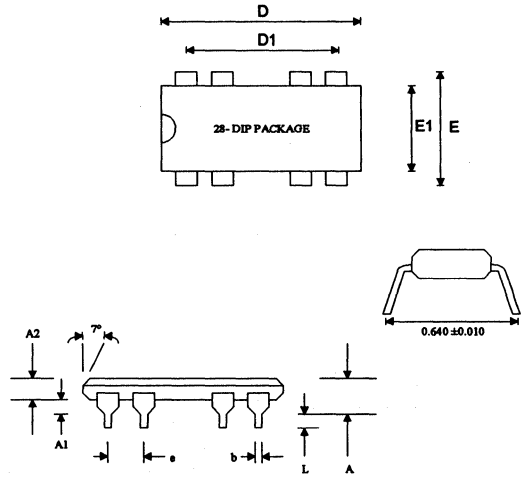
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	0.750 ±0.005
D1	0.700
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



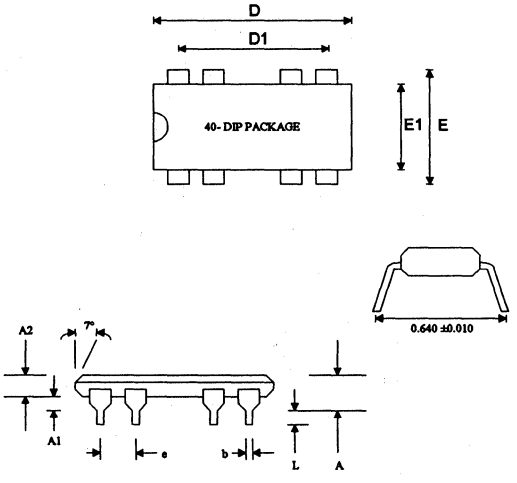




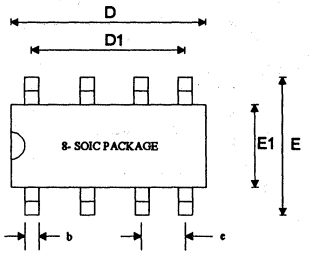
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.130 ±0.005
D	1.020 ±0.005
D1	0.900
E	0.310 ±0.010
E1	0.250 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02

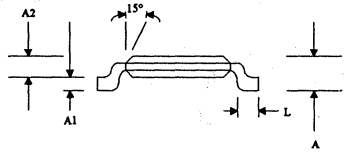


DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.150 ±0.005
D	1.450 ±0.005
D1	1.300
E	0.610 ±0.010
E1	0.550 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02

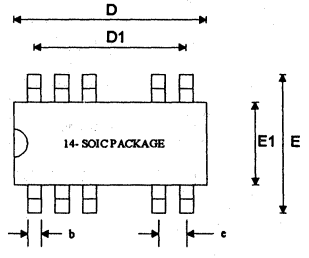


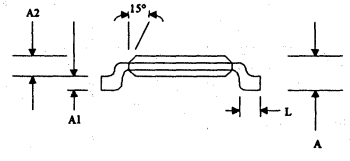
DIMENSIONS	TOLERANCE (Mil)
A	0.200 ±0.010
A1	0.015
A2	0.150 ±0.005
D	2.050 ±0.005
D1	1.900
E	0.610 ±0.010
E1	0.550 ±0.005
L	0.125 ±0.020
e	0.100
b	0.17 ±0.02



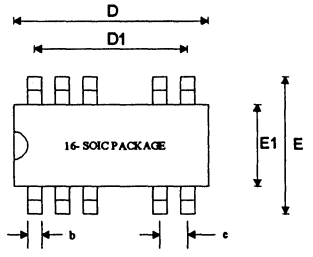


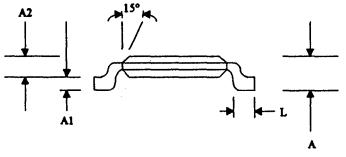
DIMENSIONS	TOLERANCE (Mil)
A	0.061 ±0.004
A1	0.004 ~ 0.010
A2	0.054 ±0.002
D	0.193 ±0.002
D1	0.150
E	0.236 ±0.008
E1	0.154 ±0.002
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



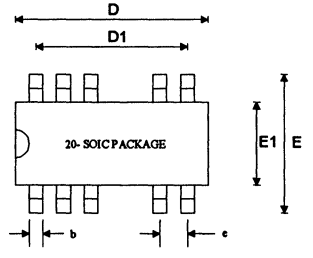


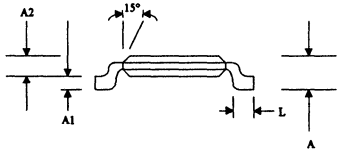
DIMENSIONS	TOLERANCE (Mil)
A	0.061 ±0.004
A1	0.004 ~ 0.010
A2	0.054 ±0.002
D	0.340 ±0.002
D1	0.300
E	0.236 ±0.008
E1	0.154 ±0.002
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



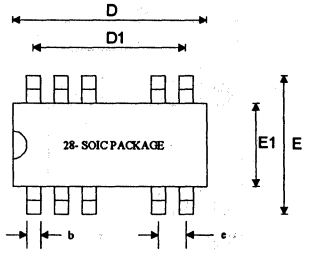


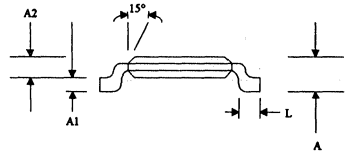
DIMENSIONS	TOLERANCE (Mil)
A	0.061 ±0.004
A1	0.004 ~ 0.010
A2	0.054 ±0.002
D	0.390 ±0.002
D1	0.350
E	0.236 ±0.008
E1	0.154 ±0.002
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



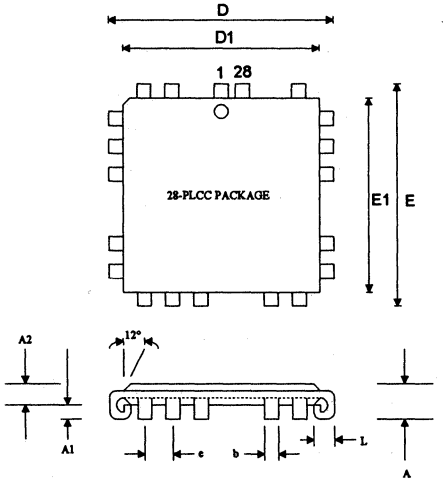


DIMENSIONS	TOLERANCE (Mil)
A	0.101 ±0.010
A1	0.006 ~ 0.008
A2	0.092 ±0.005
D	0.504 ±0.005
D1	0.450
E	0.406 ±0.010
E1	0.289 ±0.005
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02

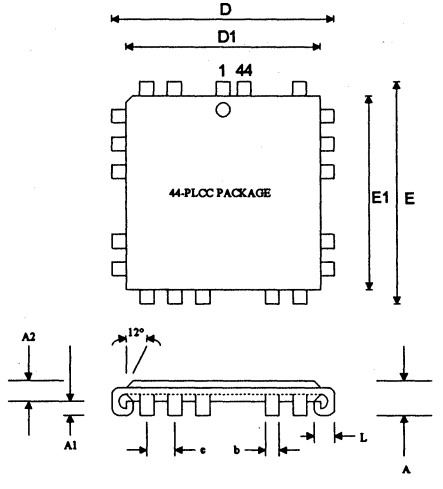




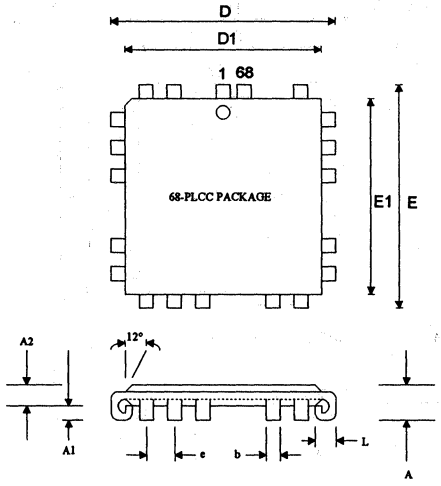
DIMENSIONS	TOLERANCE (Mil)
A	0.101 ±0.010
A1	0.006 – 0.008
A2	0.092 ±0.005
D	0.704 ±0.005
D1	0.650
E	0.406 ±0.010
E1	0.289 ±0.005
L	0.020 ±0.020
e	0.050
b	0.17 ±0.02



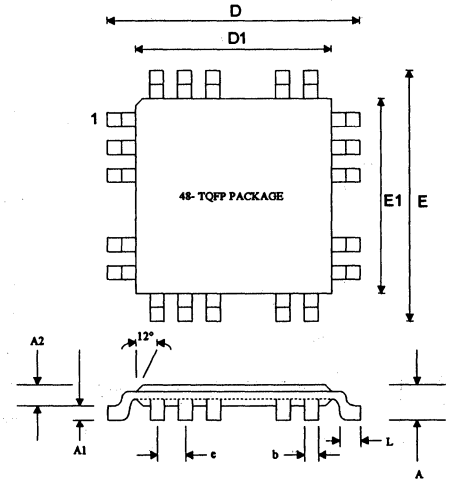
DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.05 - 0.10
A2	1.0 ±0.5
D	9.0 ±0.25
D1	7.0 ±0.10
E	9.00 ±0.25
E1	7.0 ±0.10
L	0.6 ±0.15
e	0.5
b	0.22 +0.05



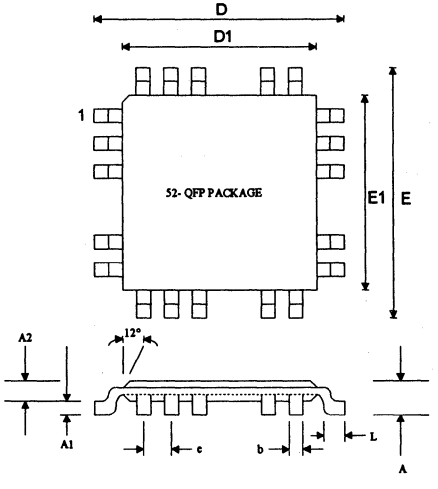
DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.05 - 0.10
A2	1.0 ±0.5
D	9.0 ±0.25
D1	7.0 ±0.10
E	9.00 ±0.25
E1	7.0 ±0.10
L	0.6 ±0.15
e	0.5
b	0.22 +0.05



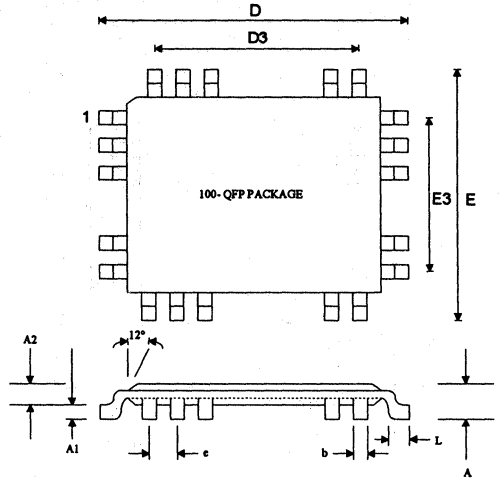
DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.05 - 0.10
A2	1.0 ±0.5
D	9.0 ±0.25
D1	7.0 ±0.10
E	9.00 ±0.25
E1	7.0 ±0.10
L	0.6 ±0.15
e	0.5
b	0.22 +0.05



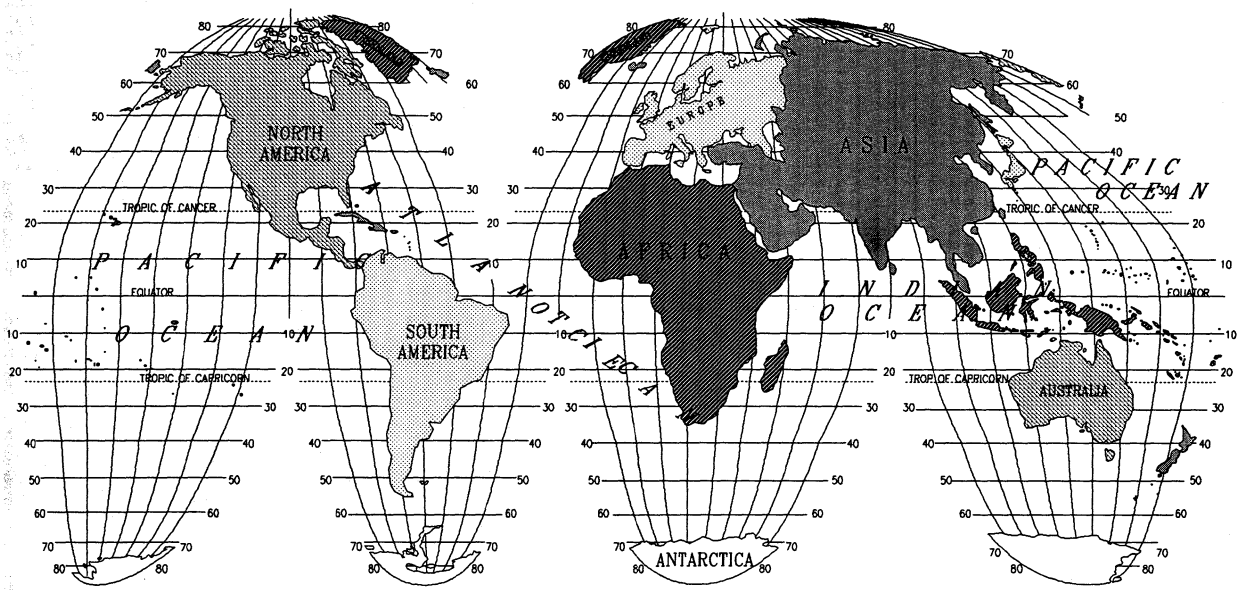
DIMENSIONS	TOLERANCE (mm)
A	1.20
A1	0.05 - 0.10
A2	1.0 ±0.5
D	9.0 ±0.25
D1	7.0 ±0.10
E	9.00 ±0.25
E1	7.0 ±0.10
L	0.6 ±0.15
e	0.5
b	0.22 +0.05



DIMENSIONS	TOLERANCE (mm)
A	2.26 ±0.13
A1	0.23 ±0.07
A2	2.03 ±0.06
D	14.1 ±0.20
D1	10 ±0.10
E	14.1 ±0.20
E1	10 ±0.10
L	0.88 ±0.15
e	0.65
b	0.30 ±0.08



DIMENSIONS	TOLERANCE (mm)
A	3.04 ±0.30
A1	0.30 -0.03
A2	2.71 ±0.16
D	23.20 ±0.25
D3	18.85
E	17.20 ±0.25
E3	12.35
L	0.65 ~ 0.95
e	0.65
b	0.22 ~ 0.38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