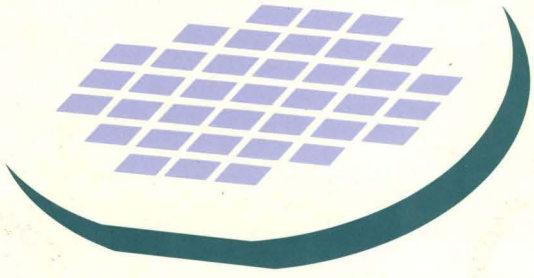


STARTECH

SEMICONDUCTOR, INC.

DATA BOOK

STARTECH

Component Data

Catalog

1992

STARTECH Semiconductor Inc.
1219 BORDEAUX Dr. SUNNYVALE, CA 94089
TEL (408) 745-0801 FAX (408) 745-1269

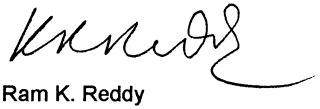
President's Message

To Our Valued Customer:

Startech Semiconductor was founded in 1990, with the charter to design, manufacture and market high performance data communication peripheral products in both the commercial and industrial semiconductor markets. Since then, Startech continues to follow that charter and enjoys a rapid growth.

Startech's products are marketed and distributed through a world-class network of representatives and distributors.

At Startech, we are dedicated to keeping your designs competitive with leading edge solutions. All our products are low power, high performance, CMOS ICs. Our commitment to you is to provide you with high quality and reliable ICs.



Ram K. Reddy
President

Introduction

Dear Customer,

Startech Semiconductor is proud to present you with our updated 1992 Data Book. Startech's technical staff have worked together to provide you with the most accurate, up-to-date information.

We believe that when you design our products in your systems, you have started a partnership with a company that is committed to work with the customers and deliver quality products. Startech offers to customize any of these standard products to meet your special requirements.

If you have any questions or comments, please call us directly.

Art Khachaturian
Vice President

Contents

CROSS REFERENCE LIST

DIFFERENTIAL LINE DRIVERS

National Semiconductor	Startech Semiconductor
DS26C31C	ST26C31
DS34C86	ST34C86

DIFFERENTIAL LINE RECEIVERS

National Semiconductor	Startech Semiconductor
DS26C32C	ST26C32
DS34C37	ST34C87

DIFFERENTIAL LINE RECEIVERS / DRIVERS

Motorola Semiconductor	Startech Semiconductor
MC34050	ST34C50
MC34051	ST34C51

UARTS

National Semiconductor	Startech Semiconductor
INS8250A	ST16C450
INS82C50A	ST16C450
NS16450	ST16C450
NS16C450	ST16C450
NS16550AF	ST16C550

Silicon Systems	Startech Semiconductor
SSI73M550	ST16C550
SSI73M1550	ST16C1450 / ST16C1550
SSI73M2550	ST16C1451 / ST16C1551

VLSI Technology, Inc.	Startech Semiconductor
VL82C50A	ST16C450
VL16C450	ST16C450
VL16C550	ST16C550

Western Digital Inc.	Startech Semiconductor
WD16C450	ST16C450
WD16C550	ST16C550

Texas Instruments	Startech Semiconductor
TL16C450	ST16C450
TL16C550A	ST16C550

Exar Corporation	Startech Semiconductor
XR16C450	ST16C450
XR16C550	ST16C550

CROSS REFERENCE LIST

UARTS WITH PRINTER

VLSI Technology, Inc.	Startech Semiconductor
VL16C452	ST16C452
VL16C552	ST16C552 / ST16C553
Western Digital Inc.	Startech Semiconductor
WD16C452	ST16C452
WD16C552	ST16C552 / ST16C553
Texas Instruments	Startech Semiconductor
TL16C452	ST16C452
TL16C552	ST16C552
Exar Corporation	Startech Semiconductor
XR16C452	ST16C452
XR16C552	ST16C552

VIDEO DOT CLOCK GENERATOR

Integrated Circuit Systems, Inc.	Startech Semiconductor
ICS1394XXX	ST49C394-XX
ICS2494XXX	ST49C214-XX
ICS90C61AXXX	ST49C061-XX
Avasem Corporation	Startech Semiconductor
AV9103-XX	ST49C103-XX
AV9104-XX	ST49C104-XX / ST49C114-XX

FREQUENCY SYNTHESIZERS

1

Index

STARTECH

ST49C061

APR 1992

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

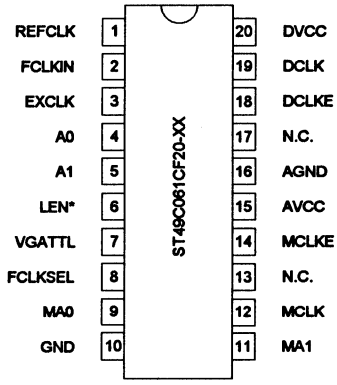
GENERAL DESCRIPTION

The ST49C061 is a monolithic analog CMOS device designed to generate dual frequency outputs from seven possible combinations for video Dot clock frequencies and four memory clock frequencies for high performance video display systems. The ST49C061 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2µ process to achieve 130 MHz speed for high end frequencies.

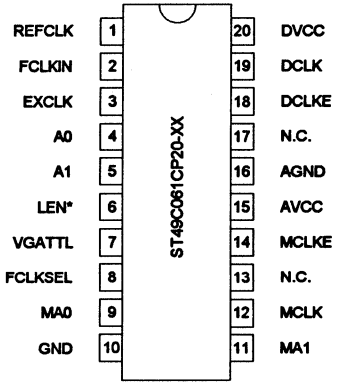
The ST49C061 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C061 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device).

The ST49C061 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and two address lines for memory clock selection.

SOIC Package



Plastic-DIP Package



FEATURES

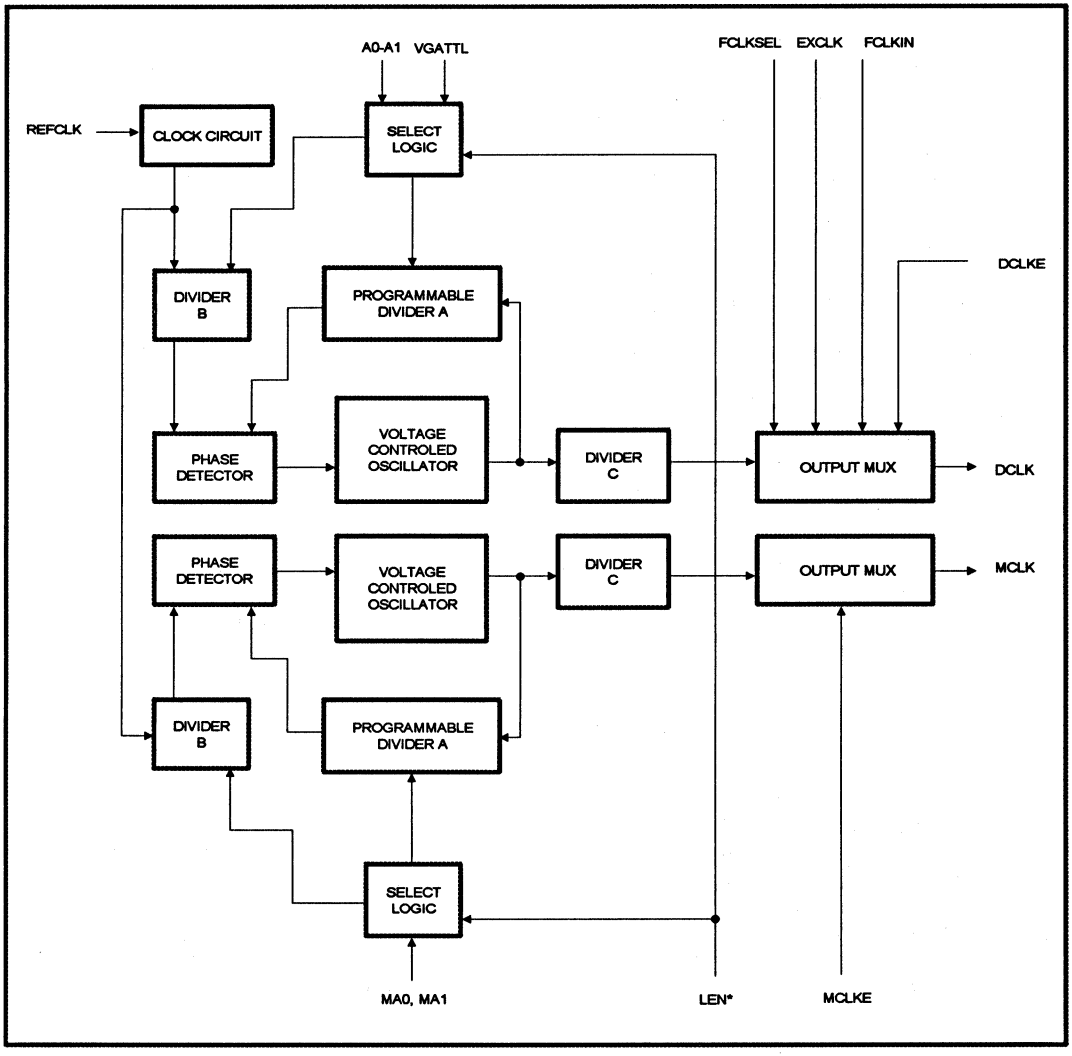
* Can replace multiple oscillators/crystals
* Pin -to-pin compatible to ICS90C61A
* Programmable analog phase locked loop
* High speed (up to 130 MHz output)
* Low power single 5V CMOS technology
* 20 pin dip or SOIC package
* Compatible with Western Digital Imaging Video Graphics Array clock requirements.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C061CP20-xx	Plastic-DIP	0° C to +70° C
ST49C061CF20-xx	SOIC	0° C to +70° C
ST49C061CJ20-xx	PLCC	0° C to +70° C

ST49C061

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
REFCLK	1	I	External 14.318 MHz system reference clock input.
FCLKIN	2	I	Feature clock input.
EXCLK	3	I	External clock input. For additional clock frequency.
A0	4	I	Dot clock Frequency select address 1.
A1	5	I	Dot clock Frequency select address 2.
LEN*	6	I	Address latch enable input (active low). To latch selected programmed clock output.
VGATTL	7	I	Control input for DCLK selection.
FCLKSEL	8	I	Control input for FCLK selection.
MA0	9	I	Memory clock Frequency select address 1.
DGND	10	O	Digital ground.
MA1	11	I	Memory clock Frequency select address 2.
MCLK	12	O	Programmed memory clock output frequency.
N.C.	13		No connect.
MCLKE	14	I	MCLK output enable.
AVCC	15	I	Analog supply voltage. Single +5 volts.
AGND	16	O	Analog ground.
N.C.	17		No connect.
DCLKE	18	I	DCLK output enable.
DCLK	19	O	Programmed video clock output frequency.
DVCC	20	I	Digital supply voltage. Single +5 volts.

ST49C061

GENERAL INFORMATION

The Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. The VGA controller has capability to change two of its clock inputs VCLK1 and VCLK2 to outputs when working with a clock chip. These outputs are used to select the required video frequency.

The ST49C061 is programmed to generate different video clock frequencies using the inputs of A0 and A1. The VGATTL selects one of the two preprogrammed registers to provide four of eight clock frequencies.

The EXCLK and FCLKIN are additional inputs that may be internally connected to the DCLK output. The additional inputs are useful for supporting modes that require frequencies not provided by the ST49C061.

FREQUENCY SELECT CALCULATION

The ST49C061 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.
The accuracy of the frequencies produced by the ST49C061 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

DCLK = (Reference clock) X (A/B.C)
MCLK = (Reference clock) X (A/B.C)

where A=1,2,3,.....127,
B=1,2,3,.....127, and
C=1,2,4

For proper output frequency, the ST49C061 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask options are provided for custom applications.

* Any frequency can be in any decoding position.
* DCLK, can control selection of the internal frequencies.

					ST49C061-01	ST49C061-02
Video clock address (Hex)	FCLKSEL	VGATTL	A1	A0	Frequency (MHz)	Frequency (MHz)
0	1	0	0	0	REFCLK	REFCLK
1	1	0	1	0	16.256	16.108
2	1	0	0	1	32.000	32.216
3	1	0	1	1	44.900	44.744
0	1	1	0	0	25.175	25.057
1	1	1	1	0	28.322	28.089
2	1	1	0	1	65.000	EXTCLK
3	1	1	1	1	36.000	36.242
X	0	X	X	X	FCLKIN**	FCLKIN**
Memory clock address (Hex)			MA1	MA0	Frequency (MHz)	Frequency (MHz)
0			0	0	40.000	41.612
1			0	1	37.500	37.585
2			1	0	36.000	36.242
3			1	1	44.900	44.744
Compatible with Video Controller					ICS-PR1	ICS-PR2 WD90C30

** Note: FCLKIN and EXCLK may be programmed to output custom frequencies.

ST49C061

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time			4	ns	
T_5	Fall time			4	ns	
T_6	Duty cycle	40	48/52	60	%	
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

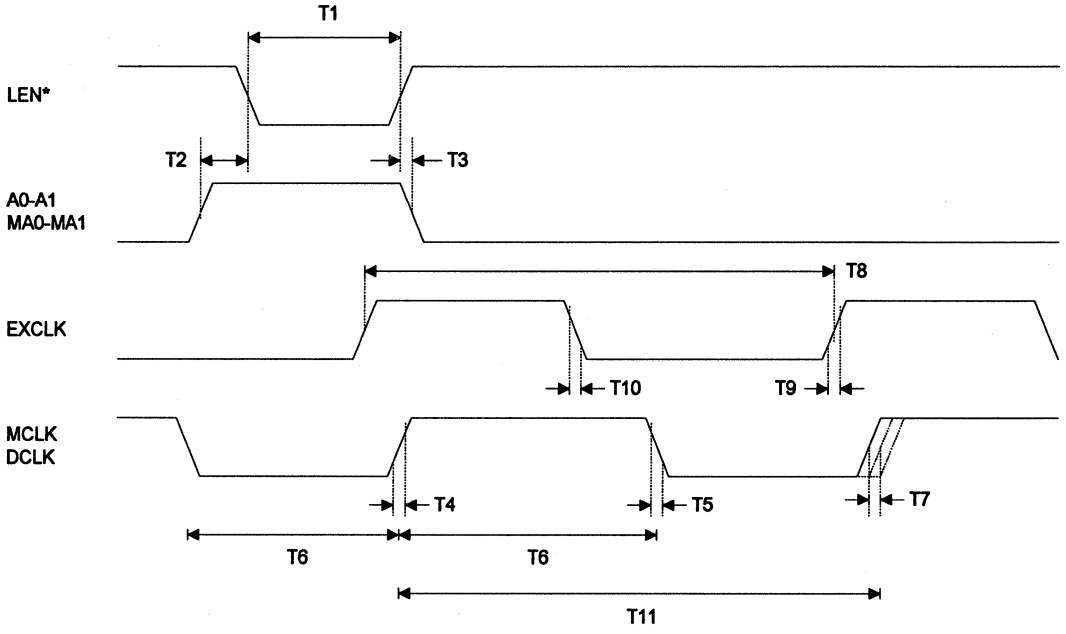
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	
V_{OH}	Output high level	2.4			V	
I_{IL}	Input low current			-5	µA	
I_{IH}	Input high current			5	µA	
I_{CC}	Operating current		10		mA	No load.

ST49C061

TIMING DIAGRAM



STARTECH

ST49C103/104/114

APR 1992

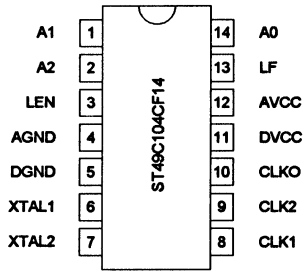
PREPROGRAMMED FREQUENCY GENERATOR

DESCRIPTION

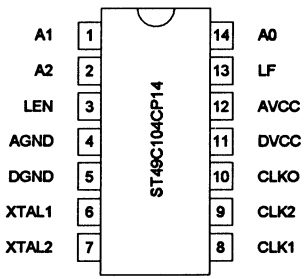
The ST49C103 and ST49C104 are mask programmable monolithic analog CMOS devices designed to generate up to 8 single frequency outputs from a single input clock. The ST49C104 will provide eight different output frequencies and the ST49C103 will provide four different output frequencies. They are designed in a 1.2µ process to achieve 130 MHz speed for high end frequencies.

The ST49C103 and ST49C104 are designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C104 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The latch enable pin is also mask programmable to be active high, active low or rising or falling edge sensitive.

SOIC Package



Plastic-DIP package



FEATURES

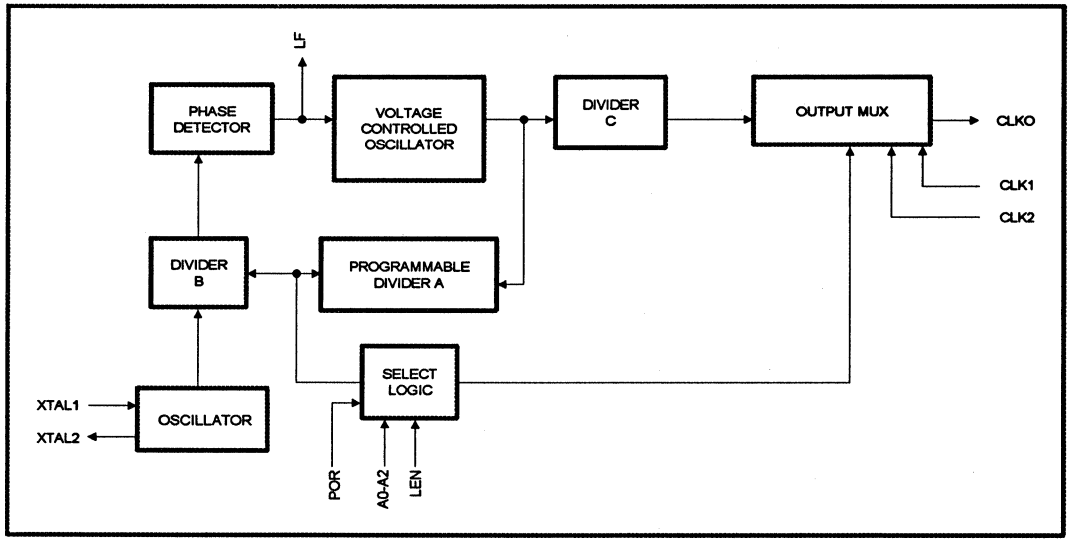
* Can replace up to 8 oscillators/crystals and a multiplexer
* Pin-to-pin compatible to Avasem AV9104/AV9103
* Programmable analog phase locked loop
* Low power single 5V CMOS technology
* 8 or 14 pin DIP or SOIC package.

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C103CP8	Plastic-DIP	0° C to +70° C
ST49C103CF8	SOIC	0° C to +70° C
ST49C104CP8	Plastic-DIP	0° C to +70° C
ST49C104CF8	SOIC	0° C to +70° C
ST49C104CP14	Plastic-DIP	0 ° C to +70° C
ST49C104CF14	SOIC	0° C to +70° C
ST49C114CP14	Plastic-DIP	0° C to +70° C
ST49C114CF14	SOIC	0° C to +70° C

ST49C103/104/114

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C104 14 pin package)

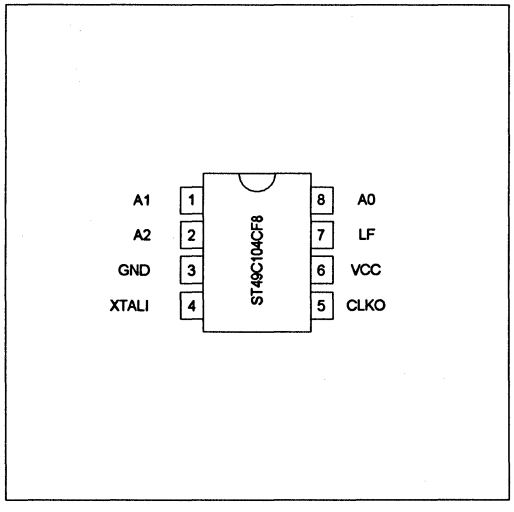
Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2	I	Frequency select address input 3.
LEN	3	I	Address latch enable input. To latch selected programmed clock output.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
XTAL1	6	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	O	Crystal output.
CLK1	8	I	External clock 1 input.
CLK2	9	I	External clock 2 input / output select.
CLKO	10	O	Programmed output clock.
DVCC	11	I	Digital supply voltage. Single +5 volts.
AVCC	12	I	Analog supply voltage. Single +5 volts.
LF	13	O	Loop filter.
A0	14	I	Frequency select address input 1.

ST49C114/ST49C104 have same pin out, except ST49C114 has higher output drive level.

ST49C103/104/114

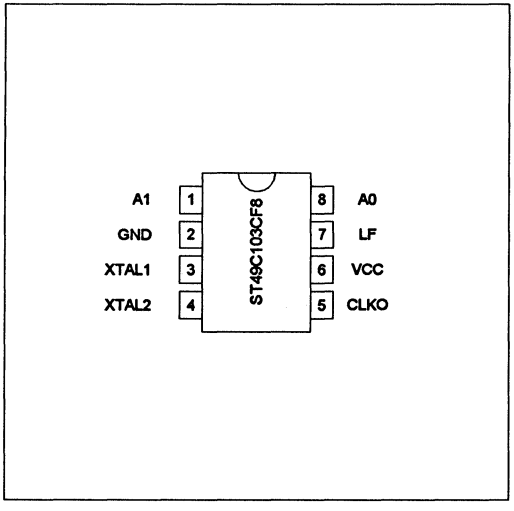
SYMBOL DESCRIPTION (ST49C104 8 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2	I	Frequency select address input 3.
GND	3	O	Digital ground.
XTAL1	4	I	External clock input. Internal phase locked loop reference clock .
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
LF	7	O	Loop filter.
A0	8	I	Frequency select address input 1.



SYMBOL DESCRIPTION (ST49C103 8pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
GND	2	O	Digital ground.
XTAL1	3	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
LF	7	O	Loop filter.
A0	8	I	Frequency select address input 1.



ST49C103/104/114

FREQUENCY SELECT CALCULATION

The ST49C104 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C104 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B.C)

where A=1,2,3,.....127
B=8, 16, 32 ,64
C=1,2,4,8

For proper output frequency, the ST49C104 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

The following mask options are provided for custom applications.

* Latch Enable can be edge triggered or level sensitive.
* Latch Enable can be active high or active low.
* Any frequency can be in any decoding position.
* CLK 1 and CLK 2 can be included in decoding table.
* CLK2 can control selection of either CLK 1 or the internal frequencies.

MASK OPTIONS

FEATURE	ST49C104 14-pin	ST49C104 8-pin	ST49C103 8-pin
8 output frequencies	X	X	
4 output frequencies			X
Programmable LEN pin	X	X	X
Clock input only		X	
Crystal or clock input	X		X
CLK1, CLK2 available for output mux	X		

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time			4	ns	
T_5	Fall time			4	ns	
T_6	Duty cycle	40	48/52	60	%	
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

Input clock frequency = 14.318 MHz
* Input clock frequency = 16.0 MHz
** Input clock frequency = 8.0 MHz

A2 A1 A0	ST49C104-1 NOMINAL	ACTUAL	ST49C104-2 NOMINAL	ACTUAL	ST49C104-3 NOMINAL	ACTUAL	ST49C114-5* NOMINAL	ACTUAL	ST49C103** NORMAL	ACTUAL
00 0 Xtal	Xtal	25.175	25.280	50.350	50.560	39.000	39.0000	32.00	32.00	32.00
0 0 1	16.257	16.331	28.322	28.412	56.664	56.824	25.000	25.000	40.00	40.00
0 1 0	Clk2	Clk2	32.514	32.663	65.028	65.326	30.750	30.750	50.00	50.00
0 1 1	32.514	32.663	36.000	35.795	72.000	71.590	26.250	26.250	1.00	1.00
1 0 0	25.175	25.056	40.000	39.822	80.000	79.640	32.000	32.000	N/A	
1 0 1	28.322	28.412	44.900	44.744	89.800	89.488	25.250	25.250	N/A	
1 1 0	24.000	23.938	50.000	50.113	75.000	75.169	31.250	31.250	N/A	
1 1 1	40.000	39.822	65.000	65.326	108.00	108.280	37.500	37.500	N/A	

Address latch (LEN)	State
ST49C104-1	Transparent for LEN high
ST49C104-2	Transparent for LEN low
ST49C104-3	Transparent for LEN low

ST49C103/104/114

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

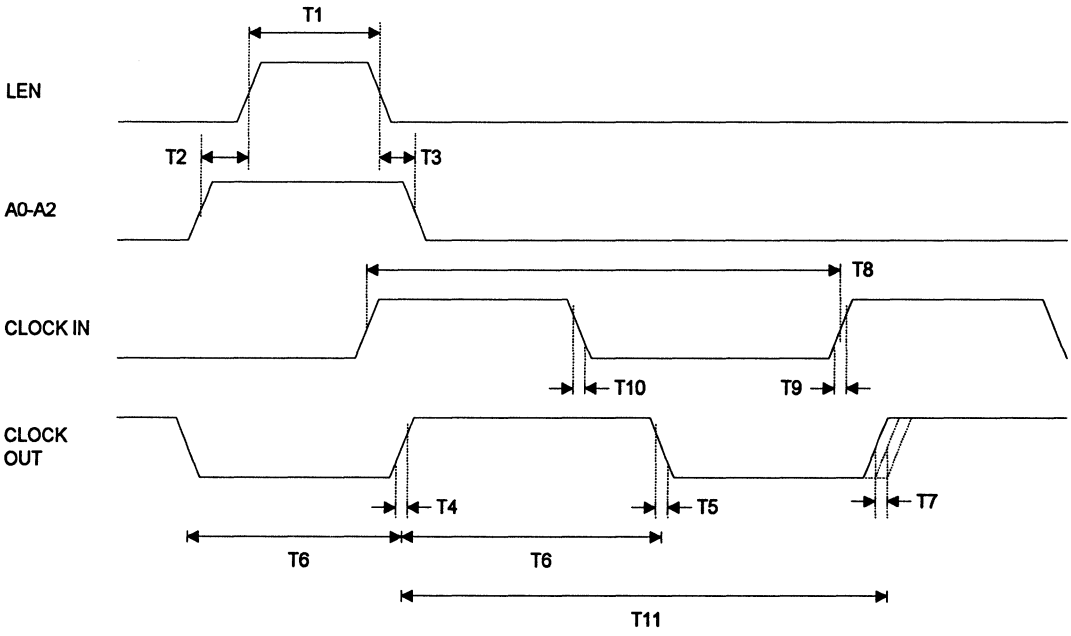
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	
V_{OH}	Output high level	2.4			V	
I_{IL}	Input low current			-5	µA	Except crystal input
I_{IH}	Input high current			5	µA	
I_{CC}	Operating current		10		mA	No load.

A2 A1 A0	ST49C114-6** NOMINAL	ACTUAL				
0 0 0	25.500	25.500				
0 0 1	16.500	16.500				
0 1 0	20.750	20.750				
0 1 1	22.500	22.500				
1 0 0	24.500	24.500				
1 0 1	19.500	19.500				
1 1 0	15.000	15.000				
1 1 1	14.000	14.000				

TIMING DIAGRAM



ST49C103/104/114

STARTECH

ST49C214

APR 1992

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

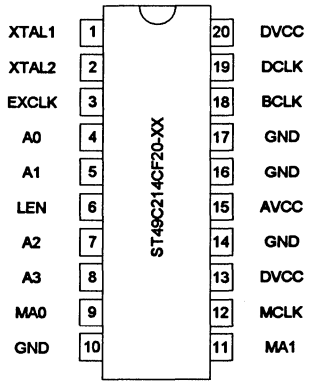
GENERAL DESCRIPTION

The ST49C214 is a monolithic analog CMOS device designed to generate dual frequency outputs from sixteen possible combinations for video Dot clock frequencies and four memory clock frequencies for high performance video display systems. The ST49C214 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2µ process to achieve 130 MHz speed for high end frequencies.

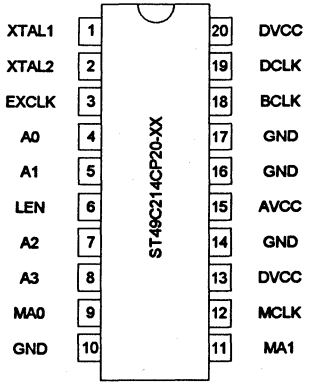
The ST49C214 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C214 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device) or external crystal connected between XTAL1 and XTAL2.

The ST49C214 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and two address lines for memory clock selection.

SOIC Package



Plastic-DIP Package



FEATURES

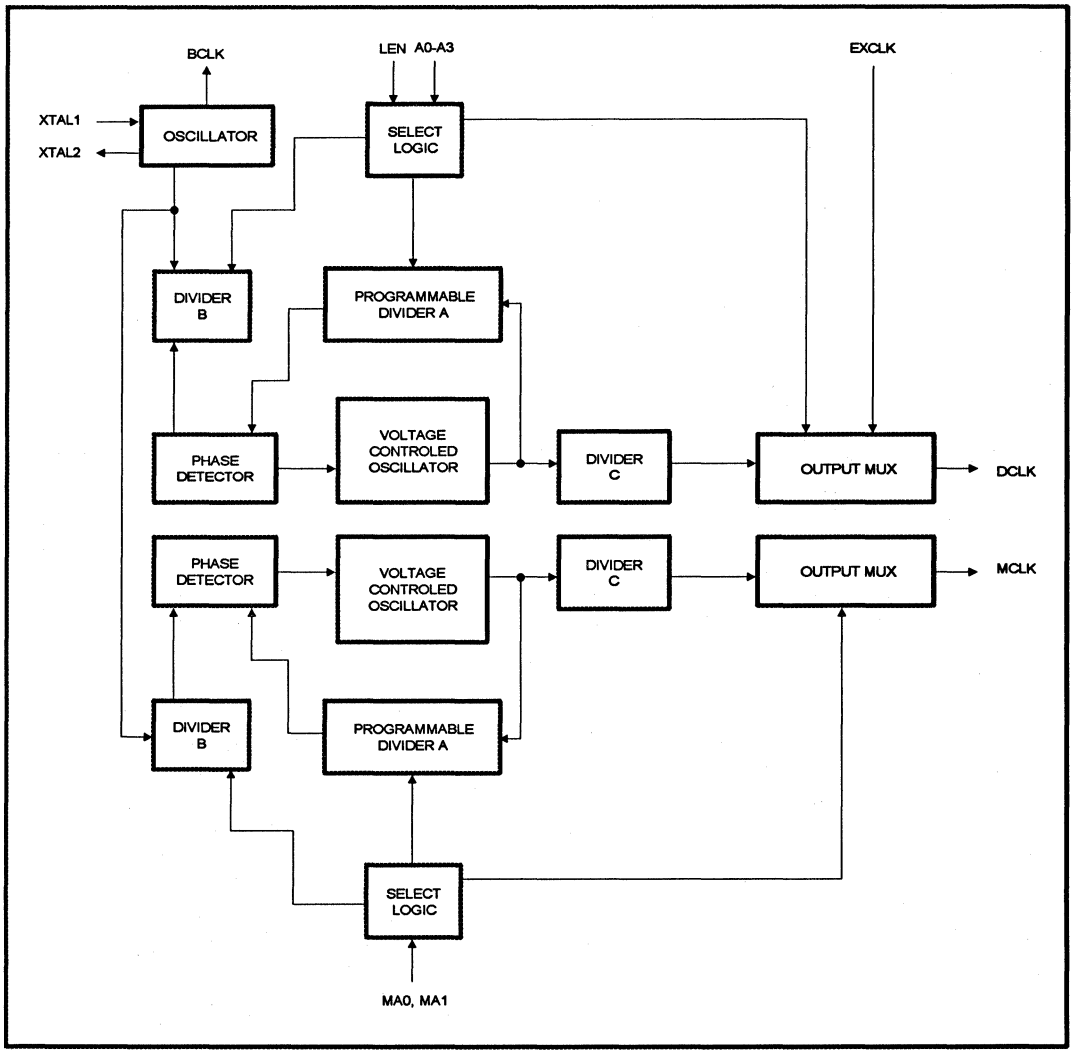
* Can replace multiple oscillators/crystals
* Pin -to-pin compatible to ICS2494
* Programmable analog phase locked loop
* High speed (up to 130 MHz output)
* Low power single 5V CMOS technology
* 20 pin dip or SOIC package

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C214CP20-xx	Plastic-DIP	0° C to +70° C
ST49C214CF20-xx	SOIC	0° C to +70° C
ST49C214CJ20-xx	PLCC	0° C to +70° C

ST49C214

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL1	1	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	2	O	Crystal output.
EXCLK	3	I	External clock input.
A0	4	I	Dot clock Frequency select address 1.
A1	5	I	Dot clock Frequency select address 2.
LEN	6	I	Address latch enable input (active high). To latch selected programmed clock output.
A2	7	I	Dot clock Frequency select address 3.
A3	8	I	Dot clock Frequency select address 4.
MA0	9	I	Memory clock Frequency select address 1.
GND	10	O	Digital and Analog ground.
MA1	11	I	Memory clock Frequency select address 2.
MCLK	12	O	Programmed memory clock output frequency.
DVCC	13	I	Digital supply voltage. Single +5 volts.
GND	14	O	Digital and Analog ground.
AVCC	15	I	Analog supply voltage. Single +5 volts.
GND	16	O	Digital and Analog ground.
GND	17	O	Digital and Analog ground.
BCLK	18	O	Buffered crystal clock output frequency.
DCLK	19	O	Programmed video clock output frequency.
DVCC	20	I	Digital supply voltage. Single +5 volts.

ST49C214

FREQUENCY SELECT CALCULATION

The ST49C214 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.
The accuracy of the frequencies produced by the ST49C214 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

XCLK = (Reference clock) X (A/B.C)

where A=1,2,3,.....127,
B=1,2,3,.....127, AND
C=1,2,4

For proper output frequency, the ST49C214 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask option are provided for custom applications.

* Any frequency can be in any decoding position.

Video clock address (Hex)	ST49C214-1 Frequency (MHz)	ST49C214-2 Frequency (MHz)	ST49C214-3 Frequency (MHz)	ST49C214-4 Frequency (MHz)	ST49C214-5 Frequency (MHz)
0	XTAL	30.000	25.175	20.000	50.350
1	65.028	77.250	28.325	24.000	56.644
2	EXCLK	EXCLK	85.000	32.000	65.000
3	36.000	80.000	44.900	40.000	72.000
4	25.175	31.500	40.000	50.000	80.000
5	28.322	36.000	48.000	66.667	89.800
6	24.000	75.000	50.000	80.000	63.000
7	40.000	50.000	81.150	100.000	75.000
8	44.900	40.000	25.175	54.000	25.175
9	50.350	50.000	28.325	70.000	28.322
A	16.257	32.000	37.500	90.000	31.500
B	32.514	44.900	44.900	110.000	36.000
C	56.644	25.175	40.000	25.000	40.000
D	20.000	28.322	32.500	33.333	44.900
E	41.539	65.000	50.000	40.000	50.000
F	80.000	36.000	65.000	50.000	65.000
Memory clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	36.000	36.000	16.000	40.000
1	35.600	44.347	40.000	24.000	41.612
2	43.900	37.500	45.000	50.000	44.744
3	49.100	44.773	50.000	66.667	50.000

Compatible with	ICS-236	ICS-242	ICS-231	ICS-244	ICS-237
Video Controller	GD6410	WD90C30	ET4000		ET4000

ST49C214

Video clock address (Hex)	ST49C214-6 Frequency (MHz)	ST49C214-8 Frequency (MHz)			
0	25.175	25.175			
1	28.322	28.322			
2	40.000	40.000			
3	65.000	32.500			
4	44.900	50.000			
5	50.000	65.000			
6	130.000	38.000			
7	75.000	44.900			
8	25.175	31.500			
9	28.322	36.000			
A	EXCLK	80.000			
B	EXCLK	63.000			
C	60.000	50.000			
D	80.000	100.000			
E	EXCLK	76.000			
F	EXCLK	110.000			
Memory clock address (Hex)	**Frequency (MHz)**	**Frequency (MHz)**			
0	32.900	70.000			
1	35.600	63.830			
2	43.900	60.000			
3	49.100	81.000			

Compatible with	**ICS-253**	
Video Controller	NCR22C22E	HT216

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time			4	ns	
T_5	Fall time			4	ns	
T_6	Duty cycle	40	48/52	60	%	
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

ST49C214

ABSOLUTE MAXIMUM RATINGS

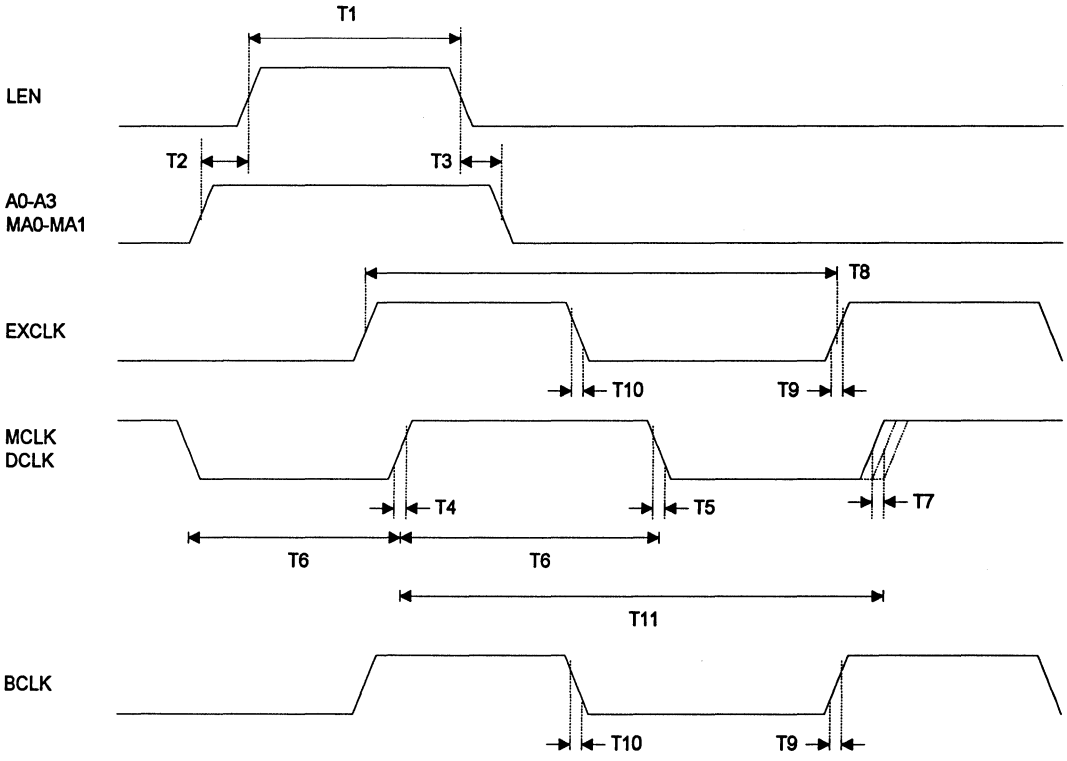
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	
V_{OH}	Output high level	2.4			V	
I_{IL}	Input low current			-5	µA	Except crystal input
I_{IH}	Input high current			5	µA	
I_{CC}	Operating current		10		mA	No load.

TIMING DIAGRAM



ST49C214

ST49C214

ST49C214- Frequency generator programming information

2. Please fill in the nominal frequencies required.

3. Crystal or input clock frequency _____

A3	A2	A1	A0	Nominal DCLKO	Actual DCLKO	
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			
		MA1	MA0	Nominal MCLKO	Actual MCLKO	
		0	0			
		0	1			
		1	0			
		1	1			

STARTECH

ST49C394

APR 1992

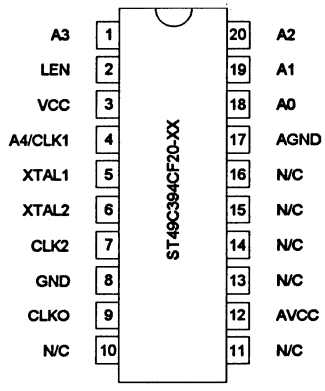
PREPROGRAMMED VIDEO DOT CLOCK FREQUENCY GENERATOR

GENERAL DESCRIPTION

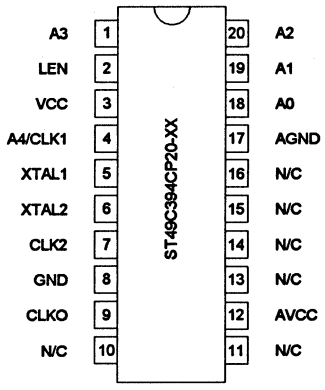
The ST49C394 is a monolithic analog CMOS device designed to generate dot clock frequency outputs from thirty two possible combinations in high performance video display systems. The ST49C394 is a mask programmable device that allows complete flexibility in frequency choice. It is designed in a 1.2µ process to achieve 135MHz speed for high end custom applications.

The ST49C394 is designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter, the ST49C394 utilizes a high speed analog CMOS phase locked loop that uses either the system clock or a crystal for its reference. The programmed clock outputs are selectable via four address lines and an address latch enable pin.

SOIC Package



Plastic-DIP Package



FEATURES

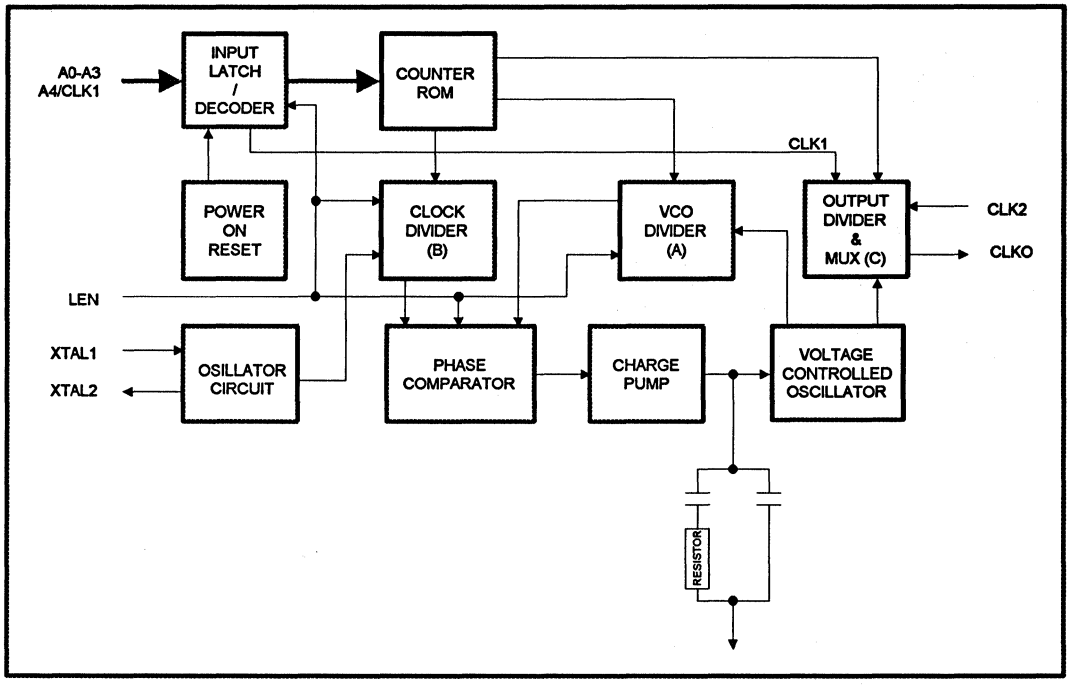
* Can replace multiple crystals or oscillators
* Pin -to-pin compatible to ICS1394
* Programmable analog phase locked loop
* High speed (up to 135 MHz output)
* Low power single 5V CMOS technology
* 20 pin DIP or SOIC package

ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C394CP20-xx	Plastic-DIP	0° C to +70° C
ST49C394CF20-xx	SOIC	0° C to +70° C
ST49C394CJ20-xx	PLCC	0° C to +70° C

ST49C394

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL1	5	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	6	O	Crystal output.
CLK2	7	I	External clock input 2.
A0	18	I	Frequency select address 1.
A1	19	I	Frequency select address 2.
LEN	2	I	Address latch enable input (active high). May be disabled via internal option mask.
A2	20	I	Frequency select address 3.
A3	1	I	Frequency select address 4.
A4/CLK1	4	I	Frequency select address 5 or external clock input 1..
GND	8	O	Digital ground.
CLKO	9	O	Programmed clock output.
VCC	3	I	Digital supply voltage. Single +5 volts.
AGND	17	O	Analog ground.
AVCC	12	I	Analog supply voltage. Single +5 volts.

ST49C394

FUNCTIONAL DESCRIPTION

The ST49C394 is designed to output one of the 16 or 32 possible mask preprogrammable frequencies.
For one of 16 output selections, address lines A0-A3 and LEN (latch enable) are used and the selected address (A0-A3) is latched on the falling edge of LEN. For one of 32 output selections, address lines A0-A4 and LEN are used. The unused A4 address line in the one of 16 mode can be used (mask programmed) as an external clock input. The ST49C394 is designed to work with the existing ICS1394 footprint without modifing the art-work and components. The ST49C394 does not utilize pins11, 13, 14, 15, and 16 as these functions are implemented internally to reduce the external component count and noise problems.

POWER ON RESET

An internal power on reset is provided to set the latched address to "0000".

FREQUENCY SELECT CALCULATION

The ST49C394 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.
The accuracy of the frequencies produced by the ST49C394 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

CLKO=(Reference clock) X (A/BxC)

where A=1,2,3,.....127,
B=1,2,3,.....127,and
C=1, 2, 4, 8, 16, 32, 64.

For proper operation, the ST49C394 can accept reference frequencies from 5 - 40 MHz and divider ratios up to 15.

MASK OPTIONS

The following mask options are provided for custom applications.

* Address is latched utilizing the LEN pin.
* Transparent address input.
* CLK1 can be preprogrammed as external clock input.
* Selectable/Programmable clock frequencies.

Video clock address (Hex)	ST49C394-24 Frequency (MHz)	ST49C394-30 Frequency (MHz)			
0	25.175	14.318			
1	28.322	16.257			
2	32.514	FREQ0			
3	36.000	32.514			
4	40.000	25.175			
5	44.900	28.322			
6	65.000	24.000			
7	84.000	40.000			
8	25.175	14.318			
9	28.322	16.257			
A	40.000	FREQ0			
B	44.900	36.000			
C	32.514	25.175			
D	28.322	28.322			
E	36.000	24.000			
F	65.000	40.000			
10	25.175	14.318			
11	28.322	65.028			
12	32.514	FREQ0			
13	36.000	36.000			
14	40.000	25.175			
15	44.900	28.322			
16	56.000	24.000			
17	65.000	40.000			
18	25.175	44.900			
19	28.322	50.344			
1A	32.514	16.257			
1B	40.000	32.514			
1C	44.900	56.644			
1D	60.000	20.000			
1E	80.000	50.000			
1F	84.000	80.000			

* Input clock frequency=14.31818
* Strobed address: No

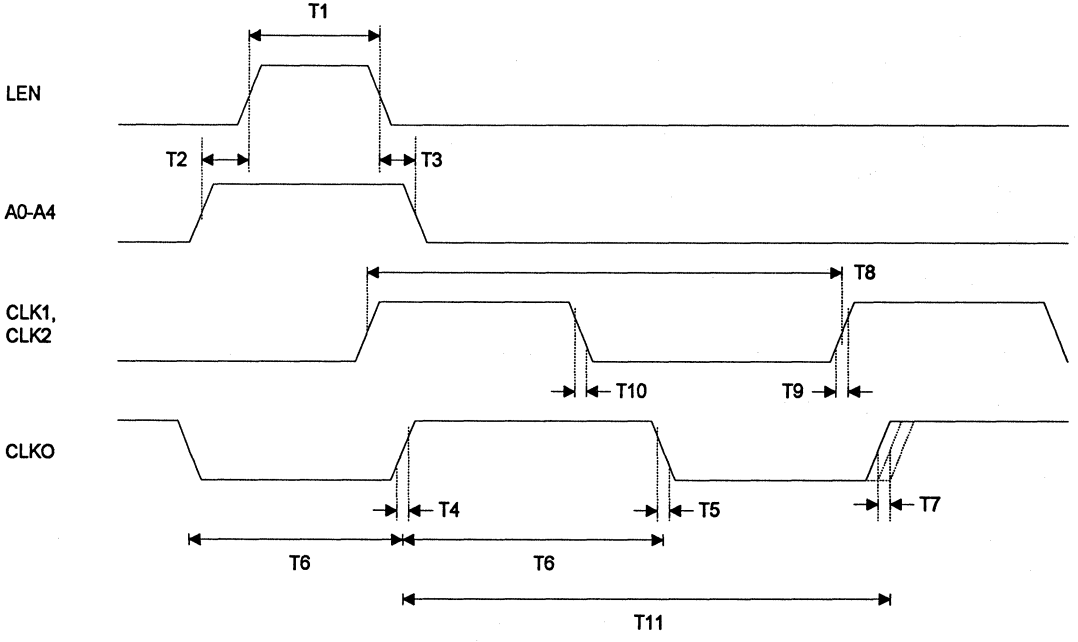
ST49C394

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Enable pulse width	20			ns	
T_2	Setup time address to enable	20			ns	
T_3	Hold time to address enable	10			ns	
T_4	Rise time			4	ns	
T_5	Fall time			4	ns	
T_6	Duty cycle	40	48/52	60	%	
T_7	Jitter		±85	±100	ps	
T_8	Input frequency	5		40	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	
V_{OH}	Output high level	2.4			V	
I_{IL}	Input low current			-5	µA	Except crystal input
I_{IH}	Input high current			5	µA	
I_{CC}	Operating current		10		mA	No load.

ST49C394

LINE DRIVERS / RECEIVERS

Index

STARTECH

ST26C31

APR 1992

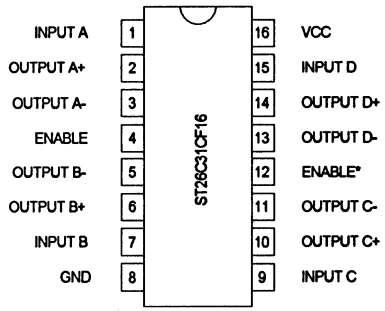
QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

DESCRIPTION

The ST26C31 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST26C31 circuit.

The ST26C31 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

SOIC package

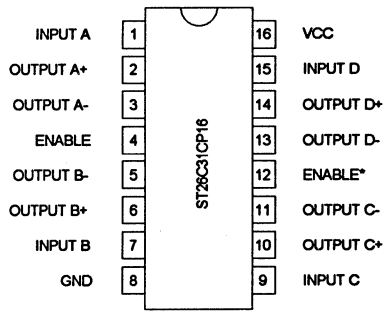


2

FEATURES

* Pin-to-pin compatible with National DS26C31C
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

Plastic-DIP package

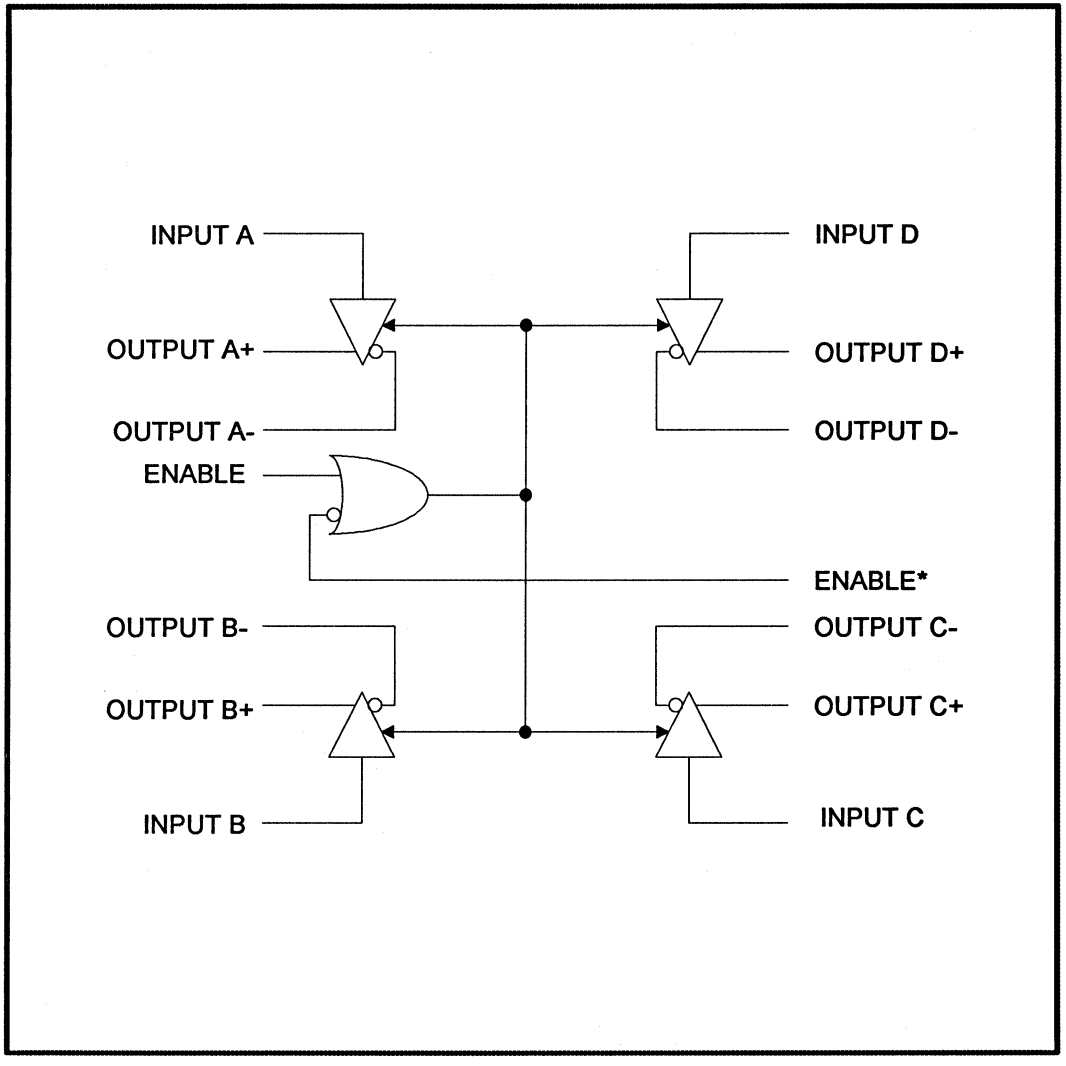


ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C31CP16	Plastic-DIP	0° C to + 70° C
ST26C31CF16	SOIC	0° C to + 70° C

ST26C31

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A	1	I	Driver A input pin.
OUTPUT A+	2	O	Driver A differential non-inverting output pin.
OUTPUT A-	3	O	Driver A differential inverting output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four drivers. All four drivers are gated with two input or gate.
OUTPUT B-	5	O	Driver B differential inverting output pin.
OUTPUT B+	6	O	Driver B differential non-inverting output pin.
INPUT B	7	I	Driver B input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverting output pin.
OUTPUT C-	11	O	Driver C differential inverting output pin.
ENABLE*	12	I	Gate control (active low). See ENABLE pin description.
OUTPUT D-	13	O	Driver D differential inverting output pin.
OUTPUT D+	14	O	Driver D differential non-inverting output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

ST26C31

Functional table

Enable	Enable*	Input	Differential Non-Inverting Output	Differential Inverting Output
L	H	X	Z	Z
L	L	L	L	H
L	L	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	L	H
H	H	H	H	L

X=Don't care
Z=Three state (high impedance)

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	
T_2	Differential output rise and fall time		8	10	ns	
T_3	Output enable time		18	20	ns	
T_4	Output disable time		18	20	ns	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

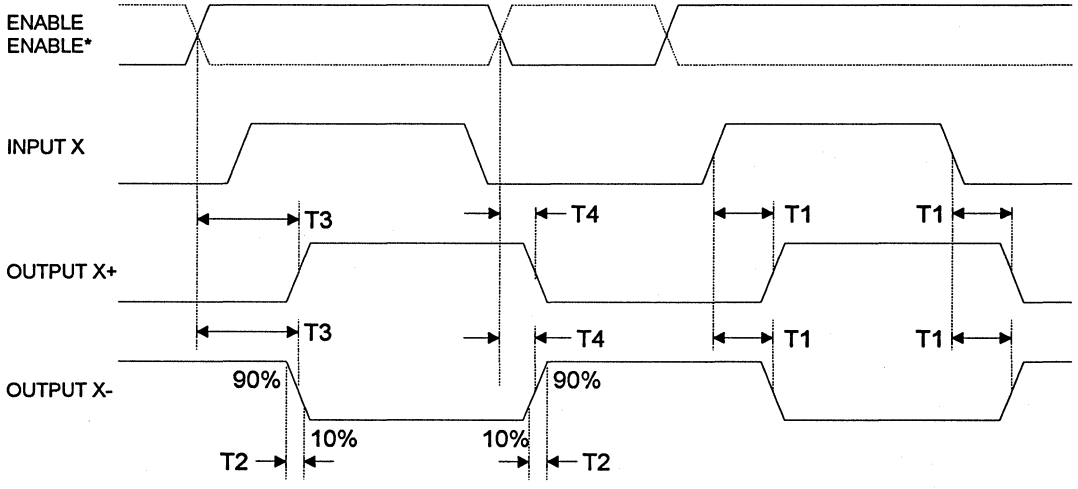
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Input high level	2.0			V	
V_{IL}	Input low level			0.8	V	
V_{OH}	Output high level	2.5			V	
V_{OL}	Output low level			0.5	V	
V_{OS}	Differential output level	2.0			V	R_L=100 ohms
V_{OC}	Common mode output voltage			3.0	V	R_L=100 ohms
V_{OD}	Difference in common mode output			0.4	V	R_L=100 ohms
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	

ST26C31

DIFFERENTIAL LINE DRIVER TIMING



STARTECH

ST26C32

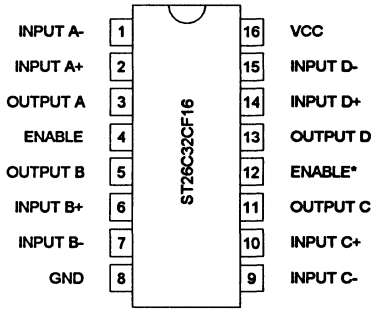
APR 1992

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of +/- 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.
The ST26C32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST26C32 is suitable for low power 5V operation.

SOIC package

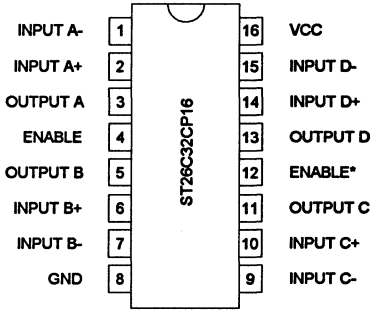


2

FEATURES

* Pin-to-pin compatible with National DS26C32C
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

Plastic-DIP package

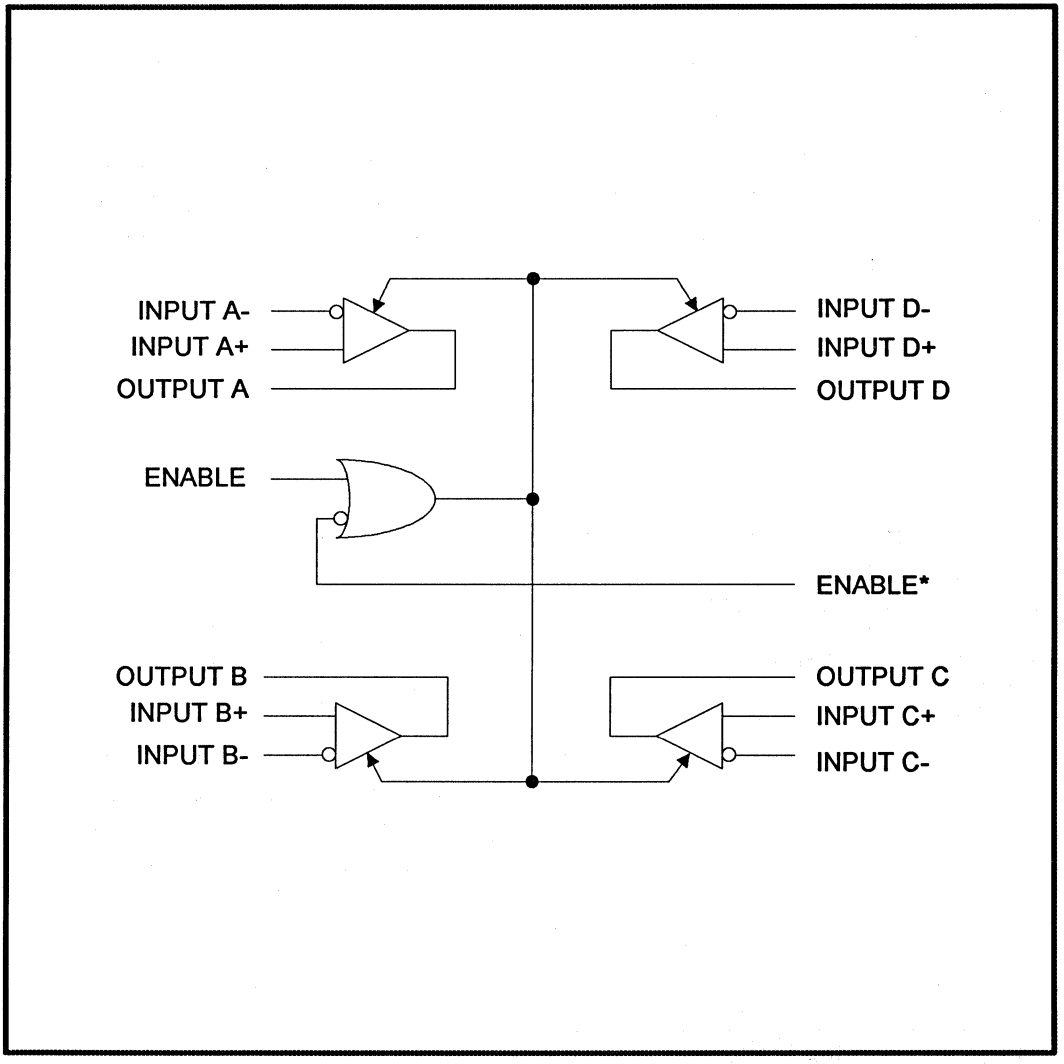


ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C32CP16	Plastic-DIP	0° C to + 70° C
ST26C32CF16	SOIC	0° C to + 70° C

ST26C32

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables all four receivers.
INPUT B+	5	I	Receiver B differential non-inverting input pin.
INPUT B-	6	I	Receiver B differential inverting input pin.
OUTPUT B	7	O	Receiver B output pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Receiver C differential non-inverting input pin.
INPUT C-	10	I	Receiver C differential inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE*	12	I	Gate control (active low). See ENABLE description
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

ST26C32

Functional table

Enable	Enable*	Output	Differential Non-Inverting Input	Differential Inverting Input
L	H	Z	X	X
H	L	L	L	H
H	L	H	H	L

X=Don't care
Z=Three state (high impedance)

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	
T_3	Output enable time		18	20	ns	
T_4	Output disable time		18	20	ns	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

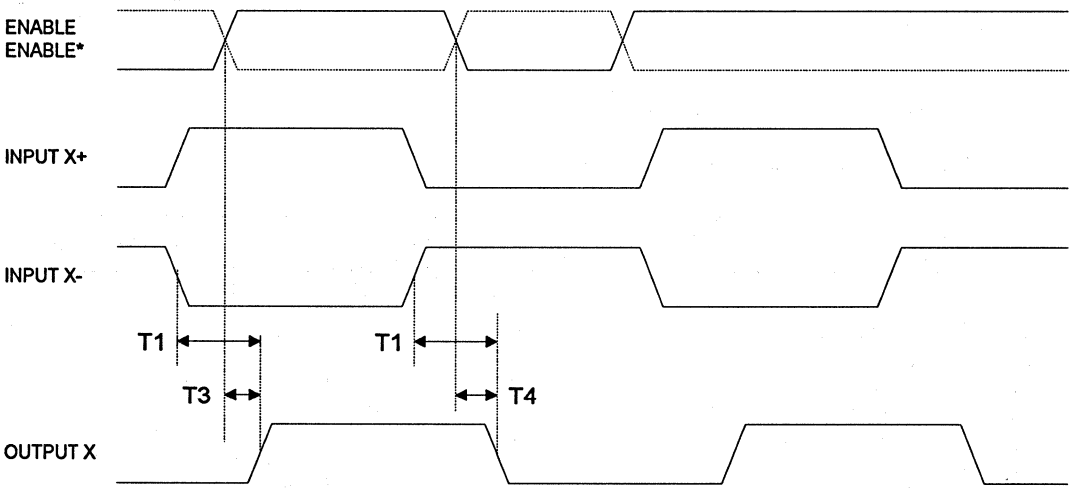
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8			V	I_{OH}=-6mA
V_{OL}	Output low level			0.4	V	I_{OH}=6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	mA	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_R	Input resistance		10		Kohm	-7V < V_{CM} < +7V

ST26C32

DIFFERENTIAL LINE RECEIVER TIMING



STARTECH

ST34C50
ST34C51

APR 1992

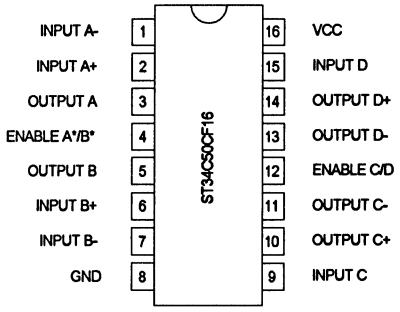
DUAL RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER AND DRIVER

GENERAL DESCRIPTION

The ST34C50/51 is a CMOS dual differential line receiver and driver, designed to meet the standard RS-422, RS-423 requirements and digital data transmission over balanced lines. The ST34C50/51 has an input sensitivity of 200mv over the common mode input voltage range of +/- 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C50/51 circuit.

The ST34C50/51 is a high speed line receiver and driver, designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C50/51 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C50/51 is suitable for low power 5V operation with minimum board space requirements. ST34C50/51 provides dual differential line receiver with three state control pin and dual line driver with three state control capability.

SOIC Package

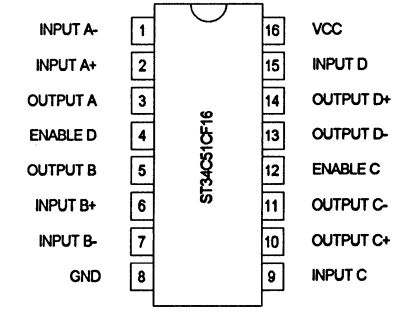


ST34C50CF / ST34C50CP

FEATURES

* Pin -to-pin compatible to Motorola MC34050 and MC34051
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422/423 requirements
* Low propagation delays
* High speed
* Dual line receiver with three state control
* Dual line driver with three state control

SOIC Package

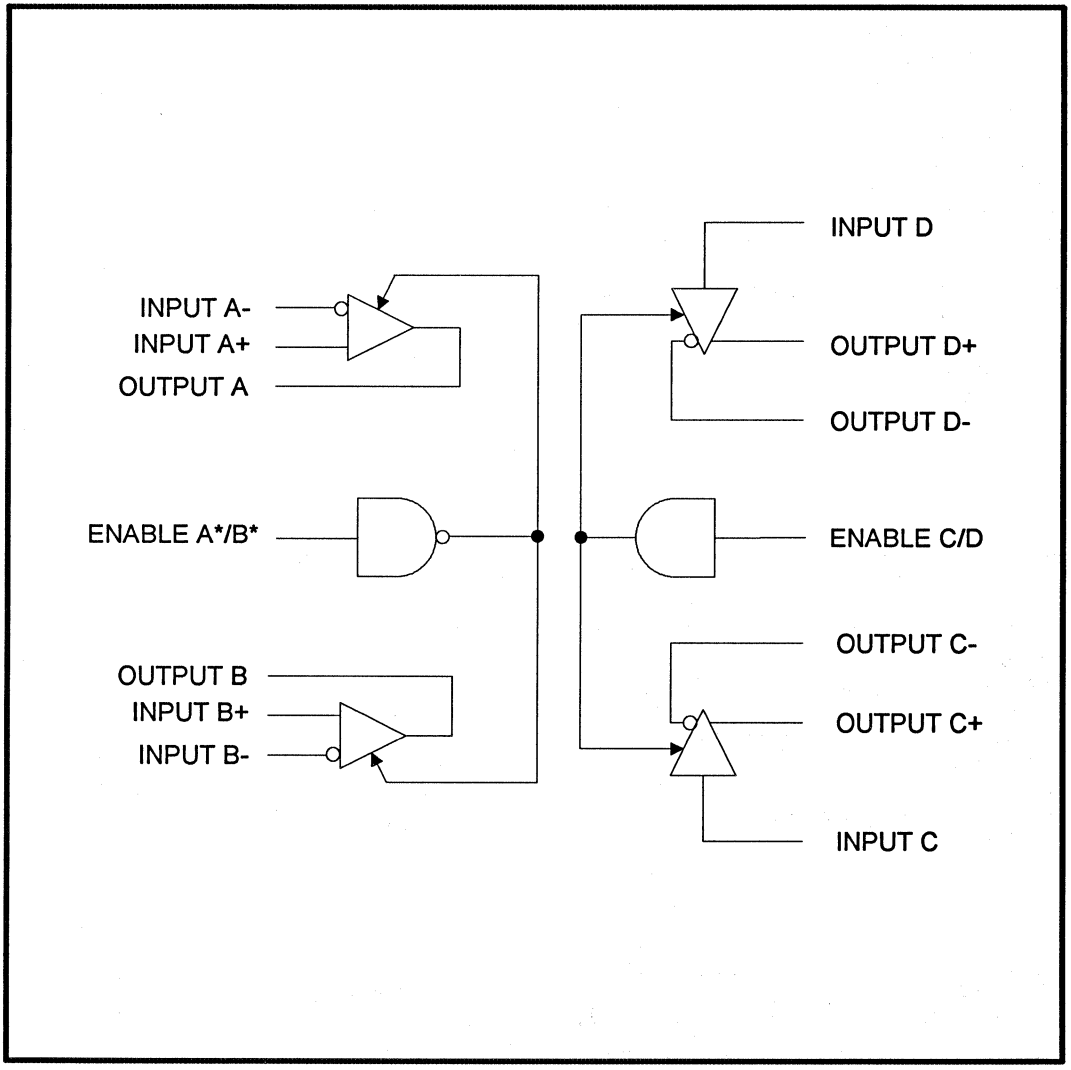


ST34C51CF / ST34C51CP

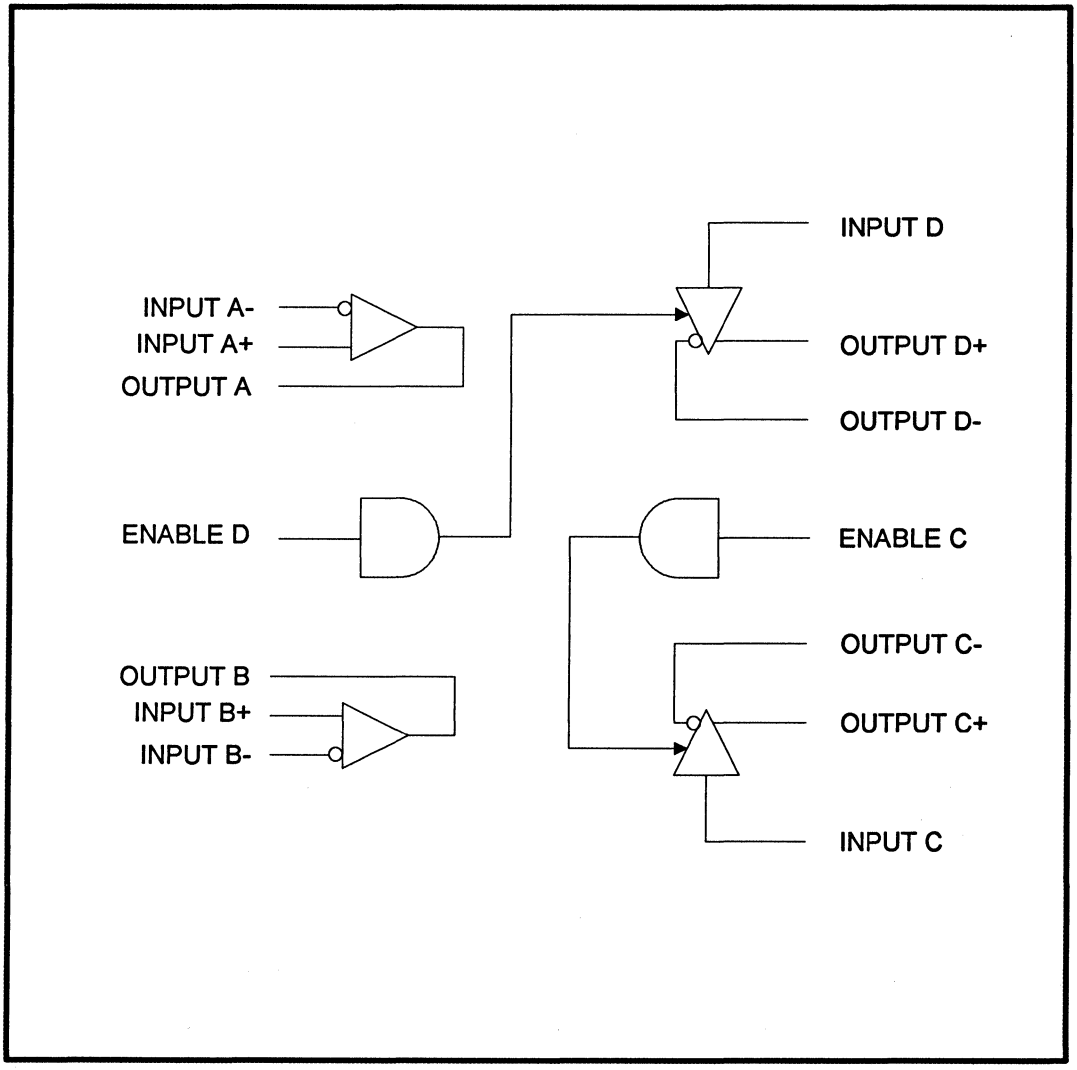
ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C50CP16	Plastic-DIP	0° C to + 70° C
ST34C50CF16	SOIC	0° C to + 70° C
ST34C51CP16	Plastic-DIP	0° C to + 70° C
ST34C51CF16	SOIC	0° C to + 70° C

ST34C50 BLOCK DIAGRAM



ST34C51 BLOCK DIAGRAM



ST34C50
ST34C51

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active low , ST34C50 only). This pin enables/ disables the two line receiver outputs (out A and out B of ST34C50).
ENABLE D	4*	I	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver D section.
OUTPUT B	5	O	Receiver B output pin.
INPUT B +	6	I	Receiver B differential non-inverting input pin.
INPUT B -	7	I	Receiver B differential inverting input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverted output pin.
OUTPUT C -	11	O	Driver C differential inverted output pin.
ENABLE C/D	12	I	Gate control (active high, ST34C50 only). This pin enables/ disables the two line driver outputs (output C and output D of ST34C50).
ENABLE C	12*	I	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver C section.
OUTPUT D -	13	O	Driver D differential inverted output pin.
OUTPUT D+	14	O	Driver D differential non-inverted output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

Receiver Functional table (ST34C50 only)

Enable	Output	Differential Non-Inverting Input	Differential Inverting Input
H	Z	X	X
L	L	L	H
L	H	H	L

X=Don't care
Z=Three state (high impedance)
Receive sections of the ST34C51 are enabled all the time.

Driver Functional table (ST34C50 only)

Enable C/D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)

***Driver Functional table (ST34C51only)**

Enable C or D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)
* for each section of ST34C51.

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	
T_2	Differential output rise and fall time		8	10	ns	
T_3	Output enable time		18	20	ns	
T_4	Output disable time		18	20	ns	

ST34C50
ST34C51

ABSOLUTE MAXIMUM RATINGS

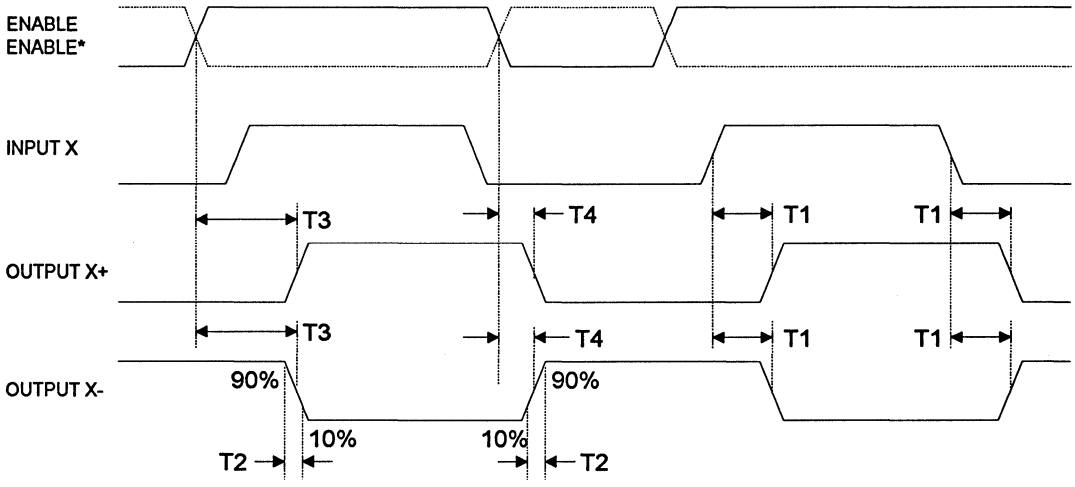
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

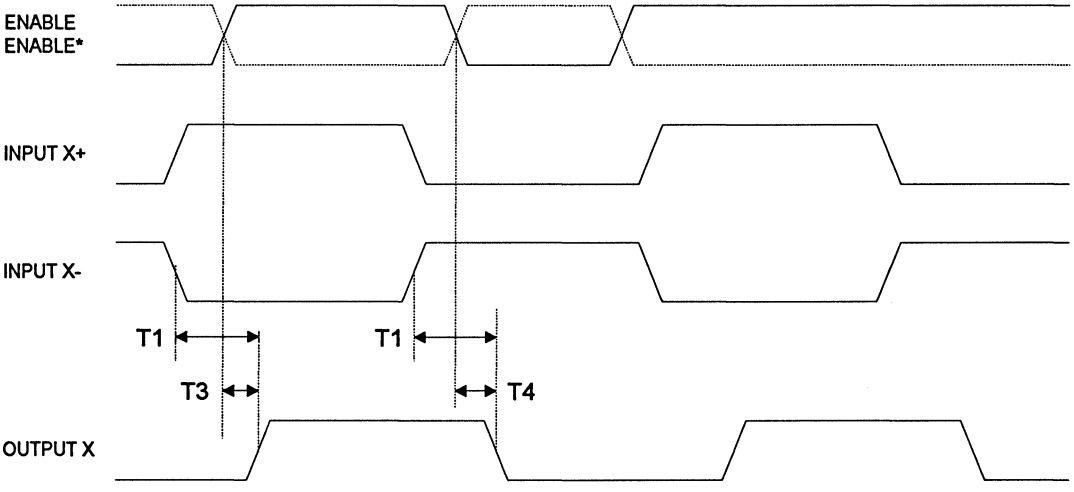
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{ROH}	Receiver output high level	3.8			V	
V_{ROL}	Receiver output low level			0.4	V	
V_{RID}	Receiver differential input level	-0.2		+0.2	V	R_L=100 ohms
V_{RH}	Receiver input hysteresis		50		mV	
I_{RIN}	Receiver input current			±1.0	mA	
V_{RR}	Receiver input resistance		10		Kohm	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_{DOH}	Driver input high level	2.5			V	
V_{DOL}	Driver output low level			0.5	V	
V_{DOS}	Driver differential output level	2.0			V	R_L=100 ohms
V_{DOC}	Driver Common mode output voltage			3.0	V	R_L=100 ohms
V_{DOD}	Driver difference in common mode output			0.4	V	R_L=100 ohms
I_{DIN}	Driver input current			±1.0	µA	

DIFFERENTIAL LINE DRIVER TIMING



DIFFERENTIAL LINE RECEIVER TIMING



STARTECH

ST34C86

APR 1992

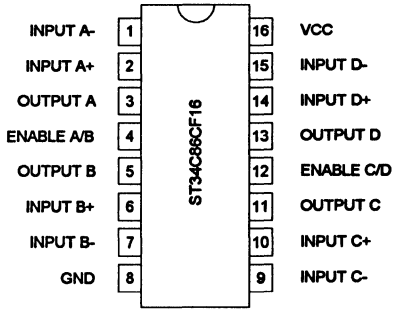
QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of +/- 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit.

The ST34C86 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

SOIC package

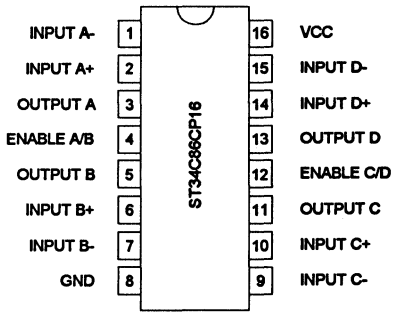


2

FEATURES

* Pin-to-pin compatible with National DS34C86
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

Plastic-DIP package

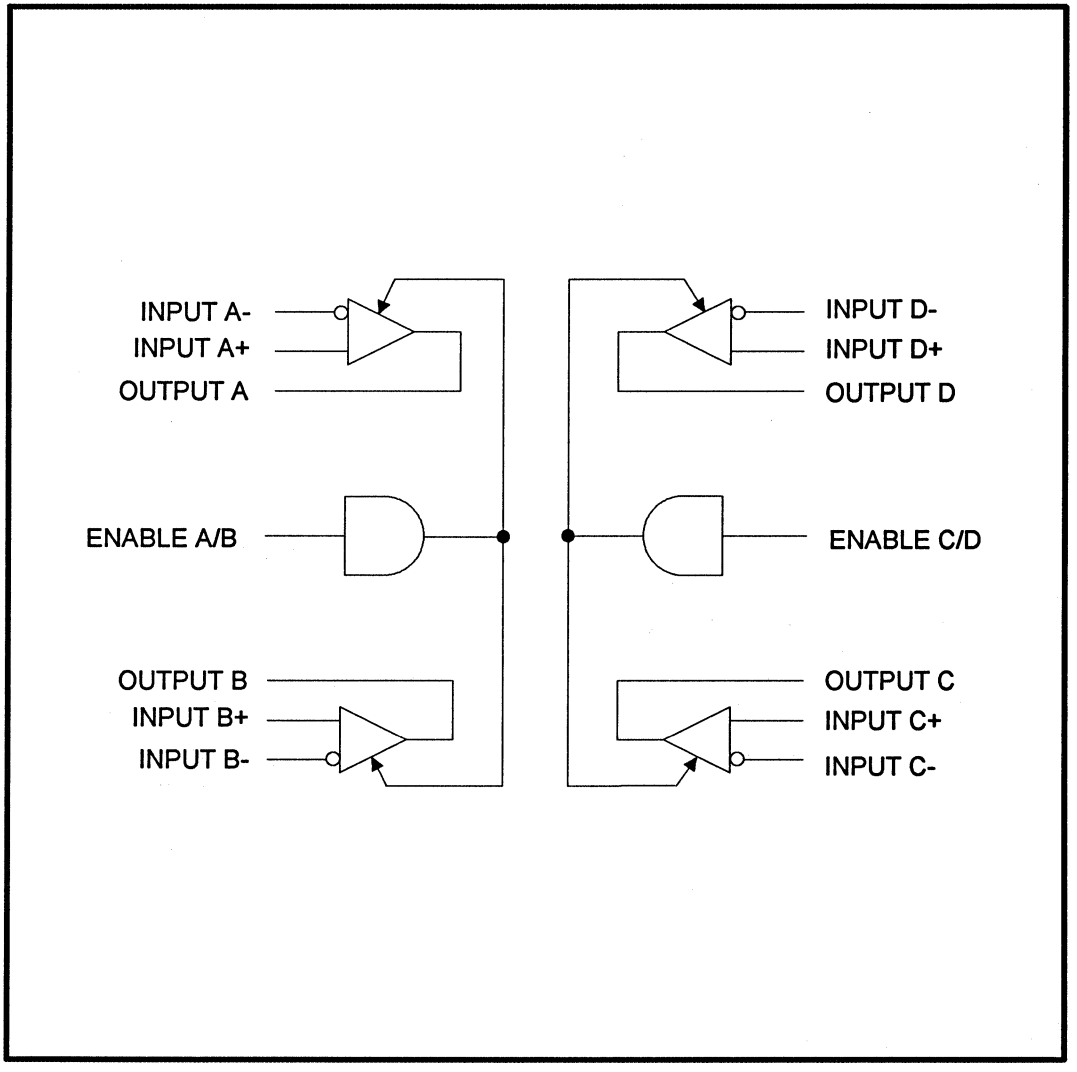


ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C86CP16	Plastic-DIP	0° C to + 70° C
ST34C86CF16	SOIC	0° C to + 70° C

ST34C86

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	I	Receiver A differential non-inverting input pin.
OUTPUT A	3	O	Receiver A output pin.
ENABLE A/B	4	I	Gate control (active high). This pin enables/disables the two line receiver outputs (out A and out B).
INPUT B+	5	I	Receiver B differential non-inverting input pin.
INPUT B-	6	I	Receiver B differential inverting input pin.
OUTPUT B	7	O	Receiver B output pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Receiver C differential non-inverting input pin.
INPUT C-	10	I	Receiver C differential inverting input pin.
OUTPUT C	11	O	Receiver C output pin.
ENABLE C/D	12	I	Gate control (active high). This pin enables/disables the two line receiver outputs (output C and output D).
OUTPUT D	13	O	Receiver D output pin.
INPUT D+	14	I	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
VCC	16	I	Power supply pin.

ST34C86

ST34C86

Functional table

Enable	Output	Differential Non-Inverting Input	Differential Inverting Input
L	Z	X	X
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	
T_3	Output enable time		18	20	ns	
T_4	Output disable time		18	20	ns	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

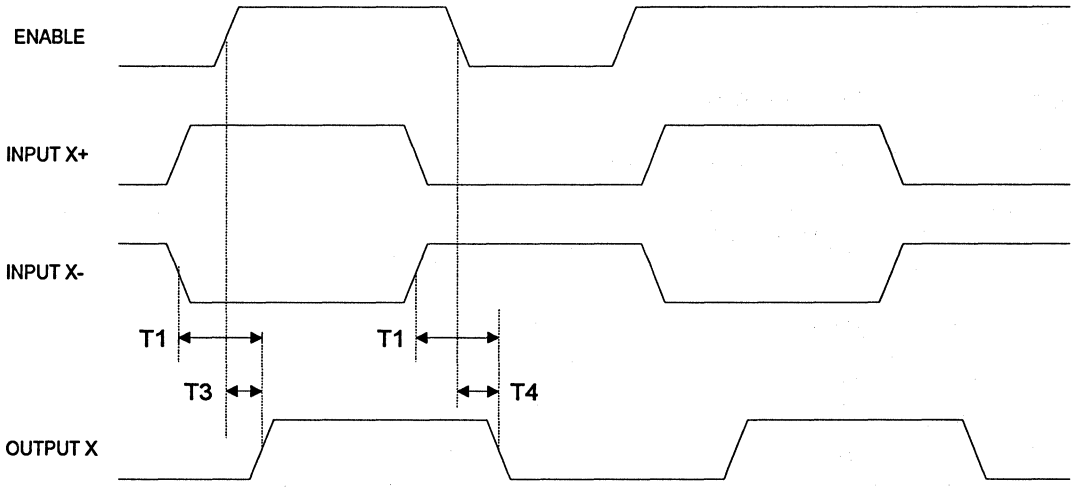
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Enable high level	2.0			V	
V_{IL}	Enable low level			0.8	V	
V_{OH}	Output high level	3.8			V	I_{OH}=-6mA
V_{OL}	Output low level			0.4	V	I_{OH}=6mA
V_{ID}	Differential input level	-0.2		+0.2	V	-7V < V_{CM} < +7V
V_H	Input hysteresis		50		mV	
I_{IN}	Input current			±1.0	mA	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	
V_R	Input resistance		10		Kohm	-7V < V_{CM} < +7V

ST34C86

DIFFERENTIAL LINE RECEIVER TIMING



STARTECH

ST34C87

APR 1992

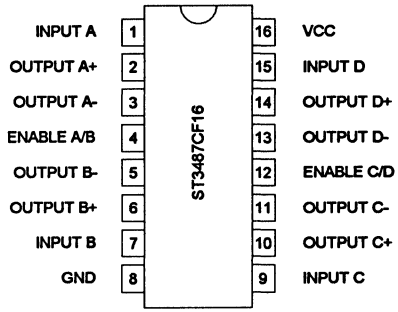
QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The ST34C87 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST34C87 circuit.

The ST34C87 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST34C87 is suitable for low power 5V operation with high input voltage protection devices.

SOIC package

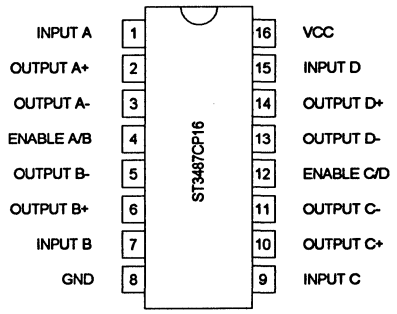


2

FEATURES

* Pin-to-pin compatible with National DS34C87
* Low power CMOS design
* Three-state outputs with enable pin
* Meets the EIA RS-422 requirements
* Low propagation delays
* High speed

Plastic-DIP package

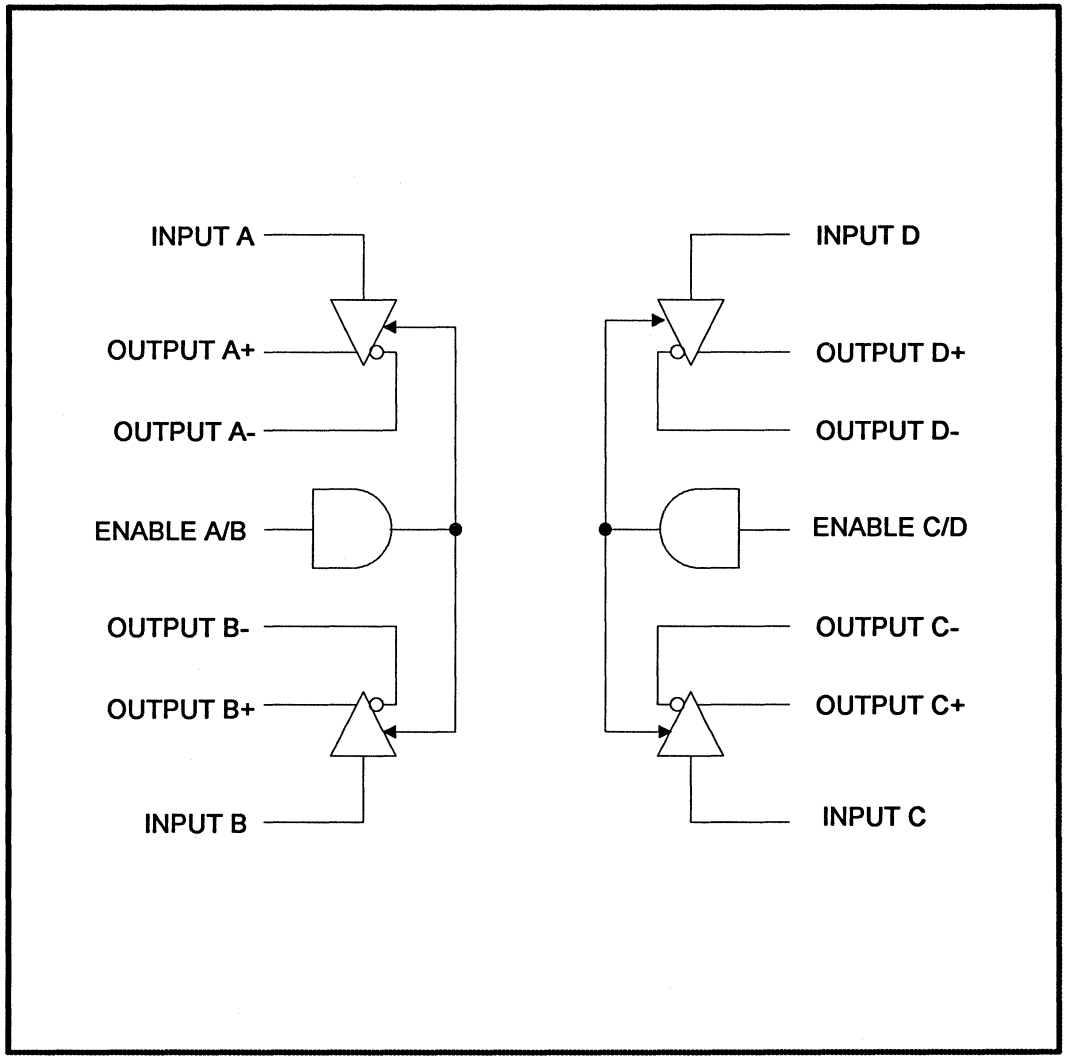


ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C87CP16	Plastic-DIP	0° C to + 70° C
ST34C87CF16	SOIC	0° C to + 70° C

ST34C87

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A	1	I	Driver A input pin.
OUTPUT A+	2	O	Driver A differential non-inverting output pin.
OUTPUT A-	3	O	Driver A differential inverting output pin.
ENABLE A/B	4	I	Gate control (active high). This pin is one of the two control pins which enables or disables two/four drivers.
OUTPUT B-	5	O	Driver B differential inverting output pin.
OUTPUT B+	6	O	Driver B differential non-inverting output pin.
INPUT B	7	I	Driver B input pin.
GND	8	O	Signal and power ground.
INPUT C	9	I	Driver C input pin.
OUTPUT C+	10	O	Driver C differential non-inverting output pin.
OUTPUT C-	11	O	Driver C differential inverting output pin.
ENABLE C/D	12	I	Gate control (active high). See ENABLE A/B pin description.
OUTPUT D*	13	O	Driver D differential inverting output pin.
OUTPUT D	14	O	Driver D differential non-inverting output pin.
INPUT D	15	I	Driver D input pin.
VCC	16	I	Power supply pin.

ST34C87

ST34C87

Functional table

Enable	Input	Differential Non-Inverting Output	Differential Inverting Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care
Z=Three state (high impedance)

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Units	Conditions
T_1	Propagation delay, input to output		8	10	ns	
T_2	Differential output rise and fall time		8	10	ns	
T_3	Output enable time		18	20	ns	
T_4	Output disable time		18	20	ns	

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

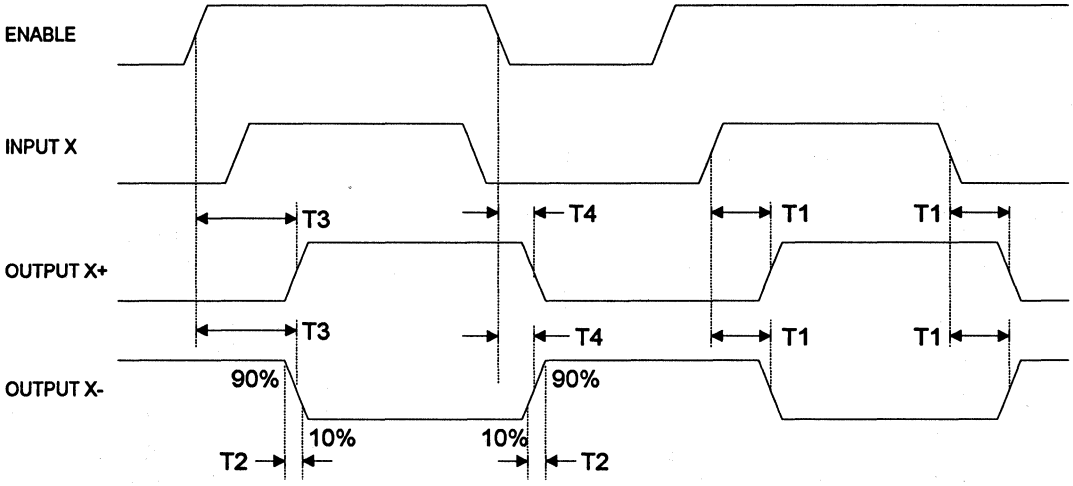
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IH}	Input high level	2.0			V	
V_{IL}	Input low level			0.8	V	
V_{OH}	Output high level	2.5			V	
V_{OL}	Output low level			0.5	V	
V_{OS}	Differential output level	2.0			V	R_L=100 ohms
V_{OC}	Common mode output voltage			3.0	V	R_L=100 ohms
V_{OD}	Difference in common mode output			0.4	V	R_L=100 ohms
I_{IN}	Input current			±1.0	µA	
I_{CC}	Operating current		200		µA	
I_{OZ}	Three state output leakage		±2.0		µA	

ST34C87

DIFFERENTIAL LINE DRIVER TIMING



UARTS

Index

STARTECH

ST16C450

APR 1992

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

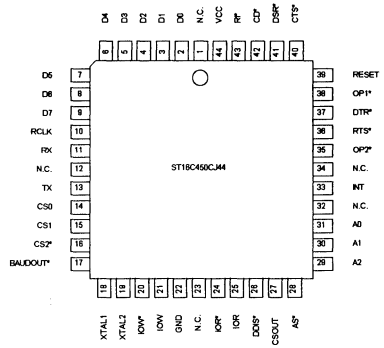
DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

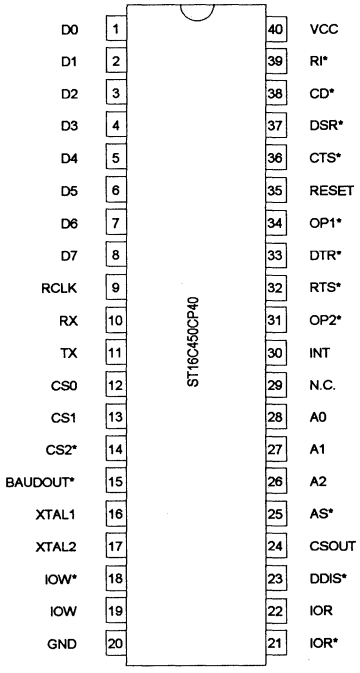
The ST16C450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C450 provides internal loopback capability for on board diagnostic testing.

The ST16C450 is fabricated in an advanced 1.2 µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

* Pin to pin and functional compatible to NS16450, VL16C450, WD16C450
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

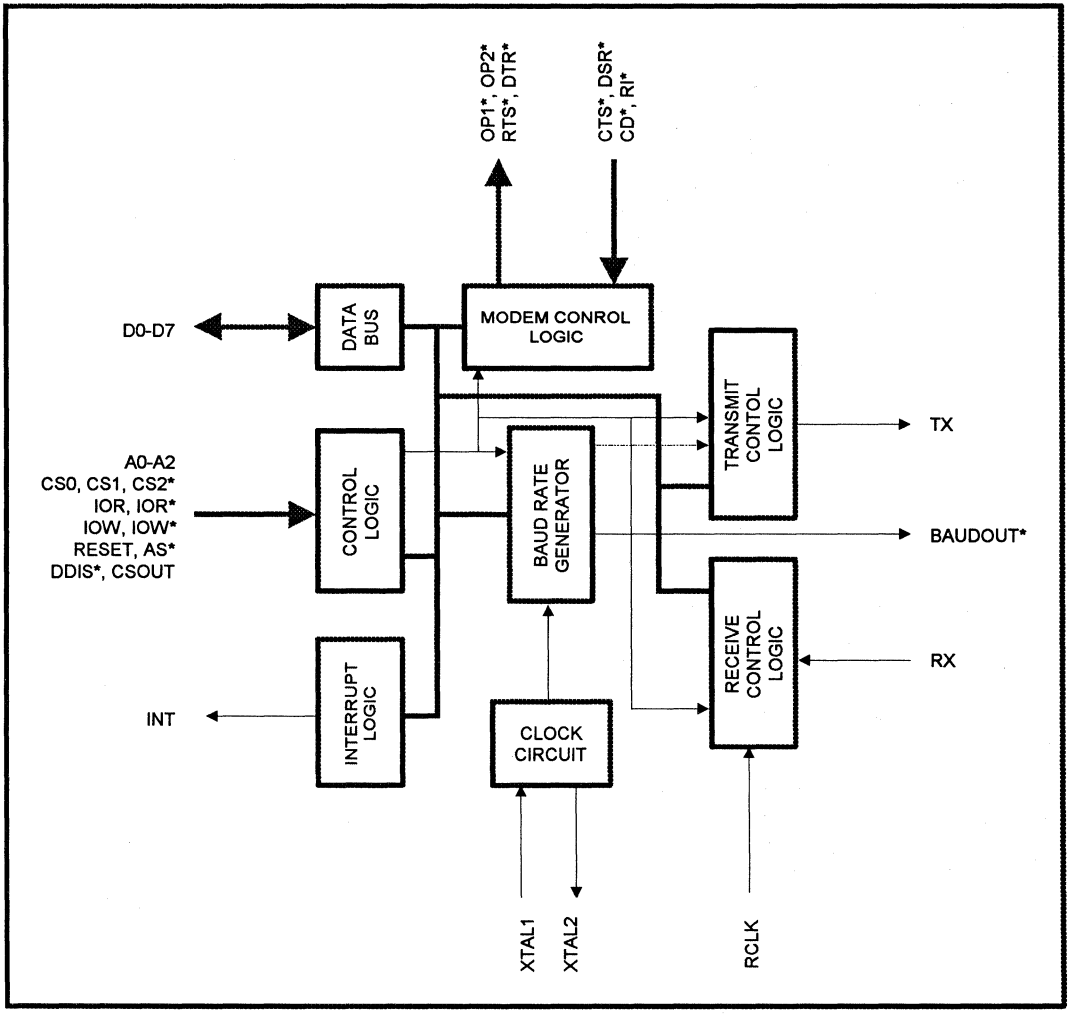
Partnumber	Package	Operating temperature
ST16C450CP40	Plastic-DIP	0° C to + 70° C
ST16C450CJ44	PLCC	0° C to + 70° C

*** Industrial operating range are available.**

3

ST16C450

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the ST16C450 receiver section if receiver data rate is different from transmitter data rate.
RX	10	I	Serial data input. The serial information (data) received from serial port to ST16C450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS1	13	I	Chip select 2 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS2*	14	I	Chip select 3 (active low). A low at this pin (while CS0=1 and CS1=1) will enable the ST16C450 / CPU data transfer operation.
BAUDOUT*	15	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide the receiver clock.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

ST16C450

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	Write strobe (active high). Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C450 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	O	Signal and power ground.
IOR*	21	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C450 data bus to the CPU.
IOR	22	I	Read strobe (active high). Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C450 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23	O	Drive disable (active low). This pin goes low when the CPU is reading data from the ST16C450 to disable the external transceiver or logics.
CSOUT	24	O	Chip select out. A high on this pin indicates that the ST16C450 has been enabled by the chip select pin.
AS*	25	I	Address strobe (active low). A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	I	Address select line 2. To select internal registers.
A1	27	I	Address select line 1. To select internal registers.
A0	28	I	Address select line 0. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
N/C	29		No connection.
INT	30	O	Interrupt output (active high). This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	O	General purpose output (active low). User defined output. See bit-3 modem control register (MCR bit-3).
RTS*	32	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	O	Data terminal ready (active low). To indicate that ST16C450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	O	General purpose output (active low). User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	35	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	37	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive opera-

ST16C450

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			tion.
CD*	38	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
RI*	39	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C450 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C450

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16} - 1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:
0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now

ST16C450

the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C450 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNAL	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
INT	Low

ST16C450

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time			100	ns	
T_4	Baud out rise/fall time			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select			10	ns	
T_{11}	IOR* to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW*	5			ns	Note: 1
T_{13}	IOW* delay from address	25			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	Note: 1
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low
Baudout cycle

ST16C450

ST16C450

ABSOLUTE MAXIMUM RATINGS

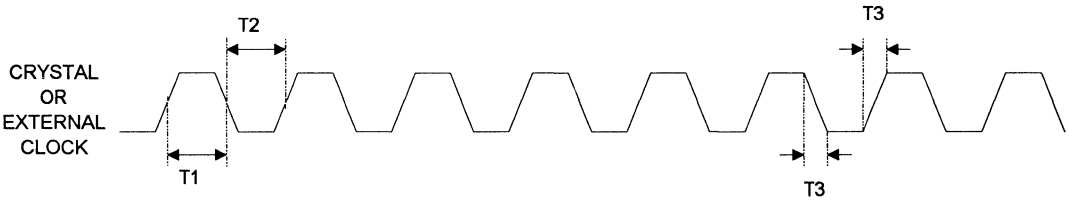
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

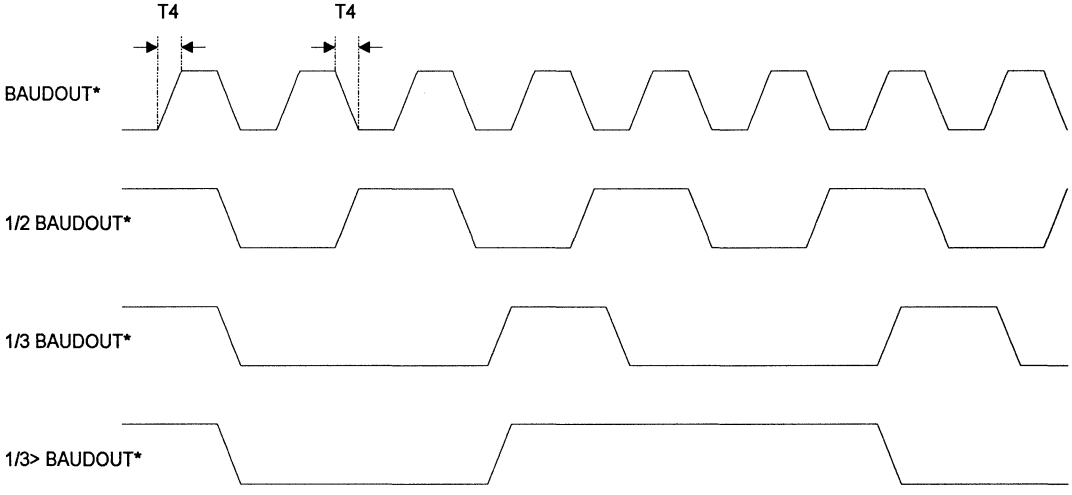
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

CLOCK TIMING



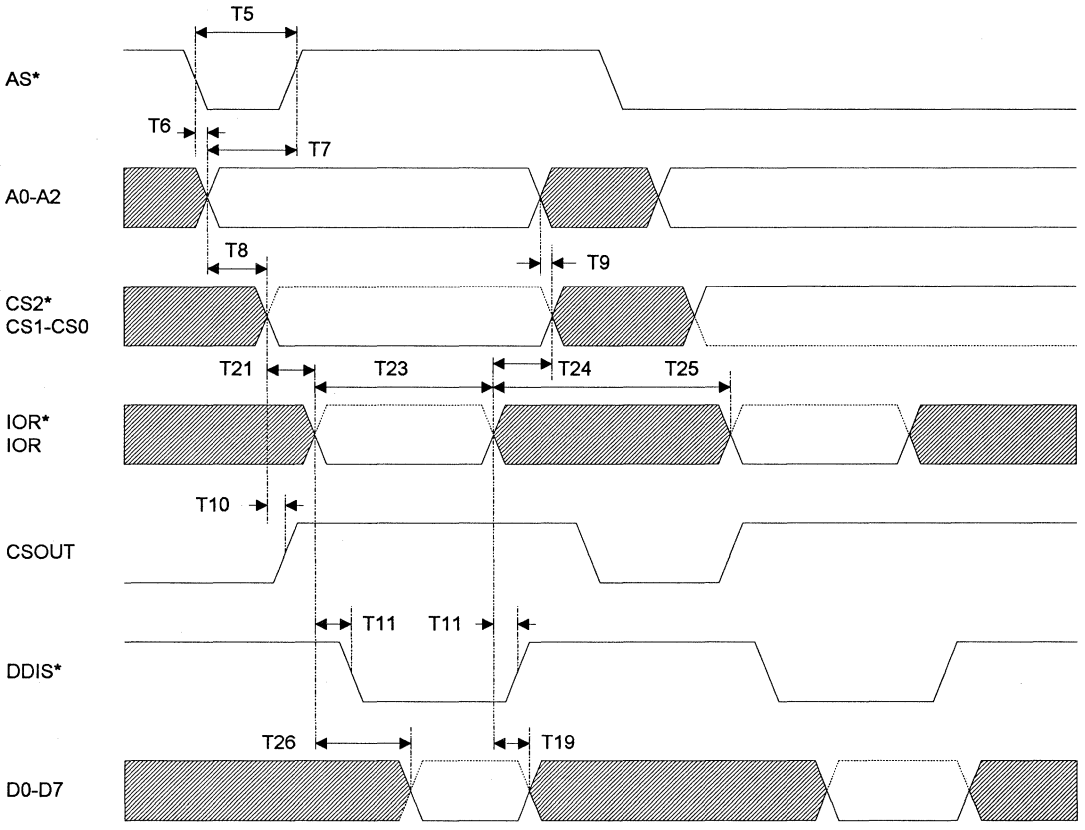
BAUDOUT* TIMING



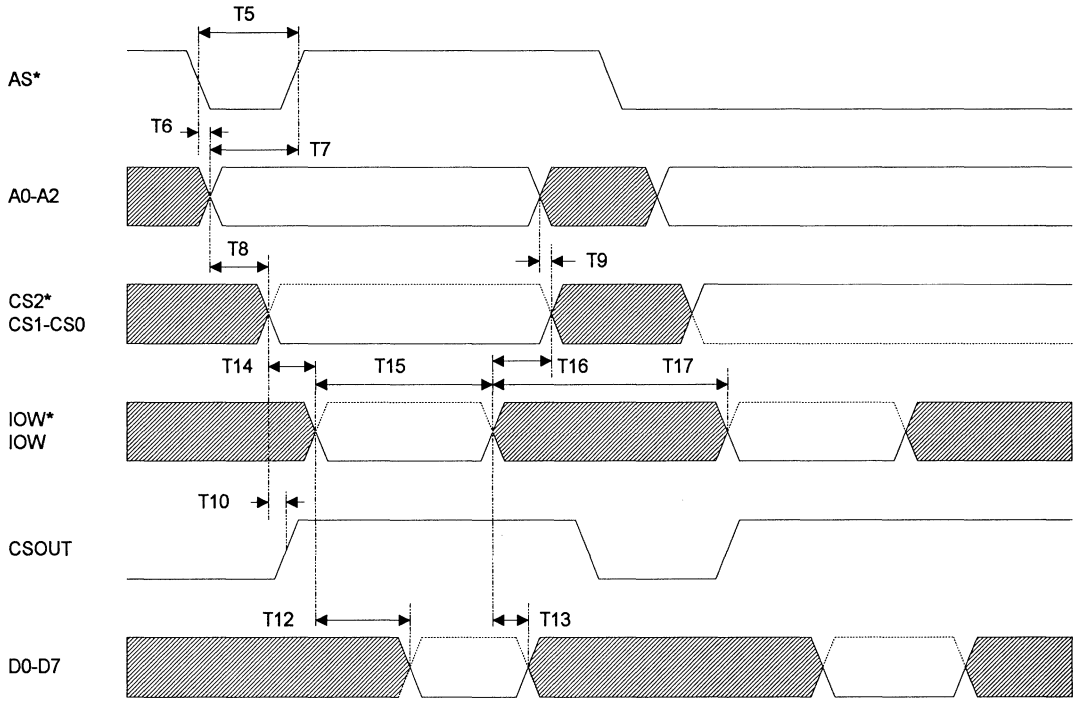
ST16C450

ST16C450

GENERAL READ TIMING

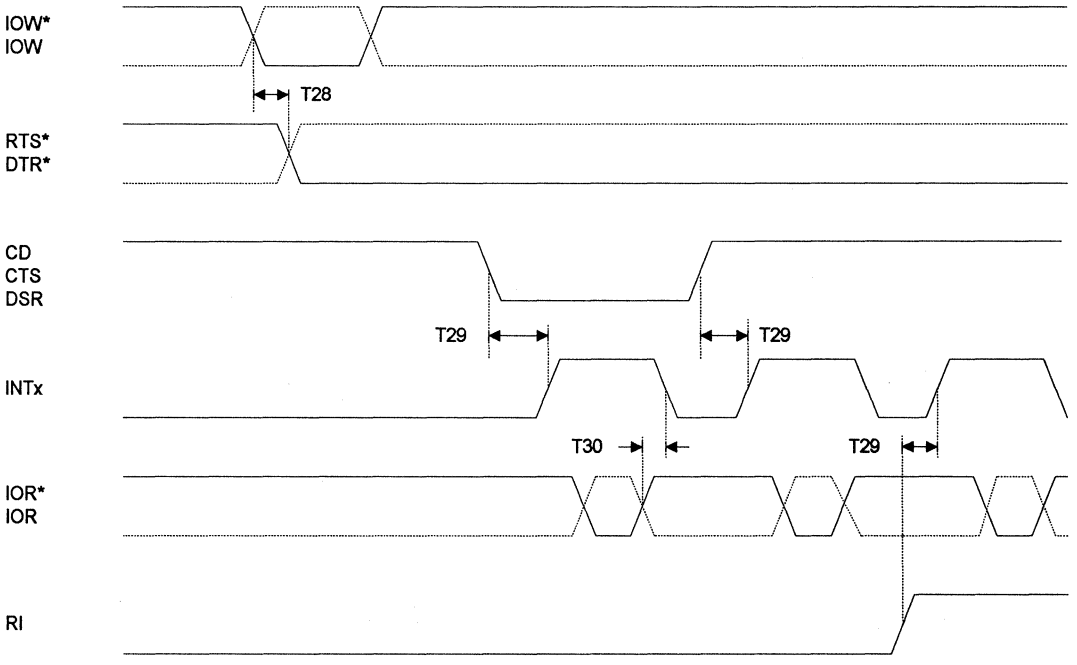


GENERAL WRITE TIMING

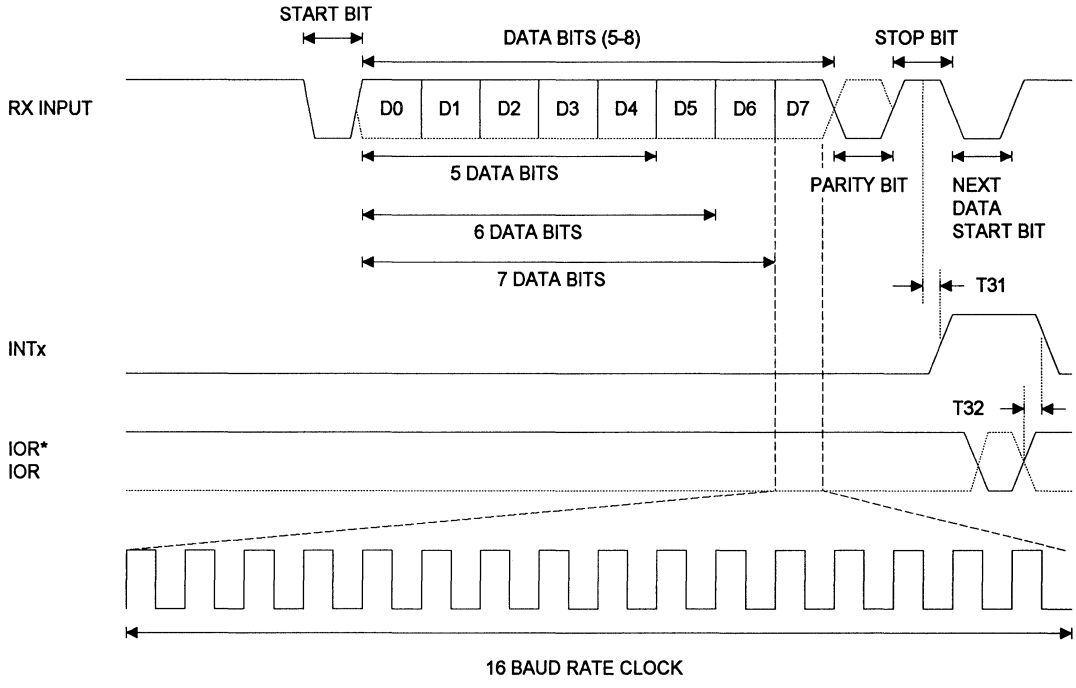


ST16C450

MODEM TIMING

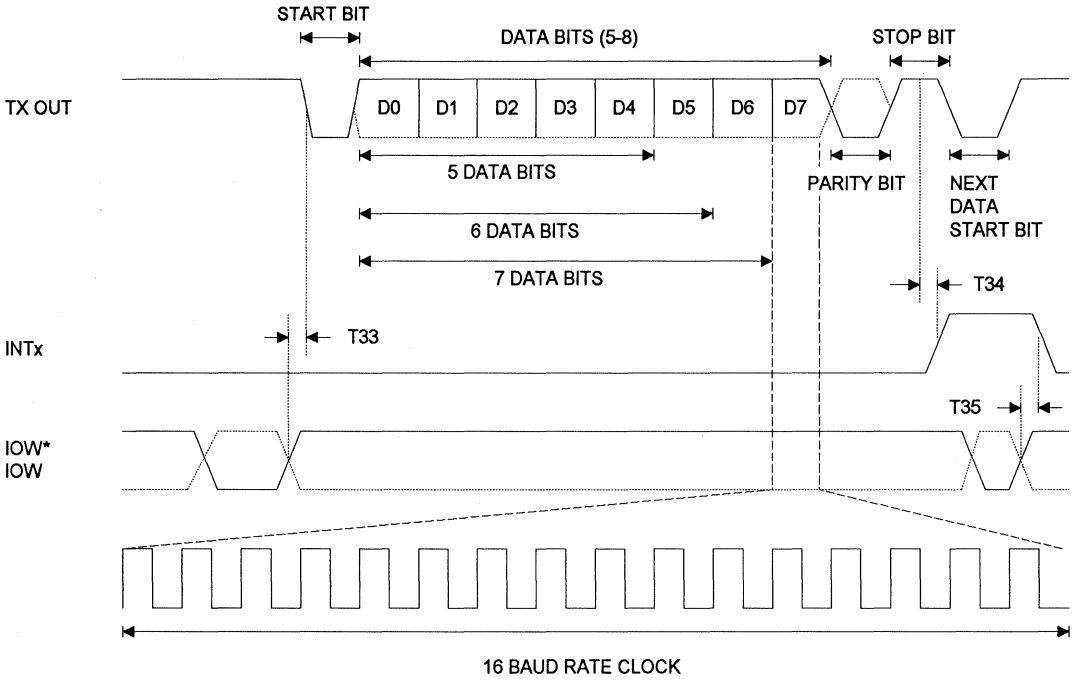


RECEIVE TIMING



ST16C450

TRANSMIT TIMING



STARTECH

ST16C1450
ST16C1451

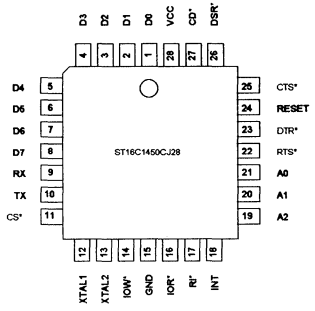
APR 1992

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C1450/51 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.
The ST16C1450/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1450/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1450/51 provides internal loop-back capability for on board diagnostic testing.
The ST16C1450/51 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



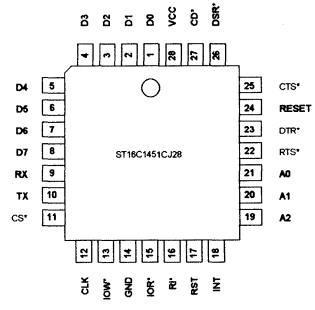
ST16C1450

3

FEATURES

* Pin to pin and functional compatible to SSI 73M1550/2550
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Software compatible with INS8250, NS16C550
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
* 28 Pin plastic-Dip and PLCC package
* Pin-to-pin compatible to ST16C1550/1551

PLCC Package



ST16C1451

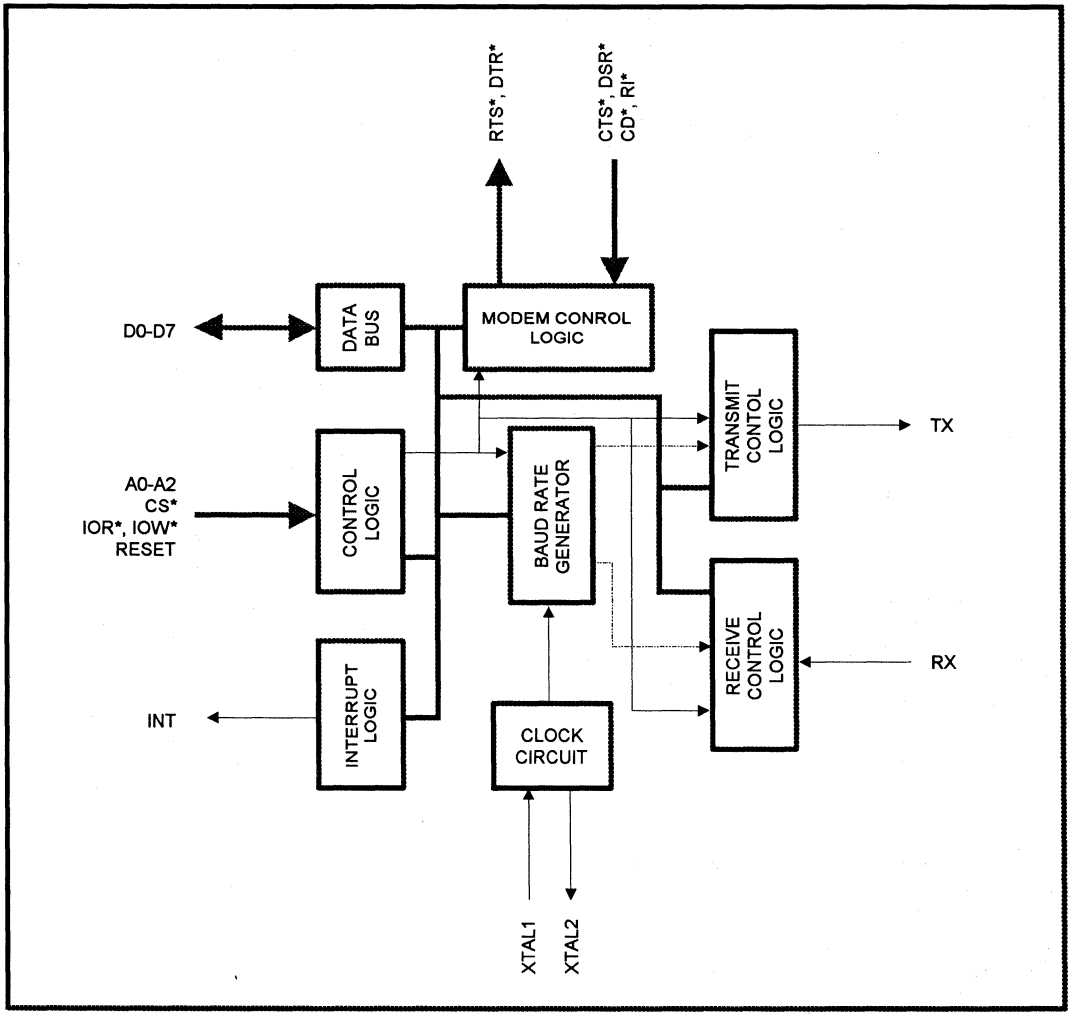
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1450CP28	Plastic-DIP	0° C to + 70° C
ST16C1450CJ28	PLCC	0° C to + 70° C
ST16C1451CP28	Plastic-DIP	0° C to + 70° C
ST16C1451CJ28	PLCC	0° C to + 70° C

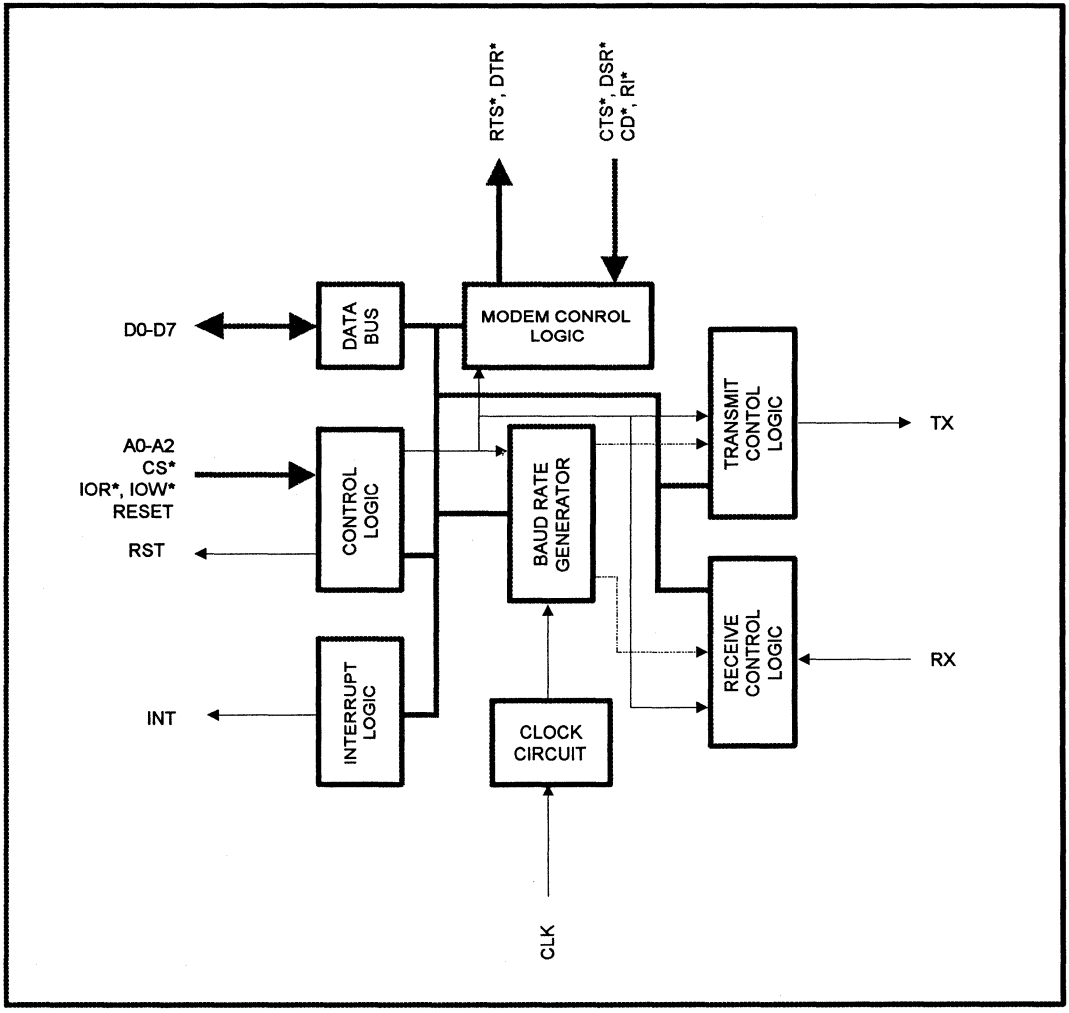
***Industrial operating range are available.**

ST16C1450
ST16C1451

ST16C1450 BLOCK DIAGRAM



ST16C1451 BLOCK DIAGRAM



ST16C1450
ST16C1451

ST16C1450 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1450 / CPU data transfer operation.
XTAL1	12	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	O	Signal and power ground.
IOR*	16	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1450 data bus to the CPU..
RI*	17	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
INT	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a

ST16C1450 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1450
ST16C1451

ST16C1451 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1451 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1451 / CPU data transfer operation.
CLK	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
IOW*	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	14	O	Signal and power ground.
IOR*	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1451 data bus to the CPU..
RI*	16	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
RST	17	O	Reaset output (active high). The ST16C1451 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a

ST16C1451 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1451 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1450
ST16C1451

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C1450 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C1450
ST16C1451

ST16C1451 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1450/51 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT-5:
0=normal ST16C450 mode.
1=special mode. Enable power down and SOFT rest.

IER BIT 4,6-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1450/51 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1450/51 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority levels

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR bit 3-7:
Not used

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-6:
Not used. Are set to zero permanently.

MCR bit-7:
0=normal mode.
1=power down mode. XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C1450/51 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used.

ST16C1450
ST16C1451

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C1450/51 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.
Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1450/51 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

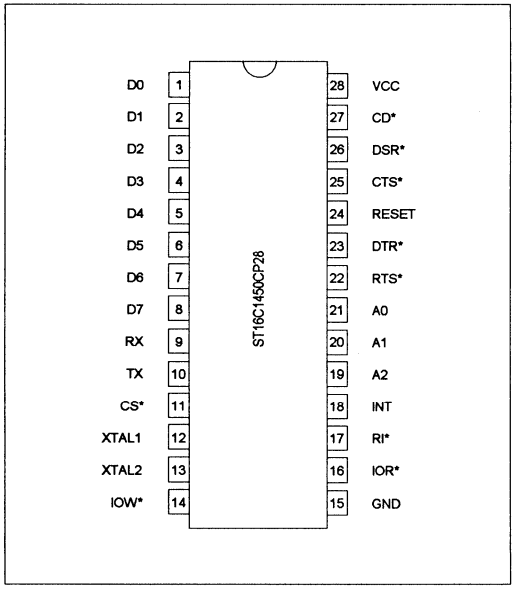
BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C1450/51 EXTERNAL RESET CONDITION

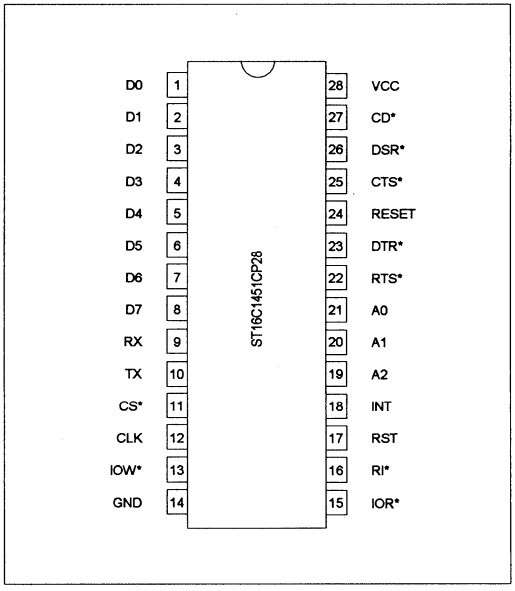
REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state mode

ST16C1450 Plastic-DIP Package



ST16C1451 Plastic-DIP Package



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ST16C1450
ST16C1451

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time			100	ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: *Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

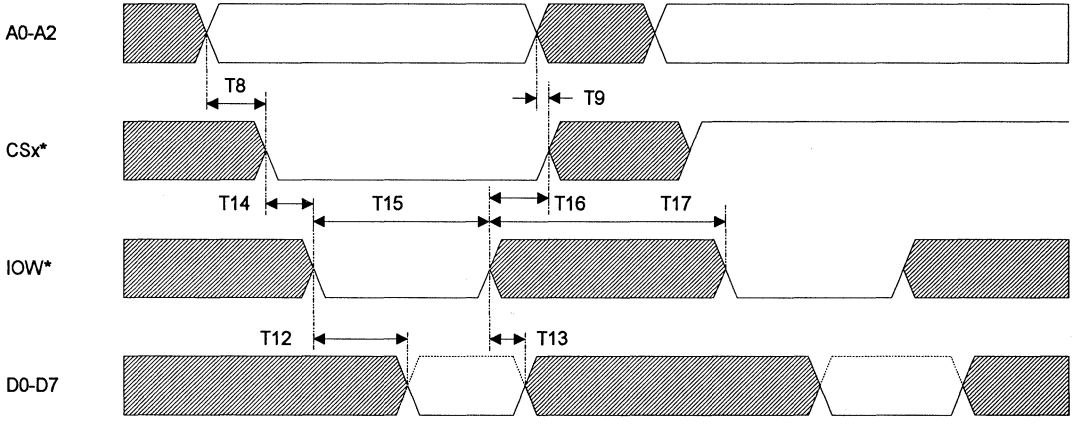
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

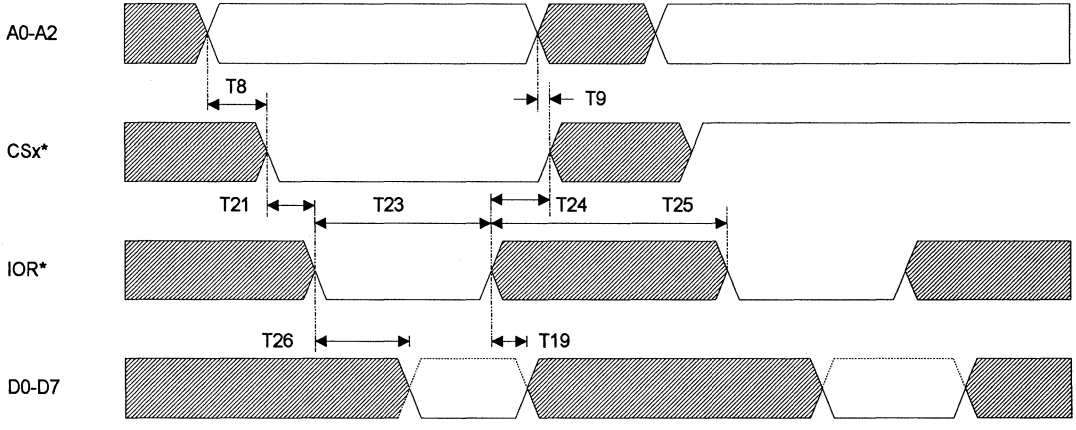
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST16C1450
ST16C1451

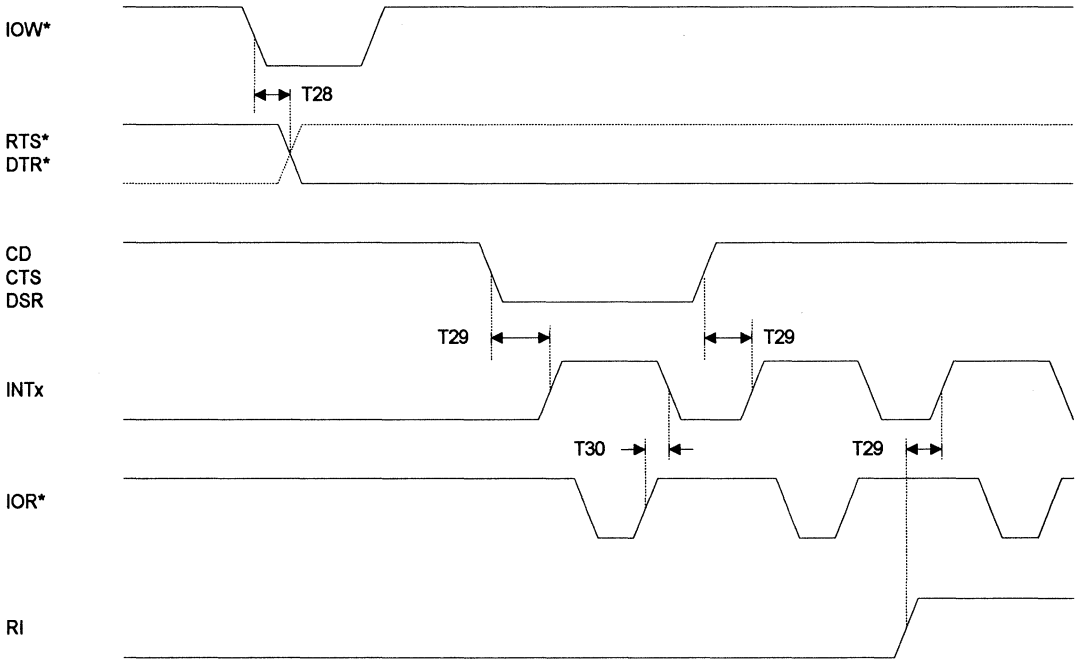
GENERAL WRITE TIMING



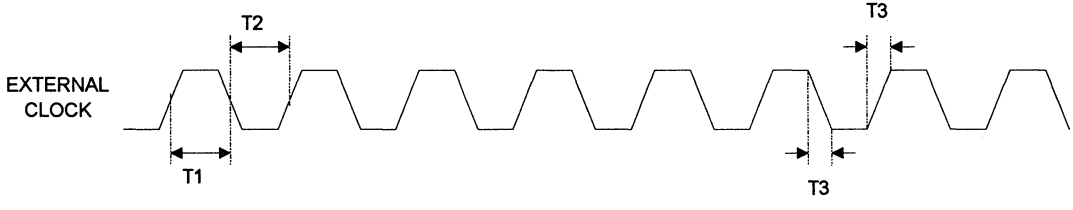
GENERAL READ TIMING



MODEM TIMING

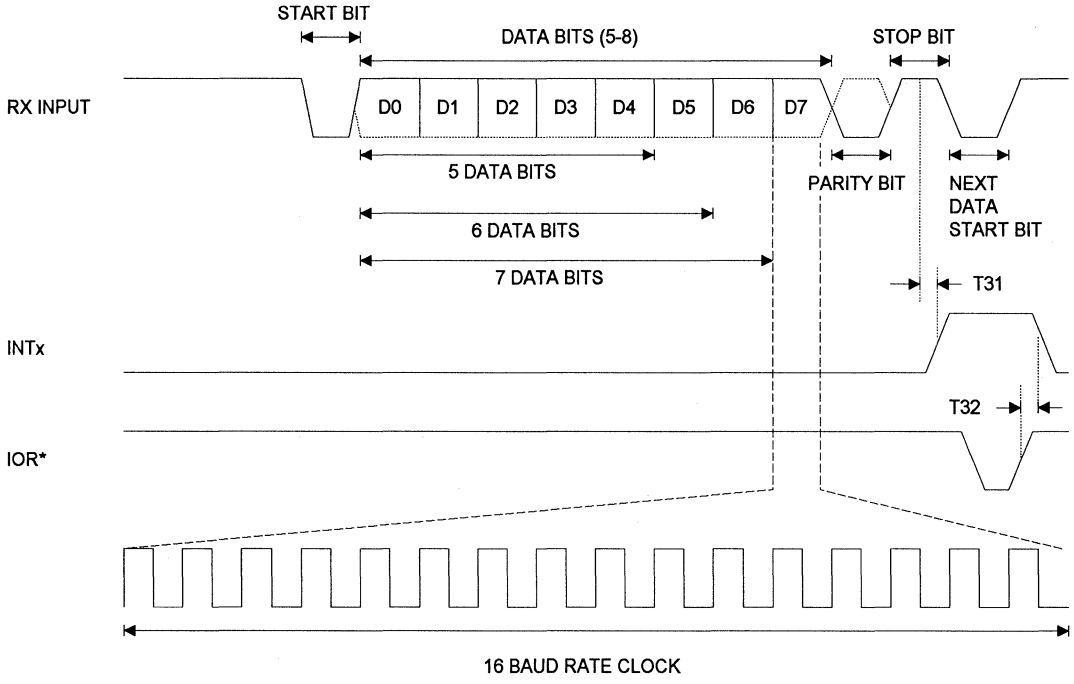


CLOCK TIMING

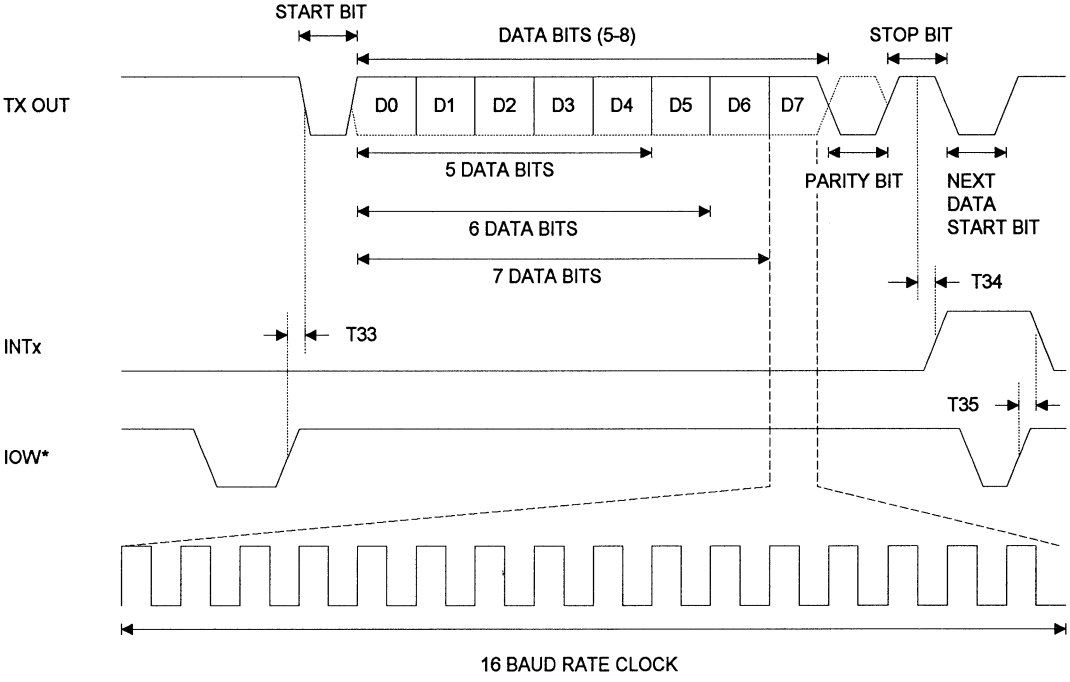


ST16C1450
ST16C1451

RECEIVE TIMING



TRANSMIT TIMING



ST16C1450
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STARTECH

ST16C2450

APR 1992

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

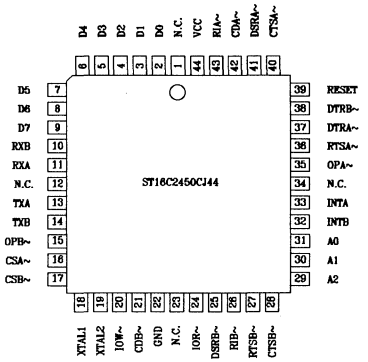
DESCRIPTION

The ST16C2450 is a dual universal asynchronous receiver and transmitter. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each uart section.

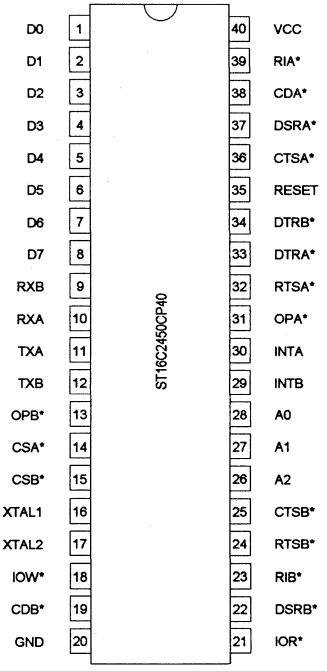
The ST16C2450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C2450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2450 provides internal loop-back capability for on board diagnostic testing.

The ST16C2450 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

* Functional compatible to NS16450, VL16C450, WD16C450
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

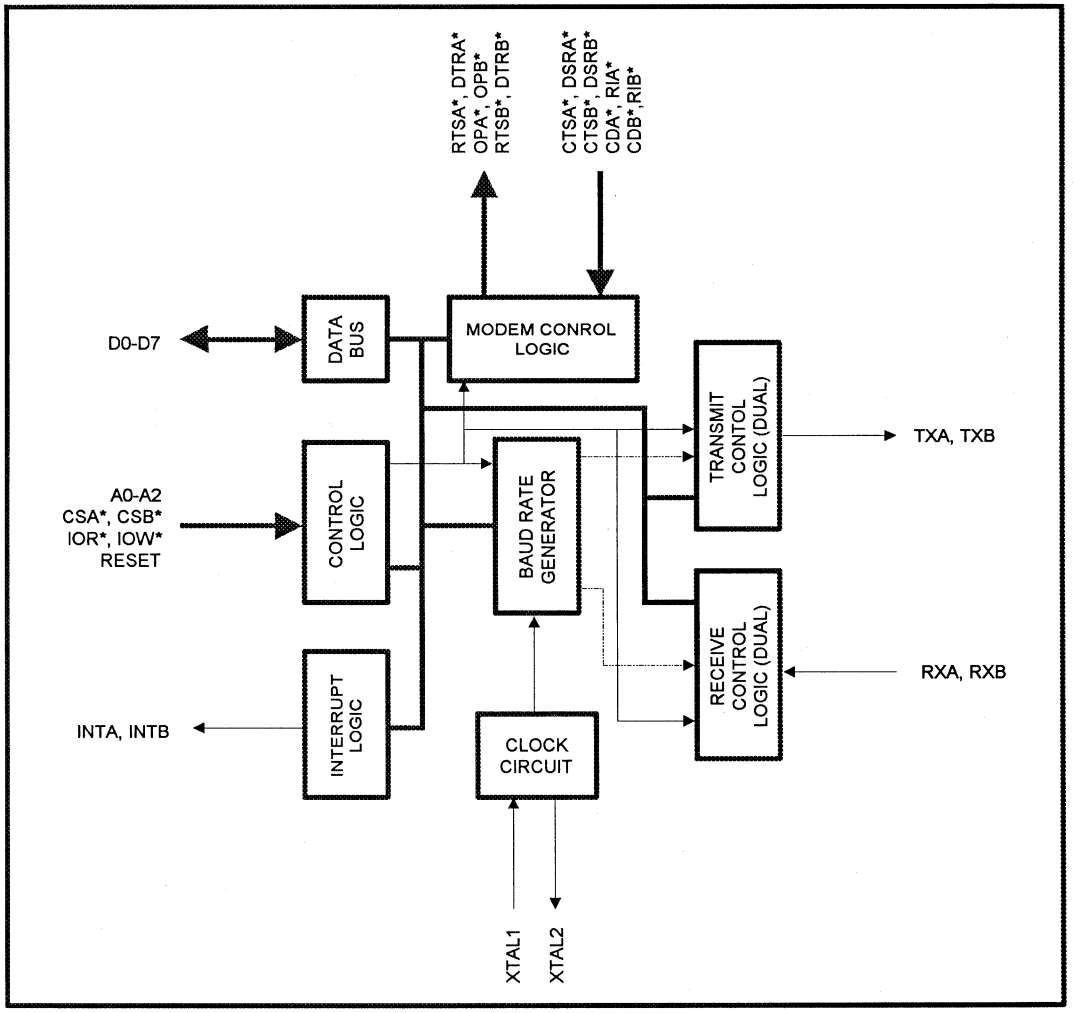
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C2450CP40	Plastic-DIP	0° C to + 70° C
ST16C2450CJ44	PLCC	0° C to + 70° C

***Industrial operating range are available**

ST16C2450

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	10,9	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A/B*	14,15	I	Chip select A/B. (active low) A low at this pin enables the ST16C2450 / CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2450 data bus to the CPU.
A0-A2	28-26	I	Address select lines. To select internal registers.
INT A/B	30,29	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

ST16C2450

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
OP2 A/B*	31	O	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
RTS A/B*	32,24	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A/B*	33,34	O	Data terminal ready A/B (active low). To indicate that ST16C2450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A/B*	36,25	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A/B*	37,22	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B*	38,19	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI A/B*	39,23	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
GND	20	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C2450

ST16C2450 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS A/B

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ST16C2450

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
not used except in local loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode and OP2* output to high.
1=set INT outout pin to normal operating mode and OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C2450 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2450 has changed state since the last time it was read.

ST16C2450

MSR BIT-1:
Indicates that the DSR* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2450 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state mode

ST16C2450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signal

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time			100	ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW*to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: *Baudout* cycle

ST16C2450

ST16C2450

ABSOLUTE MAXIMUM RATINGS

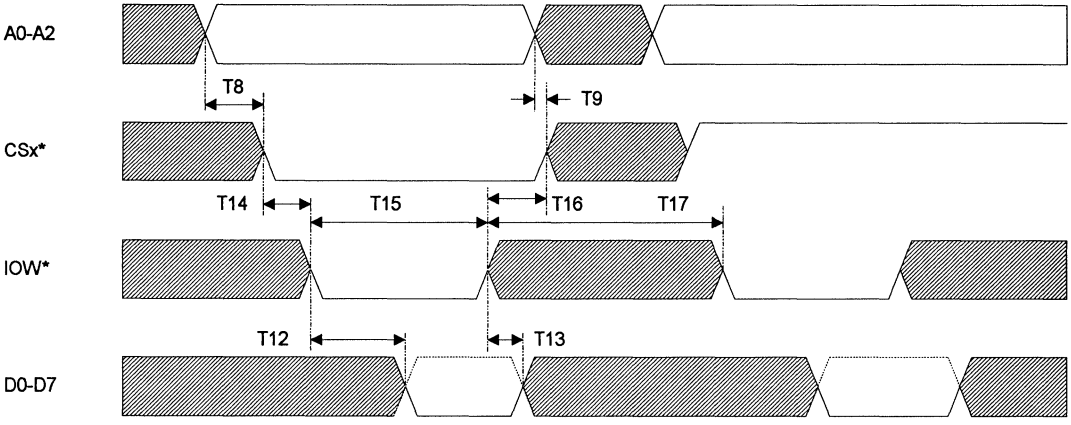
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

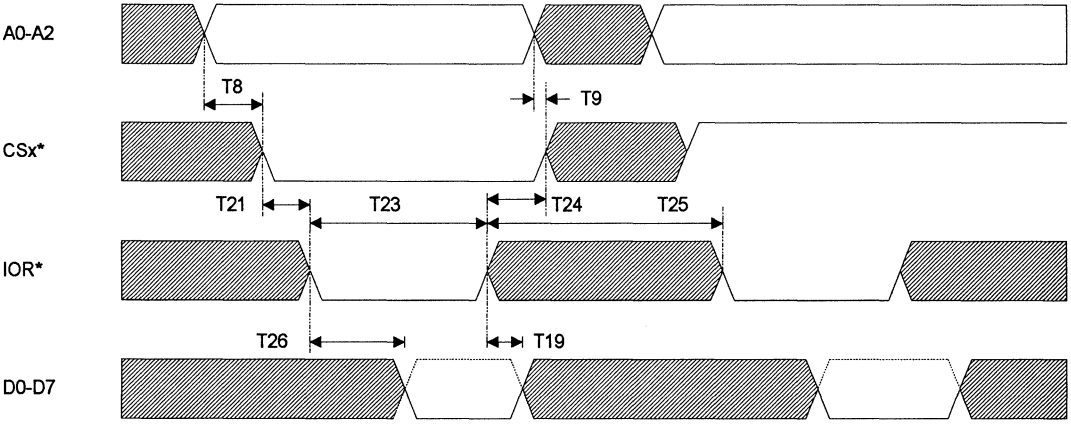
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING



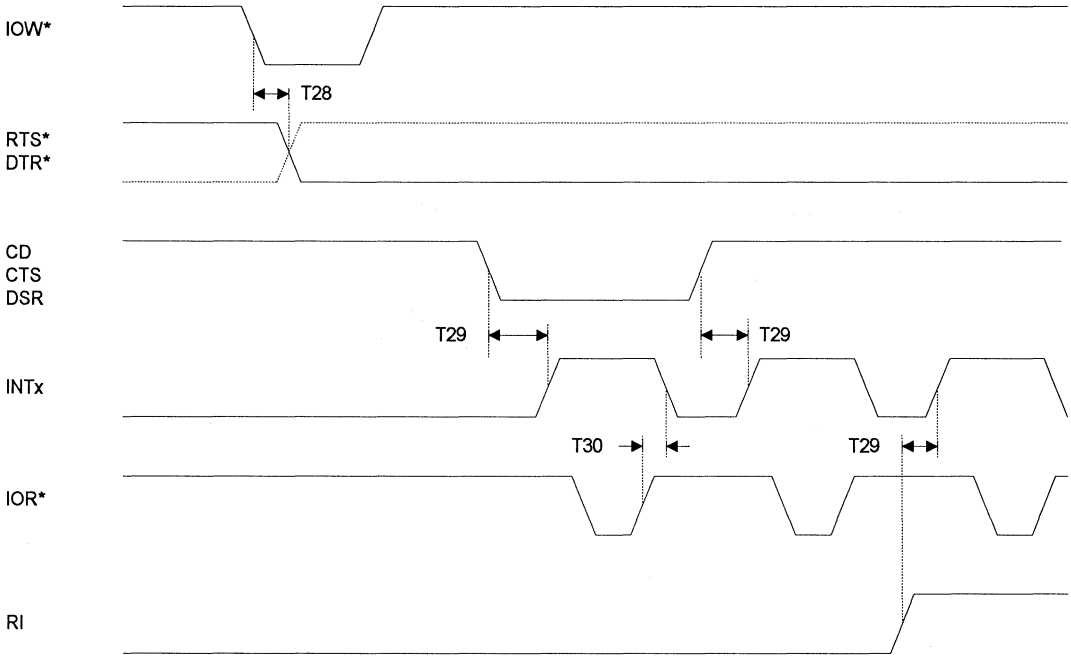
GENERAL READ TIMING



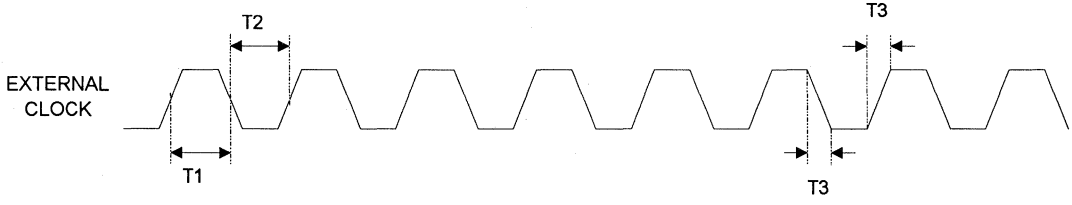
ST16C2450

ST16C2450

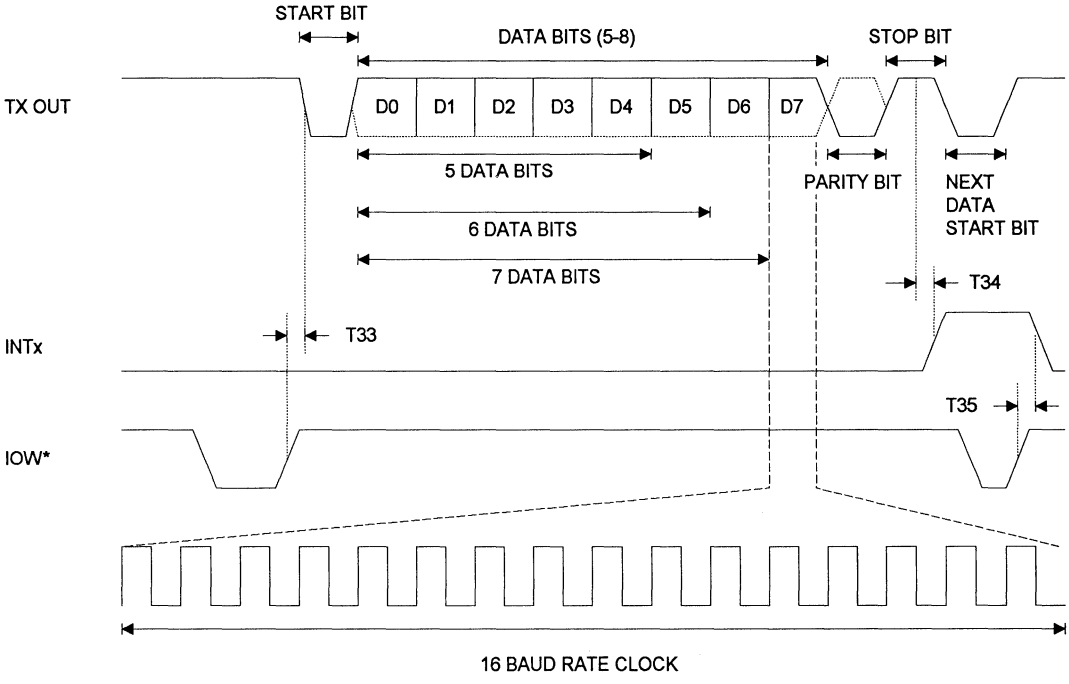
MODEM TIMING



CLOCK TIMING

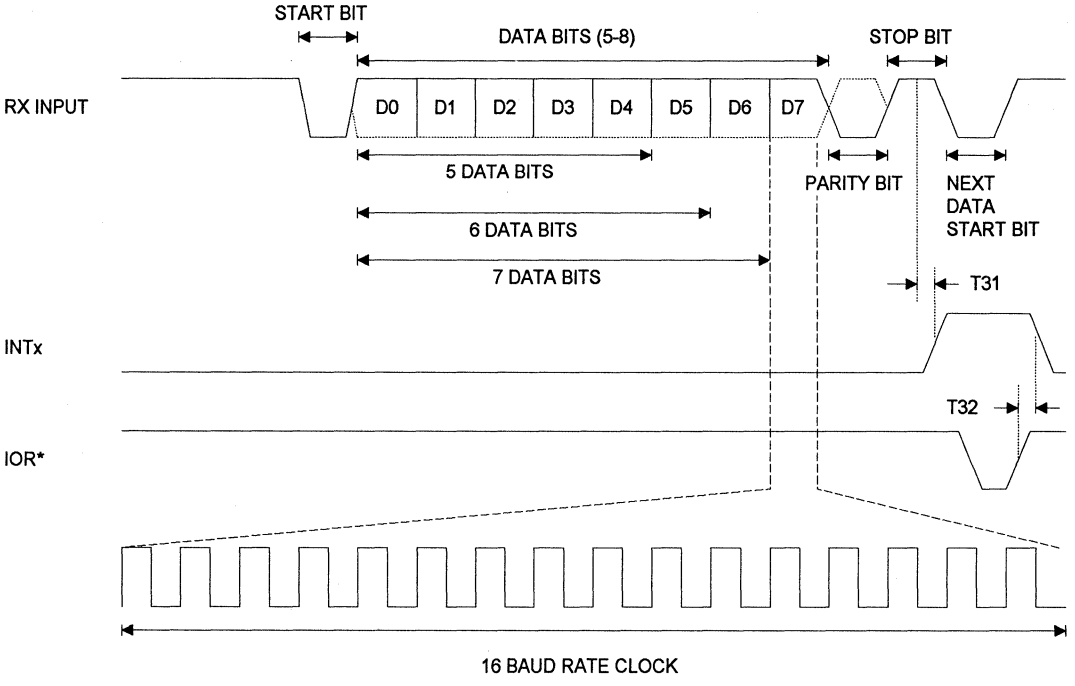


TRANSMIT TIMING



ST16C2450

RECEIVE TIMING



STARTECH

ST16C454

APR 1992

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

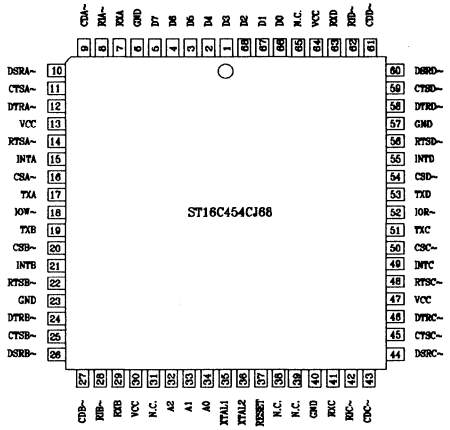
DESCRIPTION

The ST16C454 is a quad universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C454 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C454 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C454 provides internal loop-back capability for on board diagnostic testing.

The ST16C454 is fabricated in an advanced 1.2 µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

* Quad ST16C450
* Pin-to-pin compatible to ST16C554
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

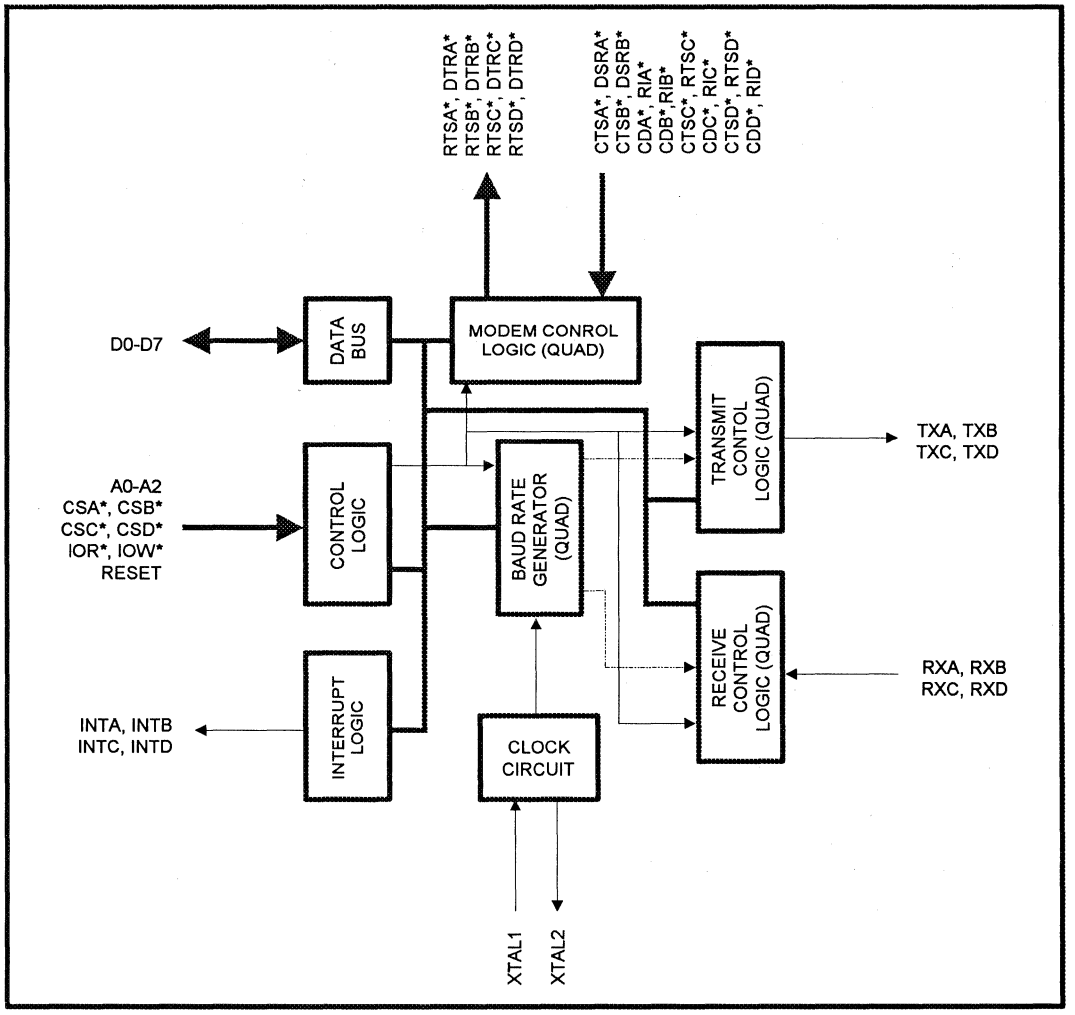
Part number	Package	Operating temperature
ST16C454CJ68	PLCC	0° C to + 70° C

***Industrial operating range available**

3

ST16C454

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input. The serial information (data) received from serial port to ST16C454 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A-B* CS C-D*	16,20 50,54	I	Chip select. (active low) A low at this pin enables the ST16C454 / CPU data transfer operation. Each UART section of the ST16C454 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,61	O	Signal and power ground.
IOR*	52	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C454 data bus to the CPU.

ST16C454

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A2	32	I	Address select line 2. To select internal registers.
A1	33	I	Address select line 1. To select internal registers.
A0	34	I	Address select line 0. To select internal registers.
INT A-B INT C-D	15,21 49,55	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS A-B* RTS C-D*	14,22 48,56	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A-B* DTR C-D*	12,24 46,58	O	Data terminal ready. (active low) To indicate that ST16C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A-B* CTS C-D*	11,25 45,59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A-B* DSR C-D*	10,26 44,60	I	Data set ready. (active low) A low on this pin indicates the

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD A-B* CD C-D*	9,27 43,61	I	MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation. Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI A-B* RI C-D*	8,28 42,62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13,60 47,64	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C454

ST16C454

ST16C454 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C454 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ST16C454

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used except, in internal loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C454 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C454 has changed state since the last time it was read.

ST16C454

MSR BIT-2:
Indicates that the RI* input to the ST16C454 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C454 provides a temporary data register to store 8 bits of information for variable use.

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time			100	ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{27}	IOR* to floating data delay	0		50	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1: *Baudout* cycle

ST16C454

ST16C454

ABSOLUTE MAXIMUM RATINGS

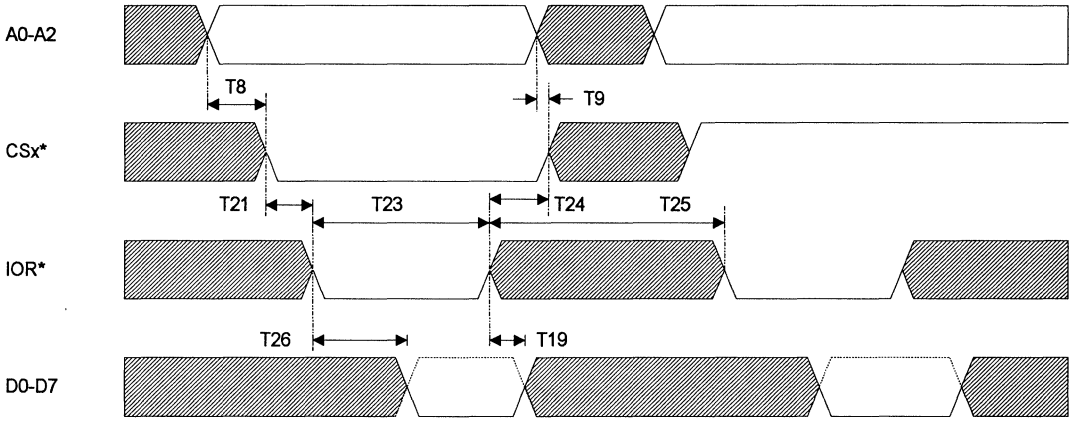
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

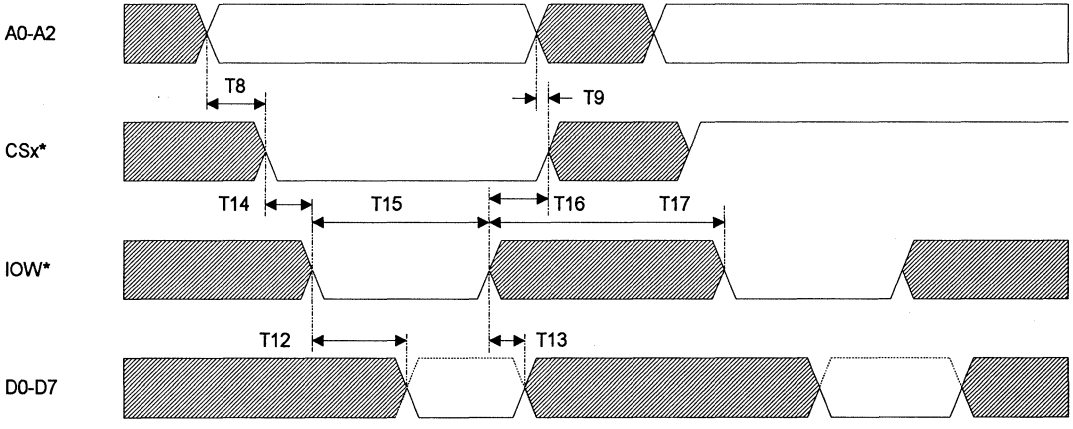
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL READ TIMING

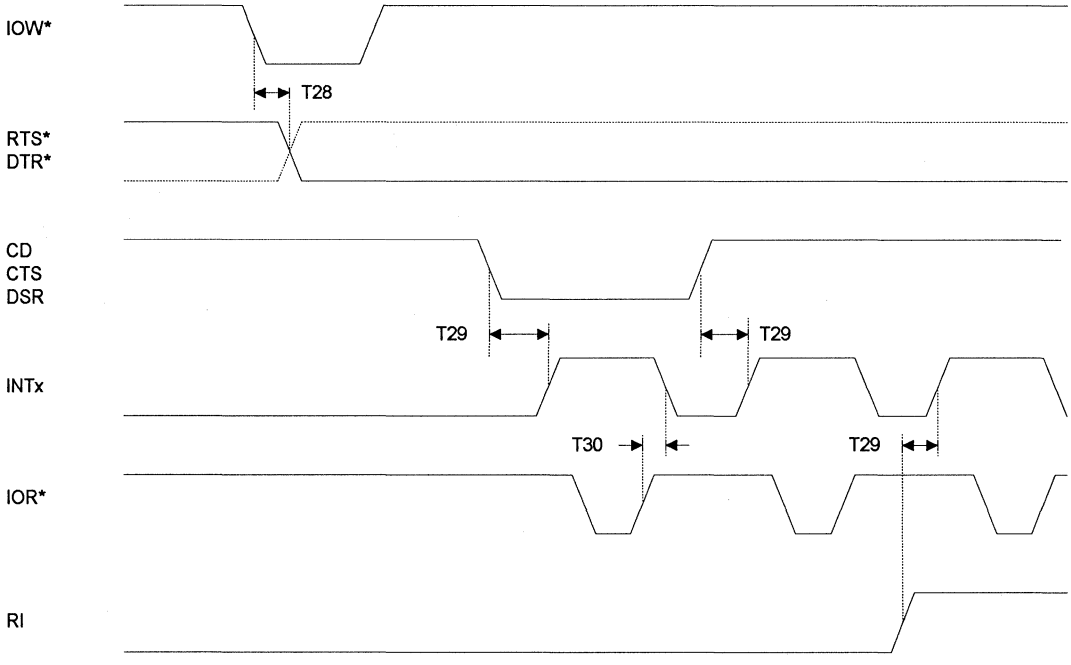


GENERAL WRITE TIMING

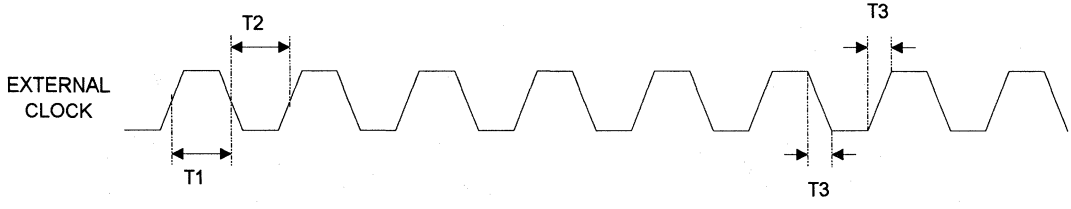


ST16C454

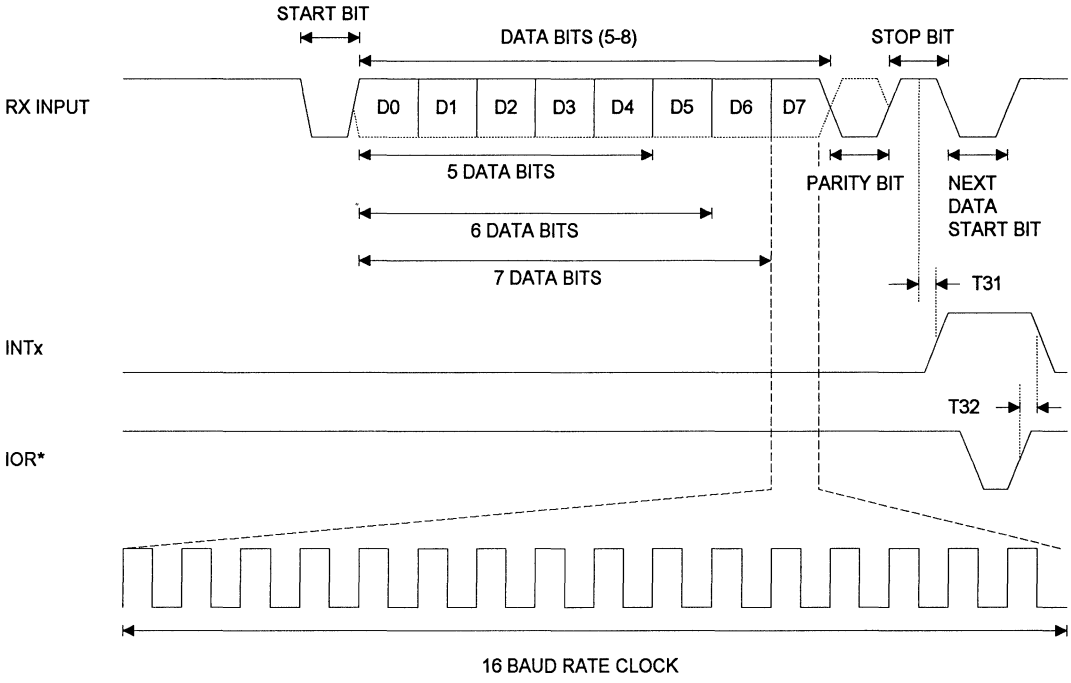
MODEM TIMING



CLOCK TIMING

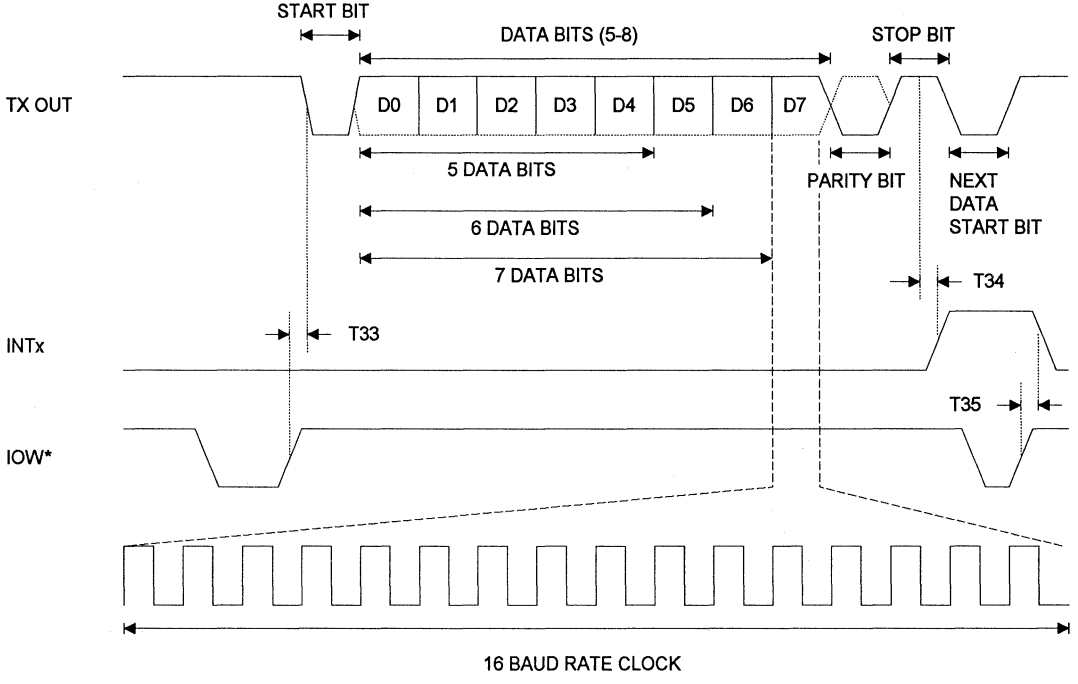


RECEIVE TIMING



ST16C454

TRANSMIT TIMING



STARTECH

ST16C550

APR 1992

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

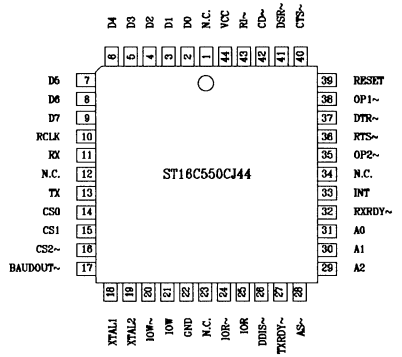
DESCRIPTION

The ST16C550 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

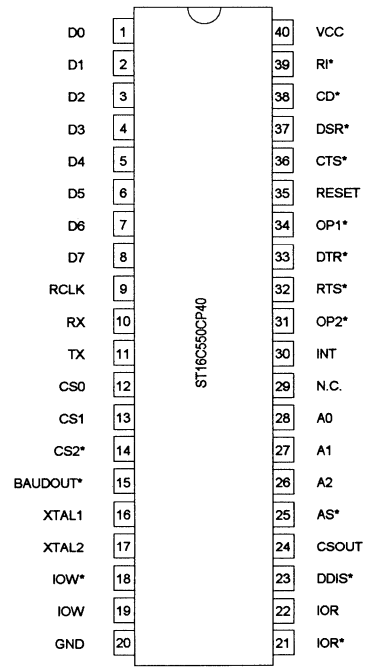
The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loopback capability for on board diagnostic testing.

The ST16C550 is fabricated in an advanced 1.2 µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

* Pin to pin and functional compatible to NS16550, VL16C550, WD16C550
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Software compatible with INS8250, NS16C450
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

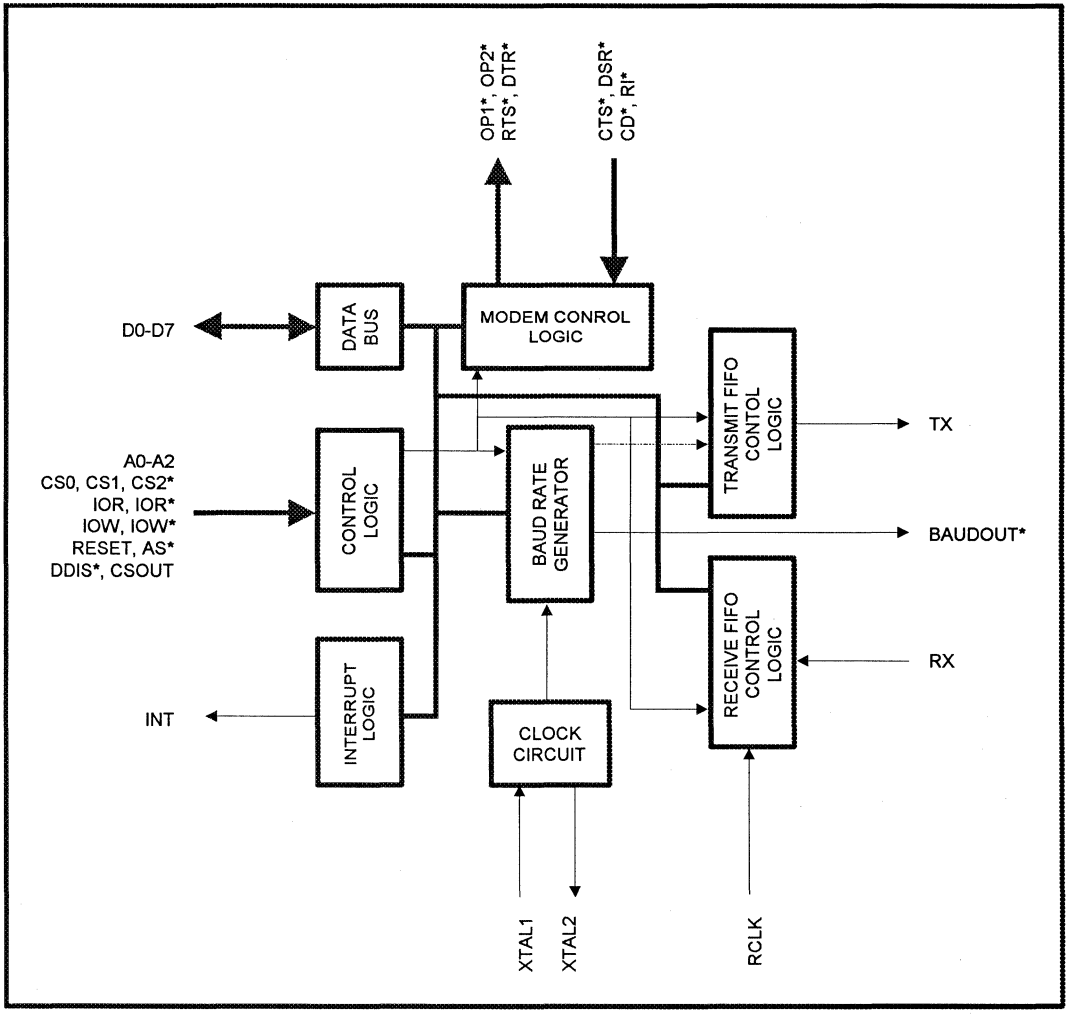
Part number	Package	Operating temperature
ST16C550CP40	Plastic-DIP	0° C to + 70° C
ST16C550CJ44	PLCC	0° C to + 70° C

***Industrial operating range are available**

3

ST16C550

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RCLK	9	I	Receive clock input. The external clock input to the ST16C550 receiver section if receiver data rate is different from transmitter data rate.
RX	10	I	Serial data input. The serial information (data) received from serial port to ST16C550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	11	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
CS1	13	I	Chip select 2. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
CS2*	14	I	Chip select 3. (active low) A low at this pin (while CS0=1 and CS1=1) will enable the ST16C550 / CPU data transfer operation.
BAUDOUT*	15	O	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide receive clock.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

ST16C550

ST16C550

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOW	19	I	Write strobe. (active high) Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C550 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	O	Signal and power ground.
IOR*	21	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C550 data bus to the CPU.
IOR	22	I	Read strobe. (active high) Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C550 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23	O	Drive disable. (active low) This pin goes low when the CPU is reading data from the ST16C550 to disable the external transceiver or logics.
TXRDY*	24	O	Transmit ready. (active low) This pin goes low when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.
AS*	25	I	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2	26	I	Address select line 2. To select internal registers.
A1	27	I	Address select line 1. To select internal registers.
A0	28	I	Address select line 0. To select internal registers.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
RXRDY*	29	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INT	30	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	O	General purpose output. (active low) User defined output. See bit-3 modem control register (MCR bit-3).
RTS*	32	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	O	Data terminal ready. (active low) To indicate that ST16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	O	General purpose output. (active low) User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	37	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.

ST16C550

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD*	38	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI*	39	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	I	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C550

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16} - 1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receive time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

ST16C550

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:
0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

ST16C550

MSR BIT-0:
Indicates that the CTS* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
RXRDY*	High
TXRDY*	High
INT	Low

SCRATCHPAD REGISTER (SR)

ST16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time			100	ns	
T_4	Baud out rise/fall ftime			100	ns	100 pF load
T_5	Address strobe width	30			ns	
T_6	Address setup time	30			ns	
T_7	Address hold time	5			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{10}	CSOUT delay from chip select	10			ns	
T_{11}	IOR* to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW*	5			ns	Note: 1
T_{13}	IOW* delay from address	25			ns	Note: 1
T_{14}	IOW* delay from chip select	10			ns	Note: 1
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	Note: 1
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{18}	Data setup time	10			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	Note: 1
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	Note: 1
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{27}	IOR* to floating data delay	0		50	ns	100 pF load

3

ST16C550

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{RCIK}		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: Applicable only when AS* is tied low
Baudout cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

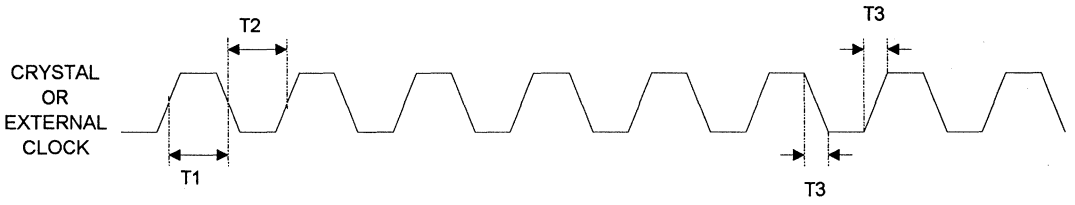
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

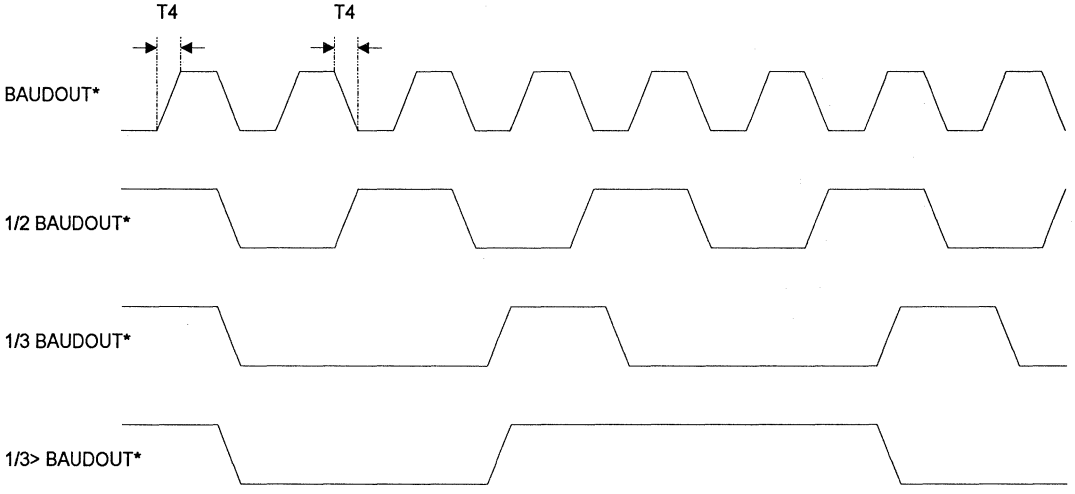
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST16C550

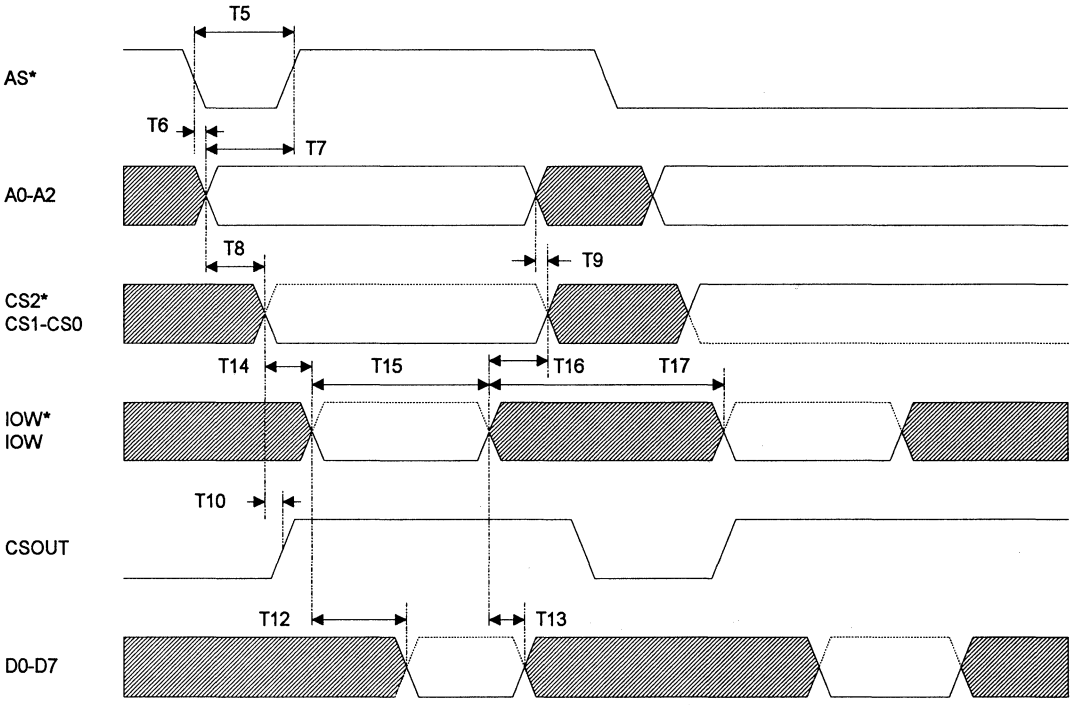
CLOCK TIMING



BAUDOUT* TIMING

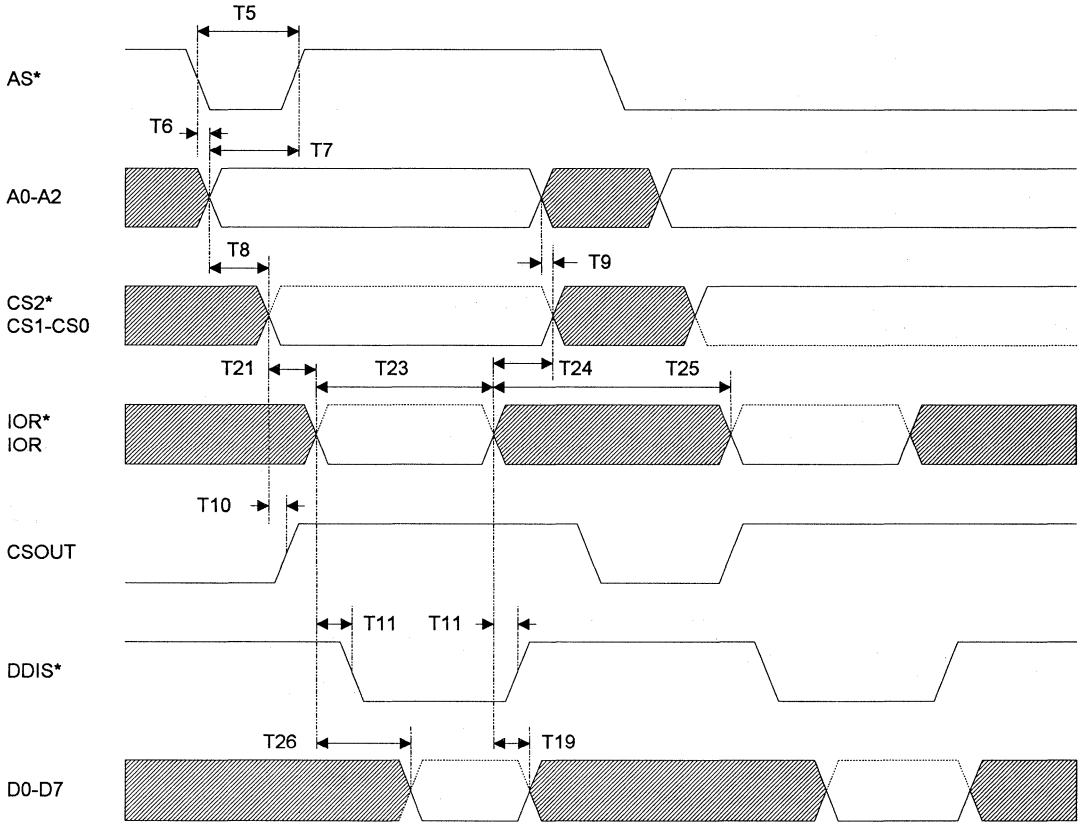


GENERAL WRITE TIMING

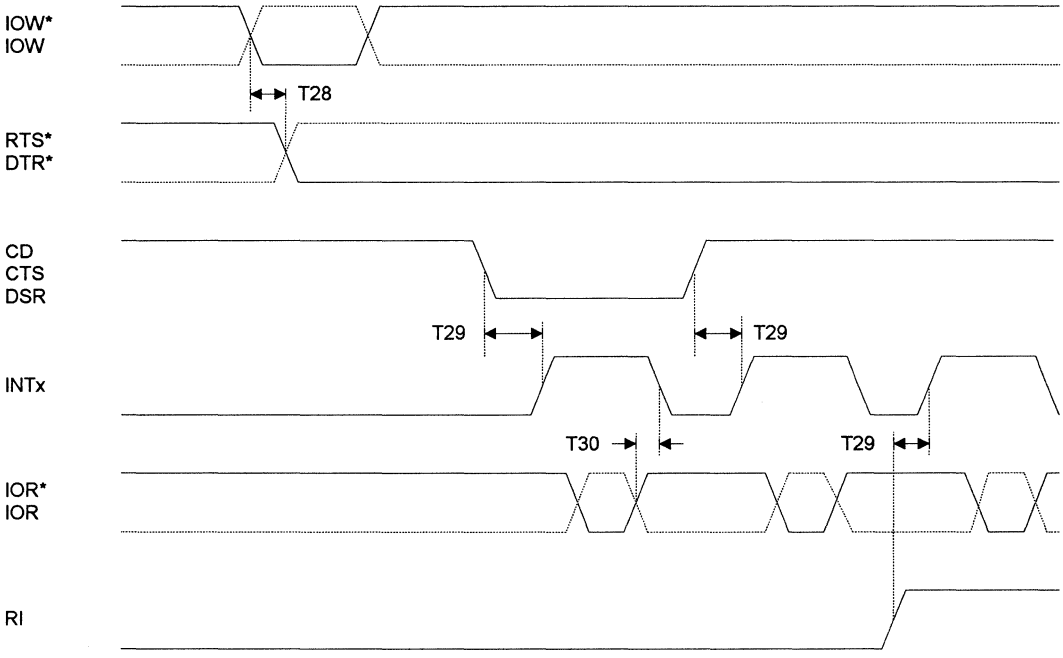


ST16C550

GENERAL READ TIMING

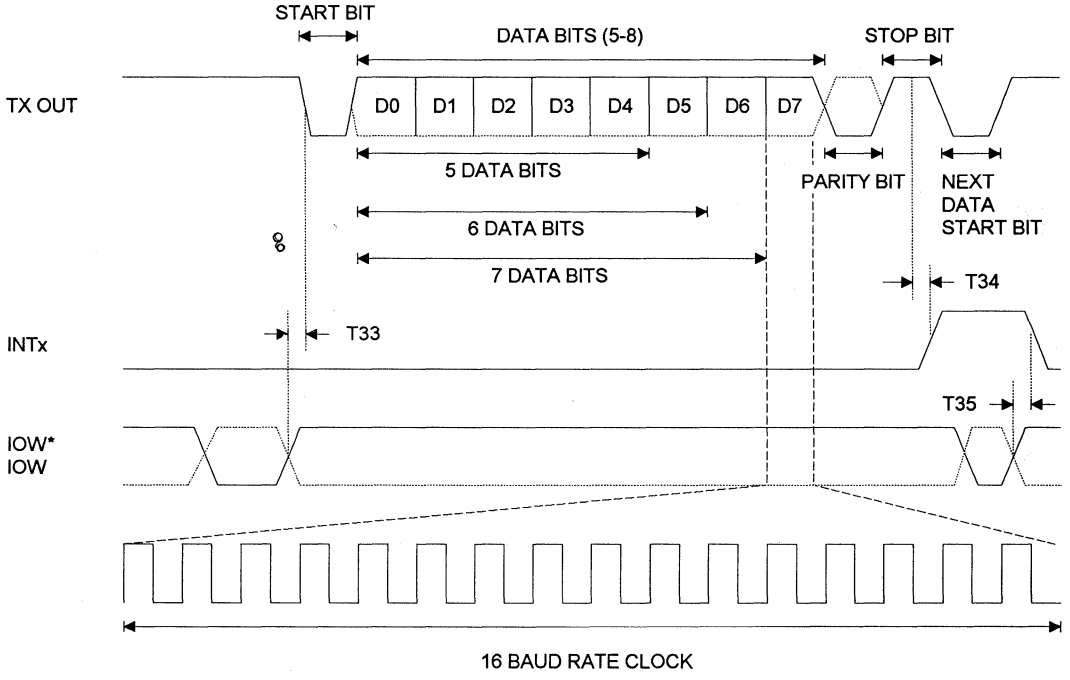


MODEM TIMING

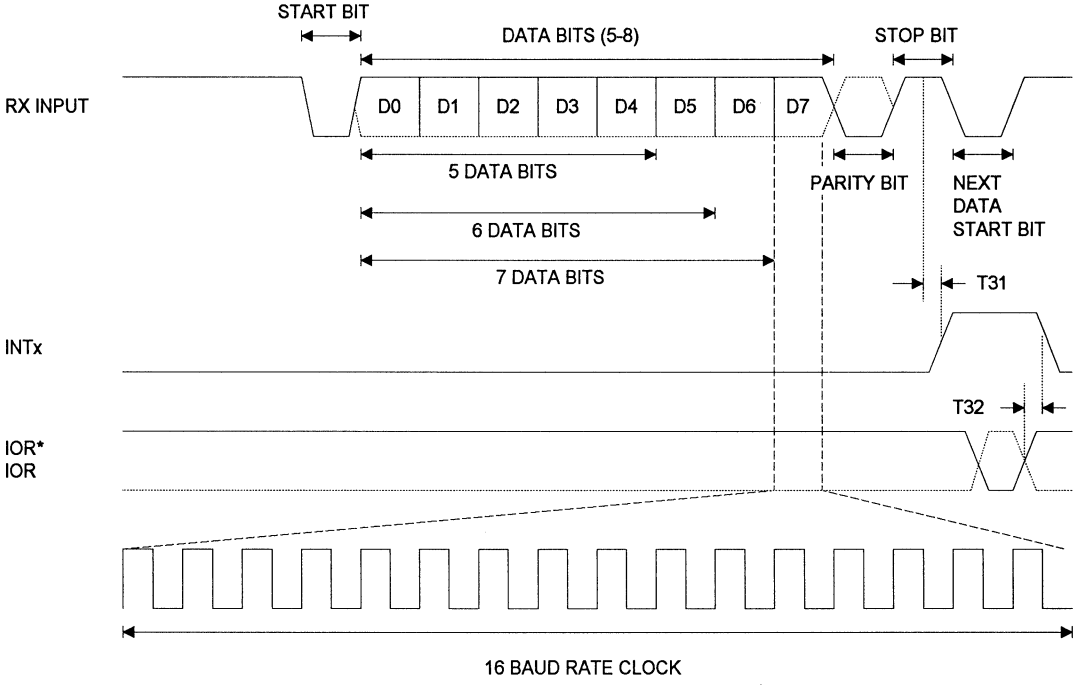


ST16C550

TRANSMIT TIMING

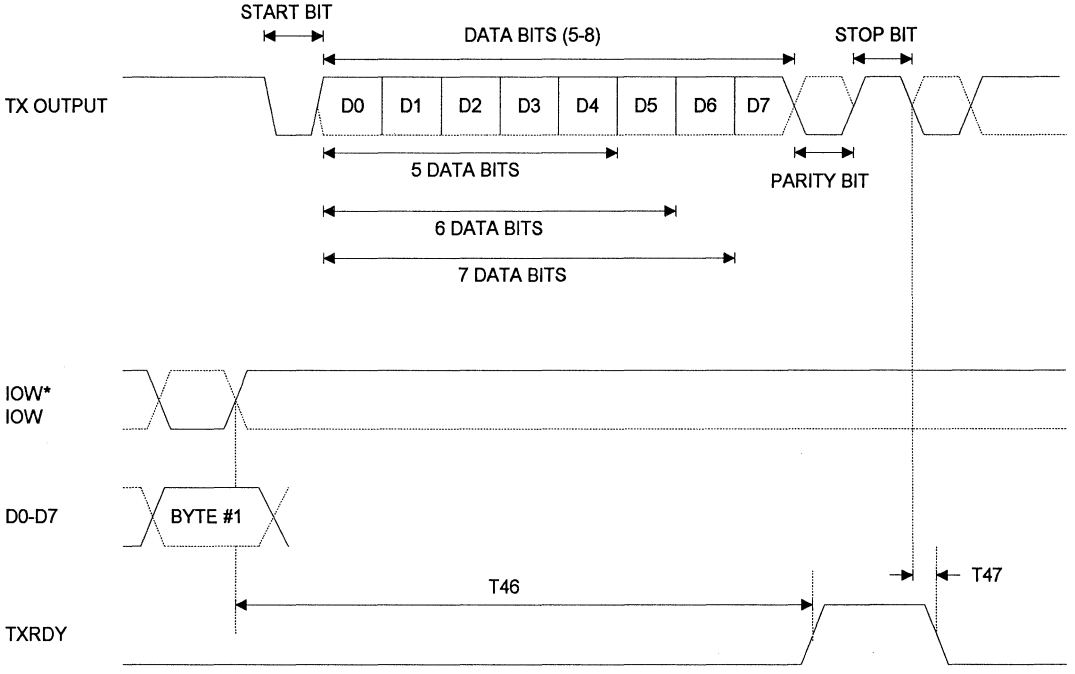


RECEIVE TIMING

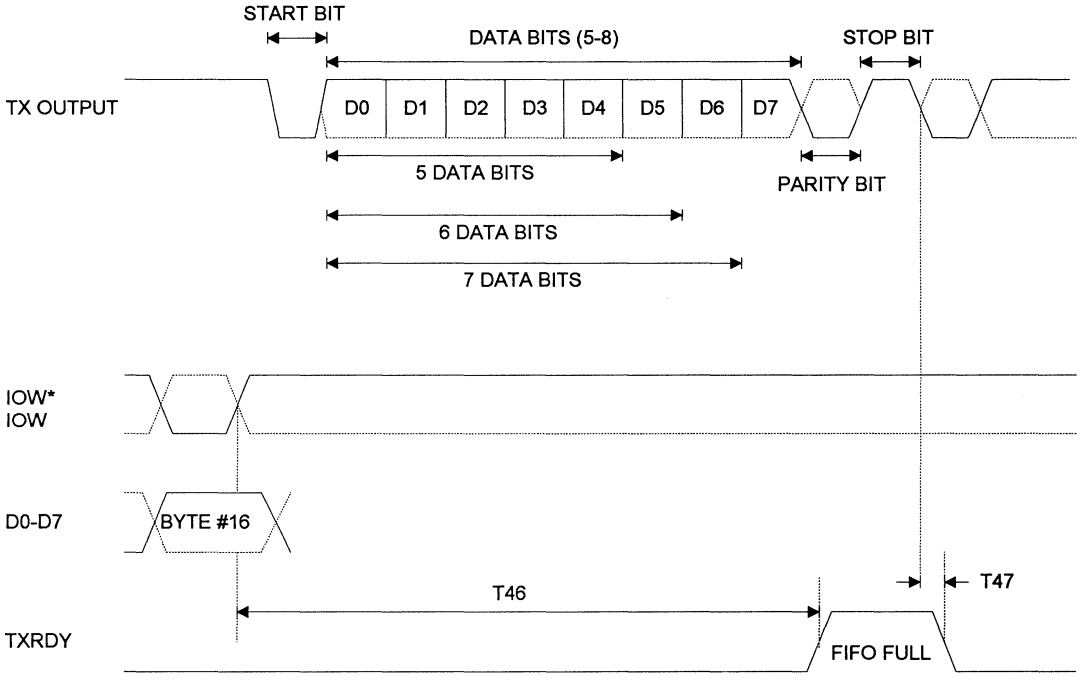


ST16C550

TXRDY TIMING FOR MODE "0"

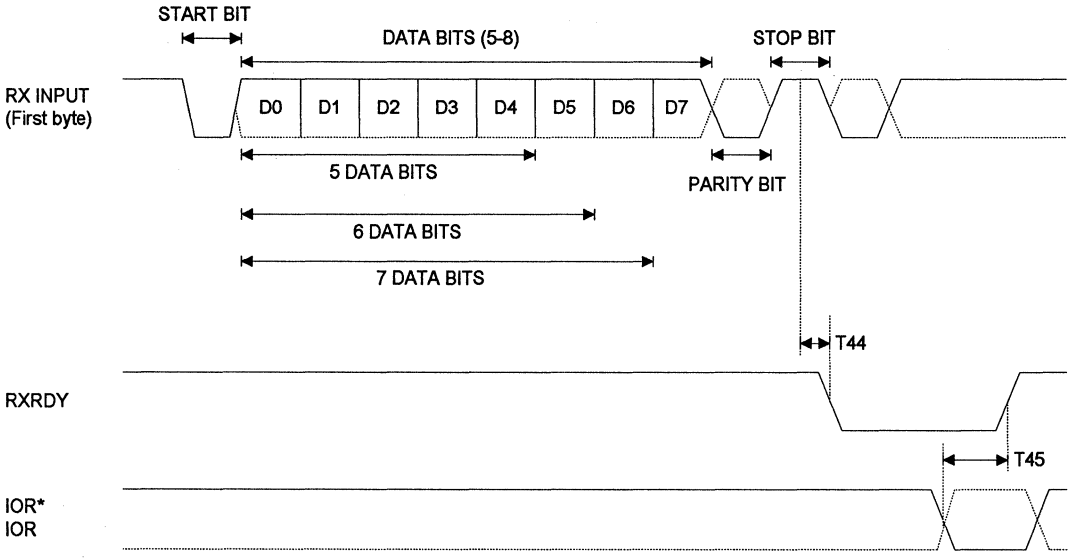


TXRDY TIMING FOR MODE "1"

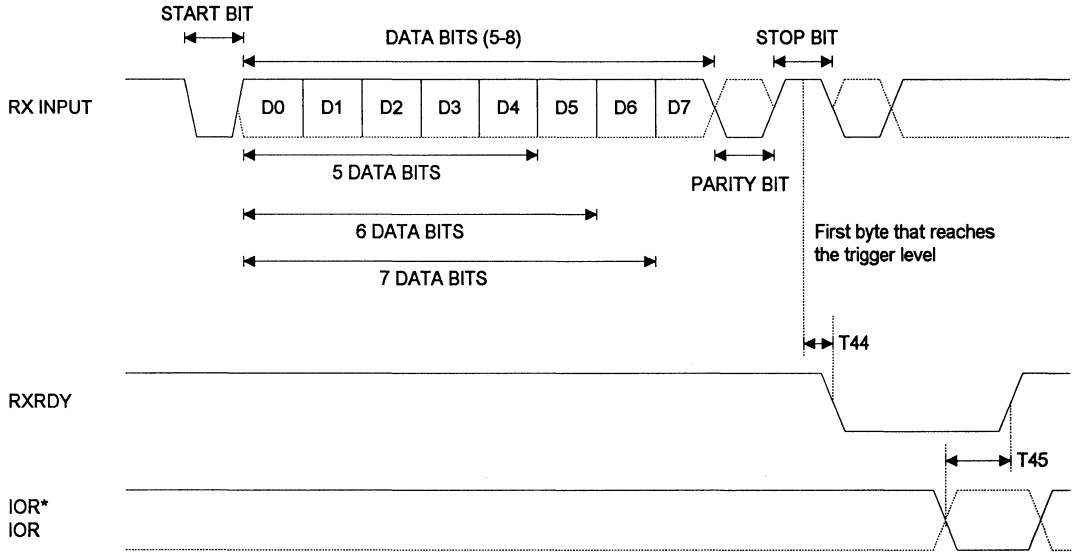


ST16C550

RXRDY TIMING FOR MODE "0"



RXRDY TIMING FOR MODE "1"



ST16C550

STARTECH

ST16C1550
ST16C1551

APR 1992

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

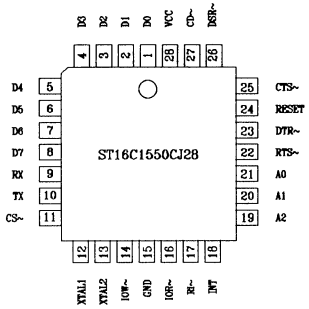
DESCRIPTION

The ST16C1550/51 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1550/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1550/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1550/51 provides internal loop-back capability for on board diagnostic testing.

The ST16C1550/51 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package

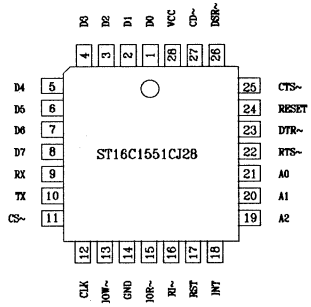


ST16C1550

FEATURES

* Pin to pin and functional compatible to SSI 73M1550/2550
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Software compatible with INS8250, NS16C550
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
* 28 Pin plastic-Dip and PLCC package
* Pin-to-pin compatible to ST16C1450/1451

PLCC Package



ST16C1551

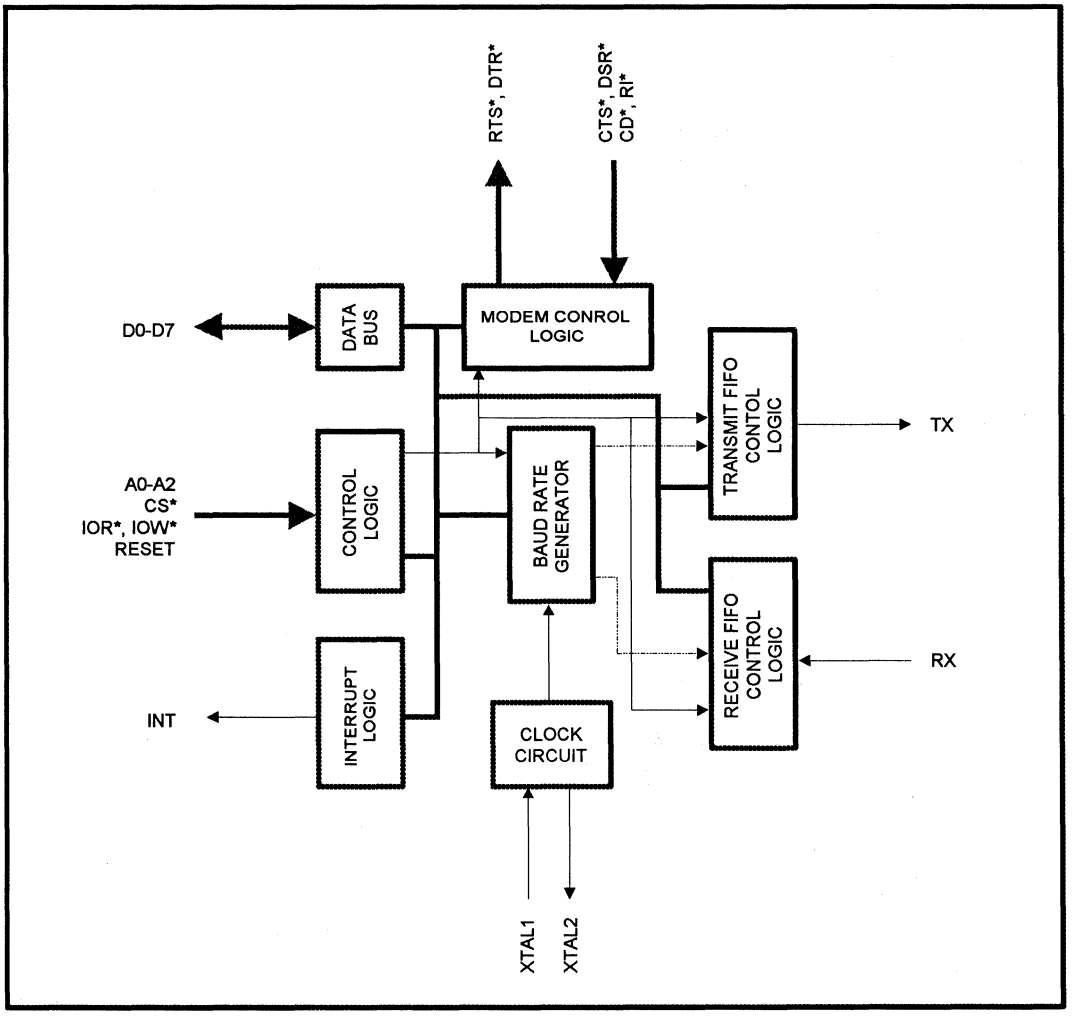
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C1550CP28	Plastic-DIP	0° C to + 70° C
ST16C1550CJ28	PLCC	0° C to + 70° C
ST16C1551CP28	Plastic-Dip	0° C to + 70° C
ST16C1551CJ28	PLCC	0° C to + 70° C

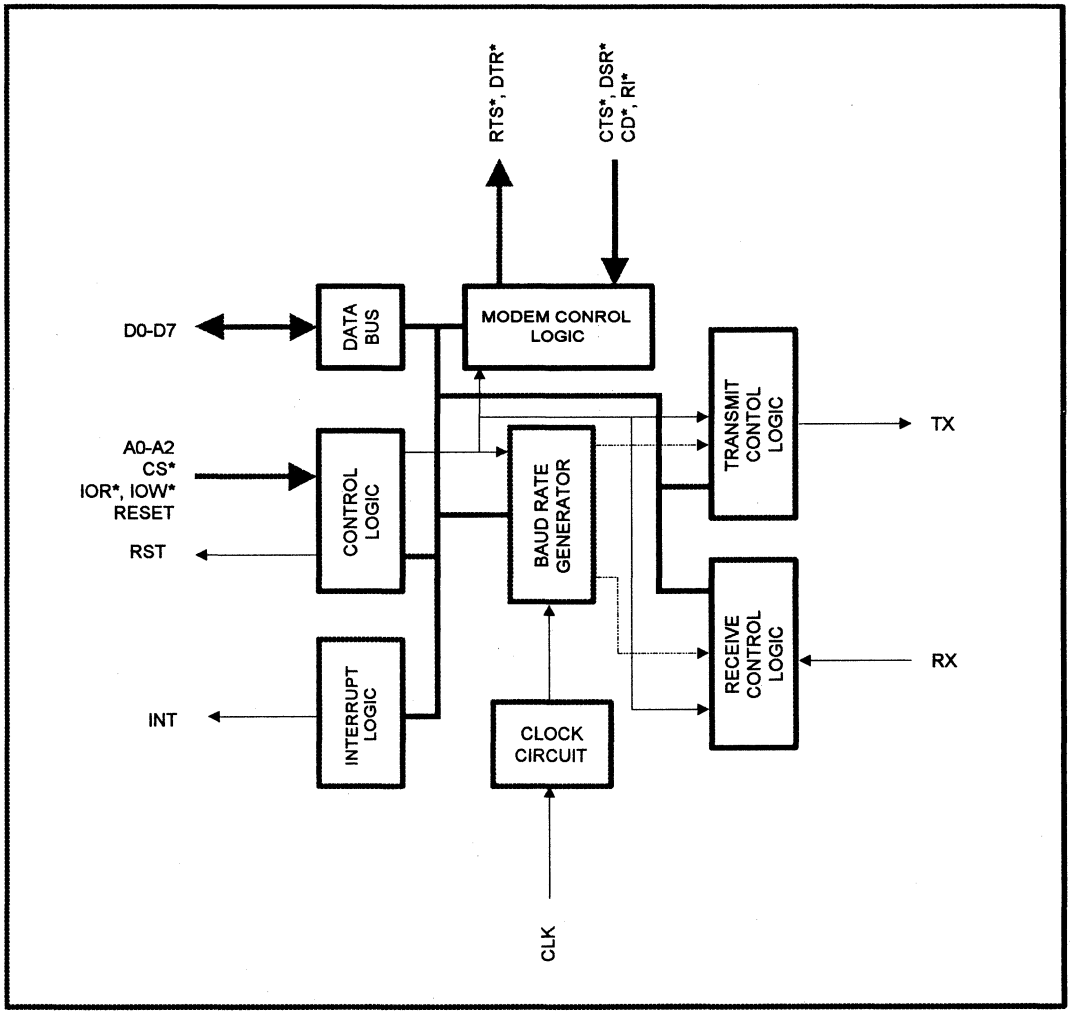
***Industrial operating range are available**

ST16C1550
ST16C1551

ST16C1550 BLOCK DIAGRAM



ST16C1551 BLOCK DIAGRAM



ST16C1550
ST16C1551

ST16C1550 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1550 / CPU data transfer operation.
XTAL1	12	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	O	Signal and power ground.
IOR*	16	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1550 data bus to the CPU..
RI*	17	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
INT	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a

ST16C1550 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
RTS*	22	O	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	O	Data terminal read (active low). To indicate that ST16C1550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	I	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	I	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1550
ST16C1551

ST16C1551 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	I	Serial data input. The serial information (data) received from serial port to ST16C1551 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX	10	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11	I	Chip select (active low). A low at this pin enables the ST16C1551 / CPU data transfer operation.
CLK	12	I	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
IOW*	13	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	14	O	Signal and power ground.
IOR*	15	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1551 data bus to the CPU..
RI*	16	I	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
RST	17	O	Reset output (active high). The ST16C1551 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	O	Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a

ST16C1551 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	I	Address select line. To select internal registers.
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DSR*	26	I	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	I	Power supply input.

ST16C1550
ST16C1551

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C1550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0/ special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0 / TX trigger (MSB)	0 / TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0 / FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C1550
ST16C1551

ST16C1551 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0 / special mode	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0 / FIFOs enabled	0 / FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0	0	loop back	INT enable	SOFT reset	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C1550/51 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C1550/51 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1550/51 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT

output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1550/51 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1550/51 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receive time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3:
This bit is used with conjunction of ISR bit 0-2:
0=normal interrupt mode
1=receive timeout indicator when priority level is set to "2" (D0=0, D1=0, and D2=1)

ISR bit-4:
This bit is the compliment of TXRDY* (ST16C550) pin.
0=transmitter is full
1=transmitter is empty or less than full

ISR bit-5:
This bit is the compliment of RXRDY* (ST16C550) pin.
0=receiver is empty.
1=receiver is not empty

ISR bit-6-7:
0=16C450 mode
1=16C550 mode

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be nabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
These bits are used to set the transmit trigger levels.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-6:
Not used. Are set to zero permanently.

MCR bit-7:
0=normal mode.
1=power down mode. CLK, XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C1550/51 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C1550/51 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C1550/51 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C1550/51 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C1550/51 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1550/51 provides a temporary data register to store 8 bits of information for variable use.

ST16C1550
ST16C1551

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state

ST16C1550/51 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time			100	ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	

Note 1: *Baudout* cycle

ST16C1550
ST16C1551

ABSOLUTE MAXIMUM RATINGS

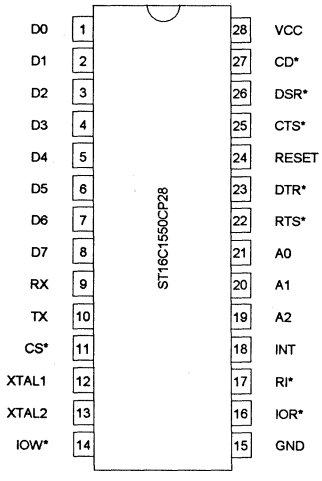
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

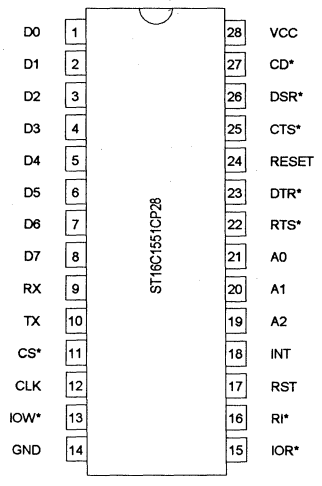
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

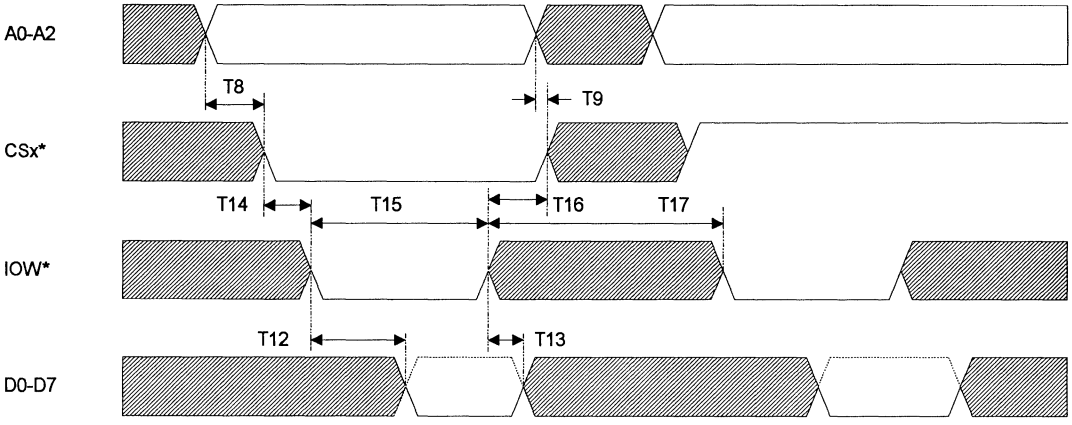
28 PIN PLASTIC-DIP ST16C1550



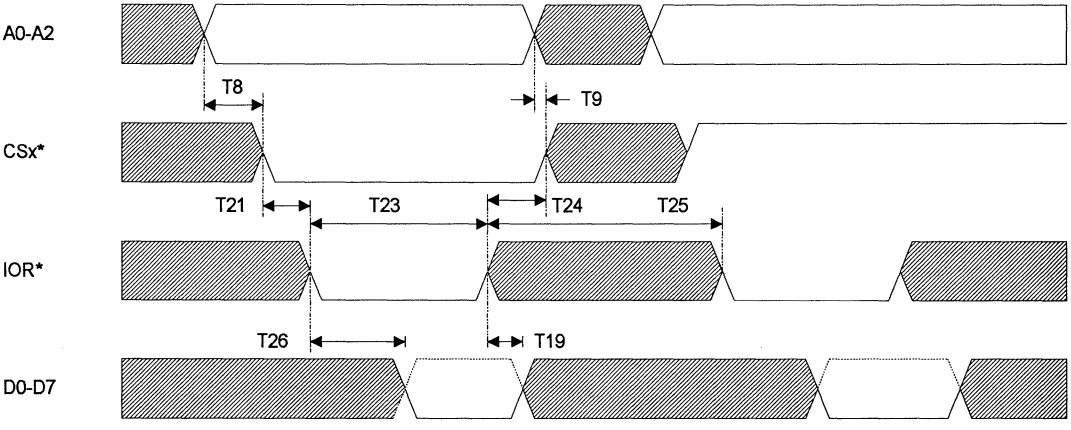
28 PIN PLASTIC-DIP ST16C1551



GENERAL WRITE TIMING

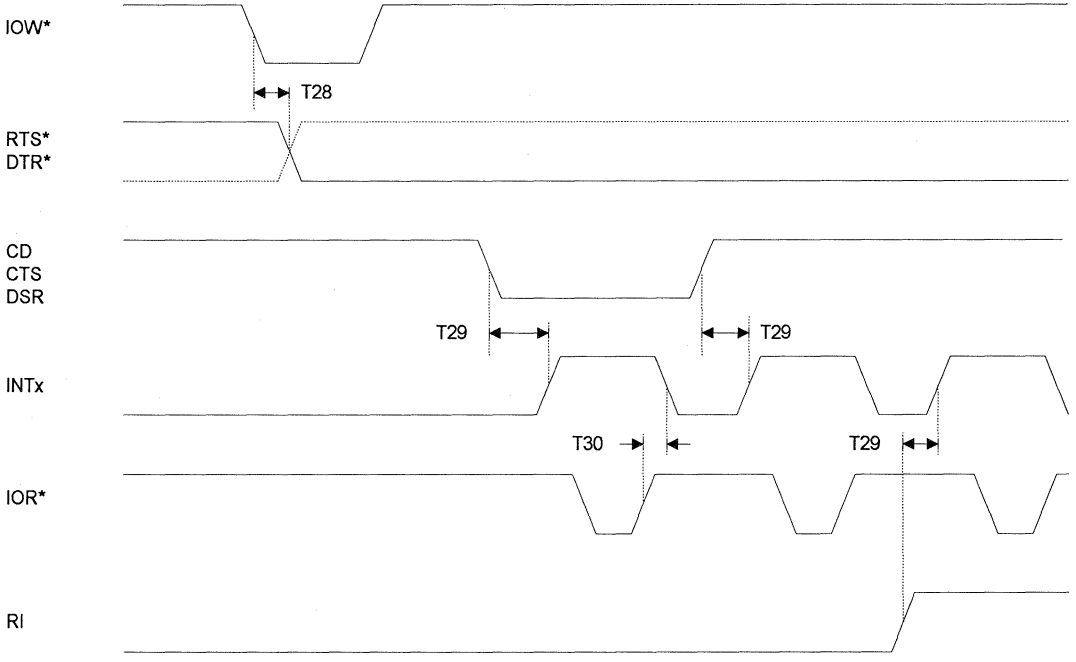


GENERAL READ TIMING

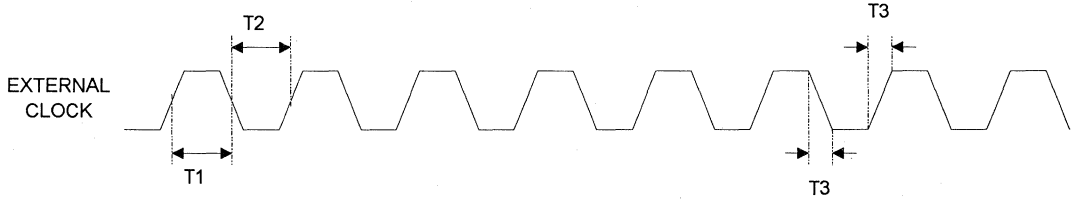


ST16C1550
ST16C1551

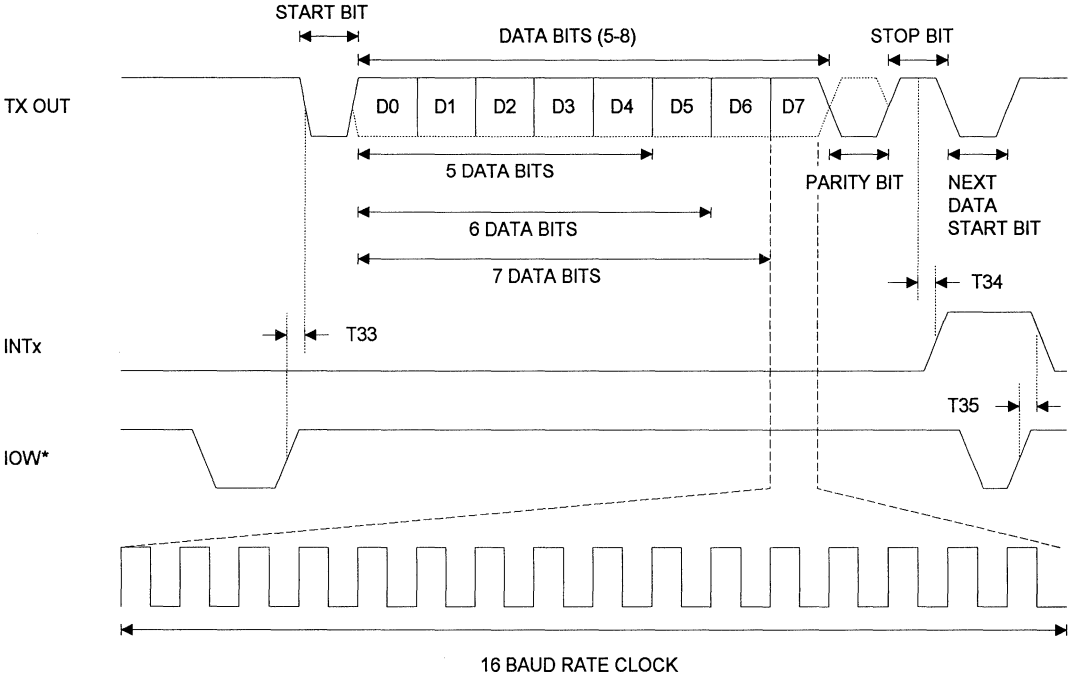
MODEM TIMING



CLOCK TIMING

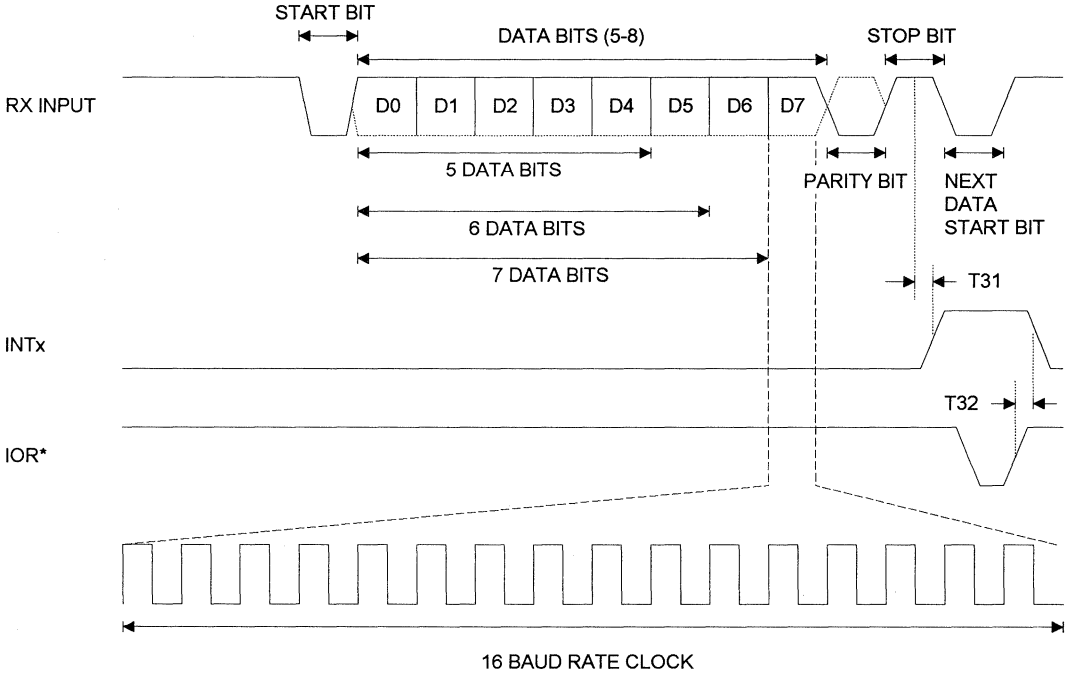


TRANSMIT TIMING



ST16C1550
ST16C1551

RECEIVE TIMING



STARTECH

ST16C2550

APR 1992

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

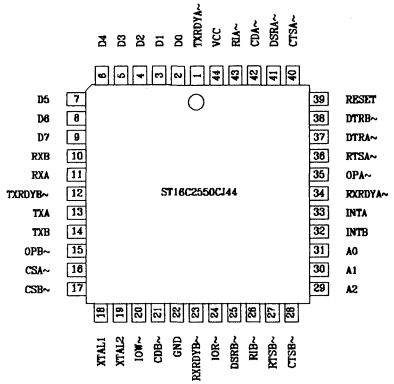
DESCRIPTION

The ST16C2550 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each uart.

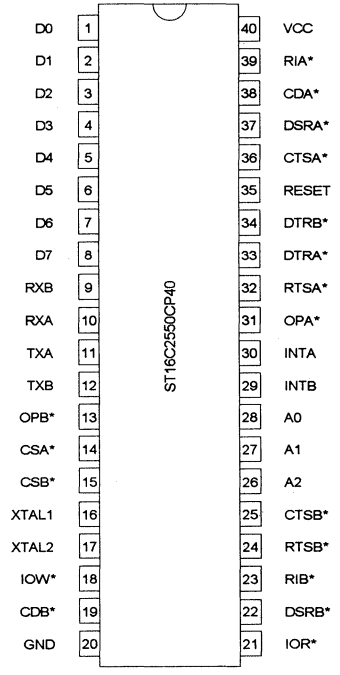
The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C2550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2550 provides internal loop-back capability for on board diagnostic testing.

The ST16C2550 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



Plastic-DIP Package



FEATURES

* Pin to pin and functional compatible to ST16C2550
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Software compatible with INS8250, NS16C550
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

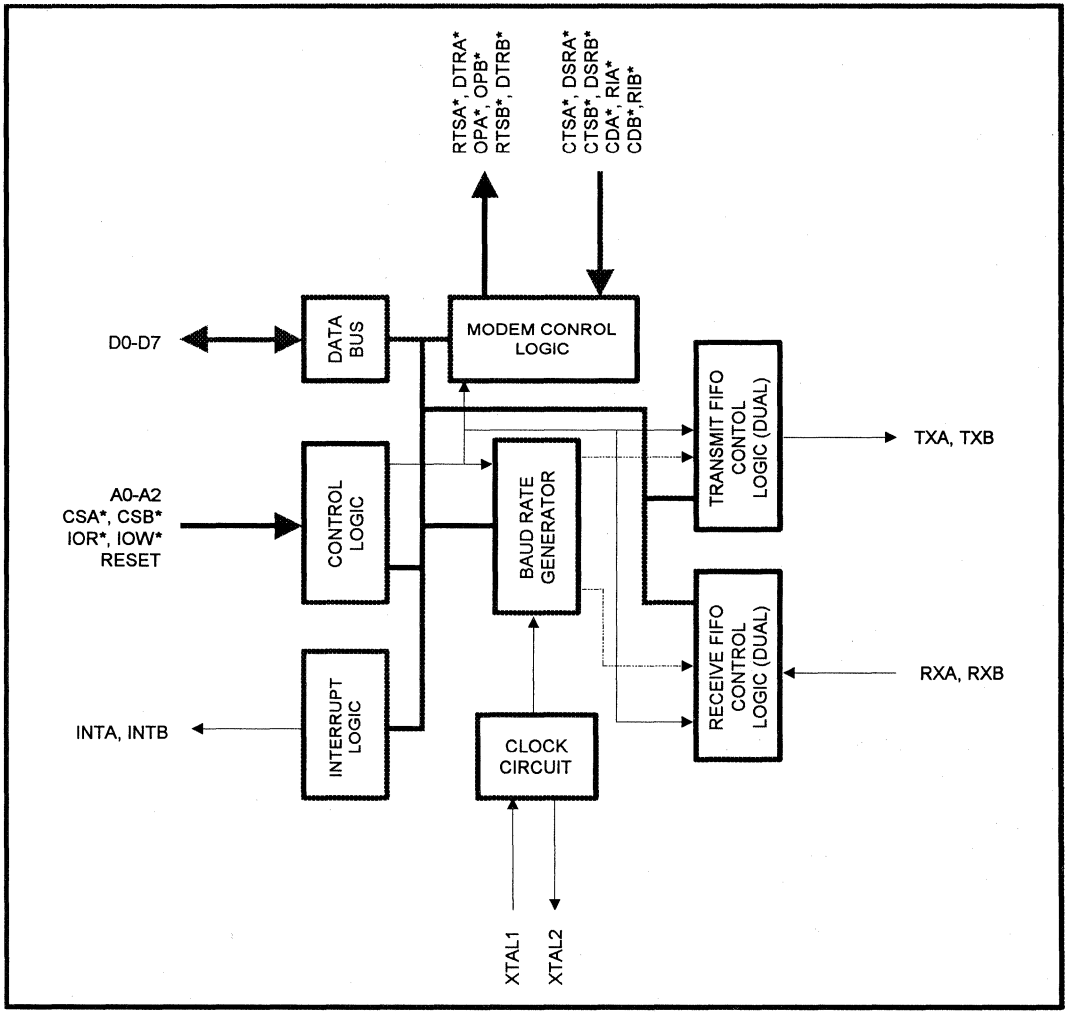
Part number	Package	Operating temperature
ST16C2550CP40	Plastic-DIP	0° C to + 70° C
ST16C2550CJ44	PLCC	0° C to + 70° C

***Industrial operating range are available**

3

ST16C2550

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	10,9	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A/B*	14,15	I	Chip select A/B. (active low) A low at this pin enables the ST16C2550 / CPU data transfer operation.
XTAL1	16	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	I	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2550 data bus to the CPU.
A0-A2	28-26	I	Address select lines. To select internal registers.
INT A/B	30,29	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

ST16C2550

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
OP2 A/B*	31	O	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
RTS A/B*	32,24	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A/B*	33,34	O	Data terminal ready A/B (active low). To indicate that ST16C2550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	35	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS A/B*	36,25	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A/B*	37,22	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B*	38,19	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI A/B*	39,23	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
VCC	40	I	Power supply input.
GND	20	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C2550

ST16C2550 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not uesed	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C2550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT

ST16C2550

output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receive time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C2550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be nabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

ST16C2550

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used exept in local loop-back mode.

MCR BIT-3:
0=set INT output pin to three state mode and OP2* output to high.
1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C2550 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a

control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C2550 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Three state mode

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C2550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

ST16C2550

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time	10			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{22}	IOR* delay from chip select	10			ns	
T_{21}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{36}	Delay from initial Write to interrupt	16		24	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: *Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

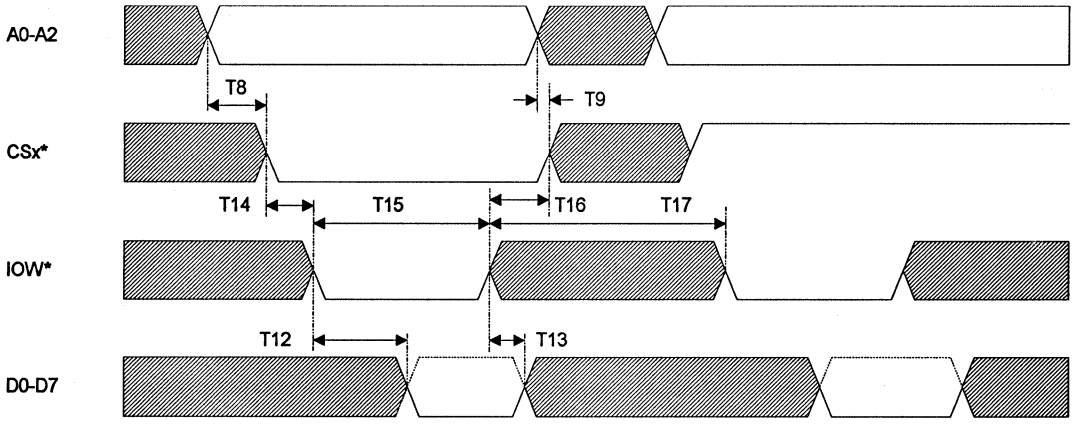
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

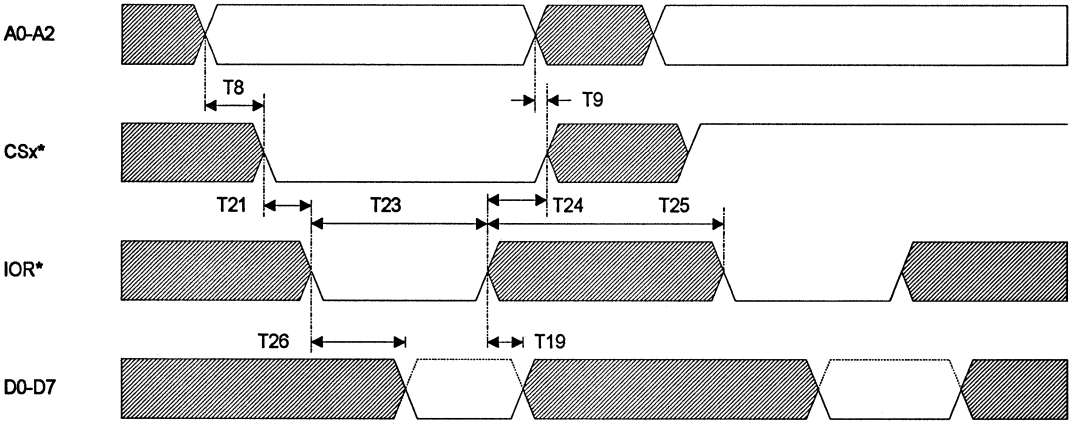
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST16C2550

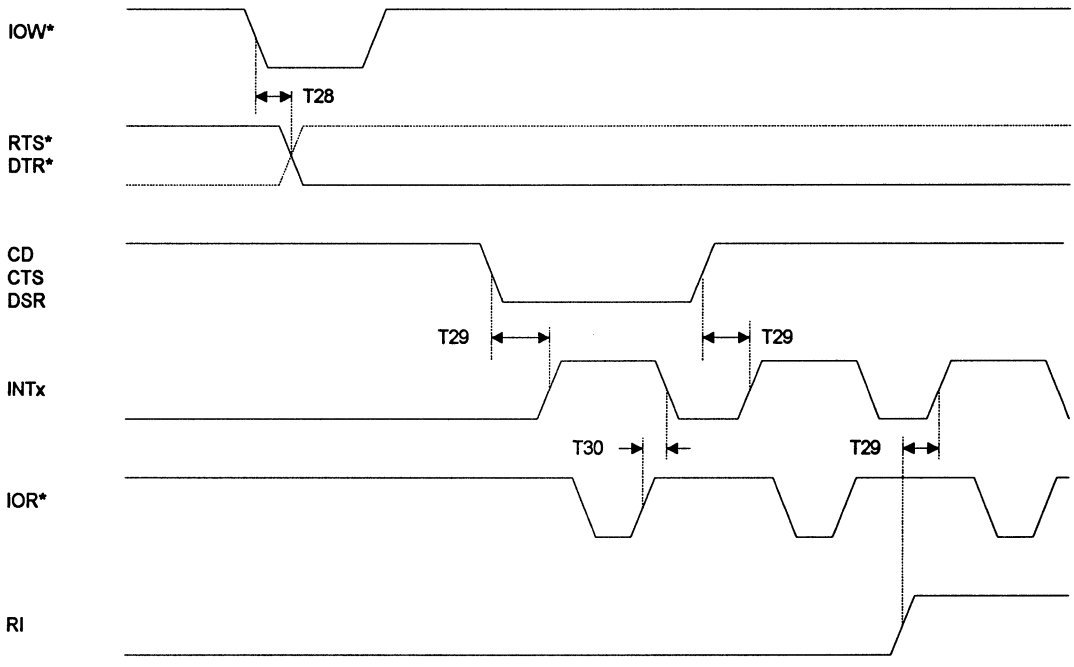
GENERAL WRITE TIMING



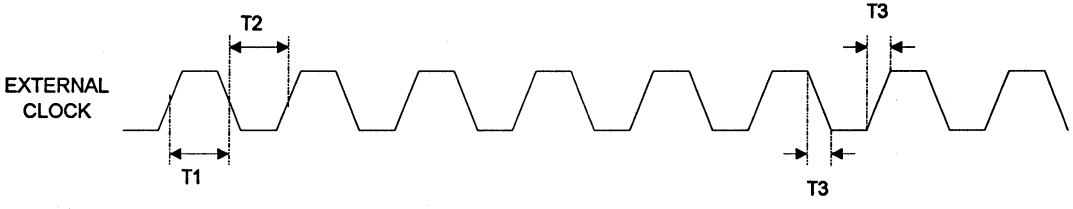
GENERAL READ TIMING



MODEM TIMING

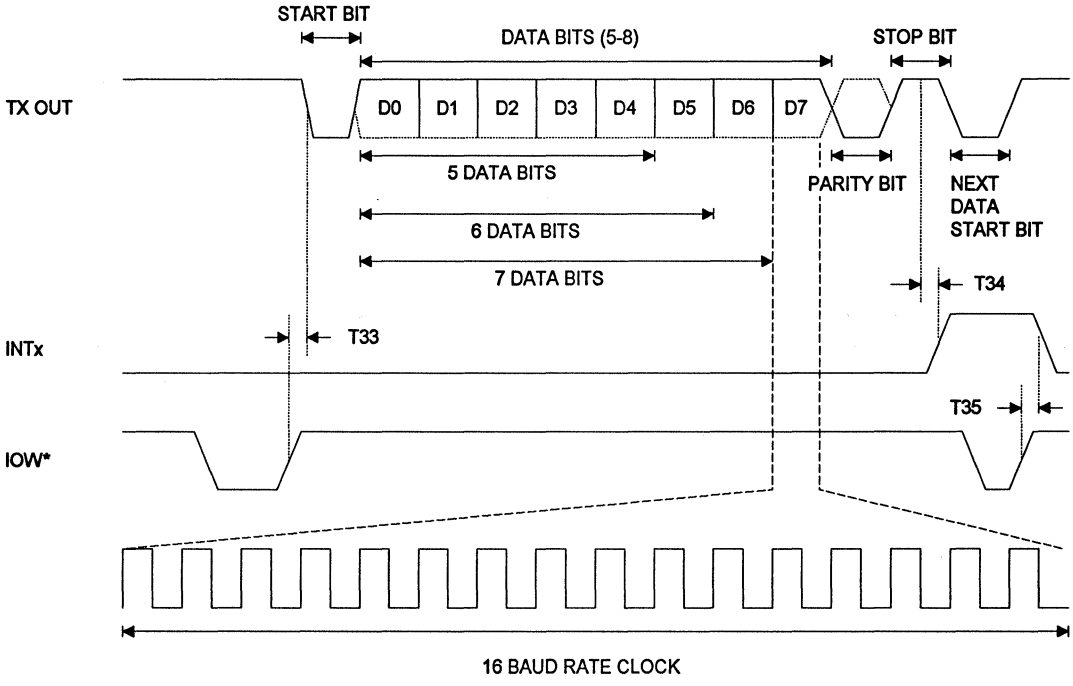


CLOCK TIMING

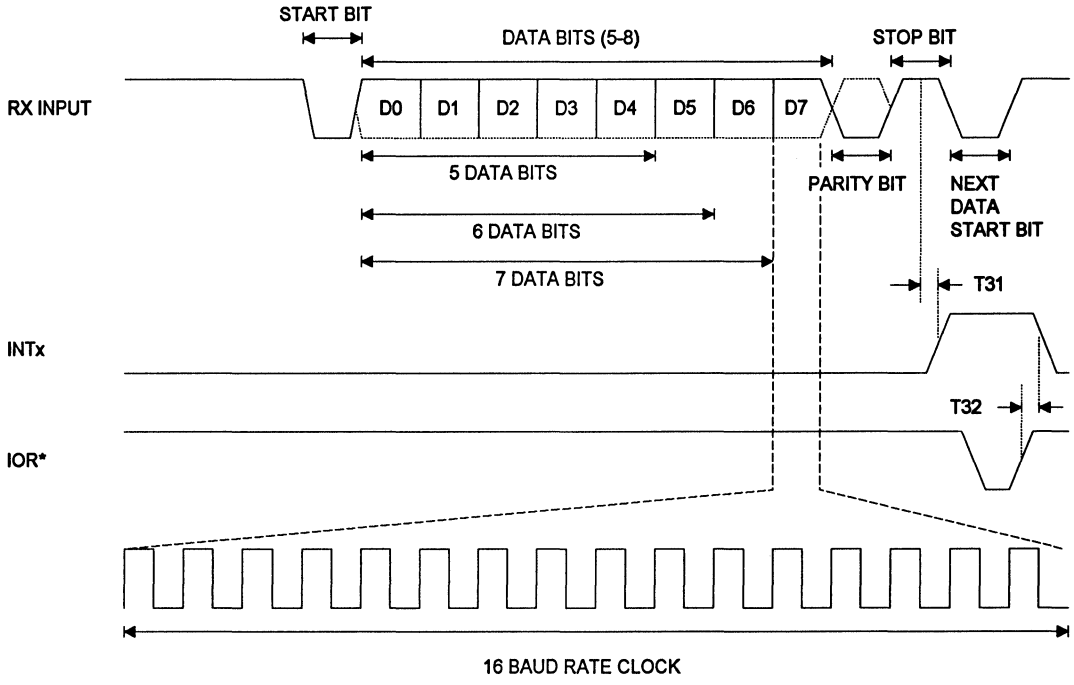


ST16C2550

TRANSMIT TIMING



RECEIVE TIMING



ST16C2550

STARTECH

ST16C554

APR 1992

QUAD ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

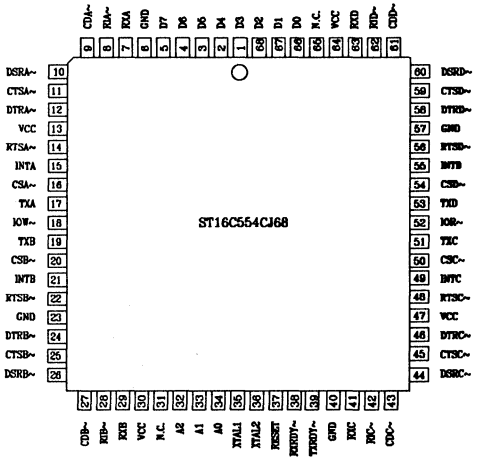
DESCRIPTION

The ST16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C554 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C554 provides internal loop-back capability for on board diagnostic testing.

The ST16C554 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



3

FEATURES

* Pin to pin and functional compatible to ST16C454
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Software compatible with INS8250, NS16C550
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

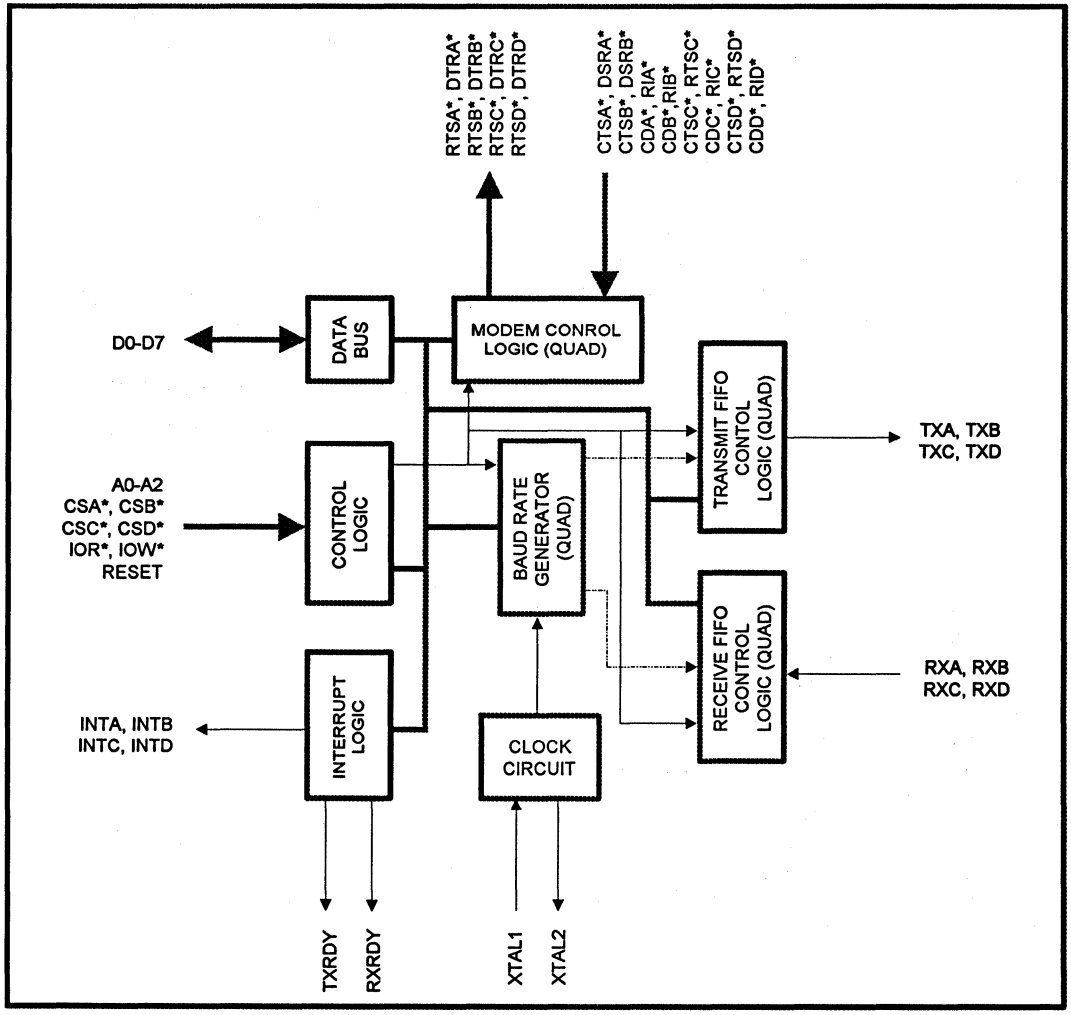
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554CJ68	PLCC	0° C to + 70° C

***Industrial operating range are available**

ST16C554

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	I	Serial data input. The serial information (data) received from serial port to ST16C554 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A-B* CS C-D*	16,20 50,54	I	Chip select. (active low) A low at this pin enables the ST16C554 / CPU data transfer operation. Each UART sections of the ST16C554 can be accessed indepently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,61	O	Signal and power ground.
IOR*	52	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C554 data bus to the CPU.

ST16C554

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
TXRDY*	39	O	Transmit ready. (active low) This pin goes low when the transmit FIFO of the ST16C554 is full. It can be used as a single or multi-transfer.
A2	32	I	Address select line 2. To select internal registers.
A1	33	I	Address select line 1. To select internal registers.
A0	34	I	Address select line 0. To select internal registers.
RXRDY*	38	O	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INT A-B INT C-D	15,21 49,55	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS A-B* RTS C-D*	14,22 48,56	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A-B* DTR C-D*	12,24 46,58	O	Data terminal ready. (active low) To indicate that ST16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CTS A-B* CTS C-D*	11,25 45,59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A-B* DSR C-D*	10,26 44,60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A-B* CD C-D*	9,27 43,61	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI A-B* RI C-D*	8,28 42,62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13,60 47,64	I	Power supply input.

3

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C554

ST16C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C554 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

ST16C554

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C554 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receive time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C554 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be nabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

ST16C554

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used, except in internal loop-back mode.

MCR BIT-3:
0=set the INT A-D output pin to three state mode..
1=Enable the INT A-D output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C554 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They

are set to "0" whenever the CPU reads this regist

MSR BIT-0:
Indicates that the CTS* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
RXRDY*	High
TXRDY*	High
INT	Three state mode

SCRATCHPAD REGISTER (SR)

ST16C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

ST16C554

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time	10			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{27}	IOR* to floating data delay	0		50	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1: *Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

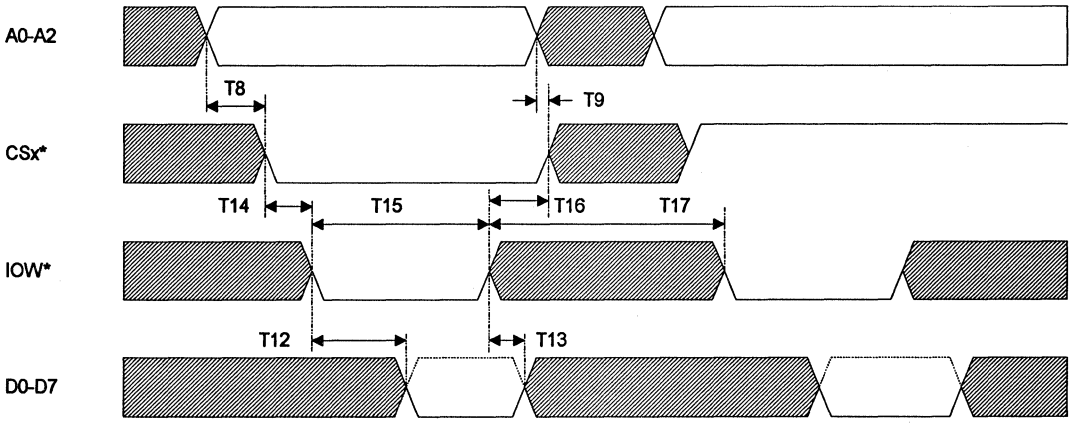
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

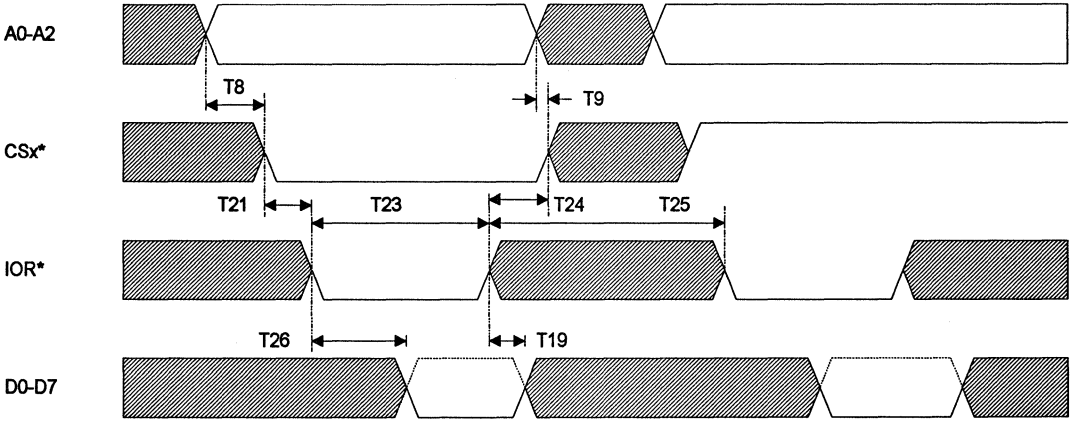
3

ST16C554

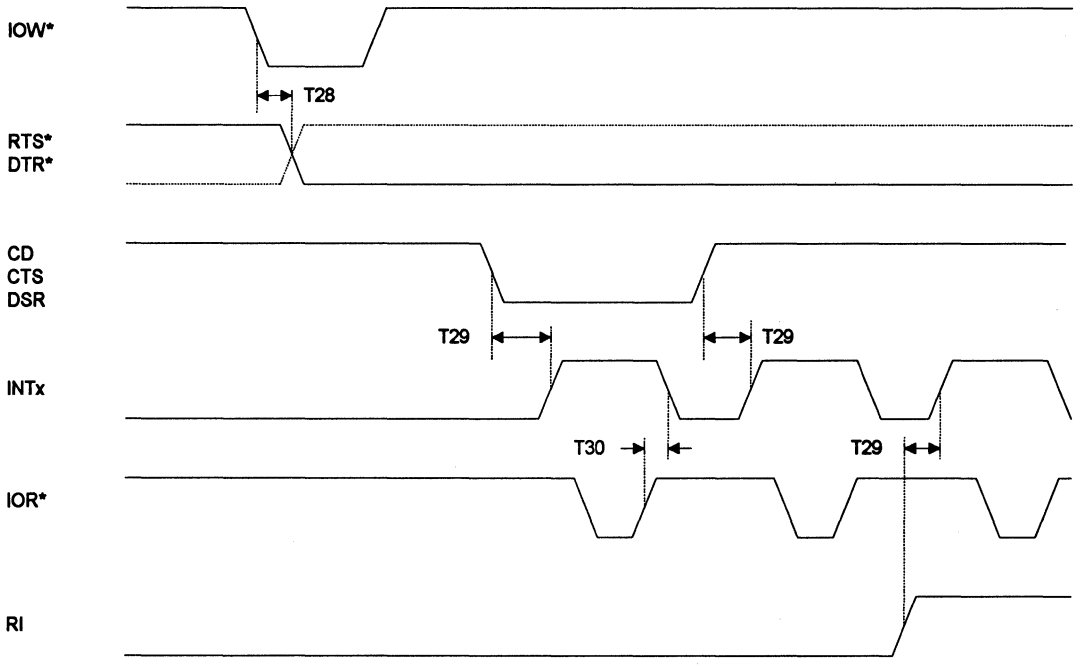
GENERAL WRITE TIMING



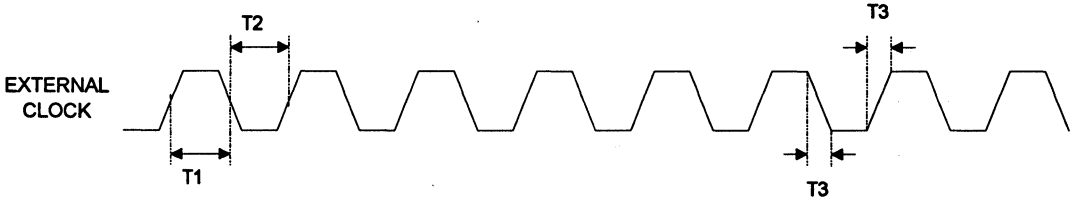
GENERAL READ TIMING



MODEM TIMING

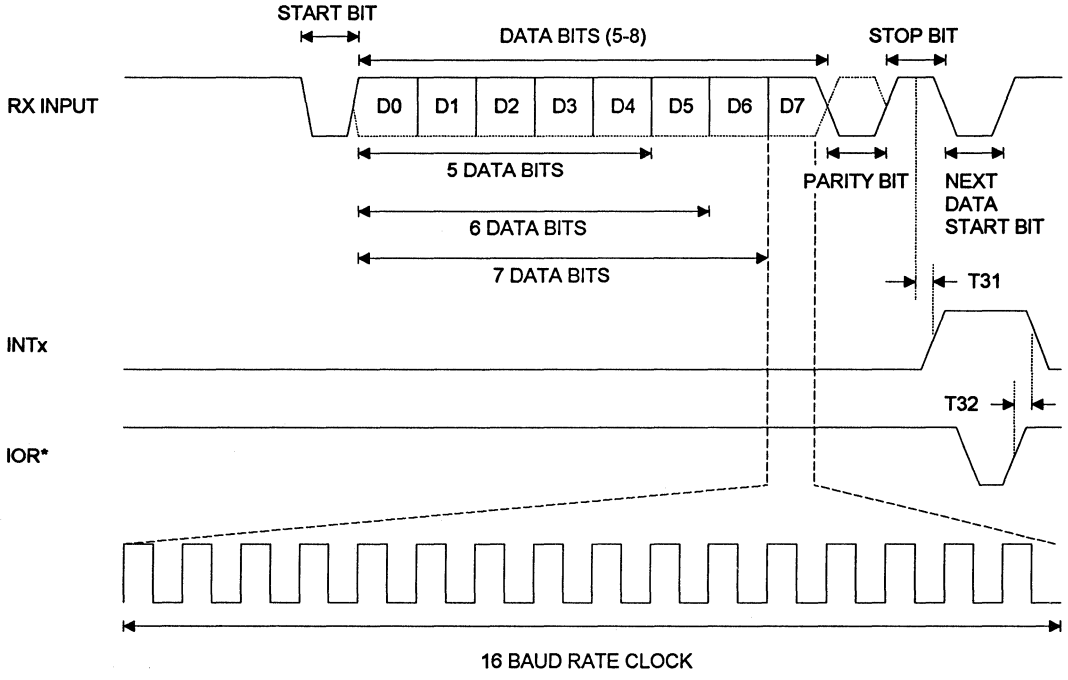


CLOCK TIMING

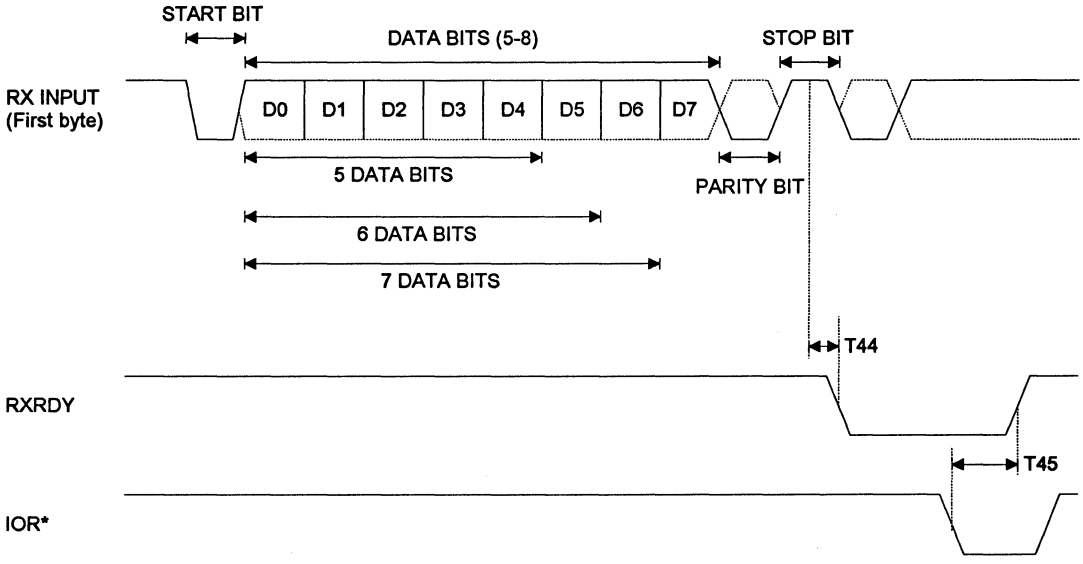


ST16C554

RECEIVE TIMING

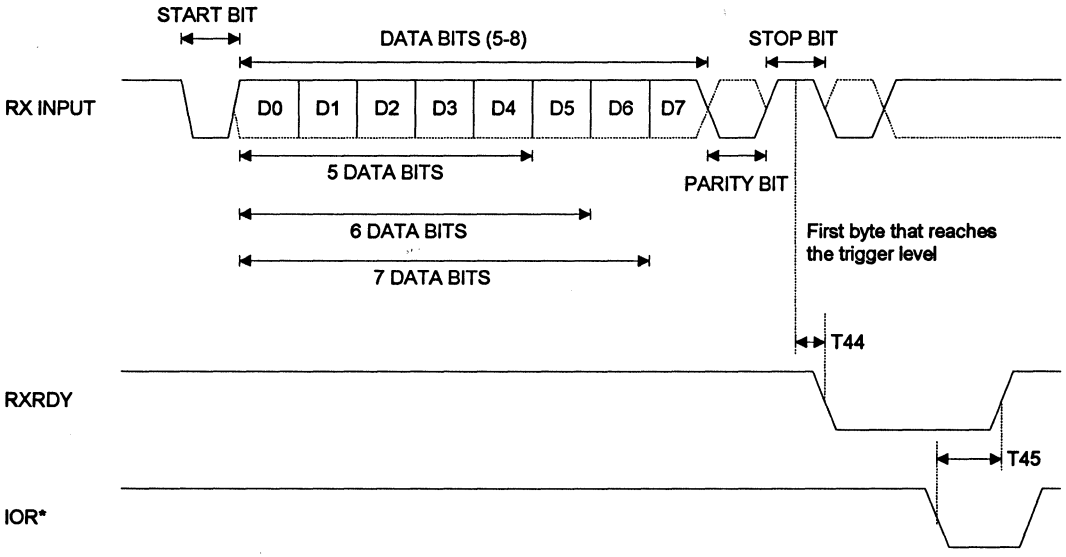


RXRDY TIMING FOR MODE "0"

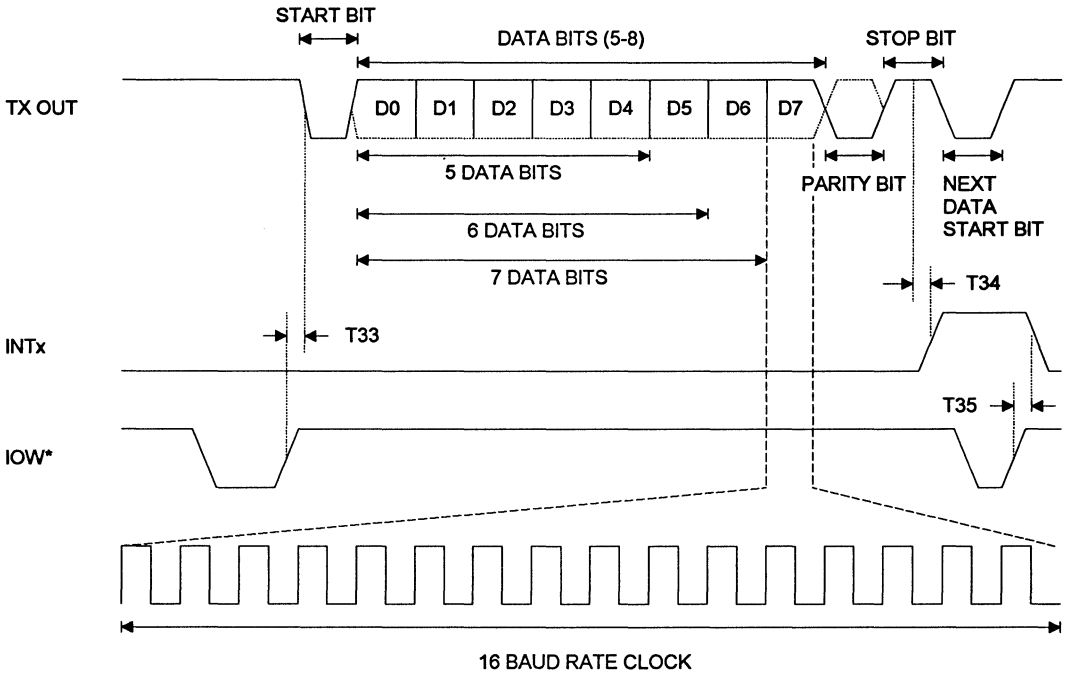


ST16C554

RXRDY TIMING FOR MODE "1"

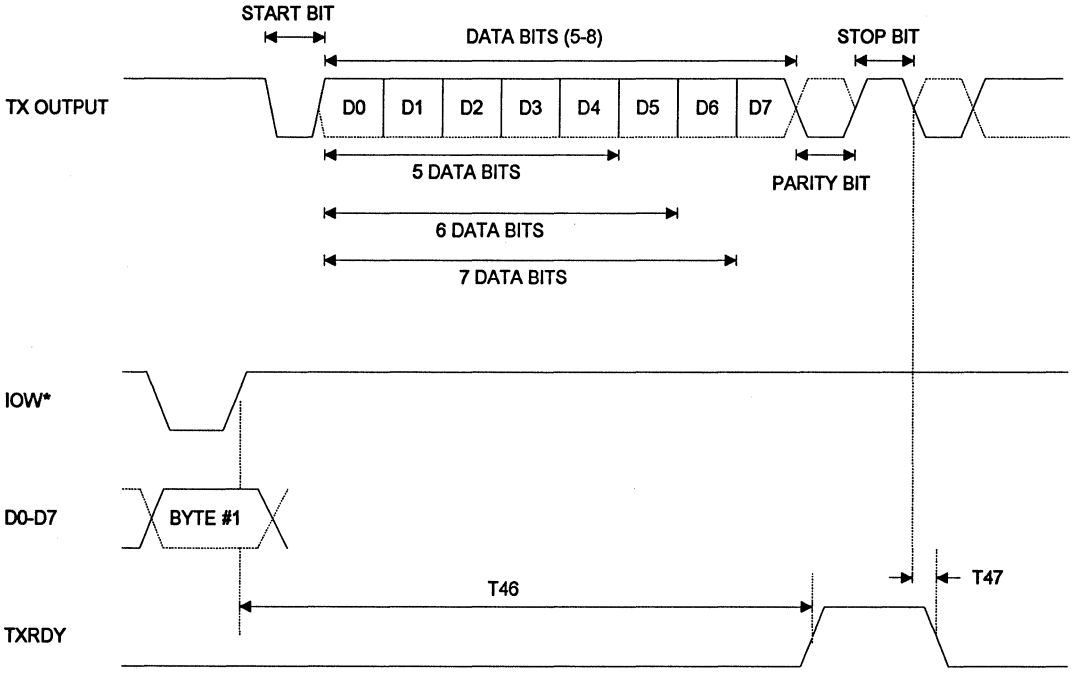


TRANSMIT TIMING

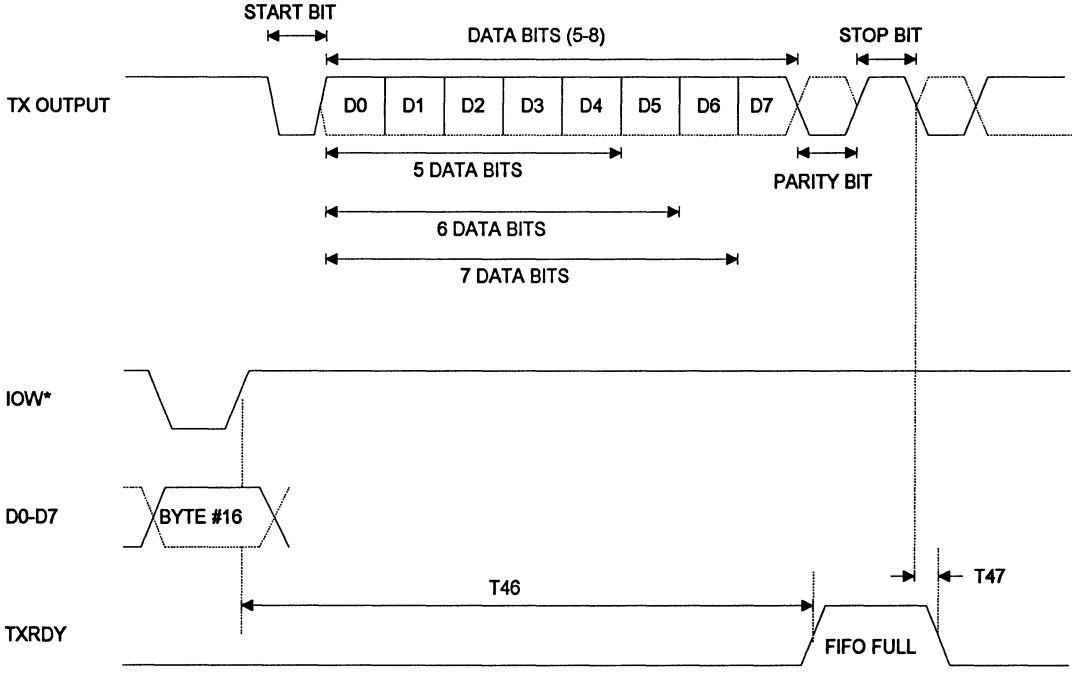


ST16C554

TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"



ST16C554

STARTECH

ST68C554

APR 1992

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

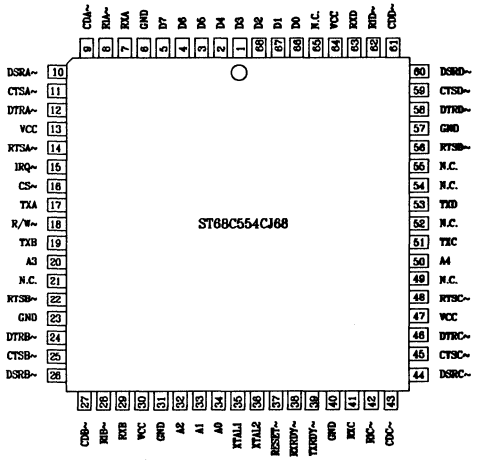
DESCRIPTION

The ST68C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST68C554 is an improved, quad version of the NS16550 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C554 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

* Motorola, Rockwell, Hitachi bus compatible
* Quad ST16C550
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* TTL compatible inputs, outputs
* 448 kHz transmit/receive operation with 7.372 MHz external clock source

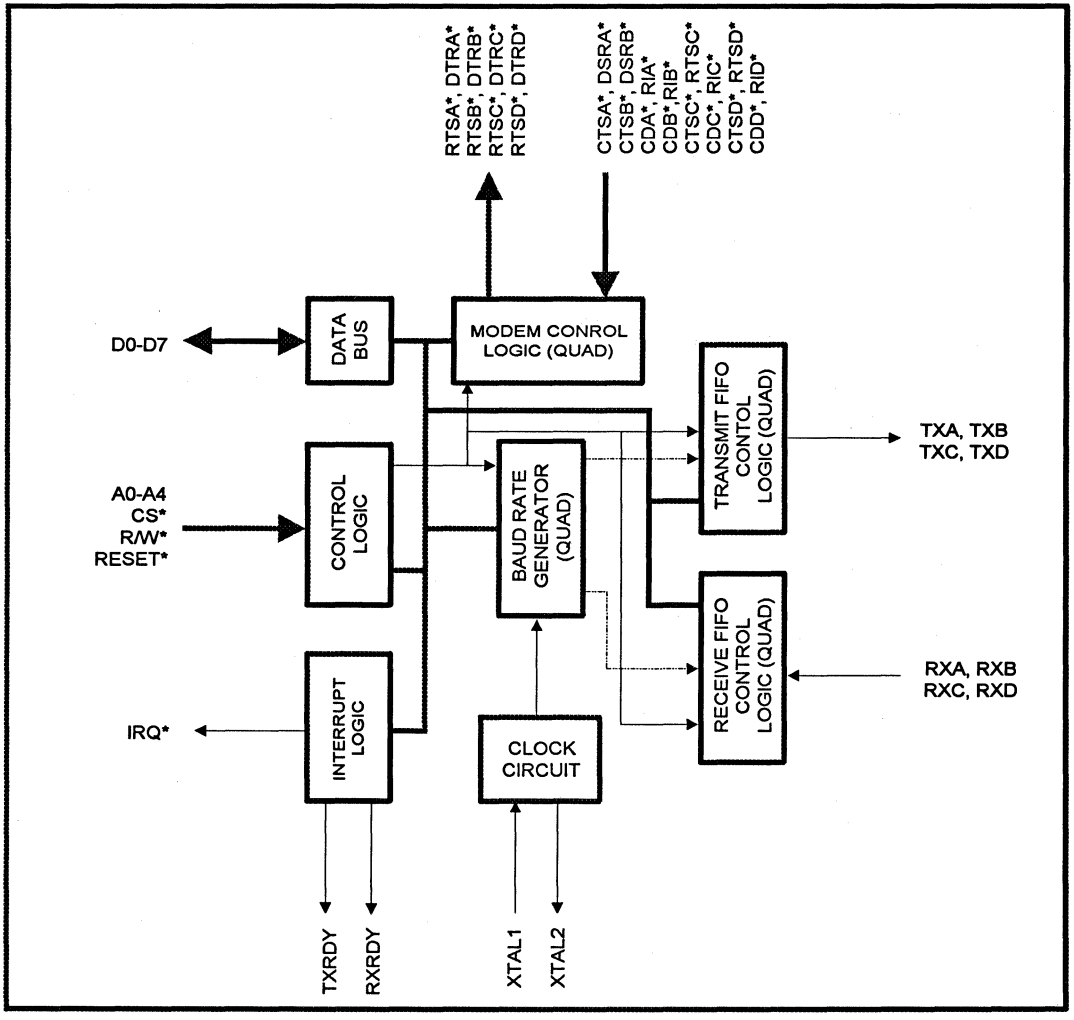
ORDERING INFORMATION

Part number	Package	Operating temperature
ST68C554CJ68	PLCC	0° C to +70°

***Industrial operating range are available**

ST68C554

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66	I/O	Bidirectional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B RX C/D	7,29 41,63	I	Serial data input . The serial information received from MODEM or RS232 to ST68C554 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B TX C/D	17,19 51,53	O	Serial data output A. The serial data of channel A is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	16	I	Chip select (active low). A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	I	Crystal input 2. See XTAL1.
R/W*	18	I	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C554 data bus to the CPU.
CD A/B* CD C/D*	9,27 43,61	I	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modem.
GND GND	6,23,31 40,57	O	Signal and power ground.

ST68C554

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DSR A/B* DSR C/D*	10,26 44,60	I	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.
RI A/B* RI C/D*	8,28 42,62	I	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTS A/B* RTS C/D*	14,22 48,56	O	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
CTS A/B* CTS C/D*	11,25 45,59	I	Clear to send A-D. (active low) The CTS* signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmitter output.
A4	50	I	Address line 4. To select one of the four UARTS.
A3	20	I	Address line 3. To select one of the four UARTS.
A2	32	I	Address line 2. To select internal registers.
A1	33	I	Address line 1. To select internal registers.
A0	34	I	Address line 0. To select internal registers.
IRQ*	15	O	Interrupt output. (active low) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
DTR A/B* DTR C/D*	12,24 46,58	O	Data terminal ready A-D. (active low) To indicate that ST68C554 is ready to receive data. This pin can be controlled

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET*	37	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	I	Power supply input.
TXRDY*	39	O	Transmit ready (active low). This pin goes low when the transmit FIFO of the ST68C554 (any one) is full. It can be used as a single or multi-transfer DMA.
RXRDY*	38	O	Receive ready (active low). This pin goes low when the receive FIFO of the ST68C554 is full. It can be used as a single or multi-transfer DMA.

SERIAL PORT SELECTION GUIDE

CS*	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

ST68C554

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:
A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST68C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode

operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR
The ST68C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D
The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the IRQ* output pin.

IER BIT-0:
0=disable the receiver ready interrupt
1=enable the receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable the modem status register interrupt
1=enable the modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D
The ST68C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C554 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receivce time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-5:
These bits are not used and are set zero.

ST68C554

ISR BIT 6-7:
0=Normal mode.
1=FIFO's are enabled.

FIFO CONTROL REGISTER (FCR)
This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER A-D
The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

LCR BIT-2:
The number of stop bits can be specified by this bit.

0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TX A-D) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D
This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high
1=force DTR* output to low

MCR BIT-1:
0=force RTS* output to high
1=force RTS* output to low

MCR BIT-2:
x=not used

MCR BIT -3:
0= Disable the IRQ* output
1=Enable IRQ* output.

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D , CTS A-D*, DSR A-D*, CD A-D*, and RI A-D*) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D*, RTS A-D* and OP A-D* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full; ST68C554 will not accept any data for transmission
1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
0=Normal
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

ST68C554

MODEM STATUS REGISTER A-D
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST68C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to ST16C550-OP1 in the MCR. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to ST16C550-OP2 in the MCR. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D
ST68C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16xCLOCK %ERROR	DVISOR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2	6	
38.4K	3	
56K	2	2.86
112K	1	

ST68C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
RTS A-D*	High
DTR A-D*	High
IRQ	Three state mode

ST68C554 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	IRQ enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST68C554

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time	10			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time from write	5			ns	
T_{13}	Data hold time from chip select	25			ns	
T_{14}	Write delay from chip select	10			ns	
T_{15}	Write strobe width	50			ns	
T_{16}	Chip select hold time from write	5			ns	
T_{17}	Write cycle delay	55			ns	
T_{18}	Data setup time	10			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{24}	Chip select hold time from read	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{18}+T_{25}	135			ns	
T_{28}	Delay from Write to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from Read to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial IRQ* reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from Write to reset interrupt			75	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from read (CS*) to reset RxRdy			1	µs	
T_{46}	Delay from write to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	

* Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

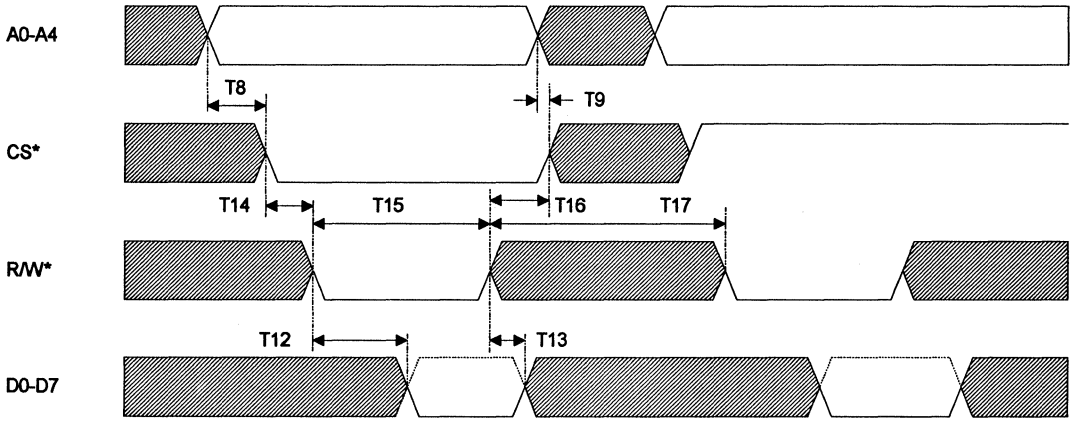
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

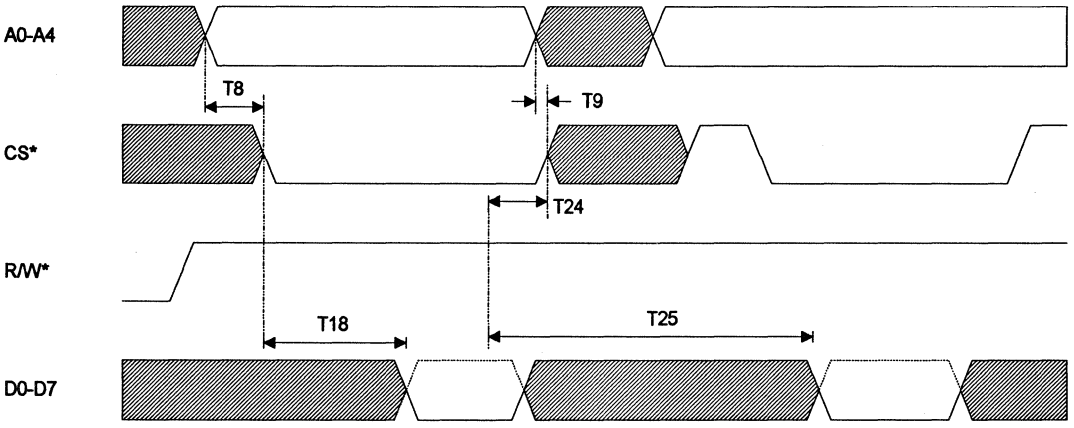
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6 mA on all outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current			6	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST68C554

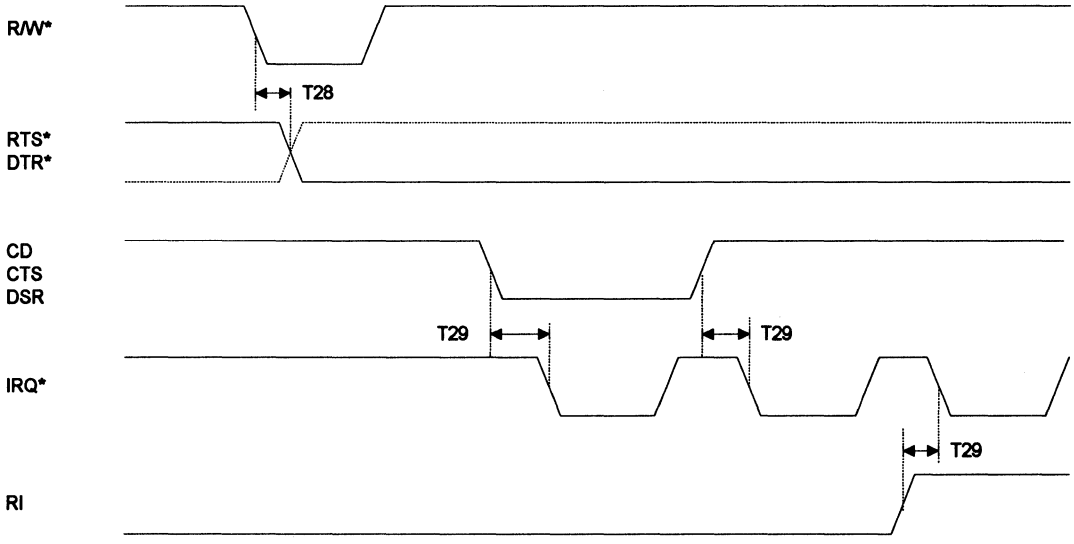
GENERAL WRITE TIMING



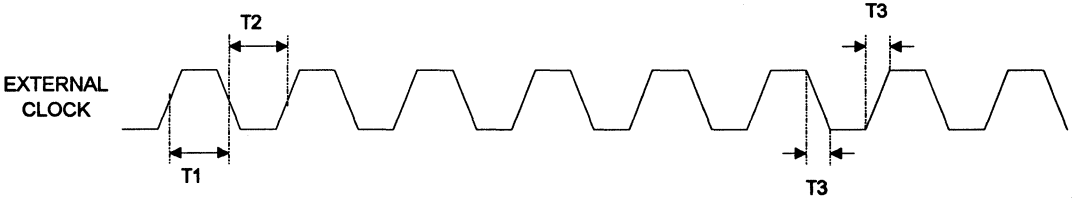
GENERAL READ TIMING



MODEM TIMING

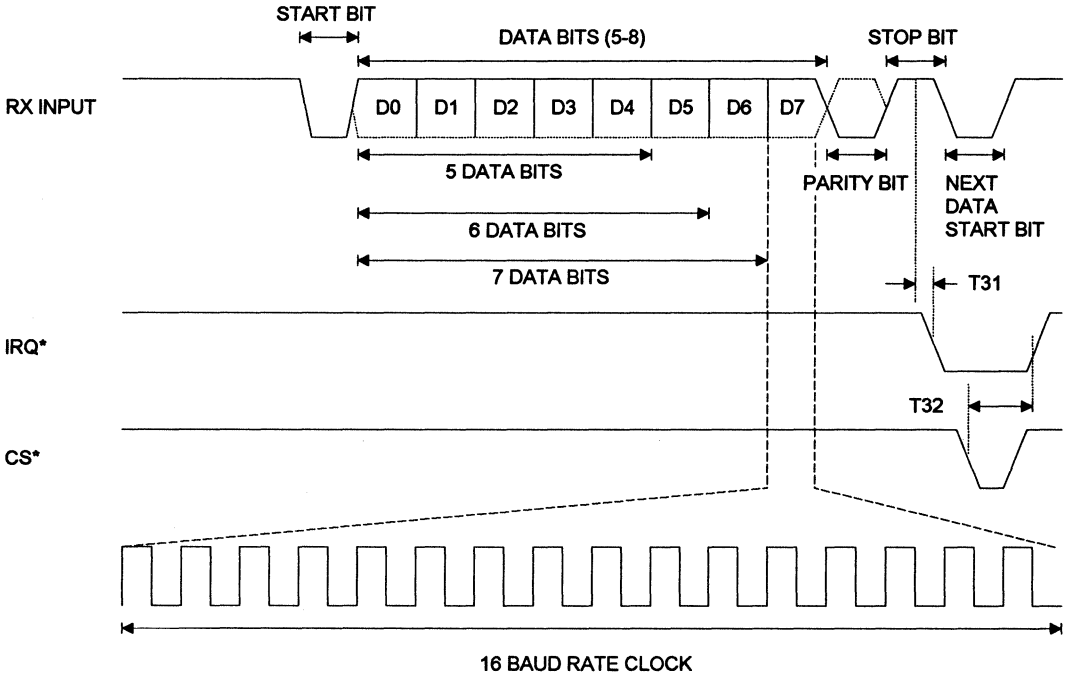


CLOCK TIMING

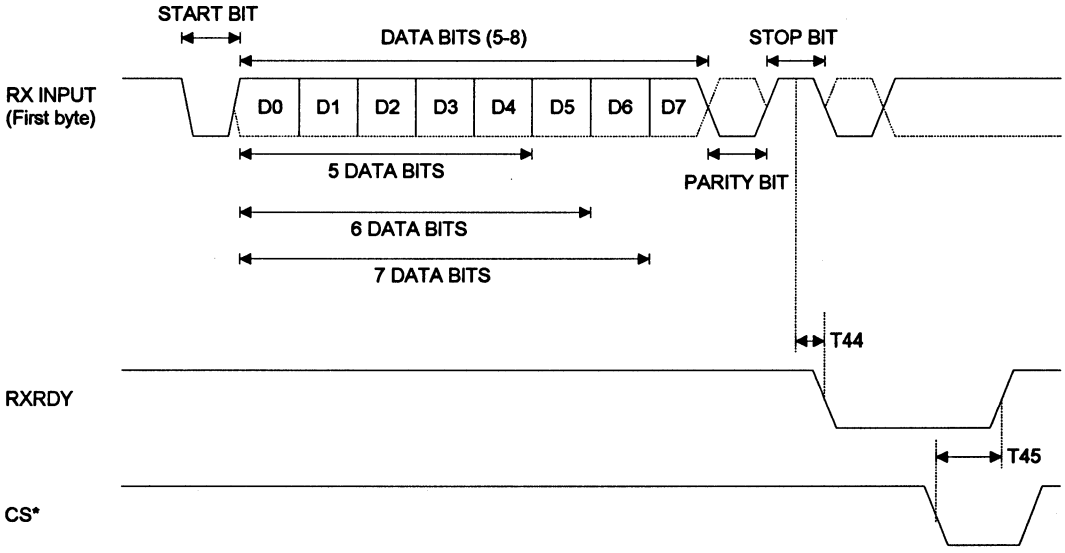


ST68C554

RECEIVE TIMING

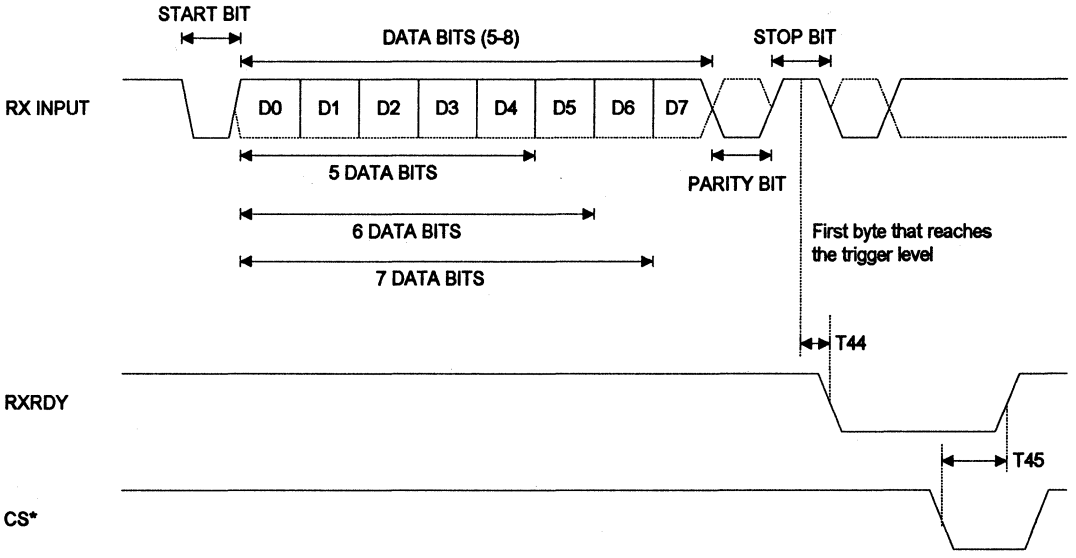


RXRDY TIMING FOR MODE "0"

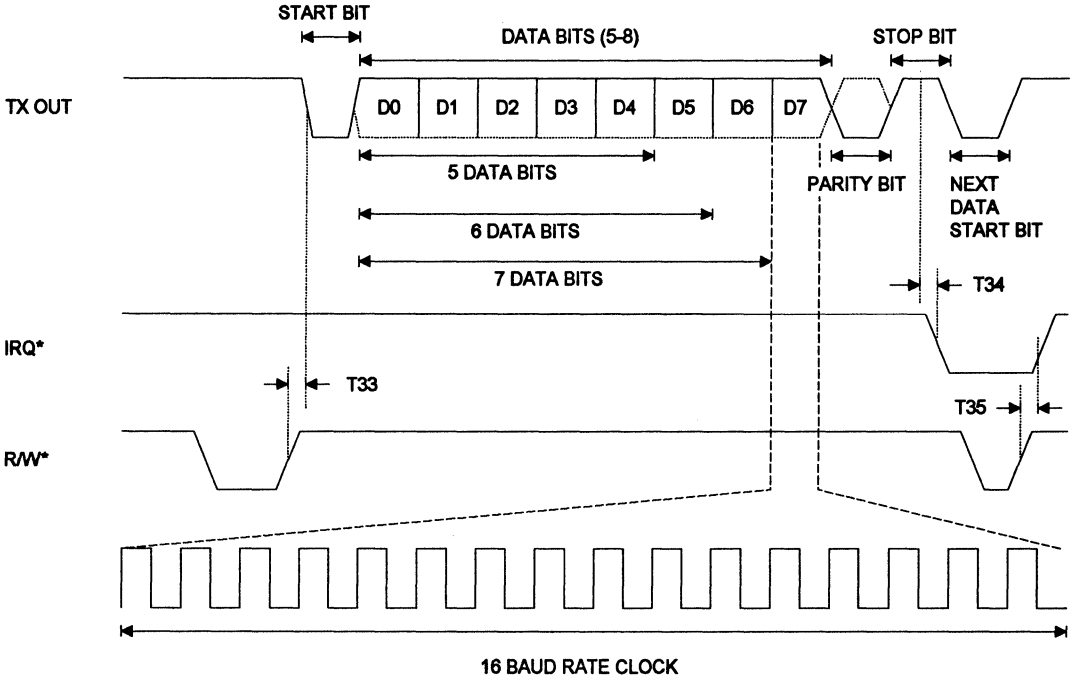


ST68C554

RXRDY TIMING FOR MODE "1"

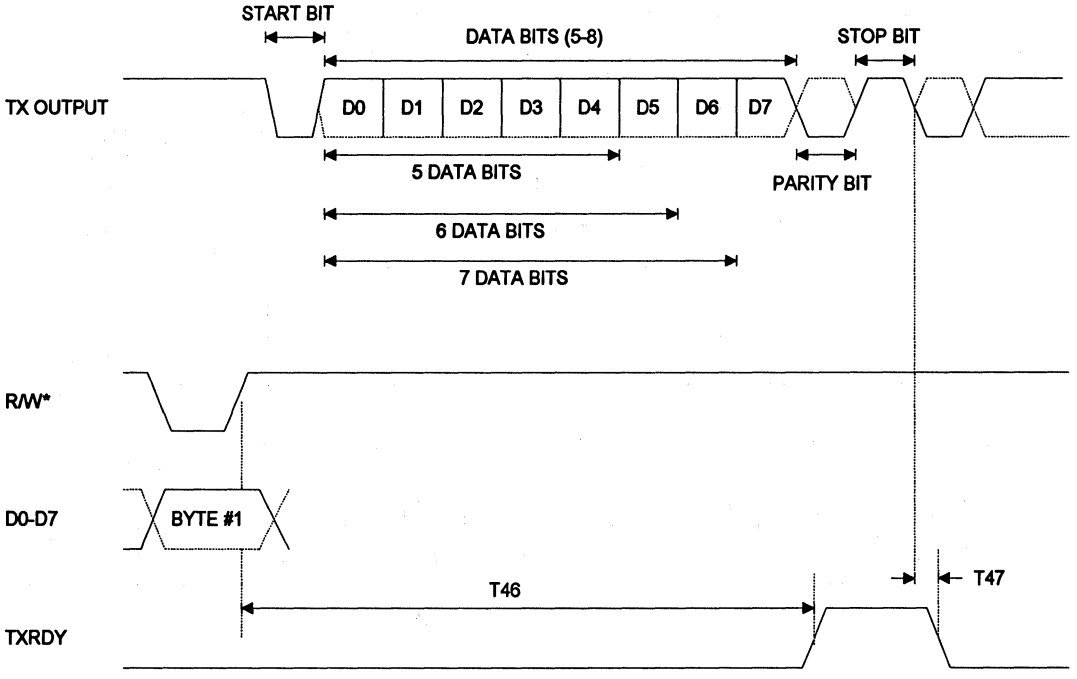


TRANSMIT TIMING

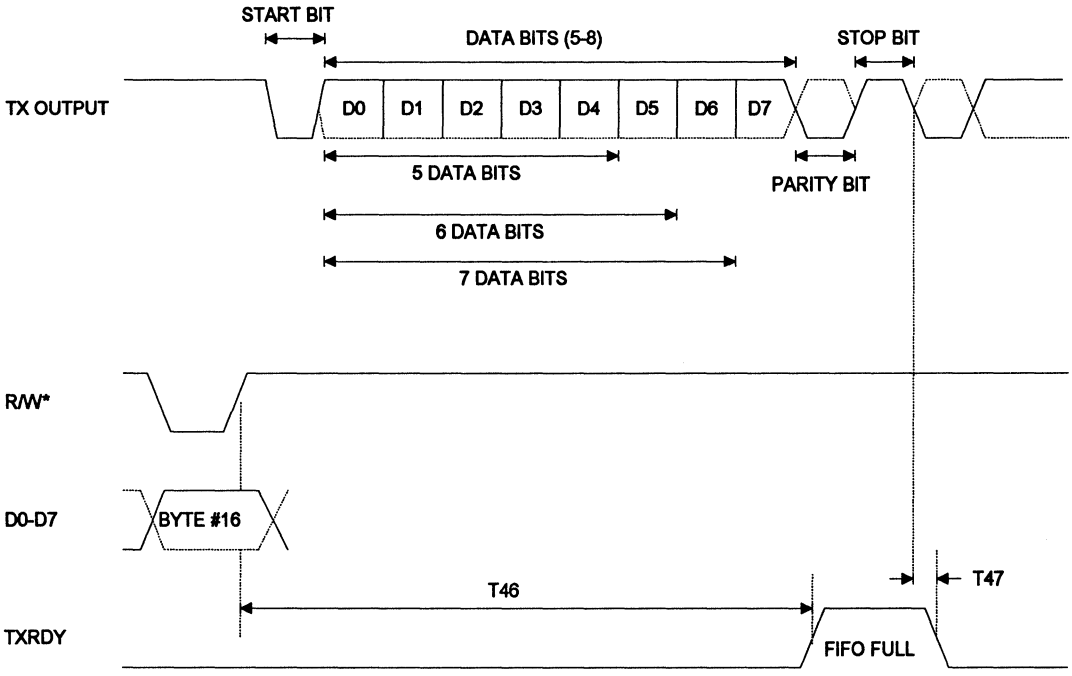


ST68C554

TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"



ST68C554

STARTECH

ST16C452AT
ST16C452PS

APR 1992

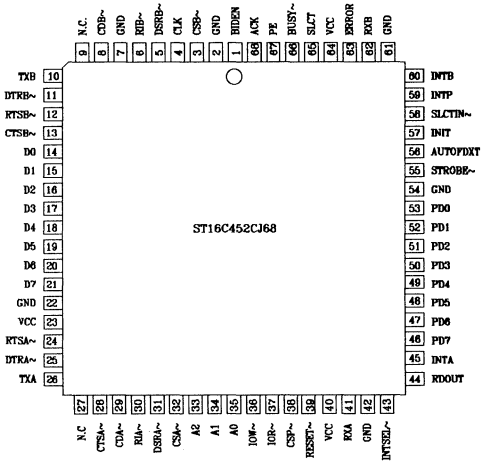
DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

The ST16C452 is a dual universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. STARTECH ST16C452PS provides additional features to control the printer port direction without any additional external logic.

The ST16C452 is an inproved version of the VL16C452 UART with higher operating speed and lower access time. The ST16C452 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C452 provides internal loop-back capability for on board diagnostic testing. The ST16C452 is fabricated in an advanced 1.2µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

* Pin to pin and functional compatible to VL16C452, WD16C452
* Fully compatible with all new bidirectional PS/2 printer port registers.
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Independent transmit and receive control
* Software compatible with INS8250, NS16C450
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
* Bidirectional hardware/software parallel port
* Bideirectional I/O ports

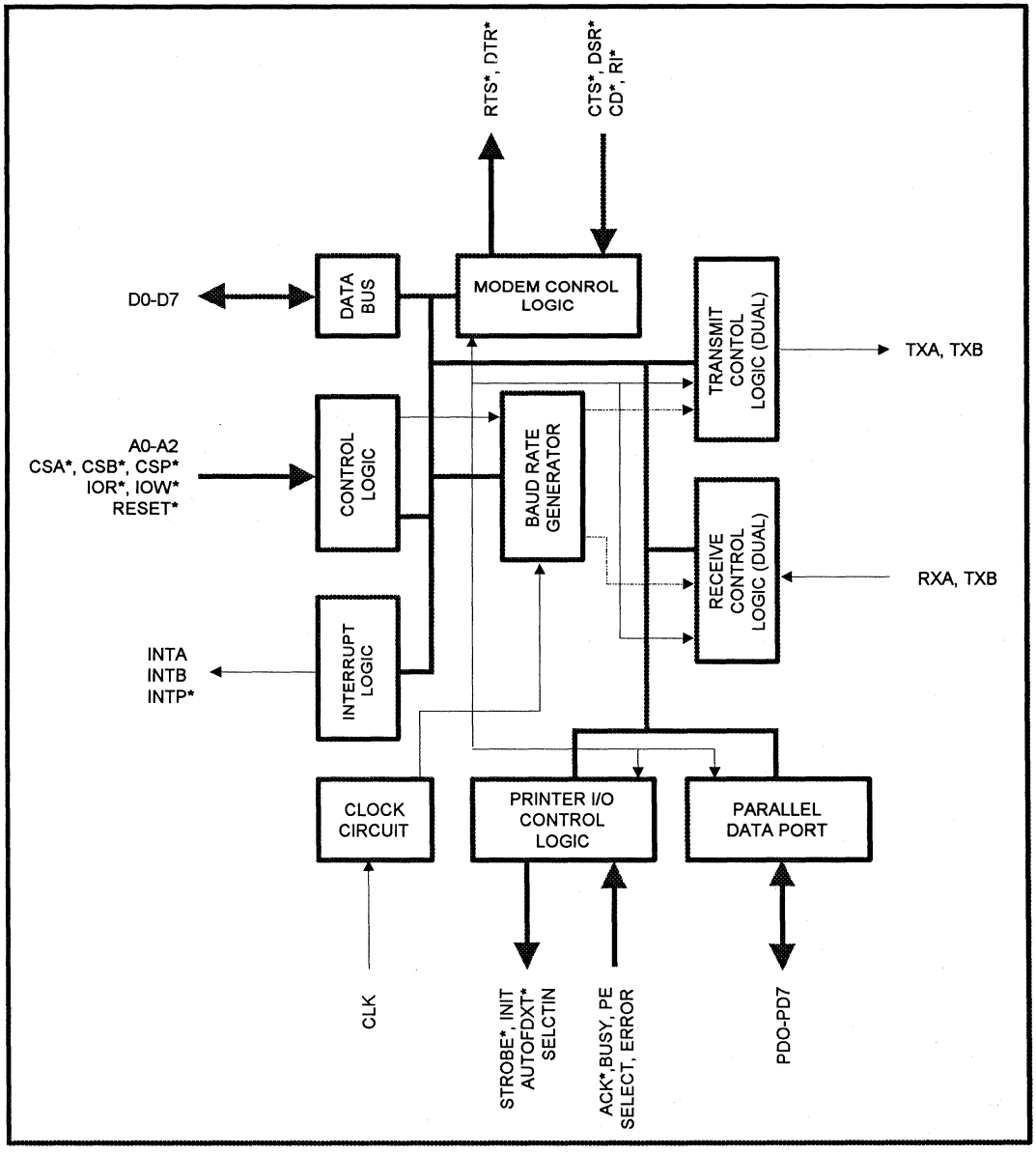
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C452CJ68	PLCC	0° C to + 70° C

***Industrial operating range are available**

ST16C452AT
ST16C452PS

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input mode for ST16C452AT and softerware controlled mode (input/output) to ST16C452PS. Alow sets the ST16C452 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C452 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C452 to en/disable the external transceiver or logics.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from

ST16C452AT
ST16C452PS

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			telephone line.
CD A/B*	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR A/B*	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B*	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C452 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*	28,13	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bidirectional parallel ports (three state). To transfer data in or out of the ST16C452 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	56	I/O	General purpose I/O or line printer autofeed (open drain active low). To signal the printer for continuous form feed.
INIT*	57	I/O	General purpose I/O or line printer initialize (open drain active low). To signal the line printer to enter internal initialization routine.
SLCTIN*	58	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
ERROR*	63	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
PE	67	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68	I	General purpose input or line printer acknowledge (active low). An output from the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of

ST16C452AT
ST16C452PS

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,22 42,54,61	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

PROGRAMMING TABLE FOR SERIAL PORTS A/B

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C452 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C452AT
ST16C452PS

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C452 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

ST16C452AT
ST16C452PS

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
This bit is used for internal loop-back mode, and is not used for regular operation.

MCR BIT-3:
0= sets the INT output pin to three state mode.
1= enables the INT output pin.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:
0=transmit holding register is full. ST16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:
Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C452 provides a temporary data register to store 8 bits of information for variable use.

SIGNALS	RESET STATE
TX	High
INTenable	High (three state)
RTS*	High
DTR*	High
INT	Three state mode

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C452 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals

ST16C452AT
ST16C452PS

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

ST16C452XX	CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
ST16C452AT	X	0	X	Output mode
ST16C452PS	X	0	AA Hex	Input mode
ST16C452PS	X	0	55 Hex	Output mode
ST16C452AT	X	1	X	Input mode
ST16C452PS	0	1	X	Output mode
ST16C452PS	1	1	X	Input mode

PRINTER PORTREGISTER DESCRIPTIONS

PORT REGISTER

Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.

ST16C452AT
ST16C452PS

Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.
I/O select register and control register bit-5 are only available for ST16C452PS parts.

ST16C452 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	High, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

ST16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt (PS only)		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
	0=Output (PS only) 1=Input (PS only) X= AT only		0=INTP output disabled 1=INTP output enabled				

ST16C452AT
ST16C452PS

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time	10			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW*to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{39}	ACK* pulse width	75			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1 *Baudout* cycle

ST16C452AT
ST16C452PS

ABSOLUTE MAXIMUM RATINGS

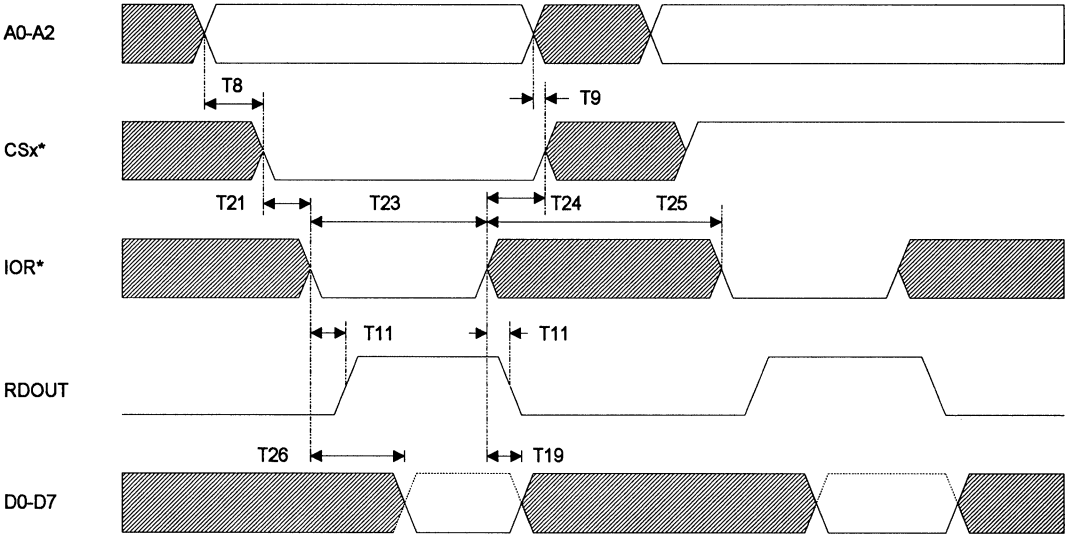
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

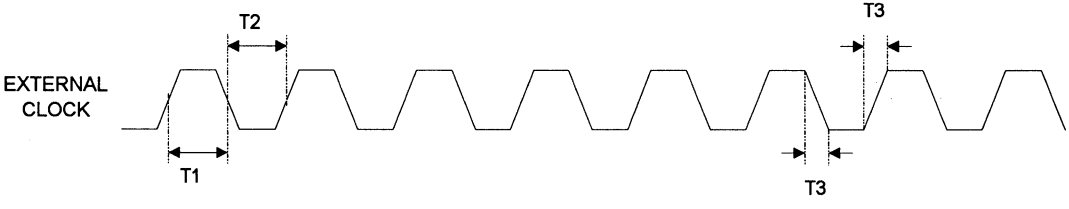
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all othe outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL READ TIMING

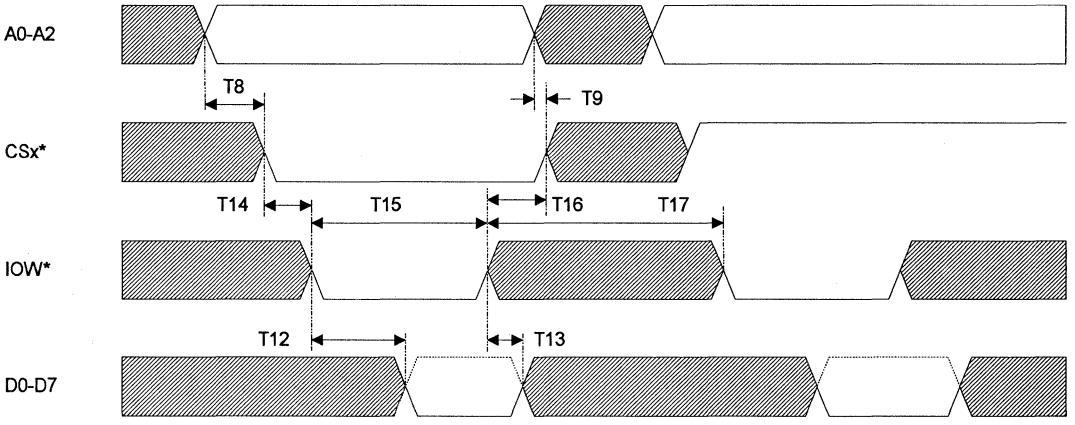


CLOCK TIMING

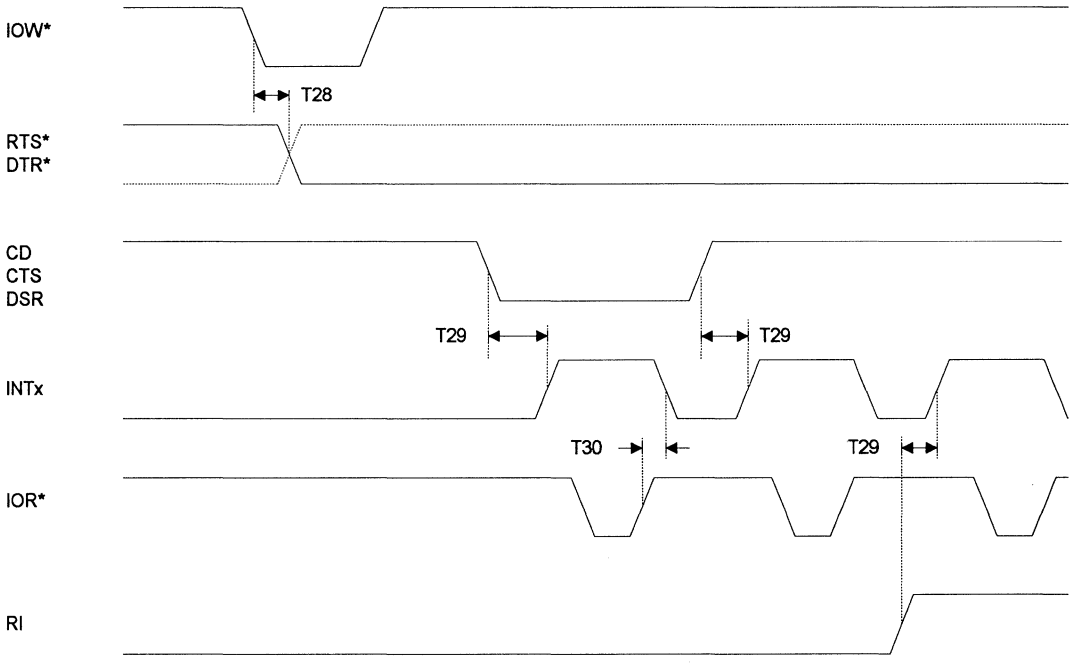


ST16C452AT
ST16C452PS

GENERAL WRITE TIMING

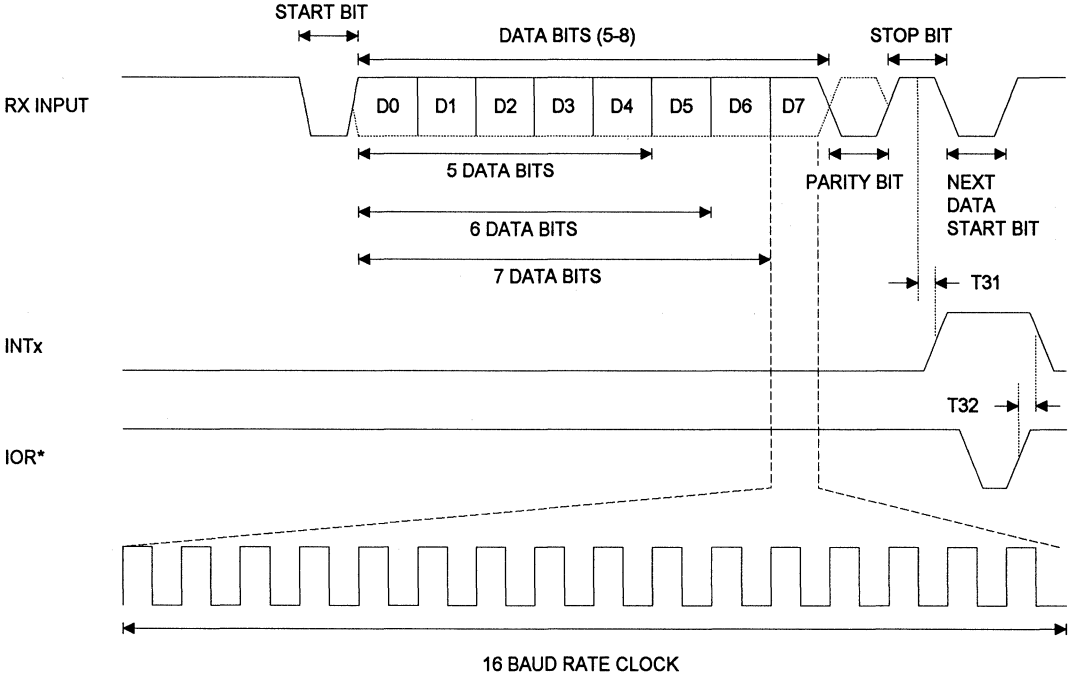


MODEM TIMING

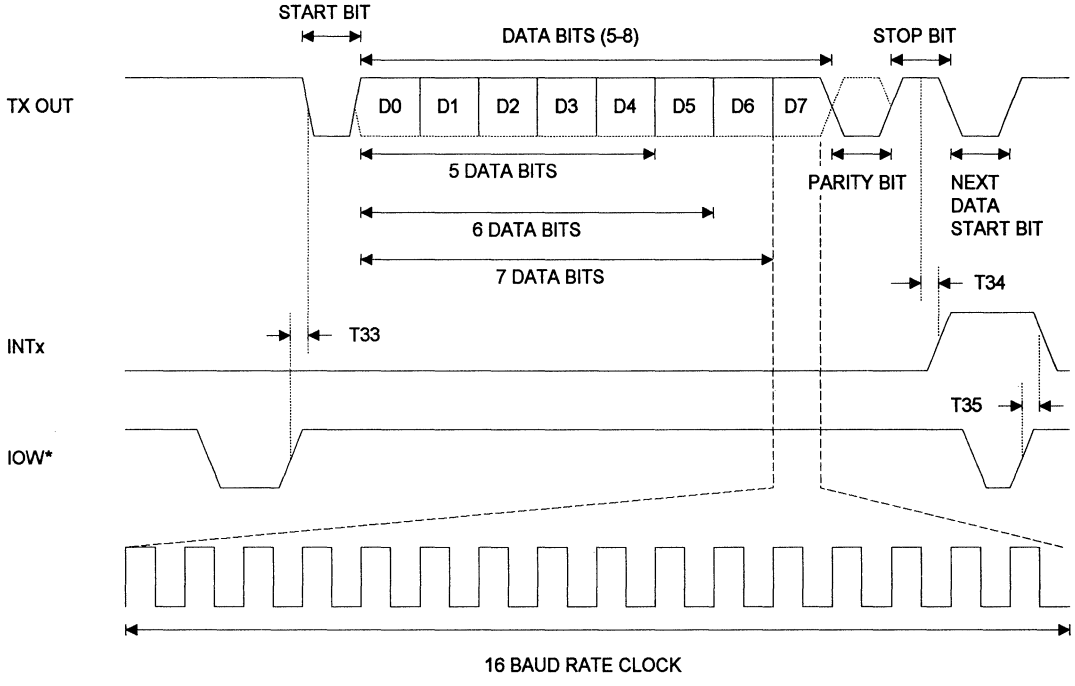


ST16C452AT
ST16C452PS

RECEIVE TIMING

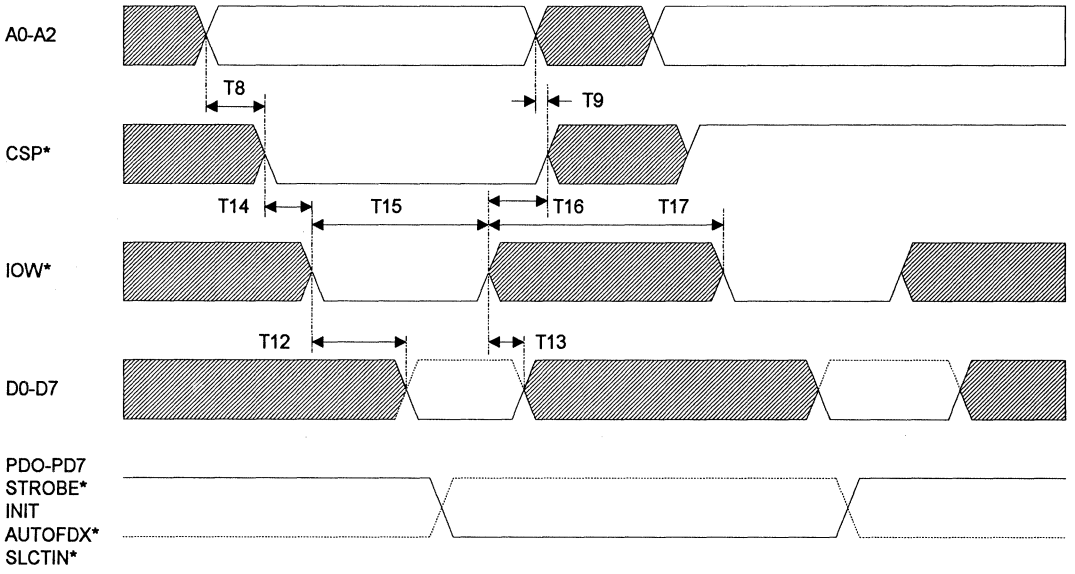


TRANSMIT TIMING

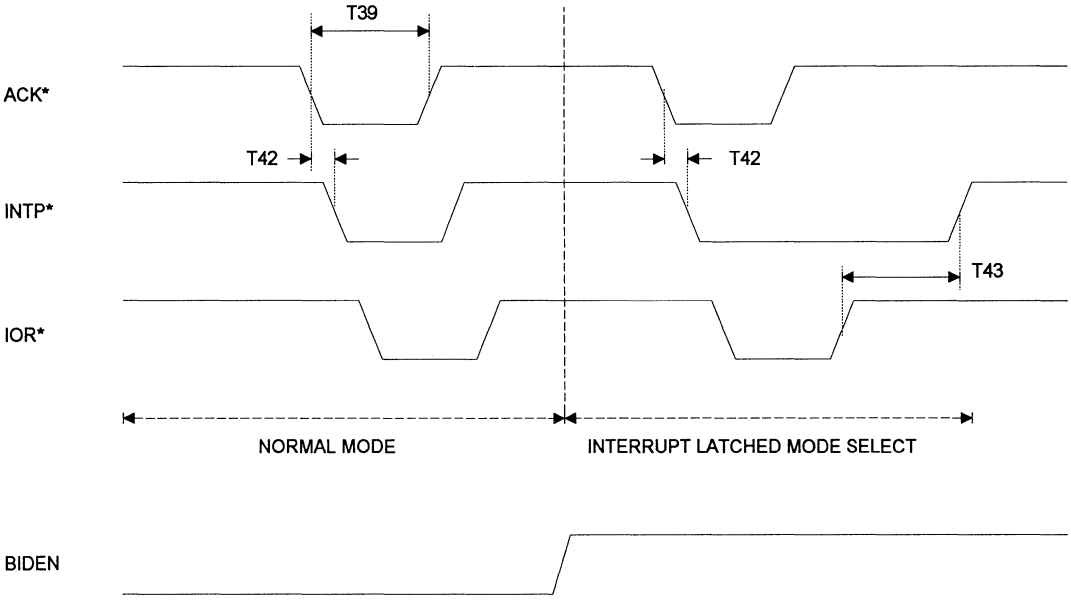


ST16C452AT
ST16C452PS

PARALLEL PORT GENERAL WRITE TIMING



PARALLEL PORT READ TIMING



ST16C452AT
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STARTECH

ST16C552

APR 1992

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT

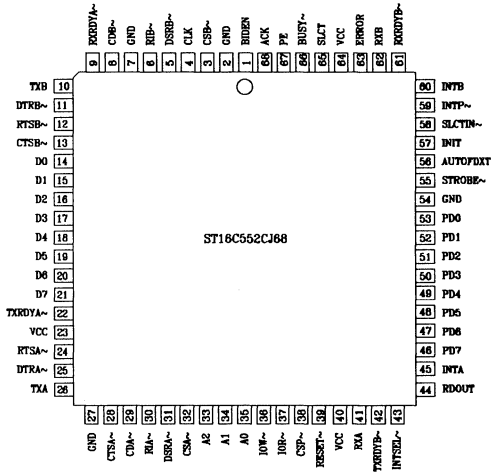
DESCRIPTION

The ST16C552 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bidirectional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C552 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C552 provides internal loopback capability for on board diagnostic testing.

The ST16C552 is fabricated in an advanced 1.2 µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

* Pin to pin and functional compatible to VL16C552, WD16C552
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Software compatible with INS8250, NS16C550
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
* Bidirectional hardware/software parallel port
* Bidirectional I/O ports

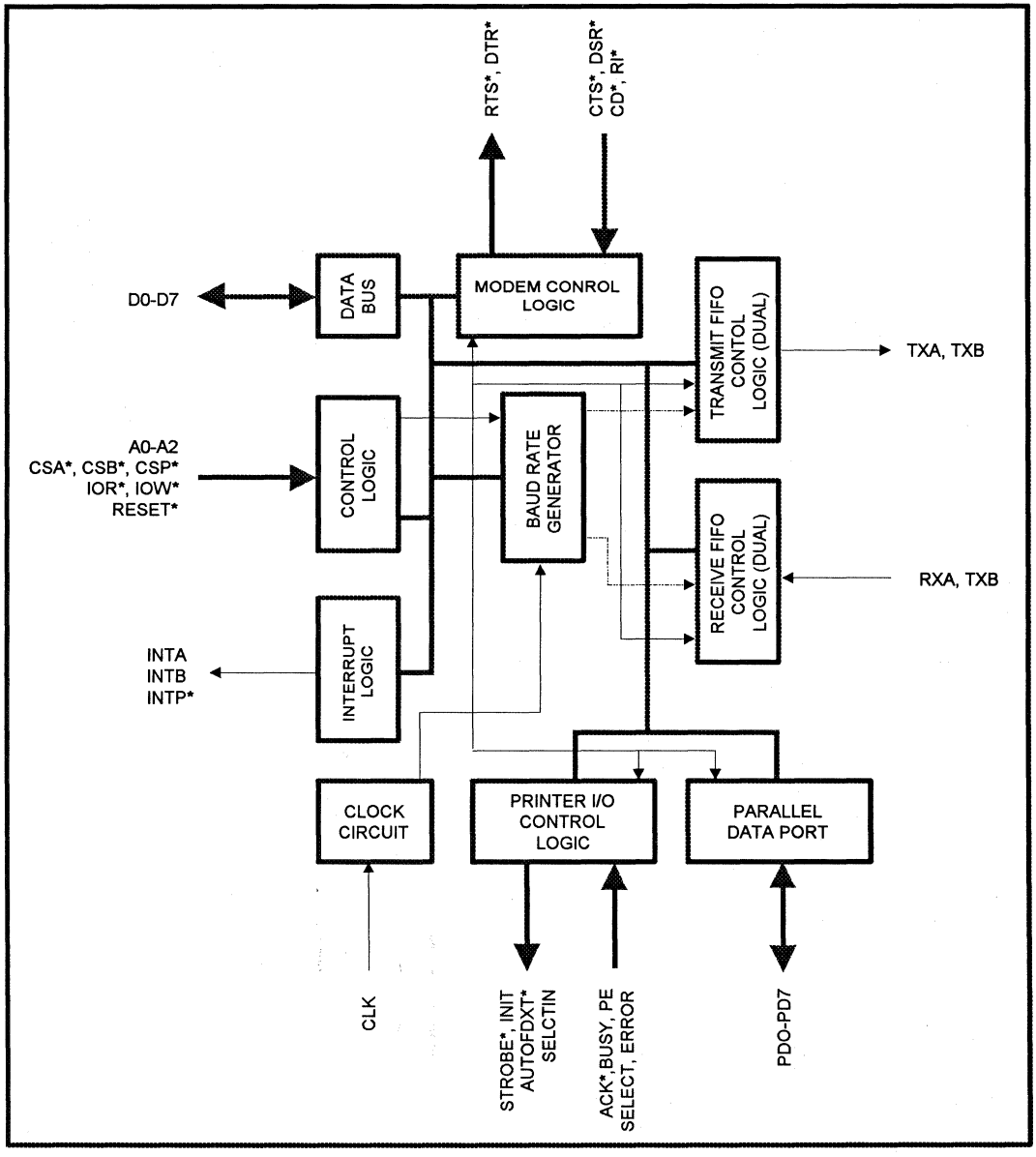
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C552CJ68	PLCC	0° C to + 70° C

***Industrial operating range are available**

ST16C552

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C552 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C552 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C552 to en/disable the external transceiver or logics.
RESET*	39	I	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

ST16C552

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD A/B*	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR A/B*	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B*	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*	36	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY A/B*	22,42	O	Transmit ready A/B (active low). This pin goes low when

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			the transmit FIFO of the ST16C552 is full. It can be used as a single or multi-transfer.
RXRDY A/B*	9,61	O	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bidirectional parallel ports (three state). To transfer data in or out of the ST16C552 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	56	I/O	General purpose I/O or line printer autofeed (open drain active low). To signal the printer for continuous form feed.
INIT	57	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	58	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
ERROR*	63	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

ST16C552

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
PE	67	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	68	I	General purpose input or line printer acknowledge (active low). An output from the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,54	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C552 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C552

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transfered to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C552 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receive time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C552 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

ST16C552

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C552 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

ST16C552

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C552 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
RTS*	High
DTR*	High
INT	Three state mode
RXRDY*	High
TXRDY*	High

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

ST16C552

PRINTER PORT REGISTER DESCRIPTIONS

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C552 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	High, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	X	Input mode

ST16C552

ST16C552 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
	0=Output 1=Input		0=INTP output disabled 1=INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time				ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt					
T_{38}	Delay from rising IOW* to output data	5			ns	
T_{39}	ACK* pulse width	75			ns	
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
N	Baud rate devisor	1		2^{16}-1		

Note 1 *Baudout* cycle

ST16C552

ABSOLUTE MAXIMUM RATINGS

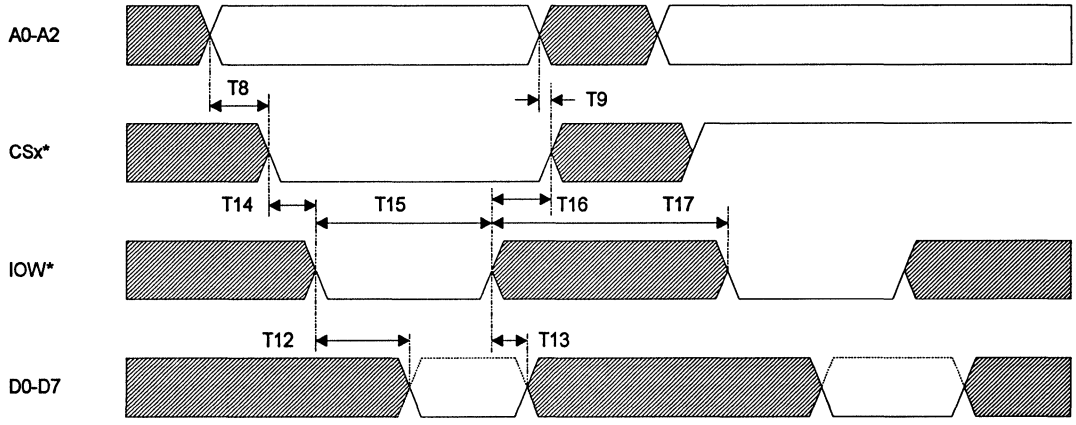
Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

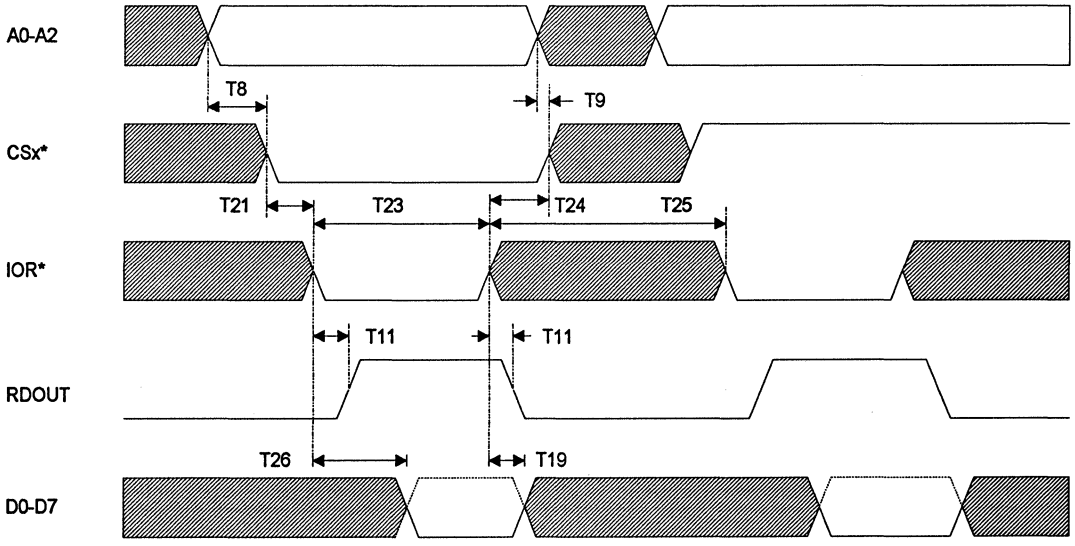
T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all othe outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

GENERAL WRITE TIMING

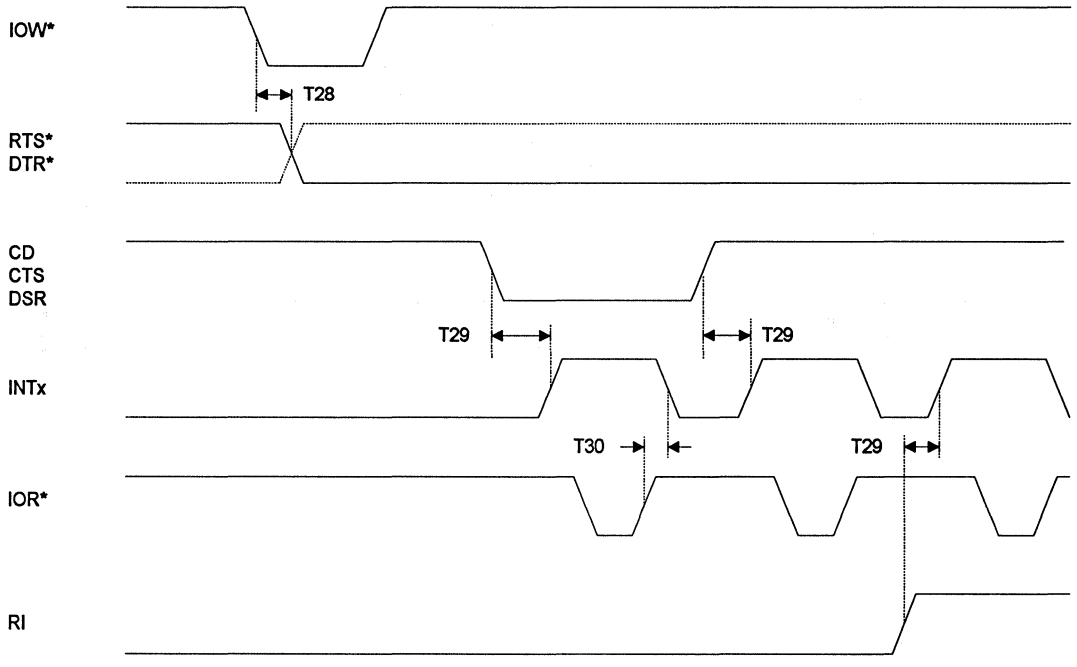


GENERAL READ TIMING

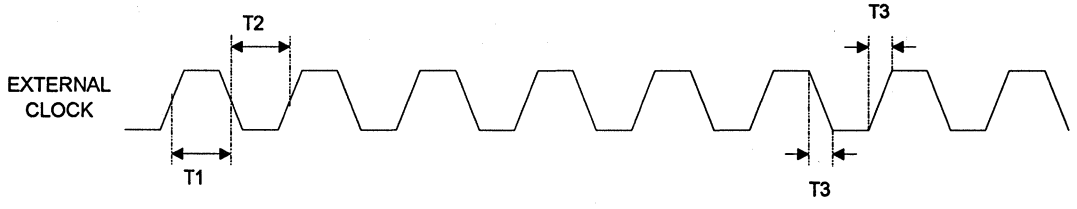


ST16C552

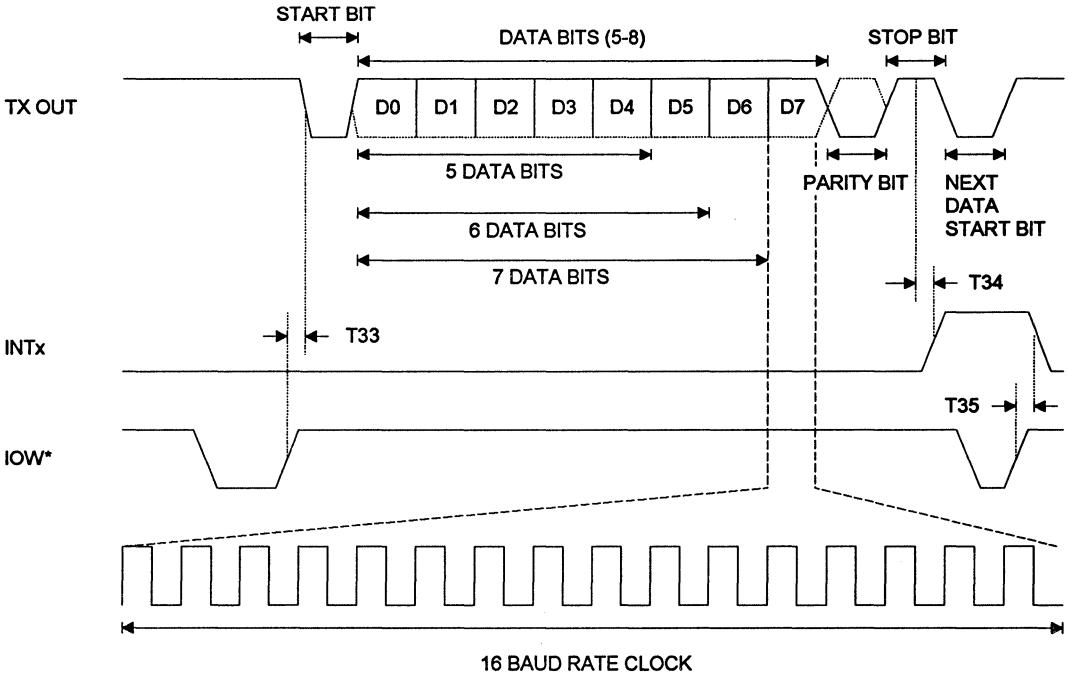
MODEM TIMING



CLOCK TIMING

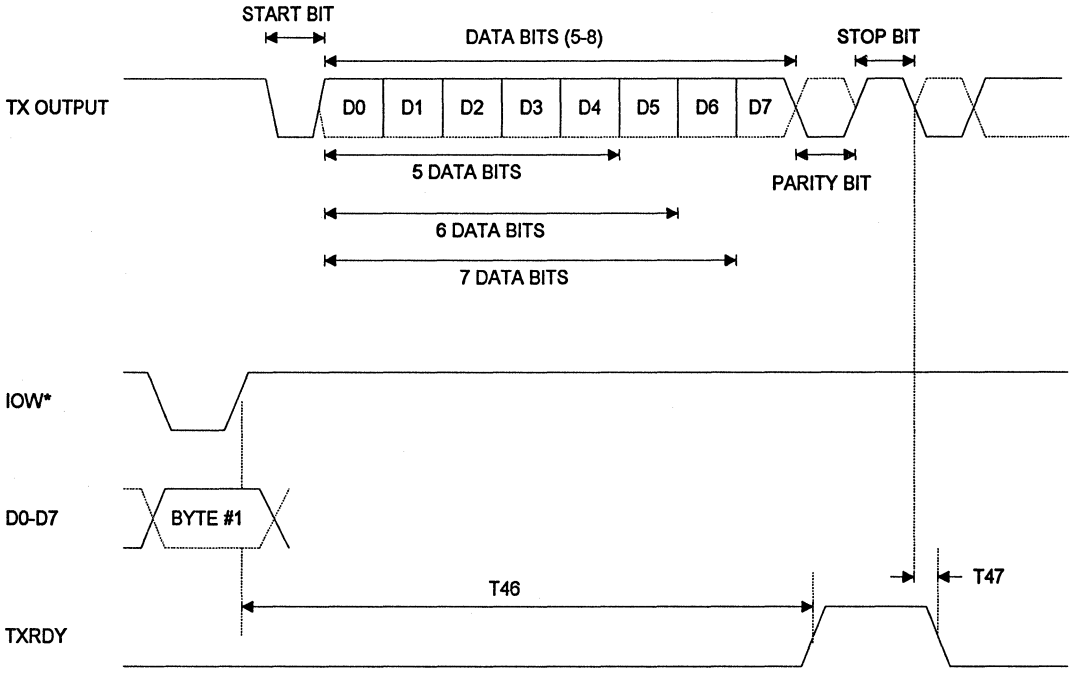


TRANSMIT TIMING

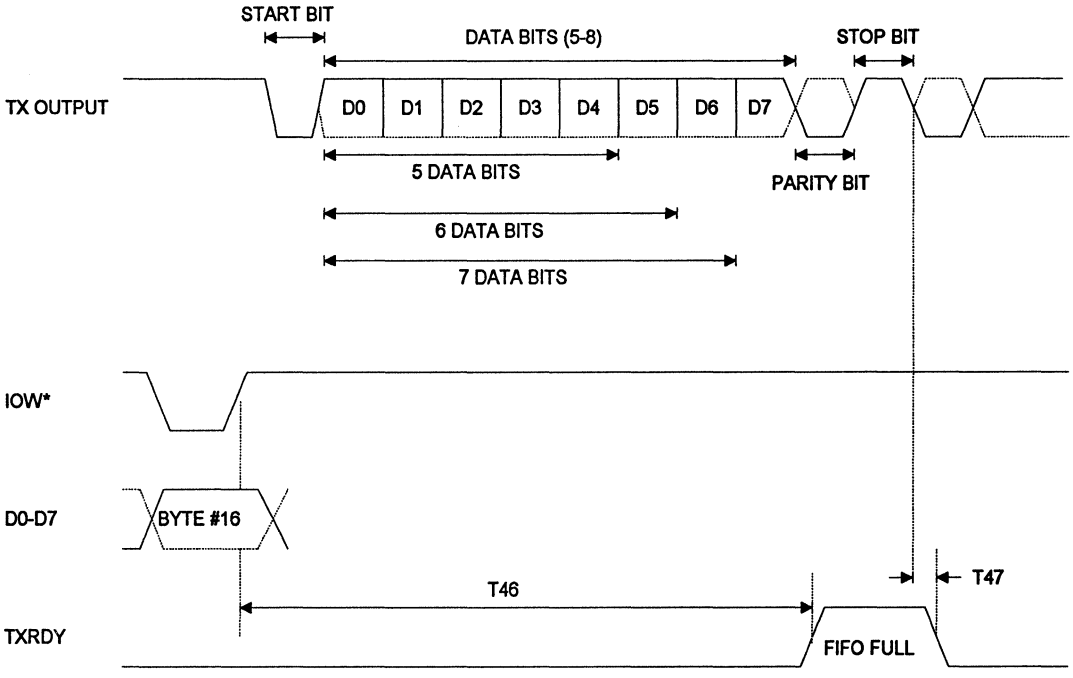


ST16C552

TXRDY TIMING FOR MODE "0"

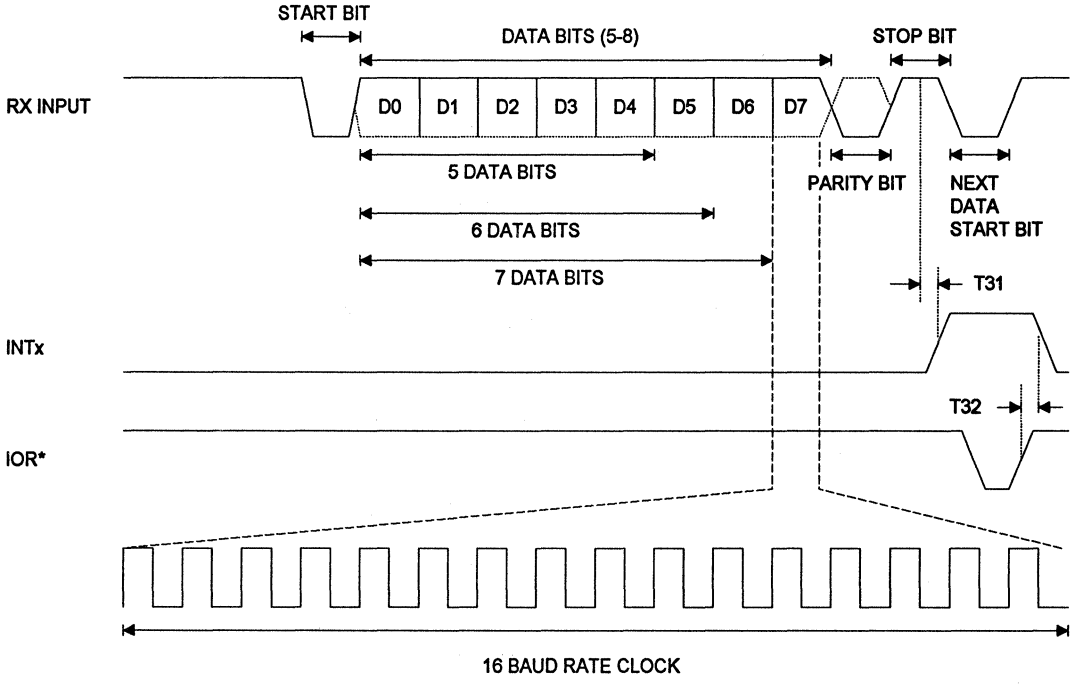


TXRDY TIMING FOR MODE "1"

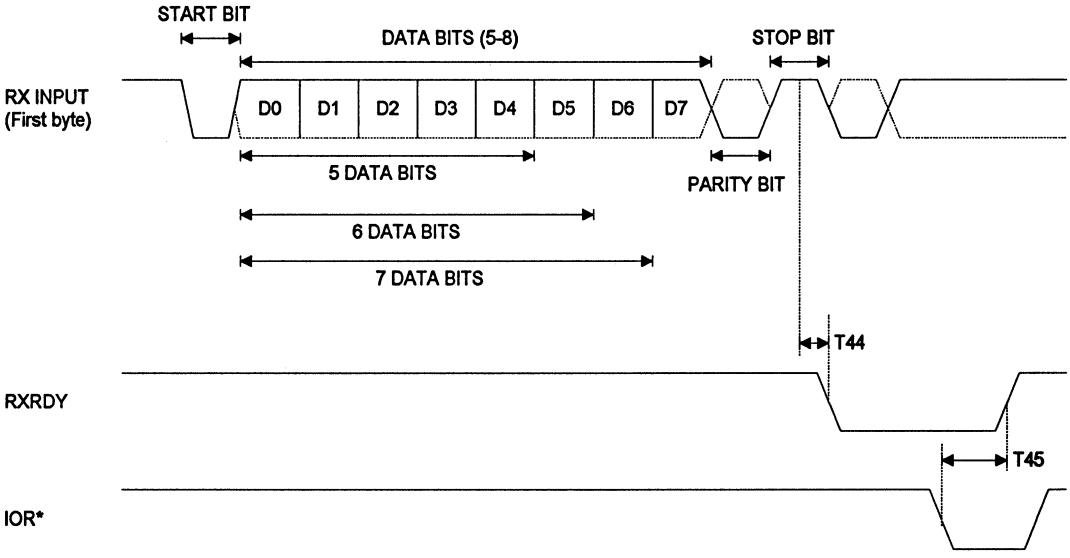


ST16C552

RECEIVE TIMING

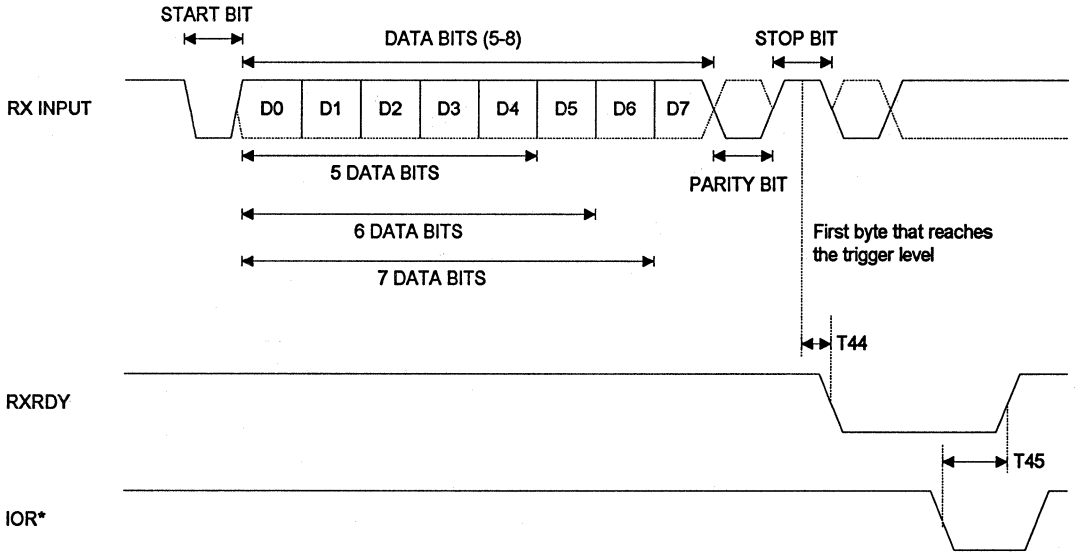


RXRDY TIMING FOR MODE "0"

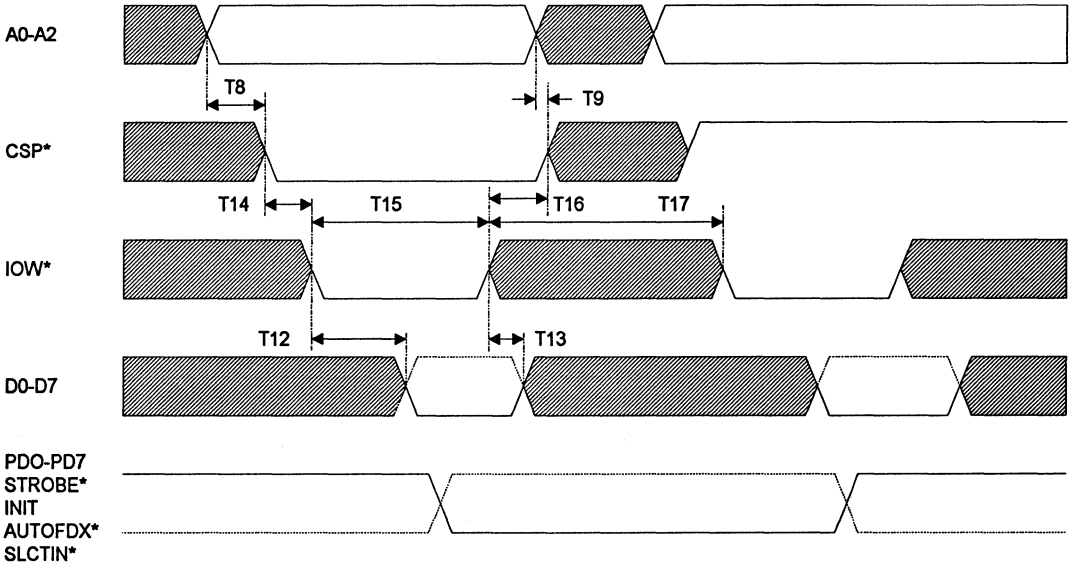


ST16C552

RXRDY TIMING FOR MODE "1"

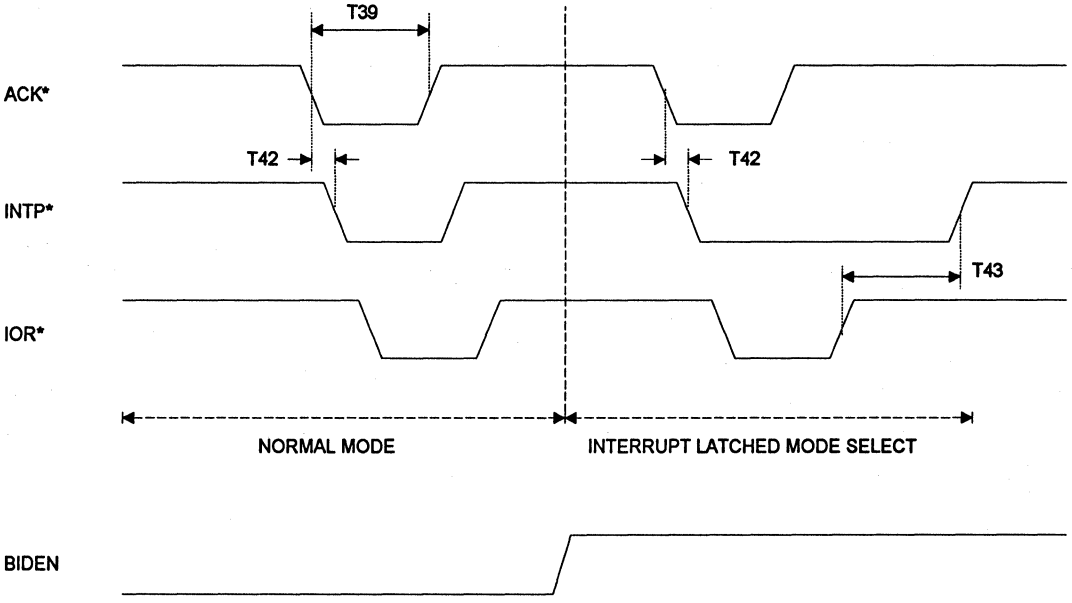


PARALLEL PORT GENERAL WRITE TIMING



ST16C552

PARALLEL PORT READ TIMING



STARTECH

ST16C553

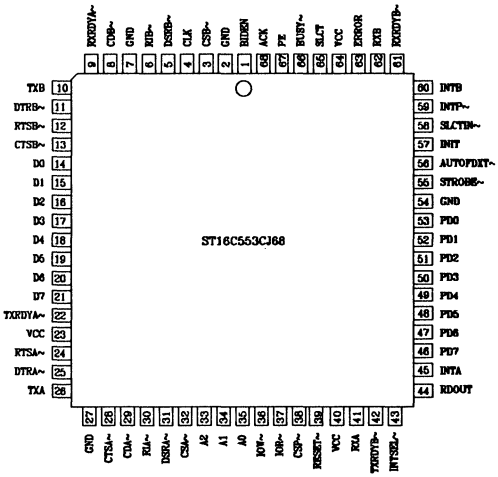
APR 1992

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT WITH 83 BYTE FIFO

DESCRIPTION

The ST16C553 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bidirectional CENTRONICS type parallel printer port with 83 byts of FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.
The ST16C553 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C553 provides internal loopback capability for on board diagnostic testing.
The ST16C553 is fabricated in an advanced 1.2 µ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

* Pin to pin and functional compatible to VL16C552, WD16C552
* 16 byte transmit FIFO
* 16 byte receive FIFO with error flags
* 83 bytes of printer output FIFO
* Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
* Programmable character lengths (5, 6, 7, 8)
* Even, odd, or no parity bit generation and detection
* Status report register
* Independent transmit and receive control
* TTL compatible inputs, outputs
* Software compatible with INS8250, NS16C550
* 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
* Bidirectional hardware/software parallel port
* Bidirectional I/O ports

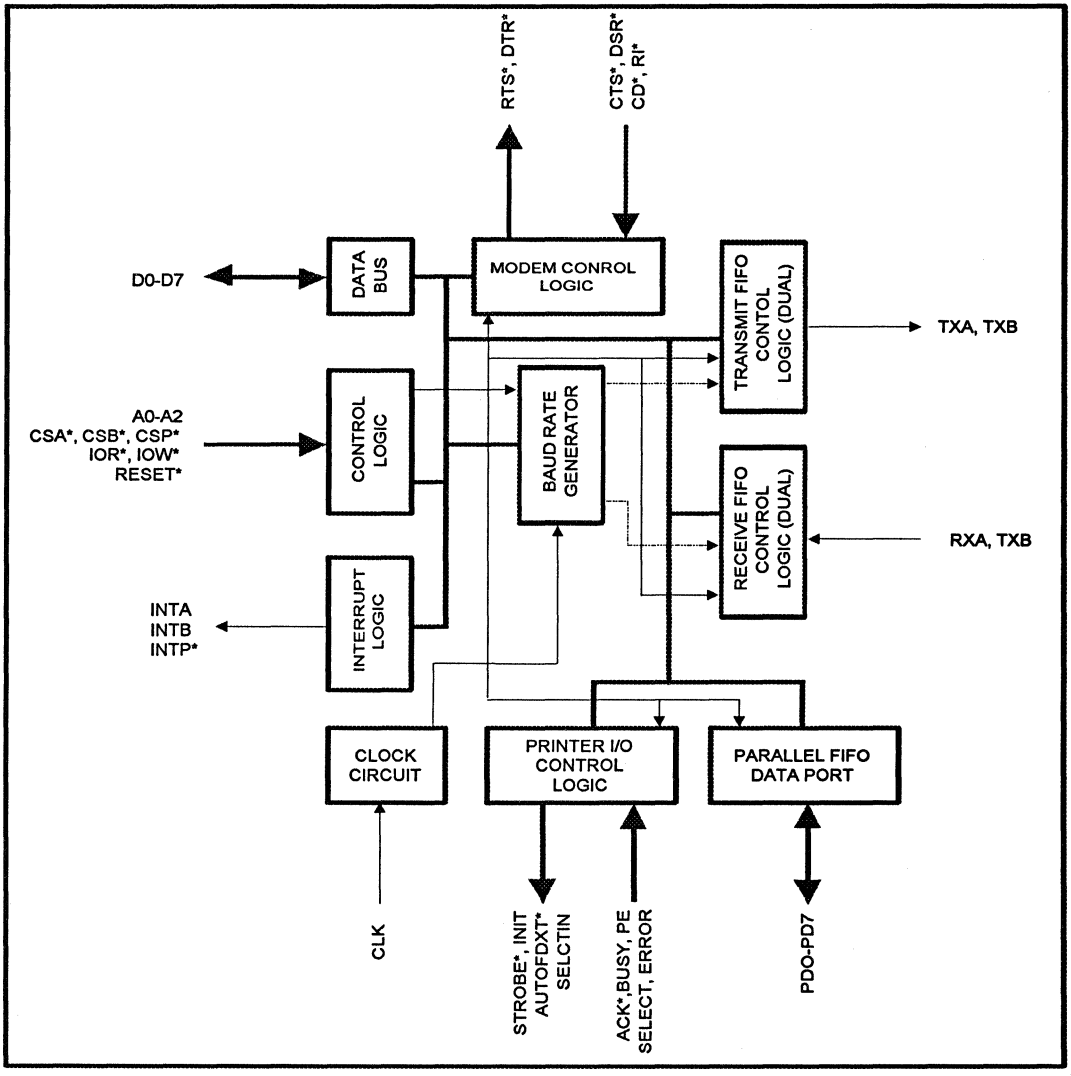
ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C553CJ68	PLCC	0° C to + 70° C

*Industrial operating rage are available

ST16C553

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	14-21	I/O	Bidirectional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2	35-33	I	Address select lines. To select internal registers.
CLK	4	I	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN	1	I	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C553 to output mode.
IOW*	36	I	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	37	I	Read strobe (active low). A low level on this pin transfers the contents of the ST16C553 data bus to the CPU.
RDOUT	44	O	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C553 to en/disable the external transceiver or logics.
RESET*	39	I	Master reset (active low). A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	I	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

ST16C553

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CD A/B*	29,8	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B	26,10	O	Serial data output A/B. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
DTR A/B*	25,11	O	Data terminal ready A/B (active low). To indicate that ST16C553 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B*	24,12	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Serial data input A/B. The serial information (data) received from serial port to ST16C553 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*	36	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY A/B*	22,42	O	Transmit ready A/B (active low). This pin goes low when the transmit FIFO of the ST16C553 is full. It can be used as a

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			single or multi-transfer.
RXRDY A/B*	9,61	O	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
CSP*	38	I	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	46-53	I/O	Bidirectional parallel ports (three state). To transfer data in or out of the ST16C553 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55	I/O	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	56	I/O	General purpose I/O or line printer autofeed (open drain active low). To signal the printer for continuous form feed.
INIT	57	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	58	I/O	General purpose I/O or line printer select (open drain active low). To select the line printer.
ERROR*	63	I	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65	I	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66	I	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
PE	67	I	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.

ST16C553

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
ACK*	68	I	General purpose input or line printer acknowledge (active low). An output from the printer to indicate that data has been accepted successfully.
INTP*	59	O	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	I	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
GND	2,7,54	O	Signal and power ground.
VCC	23,40,64	I	Power supply input.

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C553 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

ST16C553

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C553 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C553 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C553 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 2 to 2^{16}-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C553 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C553 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	1	1	0	0	RXRDY (Received Data Ready) or receice time out.
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C553 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signalling.

FCR BIT-0:
0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

ST16C553

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0=normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch enable (DLEN).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
Not used.

MCR BIT-3:
0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

MCR BIT-4:
0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. ST16C553 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a

ST16C553

control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C553 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C553 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

ST16C553 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
RTS*	High
DTR*	High
INT	Three state mode
RXRDY*	High
TXRDY*	High

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output.

PRINTER PORT REGISTER DESCRIPTIONS

PRINTER FUNCTIONAL DESCRIPTION

The ST16C553 printer section is designed to operate as normal printer interface without any additional settings for the printer FIFO. Contents of the FIFO will be cleared after reset or toggling the INT line to low state. The ST16C553 will monitor the ACK* input pin for FIFO operation, as soon as first ACK* received from printer, auto FIFO mode will trigger the FIFO operation and the user can load up to 83 bytes of data by monitoring the status register for ACK* and BUSY* signals. The FIFO data will transfer to printer at printer loading speed. The ST16C553 provides 83 bytes of FIFO for output direction to the printer only.

PORT REGISTER

Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

ST16C553

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	X	Input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER

Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"
Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C553 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7	High, output mode
STROBE*	High, output mode
AUTOFDXT*	High, output mode
INIT	Low, output mode
SLCTIN*	High, output mode

ST16C553

ST16C553

ST16C553 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt 0= Interrupt		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDXT*	STROBE*
	0=Output 1=Input		0=INTP output disabled 1=INTP output enabled				

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	60			ns	
T_2	Clock low pulse duration	60			ns	External clock
T_3	Clock rise/fall time	10			ns	
T_8	Chip select setup time	25			ns	
T_9	Chip select hold time	0			ns	
T_{11}	IOR* to drive disable delay			35	ns	100 pF load
T_{12}	Address hold time from IOW*	5			ns	
T_{13}	IOW* delay from address	25			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	5			ns	
T_{17}	Write cycle delay	55			ns	
Tw	Write cycle=T_{15}+T_{17}	135			ns	
T_{19}	Data hold time	25			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	75			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	50			ns	
Tr	Read cycle=T_{23}+T_{25}	135			ns	
T_{26}	Delay from IOR* to data			75	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{Rclk}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{38}	Delay from rising IOW* to output data	5			ns	
T_{39}	ACK* pulse width	75			ns	

3

ST16C553

ST16C553

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_{40}	PD7 - PD0 setup time	10			ns	
T_{41}	PD7 - PD0 hold time	25			ns	
T_{42}	Delay from ACK* low to interrupt low	5			ns	
T_{43}	Delay from IOR* to reset interrupt	5			ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			1	µs	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		2^{16}-1		

Note 1 *Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

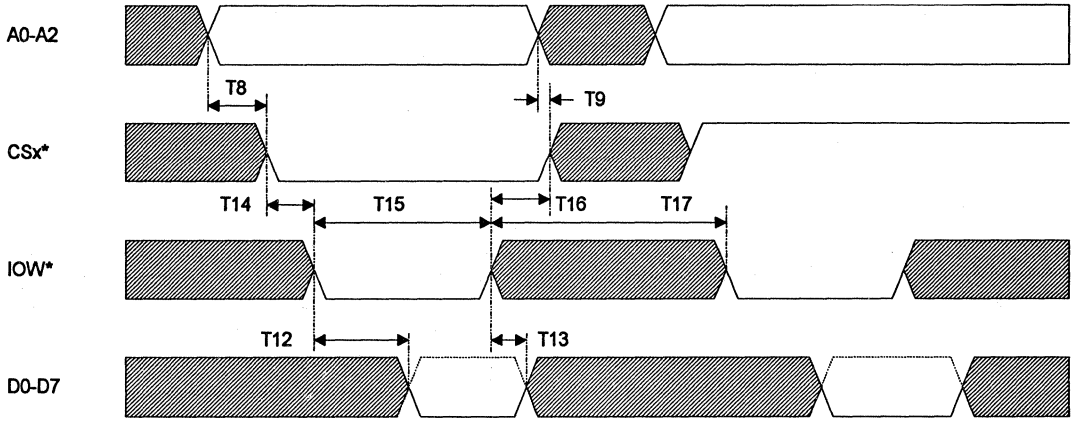
DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

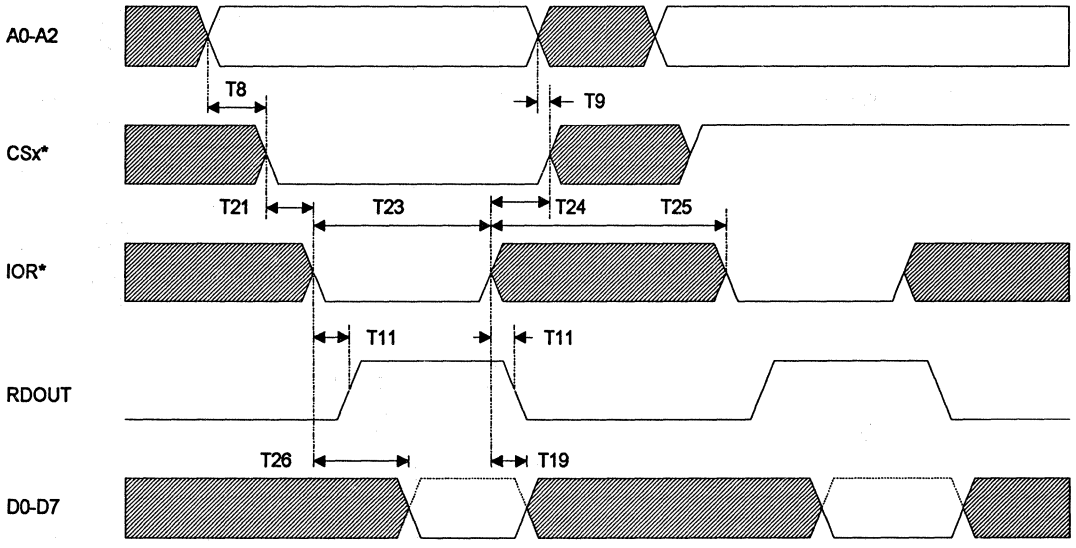
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level			0.4	V	I_{OL}= 6.0 mA D7-D0 I_{OL}= 20.0 mA PD7-PD0 I_{OL}= 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL}= 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH}= -6.0 mA D7-D0 I_{OH}= -12.0 mA PD7-PD0 I_{OH}= -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH}= -6.0 mA on all othe outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

ST16C553

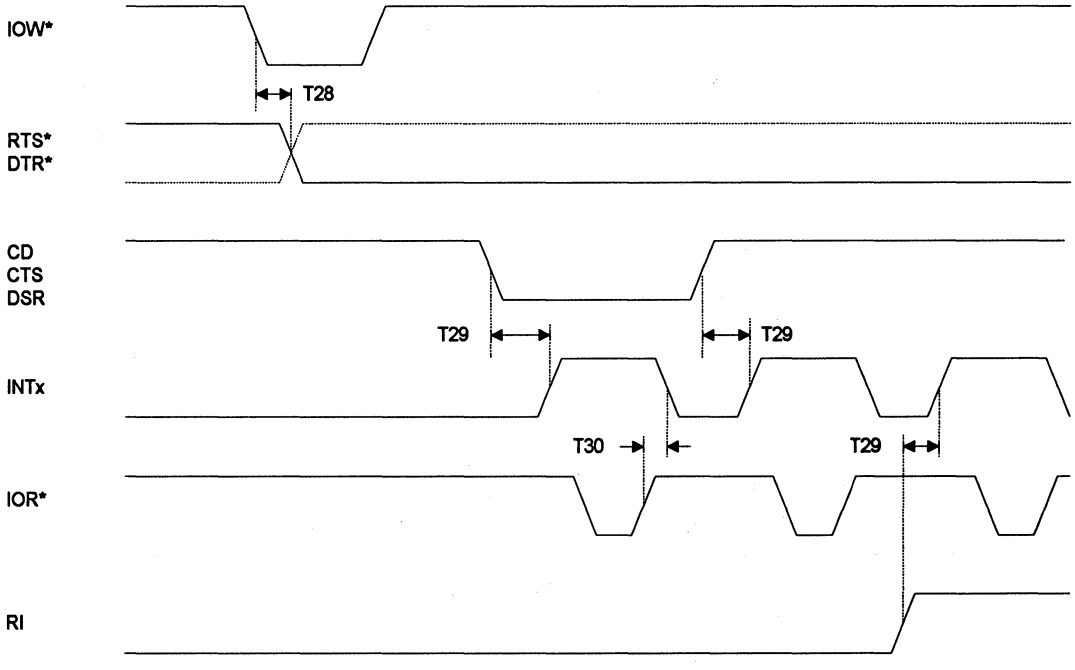
GENERAL WRITE TIMING



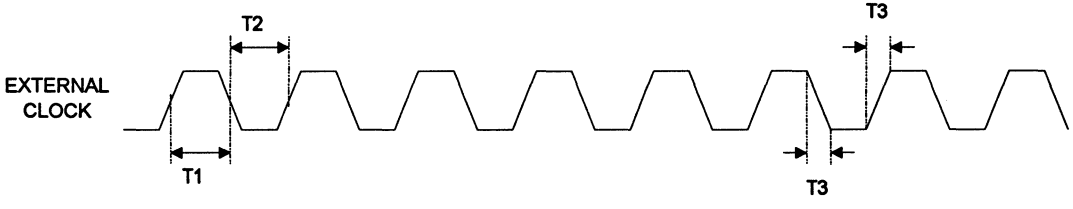
GENERAL READ TIMING



MODEM TIMING

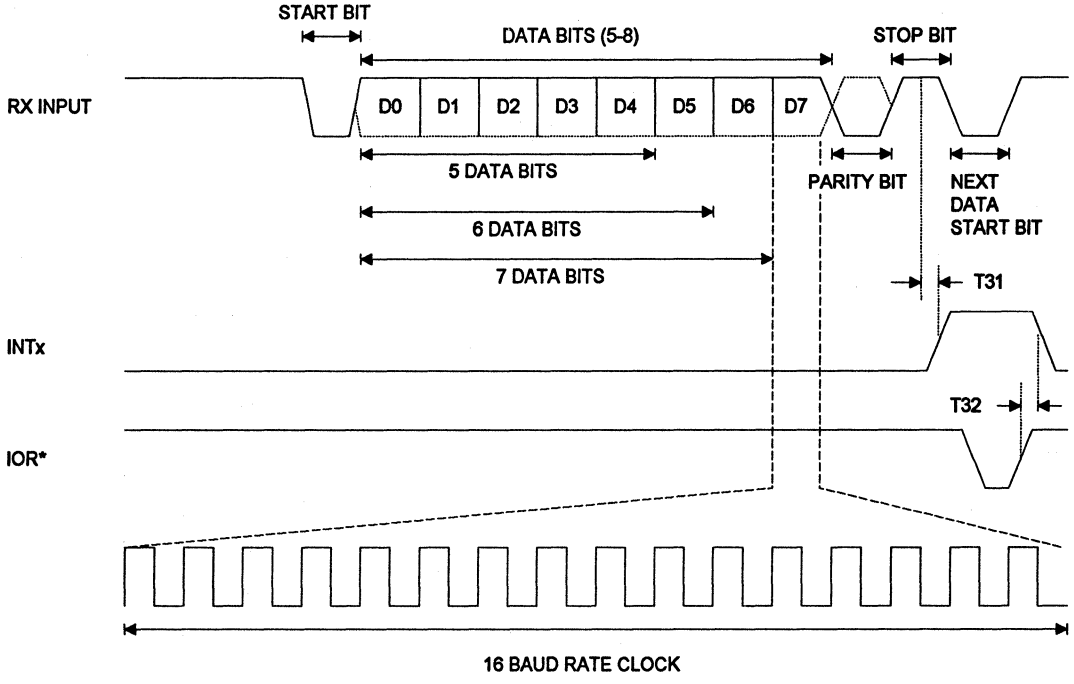


CLOCK TIMING

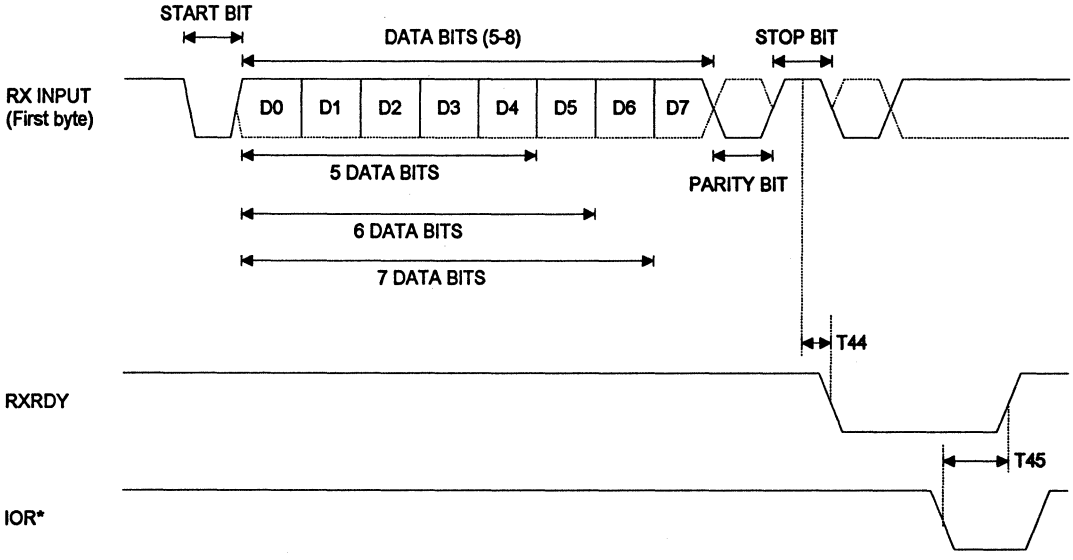


ST16C553

RECEIVE TIMING

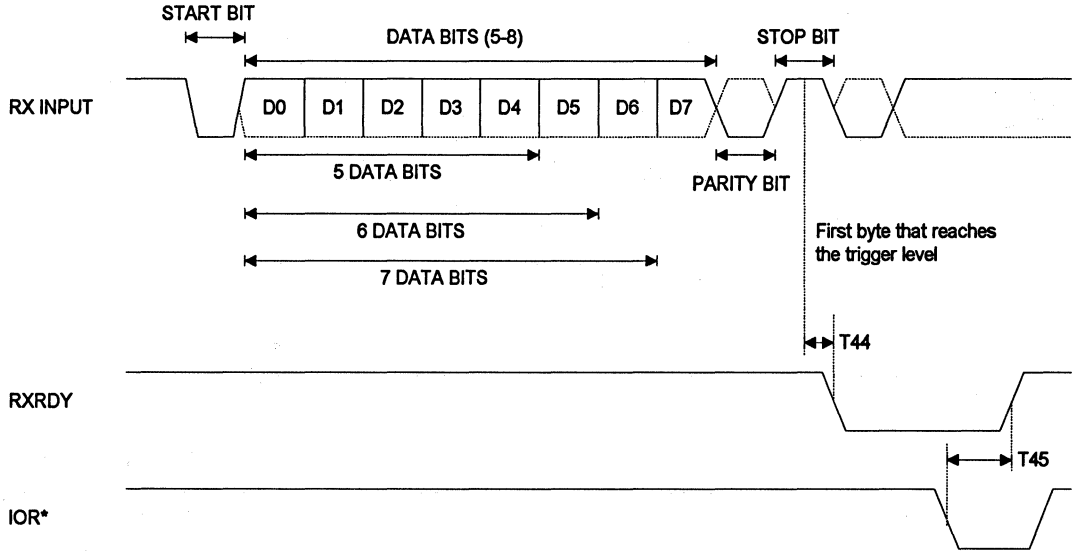


RXRDY TIMING FOR MODE "0"

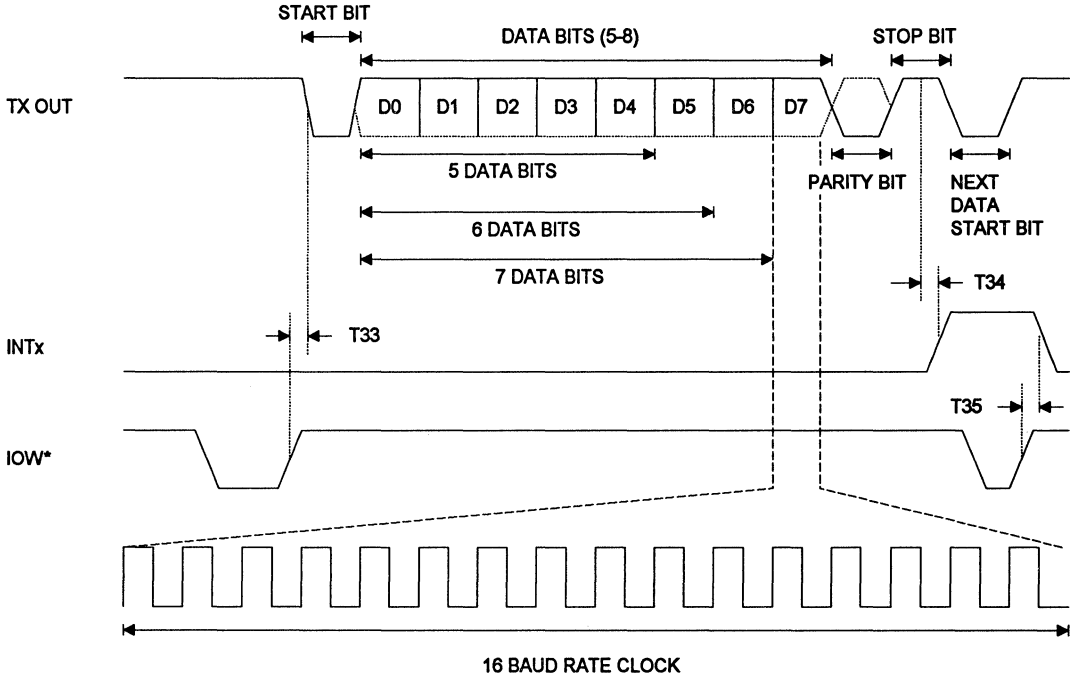


ST16C553

RXRDY TIMING FOR MODE "1"

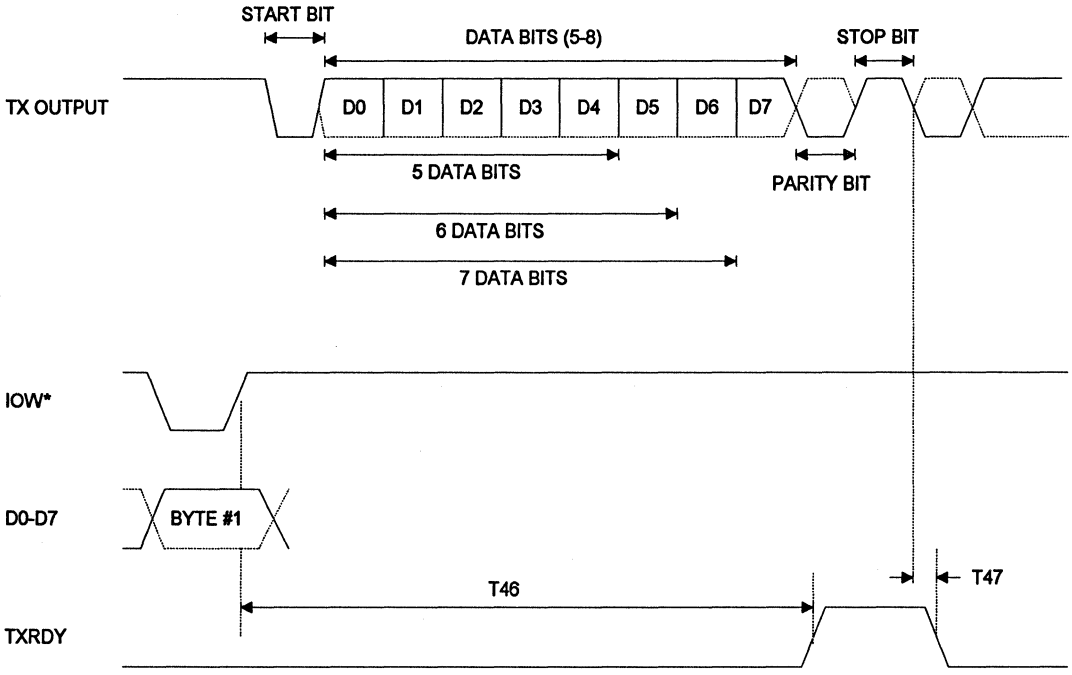


TRANSMIT TIMING

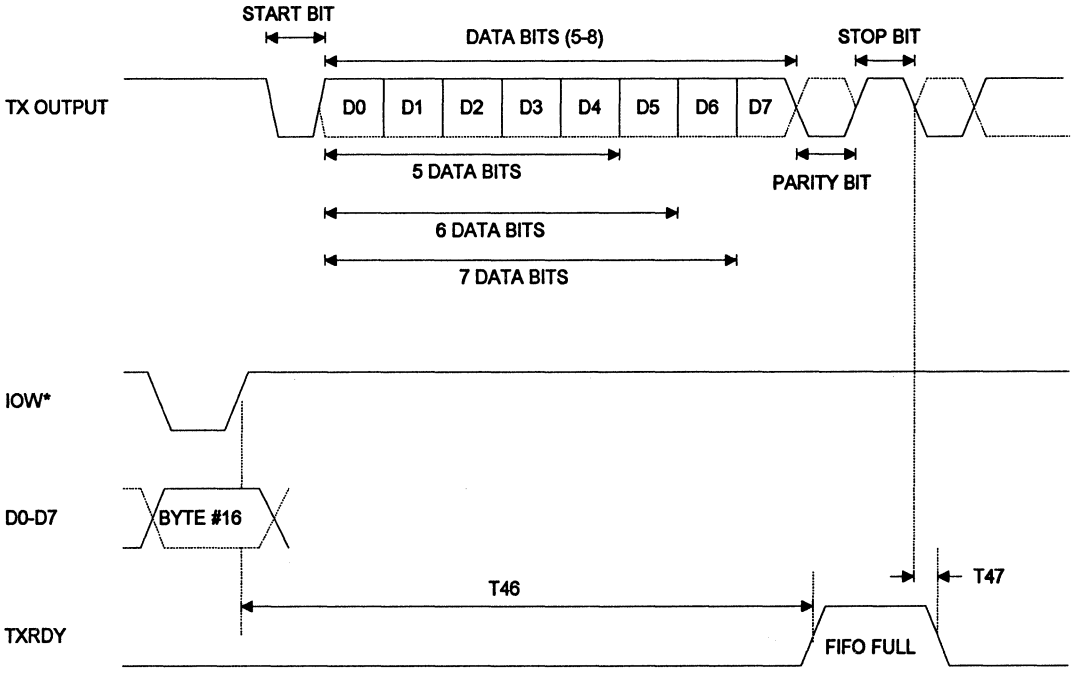


ST16C553

TXRDY TIMING FOR MODE "0"

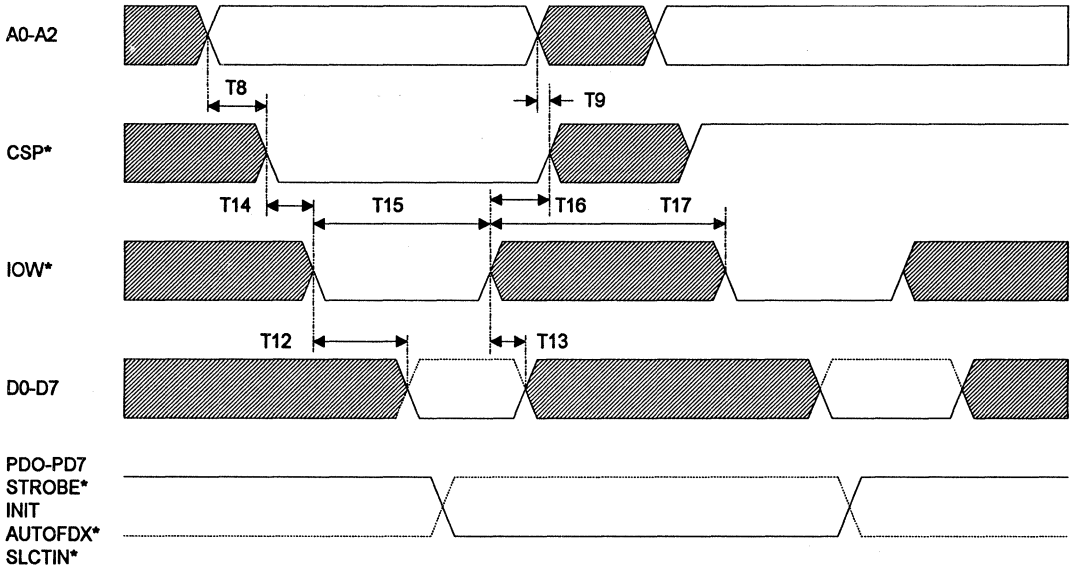


TXRDY TIMING FOR MODE "1"

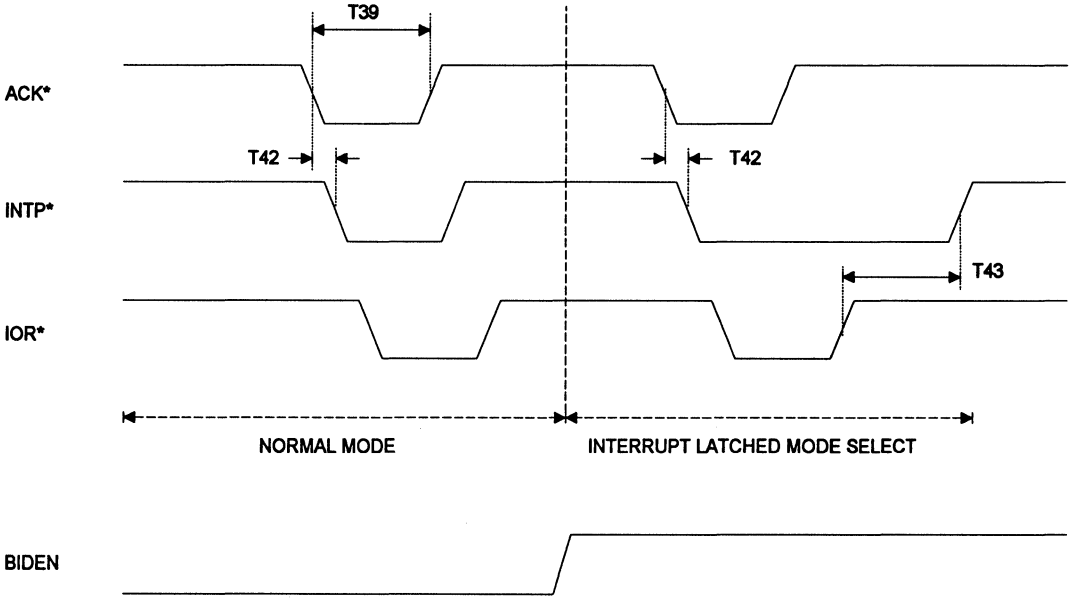


ST16C553

PARALLEL PORT GENERAL WRITE TIMING



PARALLEL PORT READ TIMING



ST16C553

COMMUNICATIONS

Index

STARTECH *Priliminary*

ST78C35

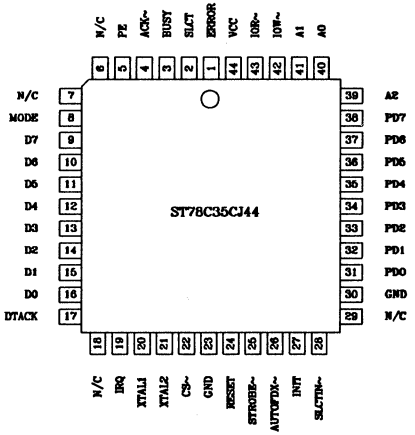
APR 1992

GENERAL PURPOSE INPUT/OUTPUT PORT WITH 128 BYTE FIFO

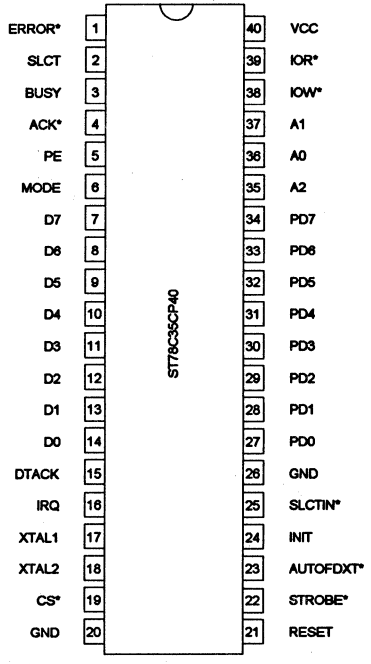
DESCRIPTION

The ST78C35 is a monolithic Bidirectional Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port.
The ST78C35 is a general purpose input/output controller with 128 byte internal FIFO. FIFO operation can be enabled or disabled and configured for either direction. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.
The ST78C35 is designed to operate as normal printer interface without any additional settings. Contents of the FIFO will be cleared after reset or setting the INIT pin to a low state. The auto FIFO operation starts after the first ACK* is received from the printer. Contents of the FIFO transfer to the printer at the printer loading speed. The ST78C35 FIFO can operate as input or output by setting the port direction.

PLCC Package



Plastic-DIP Package



FEATURES

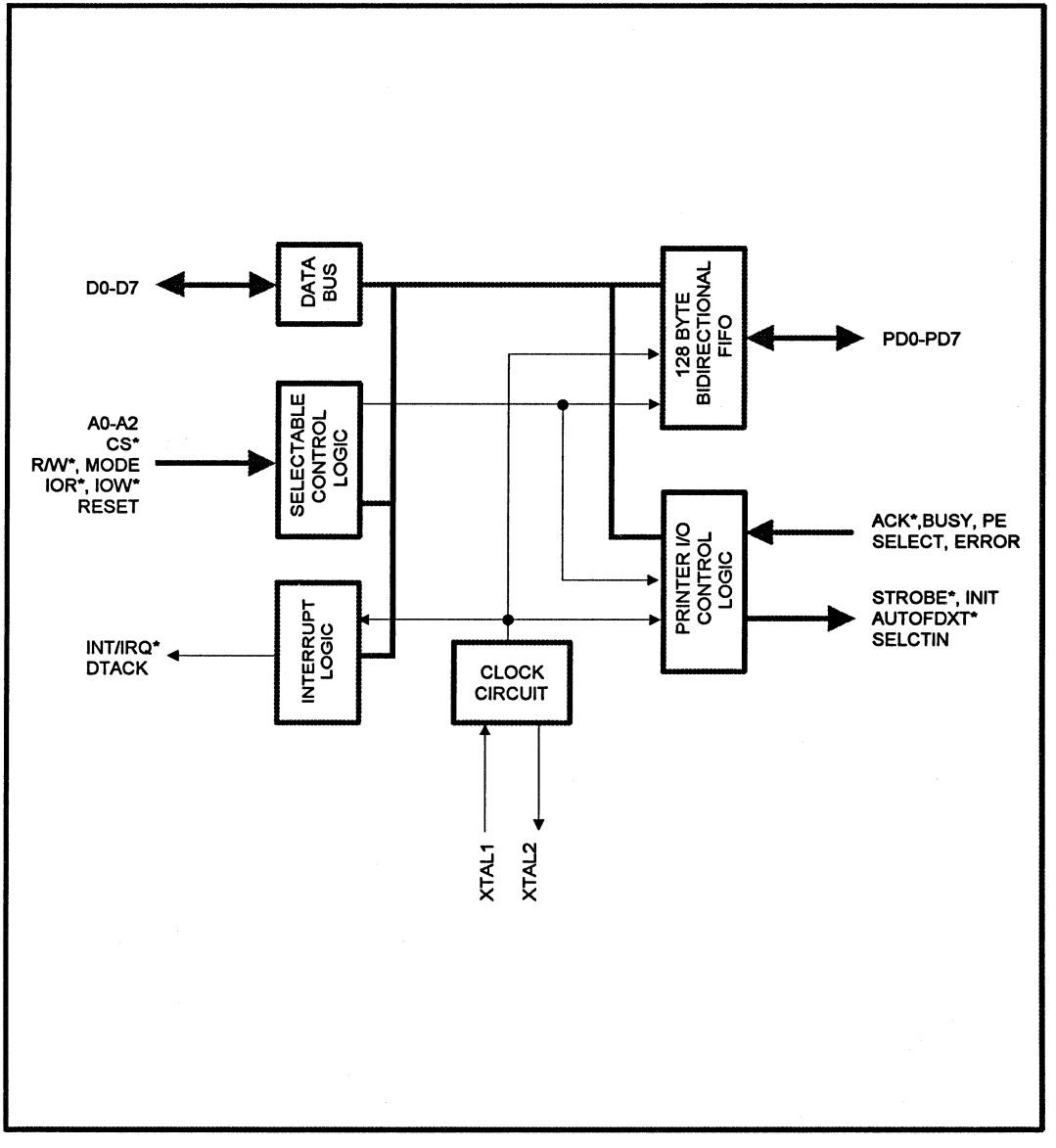
* 128 Byte input/output FIFO
* 5 General purpose input ports
* 8 Bidirectional ports
* 4 Open drain input/output ports
* Replaces all TTL logic for IBM printer port
* IBM printer port register compatible
* 4 User programmable strobe pulse widths
* Selectable FIFO trigger level
* Intel / Motorola bus compatible

ORDERING INFORMATION

Part number	Package	Operating temperature
ST78C35CJ44	PLCC	0° to + 70° C
ST78C35CP40	Plastic-DIP	0° to + 70° C

ST78C35

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
ERROR	1	I	General purpose input or CENTRONICS ERROR input pin.
SLCT	2	I	General purpose input or CENTRONICS SLCT input pin.
BUSY	3	I	General purpose input or CENTRONICS BUSY input pin.
ACK*	4	I	General purpose input or CENTRONICS ACK* input pin.
PE	5	I	General purpose input or CENTRONICS PE input pin.
MODE	8	I	Intel / Motorola Bus select. ST78C35 is set to Intel bus format when this pin is connected to VCC and Motorola bus format when this pin is connected to GND.
D7-0	9-16	I/O	Data bus.
DTACK	17	O	Data acknowledge output. This pin goes low when data has been accepted by ST78C35.
IRQ	19	O	Interrupt output. Three state output when not enabled. Polarity of this pin can be selected via setup register bit-7.
XTAL1	20	I	Crystal or External clock input. Crystal connection between XTAL1 and XTAL2 input/output pins.
XTAL2	21	O	Crystal output pin.
CS*	22	I	Chip select input. Read and write operation to ST78C35 is active when this pin is low.
GND	23	O	Supply ground pin.
RESET	24	I	Reset input pin. Polarity of this pin changes when ST78C35 is configured for Intel or Motorola bus format. This pin is active high when Intel format is selected and active low when Motorola bus format is selected.
STROBE*	25	O	General purpose open drain output or CENTRONICS STROBE* output pin.

* 44-pin PLCC package

ST78C35

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
AUTOFDX*	26	O	General purpose open drain output or CENTRONICS AUTOFDX* output pin.
INIT	27	O	General purpose open drain output or CENTRONICS INIT output pin.
SLCTIN*	28	O	General purpose open drain output or CENTRONICS SLCTIN* output pin.
GND	30	O	Supply ground pin.
PD7-PD0	38-31	I/O	General purpose input/output ports or CENTRONICS DATA port.
A2	39	I	ST78C35 A2 address line.
A0	40	I	ST78C35 A0 address line.
A1	41	I	ST78C35 A1 address line.
IOW*	42	I	Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. This pin is used as R/W* in Motorola bus format.
IOR*	43	I	Read strobe. A low on this pin will read contents of addressed register.
VCC	44	I	Power supply input pin.

* 44-pin PLCC package

PORT REGISTER
Bidirectional I/O or printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER
This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK* input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK* input state.
0= ACK* input is in low state
1= ACK* input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

COMMAND REGISTER
The state of the four open drain output pins (STROBE*, AUTOFDXT*, INIT, SLCTIN*), and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE* input pin.
0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:
AUTOFDX* input pin.
0= AUTOFDX* pin is in high state
1= AUTOFDX* pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN* input pin.
0= SLCTIN* pin is in high state
1= SLCTIN* pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt is disabled
1= Interrupt is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

4

CONTROL REGISTER.
Writing to this register will set the state of the four open drain output pins (STROBE*, AUTOFDXT*, INIT, SLCTIN), and interrupt mask register.

CON BIT-0:
STROBE* output control bit.
0= STROBE* output is set to high state
1= STROBE* output is set to low state

CON BIT-1:
AUTOFDX* output control bit.
0= AUTOFDX* output is set to high state
1= AUTOFDX* output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

ST78C35

CON BIT-3:
SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:
Interrupt output control bit.
0= IRQ output pin is disabled. Set to three state
1= IRQ output pin is enabled

CON BIT-5:
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

SETUP REGISTER
This register sets the ST78C35 operating conditions.

STR BIT-0:
FIFO select bit.
0=FIFO disable (default)
1=FIFO enabled (128 bytes)

STR BIT1-2:
Interrupt source select bits.

STR-2	STR-1	CONDITIONS
0	0	Single character interrupt (ACK*)
0	1	FIFO empty interrupt
1	0	Programmable trigger level interrupt
1	1	FIFO full interrupt

STR BIT3-4:
Strobe width select bits.

STR-4	STR-3	CONDITIONS
0	0	Strobe width=1µs
0	1	Strobe width=2µs
1	0	Strobe width=5µs
1	1	Strobe width=10µs

STR BIT-6:
Interrupt vector select bit.
0=Normal interrupt output. Contents of the interrupt register is read when Address 01 Hex is read.
1=Interrupt vector source selected. Contents of the interrupt vector register is read when Address 01 Hex is read.

STR BIT-7:
Interrupt polarity select bit.
0=Interrupt output pin is active low.
1=Interrupt output pin is active high.

FIFO STATUS REGISTER
This register provides the FIFO enable/disable and FIFO counter location.

FSR bit-0:
0=FIFO disabled
1=FIFO enabled

FSR1-7:
In Use FIFO locations in Hex format.

FIFO INTERRUPT TRIGGER REGISTER
User selectable software control FIFO trigger level interrupt select register.

FIT BIT-0:
0=Normal. Interrupt selected from setup register
1=FIFO trigger level. ST78C35 interrupt output is set when FIFO count reached to FIFO trigger level.

ST78C35

FIT BIT1-7:
FIFO trigger select level in Hex format.

USER DEFINED INTERRUPT VECTOR REGISTER
ST78C35 provides user defined interrupt service jump routine.

IVR BIT0-7:

PRINTER PORT PROGRAMMING TABLE:

A2	A1	A0	IOW*	IOR*
0	0	0	PORT REGISTER	PORT REGISTER
0	0	1		STATUS REGISTER
0	1	0	CONTROL REGISTER	COMMAND REGISTER
0	1	1	SETUP REGISTER	SETUP REGISTER
1	0	0	FIFO INTERRUPT TRIGGER REGISTER	FIFO STATUS REGISTER
1	0	1	INTERRUPT VECTOR REGISTER	INTERRUPT VECTOR REGISTER

ST78C35

ST78C35 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT	ERROR STATE	IRQ	1	1

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO-FDX*	STROBE*
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO-FDX*	STROBE*
	0=Output 1=Input		0=IRQ output disabled (three state) 1=IRQ output enabled				

SETUP REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
IRQ POLARITY	INTERRUPT VECTOR	STROBE	STROBE WIDTH SEL.	INTERRUPT WIDTH SEL.	INTERRUPT SOURCE	FIFO SOURCE	EN/DIS

FIFO INTERRUPT TRIGGER REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
FIFO TRIGGER-6	FIFO TRIGGER-5	FIFO TRIGGER-4	FIFO TRIGGER-3	FIFO TRIGGER-2	FIFO TRIGGER-1	FIFO TRIGGER-0	INTERRUPT TYPE

FIFO STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
FIFO COUNT-6	FIFO COUNT-5	FIFO COUNT-4	FIFO COUNT-3	FIFO COUNT-2	FIFO COUNT-1	FIFO COUNT-0	FIFO STATUS

INTERRUPT VECTOR REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
INTERRUPT VECTOR-7	INTERRUPT VECTOR-6	INTERRUPT VECTOR-5	INTERRUPT VECTOR-4	INTERRUPT VECTOR-3	INTERRUPT VECTOR-2	INTERRUPT VECTOR-1	INTERRUPT VECTOR-0

ST78C35

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		

ABSOLUTE MAXIMUM RATINGS

Operating supply range	7 Volts ± 5%
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.3		0.6	V	
V_{IHCK}	Clock input high level	3.0		Vcc	V	
V_{IL}	Input low level	-0.3		0.8	V	
V_{IH}	Input high level	2.2		Vcc	V	
V_{OL}	Output low level			0.4	V	I_{OL} = 6.0 mA D7-D0 I_{OL} = 20.0 mA PD7-PD0 I_{OL} = 10 mA SLCTIN*, INIT*, STROBE*, AUTOFDXT* I_{OL} = 6.0 mA on all other outputs
V_{OH}	Output high level	2.4			V	I_{OH} = -6.0 mA D7-D0 I_{OH} = -12.0 mA PD7-PD0 I_{OH} = -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH} = -6.0 mA on all other outputs
I_{CC}	Avg power supply current			12	mA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	

4

STARTECH

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ST84C72

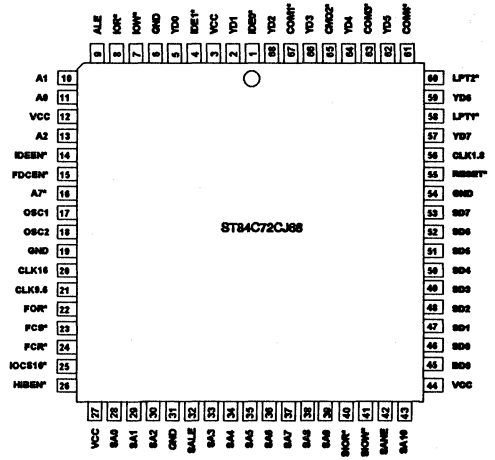
APR 1992

IDE INTERFACE WITH I/O DECODE

DESCRIPTION

The ST84C72 is designed to replace all necessary TTL logics for 16 bit IDE interface and decode logic for floppy controller and serial / parallel I/O ports. A select pin is provided to select primary or secondary address for hard and floppy decodes. On board crystal oscillator circuit provides 16, 9, and 1.8432 MHz clock outputs for some floppy controllers and uart from 48 MHz external crystal connected to ST84C72.

PLCC package



FEATURES

* Low power CMOS design
* Direct bus connect
* Replacement for more than 7 TTL parts
* High speed for new design
* Selectable I/O decode ports. (COM1-CMO4, LPT1-LPT2)
* Floppy address decode
* Pin selectable primary and secondary address decodes

ORDERING INFORMATION

Part number	Package	Operating temperature
ST84C72CJ68	PLCC	0 ° C to +70 ° C

APPLICATION NOTES

GENERAL APPLICATION NOTE FOR STARTECH UART FAMILY

The AN-450 provides additional information to guide users to design or utilize the STARTECH product line. This document can also be used for all the STARTECH UART product lines.

GENERAL INFORMATION

STARTECH offers UART's with or without FIFO capabilities, and are marked as 45X for non FIFO families and 55X for FIFO families. All parts with sharing part numbers are foot print compatible in some extent, like ST16C450 and ST16C550, ST16C2450 and ST16C2550, etc.

This section will describe general terms for commonly used flags and registers.

OVERRUN ERROR:
The flag is set to "1" to warn the user that a serial data has been received and previous serial data has not been read from receive holding register. The new serial data will over write the previous data in the receive holding register. Note that previous serial data has been lost and user does not have an access to that data.

PARITY ERROR:
This flag is set "1" to indicate that received serial data contains mismatched parity or data bit error in the received data.

PARITY:
Four common types of parities are used in the START-ECH Uart families; Odd Parity, Even Parity, Forced Mark Parity and Forced Space Parity.

ODD PARITY:
Odd Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the total count an odd number.

Example -1: A data byte with the following pattern 11010010 will require to add a parity bit of "1" to bring the total count for "1's" to an odd number. Based on this data pattern, serial data with odd parity will be transmitted as 110100101.

Example -2: A data byte with the following pattern 10011000 will require to add a parity bit of "0" to maintain the total count of "1's" to an odd number. Based on this data pattern, serial data with odd parity will be transmitted as 100110000.

EVEN PARITY:
Even Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the count an even number.

Example -3: A data byte with the following pattern 10000101 will require to add a parity bit of "1" to bring the total count for "1's" to an even number. Based on this data pattern, serial data with even parity will be transmitted as 100001011.

Example -4: A data byte with the following pattern 00001111 will require to add a parity bit of "0" to maintain the total count for "1's" to an even number. Based on this data pattern, serial data with even parity, will be transmitted as 000011110.

FORCED SPACE PARITY:
Parity bit on the serial byte is set to "0" regardless of total number of "1's" (even or odd counts).

FORCED MARK PARITY:
Parity bit on the serial byte is set to "1" regardless of total number of "1's" (even or odd counts).

FRAMING ERROR:
The flag is set to "1" to indicate that received data does not have correct start or stop bits. This can cause when the Uarts are set for 8-bits word and receiving a serial data of 7-bits word or any mismatched data patterns.

BREAK SIGNAL INDICATION:
This flag is set to "1" to warn the user that transmitter is sending continuous "0" data without stop bit (RX input is low for more that one word).

TRANSMIT/RECEIVE FIFO:
STARTECH offers 16 byte transmit FIFO and 16 byte receive FIFO for all its products with 55X part numbers. These FIFO's are static 19 X 16 bit RAM with control logic to form a ring counter. Initializing the FIFO will set the write and read pointers to the same location.

TRANSMIT EMPTY:
This flag is set "1" to indicate that, there is no character in the transmit holding and transmit shift register

APPLICATION NOTES

TRANSMIT HOLDING EMPTY:
This flag is set "1" to indicate that, there is one or more empty locations in the transmit holding register. User has to check this bit before loading characters in the transmit holding register. In non FIFO mode, user can load one character at a time when this flag is set and 16 characters when FIFO mode is utilized.

RECEIVER DATA READY:
This bit is set "1" to indicate that, receiver has one or more character in the receive holding register. User has to check this bit prior to read receive holding register. In non FIFO mode, only one character at time can be read. In FIFO mode up to 16 characters can be read if time bit is set.

RECEIVE TIME-OUT:
This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -7: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -8: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

BAUD RATE GENERATOR:
STARTECH provides a 16 bit digital divider to obtain all necessary baud rates. The 16 bit divider is broken down in to two 8-bit dividers which will be addressed as MSB divider (upper 8-bits) and LSB divider (lower 8-bits). To calculate the transmit/receive data rate it is necessary to know the provided clock rate (frequency) to START-ECH parts. STARTECH utilizes 16 clocks for each transmit bit and 16 clocks to sample the received data. Note that inorder to access these dividers, user has to enable the divisor latch access bit through the Line Control Register.

Bit rate is calculated by:
Dividing decimal number = (Clock rate) / (16 X bit rate).
To program the digital divider, dividing decimal number should be converted to hex (base 16) number and split into two 8-bits sections.

Example -5: To obtain 4800 Hz baud rate, assuming 1.8432 MHz input clock, the dividing decimal value is (input clock=1843200) / (16 X 4800) = 24

24 decimal = 0018 Hex, this value is translated to MSB = 00 Hex and LSB = 18 Hex.

BAUD RATE VERSUS BIT RATE:
The baud rate defines the width of each bit regardless of word, parity and stop bit length. Bit rate, is the rate of the transmission which each character is transmitted or received. The 2400 baud rate transmission is translated to 2400 Hz per bit for each character in a word. With 2400 baud you can transmit between 7 to 12 characters per slot.

PROGRAMMING STEPS:
The AN-450 provides the easy steps to program STARTECH Uart family. Note that all numbers are in Hex format not decimal.

Write 80 Hex to **LCR** (Line Control Register) to enable baud rate generator divider latch
to set 2400 Hz baud rate:
write 00 Hex to MSB of baud rate generator (address location 1).
Write 30 Hex to LSB of baud rate generator (address location 0).

Select you word, parity and stop bit format from START-ECH Uart data sheet.
to set 8 bits, no parity and one top bit and disable the divisor access latch
write 03 Hex to **LCR** (Line Control Register):

if you need to use Uarts with FIFO, select your receive trigger level from data sheet.

to enable FIFO with 14 character trigger level
write CF Hex to **FCR** (FIFO Control Register)

enable interrupt sources
write 01 Hex to **IER** (Interrupt Enable Register) to select receive interrupt.

to set RTS and DTR outputs to low and enable the interrupt output
write 0B Hex to **MCR** (Modem Control Register).

The STARTECH Uart is ready for transmit and receive operation.

Read **MSR** (Modem Status Register) to check the status of **CD, RI, DSR, CTS** input pins.

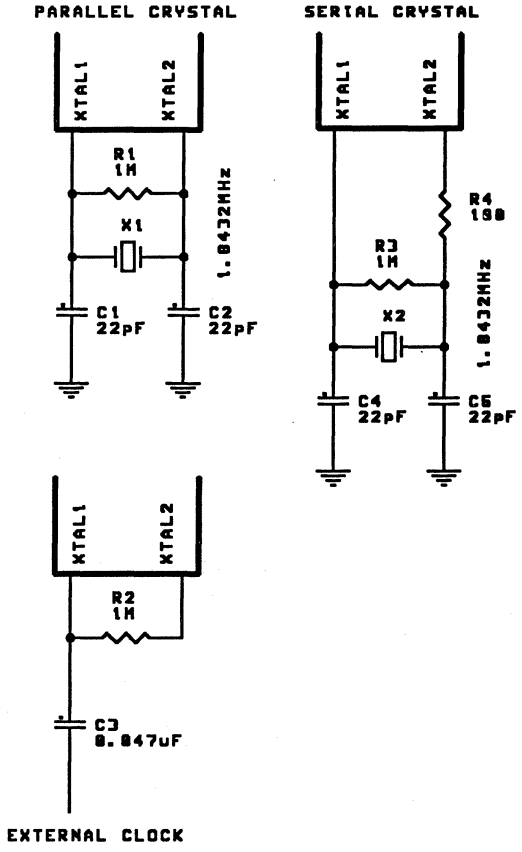
Read **LSR** (Line Status Register).

For polling applications (non interrupt mode) user has to monitor bit zero of this register to verify valid data in the receive holding register.

Check the Transmit Holding Empty bit before loading data in the transmit holding register,

continue the transmission.

Crystal/External clock connections



APPLICATION NOTES

```
; File: sample.c        Package:UART init
; This is a sample code to show how to initialize the UART series of chips
; from Startech Semiconductors.
; This also includes some basic external loop back thru' two different
; ports using the FIFO capability.
; This also includes external loop back thru a different computer

#include    <stdio.h>
#include    <string.h>
#include    <fcntl.h>

#define     TRUE            1
#define     FALSE           0

/* These are the various offsets for the registers inside the chip */
#define     RHR             0x00 /* Receive Holding Register   */
#define     THR             0x00 /* Receive Holding Register   */
#define     IER             0x01 /* Interrupt Enable Register  */
#define     FCR             0x02 /* FIFO control Register      */
#define     ISR             0x02 /* Interrupt Status Register  */
#define     LCR             0x03 /* Line control register      */
#define     MCR             0x04 /* Modem Control Register     */
#define     LSR             0x05 /* Line Status Register       */
#define     MSR             0x06 /* Modem Status Register      */
#define     SCR             0x07 /* Scratch pad Register       */

/* This two offsets are used for defining the baud rate      */
#define     DIVLSB          0x00 /* Divisor LSB latch address  */
#define     DIVMSB          0x01 /* Divisor MSB Latch address  */

/*\
 * Program table for baud rate
 * This represents the LSB and MSB divisor latch data
\*/
char baud_table[8][2] = {
        { 0x80, 0x01 },             /* 300  */
        { 0x60, 0x00 },             /* 1200 */
        { 0x30, 0x00 },             /* 2400 */
        { 0x0c, 0x00 },             /* 9600 */
        { 0x06, 0x00 },             /* 19K  */
        { 0x03, 0x00 },             /* 38k  */
        { 0x02, 0x00 },             /* 56k  */
        { 0x01, 0x00 }              /* 115k */
};
```

```
/* Baud Rates */
#define     _COM_300_          0
#define     _COM_1200_         1
#define     _COM_2400_         2
#define     _COM_9600_         3
#define     _COM_19K_          4
#define     _COM_38K_          5
#define     _COM_56K_          6
#define     _COM_115K_         7

/* Parity */
#define     _COM_NOPARITY_     0
#define     _COM_ODDPARITY_    1
#define     _COM_EVENPARITY_   2

/* Stopbits */
#define     _COM_STOP1_        0
#define     _COM_STOP2_        1
#define     _COM_STOP1_5_      1

/* word length */
#define     _COM_CHR5_         0
#define     _COM_CHR6_         1
#define     _COM_CHR7_         2
#define     _COM_CHR8_         3

/* word length */
#define     _COM_FIFO1_        0
#define     _COM_FIFO4_        1
#define     _COM_FIFO8_        2
#define     _COM_FIFO14_       3

/*\
 * This function checks the existence of a port.
 * It is very simple. Take the port address then write to the scratch pad
 * an the read it back. If the data read back the same as one that was
 *written then return TRUE else return FALSE.
\*/
int
check_port(com_port)
int com_port;
{

  int i;
```

```
    printf("Checking for port %4xH\n",com_port);
  /* Write 1010 1010 (0xaa) to scratch pad*/

    printf("Writing AAH in %4xH\n",com_port);
  outportb(com_port + SCR, 0xaa);

  /* read it back. If it the same then return TRUE */
  i = inportb(com_port + SCR);

    printf("Read back %2xH from %4xH\n",i,com_port);

  if( i == 0xaa)
      return TRUE;
  else
      return FALSE;

}

/*\
 * This is the work horse function which actually setups the UART.
 * It needs to know every thing.
\*/
int
init_uart(port,baud,parity,data,stop,fifo,trigger)
int port,baud,parity,data,stop,fifo,trigger;
{

  char lcr_byte;

  /* Set divisor latch */
  outportb(port+LCR, 0x80) ;

  printf("Divisor Latch is %2xH %2xH (High Low)\n",
                        baud_table[baud][1],baud_table[baud][0]);
 outportb(port+DIVLSB, baud_table[baud][0]) ;
 outportb(port+DIVMSB, baud_table[baud][1]) ;


  /* Reset to normal Programming */
  /* Program the lcr_byte for the above parameters */
  lcr_byte = 0x00;
  lcr_byte = data; /* Set the  bit0 & bit1 for word length */
  lcr_byte ;= stop << 3; /* Set the bit2 for stop bit */
  if(parity != _COM_NOPARITY_) {
     lcr_byte ;= 1 << 4;  /* Set the bit3 for parity */
     if(parity == _COM_EVENPARITY_)
```

```
        lcr_byte ;= 1 << 5; /* Set the bit4 for EVEN parity */
    }

    printf("LCR byte is %2xH\n",lcr_byte);
    /* Program LCR */
    outportb(port+LCR, lcr_byte) ;

    if(fifo) {
     char fifo_byte;

     printf("Programming FIFOs without DMA mode\n");

     /* Have to first set the fifo enable */
     fifo_byte = 0x01;
     outportb(port+FCR,fifo_byte);

     /* Now program the FIFO */
     fifo_byte = 0x07; /* set bit0 - FIFO enable, Reset RCVR and XMIT FIFO */
     fifo_byte ;= trigger << 7; /* set bit6 and bit7 with the trigger level */

     /* Program FCR */
     outportb(port+FCR,fifo_byte);
     if(~(inportb(port + ISR) & 0xc0)) {
         printf("This port %4xH does not have FIFOs\n");
         printf("Hence did not program Enable FIFOs\n");
     }
    }

    /* Program IER */
    printf("Programming IER for interrupt on bit0 RCV holding Register\n");
    outportb(port+IER, 0x01);

    return TRUE;
}

/*\
 * This is the test mode.
 * It gets the address of the ports checks to see if they are there.
 * Note: If a driver already exists I am not sure how to temporarily remove it.
 * Well we will worry about it later.
 * Warn the use to remove any drivers that are on the ports.
 * Especially the mouse driver.
 * pass the address to the test552 routine.
\*/
int test_mode()
{
```

```
    int i,j,k; /* generic variables */
    char port1[10], port2[10];
    int pt1,pt2;  /* this are the integer port numbers */

    void test552();

    printf("WARNING: This program will not work if the ports to be tested\n");
    printf("       have drivers installed in them. e.g Mouse driver\n");
    printf("       Please remove the drivers before doing this test.\n");

    while(TRUE) {
      printf("First Port Address (In HEX) > ");
      scanf("%s",port1);
      pt1 = strtol(port1,NULL,16);
      fflush(stdin);
      /*\
       * Check if this port exists. else loop
      \*/
      if(check_port(pt1))
          break;
      printf("Error: Port %4xH does not exist. Try again\n",pt1);
    }


    while(TRUE) {
      printf("Second Port Address (In HEX) > ");
      scanf("%s",port2);
      pt2 = strtol(port2,NULL,16);
      fflush(stdin);
      /*\
       * Check if this port exists. else loop
      \*/
      if(check_port(pt2))
          break;
      printf("Error: Port %4xH does not exist. Try again\n",pt2);
    }

    /* Test 554 with the two port addresses */
    test552(pt1,pt2);

    return TRUE;

}
```

```
/*\
 * It first generates a random number for the data size to be generated.
 * Then generates a random data whose length is equal to the data size.
 * It puts it out on both the ports and polls for the interrupt to occur.
 * It reads both the ports until all characters are received OR a timeout
 * has occured. It then prints out the error Messages if any.
 * This loop is done for ever.
\*/
void test552(p1,p2)
unsigned int p1, p2;
{
  int i,j,c,w,n;
  unsigned char outbuf[20], inbuf1[20], inbuf2[20];
  unsigned char pbuf[200];
  unsigned long timeout, pass;


  printf("ST16C552 External Loop Test Beginning\n") ;
  printf("Testing ports %4x and %4x\n\n", p1, p2) ;
  printf("Programing ports for 56K,8 bit,no parity,1 stop bit,FIFO trigger level 01\n");
  printf("This program uses POLLED mode for testing\n");
  printf("Press Cntrl-C to stop the testing and quit\n");
  printf("Note: The ports will remain at the above settings after the TEST\n");

  /* Programming ports for 8 bits, no parity, 56K baud,
                              FIFO enabled at level 01 */
  /* Program first port */
  printf("Programming port %x4\n",p1);
init_uart(p1,_COM_56K_,_COM_NOPARITY_,
        _COM_CHR8_,_COM_STOP1_,TRUE,_COM_FIFO1_);

  /* Program Second Port */
  printf("Programming port %x4\n",p2);
init_uart(p2,_COM_56K_,_COM_NOPARITY_,
        _COM_CHR8_,_COM_STOP1_,TRUE,_COM_FIFO1_);

  printf("Starting test\n");
  for (pass = 1 ; ; pass++) {
       /* generate random size for data */
       n = rand() ;
       n += n >> 8 ;
       n &= 0x0f ;

       /* Make sure we never get a 0 as the random size data */
       if(n != 0x0f)
         n++ ;
```

```
/* generate random data */
for (w = 0 ; w < n ; w++) {
      c = rand() ;
      c += c >> 8 ;
      c &= 0xff ;
      c ;= 0x01 ; /* no NULLs allowed */
      outbuf[w] = c ;
}
outbuf[w] = NULL;

printf("******** Pass %10ld Sending %d *********\015", pass, n) ;

/* Transmitt the data */
for (i = 0 ; i < n ; i++ ) {
      outportb(p1, outbuf[i]) ;
      outportb(p2, outbuf[i]) ;
}

/* loop waiting for intr pending */
for ( i = 0;;i++ ) {
     if ((~inportb(p1+ISR) & 0x01) && (~inportb(p2+ISR) & 0x01))
           break;
}

/* receive data until all has been received OR timeout */
timeout = 0x0008F ;
for (i = j = 0; ((i < 20) && (j < 20));) {
     if (inportb(p1+LSR) & 0x01) inbuf1[i++] = inportb(p1) ;
      c = rand() ;
      c += c >> 8 ;
      c &= 0x001f ;
      c++ ;
      for ( ; c != 0; c—) ;
     if (inportb(p2+LSR) & 0x01) inbuf2[j++] = inportb(p2) ;
      if (timeout— == 0) break ;
}

/* If timed out then print message else comparse data */
if(timeout == 0 )
      printf("Timed out on Ports\n");
 else {
  inbuf1[i] = inbuf2[j] = NULL;
   /* compare results */
  if (strcmp(outbuf, inbuf1) ;; ( i != n)) {
        printf("\nError:%04x Sent:   ", p2) ;
        for ( w = 0; w < n; w++ )
             printf(" %02x", outbuf[w]) ;
```

```
            printf("\n%04x Received:", p1) ;
            for ( w = 0; w < i; w++ )
                printf(" %02x", inbuf1[w]) ;
            printf("\n") ;
        }
        if (strcmp(outbuf, inbuf2) ;; ( j != n )) {
            printf("\nError:%04x Sent:   ", p1);
            for ( w = 0; w < n; w++ )
                printf(" %02x", outbuf[w]) ;
            printf("\n%04x Received:", p2) ;
            for ( w = 0; w < j; w++ )
                printf(" %02x", inbuf2[w]) ;
            printf("\n") ;
        }
    }
  }
}
```

APPLICATION NOTES

GENERAL APPLICATION NOTE FOR STARTECH CLOCK FAMILY

The ST49CXXX video / memory clock chips provide 1-130 MHz clock outputs which may cause unwanted EMI problems.
To minimize problems with meeting FCC EMI requirements, consideration should be given to the following sections of the board design.

Power supply conditioning
Printed Circuit Board Layout
Video / Memory clock outputs and drive capabilities
External clock sources
Reference clock sources
Digital control / select inputs
External loop filters

Power supply considerations
Some of the ST49CXXX clock chip contained internal loop filters for VCO circuits and some utilize external components. In both cases it is required to have spike free (or minimum) and stable supply source to the chips. To provide stable and clean supply voltage to STARTECH clock chips we recommend to use 0.1 µF capacitors close to IC's power supply lines (VCC, AVCC and DVCC inputs). Analog and digital supply lines are separated from each other to reduce noise generated due to internal digital switching.
In most of the design cases +5V and +12V supplies are provided. A clean +5V supply can be obtained from the +12V supply by utilizing a 470 ohm drop resistor and 5.1V zener diode bypassed by 0.047 µF and 2.2 µF Tantalum capacitors (or higher) to ground.
Trace width should be maximized from the supply source and good ground planes on top and bottom layers of the printed circuit board are recommended.

Printed Circuit Board (PCB) layout
We recommend to place all external components as close as possible to the clock chips to reduce trace length between pin and component connections. It is important to keep components not related to clock ICs (DRAM and other memory devices) far and not share the grounds. In applications utilizing a multi-layer board, GND, AGND, and DGND should be directly connected to the ground plane.

Video / Memory clock outputs and drive capabilities
Video clock is usually the highest frequency present in video graphics system board/card and consideration should be given to FCC EMI requirements.
The trace connecting DCLK and MCLK clock output pins to other components should be kept as close as possible and ferrite beads should be used (with optional 33 ohm resistor in series with ferrite beads) to reduce the possible emitting signals and jitter.

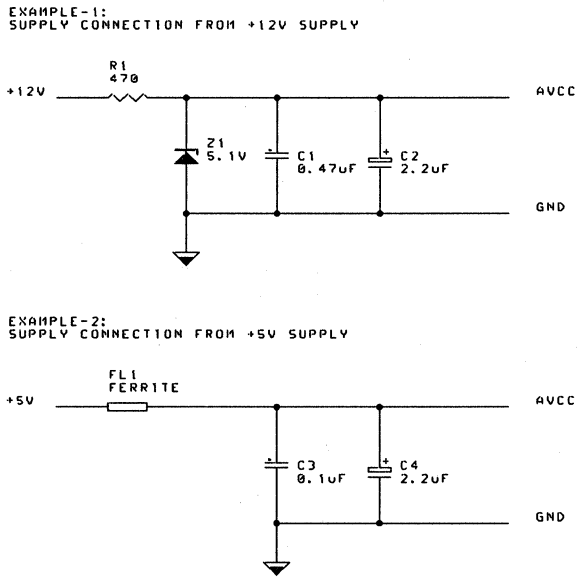
External clock sources
When an external clock source is used to bypass the internal VCO to DCLK and MCLK outputs, clock should have fast rise / fall times and minimum jitter. This signal will be connected internally to the clock output pin when it is selected / enabled. The internal VCO circuit will be locked to its internal selected frequency.

Reference clock sources
The internal oscillator circuit contains all of the passive components required for the external crystal. An appropriate parallel resonant crystal should be connected between XTAL1 and XTAL2.
The crystal leads and input pins should be maintained as close as possible, and the body of the crystal should be grounded to minimize the noise pickup. For IBM compatible applications, the 14.31818 MHz system or crystal clock is used as a reference clock to the chip.

Digital control / select inputs
The ST49CXXX provides TTL compatible address select and latch input pins to interface with CMOS or TTL / LSTTL devices. The A0-A4 and M0-M1 can also be connected to the Data bus if required.

External loop filters
The components values of the filters are critical, especial care must be taken for board layout and selection of the components. Selected components can have 10-20% tolerance for capacitors and 1-5%

tolerance for resistors. These components have to be close to the external loop filter pins and no signal traces should cross close or under these components.



QUALITY/RELIABILITY

QUALITY AND RELIABILITY

The STARTECH semiconductor quality program starts with the design of new products. Each design circuit performance is verified using simulations over voltage and temperature values beyond those of specified product operation.
The design process includes consideration of quality issues such as signal levels, power dissipation, noise generated from internal clock circuits and testability of all device functions.
The STARTECH semiconductor document control department maintains control over all manufacturing specifications, lot travelers, procurement specifications and drawings and test programs.
All changes of design are subject to approval by the Engineering, Quality and Manufacturing managers.

STARTECH semiconductor performs a thorough internal product qualification prior to the delivery of any new product or enhanced existing products other than prototypes/samples.

150 samples from three different product lots are selected to perform extended temperature operation test, 85° C/ 85% R.H. / 5.5V temperature humidity bias. Same samples are used for accelerated burn-in and electro-static tests.

STARTECH semiconductor subcontracts it's fabrication process to ORBIT semiconductor located in Sunnyvale California. packaging and final testing are also subcontracted to other vendors located locally or overseas.

Determination of the Failure Rate
In the simplest form, the failure rate prediction at a given temperature can be predicted as follows.

Failure rate = N/DH

Where:

N = number of failures
D = number of devices
H = number of hours tested

Assuming that semiconductors exhibit a log normal distribution.

Acceleration Factors
The effects of temperature, voltage, time and other related functions are key when predicting life times of semiconductor devices. Understanding these effects with the use of a more accurate mathematical model, provides a better means of evaluating the change in reaction rate to changes in temperature.

$$F(T1, T2) = \exp(-Ea/k\ (1/T1 - 1/T2))$$

Where:

F = Acceleration factor
T1 = Test temperature
T2 = Desired temperature
k = Boltzman's constant (8.63 E-5eV / K)
Ea = Thermal activation energy (eV)

The equivalent device hours can be determined at temperature T2 can be expressed as:

$$EDH\ (T2) = F\ (T1, T2) \times DH\ (T1)$$

The failure rate at T2 can be expressed as:

$$\text{Failure rate } (T2) = N/EDH\ (T2)$$

Where:

N= Number of failures
EDH= Equivalent device hours

Definition and common test methods

Accelerated operating life stress
Accelerated operating life stressing is performed to accelerate failure mechanisms, which are thermally activated, through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications.

85 °C/ 85 % R.H.
85 °C/ 85 % R.H. is an environmental stress performed at a temperature of 85 °C and relative humidity of 85%. The test is designed to measure the moisture resistance of encapsulated devices.

Electrostatic discharge testing
Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device.

CMOS latchup test
CMOS latchup test is performed to determine the sensitivity of a device input to overshoot and undershoot signals connected to device inputs.

STARTECH

Description

Package Pinout

General Information

Device number

Process

Number of gates

Number of transistors

Die size (Mil's)

Mask revision

Production date

Wafer fabrication

Assembly

Testing

Process Information

Process type

Minimum metal width

Passivation material

Bonding picture

Packaging Information

Lead frame material

Outer lead treatment

Inner lead treatment

Bonding wire material

Die attach material

Moulding material

RELIABILITY INFORMATION

A) ELECTRICAL TEST

Test condition: 125 °C

Product date code (year-month)	Sample lot QTY.	Burn-in failures at 48 Hours	Burn-in failures at 192 Hours	Burn-in failures at 500 Hours
9140	70	0	0	0
9201	70	0	0	0
9210	70	0	0	1(1)

1=Input leakage test

B) MECHANICAL TEST

Test condition-1: Pressure pot 125 °C

Product date code (year-month)	Sample lot QTY.	Burn-in failures at 48 Hours	Burn-in failures at 96 Hours
9140	35	0	0
9201	35	0	0
9210	35	0	0

Test condition-2: Pressure pot 250 °C

Product date code (year-month)	Sample lot QTY.	Burn-in failures at 96 Hours	Burn-in failures at 192 Hours
9140	35	0	1(1)
9201	35	0	0
9210	35	0	0

1= Gross functional test, unit recovered at room temperature.

ESD AND LATCH-UP INFORMATION

The specific purpose of this section is to define a practical means of establishing ESD damage levels on integrated circuits using the charged device mode. The primary focus here is on the section of achievable test parameters that will yield repeatable and correctable results.

C) ESD Test

Test condition:
5 pulses at 1 second (typical) duration's, with series resistor of 1.5 kohm and parallel capacitor of 100 pF to ground. C= °C

Product date code	Applied voltage 500 V	Applied voltage 2000 V	Applied voltage 3000 V
9140			pin-18
9201		pin-6	
9210			pin-38

D) LATCH-UP TEST

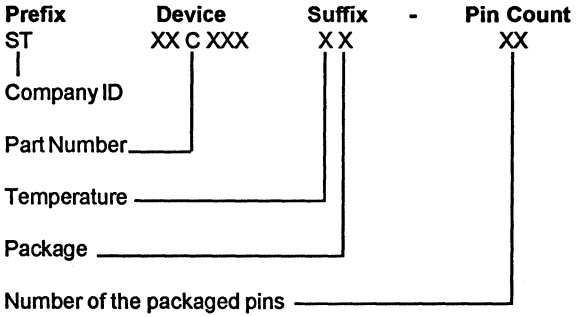
Test conditions:
Current limited to 110 mA and voltage limited to 55 Volts. Positive voltage is applied from 0 to 55 volts and then negative voltage is applied from 0 to -55 volts.

Product date code	Applied voltage Positive	Applied voltage Negative
9201	pin-39 65 mA	

Pins are selected base on their input, output, and I/O devices structures.

ORDERING INFORMATION

ORDERING INFORMATION AND PART NUMBERING GUIDE



Temperature Range

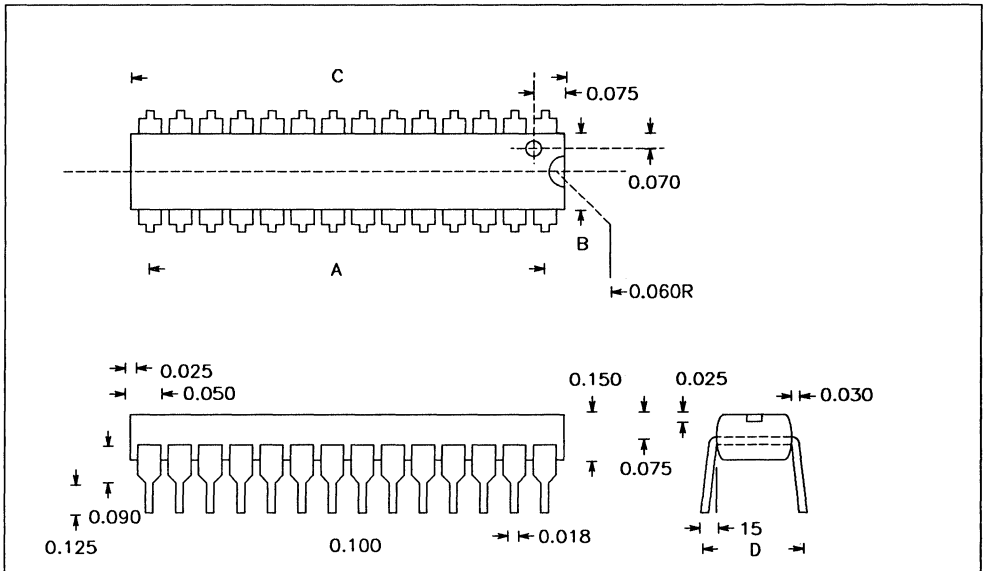
C	Commercial	0° C	To	+70° C
I	Industrial	-40° C	To	+85° C
M	Military	-55° C	To	+125° C

Package Type

P Plastic
C Ceramic
D Cerdip
L Leadless Chip Carrier (LCC)
J Plastic Leaded Chip Carrier (PLCC)
F Flat Pack
Q Quad Flat Pack
G Pin Grid

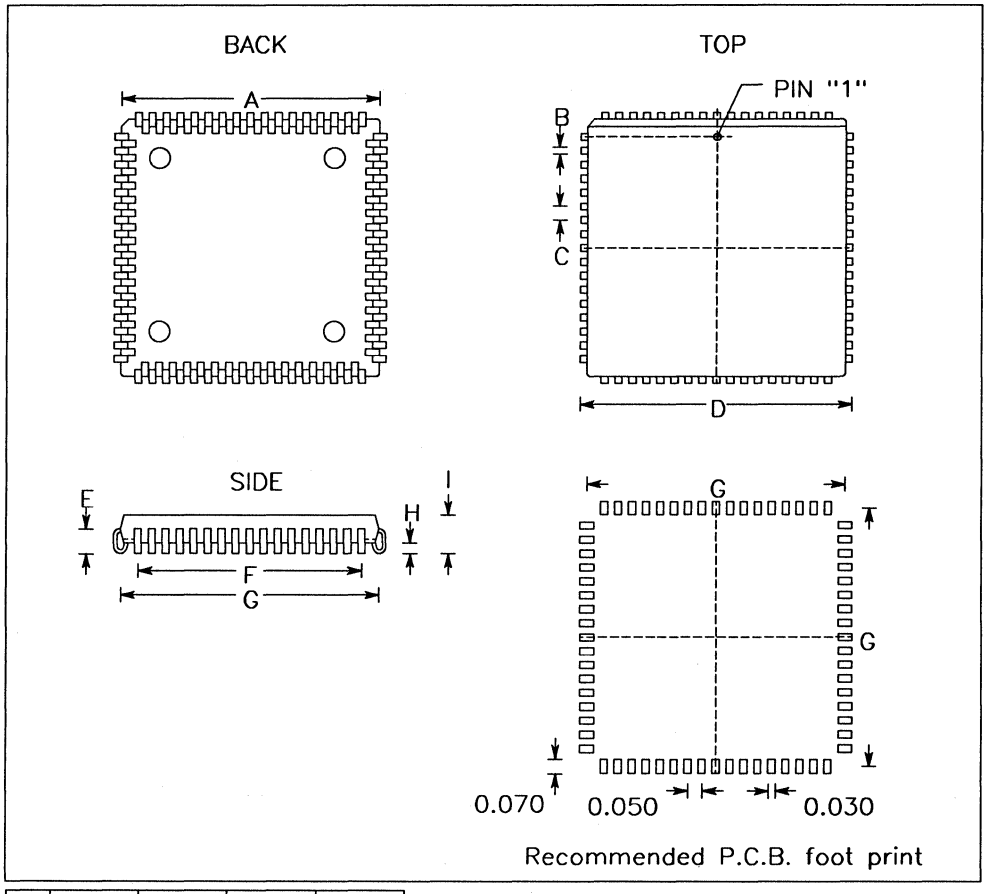
PACKAGING INFORMATION

PLASTIC DIP PACKAGING INFORMATION



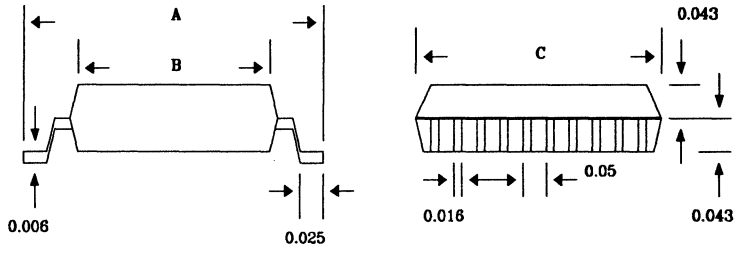
	8PIN	14PIN	16PIN	18PIN	20PIN	24PIN	28PIN	40PIN	48PIN
A	0.300	0.600	0.700	0.800	0.900	1.100	1.300	1.900	2.300
B	0.250	0.250	0.250	0.250	0.250	0.540	0.540	0.550	0.550
C	0.385	0.756	0.856	0.856	1.026	1.256	1.406	2.056	2.416
D	0.300	0.300	0.300	0.300	0.300	0.600	0.600	0.600	0.600

PLCC PACKAGING INFORMATION



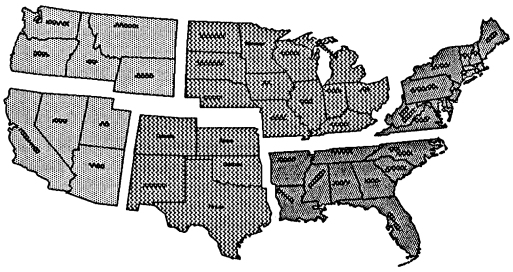
	44PIN	52PIN	68PIN	84PIN
A	0.653	0.730	0.954	1.154
B	0.029	0.029	0.029	0.029
C	0.050	0.050	0.050	0.050
D	0.690	0.790	0.990	1.190
E	0.110	0.110	0.110	0.110
F	0.500	0.600	0.800	1.000
G	0.610	0.710	0.910	1.110
H	0.026	0.026	0.026	0.026
I	0.182	0.182	0.182	0.182

PLASTIC SOIC PACKAGING INFORMATION



	8PIN	14PIN	16PIN	20PIN
A	0.236	0.236	0.406	0.406
B	0.154	0.154	0.154	0.295
C	0.192	0.339	0.405	0.504

REPRESENTATIVES



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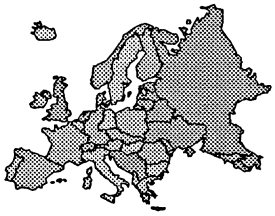

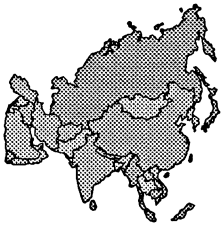

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Index