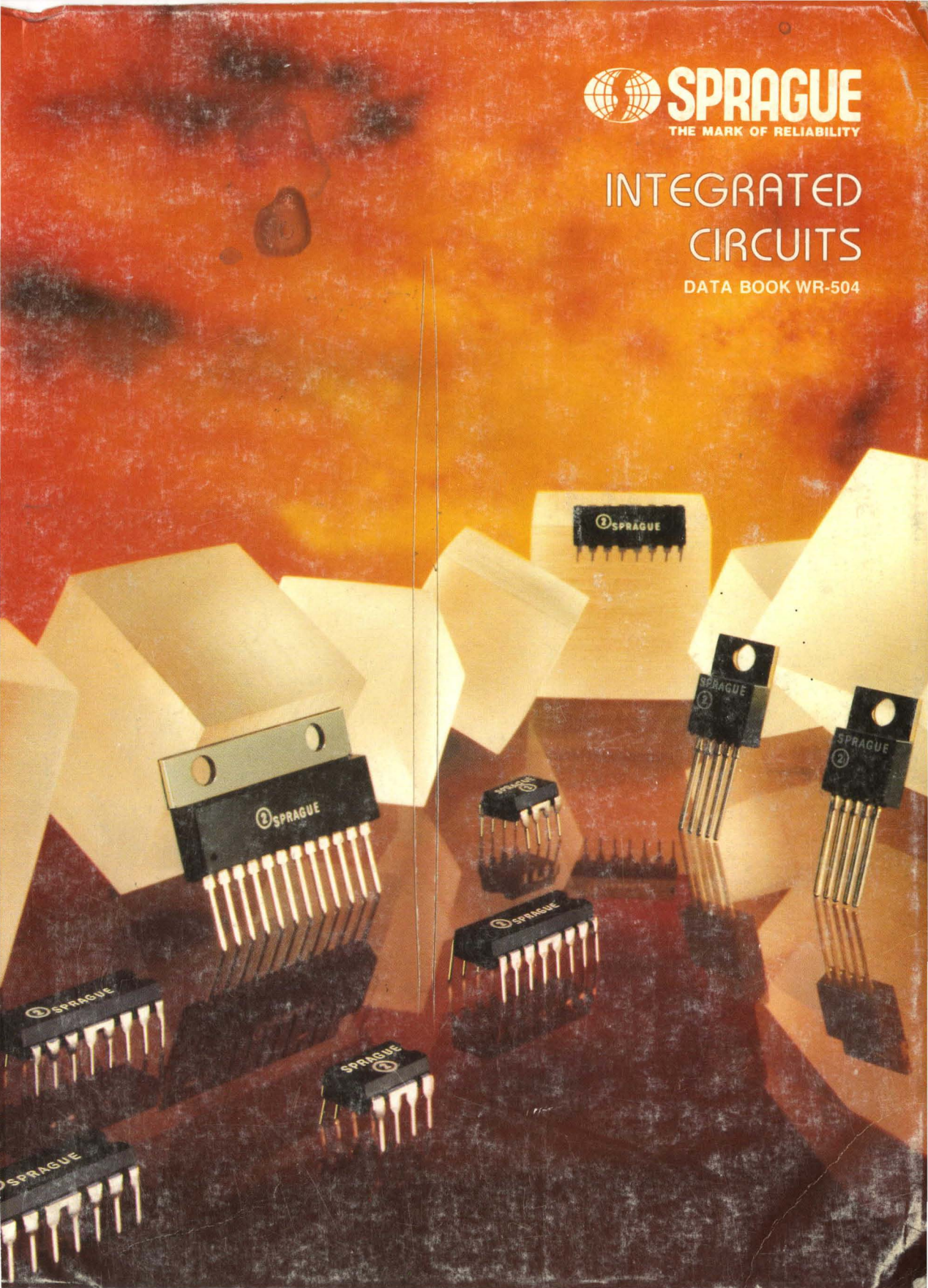
SPRAGUE
THE MARK OF RELIABILITY

INTEGRATED CIRCUITS

DATA BOOK WR-504



SPRAGUE
THE MARK OF RELIABILITY

INTEGRATED CIRCUITS

POWER INTERFACE ICs
- High Voltage
- High Current
- BiMOS Smart Power

MILITARY DRIVERS

MILITARY CMOS

LINEAR ICs
- Power Op Amps
- Radio/Communications
- Power Supply
- Audio

SPRAGUE ELECTRIC COMPANY

A UNIT OF THE PENN CENTRAL CORPORATION

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*QPL version of ULS-2003H-883.

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®C-QUAM (Compatible Quadrature Amplitude Modulation) is a registered trademark of Motorola, Inc.

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SECTION 7 — LINEAR AND SPECIAL FUNCTION ICs

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*Complete information is provided in Data Book CN-250, Discrete Semiconductors.

Product Index in Numerical Order

*Complete information is provided in Data Book CN-250, Discrete Semiconductors.
†Complete information is provided in Data Book SN-500, Sensor ICs.

Product Index in Numerical Order

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Product Index in Numerical Order

*Complete information is provided in Data Book CN-250, Discrete Semiconductors.

Product Index in Numerical Order

1

SECTION 1—GENERAL INFORMATION

9841

SEMICONDUCTOR GROUP
SPRAGUE ELECTRIC COMPANY

Sprague Electric Company was founded in 1926 and is recognized as a pioneer in the research, development, and manufacture of reliable, high-quality electronic components for the electrical and electronics industries. It is one of four business units making up the Electronics, Defense, and Telecommunications Group of The Penn Central Corporation. Its products are used in virtually every electronics application ranging from air-conditioners, cars, radios and TVs, to computers, communications, and space vehicles. Sprague manufactures active and passive electronic components in 17 locations in the United States and in 5 countries in Europe and the Far East.

Headquarters for the Sprague Semiconductor Group is on a 40-acre site in Worcester, Massachusetts. Manufacturing operations and many support services have been in place there since 1966 in a modern plant that now occupies 183,000 square feet. The current Worcester employment level is in excess of 750 people.

Additional production facilities occupying 223,000 square feet are on a 30-acre site in Willow Grove, Pennsylvania. Other support operations are located in Manila, Republic of the Philippines, Hong Kong, and Ferney Voltaire, France.

The Semiconductor Group has concentrated its activities in the areas of CMOS logic and high-performance power and smart power integrated circuits serving the computer, industrial control and radio markets. It manufactures standard and custom integrated circuits for specialized, high-volume applications. A reputation for versatility and unique capability has been established, making Sprague the standard of performance for electronic products of this type. Distinctive circuits, involving proprietary designs and state-of-the-art processing, have helped establish the Sprague Semiconductor Group as a leader in its field.

The three basic process technologies available from Sprague are bipolar, CMOS, and DMOS. These three technologies are used separately or in combination in the form of merged process technologies. Merged technology capabilities include:

Bipolar + CMOS	BiMOS
(high-current) DMOS + CMOS	D/CMOS
CMOS + (high-voltage) DMOS	C/DMOS
CMOS + DMOS + Bipolar	

This merging gives Sprague a design flexibility to incorporate multiple system functions in a cost-effective (and often unique) manner. Functions which are currently being merged in monolithic silicon chips by Sprague include:

Input Sense (Hall effect, photosensitive, low-level)
Information Processing (Analog or digital)
Output Control (High voltage and/or high current)

"Smart Power" is a monolithic combination of information processing and output drive capability of 2 A and/or 2 W or greater. Sprague developed and has been a leader in smart power technology since 1977.

Bipolar Capabilities

Sprague has a mature and broad range of bipolar technologies that are used in small-signal linear products and in power and smart power integrated circuits. Multiple bipolar sink and source functions with current capability to 8 A per channel and voltage capability to 200 V are available. Two-level metal processes are used extensively in power bipolar structures greater than 2 A. The two-level metal construction provides power devices which are superior in SOA performance to conventional single-level metal construction.

Function Type	Current/Voltage Capabilities (per channel)
Sink Driver	8 A/40 V 4 A/60 V 1 A/150 V
Source Driver	−8 A/40 V −4 A/60 V −100 mA/150 V

CMOS Capabilities

Sprague offers a wide range of CMOS process technologies produced in a military (MIL-M-38510) qualified plant. These technologies cover the range from high voltage to low voltage/high density. The base technologies are:

Process	Nominal Dimensions	Operating Voltage
F-Metal Gate (P-well)	6-8 μm	1.5-15 V
HIIA Silicon Gate	4 μm	3-20 V
HII Silicon Gate	3 μm	2-8 V
HIII Silicon Gate	2 μm	2-8 V

The silicon gate processes are available with either N or P wells, double-silicon, and polysilicon resistors and capacitors. HII and HIII are available with two-level metal.

I^2L Merged with Analog Bipolar

This technology is available with feature sizes from 4 to 8 microns, and maximum bipolar operating voltages from 6 V to 20 V. In all cases the logic portion functions down to 1.0 V. These technologies can include 2 k/square resistors, Schottky diodes, and two-level metal.

DMOS Capabilities

A process technology with multiple, independent, lateral DMOS power output devices with capabilities to 200 V and 200 mA per output stage is available. The output DMOS devices are enhancement-mode N-channel DMOS structures. The process has been designed to allow for the integration of bipolar and CMOS elements on the same monolithic chip while optimizing the DMOS power output performance.

BiMOS Smart Power Capabilities

The first CMOS + bipolar smart power integrated circuits in the industry were developed by Sprague in 1977-78 (UCN-4401/4801). Since then, Sprague has developed a family of BiMOS processes to optimize size (cost)/performance for a variety of applications. A summary of current processes is given below:

BiMOS II	5-12 V logic supply voltage 100 V/4 A (per channel) power bipolar 5 MHz logic operation at 5 V supply 1x relative size
BiMOS III	5-12 V logic supply voltage 150 V/2 A (per channel) power bipolar 5 MHz logic operation at 5 V supply 1x relative size
BiMOS IV	5-12 V logic supply voltage 40 V/4 A (per channel) power bipolar 5 MHz logic operation at 5 V supply 0.5x relative size
BiMOS V (developmental)	5-7 V logic supply voltage 80 V/2 A (per channel) power bipolar 10 MHz logic operation at 5 V supply 0.25x relative size

With the evolution of Sprague BiMOS, logic content has increased significantly and chip size per function has decreased dramatically.

The majority of the standard products designed to date with Sprague BiMOS processes have used CMOS as a digital logic function with power bipolar. Sprague has recently begun to utilize the CMOS for analog functions as well.

C/DMOS Smart Power Capabilities

Sprague has developed a series of display driver devices based on a C/DMOS (lateral) process. The CMOS has the performance characteristics of BiMOS II and the output devices are N-channel DMOS devices with output ratings of 225 V breakdown and 50 mA current capability. This process is well-suited for multi-channel high-voltage/low-current applications.

D/CMOS Smart Power Capabilities

Presently under advanced development at Sprague is a D/CMOS technology which incorporates Sigate CMOS logic and either a single-channel high-current (20 A) DMOS capability or multi-channel DMOS power outputs rated at 50 V and a current capability in the 2 A range.

Summary of Sprague Power Integrated Circuit Technologies for Multi-Channel Applications

Characteristic	Linear Bipolar	BiMOS/ CMOS Bipolar	CMOS/Bipolar/ DMOS Vertical DMOS
Current per Channel	8A	4 A	4 A
Current per Chip	32 A	16 A	16 A
ON Resistance	0.25	0.5	0.1-0.3
Sustaining Voltage	50-80 V	50-80 V	50-80 V
Breakdown Voltage	80-200 V	80-150 V	50-80 V
Extensive Logic on Chip	No	Yes	Yes
Logic Data Rate	NA	5-10 MHz	5-10 MHz
Logic Predrive Power	High	Low	Low
Linear Functions	Yes	Yes	Yes
Source/Sink Functions	Yes	Yes	Sink Only*
Cost	Low	Moderate	High

*May require bootstrapping for N-channel MOS source function or a bipolar source function could be used with bootstrapping.

Power IC Packages

Power and smart power IC performance is dependent on the power efficiency of the silicon chip (chip power dissipation), the maximum allowable junction temperature (typically 125°C to 150°C), and the availability of a low thermal-resistance path from the chip to a suitable external heat sink. Sprague specifies an approximate thermal resistance from junction to air and junction to case or, for highest power dissipation requirements, junction to tab or heat sink. For minimum power dissipation requirements (to 2 W), industry-standard packages with copper leadframes are adequate. For medium power dissipation requirements (3-8 W), packages with heat-sink contact tabs are available (DIPs and SOICs) or will be soon (PLCCs). Highest package power dissipation requirements (3-30 W) are answered with power tab SIPs. Complete information on Sprague packages is given in Seciton 8 of this Data Book.

TYPICAL CUSTOM DESIGN SCHEDULE

Task	Time in Weeks
Define Specifications	—
Circuit Design	2-15
Breadboard Construction and Analysis	4-8
Circuit Layout and Maskmaking	4-12
Prototype Processing	2-10
Prototype Evaluation	3-8
Production Pilot Run	8-12
Production Volume	5-10

Nominal Developmental Cycle of 28 to 48 weeks.

INTEGRATED CIRCUIT PART-NUMBERING SYSTEMS

UD N - 6116 A - 1

INSTRUCTIONS.
- 1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
- BU = BURNED-IN PARTS TO DOUBLE-DEUCE PROGRAM*
- MIL = MILITARY GRADE, NON-COMPLIANT, WITH SCREENING TO MIL-STD-883, CLASS B*
- 883 = MILITARY GRADE, COMPLIANT, WITH SCREENING TO MIL-STD-883, CLASS B*

PACKAGE DESIGNATION.
- A = PLASTIC, DUAL IN-LINE
- B = PLASTIC, DUAL IN-LINE SEMI-TAB
- C = UNPACKAGED CHIP
- CW = PROBED WAFER
- EK = CERAMIC/METAL HERMETIC, LEADLESS CHIP CARRIER
- EP = PLASTIC, LEADED CHIP CARRIER
- H = CERAMIC/METAL HERMETIC, DUAL IN-LINE
- L = PLASTIC, SOIC
- LB = PLASTIC, WIDE-BODY SOIC POWER TAB
- LW = PLASTIC, WIDE-BODY SOIC
- M = PLASTIC, 8-PIN DUAL IN-LINE
- R = CERAMIC/GLASS HERMETIC, DUAL IN-LINE
- W = PLASTIC, 12-LEAD SINGLE IN-LINE POWER TAB
- Z = PLASTIC, 5-LEAD SINGLE IN-LINE POWER TAB (TO-220)
- ZH = Z PACKAGE WITH FORMED LEADS FOR HORIZONTAL MOUNT
- ZV = Z PACKAGE WITH FORMED LEADS FOR VERTICAL MOUNT

DEVICE TYPE (FOUR DIGITS).

OPERATING AMBIENT TEMPERATURE RANGE.
- N = COMMERCIAL/INDUSTRIAL, SEE DETAIL SPECIFICATIONS
- Q = EXTENDED (−40°C TO +85°C)
- S = FULL MILITARY (−55°C TO +125°C)

FAMILY (UC, UD, UG, OR UL).

UH D - 400 - 1

INSTRUCTIONS.
- 1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
- BU = BURNED-IN PARTS TO DOUBLE-DEUCE PROGRAM*
- 883 = MILITARY GRADE, COMPLIANT, WITH SCREENING TO MIL-STD-883C, CLASS B*

DEVICE TYPE (THREE DIGITS).

PACKAGE DESIGNATION.
- C = CERAMIC/METAL HERMETIC, 14-LEAD FLAT PACK (−55°C to +125°C)
- D = CERAMIC/METAL HERMETIC, 14-PIN DUAL IN-LINE (−55°C to +125°C)
- K = UNPACKAGED CHIP OR PROBED WAFER
- P = PLASTIC, 14-PIN DUAL IN-LINE (−20°C to +85°C)

FAMILY (UH ONLY).

*Parts with suffix "-BU" are available only with temperature codes "N" and "Q" or prefix "UHP."
*Parts with suffixes "-MIL" and "-883" are available only with temperature code "S" or prefixes "UHC" and "UHD." See Section 6 for deivce availability.

INTEGRATED CIRCUIT PART-NUMBERING SYSTEMS

CMOS LOGIC

883C **4011B** **C**

- **C** — **PACKAGE DESIGNATION.** C = CERAMIC/GLASS HERMETIC
- **4011B** — **DEVICE TYPE.** (FOUR DIGITS PLUS ONE OR TWO LETTERS)
- **883C** — **FAMILY.** 883C = MILITARY GRADE, COMPLIANT WITH SCREENING TO MIL-STD-883, CLASS B

JAN TO MIL-STD-883
(ULS-2003H-883 AND SERIES 4000B CMOS LOGIC)

M38510 / 141 03 B E C

- **C** — **LEAD FINISH.** A = KOVAR/SOLDER
  B = KOVAR/TIN PLATE
  C = KOVAR/GOLD PLATE
  X = ANY (A, B, or C acceptable)
- **E** — **PACKAGE.** A = 14-LEAD FLAT PACK (F-1)
  C = 14-PIN DIP (D-1)
  E = 16-PIN DIP (D-2)
  F = 16-LEAD FLAT PACK (F-5)
- **B** — **PRODUCT ASSURANCE LEVEL.** B = CLASS B
- **03** — **DEVICE TYPE**
- **141** — **DETAIL SPECIFICATION**
- **M38510** — **PREFIX**

All possible combinations of device types, temperature ranges, and package types are not necessarily available.
Consult individual data book pages for complete information.

THE SPRAGUE ELECTRIC 'DOUBLE-DEUCE' BURN-IN PROGRAM FOR INTEGRATED CIRCUITS

THE EXPENSE OF DEVICE FAILURE is more than the time and money spent locating and replacing a defective integrated circuit. The total cost can include the price of assembly rework, system downtime, service calls, warranty claims and lost customer goodwill.

Costs of $25 for each in-house failure and $250 for each field failure are not uncommon. At a relatively low cost, Sprague Electric Company's "Double-Deuce" screening program removes marginal devices before shipment. Improved customer satisfaction with performance and reliability is an immeasurable but certain bonus of the program.

"Double-Deuce" screening is done during the last stage of production. Because Sprague does the screening, only qualified devices are received by the user.

QUALITY AND RELIABILITY

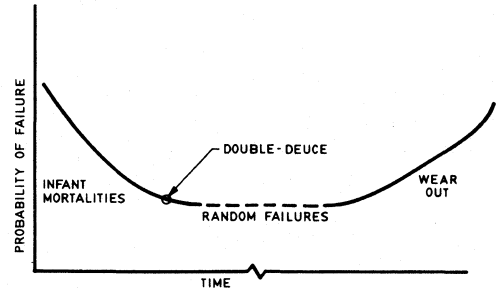
Quality and reliability are terms that are often used interchangeably. Quality implies reliability, but a product's merit should always be defined by both.

Quality is the extent to which a device conforms to specifications when it is shipped to the user. Quality is verified by testing. Inspections at every step of production of Sprague integrated circuits ensure the devices meet demanding standards for workmanship and materials.

Inspections of integrated circuits under the "Double-Deuce" program have been made even more stringent to secure a higher level of quality.

Reliability is the measure of an integrated circuit's ability to meet specifications over time. Reliability is a product of design and process control. Accelerated-life tests provide the manufacturer and user with an indication of the reliability of a device. Normally, a small number of integrated circuits exhibit signs of early failure or infant mortality. This statistic, taken from the steepest part of the IC lifetime probability curve, is often used to project time-to-failure for integrated circuits. Because the "Double-Deuce" program eliminates early failures, Sprague integrated circuits delivered after the screening process have a higher degree of reliability.

PROBABILITY OF FAILURE AS A FUNCTION OF TIME



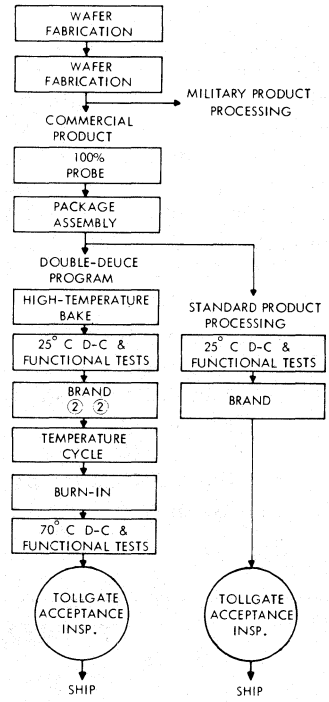
Dwg. No. A-11,417

OUTLINE OF THE 'DOUBLE-DEUCE' PROCESS

The "Double-Deuce" burn-in program uses high stress levels to accelerate the failure mechanisms associated with infant mortality. These normally occur within the first few hours of user application. Although typically less than 1 per cent of a lot will be rejected, user confidence in lot integrity is greatly improved. The screening program is designed to eliminate the following failure modes:

Stress	Failure Mode
High-Temp. Bake	Contamination
Temp. Cycling	Package-Related
Burn-In	Process-Related
High-Temp. Testing	Electrical Degradation

The majority of early integrated circuit failures (infant mortality or ionic contamination) can be attributed to manufacturing defects, package or assembly defects, or final test escapes. The "Double-Deuce" program is designed to eliminate weaker parts, reduce or eliminate user shipment inspection, assembly rework, system checkout, and warranty returns.



Dwg. No. A-11,418A

TEST PROCEDURES

The "Double-Deuce" burn-in program includes five test procedures:

1. High-Temperature Bake

This is a process designed to stabilize electrical drift and to accelerate chemical degradation such as surface contamination. It is a four-hour bake at +175°C without electrical stress (similar to MIL-STD-883, Method 1008).

2. Temperature Cycling

This is a screening process designed to mechanically stress the integrated circuit by alternately heating and cooling it. Potential failures are seal or bond failure, cracked packages or chips.

The process has 10 cycles with 10 minutes of dwell at −65°C and 10 minutes of dwell at +150°C (air to air), with a maximum transfer time of five minutes (MIL-STD-883, Method 1010, Condition C). At Sprague's option, this process may be changed to thermal shock (liquid to liquid) for 10 cycles, five minutes at 0°C and five minutes at +100°C with a transfer time of 10 seconds (MIL-STD-883, Method 1011, Condition A).

3. Burn-In

The burn-in, or accelerated-life test, is performed to screen out marginal devices, those with inherent defects, or defects resulting from manufacturing deviations that can cause time-dependent or stress-dependent failures. Without this conditioning, marginal circuits that initially meet all specifications could exhibit early lifetime failures under normal operating conditions. The test is conducted for 96 hours at a junction temperature of +150°C under electrical stress conditions (similar to MIL-STD-883, Method 1015) such as:

Type of Device	Electrical Stress
Bipolar Interface	Steady-State Reverse Bias
Linear Devices	Steady-State Forward Bias
I^2L and MOS Logic	Clocked

The burn-in conditions (96 hours at T_J = +150°C) are equivalent to 525 hours at T_J = +125°C for ionic contamination (E_A = 1.0 eV) or for 192 hours at T_J = +125°C for infant mortality defects (E_A = 0.4 eV).

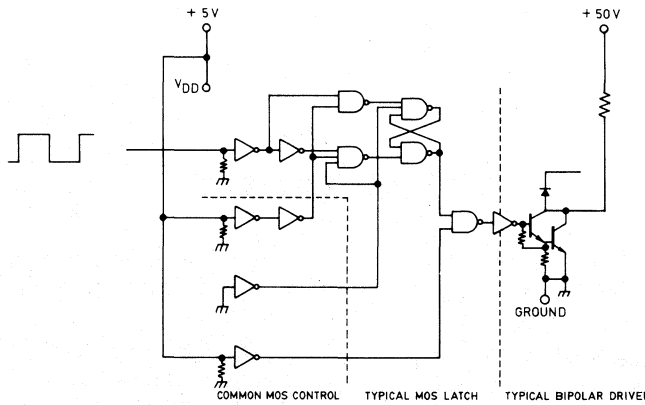
4. High-Temperature Test

Every device is subjected to complete electrical tests at +70°C for function and d-c parameters (similar to MIL-STD-883, Methods 3001 through 3014 and 4001 through 4007, as applicable). Relaxed +25°C limits or published high-temperature limits, are used to remove devices with circuit anomalies such as beta mismatch, high leakage current, and intermittent bonds, which may only affect the circuit at higher temperatures.

5. Outgoing Quality Control Inspection

All "Double-Deuce" product is inspected to an outgoing sampling plan that guarantees the product will meet an acceptable quality level of 0.10%.

TYPICAL BiMOS DRIVER BURN-IN



Dwg. No. A-11,419

HOW TO ORDER DEVICES IN 'DOUBLE-DEUCE' PROGRAM

All standard Sprague integrated circuits are branded with the Sprague registered trademark, ②.

Integrated circuits screened to the added requirements of the "Double-Deuce" program are marked:

②②

The double "circle-deuce" identifies a part subjected to the screening program for extra reliability.

Devices processed in the "Double-Deuce" burn-in program are specified by adding the suffix "BU" to the end of the part number. For example, to order ULN-2023A with this processing, specify ULN-2023ABU; to order UDN-6118R-2, specify UDN-6118R-2BU.

DEVICES CURRENTLY AVAILABLE

ULN-2001A/R through 2025A/R
ULN-2031/32A
ULN-2061/62M
ULN-2064B through 2071B
ULN-2075/77B
ULN-2082/83A
ULN-2111A
UDN-2541B
UDN-2595A
ULN-2801A/R through 2825A/R
UDN-2952B
UDN-2981A through 2984A
UDN-3611M through 3614M
UCN-4202A
UCN-5800A
UCN-5801A
UCN-5810A
UCN-5815A
Series UDN-5700A
UDN-5712M
UDN-6118A/R
ULN-8130A
ULN-8160A/R

Unlisted devices may be processed in the "Double-Deuce" burn-in program if order size is sufficient.

PARTNERSHIP AND SEMI-STANDARD ICs

Introduction

Change or Die! It's the first law of survival for today's high-technology industries, and the world of integrated circuits certainly epitomizes both change and a struggle to survive. Few industries have ever progressed at such a rate and with such inescapable and accelerated obsolescence of both product and technology.

The rapid growth of semiconductor continues to present new concepts and opportunities, such as combining semi-standard ICs and partnerships. The basic concept is to provide standard building blocks for a volume market segment. The semi-standard IC may afford new, reliable, and cost-effective solutions to those users/vendors willing and able to explore this possibility.

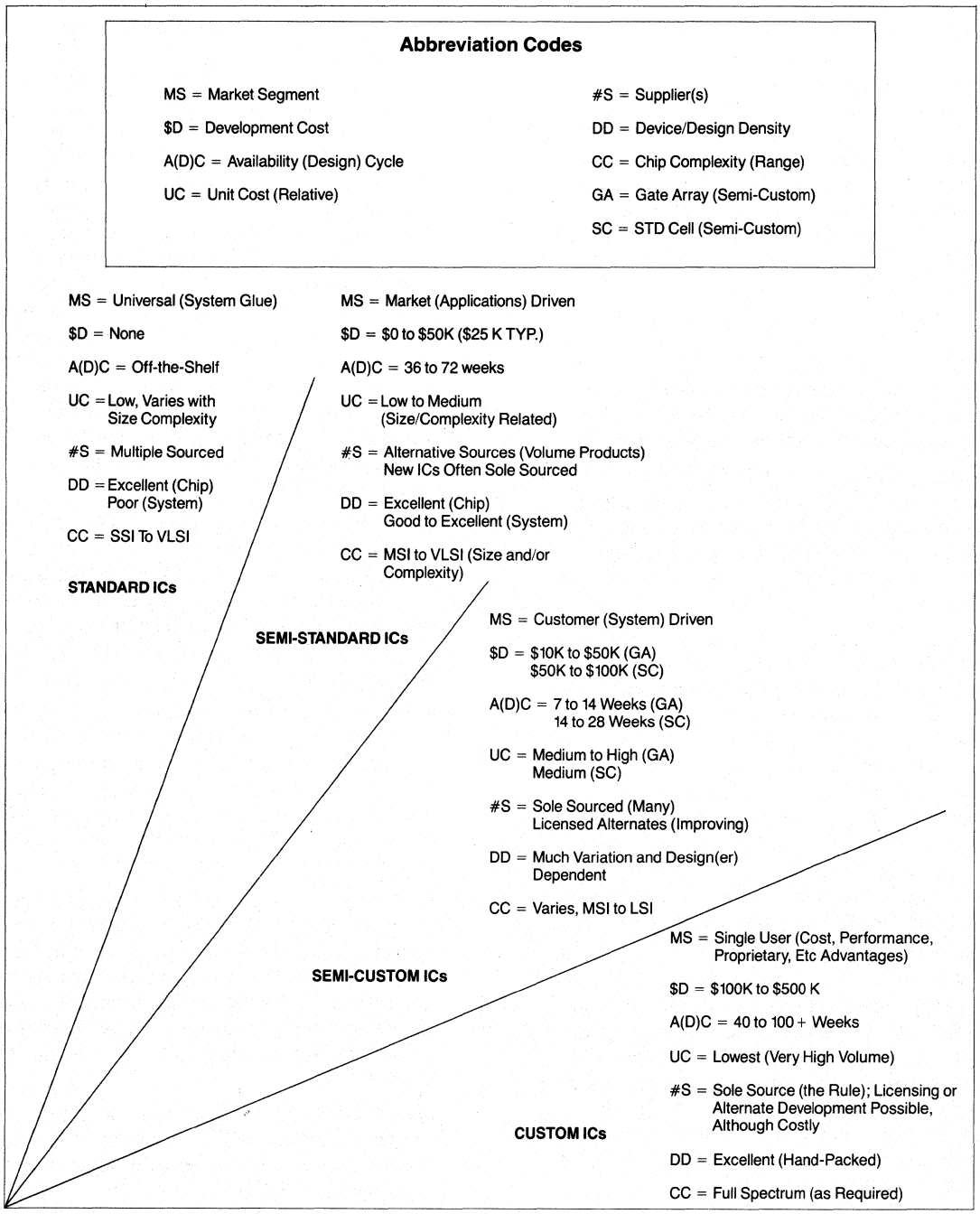
The available alternatives are:

STANDARD: A wide variety of logic, linear, memory, and others utilizing many biopolar, MOS, and increasingly, merged (bipolar/MOS combined) technologies. Complexity ranges from multiple gates to 256K memories and 32-bit microprocessors.

SEMI-STANDARD: Circuits that are market or applications driven, useful to specific target segments. An increasing number of ICs are being created to satisfy particular customer needs not well accommodated by the other approaches. These might be considered as application-specific and range from rather broad and general-purpose (such as relay drivers) to very specific (such as three-phase brushless dc motor ICs). Various technology alternatives are available.

SEMI-CUSTOM: An alternative for many users seeking the basic attributes of custom ICs, but without the development time and cost and the high volume requirements of proprietary designs. There are many — perhaps too many — suppliers, with bipolar, MOS, and merged technologies fabricating gate arrays, standard cell, linear, etc. These may also be used for application-specific ICs, but are limited almost exclusively to low-power logic or analog operation with restricted voltage, current, and power capabilities.

CUSTOM: Limited to a small, probably diminishing, set of users that seek the proprietary features, performance, low cost (in very high volume), and size reductions. There is a considerable variety of technologies, packaging, and vendors, but the usual program requirements dictate much development funding and large volume production.


Abbreviation Codes
MS = Market Segment
$D = Development Cost
A(D)C = Availability (Design) Cycle
UC = Unit Cost (Relative)
#S = Supplier(s)
DD = Device/Design Density
CC = Chip Complexity (Range)
GA = Gate Array (Semi-Custom)
SC = STD Cell (Semi-Custom)
MS = Universal (System Glue)
$D = None
A(D)C = Off-the-Shelf
UC = Low, Varies with Size Complexity
#S = Multiple Sourced
DD = Excellent (Chip) Poor (System)
CC = SSI To VLSI
STANDARD ICs
MS = Market (Applications) Driven
$D = $0 to $50K ($25 K TYP.)
A(D)C = 36 to 72 weeks
UC = Low to Medium (Size/Complexity Related)
#S = Alternative Sources (Volume Products) New ICs Often Sole Sourced
DD = Excellent (Chip) Good to Excellent (System)
CC = MSI to VLSI (Size and/or Complexity)
SEMI-STANDARD ICs
MS = Customer (System) Driven
$D = $10K to $50K (GA) $50K to $100K (SC)
A(D)C = 7 to 14 Weeks (GA) 14 to 28 Weeks (SC)
UC = Medium to High (GA) Medium (SC)
#S = Sole Sourced (Many) Licensed Alternates (Improving)
DD = Much Variation and Design(er) Dependent
CC = Varies, MSI to LSI
SEMI-CUSTOM ICs
MS = Single User (Cost, Performance, Proprietary, Etc Advantages)
$D = $100K to $500 K
A(D)C = 40 to 100 + Weeks
UC = Lowest (Very High Volume)
#S = Sole Source (the Rule); Licensing or Alternate Development Possible, Although Costly
DD = Excellent (Hand-Packed)
CC = Full Spectrum (as Required)
CUSTOM ICs

Vendor Definition/Selection

To create a semi-standard IC it is imperative that both parties understand their partner's fundamental strengths and weaknesses. Usually, new circuits originate from defining user requirements, executed by the supplier. It is very important, initially, that potential users approach the proper set of suppliers.

Often the user does not understand which IC suppliers are capable and willing to fabricate a particular circuit function. Selecting a suitable supplier must be the very first priority, and should include considerations of technology, product design strengths, reputation, size (which must be sufficient to support user requirements), proximity (often helpful), and the portion of development costs to be borne by the user. Suppliers fall into three categories:

1. Large volume suppliers offer broad product lines and usually extensive process capabilities, but generally require very high volumes to satisfy business thresholds. Many offer semi-custom and custom, and are usually founded on standard (commodity) ICs.

2. Medium volume suppliers usually are more niche market oriented, and use special expertise in marketing, applications, design, and technology toward selective market segments. Thresholds generally are lower than with large volume suppliers, and often medium volume suppliers are more inclined to form special partnerships with customers. A number of potential suppliers with specific skills: analog, digital, power, precision linear, data conversion, high frequency ICs, etc. are available from the many volume specialists. These suppliers are prime candidates for designing and developing semi-standard ICs.

3. Small volume suppliers/independent specialists are those not covered in the first two categories. An increasing number of operations with rather specialized skills in IC design, assembly, testing, wafer fabrication, burn-in (reliability/test operations), etc. are available. However, despite the concept that an IC might be designed, processed, tested, assembled, etc. by combining such separate entities, the coordination of various, distinct groups is definitely not for the novice.

Semi-Standard Circuits

Potential users initiating a semi-standard IC must determine that a nonproprietary design is suitable (multiple users mandated), and that the originator's advantage is to be one of cost, performance, size, reliability, etc. Being an originator affords at least a temporary advantage or maintains competitive equality. In some instances an exclusive period may be negotiated, but the user must be willing and able to commit volume business and/or funds to secure exclusivity. Users with leadership positions may enhance their advantage, while those already behind may close in on, or surpass, the competition. From a supplier viewpoint, it is preferable to have a leader as a partner, but if the product has substantial promise and product life, execution of the design may be undertaken, for a follower. Other partnership concerns are:

Unit Price: Does the estimated unit price offer an advantage to the user while providing a reasonable return to the supplier? If not both, it is probably best to abandon the project. Be certain to compare total system cost. Realize there is a learning curve; the cost reductions generally occur in the future, rather than immediately.

Volume: Does the basic application, plus any spin offs, provide sufficient market potential to interest the supplier? ICs are very much batch process/volume businesses; smaller volume markets are probably best suited to the smaller specialists. The supplier, often aided by the user, may need or desire to determine overall market potential.

Seed Money: Certain suppliers will not undertake design of a new IC without some commitment on the part of the user; others may be more concerned with the *window of opportunity* and proceed with internal funding. Much of this depends upon the awareness, confidence, and decision-making capabilities of vendor marketing, applications, and design engineers.

Specifications: These take on many forms; the initial approach may begin with telephone discussions of function, form, ratings, etc. Early dialogue may be very general in nature, and — in fact — usually

should be, to allow the supplier to broaden the scope of the potential market. However, at some point an agreement relating to function, form, and ratings is mandated; start with basics and expand and refine. Limit specifications to those necessary to ensure a quality and reliable design without excessive safety margins; remember that the device cost will be affected.

Schedules: State-of-the-art ICs take time to develop; users should be certain that their anticipated production dates are realistic and that the supplier has sufficient time. Our past experience indicates this to be a frequent problem. Investigate suppliers and technology early, and commit swiftly, then follow up the progress to prevent surprises. No vendor intends to slip schedules, but IC design and fabrication often goes through serial, iterative, time-consuming modifications and redesigns.

Alternatives: Both partners should have alternatives; the supplier needs other prospective users, while the user needs other approaches to fabricate his system should delays occur. Not all programs flow smoothly, and problems may be encountered on either side. The user may use discrete circuitry or combinations of ICs and discretes for early entry to the market; thus, heavy financial commitment may be avoided for an early test market using a swift, though costlier, alternative approach.

Advantages versus Features: If the basic objective relates to achieving cost benefits, improved quality and/or reliability, performance, size reduction, or similar concepts, do not add unnecessary *bells and whistles!* These cost money and, often, time. Know the difference between an advantage and a feature, which is often unneeded, unused, and uncompetitive. Also, avoid the NIH (not invented here) syndrome; use supplier or even competitor ideas, if they fit the basic objective.

Revolution versus Evolution: Evolutions are much more predictable, but the occasional *revolution* will advance technology, markets and, often, profits to a new plateau. Distinguishing between them is not difficult, but judging and committing to a successful revolution requires knowledge, intuition, and courage. Semiconductor technology has had many revolutions, but unless such an approach is truly necessary it is swifter, and usually, safer to take the evolutionary route. Have an honest appraisal of the circuit requirements by potential suppliers and choose accordingly. Competent vendor applications engineers will steer you toward a suitable solution, without attempting to use the next revolutionary technology unless it is necessary. Many opportunities suffer from missing a window of opportunity while struggling with an unnecessary, unproven approach.

There is a three-party possibility, for example, with suppliers of displays or motors and with a common end user. In such cases, the two suppliers are likely to form a partnership with a common customer or market segment objective. The creation of a new semi-standard IC aids the user and the motor or display or printhead or other supplier, while adding another building block to the IC supplier's catalog. However, these three-part combinations are considerably more difficult to execute than the user/supplier version.

SEMI-STANDARD vs. SEMI-CUSTOM

Although the semi-custom IC has received great media attention, extremely optimistic growth forecasts, and has approximately 100 suppliers worldwide, the suppliers of semi-standard have been quietly chipping away at a large and growing market.

Semi-custom ICs are manufactured using three basic approaches: gate arrays, standard cells, and cell-oriented custom design. However, each of these approaches uses a standard wafer containing a suitable number and type of components or functions (cells). In essence, the user customizes a section of his design on a chip, but is not afforded the optimization of minimum size, nor maximum capability that is afforded by suitable use of semi-standard or custom ICs. This approach largely combines other IC functions within a single device; semi-standard also accomplishes this, but adds a new dimension.

To an increasing degree, many semi-standard ICs combine the capabilities of logic, analog, and discrete devices. Many new prospects for power interface require the combinations of high-voltage and/or high-current (usually discretes) with logic and/or analog circuitry, and represent a strong growth market. Medium volume suppliers are strong contenders for power ICs to displace discrete/IC combinations, while some companies continue further integration of data conversion, mainly displacing hybrids with advanced ICs.

The semi-standard IC offers the cost and reliability benefits of consistent high volume production, little or no wasted circuitry area, standardized testing, and — increasingly — alternate suppliers. Circuits are designed by experts, rather than engineers who are often unfamiliar with sophisticated IC technology and design. While there definitely is a need and place for the semi-custom, the semi-standard affords parameters, functions, and cost reductions generally outside the market covered by semi-custom.

MARKET FOR SEMI-STANDARD ICs

Data on the semi-standard IC market do not exist as separate entities, but the market is very large, and rapidly expanding. The future prospects should track or exceed the dramatic growth of the entire industry; projections for worldwide sales of ICs indicate that between 1983 and 1990 the industry is to increase 400 percent. Opportunities for the joint creation of semi-standard hardware abound, but both users and suppliers need to improve awareness and communications. All classical segments of the market present such opportunities (automotive, computers, peripherals, telecom, and major appliances). The size and scope of any opportunity, obviously, vary, but prospects surround us.

DEFINITION OF TERMS

ADVANCE INFORMATION is issued to advise customers of proposed additions to the product line. The specifications given are target or goal specifications and may, therefore, change without notice. Contact your local Sprague sales office for details of current status.

PRELIMINARY INFORMATION is issued to advise customers of additions to the product line which, nevertheless, still have "pre-production" status. Details given may, therefore, change without notice although it is expected that the performance data is representative of "full production" status. Contact your local Sprague sales office for details of current status.

ABSOLUTE MAXIMUM RATINGS are limiting values of operation and environmental conditions and should not be exceeded under the worst probable conditions. Sprague Electric chooses these values to provide acceptable serviceability of the device.

The equipment manufacturer should design so that initially, and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions.

The absolute maximum output current ratings are the maximum allowable under any condition. In application, current will be limited by duty cycle, ambient temperature, heat sinking, and other heat sources. Under any set of conditions, the specified maximum junction temperature must not be exceeded:

Prefix UCN- ..... +125°C, maximum.
Prefix UCS-..... +130°C, maximum.
All others..... +150°C, maximum.

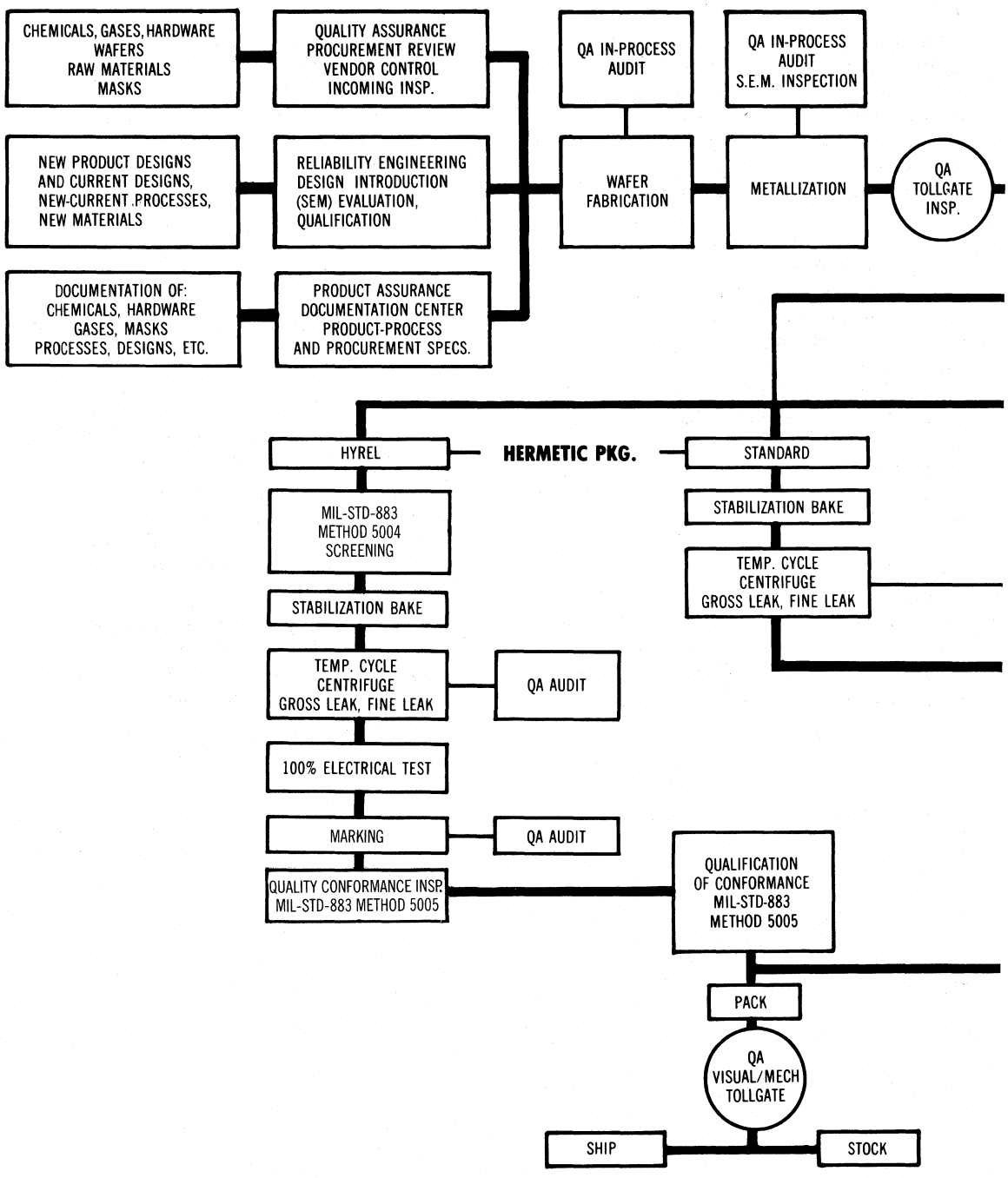
TYPICAL ELECTRICAL CHARACTERISTICS values are given for circuit design information only. Although these values are indicative of the peak distribution for a large number of production lots, these values should not be construed as guaranteed for any particular device or production lot.

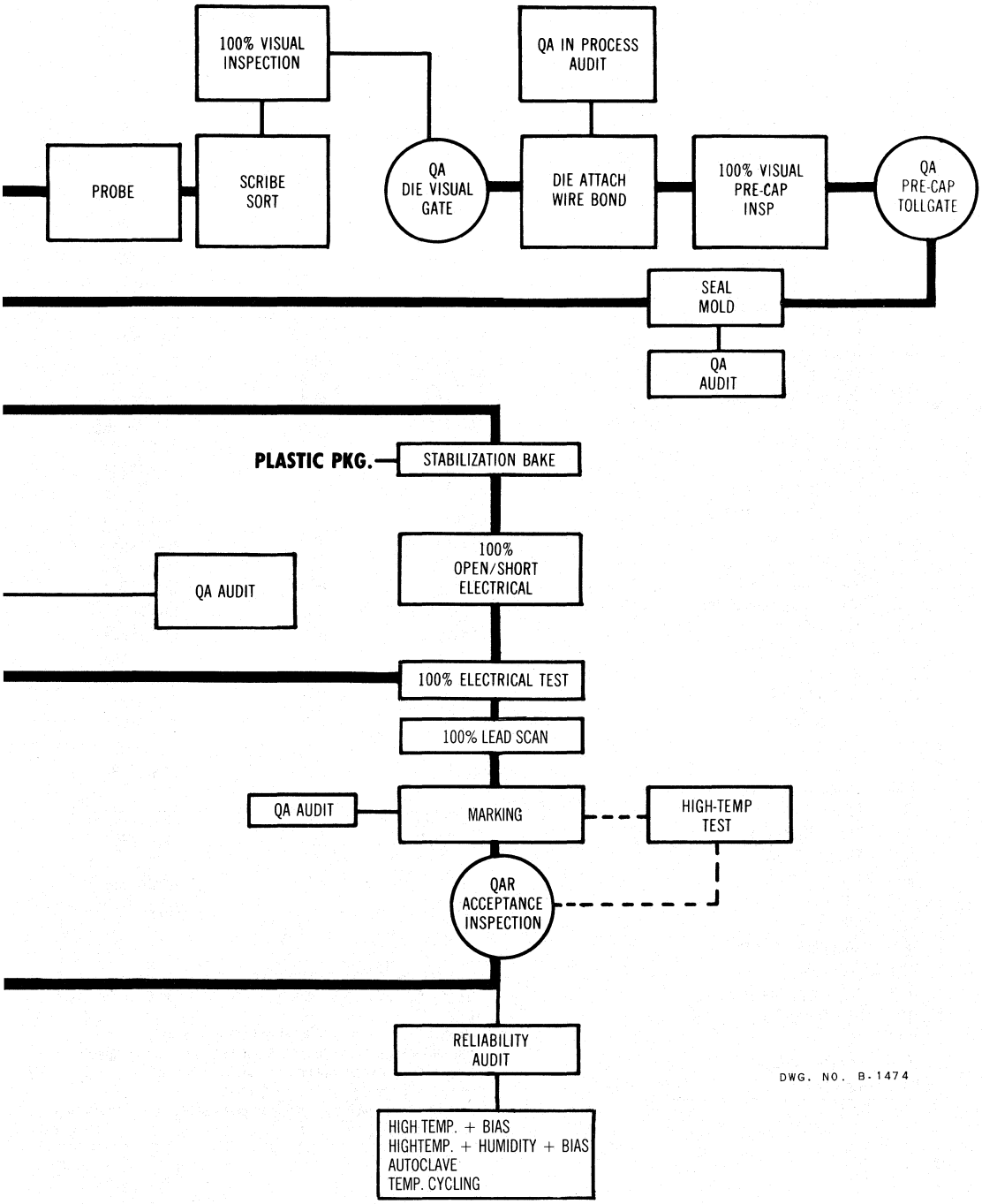
ELECTRICAL CHARACTERISTICS LIMITS are those values that are guaranteed by Sprague Electric under the test conditions shown.

RECOMMENDED OPERATING CONDITIONS are given for optimum device performance. Operation outside these conditions is permitted (within the Absolute Maximum Ratings) without any implied guarantee of level of performance.

It is recommended that equipment manufacturers consult Sprague Electric whenever device applications involve unusual electrical, mechanical, or environmental operating conditions.

QUALITY ASSURANCE FLOW CHART




100% VISUAL INSPECTION
QA IN PROCESS AUDIT
PROBE
SCRIBE SORT
QA DIE VISUAL GATE
DIE ATTACH WIRE BOND
100% VISUAL PRE-CAP INSP
QA PRE-CAP TOLLGATE
SEAL MOLD
QA AUDIT
PLASTIC PKG.
STABILIZATION BAKE
100% OPEN/SHORT ELECTRICAL
QA AUDIT
100% ELECTRICAL TEST
100% LEAD SCAN
QA AUDIT
MARKING
HIGH-TEMP TEST
QAR ACCEPTANCE INSPECTION
RELIABILITY AUDIT
HIGH TEMP. + BIAS
HIGHTEMP. + HUMIDITY + BIAS
AUTOCLAVE
TEMP. CYCLING
DWG. NO. B-1474

CROSS-REFERENCE in Alphanumerical Order

The suggested Sprague replacement devices are based on similarity as shown in currently published data. Exact replacement in all applications is *not* guaranteed. The user should compare the specifications of the competitive and recommended Sprague replacement.

Manufacturers' Abbreviations:

AMI	American Microsystems
CS	Cherry Semiconductor
DI	Dionics, Inc.
EXR	Exar Integrated Systems
FSC	Fairchild Semiconductor
FUJ	Fujitsu
GE	General Electric
HIT	Hitachi Ltd.
IP	Integrated Power
ITT	ITT Semiconductors
LT	Linear Technology
MAT	Matsushita
MIT	Mitsubishi Electric Corp.
MOT	Motorola Semiconductor
NEC	Nippon Electric Co.
NS	National Semiconductor
OKI	Oki Semiconductor
PE	Pro-Electron ♀
PLS	Plessey Semiconductor
RCA	RCA
RFA	Rifa
SAM	Samsung Semiconductor
SANY	Sanyo
SG	Silicon General Inc.
SIEM	Siemens Corp.
SIG	Signetics Corp.
SIL	Siliconix
SGS	SGS/ATES
SPR	Sprague Electric Co.
THM	Thomson-CSF
TI	Texas Instruments
TLF	AEG-Telefunken
TOKO	RCL Toko
TOS	Toshiba Corp.
UNI	Unitrode

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
CA1724E	RCA	TPQ-3724
CA1725E	RCA	TPQ-3725
CA2111AE	RCA	ULN-2111A
CA3045	RCA	ULS-2045R§
CA3045F	RCA	ULS-2045R§
CA3045L	RCA	ULS-2045H
CA3046	RCA	ULN-2046A
CA3054	RCA	ULN-2054A
CA3081	RCA	ULN-2081A
CA3082	RCA	ULN-2082A
CA3083	RCA	ULN-2083A
CA3086	RCA	ULN-2086A
CA3146E	RCA	ULN-2046A-1
CA3183AE	RCA	ULN-2083A-1
CA3183E	RCA	ULN-2083A-1
CA3219E	RCA	UDN-2543B
CA3724G	RCA	TPQ-3724
CA3725G	RCA	TPQ-3725
CS166	CS	ULN-2429A
DH3724CN	NS	TPQ-3724
DH3725CN	NS	TPQ-3725
DI302	DI	UDN-7183A
DI507	DI	UDN-6116A-1¶

♀European registration; manufactured by various companies including ITT, Philips, SGS/ATES, Siemens, Thomson-CSF, AEG-Telefunken, & Valvo.
¶ Sprague device includes internal pull-down resistors.
† Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.
§ Sprague engineering bulletin in preparation.
() Functional equivalent only; improved performance but not necessarily pin compatible.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
DI509	DI	UDN-6116A-2¶
DI510	DI	UDN-6510A
DI512	DI	UDN-6514A
DI154	DI	UDN-6118A-2¶
DM3724CN	NS	TPQ-3724
DM3725CN	NS	TPQ-3725
DS3611N	NS	UDN-3611M
DS3612N	NS	UDN-3612M
DS3613N	NS	UDN-3613M
DS3614N	NS	UDN-3614M
FPQ2222	FSC	TPQ-2222
FPQ2907	FSC	TPQ-2907
FPQ3724	FSC	TPQ-3724
FPQ3725	FSC	TPQ-3725
FSA2619P	FSC	TND-908
FSA2719P	FSC	TND-903
GEL2113	GE	ULN-2111A
HA12402	HIT	ULN-2204A
IP2064	IP	ULN-2064B
IP2065	IP	ULN-2065B
IP2066	IP	ULN-2066B
IP2067	IP	ULN-2067B
IP2068	IP	ULN-2068B
IP2069	IP	ULN-2069B
IP2070	IP	ULN-2070B
IP2071	IP	ULN-2071B
IP2074	IP	ULN-2074B
IP2075	IP	ULN-2075B
IP2076	IP	ULN-2076B
IP2077	IP	ULN-2077B
IP3525A	IP	SG 3525A
IP3526	IP	SG 3526A
IP5560C	IP	NE 5560
IP5561C	IP	NE 5560
ITT552	ITT	ULN-2001A
ITT554	ITT	ULN-2002A
ITT556	ITT	ULN-2003A
ITT652	ITT	ULN-2001A
ITT654	ITT	ULN-2002A
ITTT656	ITT	ULN-2003A
KA2508A	SAM	UDN-2508A
KA2588A	SAM	UDN-2588A
L165	SGS	ULN-3751Z
L201	SGS	ULN-2001A
L202	SGS	ULN-2002A
L203	SGS	ULN-2003A
L204	SGS	ULN-2004A
L272	SGS	(ULN-3755B)
L293	SGS	(UDN-2993B)
L295	SGS	(UDN-2962W)
L298	SGS	(UDN-2998W)
L601	SGS	ULN-2821A
L602	SGS	ULN-2822A
L603	SGS	ULN-2823A
L604	SGS	ULN-2824A
LA1160	SANY	ULN-2243A
LA3045	SANY	ULS-2045H
LA3046	SANY	ULN-2046A
LA3086	SANY	ULN-2086A
LB1231	SANY	ULN-2001A
LB1232	SANY	ULN-2002A
LB1233	SANY	ULN-2003A
LB1234	SANY	ULN-2004A
LM380N	NS	ULN-2280B
LM384N	NS	ULN-3784B
LM2111N	NS	ULN-2111A
LM2113N	NS	ULN-2111A
LM3045D	NS	ULS-2045H
LM3046N	NS	ULN-2046A
LM3054N	NS	ULN-2054A

¶Sprague device includes internal pull-down resistors.
()Functional equivalent only; improved performance but not necessarily pin compatible.

COMPETITIVE CROSS-REFERENCE

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
LM3086N	NS	ULN-2086A
LM3611N	NS	UDN-3611M
LM3612N	NS	UDN-3612M
LM3613N	NS	UDN-3613M
LM3614N	NS	UDN-3614M
M54523P	MIT	ULN-2003A
M54524P	MIT	ULN-2001A
M54525P	MIT	ULN-2002A
M54526P	MIT	ULN-2004A
M54532P	MIT	ULN-2064B
M54562P	MIT	UDN-2982A
M54563P	MIT	UDN-2981A
MB3759C	FUJ	TL-594IJ§
MB3759P	FUJ	TL-594IN§
MB3760C	FUJ	TL-595IJ§
MB3760P	FUJ	TL-595IN§
MC1309	MOT	ULN-3809A
MC1357P	MOT	ULN-2111A
MC1411L	MOT	ULN-2001R§
MC1411P	MOT	ULN-2001A
MC1411TP	MOT	ULQ-2001A§
MC1412L	MOT	ULN-2002R§
MC1412P	MOT	ULN-2002A
MC1412TP	MOT	ULQ-2002A§
MC1413L	MOT	ULN-2003R§
MC1413P	MOT	ULN-2003A
MC1413TP	MOT	ULQ-2003A§
MC1416L	MOT	ULN-2004R§
MC1416P	MOT	ULN-2004A
MC1416TP	MOT	ULQ-2004A§
MC1417P	MOT	UDN-2580A
MC1471P1	MOT	UDN-5711M
MC1472P1	MOT	UDN-5712M
MC1472U	MOT	UDN-5712R§
MC1473P1	MOT	UDN-5713M
MC1474P1	MOT	UDN-5714M
MC3346	MOT	ULN-2046A
MC3359P	MOT	ULN-3859A
MC3386P	MOT	ULN-2086A
ML3045		ULS-2045H
ML3046		ULN-2046A
ML3086		ULN-2086A
MPQ2221	MOT	TPQ-2221
MPQ2222	MOT	TPQ-2222
MPQ2369	MOT	TPQ-2369
MPQ2483	MOT	TPQ-2483
MPQ2484	MOT	TPQ-2484
MPQ2906	MOT	TPQ-2906
MPQ2907	MOT	TPQ-2907
MPQ3724	MOT	TPQ-3724
MPQ3725	MOT	TPQ-3725
MPQ3725A	MOT	TPQ-3725A
MPQ3798	MOT	TPQ-3798
MPQ3799	MOT	TPQ-3799
MPQ3904	MOT	TPQ-3904
MPQ3906	MOT	TPQ-3906
MPQ6001	MOT	TPQ-6001
MPQ6002	MOT	TPQ-6002
MPQ6100	MOT	TPQ-6100
MPQ6100A	MOT	TPQ-6100A
MPQ6501	MOT	TPQ-6501
MPQ6502	MOT	TPQ-6502
MPQ6600	MOT	TPQ-6600
MPQ6600A	MOT	TPQ-6600A
MPQ6700	MOT	TPQ-6700
MSL912R	OKI	UDN-6118A-2
N5111A	SIG	ULN-2111A
NA3086		ULN-2086A
NE564N	SIG	NE 564N
NE564F	SIG	NE 564F
NE594N	SIG	UDN-6118A-2

§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
NE594F	SIG	UDN-6118R-2
NE5501N	SIG	ULN-2021A
NE5502N	SIG	ULN-2022A
NE5503N	SIG	ULN-2023A
NE5504N	SIG	ULN-2024A
NE5560F	SIG	NE 5560F
NE5560N	SIG	NE 5560N
NE5561N	SIG	NE 5561N
NE5563F	SIG	ULN-8163R
NE5563N	SIG	ULN-8163A
NE5568N	SIG	NE 5568N
NE5601N	SIG	ULN-2001A
NE5602N	SIG	ULN-2002A
NE5603N	SIG	ULN-2003A
NE5604N	SIG	ULN-2004A
PBD352301J	RFA	ULN-2001R§
PBD352301N	RFA	ULN-2001A
PBD352302J	RFA	ULN-2004R§
PBD352302N	RFA	ULN-2004A
PBD352303J	RFA	ULN-2003R§
PBD352303N	RFA	ULN-2003A
PBD352304J	RFA	ULN-2002R§
PBD352304N	RFA	ULN-2002A
PBD352311N	RFA	ULN-2021A
PBD352312N	RFA	ULN-2024A
PBD352313N	RFA	ULN-2023A
PBD352314N	RFA	ULN-2022A
PBD353801J	RFA	ULN-2801R§
PBD353802J	RFA	ULN-2804R§
PBD353803J	RFA	ULN-2803R§
PBD353804J	RFA	ULN-2802R§
PWM25CK	SIL	SG 3525AJ
PWM27CK	SII	SG 3527AJ
Q2T2222	TI	TPQ-2222
Q2T3725	TI	TPQ-3725
S4534	AMI	UCN-5801A

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SG2003J	SG	ULS-2003R
SG2003N	SG	ULN-2003A
SG2004J	SG	ULS-2004R
SG2004N	SG	ULN-2004A
SG2064W	SG	ULN-2064B
SG2065W	SG	ULN-2065B
SG2066W	SG	ULN-2066B
SG2067W	SG	ULN-2067B
SG2068W	SG	ULN-2068B
SG2069W	SG	ULN-2069B
SG2070W	SG	ULN-2070B
SG2071W	SG	ULN-2071B
SG2074W	SG	ULN-2074B
SG2075W	SG	ULN-2075B
SG2076W	SG	ULN-2076B
SG2077W	SG	ULN-2077B
SG2841N	SG	UDN-2841B
SG2845N	SG	UDN-2845B
SG3045J	SG	ULS-2045H
SG3046N	SG	ULN-2046A
SG3081N	SG	ULN-2081A
SG3082N	SG	ULN-2082A
SG30832N	SG	ULN-2083A
SG3086N	SG	ULN-2086A
SG3146N	SG	ULN-2046A-1
SG3173P	SG	ULN-3751Z
SG3183N	SG	ULN-2083A-1
SG3525AJ	SG	SG-3525AJ
SG3525AN	SG	SG-3525AN
SG3526J	SG	SG-3526J
SG3526N	SG	SG-3526N
SG3527AJ	SG	SG-3527AJ
SG3527AN	SG	SG-3527AN
SG3548N	SG	(ULN-8130A)
SG3635P	SG	UDN-2935Z
SG3637	SG	UDN-2545B
SG3638AS	SG	UDN-2976W
SG3643AS	SG	(UDN-2962W)
SG3821J	SG	ULS-2045H
SG3821N	SG	ULN-2046A

§Sprague engineering bulletin in preparation.
()Functional equivalent only; improved performance but not necessarily pin compatible.

COMPETITIVE CROSS-REFERENCE

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SG3822N	SG	ULN-2054A
SG3851J	SG	ULS-2011R
SG3851N	SG	ULN-2011A
SG3852J	SG	ULS-2012R
SG3852N	SG	ULN-2012A
SG3853J	SG	ULS-2013R
SG3853N	SG	ULN-2013A
SG3854J	SG	ULS-2014R
SG3854N	SG	ULN-2014A
SG3886N	SG	ULN-2086A
SG6118N	SG	UDN-6118A
Si3525BK	SII	(SG-3525AJ)
Si3527BK	SII	(SG-3527AJ)
SL3045C	PLS	ULS-2045R
SL3046C	PLS	ULN-2046A
SL3054	PLS	ULN-2054A
SL3081C	PLS	ULN-2081A
SL3082C	PLS	ULN-2082A
SL3083E	PLS	ULN-2083A
SL3086	PLS	ULN-2086A
SL3145E	PLS	ULS-2045H
SL3146E	PLS	ULN-2046A-1
SL3183E	PLS	ULN-2083A-1
SN75064NE	TI	ULN-2064B
SN75065NE	TI	ULN-2065B
SN75066NE	TI	ULN-2066B
SN75067NE	TI	ULN-2067B
SN75068NE	TI	ULN-2068B
SN75069NE	TI	ULN-2069B
SN75070NE	TI	ULN-2070B
SN75071NE	TI	ULN-2071B
SN75074NE	TI	ULN-2074B
SN75075NE	TI	ULN-2075B
SN75076NE	TI	ULN-2076B
SN75077NE	TI	ULN-2077B
SN75407P	TI	UDN-5732M
SN75437ND	TI	UDN-2543B

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SN75465J	TI	ULN-2025R§
SN75465N	TI	ULN-2025A
SN75466J	TI	ULN-2021R§
SN75466N	TI	ULN-2021A
SN75467J	TI	ULN-2022R§
SN75467N	TI	ULN-2022A
SN75468J	TI	ULN-2023R§
SN75468N	TI	ULN-2023A
SN75469J	TI	ULN-2024R§
SN75469N	TI	ULN-2024A
SN75471P	TI	UDN-3611M†
SN75472P	TI	UDN-3612M†
SN75473P	TI	UDN-3613M†
SN75474P	TI	UDN-3614M†
SN75475P	TI	UDN-5712M†
SN75476P	TI	UDN-5711M†
SN75477P	TI	UDN-5722M†
SN75478P	TI	UDN-5713M†
SN75479P	TI	UDN-5714M†
SN755512N	TI	UCN-5811A
SN75518N	TI	UCN-5818A
SN75500N	TI	UCN-5857A
SN75501N	TI	UCN-5858A
SN75551FN	TI	UCN-5851EP
SN75552FN	TI	UCN-5852EP
SN75553FN	TI	UCN-5853EP
SN75554FN	TI	UCN-5853EP
SN75605K	TI	UDN-2950Z
SN76642N	TI	ULN-2111A
SN76643N	TI	ULN-2111A
SP3724QD	TI	TPQ-3724
SP3725QD	TI	TPQ-3725
TA7272P	TOS	(ULN-3755W)
TA7613P	TOS	ULN-2204A
TAA930		ULN-2111A
TCA365	SIEM	(ULN-3751Z)
TD62001AP	TOS	ULN-2001A
TD62001P	TOS	ULN-2001A
TD62002AP	TOS	ULN-2002A

†Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.
§Sprague engineering bulletin in preparation.
()Functional equivalent only; improved performance but not necessarily pin compatible.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
TD62001P	TOS	ULN-2001A
TD62002AP	TOS	ULN-2002A
TD62002P	TOS	ULN-2002A
TD62003AP	TOS	ULN-2003A
TD62003P	TOS	ULN-2003A
TD62004AP	TOS	ULN-2004A
TD62004P	TOS	ULN-2004A
TD62064AP	TOS	ULN-2064B
TD62064P	TOS	ULN-2064B
TD62074AP	TOS	ULN-2074B
TD62074P	TOS	ULN-2074B
TD62081AP	TOS	ULN-2801A
TD62082AP	TOS	ULN-2802A
TD62083	TOS	ULN-2803A
TD62084AP	TOS	ULN-2804A
TD62101P	TOS	ULN-2001A
TD62103P	TOS	ULN-2003A
TD62104P	TOS	ULN-2004A
TD62479P	TOS	UDN-5714M
TD62781AP	TOS	UDN-6118A-2
TD62782AP	TOS	UDN-6128A-2
TDA1060	PE	NE 5560N
TDA1083	PE	ULN-2204A
TID121	TI	TND-933
TID122	TI	TND-940
TID123	TI	TND-938
TID124	TI	TND-939
TL494CJ	TI	TL-594CJ§
TL494CN	TI	TL-594CN
TL494IJ	TI	TL-594IJ§
TL494IN	TI	TL-594IN§
TI495CJ	TI	TL-595CJ§
TL495CN	TI	TL-595CN
TL495IJ	TI	TL-595IJ§
TL495IN	TI	TL-595IN§
TL594CJ	TI	TL-594CJ§
TL594CN	TI	TL-595CN
TL594IJ	TI	TL-594IJ§
TL594IN	TI	TL-594IN§
TL595CJ	TI	TL-595CJ§
TL595CN	TI	TL-595CN
TL595IJ	TI	TL-595IJ§
TL595IN	TI	TL-595IN§
U417B	TLF	ULN-2204A
UA3045DM	FSC	ULS-2045H
UA3046PC	FSC	ULN-2046A
UA3054PC	FSC	ULN-2054A
UA3086PC	FSC	ULN-2086A
UC494ACJ	UNI	TL-594CJ§
UC494ACN	UNI	TL-594CN
UC495ACJ	UNI	TL-595CJ§
UC495ACN	UNI	TL-595CN
UC3525AJ	UNI	SG-3525AJ
UC3525AN	UNI	SG-3525AN
UC3526J	UNI	SG-3526J
UC3526N	UNI	SG-3526N
UC3527AJ	UNI	SG-3527AJ
UC3527AN	UNI	SG-3527AN
UC3717	UNI	(UDN-2953B)
UC3903	UNI	(ULN-8130A)
UCN-4810A	SPR	UCN-5801A
UCN4801N	TI	UCN-5810A
UCN-4815A	SPR	UCN-5815A
UDN-2541B	SPR	(UDN-2543B)
UDN-2542B	SPR	(UDN-2543B)
UDN2841B	MOT	UDN-2841B
UDN2841NE	TI	UDN-2841B
UDN-2845B	MOT	UDN-2845B
UDN2845NE	TI	UDN-2845B

§Sprague engineering bulletin in preparation.
()Functional equivalent only; improved performance but not necessarily pin compatible.

COMPETITIVE CROSS-REFERENCE

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
UDN-2952W	SPR	(UDN-2954W)
UDN5711N	TI	UDN-5711M
UDN5712N	TI	UDN-5712M
UDN5713N	TI	UDN-5713M
UDN5714N	TI	UDN-5714M
UDN-6126A	SPR	UDN-6116A
UDN-6148A	SPR	UDN-6138A
UDN-6164A	SPR	UDN-6116A-1
UDN-6184A	SPR	UDN-6118A-1
UDS-0400H	SPR	UHD-400
UDS-0400H-1	SPR	UHD-400-1
UDS-0400J	SPR	UHC-400
UDS-0400J-1	SPR	UHC-400-1
UDS-0402H	SPR	UHD-402
UDS-0402H-1	SPR	UHD-402-1
UDS-0402J	SPR	UHC-402
UDS-0402J-1	SPR	UHC-402-1
UDS-0403H	SPR	UHD-403
UDS-0403H-1	SPR	UHD-403-1
UDS-0403J	SPR	UHC-403
UDS-0403J-1	SPR	UHC-403-1
UDS-0406H	SPR	UHD-406
UDS-0406H-1	SPR	UHD-406-1
UDS-0406J	SPR	UHC-406
UDS-0406J-1	SPR	UHC-406-1
UDS-0407H	SPR	UHD-407
UDS-0407H-1	SPR	UHD-407-1
UDS-0407J	SPR	UHC-407
UDS-0407J-1	SPR	UHC-407-1
UDS-0408H	SPR	UHD-408
UDS-0408H-1	SPR	UHD-408-1
UDS-0408J	SPR	UHC-408
UDS-0408J-1	SPR	UHC-408-1
UDS-0432H	SPR	UHD-432
UDS-0432H-1	SPR	UHD-432-1
UDS-0432J	SPR	UHC-432
UDS-0432J-1	SPR	UHC-432-1
UDS-0433H	SPR	UHD-433
UDS-0433H-1	SPR	UHD-433-1
UDS-0433J	SPR	UHC-433
UDS-0433J-1	SPR	UHC-433-1
UDS-0500H	SPR	UHD-500
UDS-0500J	SPR	UHC-500
UDS-0502H	SPR	UHD-502
UDS-0502J	SPR	UHC-502
UDS-0503H	SPR	UHD-503
UDS-0503J	SPR	UHC-503
UDS-0506H	SPR	UHD-506
UDS-0506J	SPR	UHC-506
UDS-0507H	SPR	UHD-507
UDS-0507J	SPR	UHC-507
UDS-0508H	SPR	UHD-508
UDS-0508J	SPR	UHC-508
UDS-0532H	SPR	UHD-532
UDS-0532J	SPR	UHC-532
UDS-0533H	SPR	UHD-533
UDS-0533J	SPR	UHC-533
ULN-2001A	MOT	ULN-2001A
ULN2001A	SGS	ULN-2001A
ULN2001AJ	TI	ULN-2001R§
ULN2001AN	TI	ULN-2001A
ULN2002A	MOT	ULN-2002A
ULN2002A	SGS	ULN-2002A
ULN2002AJ	TI	ULN-2002R§
ULN2002AN	TI	ULN-2002A
ULN2003A	MOT	ULN-2003A
ULN2003A	SGS	ULN-2003A
ULN2003AJ	TI	ULN-2003R§
ULN2003AN	TI	ULN-2003A
ULN-2003F	SIG	ULN-2003R§
ULN2003N	SIG	ULN-2003A
ULN2004A	MOT	ULN-2004A
ULN-2004A	SGS	ULN-2004A
ULN2004AJ	TI	ULN-2004R§
ULN2004AN	TI	ULN-2004A
ULN2004F	SIG	ULN-2004R§
ULN2004N	SIG	ULN-2004A

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Competitive Part Number	Manufacturer	Suggested Sprague Replacement
ULN2005AJ	TI	ULN-2005R§
ULN2005AN	TI	ULN-2005A
ULN2064B	MOT	ULN-2064B
ULN2064B	SGS	ULN-2064B
ULN2064NE	TI	ULN-2064B
ULN2065B	MOT	ULN-2065B
ULN2065B	SGS	ULN-2065B
ULN2065NE	TI	ULN-2065B
ULN2066B	MOT	ULN-2066B
ULN-2066B	SGS	ULN-2066B
ULN2066NE	TI	ULN-2066B
ULN2067B	MOT	ULN-2067B
ULN2067B	SGS	ULN-2067B
ULN2067NE	TI	ULN-2067B
ULN2068B	MOT	ULN-2068B
ULN2068B	SGS	ULN-2068B
ULN2068NE	TI	ULN-2068B
ULN2069B	MOT	ULN-2069B
ULN2069B	SGS	ULN-2069B
ULN2069NE	TI	ULN-2069B
ULN2070B	SGS	ULN-2070B
ULN2071B	SGS	ULN-2071B
ULN2074B	MOT	ULN-2074B
ULN2074B	SGS	ULN-2074B
ULN2074NE	TI	ULN-2074B
ULN2075B	MOT	ULN-2075B
ULN-2075B	SGS	ULN-2075B
ULN2075NE	TI	ULN-2075B
ULN2076B	SGS	ULN-2076B
ULN2077B	SGS	ULN-2077B
ULN-2113A	SPR	ULN-2111A
ULN-2240A	SPR	(ULN-3840A)
ULN-2281B	SPR	ULN-3784B
ULN-2401A	SPR	(ULN-2455A)
ULN2801A	MOT	ULN-2801A
ULN2801A	SGS	ULN-2801A
ULN2802A	MOT	ULN-2802A
ULN2802A	SGS	ULN-2802A
ULN2803A	MOT	ULN-2803A
ULN2803A	SGS	ULN-2803A
ULN2804A	MOT	ULN-2804A
ULN2804A	SGS	ULN-2804A
ULN2805A	SGS	ULN-2805A
ULN-3006M	SPR	UGN-3201M
ULN-3006T	SPR	UGN-3019T
ULN-3007M	SPR	UGN-3203M
ULN-3008M	SPR	UGN-3501M
ULN-3008T	SPR	UGN-3501T
ULN-3100M	SPR	UGN-3600M
ULN-3101M	SPR	UGN-3601M
ULN-3330Y-2	SPR	ULN-3330Y
ULN-3783M	SPR	ULN-3782M
ULN-3838A	SPR	ULN-3839A
ULN-8125A	SPR	SG-3525AN
ULN-8125R	SPR	SG-3525AJ
ULN-8126A	SPR	SG-3526N
ULN-8126R	SPR	SG-3526J
ULN-8127A	SPR	SG-3527AN
ULN-8127R	SPR	SG-3527AJ
ULN-8160A	SPR	NE-5560N
ULN-8160R	SPR	NE-5560F
ULN-8161M	SPR	NE-5561N
ULN-8168M	SPR	NE-5568N
ULN-8194A	SPR	TL-594CN
ULN-8194R	SPR	TL-594CJ§
ULN-8195A	SPR	TL-595CN
ULN-8195R	SPR	TL-595CJ§
ULQ-8194A	SPR	TL-594IN§
ULQ-8194R	SPR	TL-594IJ§
ULQ-8195A	SPR	TL-595IN§
ULQ-8195R	SPR	TL-595IJ§
ULS-3006T	SPR	UGS-3019T
UPA2001C	NEC	ULN-2001A
UPA2002C	NEC	ULN-2002A
UPA2003C	NEC	ULN-2003A
UPA2004C	NEC	ULN-2004A

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COMPETITIVE CROSS-REFERENCE

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
US5438A	SPR	UHD-408
US5438J	SPR	UHC-408
US5439J	SPR	UHC-408
US7438A	SPR	UHP-0408
US7438J	SPR	UHC-408
US7439J	SPR	UHL-408
XR2001CN	EXR	ULN-2001R§
XR2001P	EXR	ULQ-2001A§
XR2002CN	EXR	ULN-2002R§
XR2002P	EXR	ULQ-2002A§
XR2003CN	EXR	ULN-2003R§
XR2003P	EXR	ULQ-2003A§
XR2004CN	EXR	ULN-2004R§
XR2004P	EXR	ULQ-2004A§
XR2011CN	EXR	ULN-2011R§
XR2011CP	EXR	ULN-2011A
XR2012CN	EXR	ULN-2012R§
XR2012CP	EXR	ULN-2012A
XR2013CN	EXR	ULN-2013R§
XR2013CP	EXR	ULN-2013A
XR2014CN	EXR	ULN-2014R§
XR2014CP	EXR	ULN-2014A
XR2201CP	EXR	ULN-2001A
XR2202CP	EXR	ULN-2002A
XR2203CP	EXR	ULN-2003A
XR2204CP	EXR	ULN-2004A
XR2205CP	EXR	ULN-2005A
XR6118P	EXR	UDN-6118A
XR6118P-2	EXR	UDN-6118A-2
XR6128P	EXR	UDN-6128A
ZN1060	FER	NE 5560N
552	ITT	ULN-2001A
554	ITT	ULN-2002A
556	ITT	ULN-2003A
652	ITT	ULN-2001A
654	ITT	ULN-2002A
656	ITT	ULN-2003A
9665DC	FSC	ULN-2001R§
9665DM	FSC	ULS-2001R
9665PC	FSC	ULN-2001A
9666DC	FSC	ULN-2002R§
9666DM	FSC	ULS-2002R
9666PC	FSC	ULN-2002A
9667DC	FSC	ULN-2003R§
9667DM	FSC	ULS-2003R
9667PC	FSC	ULN-2003A
9668DC	FSC	ULN-2004R§
9668DM	FSC	ULS-2004R
9668PC	FSC	ULN-2004A

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COMPETITIVE PART-NUMBERING SYSTEMS

Cherry Semiconductor

CS 123 D

PACKAGE. D = PLASTIC DIP.

Exar

XR 2001 C N

PACKAGE. D = SMALL OUTLINE.
N = CERDIP.
P = PLASTIC DIP.

GRADE. C = COMMERCIAL, 0°C TO +70°C.
M = MILITARY, −55°C TO +125°C.
BLANK = IMPROVED COMMERCIAL.

Fairchild

μA 705 P C

TEMPERATURE. C = 0°C TO +70/+75°C.
L = −55°C TO +85°C.
M = −55°C TO +125°C.

PACKAGE. D = CERAMIC DIP.
J = FLANGE MOUNT (TO-66).
K = FLANGE MOUNT (TO-3).
P = PLASTIC DIP.
R = CERAMIC MINI-DIP.
T = MINI-DIP.
U = POWER TAB (TO-220).

Fujitsu

MB 3759 E C

PACKAGE. C = CERAMIC.
P = PLASTIC DIP.
Z = CERDIP.

Hitachi

HA 1199 P

P = PLASTIC DIP.
C = CERAMIC DIP.
CG = CERAMIC LEADLESS CHIP CARRIER.
CP = PLASTIC LEADED CHIP CARRIER.
SO = SMALL OUTLINE.
G = CERDIP.

COMPETITIVE PART-NUMBERING SYSTEMS

Integrated Power

IP 3 P 45 T

PACKAGE. D = CERAMIC.
J = CERDIP.
K = METAL FLANGE MOUNT (TO-3).
N = PLASTIC DIP.
T = POWER TAB (TO-220).

TEMPERATURE. 1 = −55°C TO +125°C.
2 = −25°C TO +85°C.
3 = 0°C TO +70°C.

JAN

M38510 / 14103 B E C

LEAD FINISH. A = KOVAR/SOLDER.
B = KOVAR/TIN PLATE.
C = KOVAR/GOLD PLATE.

PACKAGE. A = 14-PIN FLAT PACK.
C = 14-PIN CERAMIC DIP.
E = 16-PIN CERAMIC DIP.
F = 16-PIN FLAT PACK.

PRODUCT ASSURANCE LEVEL. B = CLASS B.
S = CLASS S.

Mitsubishi

M 5 4523 P

PACKAGE. K = CERDIP.
P = PLASTIC DIP.

TEMPERATURE. 5 = COMMERCIAL/INDUSTRIAL.
9 = MILITARY.

Motorola

MC 1311 P

PACKAGE. D = SMALL OUTLINE.
K = METAL FLANGE MOUNT (TO-3).
L = CERAMIC DIP.
P = PLASTIC DIP.
PQ = PLASTIC QUAD IN-LINE.
R = METAL FLANGE MOUNT (TO-66).
T = POWER TAB (TO-220).
U = CERAMIC DIP.

National Semiconductor

LM 380 N

PACKAGE. N = PLASTIC DIP.
D = CERAMIC DIP.
T = POWER TAB (TO-220).

COMPETITIVE PART-NUMBERING SYSTEMS

Pro-Electron

TD A 1060 P

PACKAGE. D = CERDIP.
P = PLASTIC DIP.
Q = PLASTIC QUAD IN-LINE.
BLANK = SEE DETAIL SPECIFICATION.

TEMPERATURE. A = SEE DETAIL SPECIFICATION.
B = 0° TO +70°C.
C = −55°C TO +125°C.
F = −40°C TO +85°C.

RCA

CA 758 E

PACKAGE. D = CERAMIC DIP.
E = PLASTIC DIP.
F = CERDIP.
M = POWER TAB (TO-220).
Q = PLASTIC QUAD IN-LINE.
W = STAGGERED-LEAD PLASTIC QUAD IN-LINE.
BLANK = SEE DETAILED SPECIFICATION.

Signetics

NE 564 N

PACKAGE. A = PLASTIC LEADED CHIP CARRIER.
D = SMALL OUTLINE.
F = CERDIP.
FE = MINI-CERDIP.
G = LEADLESS CHIP CARRIER.
I = CERAMIC DIP.
N = PLASTIC DIP.
T = SMALL OUTLINE.
U = PLASTIC SIP.

TEMPERATURE. NE = 0°C TO +70°C.
SA = −40°C TO +85°C.
SE = −55°C TO +125°C.
SU = −25°C TO +85°C.

Silicon General

SG 1524 F

PACKAGE. J = CERDIP.
K = METAL FLANGE MOUNT (TO-3).
L = LEADLESS CHIP CARRIER.
M = MINI-DIP.
N = PLASTIC DIP.
P = POWER TAB (TO-220).
R = METAL FLANGE MOUNT (TO-66).
W = PLASTIC DIP SEMI-TAB.
Y = MINI-CERDIP.

COMPETITIVE PART-NUMBERING SYSTEMS

Siliconix

PWM 25 B K

PACKAGE. J = PLASTIC DIP.
K = CERDIP.
P = CERAMIC DIP.
R = CERAMIC DIP.
Y = SMALL OUTLINE.

TEMPERATURE. A = −55°C TO +125°C.
B = −25°C TO +85°C.
C = 0°C TO +70°C.
D = −40°C TO +85°C.

Texas Instruments

SN 75 064 NE

PACKAGE. D = SMALL OUTLINE (0.150″ WIDE).
DW = SMALL OUTLINE (0.300″ WIDE).
FG = CERAMIC RECTANGULAR LEADLESS CHIP CARRIER.
FH = LEADLESS CHIP CARRIER.
FK = CERAMIC SQUARE LEADLESS CHIP CARRIER.
FM = PLASTIC RECTANGULAR LEAD CHIP CARRIER.
FN = PLASTIC SQUARE LEADED CHIP CARRIER.
J = CERDIP.
JD = CERAMIC DIP.
K = POWER TAB (TO-220).
N = PLASTIC DIP.
ND = PLASTIC DIP SEMI-TAB.
NE = PLASTIC DIP SEMI-TAB.
P = PLASTIC MINI-DIP.

TEMPERATURE. 55 = −55°C TO +125°C.
75 = 0°C TO +70°C.

TL 494 C J

PACKAGE. AS SHOWN ABOVE.

TEMPERATURE. C = 0°C TO +70°C.
E = −40°C TO +85°C.
I = −25°C TO +85°C.
M = −55°C TO +125°C.

Toshiba

TA 7272 P

PACKAGE. C = CERAMIC.
P = PLASTIC.

HOW TO ORDER

TO PLACE AN ORDER, obtain price and delivery information, or request technical literature, contact your local Sprague sales office or sales representative. See inside back cover, or:

From U.S. and Canada:	Sprague Electric Co. 92 Hayden Avenue Lexington, MA 02173 (617) 862-5500 Telex: 710-321-0021
From Europe and Mideast:	Sprague World Trade Corp. 18 Avenue Louis Casai 1209-Geneva Switzerland 98-4021 Telex: 845-23469
From Asia:	Sprague Asia Ltd. G.P.O. Box 4289 Hong Kong 0-283188 Telex: 43395

REQUESTS FOR technical information and applications assistance can be sent to the appropriate manufacturing facility.

For integrated circuits:

Sprague Electric Company
Semiconductor Group
115 Northeast Cutoff
Worcester, MA 01606
(617) 853-5000
(800) 247-2076 in Mass.
(800) 247-2077
Telex: 710-340-6304

For Hall effect and optoelectronic sensors:

Sprague Electric Company
Sensor Division
70 Pembroke Road
Concord, NH 03301
(603) 224-2755
(603) 224-1961
Telex: 710-361-1495

For discrete semiconductor chips, discrete semiconductors in plastic packages, MOS capacitors:

Sprague Electric Company
Discrete Semiconductor Division
70 Pembroke Road
Concord, NH 03301
(603) 224-1961
Telex: 710-361-1495

2

SECTION 2—HIGH-VOLTAGE (≥100 V) INTERFACE DRIVERS

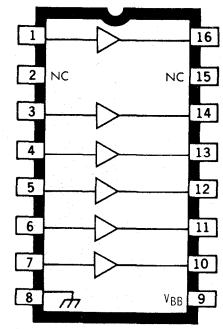
SELECTION GUIDE

(in order of output breakdown voltage rating)

V_{OUT}	I_{OUT}	Outputs	Device Type	Page
100 V	250 mA	Sink 4	Series UHP-500	3-3
100 V	250 mA	Sink 4	Series UHC-500	6-7
100 V	350 mA	Sink 8†	UCN-5823A	5-55
100 V	350 mA	Sink 8†	UCN-5843A	5-82
100 V	350 mA	Sink 8†	UCS-4823H	6-79
−115 A	20 mA	Sink 8	Series UDN-7180A	2-17
115 V	−25 mA	Source 6	UDN-6116/26A-1	2-3
115 V	−25 mA	Source 8	UDN-6118/28A-1	2-3
120 V	300 mA	Sink 4	UDS-5791H	6-97
140 V	−25 mA	Source 8	UDN-6514A/R	2-7
150 V	−40 mA	Source 10†	UCN-5910A	5-129
150 V	250 mA	Sink 7	Series ULN-7000A	2-13
150 V	350 mA	Sink 4†	UCN-5900A	5-123
150 V	350 mA	Sink 8†	UCN-5901A	5-123
150 V	1.0 A	Sink 4	ULN-7064/68/74B	2-15
200 V	−25 mA	Source 8	UDN-6510A/R	2-7
200 V	200 mA	Sink 8	UDN-6540B	2-10
225 V	100 mA	Sink 32	UCN-5851/52A/EP	5-87

Voltage ratings shown are maximum allowable; current ratings are maximum tested condition.
†Latched drivers.

SERIES UDN-6100A AND UDN-6100R FLUORESCENT DISPLAY DRIVERS



Dwg. No. A-9643A

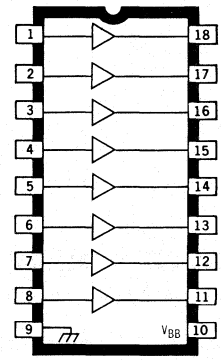
UDN-6116*

FEATURES

- •Digit or Segment Drivers
- •Low Input Current
- •Integral Output Pull-Down Resistors
- •High Output Breakdown Voltage
- •Single or Split Supply Operation

CONSISTING of six or eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. All devices are capable of driving the digits and/or segments of these displays and are designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications. The highest voltage parts (suffix A-1) are also used in gas-discharge display applications as anode (digit) drivers.

Twenty-four standard devices are listed, so that a circuit designer may select the optimum device for his application. Input characteristics, number of drivers, package style, and output voltage are tabulated for each device in the Device Type Number Designation chart. With any device, the output load is activated when the input is pulled towards the positive supply (active 'high'). All units operate over the temperature range of −20°C to +85°C.



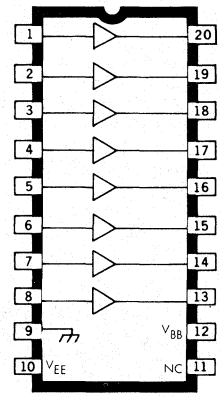
Dwg. No. A-9641A

UDN-6118*
UDN-6128*

***Always specify complete part number, such as:**

UD N — 6116 A — 2

- **INSTRUCTIONS:** SELECTED VERSION. SEE TYPE NUMBER DESIGNATION, NEXT PAGE.
- **PACKAGE:** A = PLASTIC DIP, R = CERAMIC DIP
- **DEVICE TYPE.**
- **OPERATING TEMPERATURE RANGE.** N = −20°C to +85°C
- **FAMILY.** UD = DIGITAL DRIVERS



DWG. NO. A-11,222

UDN-6138*

DEVICE TYPE NUMBER DESIGNATION

Input Compatibility	No. of Drivers	V_{OUT}	No. of Pins	Type Number	
				Plastic DIP	Ceramic DIP
5V TTL, CMOS	6	60 V	16	UDN-6116A-2	UDN-6116R-2
		80 V	16	UDN-6116A	UDN-6116R
		110 V	16	UDN-6116A-1	—
	8	60 V	18	UDN-6118A-2	UDN-6118R-2
		80 V	18	UDN-6118A	UDN-6118R
		110 V	18	UDN-6118A-1	—
		±30 V	20	UDN-6138A-2	—
		±40 V	20	UDN-6138A	—
6-15V CMOS, PMOS	8	60 V	18	UDN-6128A-2	UDN-6128R-2
		80 V	18	UDN-6128A	UDN-6128R
		110 V	18	UDN-6128A-1	—

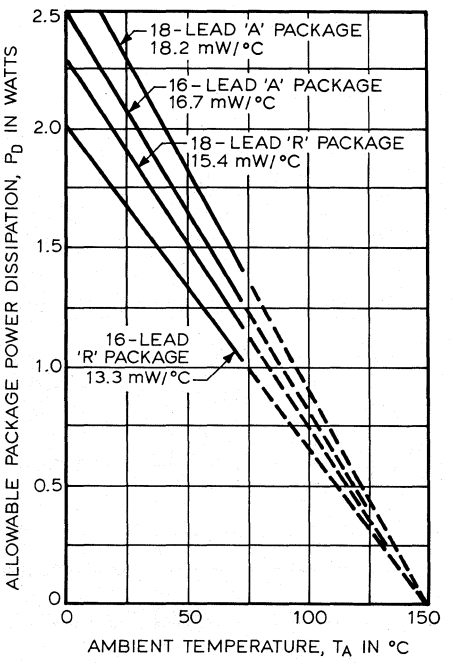
ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

(Voltages are with reference to ground unless otherwise shown)

Supply Voltage, V_{BB} (all devices, suffix A or R) . . . . . 85 V
(UDN-6138A or R, ref. V_{EE}) . . . . . 85 V
(all devices, suffix A-1) . . . . . 115 V
(all devices, suffix A-2 or R-2) . . . . . 65 V
(UDN-6138A-2 or R-2, ref, V_{EE}) . . . . . 65 V
Supply Voltage, V_{EE} (UDN-6138 all suffixes) . . . . . −40 V
Input Voltage, V_{IN} (all devices) 20
(UDN-6138 all suffixes, ref. V_{EE}) . . . . . 55 V
Output Current, I_{OUT} . . . . . −40 mA
Allowable Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

Caution: The high input impedance of these devices makes them susceptible to static discharge damage associated with handling and testing. Techniques similar to those used for handling MOS devices should be employed.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-14,318

ELECTRICAL CHARACTERISTICS (over operating temperature range)

Note: All Values Specified At ——

Suffixes	A	R	A-1	A-2	R-2	
V_{BB} =	80	80	110	60	60	Volts
*V_{EE} =	0	0	NA	0	0	Volts

*UDN-6138

Characteristic	Symbol	Applicable Devices		Test Conditions	Limits			
		Basic Part. No.	Suffix		Min.	Typ.	Max.	Units
Output Leakage Current	I_{OUT}	All	All	V_{IN} = 0.4 V	—	—	15	µA
Output OFF Voltage	V_{OUT}	All	All	V_{IN} = 0.4 V	—	—	1.0	V
Output Pull-Down Current	I_{OUT}	All	A or R	Input Open, V_{OUT} = V_{BB}	450	650	1100	µA
			A-1		600	900	1500	µA
			A-2 or R-2		350	500	775	µA
Output ON Voltage	V_{OUT}	UDN-6116/18/38	A or R	V_{IN} = 2.4 V, I_{OUT} = −25 mA	77	78	—	V
			A-1		107	108	—	V
			A-2 or R-2		57	58	—	V
		UDN-6128	A or R	V_{IN} = 4.0 V, I_{OUT} = −25 mA	77	78	—	V
			A-1		107	108	—	V
			A-2 or R-2		57	58	—	V
Input ON Current	I_{IN}	UDN-6116/18/38	All	V_{IN} = 2.4 V	—	120	225	µA
				V_{IN} = 5.0 V	—	375	650	µA
		UDN-6128	All	V_{IN} = 4.0 V	—	130	250	µA
				V_{IN} = 15 V	—	675	1150	µA
Supply Current	I_{BB}	All	All	All Inputs Open	—	10	100	µA
		UDN-6116	A or R	All Inputs = 2.4 V	—	5.0	7.5	mA
			A-1	Two Inputs = 2.4 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 2.4 V	—	4.0	6.0	mA
		UDN-6118/38	A or R	All Inputs = 2.4 V	—	6.0	9.0	mA
			A-1	Two Inputs = 2.4 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 2.4 V	—	5.5	8.0	mA
		UDN-6128	A or R	All Inputs = 4.0 V	—	6.0	9.0	mA
			A-1	Two Inputs = 4.0 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 4.0 V	—	5.5	8.0	mA

RECOMMENDED OPERATING CONDITIONS

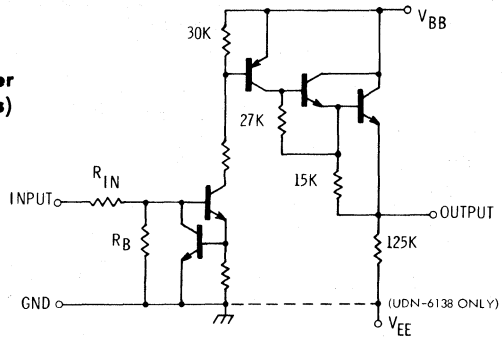
Supply Voltage	V_{BB}	UDN-6116/18/28	A or R		5.0	—	70	V
			A-1		5.0	—	100	V
			A-2 or R-2		5.0	—	50	V
		UDN-6138	A		5.0	—	−40	V
			A-2		5.0	—	−30	V
	V_{EE}	UDN-6138	A		0	—	−40	V
			A-2		0	—	−30	V
Input ON Voltage	V_{IN}	UDN-6116/18/38	All		2.4	—	15	V
		UDN-6128	All		4.0	—	15	V
Output ON Current	I_{OUT}	All	All		—	—	−25	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

PARTIAL SCHEMATIC

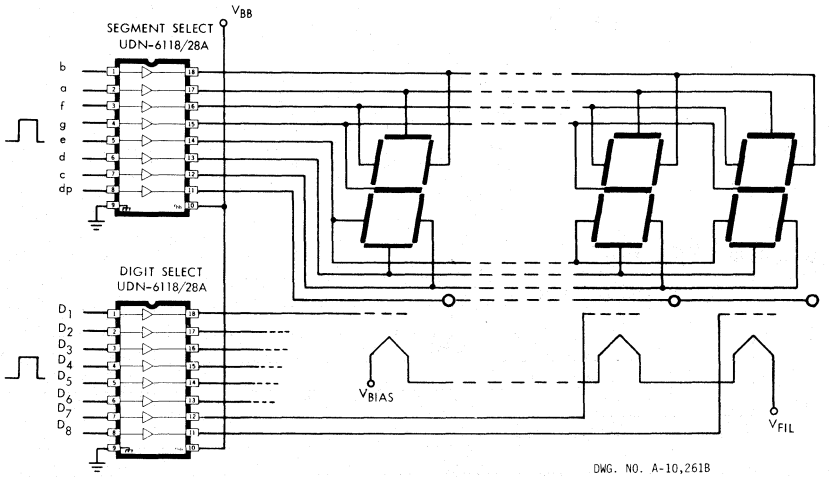
Type (All Suffixes)	R_{IN}	R_B
UDN-6116/18/38	10 kΩ	30 kΩ
UDN-6128	20 kΩ	20 kΩ

One Driver (All Types)



DWG.NO. A-10,592C

TYPICAL MULTIPLEXED FLUORESCENT DISPLAY

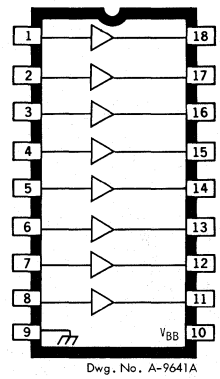


DWG. NO. A-10,261B

UDN-6510A/R AND UDN-6514A/R HIGH-VOLTAGE SOURCE DRIVERS

FEATURES

- TTL/MOS-Compatible Inputs
- High Output-Breakdown Voltage
- 40 mA Output-Current Capability
- Low Power Dissipation
- Reliable Monolithic Construction



Dwg. No. A-9641A

EASY, EFFECTIVE INTERFACE for low-level TTL or MOS circuitry and high-voltage loads is available with Sprague UDN-6510A/R and UDN-6514A/R bipolar integrated circuits. These eight-channel devices drive the anodes of gas-discharge displays or the grids and anodes of large, multiplexed dot-matrix vacuum-fluorescent display panels.

Types UDN-6510A and UDN-6510R supply an output-voltage swing of up to 100 V with a maximum V_{BB} of 200 V. Typically, the output is switched between +100 V and +180 V.

Types UDN-6514A and UDN-6514R can switch output-voltage levels from ground to +135 V with appropriate pull-down circuitry and a maximum supply voltage of +140 V.

Each device in the series has eight independent drivers made up of switched constant-current level shifters and PNP/NPN driver stages. Driver inputs operate with open-drain PMOS or CMOS, or with open-collector or standard TTL.

Types UDN-6510R and UDN-6514R are furnished in 18-pin dual in-line industrial-grade, hermetically sealed ceramic packages. Types UDN-6510A and UDN-6514A are supplied in inexpensive 18-pin dual in-line plastic packages. To simplify applications designs, all units have input connections on one side of the package and output pins on the other. All devices are rated for operation over the temperature range of −20°C to +85°C.

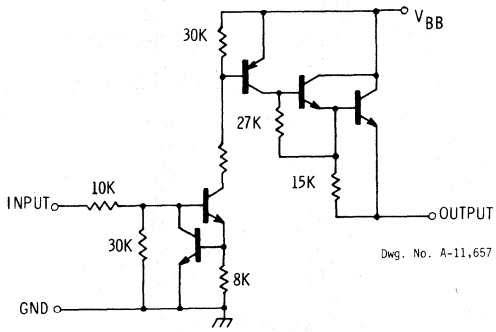
ABSOLUTE MAXIMUM RATINGS

at T_A = +25°C

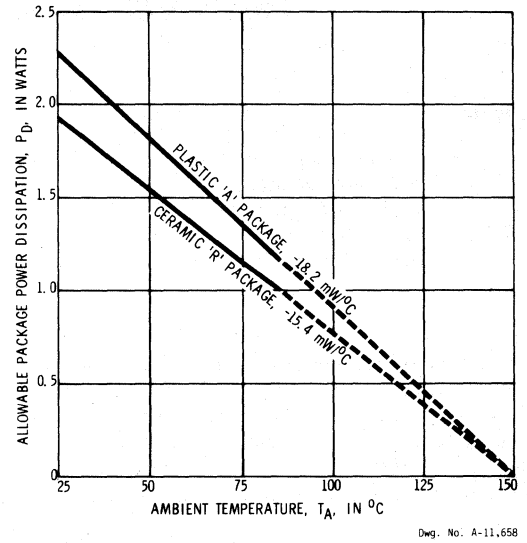
(V_{REF} = GROUND unless otherwise specified)

Supply Voltage, V_{BB} (UDN-6510A/R) ..... 200 V
(UDN-6514A/R) ..... 140 V
Output OFF Voltage (V_{REF} = V_{BB}), V_{OUT} (UDN-6510A/R) ..... −100 V
Input Voltage, V_{IN} ..... 20 V
Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

PARTIAL SCHEMATIC
One Driver (All Types)



PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Caution: The high input impedance of these devices makes them susceptible to static discharge damage associated with handling and testing. Techniques similar to those used for handling MOS devices should be employed.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 200 V (UDN-6510A/R) or 140 V (UDN-6514A/R), all voltage measurements are referenced to ground (unless otherwise noted)

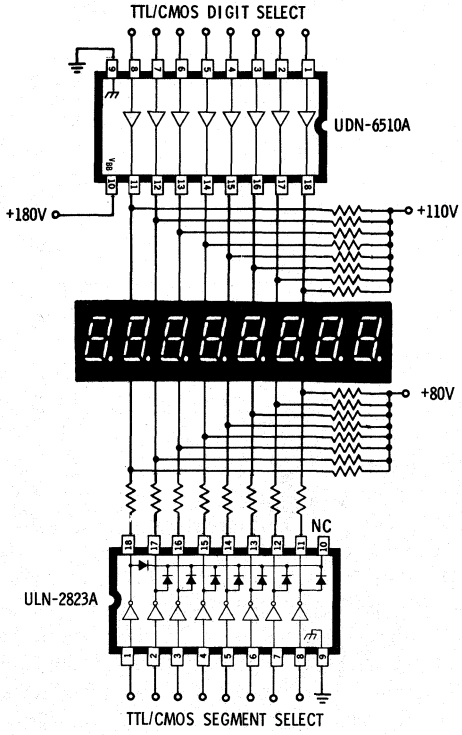
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{OUT}	UDN-6510A/R	V_{OUT} = 100 V, V_{IN} = 0.4 V, T_A = +70°C	—	—	15	μA
		UDN-6514A/R	V_{OUT} = 0 V, V_{IN} = 0.4 V, T_A = +70°C	—	—	15	μA
Output ON Voltage	V_{OUT}	UDN-6510A/R	V_{IN} = 2.4 V, I_{OUT} = −25 mA	195	197	—	V
		UDN-6514A/R	V_{IN} = 2.4 V, I_{OUT} = −25 mA	135	137	—	V
Input ON Current	I_{IN}	All	V_{IN} = 2.4 V	—	120	225	μA
			V_{IN} = 5.0 V	—	375	650	μA
Supply Current	I_{BB}	All	All inputs open	—	10	100	μA
			One input = 3.5 V	—	—	500	μA

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	V_{BB}	UDN-6510A/R		55	—	180	V
		UDN-6514A/R		55	—	130	V
Output OFF Voltage	V_{OUT}	UDN-6510A/R	Reference V_{BB}	—	—	−80	V
Input ON Voltage	V_{IN}	All		2.4	—	15	V
Output ON Current	I_{OUT}	All		—	—	−25	mA

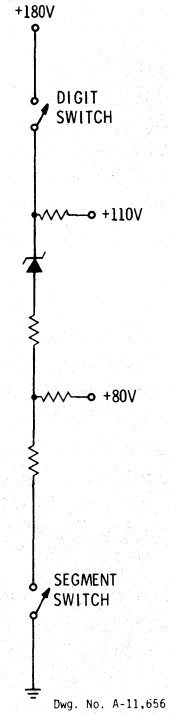
NOTE: Negative current is defined as coming out of the specified device pin.

TYPICAL PLASMA GAS-DISCHARGE DISPLAY APPLICATION



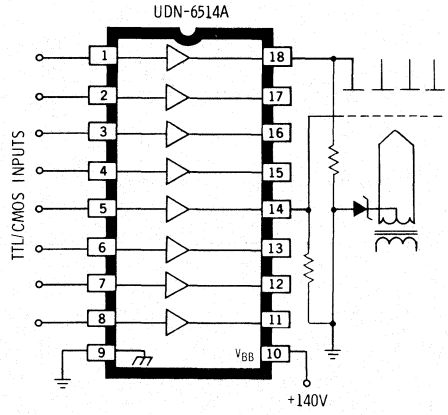
Dwg. No. A-11,655

EQUIVALENT CIRCUIT



Dwg. No. A-11,656

MULTIPLEXED DOT-MATRIX VACUUM-FLUORESCENT DISPLAY APPLICATION

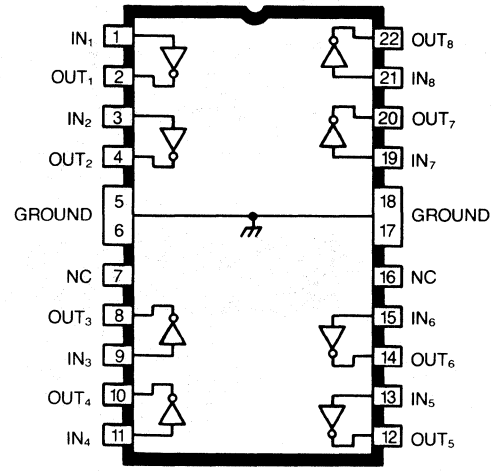


Dwg. No. A-11,659

UDN-6540B
8-CHANNEL DMOS HIGH-VOLTAGE DRIVER

FEATURES

- 200 V Outputs
- CMOS, PMOS Compatible
- Internal Gate Limiting Resistors
- Diode Clamped Inputs and Outputs
- Improved Output SOA

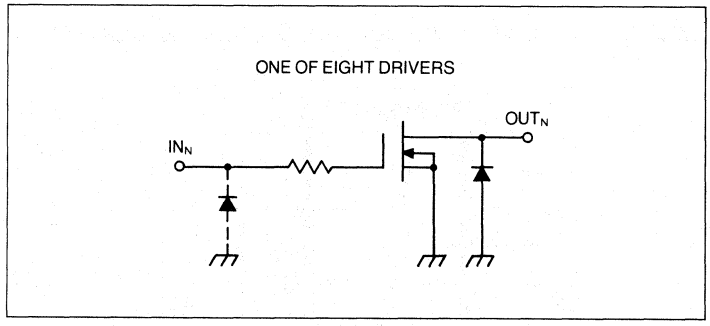


Dwg. No. W-103

The UDN-6540B is an eight-channel high-voltage DMOS driver capable of sinking 200 mA and maintaining an output OFF voltage of 200 V. This device has many possible applications such as driving piezoelectric elements, gas-discharge or electroluminescent displays, and other high-voltage power loads. This device is input compatible with 7-20 V logic such as PMOS, CMOS, and high-voltage open collector TTL.

Because DMOS outputs have output SOA superior to that of conventional bipolar technologies, the UDN-6540B is ideal for inductive load applications. Unlike NPN transistors, DMOS devices can operate safely to their breakdown voltage limit without risk of secondary breakdown (latch-back) or sacrifice of reliability.

The UDN-6540B is furnished in a 22-pin dual in-line package with 0.400" row centers and sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat-sinks for increased power dissipation with standard IC sockets and printed wiring boards.

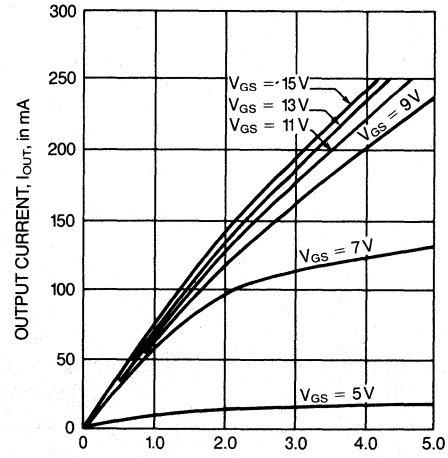


Dwg. No. W-104

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{DS} 200V
Input Voltage, V_{IN} 20V
Output Current, I_{OUT} 250mA
Power Dissipation, P_D ..... See Graph
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range, T_A .... −20°C to +85°C

OUTPUT CURRENT AS A FUNCTION OF V_{DS}

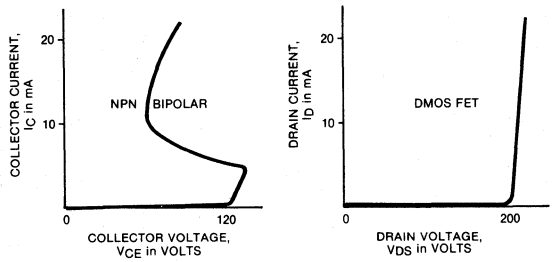


Dwg. No. W-169

ELECTRICAL CHARACTERISTICS at T_A = +25°C

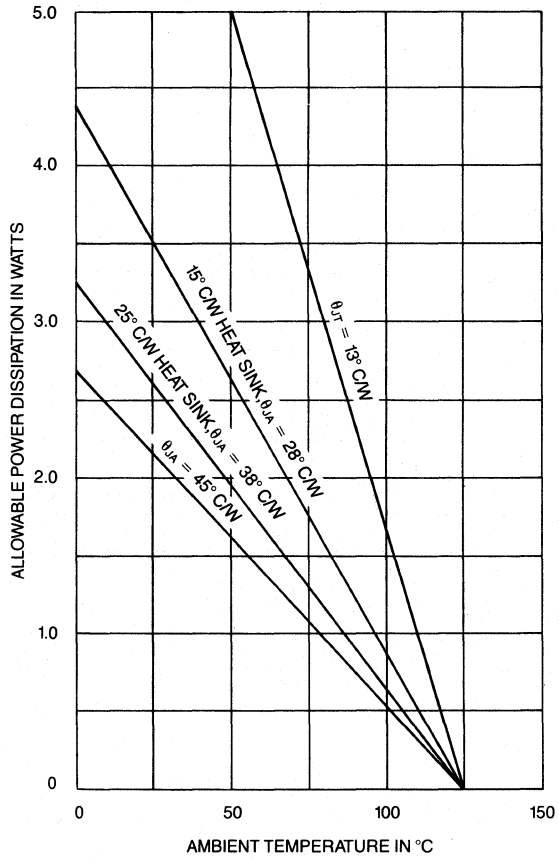
Characteristics	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{DSS}	V_{DS} = 200V, Gate Shorted to Source	—	10	µA
Drain to Source ON Voltage	$V_{DS(ON)}$	V_{GS} = 10V, I_{OUT} = 100mA	—	2.5	V
		V_{GS} = 10V, I_{OUT} = 200mA	—	5.0	V
		V_{GS} = 15V, I_{OUT} = 200mA	—	4.0	V
Input Threshold Voltage	V_{TH}	I_{OUT} = 10mA, V_{DS} = 0.5V	—	7.0	V
		I_{OUT} = 50mA, V_{DS} = 1.0V	—	8.5	V
Turn-On Delay	t_{ON}	0.5E_{IN} to 0.5E_{OUT}, R_L = 1 kΩ, V_{OUT} = 200V	—	0.5	µs
Turn-Off Delay	t_{OFF}	0.5E_{IN} to 0.5E_{OUT}, R_L = 1 kΩ, V_{OUT} = 200V	—	0.5	µs

BREAKDOWN CHARACTERISTICS



Dwg. No. SD-113

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. W-105

SERIES ULN-7000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

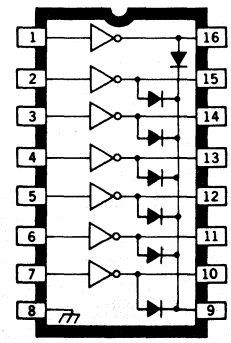
These high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

Series ULN-7001A devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.

Series ULN-7002A is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-7003A has a 2.7 kΩ series base resistor for each Darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs—particularly those beyond the capabilities of standard logic buffers.

Series ULN-7004A has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-7003A, while the required input voltage is less than that required by Series ULN-7002A.

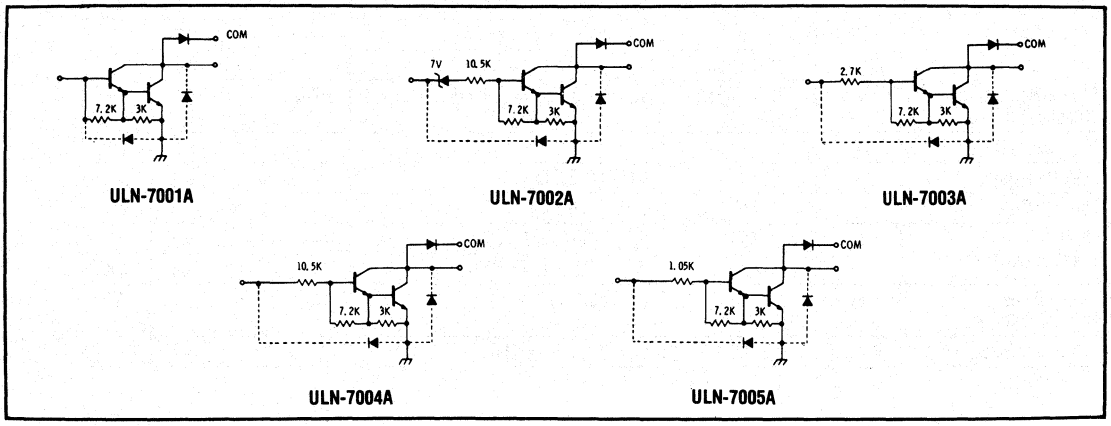


Series ULN-7005A is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 250 mA when driven from a "totem pole" logic output.

Series ULN-7000A is the original high-voltage, high-current Darlington Array. The output transistors are capable of sinking 300 mA and will sustain at least 150 V in the OFF state. Outputs may be paralleled for higher load-current capability.

All Series ULN-7000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These devices can also be supplied in a hermetic dual in-line package for use in military and aerospace applications.

PARTIAL SCHEMATICS



ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} . . . . . 150 V
Input Voltage,
V_{IN} (ULN-7002/7003/7004A) . . . . . 30 V
(ULN-7005A) . . . . . 15 V
Continuous Collector Current, I_C . . . . . 300 mA
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D (total package) . . . . . 2.0 W*
Operating Ambient Temperature Range, T_A . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Derate at rate of 16.67 mW/°C above 25°C.

Device Number Designation

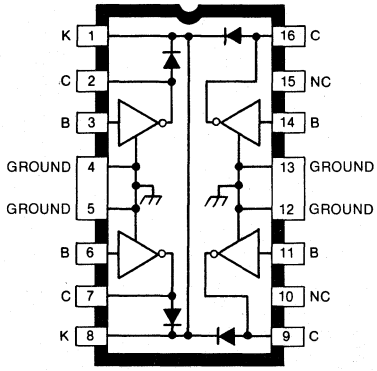
Logic	Type Number
General Purpose PMOS, CMOS	ULN-7001A
14-25 V PMOS	ULN-7002A
5 V TTL, CMOS	ULN-7003A
6-15 V CMOS, PMOS	ULN-7004A
High-Output TTL	ULN-7005A

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	V_{CE} = 150 V, T_A = 25°C	—	—	50	μA
			V_{CE} = 150 V, T_A = 70°C	—	—	100	μA
		ULN-7002A	V_{CE} = 150 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
		ULN-7004A	V_{CE} = 150 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	I_C = 100 mA, I_B = 250 μA	—	1.2	1.3	V
			I_C = 250 mA, I_B = 350μA	—	1.4	1.6	V
Input Current	$I_{IN(ON)}$	ULN-7002A	V_{IN} = 17 V	—	0.82	1.25	mA
		ULN-7003A	V_{IN} = 3.85 V	—	0.93	1.35	mA
		ULN-7004A	V_{IN} = 5.0 V	—	0.35	0.5	mA
			V_{IN} = 12 V	—	1.0	1.45	mA
		ULN-7005A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	ULN-7002A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	13	V
		ULN-7003A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
		ULN-7004A	V_{CE} = 2.0 V, I_C = 100 mA	—	—	5.0	V
			V_{CE} = 2.0 V, I_C = 150 mA	—	—	6.0	V
			V_{CE} = 2.0 V, I_C = 200 mA	—	—	7.0	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	8.0	V
		ULN-7005A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULN-7001A	V_{CE} = 2.0 V, I_C = 250 mA	1000	—	—	—
Input Capacitance	C_{IN}	All		—	15	25	pF
Turn-On Delay	t_{PLH}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	All	V_R = 150 V, T_A = 25°C	—	—	50	μA
			V_R = 150 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	All	I_F = 250 mA	—	1.7	2.0	V
Sustaining Voltage	$V_{CE(SUS)}$	All	L = 2 mH; R = 450 Ω	90	—	—	V

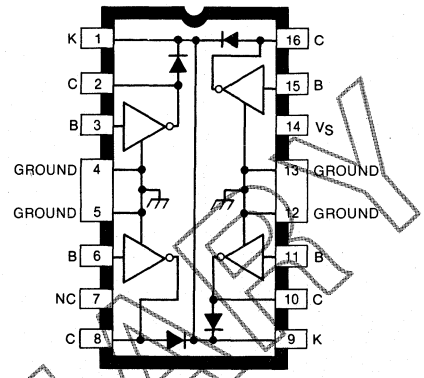
ULN-7064B, ULN-7068B AND ULN-7074B QUAD HIGH-VOLTAGE, 1 A DARLINGTON ARRAYS

ULN-7064B



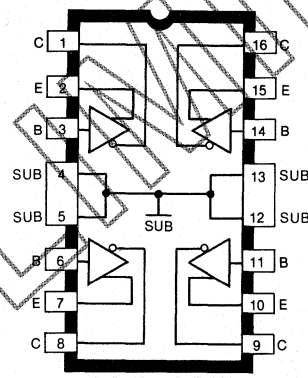
Dwg. No. A-13,669

ULN-7068B



Dwg. No. A-13,670

ULN-7074B



Dwg. No. A-13,671

The ULN-7064B, ULN-7068B and ULN-7074B quad Darlington arrays are high-voltage versions of the industry standard ULN-2064B through ULN-2077B Darlington arrays. The ULN-7064B is the basic driver. Four open-collector Darlingtons feature 150 V minimum breakdowns, 90 V sustaining voltages and integral diodes for inductive load transient suppression.

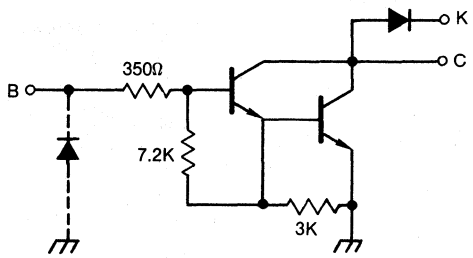
The ULN-7068B includes additional predriver stages for minimum input loading. The ULN-7074B features open emitter outputs for emitter follower or output current sensing applications.

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . . 150 V
Sustaining Voltage, $V_{CE(sus)}$ . . . . . 90 V
Continuous Output Current, I_C . . . . . 1.0 A

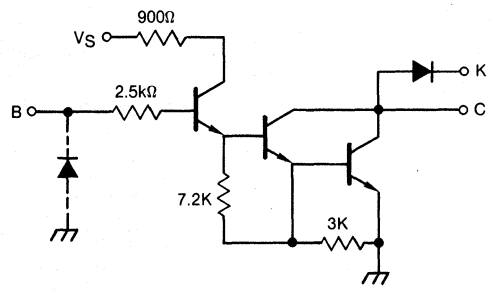
PARTIAL SCHEMATICS

ULN-7064B



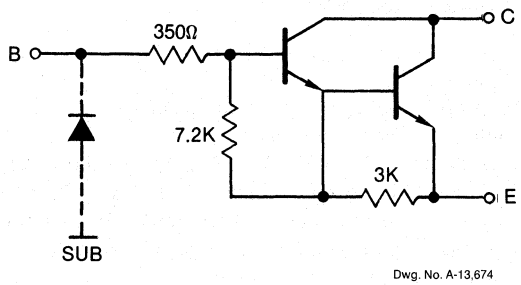
Dwg. No. 13,672

ULN-7068B



Dwg. No. A-13,673

ULN-7074B

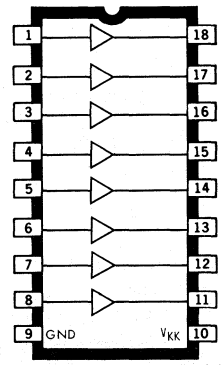


Dwg. No. A-13,674

SERIES UDN-7180A
GAS DISCHARGE DISPLAY SEGMENT DRIVERS

FEATURES

- Reliable Monolithic Construction
- High Output Breakdown Voltage
- Low Power
- TTL/MOS Compatible Inputs



Dwg. No. A-9640A

Description

Series UDN-7180A segment drivers are monolithic high-voltage bipolar integrated circuits for interfacing between MOS or other low-voltage circuits and the cathode of gas-discharge display panels.

These drivers reduce substantially the number of discrete components required with panels (Beckman, Burroughs, Dale, Matsushita, NEC, Pantek, etc) in calculator, clock and instrumentation applications.

The UDN-7183A, UDN-7184A, and UDN-7186A drivers contain appropriate level shifting, signal amplification, current limiting, and output OFF-state voltage bias. The UDN-7180A driver requires external current limiting and is intended for higher-current applications or where individual outputs are operated at different current levels (i.e. with alpha-numeric displays). All inputs have pull-down resistors for direct connection to open-drain PMOS logic.

These devices provide output currents suitable for display segments in a wide variety of display sizes and number of display digits. Either a fixed split supply operation or a feedback-controlled scheme is allowed.

Applications

The Series UDN-7180A drivers can be used in a wide variety of low-level to high-voltage applications utilizing gas discharge displays such as those found in calculators, clocks, point-of-sale terminals, and instruments. Their high reliability combined with minimum size, ease of installation, and the cost advantages of a complete monolithic interface make them the ideal choice in many applications. A typical application showing the use of these devices, and their counterpart anode drivers, is shown.

ABSOLUTE MAXIMUM RATINGS at +25°C

Supply Voltage, V_{KK} ..... −115 V
Input Voltage, V_{IN} ..... +20 V
Output Current, I_{OUT}: UDN-7180A ..... 20 mA
UDN-7183A ..... 3.25 mA
UDN-7184A ..... 2.0 mA
UDN-7186A ..... 1.0 mA
Power Dissipation, P_D ..... 1.13 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at the rate of 9.1 mW/°C above 25°C

Due to the high input impedance of these devices, they are susceptible to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{KK} = 110 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	UDN-7180/83A Typ.	UDN-7180/83A Max.	UDN-7184A Min.	UDN-7184A Typ.	UDN-7184A Max.	UDN-7186A Min.	UDN-7186A Typ.	UDN-7186A Max.	Units
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 2.4 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 2.4 V, V_{KK} = −70 V	1	—	−66	—	—	−65	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 2.4 V, I_{ON} = 14 mA		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 2.4 V, V_{KK} = −110 V, Test output held at −60 V	3A	* UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, V_{KK} = −110 V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	4	—	100	200	—	100	200	—	100	200	μA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	−125	−175	—	−125	−175	—	−125	−175	μA

NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.
4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

TEST CIRCUITS

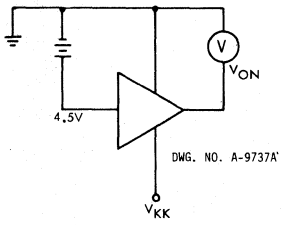


FIGURE 1

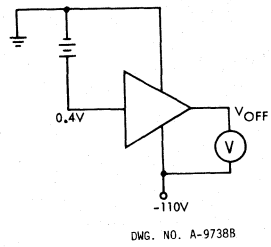


FIGURE 2

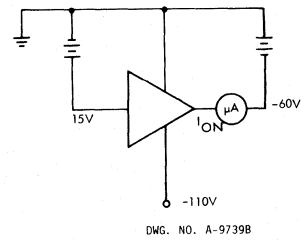


FIGURE 3A

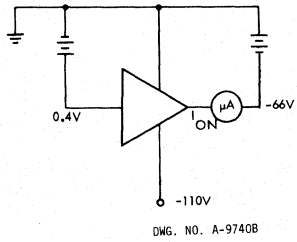


FIGURE 3B

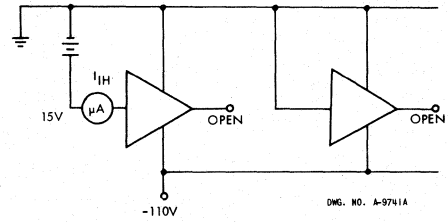


FIGURE 4

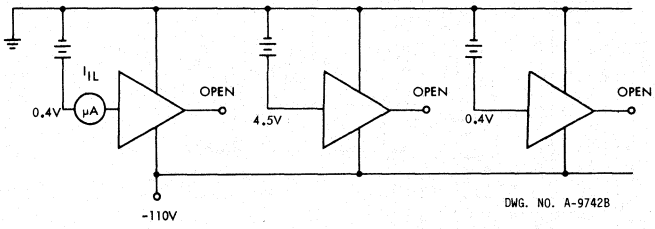


FIGURE 5

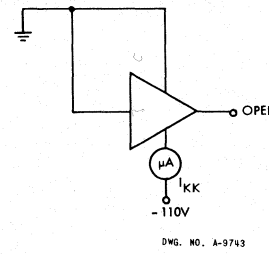
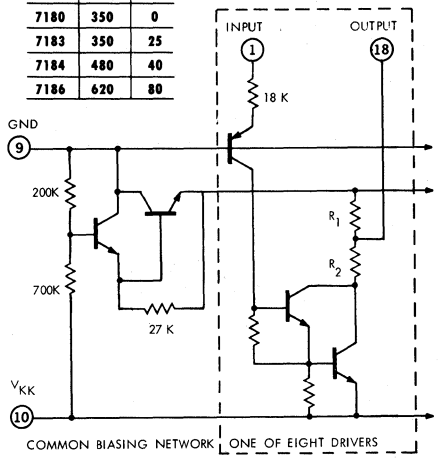


FIGURE 6

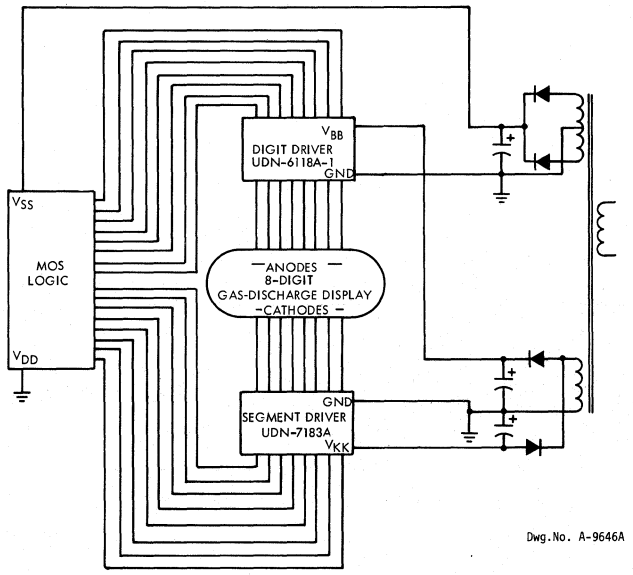
PARTIAL SCHEMATIC

	R_1 (kΩ)	R_2 (kΩ)
7180	350	0
7183	350	25
7184	480	40
7186	620	80



Dwg.No. A-9644C

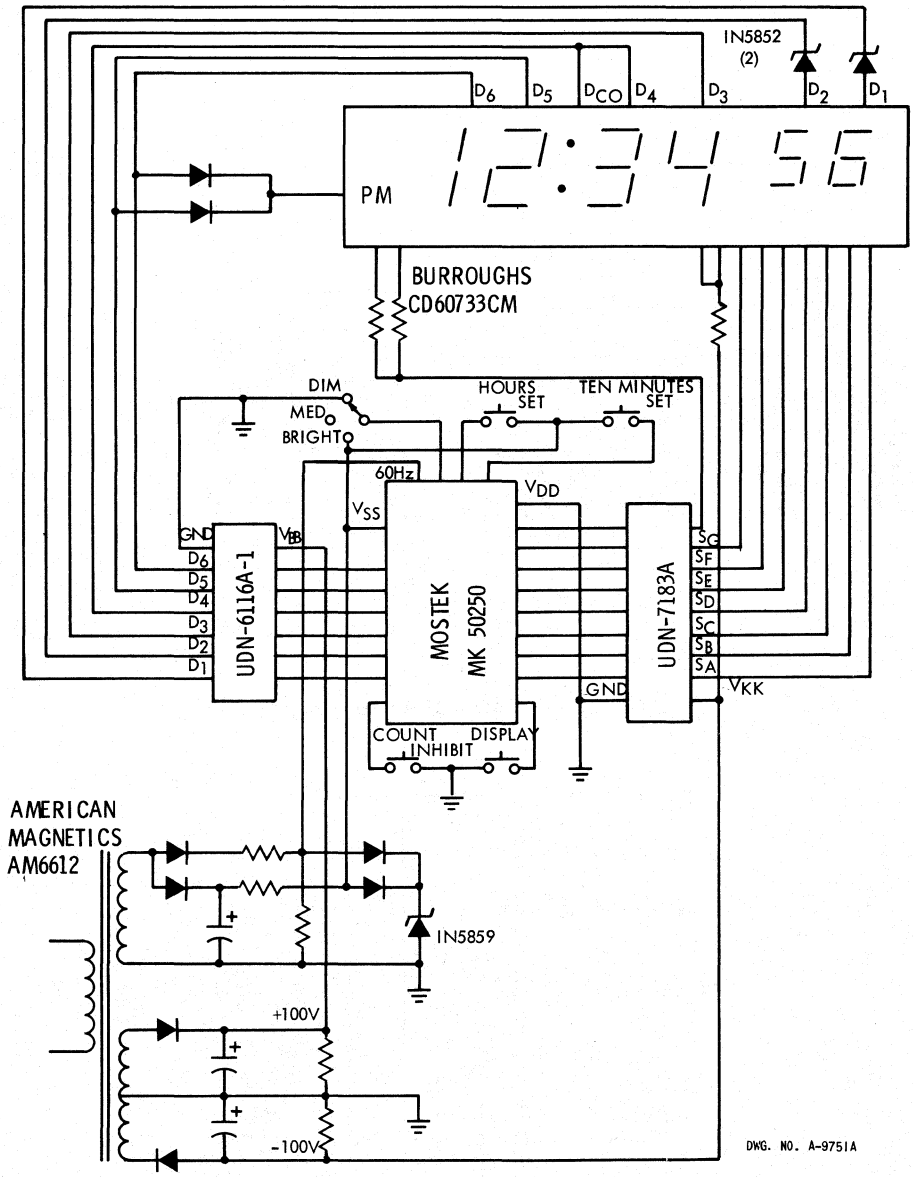
TYPICAL APPLICATION

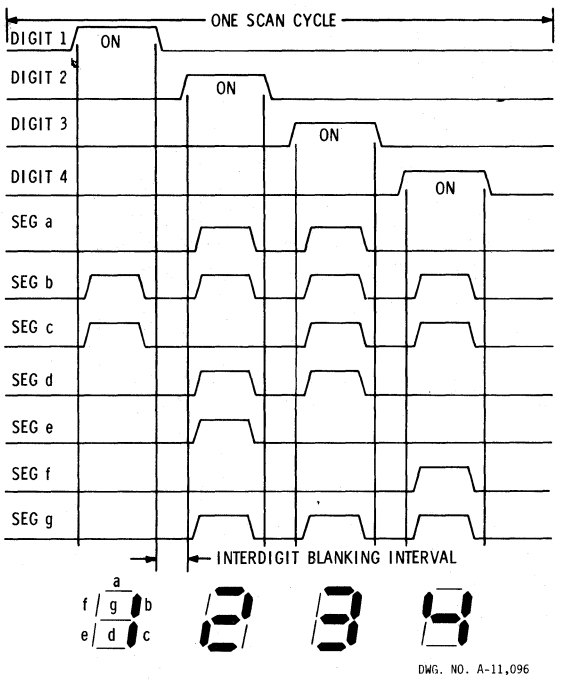


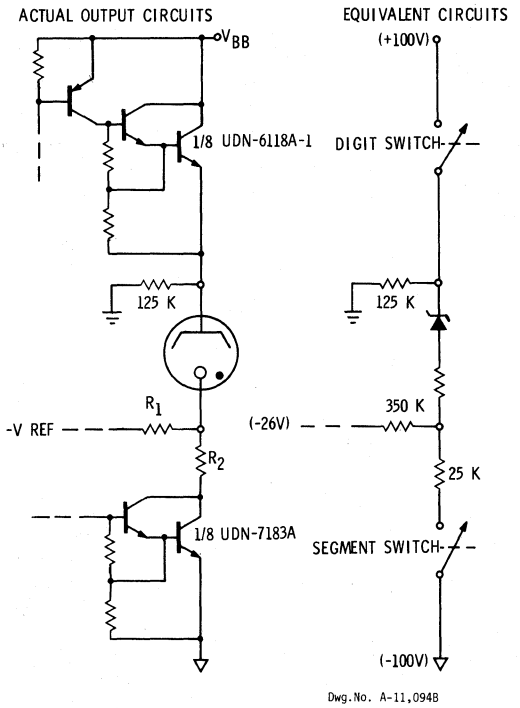
Dwg.No. A-9646A

2

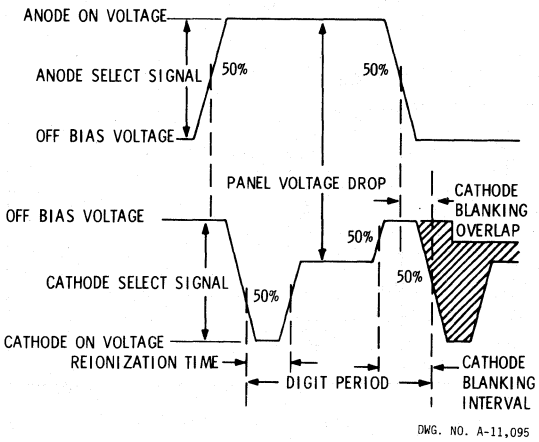
TYPICAL SIX-DIGIT CLOCK







ANODE AND CATHODE WAVEFORMS



A MONOLITHIC IC SERIES FOR GAS-DISCHARGE DISPLAY INTERFACE

Introduction

The switching of the high voltages necessary for display panels such as the Burroughs Panaplex® has long presented difficulties to the semiconductor industry – particularly to IC manufacturers. It is difficult to fabricate devices capable of sustaining 200 volts or greater with standard IC processes of today. Solutions to the high voltage gas discharge display interface also must be inexpensive as well as functional; this cost/simplicity factor prohibits most unusual or exotic circuit designs and/or IC processes.

The earliest (and a great many recent) gas discharge interface schemes used discrete components, but that has been an increasingly cumbersome and expensive solution. Competition at the system level has largely come from LEDs, and a great many standard ICs are available for the smaller LEDs. In most instances, the small displays have gone to LEDs. However, the larger display applications are still an opportunity for gas discharge since character size and cost are not directly related. The cost impact upon the potential for gas discharge displays in many systems is a function of interface complexity and cost, and it was to this end that a joint Sprague/Burroughs effort was launched.

Early Sprague/Burroughs meetings were held to define the relevant factors involved in such a program and provide the necessary insight for both parties into the capabilities of diode isolated ICs, the voltage and current requirements of the Panaplex displays, the need for minimization of power (battery systems), packaging of the circuits, component count and cost, etc. Add to this the potential for use with feedback controlled supplied, poorly regulated d-c supplies, the wide variety of numbers of display digits, the range of digit sizes (in use or contemplated), etc., and our task was not to be an easy one.

Our direction was determined by two factors: a history of fabricating 130-140 volt PN diode isolated display circuits, and a more recent effort to utilize compatible thin-film resistor technology. These factors, coupled with considerable expertise in designing and processing high voltage ICs, dictated an approach utilizing a split (± 100 V) supply. The split supply would provide the 200 volts needed to ionize the display and the resistor capability would greatly aid the incorporation of functions previously done by discrete components – including both input and output (segment) current limiting, pulldown (open drain PMOS), pullup and pulldown reference for IC outputs, and a high impedance voltage divider for the output OFF bias. All level shifting is accomplished via use of PNP or NPN transistors, and the capacitors previously required were negated.

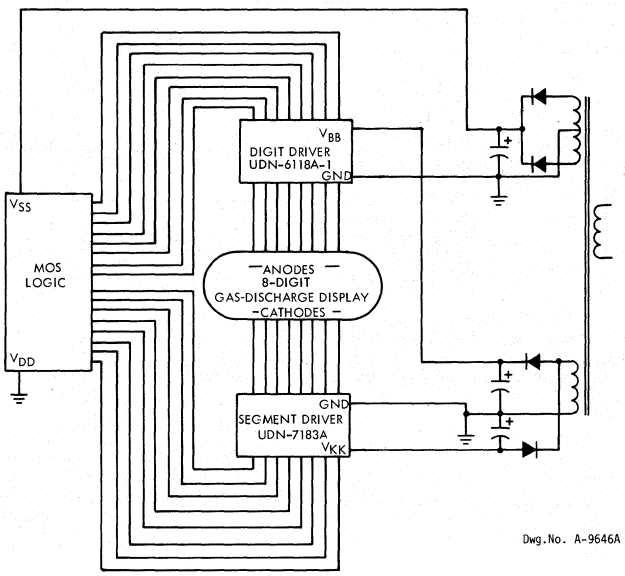


Figure 1

Basic Scheme

Replacing discrete components through incorporating their function into this IC series results in the block diagram of Figure 1 with its basic requirement for a single digit and single segment driver; a scheme capable of driving as many as eight digits and the eight segments. Additional digits or segments beyond the eight provided in an 18-lead DIP may be driven by combinations of packages beyond the minimum two necessary. Example: three ICs—two digit and one segment—will fulfill the needs of a 12 to 16 digit calculator.

Included in this series of high voltage interface are two digit driver packages: UDN-6116 (6-digit), and UDN-6118 (8-digit). Segment drivers include the UDN-7180, UDN-7183, UDN-7184, and UDN-7186, and the four offer current ranges compatible with display sizes from 0.250″ to 1″ panels, and others will be made available as needs are defined.

Digit Interface

The digit driver is the more complex of the two and its schematic is shown in Figure 2. Input address polarity is positive (active high in TTL parlance) and the circuit is designed to interface from TTL (4.5 volts from open collector—or using pull-up to V_{CC}), CMOS, PMOS, etc. Input current-limiting and one-half of the pull-down for open drain PMOS is the function of R_5; R_6 adds the second half of the pull-down to the ground bus. The protective value of R_4 and R_5 must be noted; a junction failure in Q_1 has the two resistors as a current limiter to the MOS (or TTL) output and will minimize the likelihood of destroying the low level logic outputs.

Input transistor Q_4 is a high voltage inverter and sinks the base current of PNP Q_3. A positive input (4.5 to 20 V) will turn on Q_4 and this base current (65 μA typ.) for PNO Q_3 will turn on the output Darlington (Q_1 and Q_2) and source digit current.

ELECTRICAL CHARACTERISTICS: $T_A = +25°C$, $V_{KK} = 110$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	UDN-7180/83A Typ.	UDN-7180/83A Max.	UDN-7184A Min.	UDN-7184A Typ.	UDN-7184A Max.	UDN-7186A Min.	UDN-7186A Typ.	UDN-7186A Max.	Units
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 2.4 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 2.4 V, $V_{KK} = -70$ V	1	—	−66	—	—	−65	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 2.4 V, $I_{ON} = 14$ mA		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 2.4 V, $V_{KK} = -110$ V, Test output held at −60 V	3A	UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, $V_{KK} = -110$ V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	4	—	100	200	—	100	200	—	100	200	μA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	−125	−175	—	−125	−175	—	−125	−175	μA

NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.
4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

PARTIAL SCHEMATIC

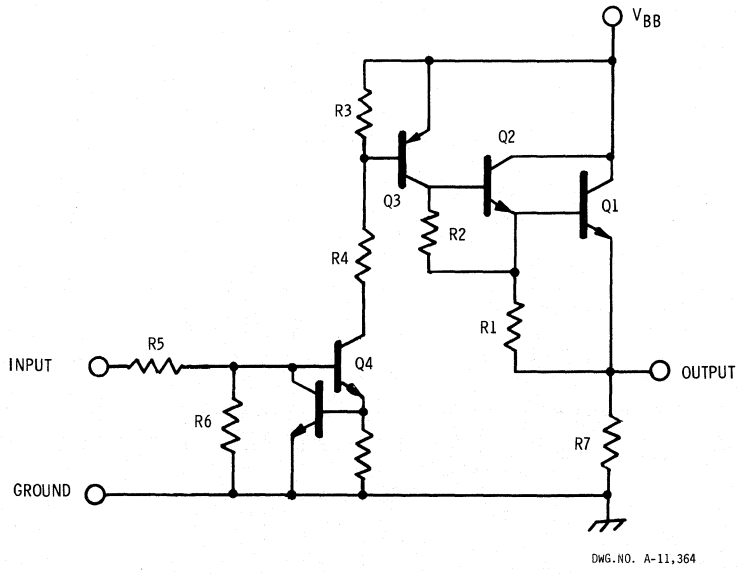


Figure 2

Consistent ionization and extinguishing of the display panel is the result of the 60-75 volt swings available from both digit and segment ICs. The conditions that previously created problems for the direct MOS drive with minimal swings at the output have been very adequately handled with the increased output swings of the 6100/7100 series. Problems from leading zero blanking, low temperature, low ambient light, etc. which previously gave difficulty are well taken care of with this series of ICs.

Segment Interface

The segment driver circuit is shown in Figure 3 and the value of R_2 (segment limiting) is determined via masking for the appropriate display current. Its counterpart pull-up resistor R_1 is also changed to some known ratio of R_2. The ground terminal (#9) is referenced near, or connected directly to ground, and the V_{KK} line is typically a -90 to -100 volts.

The input PNP (Q_1) serves as a level translator and provides d-c level shifting to the output Darlington (Q_2 and Q_3). Emitter resistor (R_3) both limits the input current and furnished pull-down for open drain PMOS. An added intent is the measure of protection furnished the MOS by the very high impedance of R_3.

The basic switching function is the combination of PNP Q_1, Darlington Q_2 and Q_3, and the associated resistors R_1, R_2, and R_3. Address polarity is again active high. The input may be raised a maximum of 20 volts above ground and will function with input levels obtained from CMOS and open collector TTL (4.5 V).

PARTIAL SCHEMATIC

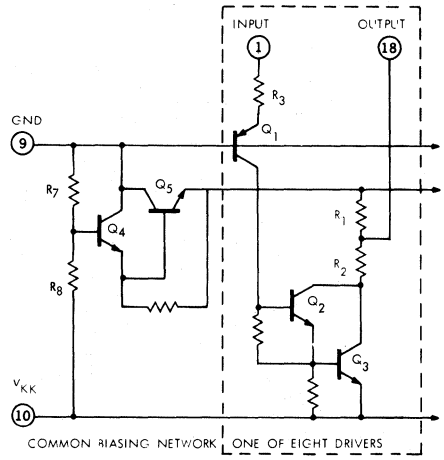


Figure 3

TYPICAL APPLICATION

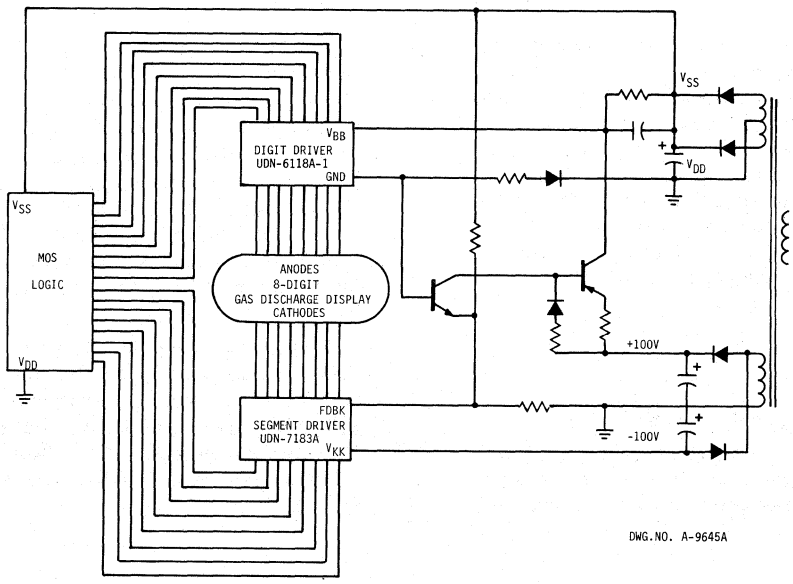


Figure 4

The OFF output biasing network is common to all the individual drivers with the level of bias determined by the ratio of R_7 to the total of R_7 and R_8. As in the digit driver, the value of output bias is $\approx \frac{2}{3}$ the voltage across V_{KK} and ground—thus insuring sufficient 'on to off' swings to properly fire, and effectively extinguish unaddressed segments during a scan. Emitter follower Q_4 and Q_5 sources current to the pull-up bus connected to the various outputs as they are turned on during the display scan.

Minimum Component Interface

The impact of this new product family may be seen in the typical digital clock of Figure 5. This a-c powered clock uses a Mostek 50250 clock IC, a UDN-6116A-1 digit driver, and a UDN-7183 segment driver. Total component count is approximately 30 pieces, and the board layout is straightforward and uses single-sided board.

Many calculator interface schemes use considerble numbers of components (70 to 100 typically) to drive gas discharge panels. As one example: a twelve digit/eight segment machine uses 85-90 discretes while the new IC version uses only three packages, and results in less space along with considerable simplification. Other applications will benefit similarly with this series of circuits.

Summary

Display technology and usage has emerged at a mind boggling rate in the past several years—largely due to the fantastic growth rate of calculators. The planar gas panels have been an integral portion of this burgeoning market, but like all the other displays

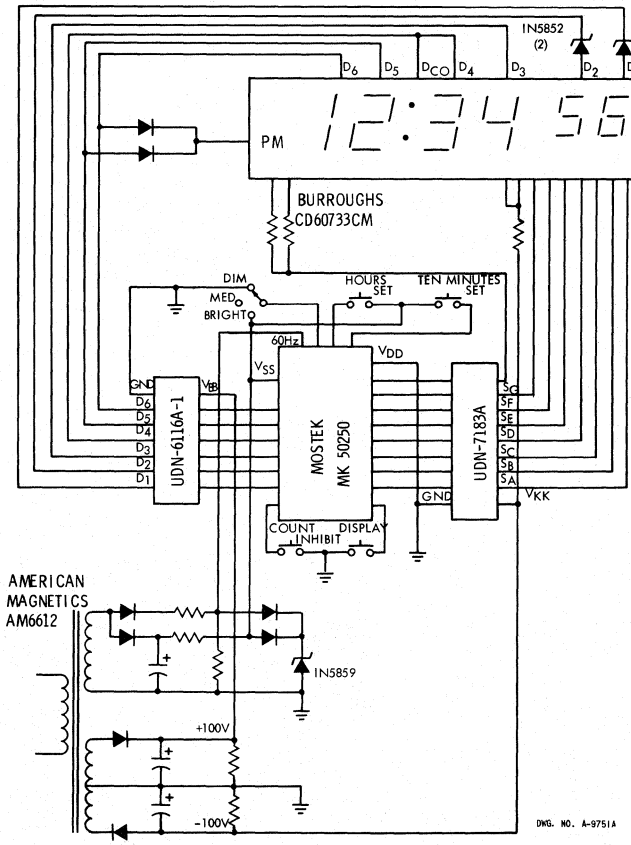


Figure 5

available does not meet the requirements for an ideal display.

Gas discharge panels are a fine combination of aesthetics, reliability, low cost, large character size, multiplexing capability, etc., but have been impacted to some degree by the lack of an available and inexpensive, totally monolithic interface. The move toward IC interface for displays has stifled some potential — largely in favor of LEDs; although many applications requiring large characters and/or in high ambient light turn toward gas panels. The planar gas discharge display is a long way from obscurity, and the availability of this family of ICs should open up new areas as well as satisfying existing systems.

The intent from the inception of this program has been to produce and provide a standard, inexpensive and easy to use interface for gas discharge displays. A great many potential applications exist for these circuits in consumer and commercial products. From the calculator and digital clock areas this product also will find use in automotive dashboards, point-of-sale systems, electronic cash registers and scales, and instrumentation. The market for displays is still very elastic, and many applications for gas discharge panels are continuing to appear. The Sprague contribution to this market is this series of state-of-the-art interface ICs.

TRENDS IN IC INTERFACE FOR ELECTRONIC DISPLAYS

Introduction

Display technology was truly set into high gear by the explosion of the electronic calculator business. Expansion at a phenomenal pace continues, encompassing a multitude of products, particularly high-volume consumer products (calculators, clocks, games, and watches). Recently, further stimulated by the "microprocessor revolution," with its far-reaching effects, and the resulting changeover to solid state design from electromechanical, mechanical, fluidic, or electrical systems, the vistas for displays have expanded well beyond the horizon. Products have been and are being developed, using microprocessors and displays, that never previously existed.

To augment this microprocessor revolution, semiconductor manufacturers are developing many new interface circuits useful with displays, although some of these will not be exclusively for display systems. To accomplish this, the present boundaries of device design, process, packaging, and electrical parameters will require continual extension and expansion.

Display Buffers

A continuing evolution of standard interface ICs is needed to buffer low-level logic from high-voltage and/or high-current loads. Some of this buffer development will serve display systems. Since there already is a broad assortment of buffers (particularly for low- to medium-current LED applications), the ongoing development in simple or low-order interface will mainly concentrate upon further reduction in discrete component count, package improvement (particularly for high-current/high-power devices), improvements in device current, voltage, switching speed, and greater reliability.

Figures 1, 2, and 3 show some Sprague interface ICs that represent buffer circuits; other vendors supply similar, or identical, high-current or high-voltage buffers to allow operation of displays from low-level logic. Two basic changes have occurred relatively recently:

1. Greater use of 18-pin DIPs for eight driver channels (Source Driver, Figure 2).
2. Creation of sourcing functions (Figures 2 and 3; useful for LED, gas-discharge, vacuum fluorescent, incandescent, and electromagnetic displays, depending upon device ratings). While further buffer designs are needed (particularly in high-current (> 2 A) and high-voltage (> 100 V) circuits), the main emphasis will be toward the incorporation of logic and control circuitry with output buffers.

Complex Interface

Paralleling (though lagging) the microprocessor LSI revolution is the area of greatest future for IC display circuits: The need for complex, smart or high-order interface. This will be MSI to LSI logic (with perhaps some linear functions) combined with suitable output buffers.

UDN-6116A-1 GAS-DISCHARGE DRIVER

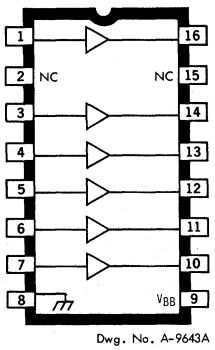


Figure 1A

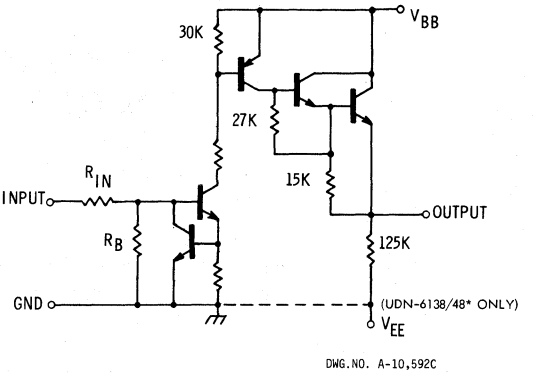


Figure 1B

SERIES UDN-2980 SOURCE DRIVER

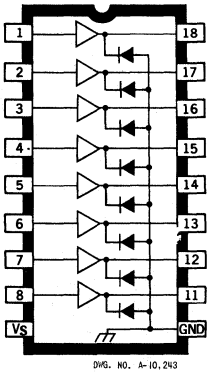


Figure 2A

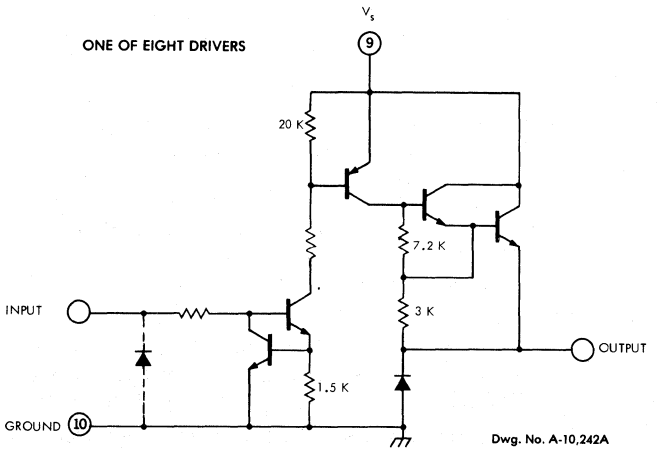


Figure 2B

Display interface ICs (similar to the MOS I/O control chips), both custom and standard product, are becoming available in this category. High-volume applications may justify custom ICs, but the more general trend will be toward standard, off-the-shelf designs — chiefly due to the high costs of developing custom ICs.

The higher voltage displays (gas-discharge, vacuum fluorescent, a-c plasma, and d-c electroluminescent) may share some circuits (if appropriately planned and designed), particularly in the area of matrix displays. It is difficult to imagine, however, much commonality between high-current LEDs, high-voltage gas-discharge or a-c plasma, and low-power LCDs,

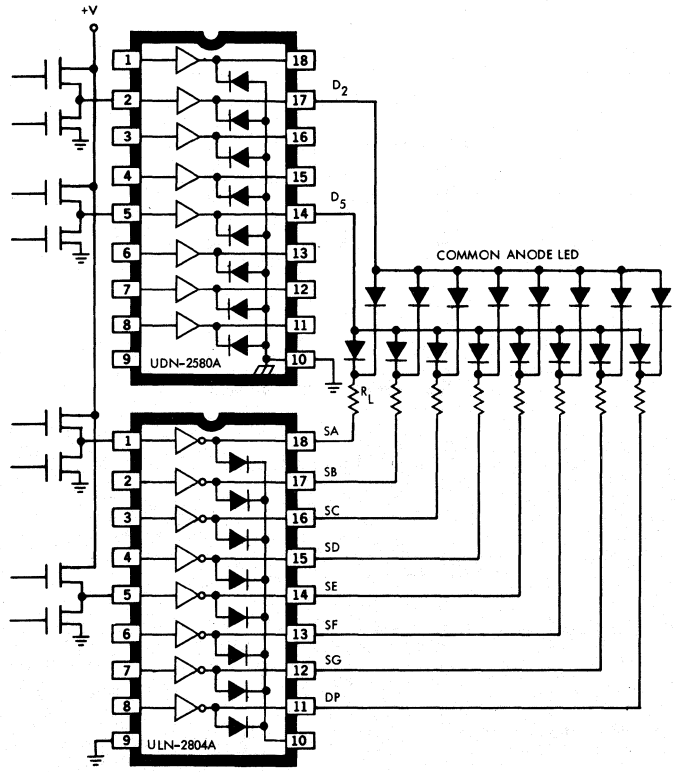


Figure 3
8-DIGIT/8-SEGMENT HIGH-CURRENT LED INTERFACE

although they should share considerably the development of cellular CAD circuit designs. Basic shift registers, latches and decoders do have considerable commonality.

In Figure 4 is a pinout and logic diagram of a BiMOS Sprague IC combining logic and output drive. Although not expressly intended for display applications, this BiMOS (CMOS logic and bipolar outputs) IC has a great deal of utility to engineers working with lower voltages and high currents (LEDs, incandescent and electromagnetic displays). Type UCN-5801A is a parallel-in/parallel-out unit composed of eight 'D' latches and eight 350 mA/50 V bipolar Darlington outputs.

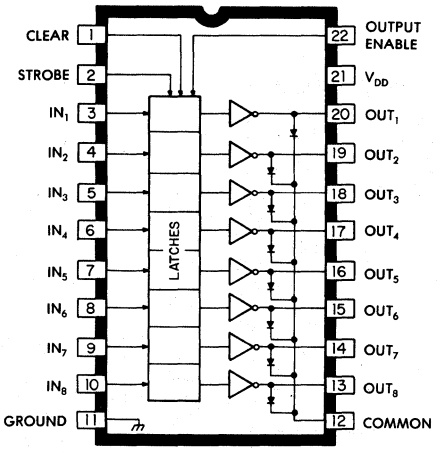


Figure 4A

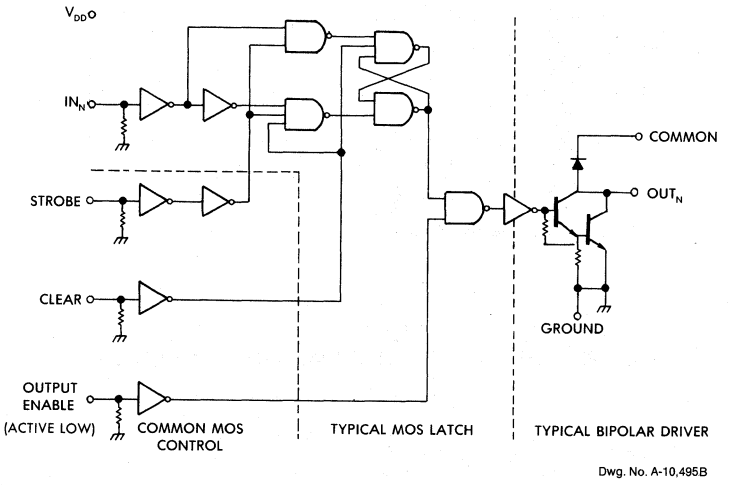


Figure 4B
UCN-5801A BIMOS LATCH/DRIVER

More recently, Sprague has designed a serial-in/parallel-out BiMOS interface IC expressly for use with vacuum fluorescent displays. Figure 5 shows the UCN-5810A 10-bit serial-in/parallel-out interface for use with VF displays; the use of serial data allows 10 output lines, data in and data out in a standard 18-lead DIP. It makes possible both fewer IC packages and simpler PC board wiring, although it is slower than a parallel data approach. It uses only a single pin of the I/O ports.

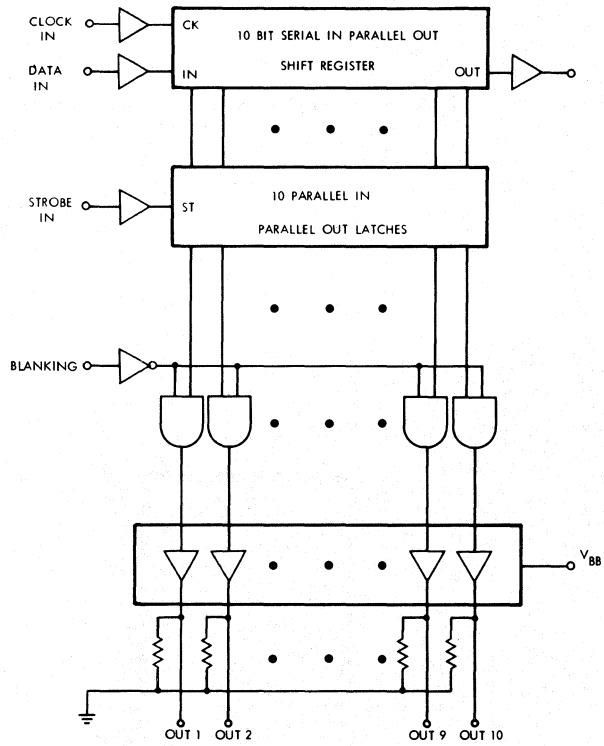


Figure 5B
UCN-5810A VF DRIVER BLOCK DIAGRAM

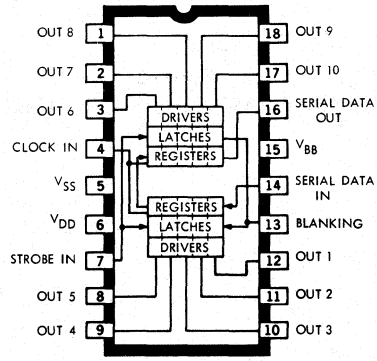


Figure 5A
UCN-5810A PINOUT

A slightly more recent design for vacuum fluorescent displays is the Sprague UCN-5815A. This is a 22-lead, 8-bit parallel-in/parallel-out BiMOS unit. The unit may have data inputs and a strobe bus (see Figure 6). The chip enable/blanking pin provides control of VF buffers. A power-on-clear is internally incorporated.

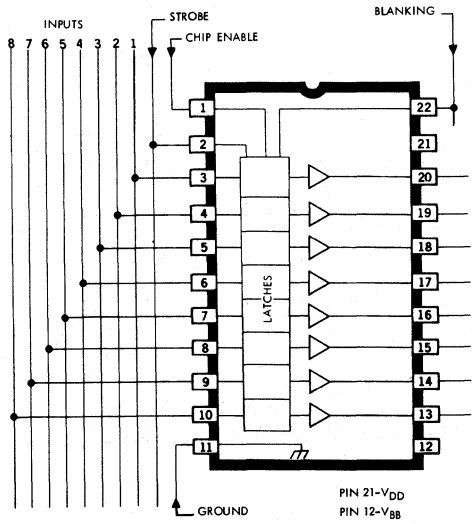


Figure 6
UCN-5815A PARALLEL 8-BIT VF INTERFACE

Device Technologies

With the exception of LCD displays (which at least until recently have been largely, if not entirely, driven by MOS) the display and interface technologies in high-volume use are mainly associated with bipolar semiconductors. Early display interface ICs (particularly devices such as the 7447 and 7448) were aimed at LED technology and represent MSI with modest output capability. The increasing use of higher voltage displays, multiplexed high-current applications, and the need for greater circuit complexity and low pin count will dictate other technologies, such as I^2L, BiMOS, CMOS/DMOS, and possibly DMOS.

Standard Bipolar

Standard bipolar technology, long associated with TTL or linears (early op amps), appears very limited in scope for the future. Circuit density and supply power requirements will dictate other processes for functions beyond the simple MSI level. The advantages of standard bipolar ICs appear to be in the areas of simple high-current, high-power or high-voltage interface. In particular, applications requiring the combination of high voltages ($\geq$ 100 V) or multiple high-current outputs ($\geq$ 2 A) will restrict the logic/control circuitry to a low level. Cost, chip size and package power dissipation will restrict this circuitry largely to versatile, simple buffers.

I^2L

Anticipated to increase significantly is the use of I^2L for systems of low to modest voltages (LEDs through VF). The present limits of I^2L appear to be limited to applications below the 50- to 60-volt level. I^2L, with its combination of circuit density, low power and reasonable switching speeds should make a fine match for LEDs or other low-voltage display applications. For higher voltages (>25 or 30 V), prospects the penalty of reduced circuit density may diminish its cost effectiveness. Some increase in standoff voltage may be afforded by the uses of cascaded output transistors or process improvements, thus reducing the need to sacrifice logic density. Without a standard I^2L logic family, the main market penetration would appear to be custom designs although there is a definite opportunity for standard interface for lower voltage applications, particularly LEDs and vacuum fluorescent.

BiMOS

BiMOS, a combination of CMOS and bipolar for interface ICs, seems to fit a technology niche of higher breakdown voltages than I^2L, especially where logic power and supply voltage range (5 to 15 V) is important. BiMOS or BiFET ICs, which are presently on the market, are largely related to operational amplifiers, although other uses, such as the Sprague application of BiMOS to interface, are emerging.

Currently, it is feasible to design and manufacture BiMOS interface with breakdown voltages in the 80 to 100 V range. With additional time and greater concentration on increasing BV, it appears that higher voltages ($\geq$ 150 V) for output buffers could be obtained. By obtaining breakdowns in the 120 V to 160 V range, BiMOS then becomes a viable IC technology for interface for the higher voltage displays: d-c gas-discharge with $\pm$ 100 to $\pm$ 130 V; a-c plasma with 160 to 170 V, and glow transfer or d-c electroluminescent (DCEL) opportunities with a range of 120-150 volts.

Switching speeds and output configurations (active pull-down or resistive) are critical to matrix displays (particularly a-c plasma) with large numbers of drive lines. Adding active pull-down or pull-up will tend to increase chip size (and cost), thus adding to the potential overall difficulty of BiMOS with its greater process complexity and slightly longer manufacturing cycle. This does appear to be a very key technology for the near future. Its product niche will include for applications requiring 60 to 100 V (or more) breakdowns, low-power logic, wide supply range, modest speeds, and MSI to small LSI.

CMOS/DMOS

Chiefly being carried on by Texas Instruments, CMOS/DMOS display interface appears to be intended for much of the same display market as BiMOS. Product information now available indicates 60 to 100 V breakdown (DMOS outputs), CMOS logic, low to modest output currents ($\leq$25 mA), and logic speeds to 4 MHz. Designs now being promoted are targeted toward a-c plasma and vacuum fluorescent panels.

Two apparent disadvantages now appear to exist:

1. Logic operates from 12 V $\pm$ 10% (may be done to provide maximum speed).
2. Output drive current is insufficient for high-current displays (without 100 mA, or more, the larger matrix panels will use discretes or another technology).

These shortcomings may be modified with time, although it is doubtful if 500 mA to 1 A DMOS outputs are practical.

Dielectric Isolation

Affording the highest breakdown voltage capability of present technologies is dielectric isolation. Since there is no collector-to-substrate PN junction, nor a collector-to-isolation wall PN junction, considerable improvement in collector-to-base and collector-to-emitter voltage is possible. Additionally, transistor sizes are considerably smaller than their PN-isolated counterparts. The dielectrically isolated devices offered by Dionics span a spectrum of approximately 100 volts to 280 volts (a-c plasma driver). DI affords the maximum breakdown voltage capability currently available.

Opposing this great advantage in breakdown voltage, however, is the increased process complexity of dielectrically isolated ICs. Definite improvements are needed in the area of process simplification, cost reduction, and alternate sources. Large-volume use of DI circuits will be restrained until these problems (particularly alternate sources) can be overcome. DI interface, with its potential for 300 V transistors, has a great promise if the barriers can be overcome.

Packaging

Semiconductor design and process have greatly outstripped packaging currently in use, particularly the area of power-handling capability. Greater concentration and resources are required to solve some of the following display interface related problems:

1. DIP power dissipation.
2. Greater number of leads (and smaller package sizes).
3. Improved plastic DIP resistance to moisture and corrosive environments.
4. Lower package manufacturing costs.
5. Smaller module or display subassemblies.

Power dissipation difficulties (strobed high currents) are most associated with LEDs. Use of very low duty-cycle and bright LEDs (particularly alphanumeric and matrix) dictates a need for multiplexing with peak currents as high as 3 A. Nothing currently on the market exceeds 1.75 A per output, and DIP ratings preclude d-c operation at such currents. However, many of the high-current applications are within the capability of standard bipolar ICs now offered.

For LSI ICs containing many I/O lines, the 24-, 28-, and 40-lead DIPs are standard. Since package size and cost increase together, it may be desirable to constrain many newer ICs to 18-, 20-, or 22-lead DIPs (with 0.300″ spacing, 22 also in use with 0.450″ width). Printed wiring board real estate is increasingly dictating smaller size. Solutions such as the quad in-line (Rockwell) or less than 0.100″ centers are possible. There are problems associated with a non-standard configuration (lack of sockets and higher prices) and the smaller physical size will not aid the quest for higher power (LEDs).

Improvements in plastic DIP moisture resistance and reliability are already underway; uses of tri-metal schemes (such as RCA's), silicon nitride or quartz passivation will continue to improve resistance to moisture and corrosive fumes. For display applications, these reliability improvements are of greatest concern in high-voltage devices.

Lower package costs are necessary to further increase the use of ICs in areas such as flat panel matrix displays. Currently, much of the cost of such a system is related to drive electronics, and much of the cost of the interface is the assembly cost of the DIPs (or hybrids). Increased use of automated assembly, film-carrier techniques and solder bumps will enhance the choice of ICs over discretes, and flat panel over CRT.

Also of concern is the possible mating of IC chips, solder-bump chips, or film-strip chips into the display assembly. Candidates for such a treatment would include d-c and a-c plasma, LEDs (already being done to a degree), DCEL, ACEL, LCD, and VF. Panel technologies using thick or thin-film techniques could benefit from such an approach. The biggest barrier to such an integrated assembly is the market data needed to justify tooling and lead time. It will only require one manufacturer willing to be a pioneer to further swing display technology into integrated systems. Prospects for purchasing a display complete with all drive electronics, such as a flat panel a-c plasma matrix (chips mounted via hybrid techniques on the rear of the glass envelope), are improving with time.

Summary

A bright future exists for IC interface in display systems; the combination of logic (from MSI to small LSI) with suitable output buffers will further assist display designs. The following IC Technology-Display Interface matrix lists the key characteristics and primary display applications of various semiconductor technologies. Since many of these characteristics are changing, the table lists the device characteristics either now available or for the near future.

The most dynamic technologies for the immediate future appear to be BiMOS, I^2L, CMOS/DMOS, and, perhaps soon, DMOS. Sprague, Dionics, RCA, Texas Instruments, National Semiconductor, and others are using these device technologies to carve market niches where suitable. The dynamics of the IC market make for an uncertain future for any supplier of display circuitry unable or unwilling to continue the technological advancement necessary to meet the changing demands of the display market.

IC TECHNOLOGY — DISPLAY INTERFACE

				LOGIC			
					Supply		Primary Display
Technology	Breakdown V	Output 1	Speed	Complexity (max)	Range	Power	Suitability
Linear Process Bipolar	10 to −170 V	<10 mA to 2 A	<1 MHz	MSI	5 V	High	LEDs, GD, VF, ACP, DCEL, EM
I^2L	20 to −60 V	<10 mA to 2 A	3-6 MHz	LSI	5 V	Low-Modest	LED, VF, EM
BiMOS	50 to −150 V	<10 MA to 500 mA	2-5 MHz	LSI	5 to 15 V	Low	LED, GD, VF, ACP, DCEL, EM
CMOS/DMOS	60 to −100 V	−25 mA	2-4 MHz	LSI	12 V	Low	GD, VF, ACP, LCD
DI	−200 to −300 V	<10 mA to 100 mA (est)	1 MHz (est)	MSI	5 V	High	GD, VF, ACP, DCEL

Code: GD = D-C Gas-Discharge & Glow Transfer
ACP = A-C Plasma
VF = Vacuum Fluorescent
DCEL = D-C Electroluminescent
EM = Electromagnetic

RELIABILITY OF SERIES UDN-6100A HIGH-VOLTAGE DISPLAY DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series UDN-6100A integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.
2) Accelerated testing is performed at temperatures above +125°C and is used to generate failure-rate data.
3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Table I contains Series UDN-6100A data produced by life tests that were conducted at +150°C. The data includes the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C. If these tests had been qualification tests, they would have ended at 200 hours at +150°C or 40 hours at +175°C.

The data at the bottom of Table I is compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% fail-point. The median life at a junction temperature of +150°C is 100,000 hours, in this case.

The log-normal distribution is commonly and widely used, because most semiconductor device data fits such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^o e^{-\varepsilon/kT}$$

where V_r^o = a constant
ε = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5700M, and Series UDN-2980A devices at multiple temperatures. Failure analysis of devices rejected during the testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

TABLE I
TEST RESULTS AT T_j = +150°C

TEST NUMBER	BIAS VOLTS	QTY.	HOURS ON TEST: 90	150	300	600	1200	1800	2000	5000	6000
			NUMBER OF FAILURES								
1	80	24	0	0	2	—	—	—	—	—	—
2	80	24	0	0	0	0	0	0	1	0	—
3	80	12	0	0	0	0	0	—	—	—	—
4	80	12	0	0	0	0	2	1	1	0	0
5	110	24	0	0	0	0	0	0	1	—	—
6	80	12	0	0	0	—	—	—	—	—	—
TOTAL ON TEST			108	108	108	72	72	58	57	31	8
TOTAL FAILURES			0	0	2	0	2	1	3	0	0
TOTAL GOOD			108	108	106	72	70	57	54	31	8
P_s			1.00	1.00	0.981	1.00	0.972	0.983	0.947	1.00	1.00
Cumulative P_s			1.00	1.00	0.981	0.981	0.954	0.938	0.888	0.888	0.888
$P_f = 1 - P_s$			0	0	0.019	0.019	0.046	0.062	0.112	0.112	0.112
% Failures			0	0	1.9	1.9	4.6	6.2	11.2	11.2	11.2

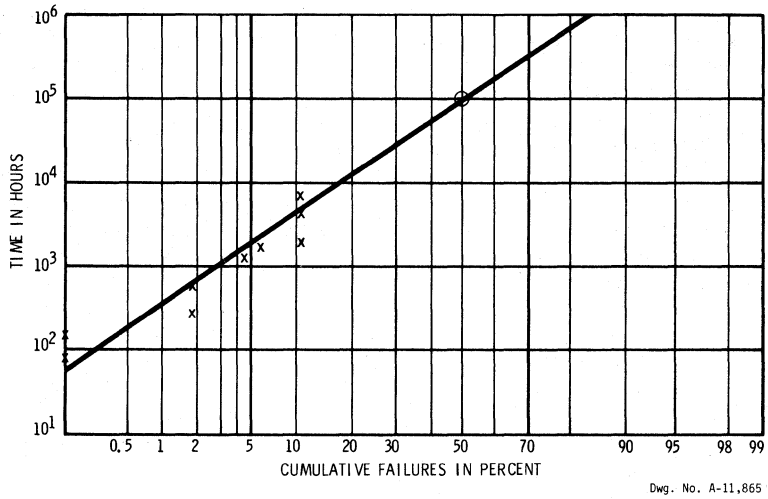


Figure 1
CUMULATIVE PERCENT OF FAILURES

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of $\varepsilon = 1.0$ eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life with lower junction temperatures may now be determined using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\Theta_{JA} + T_A$$

or

$$T_J = P_D\Theta_{JC} + T_C$$

The median lifetime, or 50% fail-point, as determined in Figure 2, is approximately 100 years at +125°C or 1,000 years at +90°C junction temperature.

The approximate failure rate ($\overline{FR}$) may be determined from $\overline{FR} = 1/\text{Median Life}$, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$\overline{FR} = 1/(4 \times 10^6 \text{ hours})$$
$$= 0.025\%/1000 \text{ hours}$$

Other failure rate values have been calculated in Table II.

TABLE II
SERIES UDN-6100A FAILURE RATES

T_J (°C)	Median Life (h)	Failure Rate (%/1000 h)
125	6×10^5	0.167
100	4×10^6	0.025
75	4×10^7	0.0025
50	5×10^8	0.0002

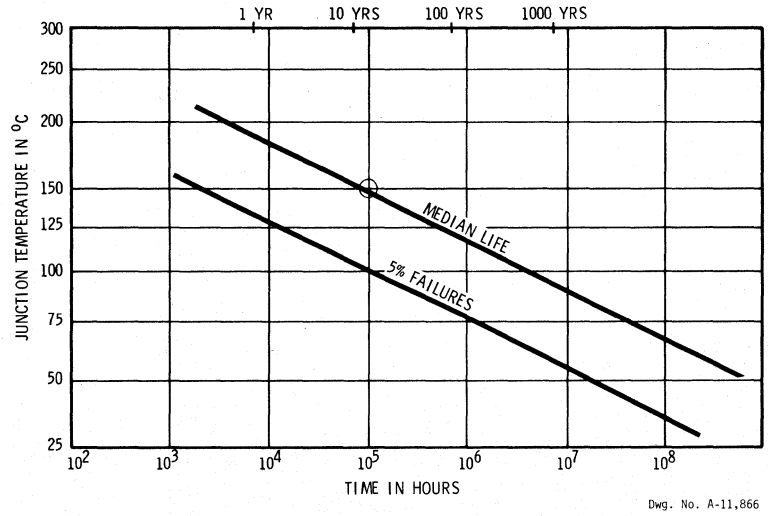


Figure 2
MEDIAN LIFE

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calculated from internal power dissipation and external ambient temperature, reaches the 5% fail-point in 10 years. Lowering the junction temperature to +70°C increases the time to 100 years.

A complete sequence of environmental tests on Series UDN-6100A, including temperature cycle, pressure cooker, and biased humidity tests are also continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K.E., and Bird, D.W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580–587 (Sprague Technical Paper TP 80-2).

2) Peck, D.S., and Trapp, O.D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6–7.

4) Goldwaite, L.R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208–213.

SECTION 3—MEDIUM-CURRENT (<1 A) INTERFACE DRIVERS

SELECTION GUIDE

(in order of tested output current rating)

I_{OUT}	V_{OUT}	Outputs	Device Type	Page
100 mA	30 V	Sink 32†	UCN-5833A/EP	5-74
100 mA	40 V	Sink 32†	UCN-5832A	5-65
100 mA	40 V	Sink 32†	UCN-5832EP	5-71
100 mA	225 V	Sink 32	UCN-5851/52A/EP	5-87
−120 mA	±25 V	Source 8	UDN-2585A	3-33
−120 mA	30 V	Source 8	UDN-2985/86A	3-69
−120 mA	50 V	Source 8†	UCN-5895A	5-118
150 mA	50 V	Sink 8†	UCN-4807A	5-17
200 mA	200 V	Sink 8	UDN-6540B	2-10
250 mA	40 V	Sink 4	Series UHP-400	3-3
250 mA	70 V	Sink 4	Series UHP-400-1	3-3
250 mA	100 V	Sink 4	Series UHP-500	3-3
250 mA	150 V	Sink 7	Series ULN-7000A	2-13
300 mA	70 V	Sink 4	UDN-2522A	3-25
300 mA	80 V	Sink 2	Series UDN-3610M	3-82
300 mA	80 V	Sink 2	Series UDN-5710M	3-90
300 mA	80 V	Sink 4	Series UDN-5700A	3-86
300 mA	120 V	Sink 4	UDS-5791H	6-97
−350 mA	35 V	Source 8	UDN-2987A	3-71
350 mA	50 V	Sink 4†	UCN-5800A	5-23
350 mA	50 V	Sink 7	Series ULN-2000A	3-13
350 mA	50 V	Sink 7	Series ULN-2000L	3-23
350 mA	50 V	Sink 8	Series ULN-2800A	3-44
350 mA	50 V	Sink 8	UDN-2596/98A	3-42
350 mA	50 V	Sink 8†	UCN-5801A	5-23
350 mA	50 V	Sink 8†	UCN-5821A	5-55
350 mA	50 V	Sink 8†	UCN-5841A	5-82
−350 mA	−50 V	Source 8	UDN-2580/88A	3-33
−350 mA	50 V	Source 8	UDN-2981/82A	3-62
−350 mA	50 V	Source 8†	UCN-5891A/B	5-113
350 mA	60 V	Sink 16†	UCN-5816A	5-49
350 mA	70 V	Sink 2	Series UDN-5720M	3-94
−350 mA	−80 V	Source 5	UDN-2956/57A	3-58
350 mA	80 V	Sink 8†	UCN-5822A	5-55
350 mA	80 V	Sink 8†	UCN-5842A	5-82
−350 mA	80 V	Source 8†	UCN-5890A/B	5-113
−350 mA	−80 V	Source 8	UDN-2580/88A-1	3-33
−350 mA	80 V	Source 8	UDN-2983/84A	3-62
350 mA	95 V	Sink 7	Series ULN-2020A	3-13
350 mA	95 V	Sink 8	Series ULN-2820A	3-44
350 mA	100 V	Sink 8†	UCN-5823A	5-55
350 mA	100 V	Sink 8†	UCN-5843A	5-82
350 mA	150 V	Sink 4†	UCN-5900A	5-123
350 mA	150 V	Sink 8†	UCN-5901A	5-123
±500 mA	40 V	2 × Full-Bridge	UDN-2993B	3-77
500 mA	50 V	Sink 7	Series ULN-2010A	3-13
500 mA	50 V	Sink 8	Series ULN-2810A	3-44
500 mA	50 V	Sink 8†	UCN-4808A	5-17
500 mA	70 V	Sink 2	Series UDN-5750M	3-94
600 mA	70 V	Sink 2	Series UDN-5740M	3-94
700 mA	60 V	Sink 4	UDN-2543B	3-30
750 mA	50 V	Sink 8	UDN-2597/99A	3-42
±800 mA	30 V	3 × Half-Bridge	UDN-2933/34B	3-55

Current ratings shown are maximum tested condition; voltage ratings are maximum allowable. Ratings of 1 A or greater are listed in Section 4. Additional ratings are listed in Section 2 (<100 mA/>100 V) and Section 5 (BiMOS Smart Power).
†Latched Smart Power drivers.

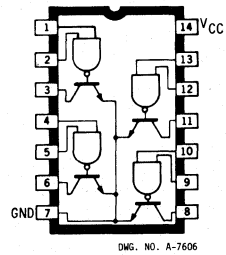
SERIES UHP-400, UHP-400-1, AND UHP-500 POWER AND RELAY DRIVERS

FEATURES

- Inputs Compatible with DTL/TTL
- 500 mA Output Current-Sink Capability
- Pinning Compatible with 54/74 Logic Series
- Transient-Protected Outputs on Relay Drivers
- High-Voltage Output:
  - 100 V Series UHP-500
  - 70 V Series UHP-400-1
  - 40 V Series UHP-400

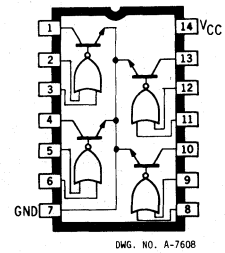
SERIES UHP-400, UHP-400-1, and UHP-500 power and relay drivers are bipolar integrated circuits with logic and high-current switching transistors on the same chip. Each output transistor is capable of sinking 500 mA in the ON state.

UHP Part Numbers			Function
400	400-1	500	Quad 2-Input AND
402	402-1	502	Quad 2-Input OR
403	403-1	503	Quad OR for Inductive Loads
406	406-1	506	Quad AND for Inductive Loads
407	407-1	507	Quad NAND for Inductive Loads
408	408-1	508	Quad 2-Input NAND
432	432-1	532	Quad 2-Input NOR
433	433-1	533	Quad NOR for Inductive Loads



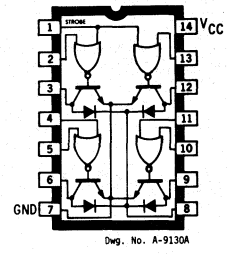
DWG. NO. A-7606

UHP-400
UHP-400-1
UHP-500



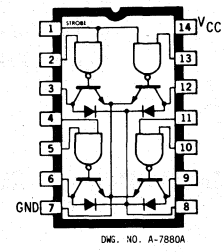
DWG. NO. A-7608

UHP-402
UHP-402-1
UHP-502



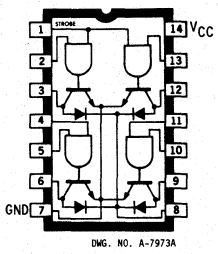
Dwg. No. A-9130A

UHP-403
UHP-403-1
UHP-503



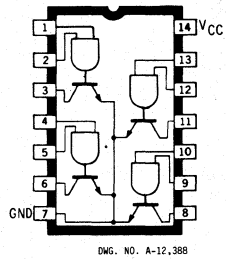
DWG. NO. A-7880A

UHP-406
UHP-406-1
UHP-506



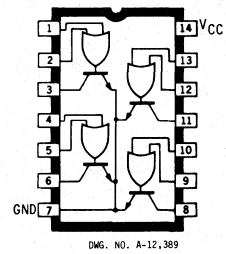
DWG. NO. A-7973A

UHP-407
UHP-407-1
UHP-507



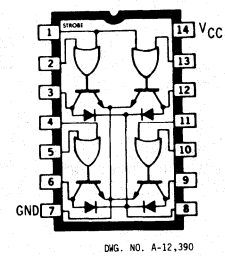
DWG. NO. A-12,388

UHP-408
UHP-408-1
UHP-508



DWG. NO. A-12,389

UHP-432
UHP-432-1
UHP-532



DWG. NO. A-12,390

UHP-433
UHP-433-1
UHP-533

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . 7 V
Input Voltage, V_{IN} . . . . . 5.5 V
Output Off-State Voltage, V_{OFF}
  Series UHP-400 . . . . . 40 V
  Series UHP-400-1 . . . . . 70 V
  Series UHP-500 . . . . . 100 V
Output On-State Sink Current, I_{ON} (one driver) . . . . . 500 mA
  (total package) . . . . . 1 A
Suppression Diode Off-State Voltage, V_R
  Series UHP-400 . . . . . 40 V
  Series UHP-400-1 . . . . . 70 V
  Series UHP-500 . . . . . 100 V
Suppression Diode On-State Current, I_F . . . . . 500 mA
Operating Free-Air Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into Any Output (ON State)	—	—	250	mA

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

Characteristic	Series	Test Conditions (Note 3)	Limits			
			Min.	Typ.	Max.	Units
Turn-On Delay Time (t_{pd0})	UHP-400	V_S = 40 V, R_L = 265Ω (6 W)	—	200	500	ns
	UHP-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	200	500	ns
	UHP-500	V_S = 100 V, R_L = 670Ω (15 W)	—	200	500	ns
Turn-Off Delay Time (t_{pd1})	UHP-400	V_S = 40 V, R_L = 265Ω (6 W)	—	300	750	ns
	UHP-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	300	750	ns
	UHP-500	V_S = 100 V, R_L = 670Ω (15 W)	—	300	750	ns

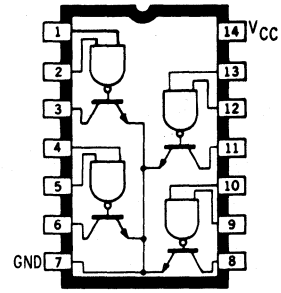
NOTES:
1. Each input tested separately.
2. Voltage values shown in the test-circuit waveforms are with respect to network ground terminal.
3. C_L = 15 pF. Capacitance value specified includes probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0 V	t_f = 7.0 ns	t_p = 1.0 μs
$V_{in(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

UHP-400, UHP-400-1, and UHP-500

Quad 2-Input AND Power Drivers

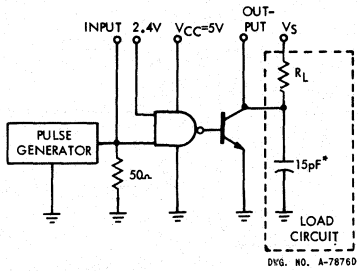


DWG. NO. A-7606

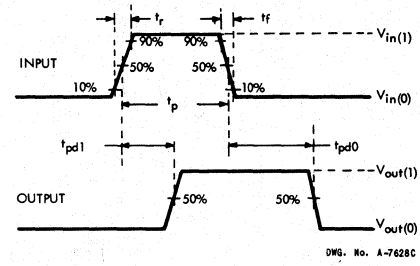
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-400	Min.	2.0 V	2.0 V	40 V	—	—	50	μA
		UHP-400-1	Min.	2.0 V	2.0 V	70 V	—	—	50	μA
		UHP-500	Min.	2.0 V	2.0 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	4.75 V	150 mA	—	—	0.5	V
			Min.	0.8 V	4.75 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.0	6.0	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	17.5	24.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at $V_{CC} = 5.0$ V.
2. Each gate.
3. Each input tested separately.
4. $T_A = +25°C$.



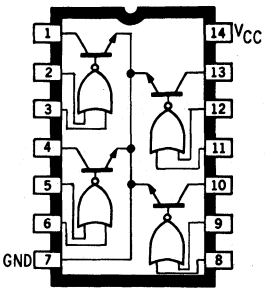
DWG. NO. A-7876D



DWG. No. A-7628C

*Includes probe and test fixture capacitance.

UHP-402, UHP-402-1, and UHP-502
Quad 2-Input OR Power Drivers

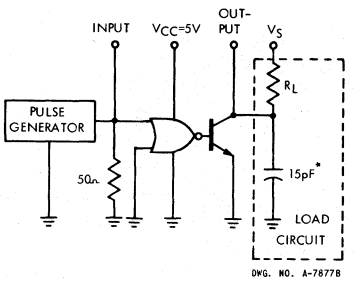


DWG. NO. A-7608

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

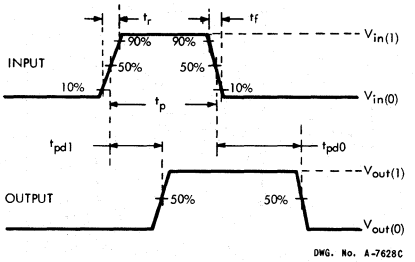
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-402	Min.	2.0 V	0 V	40 V	—	—	50	μA
		UHP-402-1	Min.	2.0 V	0 V	70 V	—	—	50	μA
		UHP-502	Min.	2.0 V	0 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	0.8 V	150 mA	—	—	0.5	V
			Min.	0.8 V	0.8 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.1	6.3	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	18	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at $V_{CC} = 5.0$ V.
2. Each gate.
3. Each input tested separately.
4. $T_A = +25°C$.



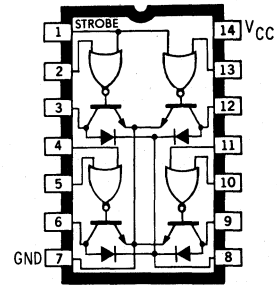
DWG. NO. A-7877B

*Includes probe and test fixture capacitance.



DWG. No. A-7628C

UHP-403, UHP-403-1, and UHP-503
Quad OR Relay Drivers

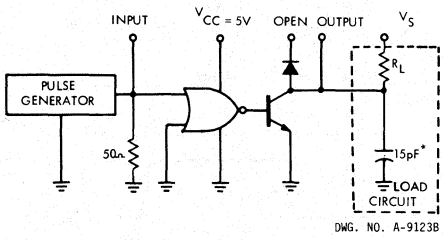


Dwg. No. A-9130A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

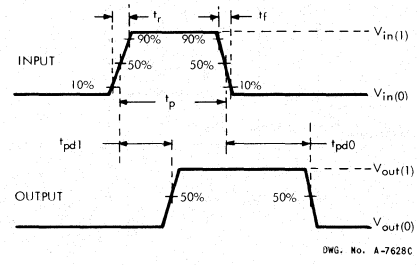
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-403	Min.	2.0 V	0 V	40 V	—	—	100	μA
		UHP-403-1	Min.	2.0 V	0 V	70 V	—	—	100	μA
		UHP-503	Min.	2.0 V	0 V	100 V	—	—	100	μA
Diode Leakage Current (Note 5)	I_R	All	Nom.	0 V	0 V	Open	—	—	200	μA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	5.0 V	5.0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	0.8 V	150 mA	—	—	0.5	V
			Min.	0.8 V	0.8 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.1	6.3	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	18	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Max.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



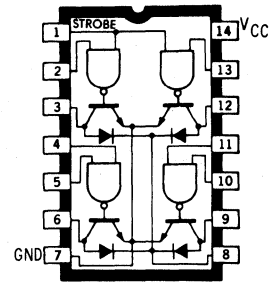
DWG. NO. A-9123B

*Includes probe and test fixture capacitance.



DWG. No. A-7628C

UHP-406, UHP-406-1, and UHP-506
Quad AND Relay Drivers

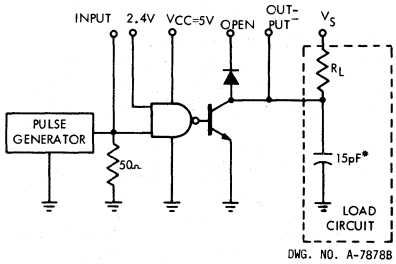


DWG. NO. A-7880A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

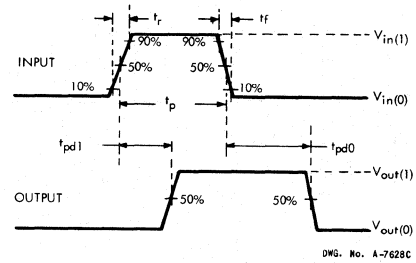
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-406	Min.	2.0 V	2.0 V	40 V	—	—	100	µA
		UHP-406-1	Min.	2.0 V	2.0 V	70 V	—	—	100	µA
		UHP-506	Min.	2.0 V	2.0 V	100 V	—	—	100	µA
Diode Leakage Current (Note 5)	I_R	All	Nom.	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	5.0 V	5.0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	4.75 V	150 mA	—	—	0.5	V
			Min.	0.8 V	4,75 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.0	6.0	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	17.5	24.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



DWG. NO. A-7878B

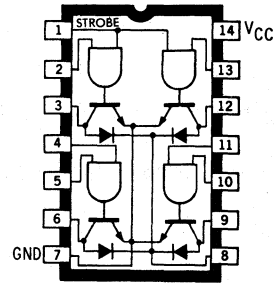
*Includes probe and test fixture capacitance.



DWG. No. A-7628C

UHP-407, UHP-407-1, and UHP-507

Quad NAND Relay Drivers

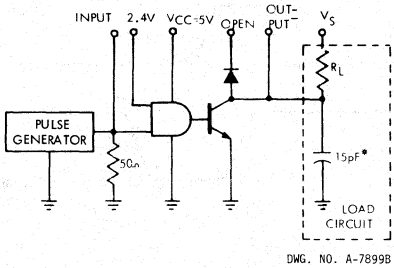


DWG. NO. A-7973A

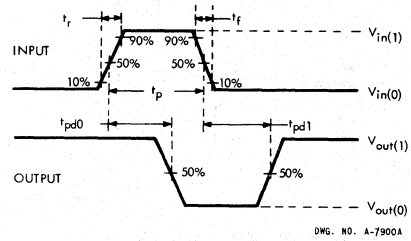
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-407	Min.	0.8 V	4.75 V	40 V	—	—	100	μA
		UHP-407-1	Min.	0.8 V	4.75 V	70 V	—	—	100	μA
		UHP-507	Min.	0.8 V	4.75 V	100 V	—	—	100	μA
Diode Leakage Current (Note 5)	I_R	All	Nom.	5.0 V	5.0 V	Open	—	—	200	μA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	0 V	0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	2.0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	2.0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	26.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



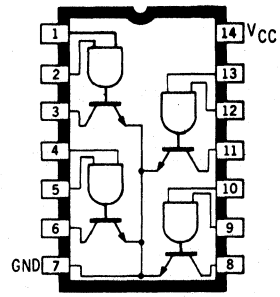
DWG. NO. A-7899B



DWG. NO. A-7900A

*Includes probe and test fixture capacitance.

UHP-408, UHP-408-1, and UHP-508
Quad 2-Input NAND Power Drivers

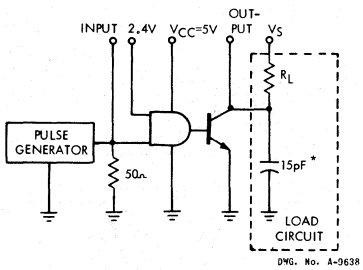


DWG. NO. A-12,388

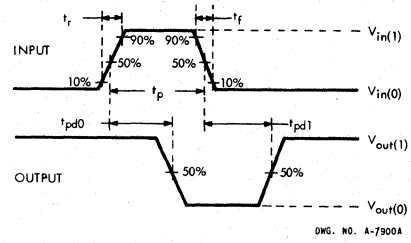
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-408	Min.	0.8 V	4.75 V	40 V	—	—	50	μA
		UHP-408-1	Min.	0.8 V	4.75 V	70 V	—	—	50	μA
		UHP-508	Min.	0.8 V	4.75 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	2.0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	2.0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	26.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.



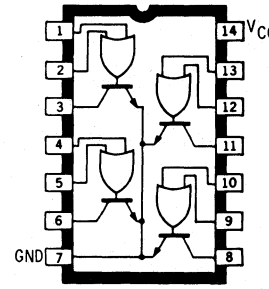
DWG. No. A-9638



DWG. NO. A-7900A

*Includes probe and test fixture capacitance.

UHP-432, UHP-432-1, and UHP-532
Quad 2-Input NOR Power Drivers

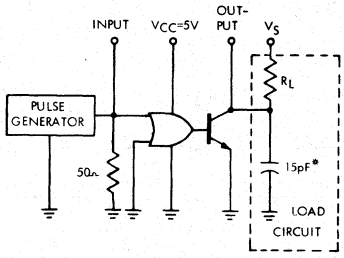


DWG. NO. A-12,389

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

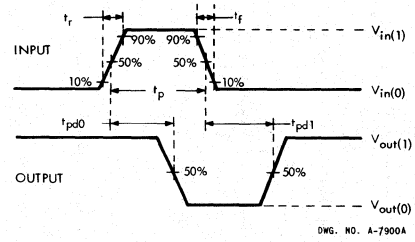
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-432	Min.	0.8 V	0.8 V	40 V	—	—	50	μA
		UHP-432-1	Min.	0.8 V	0.8 V	70 V	—	—	50	μA
		UHP-532	Min.	0.8 V	0.8 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at $V_{CC} = 5.0$ V.
2. Each gate.
3. Each input tested separately.
4. $T_A = +25°C$.



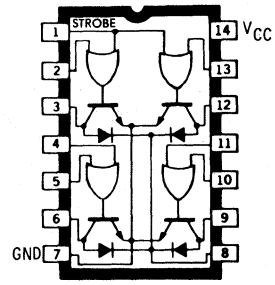
DWG. NO. A-7902B

*Includes probe and test fixture capacitance.



DWG. NO. A-7900A

UHP-433, UHP-433-1, and UHP-533
Quad NOR Relay Drivers

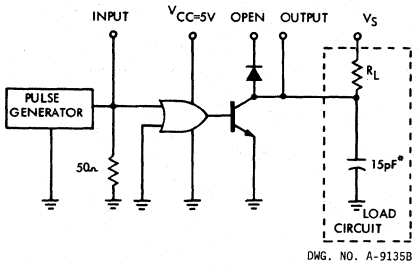


DWG. NO. A-12,390

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

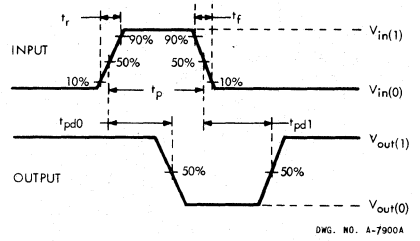
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-433	Min.	0.8 V	0.8 V	40 V	—	—	100	μA
		UHP-433-1	Min.	0.8 V	0.8 V	70 V	—	—	100	μA
		UHP-533	Min.	0.8 V	0.8 V	100 V	—	—	100	μA
Diode Leakage Current (Note 5)	I_R	All	Nom.	5.0 V	5.0 V	Open	—	—	200	μA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	0 V	0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at $V_{CC} = 5.0$ V.
2. Each gate.
3. Each input tested separately.
4. $T_A = +25°C$.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at $I_F = 200$ mA.



DWG. NO. A-9135B

*Includes probe and test fixture capacitance.



DWG. NO. A-7900A

SERIES ULN-2000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

THESE HIGH-VOLTAGE, HIGH-CURRENT Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

Peak inrush currents to 600 mA (Series ULN-2000A and ULN-2020A) or 750 mA (Series ULN-2010A) are permissible, making them ideal for driving tungsten filament lamps.

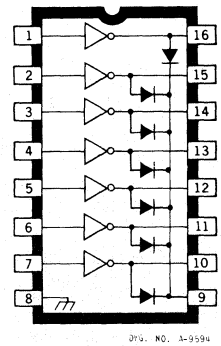
Series ULN-2001A devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.

Series ULN-2002A is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-2003A has a 2.7 kΩ series base resistor for each Darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

Series ULN-2004A has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-2003A, while the required input voltage is less than that required by Series ULN-2002A.

Series ULN-2005A is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic



DWG. NO. A-9594

output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

Series ULN-2000A is the original high-voltage, high-current Darlington array. The output transistors are capable of sinking 500 mA and will sustain at

Device Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic		Type Number	
General Purpose PMOS, CMOS	ULN-2001A	ULN-2011A	ULN-2021A
14-25 V PMOS	ULN-2002A	ULN-2012A	ULN-2022A
5 V TTL, CMOS	ULN-2003A	ULN-2013A	ULN-2023A
6-15 V CMOS, PMOS	ULN-2004A	ULN-2014A	ULN-2024A
High-Output TTL	ULN-2005A	ULN-2015A	ULN-2025A

least 50 V in the OFF state. Outputs may be paralleled for higher load-current capability. Series ULN-2010A devices are similar, except that they will sink 600 mA. Series ULN-2020A will sustain 95 V in the OFF state.

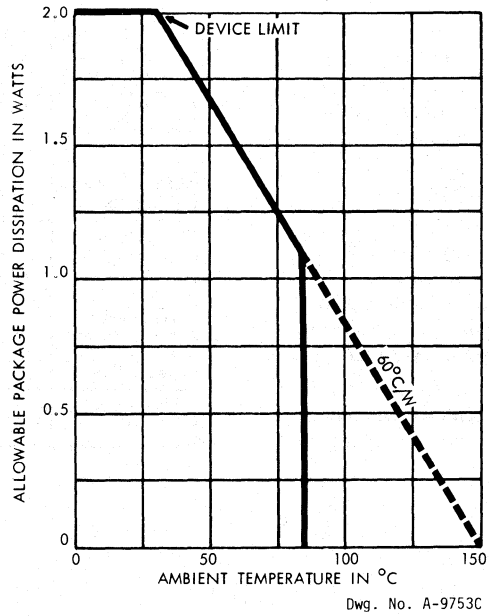
All Series ULN-2000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These can also be supplied in a hermetic dual in-line package for use in military and aerospace applications.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
for any one Darlington pair
(unless otherwise noted)

Output Voltage, V_{CE} (Series ULN-2000, 2010A)	50 V
(Series ULN-2020A)	95 V
Input Voltage, V_{IN} (Series ULN-2002, 2003, 2004A)	30 V
(Series ULN-2005A)	15 V
Continuous Collector Current, I_C (Series ULN-2000, 2020A)	500 mA
(Series ULN-2010A)	600 mA
Continuous Input Current, I_{IN}	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.0 W*
Operating Ambient Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 16.67 mW/°C above +25°C.
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)}$ = 1.6 V at +70°C with a pulse width of 20 ms and a duty cycle of 34%.

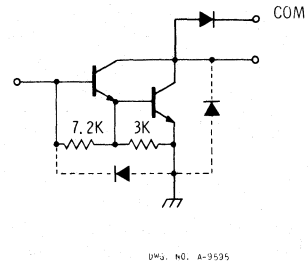
ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-9753C

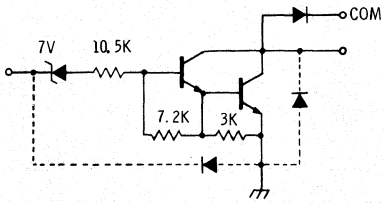
PARTIAL SCHEMATICS

Series ULN-2001A
(each driver)



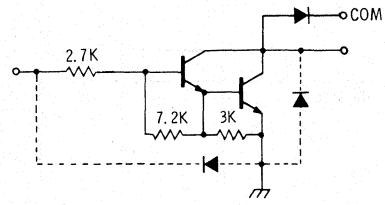
DWG. NO. A-9595

Series ULN-2002A
(each driver)



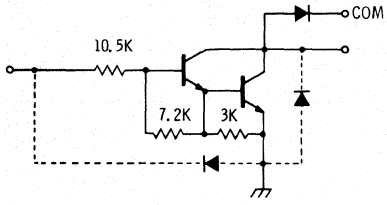
DWG. No. A-9650

Series ULN-2003A
(each driver)



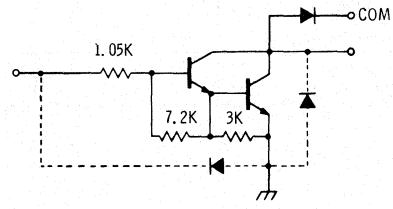
DWG. No. A-9651

Series ULN-2004A
(each driver)



DWG. NO. A-9898A

Series ULN-2005A
(each driver)



DWG. NO. A-10,228

SERIES ULN-2000A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2002A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2004A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2002A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2003A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2004A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2005A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2002A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2003A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2004A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2005A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2001A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

SERIES ULN-2010A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2012A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2014A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
				I_C = 500 mA, I_B = 600 μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2012A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2013A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2014A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2015A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2012A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	17	V
			ULN-2013A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	3.5	V
			ULN-2014A	V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	9.5	V
			ULN-2015A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2011A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
				V_{CE} = 2.0 V, I_C = 500 mA	900	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V
				I_F = 500 mA	—	2.1	2.5	V

SERIES ULN-2020A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 95 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2022A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2024A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2022A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2023A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2024A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2025A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2022A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2023A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2024A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2025A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2021A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	μA
				V_R = 95 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

TEST FIGURES

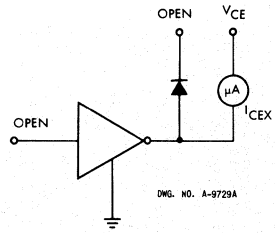


FIGURE 1A

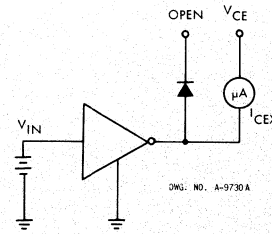


FIGURE 1B

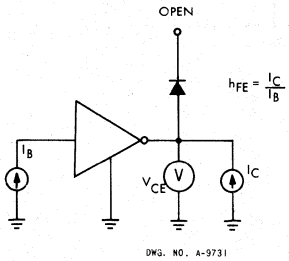


FIGURE 2

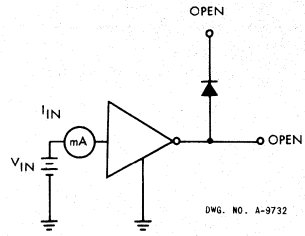


FIGURE 3

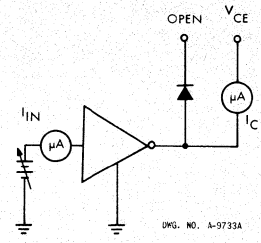


FIGURE 4

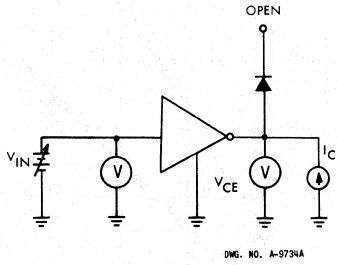


FIGURE 5

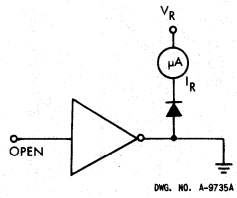


FIGURE 6

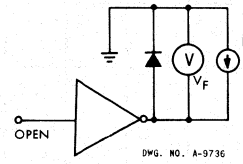
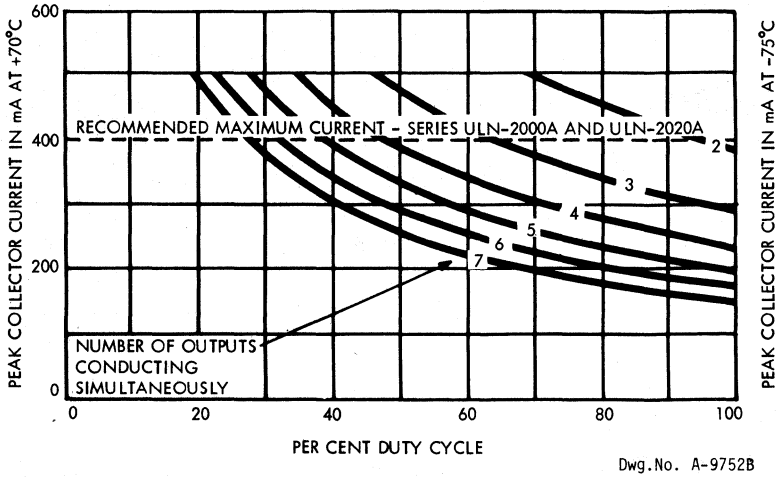


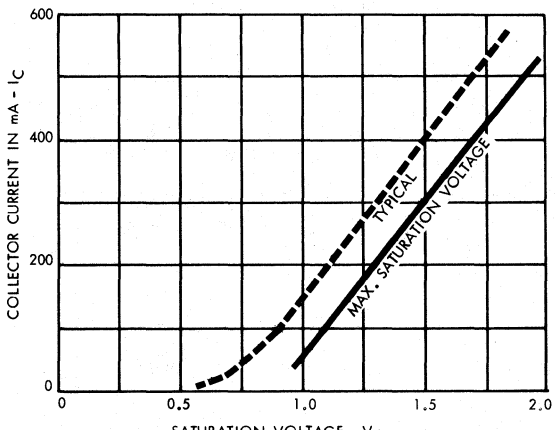
FIGURE 7

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



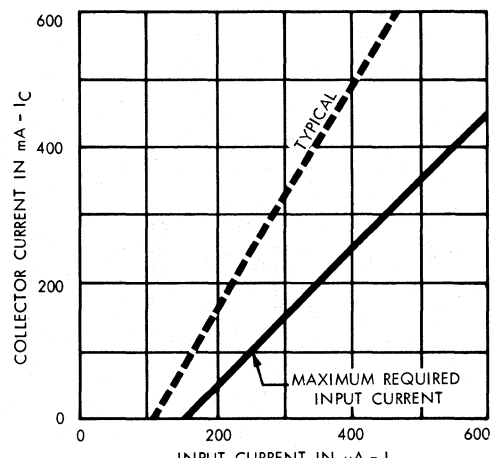
Dwg.No. A-9752B

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



DWG. NO. A-9754B

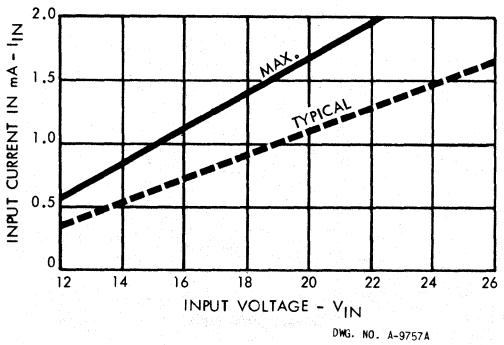
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



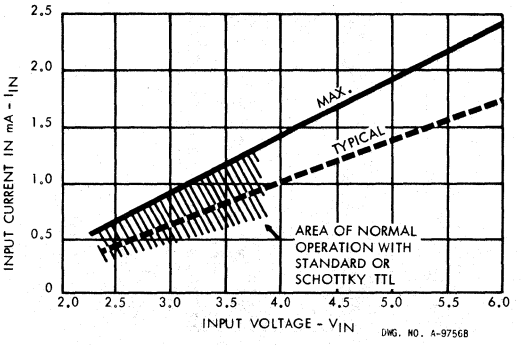
DWG. NO. A-10,872A

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

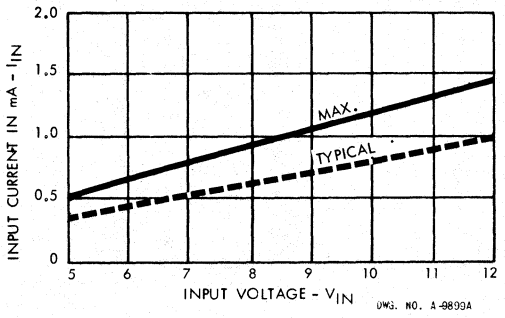
SERIES ULN-2002A



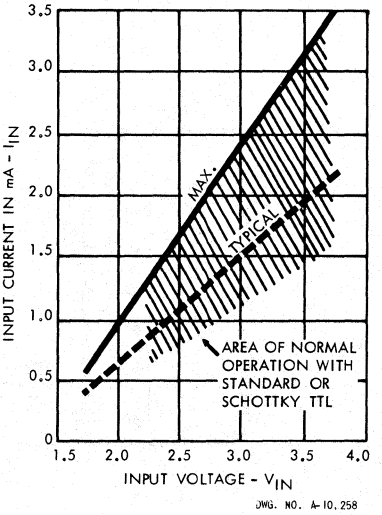
SERIES ULN-2003A



SERIES ULN-2004A

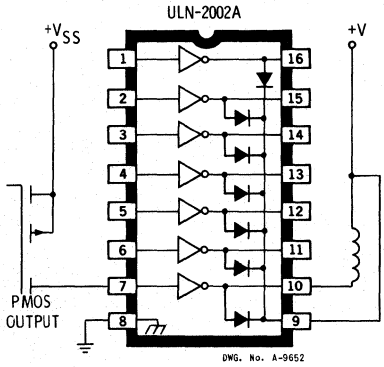


SERIES ULN-2005A

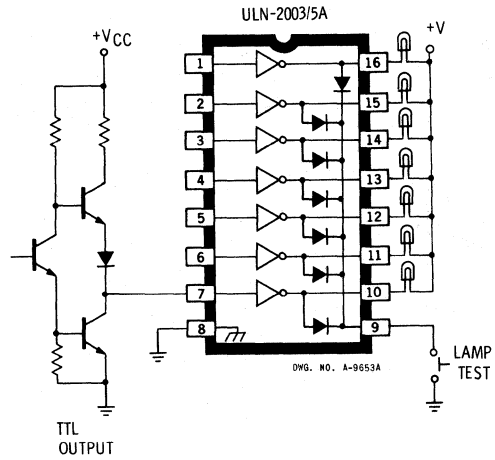


TYPICAL APPLICATIONS

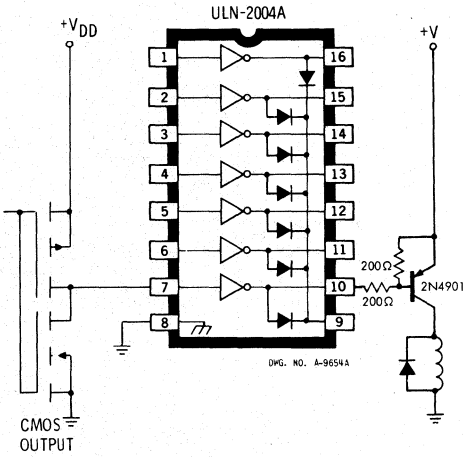
PMOS TO LOAD



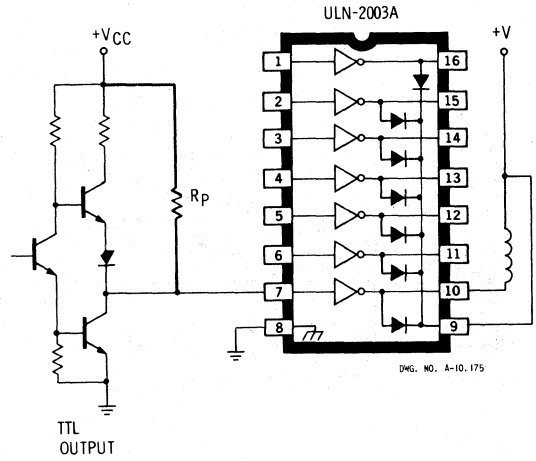
TTL TO LOAD



BUFFER FOR HIGH-CURRENT LOAD



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT



SERIES ULN-2000L
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

These high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

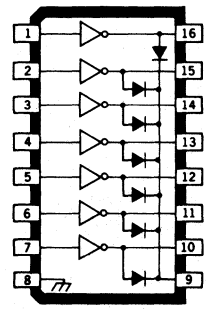
The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Outputs may be paralleled for higher load-current capability. All devices are packaged in the SOIC package.

Output pins are opposite input pins to facilitate printed wiring board layout. The ICs are priced to compete directly with discrete transistor alternatives.

The ULN-2001L is a general-purpose array that can be used with standard bipolar digital logic using external current limiting, or directly with most PMOS or CMOS.

The ULN-2002L is designed for use with 14 V to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

The ULN-2003L has a 2.7 kΩ series base resistor for each Darlingon pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs—particularly those beyond the capabilities of standard logic buffers.

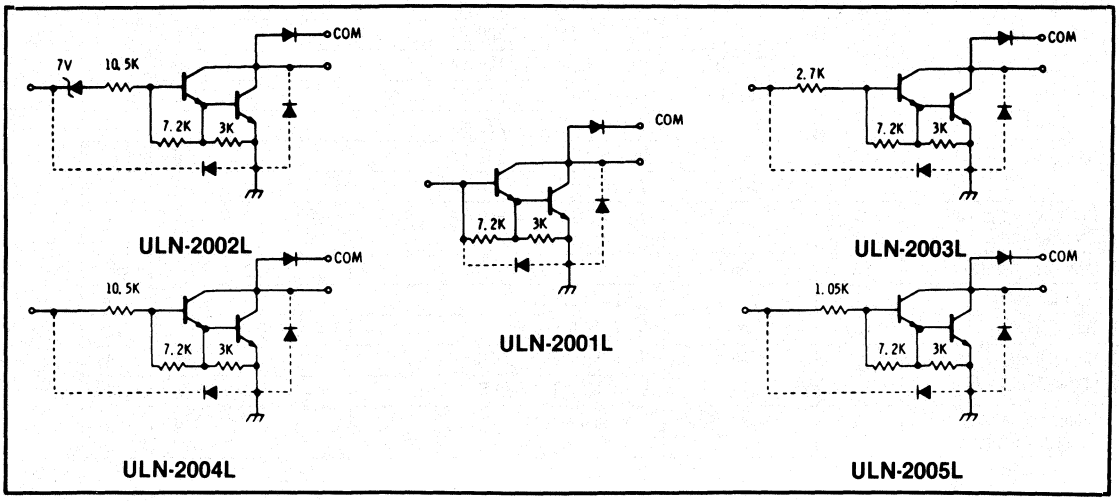


SOIC PACKAGE

The ULN-2004L has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-2003L, while the required input voltage is less than that required by Series ULN-2002L.

The ULN-2005L is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

PARTIAL SCHEMATICS



ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} . . . . . 50 V
Input Voltage,
V_{IN} (ULN-2002, 2003, 2004L) . . . . . 30 V
(ULN-2005L) . . . . . 15 V
Continuous Collector Current, I_C . . . . . 500 mA
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D (total package) . . . . . 0.96 W*
Operating Ambient Temperature Range, T_A . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Derate at rate of 7.7 mW/°C above = 25°C.

Device Number Designation

$V_{CE(MAX)}$ / $I_{C(MAX)}$	50 V / 500 mA
Logic	Type Number
General Purpose PMOS, CMOS	ULN-2001L
14-25 V PMOS	ULN-2002L
5 V TTL, CMOS	ULN-2003L
6-15 V CMOS, PMOS	ULN-2004L
High-Output TTL	ULN-2005L

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	µA
			V_{CE} = 50 V, T_A = 70°C	—	—	100	µA
		ULN-2002L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	µA
		ULN-2004L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
			I_C = 200 mA, I_B = 350µA	—	1.1	1.3	V
			I_C = 350 mA, I_B = 5 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	ULN-2002L	V_{IN} = 17 V	—	0.82	1.25	mA
		ULN-2003L	V_{IN} = 3.85 V	—	0.93	1.35	mA
		ULN-2004L	V_{IN} = 5.0 V	—	0.35	0.5	mA
			V_{IN} = 12 V	—	1.0	1.45	mA
		ULN-2005L	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	ULN-2002L	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
		ULN-2003L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
			V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
		ULN-2004L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
		ULN-2004L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
			V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
			V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
		ULN-2005L	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
DC Forward Current Transfer Ratio	h_{FE}	ULN-2001L	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	—
Input Capacitance	C_{IN}	All		—	15	25	pF
Turn-On Delay	t_{PLH}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	All	V_R = 50 V, T_A = 25°C	—	—	50	µA
			V_R = 50 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	—	1.7	2.0	V

UDN-2522A QUAD BUS TRANSCEIVER

—Data and Direct Inductive Load Control

FEATURES

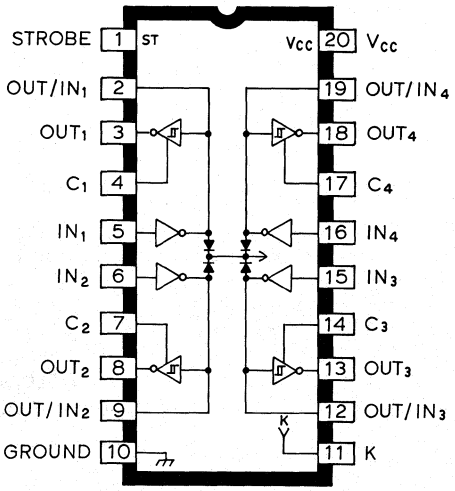
- Driver Output Current to 300 mA
- Driver Output Sustaining Voltage of 50 V
- Pulse-Width Discriminating Receivers
- Internal Receiver Hysteresis
- Compatible with TTL and MOS Logic
- Driver Output Clamp Diodes

Designed for bidirectional flow of data over unbalanced lines, the UDN-2522A quad bus transmitter/receivers feature a unique driver/receiver combination. A 300 mA output current, 50 V sustaining voltage rating, and internal clamp and blocking diodes allow these transmitter/receivers to directly control loads such as relays and solenoids, as well as the usual line receivers.

The driver stages include a common STROBE input pin for extended control flexibility. The STROBE turns off all four drivers but does not affect receiver operation. Because of the high driver output current, a large number of transmitter/receivers can be connected to a single data bus.

Each receiver's input is internally connected to its companion driver output. The receivers include a pulse-width discriminator and hysteresis for pulse reconstruction and improved noise immunity. The minimum detectable pulse width is determined by the user's choice of capacitor on the "C" pin for each of the four channels.

The UDN-2522A is rated for operation over the temperature range of −20°C to +85°C. It is packaged in a 20-pin dual in-line plastic package with copper leadframe for enhanced power dissipation. The drivers are capable of simultaneously sinking maximum rated current over the full operating temperature range.



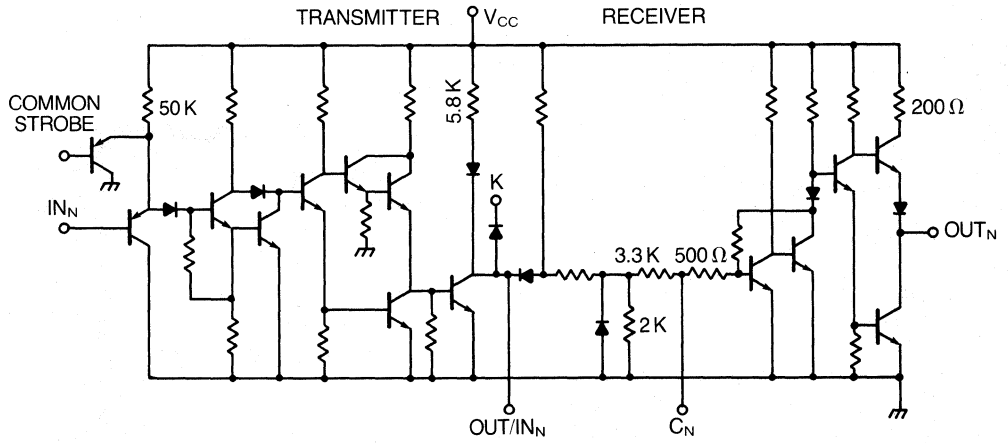
Dwg. No. A-14,178

ABSOLUTE MAXIMUM RATINGS AT T_A = +25°C

Driver Output Voltage, V_{CE}	70 V
Driver Output Sustaining Voltage, $V_{CE(sus)}$	50 V
Driver Continuous Output Current, I_{OUT}	300 mA
Driver Input Voltage, V_{IN}	5.5 V
Receiver Output Current, I_{OUT}	50 mA
Receiver Input Voltage, V_{IN}	70 V
Supply Voltage, V_{CC}	7.0 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

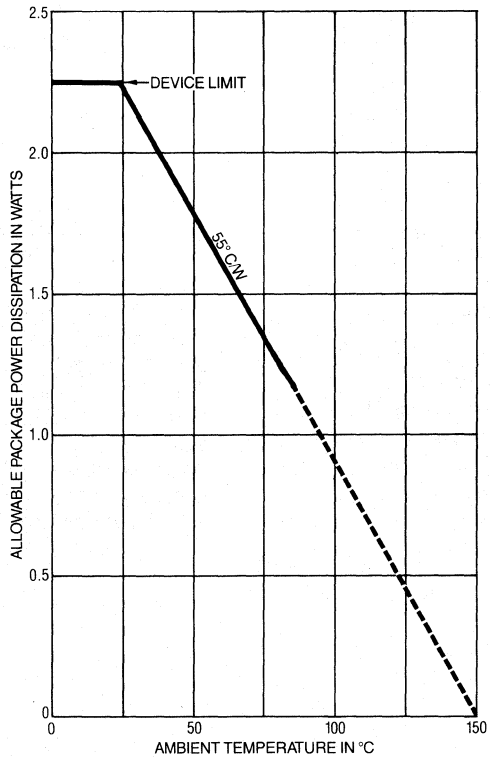
PARTIAL SCHEMATIC

(1 of 4 Channels)



Dwg. No. W-147

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



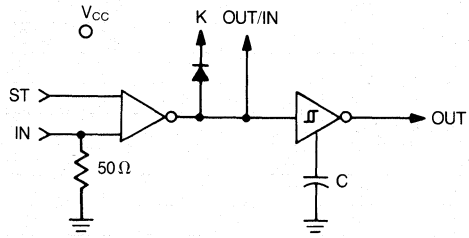
Dwg. No. A-10,379B

ELECTRICAL CHARACTERISTICS at T_A = +25°C, Figure 1 and 2, 3, 4, or 5 as specified.

Characteristic	Test Conditions						Limits			
	V_{CC}	Input	Strobe	Out/In	C	Output	Min.	Typ.	Max.	Units
DRIVERS										
Output Leakage Current	4.5V	Open	0.8V	70V†	Open	Open	—	—	70	µA
Output Saturation Voltage	4.5V	2.0V	2.0V	210mA	Open	Open	—	0.2	0.4	V
	4.5V	2.0V	2.0V	300mA	Open	Open	—	0.4	0.6	V
Output Sat. Voltage Matching	4.5V	2.0V	2.0V	210mA	Open	Open	—	±20	±50	mV
Output Sustaining Voltage*	5.0V	3L0V	2.0V	Fig. 2	Open	Open	50	—	—	V
Output Voltage	4.5V	0.8V	2.0V	−160µA	Open	Open	2.25	—	—	V
Logic Input Voltage	4.5V	—	—	Open	Open	Open	2.0	—	—	V
	4.5V	—	—	Open	Open	Open	—	—	0.8	V
Logic Input Current	5.5V	5.5V	2.0V	Open	Open	Open	—	—	20	µA
	5.5V	0.1V	2.0V	Open	Open	Open	−1.0	—	−20	µA
Strobe Input Current	5.5V	2.0V	5.5V	Open	Open	Open	—	—	50	µA
	5.5V	2.0V	0.1V	Open	Open	Open	—	—	−50	µA
Input Clamp Voltage	Open	−12mA	Open	Open	Open	Open	0	—	−1.6	V
Propagation Delay Time	5.5V	3L0V	2.0V	Fig. 3	Open	Open	—	—	750	ns
	5.5V	2.0V	3L0V	Fig. 3	Open	Open	—	—	750	ns
	5.5V	3L0V	2.0V	Fig. 4	Open	Open	—	—	1.4	µs
	5.5V	2.0V	3L0V	Fig. 4	Open	Open	—	—	1.4	µs
	4.5V	0J3V	2.0V	Fig. 3	Open	Open	—	—	600	ns
	4.5V	2.0V	0J3V	Fig. 3	Open	Open	—	—	600	ns
	4.5V	0J3V	2.0V	Fig. 4	Open	Open	—	—	600	ns
	4.5V	2.0V	0J3V	Fig. 4	Open	Open	—	—	600	ns
Output Rise Time	4.5V	3L0V	2.0V	Fig. 3	Open	Open	—	—	175	ns
Ouput Fall Time	5.5V	0J3V	2.0V	Fig. 3	Open	Open	—	—	175	ns
Clamp Diode Leakage Current	V_R = 70V			0.0V	Open	Open	—	—	70	µA
Clamp Diode Forward Voltage	I_F = 300mA				Open	Open	—	1.6	1.8	V
Supply Current (All Drivers)	5.5V	0.0V	0.8V	—	Open	Open	—	—	20	mA
	5.5V	2.0V	2.0V	—	Open	Open	—	—	50	mA
RECEIVERS										
Output Voltage	4.5V	0.8V	2.0V	Open	2.0V	4.0mA	—	—	0.5	V
	4.5V	2.0V	2.0V	Open	0.0V	−400µA	2.4	—	—	V
Short-Circuit Output Current	5.5V	2.0V	2.0V	Open	Open	0.0V	−2.0	—	−50	mA
Input Current	5.5V	Open	0.0V	4.0V	Open	Open	−250	—	—	µA
	4.5V	Open	0.0V	0.1V	Open	Open	—	—	−500	µA
Input Voltage	4.5V	Open	0.0V	—	Open	Low	2.0	—	—	V
	4.5V	Open	0.0V	—	Open	High	—	—	0.8	V
Input Voltage Hysteresis	4.5V	Open	0.0V	0J3L0V	Open		250	—	775	mV
Propagation Delay Time	4.5V	Open	0.0V	0J3V	Open	Fig. 5	—	—	375	ns
	5.5V	Open	0.0V	3L0V	Open	Fig. 5	—	—	375	ns
Output Fall Time	5.5V	Open	0.0V	0J3V	Open	Fig. 5	—	—	75	ns
Output Rise Time	5.5V	Open	0.0V	3L0V	Open	Fig. 5	—	—	75	ns
Noise Immunity	5.5V	Open	0.0V	0J2V	0.1µF	Open	400	—	—	µs
	4.5V	Open	0.0V	0J2V	0.1µF	Open	—	—	1400	µs

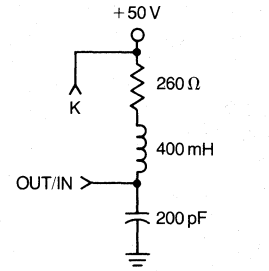
Note: Negative current is defined as coming out of (sourcing) the specified device pin.
**$V_{OUT\ (sus)}$ is measured with a 5 ms ON pulse, 12 ms after turn-OFF.*
†Output clamp diode reverse-biased with V_K = 71 V.

TEST FIGURES



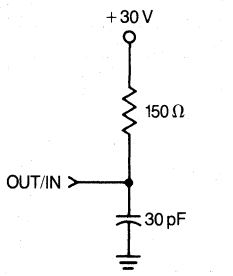
Dwg. No. W-148

Figure 1



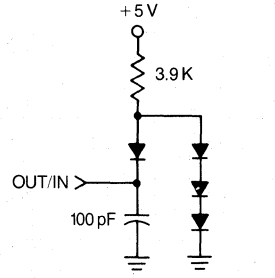
Dwg. No. W-149

Figure 2



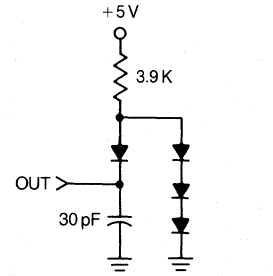
Dwg. No. W-151

Figure 3



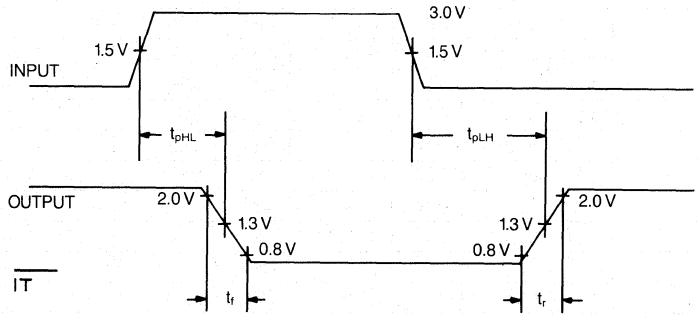
Dwg. No. W-150

Figure 4



Dwg. No. W-152

Figure 5



Dwg. No. W-153

TIMING WAVESHAPES
(Figures 4 and 5)

APPLICATIONS INFORMATION

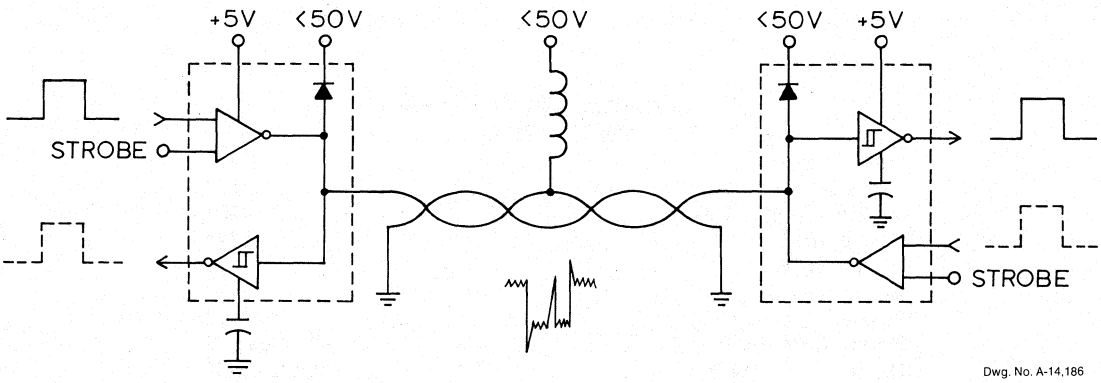
Systems designers are often concerned with interfacing subsystems and transmitting data a considerable distance. Whether it is to a nearby circuit board or to another unit in a large spread-out system, the quality of the signal reproduced in the receiving unit is dependent on:

Driver characteristics
Transmission line characteristics
Line length
General layout and noise environment
Receiver characteristics
Data transmission rate

Unbalanced (common-mode) data transmission is often preferred, since the cabling requires only a single wire plus ground and the circuits are generally lower in cost. However, the data transmission is susceptible to common-mode noise, such as ground IR noise and crosstalk. For noise immunity, the receiver should include pulse-width discrimination and hysteresis. A bus should not extend out of its subsystem's electronic enclosure without special care. Cables should be in the form of twisted pair or flat cable where the signal wires are alternated with ground wires.

If power loads are not being driven, a high output current drive capability allows party-line operation with a low line impedance. The line can be terminated at both ends and still give considerable noise margin at the receiver.

TYPICAL APPLICATION

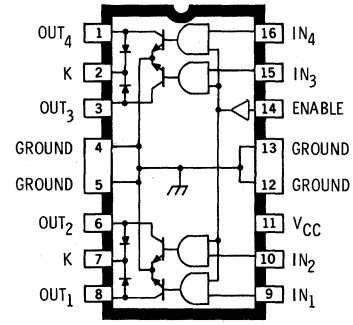


Dwg. No. A-14,186

UDN-2543B QUAD NAND-GATE POWER DRIVER —For Incandescent or Inductive Loads

FEATURES

- 1.0 A Output Current
- Output Voltage to 60 V
- Low Output-Saturation Voltage
- Integral Output-Suppression Diodes
- Efficient Input/Output Pin Structure
- TTL, CMOS, PMOS, NMOS Compatible
- Over-Current Protected



Dwg. No. A-11,561

Providing interface between low-level signal processing circuits and power loads to 240 W, the UDN-2543B quad power driver combines NAND logic gates and high-current bipolar outputs. Each of the four independent outputs can sink up to 1 A in the ON state. The outputs have a minimum breakdown voltage of 60 V and a sustaining voltage of 35 V. Inputs are compatible with most TTL, DTL, LSTTL, and 5 V CMOS and PMOS logic systems.

Over-current protection has been designed into the UDN-2543B and typically occurs at 1 A. It protects the device from output short-circuits with supply voltages of up to 25 V. When the maximum driver output current is reached, that output stage is driven linearly. If the over-current condition continues, that output driver's thermal limiting will operate, limiting the driver's power dissipation and junction temperature. The outputs also include transient suppression diodes for use with inductive loads such as relays, solenoids, and dc stepping motors. In display applications, the diodes can be used for the lamp-test function.

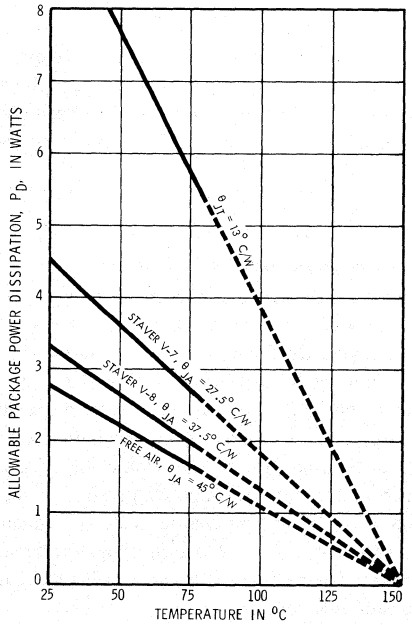
The UDN-2543B is supplied in a 16-pin dual in-line plastic package with heat-sink contact tabs. The lead configuration allows easy attachment of an inexpensive heat-sink and fits a standard integrated circuit socket or a printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

Output Voltage, V_{CE}	60 V
Over-Current Protected Output Voltage, V_{CE}	25 V
Min. Output Sustaining Voltage, $V_{CE(SUS)}$	35 V
Output Current, I_{OUT}	1.0 A*
Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	18 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

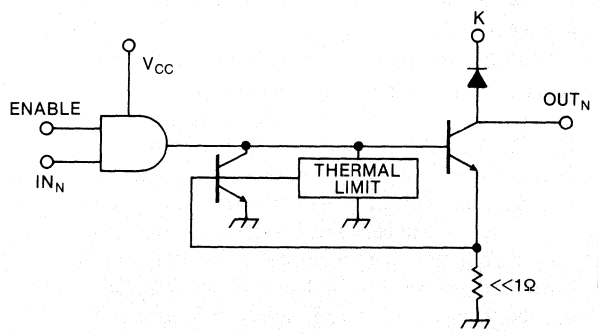
*Outputs are current limited at approximately 1.0 A per driver and junction temperature limited if current in excess of 1.0 A is attempted. See Circuit Description and Applications Section for further information.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,793A

FUNCTIONAL BLOCK DIAGRAM
(1 of 4 Channels)



Dwg. No. D-1005

3

ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{ENABLE} = 2.0 V	–	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{ENABLE} = 0.8 V	–	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{ENABLE} = 0.8 V	35	–	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	200	mV
		I_{OUT} = 400 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	400	mV
		I_{OUT} = 700 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	600	mV
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	–	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	–	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.0 V	–	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.8 V	–	-10	µA
Total Supply Current	I_{CC}	I_{OUT} = 700 mA, V_{IN}* = V_{ENABLE} = 2.0 V	–	65	mA
		Outputs Open, V_{IN}* = 0.8 V, V_{ENABLE} = 2.0 V	–	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	–	1.6	V
		I_F = 1.5 A	–	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, V_{IN} = V_{ENABLE} = 2.0 V, $D_1 + D_2$ or $D_3 + D_4$	–	50	µA

**All inputs simultaneously, all other tests are performed with each input tested separately.*

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-on/in-rush current can destroy semiconductor lamp drivers and contributes to poor lamp reliability. However, lamps with steady-state current ratings up to 700 mA can be driven with the UDN-2543A without the need for warming or current limiting resistors.

When an incandescent lamp is initially turned ON, the cold lamp filament is at minimum resistance and would normally allow a 10× to 12× in-rush current. With the UDN-2543A, during turn-on, the high in-rush current is sensed by the internal low-value sense resistor, drive current to the output stage is diverted by the shunting transistor, and the load current is limited to approximately 1 A. During this short transition period, the output driver is driven in a linear fashion. During lamp warm-up, the filament resistance increases to its maximum value, the output driver goes into saturation and applies full supply voltage to the lamp.

The internal diodes can be used to perform the lamp-test function.

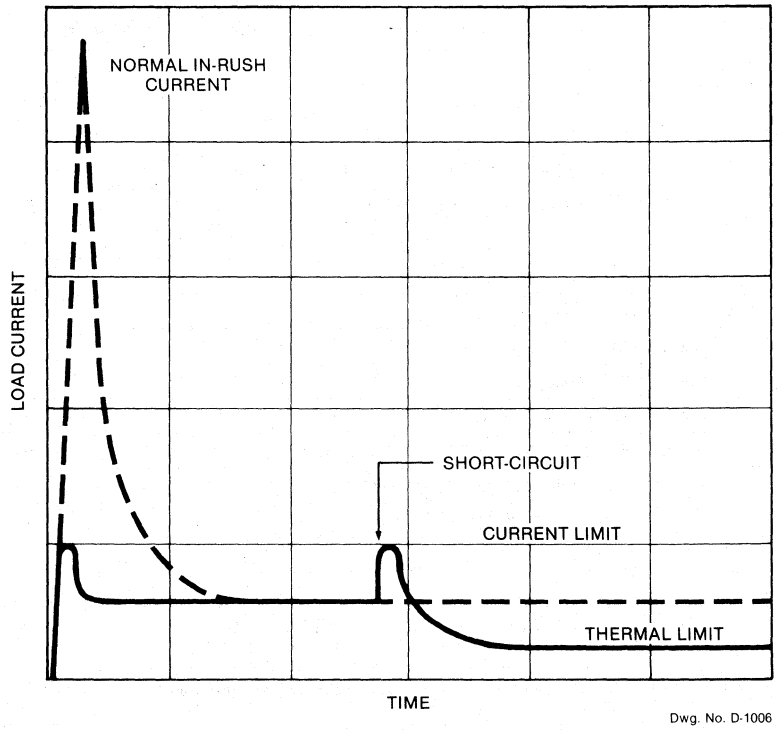
INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes which occur when turning OFF an inductive load.

FAULT CONDITIONS

(Shorted Load or Stalled Motor)

In the event of a shorted load, shorted winding, or stalled motor, the load current will attempt to increase. As described above, the drive current to the output stage is diverted (limiting the load current to about 1 A), causing the output stage to go linear. As the junction temperature of the output stage increases, the thermal limit circuit will become operational, further decreasing the drive current. The load current (junction temperature) is then a function of ambient temperature, state of remaining drivers, supply voltage, and load resistance. If the fault condition is corrected, the output driver will return to its normal saturated condition.



Dwg. No. D-1006

SERIES UDN-2580A
8-CHANNEL SOURCE DRIVERS

FEATURES

- TTL, CMOS, PMOS, NMOS Compatible
- High Output Current Ratings
- Internal Transient Suppression
- Efficient Input/Output Pin Structure

THIS versatile family of integrated circuits, originally designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic- and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

Series UDN-2580A source drivers can drive incandescent, LED, or vacuum fluorescent displays. Internal transient-suppression diodes permit the drivers to be used with inductive loads.

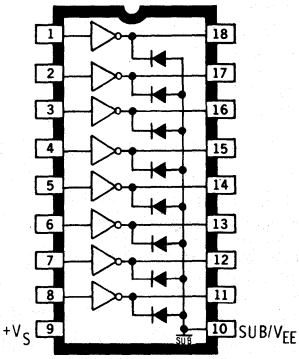
Type UDN-2580A is a high-current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

Type UDN-2585A is a driver designed for applications requiring low output saturation voltages. Typical loads are low-voltage LEDs and incandescent displays. The eight non-Darlington outputs will simultaneously sustain continuous load currents of -120 mA at ambient temperatures to $+70°C$.

Type UDN-2588A, a high-current source driver similar to Type UDN-2580A, has separate logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies.

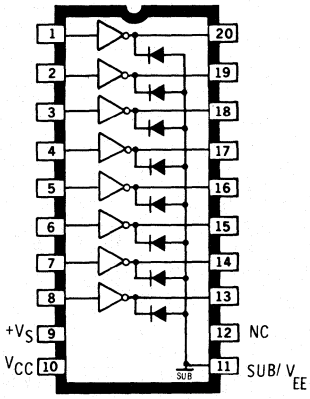
Types UDN-2580A and UDN-2588A are rated for operation with output voltages of up to 50 V. Selected devices, carrying the suffix "-1" on the Sprague part number, have maximum ratings of 80 V.

Types UDN-2580A and UDN-2585A are furnished in 18-pin dual in-line plastic packages; Type UDN-2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.



DWG.NO. A-11,359

UDN-2580A
UDN-2585A



DWG.NO. A-11,357

UDN-2588A

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature for Any One Driver (unless otherwise noted)

	UDN-2580A	UDN-2580A-1	UDN-2585A	UDN-2588A	UDN-2588A-1
Output Voltage, V_{CE}	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_S (ref. sub.)	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_{CC} (ref. sub.)	—	—	—	50 V	80 V
Input Voltage, V_{IN} (ref. V_S)	−30 V	−30 V	−20 V	−30 V	−30 V
Total Current, $I_{CC} + I_S$	−500 mA	−500 mA	−250 mA	−500 mA	−500 mA
Substrate Current, I_{SUB}	3.0 A	3.0 A	2.0 A	3.0 A	3.0 A

Allowable Power Dissipation, P_D (single output) ..... 1.0 W
(total package) ..... 2.2 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 18 mW/°C above 25°C

For simplification, these devices are characterized on the following pages with specific voltages for inputs, logic supply (V_S), load supply (V_{EE}), and collector supply (V_{CC}). Typical use of the UDN-2580A and UDN-2580A-1 is with negative referenced logic. The more common application of the UDN-2585A, UDN-2588A, and UDN-2588A-1 is with positive referenced logic supplies. In application, the devices are capable of operation over a wide range of logic and supply voltage levels:

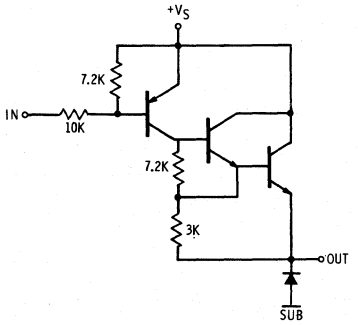
TYPICAL OPERATING VOLTAGES

V_S	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
0 V	−15 V to −3.6 V	−0.5 V to 0 V	NA	−25 V	UDN-2585A
				−50 V	UDN-2580A
				−80 V	UDN-2580A-1
+5 V	0 V to +1.4 V	+4.5 V to +5 V	NA	−20 V	UDN-2585A
				−45 V	UDN-2580A
				−75 V	UDN-2580A-1
			≤5 V	−45 V	UDN-2588A
				−75 V	UDN-2588A-1
+12 V	0 V to +8.4 V	+11.5 V to +12 V	NA	−13 V	UDN-2585A
				−38 V	UDN-2580A
				−68 V	UDN-2580A-1
			≤12 V	−38 V	UDN-2588A
				−68 V	UDN-2588A-1
+15 V	0 V to +11.4 V	+14.5 V to +15 V	NA	−10 V	UDN-2585A
				−35 V	UDN-2580A
				−65 V	UDN-2580A-1
			≤15 V	−35 V	UDN2588A
				−65 V	UDN-2588A-1

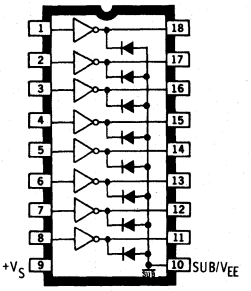
NOTE: The substrate must be tied to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal circuit operation.

UDN-2580A
UDN-2580A-1

PARTIAL SCHEMATIC



DWG.NO. A-11,358



DWG.NO. A-11,359

3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = −45 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UDN-2580A	V_{IN} = −0.5 V, V_{OUT} = V_{EE} = −50 V	—	50	μA
			V_{IN} = −0.4 V, V_{OUT} = V_{EE} = −50 V, T_A = 70°C	—	100	μA
		UDN-2580A-1	V_{IN} = −0.5 V, V_{OUT} = V_{EE} = −80 V	—	50	μA
			V_{IN} = −0.4 V, V_{OUT} = V_{EE} = −80 V, T_A = 70°C	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2580A	V_{IN} = −0.4 V, I_{OUT} = −25 mA, Note 1	35	—	V
		UDN-2580A-1	V_{IN} = −0.4 V, V_{EE} = −75 V, I_{OUT} = −25 mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	V_{IN} = −2.4 V, I_{OUT} = −100 mA	—	1.8	V
			V_{IN} = −3.0 V, I_{OUT} = −225 mA	—	1.9	V
			V_{IN} = −3.6 V, I_{OUT} = −350 mA	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	V_{IN} = −3.6 V, I_{OUT} = −350 mA	—	−500	μA
			V_{IN} = −15 V, I_{OUT} = −350 mA	—	−2.1	mA
	$I_{IN(OFF)}$	Both	I_{OUT} = −500 μA, T_A = 70°C, Note 3	−50	—	μA
Input Voltage	$V_{IN(ON)}$	Both	I_{OUT} = −100 mA, V_{CE} ≤1.8 V, Note 4	—	−2.4	V
			I_{OUT} = −225 mA, V_{CE} ≤1.9 V, Note 4	—	−3.0	V
			I_{OUT} = −350 mA, V_{CE} ≤2.0 V, Note 4	—	−3.6	V
	$V_{IN(OFF)}$	Both	I_{OUT} = −500 μA, T_A = 70°C	−0.2	—	V
Clamp Diode Leakage Current	I_R	UDN-2580A	V_R = 50 V, T_A = 70°C	—	50	μA
		UDN-2580A-1	V_R = 80 V, T_A = 70°C	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, t_p ≤300 μs, duty cycle ≤2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

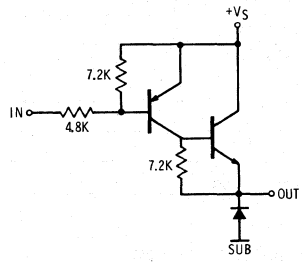
UDN-2585A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 0$ V, $V_{EE} = -20$ V (unless otherwise noted)

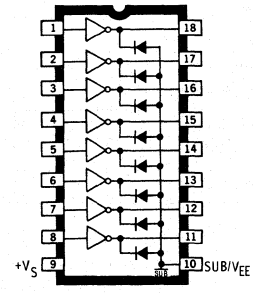
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} = -0.5$ V, $V_{OUT} = V_{EE} = -25$ V	—	50	μA
		$V_{IN} = -0.4$ V, $V_{OUT} = V_{EE} = -25$ V, $T_A = 70°C$	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = -0.4$ V, $I_{OUT} = -25$ mA, Note 1	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = -4.6$ V, $I_{OUT} = -60$ mA	—	1.1	V
		$V_{IN} = -4.6$ V, $I_{OUT} = -120$ mA	—	1.2	V
Input Current	$I_{IN(ON)}$	$V_{IN} = -4.6$ V, $I_{OUT} = -120$ mA	—	−1.6	mA
		$V_{IN} = -14.6$ V, $I_{OUT} = -120$ mA	—	−5.0	mA
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = -120$ mA, $V_{CE} \leq 1.2$ V, Note 3	—	−4.6	V
	$V_{IN(OFF)}$	$I_{OUT} = -100$ μA, $T_A = 70°C$	−0.4	—	V
Clamp Diode Leakage Current	I_R	$V_R = 25$ V, $T_A = 70°C$	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 120$ mA	—	2.0	V
Input Capacitance	C_{IN}		—	25	pF
Turn-On Delay	t_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, $t_p \leq 300$ μs, duty cycle ≤2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
4. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

PARTIAL SCHEMATIC



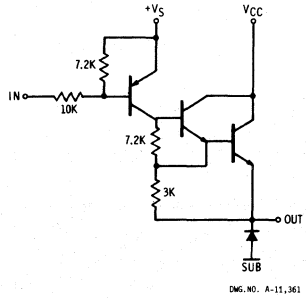
DWG.NO. A-11,360



DWG.NO. A-11,359

UDN-2588A
UDN-2588A-1

PARTIAL SCHEMATIC



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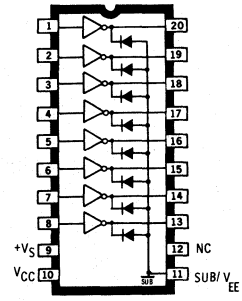


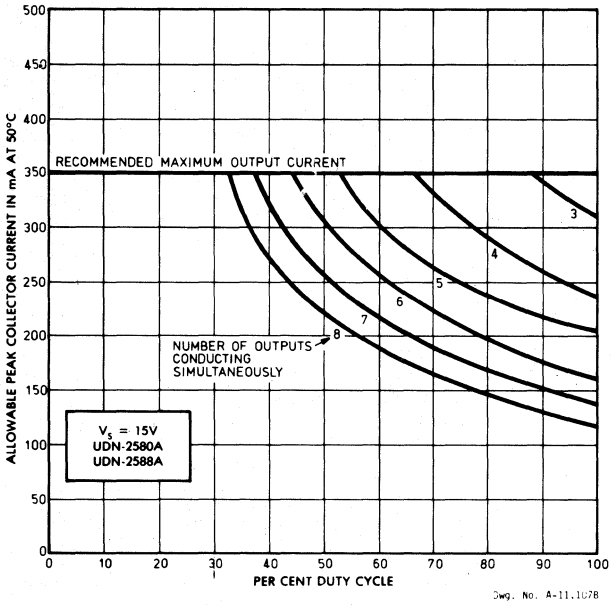
DWG. NO. A-11,357

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V, V_{CC} = 5.0 V, V_{EE} = −40 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UDN-2588A	V_{IN} ≥4.5 V, V_{OUT} = V_{EE} = −45 V	—	50	μA
			V_{IN} ≥4.6 V, V_{OUT} = V_{EE} = −45 V, T_A = 70°C	—	100	μA
		UDN-2588A-1	V_{IN} ≥4.5 V, V_{OUT} = V_{EE} = −75 V	—	50	μA
			V_{IN} ≥4.6 V, V_{OUT} = V_{EE} = −75 V, T_A = 70°C	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2588A	V_{IN} ≥4.6 V, I_{OUT} = −25 mA, Note 1	35	—	V
		UDN-2588A-1	V_{IN} ≥4.6 V, V_{EE} = −70 V, I_{OUT} = −25 mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	V_{IN} = 2.6 V, I_{OUT} = −100 mA, Ref. V_{CC}	—	1.8	V
			V_{IN} = 2.0 V, I_{OUT} = −225 mA, Ref. V_{CC}	—	1.9	V
			V_{IN} = 1.4 V, I_{OUT} = −350 mA, Ref. V_{CC}	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	V_{IN} = 1.4 V, I_{OUT} = −350 mA	—	−500	μA
			V_S = 15 V, V_{EE} = −30 V, V_{IN} = 0 V, I_{OUT} = −350 mA	—	−2.1	mA
	$I_{IN(OFF)}$	Both	I_{OUT} = −500 A, T_A = 70°C, Note 3	−50	—	μA
Input Voltage	$V_{IN(ON)}$	Both	I_{OUT} = −100 mA, V_{CE} ≤1.8 V, Note 4	—	2.6	V
			I_{OUT} = −225 mA, V_{CE} ≤1.9 V, Note 4	—	2.0	V
			I_{OUT} = −350 mA, V_{CE} ≤2.0 V, Note 4	—	1.4	V
	$V_{IN(OFF)}$	Both	I_{OUT} = −500 μA, T_A = 70°C	4.8	—	V
Clamp Diode Leakage Current	I_R	UDN-2588A	V_R = 50 V, T_A = 70°C	—	50	μA
		UDN-2588A-1	V_R = 80 V, T_A = 70°C	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

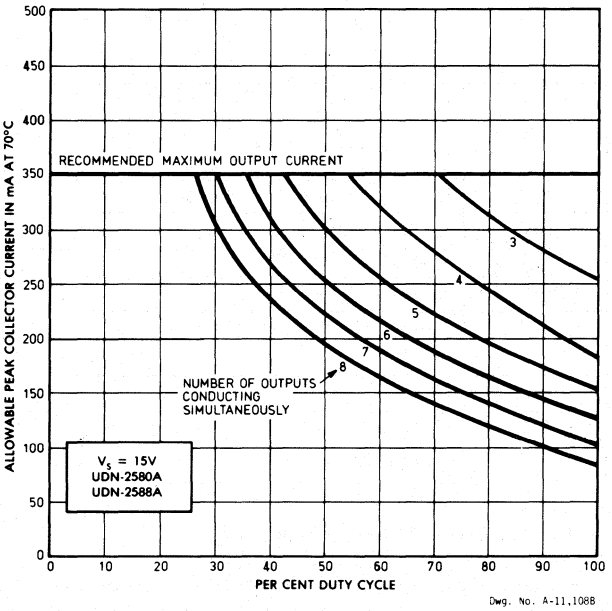
NOTES: 1. Pulsed test, t_p ≤300 μs, duty cycle ≤2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.
6. V_{CC} must never be more positive than V_S.

ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE



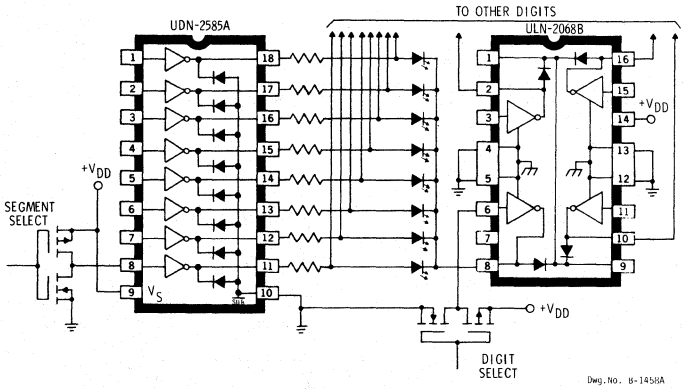
Dwg. No. A-11,107B

ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE

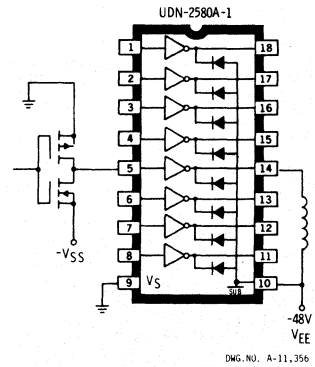


Dwg. No. A-11,108B

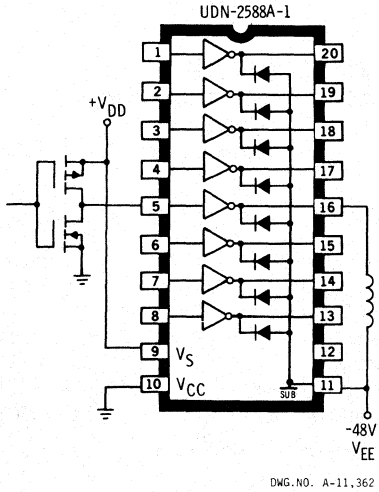
TYPICAL APPLICATIONS



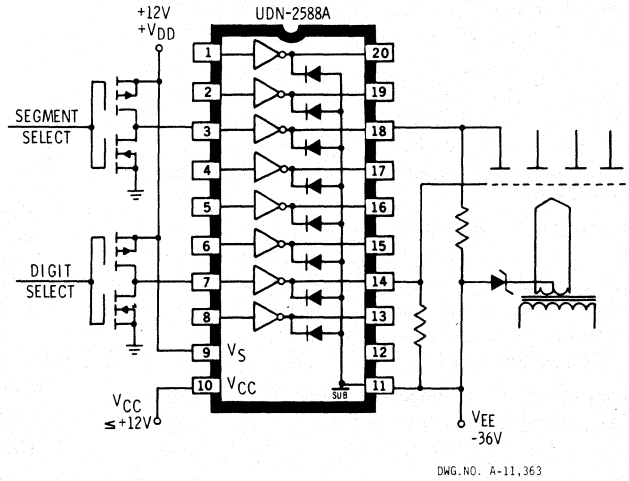
COMMON-CATHODE LED DRIVER



TELECOMMUNICATIONS RELAY DRIVER (Negative Logic)



TELECOMMUNICATIONS RELAY DRIVER (Positive Logic)

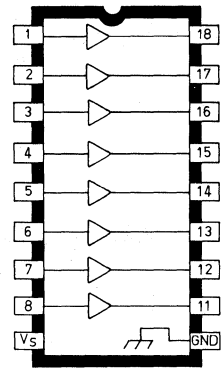


VACUUM FLUORESCENT DISPLAY DRIVER (Split Supply)

UDN-2595A
8-CHANNEL CURRENT-SINK DRIVER

FEATURES

- 200 mA Current Rating
- Low Saturation Voltage
- TTL, CMOS, NMOS Compatible
- Efficient Input/Output Pin Format
- 18-Pin Dual In-Line Plastic Package



Dwg. No. A-11,407

DEVELOPED for use with low-voltage LED and incandescent displays requiring low output saturation voltage, Type UDN-2595A meets many other interface needs, including those exceeding the capabilities of standard logic buffers.

The eight non-Darlington outputs of this driver can simultaneously sink load currents of 100 mA at ambient temperatures of up to +85°C.

The eight-channel driver's active low inputs can be linked directly to TTL, Schottky TTL, DTL, 5 to 16 V CMOS, and NMOS logic. All input connections are on one side of the package, output connections on the other, for simplified layout of printed wiring boards.

Type UDN-2595A is supplied in an 18-pin dual-in-line plastic package with a copper lead frame that maximizes the driver's power-handling capabilities. A hermetically sealed version of Type UDN-2595A, with reduced package power dissipation ratings, is available on special order.

This device complements Sprague Type UDN-2585A, an eight-channel source driver.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

for any one driver
(unless otherwise noted)

Output Voltage, V_{CE} ..... 20 V
Supply Voltage, V_S ..... 20 V
Input Voltage, V_{IN} ..... 20 V
Output Collector Current, I_C ..... 200 mA
Ground Terminal Current, I_{GND} ..... 1.6 A
Allowable Power Dissipation, P_D
(single output) ..... 1.0 W
(total package) ..... 2.2 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

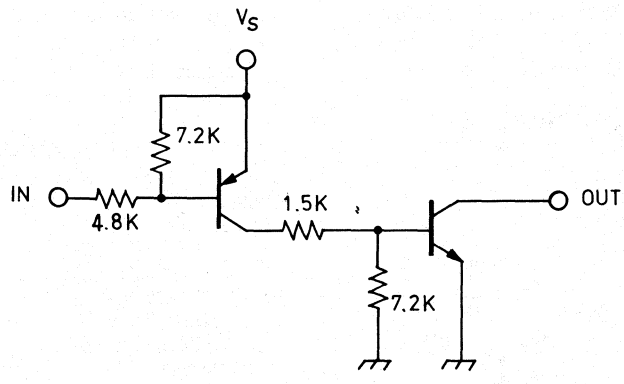
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5$ V, V_{OUT} = 20 V, T_A = 25°C	—	50	µA
		$V_{IN} \geq 4.6$ V, V_{OUT} = 20 V, T_A = 70°C	—	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = 0.4 V, I_{OUT} = 50 mA	—	0.5	V
		V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	0.6	V
Input Current	$I_{IN(ON)}$	V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	−1.6	mA
		V_{IN} = 0.4 V, I_{OUT} = 100 mA, V_S = 15 V	—	−5.0	mA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = 100 mA, $V_{OUT} \leq$ 0.6 V, V_S = 5 V	—	0.4	V
	$V_{IN(OFF)}$	I_{OUT} = 100 µA, T_A = 70°C	4.6	—	V
Input Capacitance	C_{IN}		—	25	pF
Supply Current	I_{SS}	V_{IN} = 0.4 V, I_{OUT} = 100 mA	—	6.0	mA
		V_{IN} = 0.4 V, I_{OUT} = 100 mA, V_S = 15 V	—	20	mA

NOTES:
1. Negative current is defined as coming out of the specified device pin.
2. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified conditions.
3. I_{SS} is measured with any one of eight drivers turned ON.

3

UDN-2595A
ONE OF EIGHT DRIVERS



Dwg. No. A-11,408

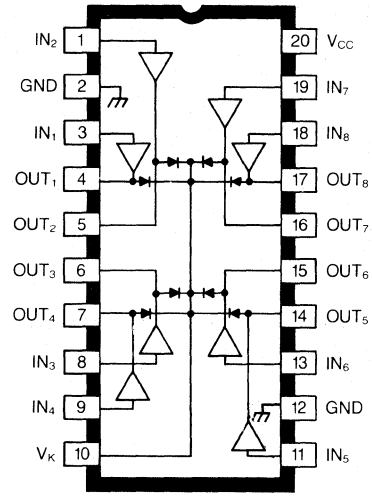
UDN-2596A THROUGH UDN-2599A
8-CHANNEL SATURATED SINK DRIVERS

FEATURES

- Low Output ON Voltages
- Up to 1.0A Sink Capability
- 50V Min. Output Breakdown
- Output Transient-Suppression Diodes
- Output Pull-Down for Fast Turn-Off
- TTL, CMOS Compatible Inputs

Low output saturation voltages at high load currents are provided by UDN-2596A through UDN-2599A sink driver ICs. These devices can be used as interface buffers between standard low-power digital logic (particularly MOS) and high-power loads such as relays, solenoids, stepping motors, and LED or incandescent displays. The eight saturated sink drivers in each device feature high-voltage, high-current open-collector outputs. Transient suppression clamp diodes and a minimum 35V output sustaining voltage allow their use with many inductive loads.

The saturated (non-Darlington) NPN outputs provide low collector-emitter voltage drops as well as improved turn-off times due to an active pull-down function within the output predrive section. The UDN-2596A and UDN-2598A are for use with output loads to 500mA while the UDN-2597A and UDN-2599A are for use with loads to 1A. Adjacent outputs may be paralleled for higher load currents.

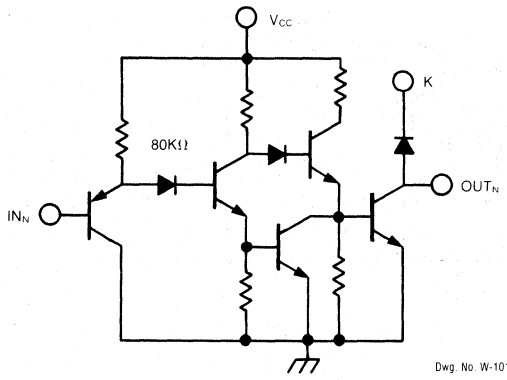


Dwg. No. W-100

Inputs require very low input current and are activated by a low logic level consistent with the much greater sinking capability associated with NMOS, CMOS, and TTL logic. The UDN-2596A and UDN-2597A are rated for use with 5V logic levels while the UDN-2598A and UDN-2599A are for use with 10V to 12V logic levels.

All devices are furnished in 20-pin DIP packages with copper leadframes for improved thermal characteristics.

ONE OF EIGHT DRIVERS



Dwg. No. W-101

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{CE} 50V
Output Current, I_{OUT}
(UDN-2596/98A) 500mA
(UDN-2597/99A) 1.0A
Supply Voltage, V_{CC}
(UDN-2596/97A) 7.0V
(UDN-2598/99A) 15V
Input Voltage, V_{IN}
(UDN-2596/97A) 7.0V
(UDN-2598/99A) 15V
Package Power Dissipation, P_D 2.27W*
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

*Derate at the rate of 18.2mW/°C above T_A = 25°C.

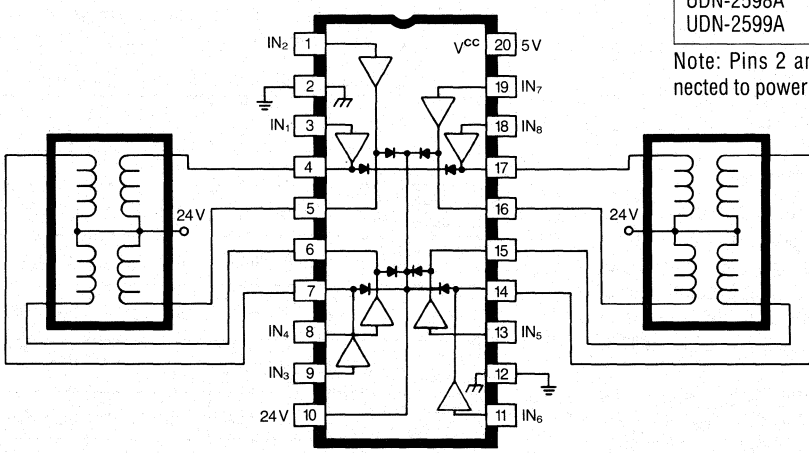
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 5.0V$ (UDN-2596/97A) or 12V (UDN-2598/99A)

Characteristics	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	All	$V_{OUT} = 50V$, $V_{IN} = 2.4V$	—	10	µA
Output Sustaining Voltage	$V_{CE(sus)}$	2596/98	$I_{OUT} = 300mA$, L = 2mH	35	—	V
		2597/99	$I_{OUT} = 750mA$, L = 2mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	2596/98	$I_{OUT} = 300mA$	—	0.5	V
		2597/99	$I_{OUT} = 750mA$	—	1.0	V
Clamp Diode Leakage Current	I_R	All	$V_R = 50V$	—	10	µA
Clamp Diode Forward Voltage	V_F	2596/98	$I_F = 300mA$	—	1.8	V
		2597/99	$I_F = 750mA$	—	1.8	V
Logic Input Current	$I_{IN(0)}$	2596/97	$V_{IN} = 0.8V$	—	−15	µA
		2598/99	$V_{IN} = 0.8V$	—	−50	µA
	$I_{IN(1)}$	2596/97	$V_{IN} = 2.4V$	—	10	µA
		2598/99	$V_{IN} = 12V$	—	10	µA
Supply Current (per driver)	$I_{CC(ON)}$	2596/98	$V_{IN} = 0.8V$	—	6.0	mA
		2597/99	$V_{IN} = 0.8V$	—	22	mA
	$I_{CC(OFF)}$	2596/97	$V_{IN} = 2.4V$	—	1.3	mA
		2598/99	$V_{IN} = 2.4V$	—	2.0	mA
Turn-On Delay	t_{pd0}	All	$0.5E_{IN}$ to $0.5E_{OUT}$	—	3.0	µs
Turn-Off Delay	t_{pd1}	All	$0.5E_{IN}$ to $0.5E_{OUT}$	—	2.0	µs

*Complete part number includes prefix UDN- and suffix A, e.g. UDN-2596A.

3

TYPICAL APPLICATION
DUAL STEPPER MOTOR DRIVE



Dwg. No. W-102A

RECOMMENDED OPERATING CONDITIONS

Type Number	Logic	I_{OUT}
UDN-2596A	5.0V	300mA
UDN-2597A	5.0V	750mA
UDN-2598A	10-12V	300mA
UDN-2599A	10-12V	750mA

Note: Pins 2 and 12 must both be connected to power ground.

SERIES ULN-2800A
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS

IDEALLY SUITED for interfacing between low-level digital logic circuitry and high-power peripheral loads, the Series ULN-2800A high-voltage, high-current Darlington transistor arrays feature peak load current ratings of 600 mA (Series ULN-2800A and ULN-2820A) or 750 mA (Series ULN-2810A) for each of the eight drivers in each device. Under the proper conditions, high-power loads of up to 4 A at 50V (200 W at 23% duty cycle) or 3.2 A at 95 V (304 W at 33% duty cycle) can be controlled. Typical loads include relays, solenoids, stepping motors, multiplexed LED and incandescent displays, and heaters. All devices feature open collector outputs and integral diodes for inductive load transient suppression.

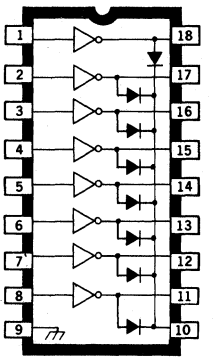
The Series ULN-2801A devices are general purpose arrays which may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate ease of circuit board layout and are priced to compete directly with discrete transistor alternatives.

The Series ULN-2802A was specifically designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also means excellent noise immunity for these devices.

The Series ULN-2803A has a 2.7 kΩ series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs – particularly those beyond the capabilities of standard logic buffers.

The Series ULN-2804A features a 10.5 kΩ series input resistor to permit their operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of the Series ULN-2803A while the required input voltage is less than that required by the Series ULN-2802A.

The Series ULN-2805A is especially designed for use with standard and Schottky TTL where higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.



DWG. NO. A-10,322

The Series ULN-2800A is the standard high-voltage, high-current Darlington array. The output transistors are capable of sinking 500mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The Series ULN-2810A devices are similar except that they will sink 600mA. The Series ULN-2820A will withstand 95 V in the OFF state.

All Series ULN-2800A Darlington arrays are furnished in an 18-pin dual in-line plastic package.

Device Type Number Designation

$V_{CE(MAX)}$ = $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULN-2801A	ULN-2811A	ULN-2821A
14 - 25 V PMOS	ULN-2802A	ULN-2812A	ULN-2822A
5 V TTL, CMOS	ULN-2803A	ULN-2813A	ULN-2823A
6 - 15 V CMOS, PMOS	ULN-2804A	ULN-2814A	ULN-2824A
High Output TTL	ULN-2805A	ULN-2815A	ULN-2825A

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

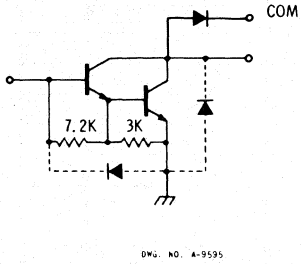
Output Voltage, V_{CE} (Series ULN-2800, 2810A)	50 V
(Series ULN-2820A)	95 V
Input Voltage, V_{IN} (Series ULN-2802, 2803, 2804A)	30 V
(Series ULN-2805A)	15 V
Continuous Collector Current, I_C (Series ULN-2800, 2820A)	500 mA
(Series ULN-2810A)	600 mA
Continuous Base Current, I_B	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.25 W*
Operating Ambient Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 18.18mW/°C above 25°C.

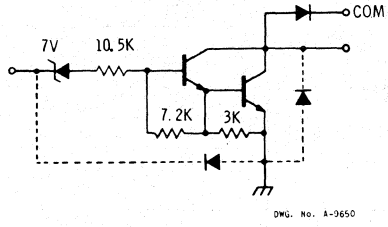
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)}$ = 1.6 V at 50°C with a pulse width of 20 ms and a duty cycle of 40%.

3

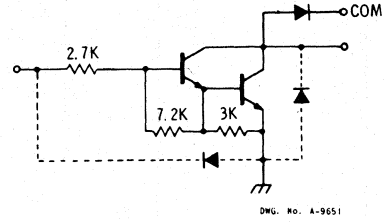
PARTIAL SCHEMATICS



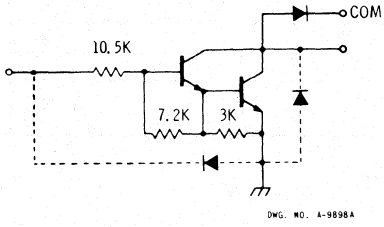
Series ULN-2801A
(each driver)



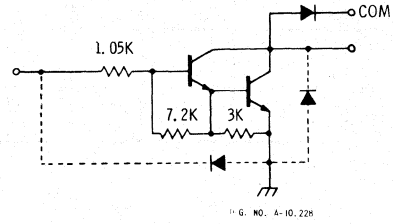
Series ULN-2802A
(each driver)



Series ULN-2803A
(each driver)



Series ULN-2804A
(each driver)



Series ULN-2805A
(each driver)

SERIES ULN-2800A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2802A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2804A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2802A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2803A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2804A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2805A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2802A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2803A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2804A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2805A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2801A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{ON}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

SERIES ULN-2810A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2812A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2814A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
				I_C = 500 mA, I_B = 600 μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2812A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2813A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2814A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2815A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2812A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	17	V
			ULN-2813A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	3.5	V
			ULN-2814A	V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	9.5	V
			ULN-2815A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2811A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
				V_{CE} = 2.0 V, I_C = 500 mA	900	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{ON}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V
				I_F = 500 mA	—	2.1	2.5	V

SERIES ULN-2820A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 95 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2822A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2824A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2822A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2823A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2824A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2825A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2822A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2823A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2824A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2825A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2821A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}		All		—	15	25	pF
Turn-On Delay	t_{ON}		All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}		All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	μA
				V_R = 95 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

TEST FIGURES

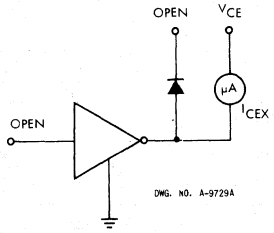


FIGURE 1A

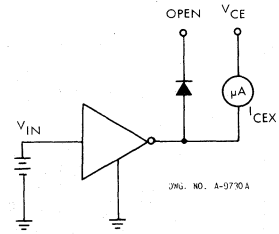


FIGURE 1B

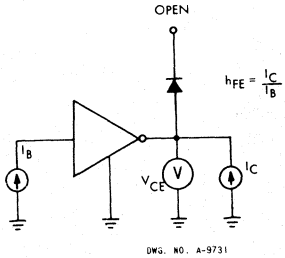


FIGURE 2

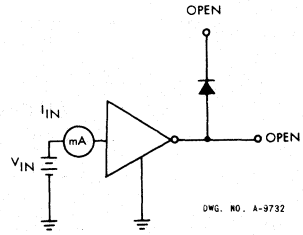


FIGURE 3

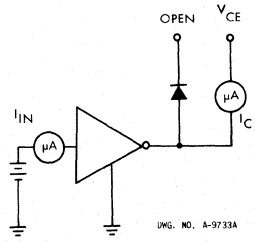


FIGURE 4

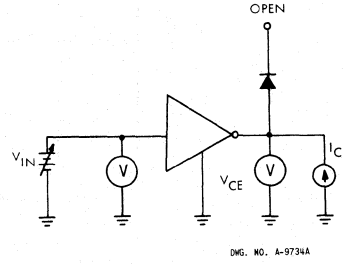


FIGURE 5

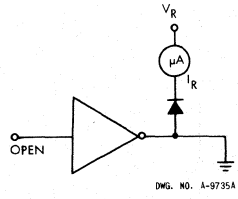


FIGURE 6

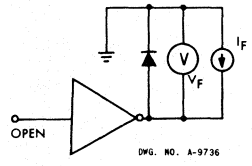
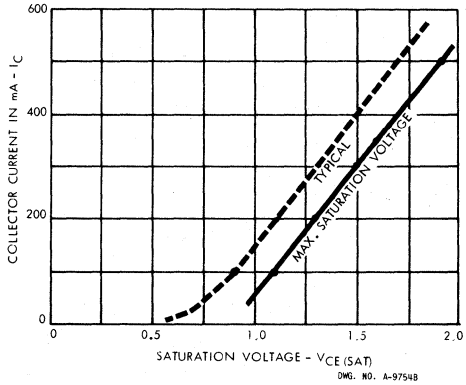
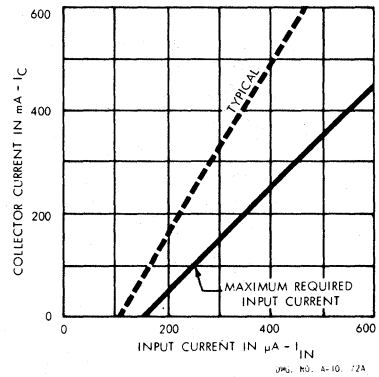


FIGURE 7

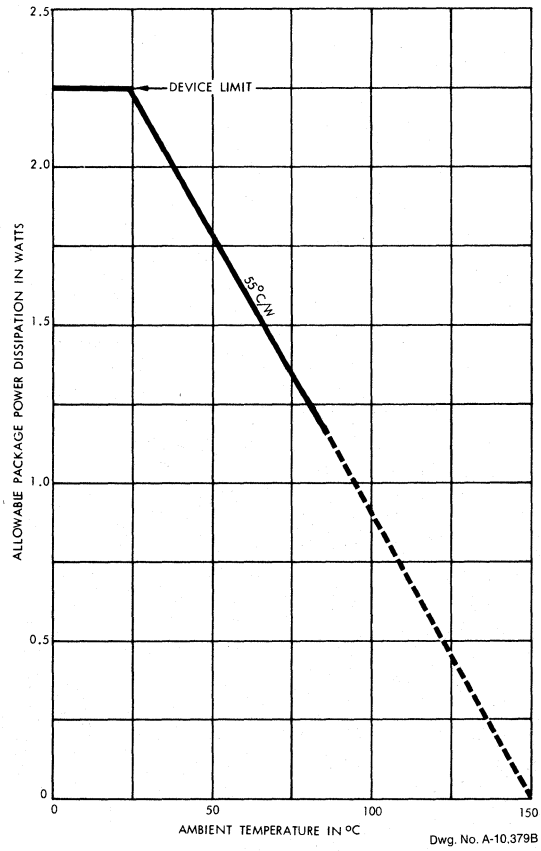
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



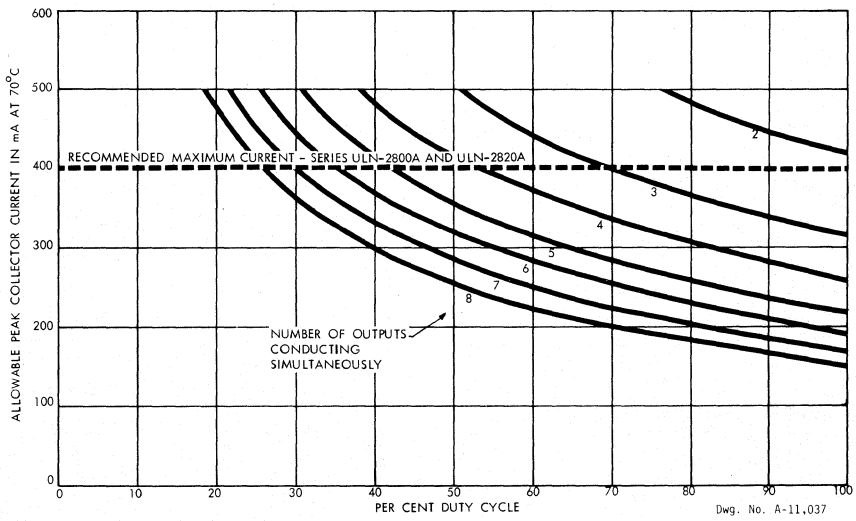
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

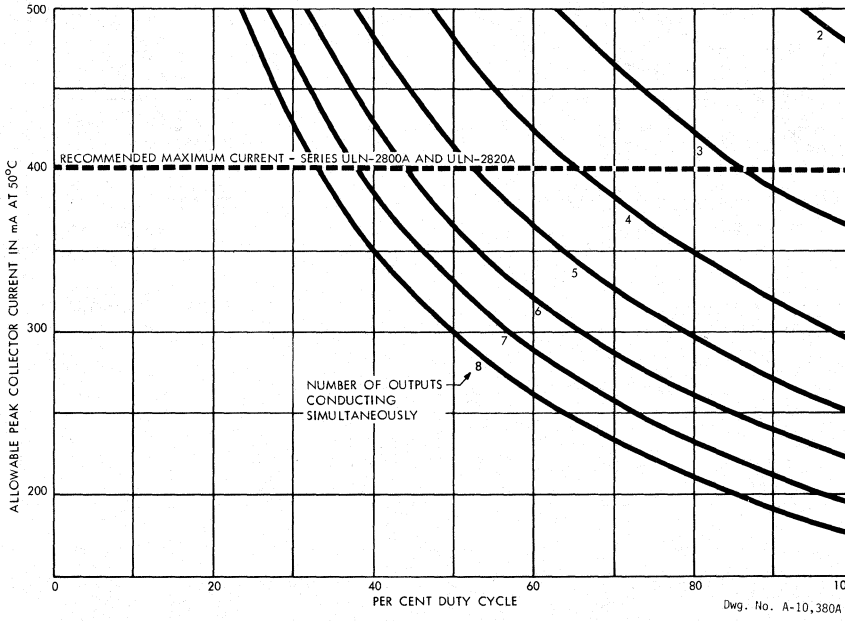


ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

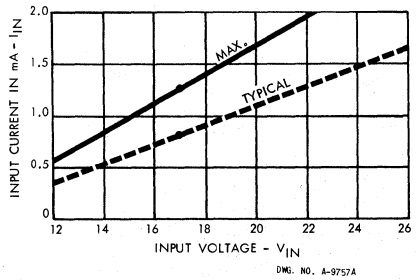


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

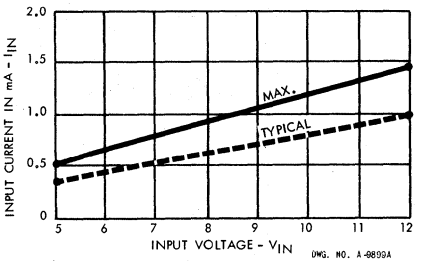




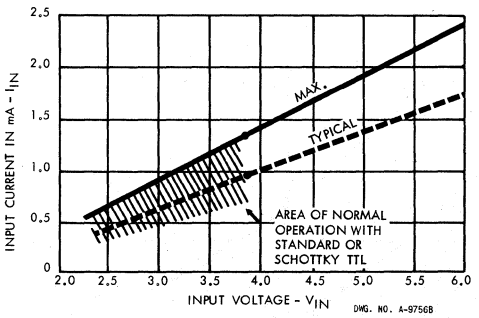
INPUT CURRENT
AS A FUNCTION OF INPUT VOLTAGE



SERIES ULN-2802A



SERIES ULN-2804A



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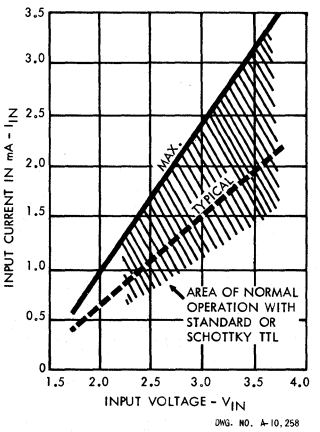
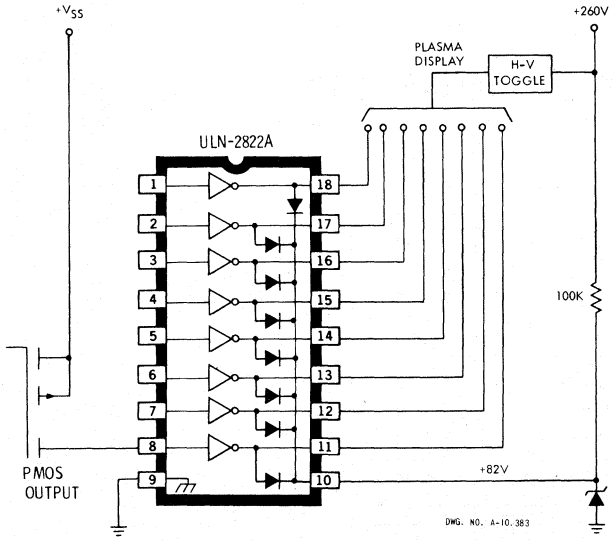
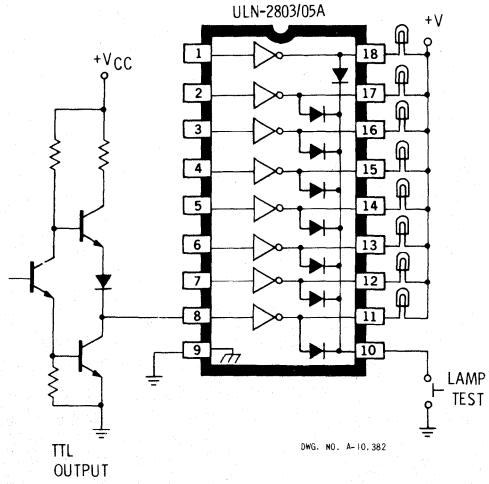


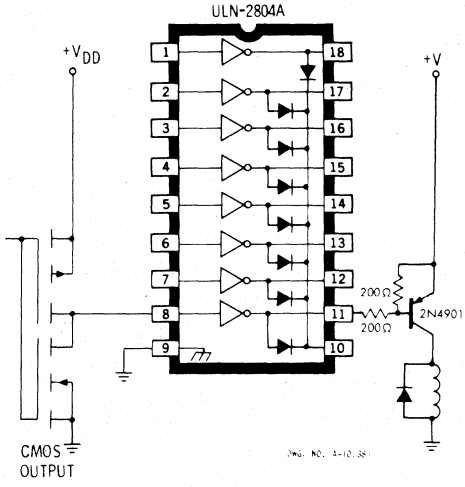
SERIES ULN-2805A



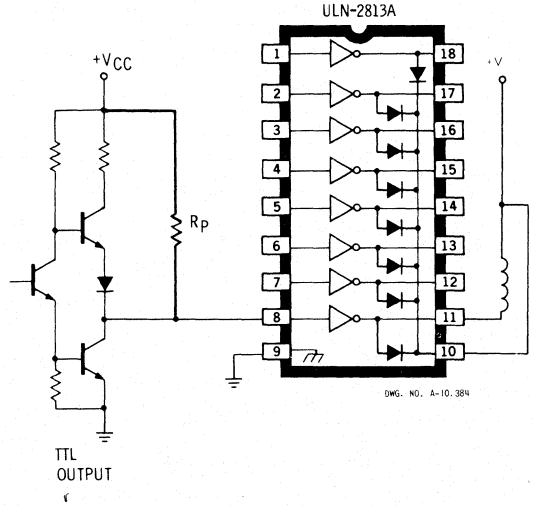
OFF VOLTAGE BIAS FOR HIGH-VOLTAGE LOADS



TTL TO LOAD

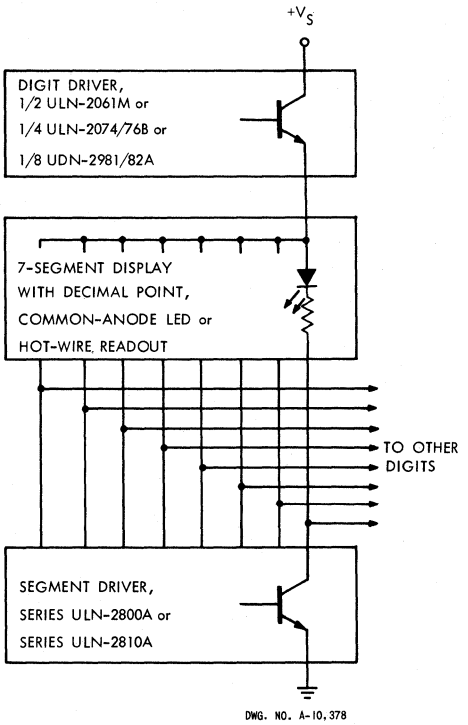


BUFFER FOR HIGHER CURRENT LOADS



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

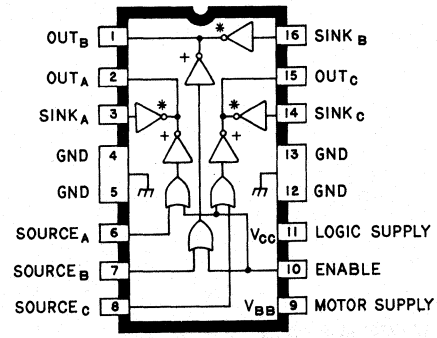
TYPICAL DISPLAY INTERFACE



UDN-2933B AND UDN-2934B
3-CHANNEL HALF-BRIDGE MOTOR DRIVERS

FEATURES

- Output Currents to 1 A
- Output Voltages to 30 V
- Low Output-Saturation Voltage
- Transient-Protected Outputs
- Tri-State Outputs
- TTL or CMOS Compatible Inputs
- Reliable Monolithic Construction



Dwg. No. A-12,356

DEVELOPED for use in 3-phase brushless d-c motor applications, Types UDN-2933B and UDN-2934B provide drive capabilities to 1 A and 30 V. Saturated drivers provide for low output voltage drops at maximum rated current.

The 1 A half-bridge drivers differ only in input circuitry: Type UDN-2933B is compatible with TTL and 5 V CMOS; Type UDN-2934B is used with 12 V CMOS.

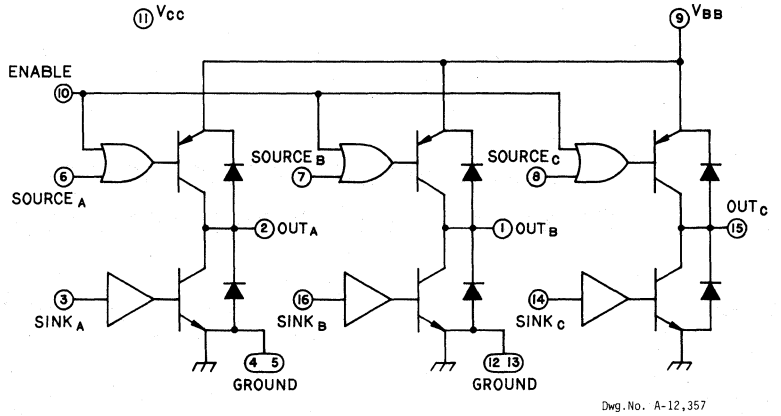
Monolithic construction and a 16-pin dual in-line package with centered heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent power dissipation ratings, minimum size, and ease of installation. The package configuration allows easy attachment of an inexpensive heat sink. It fits a standard IC socket or printed wiring board layout.

Half-bridge drivers with Darlington outputs (Type UDN-2935Z and UDN-2950Z) are supplied in TO-220 power-tab packages for operation with load currents of up to 3.5 A.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Motor Supply Voltage, V_{BB}	30 V
Logic Supply Voltage Range, V_{CC}	
(UDN-2933B)	4.5 V to 7.0 V
(UDN-2934B)	10 V to 15 V
Logic Input Voltage, V_{IN}	V_{CC}
Output Current, I_{OUT}	±1.0 A
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

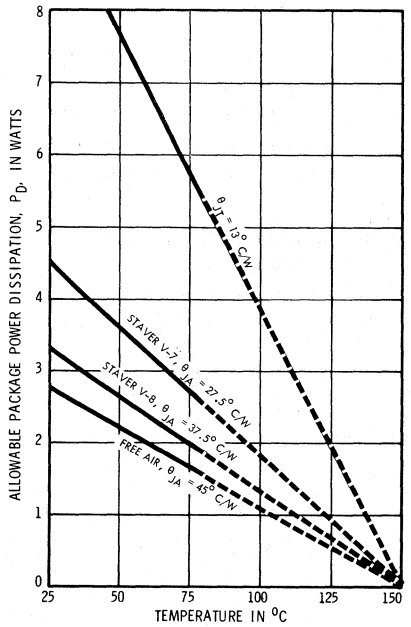
FUNCTIONAL BLOCK DIAGRAM



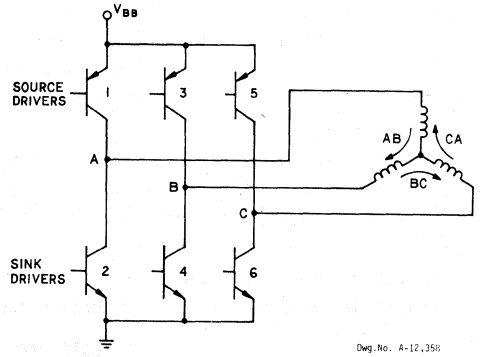
TRUTH TABLE

Sink Driver Input	Source Driver Input	Enable Input	Output
Low	Low	Low	High
Low	High	Low	Open
High	Low	Low	Disallowed
High	High	Low	Low
High	Any	High	Low
Low	Any	High	Open

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,793A



TYPICAL COMMUTATION SEQUENCE

Drivers ON*	Motor Current	Elec. Degrees
1+4	AB	0
1+6	−CA	60
3+6	BC	120
3+2	−AB	180
5+2	CA	240
5+4	−BC	300

*Enable input must be low; Source drivers are turned ON with a logic low, sink drivers are turned ON with a logic high.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 30$ V, $V_{CC} = 5$ V (UDN-2933B) or $V_{CC} = 12$ V (UDN-2934B), $T_{TAB} \leq +70°C$

Characteristic	Symbol	Applicable Devices	Test Condtions	Limits			
				Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	Both	All Drivers OFF, $V_{OUT} = 0$ V	—	−5.0	−100	μA
			All Drivers OFF, $V_{OUT} = 30$ V	—	5.0	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$I_{OUT} = -100$ mA	—	0.80	1.1	V
			$I_{OUT} = 100$ mA	—	0.08	0.2	V
			$I_{OUT} = -250$ mA	—	0.90	1.2	V
			$I_{OUT} = 250$ mA	—	0.13	0.3	V
			$I_{OUT} = -500$ mA	—	1.1	1.5	V
			$I_{OUT} = 500$ mA	—	0.25	0.6	V
			$I_{OUT} = -800$ mA	—	1.3	1.8	V
			$I_{OUT} = 800$ mA	—	0.45	0.8	V
Output Sustaining Voltage	$V_{CE(SUS)}$	Both	$I_{OUT} = \pm 800$ mA, L = 3 mH	30	—	—	V
Motor Supply Current	I_{BB}	Both	All Drivers OFF	—	50	200	μA
			1 Source + 1 Sink ON, No Loads	—	1.0	1.3	mA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 500$ mA	—	1.3	2.0	V
			$I_F = 800$ mA	—	1.3	2.0	V
Logic Input Voltage	$V_{IN(1)}$	UDN-2933B		2.4	—	—	V
		UDN-2934B		8.0	—	—	V
	$V_{IN(0)}$	UDN-2933B		—	—	0.8	V
		UDN-2934B		—	—	4.0	V
Logic Input Current	$I_{IN(1)}$	UDN-2933B	$V_{IN} = 2.4$ V	—	<1.0	10	μA
		UDN-2934B	$V_{IN} = 8.0$ V	—	<1.0	10	μA
	$I_{IN(0)}$	Both	$V_{IN} = 0.8$ V	—	−50	−300	μA
Logic Supply Current	I_{CC}	Both	All Drivers OFF	—	1.7	3.0	mA
			1 Source + 1 Sink ON	—	30	40	mA
Output Rise Time	t_r	Both	$I_{OUT} = -500$ mA, $V_{BB} = 20$ V	—	250	—	ns
			$I_{OUT} = 500$ mA, $V_{BB} = 20$ V	—	30	—	ns
Output Fall Time	t_f	Both	$I_{OUT} = -500$ mA, $V_{BB} = 20$ V	—	500	—	ns
			$I_{OUT} = 500$ mA, $V_{BB} = 20$ V	—	50	—	ns

NOTES: 1. Each driver is tested separately.
2. Positive (negative) current is defined as going into (coming out of) the specified device pin.

UDN-2956A AND UDN-2957A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- 500 mA Output Source Current
- 50 V Output Sustaining Voltage
- Output Transient Protection
- 6-16 V PMOS,CMOS Input—UDN-2956A
- TTL, DTL, 5 V CMOS Input—UDN-2957A
- Plastic or Cer-DIP Package

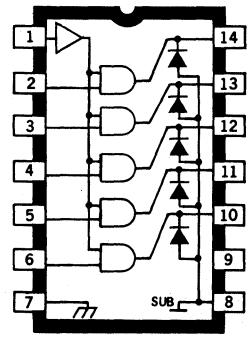
COMPRISED of five common-collector NPN Darlington output stages, associated common-base PNP input stages, and a common ENABLE stage, the UDN-2956A and UDN-2957A high-voltage, high-current source drivers are used to switch the ground end of loads that are directly connected to a negative supply. Typical loads include telephone relays, PIN diodes, and LEDs.

Both devices will sustain output OFF voltages of −80 V and will source currents to −500 mA per driver. Under normal operating conditions, these units will sustain load currents of −200 mA on each of the five drivers simultaneously at ambient temperatures up to +70°C.

The UDN-2956A driver is intended for use with MOS (PMOS or CMOS) logic input levels operating with supply voltages from 6 V to 16 V. The UDN-2957A driver has appropriate input-current limiting resistors for operation from TTL, Schottky TTL, DTL, and 5 V CMOS. With either device, the input and ENABLE levels must both be biased towards the positive supply to activate the output load.

Integral transient-suppression diodes allow these devices to be used with inductive loads without adding discrete diodes. In order to maintain isolation between drivers, the substrate should be connected to the most negative supply.

Input connections are on one side of the dual in-line package, output connections on the other side to simplify printed wiring board layout.



Dwg. No. A-10,229A

The UDN-2956A and UDN-2957A high-voltage, high-current drivers are supplied in 14-lead dual in-line packages conforming to JEDEC outline TO-116 (MO-001AA). These devices can also be ordered in ceramic/glass (cer-DIP) hermetic packages by changing the last character of the part number from 'A' to 'R.' Except for slightly reduced package power dissipation capability, devices in cer-DIP hermetic packages have electrical ratings identical to those in plastic packages and are pin compatible with them.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
(Reference Pin 7)

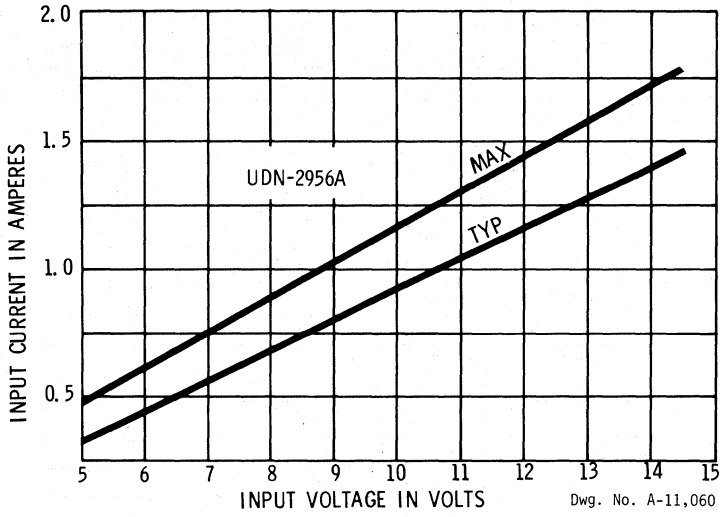
Supply Voltage, V_{EE}	−80 V
Input Voltage, V_{IN} (UDN-2956A)	+20 V
(UDN-2957A)	+10 V
Output Current, I_{OUT}	−500 mA
Power Dissipation, P_D (any one driver)	1.0 W
(total package)	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

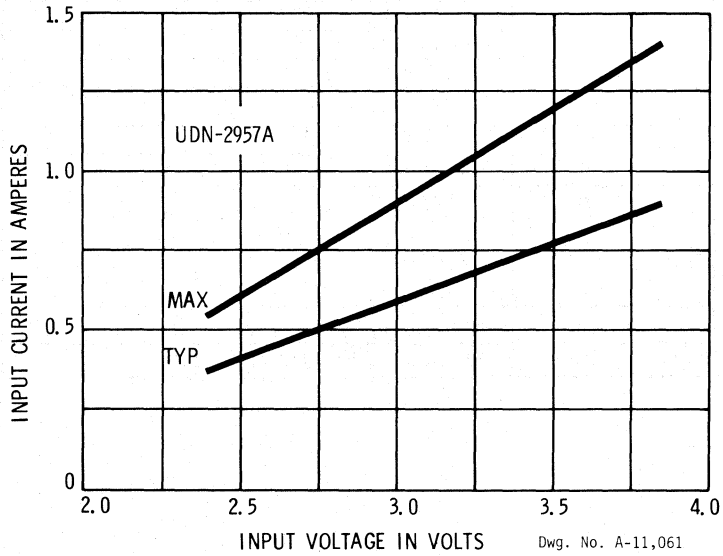
*Derate at the rate of 16.67 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{ENABLE} = V_{IN}$ (unless otherwise specified)

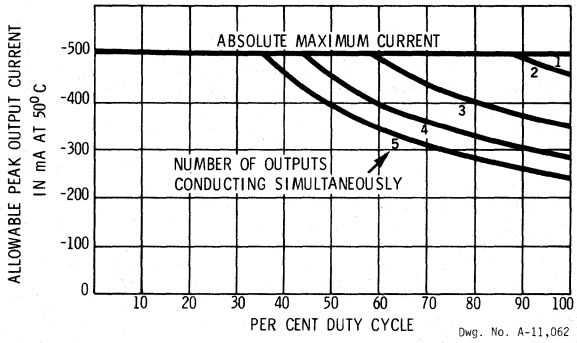
Characteristic	Symbol	Applicable Devices	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDN-2956A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 15$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 15$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
		UDN-2957A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 3.85$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 3.85$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = 70°C$	−200 μA Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDN-2956A	$V_{IN} = 6.0$ V, $I_{OUT} = -100$ mA	− 1.20 V Max.
			$V_{IN} = 7.0$ V, $I_{OUT} = -175$ mA	− 1.35 V Max.
			$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	− 1.70 V Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	− 1.20 V Max.
			$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	− 1.35 V Max.
			$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	− 1.70 V Max.
Input Current	$I_{IN(ON)}$	UDN-2956A	$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	650 μA Max.
			$V_{IN} = 15$ V, $V_{OUT} = -2.0$ V	1.85 mA Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	675 μA Max.
			$V_{IN} = 3.85$ V, $V_{OUT} = -2.0$ V	1.40 mA Max.
	$I_{IN(OFF)}$	ALL	$I_{OUT} = -500$ μA, $T_A = +70°C$	50 μA Min.
Output Source Current	I_{OUT}	UDN-2956A	$V_{IN} = 5.0$ V, $V_{OUT} = -2.0$ V	−125 mA Min.
			$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	−200 mA Min.
			$V_{IN} = 7.0$ V, $V_{OUT} = -2.0$ V	−250 mA Min.
			$V_{IN} = 8.0$ V, $V_{OUT} = -2.0$ V	−300 mA Min.
			$V_{IN} = 9.0$ V, $V_{OUT} = -2.0$ V	−350 mA Min.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	−125 mA Min.
			$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	−200 mA Min.
			$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	−250 mA Min.
			$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	−300 mA Min.
			$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	−350 mA Min.
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2956A	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
		UDN-2957A	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 80$ V	50 μA Max.
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	2.0 V Max.
Turn-On Delay	t_{ON}	ALL	0.5 E_{in} to 0.5 E_{out}, $R_L = 400\ \Omega$ $C_T = 25$ pF	4.0 μs Max.
Turn-Off Delay	t_{OFF}	ALL	0.5 E_{in} to 0.5 E_{out}, $R_L = 400\ \Omega$ $C_T = 25$ pF	10 μs Max.

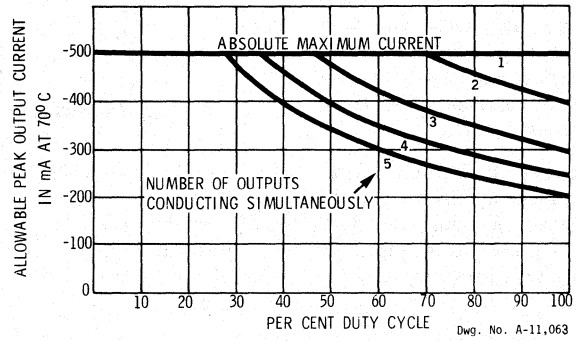
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

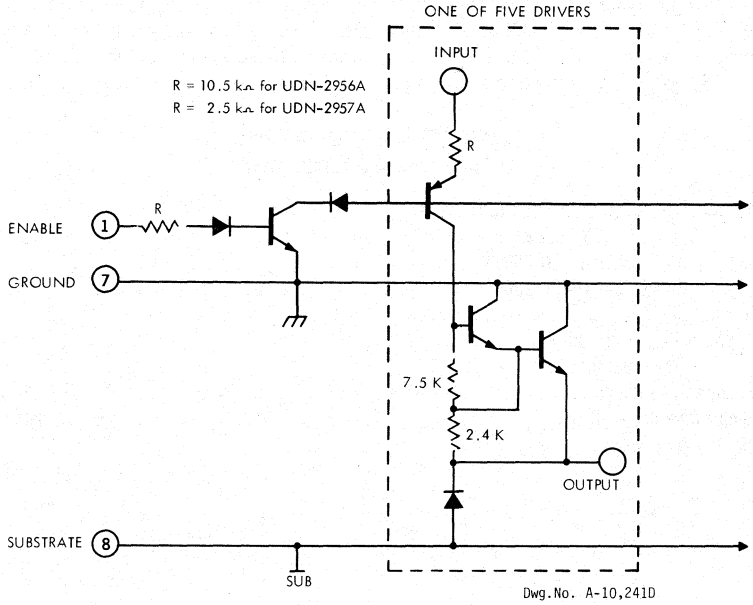




ALLOWABLE PEAK OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



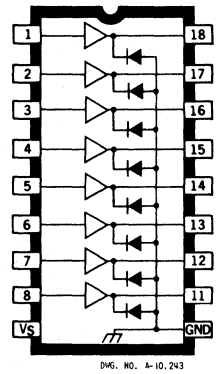




SERIES UDN-2980A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V



DWG. NO. A-10,243

RECOMMENDED for applications requiring separate logic and load grounds, load supply voltage to +80 V, and load currents to 500 mA, Series UDN-2980A source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, and LEDs.

Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. Types UDN-2981A and UDN-2982A will withstand a maximum output OFF voltage of +50 V, while Types UDN-2983A and UDN-2984A will withstand an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

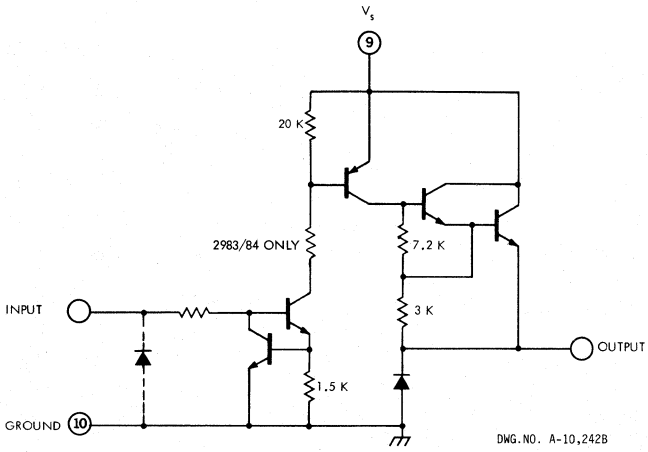
Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line packages. On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

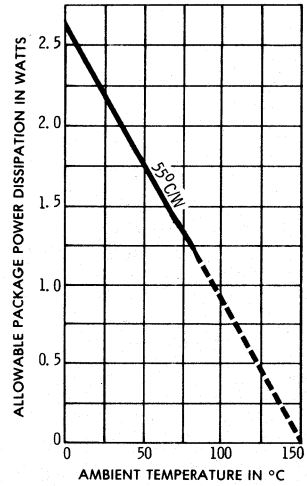
Output Voltage Range, V_{CE} (UDN-2981A & UDN-2982A)	+5 V to +50 V
(UDN-2983A & UDN-2984A)	+35 V to +80 V
Input Voltage, V_{IN} (UDN-2981A & UDN-2983A)	+15 V
(UDN-2982A & UDN-2984A)	+30 V
Output Current, I_{OUT}	−500 mA
Power Dissipation, P_D (any one driver)	1.1 W
(total package)	2.2 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

ONE OF EIGHT DRIVERS



POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,112A

3

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Test Fig.	Limit Min.	Limit Typ.	Limit Max.	Units
Output Leakage Current	I_{CEX}	UDN-2981/82A	V_{IN} = 0.4 V*, V_S = 50 V, T_A = +70°C	1	—	—	200	μA
		UDN-2983/84A	V_{IN} = 0.4 V*, V_S = 80 V, T_A = +70°C	1	—	—	200	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	V_{IN} = 2.4 V, I_{OUT} = −100 mA	2	—	1.6	1.8	V
			V_{IN} = 2.4 V, I_{OUT} = −225 mA	2	—	1.7	1.9	V
			V_{IN} = 2.4 V, I_{OUT} = −350 mA	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	UDN-2981/83A	V_{IN} = 2.4 V	3	—	140	200	μA
			V_{IN} = 3.85 V	3	—	310	450	μA
		UDN-2982/84A	V_{IN} = 2.4 V	3	—	140	200	μA
			V_{IN} = 12 V	3	—	1.25	1.93	mA
Output Source Current	I_{OUT}	UDN-2981/83A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	−350	—	—	mA
		UDN-2982/84A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	−350	—	—	mA
Supply Current (Outputs Open)	I_S	UDN-2981/82A	V_{IN} = 2.4 V*, V_S = 50 V	4	—	—	10	mA
		UDN-2983/84A	V_{IN} = 2.4 V*, V_S = 80 V	4	—	—	10	mA
Clamp Diode Leakage Current	I_R	UDN-2981/82A	V_R = 50 V, V_{IN} = 0.4 V*	5	—	—	50	μA
		UDN-2983/84A	V_R = 80 V, V_{IN} = 0.4 V*	5	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	1.0	2.0	μs
Turn-Off Delay	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	5.0	10	μs

*All Inputs Simultaneously

TEST FIGURES

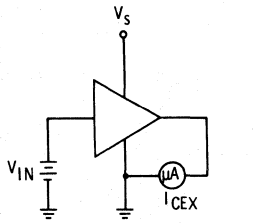


Figure 1

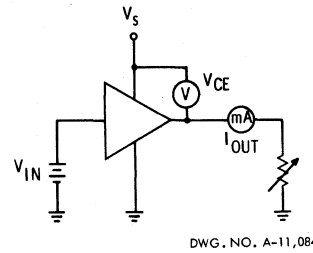


Figure 2

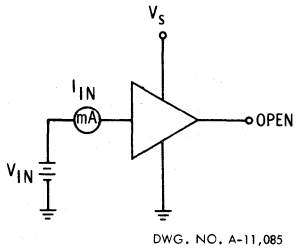


Figure 3

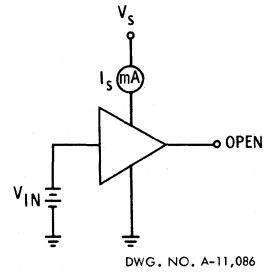


Figure 4

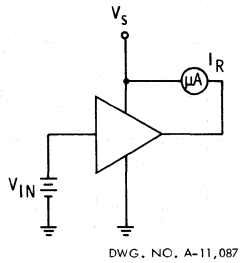


Figure 5

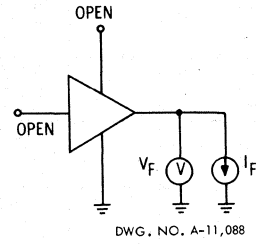
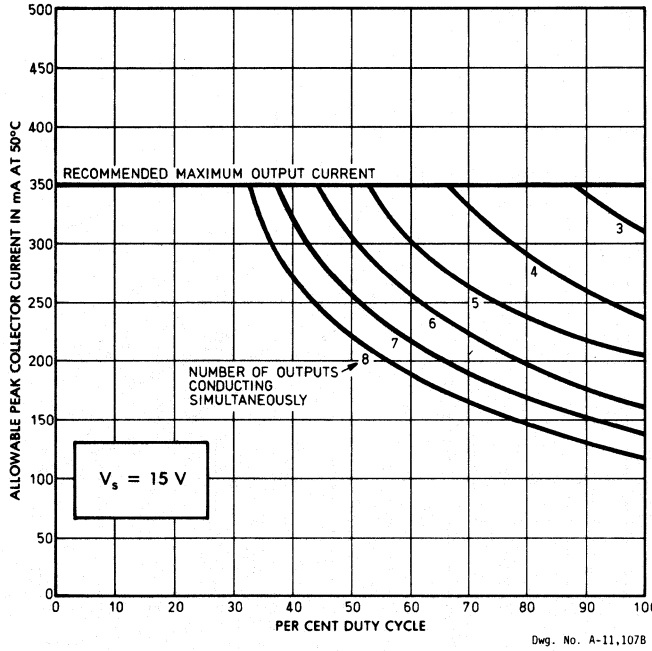
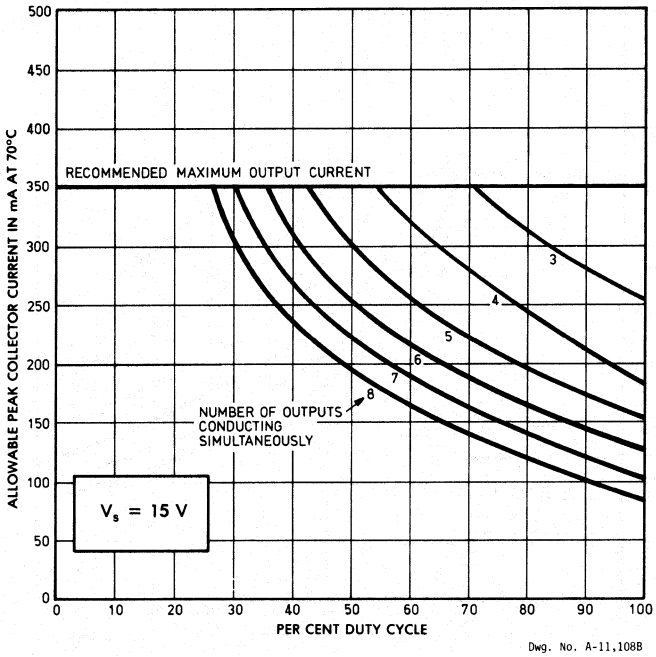


Figure 6

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE TYPE UDN-2981A/82A

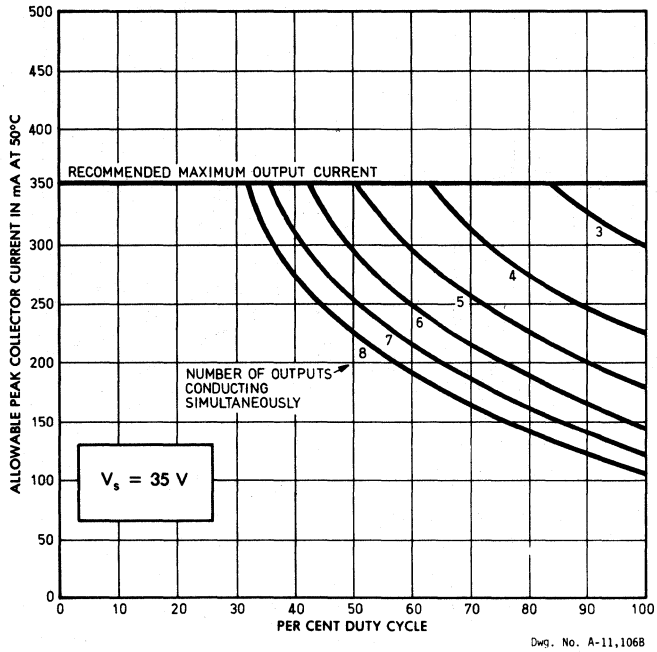


Dwg. No. A-11,107B



Dwg. No. A-11,108B

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE SERIES UDN-2980A



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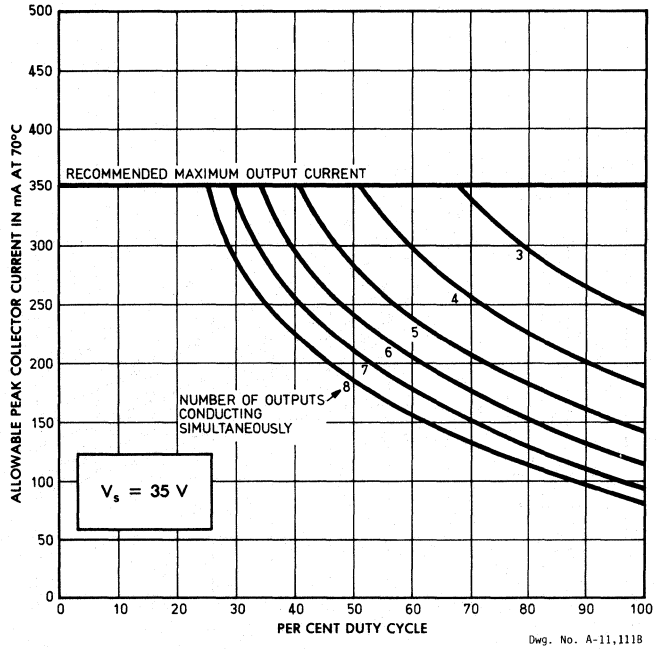
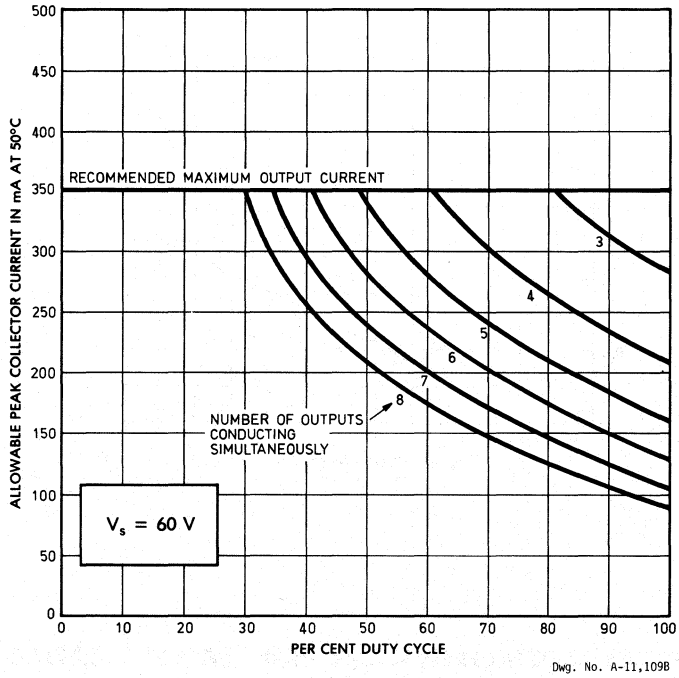
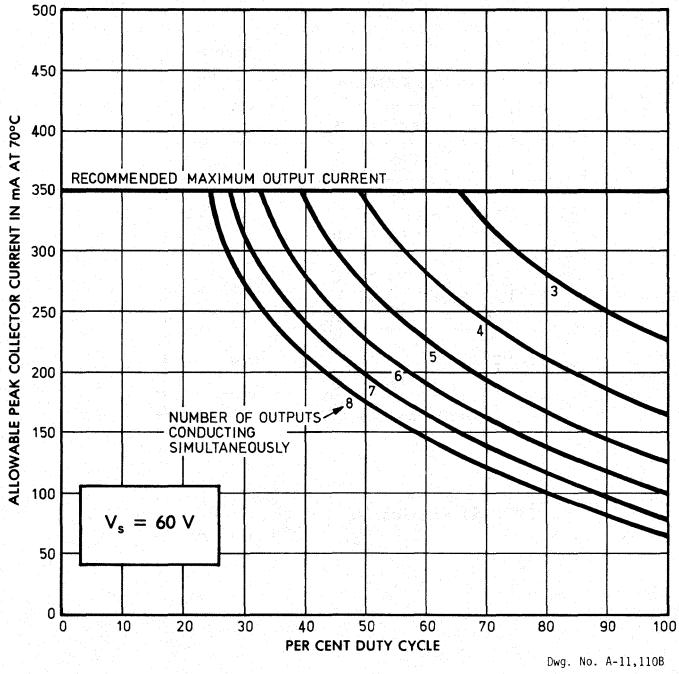


Dwg. No. A-11,111B

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE TYPES UDN-2983A/84A

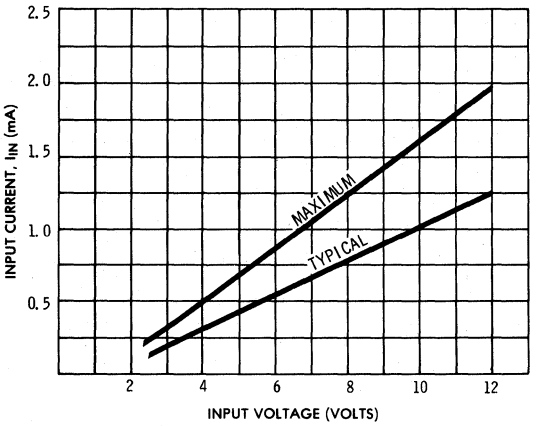


Dwg. No. A-11,109B



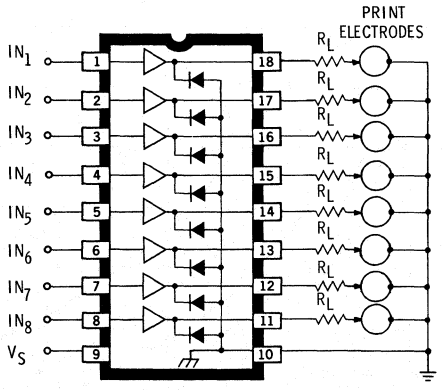
Dwg. No. A-11,110B

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg. No. A-11,115B

TYPICAL ELECTROSENSITIVE PRINTER APPLICATION



Dwg. No. A-11,113A

TYPICAL VALUES: V_S = 50 V
I_{OUT} = 200-300 mA

UDN-2985A AND UDN-2986A
8-CHANNEL SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 250 mA Output Source Current Capability
- Output Transient-Suppression Diodes
- 30 V Minimum Output Breakdown Voltage
- Low Output-Saturation Voltage

Recommended for applications requiring separate logic and load grounds, load supply voltages to 30 V, and load currents to 250 mA, the UDN-2985A and UDN-2986A source drivers are used as interface between standard low-power digital logic and LEDs, relays and solenoids. The outputs feature saturated transistors for low collector-emitter saturation voltages.

The UDN-2985A driver is for use with 5 V logic systems—TTL, Schottky TTL, DTL, and CMOS. The UDN-2986A is intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. Both devices have a minimum output breakdown rating of 30 V with a minimum output sustaining voltage of 15 V. In all cases, the output is switched ON by an active high input level.

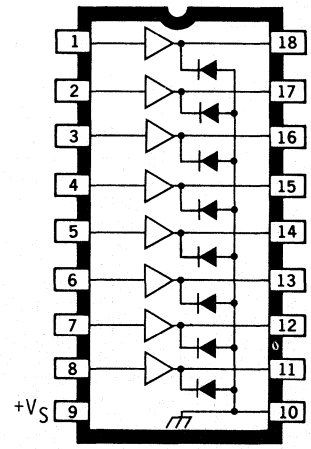
Under normal operating conditions, these devices can source up to 120 mA for each of the eight outputs at an ambient temperature of 75°C and a supply voltage of 15 V. Both devices incorporate input current-limiting resistors and output transient suppression diodes.

The UDN-2985A and UDN-2986A source drivers are supplied in 18-lead dual in-line packages. All inputs are on one side of the package, output pins on the other, to simplify printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS
at $T_A = 25°C$

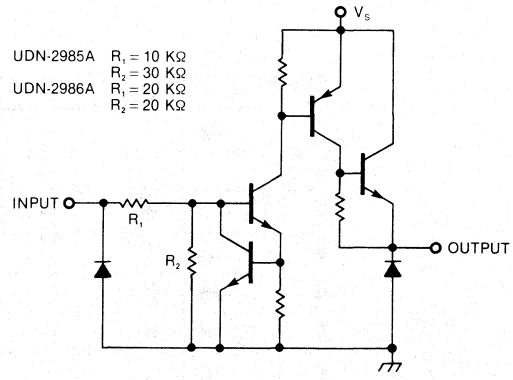
Driver Supply Voltage, V_S . . . . . 30 V
Continuous Output Current, I_{OUT} . . . . . −250 mA
Input Voltage, V_{IN} . . . . . 20 V
Package Power Dissipation, P_D . . . . . 2.2 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Derate at the rate of 18 mW/°C above $T_A = 25°C$



Dwg. No. A-10, 243

PARTIAL SCHEMATIC DIAGRAM
1 of 8 Drivers



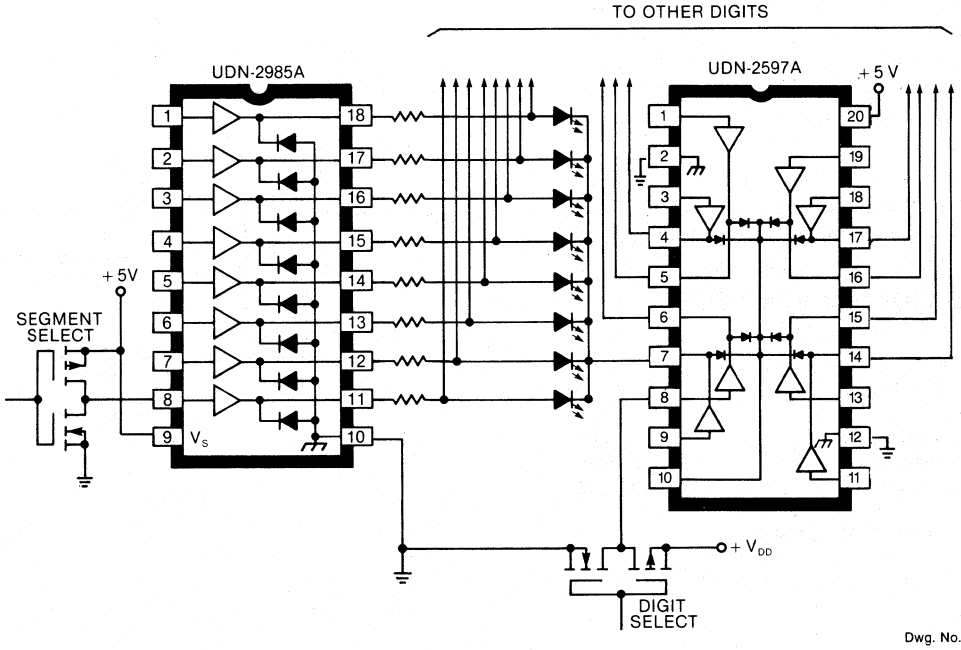
Dwg. No. DS-1013

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$, $V_S = 30V$ (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	Both	$V_{IN} = 0.4$ V, $V_{OUT} = 0$ V	–	<–1.0	–100	μA
Output Sustaining Voltage	$V_{CE(sus)}$	Both	$I_{OUT} = -120$ mA, L = 3 mH	15	–	–	V
Output Saturation Voltage	$V_{CE(SAT)}$	UDN-2985A	$V_{IN} = 2.4$ V, $I_{OUT} = -60$ mA	–	0.8	1.1	V
			$V_{IN} = 2.4$ V, $I_{OUT} = -120$ mA	–	0.9	1.2	V
		UDN-2986A	$V_{IN} = 4.0$ V, $I_{OUT} = -60$ mA	–	0.8	1.1	V
			$V_{IN} = 4.0$ V, $I_{OUT} = -120$ mA	–	0.9	1.2	V
Input Current	$I_{IN(ON)}$	UDN-2985A	$V_{IN} = 2.4$ V	–	90	225	μA
			$V_{IN} = 5.0$ V	–	280	650	μA
		UDN-2986A	$V_{IN} = 4.0$ V	–	90	250	μA
			$V_{IN} = 15$ V	–	450	1150	μA
	$I_{IN(OFF)}$	Both	$V_{IN} = 0.4$ V	–	10	15	μA
Supply Current (outputs open)	I_S	Both	$V_S = 30$ V, $V_{IN} = 2.4$ V	–	10	15	mA
Clamp Diode Leakage Current	I_R	Both	$V_R = 30$ V, $T_A = 70°C$	–	<1.0	50	μA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 120$ mA	–	1.1	2.0	V
Turn-On Delay	t_{ON}	Both		–	0.5	1.0	μs
Turn-Off Delay	t_{OFF}	Both		–	5.0	10	μs

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

COMMON-CATHODE LED DRIVER

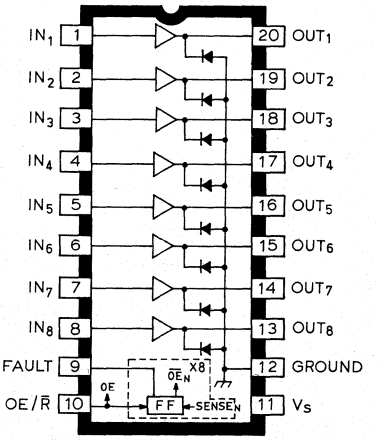


Dwg. No. DS-1014A

UDN-2987A
8-CHANNEL SOURCE DRIVER
With Over-Current Protection

FEATURES

- 350 mA Output Source Current
- Over-Current Protected
- Internal Ground Clamp Diodes
- Output Breakdown Voltage 35 V, Minimum
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Internal Thermal Shutdown



Dwg. No. A-13,285

Providing over-current protection for each of its eight sourcing outputs, the UDN-2987A driver is used as an interface between standard low-level logic and relays, motors, solenoids, LEDs and incandescent lamps. The device includes thermal shutdown and output transient protection/clamp diodes for use with sustaining voltages to 35 V.

In this driver, each channel includes a latch to turn OFF that channel if the maximum channel current is exceeded. All channels are disabled if the thermal shutdown is activated. A common FAULT output is used to indicate either chip thermal shutdown or any over-current condition. All outputs are enabled by pulling the common OE/R input high. When OE/R is low, all outputs are inhibited and the eight latches are reset. The UDN-2987A is supplied in a 20-lead dual in-line plastic package.

Under normal operating conditions each of eight outputs will source in excess of 100 mA continuously at an ambient temperature of 25°C and a supply of 35 V. The over-current fault circuit will protect the device from short-circuits to ground with supply voltages of up to 35 V.

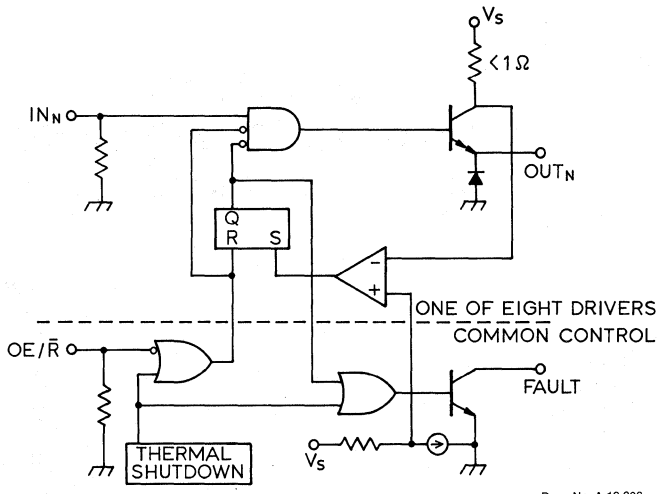
The inputs are compatible with 5 V and 12 V logic systems—TTL, Schottky TTL, DTL, PMOS, and CMOS. In all cases, the output is switched ON by an active high input level.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Driver Supply Voltage, V_S	35 V
Output Sustaining Voltage, $V_{CE(SUS)}$	35 V
Continuous Output Current, I_{OUT}	−500 mA*
FAULT Output Voltage, V_{CE}	50 V
FAULT Output Current, I_C	30 mA
Input Voltage, V_{IN}	15 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

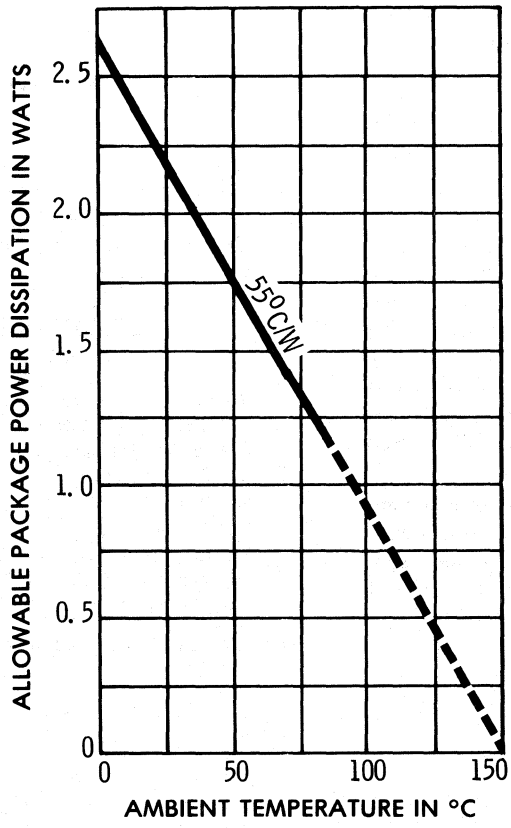
*Outputs are disabled at approximately −500 mA per driver.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,286

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,112A

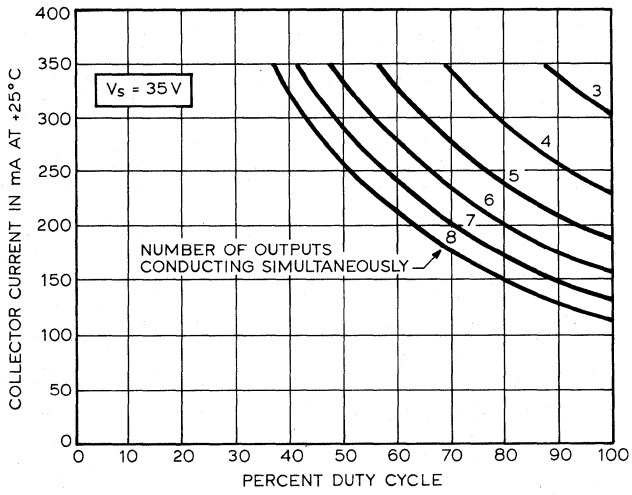
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{OE} = 2.4 V, V_S = 35 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Functional Supply Range	V_S		7.0	—	35	V
Output Leakage Current	I_{CEX}	V_{IN} = 0.4 V*	—	< −5	−200	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = −350 mA, L = 2.0 mH	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{IN} = 2.4 V, I_{OUT} = −100 mA	—	1.6	1.8	V
		V_{IN} = 2.4 V, I_{OUT} = −225 mA	—	1.7	1.9	V
		V_{IN} = 2.4 V, I_{OUT} = −350 mA	—	1.8	2.0	V
Channel Shutdown Threshold	I_M	V_{IN} = 2.4 V	−400	−500	—	mA
FAULT Leakage Current	I_{CEX}	V_{CC} = 35 V	—	<1.0	100	µA
FAULT Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 mA	—	0.3	0.8	V
Input Voltage	$V_{IN(ON)}$		2.4	—	—	V
	$V_{IN(OFF)}$		—	—	0.4	V
Input Current	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	125	170	µA
		V_{IN} = 5.0 V	—	840	1020	µA
		V_{IN} = 12 V	—	1500	1800	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	—	15	µA
Clamp Diode Leakage Current	I_R	V_R = 35 V, T_A = 70°C	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.5	1.8	V
Supply Current	$I_{S(ON)}$	V_{IN} = 2.4 V*, Outputs Open	—	13	18	mA
	$I_{S(OFF)}$	V_{IN} = 0.4 V*	—	8.0	12	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	T_J		—	15	—	°C
Propagation Delay Time	t_{PLH}	R_L = 100Ω	—	0.3	0.6	µs
	t_{PHL}	R_L = 100Ω	—	2.0	4.0	µs
Dead Time	t_d		—	1.0	—	µs

*All inputs simultaneously.

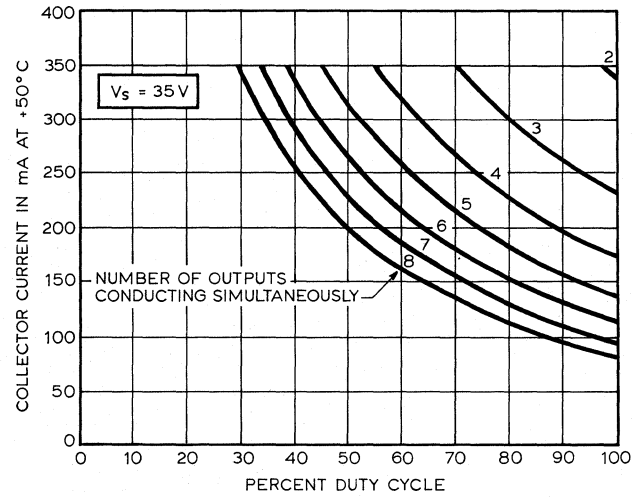
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

AT +25°C



Dwg. No. A-13,288

AT +50°C



Dwg. No. A-13,289

APPLICATIONS INFORMATION AND CIRCUIT DESCRIPTION

As with all power integrated circuits, the UDN-2987A has a maximum allowable output current rating. The 500 mA rating does not imply that operation at that value is permitted or even obtainable. The channel output current trip point is specified as −400 mA, minimum; therefore, attempted operation at current levels greater than −400 mA may cause a fault indication and channel shutdown. The device is tested at a maximum of −350 mA and that is the recommended maximum output current per driver. It provides protection for current overloads or shorted loads up to 35 V.

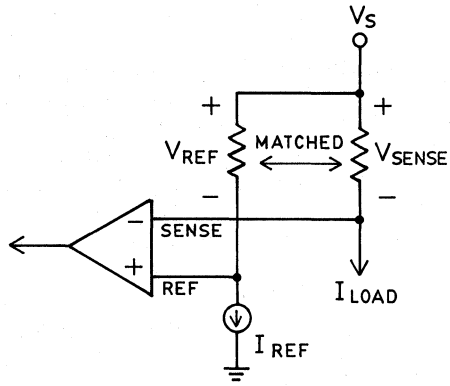
All outputs are enabled by pulling the OE/R input high. When OE/R is low or allowed to float (internal pull-down), all outputs are inhibited and the latches are reset. The latches are also reset during power-up, regardless of the state of the OE/R input.

The load current causes a small voltage drop across the internal low-value sense resistor. This voltage is compared to the voltage drop across a reference resistor with a constant current. The two resistors are matched to eliminate errors due to manufacturing tolerances or temperature effects. Each channel includes a comparator and its own latch. An over-current fault ($V_{SENSE)} > V_{REF}$) will set the affected latch and shut down only that channel. All other channels will continue to operate normally. The latch includes a 1 μs delay (t_d) to prevent unwanted triggering due to crossover currents generated when switching inductive loads. For an abrupt short circuit, the delay and output switching times will allow a brief, permissable current in excess of the trip current before the output driver is turned OFF.

A common thermal shutdown disables all outputs if the chip temperature exceeds +165°C. At thermal shutdown, all latches are reset. The outputs are disabled until the chip cools down to about +150°C (thermal hysteresis).

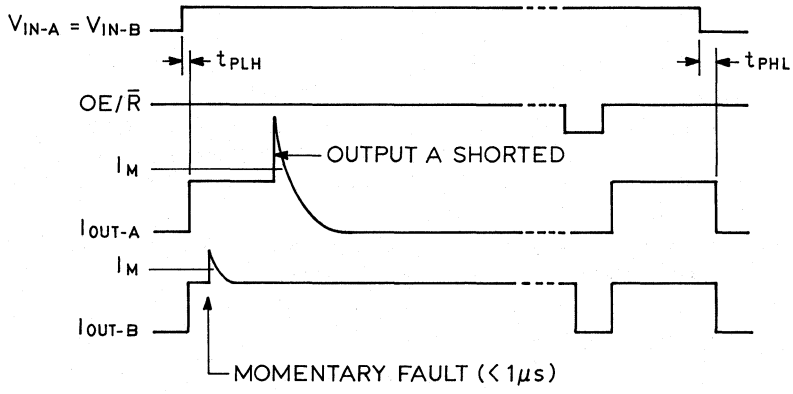
A common open-collector FAULT output is used to indicate any channel over-current condition or chip thermal shutdown.

OVER-CURRENT FAULT SENSE



Dwg. No. A-13,292

OUTPUT CURRENT WAVESHAPES

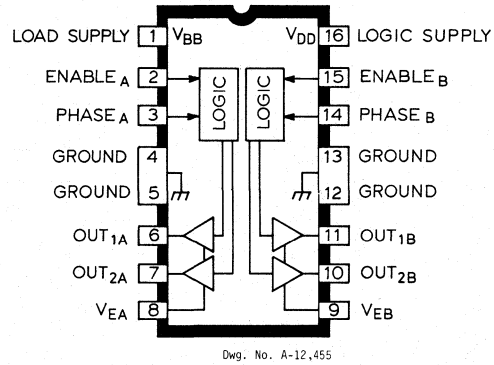


Dwg. No. A-13,293

UDN-2993B
DUAL H-BRIDGE MOTOR DRIVER

FEATURES

- ± 600 mA Output Current
- Output Voltage to 40 V
- Crossover Current Protection
- TTL/NMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- Plastic DIP With Heat-Sink Tabs (Machine Insertable)



Dwg. No. A-12,455

BRUSHLESS D-C or bipolar stepper motors to 40 V and 500 mA per phase are economically driven with the Type UDN-2993B dual H-bridge driver. Each of the pair of full-bridge drivers has separate input level shifting, internal logic, source and sink drivers in an H-bridge configuration, and internal clamp diodes.

The device provides an internally-generated deadtime to prevent crossover currents during changes in load-current phase. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Except for supply voltages, the two H-bridges are independent. The ENABLE function is provided for each bridge to allow pulse-width (chopper) modulation with the use of external comparators. The chopper-drive mode is characterized by low power-dissipation levels and maximum efficiency.

A PHASE input to each bridge determines load-current direction. In addition, the emitters from each bridge are externally available to allow the addition of current-sensing circuitry.

The Type UDN-2993B integrated circuit is supplied in a 16-pin dual in-line plastic package with a copper lead frame for optimum power dissipation without a heat sink. The lead configuration allows automatic insertion, fits a standard integrated circuit socket or printed wiring board layout, and enables easy attachment of a heat sink for maximum power-handling capability. The heat-sink tabs are at ground potential and require no insulation.

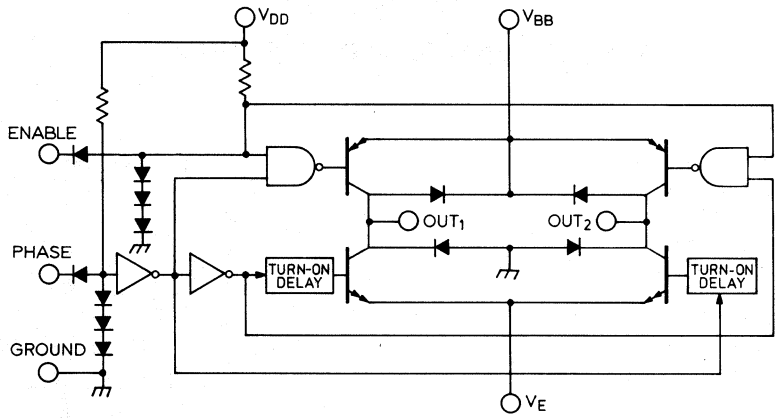
A full-bridge bipolar driver with a current rating of ±3.5 A is supplied as Type UDN-2952B. It is described in Sprague Engineering Bulletin 29319.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

Load Supply Voltage, V_{BB}	40 V
Logic Supply Voltage, V_{DD}	7.0 V
Logic Input Voltage Range, V_{PHASE} or V_{ENABLE}	−0.3 V to V_{DD} + 0.3 V
Output Current, I_{OUT}	±600 mA
Sink Driver Emitter Voltage, V_E	1.5 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

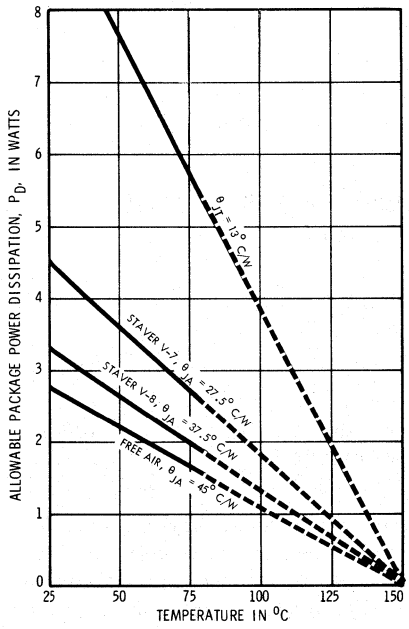
NOTE: Output current rating may be limited by chopping frequency, ambient temperature, air flow, and heat sinking. Under any set of conditions, do not exceed the specified maximum current and a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. A-12,447

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,793A

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.

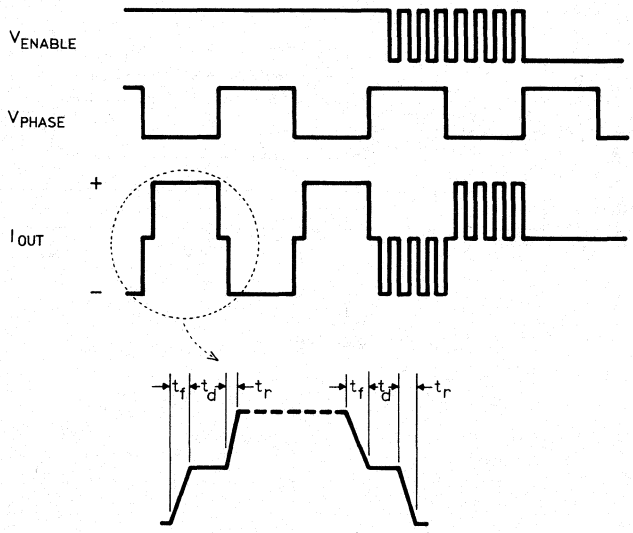
TRUTH TABLE

Enable Input	Phase Input	Output 1	Output 2
High	High	Low	High
High	Low	High	Low
Low	High	Low	Open
Low	Low	Open	Low

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 40\,V$, $V_{DD} = 5\,V$, $V_E = 0\,V$, $T_{TAB} \leq +70°C$ Figure 1 (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	40	V
Output Leakage Current	I_{CEX}	$V_{ENABLE} = 0.8\,V$, $V_{OUT} = V_{BB}$, Note 2	—	<1.0	10	µA
		$V_{ENABLE} = 0.8\,V$, $V_{OUT} = 0\,V$, Note 2	—	< −1.0	−10	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{ENABLE} = 2.4\,V$, $I_{OUT} = 500\,mA$	—	1.6	1.8	V
		$V_{ENABLE} = 2.4\,V$, $I_{OUT} = -500\,mA$	—	1.6	2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = \pm 500\,mA$, Figure 2, Note 2	40	50	—	V
Motor Supply Current	$I_{BB(ON)}$	$V_{ENABLE} = 2.4\,V$, Outputs Open, Note 2	—	1.0	3.0	mA
	$I_{BB(OFF)}$	$V_{ENABLE} = 0.8\,V$, Outputs Open, Note 2	—	<1.0	10	µA
Source Driver Rise Time	t_r	$I_{OUT} = -500\,mA$, $V_{BB} = 30\,V$	—	75	—	ns
Source Driver Fall Time	t_f	$I_{OUT} = -500\,mA$, $V_{BB} = 30\,V$	—	280	—	ns
Deadtime	t_d	$I_{OUT} = \pm 500\,mA$, $V_{BB} = 30\,V$	—	1.5	—	µs
Clamp Diode Forward Voltage	V_F	$I_F = 500\,mA$	—	1.6	1.8	V
Control Logic (PHASE or ENABLE)						
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or $V_{ENABLE} = 2.4\,V$	—	<1.0	10	µA
	$I_{IN(0)}$	V_{PHASE} or $V_{ENABLE} = 0.8\,V$	—	−200	−300	µA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	14	20	mA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	250	—	ns
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	500	—	ns

NOTES: 1. Each driver is tested separately.
2. Test is performed with $V_{PHASE} = 0.8\,V$ and then repeated for $V_{PHASE} = 2.4\,V$.
3. Negative current is defined as coming out of (sourcing) the specified device pin.



Dwg. No. A-12,448

TEST FIGURES

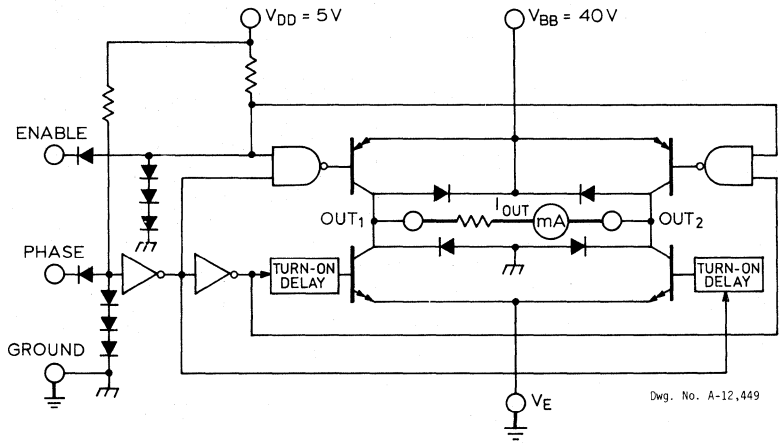


FIGURE 1

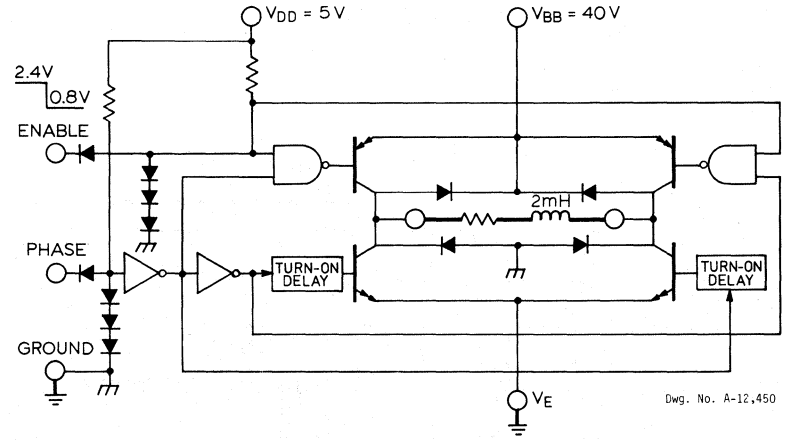
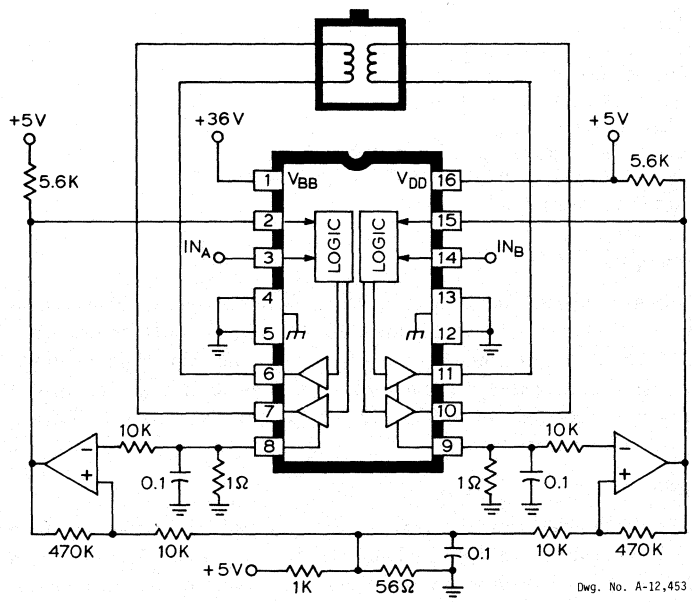
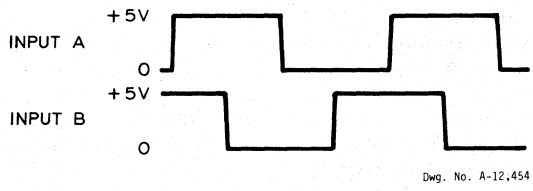


FIGURE 2

TYPICAL APPLICATION

2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)





SERIES UDN-3610M
DUAL 2-INPUT PERIPHERAL/POWER DRIVERS

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V
- Pin-for-Pin Replacement for Series LM3600N
- Pin-for-Pin Replacement for SN75451BP through SN75454BP and 75461 through 75464

Description

THESE MINI-DIP dual 2-input peripheral power drivers are bipolar monolithic integrated circuits with AND, NAND, OR, or NOR logic gates and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-3600M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, heaters, and other non-inductive loads of up to 600 mA (both drivers in parallel).

With appropriate external-diode transient-suppression, Series UDN-3600M drivers can also be used with inductive loads such as relays, solenoids, and stepping motors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	80 V
Output On-State Sink Current, I_{ON}	600 mA
Power Dissipation, P_D	1.5 W
Each Driver	0.8 W
Derating Factor Above T_A = 25°C	12.5 mW/°C or 80°C/W
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

3

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

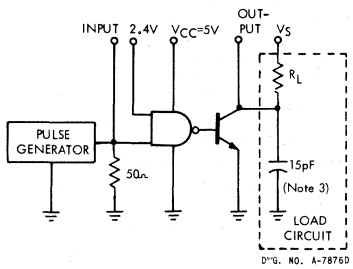
Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

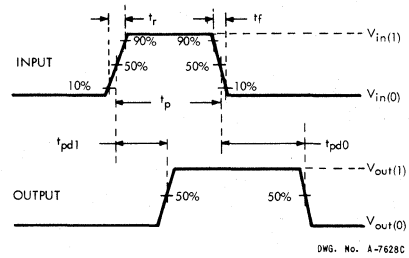
Type UDN-3611M Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	100 mA		0.25	0.4	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



DWG. NO. A-7876D



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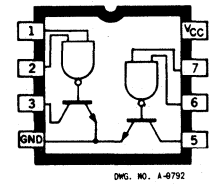
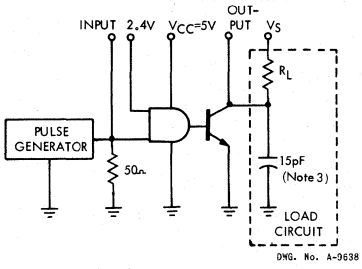


DWG. NO. A-9792

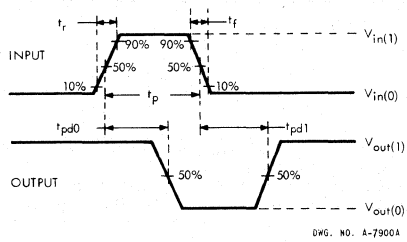
Type UDN-3612M Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

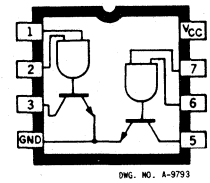
Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	100 mA		0.25	0.4	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	14	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2



DWG. No. A-9638



DWG. NO. A-7900A



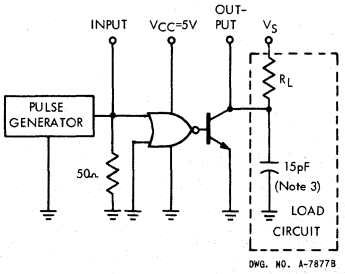
DWG. NO. A-9793

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

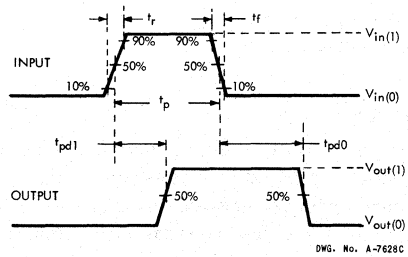
Type UDN-3613M Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	100 mA		0.25	0.4	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2



DWG. NO. A-7877B



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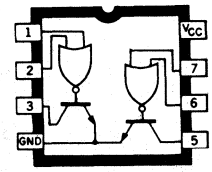


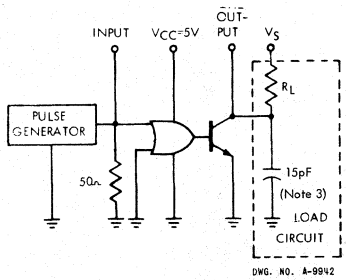
DWG. NO. A-9795

3

Type UDN-3614M Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	100 mA		0.25	0.4	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2



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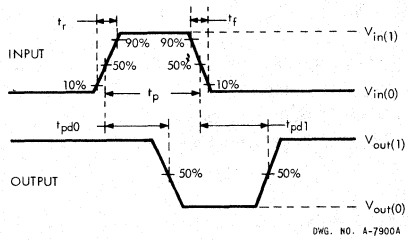

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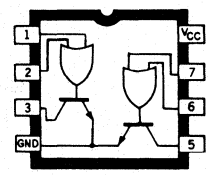


DWG. NO. A-9794

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5700A
QUAD 2-INPUT PERIPHERAL/POWER DRIVERS
—Transient-Protected Outputs

FEATURES:

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Description

THESE 16-LEAD QUAD 2-input peripheral and power drivers are bipolar monolithic integrated circuits containing AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-5700A quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need of discrete diodes. For non-inductive loads, the diode-common bus can be used for a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	80 V
Output On-State Sink Current, I_{ON}	600 mA
Suppression Diode Off-State Voltage, V_{OFF}	80 V
Suppression Diode On-State Current, I_{ON}	600 mA
Power Dissipation, P_D	2.0 W
Each Driver	0.8 W
Derating Factor Above 25°C	16.7 mW/°C or 60°C/W
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

3

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

		Test Conditions					Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

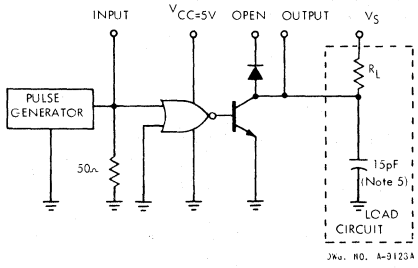
			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465Ω (10 Watts) C_L = 15 pF		300	750	ns	3

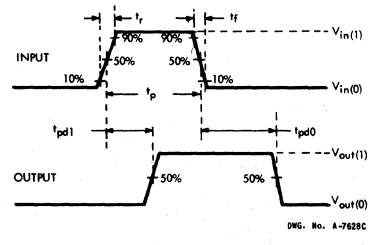
NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

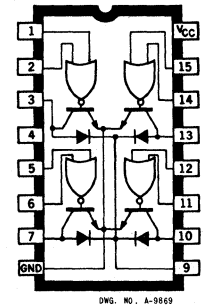
Type UDN-5703A Quad OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			72	100	mA	1, 2



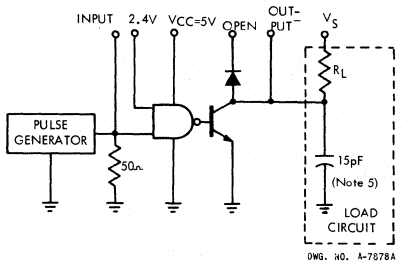


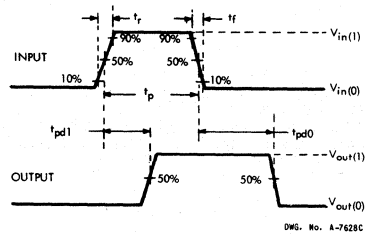


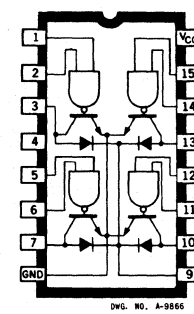
Type UDN-5706A Quad AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			70	98	mA	1, 2





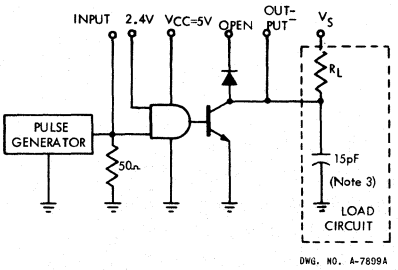


NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

Type UDN-5707A Quad NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	106	mA	1, 2



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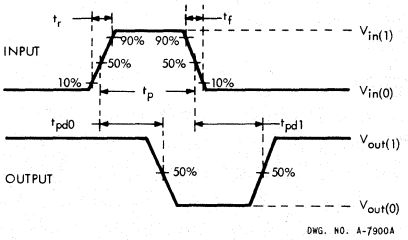

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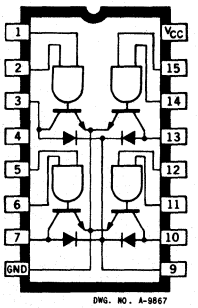
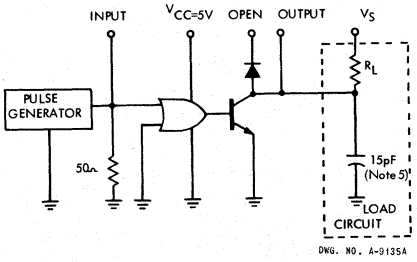


DWG. NO. A-9867

Type UDN-5733A Quad NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	100	mA	1, 2



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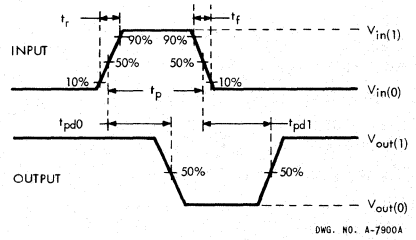

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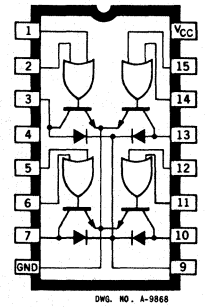


DWG. NO. A-9868

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5710M
DUAL PERIPHERAL/POWER DRIVERS
—Transient Protected Outputs

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Description

THESE MINI-DIP dual peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-5700M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to 600 mA.

The integral transientsuppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode-common bus can be used for the "lamp test" function.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . 7.0 V
Input Voltage, V_{IN} . . . . . 30 V
Output Off-State Voltage, V_{OFF} . . . . . 80 V
Output On-State Sink Current, I_{ON} . . . . . 600 mA
Suppression Diode Off-State Voltage, V_{OFF} . . . . . 80 V
Suppression Diode On-State Current, I_{ON} . . . . . 600 mA
Power Dissipation at T_A = +25°C, P_D . . . . . 1.5 W
  Each Driver . . . . . 0.8 W
  Derating Factor . . . . . 12.5 mW/°C or 80°C/W
Operating Free-Air Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−100	−200	μA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
"1" Input Current at Strobe	$I_{in(1)}$		MAX	30 V	0 V				20	μA	
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

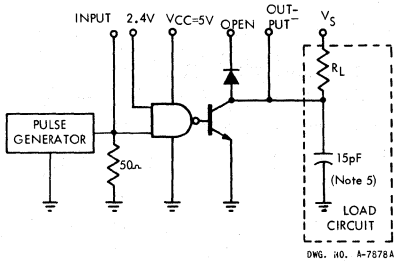
Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

Type UDN-5711M Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



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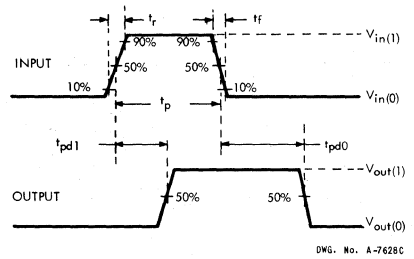

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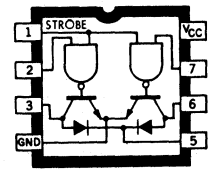
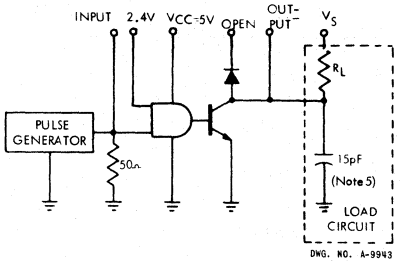


DWG. NO. A-9791

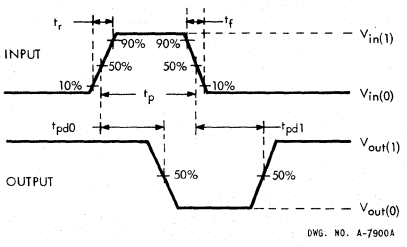
Type UDN-5712M Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

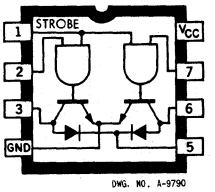
Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2



DWG. NO. A-9943



DWG. NO. A-7900A



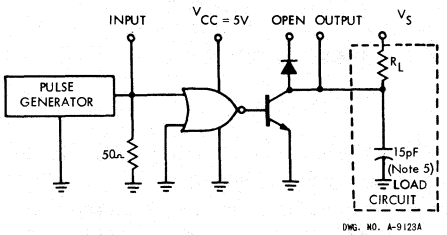
DWG. NO. A-9790

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA
5. Capacitance values specified include probe and test fixture capacitance.

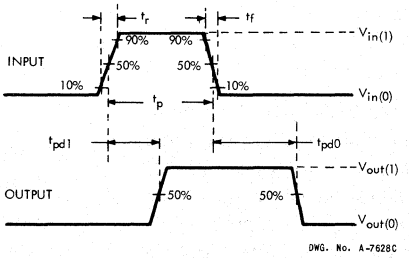
Type UDN-5713M Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2



DWG. NO. A-9123A



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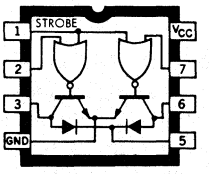
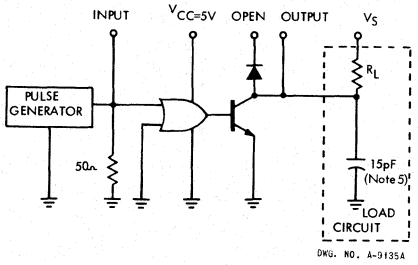


DWG. NO. A-9789

Type UDN-5714M Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2



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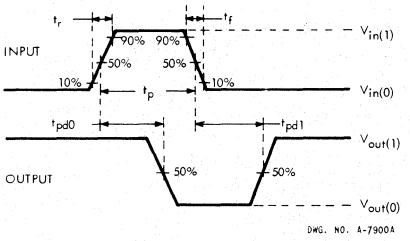

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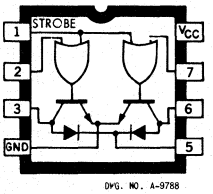


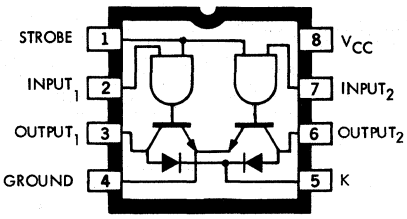
DWG. NO. A-9788

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5720M, UDN-5740M, UDN-5750M
DUAL PERIPHERAL/POWER DRIVERS
—Transient-Protected Outputs

FEATURES

- DTL/TTL/PMOS/CMOS Compatible
- Low Input Current
- Continuous Output Current to 700 mA
- 70 V Output Standoff Voltage
- Low Supply-Current Requirement



Dwg. No. A-9790B

UDN-5722/42/52M

PERIPHERAL AND POWER DRIVERS combining dual logic gates, high-current saturated output transistors, and transient-supression diodes are the Series UDN-5720/40/50M. These monolithic dual drivers surpass the interface requirements normally associated with standard logic buffers and are ideally suited for interface between low-level logic and high-current inductive loads. Internal transient-suppression diodes allow their use with loads such as stepping motors, relays, or solenoids. Additional (non-inductive) applications include driving peripheral loads such as light-emitting diodes, memories, heaters, and incandescent lamps with peak load currents of up to 700 mA. When not required for transient suppression, the diode common bus can be used to perform the "lamp test" function.

The Series UDN-5720M output transistors are capable of simultaneously sinking 350 mA continuously over the rated operating temperature range. The Series UDN-5740M is capable of sinking 600 mA continuously for a single output (57% duty cycle for both outputs). The series UDN-5750M will sink 500 mA continuously for a single output (86% duty cycle for both outputs). The outputs may be paralleled for higher load-current capability. In the OFF state, the drivers will withstand at least 70 V.

All devices in this series are supplied in a miniature 8-pin dual-in-line plastic package with a copper lead frame for superior package power dissipation ratings.

ABSOLUTE MAXIMUM RATINGS

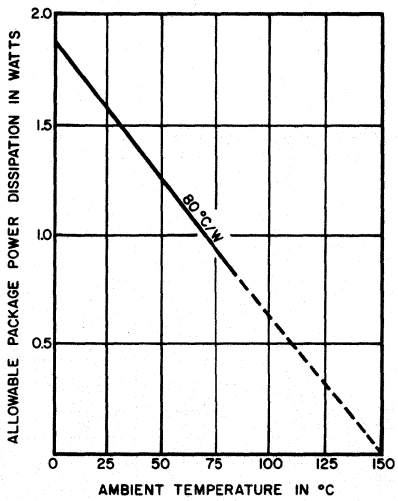
Supply Voltage, V_{CC} (UDN-5740/50M)	7.0 V
(UDN-5720M)	15 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	70 V
Output On-State Sink Current, I_{ON} (UDN-5720/50M)	600 mA
(UDN-5740M)	700 mA
Suppression Diode Off-State Voltage, V_{OFF}	70 V
Suppression Diode On-State Current, I_{ON} (UDN-5720/50M)	600 mA
(UDN-5740M)	700 mA
Allowable Package Power Dissipation, P_D	1.5 W*
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 12.5 mW/°C above T_A = +25°C

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC} (UDN-5720M)	4.75	—	12.6	V
(UDN-5740/50M	4.75	5.00	5.25	V
Output Current, I_{ON} (UDN-5720M)	—	—	350	mA
(UDN-5740M)	—	—	600	mA
(UDN-5750M)	—	—	500	mA
Operating Temperature Range	0	+25	+85	°C

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-13,220

SWITCHING CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 5.0$ V

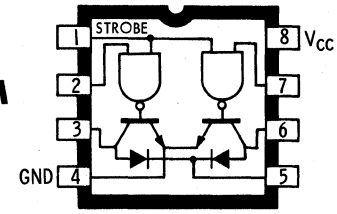
Characteristic	Symbol	Test Conditions	Limits			Notes
			Min.	Max.	Units	
Turn-On Delay Time	$t_{pd\,0}$	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	500	ns	1, 2
Turn-Off Delay Time	$t_{pd\,1}$	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	750	ns	1, 2

Notes: 1. Capacitance value specified includes probe and test fixture capacitance.
2. Voltage values shown in test circuit waveforms are with respect to network ground.

Input-Pulse Characteristics

$V_{IN(0)}$ = 0 V	$t_f \leq 7$ ns	t_p = 1 μs
$V_{IN(1)}$ = 3.5 V	$t_r \leq 14$ ns	PRR = 500kHz

UDN-5721M, UDN-5741M, UDN-5751M

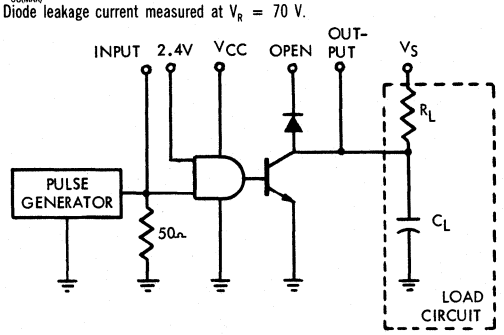


Dwg. No. A-9791A

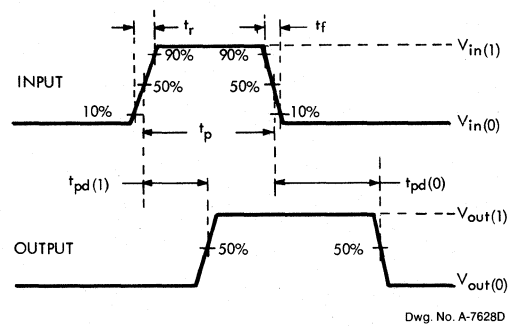
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{CEX}	—	All	4.75	2.0 V	2.0 V	70 V	—	—	100	µA	—
				Open	2.0 V	2.0 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5721	4.75	0.8 V	4.75 V	200 mA	—	0.4	0.6	V	—
			5741/51	4.75	0.8 V	4.75 V	300 mA	—	0.3	0.6	V	—
			5721	4.75	0.8 V	4.75 V	350 mA	—	0.6	0.8	V	—
			5751	4.75	0.8 V	4.75 V	500 mA	—	0.5	0.8	V	—
			5741	4.75	2.0 V	4.75 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	5.0	0 V	0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5721	5.0	5.0 V	5.0 V	300 mA	—	1.5	1.75	V	—
			5751	5.0	5.0 V	5.0 V	500 mA	—	1.5	2.0	V	—
			5741	5.0	5.0 V	5.0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5721	5.25	5.0 V	5.0 V	—	—	1.0	2.0	mA	—
				12.6	5.0 V	5.0 V	—	—	2.6	4.0	mA	—
			5741/51	5.25	5.0 V	5.0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5721	5.25	0 V	0 V	—	—	13	16	mA	—
				12.6	0 V	0 V	—	—	38	45	mA	—
			5741/51	5.25	0 V	0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5721M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.

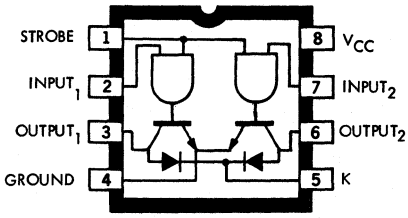


Dwg. No. A-11,746A



Dwg. No. A-7628D

UDN-5722M, UDN-5742M, UDN-5752M

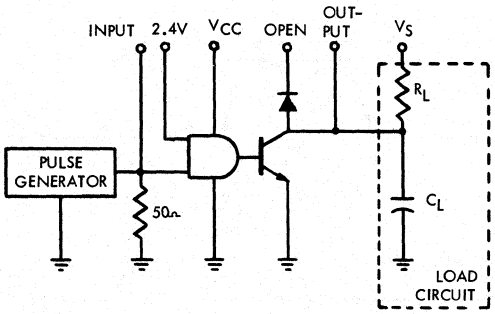


Dwg. No. A-9790B

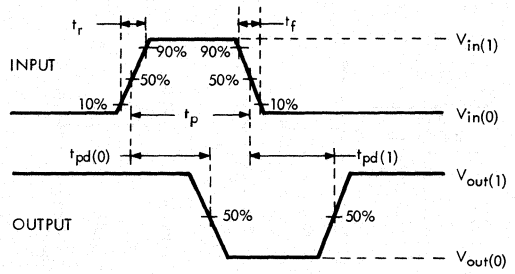
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{CEX}	—	All	4.75	0.8 V	4.75 V	70 V	—	—	100	µA	—
				Open	0.8 V	4.75 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5722	4.75	2.0 V	2.0 V	200 mA	—	0.4	0.6	V	—
			5742/52	4.75	2.0 V	2.0 V	300 mA	—	0.3	0.6	V	—
			5722	4.75	2.0 V	2.0 V	350 mA	—	0.6	0.8	V	—
			5752	4.75	2.0 V	2.0 V	500 mA	—	0.5	0.8	V	—
			5742	4.75	2.0 V	2.0 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	5.0	5.0 V	5.0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5722	5.0	0 V	0 V	300 mA	—	1.5	1.75	V	—
			5752	5.0	0 V	0 V	500 mA	—	1.5	2.0	V	—
			5742	5.0	0 V	0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5722	5.25	0 V	0 V	—	—	1.0	2.0	mA	—
				12.6	0 V	0 V	—	—	2.6	4.0	mA	—
			5742/52	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5722	5.25	5.0 V	5.0 V	—	—	13	16	mA	—
				12.6	5.0 V	5.0 V	—	—	38	45	mA	—
			5742/52	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5722M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.

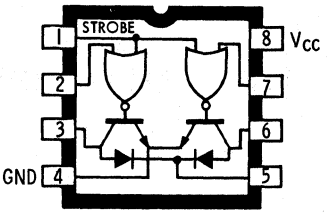


Dwg. No. A-11,746A



Dwg. No. A-7900B

UDN-5723M, UDN-5743M, UDN-5753M

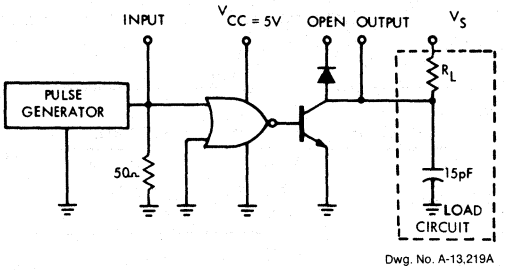


Dwg. No. A-9789A

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions V_{CC}	Test Conditions Driven Input	Test Conditions Other Input	Test Conditions Output	Limits Min.	Limits Typ.	Limits Max	Units	Notes
Output Reverse Current	I_{CEX}	—	All	4.75	2.0 V	0 V	70 V	—	—	100	µA	—
				Open	2.0 V	0 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5723	4.75	0.8 V	0.8 V	200 mA	—	0.4	0.6	V	—
			5743/53	4.75	0.8 V	0.8 V	300 mA	—	0.3	0.6	V	—
			5723	4.75	0.8 V	0.8 V	350 mA	—	0.6	0.8	V	—
			5753	4.75	0.8 V	0.8 V	500 mA	—	0.5	0.8	V	—
			5743	4.75	0.8 V	0.8 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	0	0 V	0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5723	5.0	5.0 V	5.0 V	300 mA	—	1.5	1.75	V	—
			5753	5.0	5.0 V	5.0 V	500 mA	—	1.5	2.0	V	—
			5743	5.0	5.0 V	5.0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5723	5.25	5.0 V	5.0 V	—	—	1.0	2.0	mA	—
				12.6	5.0 V	5.0 V	—	—	2.6	4.0	mA	—
			5743/53	5.25	5.0 V	5.0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5723	5.25	0 V	0 V	—	—	13	16	mA	—
				12.6	0 V	0 V	—	—	38	45	mA	—
			5743/53	5.25	0 V	0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5723M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.



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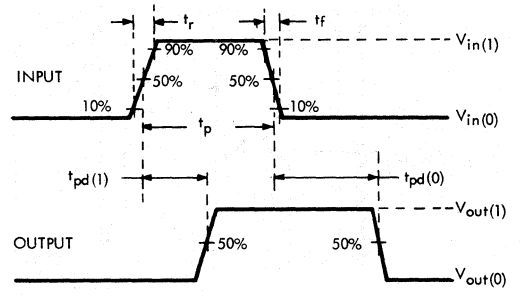

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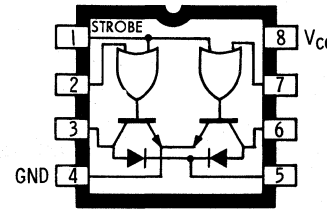
UDN-5724M, UDN-5744M, UDN-5754M

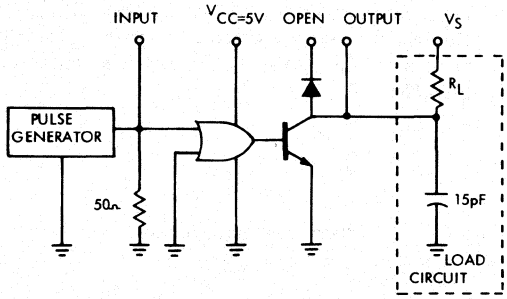


Dwg. No. A-9788A

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{CEX}	—	All	4.75	0.8 V	0.8 V	70 V	—	—	100	µA	—
				Open	0.8 V	0.8 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5724	4.75	2.0 V	0 V	200 mA	—	0.4	0.6	V	—
			5744/54	4.75	2.0 V	0 V	300 mA	—	0.3	0.6	V	—
			5724	4.75	2.0 V	0 V	350 mA	—	0.6	0.8	V	—
			5754	4.75	2.0 V	0 V	500 mA	—	0.5	0.8	V	—
			5744	4.75	2.0 V	0 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	0 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	30 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	0 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	30 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	5.0	5.0 V	5.0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5724	5.0	0 V	0 V	300 mA	—	1.5	1.75	V	—
			5754	5.0	0 V	0 V	500 mA	—	1.5	2.0	V	—
			5744	5.0	0 V	0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5724	5.25	0 V	0 V	—	—	1.0	2.0	mA	—
				12.6	0 V	0 V	—	—	2.6	4.0	mA	—
			5744/54	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5724	5.25	5.0 V	5.0 V	—	—	13	16	mA	—
				12.6	5.0 V	5.0 V	—	—	38	45	mA	—
			5744/54	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5724M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.



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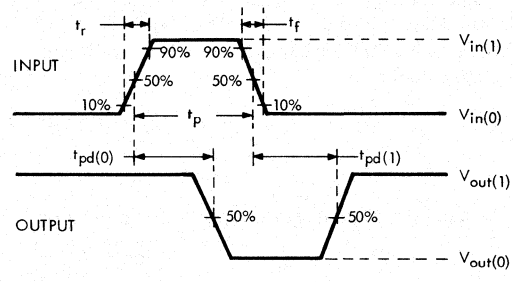

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SERIES ULN-2000A DARLINGTON TRANSISTOR ARRAYS* —Description and Application

Introduction

The increased use of electronic circuits in systems formerly built with mechanical, electro-mechanical, or hydraulic components has resulted in systems becoming more precise, more reliable, generally less expensive, smaller, more efficient, and faster. Although the drive capabilities of monolithic integrated logic circuits are adequate for most information processing applications, there now exists a large and rapidly growing number of system applications where the current-carrying and/or voltage-sustaining capability of the integrated circuit logic is inadequate. Typically, these deficiencies arise when the logic must control such peripheral components as relays, solenoids, punches, stepping motors, and a variety of indicators (incandescent, LED, or gas discharge lamps and displays).

A very common solution to this output interface inadequacy has been the addition of discrete power transistors (or SCRs) and associated passive components to the logic output in order to obtain the necessary current and/or voltage capability. Although this provides a very satisfactory electrical solution, the large number of discrete components often required, high assembly labor costs, and space (packaging) limitations often mean additional problems and cost. A simple, and less expensive solution is the use of monolithic integrated circuits.

The Series ULN-2000A is comprised of four different high-voltage/high-current interface circuits. They are capable of controlling resistive, inductive, or tungsten filament loads of up to 125 watts and are compatible with all standard digital logic families (DTL, TTL, PMOS, and CMOS) without the need for additional discrete components.

High-Voltage and High-Current Capability

A large number of interface problems have been simplified by the Series ULN-2000A high-voltage, high-current Darlington transistor arrays. These devices are suitable for voltage, current, and gain levels beyond the limits of other monolithic buffers and arrays.

The four devices in the ULN-2000A series are all comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for use with inductive loads.

All devices have an output sink current capability of 500 mA although peak inrush currents to 600 mA are permissible, making them ideal for use with tungsten filament lamps. All of the outputs will sustain "OFF" voltages of at least 50 volts. Each individual Darlington circuit may therefore switch up to 25 watts (50 V at 500 mA).

A definite asset of monolithic device technology is the very fine match between adjacent outputs when used in parallel. Applications requiring a sink current beyond the capability of a single output can be accommodated by parallel outputs. Continuous operation of all outputs at the maximum rated current is not allowed because of power dissipation limitations imposed by the package. However, as illustrated in Figure 1, under certain conditions, the Series ULN-2000A Darlington arrays are capable of switching loads totaling more than 125 watts at an ambient temperature of +70°C.

*Examples and data in this application note apply equally to Series ULN-2800A Darlington arrays.

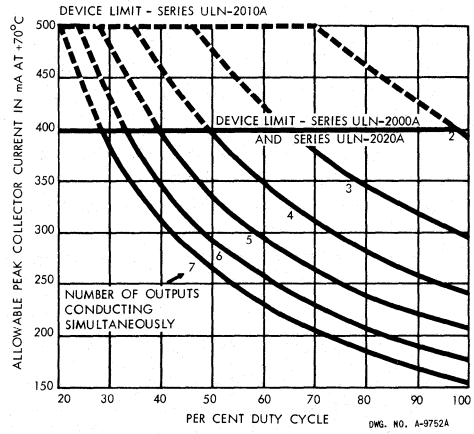


Figure 1

COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS

3

High-Power Capability

A primary limitation of many interface circuits is the power dissipation of the device package. Until recently, very little concern was expressed for monolithic integrated circuit power dissipation. Improvements in silicon device technology have brought about a growing number of monolithic circuits capable of power considerably in excess of present package technology.

The Series ULN-2000A is supplied in a 16-pin dual in-line plastic package with a copper lead frame. Shown in Figure 2 is a comparison of the allowable package power dissipation for the industry standard iron-nickel alloy (Kovar) lead frame and the Sprague copper lead frame used on these devices. As shown, at an ambient temperature of +70°C, the Kovar lead frame allows only 0.64 watts while the copper lead frame allows 1.33 watts. At +25°C the copper lead frame permits a package power dissipation of 2.0 watts!

Actual power dissipation in any application for the Series ULN-2000A devices is the sum of the individual driver power dissipations. In turn, the individual driver dissipation is the product of the collector-emitter saturation voltage, the collector current, and the duty cycle. The collector-emitter saturation voltage is dependent on the collector current and, to a lesser extent, operating temperature.

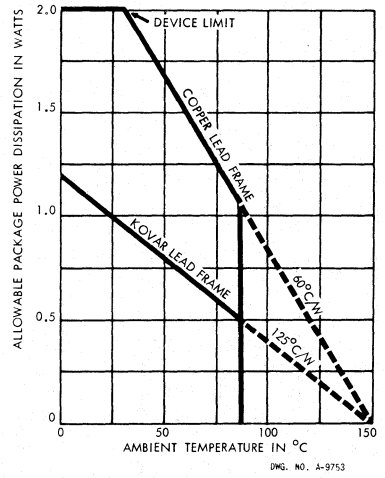


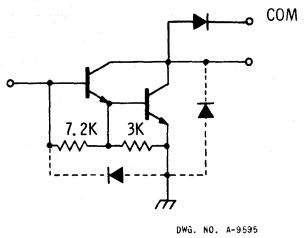
Figure 2

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

The Basic Darlington Array

The first, and basic array, in this series, is the Type ULN-2001A. This is a general-purpose version with input current limiting normally accomplished via the use of an appropriate discrete resistor connected in series with each input. It is also possible to utilize the intrinsic current limiting of many MOS outputs as shown in Figure 4; a typical P-channel characteristic.

The use of TTL in such a manner is not recommended due to the higher currents and resultant high level of package power dissipation. Outputs of most PMOS and CMOS circuits will not normally source currents of any significance due to their high source impedance.



(each driver)

Figure 3

TYPE ULN-2001A SCHEMATIC

14 to 25 Volts PMOS Applications

The Type ULN-2002A Darlington array was specifically designed for use with 14 to 25 volt PMOS devices. Each input has a 7 V Zener diode and a 10,500 ohm resistor (nominal values) to limit the input current to within the capability of most PMOS of the type specified. The basic circuit diagram is shown in Figure 5 with a typical application. Note that there are *no* pull-down resistors or other external discrete components necessary. The incorporation of the Zener diode also results in excellent noise immunity for this array.

TTL and CMOS INTERFACE

The ULN-2001A and ULN-2002A allow only a limited number of input options. Shown in Figure 6 is the basic circuit diagram of the Type ULN-2003A. This device has a series base input resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS logic operating at a supply voltage of 5 V (or 12 V CMOS using FET characteristics).

A guarantee of 200 mA output sink current capability (saturated) is provided with the worse case TTL logic *1* level of 2.4 volts. Low-power Schottky-clamped TTL logic is generally specified to have a minimum V_{OUT} of 2.7 volts. The ULN-2003A is guaranteed to sink 250 mA under this input condition. With the more typical input of 3 volts, the ULN-2003A Darlington pair will sink at least 300 mA in the "ON" state.

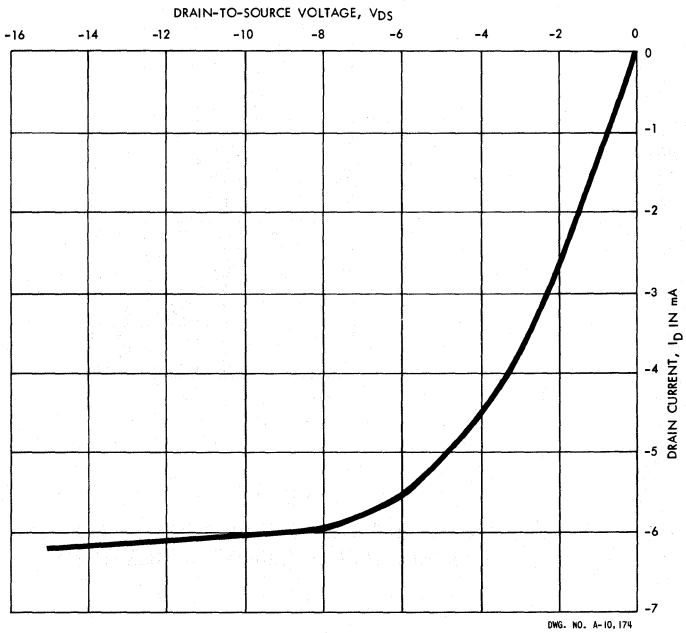


Figure 4

TYPICAL P-CHANNEL DRAIN CHARACTERISTIC

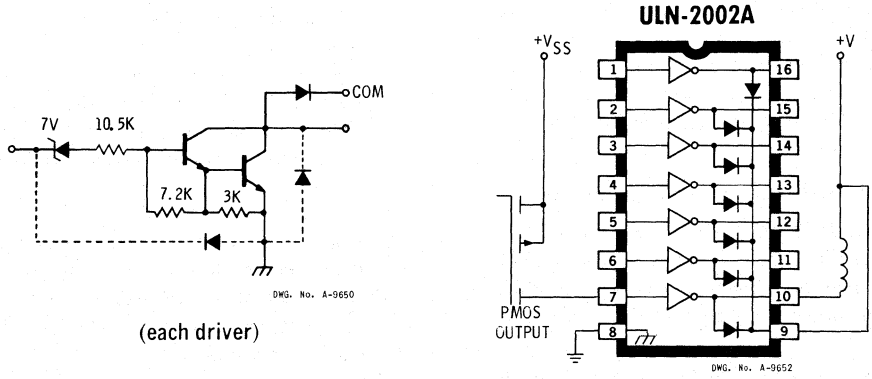


Figure 5

TYPE ULN-2002A SCHEMATIC AND APPLICATION

TTL totem pole outputs are not specified between the 400 μA logic *1* fanout condition and the maximum output short-circuit current (20 to 55 mA for the 7400 series). Between these rather wide limits lies the required ULN-2003A input current. The maximum Type ULN-2003A input current level is specified at 1.35 mA at the extrapolated TTL maximum logic *1* level of 3.85 V.

The ULN-2003A Darlington array will handle a great many interface needs – particularly those beyond the capabilities of TTL buffers. Also shown in Figure 6, is a typical application of the ULN-2003A Darlington array. Of particular interest in this application is an unusual use of the transient-suppression diodes for a non-inductive load. The lamp test feature can of course be used with any of the devices in this series.

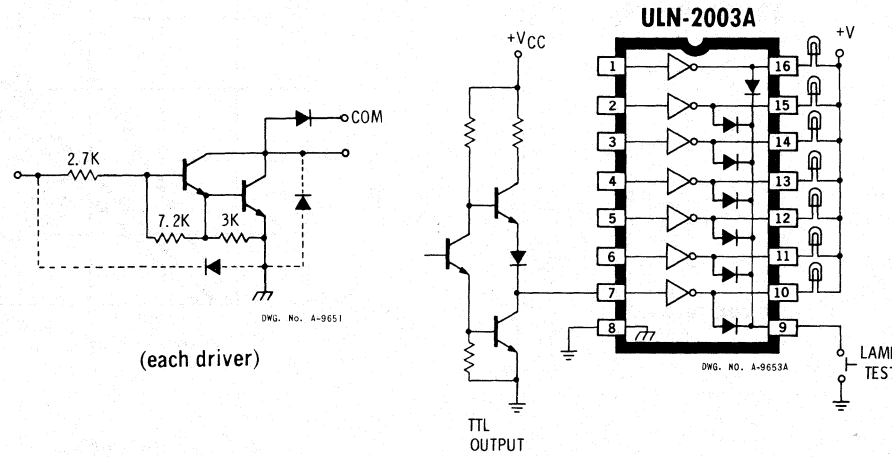


Figure 6

TYPE ULN-2003A SCHEMATIC AND APPLICATION

The diodes are designed to handle the same current and voltages as the output transistors. Switching can be accomplished through an ordinary switch or an appropriate power transistor. With the standard +70°C ambient and the most widely used lamps(No. 327 or No. 387 lamps) there is no problem with continuous operation.

6 to 15 Volt CMOS or PMOS Applications

The Type ULN-2004A Darlington array has an appropriate series input resistor (nominally 10.5 kΩ) to allow its operation directly from CMOS or PMOS logic outputs utilizing supply voltages of between 6 and 15 V.

Shown in Figure 7 is a typical application of this array. Although the discrete output buffer could be used to increase the output capability of any of the devices in this series, this is most often done by paralleling outputs as was described earlier.

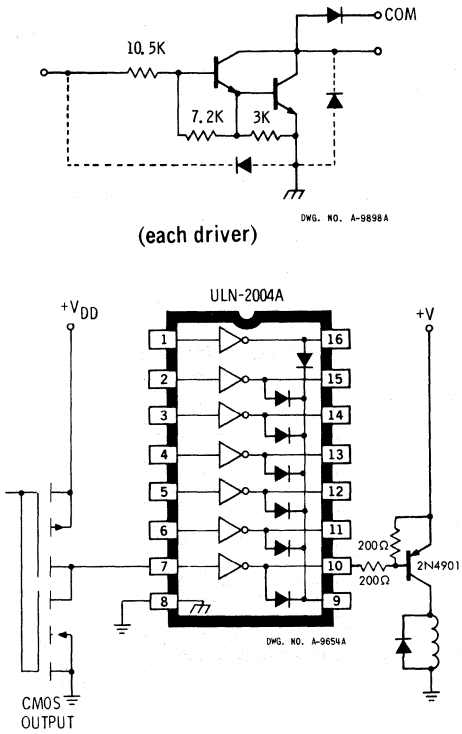


Figure 7
Type ULN-2004A SCHEMATIC AND APPLICATION

Input Current

The Darlington collector current (output in saturation) at an ambient temperature of +25°C, for any input current is the same for all four devices in this series and is shown in the graph of Figure 8. More accurately, the maximum input current for any collector current is described by the equation:

$$I_{IN(\mu A)} = I_{C(mA)} + 140\ \mu A$$

where I_{IN} is the input current in microamperes, I_C is the collector current in milliamperes, and the figure 140 represents the maximum shunt current through the emitter-base resistors. The typical input current can be described as:

$$I_{IN(\mu A)} = 0.58\ I_{C(mA)} + 110\ \mu A$$

where the figure 0.58 is an adjustment for the typical Darlington current gain and the figure 110 represents the typical shunt current.

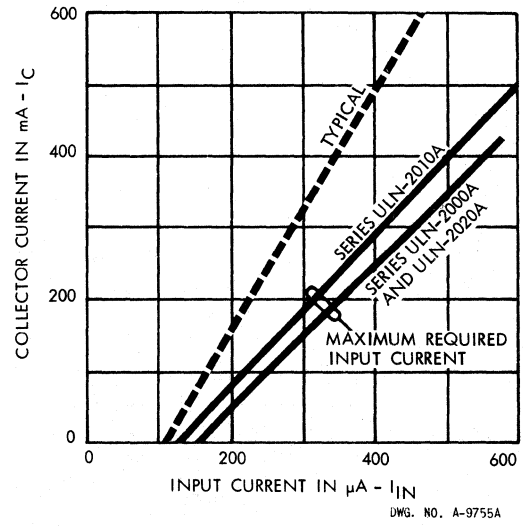
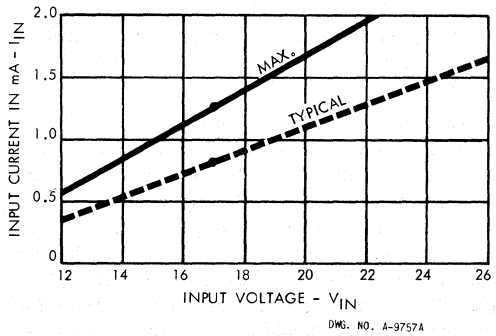
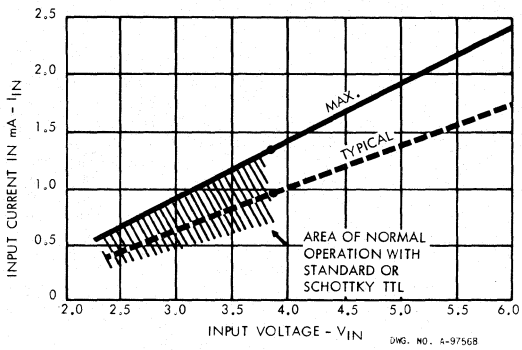


Figure 8
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

The input current as a function of input voltage is shown in Figure 9 for the ULN-2002A, ULN-2003A, and the ULN-2004A. The Type ULN-2001A Darlington array is not shown since input current is more a function of the external circuitry. Systems utilizing either CMOS or PMOS logic should be evaluated for intrinsic current limiting as was shown in Figure 4.





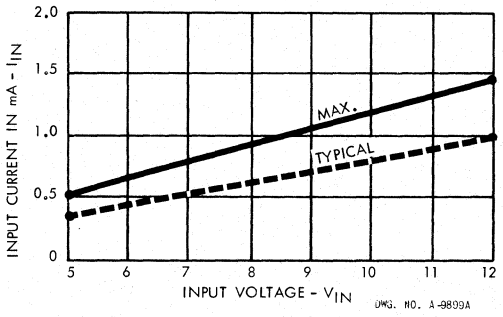


Figure 9
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Low Available Drive Current Operation

Occasionally, applications featuring minimum available input drive current and a high output load current have shown the Type ULN-2003A and ULN-2004A Darlington arrays to be inadequate for the particular requirement under worst case conditions. This usually results from the restricted drive current available from a TTL or CMOS gate operating from a nominal supply of 5 volts.

Under worst case conditions with a low logic *1* voltage (2.4 V), and a high input resistor value (3.51 kΩ), the available load current is reduced to only 145 mA. Compounding this problem would be the effect that a high drive current requirement would have on the logic output voltage since that is normally specified at only 400 μA. If the gate output is connected to additional logic elements, a minimum logic *1* voltage of 2.0 V must be maintained and at that level the worst case Darlington load current would be reduced to only 31 mA!

A simple solution to this problem is through the use of inexpensive pull-up resistors as shown in Figure 10. The minimum resistor value is determined by the maximum allowable sink current (16 mA for TTL, 360μ A for CMOS), the minimum logic *0* output voltage, and the maximum supply voltage as per the following equation:

$$R_P \geq \frac{V_S - V_{OUT(0)}}{I_{OUT}}$$

For standard TTL, the minimum value for R_P is about 316 Ω with values between 3000 Ω and 5000 Ω being used customarily. Multiple pull-up resistors in a single in-line package are shown in Sprague Engineering Bulletin No. 7041; resistors in a dual in-line package are shown in Bulletin No. 7042.

Conclusion

Since the Series ULN-2000A high-voltage, high-current Darlington transistor arrays are quite conservatively designed, the basic product is fully capable of being ordered to higher voltages and/or higher currents than the standard specifications. Presently, parts are available to withstand up to 95 volts on the output. Parts with this higher voltage rating would create a potential for switching loads far in excess of 125 watts! Aside from the higher power handling capability, the higher voltage rating is required for driving plasma or gas-discharge displays.

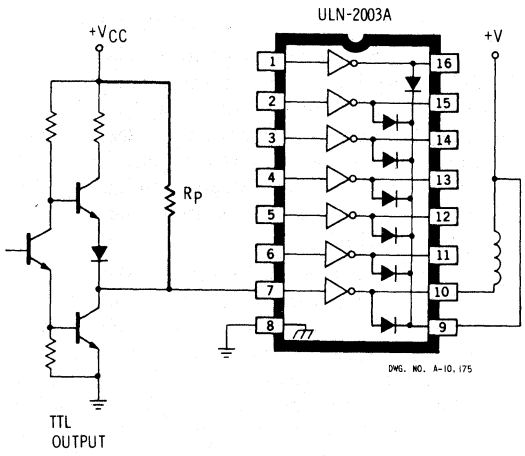


Figure 10

USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

Although not intended for high power applications, there is also available a Series ULS-2000H with hermetic sealing and an operating temperature range to +125°C. These parts are recommended for military and aerospace applications as well as commercial and industrial control applications where severe environments may be encountered.

Cer-DIP, industrial-grade hermetic devices, Series ULQ-2000R, are rated for use over the temperature range of −40°C to +85°C, permitting their use in commercial and industrial applications requiring a moderate package power dissipation (1 W at T_A = +85°C).

All of these Darlington transistor arrays offer a common solution to a great many interface needs. The minimal component count and straightforward printed wiring board layout offer benefits in cost reduction, simplicity of board layout, and savings in space. Other benefits are a reduction in insertion costs, and lower handling and inventory costs than other alternatives. Cost benefits from some of these factors are not very tangible. However, fewer components, less complex boards, etc. usually result in lower system manufacturing costs.

EXPANDING THE FRONTIERS OF IC INTERFACE FOR ELECTRONIC DISPLAYS

INTRODUCTION

The original monolithic high-voltage/high-current power drivers from Sprague were capable of sustaining 100 V and sinking load currents of 250 mA on each of four outputs. That 1970 peripheral driver capability has since been expanded and improved on to solve many of the most difficult display interfaces. Our newest devices are rated for operation to 130 V, sourcing or sinking to 1.5 A, and as many as eight drivers per package (not all together) with inputs for TTL, Schottky TTL, DTL, CMOS, and PMOS.

LAMP (INCANDESCENT) INTERFACE

Utilizing marketing inputs that related to existing hybrid interface circuits, a group at Sprague designed and manufactured monolithic ICs which initially were largely used for aircraft indicator lamp interface. Although not widely known, these quad driver units were developed quite independently (and simultaneously) to the ubiquitous TI 75451 series of high-speed, low-voltage peripheral drivers. A concentration upon circuit design factors, improvements in DIP packaging (copper alloy lead frames), and tighter, tougher control of diffusion-related parameters has allowed the manufacture of quad power drivers rather than the dual mini-DIPs offered by TI.

An increased awareness for improvements in reliability and space and power reductions provided a rather successful military market for Sprague lamp and relay interface; early success was evident in military aircraft indicator lamp interface, a tough application for TTL type ICs due to severe inrush currents resulting in secondary breakdown during "turn on". The increased current sinking capability of the Sprague ICs offers a solution to lamp interface that usually obviates the need for "warming" resistors (across the output) which slightly warm the lamp filament and thus minimize problems associated with cold lamp filaments.

The relay driver types of Sprague IC drivers (and other similar transient-protected ICs) are somewhat more useful than the so-called general purpose types, since the diode common terminal may be switched for a system lamp test. As shown in Figure 1, only a single connection to each DIP is required.

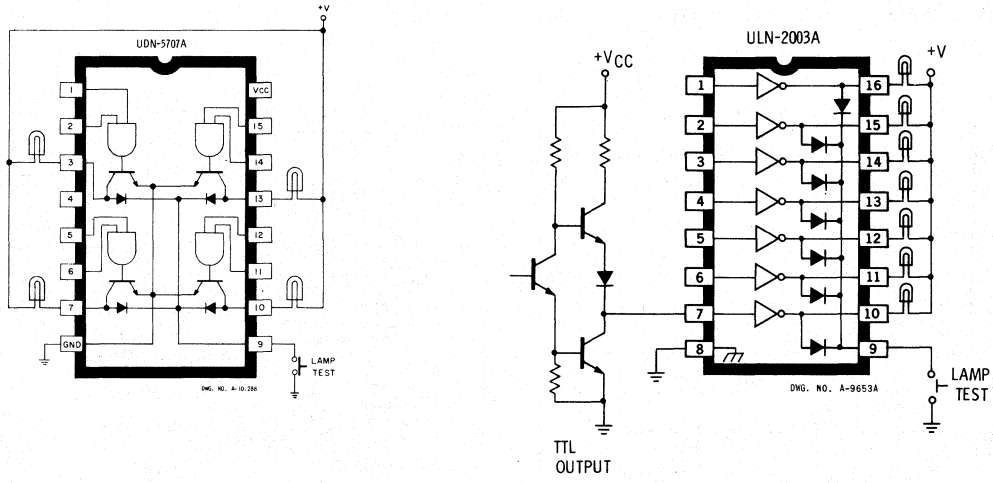


Figure 1

The high current-sinking capability of the Sprague ICs allow such loads as the #327 or #387 lamps to be driven without difficulty of secondary breakdown. The device beta will usually not allow sinking of the 10 to 13 times (nominal value) inrush current of cold lamps; but the lamp rapidly reaches a current level within the device output limitations (Figure 2 shows current as a function of time for a single #327 lamp). Sustaining this instantaneous inrush current and its peak power has been a key element in the success of many lamp interface circuits.

GAS DISCHARGE DISPLAY ICs

Early in 1972, Sprague successfully produced its first high-voltage IC designed for gas discharge displays—a five channel, 130 V unit for cathode (segment) interface. Subsequently, other circuits, both cathode and anode drivers, were produced; most of which were used in calculator applications with the Burroughs Panaplex® II. In Figure 3 is shown a display interface system utilizing the UHP-481 and UHP-491 display drivers, associated thick-film networks, and discretes. This was a step forward, but still required external discrete components.

Through a collaborative effort begun late in 1973 between Sprague Electric and Burroughs Corp. a newer, more efficient interface scheme evolved. Featured in "Electronic Displays '75," this series of monolithic IC interface devices for the high-voltage gas discharge panels has been one of the trailblazers in the world of display interface ICs. Intended for use in multiplexed display systems, these ICs present one of the easiest and least expensive solutions to a difficult interface problem. A combination of high-voltage bipolar techniques with thin-film resistor technology (circuit resistors sputtered over the IC dielectric) has provided both digit (anode) and segment (cathode) interface.

To facilitate a minimum component interface, a split supply (± 100 V) is employed to allow d-c level-shifting (rather than capacitors or >200 V transistors) and both digit and segment drivers incorporate all pull-up, pull-down, current limiting, off-bias reference, etc. which were formerly required in discrete and/or hybrid systems. With the combination of the digit and segment drivers (each capable of withstanding 120 V), the split power supply approach affords PN diode IC technology suitable for driving a display usually requiring a 180 V minimum ionization voltage (equivalent to ±90 V in the split system).

The use of the Series UDN-6100/7100A gas discharge display drivers shows the need for only two monolithic ICs for displays of up to eight digits and eight segments as shown in Figure 4. Systems requiring digit or segment counts greater than eight employ additional driver ICs, and with the exception of the Type UDN-7180A segment driver, the segment ICs all have outputs with internal current-limiting resistors for the display segments. The UDN-7180A device, for reasons of package power dissipation and/or dissimilar segment currents (certain 14 or 16 segment alphanumeric panels) can also be used, but must have external, discrete current-limiting resistors.

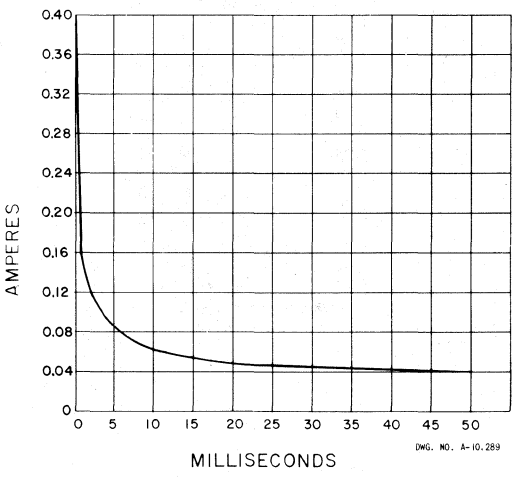


Figure 2

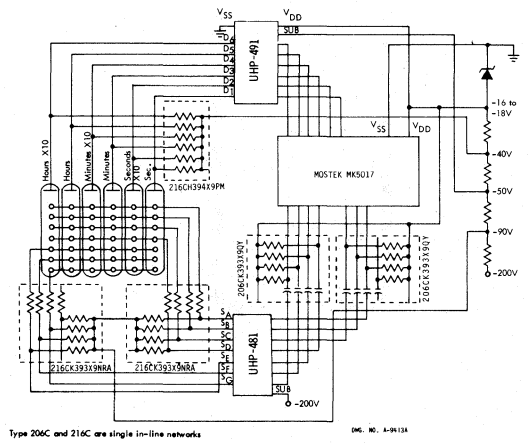


Figure 3

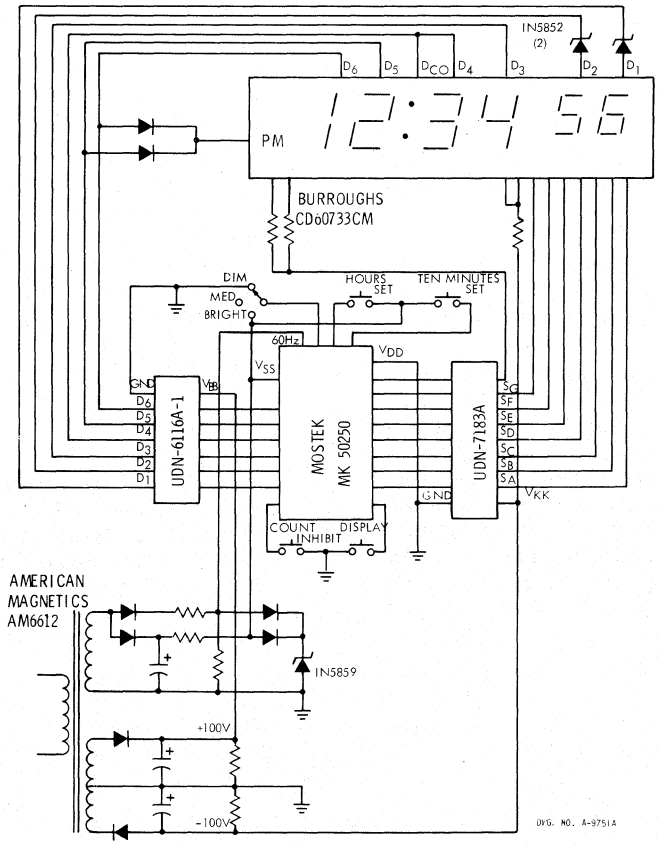


Figure 4

Higher current applications are difficult for both programmable current and switching type display drivers. Segment currents beyond 2.5 or 3 mA present package power dissipation limitations to most dual in-line packages. By using external resistors, the Type UDN-7180A driver allows segment currents of up to 14 mA.

The transistor switch with current-limiting resistor scheme used in Sprague gas discharge display drivers also minimizes problems associated with gas panel arcing which can destroy programmable current circuits. Some of the gas display manufacturers recommend the use of series resistors in each segment line to prevent destruction to the semiconductor interface circuit should such a panel arc occur. Without these series resistors (internal thin-film resistors in Sprague devices) the IC can be destroyed by the high voltage and resulting high current should the panel voltage drop to a very-low level during an arc.

LED INTERFACE

With the obvious abundance and variety of LED interface integrated circuits it would seem unlikely that there are still systems in search of an IC hardware solution to further minimize cost, component count, space, etc.; but this is definitely the case. The deficiencies are chiefly related to the limited number of current-sourcing circuits and/or high-current drivers.

The efficiency of LED displays has improved, but with the larger digits (up to 1" presently) most of the IC drivers are unable to switch the higher currents required in multiplexed systems. The rule-of-thumb generally applied uses the suggested d-c current - multiplied by the number of digits in the display. For example, a multiplexed display of 160 mA peak current will give approximately the same light intensity output as a steady 20 mA in each of eight digits. Of particular difficulty is the switching of currents associated with the lower efficiency yellow and green LEDs. Sprague has provided monolithic integrated circuit solutions to applications requiring segment currents of 350 mA and digit currents of up to 1.5 amperes!

Many of the Sprague ICs used in high-current LED applications were originally designed for use with electro-mechanical loads (relays, solenoids, motors, etc.) although the high-voltage ratings of the drivers are obviously not a concern. A combination of high-current, high-voltage Darlington drivers is shown in Figure 5.

The ULN-2074B source driver is utilized as a modified emitter-follower. Through the use of discrete diodes in the common collector line, allowing the base to be switched to a potential higher than the collector, it is then possible to obtain a saturated output. This prevents the usual emitter-follower problems associated with gain, the MOS output impedance, and power. It is also possible to now better define the voltage at the emitter output and to then provide suitable segment current-limiting resistors for the LEDs.

The ULN-2002A sink driver is a high-current Darlington array with the capability of switching multiplexed LEDs with an available limit of 155 mA for each of the seven drivers when used at a 100% duty cycle. Even the more inefficient yellow or green LEDs can be driven with higher output currents at lower duty cycles (400 mA at a 28% duty cycle).

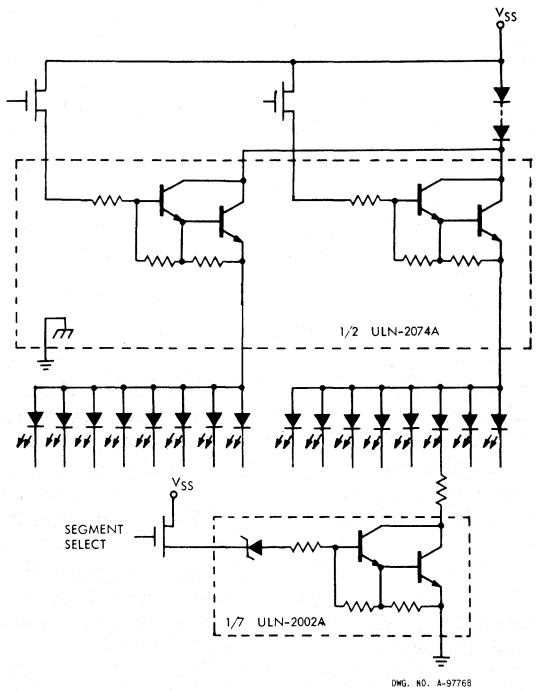


Figure 5

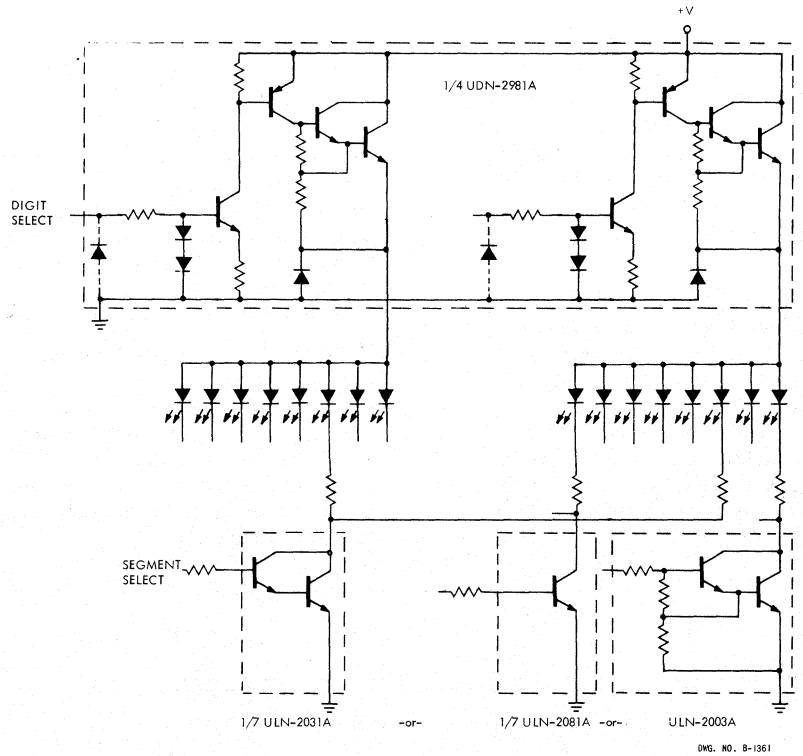


Figure 6

A new eight-channel source driver is shown as a digit switch for common anode LEDs in Figure 6. The Series UDN-2980A drivers will handle output currents to a maximum of 500 mA. Two basic versions of the driver will allow interface from TTL, Schottky TTL, DTL, PMOS, and CMOS levels. Other versions of the ULN-2003A driver are also available for use with the various logic levels.

Of the three sink drivers shown, the ULN-2003A is probably the better choice from a standpoint of both pinout and component count. It also has straightforward in-out pinning. The ULN-2031A and ULN-2081A devices offer lower cost. They are also interchangeable from a pinning aspect although the output ON voltage will be dissimilar.

A common-cathode LED configuration is shown in Figure 7 for currents of up to 1.5 A per digit! A series UDN-2980A source driver is used to switch the segment side, the ULN-2064B or ULN-2074B to switch the digit side. As has been shown with Figure 5, the IC package power dissipation must be considered with high-current applications.

The three examples that have been shown for LED interface represent only a very-small portion of the total applications area. The high-current capabilities and high gain of the Sprague drivers represent potential solutions to many difficult LED display systems - alphanumeric, seven-segment, or matrix; common-cathode or common-anode; continuous or multiplexed.

A-C PLASMA DISPLAY INTERFACE

Plasma displays, such as those manufactured by National Electronics/NCR (USA) and NEC or Fujitsu (Japan), all have one common element with their gas discharge cousin - both types use a neon gas mixture. The plasma panels emit an orange glow when switched at rather high frequencies, and light output intensity is a function of frequency. The a-c term for the plasma display is something of a misnomer since these panels actually operate from a toggled d-c supply (usually in the area of 20 kHz).

The panel is basically a neon-filled capacitor, and has plates (electrodes) which are covered with the dielectric - between which is the neon mixture. Switching this capacitive load presents a problem

with high peak currents in addition to the older problem of the high voltages which are associated with gas displays. Drive circuits use supply voltages of 150 to 260 V (depending on unipolar or bipolar drive), and the semiconductors used must switch instantaneous currents in the order of several hundred milliamperes for the larger displays.

Several high-voltage, high-current arrays made at Sprague Electric can provide an answer to one side of the a-c plasma display interface. The Series ULN-2020A Darlingtons are rated at 95 V while the Series UHP-500 power drivers are rated at 100 V. They are both able to handle the application shown in Figure 8 (a basic d-c, non-multiplexed clock interface rather than a more complex multiplexed system). The ULN-2022A is specifically designed for 14 to 25 V PMOS logic levels while the UHP-506 is intended for use with TTL.

The high-current diodes that are internal to the Sprague arrays are utilized in the unipolar drive scheme connected to a suitable OFF reference. In one POS application, a set of 14 ULN-2023A Darlington drivers replaced more than 400 discrete components. The cost and space savings in such a machine are considerable, and a very complex printed wiring board was greatly simplified.

Further improvements in interface and plasma displays will no doubt evolve, and thus benefit all concerned - display and interface vendor along with the end user. Plasma displays are well-suited to custom panels (particularly those with various sizes of characters) and with improvements in IC breakdown voltages some further simplification of interface should evolve.

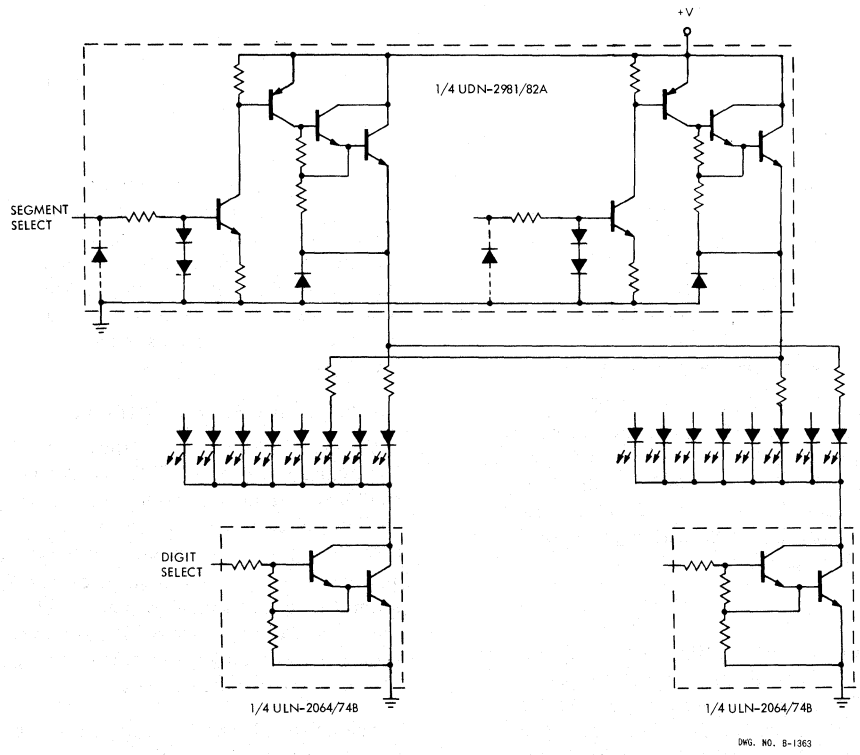


Figure 7

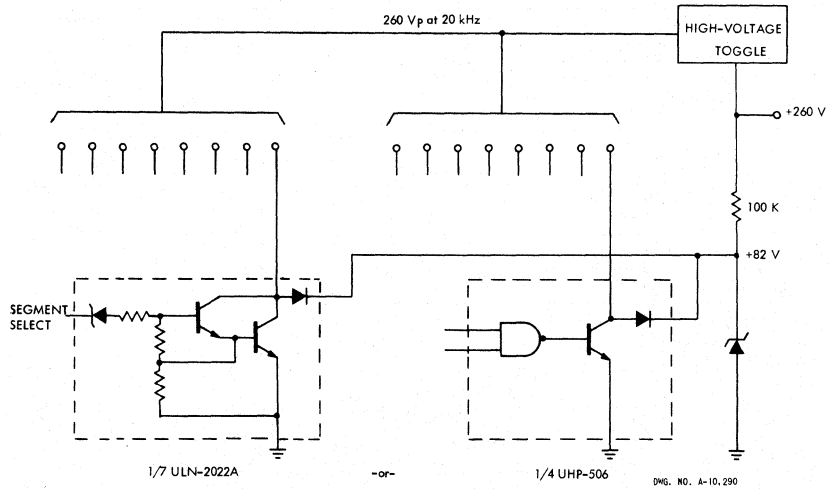


Figure 8

FLUORESCENT DISPLAY INTERFACE

Although the vast majority of fluorescent displays are directly driven from MOS logic (handheld and low-cost desk calculators), there is an emerging need for interface integrated circuits for use with the larger characters (higher currents) and the higher voltages coming into use. These blue-green display panels originated in Japan, and the manufacturers are quite aggressively pursuing markets such as POS systems, clocks, cash registers, appliances, automotive displays, etc. Larger and/or more complex styles are being made, including displays with alphanumeric capability (a starburst 14 or 16-segment pattern).

Modest voltage capability (60 or 70 volts) is all that is required of a semiconductor device to drive these panels, and the currents are in 20 to 30 mA region. These electrical requirements are well within the capability of many gas discharge digit drivers.

The UDN-6118/28A devices are designed specifically for use with fluorescent displays and include internal pull-down resistors so that up to eight segments and eight digits will require only two packages and a greatly simplified power supply. The Type UDN-6118A driver is compatible with TTL, Schottky TTL, DTL, and 5 volt CMOS. The Type UDN-6128A driver is for use with 6 to 15 volt PMOS or CMOS logic.

The future of fluorescent displays look rather strong, particularly if competition further reduces prices. For the moment at least, these displays will not seriously tax the capability of IC interface except, perhaps, from a price/cost standpoint.

HOT WIRE READOUTS

Although hot wire readouts could easily be placed in the incandescent category, their application in multidigit, multiplexed display systems more closely resembles LED circuit operation. Since hot wire displays will conduct current in either direction, isolation diodes are required to prevent sneak paths from partially turning ON unaddressed segments. Compare the typical hot wire display of Figure 10 with LED display of Figure 6. The availability of a suitable, inexpensive diode array would be of considerable asset in multiplexed hot wire systems.

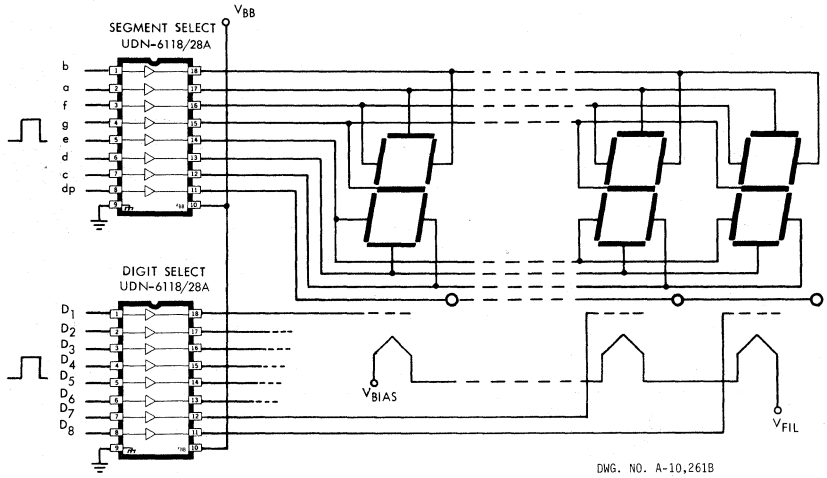


Figure 9

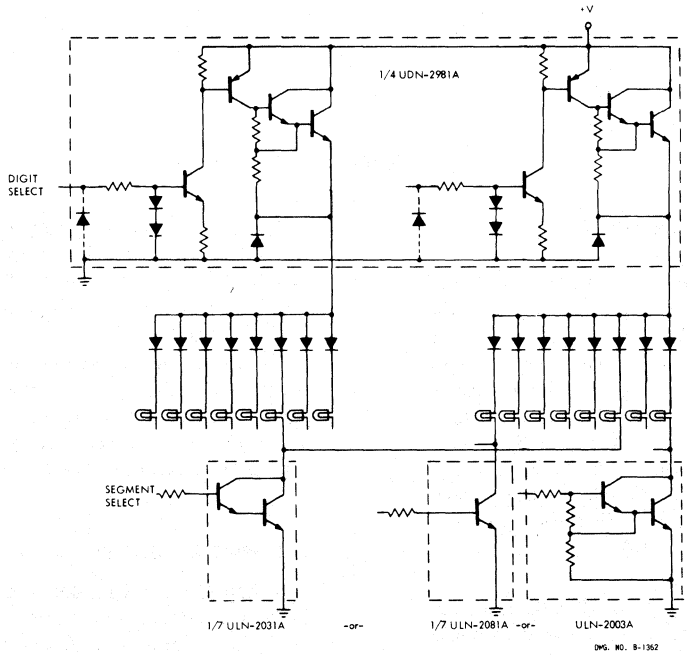


Figure 10

The hot wire readouts are available in both seven-segment and alphanumeric (16-segment) versions and are quite well-suited to high ambient light applications. They do not wash out in sunlight, although their reliability diminishes with the higher currents required in brightly lighted applications. As described, multiplexed schemes can be cumbersome because of the great number of discrete diodes required. One avionics system using a 16-character, 16-segment alphanumeric panel required 256 discrete diodes.

INTEGRATED CIRCUITS FOR CURRENT-SOURCING APPLICATIONS

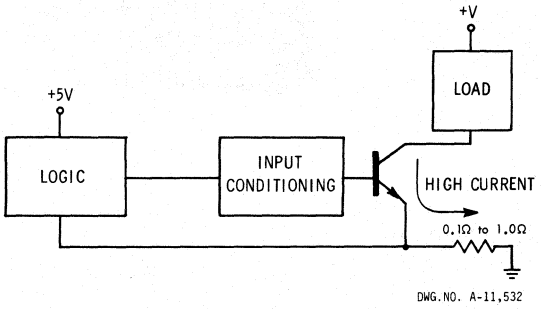
DURING RECENT YEARS, the appearance of many new low-power monolithic devices (LSI and microprocessors) has created an increased need of peripheral power driver integrated circuits. Interface drivers are typically categorized in terms of their output-drive functions. When current flows out of the driver output terminal and into the load, the device is said to "source" current. Conversely, current flows from a load into a "sink" driver.

Sprague integrated source drivers usually consist of high-voltage PNP devices and high-power NPN Darlington outputs (which provide PNP-type action), with input-level shifting. These power ICs are useful for interfacing low-level logic (TTL, CMOS, NMOS, PMOS) and high-current or high-voltage relays, solenoids, lamps (incandescent, LED, neon), motors, and displays (gas-discharge, LED, vacuum-fluorescent). They can also be used to provide multi-channel buffers for discrete power semiconductors.

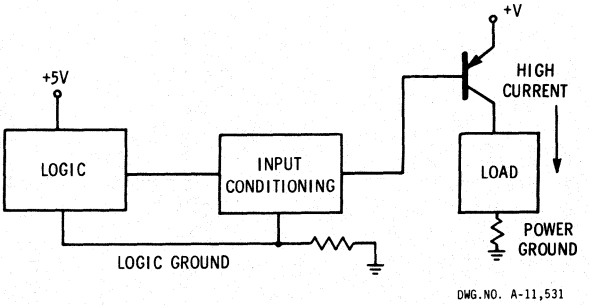
The advantages of source drivers for display interface are quite evident. The X-Y addressing of most readouts requires both source and sink functions to minimize pin count, interconnections, and package count.

A more subtle advantage of source drivers is related to their use with inductive loads or incandescent lamps. Both types of load generate troublesome transients and noise currents on common logic/load ground lines. In addition, high ground currents can shift the ground rail, affecting logic input levels, thresholds, and noise immunity. The use of source drivers can minimize many of these concerns by separating the logic and power returns.

FLOATING LOGIC-GROUND LEVEL (Sink Driver)



SEPARATE GROUND RETURNS (Source Driver)



RELAY-DRIVER APPLICATIONS

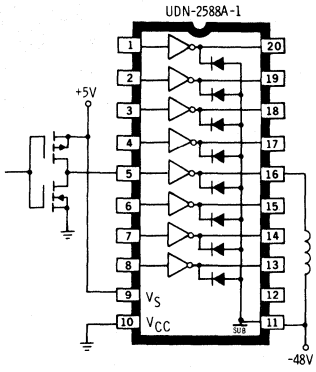
SERIES UDN-2580A, eight-channel source drivers, and Types UDN-2956A and UDN-2957A, five-channel source drivers, provide current/voltage translation from TTL, positive CMOS, or negative CMOS logic to −48 V telecommunication relays requiring less than 350 mA. All devices have internal inductive-load transient-suppression diodes.

Type UDN-2580A-1 is best driven from negative-reference CMOS or NMOS logic (−5 V or −12 V swing) in order to provide a −48 V swing at the output. The active-low input Type UDN-2588A-1 can be driven from positive logic TTL (+5 V swing) or CMOS (+12 V swing) levels. The active-high input Type UDN-2956A is similar to Type UDN-2588A-1, but it also has a chip-enable function that requires a minimum number of drive lines to control outputs from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

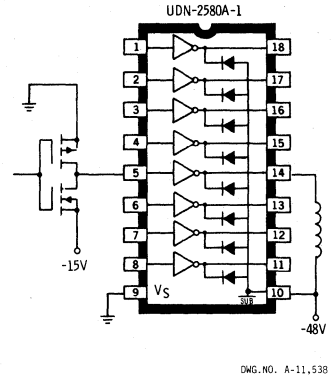
Supply Voltage, V_{EE} . . . . . −50 V
Continuous Output Current, I_{OUT} (per output) . . . . . −350 mA

TELECOMMUNICATIONS RELAY DRIVER (Positive Logic)



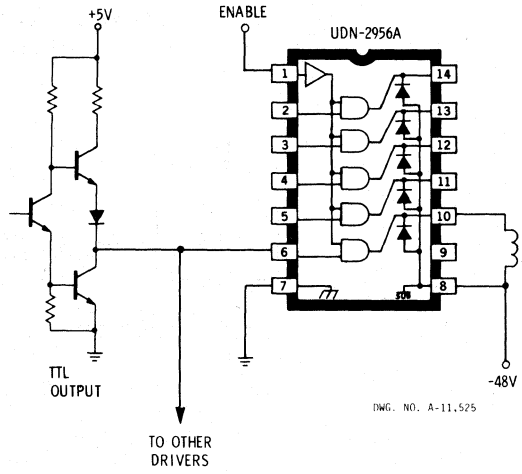
DWG. NO. A-11,524

TELECOMMUNICATIONS RELAY DRIVER (Negative Logic)



DWG.NO. A-11,538

MULTIPLEXED RELAY DRIVER



DWG. NO. A-11,525

PRINTER APPLICATIONS

SPRAGUE SOURCE DRIVERS have been used extensively in electrosensitive, thermal, and impact printer applications. Multi-channel devices in the Series UDN-2580A and UDN-2980A reduce parts count and provide up to 350 mA per output at voltages up to 75 V (resistive load). Copper lead frames make these devices capable of simultaneously delivering up to 125 mA continuously from all eight channels at an ambient temperature of +50°C.

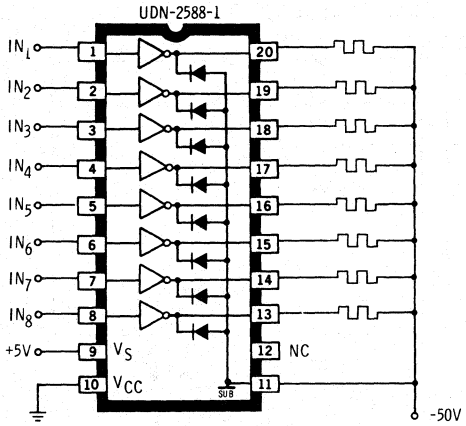
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
- UDN-2588A-1 ..... to 75 V
- UDN-2981A and UDN-2982A ..... 5 V to 45 V
- UDN-2983A and UDN-2984A ..... 35 V to 75 V

Logic Voltage, V_{IN} ..... 12 V
Continuous Output Current, I_{OUT} (per output) ..... −350 mA
Peak Output Current, I_{OP} ..... −500 mA

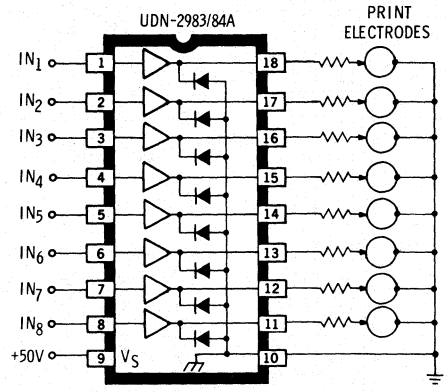
3

THERMAL PRINTER APPLICATION



DWG.NO. A-11,530

ELECTROSENSITIVE PRINTER APPLICATION



DWG.NO. A-11,529

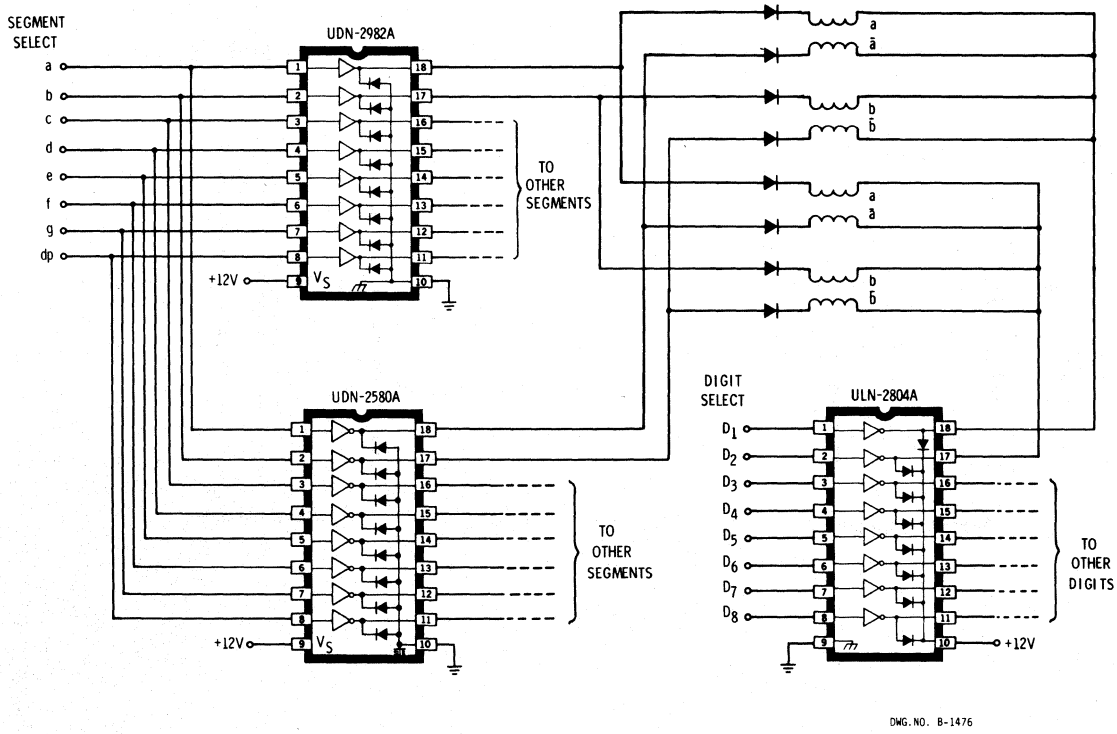
ELECTRO-MECHANICAL DISPLAY APPLICATIONS

SOURCE DRIVERS in the Series UDN-2580A and UDN-2980A, when combined with the Type ULN-2804A sink driver, provide a simple interface between 12 V CMOS logic and a multiplexed electro-mechanical display. As shown, the need for additional inverter packages is eliminated since Type UDN-2580A is activated by a low input level and Type UDN-2982A is turned ON by a high input input level. All drivers have internal inductive-load transient-suppression diodes and copper lead frames for improved package power dissipation capability.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S ..... 35 V
Continuous Output Current, I_{OUT} (per output) ..... −350 mA

MULTIPLEXED ELECTRO-MECHANICAL DISPLAY DRIVERS



VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS

SPRAGUE SERIES UDN-6100A and UDN-2580A source drivers provide solutions to problems encountered in driving higher-voltage vacuum-fluorescent and planar gas-discharge displays. Both series of parts provide TTL, CMOS, and NMOS input-logic compatibility. Series UDN-6100A devices are active high (non-inverting) drivers. Series UDN-2580A drivers are active low (inverting) devices.

At minimum cost, Series UDN-6100A-2 devices offer 60 V output breakdowns for vacuum-fluorescent displays typically utilizing less than 32 characters. Featuring a minimum 80 V output breakdown voltage, standard Series UDN-6100A drivers (no additional suffix) guarantee 25 mA per output. Suffix -1 devices provide for a 110 V breakdown, recommending them for 40 to 80-digit or dot-matrix V-F applications or gas-discharge anode-drive applications requiring the higher output voltage. All of these drivers include internal pull-down resistors and provide operation from single-ended positive supplies.

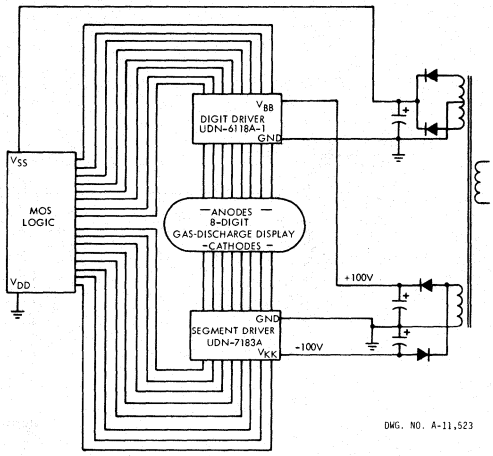
Operation from a split-supply allows the user to bias the V-F filament at ground potential or to utilize a system-supply voltage above ground (±40 V instead of +80 V). Either Type UDN-6138A or Type UDN-6148A source drivers are recommended.

For vacuum-fluorescent display applications requiring a higher current capability (operating several displays with common drive circuitry), Type UDN-2588A can be used with appropriate external output pull-down resistors to provide up to 350 mA per output.

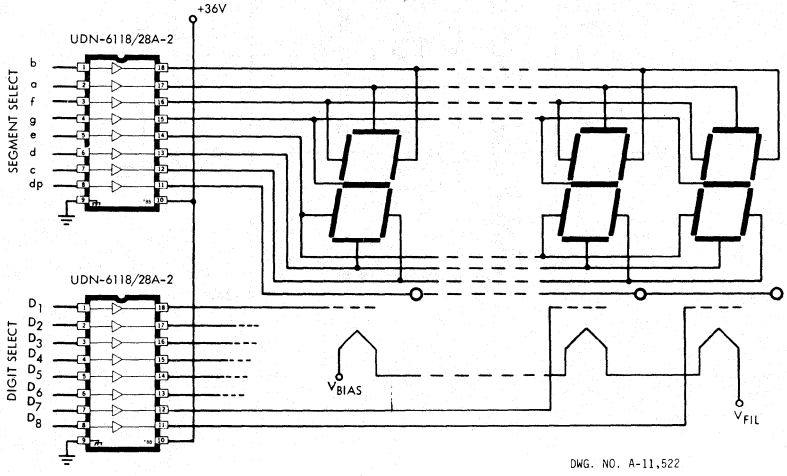
MAXIMUM OPERATING VOLTAGES

V_S V_{BB}	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
+5	<1.4	>4.5	0	−45	UDN-2588A
				−75	UDN-2588A-1
+12	<8.4	>11.5	0	−45	UDN-2588A
				−75	UDN-2588A-1
+30	2.4	<0.4	NA	−30	UDN-6138A-2
	4.0	<0.4	NA	−30	UDN-6148A-2
+40	2.4	<0.4	NA	−40	UDN-6138A
	4.0	<0.4	NA	−40	UDN-6148A
+60	TTL or CMOS		NA	0	Series UDN-6100A-2
+80	TTL or CMOS		NA	0	Series UDN-6100A
+110	TTL or CMOS		NA	0	Series UDN-6100A-1

GAS-DISCHARGE DISPLAY DRIVERS

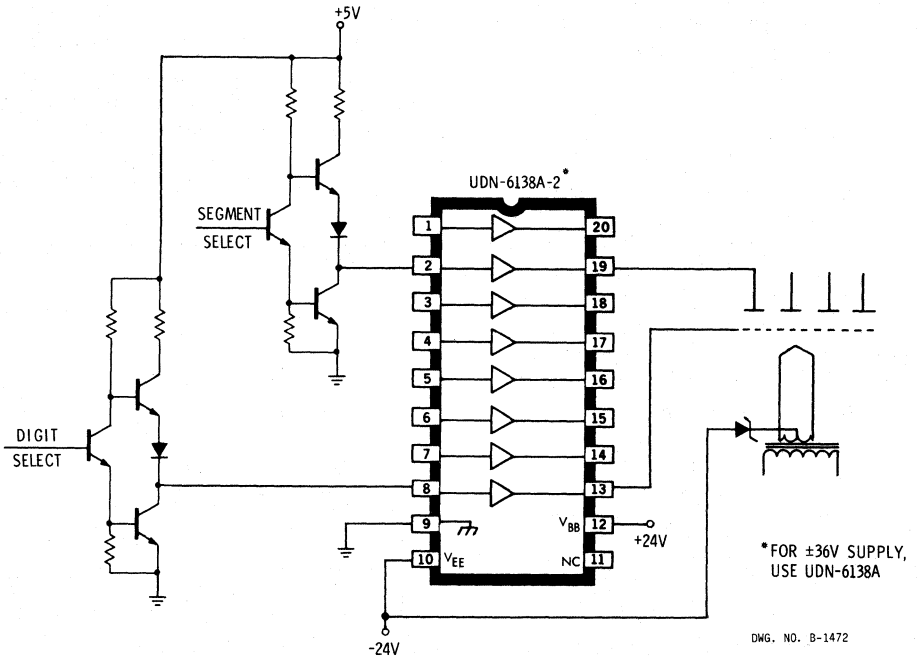


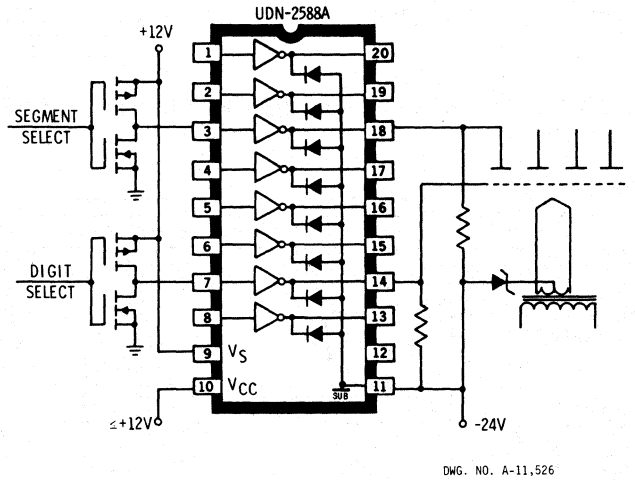
MULTIPLEXED VACUUM-FLUORESCENT DISPLAY DRIVERS



VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS (Continued)

VACUUM-FLUORESCENT DISPLAY DRIVERS (Split Supply)





INCANDESCENT LAMP DRIVER APPLICATIONS

DRIVING MULTIPLEXED incandescent lamps at voltages up to 75 V with peak currents approaching 500 mA per segment, Series UDN-2980A eight-channel source drivers, when combined with Type ULN-2069B sink drivers, provide for a very cost-effective approach. Multiplexed lamps must typically be operated at a voltage $\sqrt{N}$ (N = the number of digits) times the nominal d-c voltage, to obtain sufficient brightness. For example, a four-digit, 28 V display requires 56 V to operate satisfactorily. In addition, care must be taken to select a proper driver to withstand the substantial inrush currents created by cold filaments. Peak currents of up to ten times the nominal operating currents have been observed. Multiplexed lamps must also incorporate diodes to prevent series/parallel paths to unaddressed elements.

RECOMMENDED MAX. OPERATING CONDITIONS

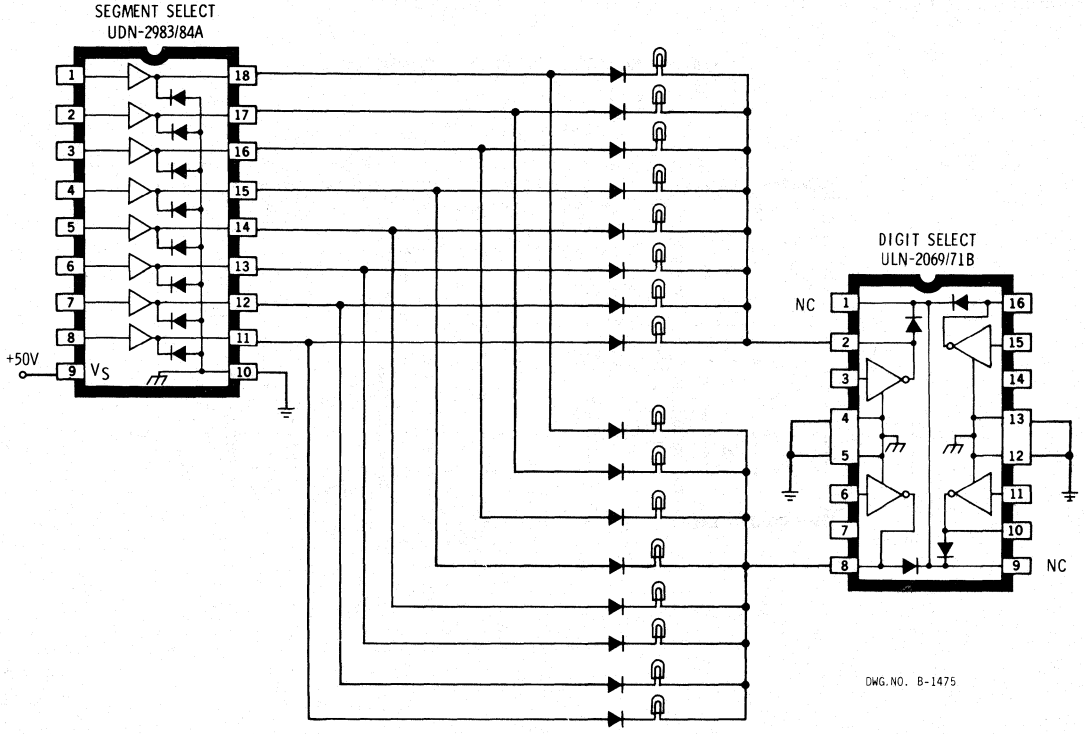
Supply Voltage Range, V_S
- UDN-2981A and UDN-2982A ..... 5 V to 45 V
- UDN-2983A and UDN-2984A ..... 35 V to 75 V

Continuous Output Current, I_{OUT} (per output) ..... −350 mA

Peak Output Current, I_{OP} ..... −500 mA

3

MULTIPLEXED LAMP DRIVER, TTL- OR MOS-COMPATIBLE



LIGHT-EMITTING DIODE APPLICATIONS

SERIES UDN-2580A and Series UDN-2980A 8-channel source drivers provide monolithic solutions to problems associated with driving multiplexed LED displays in common-cathode or common-anode configurations.

Type UDN-2585A is a non-Darlington inverting (input low = output high) source driver that is frequently used as a segment or dot driver in a common-cathode LED display where multiplexed segment or dot currents do not exceed 120 mA. This device features input logic-level compatibility with open-collector TTL, standard TTL, CMOS, and NMOS, as well as low output saturation voltages.

For common-cathode applications requiring higher segment currents, or for common-anode digit drive applications, Series UDN-2980A is recommended. This non-inverting (input high = output high) series features 350 mA per output continuous current ratings with peak currents reaching 500 mA per output. Outputs may be paralleled for higher current capability. Type UDN-2982A is logic-compatible with 2.4 V output levels of TTL and CMOS. Similar high output current ratings, for use in inverting applications, are offered by the Type UDN-2580A driver.

Combining Sprague source drivers with multi-channel, high-current sink drivers (such as Type ULN-2068B, UDN-2595A, or ULN-2814A) provides simple, compact, and economical solutions to driving high-current multiplexed LED displays.

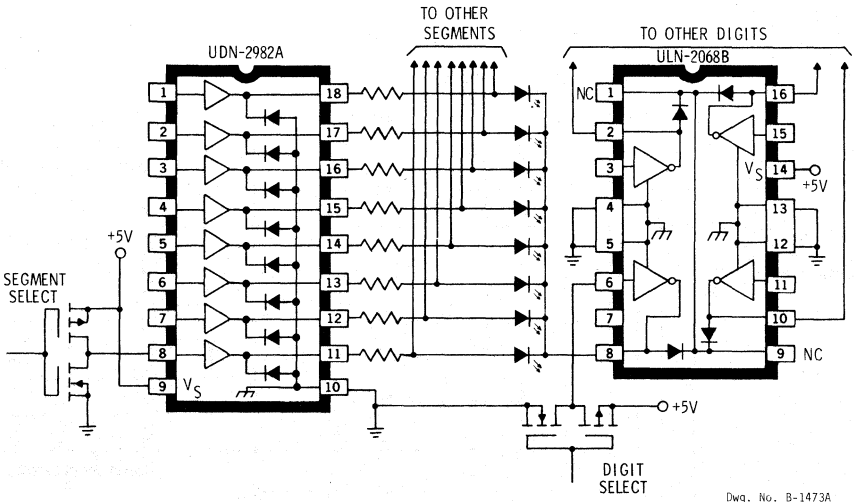
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S
- UDN-2585A ..... 15 V
- UDN-2982A ..... 45 V

Continuous Output Current, I_{OUT} (per output)
- UDN-2585A ..... −120 mA
- UDN-2982A ..... −350 mA

Input Voltage, V_{IN} ..... 15 V

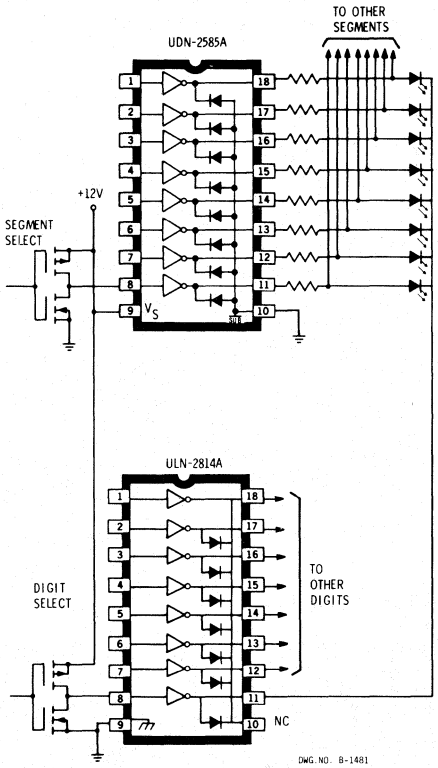
COMMON-CATHODE LED DISPLAY



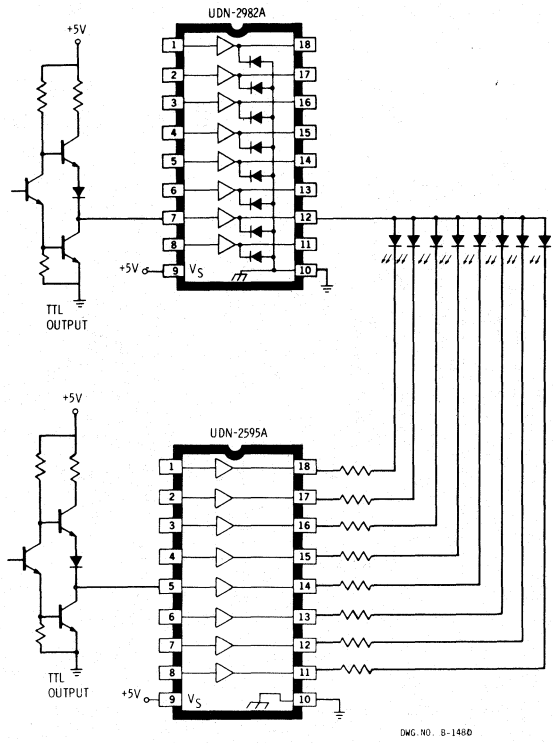
COMMON-CATHODE LED DISPLAY

LIGHT-EMITTING DIODE APPLICATIONS
(Continued)

COMMON-CATHODE LED DISPLAY



COMMON-ANODE LED DISPLAY

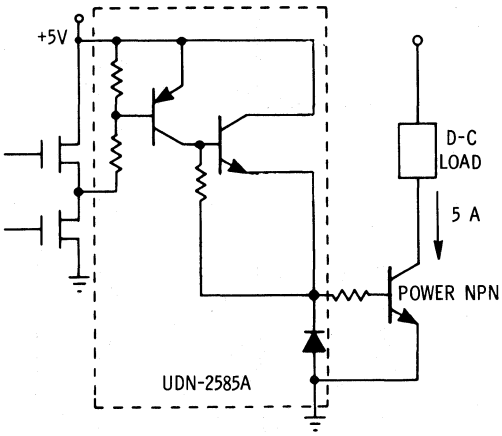


MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

SPRAGUE SOURCE DRIVERS can be employed as multi-channel pre-drivers for discrete high-current or high-voltage semiconductors, thus reducing the need for many discrete components. For instance, a UDN-2580A 8-channel source driver can provide up to 350 mA of pre-drive current into the base of power NPN devices, making 5 A load currents readily available. Higher load currents can be obtained by using power NPN Darlington devices.

For a-c loads, it is possible to use any of the Sprague source drivers to provide gate current (with appropriate current-limiting) to a power SCR or triac. This scheme can provide an economical solution to many applications such as driving incandescent lamps or a-c motors at up to 20 A.

DRIVER FOR HIGH-POWER DISCRETE DEVICES



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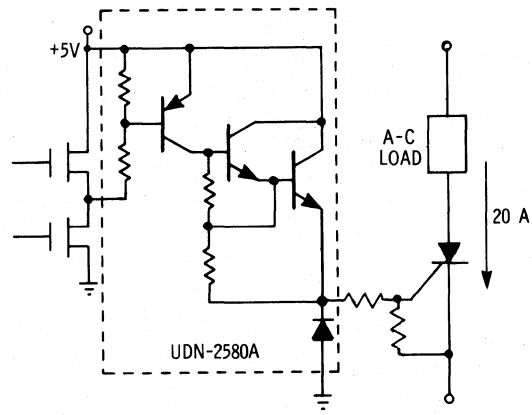

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RELIABILITY OF SERIES ULN-2000A AND ULN-2800A HIGH-CURRENT DARLINGTON DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series ULN-2000A and ULN-2800A integrated circuits and provides information that can be used to calculate the failure rate at normal junction operating temperatures.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at an ambient temperature of +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.
2) Accelerated testing is performed at junction temperatures above +125°C and is used to generate failure-rate data.
3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Tables Ia and Ib contain data produced by life tests that were conducted at +150°C and +175°C. The data include the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing alloca-

TABLE Ia
TEST RESULTS at T_j = +150°C

TEST NUMBER	QTY.	HOURS ON TEST: 90	150	300	600	1200	1800	2400	3000	5000
		NUMBER OF FAILURES								
1	12	0	0	0	0	2	0	—	—	—
2	22	0	0	0	0	0	0	0	0	—
3	22	0	0	0	0	0	0	0	0	—
4	22	0	0	2	0	0	3	0	0	—
5	22	0	0	0	0	0	0	0	0	—
6	22	0	0	0	0	0	1	0	0	—
7	12	0	0	0	0	0	0	—	—	—
8	12	0	0	0	0	0	0	—	—	—
9	90	0	0	0	2	0	0	—	—	—
10	12	0	0	0	0	0	0	—	—	—
11	12	0	0	0	0	0	0	—	—	—
12	12	0	0	0	0	0	0	0	0	—
13	12	0	0	0	0	0	0	0	0	—
14	35	0	0	0	0	0	0	1	—	—
15	12	0	0	0	1	1	0	0	0	0
16	25	0	0	0	0	0	—	—	—	—
17	25	0	0	0	0	0	—	—	—	—
TOTAL ON TEST		381	381	381	379	376	323	173	138	10
TOTAL FAILURES		0	0	2	3	3	4	1	0	0
TOTAL GOOD		381	381	379	376	373	319	172	138	10
P_s		1.00	1.00	0.995	0.992	0.992	0.988	0.994	1.00	1.00
Cumulative P_s		1.00	1.00	0.995	0.987	0.979	0.967	0.961	0.961	0.961
$P_f = 1 - P_s$		0	0	0.005	0.013	0.021	0.033	0.039	0.039	0.039
Cumulative % Failures		0	0	0.5	1.3	2.1	3.3	3.9	3.9	3.9

tion of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 40 hours at +175°C or 200 hours at +150°C to 1000 hours of qualification life test at +125°C.

The data at the bottom of Tables Ia and Ib were compiled by calculating the probability of success (P_s), the cumulative probability of success, the probabilityof failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% failure point. The mediam life at a junction temperature of +150°C is 1.6×10^5 hours. At +175°C, the median lifetime is 3.0×10^4 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^o e^{-\epsilon/kT}$$

where V_r^o = a constant
ϵ = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5710M, and Series UDN-2980A devices at

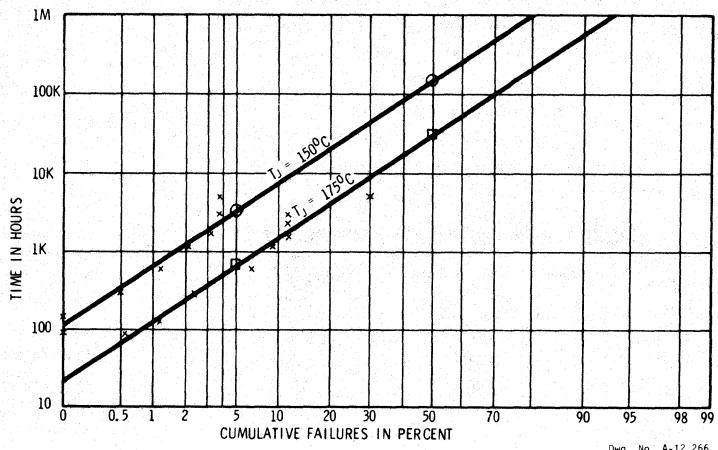
TABLE Ib
TEST RESULTS at T_j = +175°C

TEST NUMBER	QTY.	HOURS ON TEST: 90	150	300	600	1200	1800	2400	3000	5000
		NUMBER OF FAILURES								
1	25	0	0	0	7	—	—	—	—	—
2	25	0	0	0	0	0	0	0	—	—
3	25	0	0	1	2	1	0	0	—	—
4	24	0	1	0	1	0	0	0	0	—
5	19	0	0	0	0	0	0	—	—	—
6	19	0	0	0	0	0	0	—	—	—
7	12	0	0	2	3	2	—	—	—	—
8	12	0	0	0	0	0	—	—	—	—
9	12	0	0	0	0	0	0	—	—	—
10	18	0	0	0	0	0	—	—	—	—
11	12	0	0	0	0	0	2	0	0	2
12	12	0	0	0	0	0	0	—	—	—
13	12	1	0	0	0	0	0	0	—	—
14	18	0	0	1	2	0	7	—	—	—
15	12	1	0	0	0	0	0	—	—	—
16	12	0	0	0	0	0	—	—	—	—
17	24	0	0	0	0	0	0	—	—	—
18	12	0	1	0	1	0	0	0	0	—
19	24	0	0	0	0	0	—	—	—	—
TOTAL ON TEST		329	327	325	321	287	213	99	42	10
TOTAL FAILURES		2	2	4	16	3	9	0	0	2
TOTAL GOOD		327	325	321	305	284	204	99	42	8
P_s		0.994	0.994	0.988	0.950	0.990	0.958	1.00	1.00	0.800
Cumulative P_s		0.994	0.988	0.976	0.927	0.917	0.879	0.879	0.879	0.703
$P_f = 1 - P_s$		0.006	0.012	0.024	0.073	0.083	0.121	0.121	0.121	0.300
Cumulative % Failures		0.6	1.2	2.4	7.3	8.3	12.1	12.1	12.1	30.0

multiple temperatures. Failure analysis of devices rejected during this testing of Series ULN-2000A and ULN-2800A also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line drawn through +150°C and +175°C failure points has a slope corresponding to that of the 1.0 eV failure mechanism.

Figure 1
CUMULATIVE PERCENT OF FAILURES



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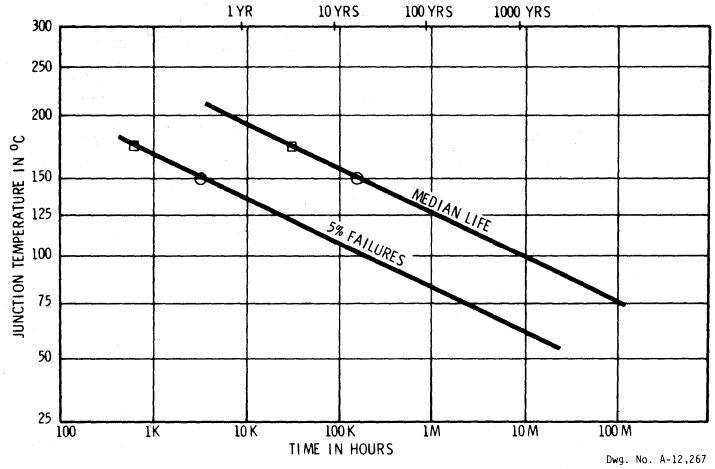


Figure 2
MEDIAN LIFE

Although not as statistically accurate as the median lifetime, the 5% failure point can be read from Figure 1. It is plotted in Figure 2.

The median life with lower junction temperatures can now be determined by using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\theta_{JA} + T_A \text{ or } T_J = P_D\theta_{JC} + T_C$$

The median lifetime, or 50% failure point, as determined in Figure 2, is approximately 100 years at +125°C or 1,000 years at +100°C junction temperature.

The approximate failure rate (FR) can be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(8.8 \times 10^6 \text{ hours})$$
$$= 0.0011\%/1000 \text{ hours} = 11 \text{ FIT}$$

where *FIT* = failures per 10^9 unit-hours

TABLE II
SERIES ULN-2000A AND ULN-2800A FAILURE RATE

T_J (°C)	Median Life (h)	Failure Rate (%/100 h)	Failures In Time (No./10^9 unit-hours)
125	1.0×10^6	0.10	1000
100	8.8×10^6	0.011	110
75	1.0×10^8	0.0010	10
50	8.8×10^8	0.00011	1.1

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calcualted from internal power dissipation and external ambient temperature, would not reach the 5% failure point in 10 years. Lowering the junction temperature to +70°C increases the time to the 5% failure point to 300 years.

A complete sequence of environmental tests on Series ULN-2000A and ULN-2800A, including temperature cycle, pressure cooker, and biased humidity tests are continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K. E., and Bird, D. W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208-213.

NOTES

SECTION 4—HIGH-CURRENT (≥1 A) INTERFACE DRIVERS

SELECTION GUIDE

(in order of tested output current rating)

I_{OUT}	V_{OUT}	Outputs	Device Type	Page
±1.0 A	26 V	Half-Bridge	UDN-2943Z	4-51
±1.0 A Linear	28 V	Power Op Amp	ULN-3751Z	4-93
±1.0 A Linear	40 V	Dual Power Op Amp	ULN-3753B/W	4-98
±1.0 A Linear	40 V	Dual Power Op Amp	ULN-3755B/W	4-107
1.0 A	50 V	Sink 4†	UCN-5813/14B	5-41
1.0 A	70 V	Sink 2	UDN-5725M	4-117
1.0 A	80 V	Sink 4†	UCN-5813/14B-1	5-41
1.0 A	150 V	Sink 4	ULN-7064/68/74B	2-15
1.25 A	50 V	Source/Sink 2	ULN-2061M	4-3
1.25 A	50 V	Sink 4	ULN-2064/66/68/70B	4-3
1.25 A	50 V	Source/Sink 4	ULN-2074B	4-3
1.25 A	60 V	Sink 4	UDN-2540B	4-14
−1.5 A	35 V	Source 4	UDN-2941B	4-48
1.5 A	−50 V	Sink 4	UDN-2841/45B	4-19
−1.5 A	−50 V	Source 4	UDN-2845B	4-19
1.5 A	80 V	Source/Sink 2	ULN-2062M	4-3
1.5 A	80 V	Sink 4	ULN-2065/67/69/71B	4-3
1.5 A	80 V	Source/Sink 4	ULN-2075B	4-3
1.75 A	60 V	Sink 4†	UCN-5825B	5-59
1.75 A	80 V	Sink 4†	UCN-5826B	5-59
±2.0 A	15 V	3 × Half-Bridge	UDN-2906W	*
±2.0 A	15 V	3 × Half-Bridge	UDN-2931B/W	4-31
±2.0 A	35 V	Half-Bridge	UDN-2935/50Z	4-34
±2.0 A	40 V	Full-Bridge	UDN-2952B/W	4-64
±2.0 A	50 V	Full-Bridge	UDN-2953B/54W	4-70
±2.0 A	50 V	2 × Full-Bridge	UDN-2998W	4-89
2.0 A	80 V	Sink 4	UDN-2545B	4-17
±3.0 A	45 V	3 × Half-Bridge	UDN-2936/37W	4-40
3.0 A PWM	45 V	Source/Sink 2	UDN-2962W	4-75
3.0 A	90 V	Sink 4	UDN-7078W	4-121
4.0 A	50 V	Sink 4	UDN-2878W	4-25
4.0 A	50 V	Sink 3	UDN-2938W/39B	4-46
4.0 A	50 V	Source/Sink 2	UDN-2975W	4-86
4.0 A PWM	50 V	Source/Sink 2	UDN-2965W-2	4-81
4.0 A	60 V	Source/Sink 2	UDN-2976W	4-86
−4.0 A	60 V	Source 4	UDN-2944W	4-55
4.0 A	80 V	Sink 4	UDN-2879W	4-25
−6.0 A	60 V	Source 4	UDN-2948W	4-58
±8.0 A	50 V	Half-Bridge	UDN-2951Z/55W	4-61

Current ratings shown are maximum tested condition; allowable peak, or start-up currents are generally higher; voltage ratings shown are maximum allowable. Devices with ratings of less than 1 A are listed in Section 3.

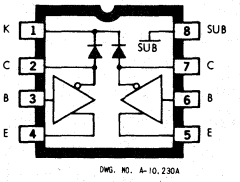
†Latched Smart Power drivers.

*New product. Contact factory for information.

ULN-2061M THROUGH ULN-2075B
1.5 A DARLINGTON SWITCHES

FEATURES

- TTL, DTL, CMOS Compatible Inputs
- Transient-Protected Outputs
- Loads to 480 Watts
- Plastic Dual In-Line Packages
- Heat-Sink Contact Tabs on Quad Arrays



ULN-2061M
ULN-2062M

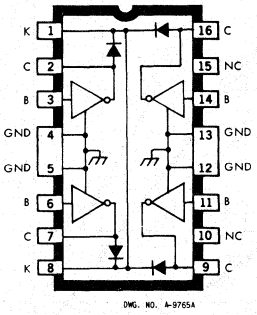
HIGH-VOLTAGE, HIGH-CURRENT Darlington arrays ULN-2061M through ULN-2075B are designed as interface between low-level logic and a variety of peripheral loads such as relays, solenoids, dc and stepper motors, multiplexed LED and incandescent displays, heaters, and similar loads to 480 watts (1.5 A per output, 80 V, 26% duty cycle).

The devices have a minimum output breakdown of 50 V and a minimum $V_{CE(SUS)}$ of 35 V measured at 100 mA, or a minimum output breakdown of 80 V and a minimum $V_{CE(SUS)}$ of 50 V.

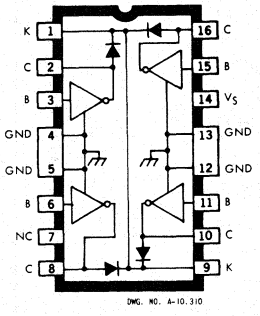
Dual-driver arrays ULN-2061M and ULN-2062M are used for common-emitter (externally connected), or emitter-follower applications. Both devices are supplied in miniature 8-pin dual in-line plastic packages.

Quad drivers ULN-2064B, ULN-2065B, ULN-2068B and ULN-2069B are intended for use with TTL, low-speed TTL, and 5 V MOS logic. Types ULN-2065B and ULN-2069B are selected for the 80 V minimum output breakdown specification. Types ULN-2068B and ULN-2069B have predriver stages and are most suitable for applications requiring high gain (low input-current loading).

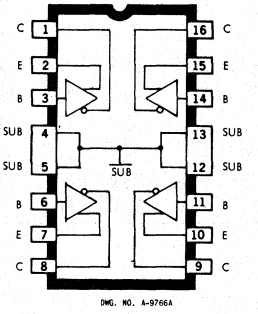
4



ULN-2064B
ULN-2065B



ULN-2068B
ULN-2069B



ULN-2074B
ULN-2075B

Isolated Darlington arrays ULN-2074B and ULN-2075B are identical to Types ULN-2064B and ULN-2065B except for the isolated Darlington pinout and the deletion of suppression diodes. These switches are for emitter-follower or similar isolated-Darlington applications.

All quad Darlington arrays (suffix "B" devices) are supplied in a 16-pin plastic dual in-line package with heat-sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat sinks for increased power dissipation with standard IC sockets and printed wiring boards.

SELECTION GUIDE

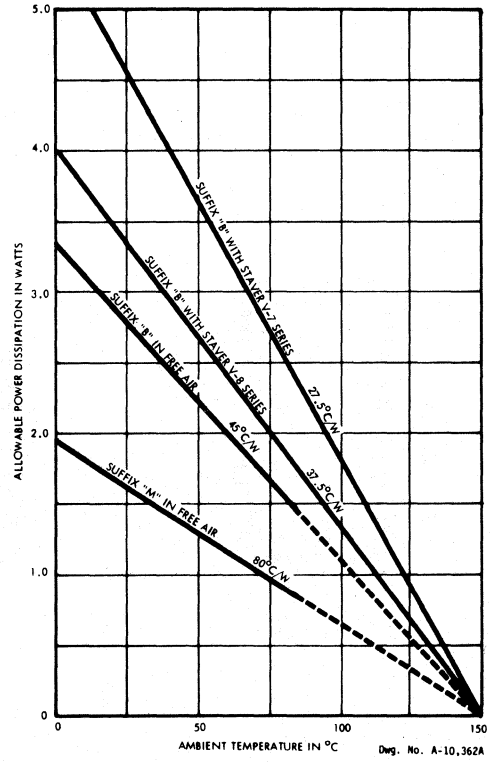
Part Number	MAX. V_{CEX}	Min. $V_{CE(SUS)}$	Max. V_{IN}	Application
ULN-2061M	50 V	35 V	30 V	TTL, DTL, Schottky TTL,
ULN-2062M	80 V	50 V	60 V	and 5 V CMOS
ULN-2064B	50 V	35 V	15 V	TTL, DTL, Schottky TTL
ULN-2065B	80 V	50 V	15 V	and 5 V CMOS
ULN-2068B	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULN-2069B	80 V	50 V	15 V	and 5 V CMOS
ULN-2074B	50 V	35 V	30 V	General Purpose
ULN-2075B	80 V	50 V	60 V	

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature for Any One Driver (unless otherwise noted)

Output Voltage, V_{CEX} . . . . . See Guide
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . See Guide
Output Current, I_{OUT} (Note 1) . . . . . 1.75 A
Input Voltage, V_{IN} (Note 2) . . . . . See Guide
Input Current, I_B (Note 3) . . . . . 25 mA
Supply Voltage, V_S (ULN-2068/69B) . . . . . 10 V
Total Package Power Dissipation . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to −150°C

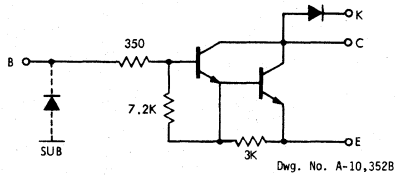
NOTES:
1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is referenced to the substrate (no connection to other pins) for Type ULN-2061/62M and ULN-2074/75B; reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

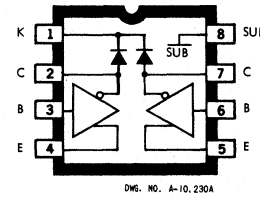


ULN-2061M AND ULN-2062M

PARTIAL SCHEMATIC



Dwg. No. A-10,352B



DWG. NO. A-10,230A

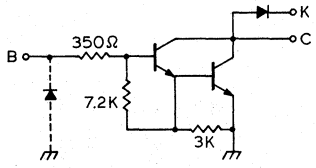
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	1	ULN-2061M	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN-2062M	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2061M	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2062M	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 µA	—	1.1	V
				I_C = 750 mA, I_B = 935 µA	—	1.2	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
				I_C = 1.25 A*, I_B = 2.0 mA	—	1.4	V
			ULN-2062M	I_C = 1.5 A*, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	1.4	4.3	mA
				V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			ULN-2061M	V_{CE} = 2.0V, I_C = 1.25 A*	—	2.5	V
			ULN-2062M	V_{CE} = 2.0 V, I_C = 1.5 A*	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN-2061M	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN-2062M	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

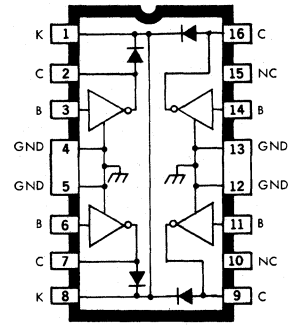
*Pulse-Test

ULN-2064B AND ULN-2065B

PARTIAL SCHEMATIC



Dwg. No. A-10,353C



Dwg. No. A-9765A

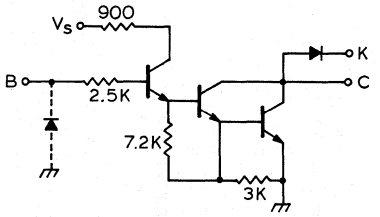
(SIMILAR TO ULN-2074B AND ULN-2075B)

ELECTRICAL CHARACTERISTICS at ± 25°C (unless otherwise noted)

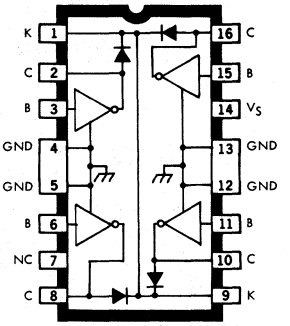
Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2064B	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN-2065B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2064B	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2065B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 µA	—	1.1	V
				I_C = 750 mA, I_B = 935 µA	—	1.2	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
				I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN-2065B	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	1.4	4.3	mA
				V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			ULN-2064B	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.5	V
			ULN-2065B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 $_{out}$	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN-2064B	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN-2065B	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

ULN-2068B AND ULN-2069B

PARTIAL SCHEMATIC



Dwg. No. A-10,354C



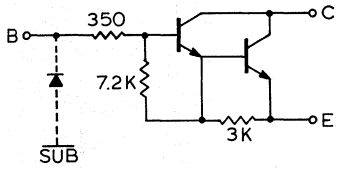
Dwg. No. A-10,310

ELECTRICAL CHARACTERISTICS AT +25°C, V_s = 5.0 V (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2068B	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN-2069B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2068B	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2069B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_{IN} = 2.75 V	—	1.1	V
				I_C = 750 mA, I_{IN} = 2.75 V	—	1.2	V
				I_C = 1.0 A, I_{IN} = 2.75 V	—	1.3	V
				I_C = 1.25 A, I_{IN} = 2.75 V	—	1.4	V
			ULN-2069B	I_C = 1.5 A, I_{IN} = 2.75 V	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.75 V	—	550	µA
				V_{IN} = 3.75 V	—	1000	µA
Input Voltage	$V_{IN(ON)}$	5	ULN-2068B	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.75	V
			ULN-2069B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.75	V
Supply Current	I_S	8	Both	I_C = 500 mA, V_{IN} = 2.75 V	—	6.0	mA
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 $_{out}$, I_C = 1.25 A	—	1.5	µs
Clamp Diode Leakage Current	I_R	6	ULN-2068B	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = 70°C	—	100	µA
			ULN-2069B	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = 70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

ULN-2074B AND ULN-2075B

PARTIAL SCHEMATIC



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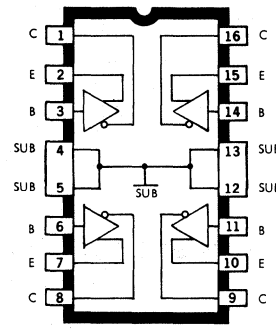


Dwg. No. A-9766A

(SIMILAR TO ULN-2064B AND ULN-2065B)

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2074B	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
			ULN-2075B	V_{CE} = 80 V	—	100	µA
				V_{CE} = 50 V, T_A = 70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2074B	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2075B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 µA	—	1.1	V
				I_C = 750 mA, I_B = 935 µA	—	1.2	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.3	V
				I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN-2075B	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	1.4	4.3	mA
				V_{IN} = 3.75 V	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
			ULN-2074B	V_{CE} = 2.0 V, I_C = 1.25 A	—	2.5	V
			ULN-2075B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	Both	0.5 E_{in} to 0.5 $_{out}$	—	1.5	µs

TEST FIGURES

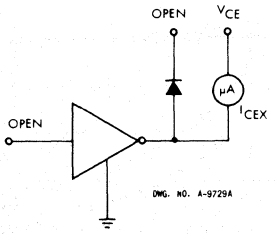


Figure 1

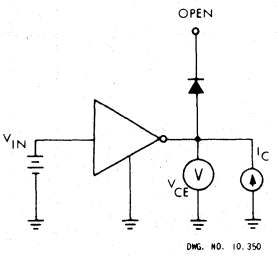


Figure 2

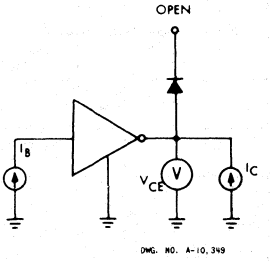


Figure 3

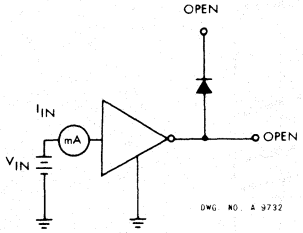


Figure 4

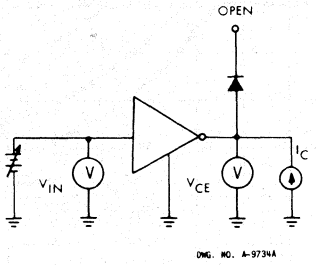


Figure 5

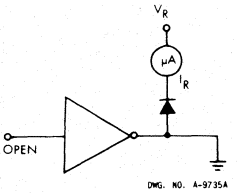


Figure 6

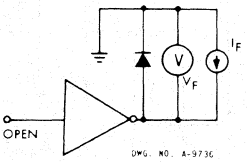


Figure 7

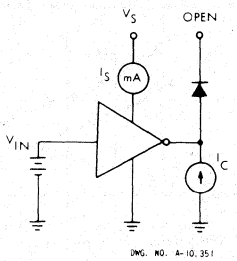
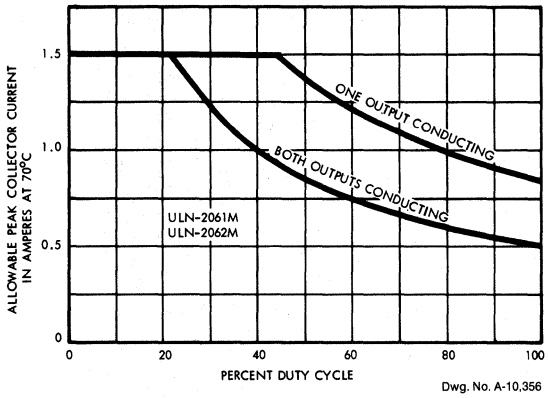
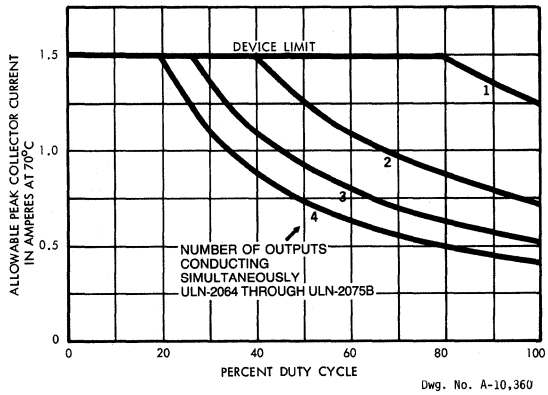


Figure 8

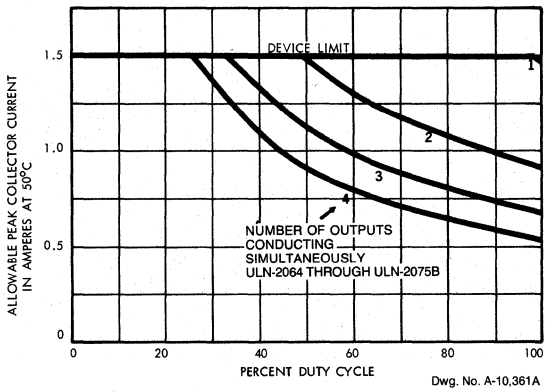
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



Dwg. No. A-10,356



Dwg. No. A-10,360



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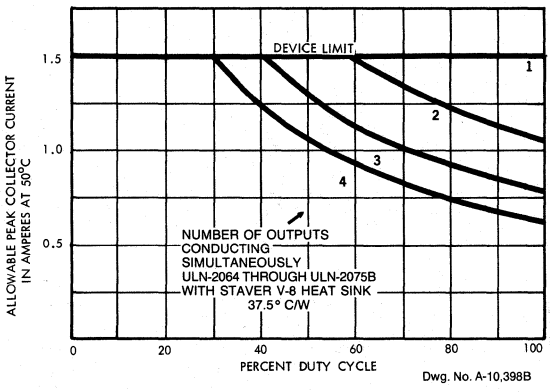
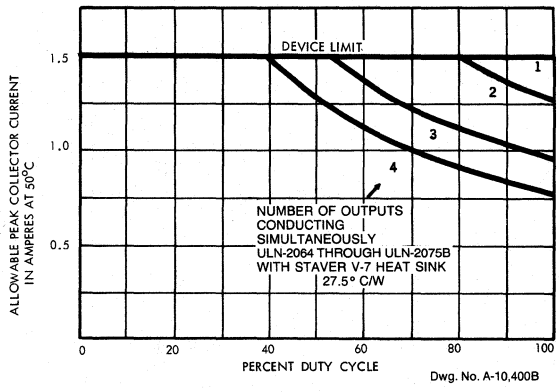
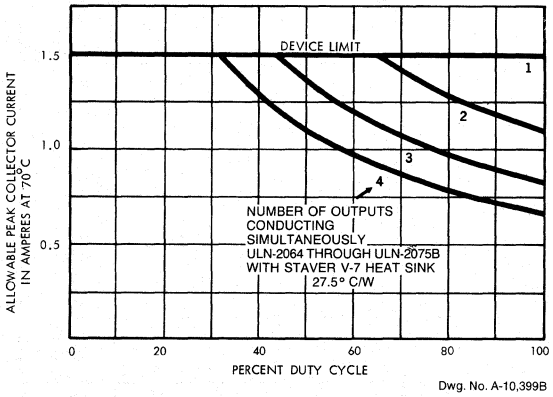


Dwg. No. A-10,398B

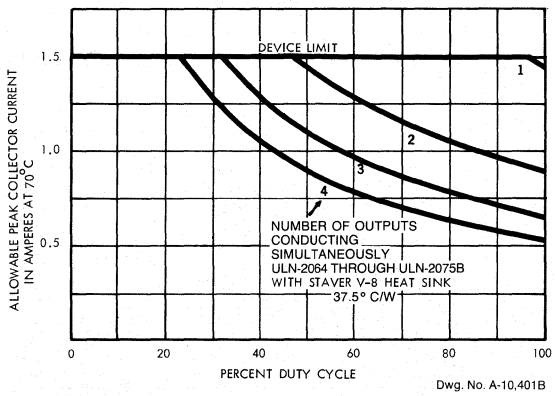


Dwg. No. A-10,400B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE (Continued)



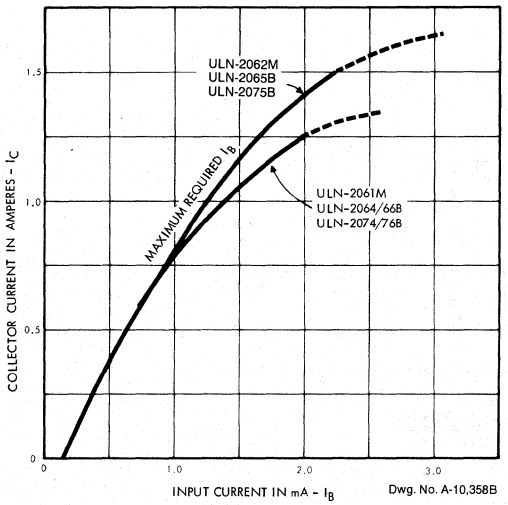
Dwg. No. A-10,399B



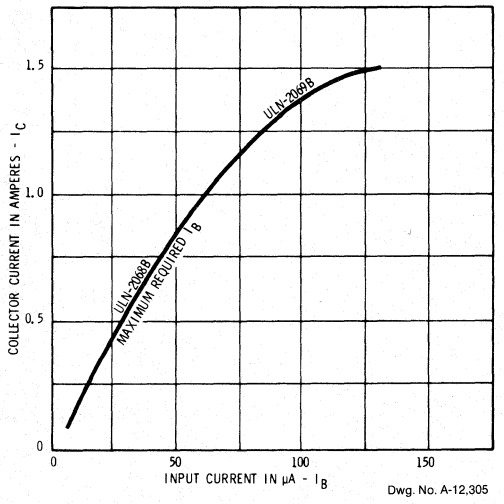
Dwg. No. A-10,401B

4

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT AT +25°C

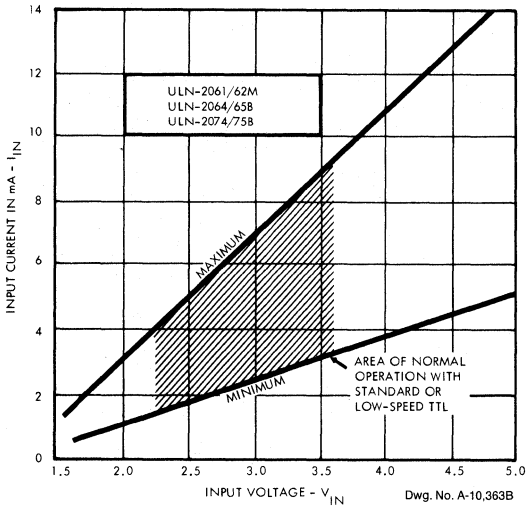


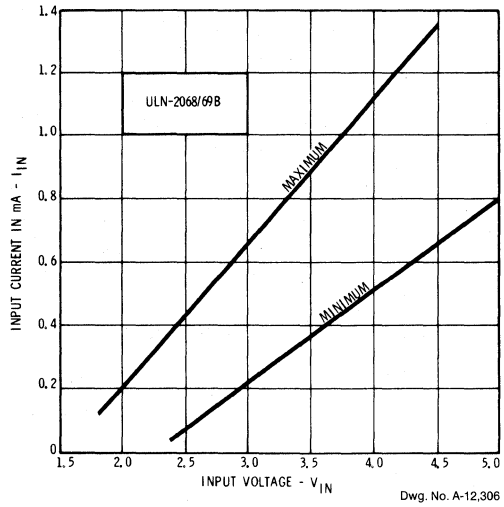
Dwg. No. A-10,358B



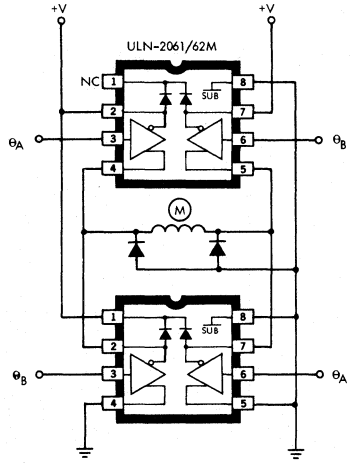
Dwg. No. A-12,305

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE AT +25°C



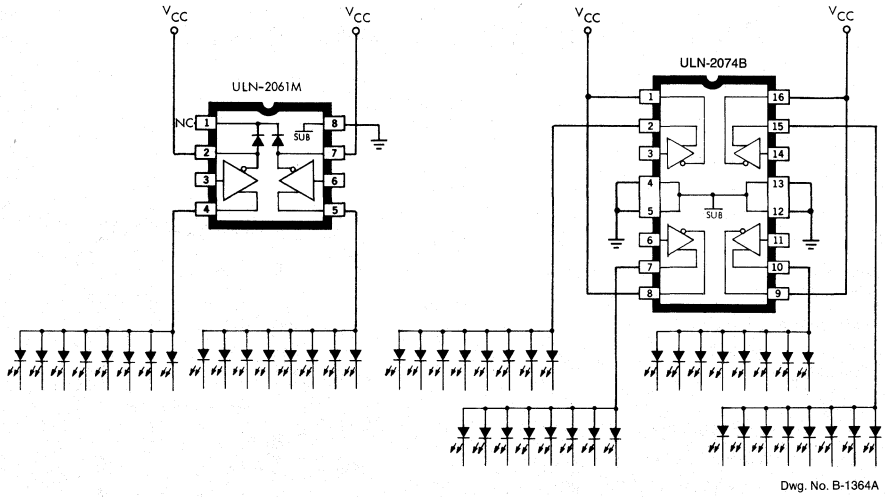


TYPICAL APPLICATION



BIDIRECTIONAL MOTOR CONTROL

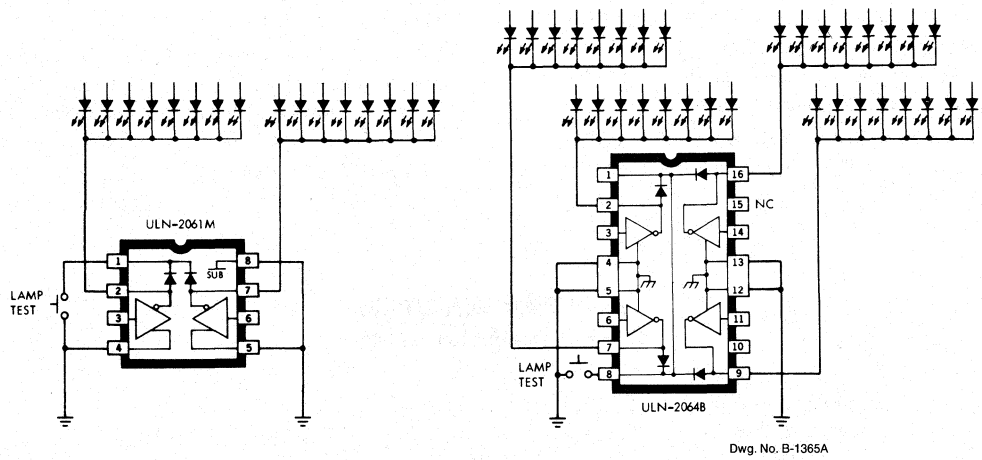
TYPICAL APPLICATIONS (Continued)



Dwg. No. B-1364A

COMMON-ANODE LED DRIVERS

(Series UDN-2980A devices can be used in similar applications at currents of up to 500 mA)



Dwg. No. B-1365A

COMMON-CATHODE LED DRIVERS

(Type ULN-2068B is also applicable)

UDN-2540B
QUAD-NAND GATE POWER DRIVER

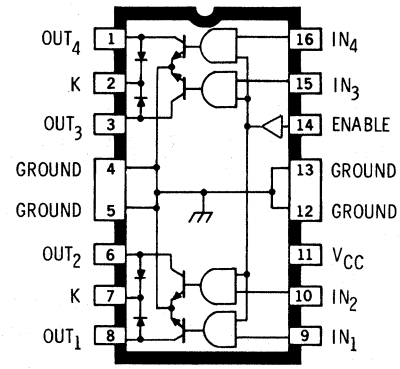
FEATURES

- 1.5 A Output Current
- Output Voltage to 60 V
- Integral Transient-Suppression Diodes
- Efficient Input/Output Pin Structure
- TTL, CMOS, PMOS, NMOS Compatible

Combining NAND logic gates and high-current bipolar outputs, the UDN-2540B power and relay driver provides interface between low-level signal-processing circuits and power loads to 350 W. Each of the four independent outputs of this device can sink up to 1.5 A in the ON state. In the OFF state the drivers will withstand at least 60 V. Transient-suppression clamp diodes and a minimum 35 V output sustaining voltage allow their use with many inductive loads.

Typical applications include relays, solenoids, and dc stepping motors. It can also be used to drive high-current incandescent lamps, LEDs, and heaters. In display applications, the diodes can be used to perform the "lamp test" function.

Inputs are compatible with most TTL, DTL, LSTTL, and 5 V or 12 V CMOS and PMOS logic.



Dwg. No. A-11,561

Each of the four outputs is recommended for continuous load currents to 1.25 A. Outputs can be paralleled for higher load currents.

The UDN-2540B is supplied in a 16-pin dual-in-line package with heat-sink contact tabs. This configuration allows attachment of an inexpensive heat sink and fits a standard integrated circuit socket or printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

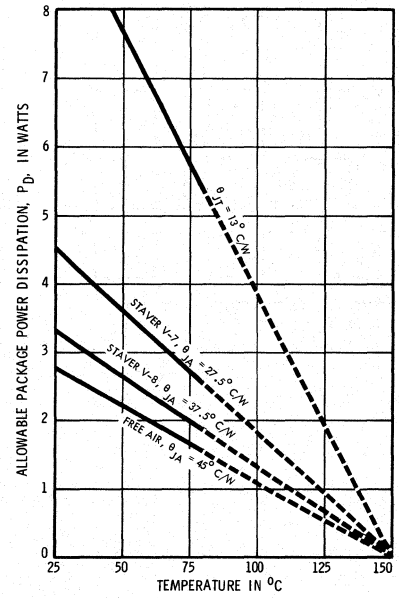
Output Voltage, V_{CE}	60 V
Output Current, I_{OUT}	1.5 A
Supply Voltage, V_{CC}	18 V
Input Voltage, V_{IN}	18 V
Power Dissipation, P_D (Each Driver)	2.5 W
(Total Package)	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_{TAB} = +70°C, V_{CC} = 4.75 V to 12.6 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.7 V, V_{ENABLE} = 2.0 V	—	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{ENABLE} = 0.7 V	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{ENABLE} = 0.7 V	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 250 mA, V_{IN} = V_{ENABLE} = 2.0 V	—	1.0	V
		I_{OUT} = 500 mA, V_{IN} = V_{ENABLE} = 2.0 V	—	1.1	V
		I_{OUT} = 750 mA, V_{IN} = V_{ENABLE} = 2.0 V	—	1.25	V
		I_{OUT} = 1.0 A, V_{IN} = V_{ENABLE} = 2.0 V	—	1.4	V
		I_{OUT} = 1.25 A, V_{IN} = V_{ENABLE} = 2.0 V	—	1.6	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	—	0.7	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.0 V	—	20	µA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.4 V	—	−200	µA
Input Clamp Voltage	V_{IK}	I_{IN} or I_{ENABLE} = −10 mA	—	−1.5	V
Total Supply Current	I_{CC}	V_{IN}* = V_{ENABLE} = 2.0 V, V_{CC} = 5.0 V, Outputs Open	—	8.0	mA
		V_{IN}* = V_{ENABLE} = 2.0 V, V_{CC} = 15 V, Outputs Open	—	33	mA
		V_{IN}* = V_{ENABLE} = 0.7 V, V_{CC} = 5.0 V	—	2.0	mA
		V_{IN}* = V_{ENABLE} = 0.7 V, V_{CC} = 15 V	—	7.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	2.1	V
		I_F = 1.25 A	—	2.5	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, V_{IN} = V_{ENABLE} = 2.0 V, D_1 + D_2 or D_3 + D_4	—	100	µA

*All inputs simultaneously, all other tests are performed with each input tested separately.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

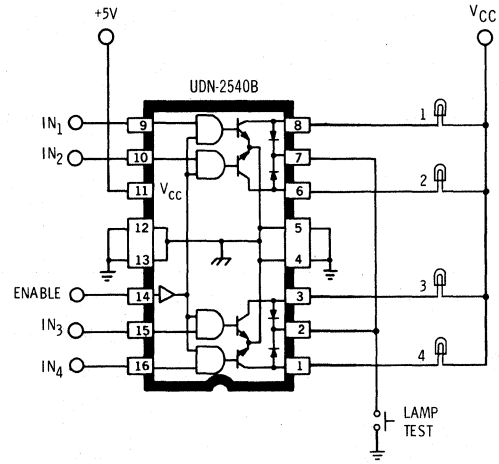


Dwg. No. A-11,793B

APPLICATIONS

Typical applications for this device include driving incandescent lamps and dc stepper motors. Lamps with steady-state current ratings up to 150 mA can be driven without current limiting or warming resistors (assumes 1.5 A peak in-rush). The internal diodes can be used to perform the "lamp test" function as shown. Bifilar (unipolar) stepper motors can be driven directly. The internal transient-suppression diodes prevent damage to the output transistor from positive high-voltage inductive spikes as the output switches OFF.

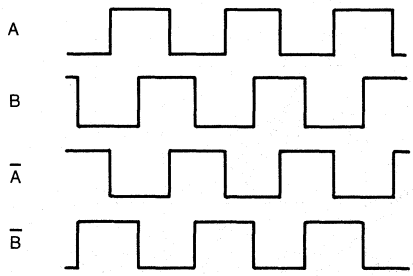
INCANDESCENT LAMP DRIVER



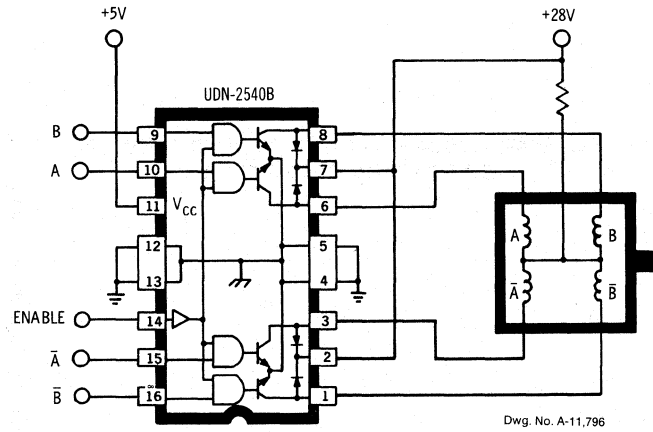
Dwg. No. A-12,048A

STEPPER-MOTOR DRIVER

INPUT WAVEFORMS



Dwg. No. A-11,795

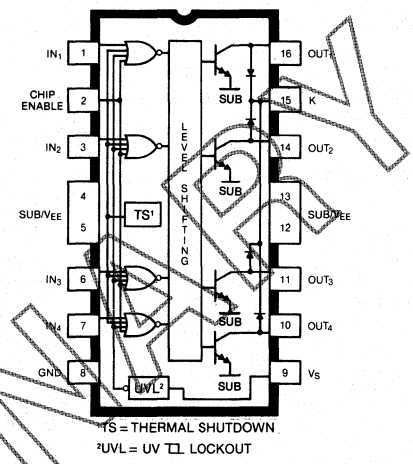


Dwg. No. A-11,796

UDN-2545B
UNIVERSAL QUAD DRIVER

FEATURES

- Output Current of 2 A
- 80 V Min. Output Breakdown
- 40 V Output Sustaining Voltage
- PMOS, CMOS, TTL Compatible
- Built-in Thermal Shutdown
- Output Transient Protection
- CHIP ENABLE for Microprocessor Control
- Under-Voltage Protection



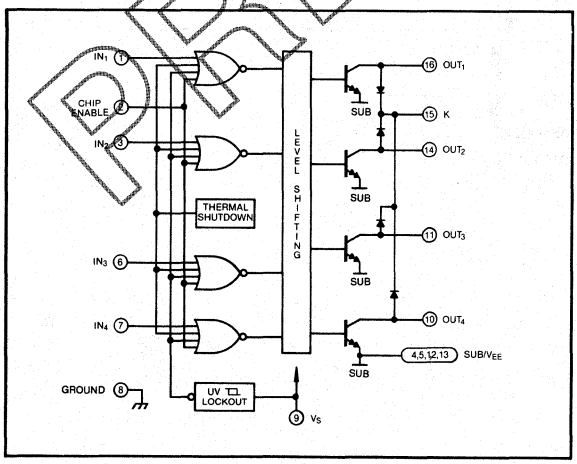
[1]TS = THERMAL SHUTDOWN
[2]UVL = UV ⊓ LOCKOUT

The UDN-2545B is a four-channel high-current, high-voltage integrated circuit designed to provide the interface between stepper motors and microprocessor or logic motor control circuitry. The UDN-2545B will accept most standard logic signal inputs and provide motor drive current to both positive and negative supply rails.

The UDN-2545B is capable of sinking up to 2.5 A and maintaining an output OFF voltage of 80 volts. This device incorporates some unique features such as under-voltage protection, thermal shutdown, and CHIP ENABLE control. The under-voltage protection guards against supply line transients and has built-in hystersis. The thermal shutdown with hystersis is to guard against damage to the device. CHIP ENABLE is especially good for use in microprocessor control. All outputs have clamp diodes for suppression of inductive loads.

The UDN-2545B is supplied in a 16 pin plastic dual in-line package with heat-sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat sinks for increased power dissipation with standard IC sockets and printed wiring boards.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{CE}	80 V
Emitter Supply Voltage, V_{EE}	−25 V
Logic Supply Voltage, V_S	20 V
Output Current, I_{OUT}	2.5 A
Input Voltage, V_{IN}	25 V
Package Power Dissipation, P_D	2.77 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

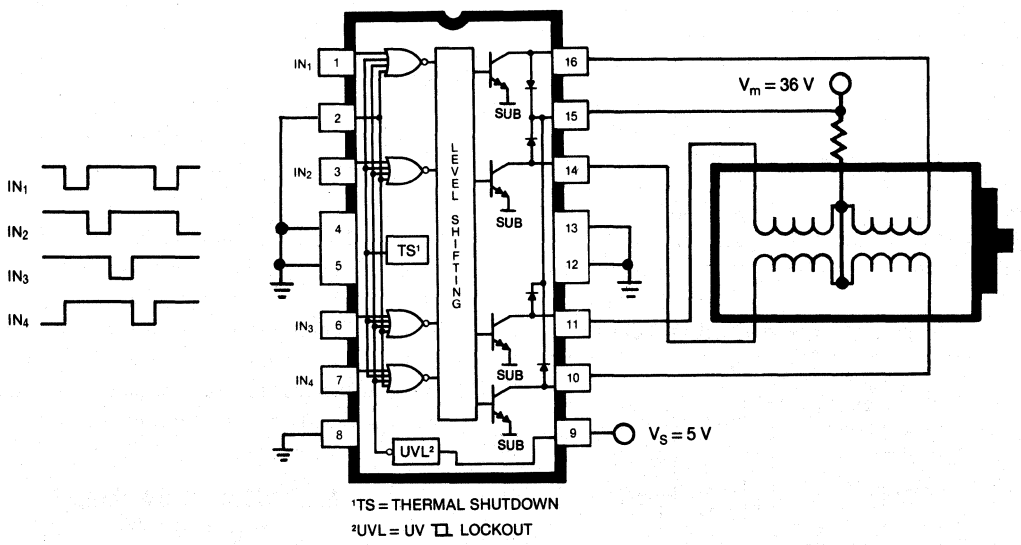
*Derate at the Rate of 22.2 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5 V to 15 V, V_{EE} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 80 V, V_{IN} = 2.0 V, Other Inputs = 0 V	—	500	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 2 A, Inputs = 5.0 V, L = 3 mH	40	—	V
Output Saturation Voltage*	$V_{CE(SAT)}$	I_{OUT} = 2 A, Inputs = 0 V	—	2.2	V
Clamp Diode Leakage Current	I_R	V_R = 80 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	2.5	V
Input Current	$I_{IN(ON)}$	V_{IN} = 0.8 V	—	−250	µA
	$I_{IN(OFF)}$	V_{IN} = V_S	—	50	µA
Supply Current	$I_{S(ON)}$	All Inputs = 0.8 V, V_S = 5.0 V	—	65	mA
		All Inputs = 0.8 V, V_S = 15 V	—	70	mA
	$I_{S(OFF)}$	All Inputs = 5.0 V, V_S = 5.0 V	—	20	mA
		All Inputs = 15 V, V_S = 15 V	—	30	mA

*Pulse Test

STEPPER MOTOR APPLICATION

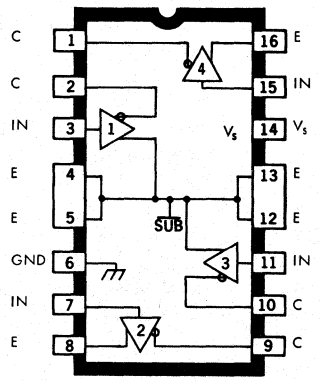


[1]TS = THERMAL SHUTDOWN
[2]UVL = UV ⊓ LOCKOUT

UDN-2841B AND UDN-2845B
QUAD DARLINGTON 1.5 A DRIVERS

FEATURES

- Inputs Compatible with DTL, TTL, LSTTL, CMOS
- −50 V Darlington Outputs
- Current-Sink or Sink-and-Source Combination
- 16-Pin Dual In-Line Plastic Package



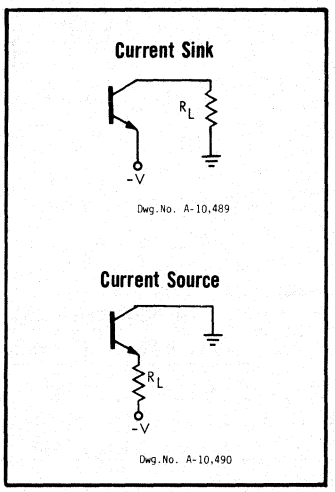
DWG. NO. A-10,323B

THIS PAIR OF QUAD DARLINGTON switches is designed for high-current, high-voltage peripheral driver applications. They provide solutions to interface problems involving electronic discharge printers, d-c motor drive (bipolar or unipolar), telephone relays, PIN diodes, LEDs, and other high-current loads operating with negative voltage supplies.

Type UDN-2841B is for current-sink applications in which the load is connected to ground. The outputs switch the negative supply. The input PNP transistor in each driver serves as a level translator. The first NPN stage provides current gain to drive the Darlington-pair outputs.

Type UDN-2845B is a current-sink, current-source combination in a single dual in-line plastic package. It can be used in bipolar switching applications in which neither end of the load is at ground potential.

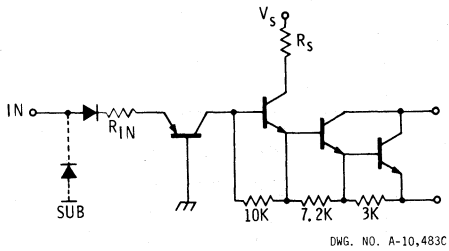
Types UDN-2841 and UDN-2845B are intended for use with 5 V TTL, Schottky TTL, DTL, and CMOS logic. Both drivers reduce component count, lower system costs, and reduce circuit and board complexity.



ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
For Single Darlington Output
(Unless Otherwise Noted)

Output Voltage, $V_{CE(OFF)}$ . . . . . 50 V
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . 35 V
Substrate Voltage, V_{SUB} . . . . . −50 V
Continuous Output Current, I_{OUT} . . . . . 1.75 A
Supply Voltage, V_S . . . . . 10 V
Input Voltage, V_{IN} . . . . . 10 V
Power Dissipation, P_D (one output) . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

SCHEMATIC
(Each Driver)

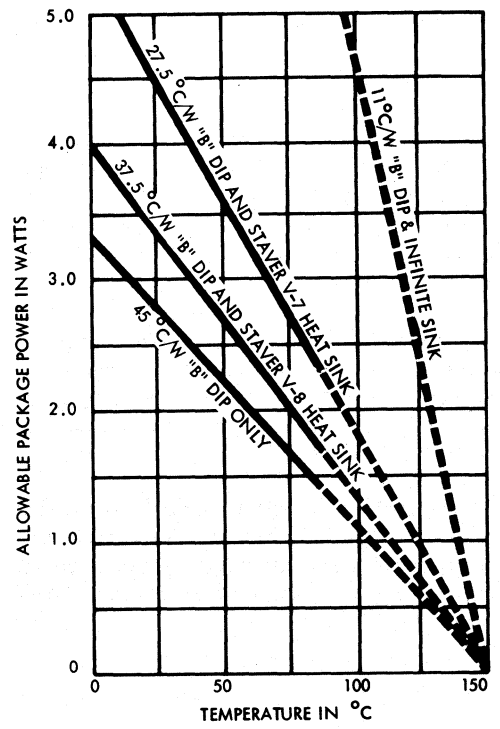


DWG. NO. A-10,483C

Type Number	Resistor Values in kΩ			
	Amplifier 1 & 3		Amplifier 2 & 4	
	R_{IN}	R_S	R_{IN}	R_S
UDN-2841B	3.3	15	3.3	15
UDN-2845B	3.3	15	3.3	1

NOTE: The substrate terminals must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal device operation.

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE



DWG. NO. A-10,488C

ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted)

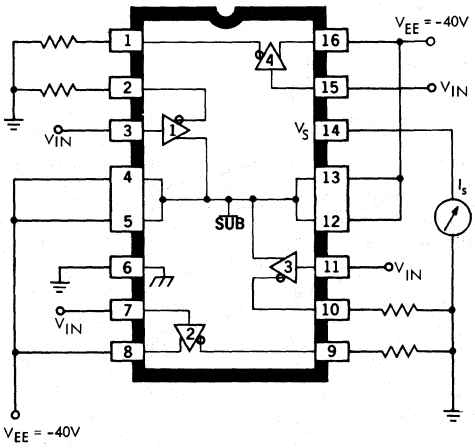
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{EE} = −50V, V_{IN} = 0.4V, T_A = 25°C	—	—	100	µA
		V_{EE} = −50V, V_{IN} = 0.4V, T_A = 70°C	—	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	V_{EE} = −50V, V_{IN} = 0.4 V, I_{OUT} = 100 mA	35	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 500mA	—	—	1.1	V
		I_{OUT} = 1.0A (Note 1)	—	—	1.4	V
		I_{OUT} = 1.5A (Note 1)	—	—	1.6	V
Input Current	$I_{IN(ON)}$	I_{OUT} = 500mA, V_{IN} = 2.4V	—	300	500	µA
Input Voltage (Note 1)	$V_{IN(ON)}$	I_{OUT} = 1.5A	—	—	2.4	V
Supply Current (Note 1)	I_S	I_{OUT} = 500mA, UDN-2841B, UDN-2845B (Note 2)	—	2.5	3.75	mA
		I_{OUT} = 500mA, UDN-2845B (Note 3)	—	3.3	7.5	mA
Turn-On Delay	$t_{pd(ON)}$	R_L = 39Ω, 0.5 V_{IN} to 0.5 V_{OUT}	—	—	2.0	µs
Turn-Off Delay	$t_{pd(OFF)}$	R_L = 39Ω, 0.5 V_{IN} to 0.5 V_{OUT}	—	—	5.0	µs

NOTES:
1. Each driver tested separately.
2. Drivers 1 & 3 (sink drivers) only, V_S = 0V, V_{EE} = −40V.
3. Drivers 2 & 4 (source drivers) only, V_S = 5V, V_{EE} = −40V.

4

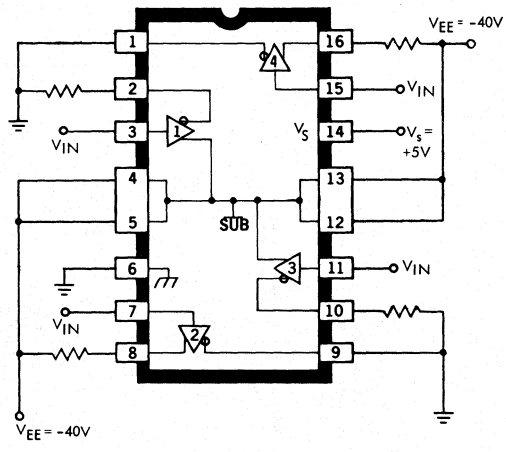
TEST CIRCUITS

UDN-2841B



DWG. NO. A-10,487A

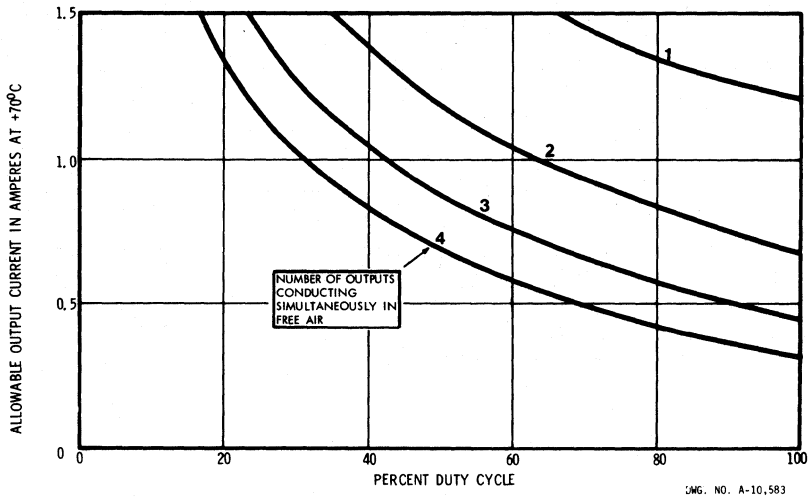
UDN-2845B



DWG. NO. A-10,484A

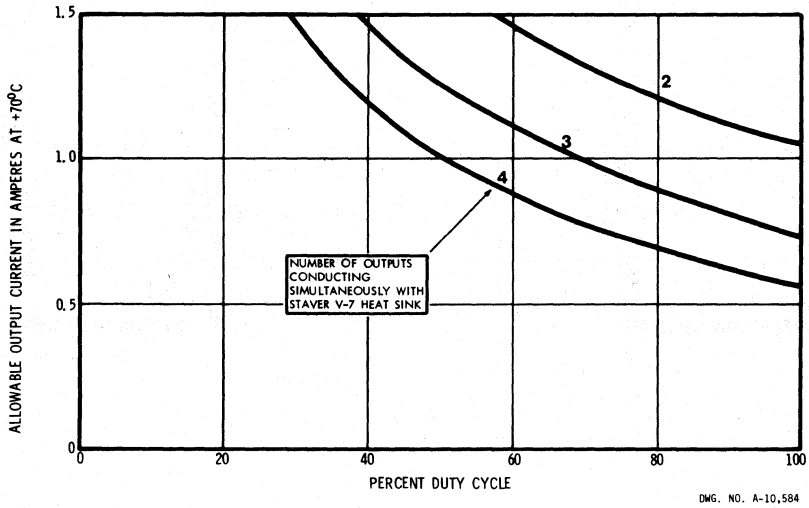
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

WITHOUT HEAT SINK



DWG. NO. A-10,583

WITH STAVER V-7 HEAT SINK



DWG. NO. A-10,584

OUTPUT-STAGE TRANSIENT PROTECTION

When switching inductive loads, the output transistors of UDN-2841B and UDN-2845B drivers should be protected by a suitable clamping technique. The simplest approach is to clamp each output with a discrete diode, as shown in Figures 1 and 2.

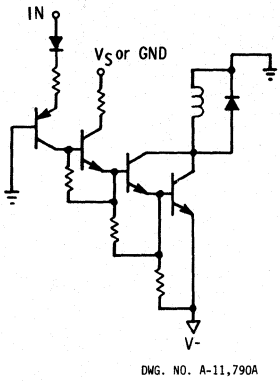


Figure 1
UDN-2841B

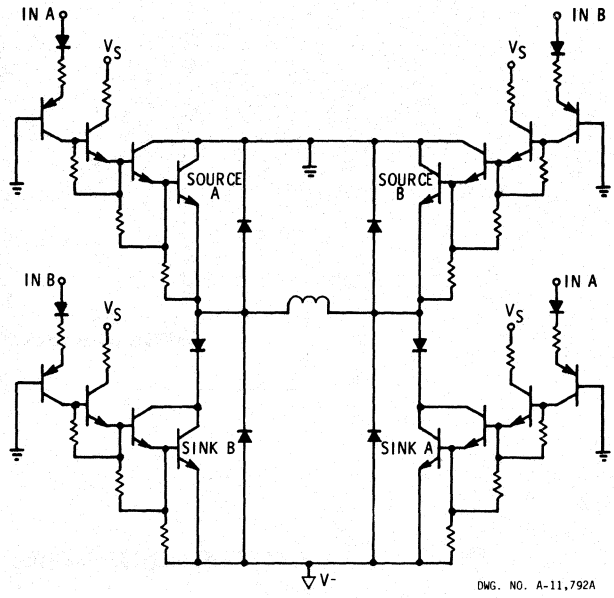


Figure 2
UDN-2845B

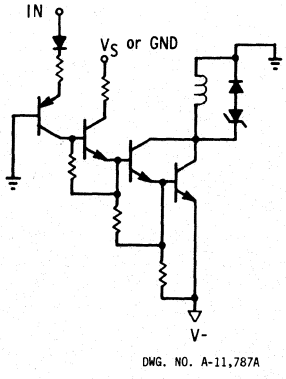
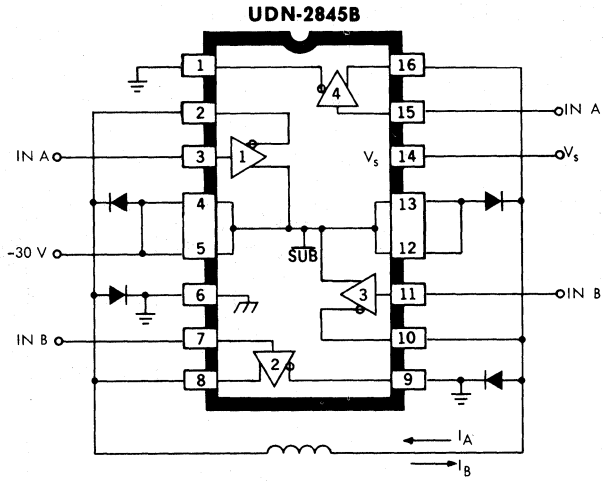


Figure 3
UDN-2841B

For improved turnoff, a combination diode/Zener diode scheme can be used. The Zener diode in the clamp circuit of Figure 3 allows the flyback voltage to rise above the supply voltage, speeding turnoff of the load. An appropriate resistor can be substituted for the Zener diode. With a 1 A load, substitution of a 15Ω resistor results in operation similar to that of the Zener diode circuit.

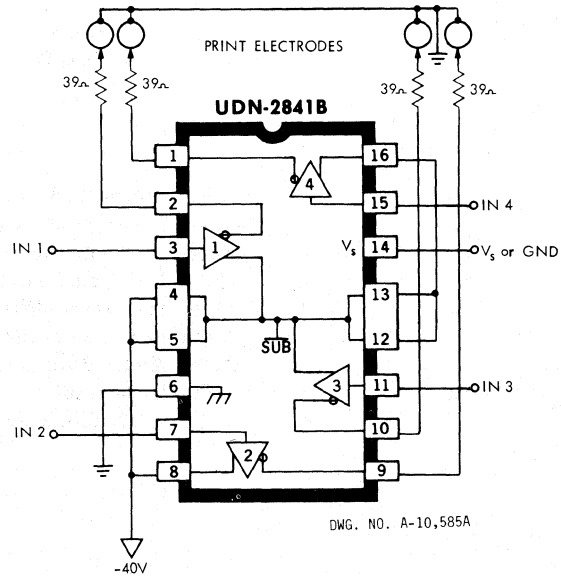
TYPICAL APPLICATIONS

BIPOLAR MOTOR DRIVER



DWG. NO. A-10,586A

ELECTROSENSITIVE PRINTER INTERFACE

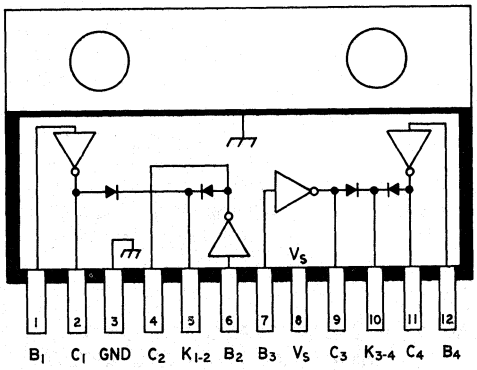


DWG. NO. A-10,585A

UDN-2878W AND UDN-2879W
QUAD HIGH-CURRENT DARLINGTON SWITCHES

FEATURES

- Output Currents to 4 A
- Output Voltages to 80 V
- Loads to 1280 W
- TTL, DTL, or CMOS Compatible Inputs
- Internal Clamp Diodes
- Plastic Single In-Line Package
- Heat-Sink Tab



DWG. NO. A-11,974

THESE QUAD DARLINGTON ARRAYS are designed to serve as interface between low-level logic and peripheral power devices such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 320 W per channel. Both integrated circuits include transient-suppression diodes that enable use with inductive loads. The input logic is compatible with most TTL, DTL, LS TTL, and 5 V CMOS logic.

Type UDN-2878W and UDN-2879W 4 A arrays are identical except for output-voltage ratings. The former is rated for operation to 50 V (35 V sustaining), while the latter has a minimum output breakdown rating of 80 V (50 V sustaining). The economical Type UDN-2878W-2 and Type UDN-2879W-2 are recommended for applications requiring load currents of 3 A or less. These less expensive devices are identical to the basic parts except for the maximum allowable load-current rating.

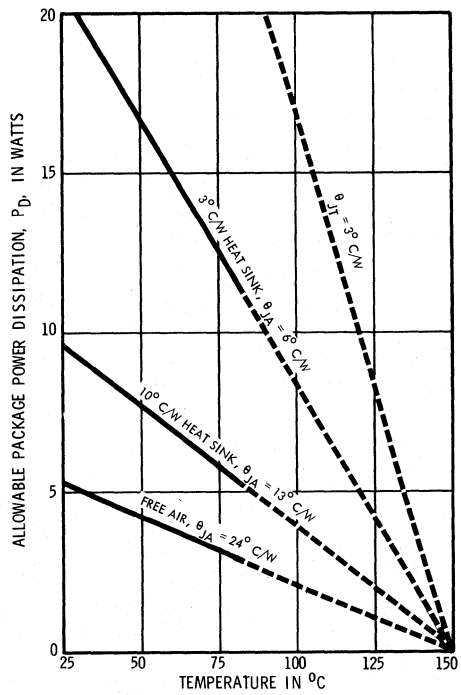
For maximum power-handling capability, all drivers are supplied in a 12-pin single in-line power-tab package. The tab is at ground potential and needs no insulation. External heat sinks are usually required for proper operation of these devices.

Device	Output Voltage	Sustaining Voltage	Output Current
UDN-2878W	50 V	35 V	4 A
UDN-2878W-2	50 V	35 V	3 A
UDN-2879W	80 V	50 V	4 A
UDN-2879W-2	80 V	50 V	3 A

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature for any driver (unless otherwise noted)

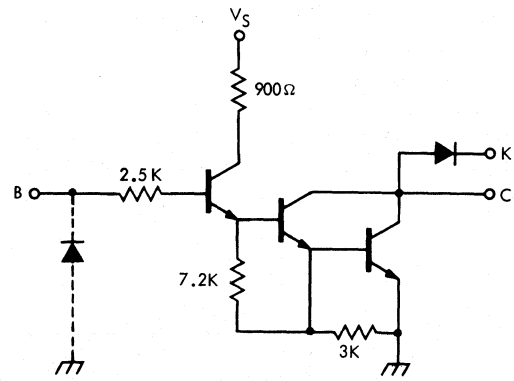
Output Voltage, V_{CEX} (UDN-2878W & UDN-2878W-2)	50 V
(UDN-2879W & UDN-2879W-2)	80 V
Output Current, I_C (UDN-2878W & UDN-2879W)	5.0 A
(UDN-2878W-2 & UDN-2979W-2)	4.0 A
Input Voltage, V_{IN}	15 V
Input Current, I_{IN}	25 mA
Supply Voltage, V_S	10 V
Total Package Power Dissipation, P_D	See Graph
Operating Ambient Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,794

PARTIAL SCHEMATIC
One of 4 Drivers



DWG. NO. A-12,037

ELECTRICAL CHARACTERISTICS at V_S = 5.0 V, T_A = +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	1	UDN-2878W/W-2	V_{CE} = 50 V	—	100	µA
				V_{CE} = 50 V, T_A = +70°C	—	500	µA
			UDN-2879W/W-2	V_{CE} = 80 V	—	100	µA
				V_{CE} = 80 V, T_A = +70°C	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	UDN-2878W/W-2	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			UDN-2879W/W-2	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 500 mA, V_{IN} = 2.75 V	—	1.1	V
				I_C = 1.0 A, V_{IN} = 2.75 V	—	1.3	V
				I_C = 2.0 A, V_{IN} = 2.75 V	—	1.5	V
				I_C = 3.0 A, V_{IN} = 2.75 V	—	1.9	V
			UDN-2878/2879W	I_C = 4.0 A, V_{IN} = 2.75 V	—	2.2	V
Input Current	I_{IN}	3	All	V_{IN} = 2.75 V	—	550	µA
				V_{IN} = 3.75 V	—	1000	µA
Input Voltage	$V_{IN(ON)}$	4	All	V_{CE} = 2.2 V, I_C = 3.0 A	—	2.75	V
			UDN-2878/2879W	V_{CE} = 2.2 V, I_C = 4.0 A	—	2.75	V
Supply Current per Driver	I_S	7	All	I_C = 500 mA, V_{IN} = 2.75 V	—	6.0	mA
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	µs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}, I_C = 3.0 A	—	1.5	µs
Clamp Diode Leakage Current	I_R	5	All	V_R = 50 V	—	50	µA
				V_R = 50 V, T_A = +70°C	—	100	µA
			UDN-2879W/W-2	V_R = 80 V	—	50	µA
				V_R = 80 V, T_A = +70°C	—	100	µA
Clamp Diode Forward Voltage	V_F	6	All	I_F = 3.0 A	—	2.5	V
			UDN-2878/2879W	I_F = 4.0 A	—	3.0	V

CAUTION: High-current tests are pulse tests or require heat sinking.

TEST FIGURES

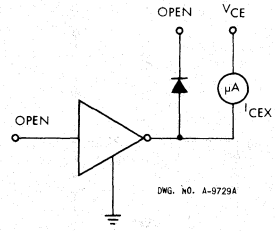


Figure 1

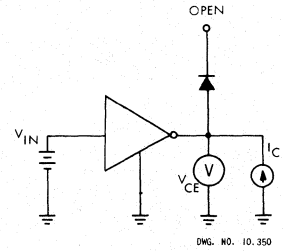


Figure 2

TEST FIGURES (Continued)

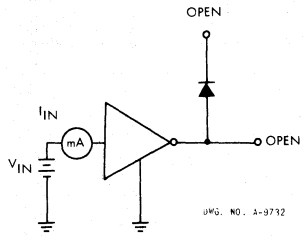


Figure 3

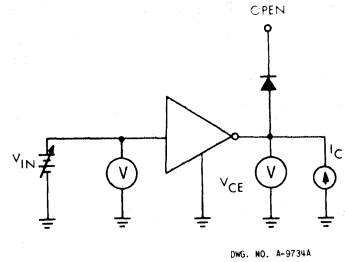


Figure 4

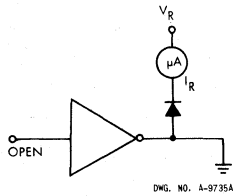


Figure 5

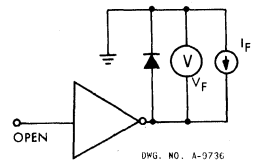


Figure 6

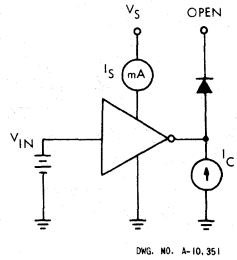
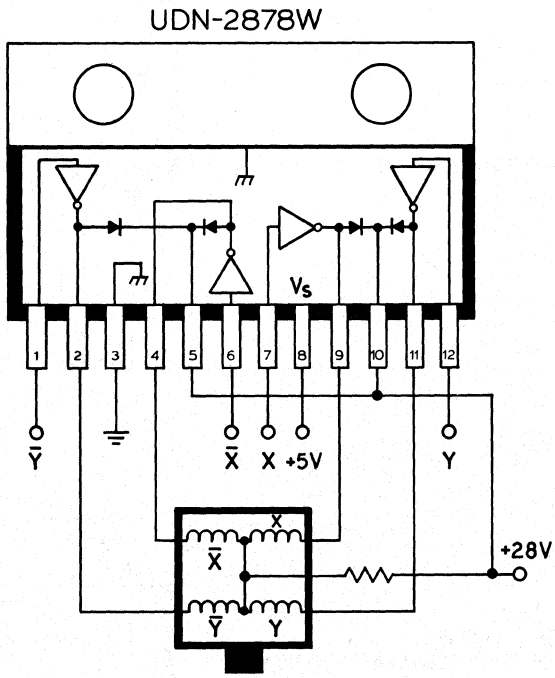


Figure 7

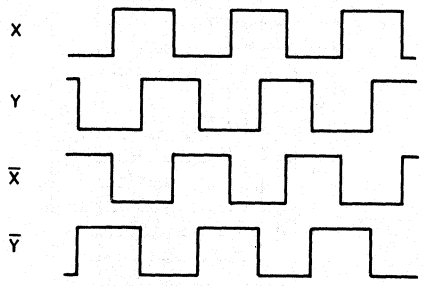
TYPICAL APPLICATIONS

STEPPER-MOTOR DRIVER



DWG. NO. A-11,975

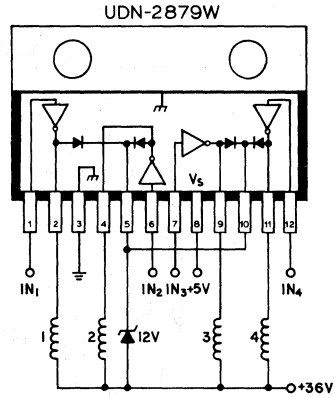
INPUT WAVEFORMS



Dwg. No. A-11,795

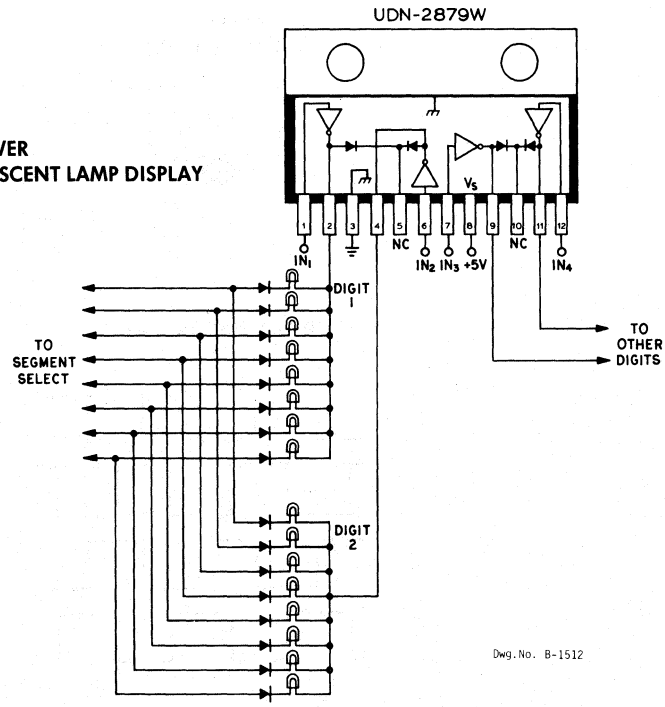
TYPICAL APPLICATIONS

PRINT-HAMMER DRIVER



DWG. NO. A-11,976

DIGIT DRIVER
FOR MULTIPLEXED INCANDESCENT LAMP DISPLAY

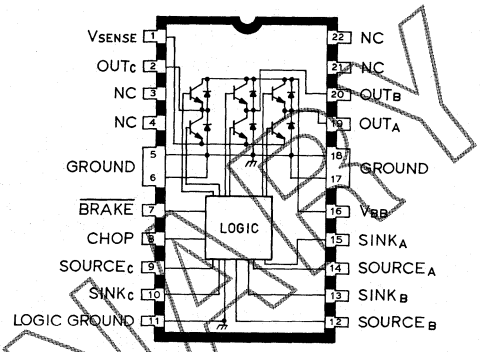


Dwg.No. B-1512

UDN-2931B AND UDN-2931W
3-PHASE BRUSHLESS DC MOTOR DRIVERS

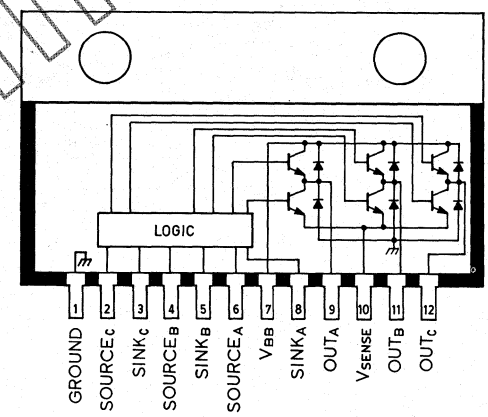
FEATURES

- Output Current of 2 A
- Internal Transient-Suppression Diodes
- Low-Saturation Output Drivers
- Anti-Crossover Protection
- Braking and Chopping Functions (UDN-2931B)
- Thermal Shutdown with Hysteresis
- External Current-Sense Capability
- Input Lockout Circuitry



Dwg. No. A-14,201

UDN-2931B



Dwg. No. A-14,202

UDN-2931W

The UDN-2931B/W 3-phase brushless dc motor driver is designed for low output saturation-voltage levels. These drivers maximize motor capacity limited by power supply constraints. The output driver features low output saturation source and sink drivers and integral output suppression diodes. The outputs are capable of maintaining an output OFF voltage of 15 V and an ON current of 2 A (3.5 A peak).

Crossover current protection has been incorporated to guard against common sink and source drivers being ON at the same time. Circuitry on the input structure has been added to lock-out the sink driver when both driver inputs have been activated at the same time.

The UDN-2931B has extended flexibility with CHOP and BRAKE functions. The CHOP function affects the source driver by switching it ON and OFF while the CHOP is being toggled. In utilizing the BRAKE function the source drivers are turned ON while the sink drivers are turned OFF. The BRAKING input is active low. Crossover-current protection is still in operation during BRAKING.

Both devices feature a common-emitter pin on the sink drivers. The emitter-current sense is useful in chopper-mode configurations. Thermal shutdown in these devices has been set to 165°C.

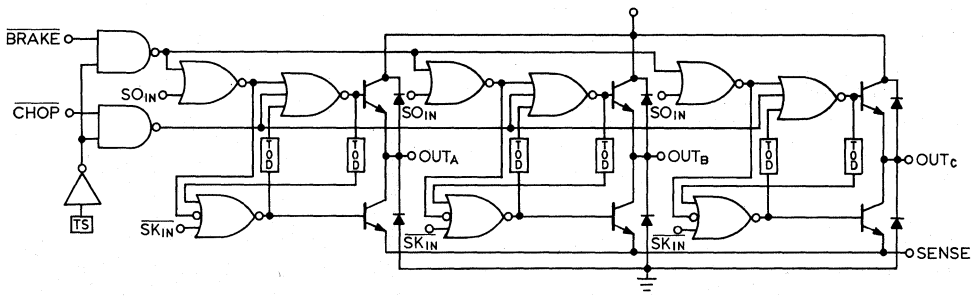
The UDN-2931B is supplied in a 16-pin dual in-line package with heat-sink contact tabs. This package allows for ease of circuit-board insertion. The UDN-2931W is supplied in a 12-pin single in-line power-tab package. These packages allow for easy attachment of an external heat-sink for extended power dissipation capabilities.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Motor Supply Voltage, V_{BB}	15 V
Output Current, I_{OUT} (Peak)	±3.5 A
(DC)	±2.0 A
Input Voltage, V_{IN}	7.0 V
Sense Voltage, V_{SENSE}	1.5 V
Package Power Dissipation, P_D	
(UDN-2931B)	2.77 W*
(UDN-2931W)	5.2 W**
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 22.22 mW/°C above $T_A = +25°C$.
**Derate at the rate of 41.16 mW/°C above $T_A = +25°C$.

FUNCTIONAL BLOCK DIAGRAM



TOD = TURN ON DELAY, TS = THERMAL SHUTDOWN

Dwg. No. A-14,203

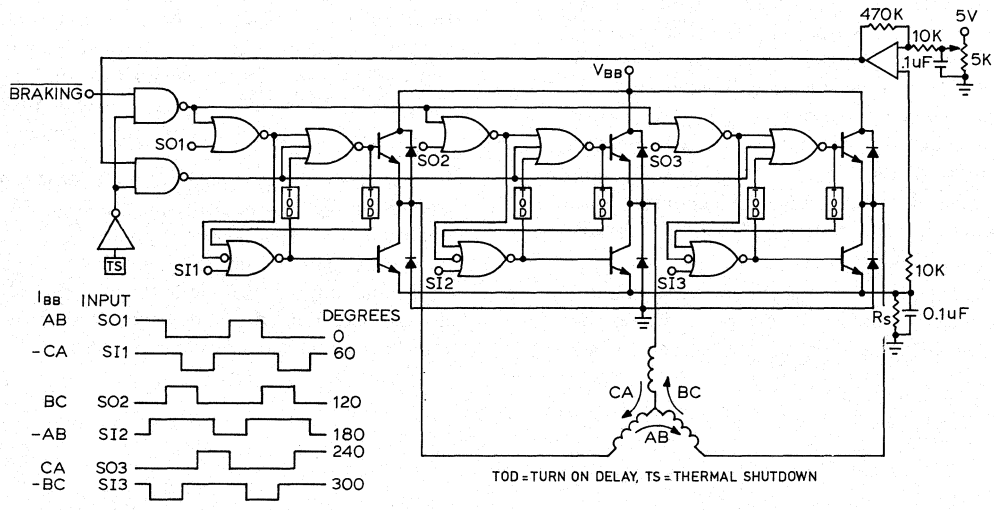
ELECTRICAL CHARACTERISTICS at T_{TAB} = +70°C. V_{BB} = 15 V

Characteristic	Symbol	Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All Drivers OFF, V_{OUT} = 0 V	—	<−1.0	−100	µA
		All Drivers OFF, V_{OUT} = 15 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = ±2 A, L = 2 mH	15	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 2 A	—	—	0.7	V
		I_{OUT} = −2 A	—	0.5	1.3	V
Motor Supply Voltage Range	V_{BB}		7.0	1.0	15	V
Motor Supply Current	$I_{BB(OFF)}$	All channels OFF	—	10	12	mA
	$I_{BB(ON)}$	One Source and Sink Driver ON, No Load	—	75	120	mA
Clamp Diode Forward Voltage	V_F	I_F = 2.0 A	—	1.7	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 15 V	—	<1.0	100	µA
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	—	<1.0	10	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−50	−200	µA
Logic Input Voltage	$V_{IN(1)}$	All inputs	2.0	—	—	V
	$V_{IN(0)}$	All inputs	—	—	0.8	V
Chopping Frequency	f_{CHOP}	I_{OUT} = 2 A, L = 2 mH, 90% Duty Cycle	—	—	400	KHz
Thermal Shutdown Temperature	T_{CR}	Note 1	—	165	—	°C

1. Thermal shutdown typically has a hysteresis of 15°C.

4

TYPICAL APPLICATION

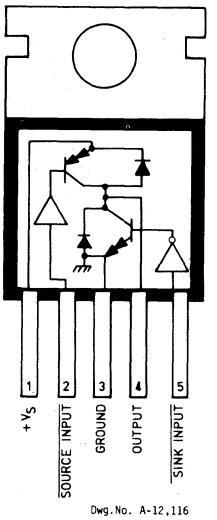


Dwg. No. A-14,204

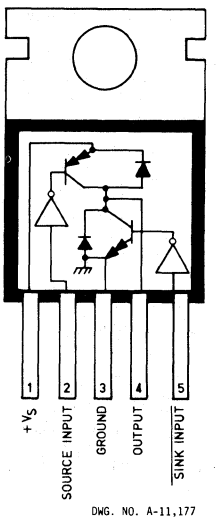
UDN-2935Z AND UDN-2950Z
BIPOLAR HALF-BRIDGE MOTOR DRIVERS

FEATURES

- 3.5 A Peak Output
- 37 V Min. Output Breakdown
- Output Transient Protection
- Tri-State Outputs
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Internal Thermal Shutdown
- High-Speed Chopper (to 100 kHz)
- UDN-2935Z Replaces SG3635P
- UDN-2950Z Replaces UDN-2949Z, SN75605
- TO-220 Style Packages



UDN-2935Z



UDN-2950Z

BOTH Type UDN-2935Z and UDN-2950Z integrated circuits are designed for servo-motor applications using pulse-width modulation. These two high-current, monolithic half-bridge motor drivers combine a sink-and-source driver with diode transient protection, input gain, level shifting, logic stages, and a voltage regulator for single-supply operation.

The UDN-2935Z output goes high with an active low input at pin 2; it is especially desirable in NMOS microprocessor applications. The UDN-2950Z output goes high with an active high input at pin 2; its inputs can be tied together for single-wire control. The input circuitry of both devices is compatible with TTL and low-voltage CMOS, PMOS, and NMOS logic. Both ICs have logic lockout (tri-state output) that prevents source and sink drivers from turning ON simultaneously.

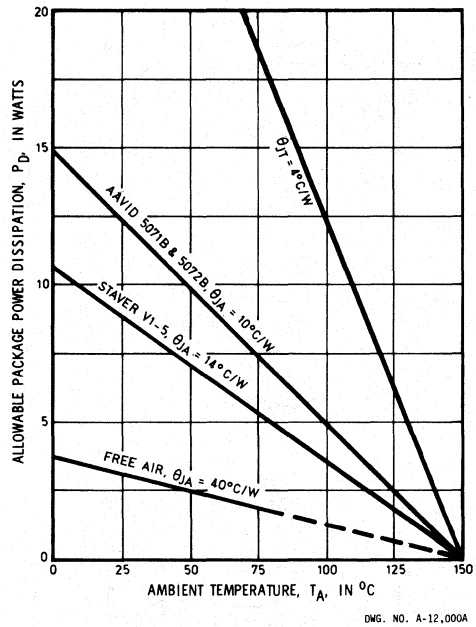
In typical applications, the chopper-drive mode is characterized by low power-dissipation levels, low saturation voltages, and short chopper-storage times for the sink drivers. The motor drivers can be used in pairs for full-bridge operation, or as triplets in three-phase brushless d-c motor-drive applications. They can also be teamed with the Sprague Electric UCN-4202A stepper motor translator/driver for bipolar d-c stepper motor control

The motor drivers' single-chip construction and power-tab TO-220 package enable cost-effective and reliable system designs supported by excellent power-dissipation ratings, minimum size, and ease of installation; because the package's heat tab is at ground potential, several devices can share a common heat sink without insulating hardware.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_S	8.0 V to 35 V
Output Voltage Range, V_{OUT}	−2.0 V to V_S + 2.0 V
Input Voltage Range, V_{IN}	−0.3 V to +7.0 V
Peak Output Current (100 ms, 10% d-c), I_{OP}	±3.5 A
Continuous Output Current, I_{OUT}	±2.0 A
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +85°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

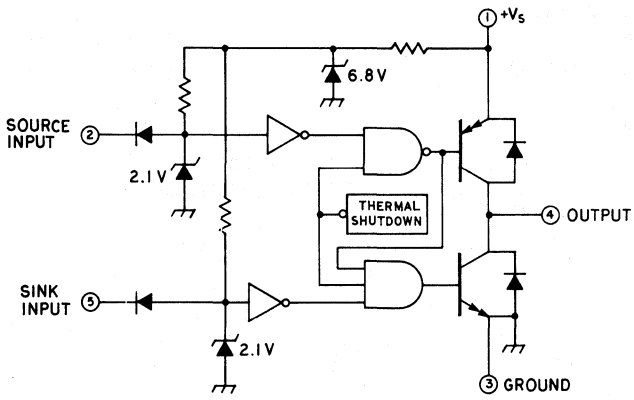


TRUTH TABLE

Source Driver, Pin 2	Sink Driver, Pin 5	Output, Pin 4	
		UDN-2935Z	UDN-2950Z
Low	Low	High	Low
Low	High	High	High Z
High	Low	Low	High
High	High	High Z	High

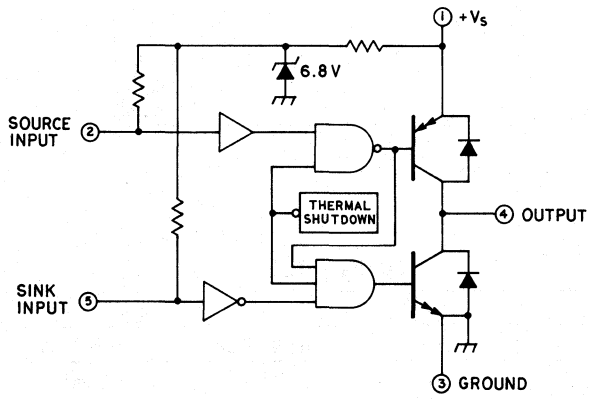
FUNCTIONAL BLOCK DIAGRAMS

UDN-2935Z



Dwg.No. A-12,113

UDN-2950Z



Dwg.No. A-12,112

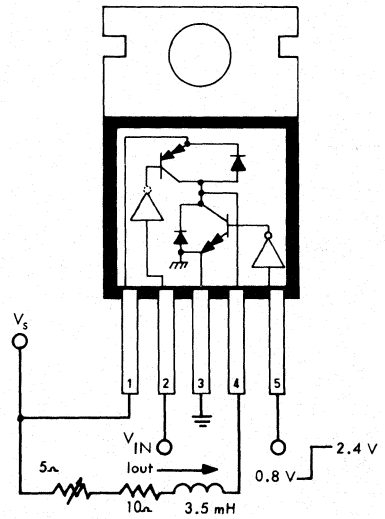
ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_{TAB} = +70°C, V_S = 35 V (unless otherwise noted)

Characteristic	Source Driver Input, Pin 2		Sink Driver Input, Pin 5	Output, Pin 4	Other	Limits		
	UDN-2935Z	UDN-2950Z				Min.	Max.	Units
Output Leakage Current	2.4 V	0.8 V	2.4 V	0 V	—	—	−500	µA
	2.4 V	0.8 V	2.4 V	35 V	—	—	500	µA
Output Sustaining Voltage	2.4 V	0.8 V	0.8 to 2.4 V	2.0 A	Fig. 1	35	—	V
Output Saturation Voltage	0.8 V	2.4 V	2.4 V	−2.0 A	—	33	—	V
	2.4 V	0.8 V	0.8 V	2.0 A	—	—	2.0	V
Output Source Current	0.8 V	2.4 V	2.4 V	—	—	−2.0	—	A
Output Sink Current	2.4 V	0.8 V	0.8 V	—	—	2.0	—	A
Input Open-Circuit Voltage	−250 µA	−250 µA	−250 µA	—	—	—	7.5	V
Input Current	—	2.4 V	2.4 V	NC	—	—	−700	µA
	2.4 V	—	2.4 V	NC	—	—	10	µA
	0.8 V	0.8 V	0.8 V	NC	—	—	−1.6	mA
Propagation Delay	2.4 V	0.8 V	0.8 to 2.4 V	2.0 A	—	—	750	ns
	0.8 to 2.4 V	2.4 to 0.8 V	2.4 V	2.0 A	—	—	2.0	µs
Clamp Diode Forward Voltage	NC	NC	NC	2.0 A	Fig. 2	—	2.2	V
Supply Current	0.8 V	2.4 V	NC	NC	—	—	35	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

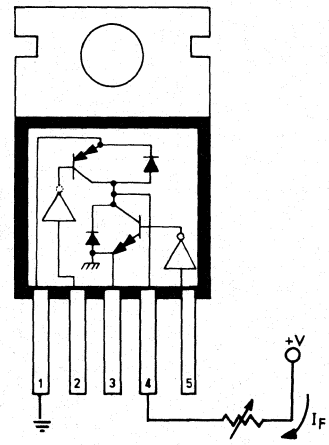
4

TEST FIGURE 1



Dwg.No. A-12,117

TEST FIGURE 2



Dwg.No. A-12,118

APPLICATION NOTES

It should be noted that an additional power dissipation component may arise from crossover currents flowing from supply to ground when current direction through the load is reversed. This is due to differences in the switching speeds between the source and sink drivers. Although the internal logic lockout protects these devices from catastrophic failure, the crossover power component can cause device operation at substantially higher junction temperatures.

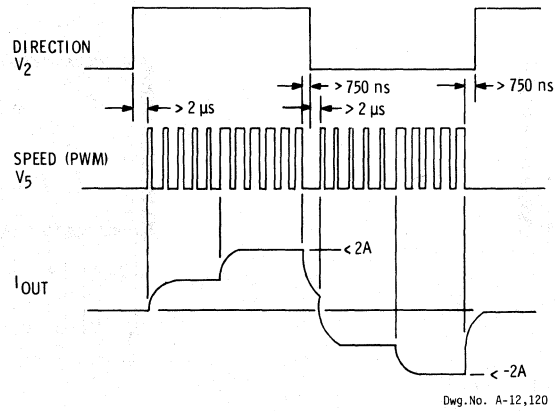
If timing conditions are ignored, the magnitude of this power can be approximated as:

$$P_D = V_S \times I_C \times t \times f$$

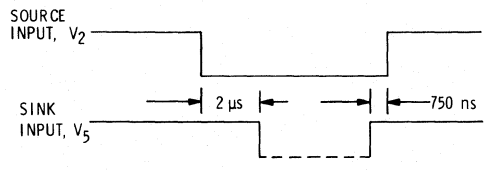
where V_S = *supply voltage*
I_C = *crossover current (≈ 3.5 A max.)*
t = *crossover current duration (≈ 1 μs)*
f = *frequency of direction change*

In some applications (high switching speeds or high package power dissipation), it is recommended that the inputs be driven separately, and that the sink driver not be turned ON for at least 2 μs (maximum source t_{PD}) after the source driver input is turned OFF. The sink driver should be turned OFF at least 750 ns (maximum sink t_{PD}) before the source driver is turned ON.

RECOMMENDED TIMING CONDITIONS
(UDN-2950Z shown)



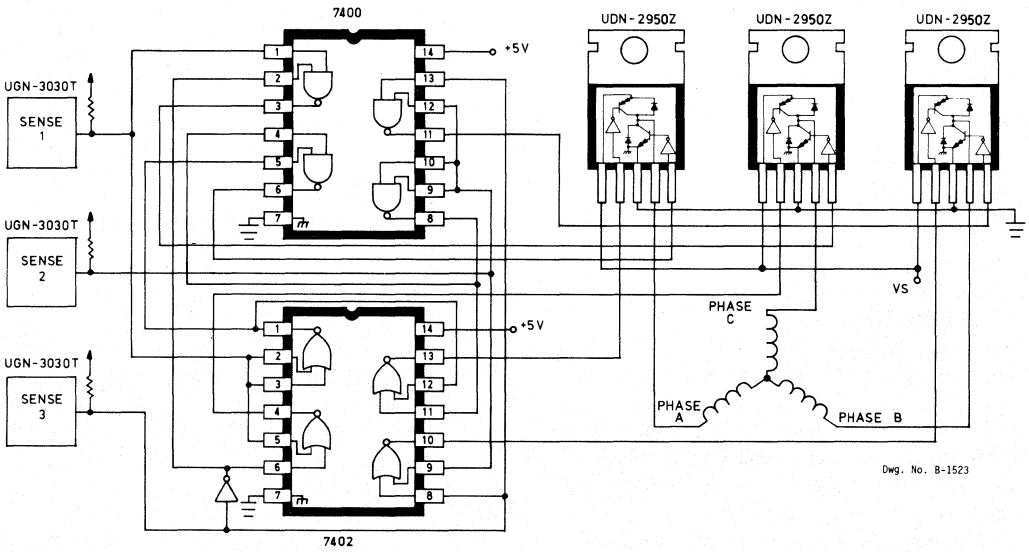
Dwg.No. A-12,120



Dwg.No. A-12,119

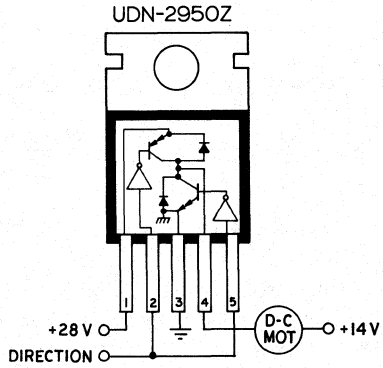
TYPICAL APPLICATIONS

3-PHASE BRUSHLESS DC MOTOR DRIVE

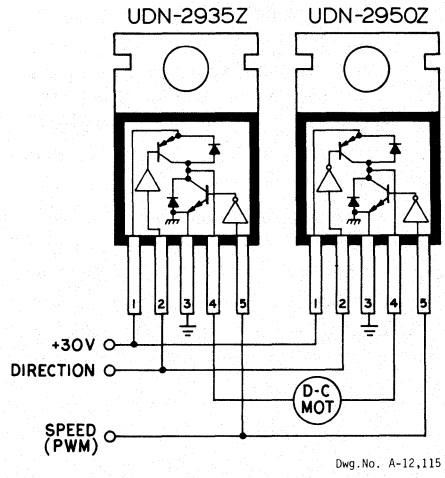


4

SINGLE-WINDING DC OR STEPPER MOTOR DRIVE



FULL-BRIDGE DC SERVO MOTOR DRIVE



UDN-2936W AND UDN-2937W
3-PHASE BRUSHLESS DC MOTOR CONTROLLERS

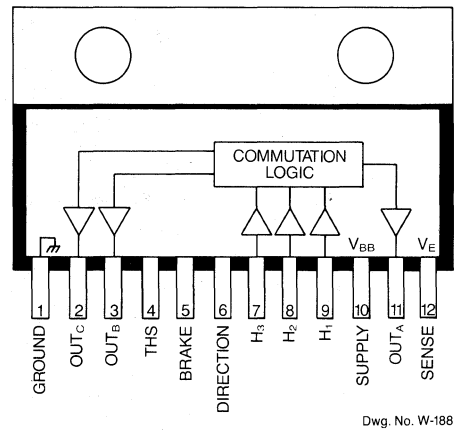
FEATURES

- 10 V to 45 V Operation
- ± 4 A Peak Output Current
- Internal Clamp Diodes
- Internal PWM Current Control
- 60° Commutation Decoding Logic
- Thermal Shutdown Protection
- Compatible with Single-Ended or Differential Hall Effect Sensors
- Braking and Direction Control (UDN-2936W Only)

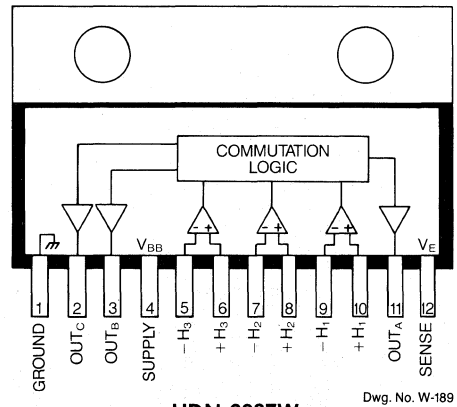
Combining logic and power, the UDN-2936W and the UDN-2937W provide commutation and drive for a three-phase brushless dc motor. Each of the three push-pull outputs are rated at 45 V and ± 3 A (± 4 A peak), and have internal ground clamp and flyback power diodes. These drivers also feature internal commutation logic, PWM current control, and thermal shutdown protection.

The UDN-2936W is compatible with single-ended digital or linear Hall effect sensors. The commutating logic is programmed for 60° electrical separation (other separation sequences, such as 120°, are available via mask programming at the factory). Current control is accomplished by sensing current through an external sense resistor and pulse-width modulating the source drivers. Voltage thresholds and hysteresis can be externally set by the user. If desired, internal threshold and hysteresis defaults (300 mV, 7.5 percent) can be used. The UDN-2936W also features braking and direction control. Internal protection circuitry prevents crossover current when braking or changing direction.

The UDN-2937W is compatible with linear differential buffered and unbuffered Hall effect sensors. By changing sensor output polarities, various commutation sequences, such as 60°, 120°, or 240°, can be set. The PWM current control threshold and hysteresis is set at 300 mV and 7.5 percent. The peak output current is determined by a user-selected external sense resistor.



UDN-2936W



UDN-2937W

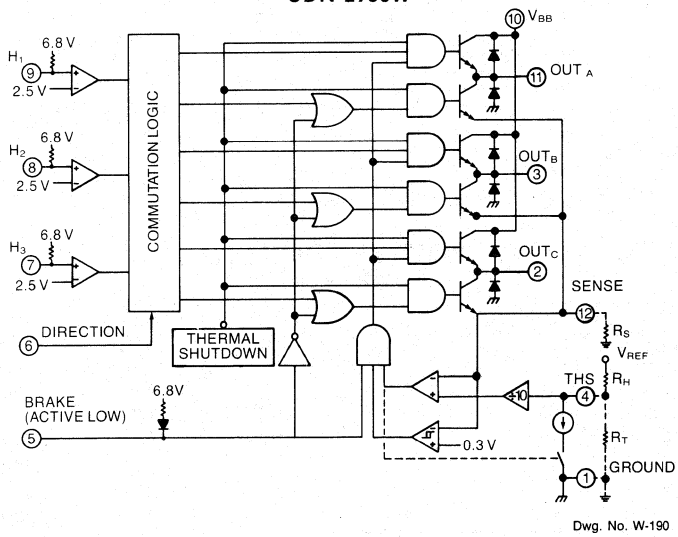
For maximum power-handling capability, the UDN-2936W and UDN-2937W are supplied in 12-pin single in-line power tab packages. An external heat sink may be required for high-current applications. The tab is at ground potential and needs no insulation.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

Supply Voltage, V_{BB} 45V
Output Current, I_{OUT} (continuous) ..... ±3A
(peak) ..... ±4A
Input Voltage Range, V_{IN} ..... −0.3V to 15V
Threshold Voltage, V_{THS} 15V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

NOTE: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
UDN-2936W



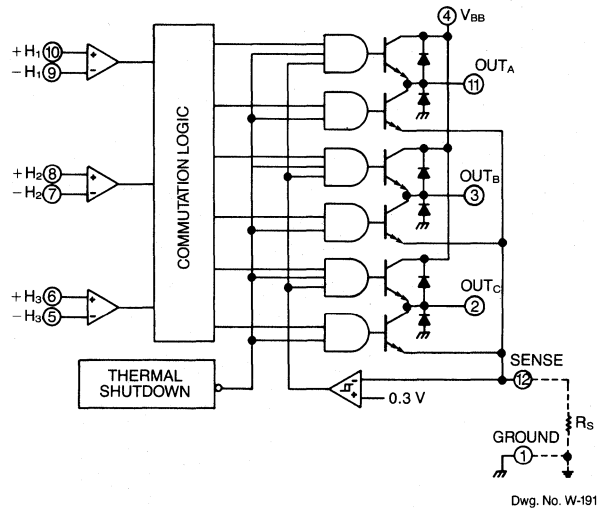
Dwg. No. W-190

COMMUTATION TRUTH TABLE
UDN-2936W

Hall Sensor Inputs					Outputs		
H_1	H_2	H_3	Direction	Brake	OUT_A	OUT_B	OUT_C
High	High	High	Low	High	Z	Low	High
High	High	Low	Low	High	High	Low	Z
High	Low	Low	Low	High	High	Z	Low
Low	Low	Low	Low	High	Z	High	Low
Low	Low	High	Low	High	Low	High	Z
Low	High	High	Low	High	Low	Z	High
High	High	High	High	High	Z	High	Low
High	High	Low	High	High	Low	High	Z
High	Low	Low	High	High	Low	Z	High
Low	Low	Low	High	High	Z	Low	High
Low	Low	High	High	High	High	Low	Z
Low	High	High	High	High	High	Z	Low
X	X	X	X	Low	Low	Low	Low

X = Irrelevant
Z = High Impedance

FUNCTIONAL BLOCK DIAGRAM
UDN-2937W



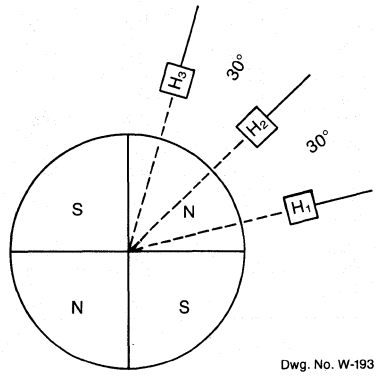
Dwg. No. W-191

COMMUTATION TRUTH TABLE
UDN-2937W

Hall Sensor Inputs*			Outputs		
$+H_1$	$+H_2$	$+H_3$	OUT_A	OUT_B	OUT_C
High	High	High	Z	Low	High
High	High	Low	High	Low	Z
High	Low	Low	High	Z	Low
Low	Low	Low	Z	High	Low
Low	Low	High	Low	High	Z
Low	High	High	Low	Z	High

* Inputs are with respect to $-H_N$ inputs.
Z = High Impedance

TYPICAL HALL EFFECT SENSOR LOCATIONS



Dwg. No. W-193

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq 70°C$, $V_{BB} = 45V$

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{BB}	Operating	10	—	45	V
Supply Current	I_{BB}	Outputs Open	—	52	60	mA
		$V_{BRAKE} = 0.8V$, UDN-2936W Only	—	54	60	mA
Thermal Shutdown Temperature	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	25	—	°C
Output Drivers						
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	—	50	µA
		$V_{OUT} = 0V$	—	—	−50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = -1A$	—	1.7	1.9	V
		$I_{OUT} = +1A$	—	1.1	1.3	V
		$I_{OUT} = -2A$	—	1.9	2.1	V
		$I_{OUT} = +2A$	—	1.4	1.6	V
		$I_{OUT} = -3A$	—	2.35	2.50	V
		$I_{OUT} = +3A$	—	1.85	2.00	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = \pm 3A$, L = 2mH	45	—	—	V
Clamp Diode Forward Voltage	V_F	$I_F = 2A$	—	1.8	2.0	V
Clamp Diode Leakage Current	I_R	$V_R = 45V$	—	—	50	µA
Output Switching Time	t_r	$I_{OUT} = \pm 2A$, Resistive Load	—	2.0	—	µs
	t_f	$I_{OUT} = \pm 2A$, Resistive Load	—	2.0	—	µs
Turn-ON Delay (Resistive Load)	t_{on}	Source Drivers, 0 to −2A	—	1.25	—	µs
		Sink Drivers, 0 to +2A	—	1.9	—	µs
Turn-OFF Delay (Resistive Load)	t_{off}	Source Drivers, −2A to 0	—	1.7	—	µs
		Sink Drivers, +2A to 0	—	0.9	—	µs
UDN-2936W Control Logic						
Logic Input Voltage	$V_{IN(1)}$	V_{DIR} or V_{BRAKE}	2.0	—	—	V
	$V_{IN(0)}$	V_{DIR} or V_{BRAKE}	—	—	0.8	V
Sensor Input Voltage Threshold	V_{IN}	H_1, H_2, or H_3	—	2.5	—	V
Input Current	$I_{IN(1)}$	$V_{DIR} = 2V$	—	150	200	µA
		$V_{BRAKE} = 2V$	—	<1.0	5.0	µA
		$V_H = 5V$	—	−190	−220	µA
	$I_{IN(0)}$	$V_{DIR} = 0.8V$	—	35	50	µA
		$V_{BRAKE} = 0.8V$	—	−5.0	−20	µA
		$V_H = 0.8V$	—	−0.64	−1.0	mA
	I_{THS}	$V_{THS} \geq 3.0V$	—	−8.0	−15	µA
		$V_{THS} < 3.0V$, $V_{SENSE} < V_{THS}/10.5$	—	−15	−30	µA
		$V_{THS} < 3.0V$, $V_{SENSE} > V_{THS}/9.5$	140	200	260	µA
Current Limit Threshold		V_{THS} / V_{SENSE} at trip point, $V_{THS} < 3.0V$	9.5	10	10.5	
Default Sense Trip Voltage	V_{SENSE}	$V_{THS} \geq 3.0V$	270	300	330	mV
Default Hysteresis		$V_{THS} \geq 3.0V$	—	7.5	—	%
Deadtime	t_d	BRAKE or DIRECTION	—	2.0	—	µs
UDN-2937W Control Logic						
Input Common-Mode Voltage Range	V_{CM}		1.5	2.0	4.0	V
Input Voltage Hysteresis	$V_{IN(HYS)}$		—	10	—	mV
Input Current	I_{IN}	$V_{IN} = 5V$	—	12	20	µA
Sense Trip Voltage	V_{SENSE}		270	300	330	mV
Hysteresis			—	7.5	—	%

4

APPLICATIONS INFORMATION

The UDN-2936 and UDN-2937W power drivers provide commutation logic and power outputs to drive a three-phase brushless DC motor.

UDN-2936W

The UDN-2936W is designed to interface with single-ended linear or digital Hall effect devices (HEDs). Internal pull-up resistors on the UDN-2936W inputs allow for direct use with open-collector digital HEDs. The H_N inputs have 2.5 V thresholds.

The commutation logic provides decoding for HEDs with 60° electrical separation (other separations available via mask programming). At any one step in the sequencing, one half-bridge driver is sourcing, one driver is sinking, and one driver is in a high-impedance state (see truth table). Changing the logic level of the DIRECTION pin inverts the output states, thus reversing the direction of the motor. A logic low on the BRAKE pin turns ON all three sink drivers and turns OFF all source drivers, dynamically braking the motor. An internally-generated dead time (t_d) of about 2 µs prevents potentially destructive crossover currents that can occur when changing direction or braking. In some high supply voltage applications, it may be necessary to brake the motor before changing direction.

Motor current is internally controlled by pulse-width modulating the source drivers with a preset hysteresis format. Load current through an external sense resistor (R_S) is constantly monitored. When the current reaches the set trip point (determined by an external reference voltage or internal default), the source driver is disabled. Current recirculates through the ground clamp diode, motor winding, and sink driver. An internal constant-current sink reduces the trip point (hysteresis). When the decaying current reaches this lower threshold, the source driver is enabled again and the cycle repeats.

Thresholds and hysteresis can be set with external resistors or internal defaults can be used. With $V_{THS} >$ 3.0 V, the trip point is internally set at 300 mV with 7.5 percent hysteresis. Load current is then determined by the equation:

$$I_{MAX} = 0.3/R_S$$

With $V_{THS} < 3.0$ V, the threshold, hysteresis percentage, and peak current are set with external reisistors according to the equations:

Threshold Voltage (V_{THS}) = $V_{REF} \cdot R_T / (R_H + R_T)$

Hysteresis Percentage = $R_H/50\,V_{REF}$

Load Trip Current (I_{MAX}) = $V_{THS}/(10\,R_S)$

Percentage hysteresis is a fixed value independent of load current. The chopping frequency is a function of circuit parameters including load inductance, load resistance, supply voltage, hysteresis, and switching speed of the drivers.

UDN-2937W

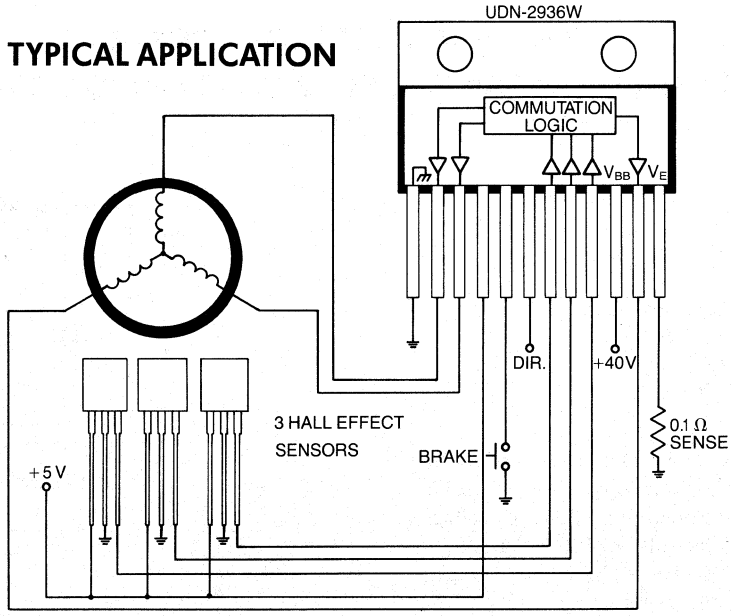
The inputs of the UDN-2937W are designed to interface directly with the outputs of differential buffered or unbuffered HEDs. Various commutation sequences (60°, 120°, 240°) can be set by using appropriate HED output polarities shown in the truth table.

The UDN-2937W load current control circuitry works the same as in the UDN-2936W except that only the internal threshold and hysteresis settings can be used. With the threshold of 300 mV and hysteresis of 7.5 percent, load current is determined by:

$$I_{MAX} = 0.3/R_S$$

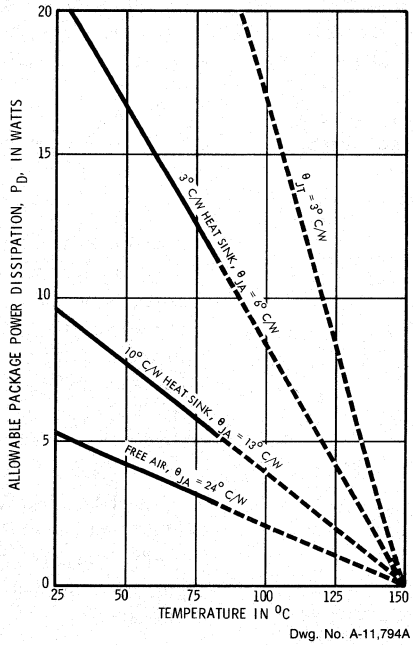
Both the UDN-2936W and UDN-2937W outputs are rated for normal operating currents of up to 3 A and start-up currents to 4 A. Internal power ground clamp and flyback diodes protect the outputs from the voltage transients that occur when switching inductive loads. Both devices also feature thermal protection circuitry. If the junction temperature reaches 165°C, the thermal shutdown circuitry turns OFF all output drivers. The outputs are re-enabled when the junction cools down to approximately 140°C.

TYPICAL APPLICATION



Dwg. No. W-192

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,794A

UDN-2938W AND UDN-2939B
3-PHASE UNIPOLAR BRUSHLESS DC MOTOR DRIVERS

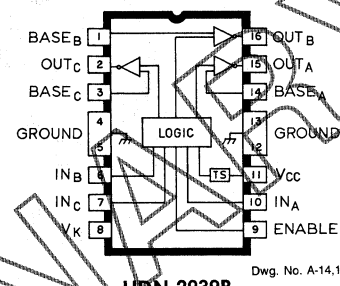
FEATURES

- Output Voltage of 30 V
- Output Current of 4 A
- Integral Transient-Suppression Diodes
- External Output Driver Capacitor Pins
- Thermal Shutdown Circuitry
- TTL, DTL, CMOS Compatible Inputs

The UDN-2938W and UDN-2939B are three-phase unipolar brushless dc motor drivers capable of handling 4 A drive currents, an output OFF voltage of 50 V, and a sustaining voltage of 30 V. The output drive structure of these devices have been designed for low saturation voltages (less than 1.0 V at 1 A). UDN-2938W and UDN-2939B are functionally identical except that the UDN-2939B has ENABLE input for extended control flexibility. The bases of the output drivers have been brought out to external pins so that capacitors may be connected in order to stimulate an ac drive and to avoid EMI and RFI problems.

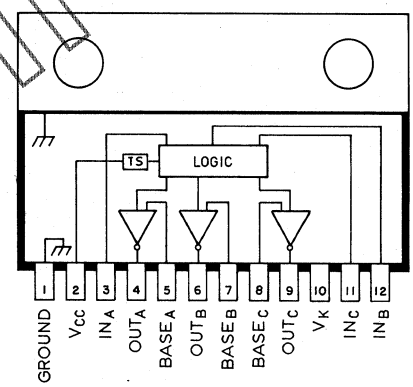
Output transient-suppression diodes have been incorporated for use with inductive loads. Inputs are active high and float low. These inputs are TTL, DTL, and 5 V-12 V CMOS compatible. The ENABLE function (UDN-2939B) is active high and, when pulled low, will turn OFF all output drivers. These devices have thermal shutdown circuitry with hysterisis to guard against overheating. This thermal shutdown circuitry is designed to operate at a temperature of 165°C. A logic supply current regulator has been introduced into these devices to maintain a relatively constant output base drive over the logic supply (V_{CC}) operating range.

The UDN-2938W is packaged in a single in-line 12-pin power-tab SIP package with lead centers at 0.100 inches. The UDN-2939B is packaged in a 16-pin dual in-line batwing package with heat-sink contact tabs.



Dwg. No. A-14,196

UDN-2939B

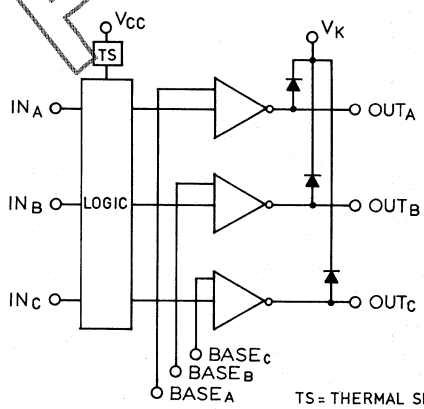


TS = THERMAL SHUTDOWN

Dwg. No. A-14,194

UDN-2938W

FUNCTIONAL BLOCK DIAGRAM



TS = THERMAL SHUTDOWN

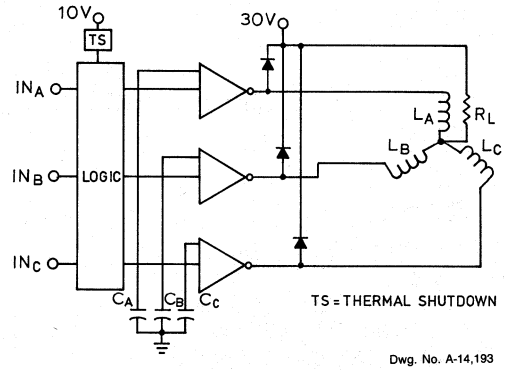
Dwg. No. A-14,195

ABSOLUTE MAXIMUM RATINGS at +25°C

Output Voltage, V_{CE} ..... 50 V
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... 30 V
Output Current, I_{OUT} ..... 5 A
Logic Supply, V_{CC} ..... 15 V
Input Voltage, V_{IN} ..... 15 V
Package Power Dissipation, P_D
(W Package) ..... 5.2 W*
(B Package) ..... 2.77 W**
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 41.16 mW/°C above T_A = +25°C.
**Derate at the rate of 22.22 mW/°C above T_A = +25°C.

TYPICAL APPLICATION



Dwg. No. A-14,193

4

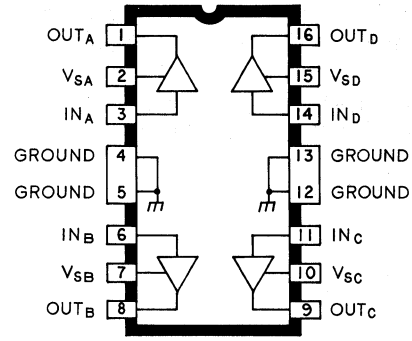
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V (Unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Logic Supply Voltage Range	V_{CC}		4.5	—	15	V
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	<1.0	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 4.0 A	30	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 1.0 A	—	0.9	1.1	V
		I_{OUT} = 4.0 A	—	1.9	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	<1.0	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.3	1.5	V
Input Voltage	$V_{IN(1)}$		—	—	2.0	V
	$V_{IN(0)}$		0.8	—	—	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	30	50	µA
	$V_{IN(0)}$	V_{IN} = 0.8 V	—	—	1.0	µA
Supply Current	$I_{CC(ON)}$	One Driver ON, No Load	—	12	15	mA
	$I_{CC(OFF)}$	All Drivers OFF	—	5.0	8.0	mA
Thermal Shutdown Temperature	T_J		—	165	—	°C

UDN-2941B
QUAD HIGH-CURRENT SOURCE DRIVER

FEATURES

- 1.5 A Output Source Current
- Minimized Saturation Voltage
- 30 V Output Sustaining Voltage
- Transient-Protected Outputs
- TTL or CMOS Compatible Inputs
- Plastic Dual In-Line Package With Heat-Sink Contact Tabs



Dwg. No. A-12,514

HIGH-CURRENT SOURCE DRIVERS are designed to serve as interface between low-level logic and a variety of peripheral power loads, including solenoids, d-c or stepper motors using pulse-width modulation, and multiplexed LED or incandescent displays.

The UDN-2941B high-current source driver has four independent emitter-follower drivers. Special circuit design techniques, resulting in reduced output-saturation voltages, allow any one driver to source up to −1.5 A continuously with minimal voltage drops and package power dissipation.

The device's high switching speed prevents "ghosting" effects when it is used to drive multiplexed displays. All outputs are rated for operation to 35 V (30 V sustaining). The low-level inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The UDN-2941B integrated circuit is supplied in a 16-pin plastic dual in-line package with copper heat-sink contact tabs. The lead configuration facilitates attachment of an inexpensive external heat sink for maximum power dissipation with standard cooling methods. It fits a standard IC socket or printed wiring board layout. The heat sink is at ground potential and needs no insulation.

Similar devices, for operation with load currents of up to −500 mA, are the 8-channel source drivers of Series UDN-2980A.

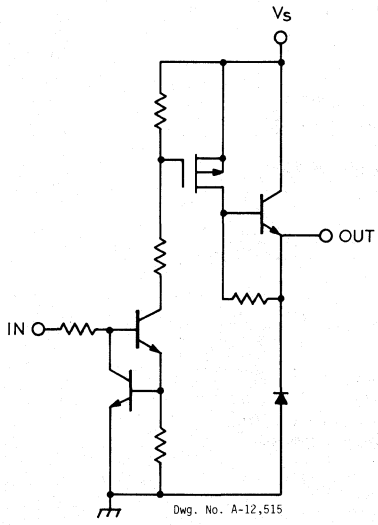
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_S . . . . . 12 V to 35 V
Peak Output Current, I_{OUT} . . . . . −2.0 A
Input Voltage, V_{IN} . . . . . 15 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature, T_S . . . . . −55°C to +150°C

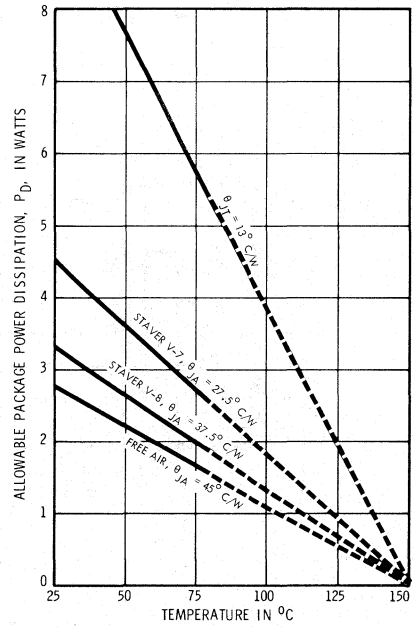
Output current rating will be limited by ambient temperature, duty cycle, heat sinking, air flow, and number of outputs conducting. Under any set of conditions, do not exceed the −2.0 A peak current and a junction temperature of +150°C.

PARTIAL SCHEMATIC

One of 4 Drivers



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,793A

4

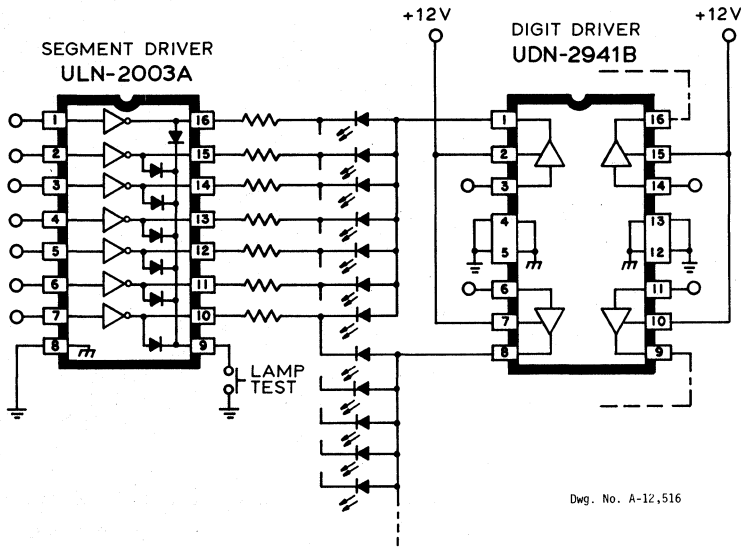
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 35$ V, $T_{TAB} \leq +70°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{IN} = 0.4$ V, $V_{OUT} = 0$ V, $T_A = +25°C$	—	< -10	-100	µA
		$V_{IN} = 0.4$ V, $V_{OUT} = 0$ V, $T_A = +70°C$	—	< -10	-500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	30	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 2.4$ V, $I_{OUT} = -1.0$ A	—	1.3	1.5	V
		$V_{IN} = 2.4$ V, $I_{OUT} = -1.5$ A	—	1.6	1.8	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 2.4$ V	—	175	500	µA
	$I_{IN(OFF)}$	$V_{IN} = 0.4$ V	—	—	-10	µA
Output Source Current	I_{OUT}	$V_{IN} = 2.4$ V	-1.5	—	—	A
Total Supply Current	I_S	$V_{IN} = 2.4$ V (Note 3), Outputs Open	—	11	15	mA
Clamp Diode Leakage Current	I_R	$V_R = 35$ V	—	<10	100	µA
Clamp Diode Forward Current	V_F	$I_F = 1.5$ A	—	1.4	2.0	V
Turn-On Delay	t_{PLH}	0.5 V_{in} to 0.5 V_{out}, Resistive Load	—	0.25	2.5	µs
Turn-Off Delay	t_{PHL}	0.5 V_{in} to 0.5 V_{out}, Resistive Load	—	0.5	5.0	µs

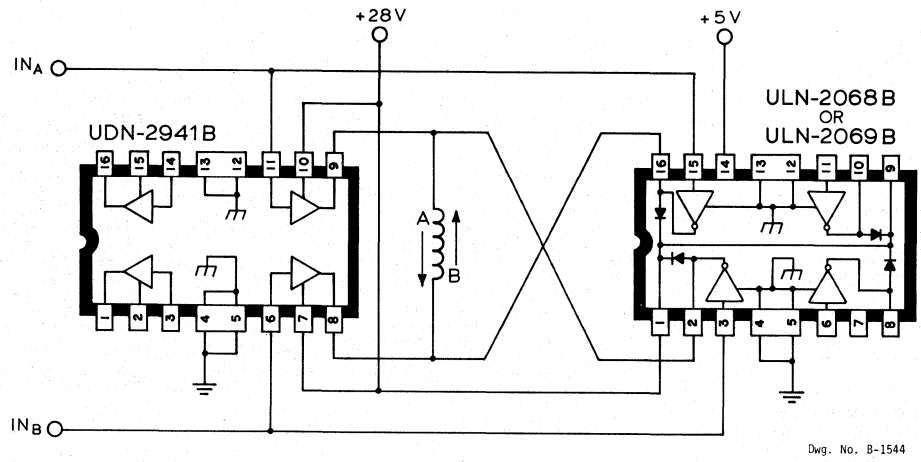
NOTES: 1. Each driver tested separately.
2. Negative current is defined as coming out of (sourcing) the specified device pin.
3. All inputs simultaneously.

TYPICAL APPLICATIONS

MULTIPLEXED COMMON-ANODE LED DISPLAY DRIVER



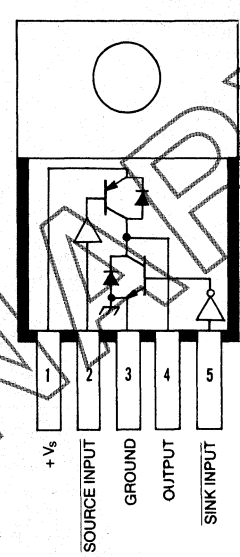
FULL-BRIDGE MOTOR DRIVER
(One of 2 Windings)



UDN-2943Z
HIGH-CURRENT BIPOLAR HALF-BRIDGE MOTOR DRIVER

FEATURES

- ±1 A Output Current
- 8.5 V to 24 V Operating Range
- Withstand 45 V Supply Transients
- Crossover-Current Protected
- Logic-Compatible Inputs
- Saturated Output Drivers
- Output Transient Protection
- Tri-State Output
- Internal Thermal Shutdown
- Internal Over-Voltage Protection
- Internal Short-Circuit Protection
- High-Speed Chopper (to 50 kHz)
- TO-220 Style Package



Dwg. No. A-14,135

DESIGNED for use as a general-purpose motor driver, the UDN-2943Z half-bridge driver combines high-current sink and source drivers with logic stages, level shifting, diode transient protection, and a voltage regulator for single-supply operation. Capable of operating in extremely harsh environments, this device can withstand high ambient temperatures, output overloads, and repeated power supply transient voltages without damage. The driver can be used in pairs for full-bridge operation, or as triplets in three-phase brushless dc motor-driver applications.

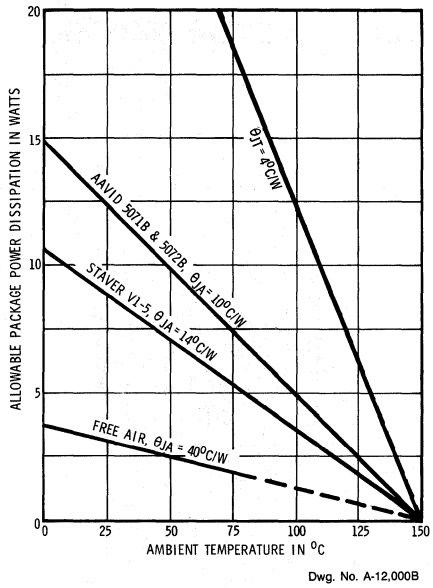
The input circuitry is compatible with TTL, low-voltage CMOS, and NMOS logic. Logic lockout prevents both source and sink drivers from turning ON simultaneously. Each driver is turned ON by an active-low input, making the UDN-2943Z especially desirable in many microprocessor applications. An accidental input open circuit will turn OFF the corresponding output. The device also provides an internally-generated dead-time to prevent crossover currents during output switching. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Saturated output drivers provide for low saturation voltage at the maximum rated current. Internal short-circuit protection, activated at load currents above 1 A, protects the source driver from accidental short-circuits between the output and ground.

The UDN-2943Z driver is rated for continuous operation with inductive loads at supply voltages of up to 24 V. With the application of increased supply voltages (to 45 V maximum), a high-voltage protective circuit becomes operative, shutting OFF both output drivers. The internal thermal shutdown is triggered by a nominal junction temperature of 160°C.

Single-chip construction and a modified 5-lead JEDEC power-tab Style TO-220 plastic package provide cost-effective and reliable systems designs. It also features excellent power dissipation ratings, minimum size, and ease of installation. The heat-sink tab is at ground potential and does not require insulation.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-12,000B

ABSOLUTE MAXIMUM RATINGS

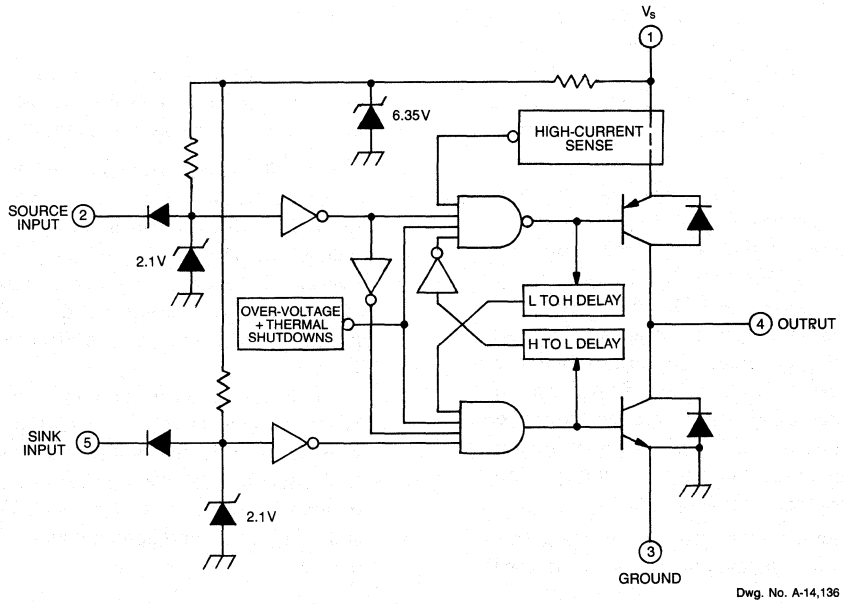
Supply Voltage Range, V_S . . . . . 8.5 V to 45 V*
Output Voltage, $V_{CE(sus)}$ . . . . . 24 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to +18 V
Continuous Output Current, I_{OUT} . . . . . ±1.0 A
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Internal high-voltage shutdown above 26 V.

LOGIC TRUTH TABLE

Source Driver, Pin 2	Sink Driver, Pin 5	Output, Pin 4
Low	Low	High
Low	High	High
High	Low	Low
High	High	High Z

FUNCTIONAL BLOCK DIAGRAM

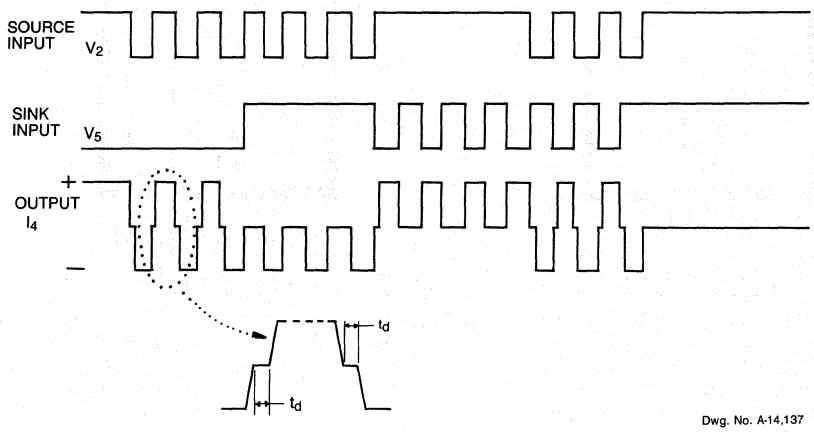


Dwg. No. A-14,136

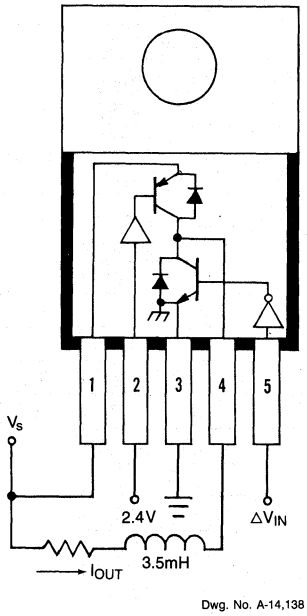
ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_{TAB} = 70°C, V_S = 24 V (unless otherwise noted)

Characteristic	Symbol	Source Driver Input, Pin 2	Sink Driver Input, Pin 5	Output, Pin 4	Other	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	2.4 V	2.4	0 V	—	—	−10	−100	µA
		2.4 V	2.4 V	45 V	—	—	10	100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	2.4 V	0.8 to 2.4 V	1.0 A	Fig. 1A	24	—	—	V
		0.8 to 2.4 V	2.4 V	−1.0 A	Fig. 1B	24	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	0.8 V	2.4 V	−1.0 A	—	—	1.2	1.8	V
		2.4 V	0.8 V	1.0 A	—	—	0.6	1.0	V
Short-Circuit Source Current	I_{SC}	0.8 V	2.4 V	0 V	—	1.1	—	1.8	A
Logic Input Voltage	$V_{IN(1)}$	—	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	—	—	—	—	—	0.8	V
Input Current	$I_{IN(1)}$	2.4 V	2.4 V	NC	—	—	10	100	µA
	$I_{IN(0)}$	0.8 V	0.8 V	NC	—	—	−50	−150	µA
Clamp Diode Forward Voltage	V_F	NC	NC	1.0 A	Fig. 2	—	1.5	2.0	V
Logic Supply Current	I_S	2.4 V	2.4 V	NC	—	—	15	20	mA
		2.4 V	0.8 V	NC	—	—	55	70	mA
		0.8 V	2.4 V	NC	—	—	25	35	mA
Thermal Shutdown Temperature	T_J	—	—	—	—	—	160	—	°C
Over-Voltage Shutdown	V_S	—	—	—	—	26	—	—	V
Propagation Delay	t_{PD}	2.4 V	2.4 to 0.8 V	1.0 A	Fig. 3	—	0.6	1.0	µs
		0.8 to 2.4 V	2.4 V	−1.0 A	Fig. 4	—	1.0	2.5	µs
		2.4 V	0.8 to 2.4 V	1.0 A	Fig. 3	—	1.1	2.5	µs
		2.4 to 0.8 V	2.4 V	−1.0 A	Fig. 4	—	0.6	1.0	µs
Dead Time	t_d	—	—	—	—	—	2.0	—	µs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

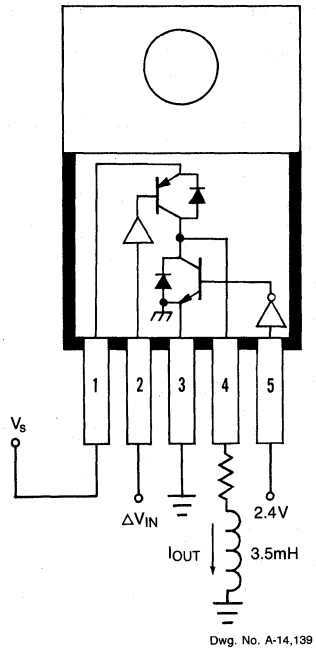


Dwg. No. A-14,137



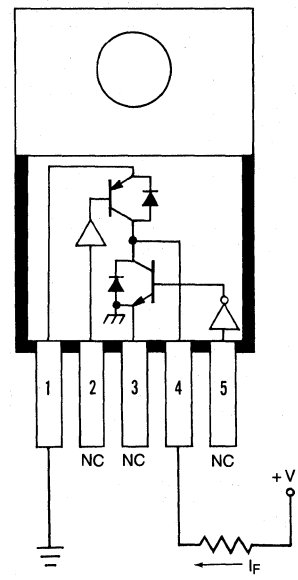
Dwg. No. A-14,138

FIGURE 1A



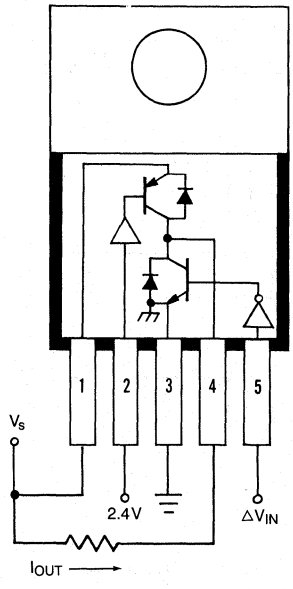
Dwg. No. A-14,139

FIGURE 1B



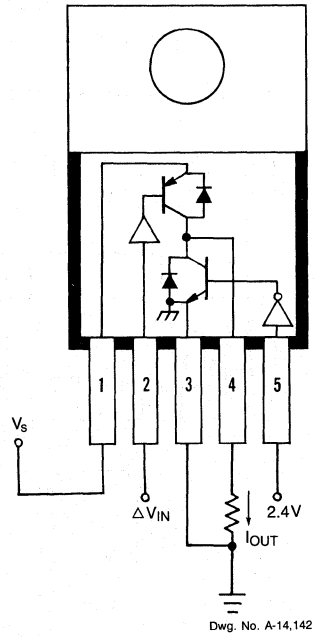
Dwg. No. A-14,140

FIGURE 2



Dwg. No. A-14,141

FIGURE 3



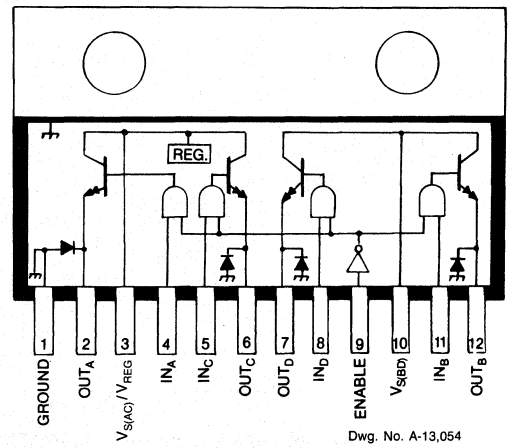
Dwg. No. A-14,142

FIGURE 4

UDN-2944W
QUAD HIGH-CURRENT, HIGH-VOLTAGE SOURCE DRIVER

FEATURES

- Output Current to 4A
- Output Voltage to 60V
- Loads to 960W
- Integral Output Suppression Diodes
- TTL and CMOS Compatible Inputs
- Plastic Single In-Line Package
- Heat-Sink Tab



Dwg. No. A-13,054

Capable of driving loads to 4A at supply voltages to 60V (inductive loads to 35V), the UDN-2944W is a quad high-current, high-voltage source driver. Each of the four power drivers can provide space- and cost-saving interface between low-level signal-processing circuits and high-power loads in harsh environments.

Individual supply lines have been provided for each pair of drivers so that different supplies can be used to drive multiple loads. The controlling inputs are TTL or CMOS compatible. The outputs include transient-suppression diodes for inductive loads.

This quad Darlington array is designed to serve as an interface between low-level circuitry and peripheral-power loads such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 240W per channel. The UDN-2944W is an ideal complement to the UDN-2878W quad 4A sink driver.

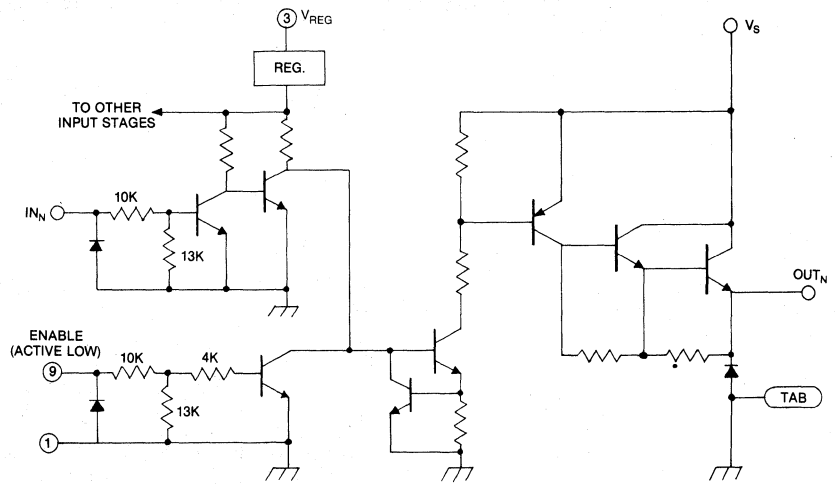
For maximum power-handling capability, the UDN-2944W driver is supplied in a 12-pin single in-line, power-tab package that allows efficient attachment of an external heat sink for maximum allowable package power dissipation. An external heat sink is usually required for proper operation of this device. The tab is at ground potential and needs no insulation.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Supply Voltage Range V_s . . . . . 10 V to 60 V
Output Current, I_{OUT} (DC) . . . . . −4 A
(Peak) . . . . . −5 A
Input Voltage, V_{IN} . . . . . 15 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

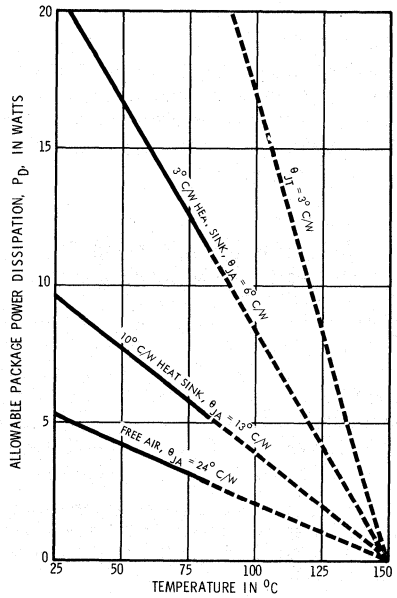
Output current rating will be limited by ambient temperature, duty cycle, heat sinking, air flow, and number of outputs conducting. Under any set of conditions, do not exceed the −5.0 A peak current and ajunction temperature of +150°C.

PARTIAL SCHEMATIC



Dwg. No. A-13,058

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,794A

NOTE: Pin 3 must be connected to V_S for operation of input logic gates.

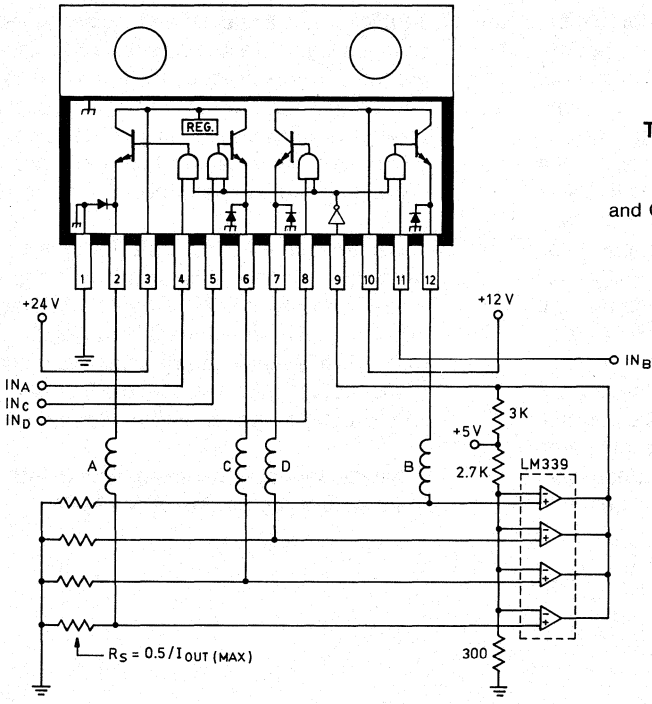
TRUTH TABLE

Input	Enable	Output
L	L	L
H	L	H
L	H	L
H	H	L

ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_{TAB} ≤70°C, V_S = 60V, V_{ENABLE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Voltage Range	V_S		10	60	V
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, V_{ENABLE} = 2.4V	—	50	μA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = −4A, L = 3 mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = −1A, V_{IN} = 2.4V	—	1.8	V
		I_{OUT} = −4A, V_{IN} = 2.4V	—	2.5	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.4V	—	220	μA
		$V_{IN(1)}$ or $V_{ENABLE\ (1)}$ = 12V	—	1.5	mA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.8V	—	50	μA
Total Supply Current	I_S	All drivers ON, All outputs open	—	25	mA
Clamp Diode Leakage Current	I_R	V_R = 60V	—	50	μA
Clamp Diode Forward Voltage	V_F	I_F = 4A	—	2.2	V
Turn-On Delay	t_{ON}	0.5 E_{in} to 0.5 E_{out}, R_L = 15Ω	—	2.0	μs
Turn-Off Delay	t_{OFF}	0.5 E_{in} to 0.5 E_{out}, R_L = 15Ω	—	10	μs

NOTE: Negative current is defined as coming out of (sourcing) the device being tested.



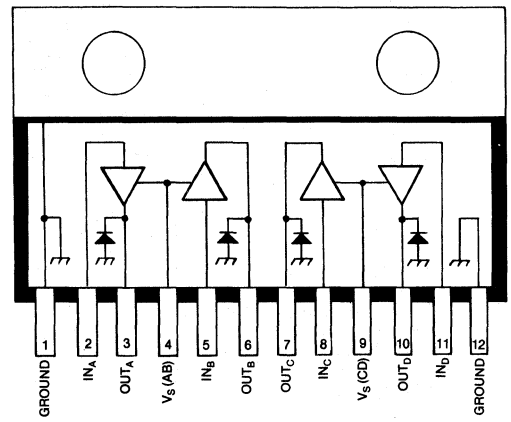
TYPICAL APPLICATION
QUAD RELAY DRIVE
Using 2 Voltage Sources
and Optional PWM Current Limiting

4

UDN-2948W
QUAD HIGH-CURRENT, HIGH-VOLTAGE SOURCE DRIVER

FEATURES

- Output Current to 6 A per Channel
- Output Voltage to 60 V
- Integral Output Suppression Diodes
- TTL and CMOS Compatible Inputs
- Plastic Single In-Line package
- Heat Sink Tab



Dwg. No. A-13,055

Providing space and cost-saving interface between microprocessor/LSI circuits and high-power peripheral loads such as solenoids, dc or stepper motors, incandescent displays, heaters, and similar loads, the UDN-2948W quad high-current, high-voltage source driver can drive loads to −6 A at supply voltages to 60 V (inductive loads to 35 V). The low-level inputs are TTL or CMOS compatible. The outputs include transient-suppression diodes for inductive loads. Individual supply lines are provided for each pair of drivers so that different supplies can be used to drive multiple loads.

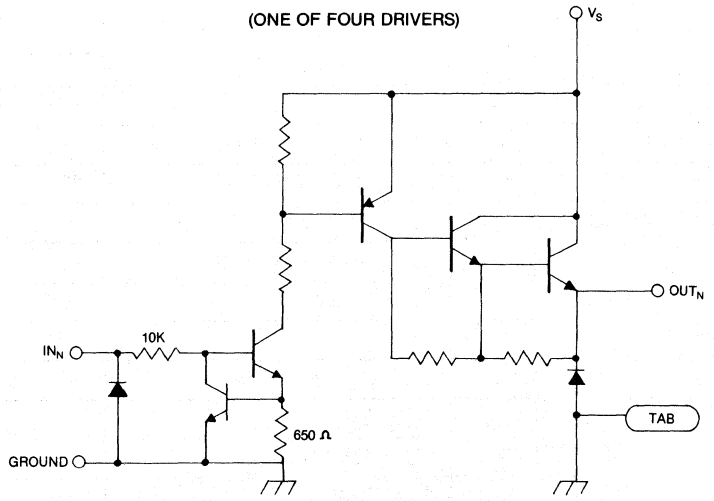
The application of source drivers for X-Y addressing of multiplexed power loads are obvious. A more subtle advantage of high-current source drivers is with inductive loads or incandescent lamps. Both types of load normally generate troublesome transients and noise currents on common logic/load ground lines. In addition, high ground currents produce IR drops that can shift the ground rail, affecting logic input levels, thresholds, and noise immunity. The use of source drivers can minimize many of these concerns by separating the logic and power returns.

For maximum allowable package power capability, the UDN-2948W driver is supplied in a 12-pin single in-line, power-tab package that allows efficient attachment of an external heat sink. The external heat sink is usually required for proper operation of this device. The heat sink tab is at ground potential and needs no insulation.

Similar 4 A devices with an input ENABLE control are supplied as the UDN-2944W.

FUNCTIONAL BLOCK DIAGRAM

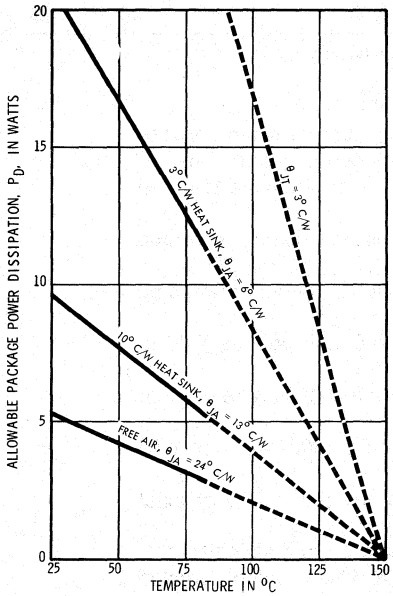
(ONE OF FOUR DRIVERS)



Dwg. No. A-13,056

4

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,794A

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Supply Voltage Range, V_S ..... 5.0V to 60V
Output Sustaining Voltage, $V_{CE(sus)}$ ..... Min. 35V
Output Current, I_{OUT} (dc) ..... −6A
(peak) ..... −7A
Input Voltage, V_{IN} 15V
Package Power Dissipation, P_D 5.2W*
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 41.6 mW/°C above T_A = +25°C.

Output current rating will be limited by ambient temperature, duty cycle, heat sinking, air flow, and number of outputs conducting. Under any set of conditions, do not exceed the −7.0A peak current and a junction temperature of +150°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq 70°C$, $V_S = 60$ V, (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Voltage Range	V_S		5.0	60	V
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, V_{IN} = 0.4V	—	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = −6A, L = 3 mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = −1A, V_{IN} = 2.4V	—	1.8	V
		I_{OUT} = −4A, V_{IN} = 2.4V	—	2.2	V
		I_{OUT} = −6A, V_{IN} = 2.4V	—	2.6	V
Input Voltage	$V_{IN(ON)}$		2.4	—	V
	$V_{IN(OFF)}$		—	0.8	V
Input Current	$I_{IN(ON)}$	V_{IN} = 2.4V	—	220	µA
		V_{IN} = 12V	—	1.5	mA
	$I_{IN(OFF)}$	V_{IN} = 0.8V	—	10	µA
Total Supply Current	I_S	One Driver ON, All Outputs Open	—	1.8	mA
Clamp Diode Leakage Current	I_R	V_R = 60V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 6A	—	2.9	V
Turn-On Delay	t_{ON}	0.5 E_{in} to 0.5 E_{out}, R_L = 15	—	2.0	µs
Turn-Off Delay	t_{OFF}	0.5 E_{in} to 0.5 E_{out}, R_L = 15	—	10	µs

NOTE: Negative current is defined as coming out of (sourcing) the device being tested.

APPLICATION NOTES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Use appropriate hardware including a lock washer or torque washer.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used.
4. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
5. The mounting hole should be as clean as possible with no burrs or ridges.
6. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
7. Strain relief must be provided if there is any probability of axial stress to the leads.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

UDN-2951Z AND UDN-2955W
8 A HALF-BRIDGE MOTOR DRIVERS

FEATURES

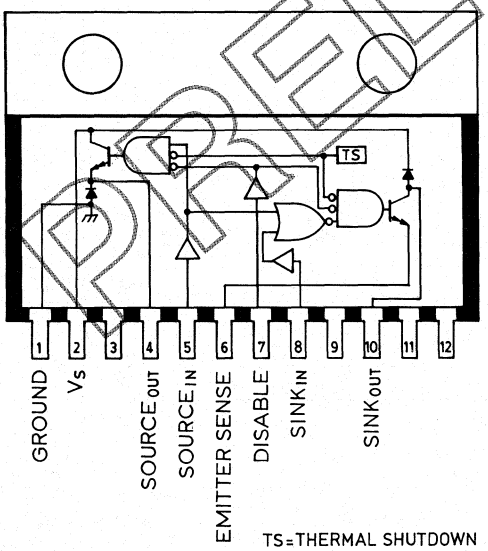
- 8 A Output Capability (DC)
- 50 V Operating Range
- Thermal Shutdown Circuitry
- Built-In Crossover Delays
- Disable and Emitter-Sense pins (UDN-2955W)
- Overvoltage Protection
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Internal Linear-Overcurrent Limiter

The UDN-2951Z and UDN-2955W half-bridge motor drivers can handle 8 A continuous load currents and output voltages up to 50 V. Both devices feature TTL, CMOS, PMOS, and NMOS compatible inputs, level shifting, and an internal voltage regulator for single-supply operation. Output transient-suppression diodes in both sink and source drivers have been incorporated.

The UDN-2951Z and UDN-2955W both have internal delay times to guard against hazardous cross-over currents. Both devices maintain internal current limiting, overvoltage protection up to 75 V, and thermal shutdown at 165°C.

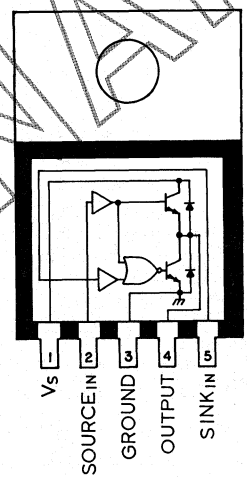
The UDN-2955W has extended flexibility with an external emitter sense pin on the sink driver, separated sink and source outputs, and a DISABLE input that can be used in high-speed chopper applications.

The UDN-2951Z is supplied in a TO-220 power-tab package for enhanced power dissipation capabilities and minimal size. The UDN-2955W is supplied in a 12-pin single in-line plastic power-tab package for exceptional power handling capabilities. This power-tab configuration allows for easy attachment of an external heat-sink for extended power-handling capabilities.



Dwg. No. A-14,192

UDN-2955W



Dwg. No. A-14,191

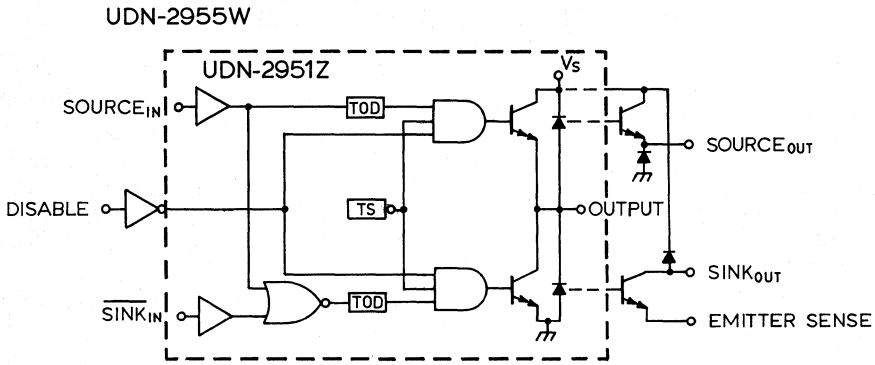
UDN-2951Z

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage Range, V_S	10 V to 75 V†
Output Voltage Range, V_{OUT}	0 V to 50 V
Output Current, I_{OUT} (DC)	8 A
Input Voltage Range, V_{IN}	−0.7 V to 9.0 V
Package Power Dissipation, P_D	
(Z Package)	3.125 W*
(W Package)	5.2 W**
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 25 mW/°C above T_A = +25°C.
**Derate at the rate of 41.66 mW/°C above T_A = +25°C.
†Internal over-voltage shutdown above 50 V.

FUNCTIONAL BLOCK DIAGRAM



TOD = TURN ON DELAY, TS = THERMAL SHUTDOWN

Dwg. No. A-14,190

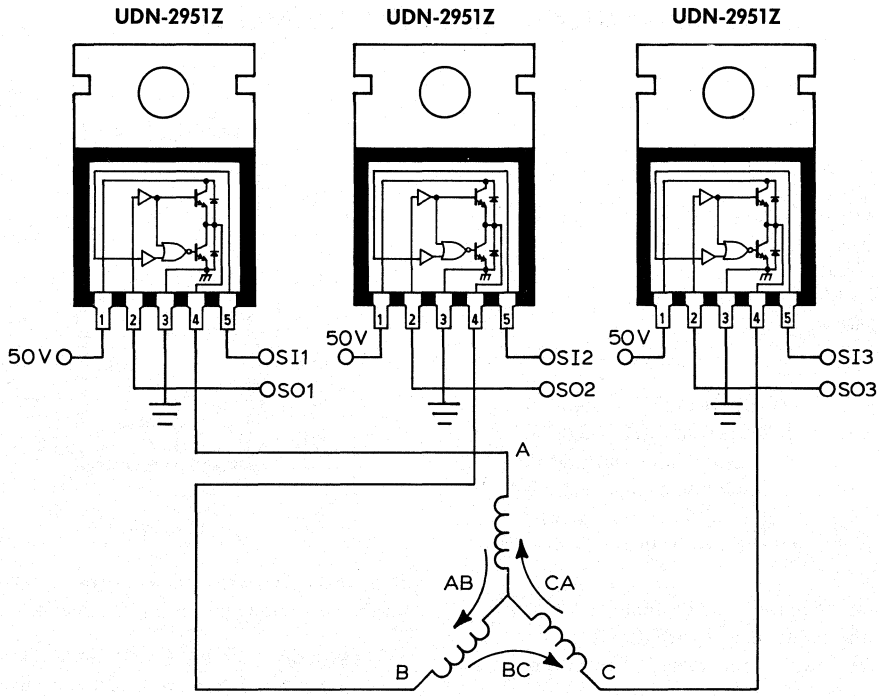
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 50 V, DISABLE (UDN-2955W) = 0 V

Characteristic	Symbol	Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	—	50	µA
		V_{OUT} = 0 V	—	—	−50	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = ±8 A, L = 3 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = ±8 A	—	—	2.0	V
Short-Circuit Source Current	I_{OUT}		−8.0	—	−12	A
Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	—	—	0.5	mA
	$I_{IN(0)}$	V_{IN} = 0.8 V	−6.0	—	—	µA
Propagation Delay	t_{PHL}	I_{OUT} = 8 A, Resistive Load, Sink Driver	—	2.5	—	µs
	t_{PLH}	I_{OUT} = 8 A, Resistive Load, Sink Driver	—	0.2	—	µs
	t_{PHL}	I_{OUT} = −8 A, Resistive Load, Source Driver . .	—	2.5	—	µs
	t_{PLH}	I_{OUT} = −8 A, Resistive Load, Source Driver	—	2.5	—	µs
Clamp Diode Forward Voltage	V_F	I_F = 8 A	—	2.0	—	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	µA
Supply Current	I_S	V_{SOURCE} = 2.0 V	—	—	12	mA
		V_{SINK} = V_{SOURCE} = 0.8 V	—	—	20	mA
Thermal Shutdown Temperature	T_J	Note 1	—	165	—	°C
Over-Voltage Shutdown	V_S		50	—	60	V

1. Thermal shutdown has a typical hysteresis of 15°C.

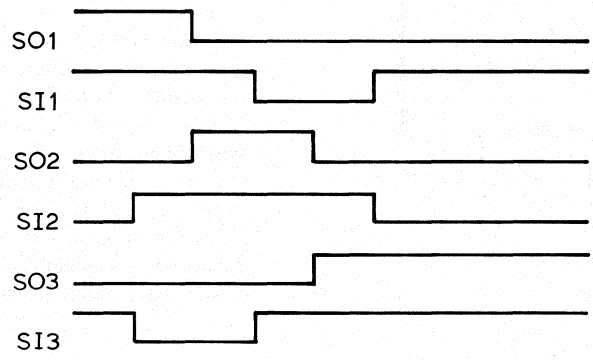
TYPICAL APPLICATION

3-PHASE BRUSHLESS DC MOTOR DRIVE



Dwg. No. A-14,144

INPUT WAVEFORMS



Dwg. No. A-14,145

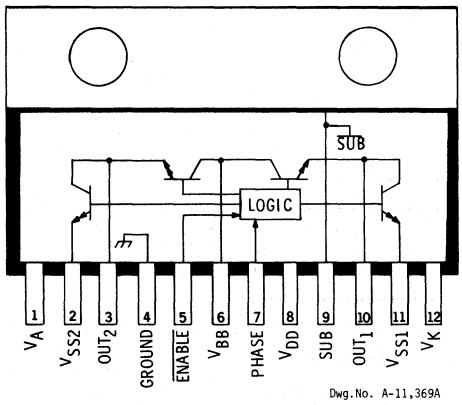
UDN-2952B AND UDN-2952W FULL-BRIDGE MOTOR DRIVERS

FEATURES

- High Output Current
- Adjustable Short-Circuit Protection
- Thermal Protection
- Internal Clamp Diodes
- TTL, DTL, PMOS, CMOS Compatible
- DIP or SIP Packaging

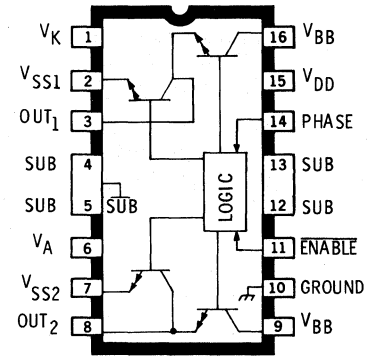
FULL-BRIDGE MOTOR-DRIVER integrated circuits, Types UDN-2952B and UDN-2952W combine low-level logic circuitry and Darlington output power drivers for bidirectional control of d-c motors or solenoids operating with continuous load currents of up to 2A and peak start-up currents as high as 3.5A.

For applications requiring load currents of 1A or less (2A peak), the economical Type UDN-2952B-2 and UDN-2952W-2 are recommended. The lower-cost devices are identical to the basic parts, except for the maximum allowable load-current rating.



Dwg.No. A-11,369A

UDN-2952W



Dwg.No. A-11,368B

UDN-2952B

These monolithic integrated circuits have extensive circuit protection. Both drivers have thermal shutdown networks that disable motor drive if the package power dissipation ratings are exceeded. Internal diode transient suppression is provided on-chip. Output-current limiting is determined by the user's selection of a sensing resistor.

The Type UDN-2952B full-bridge power driver is supplied in a 16-pin dual in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. Type UDN-2952W, for higher power requirements, is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation. For output currents above 700 mA at normal ambient temperatures, both drivers require an external heat sink.

ABSOLUTE MAXIMUM RATINGS at T_{TAB} = +70°C

Motor Supply Voltage Range, V_{BB} . . . . . 4.5V to 40V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5V to 15V
Substrate Voltage Range, V_{SUB} . . . . . 0V to −20V
Logic Input Voltage, V_{PHASE} or V_{ENABLE} 30V
Output Current, I_{OUT} (UDN-2952B and UDN-2952W) . . . . ±3.5A
(UDN-2952B-2 and UDN-2952W-2) . . . ±2A
Package Power Dissipation, P_D . . . . . See Graphs
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

TRUTH TABLE

$\overline{ENABLE}$	PHASE	V_{SS}	V_{DD}	OUT_1	OUT_2
High	X	X	X	Open	Open
Low	High	<0.8 V	>4.5 V	High	Low
Low	Low	<0.8 V	>4.5 V	Low	High
X	X	>0.9 V	>4.5 V	Open	Open
X	X	X	0 V	Open	Open

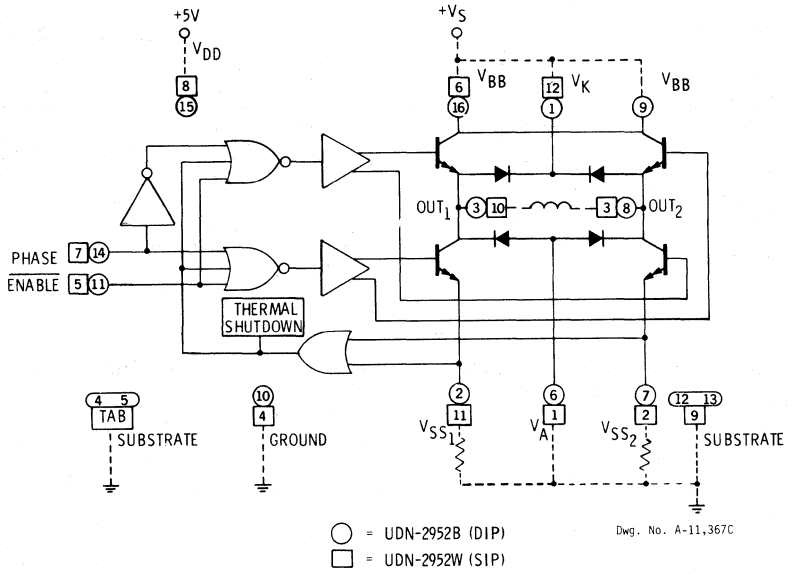
X = Irrelevant.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 40V, V_{DD} = 5V, $T_{TAB} \leq$ +70°C, Figure 1 (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Drivers (OUT_1 or OUT_2)						
Output Leakage Current	I_{CEX}	V_{ENABLE} = 5V, V_{OUT} = V_{BB}, Note 1	—	—	500	µA
		V_{ENABLE} = 5V, V_{OUT} = 0V, Note 1	—	—	−500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 0V, I_{OUT} = 1A, Notes 1 and 2	—	1.2	1.5	V
		V_{ENABLE} = 0V, I_{OUT} = 2A, Notes 1 and 3	—	1.5	2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 1A, Figure 2, Notes 1 and 2	40	—	—	V
		I_{OUT} = 2A, Figure 2, Notes 1 and 3	40	—	—	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8V, Outputs Open, Note 1	—	15	30	mA
	$I_{BB(OFF)}$	V_{ENABLE} = 2.4V, Outputs Open, Note 1	—	3.0	5.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1A, Note 2	—	1.0	1.5	V
		I_F = 2A, Note 3	—	1.8	2.2	V
Control Logic (PHASE or $\overline{ENABLE}$)						
Logic Open-Circuit Voltage	V_{IN}	I_{PHASE} or I_{ENABLE} = −250 µA	—	—	7.5	V
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or V_{ENABLE} = 2.4V	—	−50	−100	µA
	$I_{IN(0)}$	V_{PHASE} or V_{ENABLE} = 0.8V	—	−1.0	−1.6	mA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	15	30	mA
Sense Trigger Voltage	V_{SS}	V_{ENABLE} = 0.8V	—	850	—	mV
Turn-On Delay Time	t_{pd0}	Source Drivers	—	1.0	—	µs
		Sink Drivers	—	0.5	—	µs
Turn-Off Delay Time	t_{pd1}	Source Drivers	—	2.0	—	µs
		Sink Drivers	—	1.0	—	µs
Thermal Shutdown	T_J		—	175	—	°C

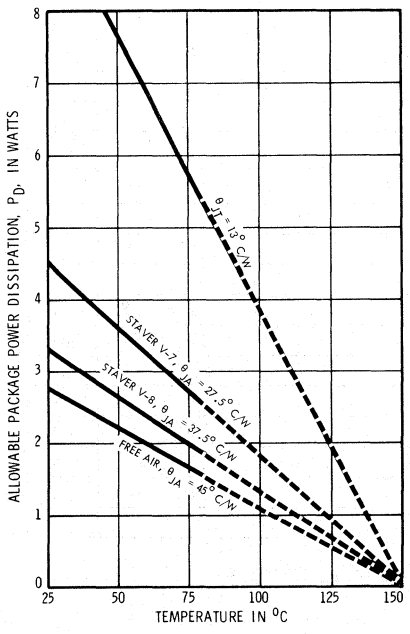
NOTES: 1. Test is performed with V_{PHASE} = 0.8V and then repeated for V_{PHASE} = 2.4V.
2. Output measurement at 1A are applicable to the UDN-2952B, UDN-2952B-2, UDN-2952W, and UDN-2952W-2.
3. Output measurements at 2A are applicable only to the UDN-2952B and UDN-2952W.

FUNCTIONAL BLOCK DIAGRAM



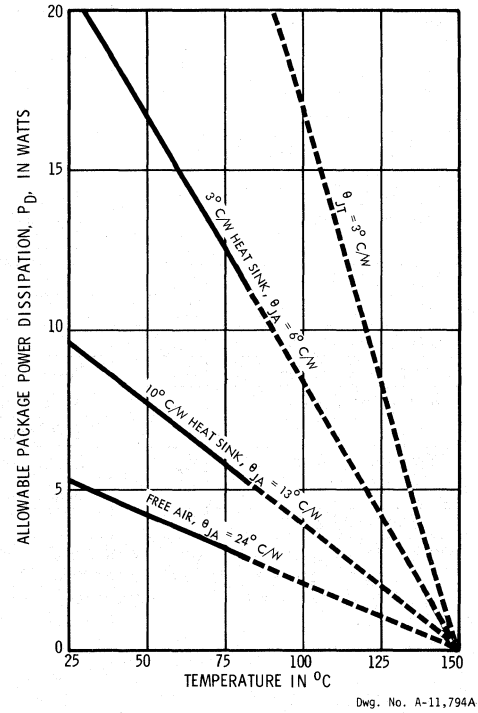
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

UDN-2952B



Dwg. No. A-11,793A

UDN-2952W



Dwg. No. A-11,794A

TEST FIGURES

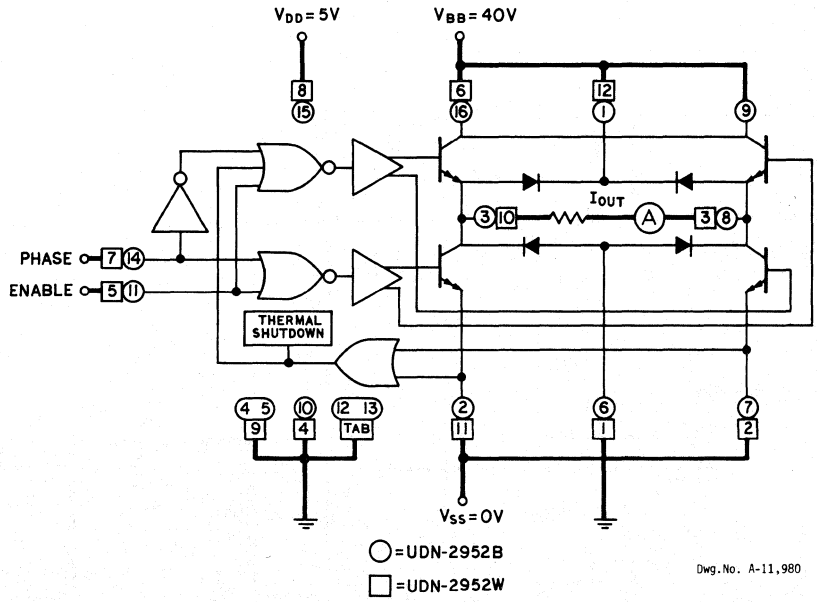


FIGURE 1

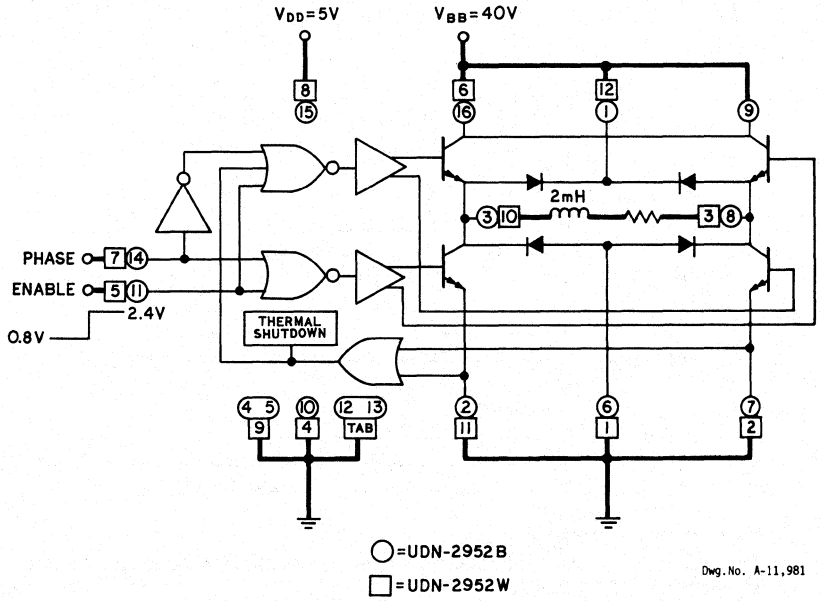
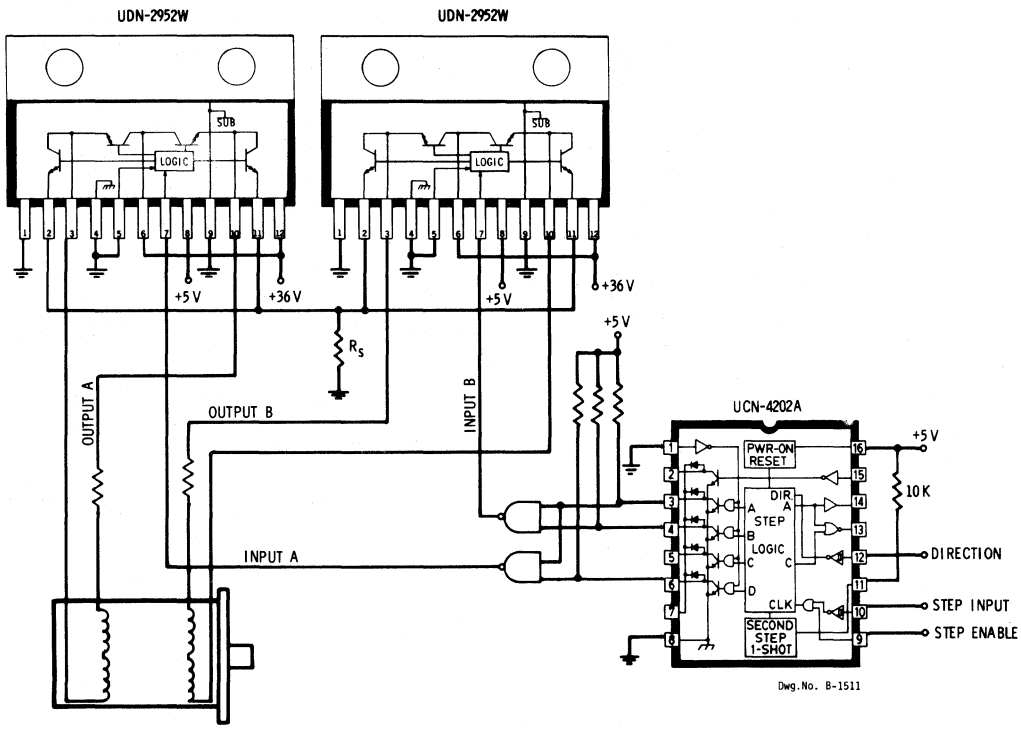
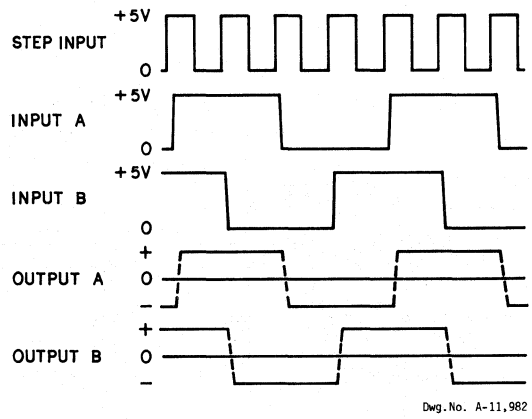


FIGURE 2

TYPICAL APPLICATIONS



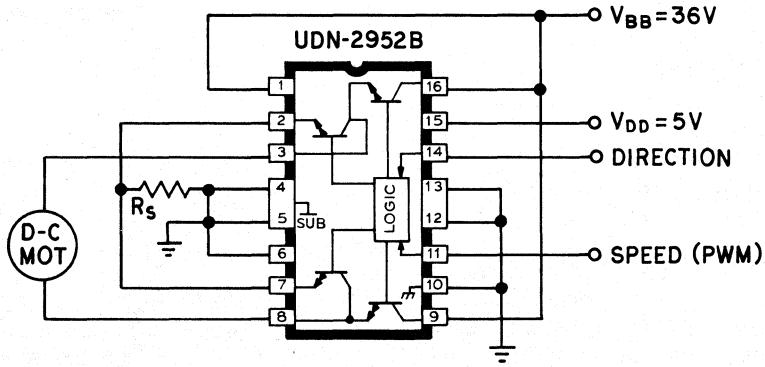


NOTES:

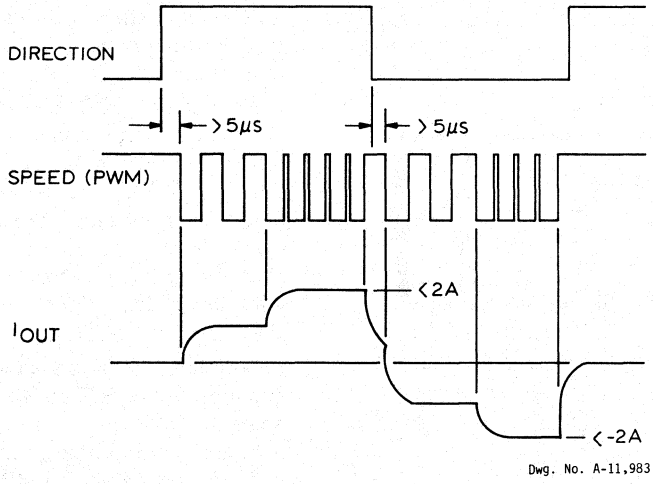
1. This is *not* a bipolar chopper application.
2. Resistor R_S sets the maximum allowable output current for protection against crossover currents and short circuits. $R_S = 0.6/I_{LIMIT}$.

TYPICAL APPLICATIONS

FULL-BRIDGE DC SERVO MOTOR APPLICATION



Dwg.No. A-11,984



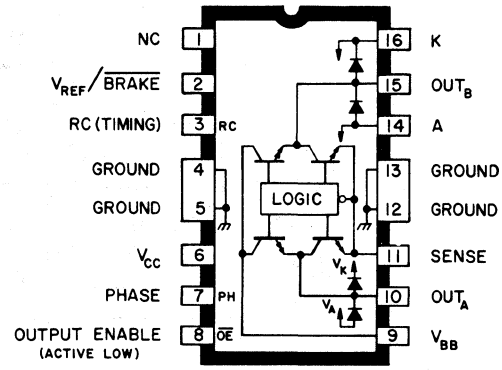
Dwg. No. A-11,983

UDN-2953B AND UDN-2954W FULL-BRIDGE PWM MOTOR DRIVERS

FEATURES

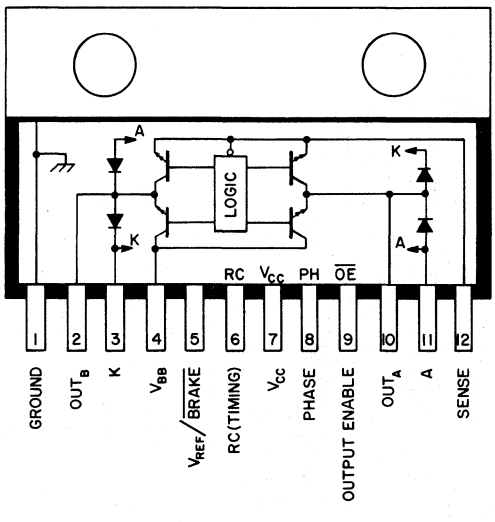
- 50 V Output Voltage Rating
- 2 A Continuous Output Rating
- Internal Flyback Diodes
- Thermal Shutdown
- Crossover Current Protection
- BRAKE, ENABLE, and Current-Limit Functions

The UDN-2953B and UDN-2954W are designed for bidirectional control of dc or stepper motors with continuous output currents to 2 A and peak start-up currents as high as 3.5 A. For pulse-width modulated (chopped-mode) operation, the output current is determined by the user's selection of a reference voltage and sensing resistor while the OFF pulse duration is set by an external RC timing network. PWM operation is characterized by maximum efficiency and low power-dissipation levels. Extensive internal circuit protection includes thermal shutdown with hysterisis, transient-suppression diodes, and crossover current protection.



Dwg. No. A-13,024

UDN-2953B



Dwg. No. A-13,023

UDN-2954W

When the $V_{REF}/\overline{BRAKE}$ pin is low (<0.8 V, the braking function is enabled. This turns both sink drivers OFF and the source drivers are turned ON. When $V_{REF}/\overline{BRAKE}$ is set above 2.4 V, that voltage (and the current sensing resistor) determines the load current trip point. An RC TIMING pin is available to use for an internal one-shot to control load current decay time.

The UDN-2953B driver is supplied in a 16-pin dual-in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. The UDN-2954W, for higher package power dissipation requirements, is supplied in a 12-pin single in-line power tab package. In both package styles, the heat sink is at ground potential and needs no insulation.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

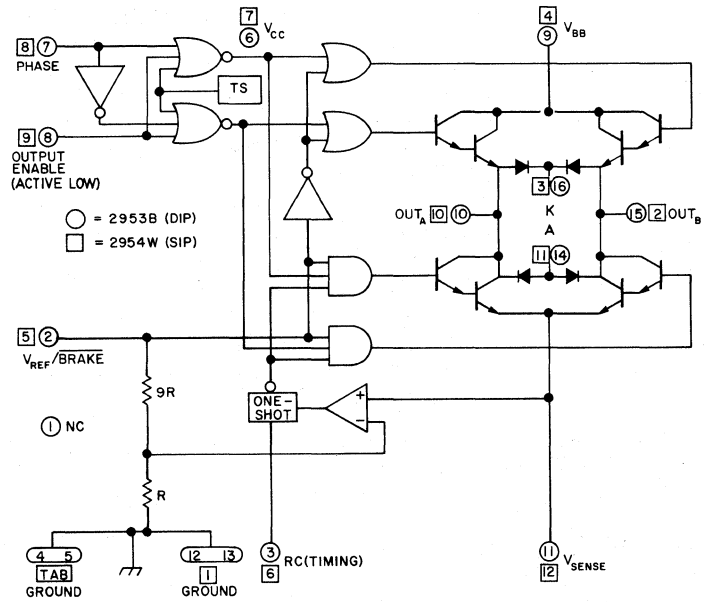
Motor Supply Voltage, V_{BB} . . . . . 50 V
Output Current, I_{OUT} (Peak) . . . . . ±3.5 A
(Continuous) . . . . . ±2.0 A
Flyback Diode Voltage, V_K . . . . . V_{BB}
Minimum Clamp Diode Voltage, V_A . . . . . Ground
Logic Supply Voltage, V_{CC} . . . . . 7.0 V
Logic Input Voltage, V_{PHASE}, V_{ENABLE} . . . . . V_{BB}
Sense Voltage, V_{SENSE} . . . . . 1.5 V
Reference Voltage, V_{REF}/$\overline{BRAKE}$ . . . . . 15 V
Package Power Dissipation, P_D . . . . . See Graphs
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_{BB} = 50$ V, $V_{CC} = 5$ V, $V_{SENSE} = 0$ V, 5 kΩ RC to Ground

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers (OUT_A or OUT_B)						
Output Supply Range	V_{BB}		6.5	—	50	V
Output Leakage Current	I_{CEX}	V_{ENABLE} = 5 V, V_{OUT} = V_{BB}, (note)	—	—	50	µA
		V_{ENABLE} = 5 V, V_{OUT} = 0 V, (note)	—	—	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±2 A, L = 2 mH	50	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{ENABLE} = 0 V, I_{OUT} = ±0.5 A	—	1.0	1.2	V
		V_{ENABLE} = 0 V, I_{OUT} = ±1.0 A	—	1.2	1.4	V
		V_{ENABLE} = 0 V, I_{OUT} = ±2.0 A	—	1.5	1.8	V
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 2 A	—	1.8	2.2	V
Motor Supply Current	$I_{BB(ON)}$	V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V, No Load	—	20	30	mA
	$I_{BB(OFF)}$	V_{ENABLE} = V_{REF} = 2.4 V, No Load	—	1.7	2.5	mA
		V_{ENABLE} = 5 V, V_{REF} = 0.8 V, No Load	—	40	60	mA
Control Logic						
Logic Supply Range	V_{CC}		4.5	5.0	5.5	V
Logic Input Current	$I_{IN(1)}$	All Inputs = 2.4 V	—	<−1	−10	µA
	$I_{IN(0)}$	All Inputs = 0.8 V	—	−50	−200	µA
Logic Input Voltage	$V_{IN(1)}$	All Inputs	2.4	—	—	V
	$V_{IN(0)}$	All Inputs	—	—	0.8	V
V_{REF} Open-Circuit Voltage	$V_{REF(OPEN)}$	I_{REF} = 0	—	V_{CC}/2	—	V
Current Limit Threshold		V_{REF}/V_{SENSE} at Trip Point	9.5	10	10.5	—
Turn-On Delay	t_{on}	All Drivers	—	1.0	—	µs
Turn-Off Delay	t_{off}	All Drivers	—	1.0	—	µs
Thermal Shutdown Temp.	T_J		—	165	—	°C
Logic Supply Current	I_{CC}	V_{ENABLE} = V_{REF} = 2.4 V	—	15	20	mA
		V_{ENABLE} = 0.8 V, V_{REF} = 2.4 V	—	22	30	mA

Note: Tests performed at OUT_B with V_{PHASE} = 0.8 V and at OUT_A with V_{PHASE} = 2.4 V

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,028

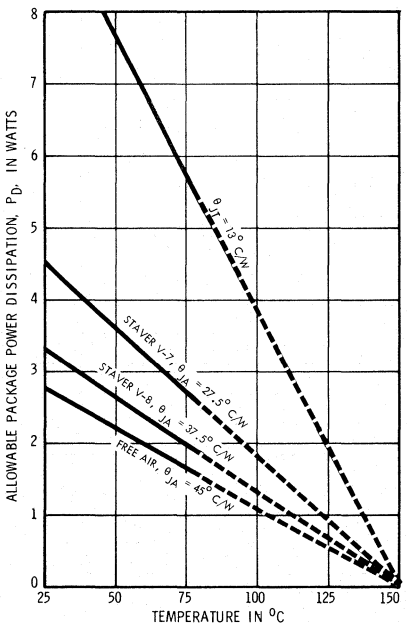
TRUTH TABLE

OUTPUT ENABLE	PHASE	V_{REF}/$\overline{BRAKE}$	OUT_A	OUT_B
Low	High	>2.4 V	High	Low
Low	Low	>2.4 V	Low	High
High	X	>2.4 V	Open	Open
X	X	<0.8 V	High	High

X = Irrelevant.

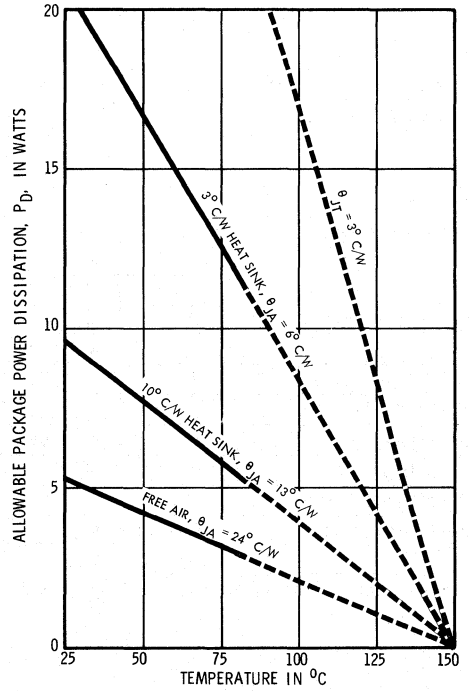
ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

UDN-2953B



Dwg. No. A-11,793A

UDN-2954W



Dwg. No. A-11,794A

APPLICATIONS

The UDN-2953B and UDN-2954W full-bridge drivers are ideal for driving 2-phase bipolar stepper, bidirectional dc servo, and brushless dc motors with various pulse-width modulation (PWM) current-control formats. Output current is controlled by using an external sense resistor and an optional RC network and reference voltage for an internal fixed-frequency PWM circuit, or by using an external PWM source.

The output current trip point is set by:

$$I_{OUT} = V_{REF}/10\,R_{SENSE}$$

When the current in the sense resistor (typically $\leq 0.5\,\Omega$) reaches the set point, an internal one-shot turns OFF the sink drivers for a time period (t_{off}) determined by an RC time constant. The actual peak load current will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 μs.

The t_{off} time interval (see Fig. 1) is approximately RC within the range of 20 kΩ to 100 kΩ and 200 pF to 500 pF. If the RC pin is tied to V_{CC}, internal delay circuitry is activated, allowing PWM operation without the external RC network. Under this condition, I_{CC} will increase approximately 6 mA. The internally-generated t_{off} is approximately 12 μs at V_{CC} = 5 V and T_A = +25°C, increasing slightly with increasing temperatures.

For external current control, V_{REF} can be between 2.4 V and 15 V. If left unconnected, V_{REF} defaults to $V_{CC}/2$ (Fig. 2).

Average motor current can also be adjusted by external pulse-width modulation using the OUTPUT ENABLE pin. Toggling the OUTPUT ENABLE line shuts OFF both the source and sink drivers. Both the flyback and ground-clamp diodes conduct, resulting in very fast current decay. In this mode, the RC pin should be connected to ground through a 5 kΩ resistor.

With the RC pin connected to V_{CC}, V_{REF} and R_{SENSE} selected for a trip point greater than normal operation, but less than 3.5 A, over-current protection is provided (Fig. 3).

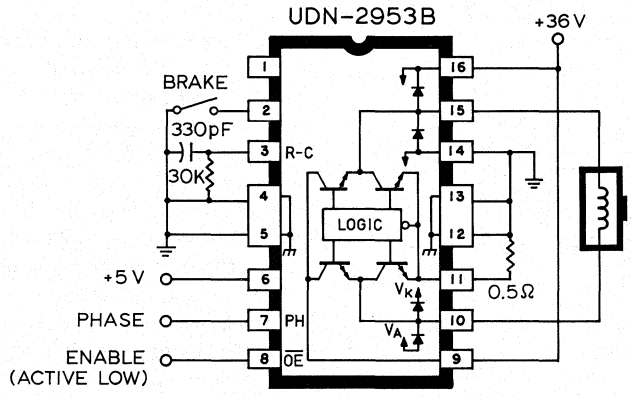
A logic low at the $V_{REF}/\overline{BRAKE}$ pin turns ON both source drivers and turns OFF both sink drivers, thus dynamically braking the motor.

An internally-generated deadtime of about 3 μs reduces crossover-currents that can occur when switching phases or braking.

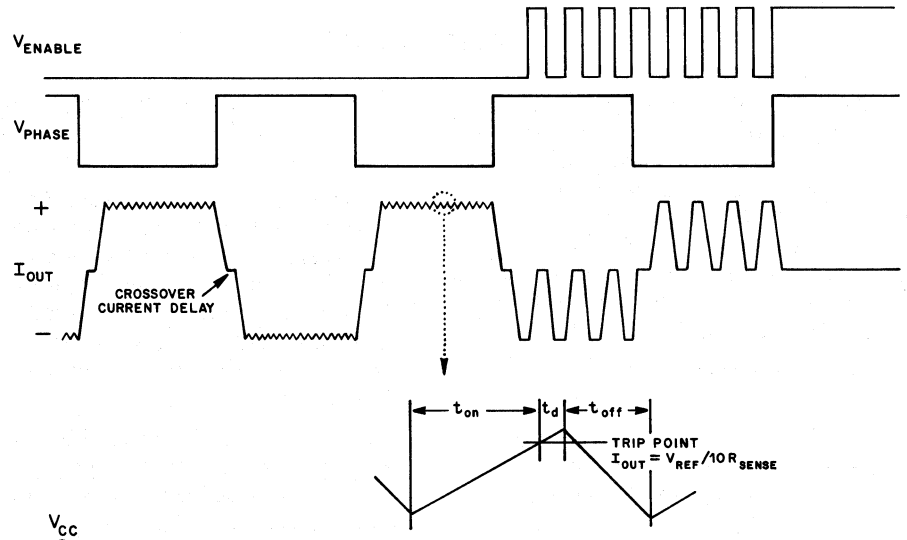
Thermal protection circuitry is activated and turns OFF all drivers at a junction temperature of typically 165°C. It is only intended to protect the chip from catastrophic failures due to excessive junction temperatures. The thermal shutdown has a hysteresis of approximately 8°C.

4

TYPICAL APPLICATION

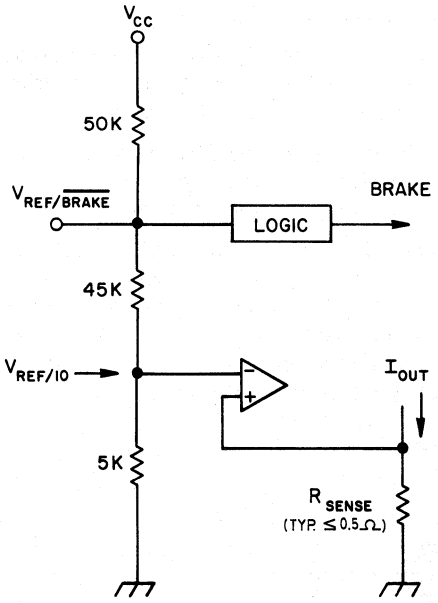


Dwg. No. A-12,649B



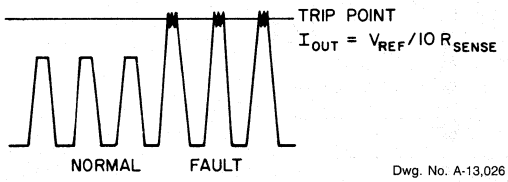
Dwg. No. A-13,027A

FIGURE 1



Dwg. No. A-13,025

FIGURE 2



Dwg. No. A-13,026

FIGURE 3

MOUNTING OF POWER TAB DEVICES

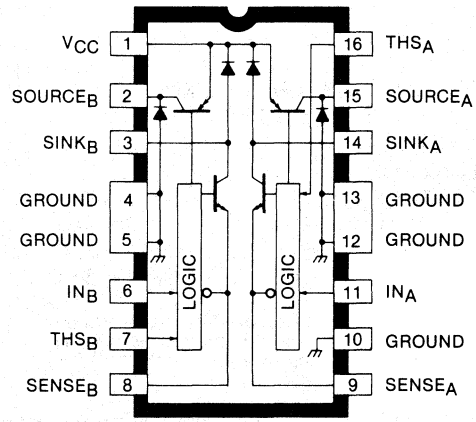
Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. "Brute force" mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

UDN-2962B AND UDN-2962W
DUAL SOLENOID/MOTOR DRIVERS
Pulse-Width Modulated Current Control

FEATURES

- 4 A Peak Output
- 45 V Min. Sustaining Voltage
- Internal Clamp Diodes
- TTL/PMOS/CMOS Compatible Inputs
- High-Speed Chopper
- DIP or SIP Packaging



UDN-2962B

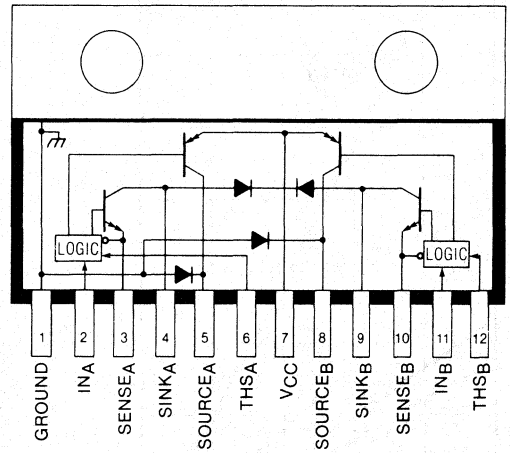
Dwg. No. D-1000

Using PWM to minimize power dissipation and maximize load efficiency, the UDN-2962B and UDN-2962W dual drivers are recommended for impact printer solenoids and stepper motors. Each device is comprised of two source/sink driver pairs rated for continuous operation to ±3A. They can be connected to drive two independent loads or a single load in the full-bridge configuration. All drivers include output clamp/flyback diodes, input gain and level shifting, a voltage regulator for single-supply operation, and pulse-width modulated output-current control circuitry. Inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The peak output current and hysteresis for each source/sink pair is set independently. Output current, threshold voltage, and hysteresis are set by the user's selection of external resistors. At the specified output-current trip level, the source driver turns OFF. The internal clamp diode then allows current to flow without additional input from the power supply. When the lower current trip point is reached, the source driver turns back ON.

The UDN-2962B dual solenoid/motor driver is supplied in a 16-pin dual in-line plastic package with copper heat-sink contact tabs for medium package power dissipation levels (2.2W to >5W at +50°C). The lead configuration enables easy

Continued next page



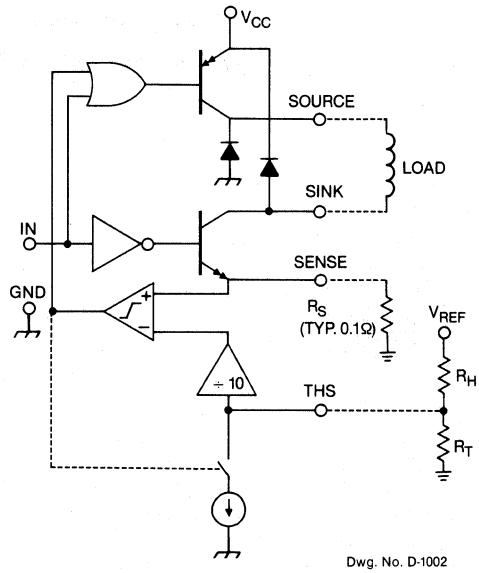
UDN-2962W

Dwg. No. D-1001

attachment of a heat sink while fitting a standard printed wiring board layout. The UDN-2962W, for higher package power dissipation requirements, is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation. With either package, for high-current or high-frequency applications, external heat sinking may be required.

FUNCTIONAL BLOCK DIAGRAM

(One of Two Drivers)



Dwg. No. D-1002

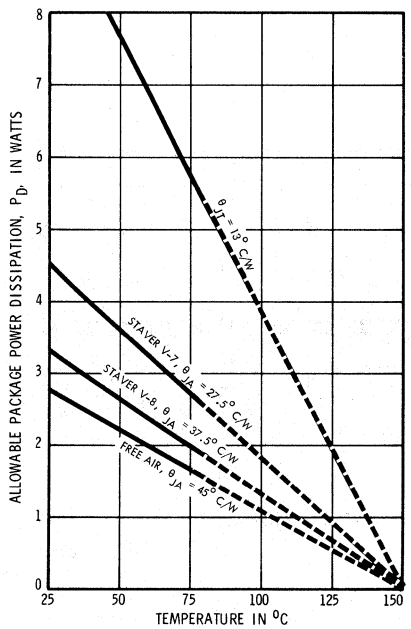
ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

Supply Voltage, V_{CC}	45V
Peak Output Current, I_{OUT}	±4A
Input Voltage Range, V_{IN}	−0.3V to +7.0V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

NOTE: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

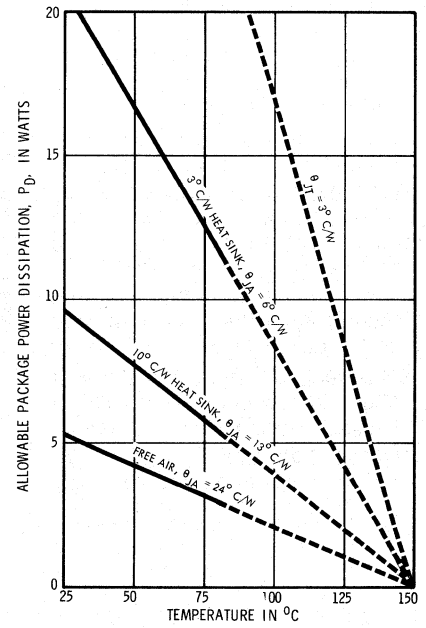
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

UDN-2962B



Dwg. No. A-11,793A

UDN-2962W



Dwg. No. A-11,794A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_{TAB} \leq$ +70°C, V_{CC} = 45V, V_{SENSE} = 0V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	V_{CC}	Operating	20	—	45	V
Output Drivers						
Output Leakage Current	I_{CEX}	V_{IN} = 2.4V, V_{SOURCE} = 0V	—	< −1.0	−100	μA
		V_{IN} = 2.4V, V_{SINK} = 45V	—	<1.0	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Drivers, I_{LOAD} = 3.0A	—	2.1	2.3	V
		Source Drivers, I_{LOAD} = 1.0A	—	1.7	1.9	V
		Sink Drivers, I_{LOAD} = 3.0A	—	1.7	1.9	V
		Sink Drivers, I_{LOAD} = 1.0A	—	1.1	1.3	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±3.0A, L = 3.5 mH	45	—	—	V
Output Current Regulation	ΔI_{OUT}	V_{THS} = 0.6V to 1.0V, L = 3.5 mH	—	—	±25	%
		V_{THS} = 1.0V to 2.0V, L = 3.5 mH	—	—	±10	%
		V_{THS} = 2.0V to 5.0V, L = 3.5 mH	—	—	±5.0	%
Clamp Diode Forward Voltage	V_F	I_F = 3.0A	—	1.7	2.0	V
Output Rise Time	t_r	I_{LOAD} = 3.0A 10% to 90%, Resistive Load	—	0.5	1.0	μs
Output Fall Time	t_f	I_{LOAD} = 3.0A, 90% to 10%, Resistive Load	—	0.5	1.0	μs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.4V	—	1.0	10	μA
	$I_{IN(0)}$	V_{IN} = 0.8V	—	−20	−100	μA
	$I_{THS(ON)}$	$V_{THS} \geq$ 500 mV, $V_{SENSE} \leq V_{THS}/10.5$	—	−2.0	—	μA
	$I_{THS(HYS)}$	$V_{SENSE} \geq V_{THS}/9.5$, V_{THS} = 0.6V to 5.0V	140	200	260	μA
V_{THS}/V_{SENSE} Ratio	—	V_{THS} = 2.0V to 5.0V	9.5	10	10.5	—
Supply Current (Total Device)	I_{CC}	V_{IN} = 2.4V, Outputs OFF	—	8.0	12	mA
		V_{IN} = 0.8V, Outputs Open	—	25	40	mA
Propagation Delay Time (Resistive Load)	t_{pd}	50% V_{IN} to 50% V_{OUT}, Turn OFF	—	—	2.5	μs
		50% V_{IN} to 50% V_{OUT}, Turn ON	—	—	3.0	μs
		100% V_{SENSE} to 50% V_{OUT}*	—	—	2.0	μs

*Where $V_{SENSE} \geq V_{THS}/9.5$
NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

TRUTH TABLE

V_{IN}	V_{SENSE}	SOURCE DRIVER	SINK DRIVER
High	NA	Off	Off
Low	$<V_{THS}/10$	On	On
Low	$>V_{THS}/10$	Off	On

APPLICATIONS

The UDN-2962B/W driver is intended for use as a free-running, pulse-width modulated, motor or solenoid driver.

The source and sink drivers are both turned ON by a low level at the input. When the load current reaches the trip point (set by external resistors), the comparator output goes high and the source driver is turned OFF. The internal clamp diode then allows current to flow without further input from the power supply. An internal constant current sink reduces the trip point (hysteresis) until the decaying current reaches the lower threshold, when the comparator output goes low and the source driver is again turned ON. Hysteresis percentage is a function of the external resistance R_H and is independent of the peak output load current set by R_T. The chopping frequency is asynchronous and a function of the system and circuit parameters, including load inductance, supply voltage, hysteresis setting, and switching speed of the driver.

Maximum load current and hysteresis percentage are determined by the user:

$$R_H = 50 V_{REF} H$$

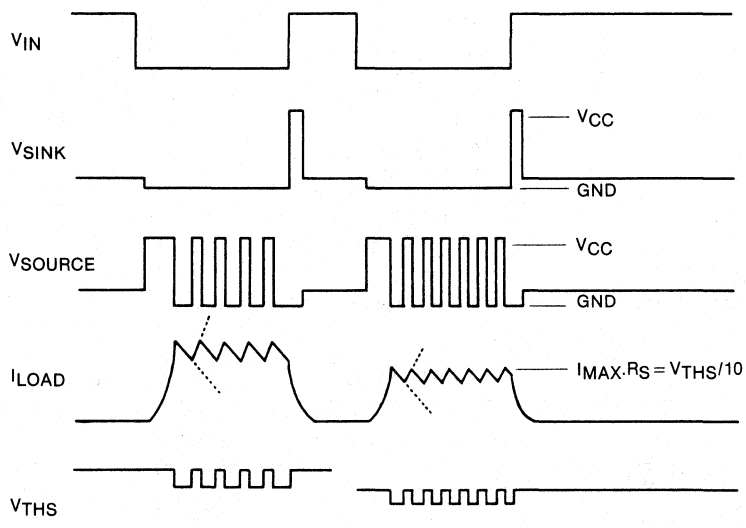
$$R_T = \frac{R_H(10\, I_{MAX}\, R_S)}{V_{REF} - (10\, I_{MAX}\, R_S)}$$

where $10\, I_{MAX}\, R_S = V_{THS} = 0.6$ to $5.0V$

and H = desired hysteresis in percent.

Graphical solutions for R_H and R_T, with $V_{REF} = 5$ V and $R_S = 0.1\ \Omega$, follow.

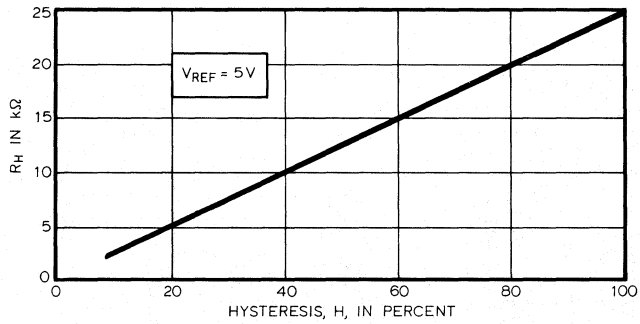
TYPICAL WAVESHAPES



Dwg. No. D-1003

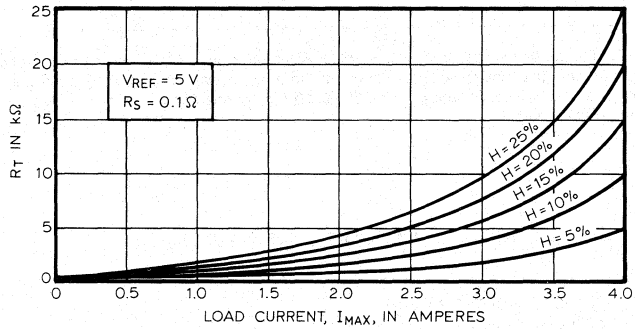
APPLICATIONS

RESISTOR R_H VALUE AS A FUNCTION OF HYSTERESIS



Dwg. No. A-12,417

RESISTOR R_T VALUE AS A FUNCTION OF PEAK LOAD CURRENT



Dwg. No. A-12,416

For optimum operation of the UDN-2962B/W, the following design guidelines should be observed:

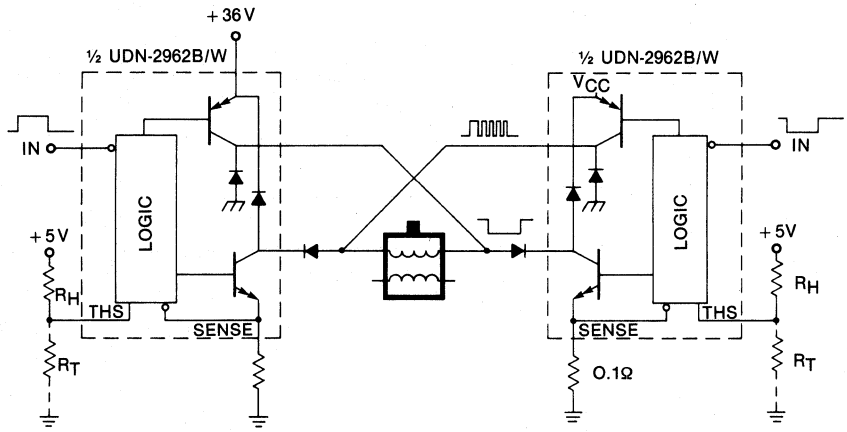
1. The V_{CC} supply should be decoupled with an electrolytic capacitor (10 μF or greater). This capacitor should be placed as close to the driver as possible.

2. To minimize IR drops in the ground line, the printed wiring board should utilize a heavy ground plane; the driver should be soldered into the board, not used in a socket.

3. When using the UDN-2962B/W in an H-bridge configuration, a high-speed discrete diode must be used in series with each sink driver.

TYPICAL APPLICATION

BIPOLAR, PULSE-WIDTH MODULATED, STEPPER-MOTOR DRIVE



Dwg. No. D-1004

R_H AND R_T DETERMINE HYSTERESIS AND PEAK CURRENT

NOTE: Each of the drivers within the ***UDN-2962B/W*** *includes an internal logic delay to prevent potentially destructive crossover currents within the driver during phase changes. However, never simultaneously enable both inputs in the full-bridge configurations: A destructive short-circuit to ground will result.*

MOUNTING POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. Brute force mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

UDN-2965W-2 DUAL SOLENOID/MOTOR DRIVER

—Pulse-Width Modulated Current Control

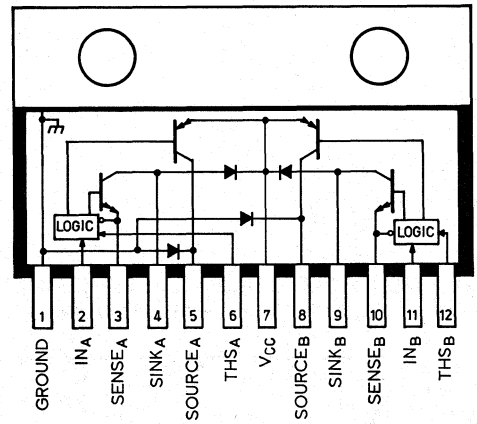
FEATURES

- 5 A Peak Output
- 50 V Min. Output Sustaining Voltage
- TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- Internal Thermal Shutdown
- High-Speed Chopper
- Plastic SIP With Heat-Sink Tab

DESIGNED TO DRIVE impact printer solenoids and stepper motors, the UDN-2965W-2 includes two independent driver pairs rated for continuous operation to ±4 A. Each half-bridge driver includes diode transient protection, input gain and level shifting, a voltage regulator for single-supply operation, thermal protection, and pulse-width modulate (PWM) output-current control. Inputs are compatible with most TTL, DTL, LSTTL, and low-voltage CMOS or PMOS logic.

The PWM mode helps minimize power dissipation and maximize load efficiency. The peak output current and hysteresis for each half-bridge is set independently. Output current, threshold voltage, and hysteresis are set by the user's selection of external resistors. If desired, internal threshold and hysteresis defaults (400 mV and ≤10%) can be used. At the specified output-current trip level, the source driver turns OFF. The internal flyback diode then allows current to flow without additional input from the power supply. When the lower current trip point is reached, the source driver turns back ON.

For maximum power-handling capability, the driver is supplied in 12-pin single in-line power tab package. An external heat sink is required for proper operation. The tab is at ground potential and needs no insulation.



Dwg. No. A-12,413A

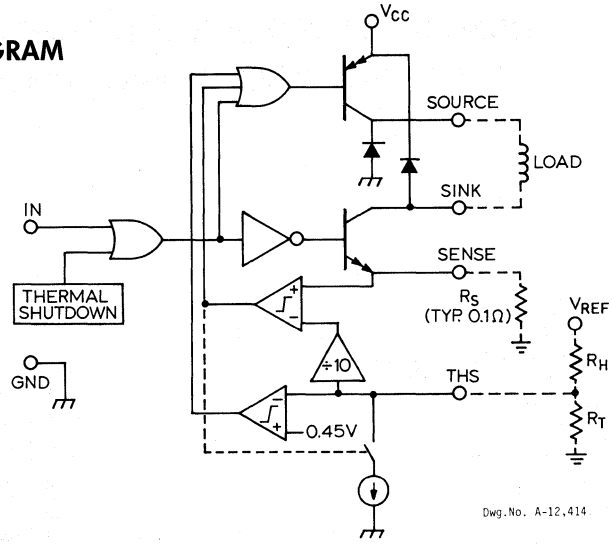
Devices with sustaining voltage ratings of 60 V are presently in development as the UDN-2965W (no suffix). Similar dual 4 A solenoid drivers, for non-PWM applications, are available as Sprague Types UDN-2975W and UDN-2976W.

ABSOLUTE MAXIMUM RATINGS at $T_{TAB} \leq +70°C$

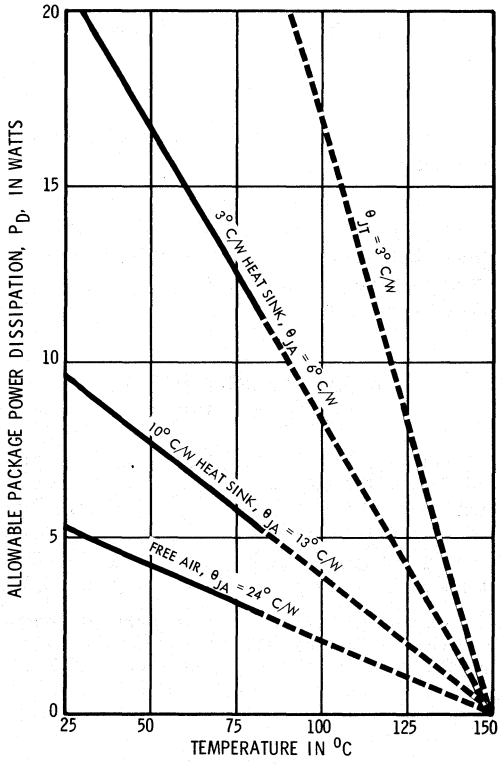
Supply Voltage, V_{CC}	50 V
Peak Output Current, I_{OUT}	±5 A
Input Voltage Range, V_{IN}	−0.3 V to +7.0 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

NOTE: Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current and a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



TRUTH TABLE

V_{IN}	V_{THS}	V_{SENSE}	Source Driver	Sink Driver	Hysteresis
High	NA	NA	Off	Off	NA
Low	<0.4 V	NA	Off	On	NA
Low	0.6 V to 4.0 V	$<V_{THS}/10$	On	On	Set by R_{TH}
Low	0.6 V to 4.0 V	$>V_{THS}/10$	Off	On	—
Low	>4.5 V	<0.4 V	On	On	5% to 10%
Low	>4.5 V	>0.4 V	Off	On	—

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_{CC} = 50\ V$, $V_{SENSE} = 0\ V$ (unless otherwise noted)

Chatacteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating	20	—	50	V
Output Drivers						
Output Leakage Current	I_{CEX}	$V_{IN} = 2.4\ V$, $V_{SOURCE} = 0\ V$	—	<-1.0	-100	µA
		$V_{IN} = 2.4\ V$, $V_{SINK} = 50\ V$	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Source Drivers, $I_{LOAD} = 4.0\ A$	—	2.3	2.5	V
		Source Drivers, $I_{LOAD} = 1.0\ A$	—	1.7	1.8	V
		Sink Drivers, $I_{LOAD} = 4.0\ A$	—	2.1	2.3	V
		Sink Drivers, $I_{LOAD} = 4.0\ A$	—	1.0	1.2	V
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = \pm 4.0\ A$, $L = 3.5\ mH$	50	—	—	V
Output Current Regulation	ΔI_{OUT}	$V_{THS} = 0.6\ V$ to $1.0\ V$, $L = 3.5\ mH$	—	—	±25	%
		$V_{THS} = 1.0\ V$ to $2.0\ V$, $L = 3.5\ mH$	—	—	±10	%
		$V_{THS} = 2.0\ V$ to $4.0\ V$, $L = 3.5\ mH$	—	—	±5.0	%
Clamp Diode Forward Voltage	V_F	$I_F = 4.0\ A$	—	1.8	2.0	V
Output Rise Time	t_r	$I_{LOAD} = 4.0\ A$, 10% to 90%, Resistive Load	—	0.5	1.0	µs
Output Fall Time	t_f	$I_{LOAD} = 4.0\ A$, 90% to 10%, Resistive Load	—	0.5	1.0	µs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 2.4\ V$	—	1.0	10	µA
	$I_{IN(0)}$	$V_{IN} = 0.8\ V$	—	-20	-100	µA
	$I_{THS(OFF)}$	$V_{THS} \leq 400\ mV$	—	-60	—	µA
	$I_{THS(ON)}$	$V_{THS} \geq 500\ mV$, $V_{SENSE} \leq V_{THS}/10.5$	—	-2.0	—	µA
	$I_{THS(HYS)}$	$V_{SENSE} \geq V_{THS}/9.5$, $V_{THS} = 0.6\ V$ to $4.5\ V$	140	200	260	µA
Output Disable Voltage	$V_{THS(OFF)}$		—	—	400	mV
V_{THS}/V_{SENSE} Ratio	—	$V_{THS} = 2.0\ V$ to $4.0\ V$	9.5	10	10.5	—
Default Sense Trip Voltage	V_{SENSE}	$V_{THS} = 4.5\ V$	380	400	420	mV
Default Hysteresis	H	$V_{THS} = 4.5\ V$	5.0	—	10	%
Supply Current (Total Device)	I_{CC}	$V_{IN} = 2.4\ V$, Outputs OFF	—	20	25	mA
		$V_{IN} = 0.8\ V$, Outputs Open	—	47	50	mA
Propagation Delay Time (Resistive Load)	t_{pd}	50% V_{IN} to 50% V_{OUT}, Turn OFF	—	—	2.5	µs
		50% V_{IN} to 50% V_{OUT}, Turn ON	—	—	3.0	µs
		100% V_{SENSE} to 50% V_{OUT}*	—	—	2.0	µs
Thermal Shutdown	T_J		—	175	—	°C

*Where $V_{SENSE} \geq V_{THS}/9.5$

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

NOTE: Each of the drivers within the UDN-2965W includes an internal logic delay to prevent potentially destructive crossover currents within the driver during phase changes. However, never simultaneously enable both inputs in the full-bridge configuration: A destructive short-circuit to ground will result.

APPLICATIONS

The UDN-2965W driver is intended for use as a free-running, pulse-width modulated, motor or solenoid driver.

The source and sink drivers are both turned ON by a low level at the input. When the load current reaches the trip point (set by external resistors or internal default), the comparator output goes high and the source driver is turned OFF. The internal flyback diode then allows current to flow without further input from the power supply. An internal constant current sink reduces the trip point (hysteresis) until the decaying current reaches the lower threshold, when the comparator output goes low and the source driver is again turned ON. Hysteresis percentage is a function of the external resistance R_H and is independent of the peak output load current set by R_T. The chopping frequency is asynchronous and a function of the system and circuit parameters, including load inductance, supply voltage, hysteresis setting, and switching speed of the driver.

Maximum load current and hysteresis percentage are determined by the user:

$$R_H = 50\, V_{REF}\, H$$

$$R_T = \frac{R_H(10\, I_{MAX}\, R_S)}{V_{REF} - (10\, I_{MAX}\, R_S)}$$

where $10\, I_{MAX}\, R_S = V_{THS} = 0.6$ to 4.0 V

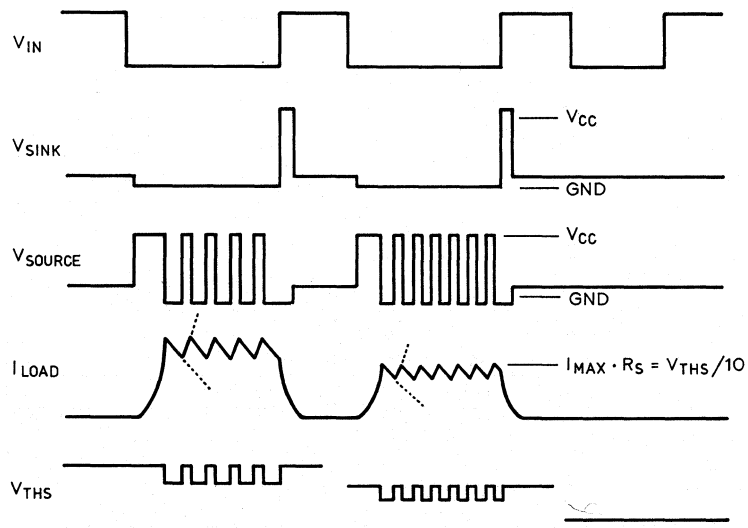
and H = desired hysteresis in percent.

Graphical solutions for R_H and R_T, with V_{REF} = 5 V and $R_S = 0.1\ \Omega$, follow.

Pulling V_{THS} down to less than 0.4 V disables the source driver, turning the load OFF. With V_{THS} greater than 4.5 V, the hysteresis is fixed at (defaults to) between 5% and 10% and the peak load current is fixed at:

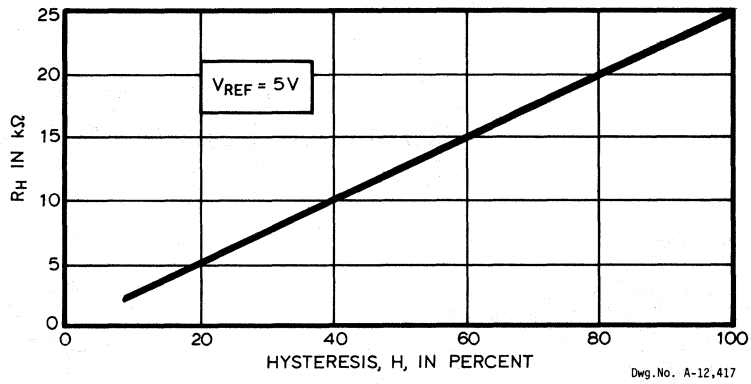
$$I_{MAX} = 0.4/R_S$$

TYPICAL WAVESHAPES



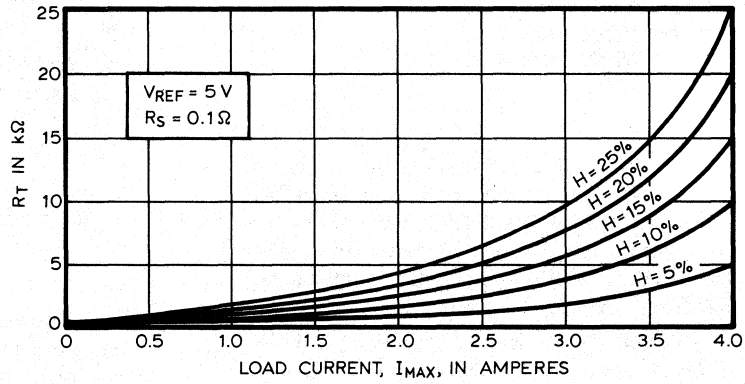
Dwg.No. A-12,415

RESISTOR R_H VALUE AS A FUNCTION OF HYSTERESIS



Dwg.No. A-12,417

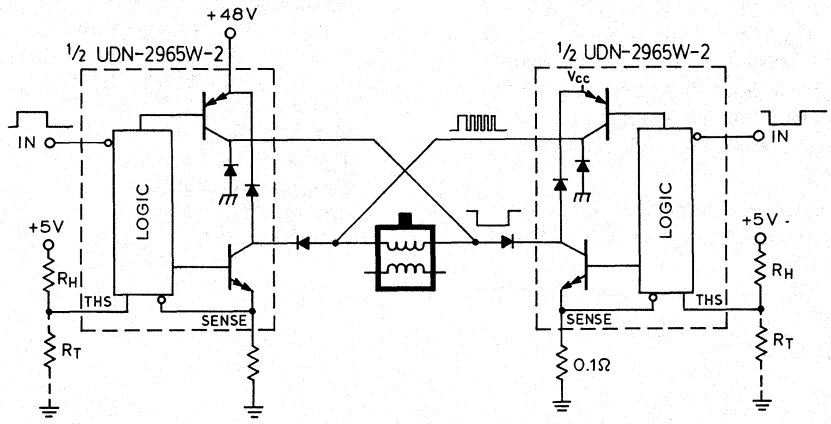
PEAK LOAD CURRENT AS A FUNCTION OF RESISTOR R_T VALUE



Dwg.No. A-12,416

4

BIPOLAR, PULSE-WIDTH MODULATED, STEPPER-MOTOR DRIVE



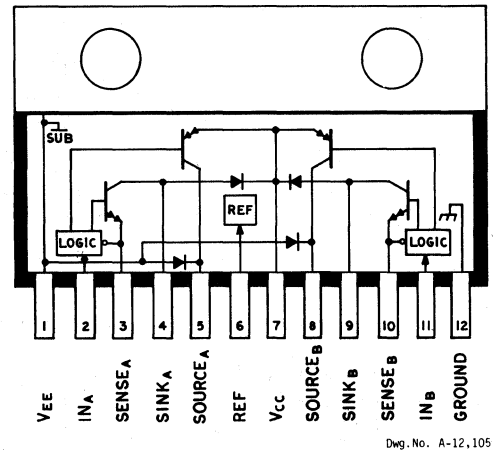
R_H AND R_T DETERMINE HYSTERESIS AND PEAK CURRENT

Dwg. No. B-1538

UDN-2975W AND UDN-2976W
DUAL 4A SOLENOID DRIVERS

FEATURES

- 5 A Peak Output
- TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Output Voltage to 60 V
- Single-Ended or Split Supply
- Adjustable Short-Circuit Protection
- Internal Clamp Diodes
- Plastic SIP With Heat-Sink Tab



Dwg. No. A-12,105

CURRENT CONTROL for operation of a pair of print solenoids is provided by both Type UDN-2975W and UDN-2976W. Each IC's dual driver sections operate directly from the printer control line. The two devices differ only in output-voltage ratings. They can be used at currents of up to 4 A.

Type UDN-2975W is rated at 50 V. Type UDN-2976W is rated at 60 V or ±30 V. Inputs are compatible with most TTL, DTL, LSTTL, and 5 V to 15 V CMOS and PMOS logic.

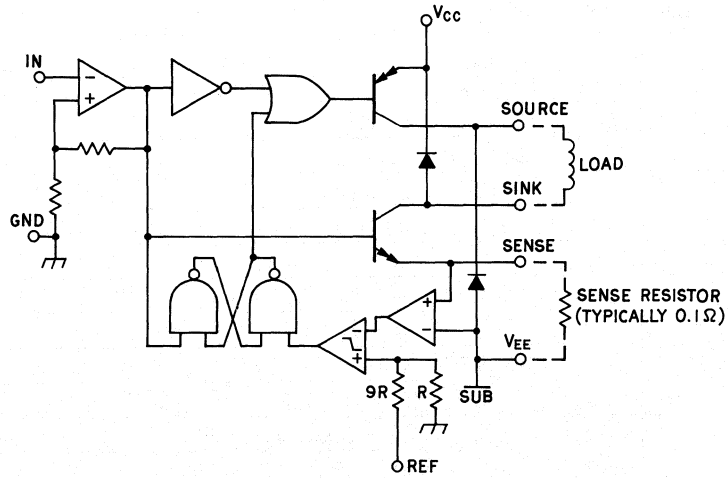
Current is controlled by a current-sensing latch method that uses only one external sensing resistor for each driver. The load current is compared with the reference voltage and, at the level fixed by the system designer ($V_{REF}/10 = I_{LOAD} \times R_{SENSE}$), a latch is set, shutting OFF one of the output transistors. The internal flyback diode then maintains the flux without further input from the power supply, resulting in maximum efficiency. The latch is reset by pulling the input high.

For the maximum in power-handling capability, the integrated circuits are supplied in 12-pin single in-line power tab packages. For proper operation, an external heat sink is required. The tab is at V_{EE} potential and must be insulated from ground when Type UDN-2976W is used with a split supply.

ABSOLUTE MAXIMUM RATINGS
at T_{TAB} = +70°C

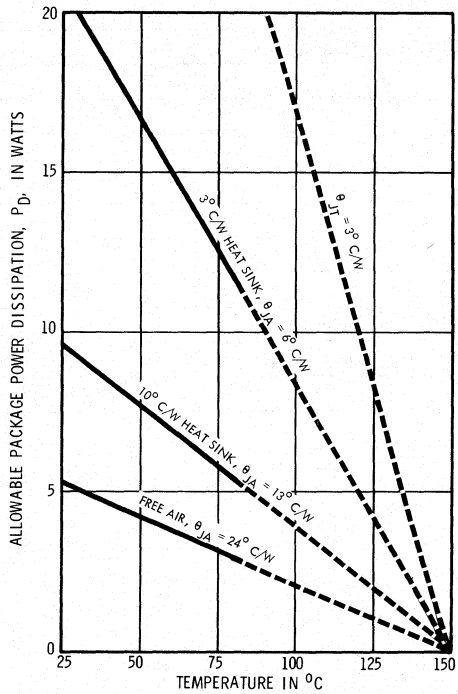
Supply Voltage, V_{CC} (Ref. V_{EE}, UDN-2975W)	50 V
(Ref. V_{EE}, UDN-2976W)	60 V
V_{EE} (Ref. GND, UDN-2975W)	0 V
(Ref. GND, UDN-2976W)	−30 V
Peak Output Current, I_{OUU}	5 A
Input Voltage, V_{IN}	15 V
Reference Voltage, V_{REF}	5 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. A-12,106A

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,794A

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the substrate (pin 1) must be connected to the most negative point in the external circuit.

TRUTH TABLE

V_{IN}	V_{SENSE}	Source Driver	Sink Driver	Function
High	NA	Off	Off	Off
Low	$<V_{REF}/10$	On	On	On
Low	$>V_{REF}/10$	Off	On	Flyback

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_{TAB} \leq$ +70°C, V_{CC} = 45 V (UDN-2975W) or 55 V (UDN-2976W), $V_{EE} = V_{SENSE}$ = 0 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Supply Voltage Range	V_{CC}	UDN-2975W	Operating	20	50	V
		UDN-2976W	Operating	20	60	V
Supply Current	I_{CC}	Both	Outputs Open	—	25	mA
	I_{EE}	Both	Outputs Open	—	−20	mA
Output Drivers						
Output Leakage Current	I_{CEX}	UDN-2975W	V_{IN} = 2.4 V, V_{CC} = 50 V, V_{SOURCE} = 0 V	—	100	µA
			V_{IN} = 2.4 V, $V_{SINK} = V_{CC}$ = 50 V	—	100	µA
		UDN-2976W	V_{IN} = 2.4 V, V_{CC} = 60 V, V_{SOURCE} = 0 V	—	100	µA
			V_{IN} = 2.4 V, $V_{SINK} = V_{CC}$ = 60 V	—	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	Source Drivers, I_{LOAD} = 4 A	—	3.5	V
			Sink Drivers, I_{LOAD} = 4 A	—	2.5	V
Output Sustaining Voltage (Source drivers only)	$V_{CE(SUS)}$	UDN-2975W	I_{LOAD} = 4 A, L = 3.5 mH	50	—	V
		UDN-2976W	I_{LOAD} = 4 A, L = 3.5 mH	60	—	V
Clamp Diode Forward Voltage	V_F	Both	I_F = 4 A	—	2.0	V
Output Rise Time	t_r	Both	I_{LOAD} = 4 A, 10% to 90%, Resistive Load	—	2.0	µs
Output Fall Time	t_f	Both	I_{LOAD} = 4 A, 90% to 10%, Resistive Load	—	2.0	µs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	Both		2.0	—	V
	$V_{IN(0)}$	Both	See Notes	—	0.5	V
Logic Input Current	$I_{IN(1)}$	Both	V_{IN} = 2.4 V	—	20	µA
	$I_{IN(0)}$	Both	V_{IN} = 0.4 V	—	−20	µA
	$I_{REF(1)}$	Both	V_{REF} = 5.0 V	—	−20	µA
Reference/Sense Ratio	—	Both	V_{REF} = 2.0 to 5.0 V	9.5	10.5	—
Propagation Delay Time	t_{pd}	Both	50% V_{in} to 50% V_{out}, Resistive Load	—	3.0	µs
			100% V_{sense} to 50% V_{out}*, Resistive Load	—	3.0	µs
Minimum Reset Pulse Width	t_{in}	Both		—	1.0	µs

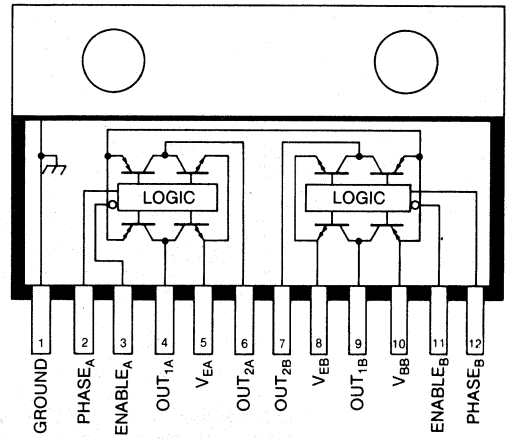
*Where $V_{sense} = V_{REF}/10.5$

NOTES: Negative current is defined as coming out of (sourcing) the specific device pin.
For improved noise immunity, hysteresis insures $V_{IN(0)}$ of 0.8 V max. after V_{IN} is 0.5 V or less.

UDN-2998W
DUAL FULL-BRIDGE MOTOR DRIVER

FEATURES

- ±3A Peak Output Current
- Output Voltage to 50V
- Integral Output Suppression Diodes
- Output Current Sensing
- TTL/CMOS Compatible Inputs
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protected



Dwg. No. W-10

As an interface between low-level logic and solenoids, brushless dc motors, or stepper motors, the UDN-2998W dual full-bridge driver will operate inductive loads up to 50V with continuous output currents of up to 2A per bridge or peak (start-up) currents to 3A. The control inputs are compatible with TTL, DTL, and 5V CMOS logic. Except for a common supply voltage and thermal shutdown, the two drivers in each package are completely independent.

For external PWM control, an OUTPUT ENABLE for each bridge circuit is provided and the sink driver emitters are pinned out for connection to external current-sensing resistors. The chopper drive mode is characterized by low power dissipation levels and maximum efficiency. A PHASE input to each bridge determines load-current direction.

Extensive circuit protection is provided on-chip. Both ground-clamp and flyback diodes for each bridge are provided. A thermal shutdown circuit disables the load drive if chip temperature rating (package power dissipation) is exceeded. Internally-generated delays provide crossover-current protection.

The UDN-2998W is packaged in a 12-pin single in-line power tab package for high power capabilities. Driving either of the bridges at the full 2A dc rating requires the use of an external heat-sink. The tab is a ground potential and needs no insulation.

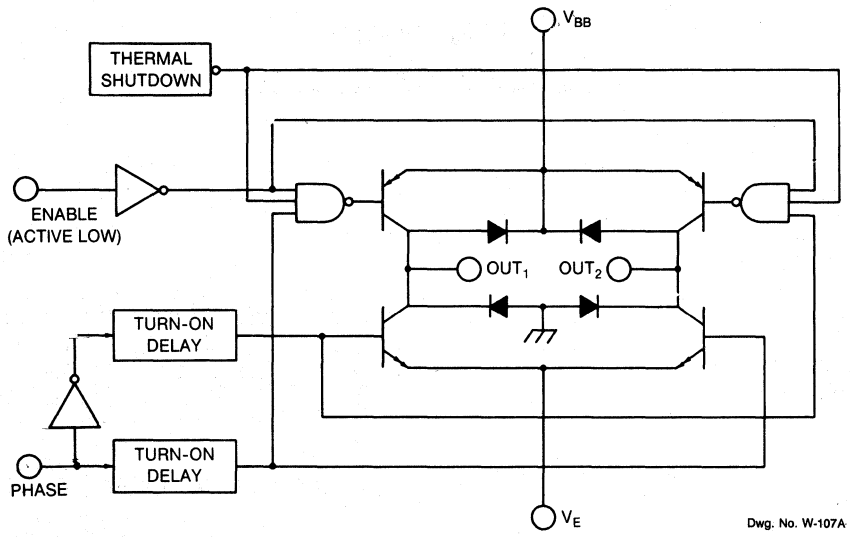
A similar dual full-bridge driver for use with continuous load currents to ±500mA is the UDN-2993B.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

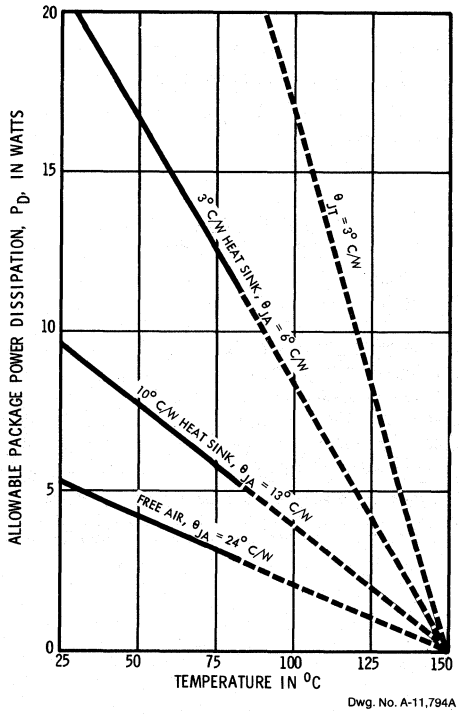
Supply Voltage, V_{BB} 50V
Output Current, I_{OUT} (DC) ..... ±2A
(Peak) ..... ±3A
Sink Driver Emitter Voltage, V_E 1.5V
Logic Input Voltage Range,
V_{PHASE} or V_{ENABLE} ..... −0.3V to 15V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

NOTE: Output current rating may be limited by chopping frequency, ambient temperature, air flow, or heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.

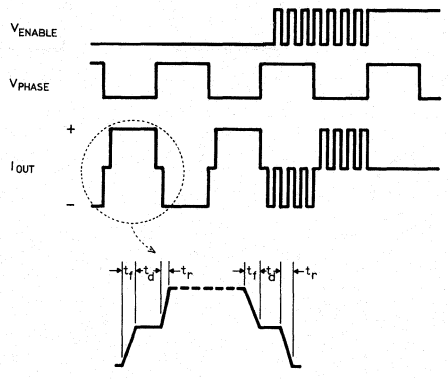
TRUTH TABLE

Enable Input	Phase Input	Output 1	Output 2
Low	High	High	Low
Low	Low	Low	High
High	High	Open	Low
High	Low	Low	Open

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_{BB} = 50\,V$

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	50	V
Output Leakage Current	I_{CEX}	$V_{OUT} = 50\,V$, $V_{ENABLE} = 2.0\,V$, Note 2	—	<5.0	50	µA
		$V_{OUT} = 0$, $V_{ENABLE} = 2.0\,V$, Note 2	—	<-5.0	−50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 1\,A$, Sink Driver	—	1.2	1.4	V
		$I_{OUT} = 2\,A$, Sink Driver	—	1.7	1.9	V
		$I_{OUT} = -1\,A$, Source Driver	—	1.7	1.9	V
		$I_{OUT} = -2\,A$, Source Driver	—	2.0	2.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = \pm 2\,A$, $L = 3.5\,mH$, Note 2	50	—	—	V
Source Driver Rise Time	t_r	$I_{OUT} = -2\,A$	—	500	—	ns
Source Driver Fall Time	t_f	$I_{OUT} = -2\,A$	—	750	—	ns
Deadtime	t_d	$I_{OUT} = \pm 2\,A$	—	2.5	—	µs
Clamp Diode Leakage Current	I_R	$V_R = 50\,V$	—	<5.0	50	µA
Clamp Diode Forward Voltage	V_F	$I_F = 2\,A$	—	1.5	2.0	V
Supply Current	I_{BB}	$V_{ENABLE(1)} = V_{ENABLE(2)} = 0.8\,V$	—	25	30	mA
		$V_{ENABLE(1)} = V_{ENABLE(2)} = 2.0\,V$	—	20	25	mA
Control Logic (PHASE or ENABLE)						
Logic Input Voltage	$V_{IN(0)}$		0.8	—	—	V
	$V_{IN(1)}$		—	—	2.0	V
Logic Input Current	$I_{IN(0)}$	V_{PHASE} or $V_{ENABLE} = 0.8\,V$	—	−5.0	−25	µA
	$I_{IN(1)}$	V_{PHASE} or $V_{ENABLE} = 2.0\,V$	—	<1.0	10	µA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	0.4	1.0	µs
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	2.0	4.0	µs

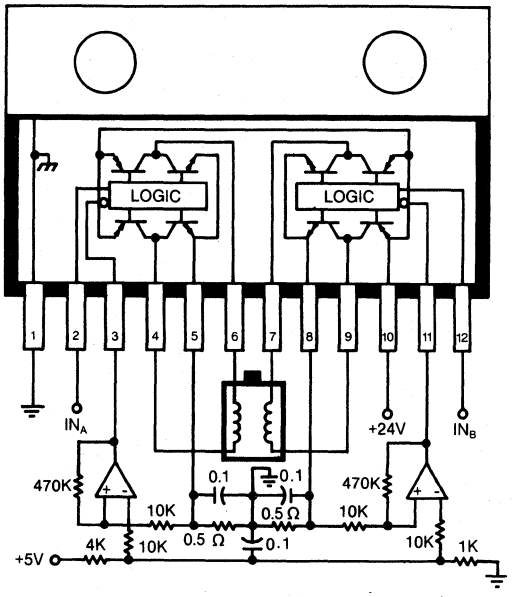
NOTES:
1. Each driver is tested separately.
2. Test is performed with $V_{PHASE} = 0.8\,V$ and then repeated for $V_{PHASE} = 2.0\,V$.
3. Negative current is defined as coming out of (sourcing) the specified device pin.



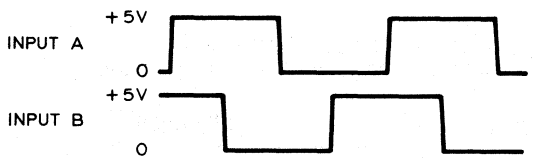
Dwg. No. A-14,272

TYPICAL APPLICATION

2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)



Dwg. No. W-108



Dwg. No. A-12,454

ULN-3751Z
POWER OPERATIONAL AMPLIFIER

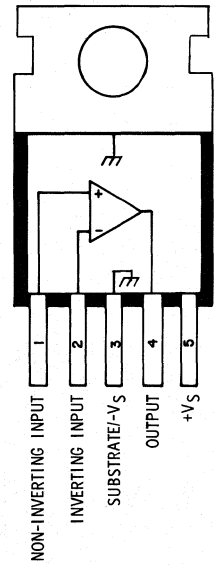
FEATURES

- ±3 V to ±13 V Operation
- High Output Swing
- Peak Output Current to ±3.5 A
- Low Input Offset
- 90 dB Typical Open-Loop Gain
- Internal Thermal Shutdown
- High Common-Mode Input Range
- Unity Gain Stable
- Pin Compatible with L165, L465, SG1173

As a combination general-purpose operational amplifier and power booster, the ULN-3751Z integrated circuit simplifies circuit design, reduces component count, and enhances system reliability.

The power op amp features high-impedance differential inputs, a unity-gain stable amplifier that needs no external compensation, and a high-current power output. Typical applications include use as a voice-coil motor driver, linear servo amplifier, power oscillator, bipolar voltage regulator, and audio power driver.

The ULN-3751Z is for applications demanding up to ±3.5 A of output current. It is furnished in a modified 5-lead JEDEC-style TO-220 plastic package. Lead forming for vertical or horizontal mounting is available (ULN-3751ZV or ULN-3715ZH). The heat sink tab is at substrate potential and must be insulated from ground when the device is used with a split supply.



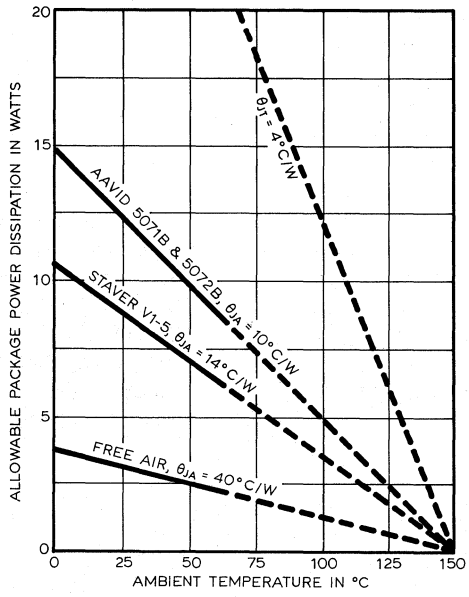
Dwg. No. A-12,364

This power op amp operates over a recommended supply voltage range of ±3 V to ±13 V. Dual power op amps are available as the ULN-3755B (16-pin DIP) and the high-power ULN-3755W (12-pin SIP). Both of those devices include output current sensing and a voltage boost connection to maximum output voltage swing to ±20 V supplies at up to ±3.5 A peak output current.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Supply Voltage Differential ($+V_S$ to $-V_S$) . . . . . 28 V
Peak Output Current, I_{OUT} . . . . . ± 3.5 A
Input Voltage Range, V_{IN} . . . . . $+V_S$ to $-V_S$ -0.3 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . 0°C to $+70°C$
Storage Temperature Range, T_S . . . . . $-40°C$ to $+150°C$

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-14,249

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_S = \pm 6.0$ V (unless otherwise noted)

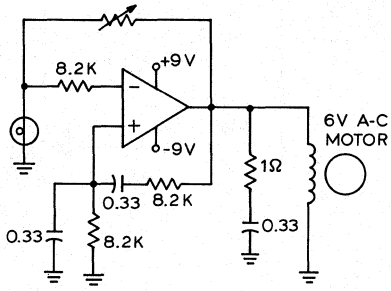
Characteristic	Test Conditions	Limits			
		Min.	Typ.	Max.	Unit
Functional Supply Voltage Range	$+V_S$ to $-V_S$	6.0	—	26	V
Quiescent Supply Current		—	40	60	mA
Input Bias Current	$V_{IN} = 0$, $I_{OUT} = 0$	—	−60	−1000	nA
Input Offset Voltage	$V_{IN} = 0$, $I_{OUT} = 0$	—	±2.0	±10	mV
Input Offset Current	$V_{IN} = 0$, $I_{OUT} = 0$	—	10	100	nA
Input Noise Voltage†	BW = 40 Hz to 15 kHz	—	4.0	—	μV
Input Noise Current†	BW = 40 Hz to 15 kHz	—	60	—	pA
Crossover Distortion†	$P_{OUT} = 50$ mW, $R_L = 4\ \Omega$	—	<0.05	—	%
Common Mode Rejection	$\Delta V_{CM} = 2$ V	60	85	—	dB
Input Common Mode Range†	Positive	—	$+V_S - 2$ V	—	V
	Negative	—	$-V_S - 0.3$ V	—	V
Open-Loop Voltage Gain	f = 0	80	90	—	dB
Slew Rate	$V_{IN} = V_{OUT} = 6$ Vpp, $R_L = \infty$	1.0	2.3	—	V/μs
Gain-Bandwidth Product†	$A_V = 40$ dB	—	3.5	—	MHz
Output Voltage Swing	$I_{out} = 1.0$ A	4.5	4.7	—	V
	$I_{OUT} = -1$ A	−4.5	−4.7	—	V
Supply Voltage Rejection	$+V_S$, $\Delta V = 1$ V	60	85	—	dB
	$-V_S$, $\Delta V = 1$ V	60	80	—	dB
Thermal Shutdown Temp.†		—	160	—	°C

*This parameter is tested to a lot sample plan only.
†Typical values given for circuit design information only.

4

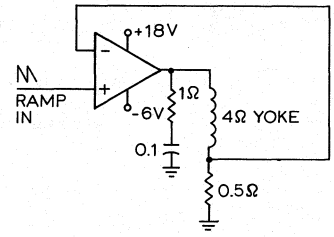
TYPICAL APPLICATIONS

WIEN BRIDGE OSCILLATOR/MOTOR DRIVER



Dwg. No. A-12,376B

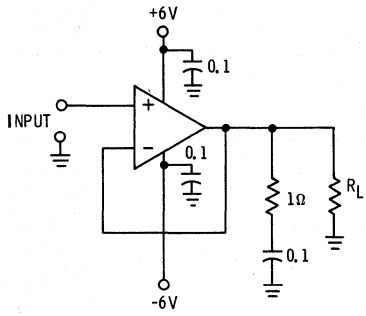
VIDEO MONTOR VERTICAL DEFLECTION MAP



Dwg. No. A-12,375A

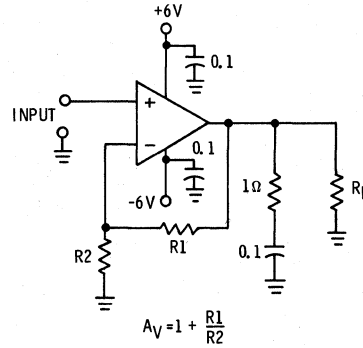
TYPICAL APPLICATIONS

UNITY GAIN VOLTAGE FOLLOWER



Dwg. No. A-12,551

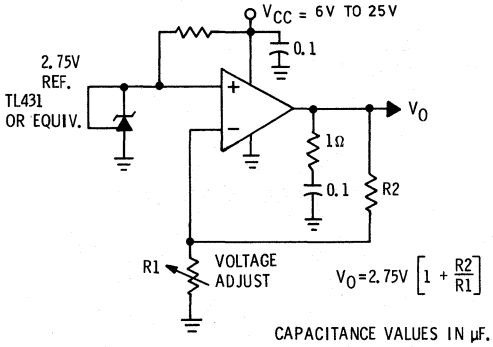
NON-INVERTING POWER AMPLIFIER



CAPACITANCE VALUES IN µF.

Dwg. No. A-12,552

LINEAR VOLTAGE REGULATOR

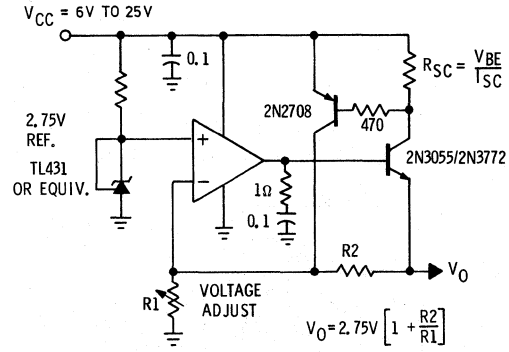


CAPACITANCE VALUES IN µF.

Dwg. No. A-12,553A

HIGH-POWER LINEAR REGULATOR

(Short-Circuit Protected)

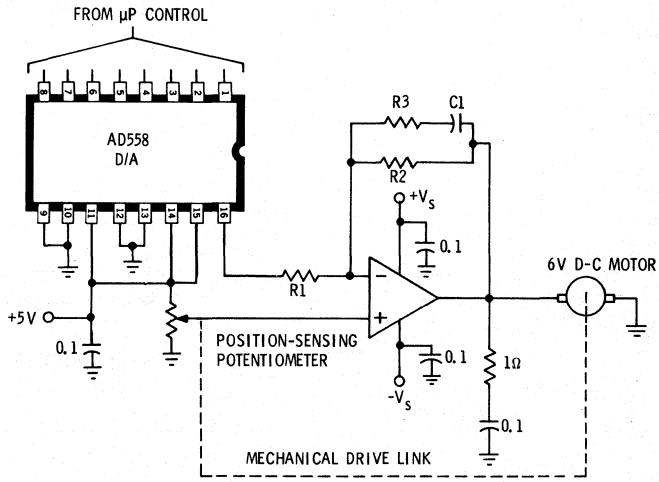


CAPACITANCE VALUES IN µF.

Dwg. No. A-12,554B

TYPICAL APPLICATIONS

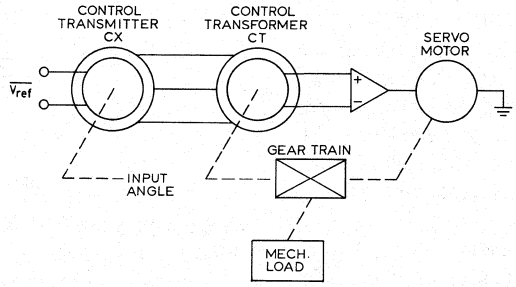
SINGLE-ENDED POSITION SERVO WITH SENSE POTENTIOMETER



R1, R2 DEFINE D-C GAIN.
R3, C1 PICKED TO PROVIDE LOOP COMPENSATION.
CAPACITANCE VALUES IN µF.

Dwg. No. A-12,556

SIMPLIFIED SERVO APPLICATION WITH CONTROL TRANSFORMERS



Dwg. No. A-14,250

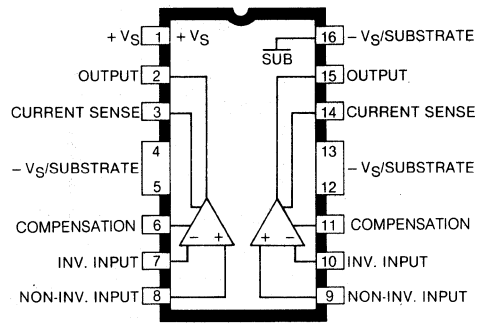
ULN-3753B AND ULN-3753W
DUAL POWER OPERATIONAL AMPLIFIERS

FEATURES

- Operating Supply Range ±3 V to ±20 V
- Output Current to ±3.5 A Peak
- Output-Current Limiting
- Output-Current Sensing
- High Output-Voltage Swing
- Low Crossover Distortion
- Low Input Offset Voltage
- Externally Compensated
- High Open-Loop Gain
- Output Protection Diodes
- Thermal Shutdown Protection
- Excellent Supply and Common-Mode Rejection
- Single or Dual In-Line Power Packages

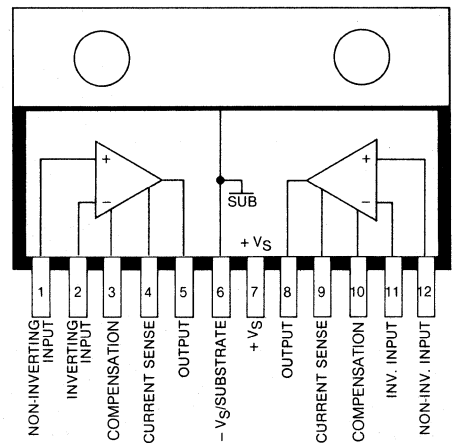
APPLICATIONS

- Dual Half-Bridge and Full-Bridge Motor Drivers
  - Linear Servo Motors
  - Voice Coil Motors
  - AC and DC Motors
  - Microstepping Applications
- Power Transconducting Amplifier
- Audio Power Amplifier, Stereo or BTL
- Power Oscillator/Amplifier
- Dual Bipolar Voltage Regulator



Dwg. No. A-13, 636

ULN-3753B



Dwg. No. A-13, 632

ULN-3753W

High-current linear servo loads, such as voice coil motors used in disc-drive applications, are ideal applications for the ULN-3753B and ULN-3753W dual high-power operational amplifiers. Their building block design concept also makes them ideal for a wide variety of other motor drive applications, audio power amplifiers, power oscillators, and linear voltage regulators. External compensation permits user adjustment of bandwidth and phase margin at any gain level.

The ULN-3753B is furnished in a 16-pin dual in-line package with copper heat-sink contact tabs. For higher power requirements, the ULN-3753W is supplied in a 12-pin single in-line power tab package.

The inputs are designed to allow a wide common mode range from the negative supply, (or ground in single supply applications) to within approximately 2 V of the positive supply. Common-mode and power supply rejection are in excess of 60 dB. The amplifiers' wide output swing is complemented by current sensing, which is referenced to the negative supply and allows for feedback as required to produce a transconductance characteristic.

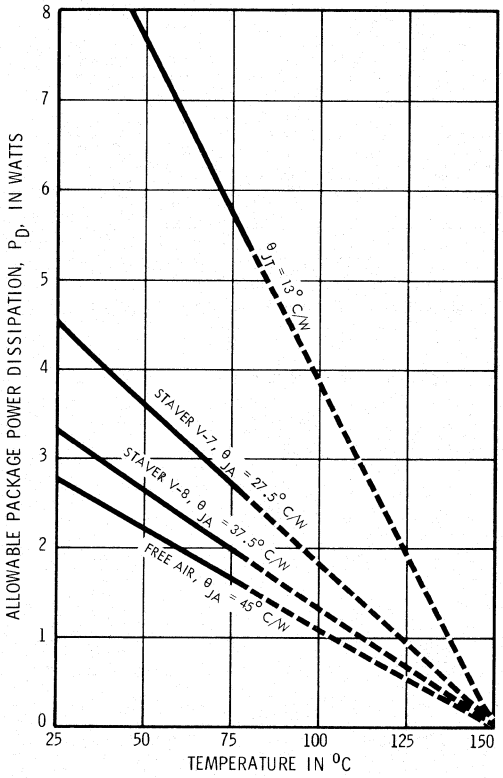
The ULN-3753B (batwing DIP) can typically dissipate 6 W at a tab temperature of 70°C. The lead configuration enables easy attachment of a heat sink while fitting a standard socket or printed wiring board layout. The ULN-3753W (SIP) can safely dissipate significantly higher power levels with appropriate heat sinking. With either package configuration, the heat sink is at the negative supply, or at ground in a single-ended application.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Differential ($+V_S$ to $-V_S$)	40 V
Peak Supply Voltage (50 ms)	45 V
Continuous Output Current, I_{OUT} ($V_S = \pm 15$ V)	± 2.0 A
($V_S = \pm 6$ V)	± 2.5 A
Peak Output Current, I_{OUT} (50 ms)	± 3.5 A
Package Power Dissipation, P_D	See Graphs
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

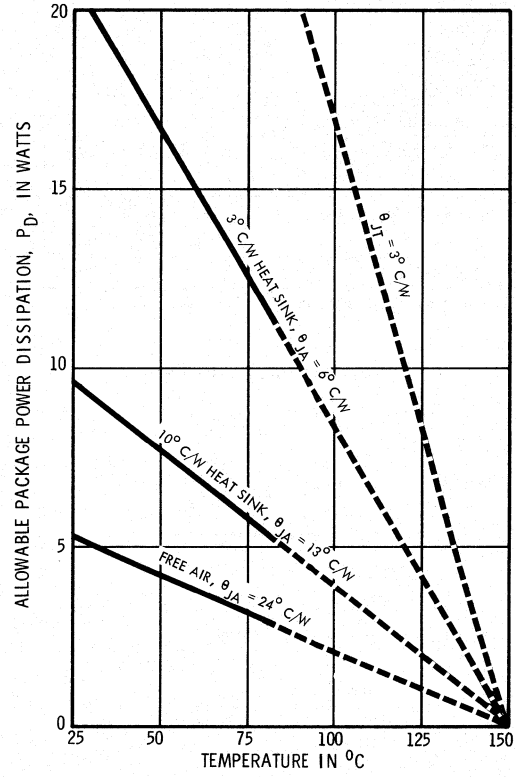
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

ULN-3753B



Dwg. No. A-11, 793B

ULN-3753W



Dwg. No. A-11, 794A

4

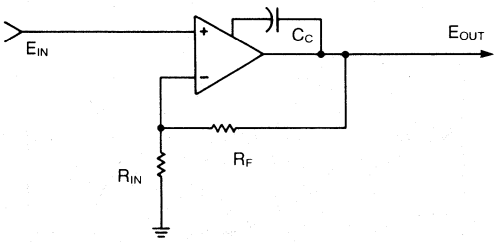
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_S = \pm 6V$, $C_C = 0$, each amplifier tested separately (unless otherwise specified)

Characteristic	Test Conditions	Limits			Units
		Min.	Typ.	Max.	
Functional Supply Voltage Range	$+V_S$ to $-V_S$	6.0	—	40	V
Quiescent Supply Current		—	90	150	mA
Input Bias Current	$V_{OUT} = 0$	—	−80	−1000	nA
Input Offset Voltage	$V_{OUT} = 0$, $I_{OUT} = 0$	—	±1.0	+10	mV
Input Offset Volt. TC†	Over Op. Temp. Range	—	−15	—	µV/°C
Input Offset Current	$V_{OUT} = 0$, $I_{OUT} = 0$	—	10	100	nA
Input Noise Voltage†	BW = 40 Hz to 15 kHz	—	4.0	—	µV
Input Noise Current†	BW = 40 Hz to 15 kHz	—	60	—	pA
Crossover Distortion†	$P_{OUT} = 50$ mW, $R_L = 4\Omega$	—	0.2	—	%
Common Mode Rejection	$V_{CM} = 3V$	60	85	—	dB
Input Common Mode Range*	$V_S = +6V$	−6.3	—	+4.0	V
	$V_S = +15V$	−15.3	—	+13	V
Open Loop Voltage Gain	f = 0	80	100	—	dB
Slew Rate	$V_{IN} = V_{OUT} = 6$ Vpp	5.0	10	—	V/µs
Gain-Bandwidth Product†	$A_V = 40$ dB	—	3.0	—	MHz
Channel Separation†	$I_{OUT} = 100$ mA, f = 1 kHz	—	60	—	dB
Output Voltage Swing	$I_{OUT} = 1A$	9.0	9.5	—	Vpp
Supply Voltage Rejection	$+V_S$, $\Delta V = 1V$	60	85	—	dB
	$-V_S$, $\Delta V = 1V$	60	80	—	dB
Thermal Resistance, Θ_{JT}*	ULN-3753B	—	—	15	°C/W
	ULN-3753W	—	—	3.0	°C/W
Thermal Shutdown Temp.†		—	165	—	°C

*This parameter is tested to a lot sample plan only.

†Typical values given for circuit design information only.

NON-INVERTING AMPLIFIER

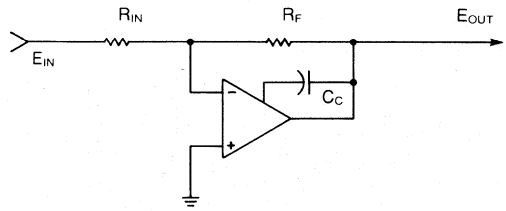


$$\frac{E_{OUT}}{E_{IN}} = 1 + \frac{R_F}{R_{IN}}$$

IF $R_F = 0$ or $R_{IN} = \infty$, $E_{OUT} = E_{IN}$

Dwg. No. W-155

INVERTING AMPLIFIER

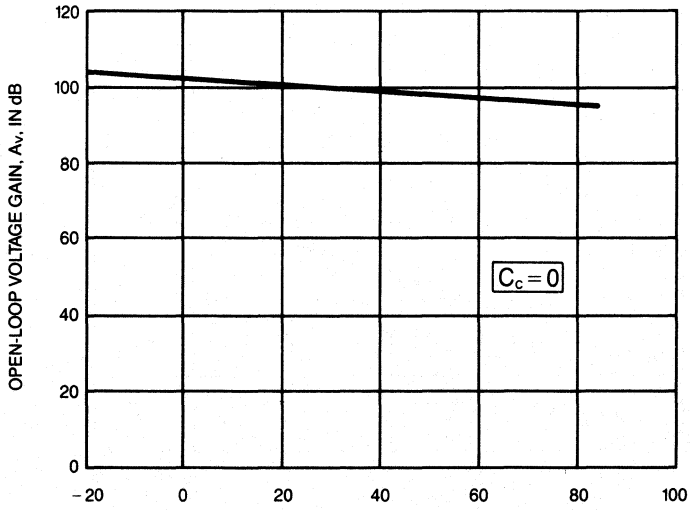


$$\frac{E_{OUT}}{E_{IN}} = -\frac{R_F}{R_{IN}}$$

Dwg. No. W-156

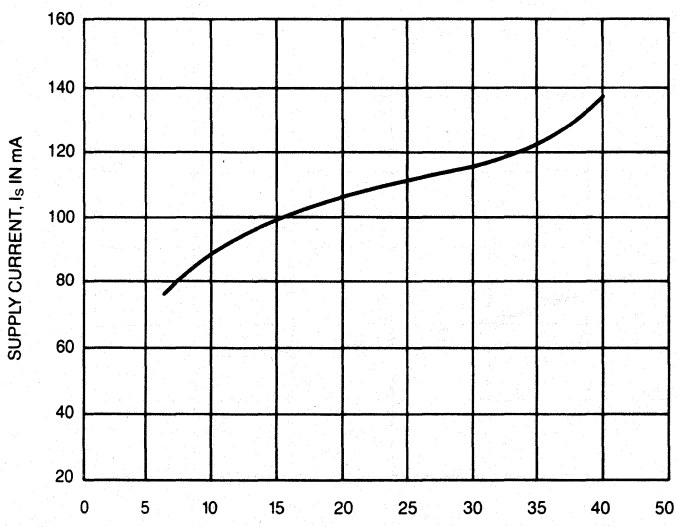
TYPICAL CHARACTERISTICS

OPEN-LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



Dwg. No. W-158

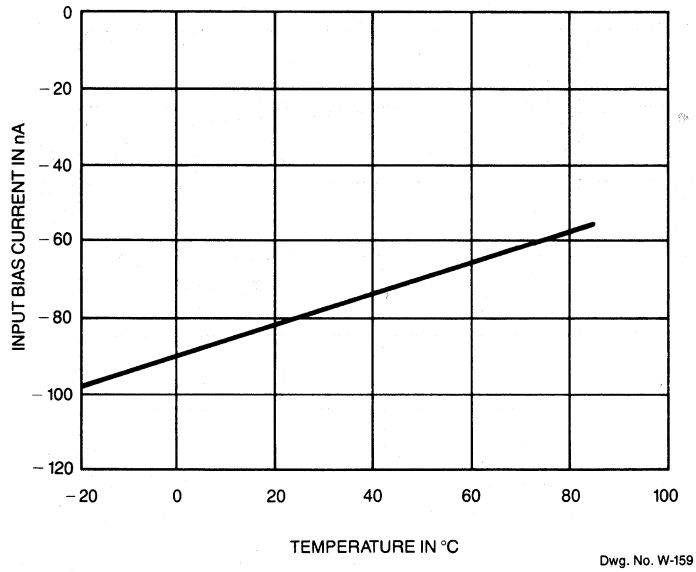
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE DIFFERENTIAL



Dwg. No. W-161

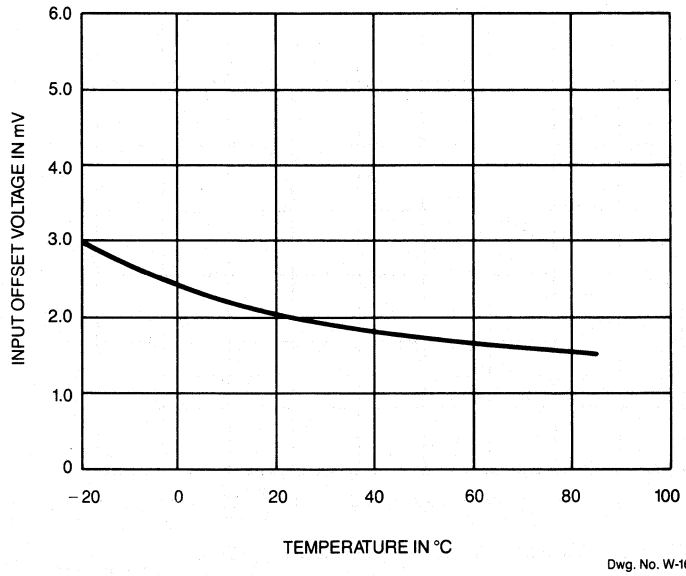
TYPICAL CHARACTERISTICS

**INPUT BIAS CURRENT
AS A FUNCTION OF TEMPERATURE**



Dwg. No. W-159

**INPUT OFFSET VOLTAGE
AS A FUNCTION OF TEMPERATURE**



Dwg. No. W-160

APPLICATIONS

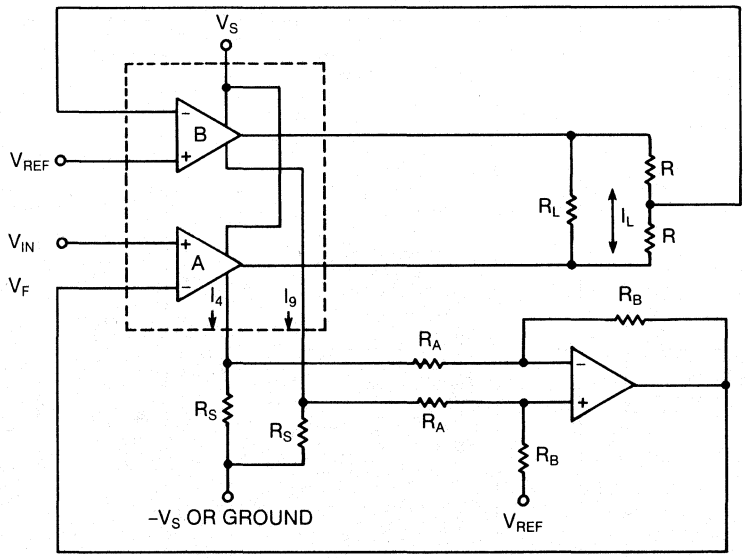


FIGURE 1 Dwg. No. W-162

CURRENT-SENSE TRANSCONDUCTANCE AMPLIFIER

The ULN-3753B/W current-sense terminals can be used to obtain a transconductance function. This characteristic is commonly used in motor control applications such as voice coil servo or micro-stepping positioning systems found in many computer disk drives.

Figure 1 shows a ULN-3753W dual amplifier connected as a transconductance amplifer. In this example, amplifier B is used as a slave to amplifier A. Feedback from the current-sensing resistors (R_S) in the emitters of the output current-sinking transistors, is applied to the summing network and scaled to the inverting input of amplifier A where it is compared to the input voltage. The current-sensing feedback imparts a transconductance characteristic to the amplifier's transfer function. That is, the voltage developed across the sensing resistors is directly proportional to the output current. Using this voltage as a feedback source allows expressing the gain of the circuit as output current in amperes vs. input voltage in volts. The gain assumes the dimensions of a transconductance function, expressed in mhos.

The negative-feedback forces the amplifier to adjust the output current to attain a value such that the feedback voltage equals the applied input voltage. The transfer function of the transconductance amplifier is approximately:

$$I_L/(V_{IN} - V_{REF}) = R_A/R_BR_S$$

In the figure, resistors R_A, R_B, and R_S define the transconductance gain. To avoid limiting the transconductance amplifier's output compliance (swing capability), low-value current-sensing resistors (R_S) should be used.

APPLICATIONS

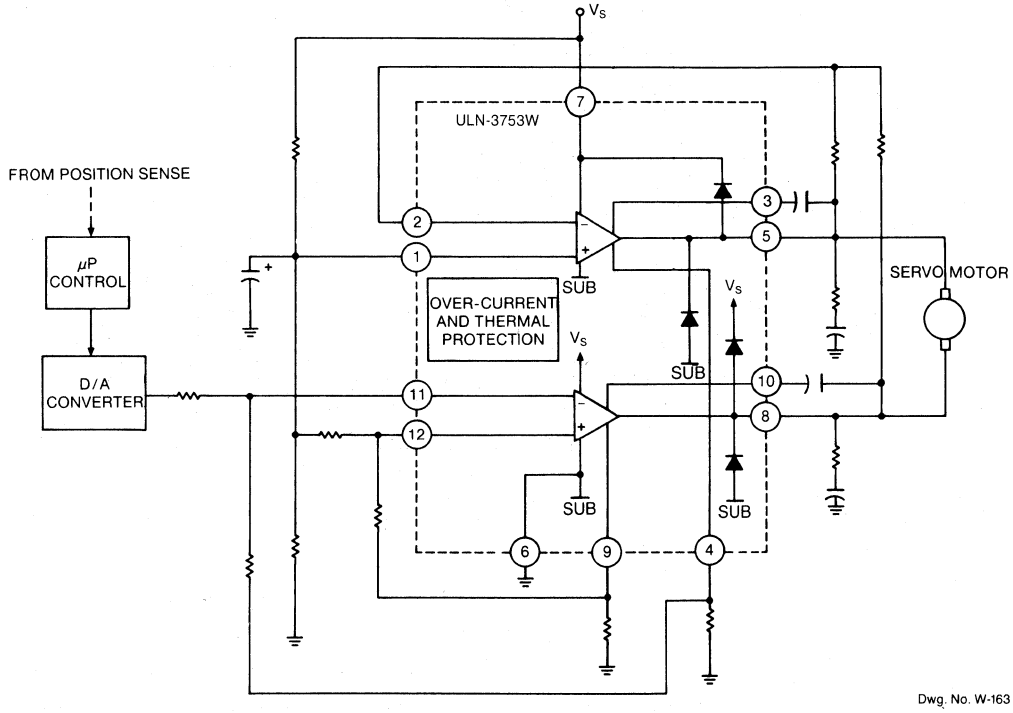


FIGURE 2

DIGITALLY CONTROLLED POSITION SERVO

In a position-control application, a microprocessor is often used to control a servomotor's shaft angle or to control position as in a disk drive application. The circuit requires small-signal input op amps, drivers, and power output stages. The circuit derives its input from the D/A converter whose output is determined by a code from the controlling microprocessor and related digital control circuitry. The sensed position signal normally undergoes processing and comparison with the desired position, through the microprocessor system that produces an error signal to control the servo amplifier's output.

The circuit includes thermal and short-circuit protection, matching and thermal tracking inherent to monolithic construction. The configuration shown in Figure 2 uses a ULN-3753W dual power operational amplifier whose two independent outputs are connected in a push-pull, H-bridge arrangement. The IC's outputs also include clamping diodes with current-handling capacity equal to that of the output drivers.

The current-sense pins (4 and 9) provide access to the emitters of the H-bridge current sinks, thereby providing convenient output current sensing, while allowing separate low-current signal ground returns.

APPLICATIONS

TWO-PHASE 60 Hz AC MOTOR DRIVER

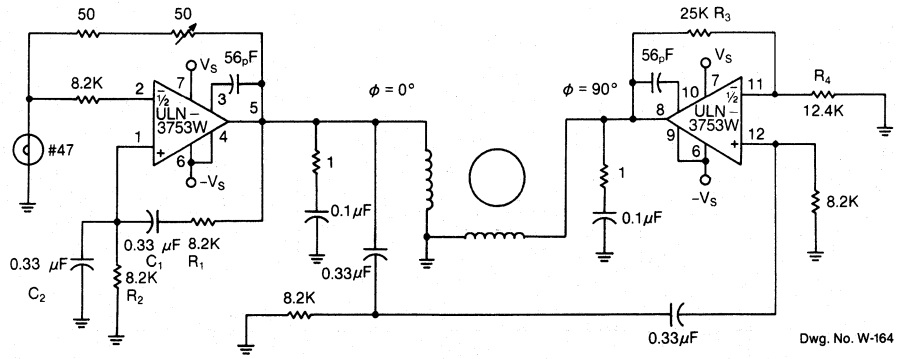


FIGURE 3

THREE-PHASE 400 Hz AC MOTOR DRIVER

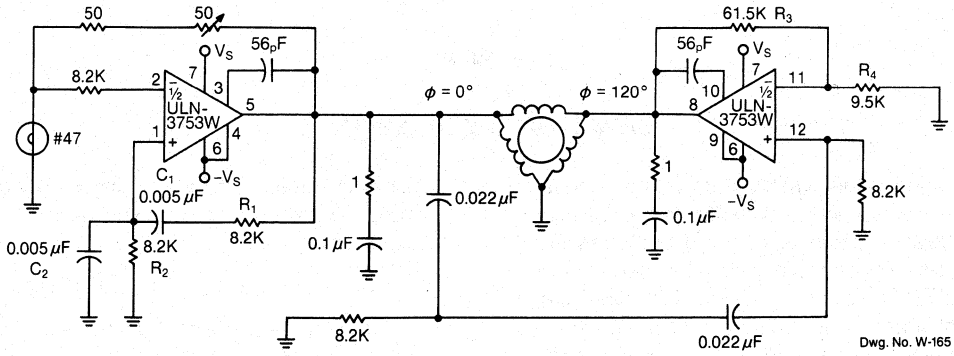


FIGURE 4

N-PHASE MOTOR DRIVE

Because of its high amplification factor and built-in power-output stage, an integrated power operational amplifier makes a convenient driver for ac motors. One op amp can be configured as an oscillator to generate the required ac signal. The power-output stage, of course, supplies the high-current drive to the motor.

As shown in the motor-drive circuits in Figure 3 and 4, the controlling op amp is configured as a Weinbridge oscillator. The R_1C_1, R_2C_2 feedback networks determine the oscillation frequency, according to the following expression:

$$f_o = 1/(2\pi R_1R_2C_1C_2)$$

By varying either R_1 or R_2, the oscillator frequency can be adjusted over a narrow range.

The R_3/R_4 ratio sets the second amplifier's gain to compensate for signal attenuation occurring in the phase shifters.

The circuits can be driven from an external source, such as a pulse or square wave, setting the gain of the left-hand amplifier to a level less than that required for oscillation. The RC feedback networks then function as an active filter causing the outputs to be sinusoidal.

APPLICATIONS

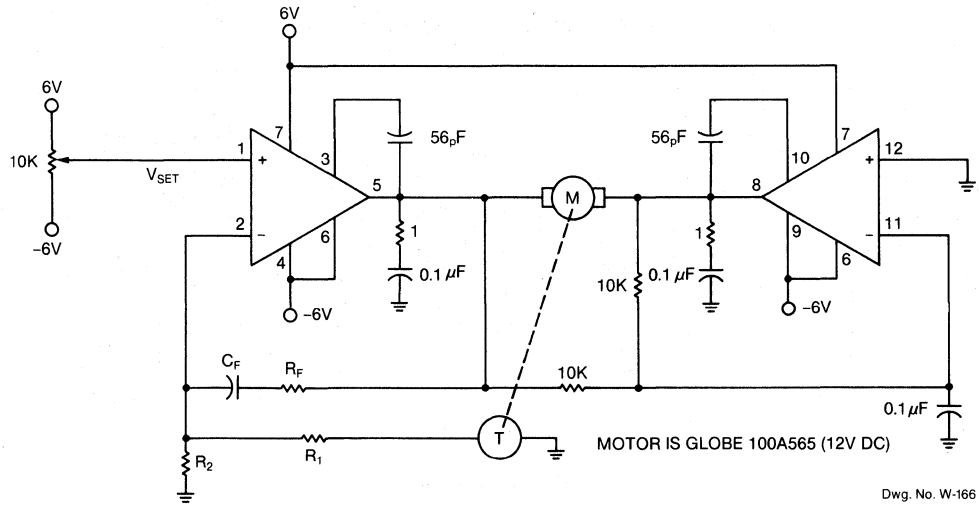


FIGURE 5

DC MOTOR SPEED CONTROL

In addition to the synchronous ac motor drives described above, the ULN-3753B/W can be used to provide accurate speed control of dc motors. Figure 5 shows a closed-loop system for controlling the speed of a 12 V dc motor. The circuit provides bidirectional speed control. The amplifiers' push-pull configuration ensures a full rail-to-rail voltage swing (minus the output stages' saturation drops) across the motor in either direction.

The circuit uses a mechanically-coupled tachometer to provide speed-stabilizing feedback to the first amplifier section. The motor's speed and direction of rotation is set by adjusting the 10 kΩ potentiometer at the amplifier's noninverting input. The motor speed, in rpm, is given by the following expression:

$$S = V_{SET}(R_1 + R_2)/.0027\,R_2$$

The R_FC_F feedback network prevents oscillation by compensating for the inherent dynamic mechanical lag of the motor. The R_FC_F time constant is selected to match the particular motor's response or dynamic time constant. This should yield a good starting point for stabilizing the system with optimum response achieved by varying the compensating capacitor.

ULN-3755B AND ULN-3755W
DUAL POWER OPERATIONAL AMPLIFIERS

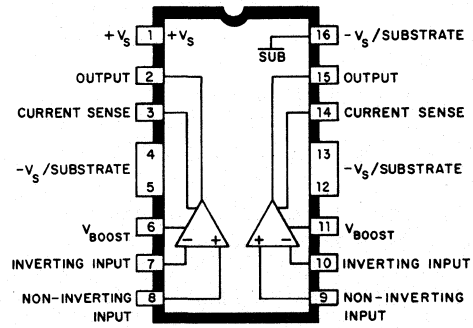
FEATURES

- Operating Supply Range ±3 to ±20 Volts
- Output Current to ±3.5 A Peak
- Output Current Limiting
- Output Current Sensing
- High Output-Voltage Swing
- Low Crossover Distortion
- Low Input Offset Voltage
- Unity-Gain Stable
- High Open-Loop Gain
- Output Protection Diodes
- Thermal Shutdown Protection
- Excellent Supply and Common-Mode Rejection
- Single or Dual In-Line Power Packages

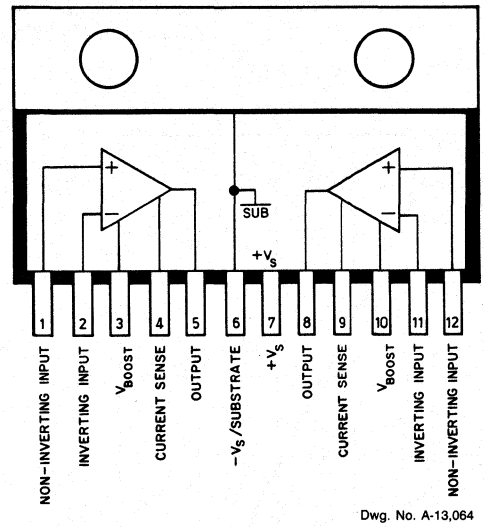
APPLICATIONS

- Dual Half-Bridge and Full-Bridge Motor Drivers
  - Linear Servo Motors
  - Voice Coil Motors
  - AC and DC Motors
  - Microstepping Applications
- Power Transconductance Amplifier
- Audio Power Amplifier
  - Stereo or BTL
- Power Oscillator/Amplifier
- Dual Bipolar Voltage Regulator

Consisting of two high-power operational amplifier circuits in a single in-line power-tab package or a batwing dual in-line package, the ULN-3755B and ULN-3755W are specifically designed to drive high-current linear servo loads such as voice coil motors used in disc-drive applications. Their building block design concept also makes them ideal for a wide variety of other motor drive applications, for use as audio power amplifiers, power oscillators, and linear voltage regulators. Low crossover distortion eliminates servo hunting under null conditions and is required for most audio applications.



ULN-3755B Dwg. No. A-13,063



Dwg. No. A-13,064

ULN-3755W

The ULN-3755B is furnished in a 16-pin dual in-line package with copper heat-sink contact tabs. For higher power requirements, the ULN-3755W is supplied in a 12-pin single in-line power tab package.

Continued next page

The inputs are designed to allow a wide common mode range from the negative supply, (or ground in single supply applications) to within approximately two volts of the positive supply. Common-mode and power supply rejection are in excess of 60 dB. The amplifiers' wide output swing is complemented by current sensing, which is referenced to the negative supply and allows for feedback as required to produce a transconductance characteristic.

Separate supply pins are provided for the low-level input and high-level output circuits to allow voltage boost or bootstrapping to maximize output swing.

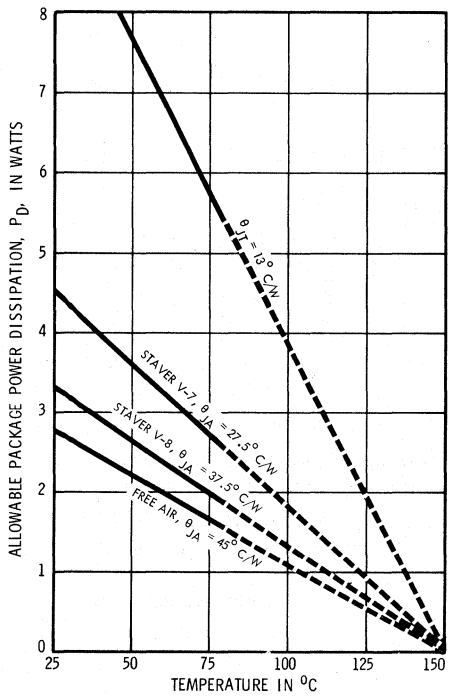
The ULN-3755B (batwing DIP) can typically dissipate 6 W at a tab temperature of +70°C. The lead configuration enables easy attachment of a heat sink while fitting a standard socket or printed wiring board layout. The ULN-3755W (SIP) can safely dissipate significantly higher power levels with appropriate heat sinking. With either package configuration, the heat sink is at the negative supply, or ground in a single-ended application.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Differential ($+V_S$ to $-V_S$) ..... 40 V
Peak Supply Voltage (50 ms) ..... 45 V
Continuous Ouput Current
I_{OUT} (V_S = ±15 V) ..... ±2.0 A
(V_S = ±6 V) ..... ±2.5 A
Peak Output Current, I_{OUT} (50 ms) ..... ±3.5 A
Package Power Dissipation, P_D ..... See Graphs
Operating Temperature Range, T_A .. −20°C to +85°C
Storage Temperature Range, T_S ... −55°C to +125°C

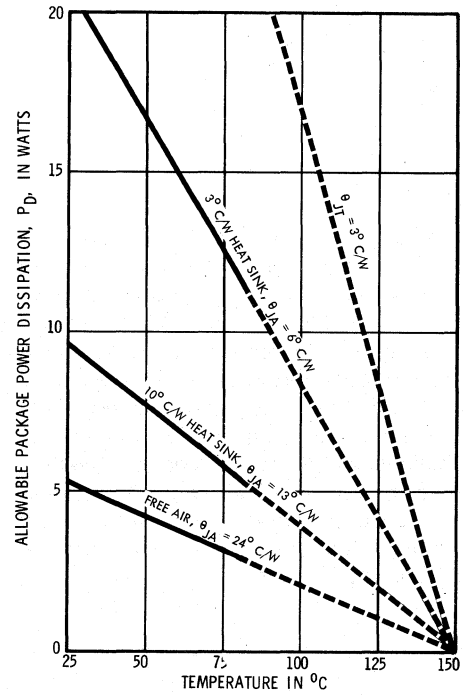
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

ULN-3755B



Dwg. No. A-11,793B

ULN-3755W



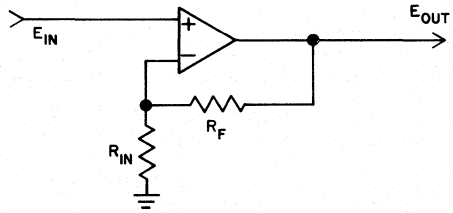
Dwg. No. A-11,794A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_S = \pm 6.0\,V$, $V_{BOOST} = +9.0\,V$, each amplifier tested separately (unless otherwise specified)

Characteristic	Test Conditions	Limits			
		Min.	Typ.	Max.	Unit
Functional Supply Voltage Range	$+V_S$ to $-V_S$	6.0	—	40	V
Quiescent Supply Current	I_{BOOST} (Each Amp.)	—	7.0	10	mA
	$+I_S$ (Total)	—	75	130	mA
Input Bias Current	$V_{OUT} = 0$	—	−80	−1000	nA
Input Offset Voltage	$V_{OUT} = 0$, $I_{OUT} = 0$	—	±1.0	±10	mV
Input Offset Volt. TC†	Over Op. Temp. Range	—	−15	—	µV/°C
Input Offset Current	$V_{OUT} = 0$, $I_{OUT} = 0$	—	10	100	nA
Input Noise Voltage†	BW = 40 Hz to 15 kHz	—	4.0	—	µV
Input Noise Current†	BW = 40 Hz to 15 kHz	—	60	—	pA
Crossover Distortion†	$P_{OUT} = 50$ mW, $R_L = 4\Omega$	—	0.2	—	%
Common Mode Rejection	$\Delta V_{CM} = 3\,V$	60	85	—	dB
Input Common Mode Range*	$V_S = \pm 6\,V$	−6.3	—	+4.0	V
	$V_S = \pm 15\,V$	−15.3	—	+13	V
Open-Loop Voltage Gain	f = 0	80	100	—	dB
Slew Rate	$V_{IN} = V_{OUT} = 6$ Vpp	0.5	1.0	—	V/µs
Gain-Bandwidth Product†	$A_V = 40$ dB	—	800	—	kHz
Channel Separation†	$I_{out} = 100$ mA, f = 1 kHz	—	60	—	dB
Output Voltage Swing	$I_{OUT} = 1\,A$, $V_{BOOST} = +6\,V$	9.0	9.5	—	Vpp
	$I_{OUT} = 1\,A$, $V_{BOOST} = +9\,V$	9.5	10.1	—	Vpp
Supply Voltage Rejection	$+V_S$, $\Delta V = 1\,V$	60	85	—	dB
	$-V_S$, $\Delta V = 1\,V$	60	80	—	dB
Thermal Resistance, Θ_{JT}*	ULN-3755B	—	—	15	°C/W
	ULN-3755W	—	—	3.0	°C/W
Thermal Shutdown Temp.†		—	165	—	°C

*This parameter is tested to a lot sample plan only.
†Typical values given for circuit design information only.

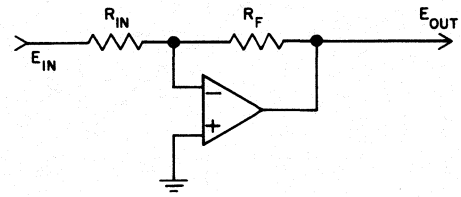
NON-INVERTING AMPLIFIER



$$\frac{E_{OUT}}{E_{IN}} = 1 + \frac{R_F}{R_{IN}}$$

IF $R_F = 0$ or $R_{IN} = \infty$ THEN $E_{OUT} = E_{IN}$

INVERTING AMPLIFIER



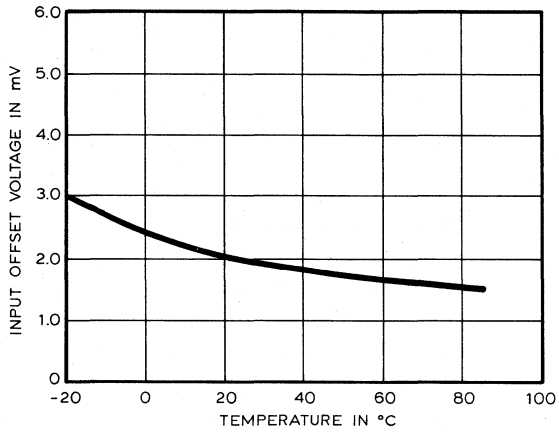
$$\frac{E_{OUT}}{E_{IN}} = -\frac{R_F}{R_{IN}}$$

Dwg. No. A-13,062

Dwg. No. A-13,061

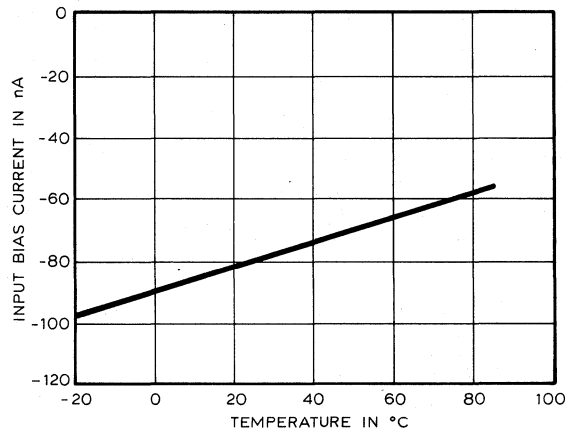
TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



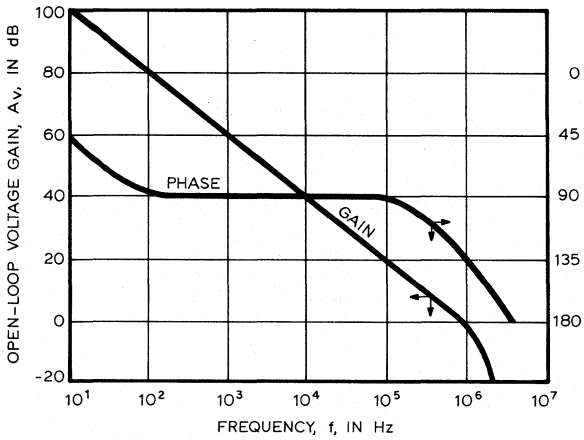
Dwg. No. A-13,294

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



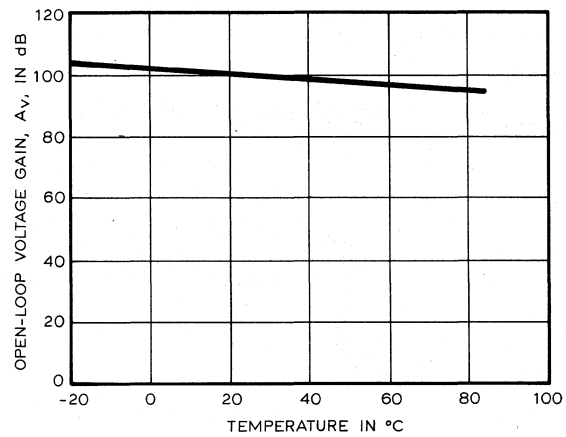
Dwg. No. A-13,295

OPEN-LOOP VOLTAGE GAIN AND PHASE AS A FUNCTION OF FREQUENCY



Dwg. No. A-13,296

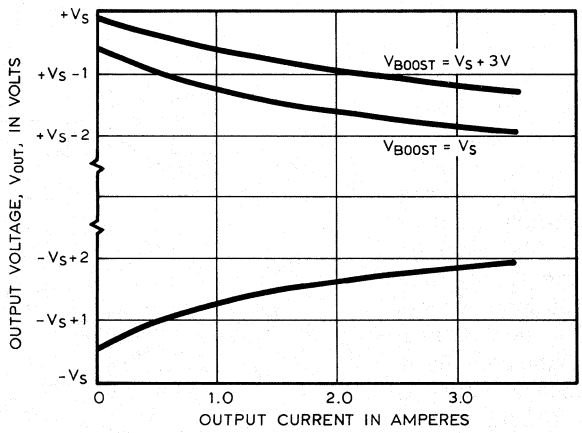
OPEN-LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



Dwg. No. A-13,297

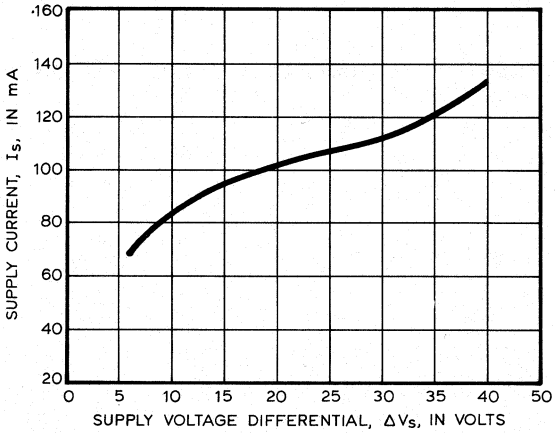
TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING AS A FUNCTION OF OUTPUT CURRENT



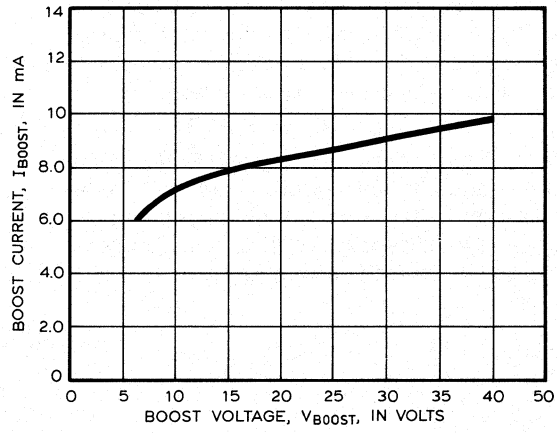
Dwg. No. A-13,298

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



Dwg. No. A-13,299

BOOST CURRENT AS A FUNCTION OF BOOST VOLTAGE



Dwg. No. A-13,300

APPLICATIONS

Current-Sense Transconductance Amplifier

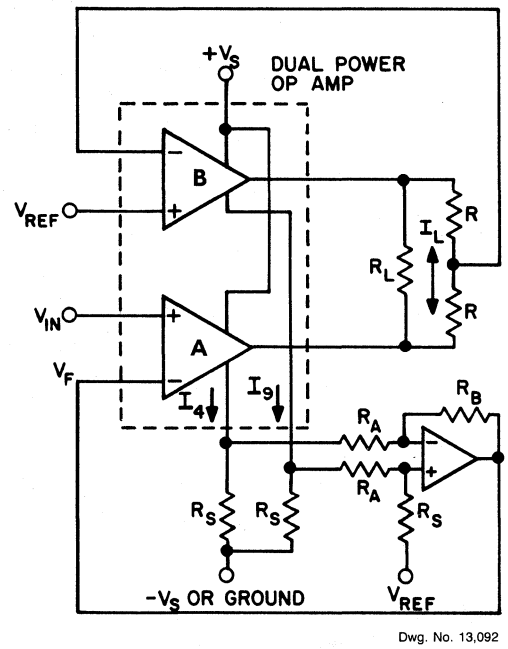
The ULN-3755B/W current-sense terminals can be used to obtain a transconductance function. This characteristic is commonly used in motor control applications such as voice coil servo or micro-stepping positioning systems found in many computer disc drives.

Figure 1 shows a ULN-3755W dual amplifier connected as a transconductance amplifier. In this example, amplifier B is used as a slave to amplifier A. Feedback from the current sensing resistors (R_S) in the emitters of the output current sinking transistors, is applied to the summing network and scaled to the inverting input of amplifier A where it is compared to the input voltage. The current sensing feedback imparts a transconductance characteristic to the amplifier's transfer function. That is, the voltage developed across the sensing resistors is directly proportional to the output current. Using this voltage as a feedback source allows expressing the gain of the circuit as output current in amperes vs. input voltage in volts. The gain thus assumes the dimensions of a transconductance function, expressed in mhos.

The negative-feedback forces the amplifier to adjust the output current to attain a value such that the feedback voltage equals the applied input voltage. The transfer function of the transconductance amplifier is approximately:

$$I_L = (V_{IN} - V_{REF}) = R_A/R_BR_S$$

In the figure, resistors R_A, R_B, and R_S define the transconductance gain. To avoid limiting the transconductance amplifier's output compliance (swing capability), low-value current-sensing resistors (R_S) should be used.



Dwg. No. 13,092

FIGURE 1
CURRENT-SENSE TRANSCONDUCTANCE AMPLIFIER

APPLICATIONS

Digitally Controlled Position Servo

In a position-control application, a microprocessor is often used to control a servomotor's shaft angle or to control position as in a disk drive application. The circuit requires small-signal input op amps, drivers, and power output stages. The circuit derives its input from the D/A converter, the output of which is determined by a code from the controlling microprocessor and related digital-control circuitry. The sensed position signal normally undergoes processing and comparison with the desired position, through the micro-processor system that produces an error signal to control the servo amplifier's output.

The circuit includes thermal and short-circuit protection, matching and thermal tracking inherent to monolithic construction. The configuration shown in Figure 2 uses a ULN-3755W dual power operational amplifier whose two independent outputs are connected ina push-pull, H-bridge arrangement. The IC's outputs also include clamping diodes with current-handling capacity equal to that of the output drivers.

The current-sense pins (4 and 9) provide access to the emitters of the H-bridge current sinks, thereby providing convenient output current sensing, while allowing separate low-current signal ground returns.

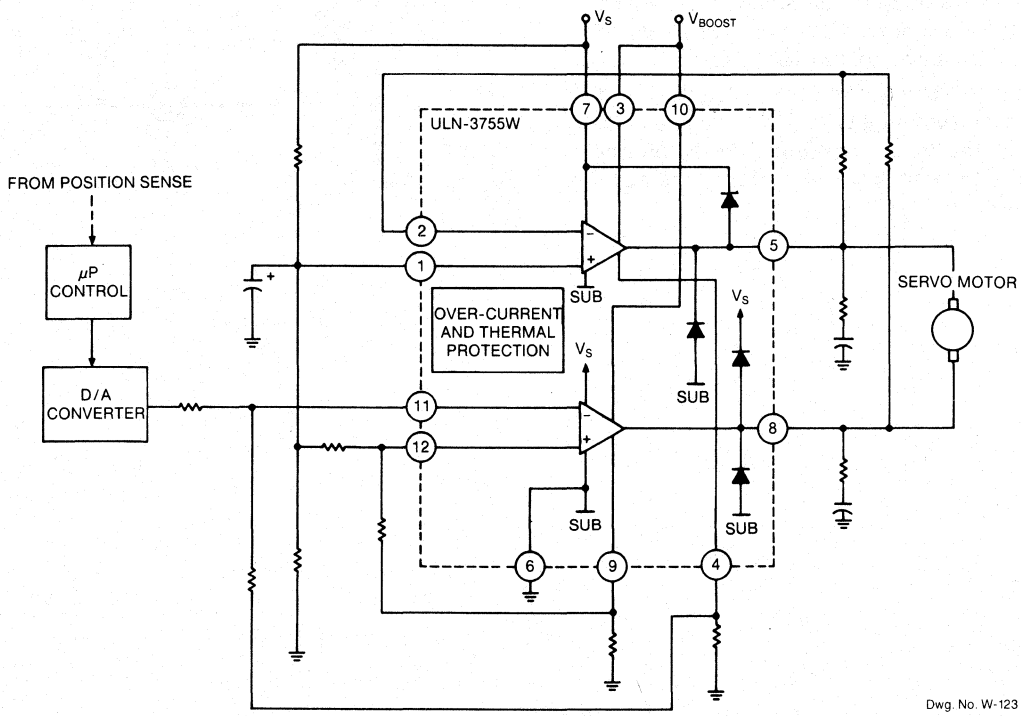


FIGURE 2
DIGITALLY CONTROLLED POSITION SERVO

APPLICATIONS

Increased Output-Voltage Swing

If a voltage higher than the supply is applied to the ULN-3755W's boost pins, as shown, the positive output swing is limited only by the saturation resistance of the output transistors (typically less than 0.5 ohms). For example, with a 12 V supply, the circuit typically supplies a 10.5 Vpp output swing at 1 A output current. Note that the externally-supplied boost voltage should be at least 3 V higher than the load supply voltage. This criterion satisfied, the boost voltage can be any value within the IC's 40 V absolute maximum rating.

Although the boost feature provides important additional output swing at the amplifier's full rated current, the IC's boost input requires only a low, unregulated current. This can be obtained from inexpensive, modular dc to dc converters, a simple overwinding in the motor, or a voltage doubler from the motor's driven phases.

An example of a simple voltage doubler boost supply is shown in Figure 3. This circuit affects the doubling by connecting a series diode-capacitor between the main supply and each end of the load.

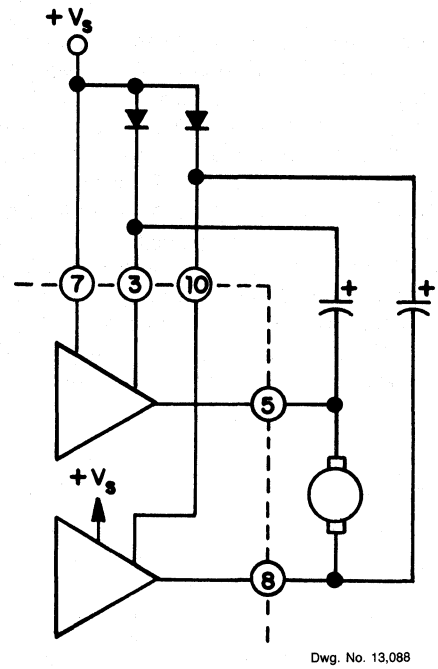


FIGURE 3
VOLTAGE DOUBLER BOOST SUPPLY

APPLICATIONS

N-Phase Motor Drive

Because of its high amplification factor and built-in power-output stage, an integrated power operational amplifier makes a convenient driver for ac motors. One op amp can be configured as an oscillator to generate the required ac signal. The power-output stage, of course, supplies the high-current drive to the motor.

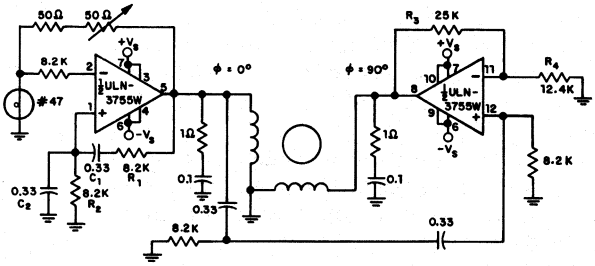
As shown in the motor-drive circuits in Figure 4, the controlling op amp is configured as a Weinbridge oscillator. The R_1C_1, R_2C_2 feedback networks determine the oscillation frequency, according to the following expression:

$$f_o = 1/(2\pi\sqrt{R_1R_2C_1C_2})$$

By varying either R_1 or R_2, the oscillator frequency can be adjusted over a narrow range.

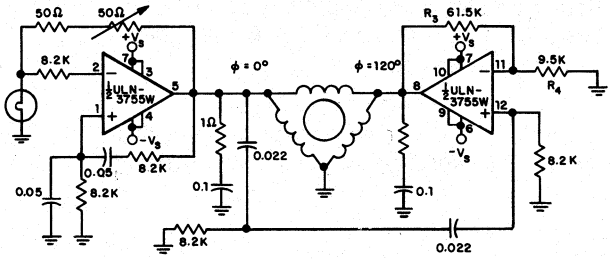
The R_3/R_4 ratio sets the second amplifier's gain to compensate for signal attentuation occuring in the phase shifters. A separate boost supply can be used to obtain additional output-swing capability.

The circuits can be driven from an external source, such as a pulse or square wave, setting the gain of the left-hand amplifier to a level less than that required for oscillation. The RC feedback networks then function as an active filter causing the outputs to be sinusoidal.



Dwg. No. 13,089

FIGURE 4a
TWO-PHASE 60 HZ AC MOTOR DRIVER



Dwg. No. 13,090

FIGURE 4b
THREE-PHASE 400 HZ AC MOTOR DRIVER

APPLICATION TIPS

1. Due to the nature of the composite PNP/NPN output structure, all applications of these devices require use of an output R-C compensation network, as shown in Figures 2, 4, and 5. Values shown are typical and will vary somewhat depending on load impedance.
2. As is the usual practice in high-gain power circuits, input and output grounds should be kept separate.
3. The current sense pins are the emitters of the power driver output totem poles and must be grounded or returned to the negative supply if not used for current sensing.
4. Provide good high-frequency supply bypass (ceramic or film capacitor).
5. All input, output, and supply leads should be properly dressed and kept as short as possible.
6. If the boost or bootstrapping capability is not used, the boost pins must be connected to the positive supply.

APPLICATIONS

ICs Control Motor Speed

In additional to the synchronous ac motor drives described above, the ULN-3755B/W can be used to provide accurate speed control of dc motors. Figure 5 shows a closed-loop system for controlling the speed of a 12 V dc motor. The circuit provides a bidirectional speed control. The amplifiers' push-pull configuration ensures a full rail-to-rail voltage swing (minus the output stages' saturation drops) across the motor in either direction.

The circuit uses a mechanically-coupled tachometer to provide speed-stabilizing feedback to the first amplifier section. The motor's speed and direction of rotation is set by adjusting the 10 kΩ potentiometer at the amplifier's noninverting input. The motor speed, in rpm, is given by the following expression:

$$S = V_{SET}(R_1 + R_2)/.0027\,R_2$$

The R_FC_F feedback network prevents oscillation by compensating for the inherent dynamic mechanical lag of the motor. The R_FC_F time constant is selected to match the particular motor's response or dynamic time constant. This should yield a good starting point for stabilizing the system with optimum response achieved by varying the compensating capacitor.

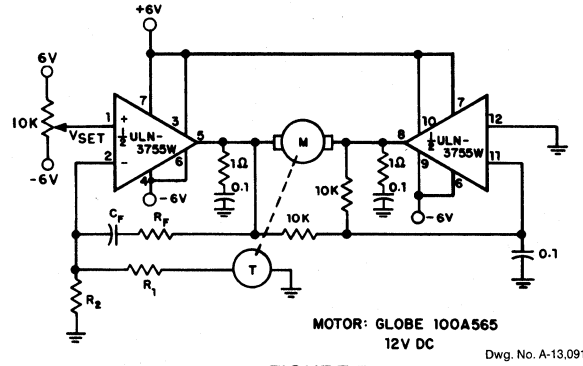


FIGURE 5
DC MOTOR SPEED CONTROL

MOUNTING POWER TAB 'W' DEVICES

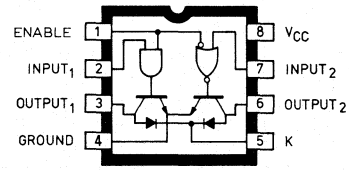
Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. Brute force mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialyphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

UDN-5725M
DUAL PERIPHERAL/POWER DRIVER
—Enhanced Output Capability

FEATURES

- DTL/TTL/PMOS/CMOS Compatible
- Low Input Current
- Continuous Output Current to 1 A
- 70 V Output Standoff Voltage
- Low Supply-Current Requirement



Dwg. No. 13,242

The UDN-5725M power driver combines NAND and NOR logic gates in a configuration particularly useful with small brushless dc motor drivers. The integrated circuit includes high-current saturated output transistors and transient-suppression diodes. It can be used in many applications beyond the capabilities of standard logic buffers: With inputs tied together, one of two loads is energized by a single input signal.

Additional applications include driving peripheral loads such as solenoids, light-emitting diodes, memories, heaters, and incandescent lamps with peak load currents of up to 1.2 A.

Each of the output transistors is capable of sinking 800 mA continuously at 55°C, or 650 mA at 85°C. In the OFF state, the drivers will withstand at least 70 V.

The UDN-5725M is supplied in a miniature 8-pin dual-in-line plastic package with a copper lead frame for superior package power dissipation ratings.

For applications requiring output currents of up to 700 mA, Series UDN-5740M is recommended.

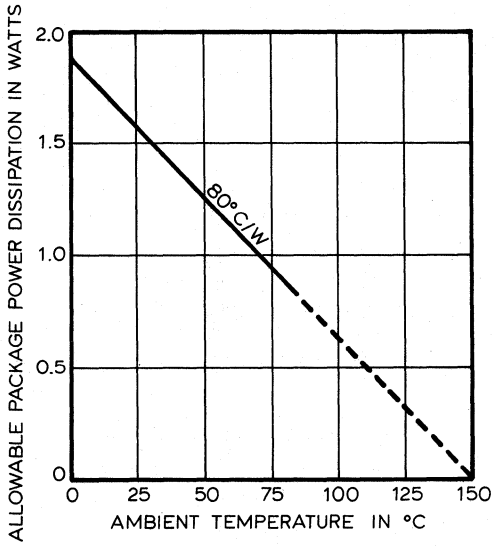
4

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Off-State Voltage, V_{OFF}	70 V
Output On-State Sink Current, I_{ON} (continuous)	1.0 A†
(peak)	1.2 A
Logic Supply Voltage, V_{CC}	16 V
Input Voltage, V_{IN}	30 V
Suppression Diode Off-State Voltage, V_{OFF}	70 V
Suppression Diode On-State Current, I_{ON}	1.0 A
Allowable Package Power Dissipation, P_D	1.5 W*
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

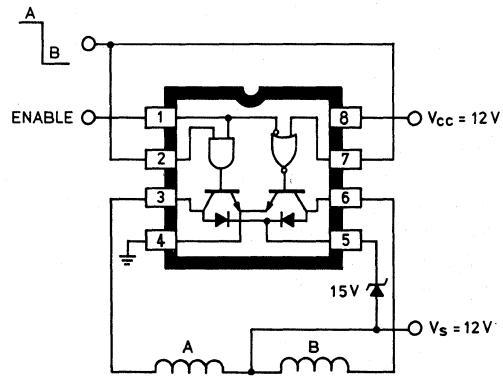
*Derate at the rate of 12.5 mW/°C above T_A = +25°C.
†Limited by P_D.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. 13,243

TYPICAL APPLICATION



Dwg. No. 13,244

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.75	12	14	V
Output Current, I_{ON}	—	—	650	mA
Operating Temperature Range	0	+25	+85	°C

TRUTH TABLE

STROBE INPUT	PHASE INPUTS 1	PHASE INPUTS 2	OUTPUTS 1	OUTPUTS 2
H	H	H	L	H
H	H	L	L	L
H	L	L	H	L
H	L	H	H	H
L	X	X	H	H

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Enable Input	Other Inputs	Output	Min.	Typ.	Max.	Units	
Output Reverse Current	I_{CEX}	—	4.75	0.8 V	2.0 V	70 V	—	—	100	μA	—
			4.75	0.8 V	0.8 V	70 V	—	—	100	μA	—
Output Voltage	$V_{CE(sat)}$	—	14	2.0 V	2.0 V	0.6 A	—	0.4	0.6	V	—
			14	2.0 V	2.0 V	0.8 A	—	0.7	1.0	V	—
			14	2.0 V	2.0 V	1.0 A	—	0.9	1.2	V	3
			14	2.0 V	0.8 V	0.6 A	—	0.4	0.6	V	—
			14	2.0 V	0.8 V	0.8 A	—	0.7	1.0	V	—
			14	2.0 V	0.8 V	1.0 A	—	0.9	1.2	V	3
	$V_{CE(sus)}$	+25°C	14	⊓	0 V	0.8 A	50	—	—	V	3,4
			14	⊓	2.0 V	0.8 A	50	—	—	V	3,4
Input Voltage	$V_{IN(1)}$	—	—	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	—	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	12.6	0.4 V	30 V	—	—	5.0	25	μA	1
	$I_{IN(1)}$	—	12.6	30 V	0 V	—	—	5.0	25	μA	1
Enable Input Current	$I_{IN(0)}$	—	12.6	0.4 V	30 V	—	—	10	50	μA	—
	$I_{IN(1)}$	—	12.6	30 V	0 V	—	—	10	50	μA	—
Input Clamp Volt.	V_{CLAMP}	—	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	5.0	0 V	0 V	Open	—	—	100	μA	2
Diode Forward Voltage	V_F	+25°C	5.0	0 V	0 V	0.6 A	—	1.5	2.0	V	—
			5.0	0 V	0 V	1.0 A	—	1.9	2.5	V	3
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	12.6	0 V	0 V	—	—	3.9	5.0	mA	—
			12.6	0 V	2.0 V	—	—	3.9	5.0	mA	—
	$I_{CC(0)}$	+25°C	12.6	2.0 V	0 V	—	—	22	30	mA	—
			12.6	2.0 V	2.0 V	—	—	22	30	mA	—

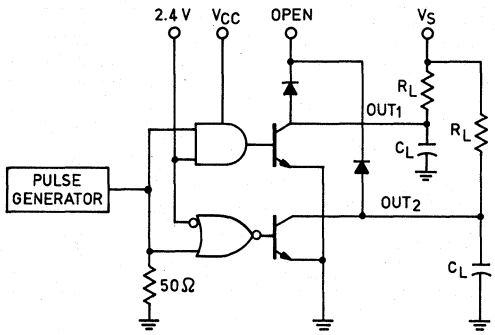
NOTES:
1. Except ENABLE input, each input tested separately.
2. Diode leakage current measured at V_R = 70 V.
3. Pulse Test.
4. L_L = 3 mH.

4

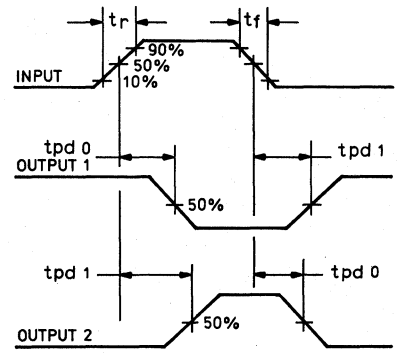
SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

Characteristic	Symbol	Test Conditions	Limits			Notes
			Min.	Max.	Units	
Turn-On Delay Time	$t_{pd\,0}$	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	500	ns	1, 2
Turn-Off Delay Time	$t_{pd\,1}$	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	750	ns	1, 2

NOTES: 1. Capacitance value specified includes probe and test fixture capacitance.
2. Voltage values shown in test circuit waveforms are with respect to network ground.



Dwg. No. 13,245



Dwg. No. 13,246

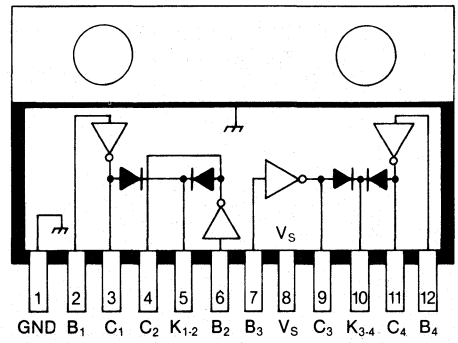
INPUT-PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	t_f = 7 ns	t_p = 1 μs
$V_{IN(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500kHz

UDN-7078W
QUAD HIGH-CURRENT DARLINGTON SWITCH

FEATURES

- Output Voltage to 90V
- 90V Sustaining Voltage
- Output Current to 3A
- TTL, DTL, or CMOS Compatible Inputs
- Internal Transient-Suppression Diodes
- Plastic Single In-Line Package
- Heat-Sink Tab



Dwg. No. DS-1015

This quad Darlington array is designed to serve as interface between low-level logic and peripheral power devices such as solenoids, motors, incandescent lamps, heaters, and similar loads up to 270 W per channel. The integrated circuit contains internal transient-suppression diodes that enable use with inductive loads. The input logic is compatible with most TTL, DTL, LSTTL, and 5V CMOS logic. The Darlington array is rated for operation to 90V and is recommended for operation with load currents of 3 A or less.

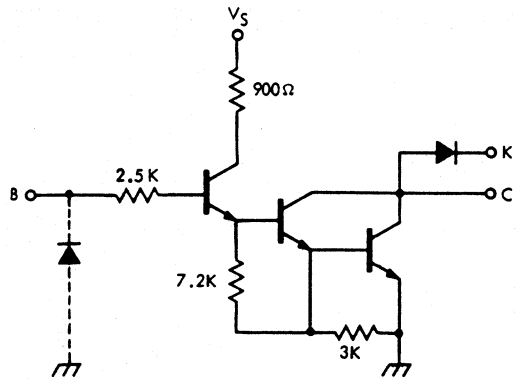
For maximum power handling capability, the device is supplied in a 12-pin single in-line plastic package with an integral power tab. The tab is at ground potential and needs no insulation. External heat sinks are usually required for proper operation of this device.

Similar quad high-current Darlington switches, for operation with supply voltages to 50V or 80V (35V or 50V sustaining), are UDN-2878W and UDN-2879W.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} < +70°C$

Output Voltage, V_{CE}	90V
Min. Sustaining Voltage, $V_{CE(sus)}$	90V
Output Current, I_C	3.0A
Supply Voltage, V_S	10V
Input Voltage, V_{IN}	15V
Total Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

PARTIAL SCHEMATIC
One of 4 Drivers



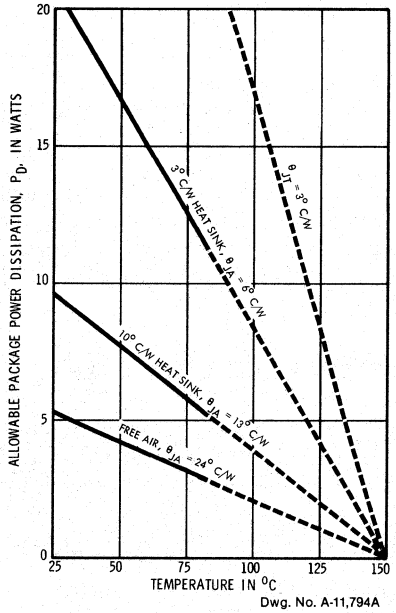
Dwg. No. A-12,037

ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_{TAB} < +70°C, V_S = 5 V

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 90V	–	100	μA
Output Sustaining Voltage	$V_{CE(sus)}$	I_C = 2.5 A	90	–	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_C = 0.5 A, V_{IN} = 2.75V	–	1.1	V
		I_C = 1.0 A, V_{IN} = 2.75V	–	1.3	V
		I_C = 2.0 A, V_{IN} = 2.75V	–	1.6	V
		I_C = 2.5 A, V_{IN} = 2.75V	–	1.9	V
		I_C = 3.0 A, V_{IN} = 2.75V	–	2.2	V
Input Voltage	$V_{IN(ON)}$	I_C = 3.0 A	2.75	–	V
	$V_{IN(OFF)}$		–	0.8	V
Input Current	$I_{IN(0)}$	V_{IN} = 0.8V	–	25	μA
	$I_{IN(1)}$	V_{IN} = 2.75V	–	550	μA
		V_{IN} = 3.75V	–	1.0	mA
Supply Current per Driver	I_S	I_C = 500 mA	–	6.0	mA
Clamp Diode Leakage Current	I_R	V_R = 90V	–	50	μA
Clamp Diode Forward Voltage	V_F	I_F = 2.5 A	–	2.5	V
		I_F = 3.0 A	–	3.0	V
Turn-On Delay	t_{PLH}	0.5 E_{in} to 0.5 E_{out}	–	1.0	μs
Turn-Off Delay	t_{PHL}	0.5 E_{in} to 0.5 E_{out}, I_C = 3.0 A	–	1.5	μs

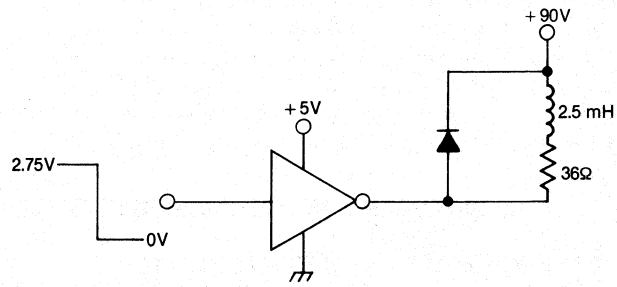
CAUTION: High-current tests are pulse tests or require heat sinking.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,794A

TEST FIGURE $V_{CE(sus)}$

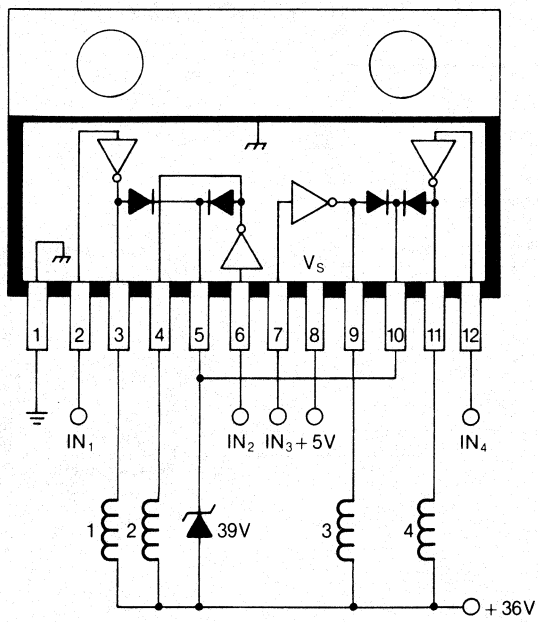


Dwg. No. DS-1016

4

TYPICAL APPLICATION

PRINT-HAMMER DRIVER



Dwg. No. DS-1017

POWER INTEGRATED CIRCUITS FOR MOTOR-DRIVE APPLICATIONS

IMPROVED SYSTEMS PERFORMANCE and reliability, lower component counts, and reduced cost are among benefits offered by space-saving Sprague power interface ICs. Many of the following devices are specifically designed for motor-drive applications. The development of these devices is especially significant in view of the increasing use of microprocessor-controlled servo and stepper motors.

Combining logic, power, and control in an integrated circuit requires special design techniques and experience. Sprague Electric has long been a leader in peripheral power interface technology.

UCN-4204B AND UCN-4205B STEPPER-MOTOR TRANSLATOR/DRIVERS

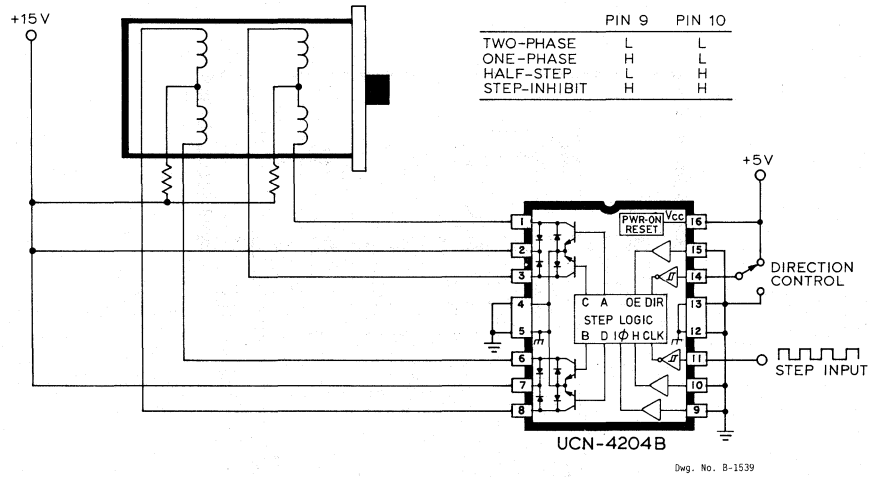
UCN-4204B & UCN-4205B INTEGRATED circuits drive permanent magnet stepper motors rated to 1.25 A and 30 V with a minimum of external components.

Internal step logic activates one or two of the four output sink drivers to step the load from one position to the next. The logic is activated when STEP INPUT (pin 10) is allowed to go HIGH. Single-phase (A-B-C-D), two-phase (DA-AB-BC-CD), or half-step (A-AB-B-BC-C-CD-D-DA) operation, and step-inhibit are selected by connections at pins 9 and 10. The sequence of states is determined by the DIRECTION CONTROL (pin 14).

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage, V_{OUT} (UCN-4204B)	15 V
(UCN-4205B-2)	25 V
Output Current, I_{OUT}	1.25 A
Logic Supply Voltage, V_{CC}	4.5 V to 5.5 V
Input Voltage, V_{IN}	5.5 V

L/R STEPPER-MOTOR DRIVE



UDN-2953B AND UDN-2954W FULL-BRIDGE MOTOR DRIVERS

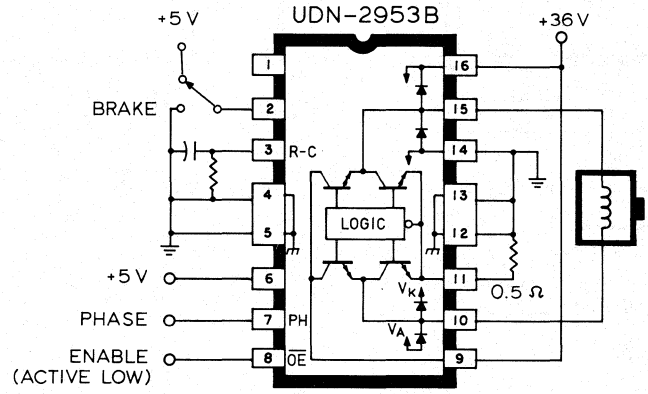
THE UDN-2953B AND UDN-2954W are designed for bidirectional, chopped-mode current control of d-c motors with peak start-up currents as high as 3.5 A. The output-current limit is determined by the user's selection of a sensing resistor. The pulse duration is set by an external RC timing network. The chopped mode of operation is characterized by low power-dissipation levels and maximum efficiency.

Internal circuit protection includes thermal shutdown with hysteresis, output transient-suppression diodes, and crossover current protection.

The UDN-2953B is supplied in a 16-pin DIP with heat-sink contact tabs. The UDN-2954W, with increased allowable package power dissipation, is supplied in a 12-lead single in-line power tab package. In both case styles, the heat sink is at ground potential and needs no insulation.

RECOMMENDED MAX. OPERATING CONDITIONS

Motor Supply Voltage, V_{BB} . . . . . 7.5 V to 50 V
Continuous Output Current, I_{OUT} . . . . . ±2.0 A
Peak Output Current, I_{OP} . . . . . ±3.5 A
Logic Supply Voltage, V_{CC} . . . . . 4.5 V to 15 V
Input Voltage, V_{IN} . . . . . 24 V



Dwg. No. A-12,649

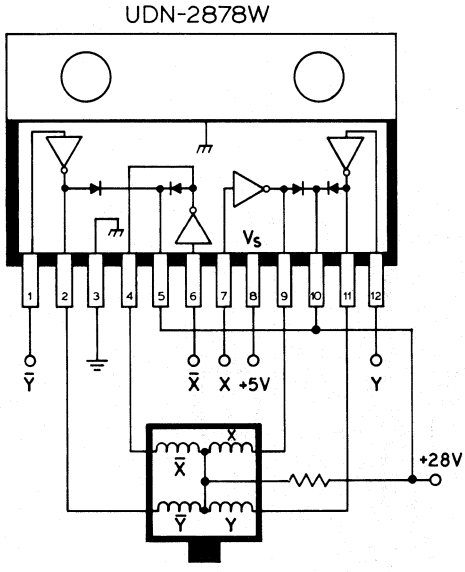
UDN-2878W AND UDN-2879W QUAD DARLINGTON SWITCHES

THE UDN-2878W AND UDN-2879W drive motor windings at up to 200 watts per channel. The integrated circuits include transient-suppression diodes and input logic that is compatible with most TTL, LS TTL, and 5 V CMOS. The 12-pin single in-line power-tab package allows maximum power-handling capability.

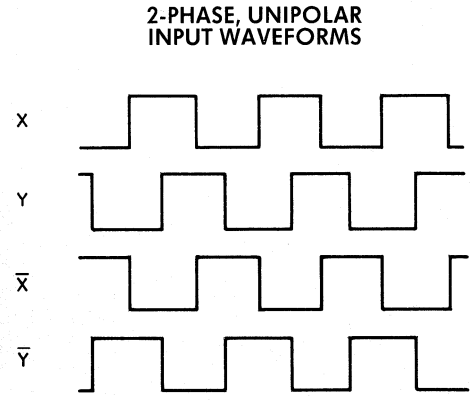
RECOMMENDED MAX. OPERATING CONDITIONS

Load Voltage, V_{CC} (UDN-2878W)	35 V
(UDN-2879W)	50 V
Continuous Output Current, I_C	4 A
Peak Output Current, I_{CP}	5 A
Logic Supply Voltage Range, V_S	4.5 to 7.0 V
Input Voltage, V_{IN}	V_S

STEPPER-MOTOR DRIVE



DWG. NO. A-11,975



Dwg. No. A-11,795

UDN-2965W-2 DUAL HIGH-POWER MOTOR DRIVER

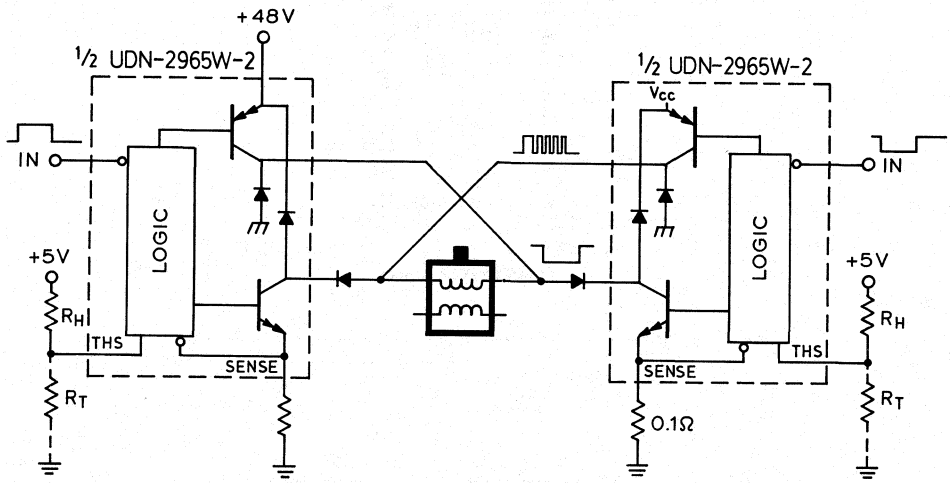
THE UDN-2965W-2 INTEGRATED CIRCUIT drives stepper motors in the full-bridge configuration. It is a high-power, multi-function interface driver that combines sink and source drivers, gain and level shifting, thermal shutdown circuitry, and pulse-width modulated current control. Output current, threshold voltage, and hysteresis are preset or may be externally set by the user. The UDN-2965W-2 is also well-suited for use as a dual high-power hammer driver.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_{CC} . . . . . 20 V to 50 V
Output Current, I_{OUT} . . . . . ±4.0 A
Input Voltage, V_{IN} . . . . . 5.5 V

4

BIPOLAR STEPPER-MOTOR DRIVE
(Pulse-Width Modulated)



R_H AND R_T DETERMINE HYSTERESIS AND PEAK CURRENT

Dwg. No. B-1538

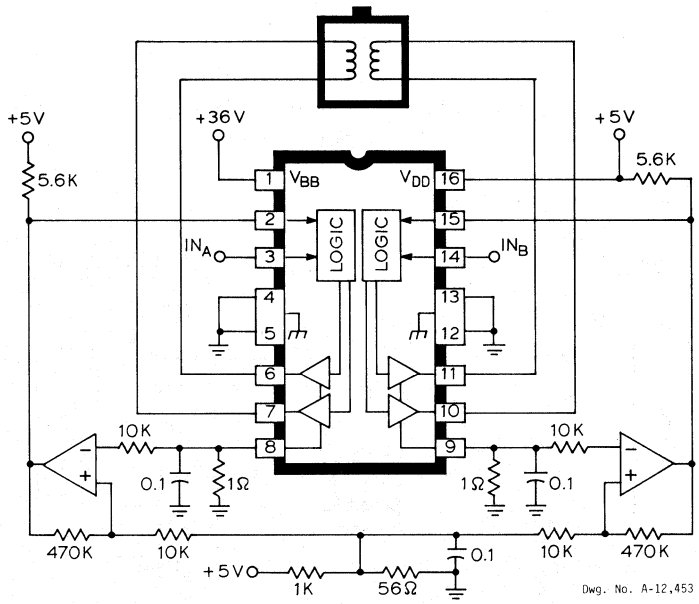
UDN-2993B DUAL FULL-BRIDGE MOTOR DRIVER

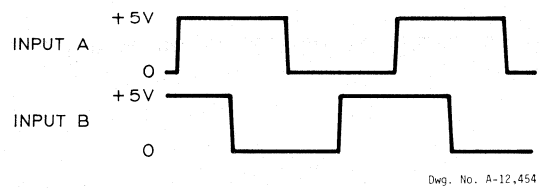
THE UDN-2993B MOTOR DRIVER contains two independent H-bridges capable of operating with load currents of up to 600 mA. An internally generated deadtime prevents potentially destructive crossover currents when changing load phase. Internal transient-suppression diodes are included for use with inductive loads. Emitter outputs allow for current sensing in pulse-width modulated applications.

RECOMMENDED MAX. OPERATING CONDITIONS

Load Voltage Range, V_{BB} . . . . . 10 V to 40 V
Output Current, I_{OUT} . . . . . ± 500 mA
Logic Voltage Range, V_{DD} . . . . . 4.5 V to 5.5 V

2-PHASE BIPOLAR STEPPER-MOTOR DRIVE
(Pulse-Width Modulated)





UCN-5800A, UCN-5801A, UCN-5813B, AND UCN-5814B UNIPOLAR MOTOR DRIVERS

DRIVING UNIPOLAR motors is one of many successful applications for the UCN-5800A, UCN-5801A, UCN-5813B, and UCN-5814B BiMOS II latched sink drivers. Selected devices, for higher voltage operation, are available as the UCN-5813B-1 and UCN-5814B-1.

All devices contain CMOS data latches, CMOS control circuitry, high-voltage, high-current bipolar Darlington outputs, and output transient protection diodes for use with inductive loads.

The UCN-5800A is a direct replacement for the original UCN-4401A. The UCN-5801A replaces the UCN-4801A. With a 5 V supply, BiMOS II devices typically operate at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. BiMOS III drivers, with output voltage ratings to 150 V, will be supplied as UCN-5900A and UCN-5901A.

Device	Package	Drivers	Features
UCN-5800A	14-pin DIP	4	Clear, Strobe, Output Enable
UCN-5801A	22-pin DIP	8	Clear, Strobe, Ouput Enable
UCN-5813B UCN-5813B-1	16-pin DIP	4	Strobe and Output Enable
UCN-5814B UCN-5814B-1	22-pin DIP	4	Clear, Strobe, Output Enable, & Chip Select

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage, V_{OUT}
- UCN-5800A & UCN-5801A . . . . . 35 V
- UCN-5813B & UCN-5814B . . . . . 35 V
- UCN-5813B-1 & UCN-5814B-1 . . . . . 50 V

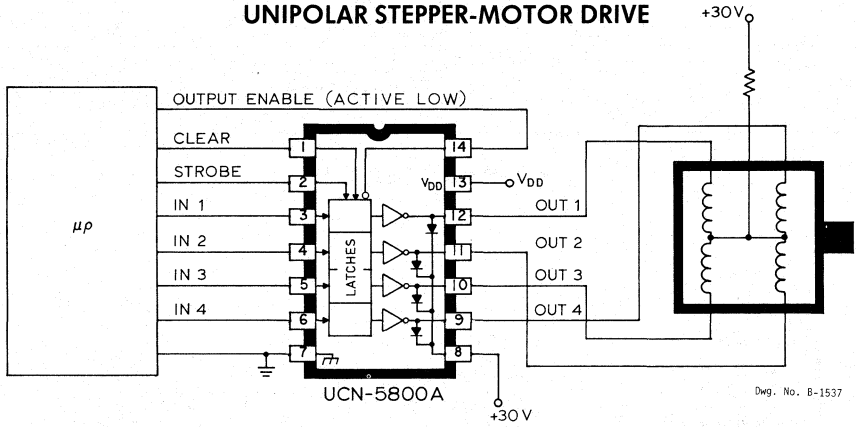
Continuous Output Current, I_{OUT}
- UCN-5800A & UCN-5801A . . . . . 350 mA
- UCN-5813B & UCN-5814B . . . . . 1.0 A
- UCN-5813B-1 & UCN-5814B-1 . . . . . 1.0 A

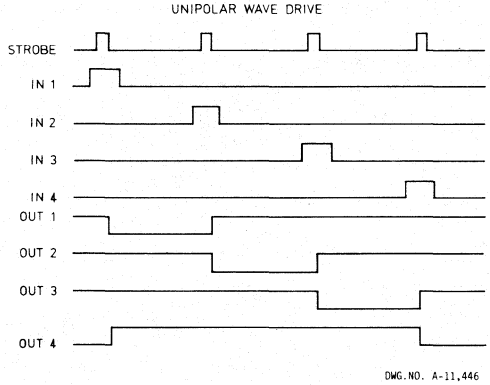
Logic Supply Voltage, V_{DD} . . . . . 4.5 V to 12 V

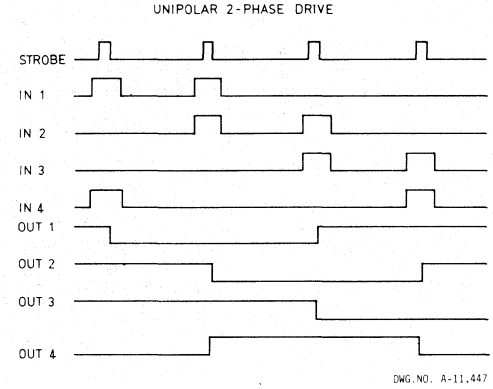
Input Voltage, V_{IN} . . . . . V_{DD}

4

UNIPOLAR STEPPER-MOTOR DRIVE







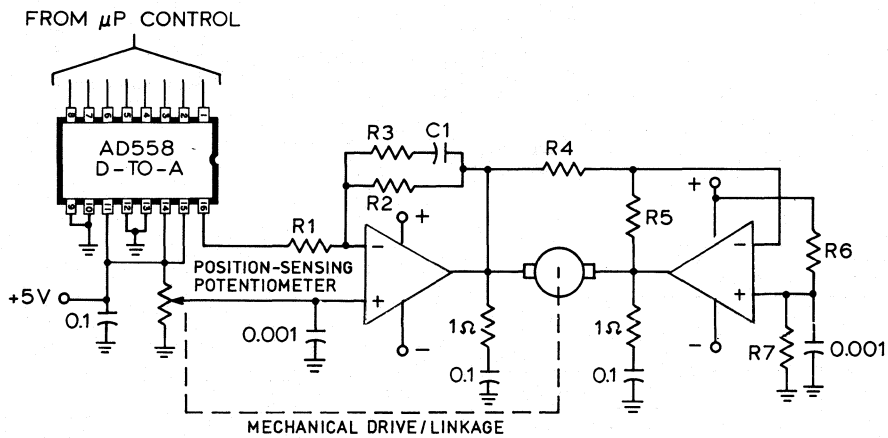
LINEAR MOTOR DRIVERS

POWER OPERATIONAL AMPLIFIERS are useful in driving voice-coil motors, linear servo motors, and ac and dc motors in a linear mode where motor speed or position is a direct function of a linear input signal. The operational amplifiers listed here are standard "building block" circuits providing almost unlimited application. The high-gain, high-impedance operational amplifier configuration allows many specialized input, output, and feedback arrangements.

All devices feature high output voltage swings, high input common mode range, high PSRR and CMRR. The unity-gain stable versions need no external compensation. Internal thermal shutdown circuitry protects these devices against output overloads. The dual amplifiers include programmable output current-sensing capability.

Part Number	Type	Max. ΔV_S	Cont. I_{OUT}	Peak I_{OP}	Features	Package	Engineering Bulletin
ULN-3751Z	Single	28 V	± 2.5 A	± 3.5 A	Unity-Gain Stable Internal Compensation	5-Lead SIP	27118.1
ULN-3753W	Dual	40 V	± 2.5 A	± 3.5 A	Prog. Current Sense, External Compensation	12-Lead SIP	27118.10
ULN-3753B			± 1.0 A	± 3.5 A		16-Pin DIP	
ULN-3755W	Dual	40 V	± 2.5 A	± 3.5 A	Bootstrapped Output, Unity-Gain Stable, Prog. Current Sense	12-Lead SIP	27118.11
ULN-3755B			± 1.0 A	± 3.5 A		16-Pin DIP	

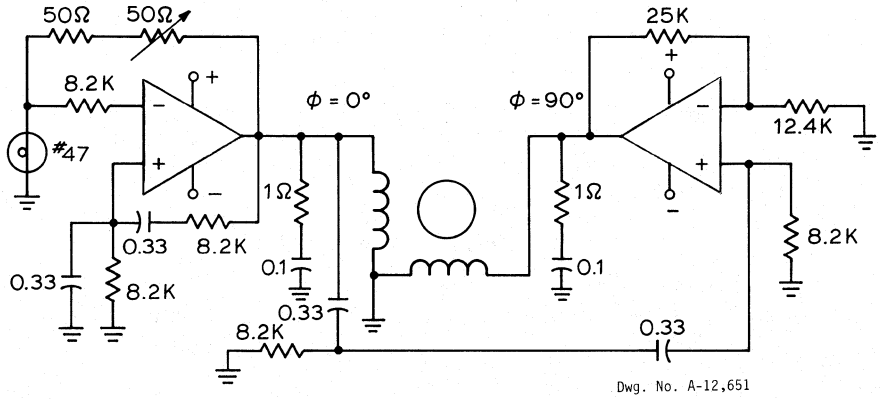
POSITION SERVO



R4 = R5 = R6 = R7
R1, R2 DEFINE D-C GAIN
R3, C1 SELECTED FOR LOOP COMP.

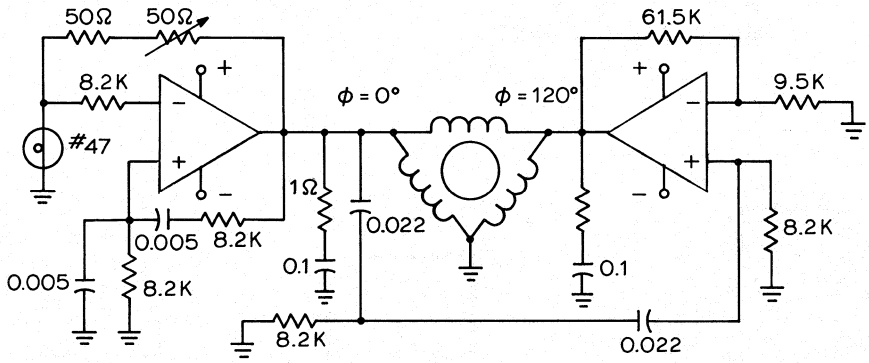
Dwg. No. A-12,652

TWO-PHASE, 60 Hz OSCILLATOR/MOTOR DRIVER



Dwg. No. A-12,651

THREE-PHASE, 400 Hz OSCILLATOR/MOTOR DRIVER



Dwg. No. A-12,650

ULN-2074B AND ULN-2075B HIGH-CURRENT DARLINGTON SWITCHES

THE ULN-2074B AND ULN-2075B high-current Darlington switches contain four isolated drivers. With appropriate input-level shifting, these devices can be used in emitter-follower (current-sourcing) applications.

The X-drive circuit shown below operates in the full-step mode with two phases ON in each position. X-drive is energy efficient and has better positional accuracy and hysteresis characteristics than conventional drive circuits.

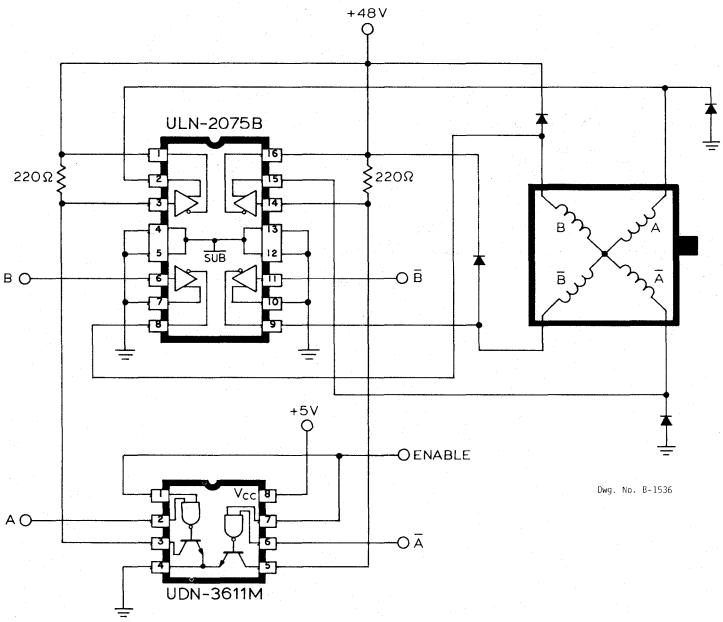
RECOMMENDED MAX. OPERATING CONDITIONS

Motor Supply Voltage, V_{BB}
- ULN-2074B ..... 35 V
- ULN-2075B ..... 50 V

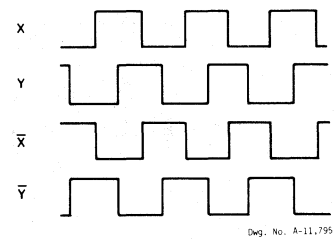
Output Current, I_{OUT}
- ULN-2074B ..... 1.25 A
- ULN-2075B ..... 1.5 A

Input Voltage, V_{IN}
- ULN-2074B ..... 30 V
- ULN-2075B ..... 50 V

X-DRIVE MOTOR CONTROL



INPUT WAVEFORMS



UDN-2941B QUAD HIGH-CURRENT SOURCE DRIVER

THE UDN-2941B high-current source driver has four independent emitter-follower drivers, associated input-level shifting, and output transient-suppression diodes. Special circuit design techniques result in reduced output-saturation voltages, and improved output-switching speeds. These two characteristics allow the UDN-2941B driver to operate high-current inductive loads at maximum efficiency.

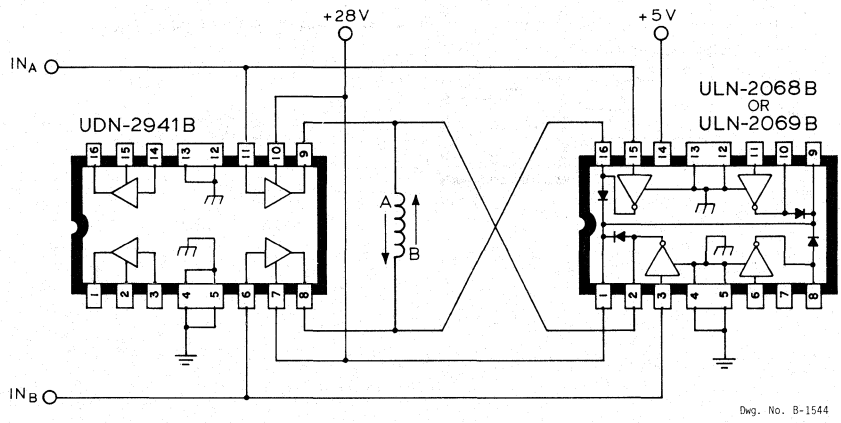
Where increased package power dissipation ratings are required, the modified bat-wing "B" package with a copper lead frame allows the attachment of an inexpensive heat sink. The heat sink is at ground potential and needs no insulation.

RECOMMENDED MAX. OPERATING CONDITIONS

Motor Supply Voltage, V_{BB} . . . . . 12 V to 30 V
Continuous Load Current, I_{OUT}
UDN-2941B . . . . . −1.5 A
ULN-2068B . . . . . 1.25 A
ULN-2069B . . . . . 1.5 A
Input Voltage, V_{IN} . . . . . 12 V

4

FULL-BRIDGE MOTOR DRIVER
(One of Two Windings Shown)



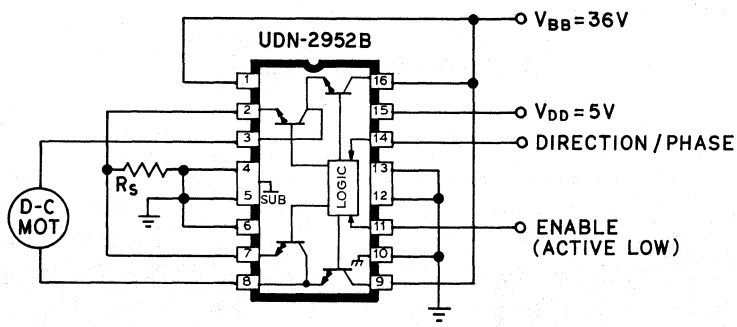
UDN-2952B AND UDN-2952W FULL-BRIDGE MOTOR DRIVERS

THE UDN-2952B AND UDN-2952W power drivers provide bi-directional control of d-c motors operating with peak start-up currents as high as 3.5 A. These integrated circuits include extensive circuit protection. Both drivers have adjustable short-circuit protection, a thermal shutdown network that disables the motor driver if package power dissipation ratings are exceeded, and internal diode transient suppression.

RECOMMENDED MAX. OPERATING CONDITIONS

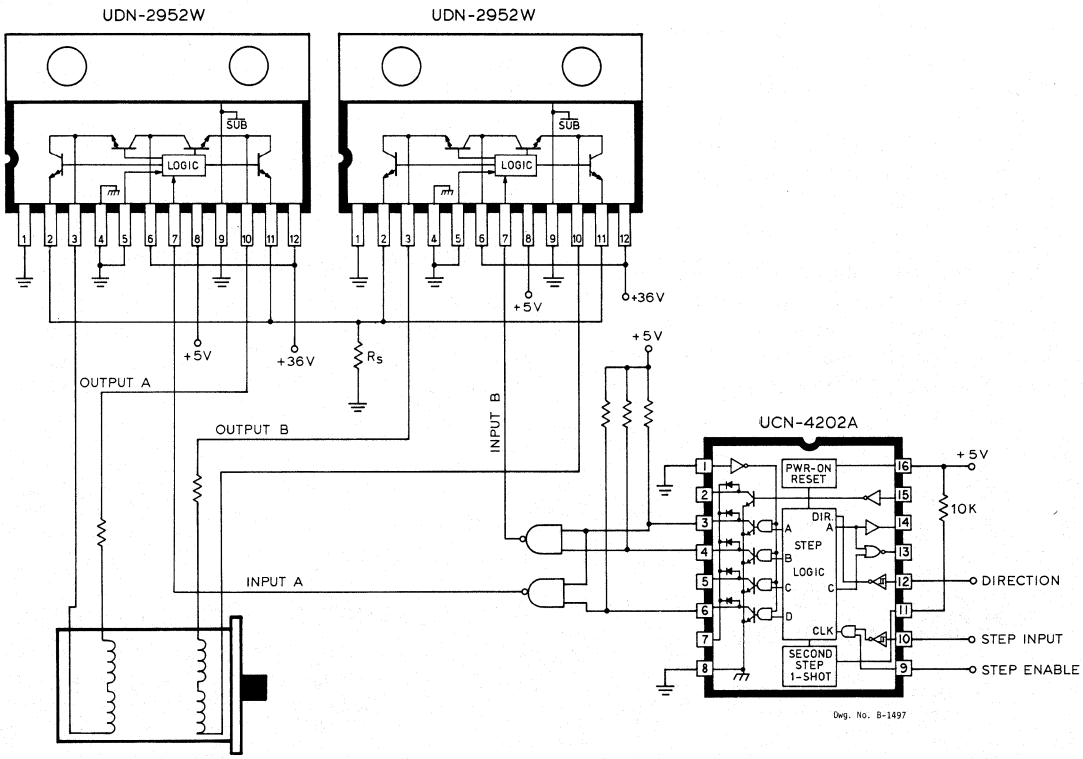
Motor Supply Voltage Range, V_{BB} . . . . . 4.5 V to 40 V
Continuous Output Current, I_{OUT} . . . . . ±2.0 A
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 13.5 V

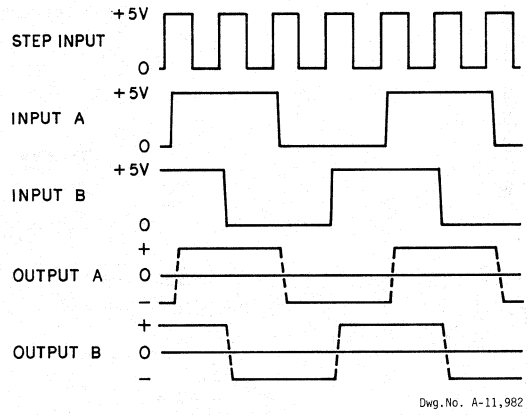
FULL-BRIDGE DC MOTOR DRIVE



Dwg.No. A-11,984

BIPOLAR STEPPER-MOTOR DRIVE





NOTES:

1. This is *not* a bipolar, pulse-width modulated application.
2. Resistor R_S sets the maximum allowable output current for protection against crossover currents and short circuits. $R_S = 0.6/I_{LIMIT}$.

UDN-2935Z AND UDN-2950Z
HIGH-CURRENT BIPOLAR HALF-BRIDGE MOTOR DRIVERS

THE UDN-2935Z AND UDN-2950Z ICs are monolithic half-bridge motor drivers in power tab TO-220 style packages. The circuits combine sink and source drivers with diode protection, gain and level shifting systems, and a voltage regulator for single-supply operation. They are designed for servo-motor drive applications using pulse-width modulation.

The PWM drive mode is characterized by minimal power dissipation requirements and allows the output to switch currents of 2 amperes. Output d-c current accuracies of better than 10% at 100 kHz can be obtained.

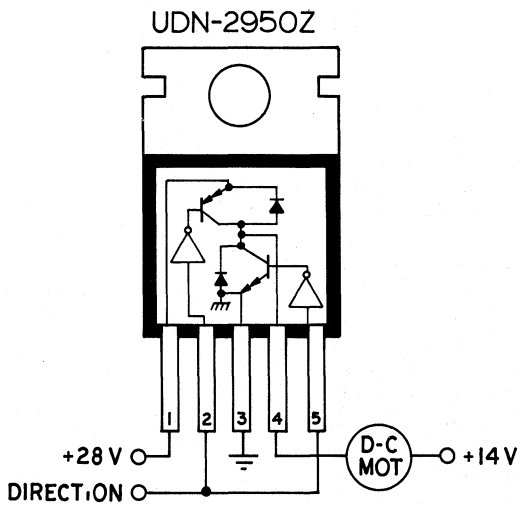
The UDN-2935Z and UDN-2950Z may be used in pairs (full-bridge) to drive d-c stepper motors or brushless d-c motors.

Either power driver may also be used in stepper motor bipolar bridge circuits as, for example, with the Sprague UCN-4202A or UCN-4204B stepper motor translator/drivers.

RECOMMENDED MAX. OPERATING CONDITIONS

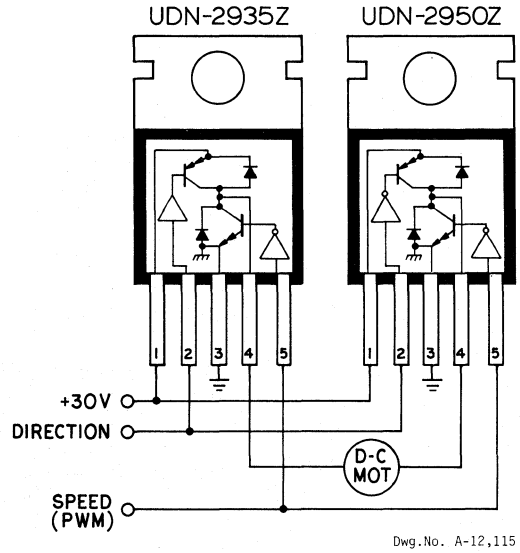
Supply Voltage, V_S	8.0 V to 35 V
Continuous Output Current, I_{OUT}	±2.0 A
Peak Output Current, I_{OP}	±3.5 A
Input Voltage, V_{IN}	5.5 V

SINGLE-WINDING DC OR STEPPER-MOTOR DRIVE



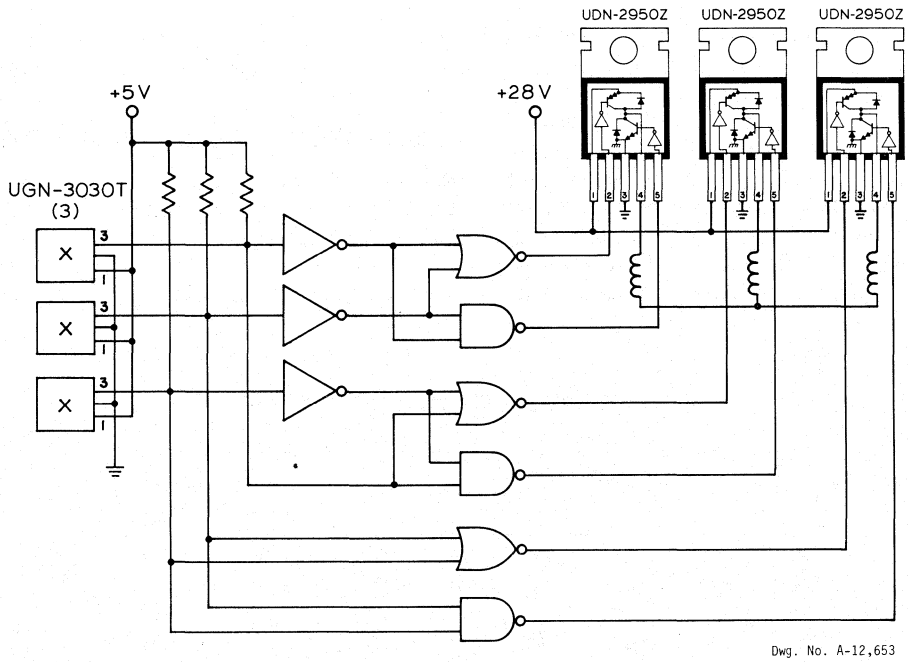
Dwg.No. A-12,114

FULL-BRIDGE DC SERVO-MOTOR DRIVE



Dwg.No. A-12,115

3-PHASE BRUSHLESS DC MOTOR CONTROL
(Using Sprague Hall Effect Sensors)



Dwg. No. A-12,653

UDN-2933B AND UDN-2934B
3-CHANNEL HALF-BRIDGE MOTOR DRIVERS

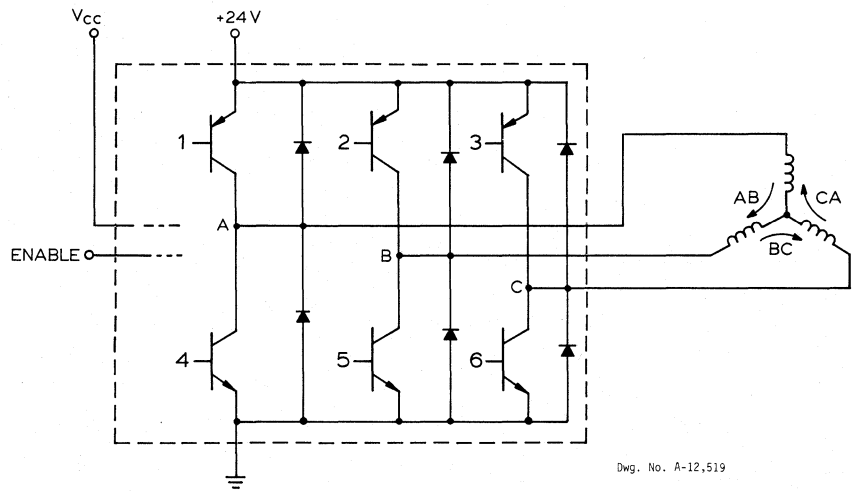
THE UDN-2933B AND UDN-2934B integrated circuits are specifically designed for three-phase, bipolar brushless d-c motor applications. Saturated drivers provide for low output-voltage drops at maximum rated current. The two devices differ only in input logic levels: The UDN-2933B is for use with TTL and 5 V CMOS. The UDN-2934B is intended for use with 12 V CMOS. Both devices have a common ENABLE function, independent inputs, internal transient suppression, and tri-state outputs allowing them to be used in diverse applications.

RECOMMENDED MAX. OPERATING CONDITIONS

Motor Supply Voltage Range, V_{BB} . . . . . 10 V to 30 V
Output Current, I_{OUT} . . . . . ±800 mA
Logic Supply Voltage Range, V_{CC}
UDN-2933B . . . . . 4.5 V to 5.5 V
UDN-2934B . . . . . 10 V to 13.5 V

3-PHASE BRUSHLESS DC MOTOR DRIVE

Driver Inputs						Motor	Electrical
1	2	3	4	5	6	Current	Degrees
Low	High	High	Low	High	Low	AB	0
Low	High	High	Low	Low	High	−CA	60
High	Low	High	Low	Low	High	BC	120
High	Low	High	High	Low	Low	−AB	180
High	High	Low	High	Low	Low	CA	240
High	High	Low	Low	High	Low	−BC	300



SWITCHING INDUCTIVE LOADS WITH POWER INTERFACE ICs

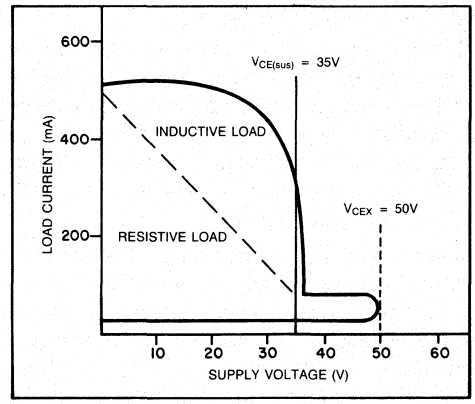
Integrated circuits that carry both logic and bipolar power devices — whether for driving print hammers, servos, steppers, relays, or brushless dc motors — are going a long way toward consolidating industrial-control electronics. Though these power interface ICs greatly simplify the system designer's task, they must be implemented carefully when they operate an inductive load.

To do so, the engineer must fully understand how the device's fundamental specifications relate to that inductive load, ensuring that the chip's breakdown limits are never exceeded. For example, the designer must be able to distinguish between the vaguely similar but quite different output-voltage specifications and know how to clamp transients since they cannot be prevented. The limitations and idiosyncrasies of ever-present parasitic elements also need to be well understood if the device is to operate flawlessly.

The biggest roadblocks to successful circuit design are two frequently misunderstood specifications. The first is the power interface chip's maximum output voltage, V_{CEX}. In most cases, this parameter approximates $V_{BR(CBO)}$, the minimum collector-base breakdown voltage with the emitter lead open. The actual designation would be $V_{BR(CEX)}$, which denotes that there is a standard resistance in the emitter lead. It should not be exceeded at any time, especially if the load is inductive.

The maximum collector-base breakdown value for a given IC is confirmed by applying a voltage to the device's output to measure its maximum leakage current, which is specified in the data sheet. Operating any load above the voltage that may produce the maximum leakage current is thus unsafe. Even with resistive loads, the user may encounter occasional trouble if the load line is steep. Trouble occurs because the line may cross the point equal to the minimum collector-emitter sustaining voltage.

The second fundamental specification, $V_{CE(sus)}$, is the greatest voltage that the chip can sustain under worst-case conditions. This limit is determined by the minimum collector-emitter voltage



DWG. NO. A-13,009

1. The limits of power interface chips are more likely to be exceeded when operating inductive loads due to the reactive voltages generated by switching. Also, the collector-emitter potential may be above the supply voltage. Thus designs must ensure the dc operating voltage stays below the device's minimum sustaining voltage, $V_{CE(sus)}$, for a given quiescent load current. In no case should its maximum output voltage, V_{CEX}, be exceeded.

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for a specified output current. It can also be measured with a coil dump test, in which the IC's output is switched off and its output voltage measured. Generally, the first test is done at 5% to 10% of the nominal output current for a given application. The coil test is often run at a high output current and for a specified inductance. Either of these conditions will satisfactorily confirm a device's minimum output-sustaining voltage.

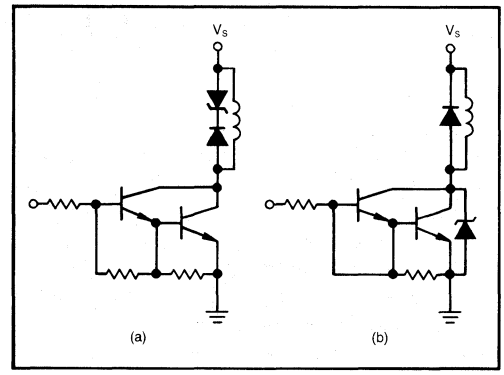
Switching inductive loads with interface ICs, then, demands careful attention to both the device's load line and the guaranteed output-sustaining voltage. With inductive loads, reactive voltages often greatly exceed the source voltages when the chip is switched off (Fig. 1). The source voltage is clamped off to a safe value with flyback diodes that are effectively shunted across the inductive load and are often internal to the device. Without such protection, or that offered by resistor-capacitor snubbing networks, the high voltage that results from switching the coil will likely damage or destroy the device. Unfortunately, internal protection alone is often insufficient, and external clamping circuitry must be added.

Of great concern to the designer is that insufficient output protection may result in gradual — and thus hard to detect — secondary breakdown. Particularly hardy power interface chips may seem to stand up well to occasional transients in excess of 100 V for a load supply voltage of 12 V; that is, until they suddenly fail.

When fast switching is a must, it is generally only achieved with a circuit that allows the output voltage to rise fast and exceed the supply voltage. For such approaches, other schemes must be used. Typically, both external Zener diodes and resistors should be employed. Together, they furnish inexpensive protection. Zener diodes, however, are often used alone.

DROPPING THE RESISTOR

The reason for this apparent omission is obvious once it is realized that the flyback voltage is not only a function of current and resistance but also of the number of outputs switching off at any time. Only well-defined or simultaneous switching sequences are suitable for resistors; without either, the magnitude of the voltage transient produced is difficult to determine. Some industrial timing circuits may be both low-speed and predictable; unfortunately, random switching is the rule rather than the exception.



DWG. NO. A-13,007

2. Arranging a Zener diode network in series to clamp a power interface chip's output allows its flyback voltage to rise above the supply voltage, enabling the device to be turned off faster (a). When poorly regulated supply voltages power a circuit that drives multiple devices whose voltage transients exceed the chip's capability, a parallel configuration is preferred (b).

Zener diodes, on the other hand, do not suffer from that limitation. The voltage rating for a series arrangement (Fig. 2a) is determined by:

$$V_Z = V_{CE(sus)} - V_{SUPPLY} - V_F$$

where V_F is the diode's forward voltage drop. Thus for an IC with a sustaining voltage of 35 V, a 15 V supply, and a diode drop of 2 V, the maximum Zener value is 18 V. For designs that use many power ICs for multiple loads, it is often practical to work with multiple Zener diodes with lower power and maximum current ratings. That avoids the cost of power devices and sidesteps their need for heat sinks.

Zener diodes can be placed in parallel across the output as well (Fig. 2b). In this case, the Zener voltage must be slightly below the minimum sustaining voltage. Automotive systems, for one, typically employ internal 30 V to 35 V clamps in their interface chips because such operations as "jump starting" two or three 12 V batteries precludes the series approach. A setup exhibiting an unregulated supply voltage, which varies con-

siderably, may also necessitate the parallel clamping approach.

Beyond staying within the chip's maximum voltage rating, the designer's second major concern is avoiding problems created by inherent parasitic elements. In the early days of the TTL device and its gold-doped low-resistivity silicon, parasitic problems were virtually non-existent. (Adding gold to improve circuit speed effectively killed parasitic elements.) Linear bipolar ICs and a wider range of power loads make parasitic concerns much more of an issue. The vast majority of today's chips are junction-isolated ICs and they all demonstrate such unwanted by-products inherent in their fabrication processes.

The most common parasites pertaining to inductive loads are the vertical PNP and lateral NPN transistors that are created by a device's protection circuitry. The internal flyback diode of a power interface chip, for instance, becomes a low-gain transistor (Fig. 3).

Most circuits are not affected by this parasitic transistor, unless the switching frequency is above the audio range. Curiously enough, many of the problems are related to power dissipation. The parasitic transistor often draws considerable power, thus raising the chip's temperature, even when the transistor's gain is below unity.

MINIMIZING THE PROBLEM

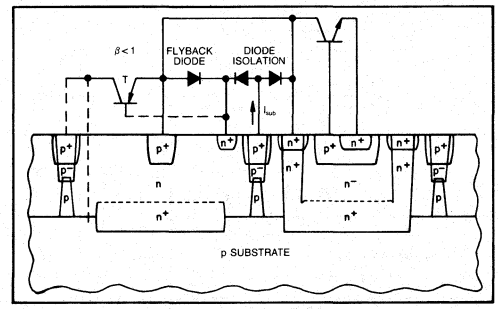
Where practical, lowering the supply voltage and decreasing the pulse repetition rate will minimize the trouble. When high switching rates and maximum source voltages are necessary, the best technique is to place a discrete diode across the devices' output stage, between collector and the supply line (or to ground if Zener clamping is used). A discrete diode, with its lower forward-voltage drop, effectively shunts the flyback diode and will conduct most of the current during clamping.

Less troublesome, but still of concern, are the lateral parasitics that may cause circuit anomalies and malfunctions. In many stepper motors particularly, the transformer action of the motor windings produces undesirable substrate currents into the IC. In effect, a negative voltage is applied at the device's output, and current is injected into its substrate.

The problem is exacerbated by the IC's junction isolation, which produces a parasitic transistor across the isolation diodes (the transistor's base lead is connected at their junction). Frequently, current injected into the device's output is sufficient to create formidable substrate currents, thus turning all lateral transistors on.

As a result, the device's leakage current may increase, and the chip may be inadvertently activated. In extreme cases, positive feedback causes the IC to destroy itself. Circuits employing small low-current stepper motors are not generally a problem, since the substrate current is seldom sufficient to turn on the transistor. In high-current applications, however, putting a discrete diode across the output device's collector-ground junction will cure the problem.

A parasitic diode exists at the input circuit to most power interface chips. In many instances, it may hinder circuit operation when a negative voltage is applied to the input, since substrate currents may be created. Connecting a discrete back-biased diode directly between input and ground diverts current away from the substrate. Provisions should be made, though, for limiting the current if the input state is to be pulled to voltages well below ground.



DWG. NO. A-13,008

3. The interface IC's flyback diode almost always creates a parasitic transistor (T) at the device's output. Further, substrate currents form a transistor across the diodes that isolate various junctions of the chip. Moreover, parasitic diodes at the inputs also are common. Adding external protection diodes at both the input and output eliminates many undesired circuit operations such as false triggering. Further, it may well prevent the device from being destroyed by the positive feedback currents that are occasionally generated.

TURNING IT OVER

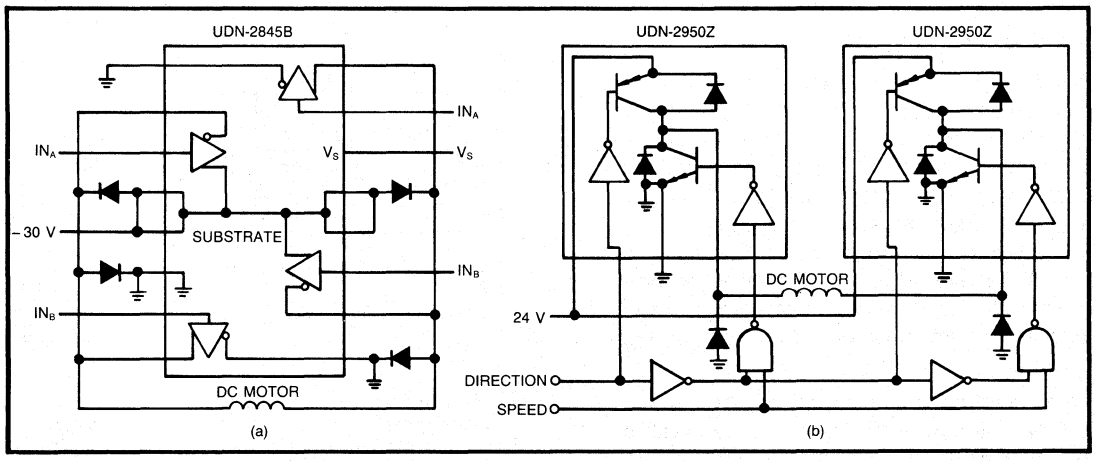
Employing power interface ICs to drive motors demands adherence to four basic design rules. First, if the device is without internal protection, diodes must be added to clamp both positive and negative overshoots caused by inductive loads. Second, if the device is protected with internal clamps, external diodes could be added. That not only serves as insurance but eliminates the effects of parasitic elements, which occasionally trigger or even destroy the chip. Third, in balanced drive arrangements, complementary input signals should be appropriately skewed. Doing so avoids crossover currents that may cause excessive heating and reduce available output current. Finally, when it is unclear if the interface chip furnishes suitable drive to the motor — or if it is difficult to damp the effects of parasitics at high outputs — discrete bipolar transistors and appropriate clamping may be the solution. The transistors driven by the chip, in turn power the motor.

Consider a dc motor circuit driven by a 1.5 A quad Darlington device that uses four discrete diodes for protection and commutation (Fig. 4a). The configuration, which employs a so-called bipolar, or bridge arrangement, allows the motor to turn either clockwise or counterclockwise.

HALF-BRIDGE OPERATION

Alternatively, the half-bridge motor driver run by a pair of chips also makes possible bipolar operation (Fig. 4b). Further, speed is controlled by a pulse-width-modulated waveform. Clamping diodes on either side of the motor take care of the problems caused when the motor changes direction. And with minimal modification, the driving circuitry accommodates ac motors as well. More specifically, no clamping diode is required between pin 4 of each device and ground. The designer need only build circuitry to control the speed of the motor; no circuitry for defining its direction is required. As before, pins 2 and 5 of each device accept complementary driving signals.

Where intermediate, or discrete, bipolar transistors drive a dc motor, it is always best to install any clamping or commutating diodes close to the motor itself. Otherwise, inductive undershoots or overshoots may find their way through the transistors, triggering or damaging them or the power interface chip.



DWG. NO. A-13,006

4. Following simple clamping and driving rules ensures trouble-free operation. Four diodes protect and properly commutate a chip that drives a two-way dc motor (a). Alternatively, two diodes protect a pulse-width modulated dc motor circuit from damage (b). In both cases, input signals should be appropriately skewed. When transistors are used as intermediate drivers, the clamping circuitry should be placed as closely to the motor as possible.

AN INTEGRATED 3-PHASE BRUSHLESS DC MOTOR DRIVER

Three-phase brushless dc motors are especially useful because they have no brushes to make noise, dust, or wear out. The brushes of a conventional motor have been replaced by position sensors, usually Hall effect or optical devices. These sensors detect the rotor position with respect to the stator windings. This information is used to drive the windings in a sequence synchronized with the rotor position, called commutation. To use a three-phase brushless motor usually requires custom ICs to perform the commutation, and discretes for drivers. Then, to control the motor current, and with it speed and torque, requires pulse width modulation circuitry. All this adds up to many components and an expensive solution.

Now, due to progress in integrated power technology, all of the functions needed to drive three phase brushless motors can be performed by one chip. The UDN-2936W incorporates Hall effect sensor decoding logic, power outputs capable of driving 2 A continuous at 50 V, PWM current limiting, direction control, dynamic braking, and integrated protection features. This device can be used to provide a simple, inexpensive, and reliable solution to the problem of driving brushless dc motors.

Overall Chip Structure

The UDN-2936W is made up of five sections, namely the commutation logic, output drivers, current limiting, direction and braking, and thermal shutdown. All logic and power functions utilize only bipolar processing, which allows for high power with an efficient use of die area.

Motor Commutation

In a three-phase motor, winding current must be synchronized to rotor position to run the motor efficiently, i.e., with unidirectional torque. Hall effect sensors detect rotor position, which must be decoded to drive the coils in the proper sequence. Hall effect sensors produce low level differential analog outputs. Today's Hall effect ICs amplify this signal 86 make it easier to use. These Hall effect ICs produce either large signal ac linear waveforms, or open collector digital signals. The UDN-2936W is compatible with both types of Hall effect IC (pull-up resistors are needed for open collector digital Hall effect ICs).

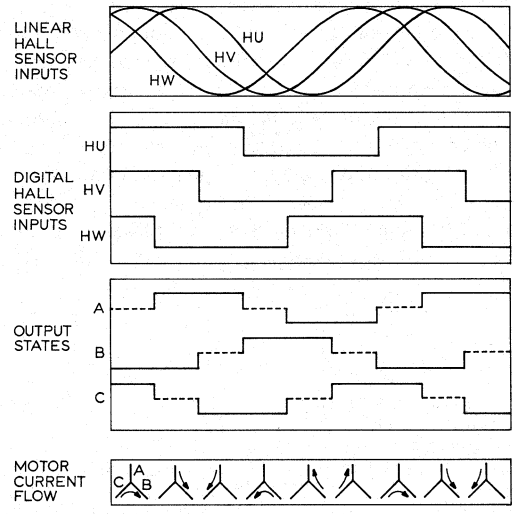


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Figure 1

Position of the Hall effect sensors determines the decoding sequence to produce the correct driving waveforms for each motor. The decoding sequence programmed into this device is based on Hall effect cells 60 electrical degrees apart. This 60 degree se-

quence is one of the most common used in the industry. The truth table and timing waveforms found in Figure 1 illustrate how the Hall cell inputs, driving output waveforms, and motor currents states are interrelated. Motors with other commutation sequences can typically be accommodated by inverting one of the position inputs.

Chopping Current Control

The current limit technique chops the source drivers to control the load current level. The maximum current and percentage ripple, or hysteresis, can be programmed by the user or left to internal default values. Source chopping produces a continuous sense voltage (see Figure 2), so this voltage is an accurate representation of load current, even during recirculation. Also, chopping only the sources produces a fast current charge-up and a slower current decay. This occurs because of the different voltages across the coil in both states, and results in a controllable current waveform. The chopping method functions as follows: When the current reaches Ilim, the source is disabled and the current recirculates through a sink driver and clamp diode. The motor current decays a fixed percentage, the source is enabled again, and the cycle repeats. The internal sense voltage comparator has a limited bandwidth that essentially filters out noise on the sense pin to prevent erroneous chopping.

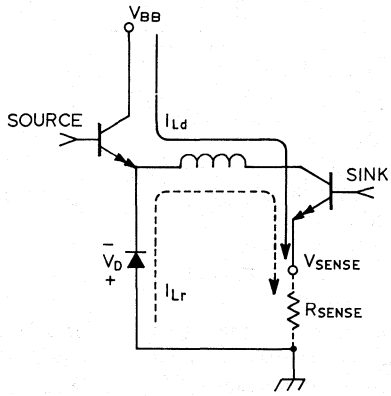


Figure 2

The limiting current level and hysteresis are determined by the user or left to internal defaults. Figure 3 illustrates these values in a typical output current waveform. A voltage divider on the V_{ref} pin sets the external V_{ref}. If set above 2.5 V, the internal V_{ref} is used. Whether V_{ref} is set internally or externally, $V_{ref}/10$ is the limiting threshold on V_{sense}. The default limiting can be programmed by:

$$Ilim = \frac{.25\ V}{R_{sense}}$$

Default hysteresis is set at 7.5%. For a V_{ref} <2.5 V, the limiting threshold is the following:

$$Ilim = \frac{V_{ref}}{10*R_{sense}}$$

In this case, hysteresis is created by drawing 200 µA from the resistor divider when the sources are chopped, lowering the limiting threshold a certain percentage. The sources turn back on when the sense voltage decays to the new lower threshold. Hysteresis is given by this expression:

$$\%hys = \frac{100*(200\ \mu A * R2)}{V_{pk}}$$

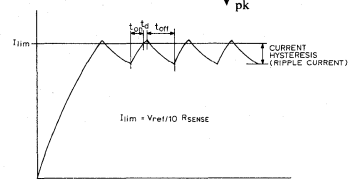


Figure 3A

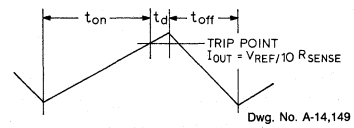


Figure 3B

The hysteresis current source, V_{ref} voltage divider, and current limiting equations can be found in Figure 4. The tables in Figure 5 aid in selecting values for R1 and R2.

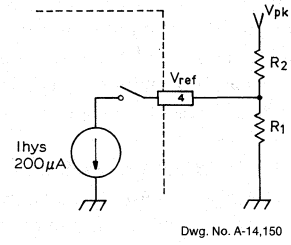
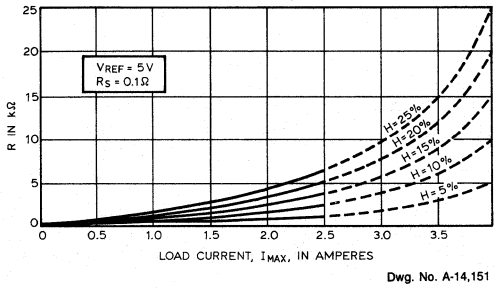


Figure 4

The internal and external current limit settings can be used together to start a motor with a high regulated current, and run it at a lower regulated current. To do this, V_{ref} must be tied above 2.5 V when the motor starts, and the V_{ref} divider switched in after start-up (see Figure 6).



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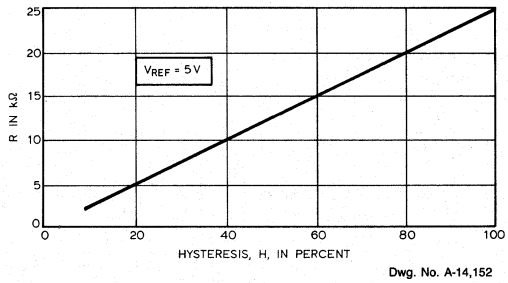

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Figure 5

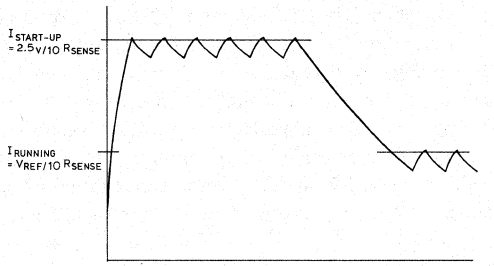

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Figure 6

Outputs

The output section consists of three half-bridges capable of sourcing or sinking 2 A continuously at a saturation voltage of less than 2 V per driver. They are built to sustain at least 50 V. Source and sink clamp diodes are included to provide a current path during commutation and chopping. These are high-performance substrate isolated diodes that virtually eliminate the wasteful parasitic substrate currents of conventional diodes. The drivers, both source and sink, are bipolar double level metal Darlingtons.

Direction and Braking

The direction control allows the motor to be reversed even while running. When direction changes polarity, the state of the outputs is reversed, i.e., if the source was ON, the sink will turn ON, and vice versa. Because the turn off times are longer than the turn on times, the drivers turning ON must be delayed by a precise amount to prevent potentially destructive crossover currents. This delay is generated internally.

The brake function uses the back EMF of the motor to brake it dynamically. The windings are effectively "shorted" together through sink drivers and clamp diodes.

Thermal Shutdown and Power Dissipation

The thermal shutdown feature protects the IC from overheating. This circuit turns OFF all drivers at about 165° C, and allows the device to cool down approximately 25° before turning ON again.

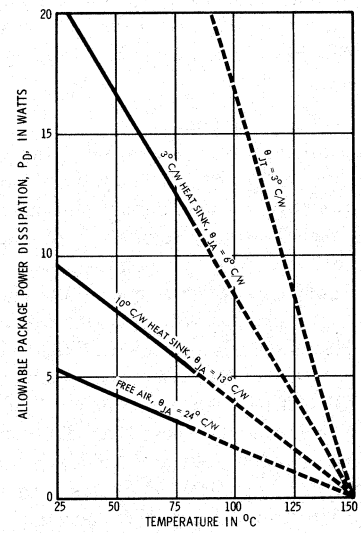


Figure 7

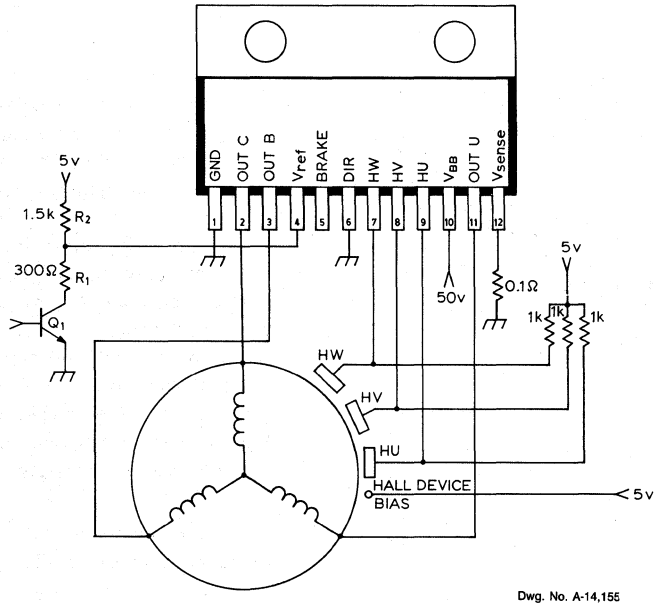


Figure 8

The device is packaged in a 12 pin power SIP that has a large copper tab for excellent heat dissipation. The design of the tab, and the fact that it is at ground, make the package easy to use with a heat sink. The maximum allowable power dissipation in 25°C ambient air without a heat sink is 5.2 W. With minimal heat sinking, dissipation greater than 10 W can be accomplished. See Figure 7 for more information on power ratings.

Application

The application shown in Figure 8 is a simple one illustrating the use of the UDN-2936W in an open loop situation with bi-level current limiting. The motor uses digital open collector Hall cells such as the Sprague UGN-3013T, so pull-up resistors are required. Three 1 kΩ resistors pull up the Hall IC outputs to a 5 V supply, the same one needed to power the Hall effect ICs themselves. If the motor is equipped with linear Hall effect ICs, such as the Sprague UGN-3503U, then there is no need for pull-up resistors on the inputs. These Hall effect sensors have a quiescent output voltage of 2.5 V, and emitter follower outputs. The UDN-2936W has a regulated internal 2.5 V reference designed to make the inputs compatible with those linear Hall effect sensors. The 5 V supply is also used as a reference in the current limiting for the V_{ref} resistor divider. Choosing R_{sense} = 0.1 ohm results in internal default limiting current of 2.5 A, and 7.5% ripple. This internal limiting is active when Q1 is off. R1 and R2 form a resistor divider, when Q1 is on, to apply 1 V to the V_{ref} input, producing 1 A of regulated running current and 5% ripple. Typically, Q1 would be off during start-up, giving 2.5 A of regulated start-up current, and then turned on to provide 1 A of running current. The values of R1, R2, and V_{sense} can be calculated using the circuit and equations of Figure 5, or the tables of Figure 6.

The motor speed is controlled by the current limiting. For a given load, speed is proportional to torque, and torque is proportional to motor current. Subsequently, the motor speed can be controlled through V_{ref}.

Conclusion

Smart power integrated circuits have come a long way in the past few years in solving numerous motor driving problems. The UDN-2936W is one example of how integrated monolithic devices can replace a drive circuit of many components with one reliable component. Also evident is the fact that bipolar transistors continue to provide economic solutions in the high current application.

POWER OP AMP APPLICATIONS

Sprague monolithic power operational amplifiers meet many high-current design challenges. The Series ULN-3750 high-gain, high-current operational amplifiers are used in power-driver applications such as servo-positioning systems (e.g., voice-coil motors for disk drives), dc motors, single-phase and multiphase motor-drive circuits, linear regulators, and in many other applications that, in the past, have required power buffers driven by conventional operational amplifiers.

Linear motor drivers will inherently produce lower electrical noise levels than their fast-switching digital counterparts. Linear position servos usually achieve substantially higher resolution and are capable of faster response than digitally controlled stepper motors. Series ULN-3750 offers increased output-voltage swing and high output-current drive, high gain as well as unity-gain stability and the capability to sense load currents without need of the usual level-shifting or sense circuitry.

The operational amplifiers in this family of ICs provide peak push-pull output currents as high as ±3.5 A, making them suitable for applications in which both current sourcing and current sinking are needed. As illustrated in the examples that follow, some of the op amps allow a very high output swing. They also provide overload and thermal protection under a variety of fault conditions.

Attention to thermal design in IC layout has minimized temperature-induced degradation of parameters while maximizing output-power capability. Single power op amp drivers are furnished in power-tab TO-220 packages (ULN-3751*Z*). Dual units are supplied in 12-pin single in-line packages (ULN-3753*W* and ULN-3755*W*) and in low-cost standard DIPs with heat-sink tabs (Series ULN-3750*B*).

SERIES ULN-3750 POWER OP AMPS

Device	Type	Peak Current Output	Short-Circuit Protection	Thermal Protect	Boost Voltage	Compensation	Functional Supply Span	Package
ULN-3751Z	Single	3.5 A	–	Yes	–	Internal	6 V to 30 V	5-Pin TO-220 Power-Tab SIP
ULN-3753W	Dual	3.5 A	Yes	Yes	–	External	6 V to 40 V	12-Pin Power-Tab SIP
ULN-3753B	Dual	3.5 A	Yes	Yes	–	External	6 V to 40 V	16-Pin Batwing DIP
ULN-3755W	Dual	3.5 A	Yes	Yes	Yes	Internal	6 V to 40 V	12-Pin Power-Tab SIP
ULN-3755B	Dual	3.5 A	Yes	Yes	Yes	Internal	6 V to 40 V	16-Pin Batwing DIP

Some of the material appearing in this application note, is taken from an article that appeared in the August 22, 1985 issue of EDN magazine

BRUTE FORCE AND SMALL SIGNALS

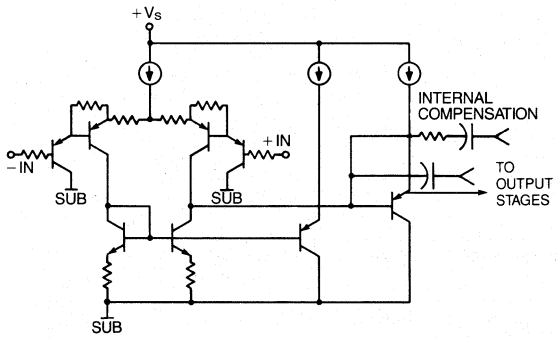
Both classical small-signal op amps and brute-force boosters must possess two attributes: they must have true differential (inverting and noninverting) inputs. Second, to minimize errors and drifts in closed-loop configurations, they must have high open-loop gain. Frosting-on-the-cake includes low offset voltage and drift, unity-gain stability, high output swing, large common-mode input range, high common-mode rejection, short-circuit protection, and a thermal-shutdown feature.

Sprague Series ULN-3750 offers all these features, and more. Consider the input section. The circuit is a classic op amp input stage found, for example, in many operational amplifiers with little power-handling capacity. The use of PNP input transistors allows the application of input voltages ranging from about 0.5 V below ground to approximately three base-emitter drops below the positive supply voltage. The ability to use ground-level input voltages is an important consideration. It allows the op amp to be easily operated from a single supply, where the input source is often referenced to ground.

The two capacitors shown in the input-circuit schematic provide compensation with adequate phase-gain margins to allow operation for closed-loop gains as low as 1. Note the graph of the amplifier's gain and phase characteristics as functions of frequency (noninverting test circuit, A_V = 1000). It exhibits a smooth, 6 dB per octave rolloff to frequencies as high as 1 MHz, and an approximate 20° phase margin at unity gain.

In the amplifier's output stage, the output transistors are completely protected from inductive kickback voltages by clamping diodes built into the chip. The clamp diodes are capable of handling currents equal to the rated capacity of the output sink/source transistors. The output transistors are connected in a quasi-complementary configuration. The lower sink transistor can provide output voltages as low as ground plus one saturation drop. The current-sense terminals can be used to impart a transconductance characteristic to the amplifier, or simply to provide a separate power output ground and minimize output-to-input feedback through a common ground resistance.

INPUT STAGE



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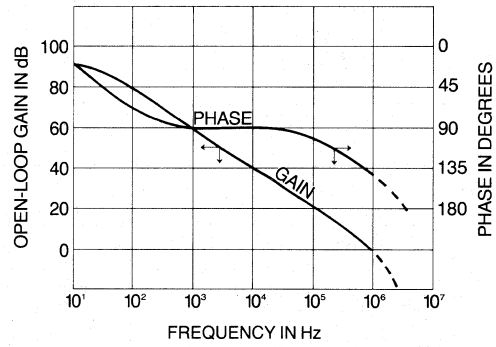
GAIN AND PHASE CHARACTERISTICS



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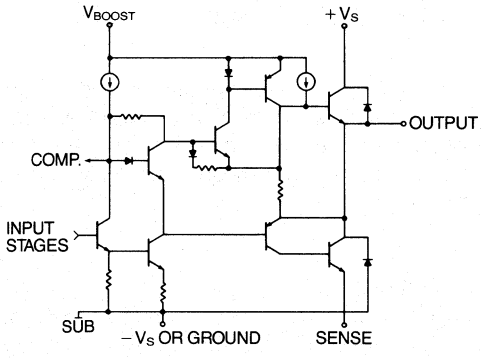
OUTPUT STAGE



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BOOST TO BOOTSTRAP

The boost terminal is a unique feature of the ULN-3755B and ULN-3755W. It increases the amplifier's available output-voltage swing by 1 V to 2 V, depending on output current, by allowing the upper source transistor to saturate (an impossibility with the usual emitter-follower lacking the boost feature). To take advantage of the boost capability, use a boost-terminal voltage that is about 3 V higher than the positive load supply voltage. The boost function allows the amplifier to be bootstrapped in ac applications by its own output or by another ac output.

The specifications shown below for the ULN-3755W apply to operation with ±6 V supplies, at an ambient temperature of +25°C. Not shown are the amplifier's absolute maximum ratings: 40 V supply span, ±3.5 A peak repetitive current, and 20 W allowable package power dissipation (with 3°C/W heat sink and +25°C ambient).

The Series ULN-3750 currently is comprised of six types. Considering allowable package power dissipation ratings, continuous output currents to ±1 A are recommended for the 16-pin batwing DIPs (suffix "B"). Applications with ratings to ±2.5 A require the TO-220 or 12-pin single in-line power tab packages (suffix "Z" and "W" respectively). All 5 types provide thermal shutdown at high junction temperatures. All are unity-gain stable. Pin count essentially dictates the features available with the various units. For example, the dual amplifiers lacking the boost capability (ULN-3753B/W) offer compensation pins for tailoring the operational amplifiers' frequency characteristics to specific applications. The single ULN-3751Z provides neither boost nor compensation options, due to the 5-pin limitation, but is unity-gain stable.

4

ULN-3755W DUAL POWER OP AMP

TYPICAL ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions*	Typical Value
Quiescent Current, $+I_S$	No Load	70 mA
I_{BOOST}	V_{BOOST} = 9 V, No Load	7.0 mA
Input Offset Voltage	V_{OUT} = 0 V, No Load	2.0 mV
Input Bias Current	V_{OUT} = 0 V	80 nA
Input Offset Current	V_{OUT} = 0 V, No Load	10 nA
Open-Loop D-C Gain	f = 0 Hz	100 dB
Slew Rate	V_{IN} = 0.2 V Step	1.0 V/μs
Output Swing	V_{BOOST} = 6 V, I_{OUT} = ±1 A	9.5 Vpp
	V_{BOOST} = 9 V, I_{OUT} = ±1 A	10.5 Vpp
Power-Supply Rejection	Either Supply	80 dB
Common-Mode Rejection		85 dB

*T_A = +25°C, $T_{TAB} \leq$ +70°C, $+V_S = V_{BOOST}$ = +6 V, $-V_S$ = −6 V (unless otherwise specified).

CAREFUL THERMAL DESIGN WRINGS WATTS FROM ICs

Power ICs are now capable of delivering tens of watts of power. It is easy to obtain such power from an IC when the device is mounted in a metal can with low thermal resistance. Moreover, it is easy to provide heat sinking for such a package. Metal packages, however, are expensive. The challenge is to develop inexpensive plastic packaging that also provides a way to keep junction temperatures at a safe level.

What's a safe level? At the moment, the prevailing industry standard for maximum junction temperature is +150°C. However, using any temperature as a reference, an IC's expected lifetime roughly doubles for every 10°C reduction in junction temperature. Note, too, that such circuit parameters as leakage current suffer significant degradation at high temperatures.

The most widely accepted IC package is the dual in-line package (DIP). Without special enhancements, though, the standard DIP is woefully inefficient for thermal transfer. The package itself provides a junction-to-ambient thermal resistance as high as 125°C/W. This figure assumes the use of a Kovar lead frame and, since the lead frame is the main carrier of heat from the IC to the outside world, changing the material to copper reduces the thermal resistance to about 60°C/W. All Sprague power operational amplifiers have copper lead frames and heat sinks.

Limiting the junction temperature to +150°C, the 60°C/W figure allows a worst-case (still air) package power dissipation of 1.33 W at +70°C. Unfortunately, this power figure is still inadequate for many modern power applications.

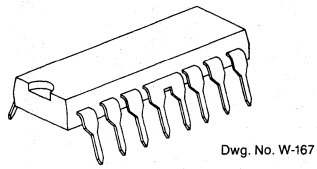
HIGH-POWER SIPs

For high-power applications, power ICs use single in-line packages similar to the TO-220, universally used for power transistors. The 5-pin ULN-3751Z uses such a package. Its maximum junction-to-tab thermal resistance is 4.0°C/W. The ULN-3755W dual power op amp is housed in a similar, but wider, package. Exhibiting 3°C/W maximum junction-to-tab thermal resistance, the IC can dissipate as much as 26 W at a tab temperature of +70°C.

ISOTHERMAL DESIGN CUTS GRADIENTS

Chip temperatures inevitably rise in high-power applications. Even with ideal packaging, the thermal resistance of the silicon chip itself will result in a temperature gradient across the chip. In linear circuits such as these op amps, the worst effects can arise from unequal heating on the chip's surface.

It is important to position input transistors as far as possible from the heat-generating output devices. What is less obvious is the need to arrange the high-



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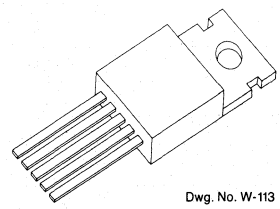
16 - PIN BATWING 'B' PACKAGE



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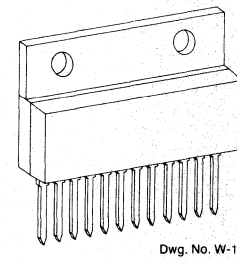
5 - PIN TO-220 'Z' PACKAGE



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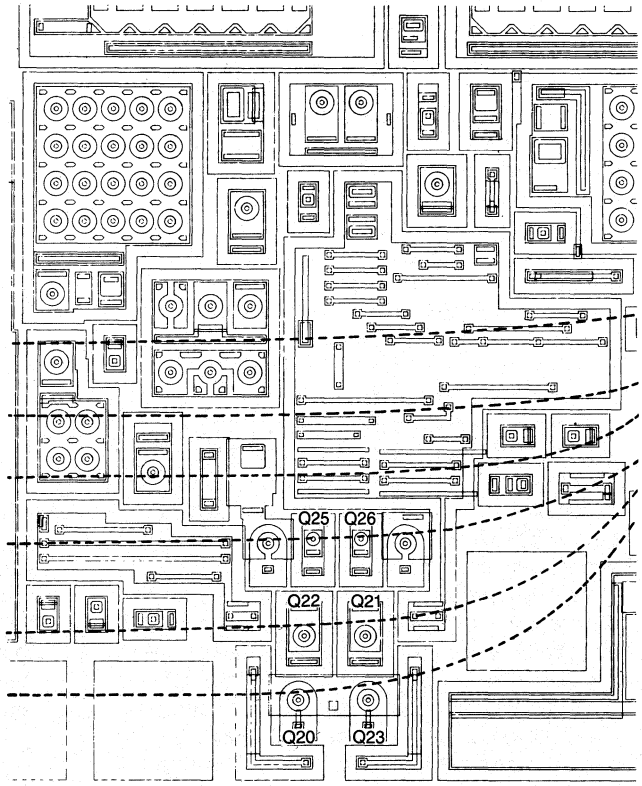
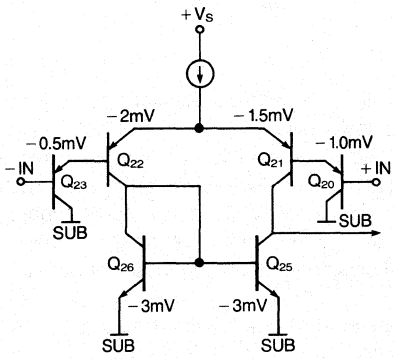
12 - PIN SINGLE IN-LINE 'W' PACKAGE

ISOTHERMAL DESIGN



Dwg. No. W-168

CHANGES IN V_{BE} WITH TEMPERATURE



Dwg. No. W-118

gain input stages so as to minimize the effects of any temperature differences between them. For example, unequal junction temperatures in the amplifier's input transistors can cause large offset-voltage and offset-current shifts.

As shown in the chip drawing and schematic, cross-coupling of the input stages cancels differences in the low-level transistors' junction temperatures. It is also necessary to lay out the stage's associated resistors to minimize temperature gradients. In this case, all input-stage resistors are arranged in the same epitaxial tub (and in the same direction) to ensure that all resistors are equally affected by the unavoidable heating.

A CASE STUDY

Note the isothermal lines shown in the chip drawing. Q_{25} and Q_{26} are at equal temperatures; these two current-mirror transistors must have the same base-emitter voltages. It's a different story, however, for Q_{21} and Q_{22}. They lie farther away from the power section, and layout considerations have made it impossible to keep them at equal temperatures. The same problem also exists for Q_{20} and Q_{23}. For the purposes of illustration, assume that a dissipation-induced temperature rise causes the base-emitter voltage of Q_{25} and Q_{26} to drop by 3 mV. Transistor Q_{22} is slightly cooler and suffers a V_{BE} decrease of 2 mV while the comparable Q_{21} drop is only 1.5 mV. Finally, Q_{20} and Q_{23} exhibit V_{BE} changes of 1 mV and 0.5 mV, respectively. As a result of thermal cross-coupling, the V_{BE} reductions from either input can be matched at 2.5 mV. The base-emitter voltage variations as a function of temperature thus cancel out. Without this cross-coupling, the total change in base-emitter voltage would be 3 mV for the left input stage and 2 mV for the right input stage.

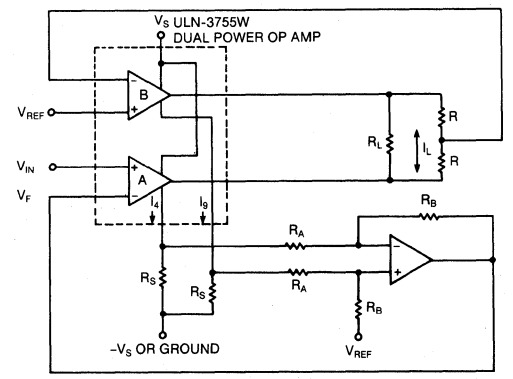
CURRENT-SENSE TRANSCONDUCTANCE

The op amps' current-sense terminals can be used to derive a transconductance function. This function is commonly used in motor control applications such as voice-coil servo or microstepping positioning systems found in many computer disk drives. The drawing at right shows the ULN-3755W dual amplifier connected as a transconductance amplifier. In this example, amplifier B is used as a slave to amplifier A. Feedback from the pair of current-sensing resistors, R_S, in the emitters of the output's current-sinking transistors is applied to the summing network and scaled to the inverting input of amplifier A, where it is compared to the input voltage.

The voltage developed across the sensing resistors is directly proportional to the output current. Using this voltage as a feedback source defines the gain of the circuit as output current in amperes as a function of the input voltage in volts. The gain thus assumes the dimensions of a transconductance function (output current divided by input voltage), expressed in siemens (formerly mhos).

Conventional monolithic power op amps can be made to operate in similar configurations where the current-sensing resistor(s) are inserted in the ground (or negative supply) return. However, that configuration is not recommended, since both the amplifier's signal and bias currents now flow through the output current sensing resistor(s), causing the high-gain signal ground to float. Operating in this mode can cause problems with stability and common-mode rejection, as well as reducing the input common-mode range. The dual power op amps in the Series ULN-3750, however, provide open-emitter outputs that can be used to sense current without degradation of the input characteristics of the high-gain stages.

The graphs below illustrate the bidirectional nature of output load current (and the same current divided between the two output sink returns).



Dwg. No. W-119

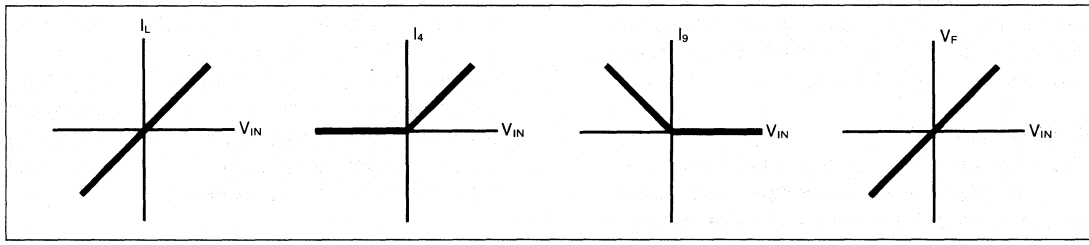
TRANSCONDUCTANCE AMPLIFIER

$I_4 - I_9 = I_L$. The external network sums and amplifies (scales) the voltages developed across the current-sensing resistors. The resulting feedback voltage (V_F) is a scaled, level-shifted version of the load current. It is possible, in certain applications, to combine this network with the input-feedback network and eliminate the small-signal operational amplifier.

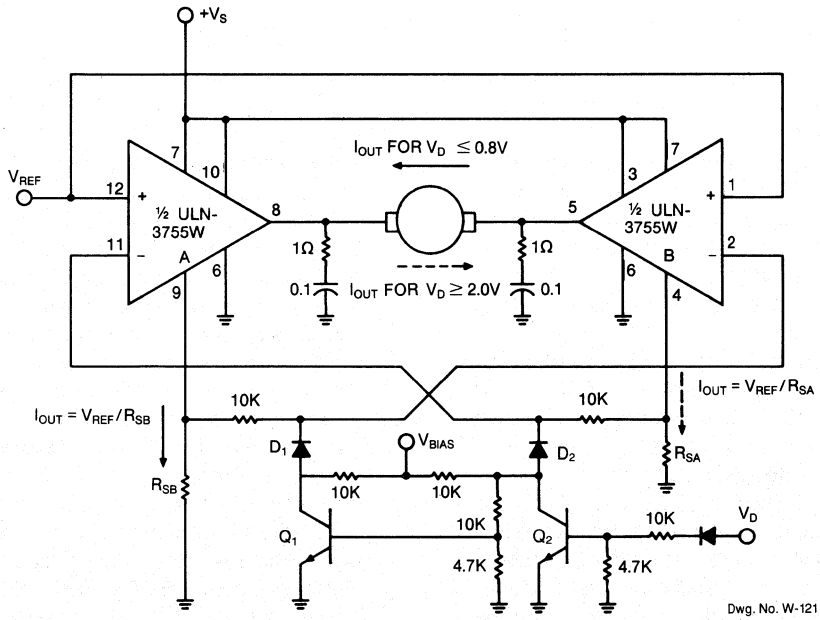
The negative feedback forces the amplifier to adjust the output current to attain a value such that the feedback voltage equals the applied input voltage. The transfer function of the transconductance amplifier is approximately:

$$I_L/(V_{IN} - V_{REF}) = R_A/(R_B R_S)$$

Resistors R_A, R_B, and R_S define the transconductance gain. To avoid limiting the transconductance amplifier's output compliance (swing capability), low-value current-sensing resistors (R_S) should be used. The product of peak output current and sensing resistance should be kept to as low a value as possible.



Dwg. No. W-120



BIDIRECTIONAL CURRENT CONTROLLER

There are many applications requiring constant current sources that can be controlled both in magnitude and direction. Examples of this requirement are found in some brushless dc motor drives as well as in numerous industrial process control systems. Both open-loop and closed-loop feedback systems are used depending on the specific requirements to be met. In any case, there exists a voltage directly proportional to the desired output current and a control signal or switch whose state determines direction.

The circuit above is a bidirectional transconductance amplifier. A voltage, proportional to the desired current, is applied to both non-inverting inputs of a ULN-3755W, which is connected in a bridge configuration. Current feedback is obtained from current-sense resistors (R_{SA} and R_{SB}). The voltage developed across the current-sense resistor is directly proportional to the load current. This sense voltage is applied to the inverting inputs of the amplifiers, as shown, to provide negative feedback. The output will adjust until the feedback voltage is equal to the programmed input voltage. This can be expanded to a switched selector network or the output of a servo-control loop.

The direction of the load current is controlled by a positive bias voltage applied to either of the inverting inputs. V_D represents the digital direction-control voltage. When V_D is low, Q_2 is OFF, allowing D_2 to conduct, driving pin 11 high. This causes the output of amplifier A to be driven low. Q_1, meanwhile, is ON, clamping the anode of D_1 to ground (or to the saturation voltage of Q_1). This results in D_1 being held OFF and allowing active feedback to pin 2 of amplifier B. Amplifier B will then source current into the load with amplifier A acting as a current sink. By raising V_D to a high level, the output of amplifier B will go low, with amplifier A acting as the controlled current source. Resistor values are non-critical except to ensure that the inverting input of the switched amplifier is held above the programming voltage (V_{REF}) applied to its non-inverting input. As shown, control voltage V_D is TTL compatible.

If V_D is the output of a pulse generator, this application will produce a time-dependent current reversal. This meets the requirements found, for example, in a typical industrial process control application where a current is passed through a pair of electrodes immersed in a conducting fluid. Alternatively, Q_2 and its drive can be replaced by a latching Hall Effect switch, such as the Sprague UGN-3075U, for use in brushless dc motor applications where current is controlled by R_S.

DIGITALLY CONTROLLED POSITION SERVO

In a position-control application, a microprocessor is often used to control a servomotor's shaft angle or to control position, as in a computer disk drive. Below is a typical discrete semiconductor circuit implementation of that concept. The basic configuration is a classic one, using two low-power operational amplifiers, many discrete passive components, and four PNP and NPN power transistors connected in a push-pull, H-bridge configuration.

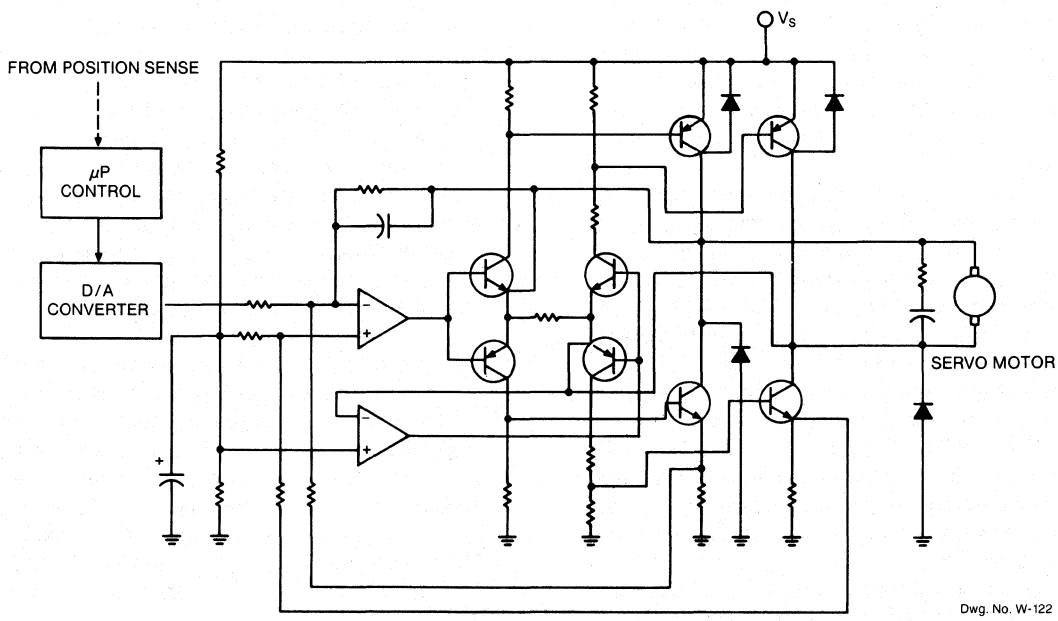
The circuit consists of small-signal input operational amplifiers and power output stages. The circuit derives its input from the D/A converter, whose output is determined by a code from the controlling microprocessor and related digital-control circuitry.

The analog equivalent of this servo-control circuit might use a multi-turn potentiometer to produce a voltage proportional to the servomotor's position. In any event, the sensed position signal normally undergoes processing and comparison with the desired position, through a digitally-based microprocessor system (or its analog equivalent) that produces an error signal to control the servo amplifier's output.

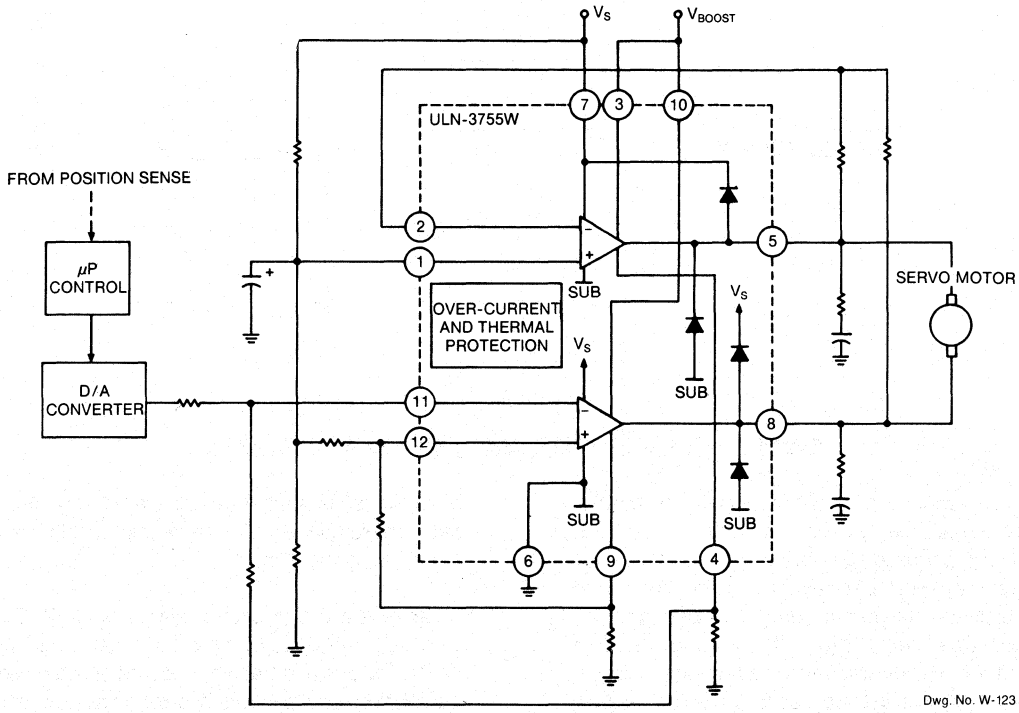
A circuit that uses far fewer components to accomplish the same position-control function is constructed around the ULN-3755W integrated circuit. In addition to the original functions, the circuit now includes thermal and short-circuit protection, as well as component matching and thermal tracking inherent to monolithic construction. The ULN-3755W dual power operational amplifier has its two independent outputs connected in a push-pull, H-bridge configuration. An 8-bit D/A converter yields a resolution of 256 shaft positions in discrete steps of 1.41°. A higher resolution converter would, of course, provide finer control. Because of its push-pull arrangement, the circuit provides bidirectional servo control.

The overall resolution of the system is a function of the position-sensing element, whether a digitally encoded disk or an analog potentiometer, and the digital control circuitry, including the microprocessor and the A/D converter. The ULN-3755W dual operational amplifier combines the small-signal summing amplifiers, predrivers, and the output H-bridge. The IC's outputs also include clamping diodes with current-handling capacity equal to that of the output drivers.

DISCRETE CIRCUIT IMPLEMENTATION



DIGITALLY CONTROLLED POSITION SERVO — INTEGRATED CIRCUIT IMPLEMENTATION



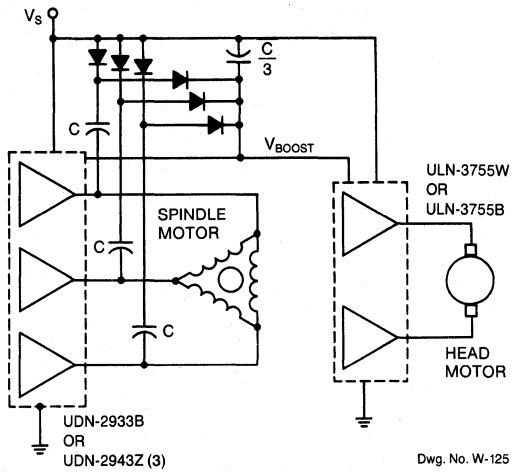
The current-sense pins (4 and 9) provide access to the emitters of the H-bridge current sinks, thereby providing convenient output-current sensing to ground (or to the negative rail), while allowing separate low-current signal ground returns. This feature helps to prevent undesirable feedback to the input stage, a common problem with conventional approaches to output-current sense.

If a voltage higher than the supply is applied to the ULN-3755W boost pins, the positive output swing is limited only by the saturation resistance of the output transistors (typically less than 0.5Ω). For example, with a 12 V supply, the circuit typically supplies a 10.5 Vpp output swing at 1 A output current. This figure is at least 1 V higher than can be expected from ICs lacking the boost capability. Note that the externally supplied boost voltage should be at least 3 V higher than the load supply voltage. This criterion satisfied, the boost voltage can be any value within the IC's 40 V absolute-maximum rating. The circuit shown will deliver continuous output currents of up to ±2.5 A and peak output currents as high as ±3.5 A.

The user must be aware that although the voltage or current limits shown are well within the IC's capabilities, the resultant power dissipation must be kept within the constraints of the overall (chip + package + heat sink) thermal rating. This rating is principally dependent on the package chosen and the amount of heat sinking provided by the user.

The boost feature provides important additional output voltage swing at the amplifier's full rated current. However, the IC's boost input requires only a low, unregulated current of 25 mA, maximum. Thanks to this modest current requirement, the boost voltage can be obtained from such compact sources as inexpensive, modular dc to dc converters. Or, in a head-positioning application in a disk drive, for example, a simple overwinding in the spindle motor (or a voltage doubler using the motor's driven phases) can easily generate such a voltage.

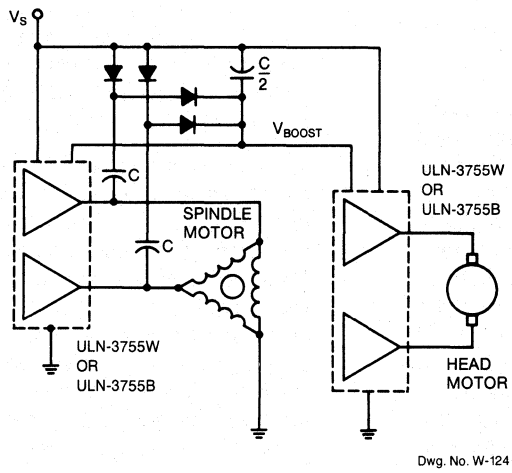
VOLTAGE-DOUBLER BOOST SUPPLY



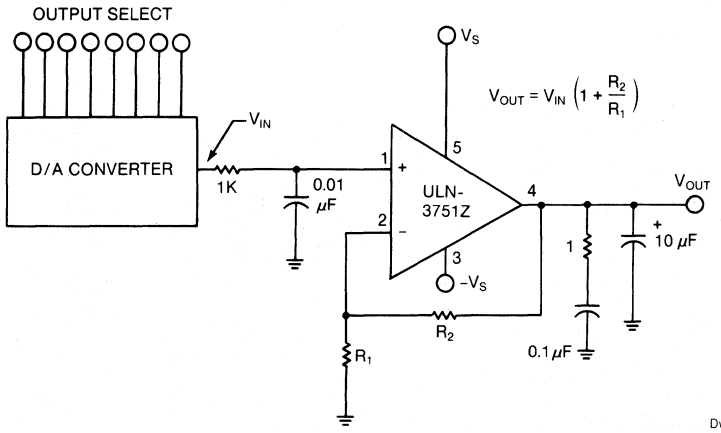
SIMPLE VOLTAGE DOUBLERS FOR OP AMP BOOST

An example of a simple-to-implement voltage-doubler boost supply is shown above. This circuit affects the doubling by connecting a series diode-capacitor network between the main supply and each of the spindle motor's driven phases. A three-diode bridge then charges the voltage-doubling capacitor to nearly twice the main supply voltage. Note that connecting the capacitor to the main supply (instead of to ground) effectively reduces rms ripple in the main supply by injecting its charge current into the supply mains concurrently with the spindle's opposing drive currents. Although, in theory, only one motor phase is needed to generate the boost, the three-phase connection is recommended to prevent unbalancing the spindle.

Below is a similar circuit using a ULN-3755W to provide linear drive to a delta-connected spindle motor. The use of linear drive instead of pulse-width-modulation results in much lower noise with only a slight reduction in efficiency. Because fast PWM transitions in the circuit above result in motor losses, the efficiency compromise of the linear configuration is not as significant as might be expected.



VOLTAGE-DOUBLER BOOST SUPPLY WITH LINEAR DRIVE

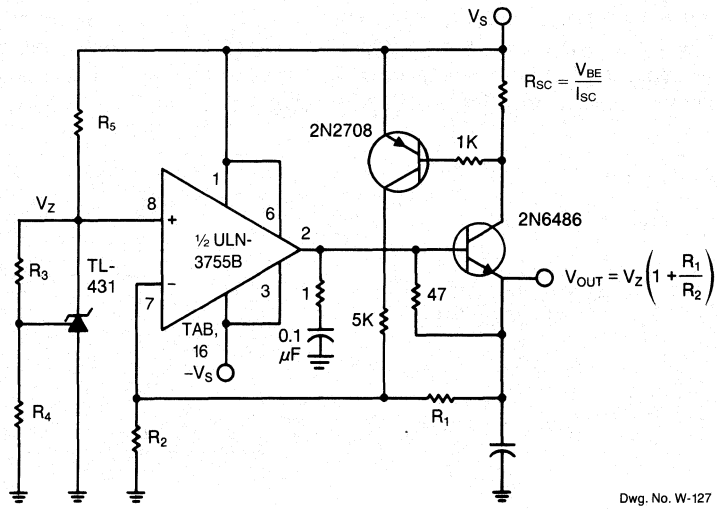


POSITIVE-OUTPUT PROGRAMMABLE REGULATOR

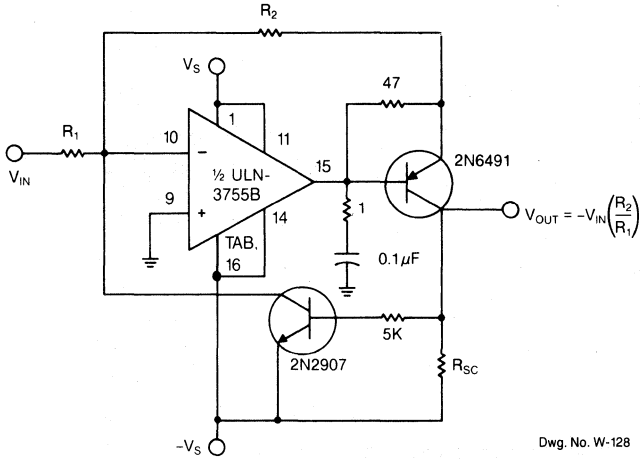
HIGH-CURRENT REGULATORS

The high current-output capability of the operational amplifiers in Series ULN-3750 makes them suitable for use in linear voltage regulators. The amplifiers' high open-loop gain and low offset voltage ensure high load regulation and accuracy. Consider, for example, the positive-output, programmable regulator above. The circuit provides output currents as high as ±3.5 A peak. Unlike most monolithic regulators, the ULN-3751Z is equally effective as a sink or a source. Therefore, the circuit maintains regulation for active loads that present reversing load currents. Note that the circuit easily handles transitions from high to low output voltages, thanks to the crowbar effect of the output's sinking capability. The input reference is the output of a D/A converter, providing programmability. An 8-bit D/A, for example, provides for 256 steps of output resolution.

For higher output currents (but without the sink capability) the addition of an external power transistor (below) provides outputs as high as the NPN power transistor's safe operating area allows. This circuit is shown using a voltage reference such as the popular three-terminal TL431. The voltage V_Z is determined by the ratio of resistors R_3 and R_4, while R_5 provides bias current. The circuit can, of course, be programmed by substituting the D/A reference above. The amplifier's output voltage is a function of the ratios of R_1 and R_2. The PNP transistor provides short-circuit (I_{SC}) current limiting according to the expression shown.



POSITIVE OUTPUT REGULATOR WITH SHORT-CIRCUIT LIMITING



Dwg. No. W-128

HIGH-CURRENT NEGATIVE OUTPUT REGULATOR

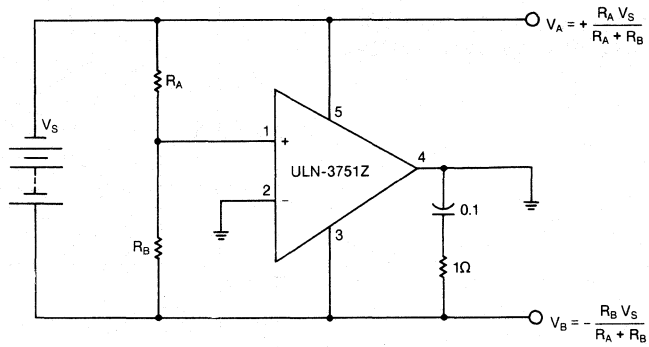
HIGH-CURRENT REGULATORS (Continued)

To configure a high-current, dual-output supply, the mirror-image circuit shown at top can be used. Simply connect this stage's input to the D/A converter or voltage reference output. The combination of this circuit and the positive output regulator on the previous page provides an accurately tracking pair of positive and negative supplies from a common reference, whether a programmable D/A converter or the simple resistor-programmed TL431. Both circuits use the ULN-3755B with external high-current pass transistors. The external devices are unnecessary if output-current loading is less than 2.5 A.

The previously described boost capability can be used to good advantage in these regulator circuits. Applying a low-current boost voltage at least 3 V higher than the load supply voltage results in a regulator with less than 1 V input-output differential, (dependent on output current) yielding high efficiency from the main supply. The 0.1 Ω/0.1 μF network at the amplifier's output provides local compensation for the output stage.

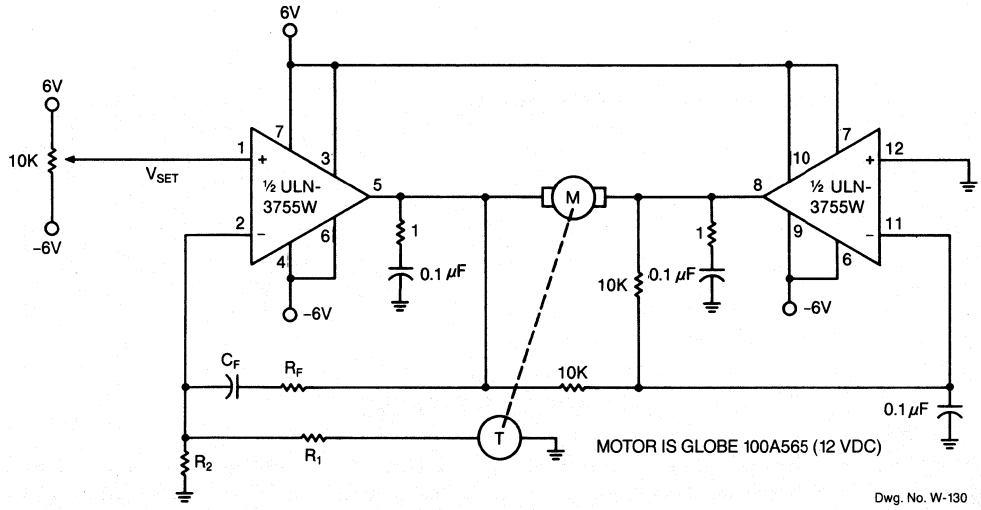
A simple split supply can also be developed using a single ULN-3751Z power op amp to generate an artificial ground, as shown below. By taking advantage of the device's four-quadrant sink/source drive capability, the outputs will ratio (rather than track) over a wide range of supply voltages and unequal load currents. *Total* load current is unrestricted, provided the *difference* in load currents is less than the maximum rated current of the power op amp. In addition, the allowable package power dissipation rating must be greater than the product of the amplifier's sourcing current ($I_A < I_B$) and the source driver voltage (V_A) or the sinking current ($I_A > I_B$) and the sink driver voltage (V_B). This circuit is also very useful in tracking supplies to enhance common-mode supply rejection.

ARTIFICIAL GROUND / SPLIT SUPPLY



Dwg. No. W-129

DC MOTOR SPEED CONTROL



Dwg. No. W-130

ICs CONTROL MOTOR SPEED

Power op amps can be used to provide accurate speed control for dc motors. The drawing above shows a closed-loop system for controlling the speed of a 12 V dc motor. The circuit provides bidirectional speed control. The amplifiers' push-pull configuration ensures a full rail-to-rail voltage swing (minus the output stages' saturation drops) across the motor in either direction.

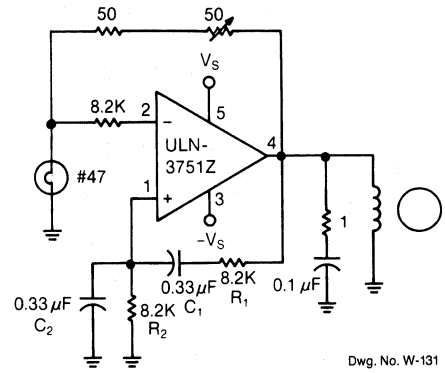
The circuit uses a mechanically-coupled tachometer to provide speed-stabilizing feedback to the first amplifier section. The motor's speed and direction of rotation is set by adjusting the 10 kΩ potentiometer at the amplifier's noninverting input.

The motor speed, in rpm, is:

$$S = V_{SET}(R_1 + R_2)/0.0027\,R_2$$

The R_FC_F feedback network prevents oscillation by compensating for the inherent dynamic mechanical lag of the motor. Select the R_FC_F time constant to match the particular motor's characteristics. By consulting with individual motor data sheets, the R_F and C_F values can be chosen to match the motor response or dynamic time constant. This should yield a good starting point for stabilizing the system. Optimal response is achieved by varying the compensating capacitor.

SINGLE-PHASE AC MOTOR DRIVER



Dwg. No. W-131

N-PHASE MOTOR DRIVE

Its high amplification factor and its built-in power-output stage make the integrated power operational amplifier a convenient driver for single-phase or multiphase ac motors. The high gain allows one op amp to be configured as an oscillator to generate the required ac signal. The power-output stage, of course, supplies the high-current drive to the motor.

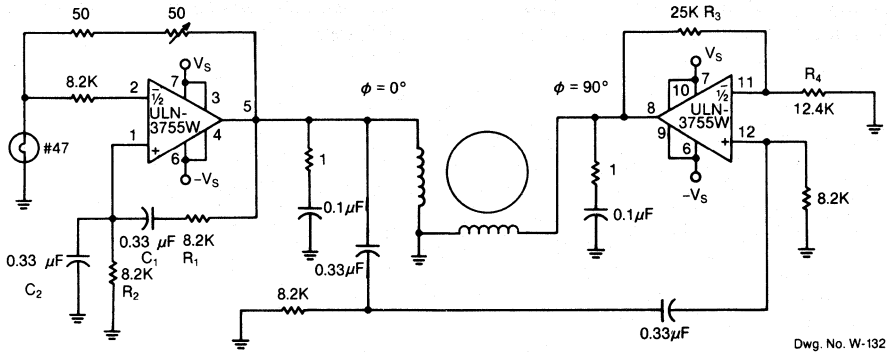
Consider, for example, the three motor-drive circuits shown here. The circuit above is a single-phase driver that uses the ULN-3751Z single power op amp. The other circuits use the ULN-3755W dual amplifier to drive two-phase and three-phase motors. Note that in all three circuits, the controlling op amp is configured as a Wein-bridge power oscillator. The R_1C_1 and R_2C_2 feedback networks determine the oscillation frequency according to the expression:

$$f_o = 1/(2\pi\sqrt{R_1R_2C_1C_2})$$

By varying either R_1 or R_2, the oscillator frequency can be adjusted over a narrow range.

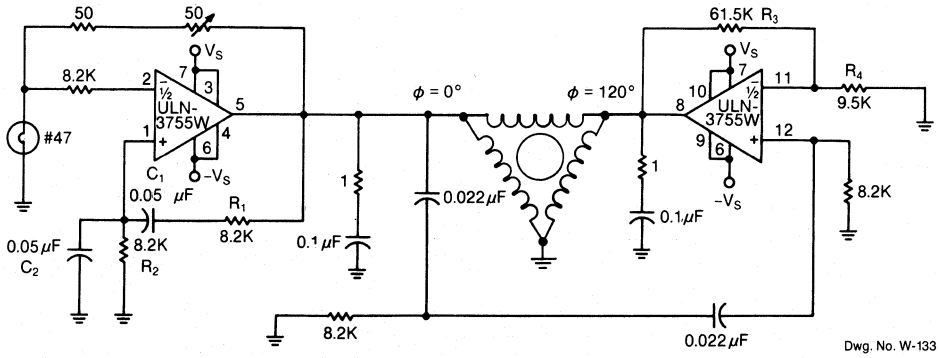
In the single-phase and two-phase examples, the oscillation frequency is 60 Hz. In the three-phase example, the frequency is 400 Hz. The Type 47 incandescent light bulb in the oscillator circuits serve to stabilize the amplifier's output amplitude. The bulb owes its stabilization qualities to its intrinsic positive

TWO-PHASE AC MOTOR DRIVER



Dwg. No. W-132

THREE-PHASE AC MOTOR DRIVER



temperature coefficient. If the amplifier's output level attempts to increase, the corresponding increase in lamp current causes a temperature rise in the filament. The heating, in turn, results in an increase in filament resistance, producing increased negative feedback and a reduction in amplifier gain. A PTC (positive temperature coefficient) resistor could be used instead of the lamp. To set the output amplitude, adjust the 50 Ω potentiometer in the feedback network.

To drive multiphase motors, it's a relatively simple matter to add another stage to the single-phase circuit. In the 60 Hz, two-phase drive, the 8.2 kΩ/0.33 μF networks provide both the 60 Hz oscillator frequency and the 90° phase shift needed by the right-hand amplifier. The 8.2 kΩ/0.005 μF networks in the three-phase drive set the 400 Hz oscillator frequency, while the 8.2 kΩ/0.022 μF networks provide the required 120° of phase shift. The motor shown is a three-phase delta-connected motor with one input grounded and the remaining inputs driven from the 0° and 120° phase-shifted amplifier outputs. The result is a balanced three-phase a-c drive.

In both the two-phase and three-phase circuits, the R_3/R_4 ratio sets the second amplifier's gain to compensate for signal attenuation occurring in the phase shifters. Again, pins 3 and 10 can be returned to a boost supply to obtain additional output-swing capability.

The three circuits can all be driven from an external source, such as a pulse or square wave output of a digital source, setting the gain of the left-hand amplifier to a level less than that required for oscillation. The RC feedback networks then function as active filters, causing the outputs to be sinusoidal.

UNIVERSAL BUILDING BLOCKS

Power operational amplifiers provide a fundamental set of universal building blocks incorporating the merged equivalent of small-signal operational amplifiers, pre-drivers, output amplifiers and various protective features such as output clamp diodes, thermal shutdown, and output-current limiting. An output-boost capability can provide for high output-voltage swing, while an output-current-sensing scheme prevents unwanted interaction between the outputs and inputs. Many applications that previously required individual low-level and high-level components can now be implemented with a single integrated circuit and few external components.

NOTES

SECTION 5—BiMOS SMART POWER INTERFACE DRIVERS

SELECTION GUIDE

Description	I_{OUT}	V_{OUT}	Device Type	Page
SERIAL-INPUT, LATCHED DRIVERS				
4-Bit	1.75 A	60 V†	UCN-5825B	5-59
4-Bit	1.75 A	80 V†	UCN-5826B	5-59
4-Bit	−2.0 A	80 V	UCN-5896W	*
8-Bit Saturated Drivers	−120 mA	50 V†	UCN-5895A	5-119
8-Bit	350 mA	50 V	UCN-5821A	5-55
8-Bit	350 mA	50 V†	UCN-5841A	5-82
8-Bit	−350 mA	50 V†	UCN-5891A/B	5-113
8-Bit	350 mA	80 V	UCN-5822A	5-55
8-Bit	350 mA	80 V†	UCN-5842A	5-82
8-Bit	−350 mA	80 V†	UCN-5890A/B	5-113
8-Bit	350 mA	100 V	UCN-5823A	
8-Bit	350 mA	100 V†	UCN-5843A	5-82
10-Bit	−25 mA	60 V	UCN-5810A	5-33
10-Bit	−25 mA	80 V	UCN-5810A-1	5-33
10-Bit	±40 mA	150 V	UCN-5910A	5-130
12-Bit	−25 mA	60 V	UCN-5811A	5-37
20-Bit	−25 mA	60 V	UCN-5812A	5-33
20-Bit	−25 mA	80 V	UCN-5811A-1	5-37
20-Bit	−25 mA	80 V	UCN-5812A-1	5-33
32-Bit TFEL Column Drivers	±15 mA	60 V	UCN-5855/56EP	*
32-Bit (no latches) AC Plasma Disp. Drive	±15 mA	100 V	UCN-5858/60A/EP	5-105
32-Bit	−25 mA	60 V	UCN-5818A	5-33
32-Bit	−25 mA	60 V	UCN-5818AF/EPF	5-51
32-Bit	−25 mA	80 V	UCN-5818A-1	5-33
32-Bit	−25 mA	80 V	UCN-5818AF/EPF-1	5-51
32-Bit TFEL Column Drivers	±20 mA	60 V	UCN-5853/54A/EP	5-95
32-Bit TFEL Column Drivers	±20 mA	80 V	UCN-5853/54A/EP-1	5-95
32-Bit	100 mA	30 V	UCN-5833A/EP	5-74
32-Bit Saturated Drivers	100 mA	30 V	UCN-5834A/EP	*
32-Bit Saturated Drivers	100 mA	40 V	UCN-5832A	5-65
32-Bit Saturated Drivers	100 mA	40 V	UCN-5832EP	5-71
32-Bit (no latches) TFEL Row Drivers	100 mA	225 V	UCN-5851/52A/EP	5-87
64-Bit	50 mA	40 V	UCN-5864C	*
PARALLEL-INPUT, LATCHED DRIVERS				
4-Bit	350 mA	50 V†	UCN-5800A	5-23
4-Bit	350 mA	150 V†	UCN-5900A	5-124
4-Bit	1.25 A	50 V†	UCN-5813/14B	5-41
4-Bit	1.25 A	80 V†	UCN-5813/14B-1	5-41
8-Bit	−25 mA	60 V	UCN-5815A	5-46
8-Bit	−25 mA	80 V	UCN-5815A-1	5-46
8-Bit	350 mA	50 V†	UCN-5801A	5-23
8-Bit	350 mA	150 V†	UCN-5901A	5-124
2 x 8-Bit (with readback)	25 mA	20 V†	UCN-5881EP	5-107
2 x 8-Bit (with readback)	−25 mA	20 V†	UCN-5882EP	5-110
SPECIAL-PURPOSE FUNCTIONS				
Stepper-Motor Translator/Driver	600 mA	20 V†	UCN-4202A	5-3
Stepper-Motor Translator/Driver	600 mA	50 V†	UCN-4203A	5-3
Stepper-Motor Translator/Driver	1.25 A	20 V†	UCN-4204B	5-10
Stepper-Motor Translator/Driver	1.0 A	30 V†	UCN-4205B-2	5-10
Stepper-Motor Translator/Driver	1.25 A	50 V	UCN-5804B	5-28
Latched 7-Segment Decoder/Driver	−40 mA	60 V	UCN-4805A	5-13
Addressable, Latched Octal Drivers	200 mA	40 V	UCN-4807A	5-17
Addressable, Latched Octal Drivers	600 mA	40 V	UCN-4808A	5-17
Addressable, Latched Hexadecimal Drivers	350 mA	60 V†	UCN-5816A	5-49
8 of 32-Bit AC Plasma Display Drivers	±15 mA	100 V	UCN-5857/59A/EP	5-103

Current ratings shown are maximum tested condition; voltage ratings are maximum allowable.
†Internal transient-suppression diodes included for inductive-load protection.
*New product, contact factory for information.

UCN-4202A AND UCN-4203A STEPPER-MOTOR TRANSLATORS AND DRIVERS

FEATURES

- 600 mA Output Current
- Full-Step or Double-Step Operation
- Single-Input Direction Control
- Power-On Reset
- Internal Transient Suppression
- Schmitt Trigger Inputs

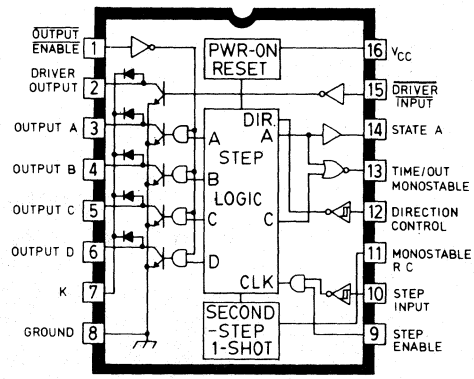
DESIGNED TO DRIVE permanent-magnet stepper motors with current ratings of up to 500 mA, these integrated circuits employ a full-step, double-pulse drive scheme that allows use of up to 90 percent of available motor torque. The two devices differ only in output-voltage ratings: Type UCN-4202A has a 20 V breakdown-voltage rating and a 15 V sustaining voltage rating; Type UCN-4203A has a 50 V breakdown-voltage rating and a 35 V sustaining voltage rating.

Both drivers are bipolar I^2L designs containing approximately 100 logic gates, TTL-compatible input/output circuitry, and 600 mA outputs with internal transient suppressors. The devices operate with a minimum of external components.

The four-phase stepper-motor load is controlled by step-logic functions. To step the load from one position to the next, STEP INPUT is pulled down to a logic low for at least 1 μs, then allowed to return to a logic high. The step logic is activated on the positive-going edge, which in turn activates one of the four current-sink outputs. DIRECTION CONTROL determines the sequence of states (A-B-C-D or A-D-C-B).

In the full-step mode, the MONOSTABLE RC timing pin is tied to V_{CC}, making states B and D stationary. A separate input pulse is required to move through each of the four output states.

In the double-step mode, states B and D are transition states with duration determined by MONOSTABLE RC timing. Improved motor torque is obtained at double the nominal motor step angle, and motor stability is improved for high step rates.



DWG. NO. A-11,184

Higher current ratings, or bipolar operation, can be obtained by using Type UCN-4202A or UCN-4203A as a logic translator to drive integrated motor drivers (Sprague UDN-2950Z, UDN-2953B, or UDN-2954W) or discrete high-power transistors.

5

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

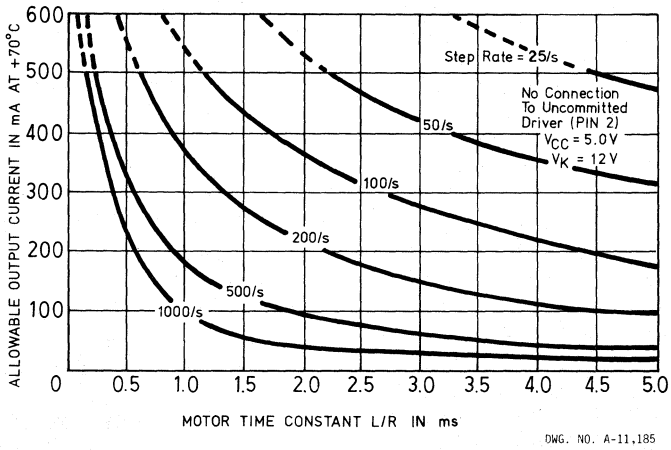
Supply Voltage, V_{CC}	7.0 V
V_K (UCN-4202A)	20 V
(UCN-4203A)	50 V
Output Voltage, V_{OUT} (UCN-4202A)	20 V
(UCN-4203A)	50 V
Input Voltage, V_{IN}	7.0 V
Output Sink Current, I_{OUT}	600 mA
Power Dissipation, P_D (One Driver)	0.8 W
(Total Package)	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 16.6 mW/°C above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristic	UCN-4202A			UCN-4203A			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage, V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
V_K	—	12	13.5	—	30	35	V
Output Voltage, V_{CE}	—	—	13.5	—	—	35	V
Output Sink Current, I_{OUT}	—	—	500	—	—	500	mA
Operating Temperature, T_A	0	25	70	0	25	70	°C

MAXIMUM COLLECTOR CURRENT AS A FUNCTION OF MOTOR TIME CONSTANT



Notes: 1. Values shown take into account static d-c losses ($V_{SAT}I_{OUT}$ and $V_{CC}I_{CC}$) as well as switching losses induced by inductive flyback through the clamp diodes at V_K = 12 V. Maximum package power dissipation is assumed to be 1.33 W at +70°C. Higher package power dissipation may be obtained at lower operating temperatures.

2. Use of external discrete flyback diodes will eliminate power dissipation resulting from switching losses and will allow the full 500 mA output capability (Output A, B, C, or D and the Driver Output) under all conditions.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +5.0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Supply Current	I_{CC}	All	2 Drivers ON	—	85	mA
TTL Inputs (Pins 1, 9, and 15), TTL Outputs (Pins 13 and 14)						
Input Voltage	$V_{IN(1)}$	All	$V_{CC} = 4.5$ V	2.0	—	V
	$V_{IN(0)}$	All	$V_{CC} = 5.5$ V	—	0.8	V
Input Current	$I_{IN(1)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 2.4$ V	—	40	μA
	$I_{IN(0)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V	—	−1.6	mA
Input Clamp Voltage	V_{IK}	All	$I_{IN} = -12$ mA	—	−1.5	V
Output Voltage	$V_{OUT(1)}$	All	$V_{CC} = 4.5$ V, $I_{OUT} = 80$ μA	2.4	—	V
	$V_{OUT(0)}$	UCN-4202A	$V_{CC} = 4.5$ V, $I_{OUT} = 3.2$ mA	—	0.4	V
		UCN-4203A	$V_{CC} = 4.5$ V, $I_{OUT} = 1.5$ mA	—	0.4	V
Output Current	$I_{OUT(SC)}$	All	$V_{CC} = 5.5$ V, $V_{OUT} = 0$	—	38	mA
Second-Step Monostable RC Input (Pin 11)						
Time Constant	t_{RC}	All		0.95	1.3	s/RC
Reset Voltage	V_{MR}	All	R = 200 kΩ, $I_{IN} = 25$ μA	—	50	mV
Reset Current	I_{MR}	All	$V_{IN} = 2.0$ V	40	—	μA
Schmitt Trigger Inputs (Pins 10 and 12)						
Threshold Voltage	V_{T+}	All		1.3	2.1	V
	V_{T-}	All		0.6	1.1	V
Hysteresis	ΔV_T	All		0.2	—	V
Input Current	$I_{IN(1)}$	All	$V_{CC} = 4.5$ V, $V_{IN} = 2.4$ V, $T_A = 25°C$	—	5.0	μA
		All	$V_{CC} = 4.5$ V, $V_{IN} = 2.4$ V, $T_A = 70°C$	—	40	μA
	$I_{IN(0)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V	—	−1.6	mA
Input Clamp Voltage	V_{IK}	All	$I_{IN} = -12$ mA	—	−1.5	V
Open Collector Outputs (Pins 2, 3, 4, 5, and 6)						
Output Leakage Current	I_{CEX}	UCN-4202A	$V_{CC} = 5.5$ V, K = Open, $V_{OUT} = 20$ V	—	500	μA
		UCN-4203A	$V_{CC} = 5.5$ V, K = Open, $V_{OUT} = 50$ V	—	500	μA
Output Saturation Voltage	$V_{CE(SAT)}$	UCN-4202A	$V_{CC} = 4.5$ V, $I_{OUT} = 300$ mA	—	500	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 400$ mA	—	750	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 500$ mA	—	900	mV
		UCN-4203A	$V_{CC} = 4.5$ V, $I_{OUT} = 300$ mA	—	850	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 400$ mA	—	1100	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 500$ mA	—	1350	mV
Output Sustaining Voltage	$V_{CE(SUS)}$	UCN-4202A	$I_{OUT} = 30$ mA, $t_p \leq 300$ μs, Duty Cycle ≤ 2%	15	—	V
		UCN-4203A	$I_{OUT} = 30$ mA, $t_p \leq 300$ μs, Duty Cycle ≤ 2%	35	—	V
Turn-On Delay	t_{pd0}	All	0.5 E_{in} (Pin 10) to 0.5 E_{out}	—	10	μs
Turn-Off Delay	t_{pd1}	All	0.5 E_{in} (Pin 10) to 0.5 E_{out}	—	10	μs
Clamp Diode Leakage Current	I_R	UCN-4202A	$V_R = 20$ V	—	50	μA
		UCN-4203A	$V_R = 50$ V	—	50	μA
Clamp Diode Forward Voltage	V_F	All	$I_F = 500$ mA	—	3.0	V

5

FUNCTIONAL DESCRIPTION

Power-On Reset

An internal RS flip-flop sets the Output A "ON" with the initial application of power. This state occurs approximately 30 μs after the logic supply voltage reaches 4 V with supply rise times of up to 10 ms/V. Once reset, the circuit functions according to the logic input conditions.

Step Enable

Pin 9 (STEP ENABLE) must be held high to enable the step pulses for advancing the motor to reach the translator logic clock circuits. Pulling this pin low inhibits the translator logic.

Step Input

Pin 10 (STEP INPUT) is normally high. The logic will advance one position on the positive transition after the input has been pulled low for at least 1 μs. The STEP INPUT current specification is compatible with NMOS and CMOS.

Direction Control

The direction of output rotation is determined by the logic level at pin 12. If the input is held high the rotation is A-D-C-B; if pulled low the rotation is A-B-C-D. This input is also NMOS and CMOS compatible.

Output Enable

Outputs A through D are inhibited (all outputs OFF) when pin 1 (OUTPUT ENABLE) is at high level. This condition creates a potential for wired-OR device outputs, or other potential control functions such as chopping or bi-level drive.

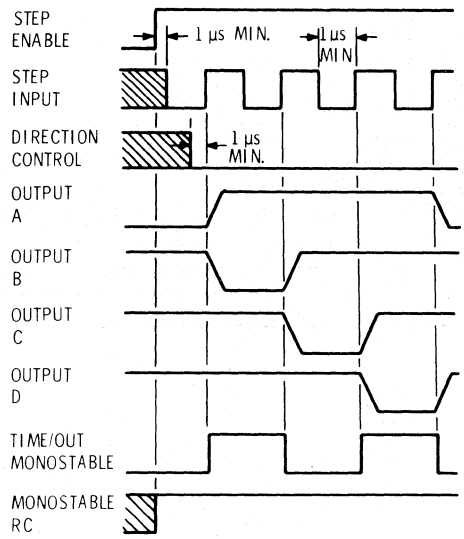
Transient Suppression

All five power outputs are diode protected against inductive transients. Zener diode or resistor "flyback" transient suppression is often used, provided the peak output voltage does not exceed the sustaining voltage rating of the device (15 V for Type UCN-4202A or 35 V for Type UCN-4203A).

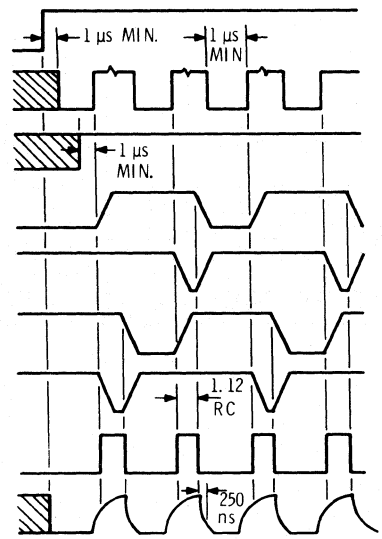
Full-Step/Double-Step

Full-step operation is the most commonly used drive technique. The devices are capable of unipolar drive without external active devices, either in a full-step mode (pin 11, Monostable RC, tied high), or in a double-step mode (pin 11 connected to RC timing). The double-step mode provides improved torque characteristics, while the specified angular increment is doubled.

FULL-STEP MODE



DOUBLE-STEP MODE



Dwg. No. A-11,844

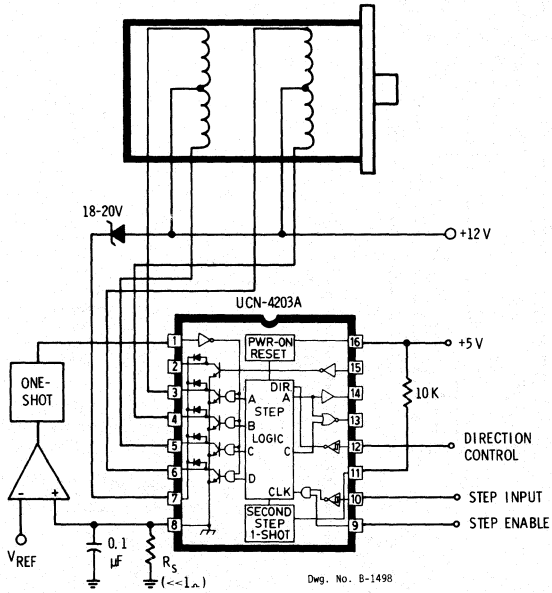
STEPPER MOTORS

(Representative List)

Manufacturer	Model	L/R	Typ. Ratings	Step
Eastern Air Devices	LA23ACK-2	1.4 ms	440 mA, 12 V	1.8°
	LA23ACK-3	1.25 ms	220 mA, 24 V	1.8°
	LA23ACY-1	1.2 ms	440 mA, 12 V	7.5°
	LA34ADK-6	2.6 ms	530 mA, 14 V	1.8°
IMC Hanson	S-114	1.6 ms	340 mA, 12 V	7.5°
	S-115	1.9 ms	130 mA, 12 V	7.5°
	S-382	1.6 ms	171 mA, 24 V	7.5°
	S-406	4.3 ms	280 mA, 24 V	15°
	S-451	3.9 ms	280 mA, 24 V	7.5°
North American Phillips	K82701-P2	1.5 ms	330 mA, 12 V	7.5°
	K83701-P2	1.5 ms	330 mA, 12 V	15°
Septor	S-0912A	1.5 ms	340 mA, 12 V	9°
Superior Electric	M061-FD-301	0.8 ms	440 mA, 12 V	1.8°
	M061-FD-311	1.5 ms	220 mA, 20 V	1.8°

TYPICAL APPLICATIONS

CHOPPER DRIVE CIRCUIT
Used to Drive a 12 V, 500 mA
Unipolar Stepper Motor



DISC DRIVE APPLICATIONS

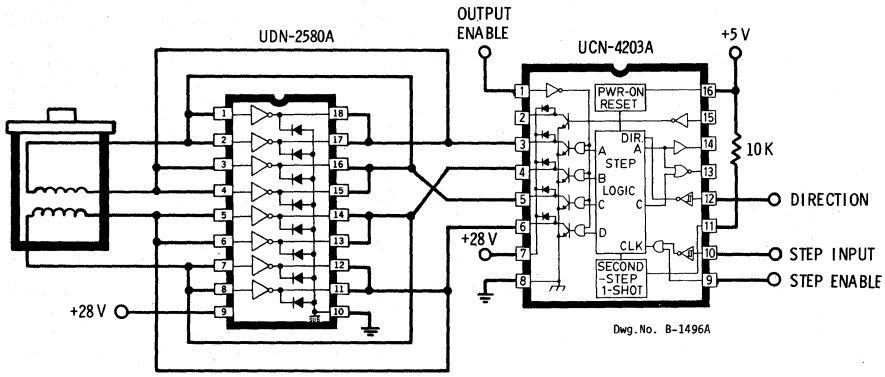
These stepper-motor translator/drivers provide additional special-purpose logic for use in disc drive applications. Pin 14 (STATE A) is high with OUTPUT A activated and is used with other drive logic in determining Track 0 Position on the disc. Pin 13 (TIME/OUT MONOSTABLE) in disc drive applications is called $\overline{\text{ON TRACK}}$ and is low with either OUTPUT A or OUTPUT C activated. It is used as a WRITE ENABLE condition with other drive logic.

An independent driver (pins 2 and 15) is used to control the head load solenoid.

TYPICAL APPLICATIONS

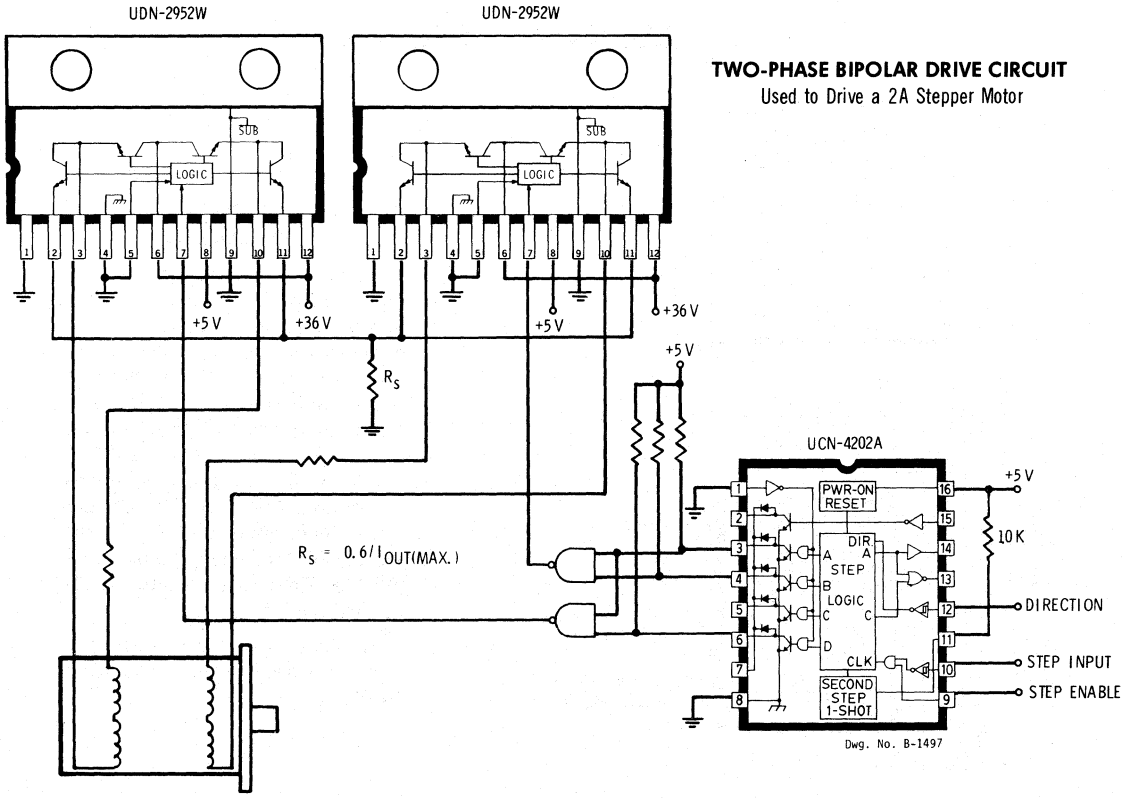
BIPOLAR DRIVE CIRCUIT

Used to Drive a 500 mA Stepper Motor



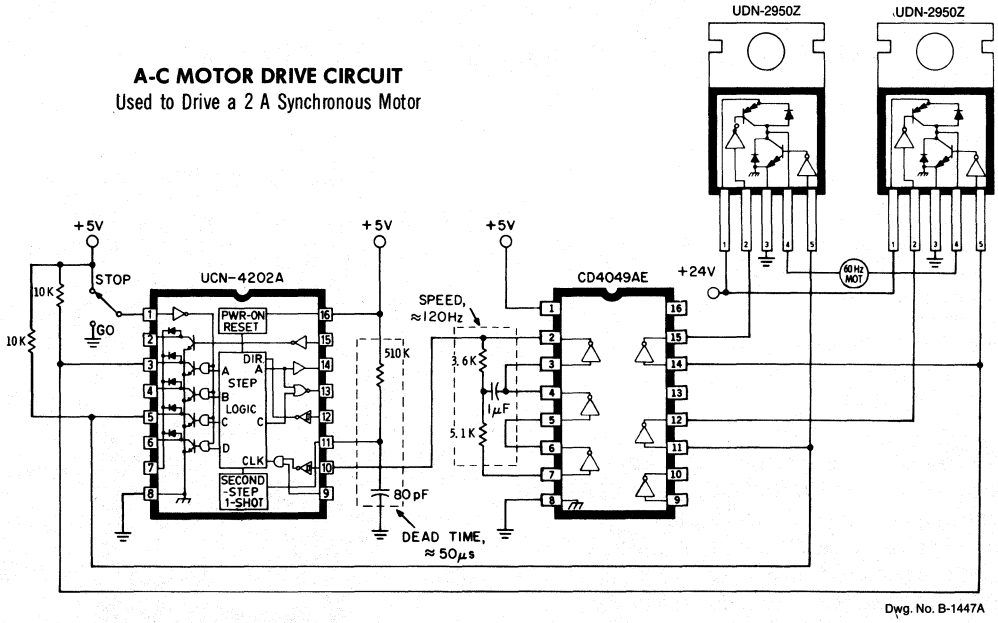
TWO-PHASE BIPOLAR DRIVE CIRCUIT

Used to Drive a 2A Stepper Motor



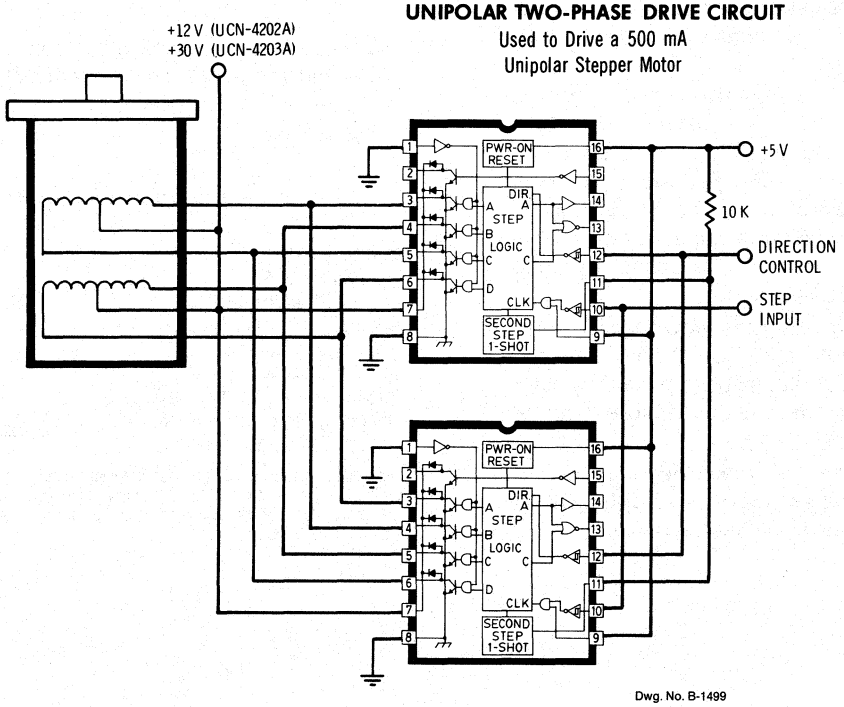
TYPICAL APPLICATIONS

A-C MOTOR DRIVE CIRCUIT
Used to Drive a 2 A Synchronous Motor



Dwg. No. B-1447A

UNIPOLAR TWO-PHASE DRIVE CIRCUIT
Used to Drive a 500 mA
Unipolar Stepper Motor



Dwg. No. B-1499

5

UCN-4204B AND UCN-4205B-2
STEPPER-MOTOR TRANSLATORS/DRIVERS

FEATURES

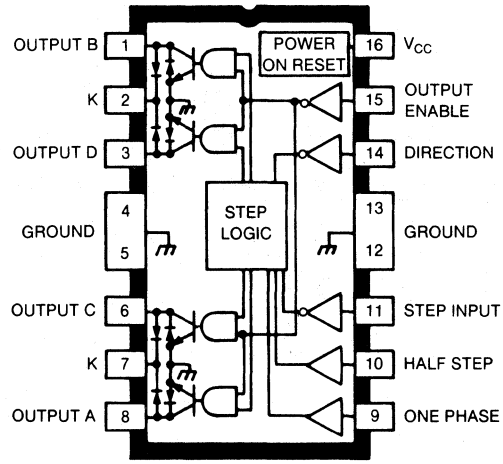
- 1.5 A Max. Output Current
- Wave Drive, Two-Phase, and Half-Step
- Internal Clamp Diodes
- Output Enable
- Internal Thermal Shutdown
- Power-ON Reset

Providing control and direct drive to unipolar four-phase stepper motors, UCN-4204B and UCN-4205B-2 integrated circuits are rated up to 1.5 A per phase and will sustain inductive loads to 15 V or 25 V, respectively. In other respects, the UCN-4204B and UCN-4205B-2 are identical. Both devices feature on-chip I^2L logic to provide direction and OUTPUT ENABLE control functions, thermal shutdown, and power-ON reset, as well as externally selectable one-phase (wave drive), two-phase, and half-step drive formats.

The one-phase or wave-drive format consists of energizing one motor phase at a time in an A-B-C-D (or D-C-B-A) sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding imbalance in the motor. Devices with 500 mA output current ratings, using this drive format, are available as Sprague UCN-4202A and UCN-4203A.

Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This mode offers an improved torque-speed product, greater detent torque, and is less susceptible to motor resonance.

Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD-D-DA), providing an eight-step sequence.



Dwg. No. W-109

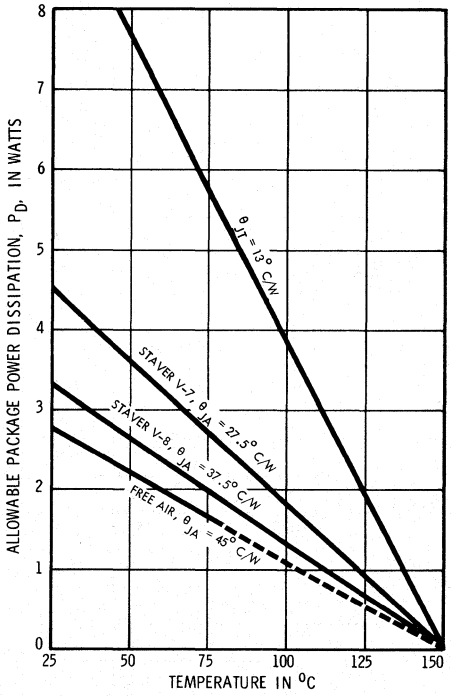
Both devices are supplied in 16-pin dual in-line plastic batwing packages with heat-sinkable tabs and copper lead frames for improved thermal characteristics.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

Output Voltage, V_{CE}
(UCN-4204B) ..... 20 V
(UCN-4205B-2) ..... 30 V
Output Sink Current, I_{OUT} ..... 1.5 A
Logic Supply Voltage, V_{CC} ..... 7.0 V
Input Voltage, V_{IN} ..... 7.0 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A .... $-20°C$ to $+85°C$
Storage Temperature Range, T_S .... $-55°C$ to $+150°C$

Output current rating will be limited by ambient temperature, heat sinking, air flow, duty cycle, and number of outputs conducting. Under any set of conditions, do not exceed a 1.5 A peak output current or a junction temperature of $+150°C$.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11, 793A

WAVE-DRIVE SEQUENCE

↓DIRECTION = L	Half Step = L, One Phase = H				→DIRECTION = H
Step	A	B	C	D	
POR	ON	OFF	OFF	OFF	
1	ON	OFF	OFF	OFF	
2	OFF	ON	OFF	OFF	
3	OFF	OFF	ON	OFF	
4	OFF	OFF	OFF	ON	

TWO-PHASE DRIVE SEQUENCE

↓DIRECTION = L	Half Step = L, One Phase = L				→DIRECTION = H
Step	A	B	C	D	
POR	ON	OFF	OFF	ON	
1	ON	OFF	OFF	ON	
2	ON	ON	OFF	OFF	
3	OFF	ON	ON	OFF	
4	OFF	OFF	ON	ON	

HALF-STEP DRIVE SEQUENCE

↓DIRECTION = L	Half Step = H, One Phase = L				→DIRECTION = H
Step	A	B	C	D	
POR	ON	OFF	OFF	OFF	
1	ON	OFF	OFF	OFF	
2	ON	ON	OFF	OFF	
3	OFF	ON	OFF	OFF	
4	OFF	ON	ON	OFF	
5	OFF	OFF	ON	OFF	
6	OFF	OFF	ON	ON	
7	OFF	OFF	OFF	ON	
8	ON	OFF	OFF	ON	

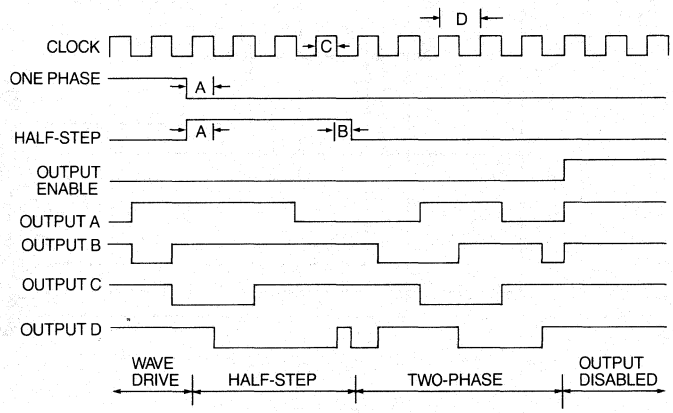
TRUTH TABLE

	PIN 9	PIN 10
TWO-PHASE	L	L
ONE-PHASE	H	L
HALF-STEP	L	H
STEP-INHIBIT	H	H

TIMING CONDITIONS

A. Minimum data set-up time ..... 1 μs
B. Minimum data hold time ..... 1 μs
C. Minimum data pulse width ..... 1 μs
D. Minimum clock period ..... 200 μs

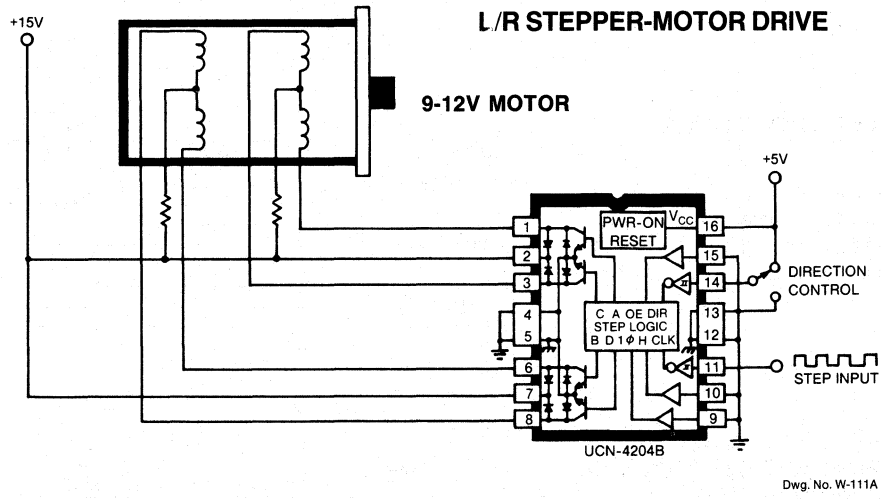
Note: Clock must be in low state when changing state of ONE PHASE, HALF-STEP, or DIRECTION or unwanted stepping may occur.



Dwg. No. W-110

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_{CC} = 5\,V$

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	UCN-4204B	$V_{CC} = 5.5\,V$, K = Open, $V_{OUT} = 20\,V$	—	50	µA
		UCN-4205B-2	$V_{CC} = 5.5\,V$, K = Open, $V_{OUT} = 30\,V$	—	50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	UCN-4204B	$I_{OUT} = 1.25\,A$, L = 3 mH	15	—	V
		UCN-4205B-2	$I_{OUT} = 1.0\,A$, L = 3 mH	25	—	V
Output Saturation Voltage	$V_{CE(sat)}$	UCN-4204B	$V_{CC} = 4.5\,V$, $I_{OUT} = 700\,mA$	—	0.5	V
			$V_{CC} = 4.5\,V$, $I_{OUT} = 1.0\,A$	—	0.7	V
			$V_{CC} = 4.5\,V$, $I_{OUT} = 1.25\,A$	—	1.0	V
		UCN-4205B-2	$V_{CC} = 4.5\,V$, $I_{OUT} = 700\,mA$	—	0.8	V
			$V_{CC} = 4.5\,V$, $I_{OUT} = 1.0\,A$	—	1.25	V
Clamp Diode Leakage Current	I_R	UCN-4204B	$V_R = 20\,V$	—	50	µA
		UCN-4205B-2	$V_R = 30\,V$	—	50	µA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 1.5\,A$	—	3.0	V
Input Current	$I_{IN(1)}$	Both	$V_{CC} = 4.5\,V$, $V_{IN} = 2.0\,V$, $T_A = 25°C$	—	5.0	µA
		Both	$V_{CC} = 4.5\,V$, $V_{In} = 2.0\,V$, $T_A = 70°C$	—	40	µA
	$I_{IN(0)}$	Both	$V_{CC} = 5.5\,V$, $V_{IN} = 0.8\,V$	—	−1.6	mA
Input Voltage	$V_{IN(1)}$	Both	$V_{CC} = 4.5\,V$	2.0	—	V
	$V_{IN(0)}$	Both	$V_{CC} = 5.5\,V$	—	0.8	V
Input Clamp Voltage	V_{IN}	Both	$I_{UB} = -12\,mA$	—	−1.5	V
Supply Current	I_{CC}	Both	2 Drivers ON	—	90	mA
Turn-ON Delay	t_{on}	Both	$0.5\,E_{in}$ (Pin 11) to $0.5\,E_{out}$	—	10	µs
Turn-OFF Delay	t_{off}	Both	$0.5\,E_{in}$ (Pin 11) to $0.5\,E_{out}$	—	10	µs



UCN-4805A
BiMOS LATCHED DECODER/DRIVER

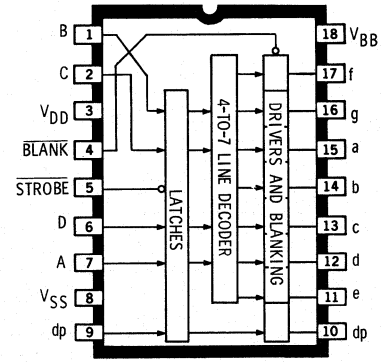
FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Hexadecimal Decoding
- Internal Pull-Up/Pull-Down Resistors
- Wide Supply Voltage Range

DESIGNED for use in high-voltage vacuum fluorescent display driver applications, the UCN-4805A latched decoder/driver combines CMOS logic with bipolar source outputs. The device consists of eight high-voltage bipolar sourcing outputs, with internal pull-down resistors and CMOS input latches, hexadecimal decoder, and control circuitry (strobe and blanking).

Type UCN-4805A is intended to serve as the segment driver with standard 7-segment displays incorporating a colon or decimal point. The integrated circuit uses hexadecimal decoding to display 0-9, A, b, C, d, E, and F.

This BiMOS latched decoder/driver has sufficient speed to permit operation with most microprocessor/LSI-based systems. The CMOS input latches provide operation over the supply voltage range of 5 to 15 V with minimum logic loading. Internal output pull-down resistors eliminate the need for external components usually required for fluorescent display applications. When used with standard TTL or low-speed TTL logic, the device may require employment of input pull-up resistors to insure a proper input logic high.



Dwg. No. A-10,984A

UCN-4805A

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ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} . . . . . 60 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} . . . . . 5.0 V to 60 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} . . . . . −40 mA
Package Power Dissipation, P_D . . . . . 1.82 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = 25°C.

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = − 25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	μA
Output Leakage Current		T_A = 70°C	—	−15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = 5.0 V	—	100	μA
		V_{DD} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	Display "8"	—	9.1	mA
		All outputs OFF	—	100	μA
	I_{DD}	V_{DD} = I/O = STROBE = 5.0 V, All other inputs = 0 V	—	200	μA
		V_{DD} = I/O = STROBE = 15 V, All other inputs = 0 V	—	500	μA
		V_{DD} = STROBE = BLANK = 5.0 V, Data latched, Display "8"	—	7.0	mA
		V_{DD} = STROBE = BLANK = 15 V, Data latched, Display "8"	—	21	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

MAXIMUM ALLOWABLE DUTY CYCLE

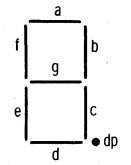
Number of Outputs ON (I_{OUT} = −25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of 50°C	60°C	70°C
8	100%	92%	78%
7	↑	100%	89%
6	↕	↑	100%
↕	↕	↕	↕
1	100%	100%	100%

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

UCN-4805A TRUTH TABLE

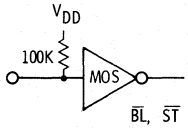
Inputs								Outputs							
D	C	B	A	dp	$\overline{BL}$	$\overline{ST}$	Character	a	b	c	d	e	f	g	dp
0	0	0	0	0	1	0	Zero	1	1	1	1	1	1	0	0
0	0	0	1	0	1	0	One	0	1	1	0	0	0	0	0
0	0	1	0	0	1	0	Two	1	1	0	1	1	0	1	0
0	0	1	1	0	1	0	Three	1	1	1	1	0	0	1	0
0	1	0	0	0	1	0	Four	0	1	1	0	0	1	1	0
0	1	0	1	0	1	0	Five	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	Six	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	Seven	1	1	1	0	0	0	0	0
1	0	0	0	0	1	0	Eight	1	1	1	1	1	1	1	0
1	0	0	1	0	1	0	Nine	1	1	1	0	0	1	1	0
1	0	1	0	0	1	0	A	1	1	1	0	1	1	1	0
1	0	1	1	0	1	0	b	0	0	1	1	1	1	1	0
1	1	0	0	0	1	0	C	1	0	0	1	1	1	0	0
1	1	0	1	0	1	0	d	0	1	1	1	1	0	1	0
1	1	1	0	0	1	0	E	1	0	0	1	1	1	1	0
1	1	1	1	0	1	0	F	1	0	0	0	1	1	1	0
X	X	X	X	1	1	0	dp	X	X	X	X	X	X	X	1
X	X	X	X	X	0	X	blank	0	0	0	0	0	0	0	0

X = irrelevant

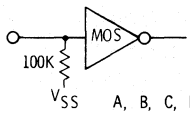


DWG. NO. A-10,985

TYPICAL INPUT CIRCUITS

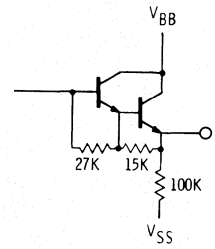


Dwg.No. A-10,979A



Dwg. No. A-10,980

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981

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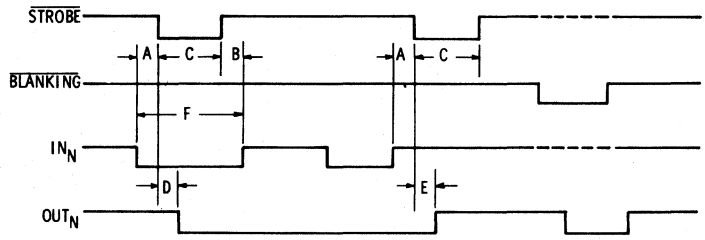
TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})



Dwg.No. A-10,982A

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 100 ns
C. Minimum Strobe Pulse Width ..... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition ..... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition ..... 1.0 μs
F. Minimum Data Pulse Width ..... 500 ns

Information present at an input is transferred to its latch when the STROBE (ST) is low. The latches will continue to accept new data as long as the STROBE is held low. Applications where the latches are bypassed (STROBE tied low) ordinarily require that the BLANKING input be low between digit selection because of possible non-synchronous decoding.

When the BLANKING (BL) input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input high, the outputs are controlled by the latch/decoder circuitry.

UCN-4807A AND UCN-4808A
BiMOS ADDRESSABLE LATCHED DRIVERS

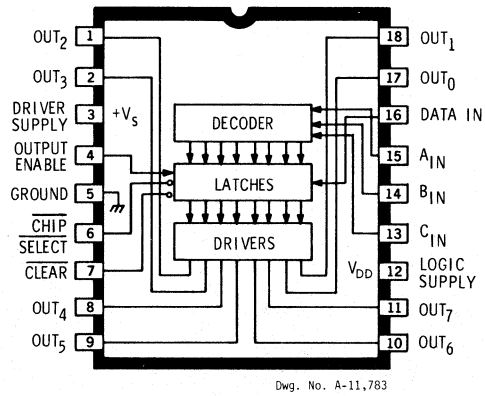
FEATURES

- Addressable Data Entry
- 50 V Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Wide Supply-Voltage Range

THESE 8-BIT, ADDRESSABLE, latched drivers are used in a wide variety of power demultiplexer applications. They can drive all types of common peripheral power loads, including lamps, relays, solenoids, LEDs, printer heads, heaters, and stepper motors. They can also be used as DMUX drivers for higher power loads requiring discrete power semiconductors.

Type UCN-4807A and UCN-4808A drivers are identical except for output current ratings. The former is rated for a maximum of 200 mA per output while the latter is capable of sinking up to 600 mA per output. The 50 V outputs are bipolar NPN saturated switches with first stage driver currents optimized for each version.

Each MSI array is comprised of a 3-bit to 8-line decoder, 8 type D latches, 8 open-collector output drivers, and MOS control circuitry for $\overline{\text{CHIP SELECT}}$, $\overline{\text{CLEAR}}$, and OUTPUT ENABLE functions. Any of the eight power loads can be addressed individually and can be turned ON or OFF independently of the other loads.



Dwg. No. A-11,783

Under normal operating conditions, all outputs of Type UCN-4807A can sustain 150 mA over the operating temperature range without derating. Type UCN-4808A will sustain 500 mA per output at 30°C and a duty cycle of 33%. Other combinations of number of outputs conducting and duty cycle are shown in the specifications.

These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of −20°C to +85°C.

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UCN-4808A DERATING

Number of Outputs ON (I_{OUT} = 500 mA)	Max. Duty Cycle (with V_{DD} = 5 V) at Ambient Temperature of				
	30°C	40°C	50°C	60°C	70°C
8	33%	29%	25%	21%	17%
7	37%	33%	29%	24%	20%
6	44%	39%	33%	28%	23%
5	52%	46%	40%	34%	28%
4	65%	58%	50%	42%	35%
3	87%	77%	67%	57%	46%
2	100%	100%	100%	85%	70%
1	100%	100%	100%	100%	100%

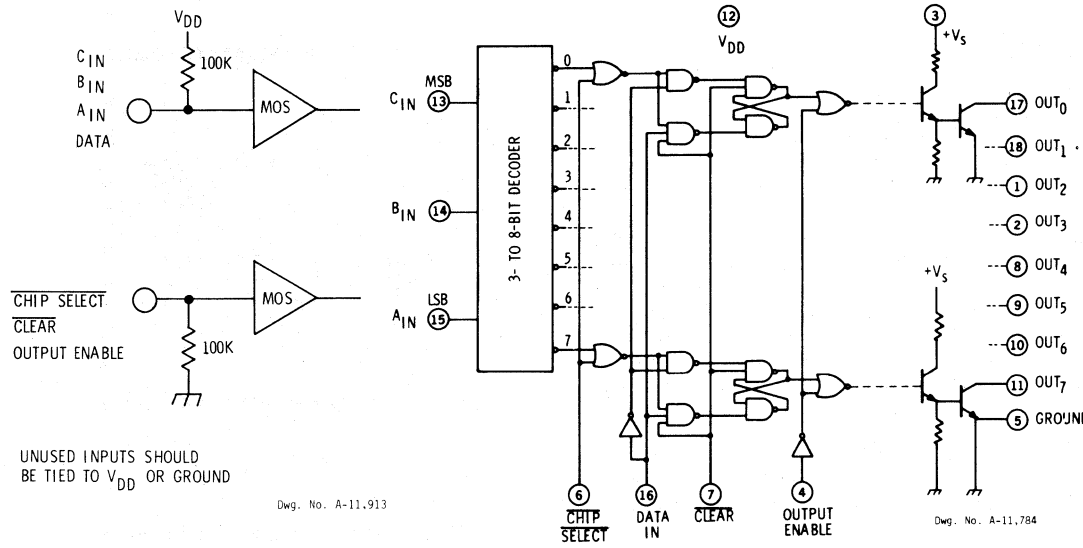
ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{OUT} ..... 50 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_S ..... 4.5 V to 5.5 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} (UCN-4807A) ..... 200 mA
(UCN-4808A) ..... 600 mA
Package Power Dissipation, P_D ..... 1.82 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = +25°C.

FUNCTIONAL BLOCK DIAGRAM

TYPICAL INPUT CIRCUITS



Terminal Designation	Function
ADDRESS	A 3-bit binary address on these pins defines which one of the 8 latches is to receive the data. C_{IN} is the most-significant bit; A_{IN} is least significant.
$\overline{\text{CHIP SELECT}}$	When this input is low, the addressed output latch will accept data. When $\overline{\text{CHIP SELECT}}$ is high, the latches will retain their existing state, regardless of ADDRESS or DATA input conditions. This input should be held high while ADDRESS is being changed. $\overline{\text{CHIP SELECT}}$ also allows an additional level of address decoding.
DATA INPUT	When $\overline{\text{CHIP SELECT}}$ is low, the data bit present here is transferred to the addressed latch and output such that (when OUTPUT ENABLE is high) "1" turns the output ON and "0" turns the output OFF.
$\overline{\text{CLEAR}}$	When $\overline{\text{CLEAR}}$ goes from high to low, all latches are reset and outputs are turned OFF.
OUTPUT ENABLE	When this input is high, the outputs are controlled by their respective latches. When OUTPUT ENABLE is low, all outputs are OFF.
OUTPUTS	These are the 8 open-collector NPN outputs.
DRIVER SUPPLY	This is the supply voltage for the first stage of the bipolar output drivers. The nominal supply is 5.0 V.
LOGIC SUPPLY	This is the CMOS logic supply voltage input. Typically it is between 4.75 V and 15.75 V.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	UCN-4807A Min.	UCN-4807A Max.	UCN-4808A Min.	UCN-4808A Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 50$ V	—	50	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	0.2	—	—	V
		$I_{OUT} = 100$ mA	—	0.3	—	—	V
		$I_{OUT} = 150$ mA	—	0.4	—	—	V
		$I_{OUT} = 200$ mA	—	—	—	0.5	V
		$I_{OUT} = 350$ mA	—	—	—	0.7	V
		$I_{OUT} = 500$ mA	—	—	—	1.0	V
Input Voltage	$V_{IN(0)}$		—	0.8	—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 15$ V	13.5	—	13.5	—	V
		$V_{DD} = 5$ V	3.5	—	3.5	—	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD} = 15$ V	—	300	—	300	μA
		$V_{IN} = V_{DD} = 5$ V	—	100	—	100	μA
Input Resistance	R_{IN}		50	—	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{DD} = 15$ V	—	5.0	—	5.0	mA
		One Driver ON, $V_{DD} = 5$ V	—	1.0	—	1.0	mA
	$I_{DD(OFF)}$	CLEAR = 0 V, SELECT = $V_{DD} = 15$ V	—	300	—	300	μA
		CLEAR = 0 V, SELECT = $V_{DD} = 5$ V	—	100	—	100	μA
	$I_{S(ON)}$	One Driver ON, $V_S = 5$ V	—	5.5	—	50	mA
		All Drivers ON, $V_S = 5$ V	—	45	—	160	mA
	$I_{S(OFF)}$	ENABLE = 0 V, $V_S = 5$ V	—	0.1	—	35	mA

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

CAUTION: Sprague CMOS devices have input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

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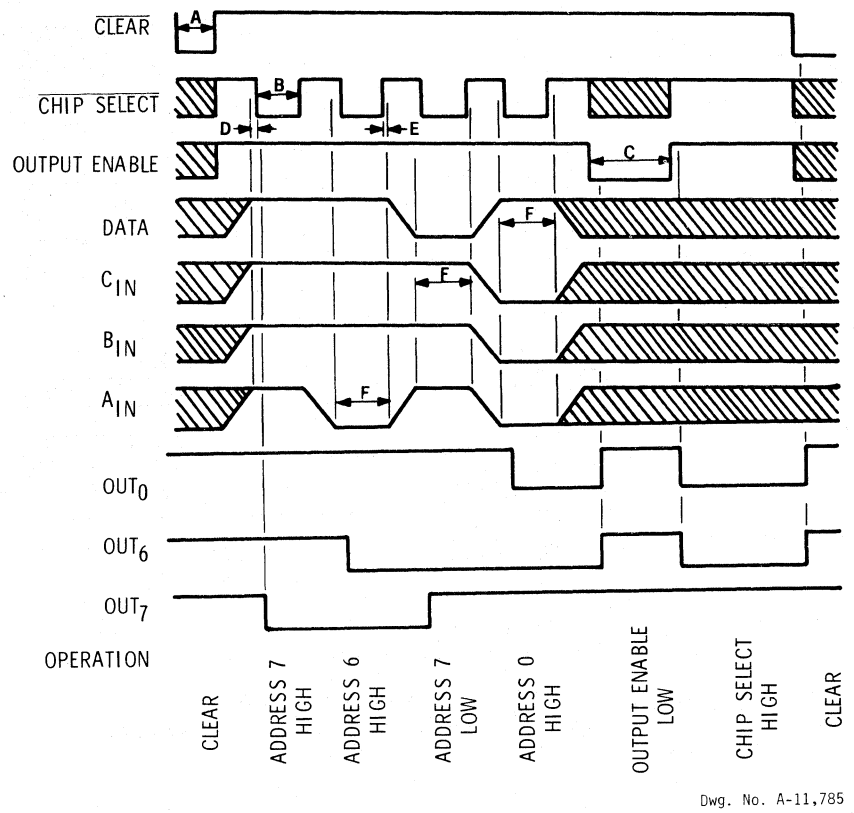
TRUTH TABLE

$\overline{\text{CHIP SELECT}}$	$\overline{\text{CLEAR}}$	DATA	C_{IN}	B_{IN}	A_{IN}	OUTPUT ENABLE	OUT_7	OUT_6	OUT_5	OUT_4	OUT_3	OUT_2	OUT_1	OUT_0	
X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	Clear
H	H	X	X	X	X	H	R	R	R	R	R	R	R	R	Memory
L	H	D	L	L	L	H	R	R	R	R	R	R	$\underline{R}$	$\overline{D}$	Address Latch 0
L	H	D	L	L	H	H	R	R	R	R	R	$\underline{R}$	$\overline{D}$	R	Address Latch 1
L	H	D	L	H	L	H	R	R	R	R	$\underline{R}$	$\overline{D}$	R	R	Address Latch 2
L	H	D	L	H	H	H	R	R	R	$\underline{R}$	$\overline{D}$	R	R	R	Address Latch 3
L	H	D	H	L	L	H	R	R	$\underline{R}$	$\overline{D}$	R	R	R	R	Address Latch 4
L	H	D	H	L	H	H	R	$\underline{R}$	$\overline{D}$	R	R	R	R	R	Address Latch 5
L	H	D	H	H	L	H	$\underline{R}$	$\overline{D}$	R	R	R	R	R	R	Address Latch 6
L	H	D	H	H	H	H	$\overline{D}$	R	R	R	R	R	R	R	Address Latch 7
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	Blanking
X	X	X	X	X	X	H	R	R	R	R	R	R	R	R	

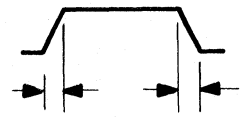
L = Low Logic Level
H = High Logic Level
D = Data (High or Low)
X = Irrelevant
R = Previous State

I/O WAVEFORMS



Dwg. No. A-11,785

Logic Level Irrelevant



Allowable Transition Time

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum $\overline{\text{CLEAR}}$ Pulse Width	300 ns
B. Minimum $\overline{\text{CHIP SELECT}}$ Pulse Width	500 ns
C. Typical OUTPUT ENABLE (Blanking) Pulse Width	5.0 μs
D. Minimum DATA or ADDRESS Setup Time	100 ns
E. Minimum DATA or ADDRESS Hold Time	100 ns
F. Minimum DATA or ADDRESS Pulse Width	700 ns

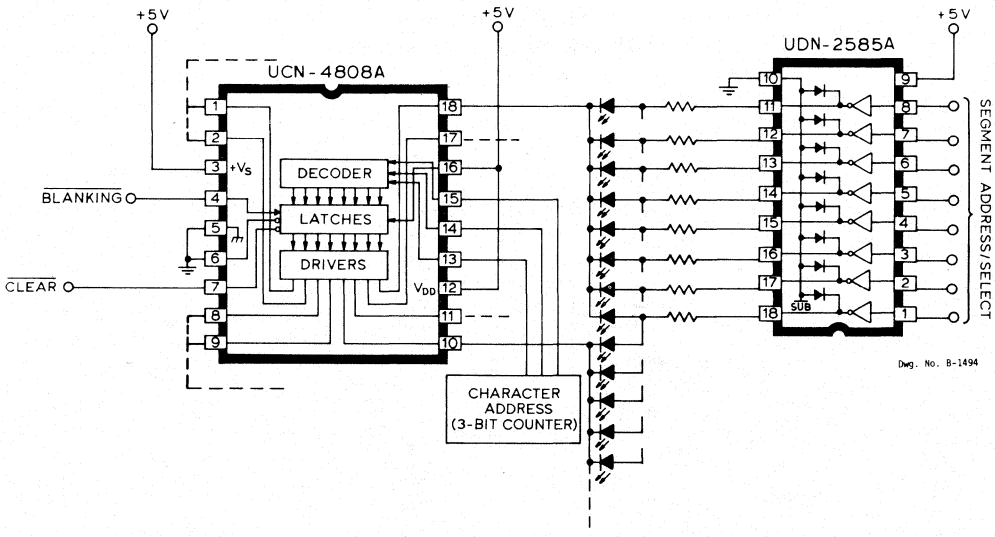
TYPICAL APPLICATIONS

A typical application for Type UCN-4808A, driving a common-cathode LED display, is shown below. Many multi-character LED displays can make use of the high-current capability of this device. With the DATA input held high, the proper address code may be furnished by a 3-bit counter. Note that with DATA held constant and the ADDRESS sequenced through the binary code, setup and hold times associated with CHIP SELECT may be ignored.

The second application illustrates the use of Type UCN-4807A or UCN-4808A as a multiplexed power driver. A wide variety of peripheral loads including lamps, relays, solenoids, LEDs, and stepper motors can be accommodated. Inductive loads require external transient suppression.

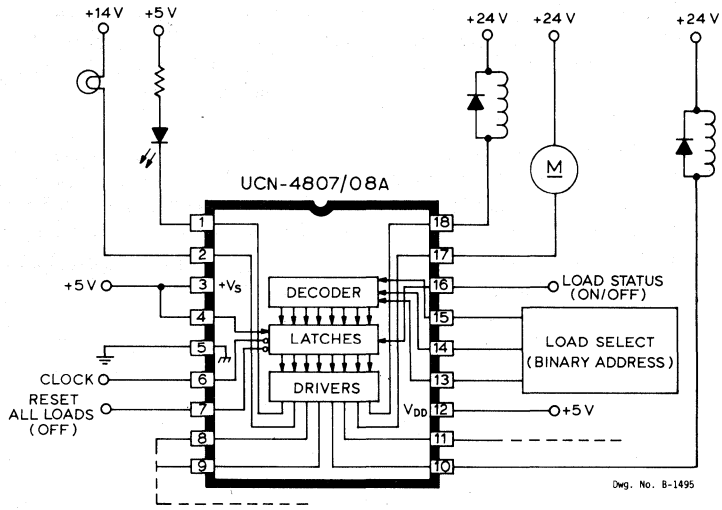
These devices can also be employed as multi-channel drivers for discrete high-current or high-voltage semiconductors.

Common-Cathode LED Display Driver

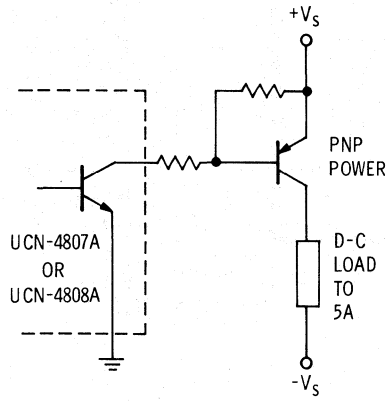


TYPICAL APPLICATIONS (Continued)

Multiplexed Power Driver



Multichannel Driver for Discrete Power Semiconductors



UCN-5800A AND UCN-5801A
BiMOS II LATCHED DRIVERS

FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

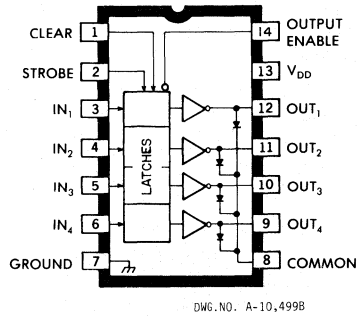
THE UCN-5800A and UCN-5801A latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. Type UCN-5800A contains four latched drivers; Type UCN-5801A contains eight latched drivers.

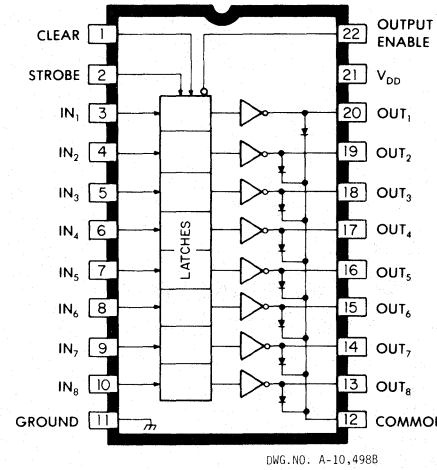
BiMOS II devices have much faster data input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.



UCN-5800A

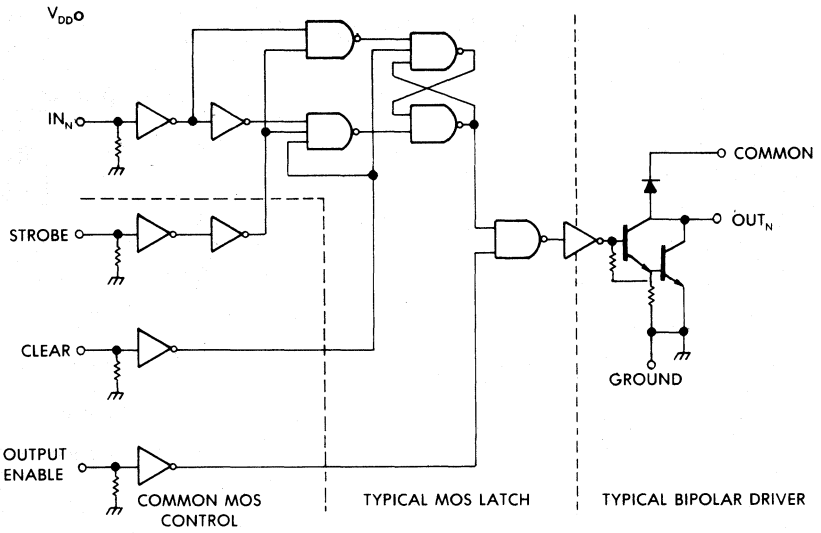


UCN-5801A

UCN-5800A, the 4-latch device, is furnished in a standard 14-pin dual in-line plastic package. UCN-5801A, the 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.

5

FUNCTIONAL BLOCK DIAGRAM



DWG.NO. A-10,495A

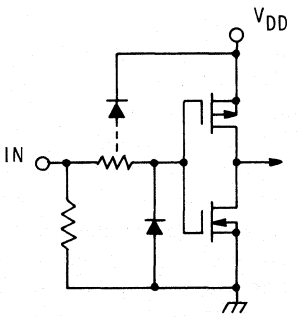
ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . . 500 mA
Package Power Dissipation, P_D
(UCN-5800A) . . . . . 1.6 W*
(UCN-5801A) . . . . . 2.0 W**
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = +25°C.
**Derate at the rate of 20 mW/°C above T_A = +25°C.

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,520

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$ (unless otherwise noted)

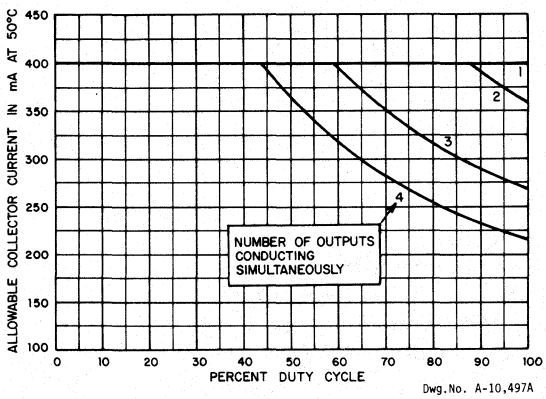
Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$, $T_A = +25°C$	—	—	50	μA
		$V_{CE} = 50\ V$, $T_A = +70°C$	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	0.9	1.1	V
		$I_C = 200\ mA$	—	1.1	1.3	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	—	V
		$V_{DD} = 10\ V$	8.5	—	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	200	—	kΩ
		$V_{DD} = 10\ V$	50	300	—	kΩ
		$V_{DD} = 5.0\ V$	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	—	200	μA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	50	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$, $T_A = +25°C$	—	—	50	μA
		$V_R = 50\ V$, $T_A = +70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

5

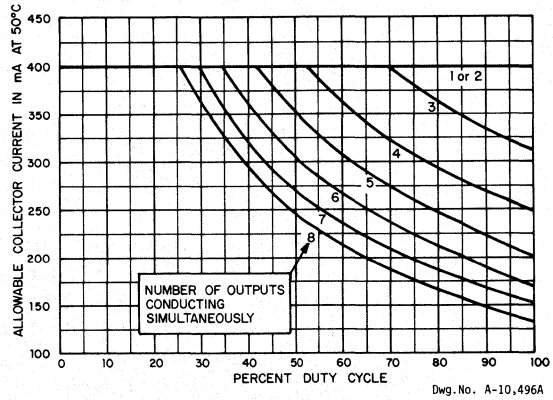
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5800A

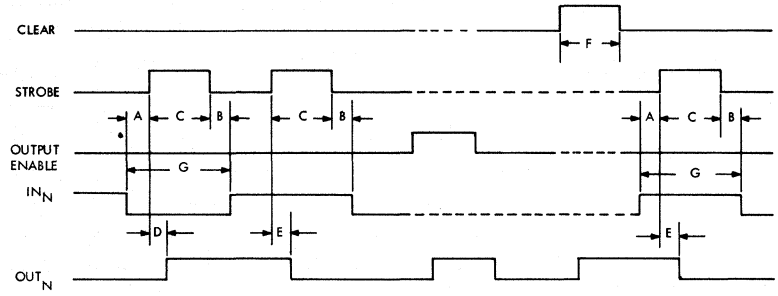


Dwg.No. A-10,497A

UCN-5801A



Dwg.No. A-10,496A



DWG.NO. A-10,895A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) . . . . . 50 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 50 ns
C. Minimum strobe pulse width . . . . . 125 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 225 ns

TRUTH TABLE

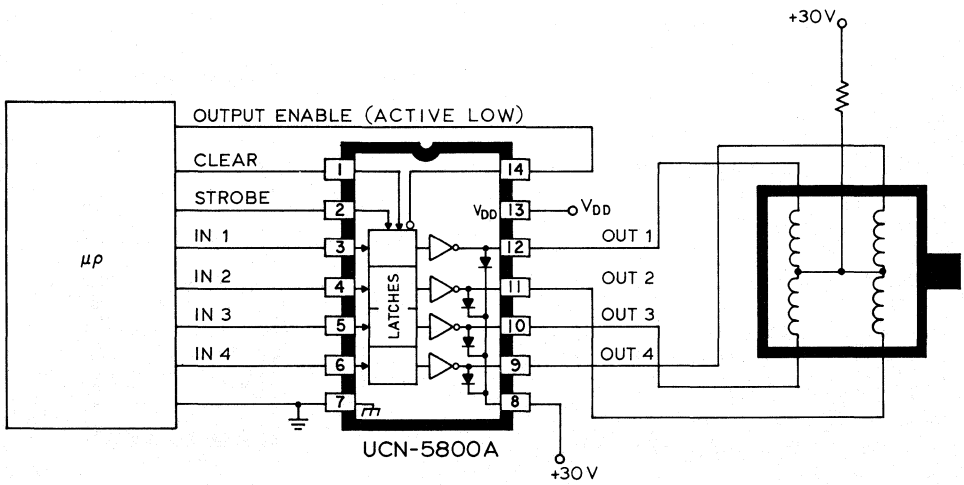
IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

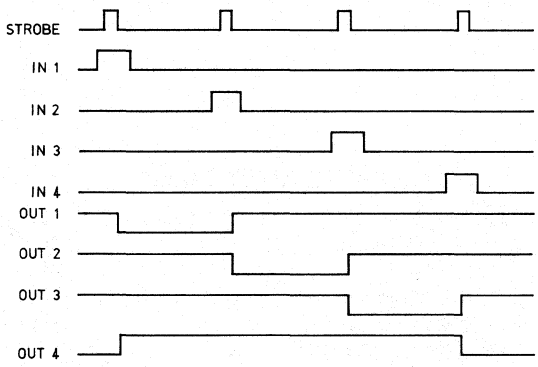
TYPICAL APPLICATION

UNIPOLAR STEPPER-MOTOR DRIVE



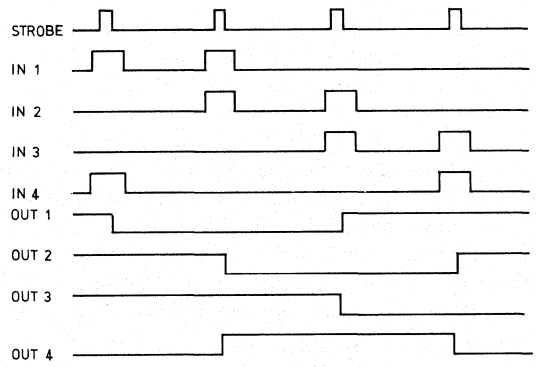
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



DWG.NO. A-11,446

UNIPOLAR 2-PHASE DRIVE



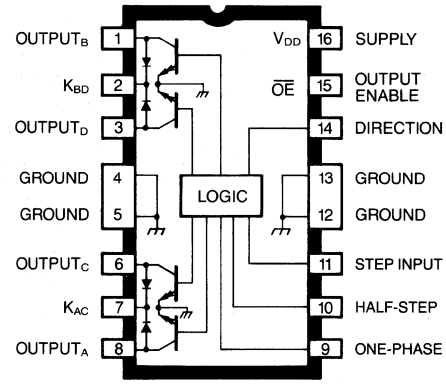
DWG.NO. A-11,447

5

UCN-5804B
BiMOS II TRANSLATOR/DRIVER

FEATURES

- 1.5 A Maximum Output Current
- 35 V Output Sustaining Voltage
- Wave-Drive, Two-Phase, and Half-Step Drive Formats
- Internal Clamp Diodes
- Output Enable and Direction Control
- Power-ON Reset
- Internal Thermal Shutdown Circuitry



Dwg. No. W-194

Combining low-power CMOS logic with high-current and high-voltage bipolar outputs, the UCN-5804B BiMOS II translator/driver provides complete control and drive for a four-phase unipolar stepper-motor with continuous output current ratings to 1.25 A per phase (1.5 A startup) and 35 V.

The CMOS logic section provides the sequencing logic, DIRECTION and OUTPUT ENABLE control, and a power-ON reset function. Three stepper-motor drive formats, wave-drive (one-phase), two-phase, and half-step are externally selectable. The inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of appropriate pull-up resistors to insure a proper input-logic high.

The wave-drive format consists of energizing one motor phase at a time in an A-B-C-D (or D-C-B-A) sequence. This excitation mode consumes the least power and assures positional accuracy regardless of any winding inbalance in the motor. Two-phase drive energizes two adjacent phases in each detent position (AB-BC-CD-DA). This sequence mode offers an improved torque-speed product, greater detent torque, and is less susceptible to motor resonance. Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-BC-C-CD-D-DA), providing an eight-step sequence.

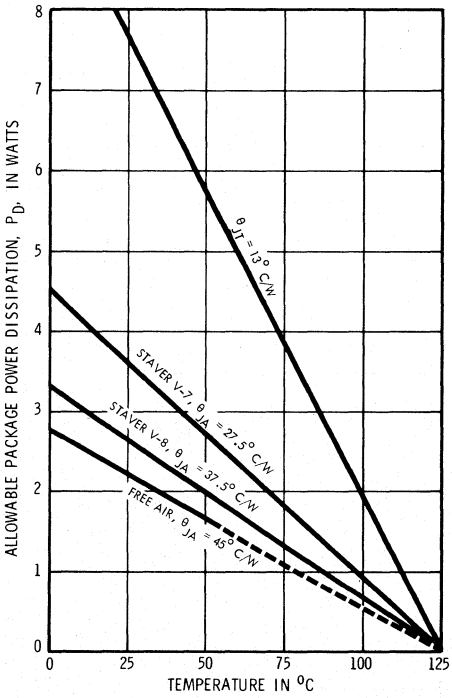
The bipolar outputs are capable of sinking up to 1.5 A and withstanding 50 V in the OFF state (sustaining voltages up to 35 V). Ground clamp and flyback diodes provide protection against inductive transients. Thermal protection circuitry disables the outputs when the chip temperature is excessive.

The UCN-5804B is rated for operation over the temperature range of −20°C to +85°C. It is supplied in a 16-pin dual in-line plastic batwing package with a copper lead frame and heat-sinkable tabs for improved power dissipation capabilities.

ABSOLUTE MAXIMUM RATINGS

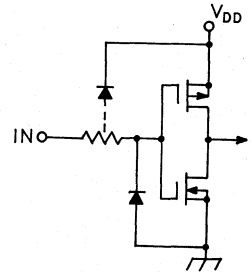
Output Voltage, V_{CE} ..... 50 V
Output Sustaining Voltage, $V_{CE\ (sus)}$ ..... 35 V
Output Sink Current, I_{OUT} ..... 1.5 A
Logic Supply Voltage, V_{DD} ..... 7.0 V
Input Voltage, V_{IN} ..... 7.0 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



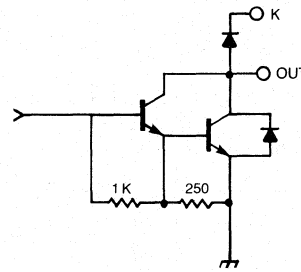
Dwg. No. W-195

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. D-196

5

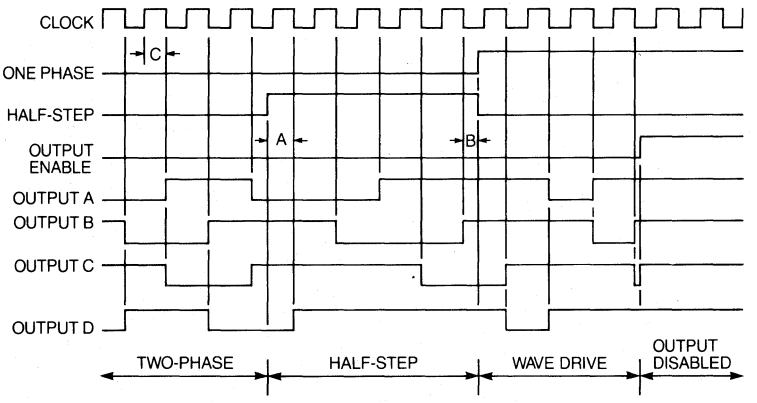
TRUTH TABLE

	PIN 9	PIN 10
TWO-PHASE	L	L
ONE-PHASE	H	L
HALF-STEP	L	H
STEP-INHIBIT	H	H

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $T_{TAB} \leq 70°C$, $V_{DD} = 4.5\ V$ to $5.5\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 50\ V$	—	10	50	µA
Output Sustaining Voltage	$V_{CE\ (sus)}$	$I_{OUT} = 1.25\ A$, $L = 3\ mH$	35	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 700\ mA$	—	1.0	1.2	V
		$I_{OUT} = 1\ A$	—	1.1	1.4	V
		$I_{OUT} = 1.25\ A$	—	1.2	1.5	V
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	10	50	µA
Clamp Diode Forward Voltage	V_F	$I_F = 1.25\ A$	—	—	3.0	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.5	5.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8\ V$	—	−0.5	−5.0	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5\ V$	3.5	—	5.3	V
	$V_{IN(0)}$		−0.3	—	0.8	V
Supply Current	I_{DD}	2 Outputs ON	—	20	30	mA
Turn-Off Delay	t_{ON}	50% Step Inputs to 50% Output	—	—	10	µs
Turn-On Delay	t_{OFF}	50% Step Inputs to 50% Output	—	—	10	µs
Thermal Shutdown Temperature	T_j		—	165	—	°C

TIMING CONDITIONS



Dwg. No. W-110A

A. Minimum data set up time..... 100 ns
B. Minimum data hold time..... 100 ns
C. Minimum step input pulse width..... 500 ns

APPLICATIONS INFORMATION

Internal power-ON reset (POR) circuitry resets $OUTPUT_A$ (and $OUTPUT_D$ in the two-phase drive format) to the ON state with initial application of the logic supply voltage. After reset, the circuit then steps according to the tables shown below.

The outputs will advance one sequence position on the high-to-low transition of the STEP INPUT pulse. Logic levels on the HALF-STEP and ONE-PHASE inputs will determine the drive format (one-phase, two-phase, or half-step). The DIRECTION pin determines the rotation sequence of the outputs. Note that the STEP INPUT must be in the low state when changing the state of ONE-PHASE, HALF-STEP, or DIRECTION to prevent erroneous stepping.

All outputs are disabled (OFF) when OUTPUT ENABLE is at a logic high. That input can be used for chopping applications without affecting the stepping logic. If the function is not required, OUTPUT ENABLE should be tied low. In that condition, all outputs depend only on the state of the step logic.

Internal thermal protection circuitry disables all outputs when the junction temperature reaches approximately 165°C. The outputs are enabled again when the junction cools down to approximately 145°C.

WAVE-DRIVE SEQUENCE

↓DIRECTION = L	Half Step = L, One Phase = H				→DIRECTION = H
Step	**A**	**B**	**C**	**D**	
POR	ON	OFF	OFF	OFF	
1	ON	OFF	OFF	OFF	
2	OFF	ON	OFF	OFF	
3	OFF	OFF	ON	OFF	
4	OFF	OFF	OFF	ON	

TWO-PHASE DRIVE SEQUENCE

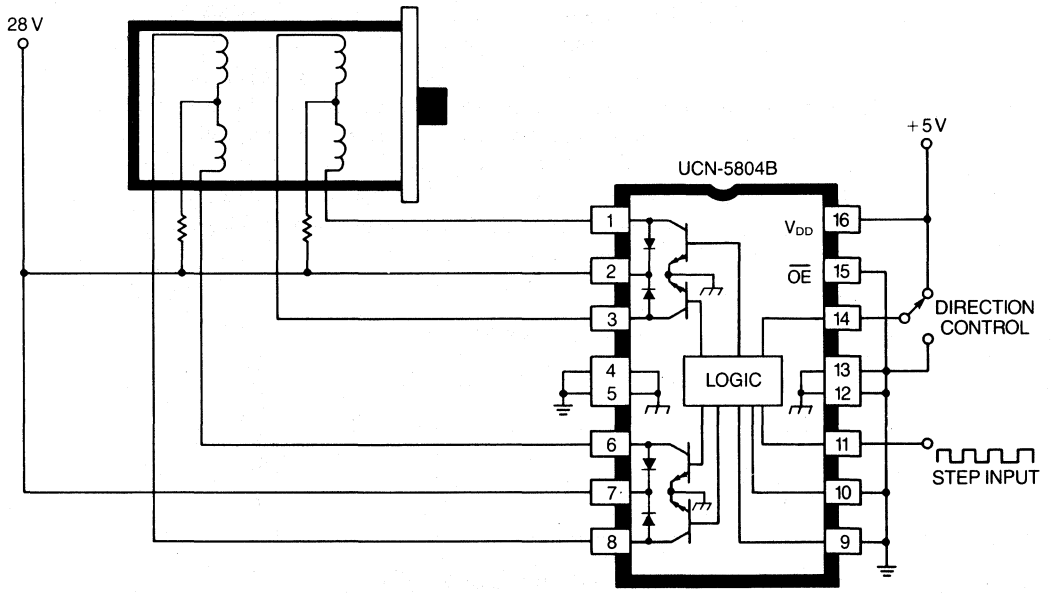
↓DIRECTION = L	Half Step = L, One Phase = L				→DIRECTION = H
Step	**A**	**B**	**C**	**D**	
POR	ON	OFF	OFF	ON	
1	ON	OFF	OFF	ON	
2	ON	ON	OFF	OFF	
3	OFF	ON	ON	OFF	
4	OFF	OFF	ON	ON	

HALF-STEP DRIVE SEQUENCE

↓DIRECTION = L	Half Step = H, One Phase = L				→DIRECTION = H
Step	**A**	**B**	**C**	**D**	
POR	ON	OFF	OFF	OFF	
1	ON	OFF	OFF	OFF	
2	ON	ON	OFF	OFF	
3	OFF	ON	OFF	OFF	
4	OFF	ON	ON	OFF	
5	OFF	OFF	ON	OFF	
6	OFF	OFF	ON	ON	
7	OFF	OFF	OFF	ON	
8	ON	OFF	OFF	ON	

TYPICAL APPLICATION

L/R STEPPER-MOTOR DRIVE



Dwg. No. D-197

UCN-5810A, UCN-5812A, AND UCN-5818A BiMOS II SERIAL-INPUT, LATCHED DRIVERS —10, 20, and 32 Bits

FEATURES

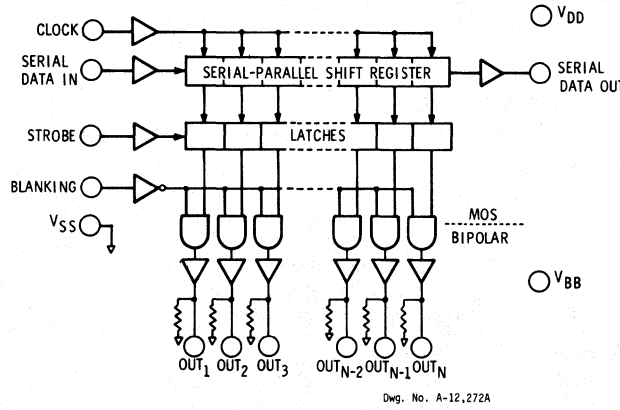
- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 60 V or 80 V Source Outputs
- Internal Pull-Down Resistors

DESIGNED for use as segment or digit drivers in high-voltage, vacuum-fluorescent display applications, Type UCN-5810A, UCN-5812A, and UCN-5818A combine a CMOS register (10, 20, or 32 bits, respectively), associated latches, and control circuitry (strobe and blanking) with 60 V bipolar source outputs. The BiMOS drivers can also be used with non-multiplexed LED displays within their output limitation of 40 mA per driver.

Selected devices (suffix −1) have maximum ratings of 80 V and 40 mA per driver. In all other respects, the basic part and the part with the "−1" suffix are identical.

BiMOS II devices have much faster input data rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high. A CMOS serial-data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.



FUNCTIONAL BLOCK DIAGRAM

Type UCN-5810A, a 10-bit driver, is furnished in an 18-pin dual in-line plastic package. It is a high-speed, pin-compatible version of the UCN-4810A driver.

Type UCN-5812A, a 20-bit driver, is furnished in a 28-pin dual in-line plastic package with 0.600″ (15.24 mm) row spacing. Type UCN-5818A, a 32-bit driver, is supplied in a 40-pin dual in-line plastic package with 0.600″ row spacing.

All devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle. The devices are also available with an extended operating temperature range (prefix UCQ-) and ceramic/glass cer-DIP hermetic packages (suffix R).

5

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

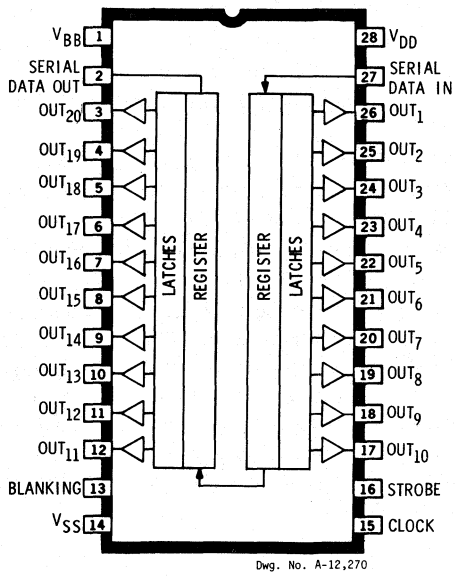
Output Voltage, V_{OUT} . . . . . 60 V
(Suffix −1) . . . . . 80 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB} . . . . . 5.0 V to 60 V
(Suffix −1) . . . . . 5.0 V to 80 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . . −40 mA
Allowable Package Power Dissipation, P_D
(UCN-5810A) . . . . . 1.82 W*
(UCN-5812A) . . . . . 2.5 W*
(UCN-5818A) . . . . . 2.8 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

*Derate linearly to 0 W at T_A = +125°C.

Part Number	Max. Allowable Duty Cycle With All Outputs ON (I_{OUT} = −25 mA) at T_A = +25°C	+40°C	+50°C	+60°C	+70°C
UCN-5810A	100%	97%	85%	73%	62%
UCN-5812A	100%	85%	75%	65%	55%
UCN-5818A	72%	61%	54%	43%	39%

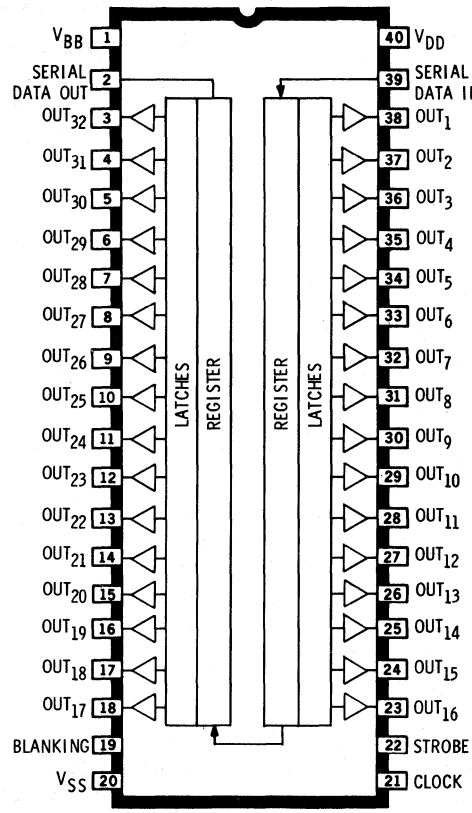
Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5812A



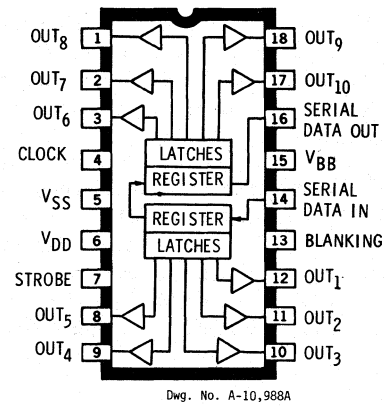
Dwg. No. A-12,270

UCN-5818A



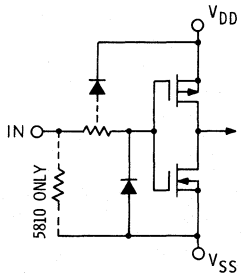
Dwg. No. A-12,269

UCN-5810A



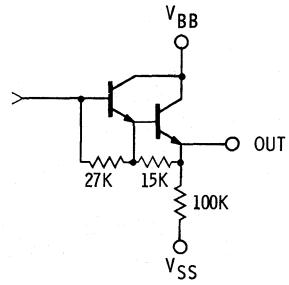
Dwg. No. A-10,988A

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,304A

TYPICAL OUTPUT DRIVER

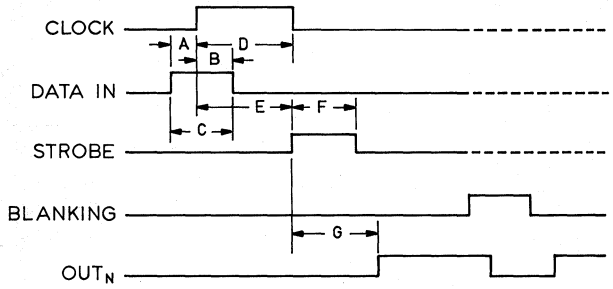


Dwg. No. A-10,981B

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}	All		—	1.0	V
Output ON Voltage	V_{OUT}	All	$I_{OUT} = -25$ mA, $V_{BB} = 60$ V	57.5	—	V
		Suffix −1	$I_{OUT} = -25$ mA, $V_{BB} = 80$ V	77.5	—	V
Output Pull-Down Current	I_{OUT}	All	$V_{OUT} = 60$ V	400	850	µA
		Suffix −1	$V_{OUT} = 80$ V = V_{BB}	550	1150	µA
Output Leakage Current	I_{OUT}	All	$T_A = +70°C$	—	−15	µA
Input Voltage	$V_{IN(1)}$	All	$V_{DD} = 5.0$ V	3.5	5.3	V
			$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	All	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	UCN-5810A	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
			$V_{DD} = V_{IN} = 12$ V	—	240	µA
		UCN-5812/18A	$V_{DD} = V_{IN} = 5.0$ V	—	0.5	µA
			$V_{DD} = V_{IN} = 12$ V		1.0	µA
	$I_{IN(0)}$	UCN-5812/18A	$V_{DD} = 12$ V, $V_{IN} = 0.8$ V	—	−1.0	µA
Input Impedance	Z_{IN}	UCN-5810A	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	All	$V_{DD} = 5.0$ V	—	20	kΩ
			$V_{DD} = 12$ V	—	6.0	kΩ
Supply Current	I_{BB}	UCN-5810A	All outputs ON, All outputs open	—	13	mA
		UCN-5812A	All outputs ON, All outputs open	—	22	mA
		UCN-5818A	All outputs ON, All outputs open	—	35	mA
		UCN-5810A	All outputs OFF, All outputs open	—	200	µA
		UCN-5812/18A	All outputs OFF, All outputs open	—	500	µA
	I_{DD}	All	$V_{DD} = 5.0$ V, All outputs OFF, Inputs = 0 V	—	100	µA
			$V_{DD} = 12$ V, All outputs OFF, Inputs = 0 V	—	200	µA
		UCN-5810A	$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
			$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA
		UCN-5812/18A	$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	0.5	mA
			$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	1.2	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
*"Suffix −1" indicates UCN-5810A-1, UCN-5812A-1 and UCN-5818A-1 only; "UCN-5810A," etc., indicates basic device and same part number with −1 suffix.



Dwg. No. A-12,649A

TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2}R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2}R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1}R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$
					$X\ X\ X\ \ldots X\ X$	H	$L\ L\ L\ \ldots L\ L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5811A AND UCN-5811A-1
12-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

- 3.3 MHz Guaranteed Data Input Rate
- Low-Power CMOS Logic and Latches
- High-Speed Source Drivers
- Active Pull-Downs
- Low-Output Saturation Voltages
- Improved Replacement for SN75512B

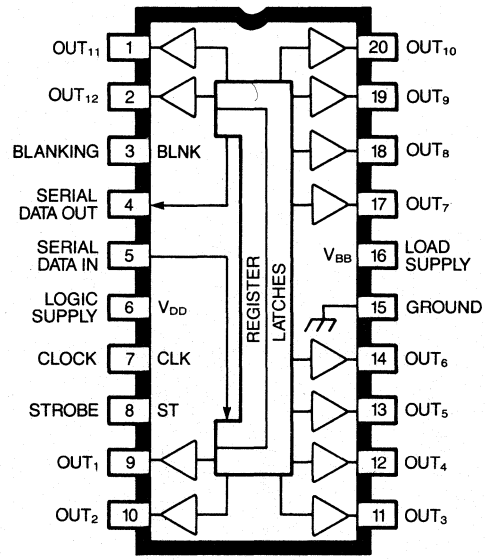
Designed primarily for use with vacuum-fluorescent displays, the UCN-5811A and UCN-5811A-1 Smart Power BiMOS II drivers feature low-output saturation voltages and high output switching speed. These devices contain CMOS shift registers, data latches, and control circuitry, and bipolar high-speed sourcing outputs with DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines.

The UCN-5811A features 60 V and −40 mA output ratings, allowing it to be used in many other peripheral power driver applications. Selected devices (UCN-5811A-1) have maximum output ratings of 80 V. In all other respects, the UCN-5811A and UCN-5811A-1 are identical.

The UCN-5811A can be used as an improved replacement for the SN75512B. The Sprague devices do not require special power-up sequencing.

The UCN-5811A and UCN-5811A-1 have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high.

Both devices are supplied in 20-pin plastic dual in-line packages. They can be operated over the ambient temperature range of −20°C to +85°C. Copper lead frames and low output saturation voltages allow all outputs to be operated at 25 mA continuously at ambient temperatures of up to 62°C.

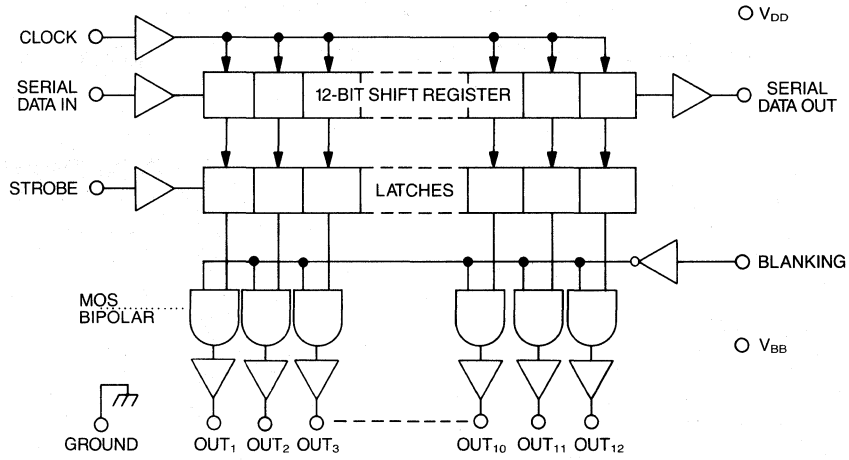


Dwg. No. W-180

ABSOLUTE MAXIMUM RATINGS
at T_A = 25° C

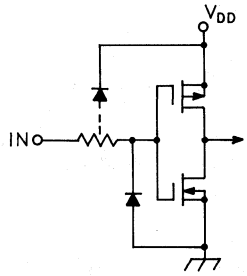
Logic Supply Voltage, V_{DD} 15V
Driver Supply Voltage, V_{BB} (UCN-5811A) 60V
(UCN-5811A-1) 80V
Continuous Output Current, I_{OUT} ..... −40 to +25mA
Input Voltage Range, V_{IN} ..... −0.3V to V_{DD} +0.3V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



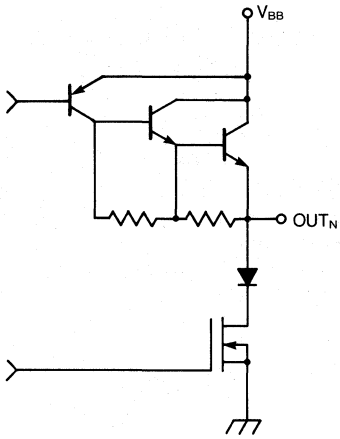
Dwg. No. W-181

TYPICAL INPUT CIRCUIT



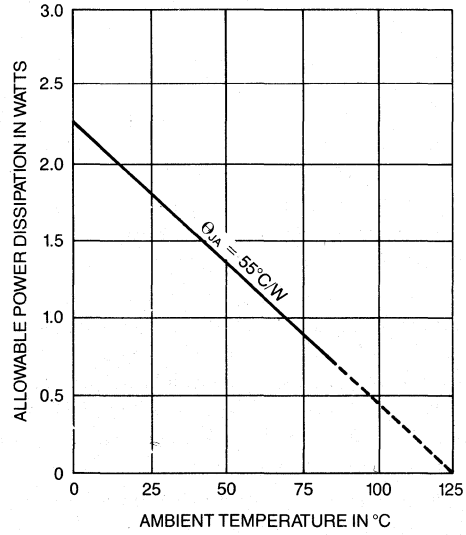
Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER



Dwg. No. W-182

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. W-183

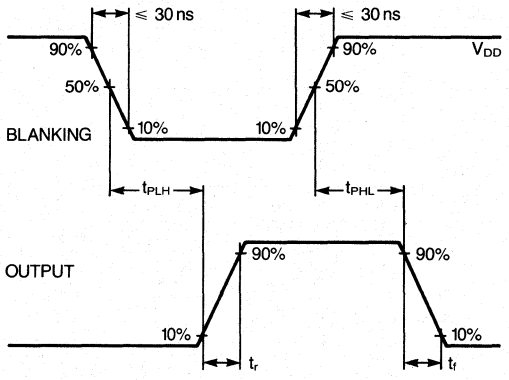
ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{BB} = 60 V (UCN-5811A) or 80 V (UCN-5811A-1), unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5V			Limits @ V_{DD} = 12V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0V, T_A = +70°C	—	−5.0	−15	—	−5.0	−15	µA
Output Voltage	$V_{OUT(H)}$	I_{OUT} = −25mA, V_{BB} = 60V	58	58.5	—	58	58.5	—	V
		I_{OUT} = −25mA, V_{BB} = 80V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(L)}$	I_{OUT} = 1mA	—	2.0	3.0	—	—	—	V
		I_{OUT} = 2mA	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(L)}$	V_{OUT} = 10V to V_{BB}	2.5	4.0	—	—	—	—	mA
		V_{OUT} = 40V to V_{BB}	—	—	—	15	18	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	+0.8	−0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8V	—	−0.05	−0.5	—	−1.0	−1.0	µA
Serial Data Output Voltage	$V_{OUT(H)}$	I_{OUT} = −200µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(L)}$	I_{OUT} = 200µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(H)}$	All Outputs High	—	3.0	5.0	—	15	20	mA
	$I_{DD(L)}$	All Outputs Low	—	2.5	4.0	—	7.0	10	mA
	$I_{BB(H)}$	Outputs High, No Load	—	7.5	12	—	7.5	12	mA
	$I_{BB(L)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30pF	—	300	550	—	125	150	ns
	t_{PLH}	C_L = 30pF	—	250	450	—	170	200	ns
Output Fall Time	t_f	C_L = 30pF	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	C_L = 30pF	—	150	170	—	150	170	ns

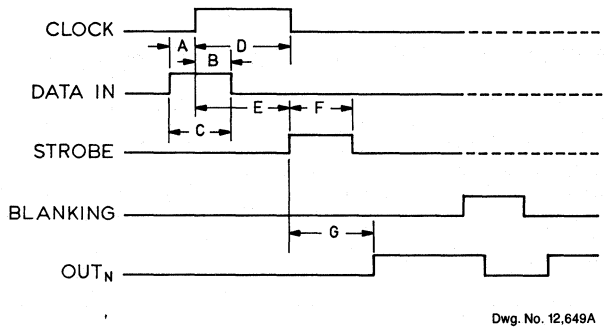
Negative current is defined as coming out of (sourcing) the specified device pin.
**UCN-5811A-1 only.*

5

TIMING WAVESHAPES



Dwg. No. W-184



Dwg. No. 12,649A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75ns
C.	Minimum Data Pulse Width	150ns
D.	Minimum Clock Pulse Width	150ns
E.	Minimum Time Between Clock Activation and Strobe	300ns
F.	Minimum Strobe Pulse Width	100ns
G.	Typical Time Between Strobe Activation and Output Transition	500ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information toward the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3...I_{N-1} I_N			I_1 I_2 I_3...I_{N-1} I_N		I_1 I_2 I_3...I_{N-1} I_N
H	⎍	H R_1 R_2...R_{N-2} R_{N-1}	R_{N-1}				
L	⎍	L R_1 R_2...R_{N-2} R_{N-1}	R_{N-1}				
X	⎎	R_1 R_2 R_3...R_{N-1} R_N	R_N				
		X X X...X X	X	L	R_1 R_2 R_3...R_{N-1} R_N		
		P_1 P_2 P_3...P_{N-1} P_N	P_N	H	P_1 P_2 P_3...P_{N-1} P_N	L	P_1 P_2 P_3...P_{N-1} P_N
					X X X...X X	H	L L L...L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5813B AND UCN-5814B
BiMOS II 4-BIT LATCHED HIGH-CURRENT DRIVERS

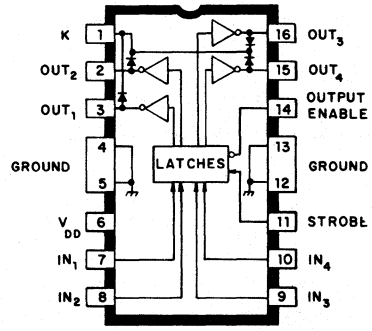
FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Bipolar Outputs
- Output Loads to 480 Watts
- Transient-Protected Outputs
- Low-Power CMOS Logic and Latches
- Internal Input Pull-Down Resistors
- Plastic Dual In-Line Packages

Smart power integrated circuits, combining low-power CMOS latches with high-current bipolar Darlington power drivers, are available as the UCN-5813B and UCN-5814B. Each device consists of four CMOS latches, common STROBE and OUTPUT ENABLE functions, and four open-collector NPN bipolar drivers with output transient-suppression diodes. The UCN-5814B contains the additional functions of INPUT ENABLE and CLEAR for easier μP interface. The INPUT ENABLE can be used as a chip address/select function to control the drive lines to several packages in a simple multiplex scheme.

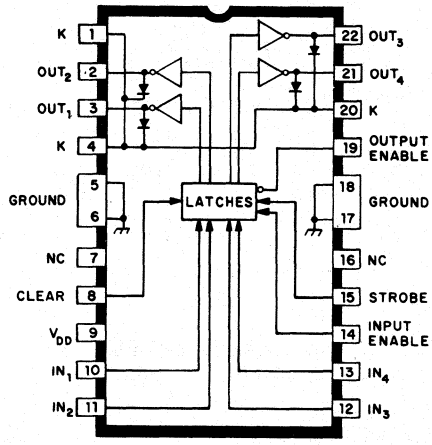
The CMOS inputs are compatible with CMOS, PMOS and NMOS logic families. TTL applications may require pull-up resistors to insure a proper logic "1" level. The bipolar outputs are rated at 50 V in the OFF state and can sustain 35 V and 1.0 A when driving inductive loads. Selected devices (-1 suffix) have maximum ratings of 80 V and 50 V sustaining. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. The outputs may be paralleled for higher load current capability.

BiMOS II devices have much improved data input rates. With a 5 V supply, they will typically operate at data input rates better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.



UCN-5813B

DWG. NO. SG-101



UCN-5814B

DWG. NO. SG-102

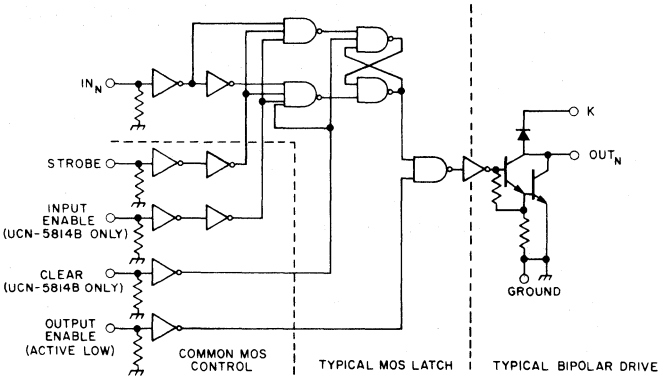
These devices are highly recommended for microprocessor-based application with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads. A similar 4-bit latched driver, for use with loads to 50 V (inductive loads to 35 V) and 350 mA, is the UCN-5800A. High-voltage devices, for operation to 150 V, are furnished as UCN-5900A.

Continued next page

5

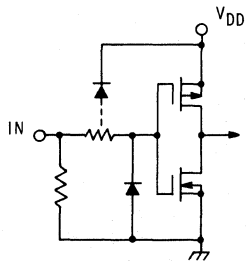
The UCN-5813B is furnished in a 16-pin dual in-line plastic package with 0.300″ row centers while the UCN-5814B device is furnished in a 22-pin package with 0.400″ row centers. Both packages feature a heat-sinkable tab for improved thermal characteristics. The lead configurations allow easy attachment of a heat sink while fitting standard integrated circuit sockets or printed wiring board layout.

FUNCTIONAL BLOCK DIAGRAM



DWG. NO. SG-103

TYPICAL INPUT CIRCUIT



DWG. NO. A-12,520

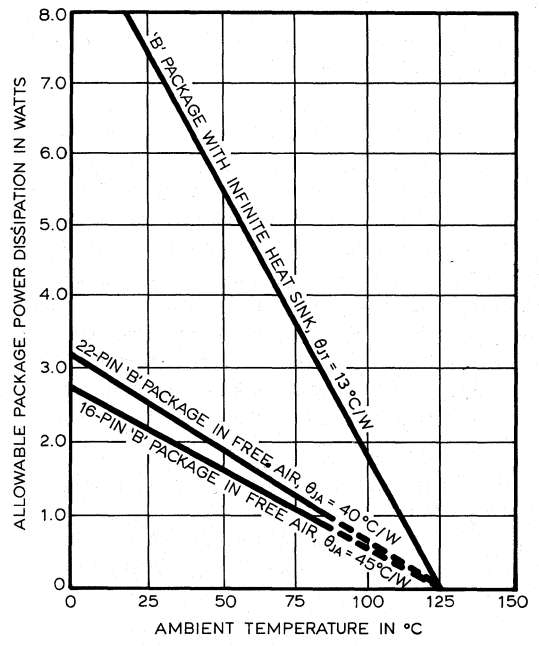
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE}
- UCN-5183B and UCN-5814B ..... 50 V
- UCN-5813B-1 and UCN-5814B-1 ..... 80 V

Output Sustaining Voltage, $V_{CE(sus)}$
- UCN-5813B and UCN-5814B ..... 35 V
- UCN-5813B-1 and UCN-5814B-1 ..... 50 V

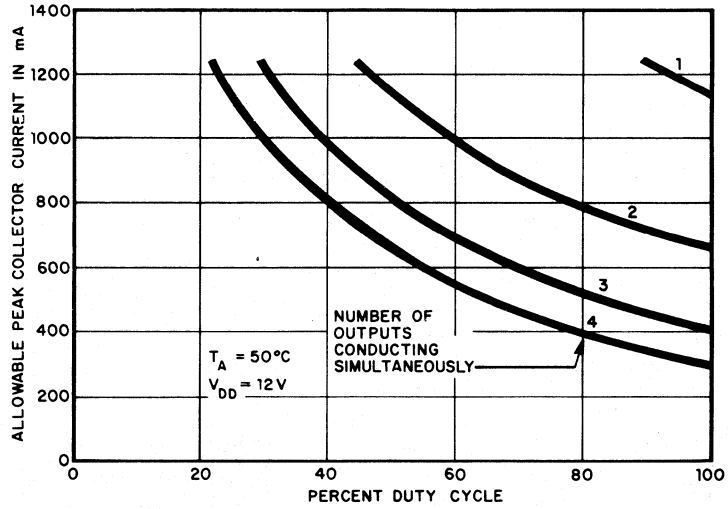
Output Current, I_{OUT} ..... 1.5 A
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A .. −20°C to +85°C
Storage Temperature Range, T_S ... −55°C to +125°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



DWG. NO. SG-104

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

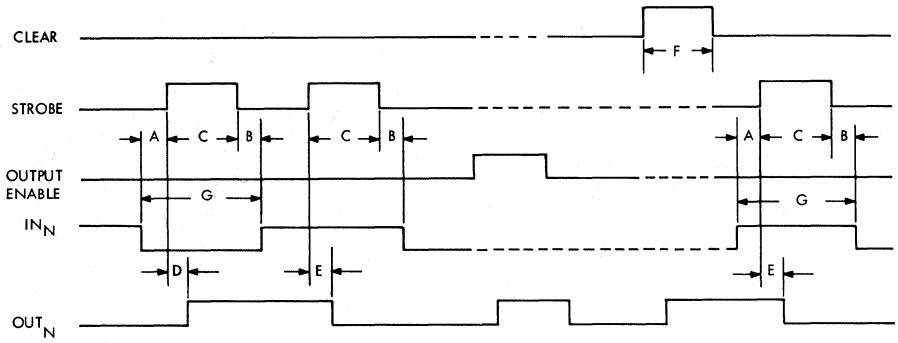


DWG. NO. SG-105

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} = +70°C$, $V_{DD} = 5.0$ V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	All	V_{OUT} = 50 V	—	100	μA
		Suffix -1	V_{OUT} = 80 V	—	100	μA
Output Sustaining Voltage	$V_{CE(sus)}$	All	I_{OUT} = 1.0 A, L = 2 mH	35	—	V
		Suffix -1	I_{OUT} = 1.0 A, L = 2 mH	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	All	I_{OUT} = 1.0 A	—	1.25	V
			I_{OUT} = 1.25 A	—	1.4	V
Clamp Diode Leakage Current	I_R	All	V_R = 50 V	—	100	μA
		Suffix -1	V_R = 80 V	—	100	μA
Clamp Diode Forward Voltage	V_F	All	I_F = 1.0 A	—	2.0	V
Input Voltage	$V_{IN(0)}$	All	V_{DD} = 5.0 V	−0.3	0.8	V
	$V_{IN(1)}$	All	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
Input Resistance	R_{IN}	All	V_{DD} = 5.0 V, Except 5813B/13B-1 STROBE Input	100	—	kΩ
		5813B/13B-1	V_{DD} = 5.0 V, STROBE Input	50	—	kΩ
		All	V_{DD} = 12 V, Except 5813B/13B-1 STROBE Input	50	—	kΩ
		5813B/13B-1	V_{DD} = 12 V, STROBE Input	25	—	kΩ
Supply Current	$I_{DD(OFF)}$	All	V_{DD} = 5.0 V, All Outputs OFF, All Inputs = 0 V	—	100	μA
			V_{DD} = 12 V, All Outputs OFF, All Inputs = 0 V	—	200	μA
	$I_{DD(ON)}$	All	V_{DD} = 5.0 V, One Output ON, All Inputs = 0 V	—	5.0	mA
			V_{DD} = 12 V, One Output ON, All Inputs = 0 V	—	10	mA

5



DWG. NO. A-10,895A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) ..... 50 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 50 ns
C. Minimum strobe pulse width ..... 125 ns
D. Typical time between strobe activation and output on to off transition ..... 500 ns
E. Typical time between strobe activation and output off to on transition ..... 500 ns
F. Minimum clear pulse width (UCN-5814B only) ..... 300 ns
G. Minimum data pulse width ..... 225 ns

TRUTH TABLE

DATA IN	INPUT ENABLE	STROBE	CLEAR	OUTPUT ENABLE	LATCH CONTENTS	OUTPUT
UCN-5813B						
X	—	X	—	1	X	OFF
X	—	0	—	0	n-1	n-1
0	—	1	—	0	0	OFF
1	—	1	—	0	1	ON
UCN-5814B						
X	X	X	X	1	X	OFF
X	X	X	1	X	0	OFF
X	X	0	0	0	n-1	n-1
X	0	X	0	0	n-1	n-1
0	1	1	0	0	0	OFF
1	1	1	0	0	1	ON

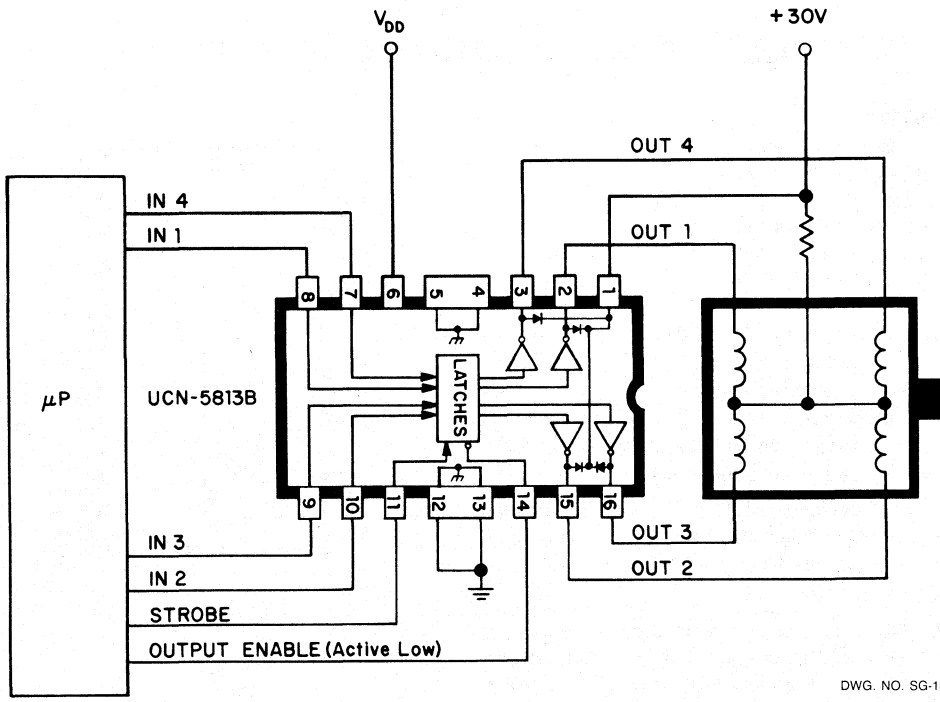
X = irrelevant
n-1 = previous output state

Information present at an input is transferred to its latch when the STROBE is high. A high OUTPUT ENABLE will force all outputs to the OFF condition, but does not affect the state of the latches. When OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

For the UCN-5814B, data is entered only when both STROBE and INPUT ENABLE are high. A high CLEAR input will set all latches to the output OFF condition, regardless of input data, INPUT ENABLE, or STROBE conditions.

TYPICAL APPLICATION

UNIPOLAR STEPPER-MOTOR DRIVE



DWG. NO. SG-106

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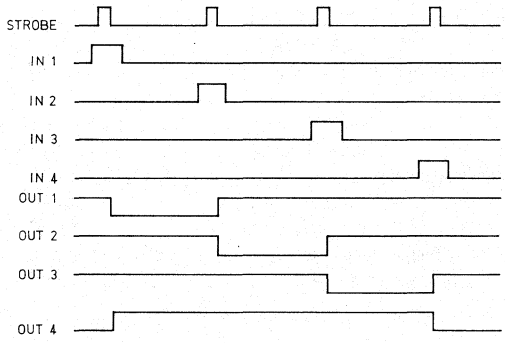
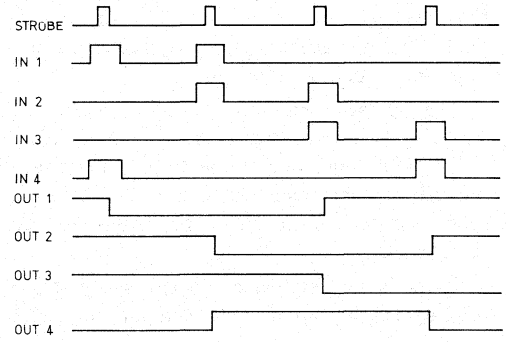
UNIPOLAR WAVE DRIVE



DWG. NO. A-11,446

UNIPOLAR 2-PHASE DRIVE

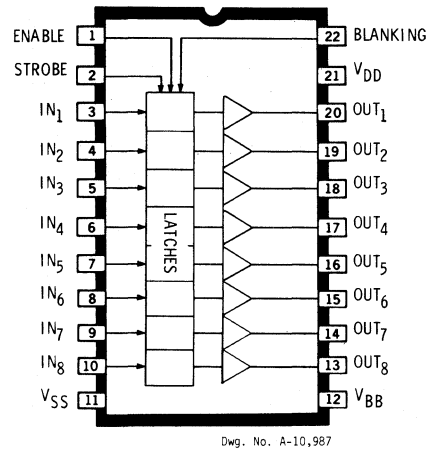


DWG. NO. A-11,447

UCN-5815A
BiMOS II 8-BIT LATCHED SOURCE DRIVER

FEATURES

- 4.4 MHz Minimum Date-Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range



Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCN-5815A BiMOSII integrated circuit consists of eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

Selected devices (UCN-5815A-1) have maximum output ratings of 80 V and 40 mA per driver. In all other respects, the UCN-5815A-1 is identical to the 60 V UCN-5815A.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 12 V. When employed with either standard TTL or low-speed TTL logic, the UCN-5815A may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures up to 60°C. To simplify circuit board layout, output pins are opposite input pins.

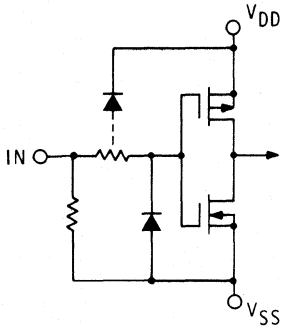
A minimum component display subsystem, requiring few or no discrete components, can be assembled using the UCN-5815A with the UCN-5810A, UCN-5812A or UCN-5818A serial-to-parallel latched driver.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCN-5815A) ..... 60 V
(UCN-5815A-1) ..... 80 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}
(UCN-5815A) ..... 5.0 V to 60 V
(UCN-5815A-1) ..... 5.0 V to 80 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... 2.0 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 20 mW/°C above T_A = +25°C.

TYPICAL INPUT CIRCUIT



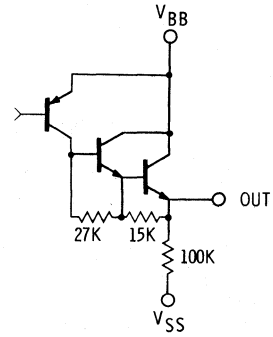
Dwg. No. A-12,517

MAXIMUM DUTY CYCLE

Number of Outputs ON (I_{OUT} = −25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of +50°C	+60°C	+70°C
8	100%	100%	86%
7	100%	100%	98%
6	100%	100%	100%
1	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL OUTPUT DRIVER



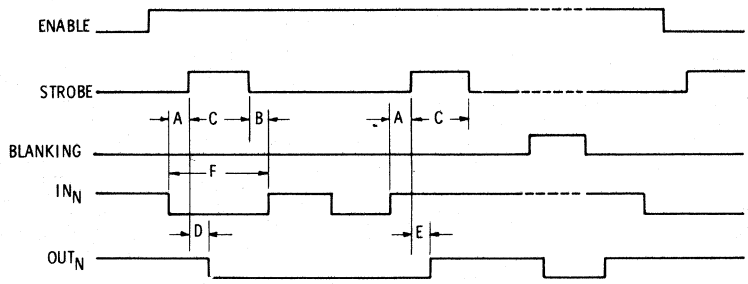
Dwg. No. A-12,546

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 4.5 V to 12 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = −25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = −25 mA, V_{BB} = 80 V, UCN-5815A-1 only	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	850	µA
		V_{BB} = V_{OUT} = 80 V, UCN-5815A-1 only	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = 70°C	—	−15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF, All outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

5



Dwg. No. A-10,991

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B.	Minimum Data Active Time After Strobe Disabled (Data Hold Time)	50 ns
C.	Minimum Strobe Pulse Width	125 ns
D.	Typical Time Between Strobe Activation and Output ON to OFF Transition	5.0 µs
E.	Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F.	Minimum Data Pulse Width	225 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz, minimum data input rate with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

UCN-5815A TRUTH TABLE

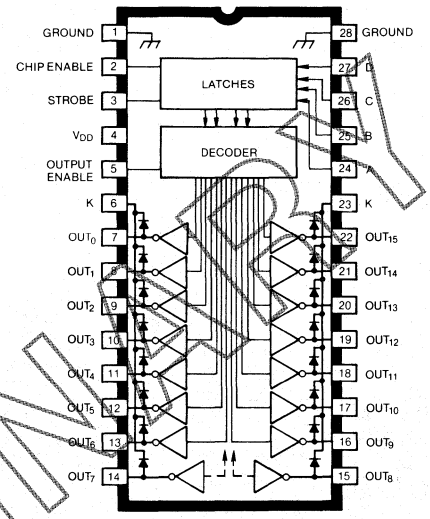
Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

UCN-5816A
DECODER/LATCH/SINK DRIVER

FEATURES

- Addressable Data Entry
- 60 V Output Voltage
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Output Transient Protection
- STROBE, CHIP ENABLE, OUTPUT ENABLE* Functions



Dwg. No. A-14,320

This sixteen-bit, addressable, latched driver is used in a wide variety of power applications. The UCN-5816A can drive all types of common peripheral power loads, including lamps, relays, solenoids, LED's, printer heads, heaters, and stepper motors. It can also be used as a decoder driver for higher power loads requiring discrete power semiconductors.

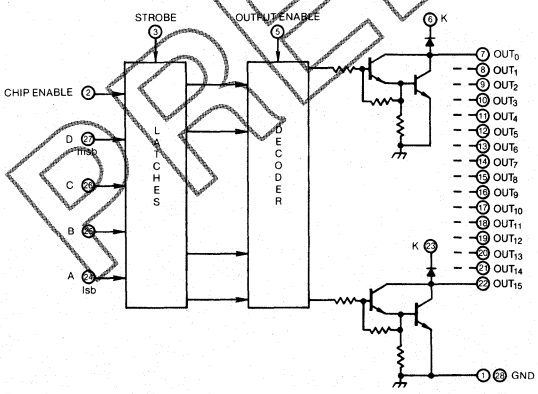
The UCN-5816A is capable of maintaining an output OFF voltage of 60 V and an output ON current of 500 mA.

The logic for this device is all new and is divided into sixteen latches, quadrant select, four 2-line to 4-line decoders, sixteen open-collector output drivers, and MOS control circuitry for CHIP ENABLE, OUTPUT ENABLE*, and STROBE functions. Any of the sixteen power loads can be addressed individually and can be turned ON or OFF independent of the other loads.

This device is supplied in a 28-pin dual in-line plastic package for operation over the temperature range of −20°C to +85°C.

*Output Enable—Active Low

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-14,319

ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Output Voltage, V_{CE}	60 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	2.5 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 25 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 60\ V$, $T_A = +25°C$	—	—	50	μA
		$V_{CE} = 60\ V$, $T_A = +70°C$	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100$ ma	—	0.9	1.1	V
		$I_C = 200$ mA	—	1.1	1.3	V
		$I_C = 350$ mA, $V_{DD} = 7.0\ V$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		−0.3	—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	—	V
		$V_{DD} = 5.0\ V$ (See note)	3.5	—	5.3	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	200	—	kΩ
		$V_{DD} = 5.0\ V$	100	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	2.0	3.0	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	1.0	1.5	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, OE = $V_{DD} = 5\ V$	—	—	100	μA
		All Drivers OFF, All Inputs = 0 V, OE = $V_{DD} = 12\ V$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 60\ V$, $T_A = +25°C$	—	—	50	μA
		$V_R = 60\ V$, $T_A = +70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350$ mA	—	1.5	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".
For Timing Conditions, see UCN-5800/01A.

TRUTH TABLE

INPUTS																			
STR	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	X	1
OE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
CE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	0
D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	X	X	X
C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	X	X	X
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	X	X	X
A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	X	X	X

OUTPUTS (all outputs OFF unless otherwise specified)																		
0	ON																	
1		ON																
2			ON															
3				ON														
4					ON													
5						ON												
6							ON										↑	↑
7								ON									Q_0	ALL
8									ON									OFF
9										ON							↓	↓
10											ON							
11												ON						
12													ON					
13														ON				
14															ON			
15																ON		

NOTE: Q_0 = The Output Conditions before the 1 to 0 transition of the STROBE pin.
1 = High Logic Level 0 = Low Logic Level X = Irrelevant

UCN-5818AF AND UCN-5818EPF BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

With Active DMOS Pulldowns

FEATURES

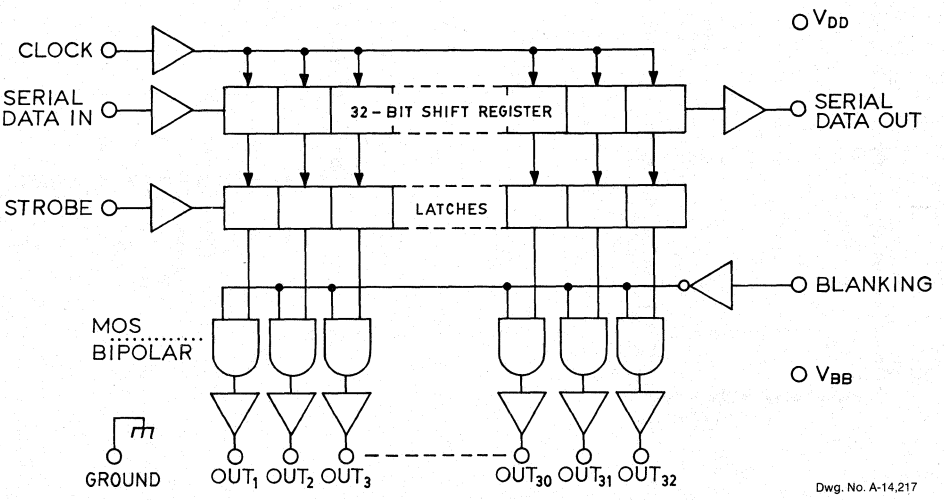
- 60 V or 80 V Source Outputs
- High-Speed Source Drivers
- Active DMOS Pull-Downs
- Low-Output Saturation Voltages
- Low-Power CMOS Logic and Latches
- 3.3 MHz Minimum Data Input Rate
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

DESIGNED primarily for use with vacuum-fluorescent displays, the UCN-5818AF and UCN-5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interface with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and −40 mA output ratings, allowing them to be used in many other peripheral power driver applications. Selected devices suffix "-1") have maximum output ratings of 80 V. In all other respects, devices with and without the "-1" suffix are identical.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of −20°C to +85°C.

Continued

FUNCTIONAL BLOCK DIAGRAM



The UCN-5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirements, and low output saturation voltage permits operation with minimum junction temperature rise. The "A" package allows all 32 outputs to be operated at −25 mA continuously at ambient temperature up to 60°C.

For high-density packaging applications, the UCN-5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface moutning on solder lands with 0.050" (1.27 mm) centers. The PLCC allows −25 mA continuous operation of up to 21 outputs simultaneously at ambient temperatures to 60°C.

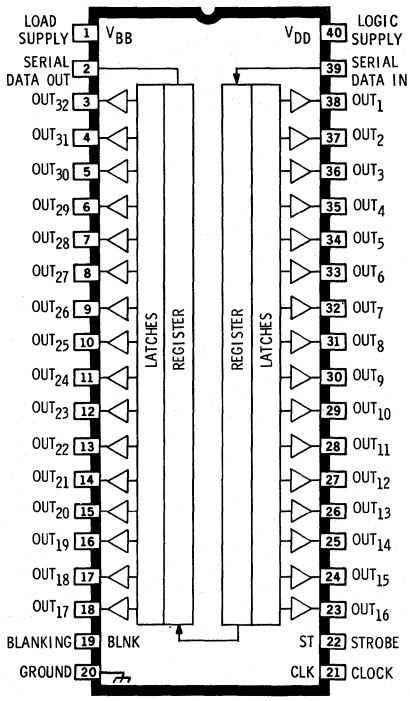
ABSOLUTE MAXIMUM RATINGS at T_A = 20l°C

Logic Supply Voltage, V_{DD}	15 V
Driver Supply Voltage, V_{BB}	60 V
(Suffix "-1")	80 V
Continuous Output Current, I_{OUT}	−40 to +15 mA
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D (UCN-5818AF)	2.8 W*
(UCN-5818EPF)	2.0 W†
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at rate of 28 mW/°C above T_A = +25°C
†Derate at rate of 20 mW/°C above T_A = +25°C

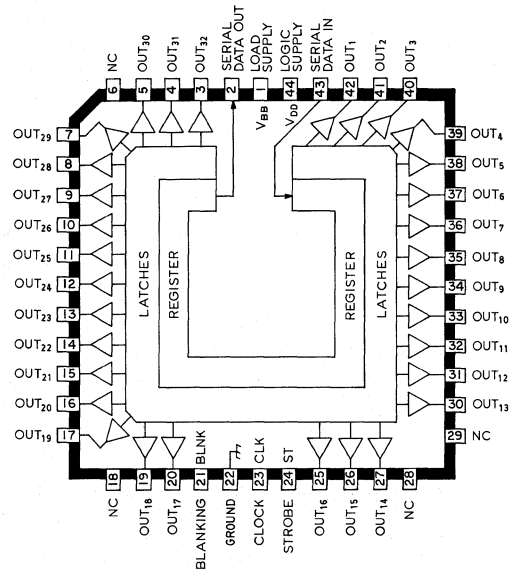
Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5818AF



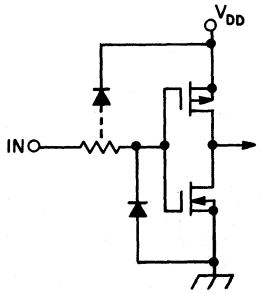
DWG. NO A-14, 313

UCN-5818EPF



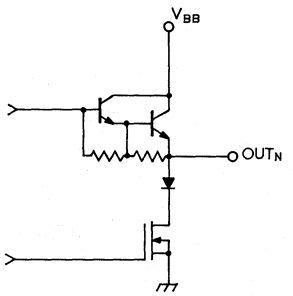
Dwg. No. A-14,218

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER

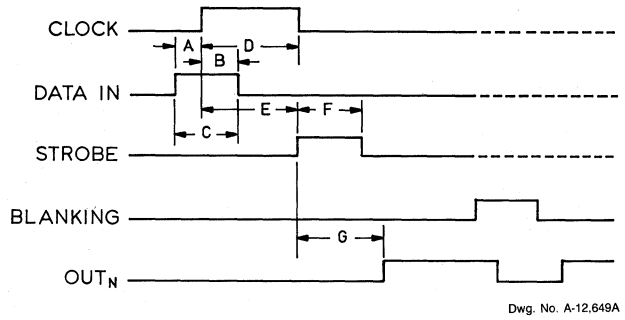


Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V (UCN-5818AF/EPF) or 80 V (suffix '-1') unless otherwise noted

Characteristic	Symbol	Test Conditions	Limits at $V_{DD} = 5$ V			Limits at $V_{DD} = 12$ V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 0$ V, $T_A = +70°C$	—	−5.0	−15	—	−5.0	−15	μA
Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -25$ mA, $V_{BB} = 60$ V	58	58.5	—	58	58.5	—	V
		$I_{OUT} = -25$ mA, $V_{BB} = 80$ V*	78	78.5	—	78	78.5	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1$ mA	—	2.0	3.0	—	—	—	V
		$I_{OUT} = 2$ mA	—	—	—	—	2.0	3.0	V
Output Pull-Down Current	$I_{OUT(0)}$	$V_{OUT} = 5$ V to V_{BB}	2.0	3.5	—	—	—	—	mA
		$V_{OUT} = 20$ V to V_{BB}	—	—	—	8.0	13	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	+0.8	−0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}$	—	0.05	0.5	—	0.1	1.0	μA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−0.05	−0.5	—	−1.0	−1.0	μA
Serial Data Output Voltage	$V_{OUT(1)}$	$I_{OUT} = -200$ μA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	$I_{OUT} = 200$ μA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	100	200	—	200	400	μA
	$I_{DD(0)}$	All Outputs Low	—	100	200	—	200	400	μA
	$I_{BB(1)}$	Outputs High, No Load	—	1.5	3.0	—	1.5	3.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	μA
Blanking to Output Delay	t_{PHL}	$C_L = 30$ pF	—	300	550	—	125	150	ns
	t_{PLH}	$C_L = 30$ pF	—	250	450	—	170	200	ns
Output Fall Time	t_f	$C_L = 30$ pF	—	1000	1250	—	250	300	ns
Output Rise Time	t_r	$C_L = 30$ pF	—	150	170	—	150	170	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
*UCN-5818AF-1 and UCN--5818EPF-1 only.



Dwg. No. A-12,649A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$
					$X\ X\ X\ \ldots X\ X$	H	$L\ L\ L\ \ldots L\ L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

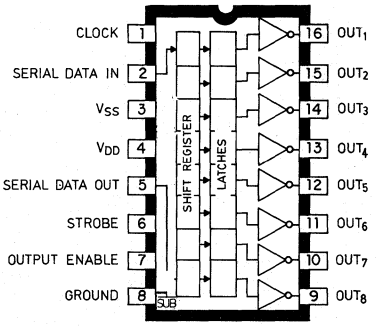
SERIES UCN-5820A
BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 3.3 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- 16-Pin Dual In-Line Plastic Package

A COMBINATION of bipolar and MOS technology gives the Series UCN-5820A an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers. Except for maximum driver output voltage ratings, the UCN-5821A, UCN-5822A, and UCN-5823A are identical.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.



DWG.NO. A-11,388B

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCN-5821A) ..... 50 V
(UCN-5822A) ..... 80 V
(UCN-5823A) ..... 100 V
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... 500 mA
Package Power Dissipation, P_D ..... 1.67 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = +25°C

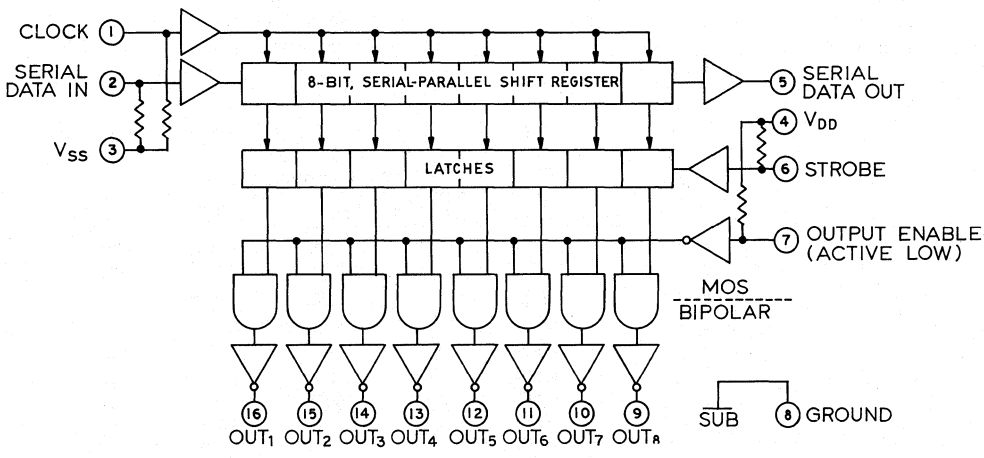
Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	73%	62%	55%	47%	40%
7	83%	71%	62%	54%	46%
6	97%	82%	72%	63%	53%
5	100%	98%	87%	75%	63%
4	100%	100%	100%	93%	79%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

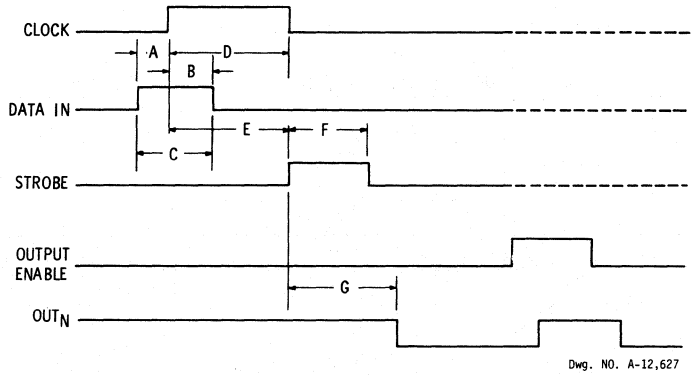
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCN-5821A	$V_{OUT} = 50\,V$	—	50	µA
			$V_{OUT} = 50\,V$, $= +70°C$	—	100	µA
		UCN-5822A	$V_{OUT} = 80\,V$	—	50	µA
			$V_{OUT} = 80\,V$, $T_A = +70°C$	—	100	µA
		UCN-5823A	$V_{OUT} = 100\,V$	—	50	µA
			$V_{OUT} = 100\,V$, $T_A = +70°C$	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\,mA$	—	1.1	V
			$I_{OUT} = 200\,mA$	—	1.3	V
			$I_{OUT} = 350\,mA$, $V_{DD} = 7.0\,V$	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 12\,V$	10.5	—	V
			$V_{DD} = 10\,V$	8.5	—	V
			$V_{DD} = 5.0\,V$	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 12\,V$	50	—	kΩ
			$V_{DD} = 10\,V$	50	—	kΩ
			$V_{DD} = 5.0\,V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One Driver ON, $V_{DD} = 12\,V$	—	4.5	mA
			One Driver ON, $V_{DD} = 10\,V$	—	3.9	mA
			One Driver ON, $V_{DD} = 5.0\,V$	—	2.4	mA
	$I_{DD(OFF)}$	ALL	$V_{DD} = 5.0\,V$, All Drivers OFF, All Inputs $= 0\,V$	—	1.6	mA
			$V_{DD} = 12\,V$, All Drivers OFF, All Inputs $= 0\,V$	—	2.9	mA

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-11,391D



TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

5

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

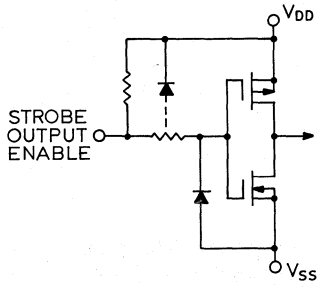
When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

SERIES UCN-5820A TRUTH TABLE

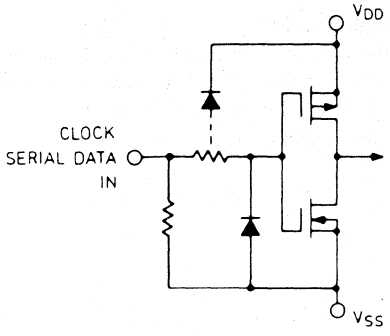
Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⎍	H R_1 R_2 ..... R_7	R_7				
L	⎍	L R_1 R_2 ..... R_7	R_7				
X	⎎	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL INPUT CIRCUITS

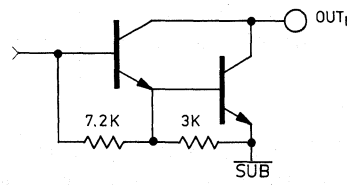


Dwg. No. A-12,658



Dwg. No. A-12,659

TYPICAL OUTPUT DRIVER

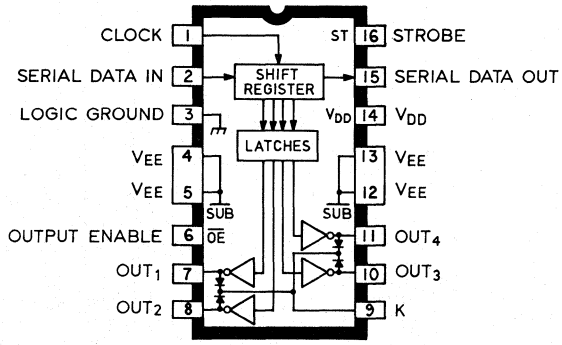


Dwg. No. A-14,314

UCN-5825B AND UCN-5826B
BiMOS II HIGH-CURRENT, SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 2 A Open Collector Outputs
- 60 V or 80 V Minimum Output Breakdown
- 35 V or 60 V Sustaining Voltage
- Output-Transient Protection
- Low-Power CMOS Logic and Latches
- Typical Data Input Rate > 5 MHz
- Internal Pull-Down Resistors
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Thermal Shutdown Circuitry



Dwg. No. A-12,557

UCN-5825B and UCN-5826B BiMOS II integrated circuits combine a 4-bit CMOS shift register, associated latches, control circuitry, and level shifting, with bipolar Darlington outputs and transient-suppression diodes for inductive load applications.

The high-current, serial-input, latched drivers can be used with relays, solenoids, stepper motors, LED displays, incandescent displays, and other high-power loads. Control circuitry for both devices includes STROBE and OUTPUT ENABLE functions, and an internal latch that disables outputs at power-up and provides thermal shutdown protection.

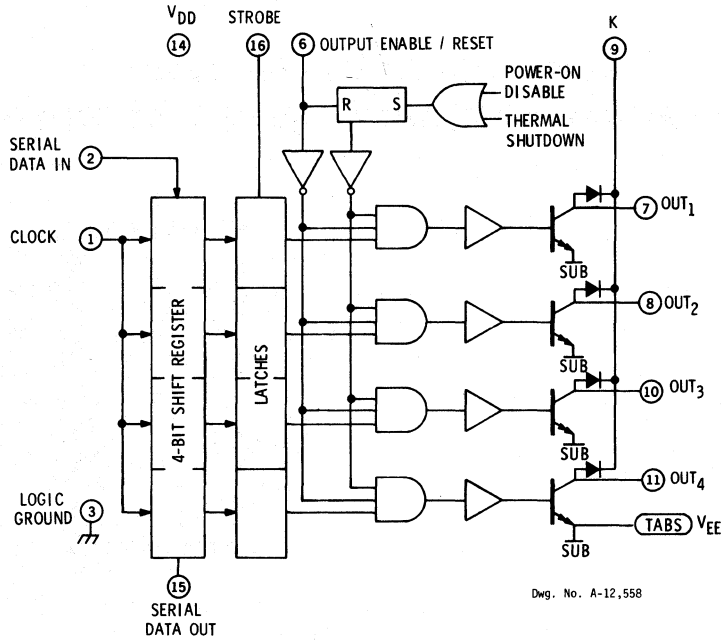
Except for output-voltage ratings, the UCN-5825B and UCN-5826B drivers are identical. The former is rated for operation to 60 V (35 V sustaining); the latter has a minimum output breakdown rating of 80 V (60 V sustaining).

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to insure a proper input-logic high level. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. With a 5 V supply, BiMOS II devices typically operate at data-input rates above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Monolithic construction and a 16-pin dual in-line package with copper heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent package power dissipation rating, minimum size, and ease of installation. The package configuration is suitable for automatic insertion, allows easy attachment of an inexpensive heat sink, and fits a standard IC socket or printed wiring board layout.

Both devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, simultaneous operation of all drivers may require a reduction in duty cycle.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,558

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

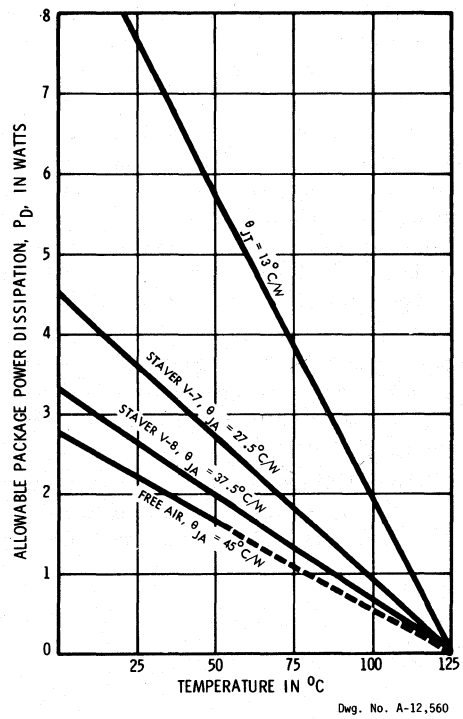
Output Voltage, V_{CE}
(UCN-5825B) ..... 60 V
(UCN-5826B) ..... 80 V
Output Voltage, $V_{CE(sus)}$
(UCN-5825B) ..... 35 V*
(UCN-5826B) ..... 60 V*
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 15 V
V_{DD} with reference to V_{EE} ..... 25 V
Emitter Supply Voltage, V_{EE} ..... −20 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 2 A
Allowable Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*For inductive load applications: The sum of the load supply voltage and clamping voltage(s).

Note: Output-current rating may be limited by duty cycle, ambient temperature, heat sinking, and a number of outputs conducting. Under any combination of conditions, do not exceed the specified maximum current rating and a junction temperature of +125°C.

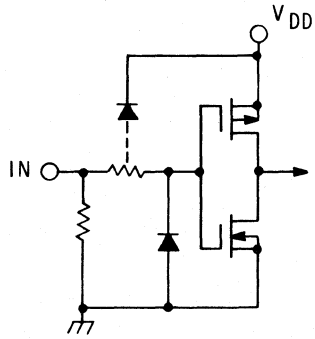
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



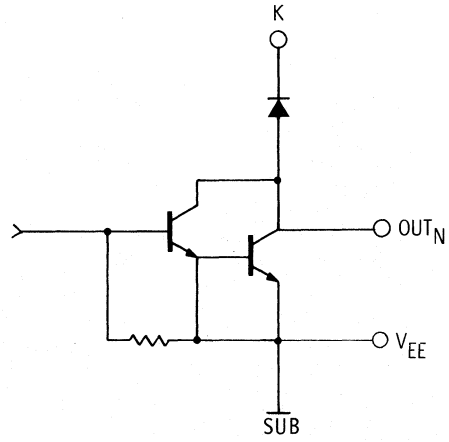
Dwg. No. A-12,560

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,559

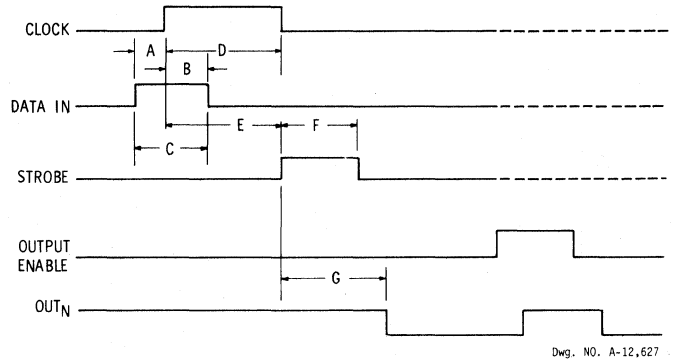
TYPICAL OUTPUT DRIVER



Dwg. No. A-12,561A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 60 V, V_{DD} = 5 V to 12 V, V_{EE} = 0 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	UCN-5825B	T_A = +25°C	—	100	µA
			T_A = +70°C	—	500	µA
		UCN-5826B	V_{CC} = 80 V, T_A = +25°C	—	100	µA
			V_{CC} = 80 V, T_A = +70°C	—	500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	I_{OUT} = 1.75 A	—	1.75	V
Output Sustaining Voltage	$V_{CE(SAT)}$	UCN-5825B	I_{OUT} = 1.75 A, L = 2 mH	35	—	V
		UCN-5826B	I_{OUT} = 1.75 A, L = 2 mH	60	—	V
Clamp Diode Leakage Current	I_R	UCN-5825B	V_R = 60 V	—	100	µA
		UCN-5826B	V_R = 80 V	—	100	µA
Clamp Diode Forward Voltage	V_F	Both	I_F = 1.75 A	—	2.0	V
Input Voltage	$V_{IN(1)}$	Both	V_{DD} = 5.0 V	3.5	5.3	V
			V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	Both	V_{DD} = 5 V to 12 V	−0.3	+0.8	V
Input Resistance	R_{IN}	Both	V_{DD} = 5.0 V	100	—	kΩ
			V_{DD} = 12 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	Both	V_{DD} = 5.0 V	—	20	kΩ
			V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{DD}	Both	All outputs OFF	—	3.0	mA
			All outputs ON	—	20	mA
Maximum Clock Frequency	f_C	Both		3.3	—	MHz
Turn-ON Delay	t_{PHL}	Both	0.5 E_{OE} to 0.5 E_{out}	—	1.0	µs
Turn-OFF Delay	t_{PLH}	Both	0.5 E_{OE} to 0.5 E_{out}	—	2.0	µs
Propagation Delay	t_{PD}	Both	0.5 E_{OE} to 0.5 E_{out}	—	100	ns



TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of the latches.

Two additional functions serve to protect the system and the device. Either power-up or overheating will set an internal latch that disables the outputs. With the latch set, data can be shifted and latched while the outputs are disabled. To resume normal operation, the latch must be reset by toggling OUTPUT ENABLE a minimum of 500 ns.

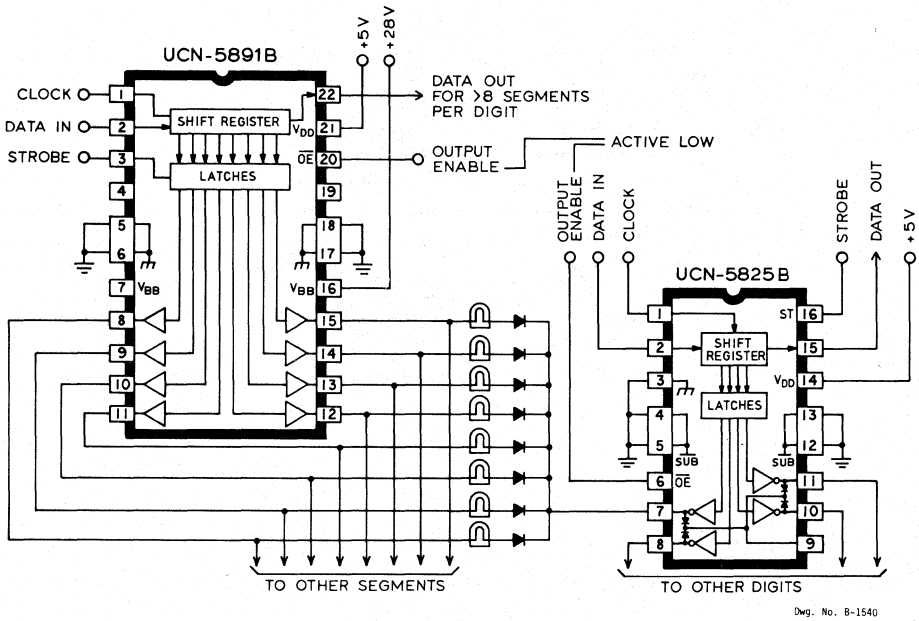
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents				Serial Data Output	Strobe Input	Latch Contents				Output Enable	Output Contents			
		I_1	I_2	I_3	I_4			I_1	I_2	I_3	I_4		I_1	I_2	I_3	I_4
H	↑	H	R_1	R_2	R_3	R_3										
L	↑	L	R_1	R_2	R_3	R_3										
X	↓	R_1	R_2	R_3	R_4	R_4										
		X	X	X	X	X	L	R_1	R_2	R_3	R_4					
		P_1	P_2	P_3	P_4	P_4	H	P_1	P_2	P_3	P_4	L	P_1	P_2	P_3	P_4
								X	X	X	X	H	H	H	H	H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL APPLICATION

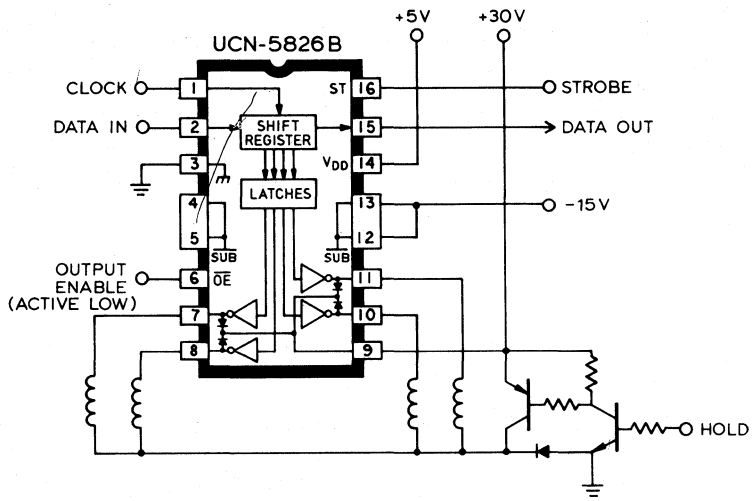
MULTIPLEXED INCANDESCENT LAMP DRIVE



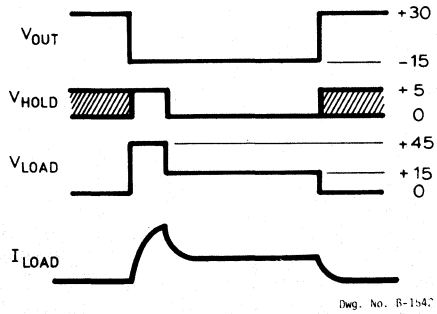
*Active Low

TYPICAL APPLICATION

BILEVEL HAMMER DRIVE



*Active Low



Dwg. No. B-1947

UCN-5832A AND UCN-5832C
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

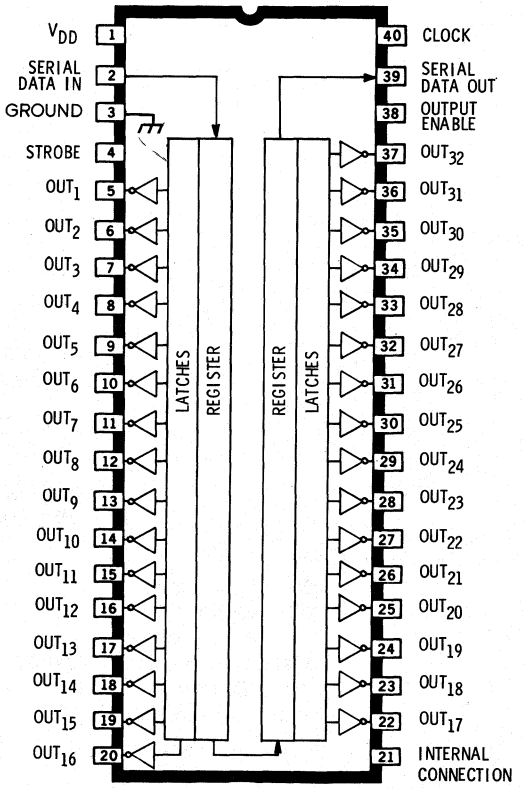
FEATURES

- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current Sink Outputs
- Low Saturation Voltage

INTENDED PRIMARILY to drive thermal printheads, Types UCN-5832A and UCN-5832C have been optimized for low output-saturation voltage, high-speed operation, and pin/pad configurations most convenient for the tight space requirements of high-resolution printheads. The integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 150 mA peak current. A combination of bipolar and MOS technologies gives BiMOS II arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

Type UCN-5832A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. Under normal operating conditions, all outputs of the packaged device will sustain 100 mA continuously without derating. Type UCN-5832C is an unpackaged, passivated, bare-back device in chip form. In this version, the shift register is divided into two 16-bit blocks for maximum flexibility. For either device, MOS serial outputs permit cascading for interface applications requiring additional drive lines.



Dwg. No. A-12,377A

A similar 32-bit serial-input latched source driver is available as UCN-5818A. High-voltage, high-current 8-bit devices are available in Series UCN-5820A.

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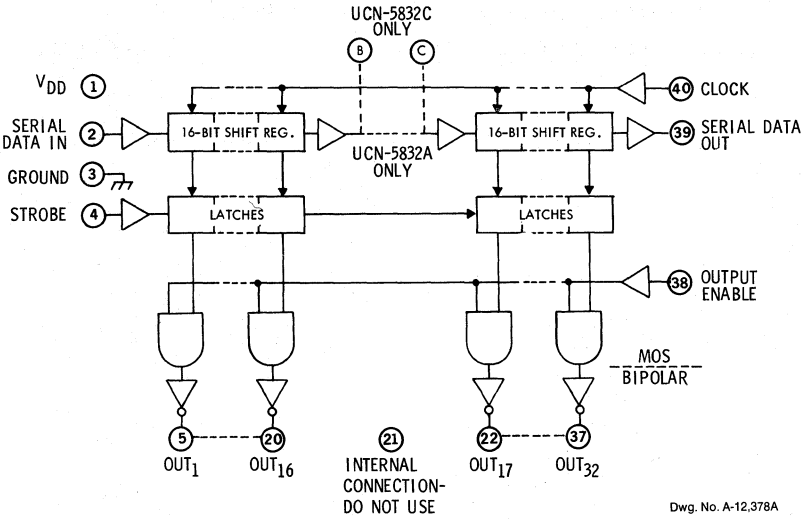
FUNCTIONAL BLOCK DIAGRAM



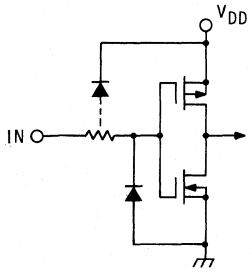
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} ..... 40 V
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 150 mA
Package Power Dissipation, P_D (UCN-5832A) ..... 2.8 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 28 mW/°C above T_A = +25°C

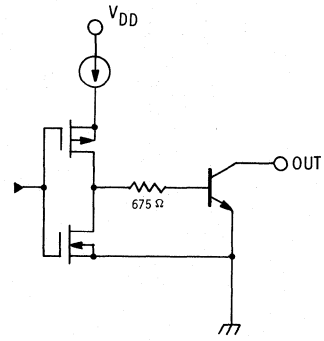
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,379A

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,380A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 40$ V, $T_A = 70°C$	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	275	mV
		$I_{OUT} = 100$ mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 3.5$ V	—	1.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−1.0	µA
Input Impedance	Z_{IN}	$V_{IN} = 3.5$ V	3.5	—	MΩ
Serial Data/Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, $I_{OUT} = 100$ mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	$I_{OUT} = 100$ mA, 10% to 90%	—	1.0	µs
Output Fall Time	t_f	$I_{OUT} = 100$ mA; 90% to 10%	—	1.0	µs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

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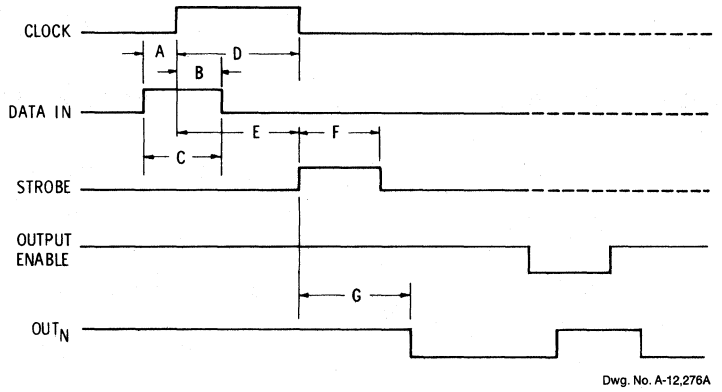


Dwg. No. A-12,276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

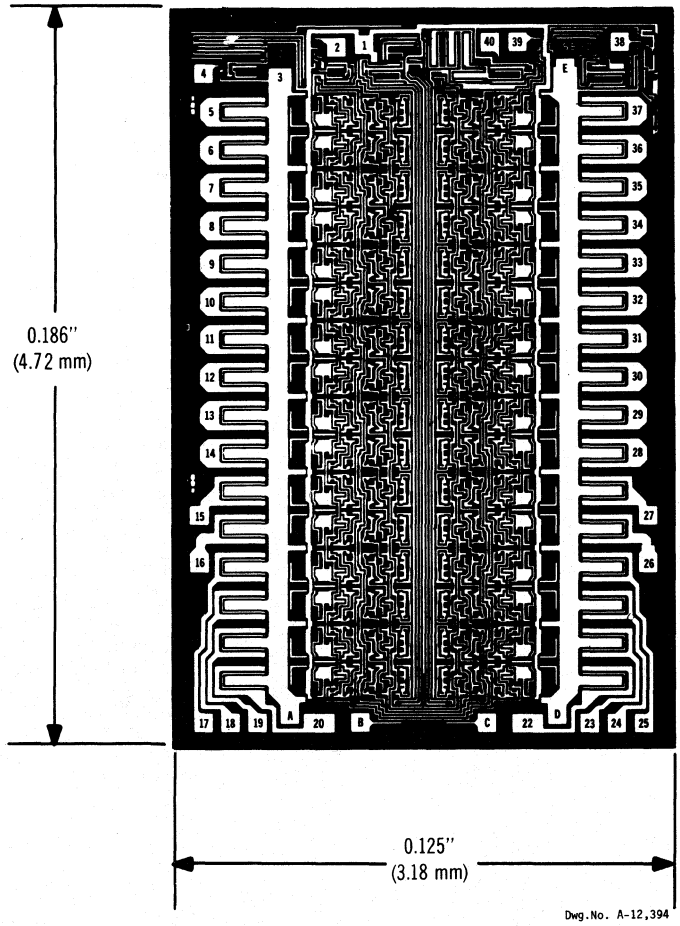
When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					$X\ X\ X\ \ldots X\ X$	L	$H\ H\ H\ \ldots H\ H$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5832C



UCN-5832 chips are of silicon planar epitaxial construction. They are identical to those used for packaged devices. When assembled correctly, they should lead to a high final test yield. All chips are visually inspected for masking, diffusion, and scribing defects. Conformance to electrical parameters can be guaranteed (at additional charge) by performing measurements on packaged units assembled from a random sample taken from the lot.

The preferred method of sale for unpackaged die is in wafer form. These are identified as UCN-5832C*W* and are supplied in 4" (100 mm) wafers that have been tested (probed) in wafer form. Electrically defective devices are identified by ink dots during this operation. Wafers do not include visual die inspection. Orders for UCN-5832C*W* will be accepted only for complete wafers.

Because Sprague Electric Company does not control the customer packaging of UCN-5832C chips or UCN-5832C*W* wafers, Sprague Electric company assumes no liability for final electrical and reliability parameters.

	PAD DESIGNATIONS	
PAD	UCN-5832A	UCN-5832C
1	V_{DD}	V_{DD}
2	SERIAL DATA IN	SERIAL DATA IN_1
3	GROUND	GROUND*
4	STROBE	STROBE
5	OUT_1	OUT_1
6	OUT_2	OUT_2
7	OUT_3	OUT_3
8	OUT_4	OUT_4
9	OUT_5	OUT_5
10	OUT_6	OUT_6
11	OUT_7	OUT_7
12	OUT_8	OUT_8
13	OUT_9	OUT_9
14	OUT_{10}	OUT_{10}
15	OUT_{11}	OUT_{11}
16	OUT_{12}	OUT_{12}
17	OUT_{13}	OUT_{13}
18	OUT_{14}	OUT_{14}
19	OUT_{15}	OUT_{15}
A	—	GROUND*
20	OUT_{16}	OUT_{16}
B	—	SERIAL DATA OUT_{16}
21	INTERNAL CONNECTION—DO NOT USE	—
C	—	SERIAL DATA IN_{17}
22	OUT_{17}	OUT_{17}
D	—	GROUND*
23	OUT_{18}	OUT_{18}
24	OUT_{19}	OUT_{19}
25	OUT_{20}	OUT_{20}
26	OUT_{21}	OUT_{21}
27	OUT_{22}	OUT_{22}
28	OUT_{23}	OUT_{23}
29	OUT_{24}	OUT_{24}
30	OUT_{25}	OUT_{25}
31	OUT_{26}	OUT_{26}
32	OUT_{27}	OUT_{27}
33	OUT_{28}	OUT_{28}
34	OUT_{29}	OUT_{29}
35	OUT_{30}	OUT_{30}
36	OUT_{31}	OUT_{31}
37	OUT_{32}	OUT_{32}
38	OUTPUT ENABLE	OUTPUT ENABLE
E	—	GROUND*
39	SERIAL DATA OUT	SERIAL DATA OUT_{32}
40	CLOCK	CLOCK

*Bonding pads *A* or *3* and *D* or *E* must be connected to the substrate. For maximum output current capability, pads *A, D, E,* and *3* must all be bonded to the substrate.

UCN-5832EP
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVER

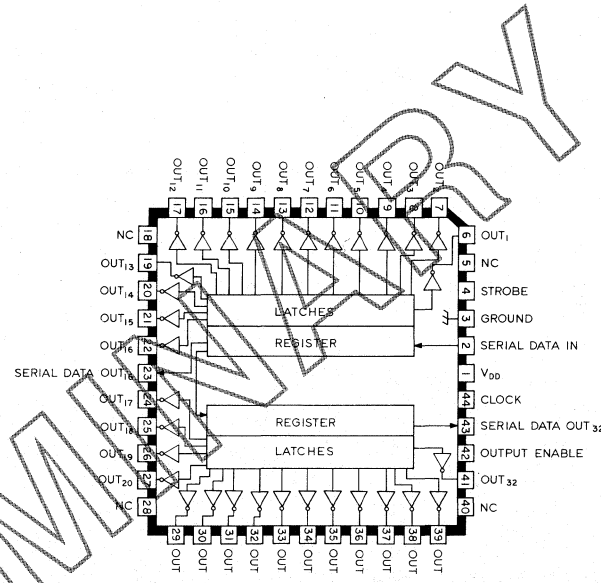
FEATURES

- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 40 V Current-Sink Outputs
- Low Saturation Voltage

Intended primarily to drive thermal printheads, the UCN-5832EP has been optimized for low output-saturation voltage, high-speed operation, and a pin configuration most convenient for the tight space requirements of high-resolution printheads.

The device has 32 bipolar open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems. Use of the driver with TTL may require input pull-up resistors to ensure an input logic high.

UCN-5832EP is packaged in a 44-pin plastic leaded chip carrier (quad) with 50-mil lead spacing.



Dwg. No. A-14,236

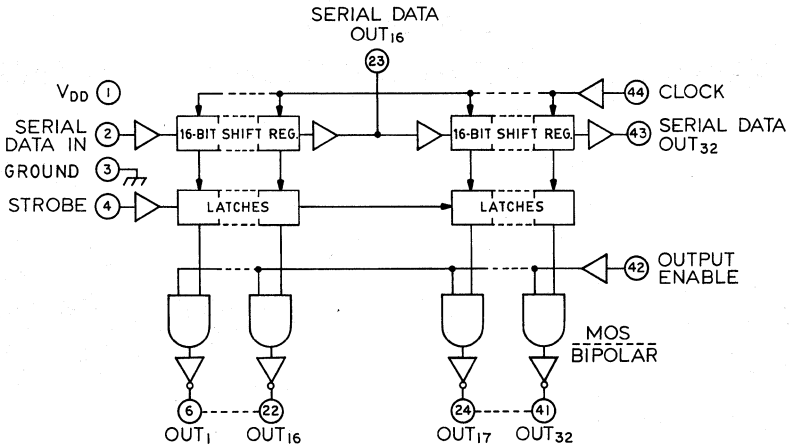
5

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT}	40 V
Logic Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	150 mA
Package Power Dissipation, P_D	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 20 mW/°C above T_A = +25°C

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

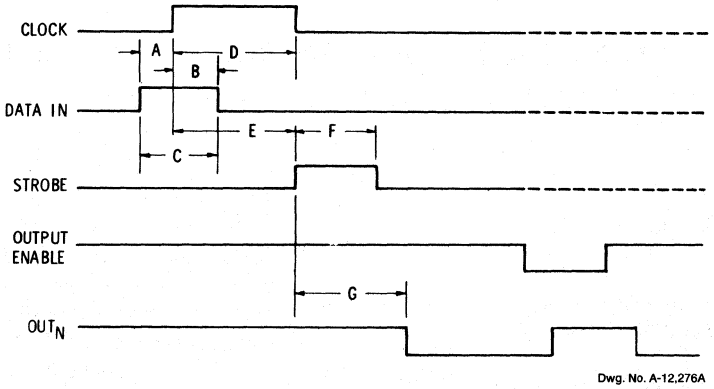


Dwg. No. A-14,237

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 40$ V, $T_A = 70°C$	—	10	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	275	mV
		$I_{OUT} = 100$ mA	250	550	mV
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{IN} = 3.5$ V	—	1.0	µA
	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	−1.0	µA
Input Impedance	Z_{IN}	$V_{IN} = 3.5$ V	3.5	—	MΩ
Serial Data/Output Resistance	R_{OUT}		—	20	kΩ
Supply Current	I_{DD}	One output ON, $I_{OUT} = 100$ mA	—	5.0	mA
		All outputs OFF	—	50	µA
Output Rise Time	t_r	$I_{OUT} = 100$ mA, 10% to 90%	—	1.0	µs
Output Fall Time	t_f	$I_{OUT} = 100$ mA; 90% to 10%	—	1.0	µs

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	↑	$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	↑	$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	↓	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					$X\ X\ X\ \ldots X\ X$	L	$H\ H\ H\ \ldots H\ H$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-5833A, UCN-5833C, UCN-5833EP
BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

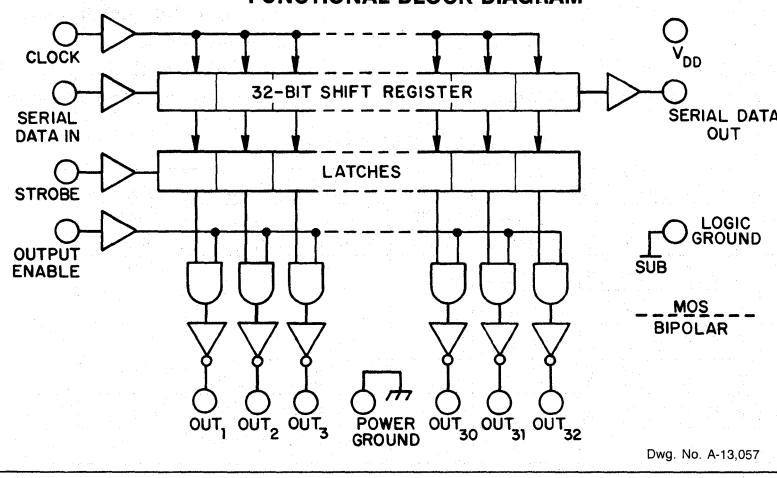
- 5 MHz Typical Data Input Rate
- 30 V Min. Output Breakdown
- Darlington Current-Sink Outputs
- Low-Power CMOS Logic and Latches
- Minimum Chip Size (UCN-5833C)

Designed primarily to reduce logic supply current, chip size and associated cost, the UCN-5833A/C/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits. The unpackaged UCN-5833C features minimum size and pad configurations most convenient for the tighter space requirements of high-resolution thermal printheads.

These 32-bit drivers have bipolar open-collector Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor/LSI-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN-5833A is supplied in a 40-pin dual in-line plastic package with 0.600″ (15.24 mm) row spacing. At an ambient temperature of +50°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. The UCN-5833C is an unpackaged, passivated, bare-back device in chip form. For high-density applications, the UCN-5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050″ (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

FUNCTIONAL BLOCK DIAGRAM



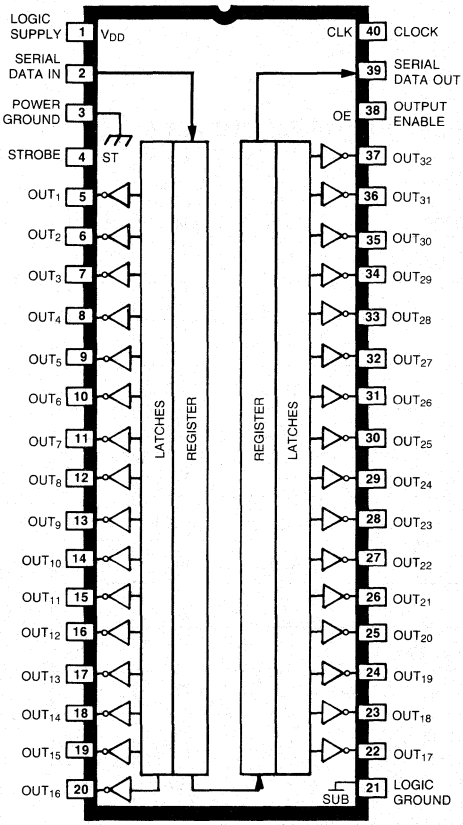
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT}	30 V
Logic Supply Voltage, V_{DD}	7.0 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} (each output)	125 mA
Package Power Dissipation, P_D (UCN-5833A)	2.8 W*
(UCN-5833EP)	2.0 W†
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 28 mW/°C above T_A = +25°C.
†Derate at the rate of 20 mW/°C above T_A = +25°C.

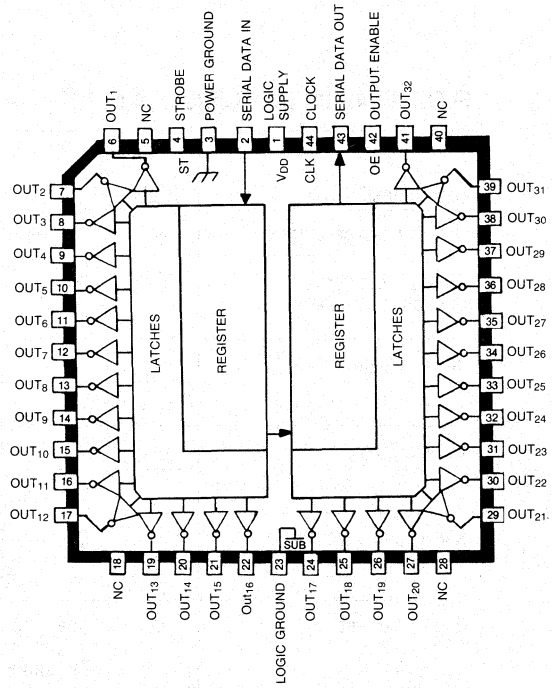
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

UCN-5833A



Dwg. No. A-13,048

UCN-5833EP



Dwg. No. A-13,049

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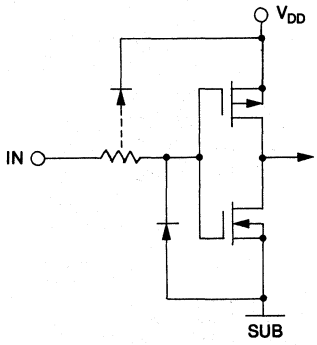
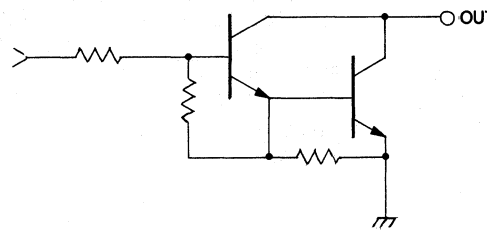
TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER

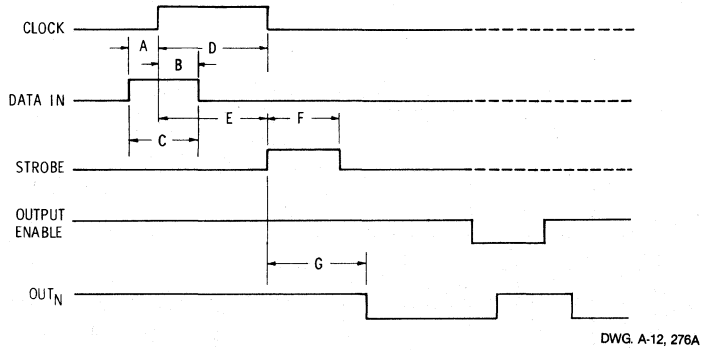


Dwg. No. A-13,051

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 30 V, T_A = 70°C	—	10	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 50 mA	—	1.2	V
		I_{OUT} = 100 mA	—	1.7	V
Input Voltage	$V_{IN(1)}$		3.5	5.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	1.0	μA
	$I_{IN(0)}$	V_{IN} = 0 V	—	−1.0	μA
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = −200 μA	4.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 μA	—	0.3	V
Supply Current	I_{DD}	One output ON, I_{out} = 100 mA	—	1.0	mA
		All outputs OFF	—	50	μA
Output Rise Time	t_r	I_{OUT} = 100 mA, 10% to 90%	—	500	ns
Output Fall Time	t_f	I_{OUT} = 100 mA, 90% to 10%	—	500	ns

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



DWG. A-12, 276A

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

		V_{DD} = 5.0V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are by-passed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.

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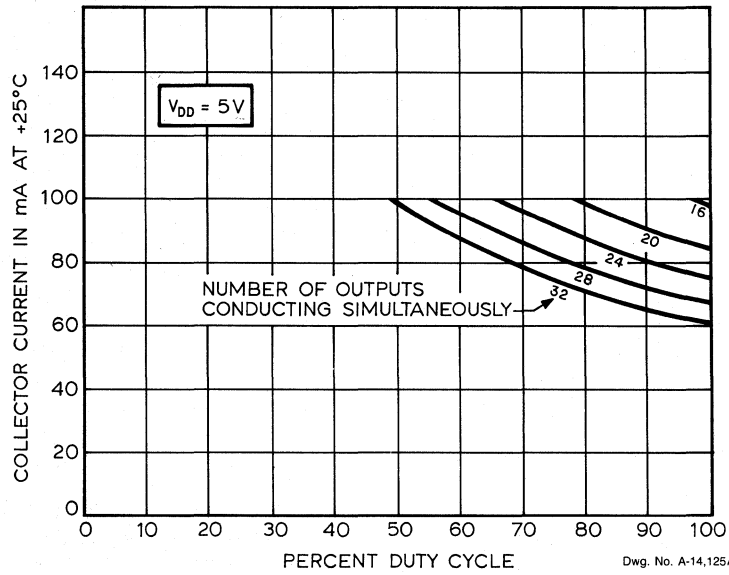
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Output Enable Input	Output Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	H $R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
L	⎍	L $R_1\ R_2\ \ldots R_{N-2}\ R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}\ R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}\ P_N$
					X X X ... X X	L	H H H ... H H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

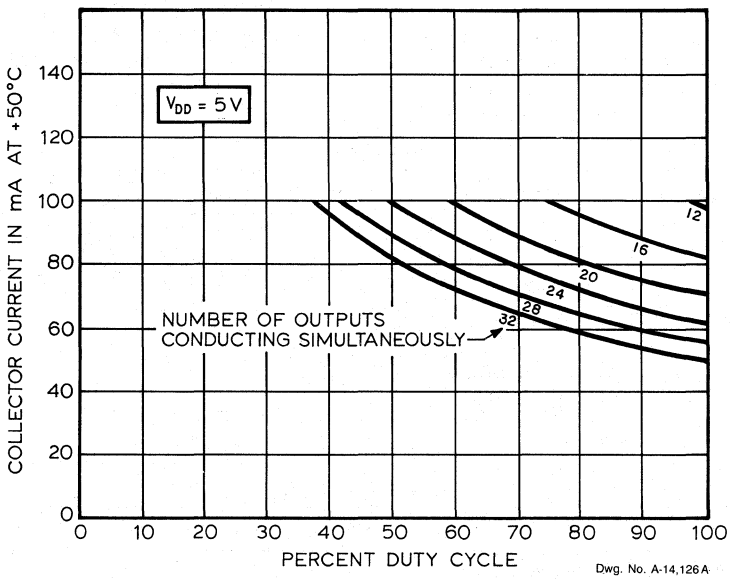
UCN-5833A

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +25°C



Dwg. No. A-14,125A

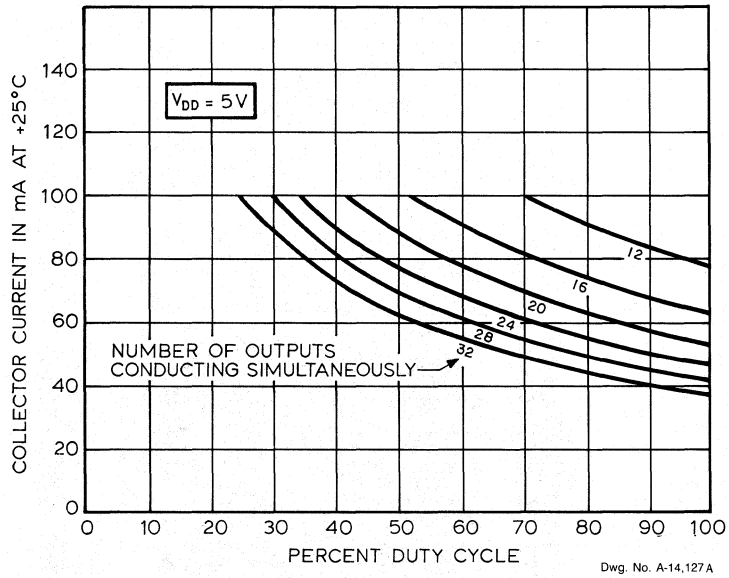
ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



Dwg. No. A-14,126A

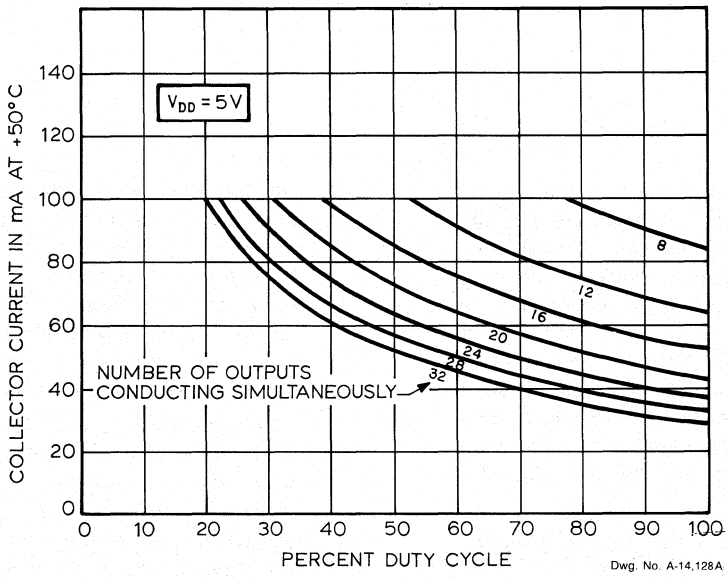
UCN-5833EP

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +25°C



Dwg. No. A-14,127A

ALLOWABLE COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



Dwg. No. A-14,128A

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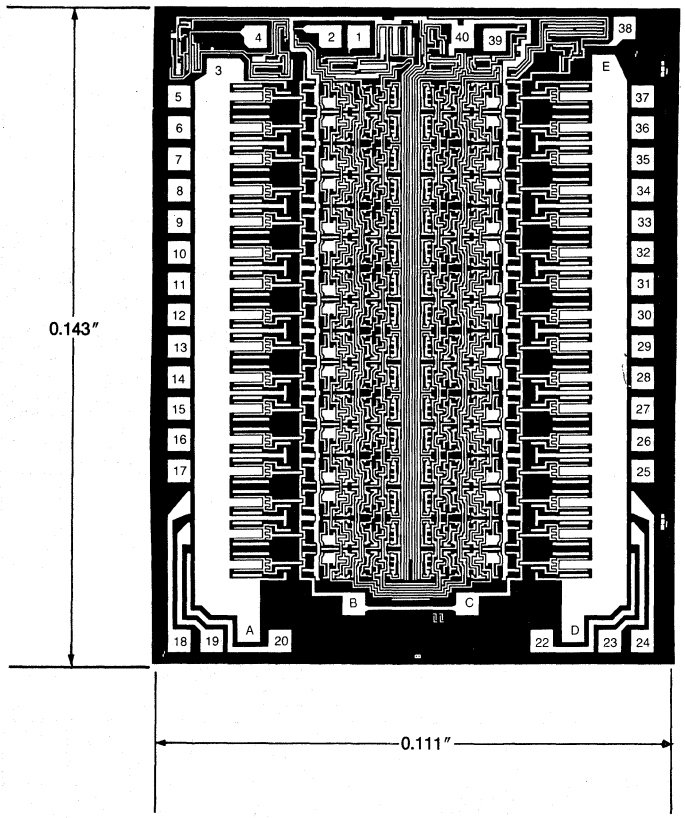
UCN-5833C



Dwg. No. A-13,052

UCN-5833C chips are of silicon planar epitaxial construction using a merged technology (bipolar power and low-power CMOS logic). They are identical to those used for packaged devices. The preferred method of sale for unpackaged die is in four-inch (100 mm) wafer form (UCN-5833CW). Users requiring separate, inspected die should contact the nearest Sprague sales office or representative. A select list of chip-processing operations, which offer value-added testing, inspection, and assembly, is available for referral.

All wafers from which chips are sold are processed through standard production techniques with 100% inspection after each critical process step. Die (in wafer form) are electrically tested as completely as practical. Defective devices are identified by an ink dot on the die. Complete conformance to all electrical specifications can be guaranteed (at additional cost) by performing measurements on packaged units assembled from a random sample of the device production lot.

Because Sprague Electric Company does not control the customer handling and packaging of die or wafers, Sprague Electric Company can assume no liability for final electrical or reliability failures that are determined to be the result of improper storage, assembly, or test by the customer.

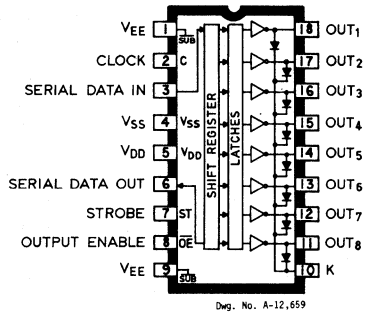
	PAD DESIGNATIONS	
PAD	UCN-5833A	UCN-5833C
1	V_{DD}	V_{DD}
2	SERIAL DATA IN	SERIAL DATA IN_1
3	POWER GROUND	POWER GROUND
4	STROBE	STROBE
5	OUT_1	OUT_1
6	OUT_2	OUT_2
7	OUT_3	OUT_3
8	OUT_4	OUT_4
9	OUT_5	OUT_5
10	OUT_6	OUT_6
11	OUT_7	OUT_7
12	OUT_8	OUT_8
13	OUT_9	OUT_9
14	OUT_{10}	OUT_{10}
15	OUT_{11}	OUT_{11}
16	OUT_{12}	OUT_{12}
17	OUT_{13}	OUT_{13}
18	OUT_{14}	OUT_{14}
19	OUT_{15}	OUT_{15}
A	—	POWER GROUND
20	OUT_{16}	OUT_{16}
B	—	LOGIC GROUND/SUB*
21	LOGIC GROUND/SUB*	—
C	—	LOGIC GROUND/SUB*
22	OUT_{17}	OUT_{17}
D	—	POWER GROUND
23	OUT_{18}	OUT_{18}
24	OUT_{19}	OUT_{19}
25	OUT_{20}	OUT_{20}
26	OUT_{21}	OUT_{21}
27	OUT_{22}	OUT_{22}
28	OUT_{23}	OUT_{23}
29	OUT_{24}	OUT_{24}
30	OUT_{25}	OUT_{25}
31	OUT_{26}	OUT_{26}
32	OUT_{27}	OUT_{27}
33	OUT_{28}	OUT_{28}
34	OUT_{29}	OUT_{29}
35	OUT_{30}	OUT_{30}
36	OUT_{31}	OUT_{31}
37	OUT_{32}	OUT_{32}
38	OUTPUT ENABLE	OUTPUT ENABLE
E	—	POWER GROUND
39	SERIAL DATA OUT	SERIAL DATA OUT_{32}
40	CLOCK	CLOCK

*The substrate must be connected to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal transistor operation. For maximum output current capability, pads *A, D, E,* and *3* must all be bonded to power ground.

SERIES UCN-5840A
BIMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- 18-Pin Dual In-Line Plastic Package



Dwg. No. A-12,659

INTEGRATING low-power CMOS logic and bipolar output power drivers permit Series UCN-5840A integrated circuits to be used in a wide variety of peripheral power driver applications. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlington output drivers.

Except for maximum driver output voltage ratings, the UCN-5841A, UCN-5842A, and UCN-5843A are identical. The UCN-5843A offers premium performance with a minimum output-breakdown voltage rating of 100 V (50 V sustaining). The drivers can be operated with a split supply where the negative supply is up to −20 V.

The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids and other inductive loads.

BiMOS II latches have higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

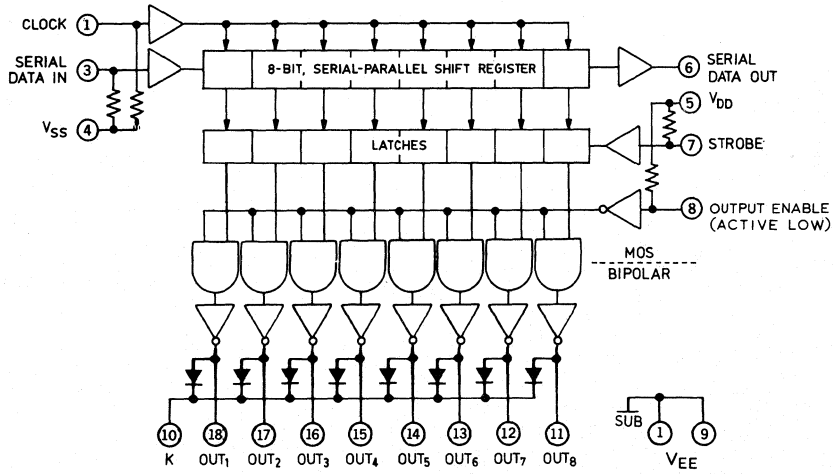
These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{CE} (UCN-5841A)	50 V
(UCN-5842A)	80 V
(UCN-5843A)	100 V
Output Voltage, $V_{CE(sus)}$ (UCN-5841A)	35 V†
(UCN-5842A)	50 V†
(UCN-5843A)	50 V†
Logic Supply Voltage Range, V_{DD}	4.5 V to 15 V
V_{DD} with Reference to V_{EE}	25 V
Emitter Supply Voltage, V_{EE}	−20 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	500 mA
Package Power Dissipation, P_D	1.82 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

†For inductive load applications.
*Derate at the rate of 18.2 mW/°C above T_A = +25°C

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,661

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

MAXIMUM ALLOWABLE DUTY CYCLE

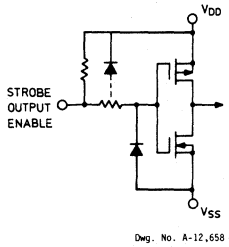
V_{DD} = 5.0 V

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 5.0 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

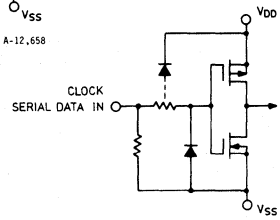
V_{DD} = 12 V

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

TYPICAL INPUT CIRCUITS

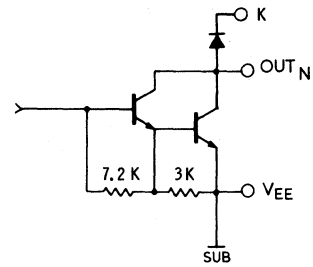


Dwg. No. A-12,658



Dwg. No. A-12,659

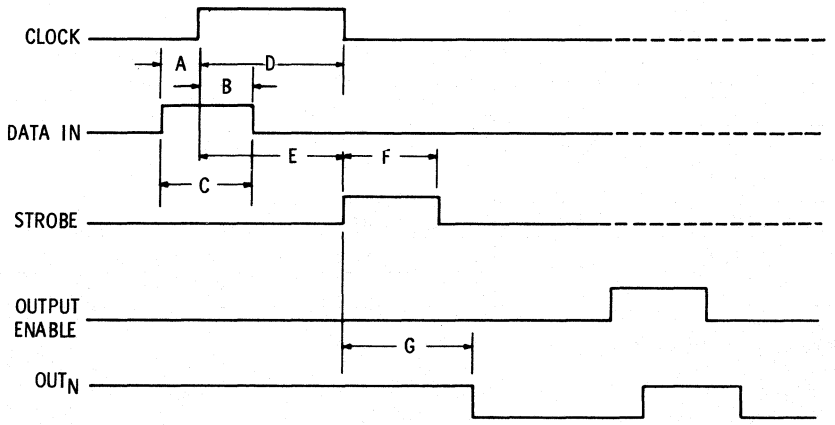
TYPICAL OUTPUT DRIVER



Dwg. No. A-12,660

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$, $V_{SS} = V_{EE} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Unit
Output Leakage Current	I_{CEX}	UCN-5841A	$V_{OUT} = 50\ V$	—	50	µA
			$V_{OUT} = 50\ V, T_A = +70°C$	—	100	µA
		UCN-5842A	$V_{OUT} = 80\ V$	—	50	µA
			$V_{OUT} = 80\ V, T_A = +70°C$	—	100	µA
		UCN-5843A	$V_{OUT} = 100\ V$	—	50	µA
			$V_{OUT} = 100\ V, T_A = +70°C$	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\ mA$	—	1.1	V
			$I_{OUT} = 200\ mA$	—	1.3	V
			$I_{OUT} = 350\ mA, V_{DD} = 7.0\ V$	—	1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	UCN-5841A	$I_{OUT} = 350\ mA, L = 2\ mH$	35	—	V
		UCN-5842A	$I_{OUT} = 350\ mA, L = 2\ mH$	50	—	V
		UCN-5843A	$I_{OUT} = 350\ mA, L = 2\ mH$	50	—	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 12\ V$	10.5	—	V
			$V_{DD} = 10\ V$	8.5	—	V
			$V_{DD} = 5.0\ V$	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 12\ V$	50	—	kΩ
			$V_{DD} = 10\ V$	50	—	kΩ
			$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	All Drivers ON, $V_{DD} = 12\ V$	—	16	mA
			All Drivers ON, $V_{DD} = 10\ V$	—	14	mA
			All Drivers ON, $V_{DD} = 5.0\ V$	—	8.0	mA
	$I_{DD(OFF)}$	ALL	All Drivers OFF, $V_{DD} = 12\ V$	—	2.9	mA
			All Drivers OFF, $V_{DD} = 10\ V$	—	2.5	mA
			All Drivers OFF, $V_{DD} = 5.0\ V$	—	1.6	mA
Clamp Diode Leakage Current	I_R	UCN-5841A	$V_R = 50$	—	50	µA
		UCN-5842A	$V_R = 80\ V$	—	50	µA
		UCN-5843A	$V_R = 100\ V$	—	50	µA
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350\ mA$	—	2.0	V



Dwg. NO. A-12,627

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

		V_{DD} = 5.0 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B.	Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C.	Minimum Data Pulse Width	150 ns
D.	Minimum Clock Pulse Width	150 ns
E.	Minimum Time Between Clock Activation and Strobe	300 ns
F.	Minimum Strobe Pulse Width	100 ns
G.	Typical Time Between Strobe Activation and Output Transition	500 ns

5

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

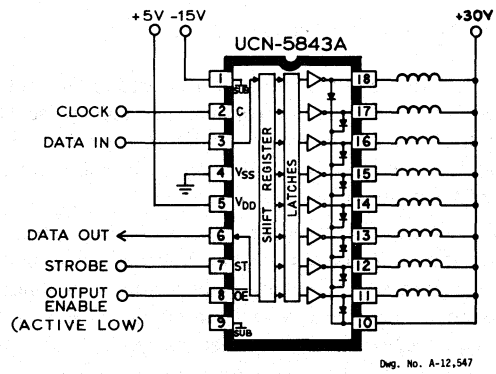
SERIES UCN-5840A TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots\ I_8$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots\ I_8$	Output Enable	Output Contents $I_1\ I_2\ I_3\ \ldots\ I_8$
H	⎍⎍	H $R_1\ R_2\ \ldots\ R_7$	R_7				
L	⎍⎍	L $R_1\ R_2\ \ldots\ R_7$	R_7				
X	⎍⎍	$R_1\ R_2\ R_3\ \ldots\ R_8$	R_8				
		X X X $\ldots$ X	X	L	$R_1\ R_2\ R_3\ \ldots\ R_8$		
		$P_1\ P_2\ P_3\ \ldots\ P_8$	P_8	H	$P_1\ P_2\ P_3\ \ldots\ P_8$	L	$P_1\ P_2\ P_3\ \ldots\ P_8$
					X X X $\ldots$ X	H	H H H $\ldots$ H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

TYPICAL APPLICATION

RELAY/SOLENOID DRIVER



UCN-5851A/EP AND UCN-5852A/EP
BiMOS II 32-CHANNEL, SERIAL-INPUT DRIVERS
—Thin-Film Electroluminescent Display Row Drivers

FEATURES

- DMOS Outputs
- Output Breakdown >225 V
- Sink up to 120 mA
- Low-Power CMOS Inputs and Logic
- 6 MHz Data Input Rate
- Refresh and Output Enable Functions
- Replaces SN75551, SN75552

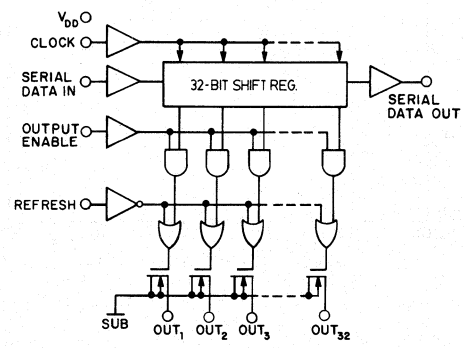
Thin-film electroluminescent display row driver applications are satisfied with the UCN-5851A/EP and UCN-5852A/EP 32-channel drivers. CMOS low-level logic, is combined with high-voltage (225 V), open-drain DMOS outputs. To facilitate pc board layout, serial data outputs run counterclockwise in the UCN-5851A/EP and clockwise in the UCN-5852A/EP.

The logic sections consist of a 32-bit shift register, refresh and output-enable gates. When both REFRESH and OUTPUT ENABLE are high, the contents of the register appears at the outputs. A serial shift register output is available to cascade shift registers. This output is not affected by the REFRESH or OUTPUT ENABLE.

The UCN-5851A and UCN-5852A are supplied in 40-pin dual in-line plastic packages with 0.600" (15.24 mm) row spacing. The UCN-5851EP and UCN-5852EP are packaged in 44-lead plastic chip carriers with 50-mil lead spacings ("J" lead bend) for surface-mount applications.

Companion TFEL column drivers are the Sprague UCN-5853A/EP and UCN-5854A/EP.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,048

5

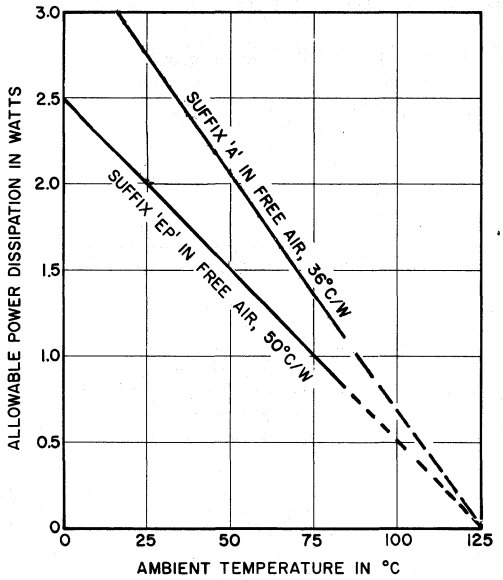
ABSOLUTE MAXIMUM RATINGS

Voltage Measurements
Referenced to Substrate

Supply Voltage, V_{DD} . . . . . 15 V
Output Voltage, V_{OUT} . . . . . 225 V
Input Voltage, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Output Current, I_{OUT} . . . . . 120 mA
Total Substrate Current, I_{SUB} . . . . . 1.5 A
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . −20°C to +85°C
Storage Temperature Range, T_S . . . −55°C to +125°C

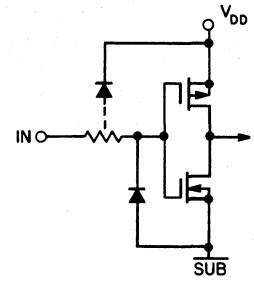
NOTE: Output current rating may be limited by duty cycle and ambient temperature (see graphs). Under any set of conditions, do not exceed the specified maximum current ratings or a junction temperature of +125°C.

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



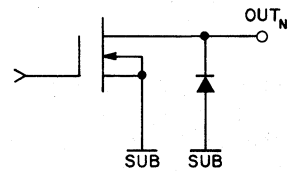
Dwg. No. A-13,033A

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,039

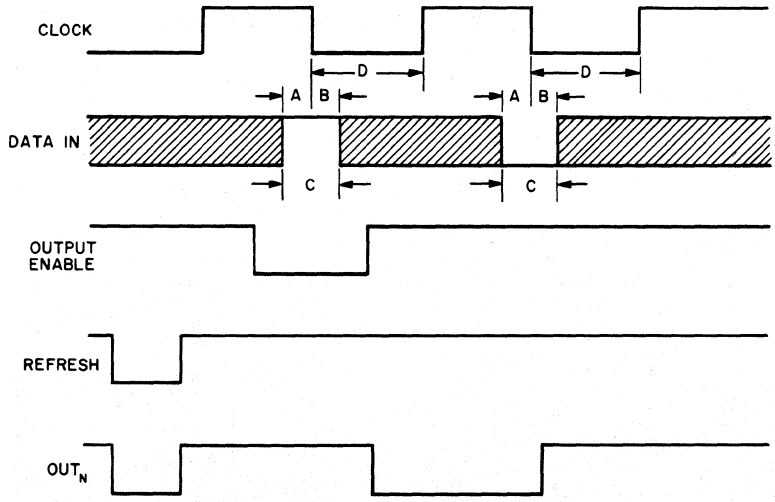
TYPICAL OUTPUT DRIVER



Dwg. No. A-13,040

ELECTRICAL CHARACTERISTICS at T_A = 0°C to +70°C, V_{DD} = 12 V, V_{SUB} = 0 (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Functional Supply Voltage Range	V_{DD}		4.5	12	15	V
Output Leakage Current	I_{OUT}	V_{OUT} = 225 V	—	—	10	µA
Output Voltage	$V_{OUT(0)}$	I_{OUT} = 20 mA, V_{DD} = 5 V	—	8.0	10	V
		I_{OUT} = 100 mA, V_{DD} = 12 V	—	15	30	V
Output Clamp Diode Voltage	V_F	I_F = 100 mA	—	1.8	2.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = −100 µA	10.5	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 100 µA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	5.3	V
		V_{DD} = 12 V	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 12 V	—	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0	—	—	−1.0	µA
Maximum Clock Frequency	f_{clk}	V_{DD} = 5.0 V	3.3	—	—	MHz
		V_{DD} = 12 V	—	7.5	—	MHz
Supply Current	I_{DD}	f_{clk} = 0	—	—	500	µA
Output Enable to Output Delay	t_{PHL}	C_L = 10 pF	—	200	500	ns
	t_{PLH}	C_L = 10 pF	—	250	500	ns
Output Fall Time	t_f	C_L = 10 pF	—	80	200	ns
Output Rise Time	t_r	C_L = 10 pF	—	300	500	ns



Dwg. No. A-13,041

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TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SUB})

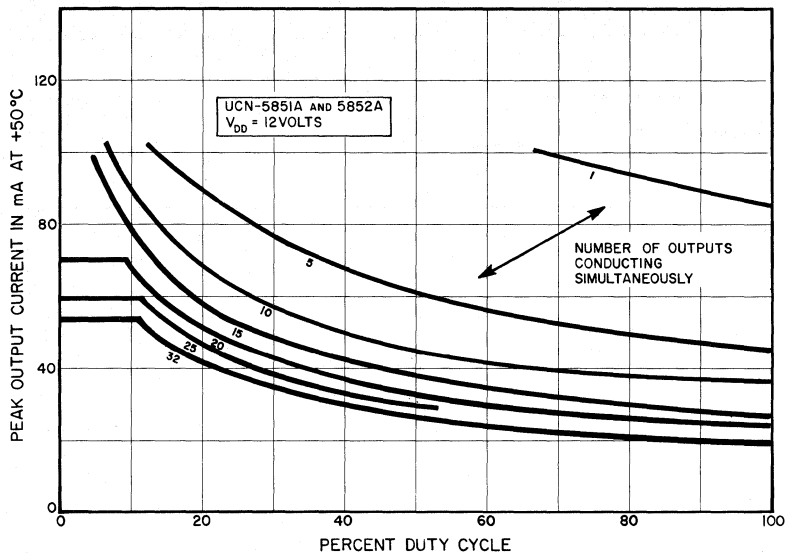
	V_{DD} = 5.0 V		V_{DD} = 12 V	
	Tested	Typ.	Typ.	Units
A. Min. Data Active Time Before Clock Pulse (Data Set-Up Time)	75	35	15	ns
B. Min. Data Active Time After Clock Pulse (Data Hold Time)	75	35	15	ns
C. Min. Clock Pulse Width	150	70	30	ns
D. Min. Clock Pulse Width	150	100	65	ns
Max. Clock Frequency	3.3	5.0	7.5	MHz

The logic section consists of a 32-bit shift register, 32 output-enable gates and 32 refresh gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the substrate common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. When REFRESH is high, a high ENABLE input will allow those outputs with a high in their associated register to be turned ON, causing the corresponding row to be connected to the composite row drive signal. When the REFRESH input is low, all outputs are turned ON.

The serial data output from the shift register may be used to cascade additional devices. This output is not affected by the OUTPUT ENABLE or REFRESH inputs.

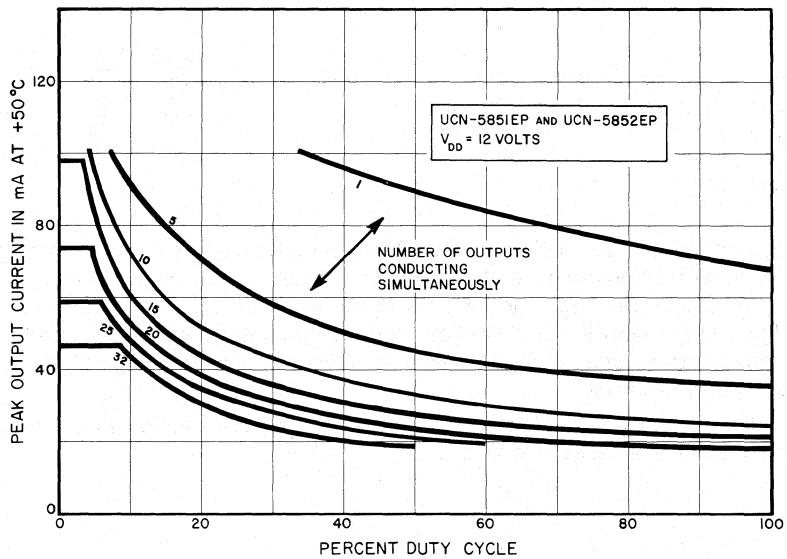
OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5851A AND UCN-5852A



Dwg. No. A-13,042

UCN-5851EP AND UCN-5852EP



Dwg. No. A-13,043

APPLICATIONS

Electroluminescent (EL) display panels are generally built as an X-Y matrix of rows and columns. Because of the construction of the panel, each cell, or pixel, that must be driven presents primarily a capacitive load (Fig. 1). The variable resistor models the electroluminescent effect, while the back-to-back Zener diodes account for the threshold voltage which must be reached prior to the emission of light. The EL display panel's capacitive nature requires that it be a-c driven.

REFRESH SCANNING

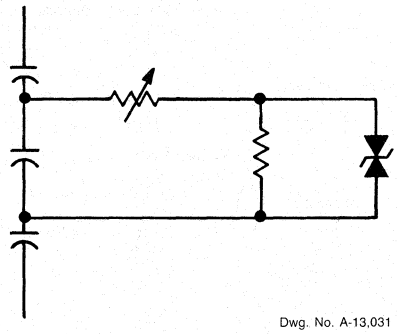
To be compatible with existing CRT systems, EL panels usually use a raster-scanning refresh approach. Refresh rates range from 60 Hz to 500 Hz. The higher the rate, the more power the panel consumes. At frequencies less than 500 Hz, the panel brightness varies linearly with excitation frequency (or the refresh rate).

At the beginning of each scan, with the columns grounded, all rows receive a positive refresh pulse (Fig. 2) from the UCN-5851/52 row-drivers through the clamp diodes in the IC outputs (Fig. 3). Depending on the panel, the refresh-pulse voltage can be as high as +225 V.

Next, the row-driver IC is turned ON by the refresh signal so that the row-driver outputs follow the composite signal back to ground and allow the cell capacitances to discharge. Thereafter, the rows are left in a floating condition until each is selected in turn by the UCN-5851/52 to be driven to a negative potential.

The threshold voltage for light emission is reached by driving the rows negative (−160 V) and the columns positive (+50 V) relative to ground, resulting in a pixel voltage which equals the difference of the driving potentials (210 V, in this case). Individual pixel control is effected by selecting the rows one at a time and pulling high only those columns which correspond to the desired ON pixels. Higher voltage levels (to +80 V and to −225 V) will generate increased light levels.

EL CELL EQUIVALENT



Dwg. No. A-13,031

FIGURE 1

ENTERING THE DATA

Before a row is selected, all the data for that line must be registered and latched into the column driver's output latch. Data for subsequent lines can be clocked into the column registers as soon as the current data enters the output latches. The column drivers must be enabled during the time that the row-driver output goes negative.

A logic "1" represents an illuminated cell. Therefore, to turn a cell ON, a positive voltage is applied to the selected column. As shown in Figure 3, the −160 V on the selected row and +50 V on the selected column define the cell to be lit. The combined voltage difference of 210 V across the cell is above the electroluminescence threshold and therefore causes light generation.

APPLICATIONS

The worst-case row-driver current requirement is when all columns in a row are turned ON. If there are 256 rows and 512 columns in the panel and each cell presents a capacitance of 4 pF, then the minimum ramp time allowed is determined as follows:

$$dt = C\ dv/i$$
$$dt = (512 \times 4\ pF) \times 210\ V / 100\ mA$$
$$dt = 4.3\ \mu s$$

where 210 V is the total voltage difference between the row and the column electrodes, and 100 mA is the recommended maximum sink current. The 4.3 μs is then the minimum allowable ramp time for the composite-row driver supply voltage.

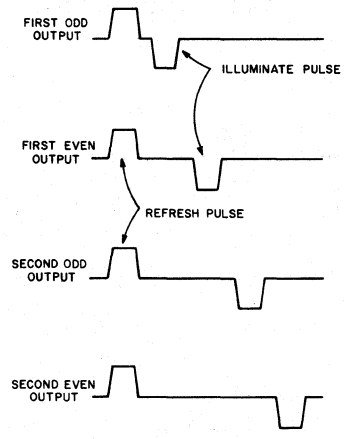
Similarly, when the positive refresh pulse is applied to all rows at the beginning of each scan, the worse-case current through the row-driver's clamp diode occurs when all the rows are at 0 V and the pulse suddenly switches to the positive refresh voltage. For a diode rating of 100 mA, the minimum allowable ramp time would again be 4.3 μs.

These minimum ramp times (dt) are smaller than those encountered in typical applications. Normally, the peak current will be lower than the 100 mA used in the examples shown and may be limited by the column driver's current capability.

The block diagram of a typical electroluminescent display, (Fig. 4), shows that the UCN-5851 row-drivers drive the odd rows and the UCN-5852 row-drivers the even rows. The odd and even rows are actuated alternately. The two drivers are identical except for the output-pin arrangements, which eliminates the need for pc board vias when connecting them to opposite sides of the panel.

Because the row-driver substrates are connected to the composite-row drive voltage (+210 V, ground, or −160 V), all clock, data, strobe, and enable signals to them must be level shifted. Optical isolators can be used very effectively. The column drivers are referenced to ground and therefore do not need such isolation.

ROW OUTPUT VOLTAGE SIGNALS

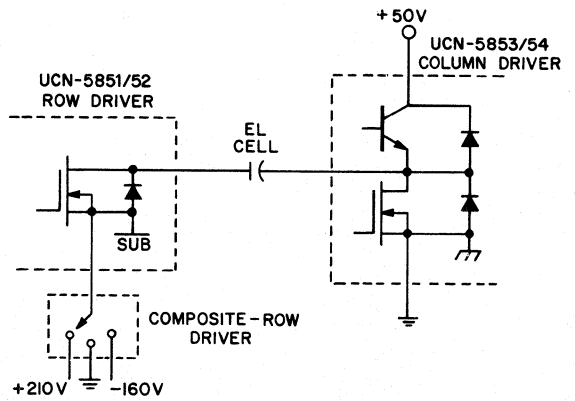


Dwg. No. A-13,030

FIGURE 2

APPLICATIONS

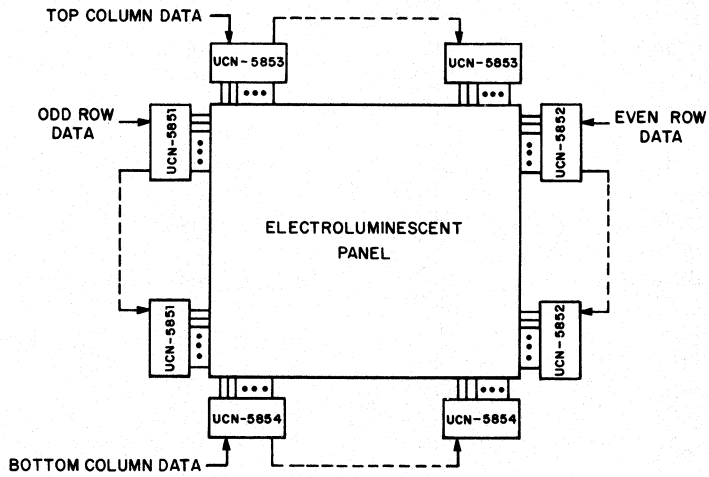
SIMPLIFIED CELL DRIVER



Dwg. No. A-13,029

FIGURE 3

ELECTROLUMINESCENT DISPLAY



Dwg. No. A-13,032

FIGURE 4

PIN DESIGNATIONS

PIN	UCN-5851A	UCN-5851EP	UCN-5852A	UCN-5852EP
1	OUT_{16}	OUT_{16}	OUT_{17}	OUT_{17}
2	OUT_{17}	OUT_{17}	OUT_{16}	OUT_{16}
3	OUT_{18}	OUT_{18}	OUT_{15}	OUT_{15}
4	OUT_{19}	OUT_{19}	OUT_{14}	OUT_{14}
5	OUT_{20}	OUT_{20}	OUT_{13}	OUT_{13}
6	OUT_{21}	OUT_{21}	OUT_{12}	OUT_{12}
7	OUT_{22}	OUT_{22}	OUT_{11}	OUT_{11}
8	OUT_{23}	OUT_{23}	OUT_{10}	OUT_{10}
9	OUT_{24}	OUT_{24}	OUT_{9}	OUT_{9}
10	OUT_{25}	OUT_{25}	OUT_{8}	OUT_{8}
11	OUT_{26}	OUT_{26}	OUT_{7}	OUT_{7}
12	OUT_{27}	OUT_{27}	OUT_{6}	OUT_{6}
13	OUT_{28}	OUT_{28}	OUT_{5}	OUT_{5}
14	OUT_{29}	OUT_{29}	OUT_{4}	OUT_{4}
15	OUT_{30}	OUT_{30}	OUT_{3}	OUT_{3}
16	OUT_{31}	OUT_{31}	OUT_{2}	OUT_{2}
17	OUT_{32}	OUT_{32}	OUT_{1}	OUT_{1}
18	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT
19	ENABLE	NC	ENABLE	NC
20	CLOCK	NC	CLOCK	NC
21	SUBSTRATE	NC	SUBSTRATE	NC
22	V_{DD}	NC	V_{DD}	NC
23	REFRESH	ENABLE	REFRESH	ENABLE
24	SERIAL DATA IN	CLOCK	SERIAL DATA IN	CLOCK
25	NC	SUBSTRATE	NC	SUBSTRATE
26	OUT_{1}	V_{DD}	OUT_{32}	V_{DD}
27	OUT_{2}	REFRESH	OUT_{31}	REFRESH
28	OUT_{3}	SERIAL DATA IN	OUT_{30}	SERIAL DATA IN
29	OUT_{4}	NC	OUT_{29}	NC
30	OUT_{5}	OUT_{1}	OUT_{28}	OUT_{32}
31	OUT_{6}	OUT_{2}	OUT_{27}	OUT_{31}
32	OUT_{7}	OUT_{3}	OUT_{26}	OUT_{30}
33	OUT_{8}	OUT_{4}	OUT_{25}	OUT_{29}
34	OUT_{9}	OUT_{5}	OUT_{24}	OUT_{28}
35	OUT_{10}	OUT_{6}	OUT_{23}	OUT_{27}
36	OUT_{11}	OUT_{7}	OUT_{22}	OUT_{26}
37	OUT_{12}	OUT_{8}	OUT_{21}	OUT_{25}
38	OUT_{13}	OUT_{9}	OUT_{20}	OUT_{24}
39	OUT_{14}	OUT_{10}	OUT_{19}	OUT_{23}
40	OUT_{15}	OUT_{11}	OUT_{18}	OUT_{22}
41	—	OUT_{12}	—	OUT_{21}
42	—	OUT_{13}	—	OUT_{20}
43	—	OUT_{14}	—	OUT_{19}
44	—	OUT_{15}	—	OUT_{18}

UCN-5853A/EP AND UCN-5854A/EP
BiMOS II 32-CHANNEL, SERIAL-INPUT, LATCHED DRIVERS
—Thin-Film Electroluminescent Display Column Drivers

FEATURES

- Totem Pole Outputs
- High Output Breakdown
- Sink or Source up to 25 mA
- Low-Power CMOS Inputs and Logic
- 7.5 MHz Data Input Rate
- Strobe and Output Enable Functions
- Replaces SN75553 and SN75554

Thin-film electroluminescent display column driver applications are satisfied with the UCN-5853A/EP and UCN-5854A/EP BiMOS II 32-channel drivers. CMOS low-level logic, 60 V bipolar source drivers, and DMOS sink drivers are combined in a monolithic integrated circuit. To facilitate pc board layout, serial data outputs run clockwise in the UCN-5853A/EP and counterclockwise in the UCN-5854A/EP. The UCN-5853A/EP and UCN-5854A/EP are rated for operation with load voltages to 60 V. Selected devices (suffix "-1") are available for operation to 80 V.

The logic sections consist of a 32-bit shift register, 32 latches, and output enable gates. When OUTPUT ENABLE is high, the contents of the latches appear at the outputs. A serial shift register output is available to cascade shift registers. This output is not affected by the STROBE or OUTPUT ENABLE.

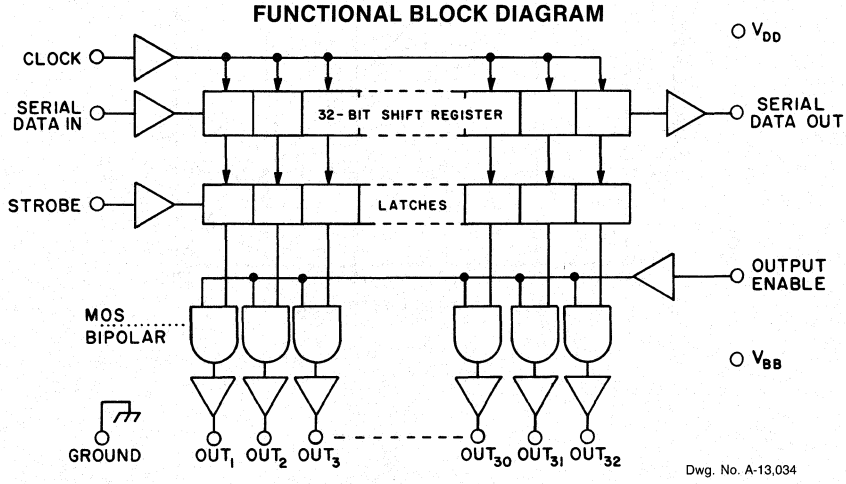
The output sections are high-voltage Darlington source drivers with DMOS sink drivers. The output configuration ensures that the output is not pulled down until the source drive has been turned OFF, eliminating the possibility of high crossover current.

The UCN-5853A and UCN-5854A are supplied in 40-pin dual in-line plastic packages with 0.600" (15.24 mm) row spacing. The UCN-5853EP and UCN-5854EP are packaged in 44-lead plastic chip carriers with 50-mil lead spacings ('J' lead bend) for surface-mount applications.

Companion TFEL row drivers are the UCN-5851A/EP and UCN-5852A/EP.

5

FUNCTIONAL BLOCK DIAGRAM

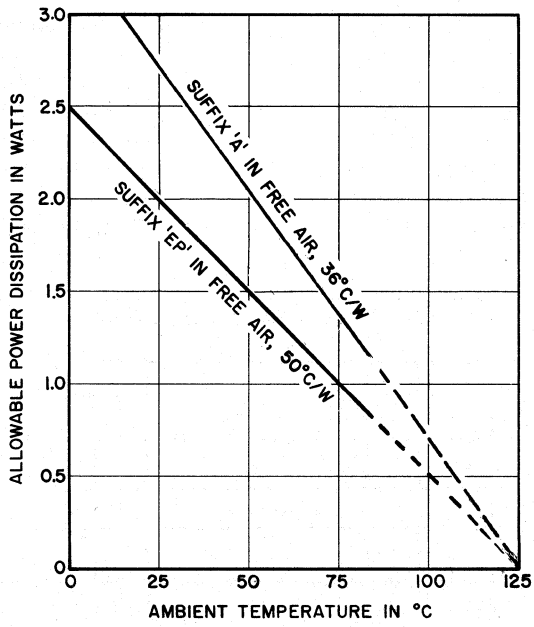


Dwg. No. A-13,034

ABSOLUTE MAXIMUM RATINGS

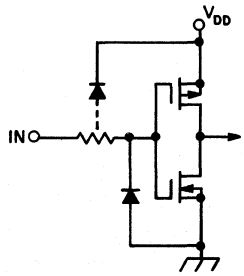
Supply Voltage, V_{DD} . . . . . 15 V
Supply Voltage, V_{BB}
(UCN-5853/54A, UCN-5853/54EP) . . . . . 60 V
(UCN-5853/54A-1, UCN-5853/54EP-1) . . . . . 80 V
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Output Current, I_{OUT} . . . . . ± 25 mA
Total Ground Current, I_{GND} . . . . . 700 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



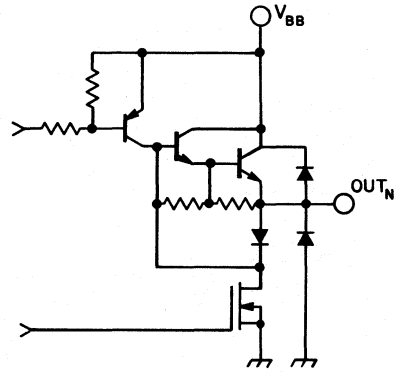
Dwg. No. A-13,033A

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,035

TYPICAL OUTPUT DRIVER

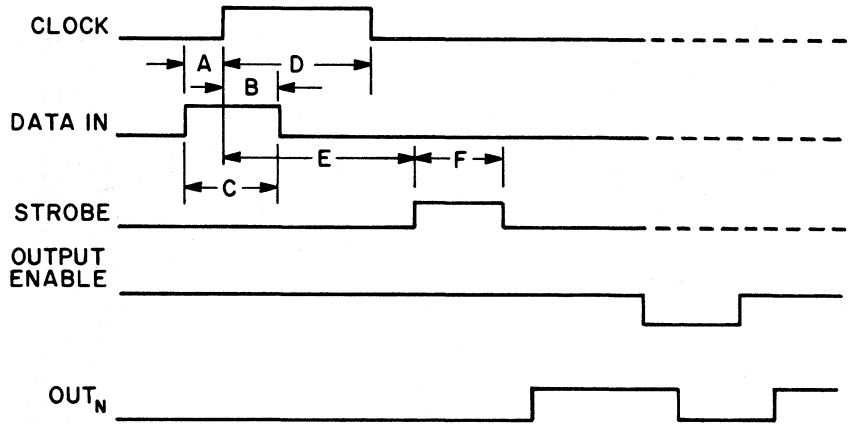


Dwg. No. A-13,036

ELECTRICAL CHARACTERISTICS at T_A = 0°C to +70°C, V_{DD} = 12 V, V_{BB} = 60 V (UCN-5853A/EP, UCN-5854A/EP) or V_{BB} = 80 V (Suffix '-1') unless otherwise specified

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage Range	V_{DD}		4.5	12	15	V
Output Voltage	$V_{OUT(1)}$	I_{OUT} = −20 mA, V_{BB} = 60 V	57.5	—	—	V
		I_{OUT} = −20 mA, V_{BB} = 80 V*	77.5	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 20 mA	—	6.0	10	V
Output Clamp Diode Voltage	V_F	I_F = 20 mA	—	2.0	2.5	V
Serial Output Voltage	$V_{OUT(1)}$	I_{OUT} = −100 µA	10.5	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 100 µA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	V_{DD} = 10.8 V	10.0	—	11.1	V
		V_{DD} = 15 V	14.2	—	15.3	V
	$V_{ON(0)}$	V_{DD} = 10.8 V	−0.3	—	0.8	V
		V_{DD} = 15 V	−0.3	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 12 V	—	—	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0	—	—	−1.0	µA
Maximum Clock Frequency	f_{clk}	V_{DD} = 5.0 V	3.3	—	—	MHz
		V_{DD} = 12 V	—	7.5	—	MHz
Supply Current	I_{DD}	f_{clk} = 0, Outputs Low	—	—	0.5	mA
		f_{clk} = 0, Outputs High	—	3.0	5.0	mA
	I_{BB}	Outputs High, No Load	—	2.5	3.5	mA
		Outputs Low	—	—	0.5	mA
Output Enable to Ouput Delay	t_{PHL}	C_L = 10 pF	—	200	500	ns
	t_{PHL}	C_L = 10 pF	—	250	500	ns
Output Fall Time	t_f	C_L = 10 pF	—	80	200	ns
Output Rise Time	t_r	C_L = 10 pF	—	300	500	ns

*UCN-5853A/EP-1 and UCN-5854A/EP-1 only.



Dwg. No. A-13,037

TIMING CONDITIONS

(T_A = +25°C, V_{DD} = 12 V, Logic Levels are V_{DD} and Ground)

	Tested	Typ.	Units
A. Min. Data Active Time Before Clock Pulse (Data Set-Up Time)	75	15	ns
B. Min. Data Active Time After Clock Pulse (Data Hold Time)	75	15	ns
C. Min. Data Pulse Width	150	30	ns
D. Min. Clock Pulse Width	150	65	ns
E. Min. Time Between Clock Activation and Strobe	300	75	ns
F. Min. Strobe Pulse Width	100	50	ns
Max. Clock Frequency	3.3	7.5	MHz

The logic section consists of a 32-bit shift register, 32 latches, and 32 output-enable gates. Serial data is entered into the shift register on the low-to-high transition of the CLOCK input. A high STROBE input transfers the contents of the shift register to the outputs of the latches. When OUTPUT ENABLE is high, the contents of the latches appear at the outputs. The SERIAL DATA output is used to cascade shift registers. This output is not affected by STROBE or OUTPUT ENABLE.

APPLICATIONS

Electroluminescent (EL) display panels are generally built as an X-Y matrix of rows and columns. Because of the construction of the panel, each cell, or pixel, that must be driven presents primarily a capacitive load (Fig. 1). The variable resistor models the electroluminescent effect, while the back-to-back Zener diodes account for the threshold voltage which must be reached prior to the emission of light. The EL display panel's capacitive nature requires that it be a-c driven.

REFRESH SCANNING

To be compatible with existing CRT systems, EL panels usually use a raster-scanning refresh approach. Refresh rates range from 60 Hz to 500 Hz. The higher the rate, the more power the panel consumes. At frequencies less than 500 Hz, the panel brightness varies linearly with excitation frequency (or the refresh rate).

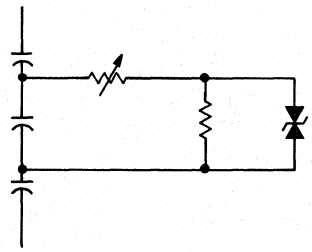
At the beginning of each scan, with the columns grounded, all rows receive a positive refresh pulse (Fig. 2) from the row-drivers through the clamp diodes in the IC outputs (Fig. 3). Depending on the panel, the refresh-pulse voltage can be as high as +225 V.

Next, the row-driver IC is turned ON by the refresh signal so that the row-driver outputs follow the composite signal back to ground and allow the cell capacitances to discharge. Thereafter, the rows are left in a floating condition until each is selected in turn by the row drivers to be driven to a negative potential.

The threshold voltage for light emission is reached by driving the rows negative (−160 V) and the columns positive (+50 V) relative to ground, resulting in a pixel voltage which equals the difference of the driving potentials (210 V, in this case). Individual pixel control is effected by selecting the rows one at a time and pulling high only those columns which correspond to the desired ON pixels. Higher voltage levels (to +80 V and to −225 V) will generate increased light levels.

5

EL CELL EQUIVALENT



Dwg. No. A-13,031

FIGURE 1

ENTERING THE DATA

Before a row is selected, all the data for that line must be registered and latched into the UCN-5853/54 column driver's output latch. Data for subsequent lines can be clocked into the column registers as soon as the current data enters the output latches. The column drivers must be enabled during the time that the row-driver output goes negative.

A logic "1" represents an illuminated cell. Therefore, to turn a cell ON, a positive voltage is applied to the selected column. As shown in Figure 3, the −160 V on the selected row and +50 V on the selected column define the cell to be lit. The combined voltage difference of 210 V across the cell is above the electroluminescence threshold and therefore causes light generation.

APPLICATIONS

The worst-case UCN-5853/54 DMOS sink driver current requirement is when all but one source driver are turned ON. That one low column driver must sink current which is a result of all the positive-going column drivers pulling all the floating rows positive. If there are 256 rows and 512 columns in the panel and each cell presents a capacitance of 4 pF, then:

$$dt = C\ dv/i$$
$$dt = (256 \times 4\ pF) \times 50\ V / 20\ mA$$
$$dt = 2.6\ \mu s$$

where 50 V is the column driver supply voltage and 20 mA is the recommended maximum current. The 2.6 μs is then the minimum allowable ramp-up time for the column-driver supply voltage.

Similarly, the worst-case source driver current requirement is when all sink drivers but one are turned ON. For a −20 mA recommended maximum source current, the minimum allowable ramp time would again be 2.6 μs.

These minimum ramp times (dt) are smaller than those encountered in typical applications.

The block diagram of a typical electroluminescent display is shown in Fig. 4. The UCN-5853 drive the top columns and UCN-5854 drive the bottom columns. They are actuated alternately. The two drivers are identical except for the output-pin arrangements, which eliminates the need for pc board vias when connecting them to opposite sides of the panel.

ROW OUTPUT-VOLTAGE SIGNALS

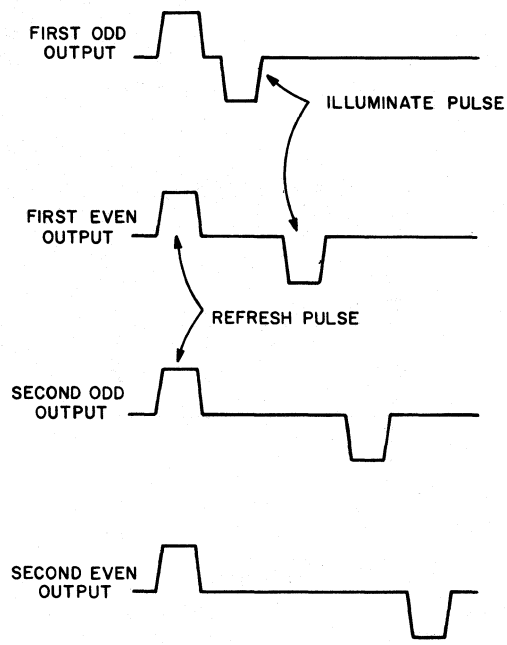


FIGURE 2

Dwg. No. A-13,030

APPLICATIONS

SIMPLIFIED CELL DRIVER

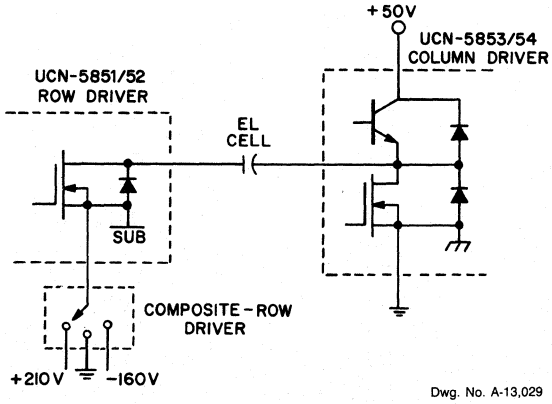


FIGURE 3

ELECTROLUMINESCENT DISPLAY

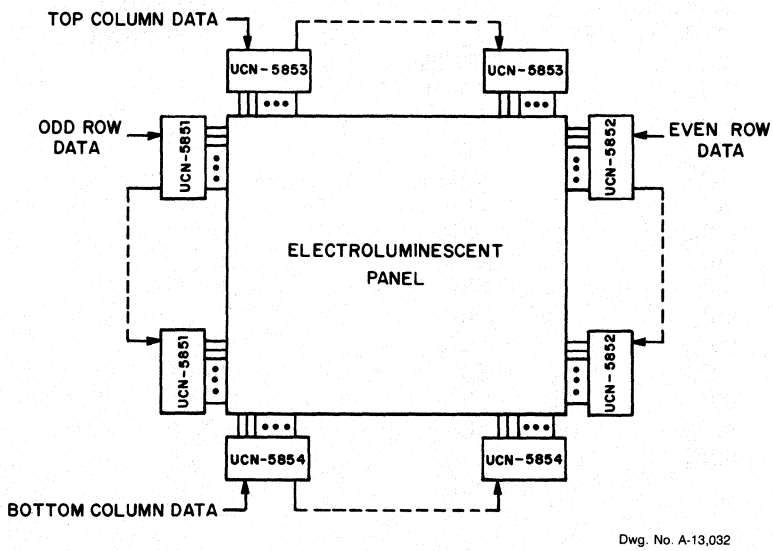


FIGURE 4

PIN DESIGNATIONS

PIN	UCN-5853A	UCN-5853EP	UCN-5854A	UCN-5854EP
1	OUT_{17}	OUT_{17}	OUT_{16}	OUT_{16}
2	OUT_{16}	OUT_{16}	OUT_{17}	OUT_{17}
3	OUT_{15}	OUT_{15}	OUT_{18}	OUT_{18}
4	OUT_{14}	OUT_{14}	OUT_{19}	OUT_{19}
5	OUT_{13}	OUT_{13}	OUT_{20}	OUT_{20}
6	OUT_{12}	OUT_{12}	OUT_{21}	OUT_{21}
7	OUT_{11}	OUT_{11}	OUT_{22}	OUT_{22}
8	OUT_{10}	OUT_{10}	OUT_{23}	OUT_{23}
9	OUT_{9}	OUT_{9}	OUT_{24}	OUT_{24}
10	OUT_{8}	OUT_{8}	OUT_{25}	OUT_{25}
11	OUT_{7}	OUT_{7}	OUT_{26}	OUT_{26}
12	OUT_{6}	OUT_{6}	OUT_{27}	OUT_{27}
13	OUT_{5}	OUT_{5}	OUT_{28}	OUT_{28}
14	OUT_{4}	OUT_{4}	OUT_{29}	OUT_{29}
15	OUT_{3}	OUT_{3}	OUT_{30}	OUT_{30}
16	OUT_{2}	OUT_{2}	OUT_{31}	OUT_{31}
17	OUT_{1}	OUT_{1}	OUT_{32}	OUT_{32}
18	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT	SERIAL DATA OUT
19	CLOCK	IC*	CLOCK	IC*
20	GROUND	NC	GROUND	NC
21	V_{BB}	NC	V_{BB}	NC
22	V_{DD}	CLOCK	V_{DD}	CLOCK
23	STROBE	GROUND	STROBE	GROUND
24	SERIAL DATA IN	V_{BB}	SERIAL DATA IN	V_{BB}
25	OUTPUT ENABLE	V_{DD}	OUTPUT ENABLE	V_{DD}
26	OUT_{32}	STROBE	OUT_{1}	STROBE
27	OUT_{31}	SERIAL DATA IN	OUT_{2}	SERIAL DATA IN
28	OUT_{30}	OUTPUT ENABLE	OUT_{3}	OUTPUT ENABLE
29	OUT_{29}	NC	OUT_{4}	NC
30	OUT_{28}	OUT_{32}	OUT_{5}	OUT_{1}
31	OUT_{27}	OUT_{31}	OUT_{6}	OUT_{2}
32	OUT_{26}	OUT_{30}	OUT_{7}	OUT_{3}
33	OUT_{25}	OUT_{29}	OUT_{8}	OUT_{4}
34	OUT_{24}	OUT_{28}	OUT_{9}	OUT_{5}
35	OUT_{23}	OUT_{27}	OUT_{10}	OUT_{6}
36	OUT_{22}	OUT_{26}	OUT_{11}	OUT_{7}
37	OUT_{21}	OUT_{25}	OUT_{12}	OUT_{8}
38	OUT_{20}	OUT_{24}	OUT_{13}	OUT_{9}
39	OUT_{19}	OUT_{23}	OUT_{14}	OUT_{10}
40	OUT_{18}	OUT_{22}	OUT_{15}	OUT_{11}
41	—	OUT_{21}	—	OUT_{12}
42	—	OUT_{20}	—	OUT_{13}
43	—	OUT_{19}	—	OUT_{14}
44	—	OUT_{18}	—	OUT_{15}

*Internal Connection. Must be connected to V_{DD}

UCN-5857A/EP AND UCN-5859A/EP
32-OUTPUT 8-BIT ADDRESSABLE DRIVERS

FEATURES

- 32 Totem Pole Outputs
- Output Breakdown of 100 V
- Output Current of ±20 mA
- Low-Power CMOS Logic
- Output Clamping Diodes

UCN-5857A/EP and UCN-5859A/EP are 8-bit addressable shift register drivers with 32-output capability. They employ totem pole outputs capable of maintaining an OFF voltage of 100 V and an ON current of ±20 mA. The devices include a two-line to four-line decoder that determines which set of outputs is controlled by the on-board eight-bit shift register.

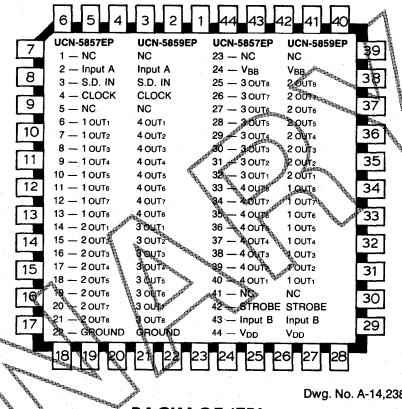
A low on the input will result in a high on the output. A high on the input will result in a low on the output. Outputs of this device are normally low. When the STROBE input is held low, outputs are controlled by the state of the shift register. When the STROBE is held high, all outputs remain low and are unaffected by the register contents. Output clamping for sink and source have been incorporated to guard against high and low transients.

These devices are furnished in a 40-pin dual in-line plastic package with 600-mil row centers or in a 44-pin plastic leaded chip carrier with 50-mil spacings (J lead bend) for surface-mount applications.

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

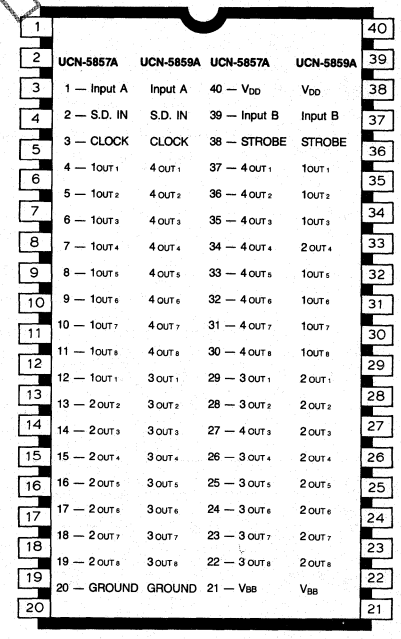
Output Voltage, V_{CE} ..... 100 V
Output Supply Voltage, V_{BB} ..... 100 V
Logic Supply Voltage, V_{DD} ..... 15 V
Output Current, I_{OUT} ..... ±20 mA
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD}+0.3 V
Package Power Dissipation, P_D ('A' Package) ..... 2.8 W*
('EP' Package) ..... 2.0 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate linearly to 0 W at $T_A = +125°C$



Dwg. No. A-14,238

PACKAGE 'EP'



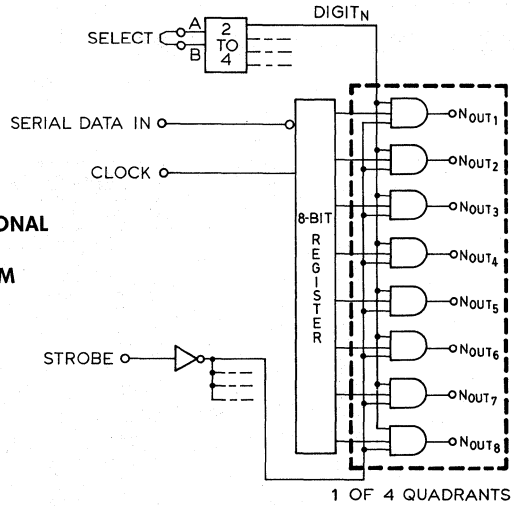
Dwg. No. A-14,239

PACKAGE 'A'

NOTE: S.D. IN = SERIAL DATA IN

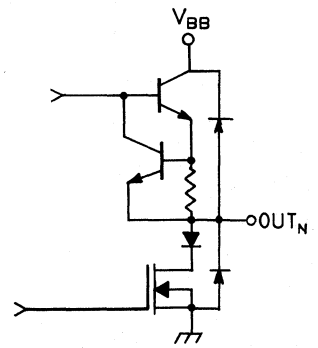
5

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-14,240

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,241

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 100 V, V_{DD} = 5 V (unless otherwise noted)

Characteristic	Symbol	Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{BB} = 100 V, V_{OUT} = 0 V	—	—	−100	µA
		V_{BB} = V_{OUT} = 100 V	—	—	100	µA
Output Saturation Voltage	$V_{OUT(1)}$	I_{OUT} = −1.0 mA	98	—	—	V
		I_{OUT} = −10 mA	97	—	—	V
		I_{OUT} = −15 mA	96	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 1.0 mA, V_{DD} = 12 V	—	—	20	V
		I_{OUT} = 10 mA, V_{DD} = 12 V	—	—	4.0	V
		I_{OUT} = 15 mA, V_{DD} = 12 V	—	—	5.0	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 5.0 V to 12 V	1.0	—	—	MΩ
Supply Current	$I_{DD(LOW)}$	V_{DD} = 12 V, All outputs low	—	—	1.0	mA
	$I_{DD(HIGH)}$	V_{DD} = 12 V, 8 outputs high	—	—	1.0	mA
Output Clamp Voltage	$V_{OUT(CLAMP)}$	I_{OUT} = 20 mA	—	—	102.5	V
		I_{OUT} = −20 mA	—	—	−2.5	V
Output Short-Circuit Current	I_{SC}		—	—	−20	mA
High-Voltage Supply Current	$I_{BB(LOW)}$	V_{DD} = 12 V, All outputs low	—	—	1.0	mA
	$I_{BB(HIGH)}$	V_{DD} = 12 V, 8 outputs high	—	—	3.0	mA

UCN-5858A/EP AND UCN-5860A/EP 32-BIT SHIFT REGISTER/DRIVERS

FEATURES

- 32 Totem Pole Outputs
- Output Breakdown of 100 V
- Output Current of ±20 mA
- Low-Power CMOS Logic
- Output Clamping Diodes
- UCN-5858 Replaces SN75501D

The UCN-5858A/EP and UCN-5860A/EP 32-channel shift register/drivers are used as row drivers for AC plasma displays. These devices are capable of maintaining an output OFF voltage of 100 V and an output ON current of ±20 mA. Outputs are totem pole design.

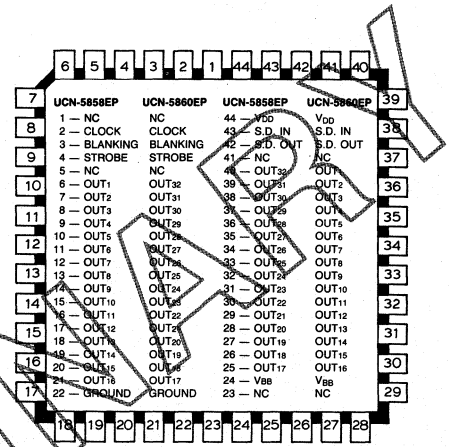
Output clamping for source and sink have been incorporated to guard against high and low transients. A low input will result in a low output. A high input will result in a high output. Outputs are controlled by their inputs when STROBE is low and BLANKING is high. When BLANKING is low, all outputs are low and unaffected by the register contents or STROBE. When STROBE is high, all outputs are unaffected by the register and are forced high (BLANKING held high).

These devices are furnished in a 40-pin dual in-line plastic package with 600-mil row centers ("A" package) or in a 44-pin plastic leaded chip carrier with 50-mil spacings for surface-mount applications.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{CE} ..... 100 V
Output Supply Voltage, V_{BB} ..... 100 V
Logic Supply Voltage, V_{DD} ..... 15 V
Output Current, I_{OUT} ..... ±20 mA
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Package Power Dissipation, P_D ('A' Package) ..... 2.8 W*
('EP' Package) ..... 2.0 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C

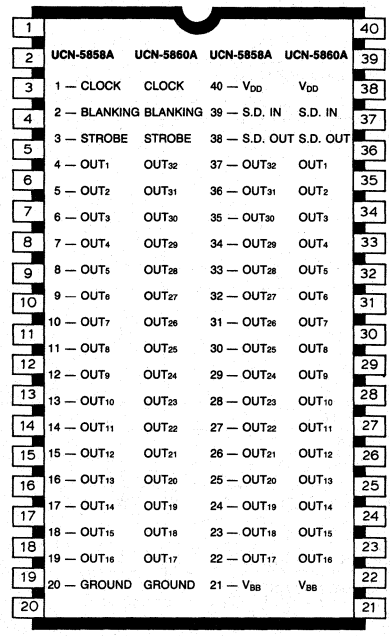
*Derate linearly to 0 W at T_A = +125°C



	UCN-5858EP	UCN-5860EP	UCN-5858EP	UCN-5860EP
1	NC	NC	V_{DD}	V_{DD}
2	CLOCK	CLOCK	S.D. IN	S.D. IN
3	BLANKING	BLANKING	S.D. OUT	S.D. OUT
4	STROBE	STROBE	NC	NC
5	NC	NC	OUT_{32}	OUT_{32}
6	OUT_1	OUT_{32}	OUT_{31}	OUT_2
7	OUT_2	OUT_{31}	OUT_{30}	OUT_3
8	OUT_3	OUT_{30}	OUT_{29}	OUT_4
9	OUT_4	OUT_{29}	OUT_{28}	OUT_5
10	OUT_5	OUT_{28}	OUT_{27}	OUT_6
11	OUT_6	OUT_{27}	OUT_{26}	OUT_7
12	OUT_7	OUT_{26}	OUT_{25}	OUT_8
13	OUT_8	OUT_{25}	OUT_{24}	OUT_9
14	OUT_9	OUT_{24}	OUT_{23}	OUT_{10}
15	OUT_{10}	OUT_{23}	OUT_{22}	OUT_{11}
16	OUT_{11}	OUT_{22}	OUT_{21}	OUT_{12}
17	OUT_{12}	OUT_{21}	OUT_{20}	OUT_{13}
18	OUT_{13}	OUT_{20}	OUT_{19}	OUT_{14}
19	OUT_{14}	OUT_{19}	OUT_{18}	OUT_{15}
20	OUT_{15}	OUT_{18}	OUT_{17}	OUT_{16}
21	OUT_{16}	OUT_{17}	V_{BB}	V_{BB}
22	GROUND	GROUND	NC	NC

Dwg. No. A-14,242

PACKAGE 'EP'



	UCN-5858A	UCN-5860A	UCN-5858A	UCN-5860A
1	CLOCK	CLOCK	V_{DD}	V_{DD}
2	BLANKING	BLANKING	S.D. IN	S.D. IN
3	STROBE	STROBE	S.D. OUT	S.D. OUT
4	OUT_1	OUT_{32}	OUT_{32}	OUT_1
5	OUT_2	OUT_{31}	OUT_{31}	OUT_2
6	OUT_3	OUT_{30}	OUT_{30}	OUT_3
7	OUT_4	OUT_{29}	OUT_{29}	OUT_4
8	OUT_5	OUT_{28}	OUT_{28}	OUT_5
9	OUT_6	OUT_{27}	OUT_{27}	OUT_6
10	OUT_7	OUT_{26}	OUT_{26}	OUT_7
11	OUT_8	OUT_{25}	OUT_{25}	OUT_8
12	OUT_9	OUT_{24}	OUT_{24}	OUT_9
13	OUT_{10}	OUT_{23}	OUT_{23}	OUT_{10}
14	OUT_{11}	OUT_{22}	OUT_{22}	OUT_{11}
15	OUT_{12}	OUT_{21}	OUT_{21}	OUT_{12}
16	OUT_{13}	OUT_{20}	OUT_{20}	OUT_{13}
17	OUT_{14}	OUT_{19}	OUT_{19}	OUT_{14}
18	OUT_{15}	OUT_{18}	OUT_{18}	OUT_{15}
19	OUT_{16}	OUT_{17}	OUT_{17}	OUT_{16}
20	GROUND	GROUND	V_{BB}	V_{BB}

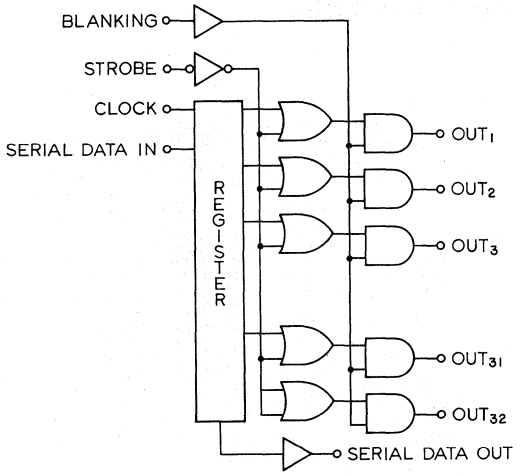
Dwg. No. A-14,243

PACKAGE 'A'

NOTE: S.D. IN = SERIAL DATA IN

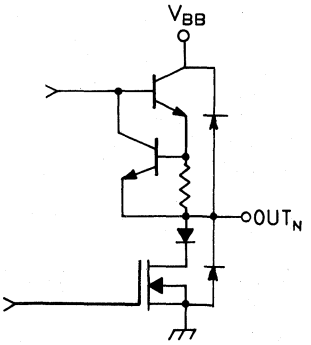
5

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-14,244

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,241

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{BB} = 100\ V$, $V_{DD} = 5\ V$ (unless otherwise noted)

Characteristic	Symbol	Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{BB} = 100\ V$, $V_{OUT} = 0\ V$	—	—	−100	µA
		$V_{BB} = V_{OUT} = 100\ V$	—	—	100	µA
Output Saturation Voltage	$V_{OUT(1)}$	$I_{OUT} = -1.0\ mA$	98	—	—	V
		$I_{OUT} = -10\ mA$	97	—	—	V
		$I_{OUT} = -15\ mA$	96	—	—	V
	$V_{OUT(0)}$	$I_{OUT} = 1.0\ mA$, $V_{DD} = 12\ V$	—	—	2.0	V
		$I_{OUT} = 10\ mA$, $V_{DD} = 12\ V$	—	—	4.0	V
		$I_{OUT} = 15\ mA$, $V_{DD} = 12\ V$	—	—	5.0	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	—	V
		$V_{DD} = 10\ V$	8.5	—	—	V
		$V_{DD} = 5.0\ V$	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 5.0\ V$ to $12\ V$	1.0	—	—	MΩ
Supply Current	$I_{DD(LOW)}$	$V_{DD} = 12\ V$, All outputs low	—	—	1.0	mA
	$I_{DD(HIGH)}$	$V_{DD} = 12\ V$, 8 outputs high	—	—	1.0	mA
Output Clamp Voltage	$V_{OUT(CLAMP)}$	$I_{OUT} = 20\ mA$	—	—	102.5	V
		$I_{OUT} = -20\ mA$	—	—	−2.5	V
Output Short-Circuit Current	I_{SC}		—	—	−20	mA
High-Voltage Supply Current	$I_{BB(LOW)}$	$V_{DD} = 12\ V$, All outputs low	—	—	1.0	mA
	$I_{BB(HIGH)}$	$V_{DD} = 12\ V$, 8 outputs high	—	—	15	mA

UCN-5881EP
BiMOS II DUAL 8-BIT LATCHED DRIVER
With Read Back

FEATURES

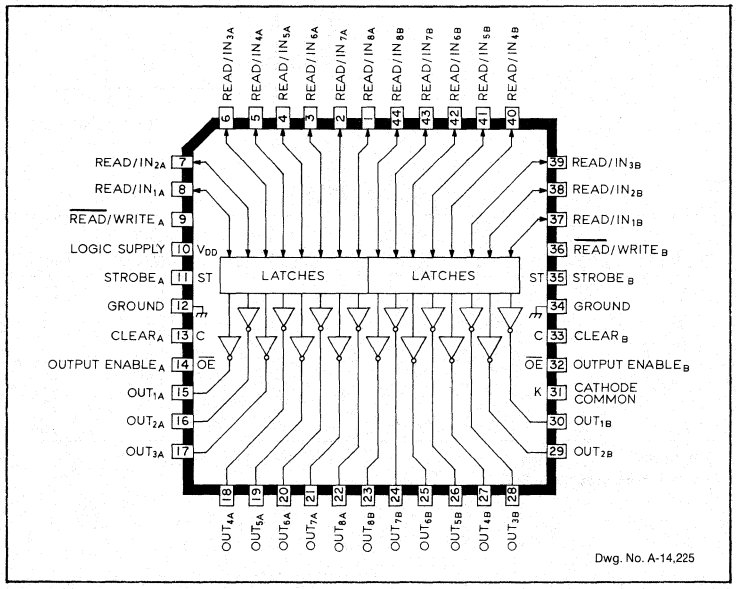
- 4.4 MHz Minimum Data Input Rate
- Low-Power CMOS Logic
- 20 V, 50 mA (Max.) Outputs
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low-Profile Leaded Chip Carrier

With 16 CMOS data latches (two sets of eight), CMOS control circuitry for each set of latches, and a bipolar saturated driver for each latch, the UCN-5881EP provides low-power interface with maximum flexibility. The driver includes thermal shutdown circuitry to protect against damage from high junction temperatures and clamp diodes for inductive load transient suppression.

The CMOS inputs cause minimal circuit loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull up resistors. When reading back, the data inputs will sink 8 mA (if its corresponding latch is low) or source 400 μA (if its corresponding latch is high). The read back feature is for error checking. It allows the system to verify that data has been received and latched.

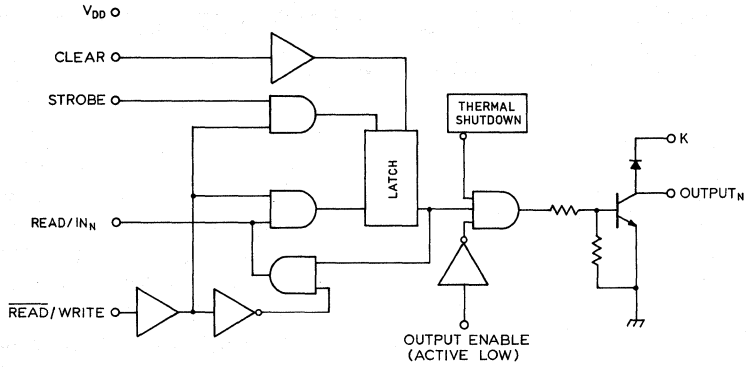
The bipolar outputs are suitable for use with low-power relays, solenoids, and stepping motors. The very-low output saturation voltage makes this device well-suited for driving LED arrays. The output transistors are capable of sinking 50 mA and will maintain at least 20 V in the OFF state. Outputs may be paralleled for higher current capability.

The UCN-5881EP dual 8-bit latched sink driver is complemented by the UCN-5882EP dual 8-bit latched source driver. It is rated for operation over the temperature range of −20°C to +85°C and is supplied in a plastic 44-lead chip carrier conforming to the JEDEC MS-007AB outline.



FUNCTIONAL BLOCK DIAGRAM

(1 of 16 Channels)

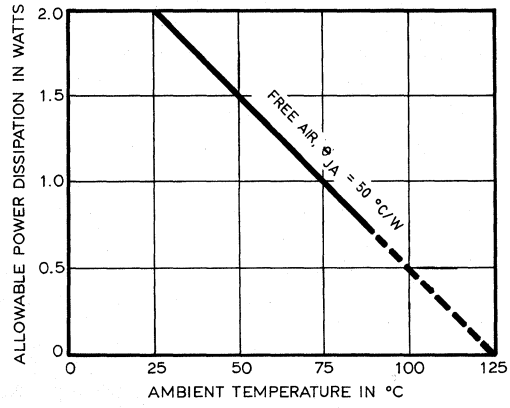


Dwg. No. A-14,227

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} . . . . . 20 V
Output Sustaining Voltage, $V_{CE(sus)}$ . . . . . 15 V
Output Current, I_{OUT} . . . . . 50 mA
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Logic Supply Voltage, V_{DD} . . . . . 15 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-14,226

TRUTH TABLE

Read/In	Strobe	Clear	Output Enable	$\overline{\text{Read}}$/Write	Latch Contents	Output
X	X	X	1	X	X	OFF
0	1	0	0	1	0	OFF
1	1	0	0	1	1	ON
X	0	0	0	1	n-1	n-1
X	X	1	X	X	0	OFF
n	X	0	X	0	n	n

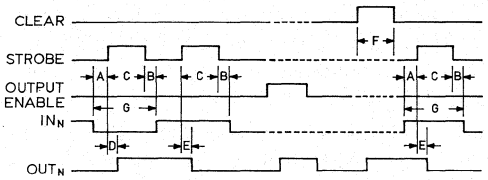
n = Present Latch Contents
n-1 = Previous Latch Contents

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 20 V	—	50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 10 mA	—	0.1	V
		I_{OUT} = 25 mA	—	0.5	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 25 mA, L = 2 mH	15	—	V
Input Voltage	$V_{IN(0)}$		−0.3	0.8	V
	$V_{IN(1)}$		3.5	5.3	V
Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−10	µA
	$I_{IN(1)}$	V_{IN} = 5 V	—	10	µA
Readback Output Voltage	$V_{OUT(1)}$	I_{OUT} = −400 µA	3.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 5.0 mA	—	0.8	V
Logic Supply Current	I_{DD}	All Drivers ON	—	12	mA
		All Drivers OFF	—	3.0	mA
Clamp Diode Leakage Current	I_R	V_R = 20 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 50 mA	—	1.5	V

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)



Dwg. No. A-14,228

A high on the $\overline{\text{READ}}$/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

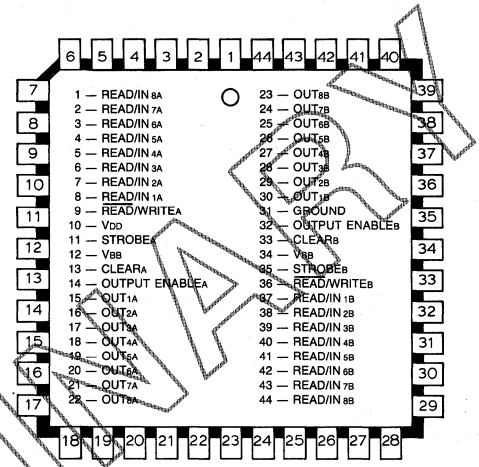
A low on the $\overline{\text{READ}}$/WRITE input will allow the latched data to be read back on the data input lines. The read back feature is for error checking applications and allows the system to verify that data has been received and latched.

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	150 ns
D. Typical Time Between Strobe Activation and Output ON to OFF transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON transition	500 ns
F. Minimum Clear Pulse Width	225 ns
G. Minimum Data Pulse Width	125 ns

UCN-5882EP
BiMOS II DUAL 8-BIT LATCHED SOURCE DRIVER
With Read Back

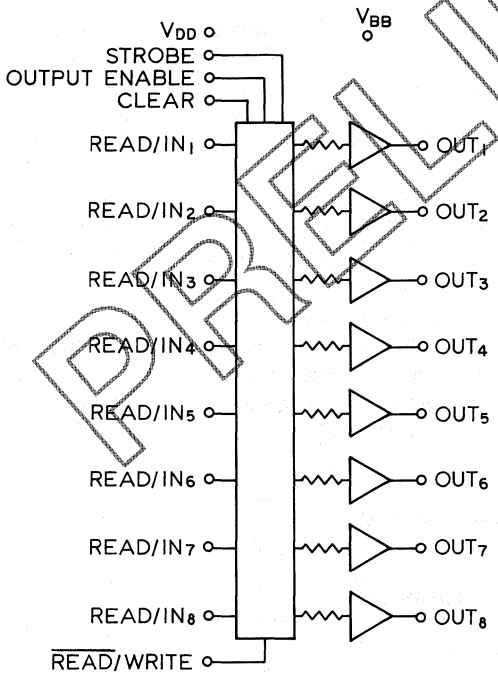
FEATURES

- READ/WRITE Inputs
- STROBE, CLEAR, OUTPUT ENABLE Functions
- Low-Power CMOS Logic
- 20 V, 50 mA Outputs
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low-Profile Leaded Chip Carrier



Dwg. No. A-14,246

FUNCTIONAL BLOCK DIAGRAM
½ UCN-5882EP



Dwg. No. A-14,247

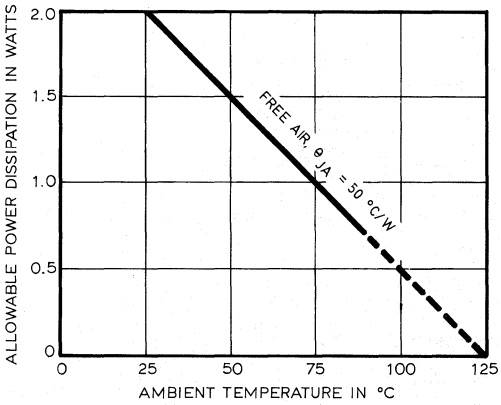
The UCN-5882EP has 16 CMOS data latches (two sets of eight), a bipolar non-Darlington driver for each latch, and CMOS control circuitry for two sets of common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides low-power interface with maximum flexibility. The UCN-5882EP includes thermal shutdown to protect against thermal damage and has read back capabilities.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with low-power relays, solenoids, stepping motors, and LEDs.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

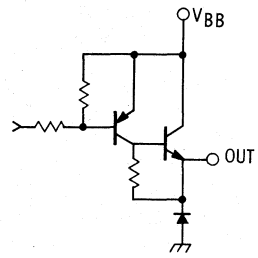
Output Voltage, V_{OUT} . . . . . 20 V
Output Current, I_{OUT} . . . . . −50 mA
Input Voltage, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Logic Supply Voltage, V_{DD} . . . . . 15 V
Package Power Dissipation, P_D . . . . . See Graph
Junction Temperature, T_J . . . . . +125°C
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-14,226

SOURCE DRIVER



Dwg.No. A-12,655

TRUTH TABLE

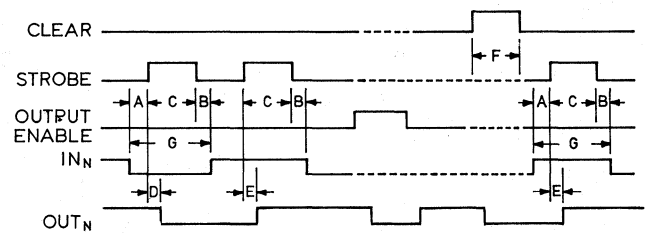
Read/In	Strobe	Clear	Output Enable	$\overline{\text{Read}}$/ Write	Latch Contents	Output
X	X	X	1	X	X	OFF
0	1	0	0	1	0	OFF
1	1	0	0	1	1	ON
X	0	0	0	1	n-1	n-1
X	X	1	X	X	0	OFF
n	X	0	X	0	n	n

n = Present Latch Contents.
n-1 = Previous Latch Contents.

5

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V, V_{BB} = 20 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V	—	50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = −25 mA	—	1.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = −25 mA, L = 2 mH	15	—	V
Input Voltage	$V_{IN(0)}$		−0.3	0.8	V
	$V_{IN(1)}$		3.5	5.3	V
Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−10	µA
	$I_{IN(1)}$	V_{IN} = 5 V	—	10	µA
Read Back Output Voltage	$V_{OUT(1)}$	I_{OUT} = −400 µA	3.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 5.0 mA	—	0.8	V
Logic Supply Current	I_{DD}		—	2.0	mA
Load Supply Current	I_{BB}	All Drivers ON, No Load	—	15	mA
		All Drivers OFF	—	50	µA
Clamp Diode Leakage Current	I_R	V_R = 20 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 50 mA	—	1.5	V



Dwg. No. A-14,317

TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

	V_{DD} = 5.0 V
A. Minimum Data Active Time before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active Time after Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	150 ns
D. Typical Time Between Strobe Activation and Output ON to OFF Transition	6.0 µs
E. Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F. Minimum Clear Pulse Width	225 ns
G. Minimum Data Pulse Width	125 ns

A high on the $\overline{\text{READ}}$/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their latches.

A low on the $\overline{\text{READ}}$/WRITE input will allow the latched data to be read back on the data input lines. The read back feature is for error checking applications and allows the system to verify that date has been received and latched.

UCN-5890A/B AND UCN-5891A/B BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

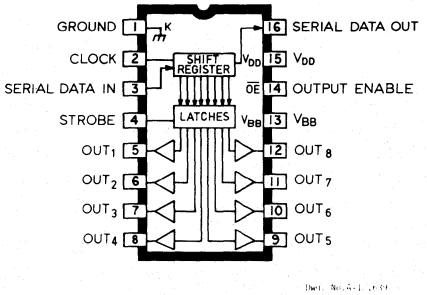
- 50 V or 80 V Source Outputs
- Output Current to −500 mA
- Output Transient-Suppression Diodes
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic and Latches

PRIMARILY DESIGNED for use with thermal or electromagnetic printers, the UCN-5890A/B and UCN-5891A/B BiMOS II serial-input, latched drivers combine an 8-bit CMOS register, associated latches, and control circuitry (strobe and output enable) with Darlington sourcing outputs. They may also be used with relays or multiplexed LED displays within their output limitation of −500 mA per driver.

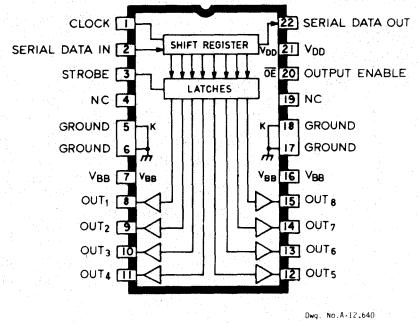
Suffix "A" devices are supplied in a standard 16-pin dual in-line plastic package. Complementary, 8-bit serial-input latched sink drivers are in Series UCN-5820A, described in Engineering Bulletin 26185.12. Suffix "B" devices are furnished in a 22-pin dual in-line package with heat-sink contact tabs that allows increased package power dissipation.

Electrical ratings for the four devices are identical except for allowable load voltage ratings. UCN-5890A and UCN-5890B are rated for operation with supply voltages of 20 V to 80 V and a minimum output sustaining voltage of 50 V. For applications using supply voltages of 20 V to 50 V (35 V sustaining), lower-cost UCN-5890A-2 and UCN-5890B-2 are recommended. The UCN-5891A and UCN-5891B are optimized for operation with supply voltages of 5 V to 50 V (35 V sustaining). A similar driver (featuring reduced output-saturation voltage), the UCN-5895A, is described in Engineering Bulletin 26182.14.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained.



UCN-5890A
UCN-5891A



UCN-5890B
UCN-5891B

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

All devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle.

5

ABSOLUTE MAXIMUM RATINGS at $T_A = +25°C$

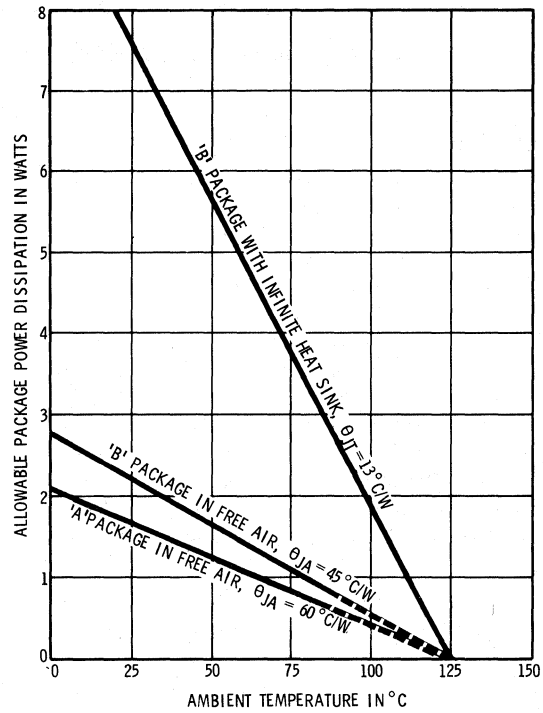
Output Voltage, V_{OUT} (UCN-5890A/B) . . . . . 80 V
(UCN-5890A/B-2) . . . . . 50 V
(UCN-5891A/B) . . . . . 50 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB}
(UCN-5890A/B) . . . . . 20 V to 80 V
(UCN-5890A/B-2) . . . . . 20 V to 50 V
(UCN-5891A/B) . . . . . 5.0 to 50 V
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current, I_{OUT} . . . . . -500 mA
Allowable Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

Number of Outputs ON at $I_{OUT} = -200$ mA	Max. Allowable Duty Cycle at T_A of					
	50°C	60°C	70°C	50°C	60°C	70°C
	Package "A"			Package "B"		
8	40%	34%	28%	53%	46%	39%
7	45%	39%	33%	60%	52%	44%
6	53%	46%	39%	70%	61%	51%
5	63%	55%	46%	84%	73%	62%
4	79%	68%	58%	100%	91%	77%
3	100%	91%	77%	100%	100%	100%
2	100%	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%	100%

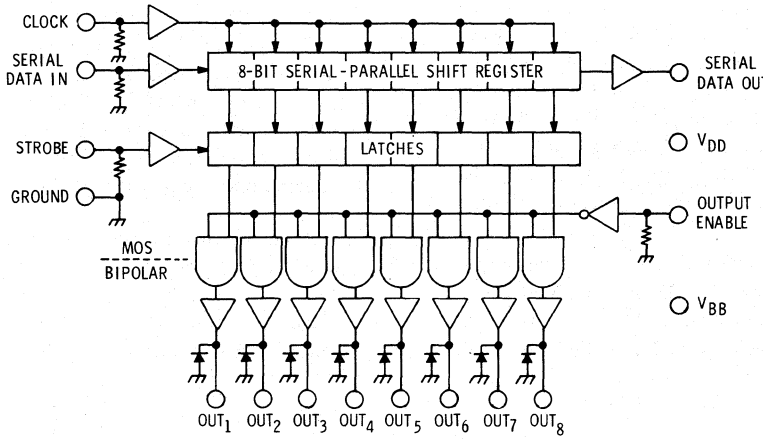
Also see Allowable Output Current graphs

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



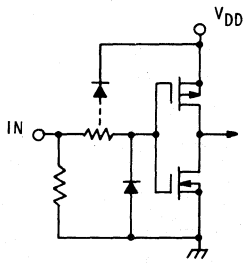
Dwg. No. A-12,645

FUNCTIONAL BLOCK DIAGRAM



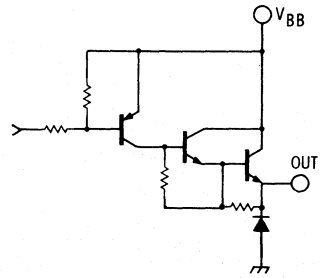
Dwg.No. A-12,654

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,520

TYPICAL OUTPUT DRIVER

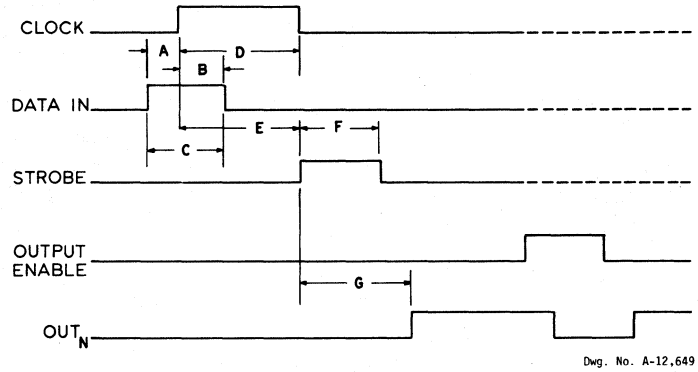


Dwg. No.A-12,648

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 80$ V (UCN-5890A/B) or 50 V (UCN-5890A/B-2 & UCN-5891A/B), $V_{DD} = 5$ V to 12 V (unless otherwise noted)

Characteristic	Symbol	V_{BB}	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	Max.	$T_A = +25°C$	—	−50	µA
			$T_A = +70°C$	—	−100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	50 V	$I_{OUT} = -100$ mA	—	1.8	V
			$I_{OUT} = -225$ mA	—	1.9	V
			$I_{OUT} = -350$ mA	—	2.0	V
Output Sustaining Voltage	$V_{CE(sus)}$	Max.	$I_{OUT} = -350$ mA, L = 2 mH, UCN-5890A/B-2 & UCN-5891A/B	35	—	V
			$I_{OUT} = -350$ mA, L = 2 mH, UCN-5890A & UCN-5890B only	50	—	V
Input Voltage	$V_{IN(1)}$	50 V	$V_{DD} = 5.0$ V	3.5	5.3	V
			$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	50 V	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	50 V	$V_{DD} = V_{IN} = 5.0$ V	—	50	µA
			$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	50 V	$V_{DD} = 5.0$ V	100	—	kΩ
			$V_{DD} = 12$ V	50	—	kΩ
Clock Frequency	f_c	50 V		3.3	—	MHz
Serial Data Output Resistance	R_{OUT}	50 V	$V_{DD} = 5.0$ V	—	20	kΩ
			$V_{DD} = 12$ V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	50 V	Output Enable to Output, $I_{OUT} = -350$ mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	50 V	Output Enable to Output, $I_{OUT} = -350$ mA	—	10	µs
Supply Current	I_{BB}	50 V	All outputs ON, All outputs open	—	10	mA
			All outputs OFF	—	200	µA
	I_{DD}	50 V	$V_{DD} = 5$ V, All outputs OFF, Inputs = 0 V	—	100	µA
			$V_{DD} = 12$ V, All outputs OFF, Inputs = 0 V	—	200	µA
			$V_{DD} = 5$ V, One output ON, All inputs = 0 V	—	1.0	mA
			$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	Max.	$T_A = +25°C$	—	50	µA
			$T_A = +70°C$	—	100	µA
Diode Forward Voltage	V_F	Open	$I_F = 350$ mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,649

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... 75 ns
C. Minimum Data Pulse Width ..... 150 ns
D. Minimum Clock Pulse Width ..... 150 ns
E. Minimum Time Between Clock Activation and Strobe ..... 300 ns
F. Minimum Strobe Pulse Width ..... 100 ns
G. Typical Time Between Strobe Activation and Output Transition ..... 1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

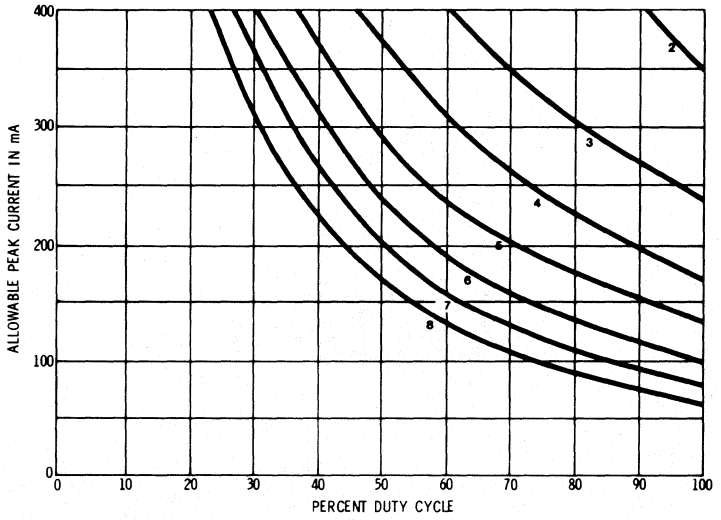
TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2}R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2}R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1}R_N$	R_N				
		$X\ X\ X\ \ldots X\ X$	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$
					$X\ X\ X\ \ldots X\ X$	H	$L\ L\ L\ \ldots L\ L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

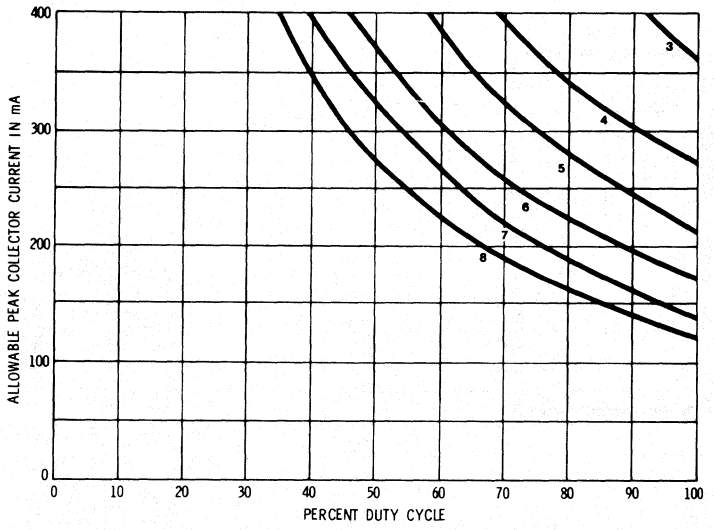
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE
at +25°C Free-Air Temperature

UCN-5890A AND UCN-5891A



Dwg. No. A-12,647

UCN-5890B AND UCN-5891B

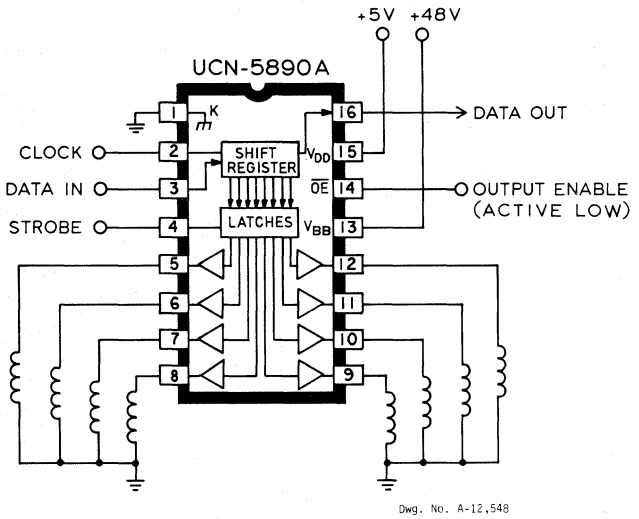


Dwg. No. A-12,646

5

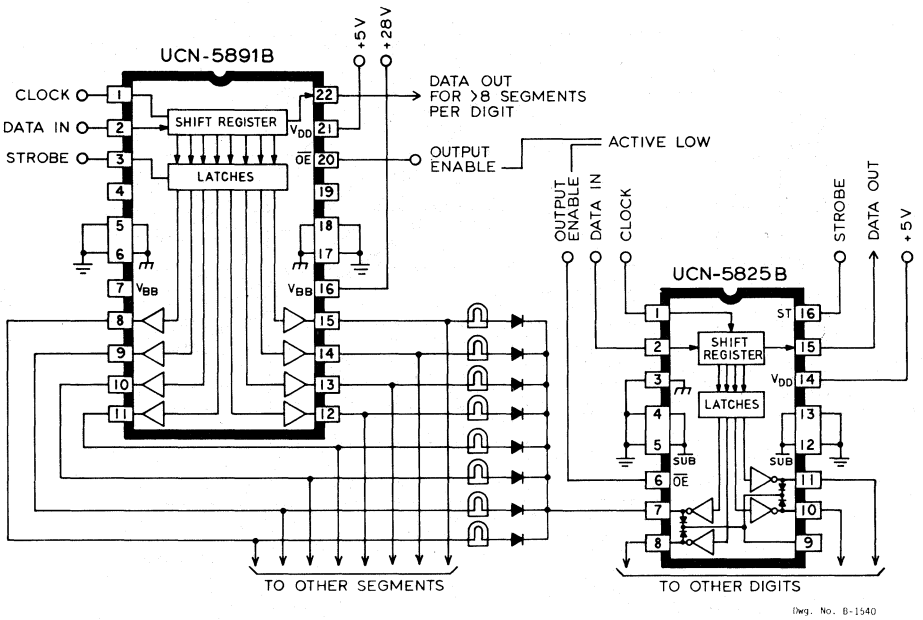
TYPICAL APPLICATIONS

SOLENOID OR RELAY DRIVER



Dwg. No. A-12,548

MULTIPLEXED INCANDESCENT LAMP DRIVER

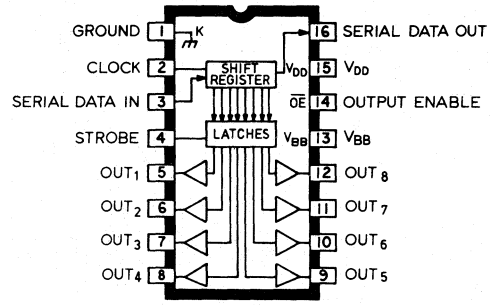


Dwg. No. B-1540

UCN-5895A AND UCN-5895A-2 BiMOS II 8-BIT, SERIAL-INPUT, LATCHED SOURCE DRIVERS

FEATURES

- Low Output-Saturation Voltage
- Source Outputs to 50 V
- Output Current to −250 mA
- 3.3 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic & Latches



Dwg. No.A-12,639

UCN-5895A AND UCN-5895A-2 BiMOS II serial-input, latched source drivers are designed for use in applications requiring low output-saturation voltages and currents to −250 mA per driver. Each driver combines an 8-bit CMOS register, associated latches and control circuitry (strobe and output enable), with saturated bipolar emitter-follower outputs. Typical loads are low-voltage LEDs and incandescent displays. They can also be used with multiplexed LED displays, thermal printers, or electromagnetic printers within their output limitations.

The UCN-5895A is rated for operation with supply voltages to 50 V and features a minimum output sustaining voltage of 35 V. The more economical UCN-5895A-2 is for use with supply voltages to 25 V (15 V sustaining). Under normal operation conditions, at +25°C, all outputs will source −120 mA continuously without derating. Similar drivers, featuring Darlington outputs for increased output ratings, are the UCN-5890A/B and UCN-5891A/B.

BiMOS II devices can operate at greatly improved data-input rates. With a 5 V supply, they will typically operate at better than 5 MHz. At 12 V, significantly higher speeds are obtained.

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors to ensure a proper input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

These devices are rated for continuous operation over the temperature range of −20°C to +85°C. Because of limitations on package power dissipation, the simultaneous operation of all output drivers may require a reduction in duty cycle. The UCN-5895A and UCN-5895A-2 are supplied in standard 16-pin dual in-line plastic packages with copper lead frames for increased allowable package power dissipation.

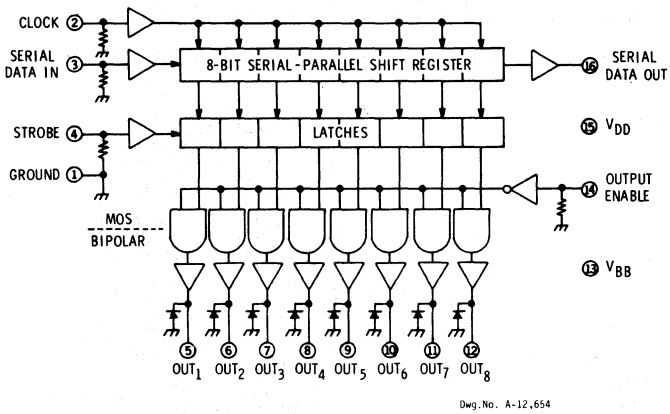
ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Output Voltage, V_{OUT} (UCN-5895A) ..... 50 V
(UCN-5895A-2) ..... 25 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 12 V
Driver Supply Voltage Range, V_{BB}
(UCN-5895A) ..... 5.0 V to 50 V
(UCN-5895A-2) ..... 5.0 V to 25 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... −250 mA
Allowable Package Power Dissipation, P_D ..... 1.67 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +125°C
*Derate at the rate of 16.67 mW/°C above T_A = +25°C.

Caution: Sprague Electric CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

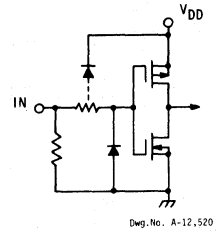
5

FUNCTIONAL BLOCK DIAGRAM



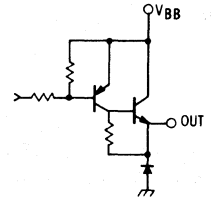
Dwg.No. A-12,654

TYPICAL INPUT CIRCUIT



Dwg.No. A-12,520

TYPICAL OUTPUT DRIVER

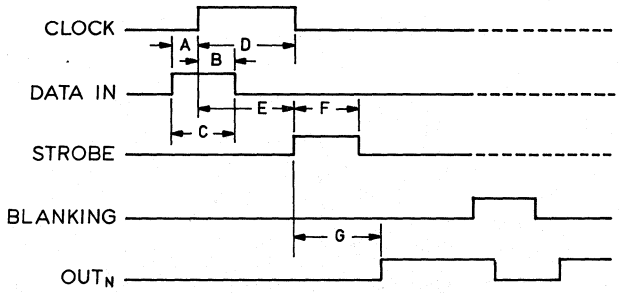


Dwg.No. A-12,655

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 25$ V, $V_{DD} = 5$ V to 12 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{OUT}	$T_A = +25°C$	—	−50	µA
		$T_A = +70°C$	—	−100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = -60$ mA	—	1.1	V
		$I_{OUT} = -120$ mA	—	1.2	V
Output Sustaining Voltage	$V_{CE(sus)}$	$I_{OUT} = -120$ mA, L = 2 mH, UCN-5895A only	35	—	V
		$I_{OUT} = -120$ mA, L = 2 mH, UCN-5895A-2 only	15	—	V
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$	$V_{DD} = 5$ V to 12 V	−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	50	µA
		$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	100	—	kΩ
		$V_{DD} = 12$ V	50	—	kΩ
Clock Frequency	f_c		3.3	—	MHz
Serial Data-Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 12$ V	—	6.0	kΩ
Turn-ON Delay	t_{PLH}	Output Enable to Output, $I_{OUT} = -120$ mA	—	2.0	µs
Turn-OFF Delay	t_{PHL}	Output Enable to Output, $I_{OUT} = -120$ mA	—	10	µs
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10	mA
		All outputs OFF	—	200	µA
	I_{DD}	$V_{DD} = 5$ V, All outputs OFF, Inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, Inputs = 0 V	—	200	µA
		$V_{DD} = 5$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA
Diode Leakage Current	I_R	$V_R = 25$ V, $T_A = +25°C$	—	50	µA
		$V_R = 25$ V, $T_A = +70°C$	—	100	µA
Diode Forward Voltage	V_F	$I_F = 120$ mA	—	2.0	V

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.



Dwg. No. A-12,649A

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . 75 ns
C. Minimum Data Pulse Width . . . . . 150 ns
D. Minimum Clock Pulse Width . . . . . 150 ns
E. Minimum Time Between Clock Activation and Strobe . . . . . 300 ns
F. Minimum Strobe Pulse Width . . . . . 100 ns
G. Typical Time Between Strobe Activation and Output Transition . . . . . 1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

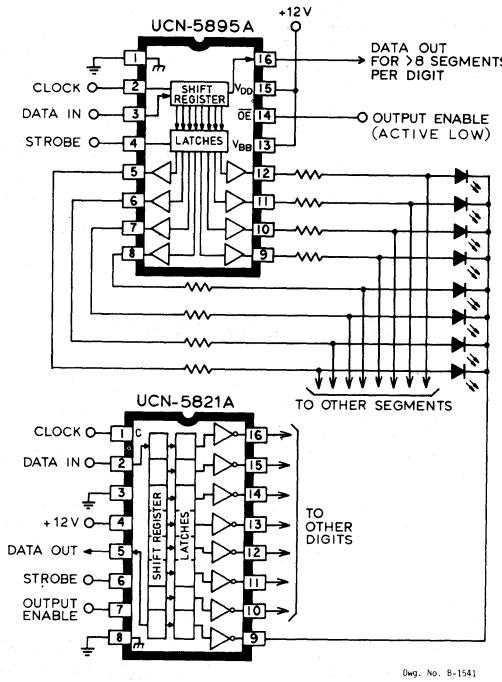
5

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$	Blanking Input	Output Contents $I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2}R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2}R_{N-1}$	R_{N-1}				
X	⎎	$R_1\ R_2\ R_3\ \ldots R_{N-1}R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1}R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1}P_N$
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

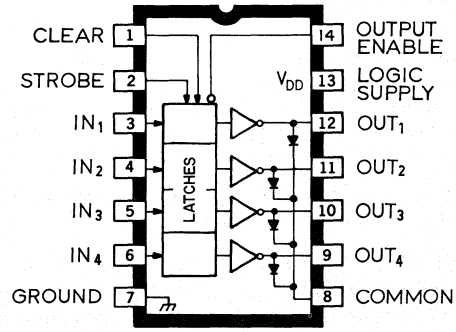
TYPICAL APPLICATION



UCN-5900A AND UCN-5901A BiMOS III LATCHED DRIVERS

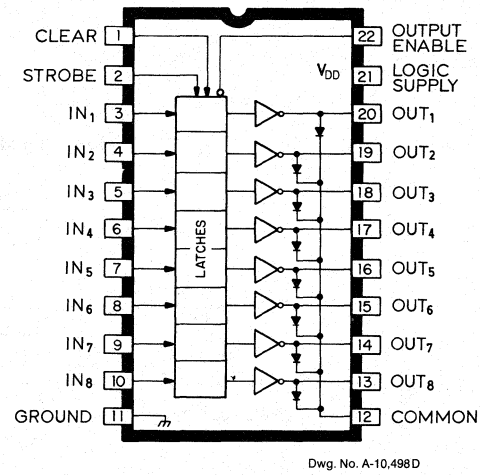
FEATURES

- High-Voltage, High-Current Outputs
- Output Sustaining Voltage of 90 V, Minimum
- Output Transient Protection
- 2 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches



Dwg. No. A-10,499D

UCN-5900A



Dwg. No. A-10,498D

UCN-5901A

UCN-5900A and UCN-5901A latched drivers are high-voltage, high-current integrated circuits with four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, and other inductive loads requiring sustaining voltage ratings up to 90 V. UCN-5900A contains four latched drivers; UCN-5901A contains eight latched drivers.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL circuits may require the use of appropriate pull-up resistors. BiMOS latches will typically operate at better than 3 MHz with a 5 V supply. With a 12 V supply, higher speeds are obtained.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 400 mA and will withstand at least 150 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The UCN-5900A 4-latch device, is furnished in a standard 14-pin dual in-line plastic package. The UCN-5901A 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400″ (10.16 mm) rows. To simplify circuit board layout, all outputs are opposite their respective inputs.

5

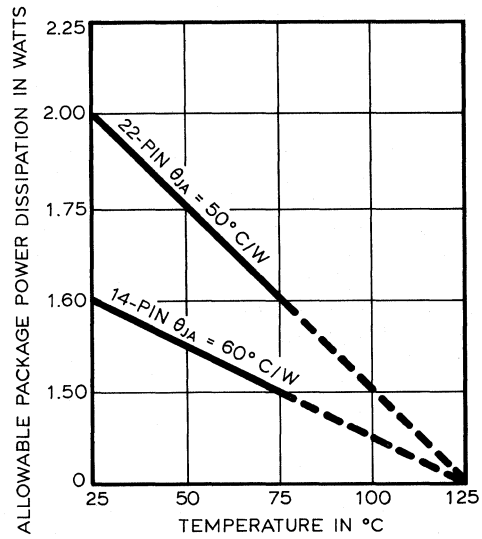
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 150 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Continuous Collector Current, I_C . . . . . 400 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.

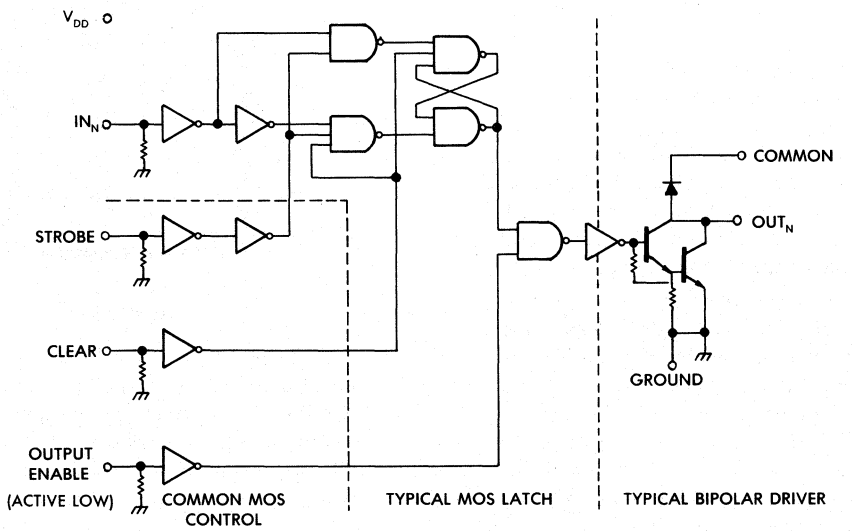
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



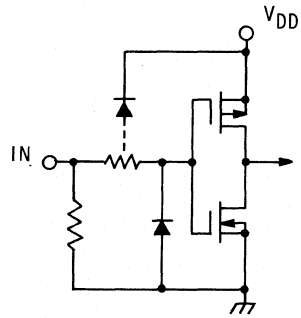
Dwg. No. A-14,220

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,495B

TYPICAL INPUT CIRCUIT



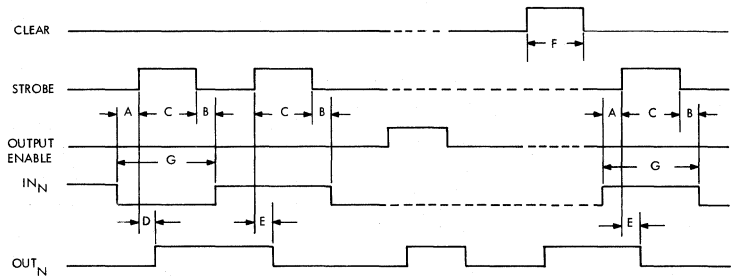
Dwg. No. A-12,520

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 150\ V, T_A = +25°C$	—	—	50	μA
		$V_{CE} = 150\ V, T_A = +70°C$	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	1.2	1.4	V
		$I_C = 200\ mA$	—	1.4	1.6	V
		$I_C = 350\ mA, V_{DD} = 7.0\ V$	—	1.6	1.9	V
Collector-Emitter Sustaining Voltage	$V_{CE(sus)}$	$I_C = 300\ mA, L = 2\ mH$	90	—	—	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	—	V
		$V_{DD} = 10\ V$	8.5	—	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	200	—	kΩ
		$V_{DD} = 10\ V$	50	300	—	kΩ
		$V_{DD} = 5.0\ V$	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	—	200	μA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	50	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 150\ V, T_A = +25°C$	—	—	50	μA
		$V_R = 150\ V, T_A = +70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

5



Dwg. No. A-10,895A

TIMING CONDITIONS

T_A = +25°C, Logic Levels are V_{DD} and Ground

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time)	100 ns
C. Minimum Strobe Pulse Width	300 ns
D. Typical Time Between Strobe Activation and Output ON to OFF transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON transition	500 ns
F. Minimum Clear Pulse Width	300 ns
G. Minimum Data Pulse Width	500 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

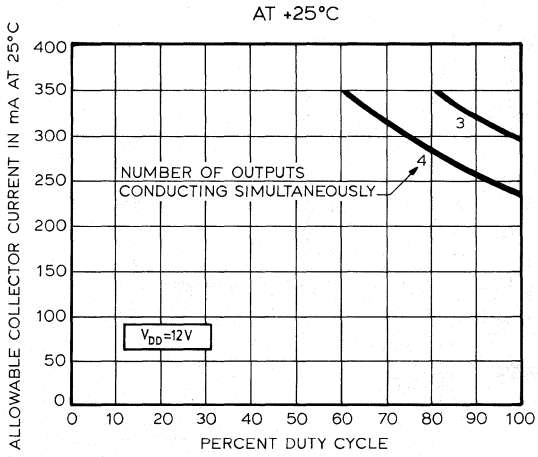
TRUTH TABLE

				OUT_N	
IN_N	STROBE	CLEAR	OUTPUT ENABLE	t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

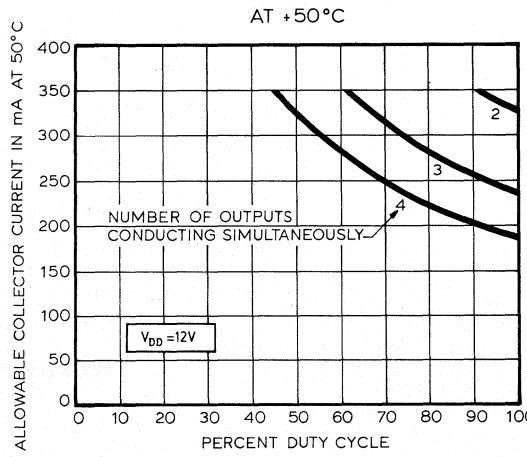
X = irrelevant
t-1 = previous output state
t = present output state

COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5900A



Dwg. No. A-14,221



Dwg. No. A-14,222

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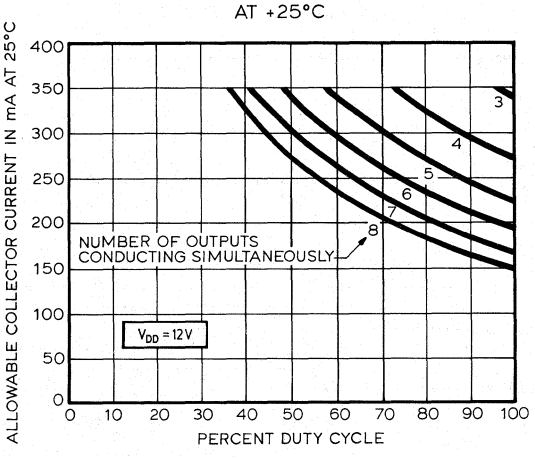
UCN-5901A



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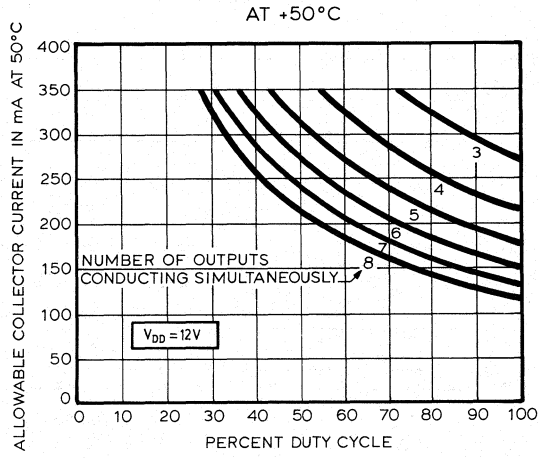

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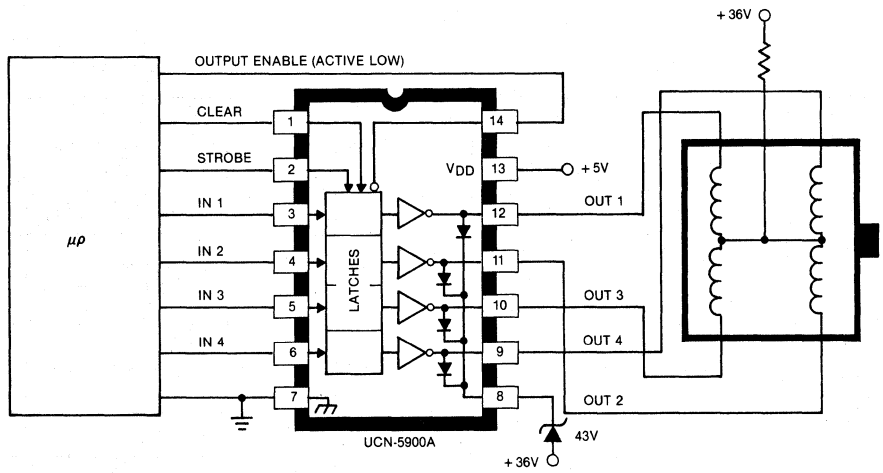
TYPICAL APPLICATION

UNIPOLAR STEPPER-MOTOR DRIVER



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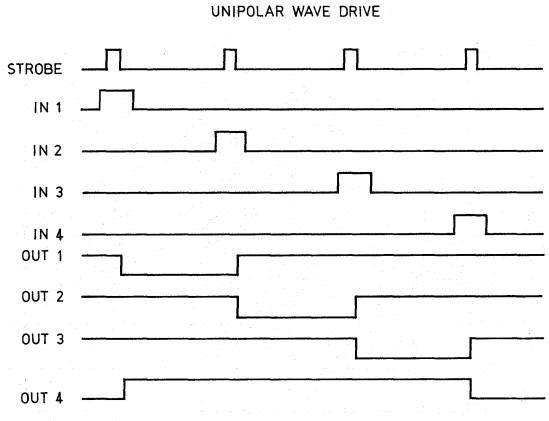

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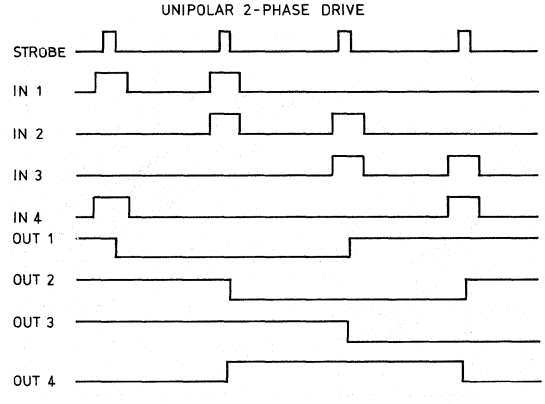

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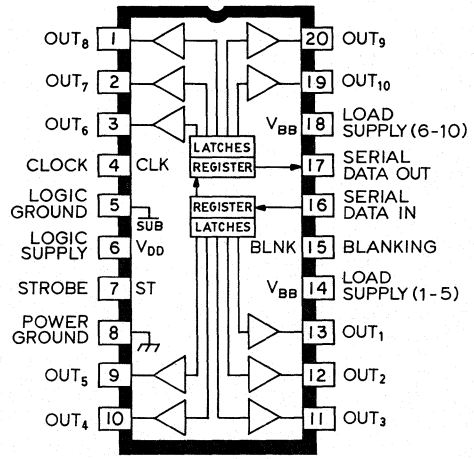
UCN-5910A HIGH-VOLTAGE BiMOS III 10-BIT, SERIAL-INPUT, LATCHED DRIVER

FEATURES

- To 150 V Output Breakdown
- 50 mA Push-Pull Outputs
- 3 MHz Minimum Data Input Rate
- Low-Power CMOS Latches
- Blanking and Strobe Functions

UCN-5910A is a smart power integrated circuit combining high-speed CMOS logic and high-voltage, power driver outputs. This serial-input, latched driver is especially useful with ink-jet and piezoelectric printers, large flat-panel vacuum-fluorescent or AC plasma displays. The UCN-5910A has an output rating of 150 V and ±50 mA. For applications requiring output ratings to only 135 V, the economical type UCN-5910A-2 is recommended. The lower-cost device is identical to the basic part, except for the minimum output breakdown voltage.

The 10-bit CMOS shift register and latches are designed for operation over a logic supply range of 5 V to 12 V. The high-impedance inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure an input logic high. Using BiMOS III logic for improved data entry rates, the CMOS circuitry will operate at better than 3.3 MHz with a 5 V supply. With a 12 V supply, significantly higher speeds are obtained. A CMOS serial-data output allows cascading devices for multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.



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The output drivers are high-voltage Darlington source drivers with DMOS sink drivers. Especially important when driving loads of 100 V or more, the active pull-down function provides better output switching than passive pulldowns.

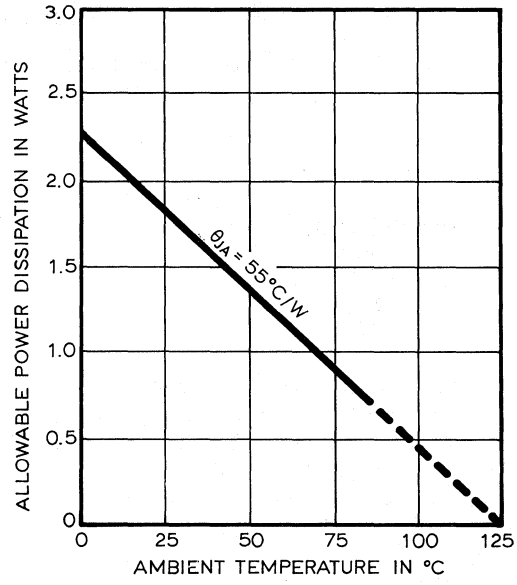
The UCN-5910A and UCN-5910A-2 are supplied in 20-pin dual in-line plastic packages. They can be operated over the temperature range of −20°C to +85°C. Copper lead frames allow all outputs (50% duty cycle) to be operated at ±20 mA at ambient temperatures up to +30°C, or at ±15 mA to +55°C.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Driver Supply Voltage, V_{BB} (UCN-5910A) . . . . . 150 V
(UCN-5910A-2) . . . . . 135 V
Output Current, I_{OUT} . . . . . ±50 mA
Logic Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage, V_{IN} . . . . . -0.3 V to $V_{DD}+0.3$ V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+125°C$

Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



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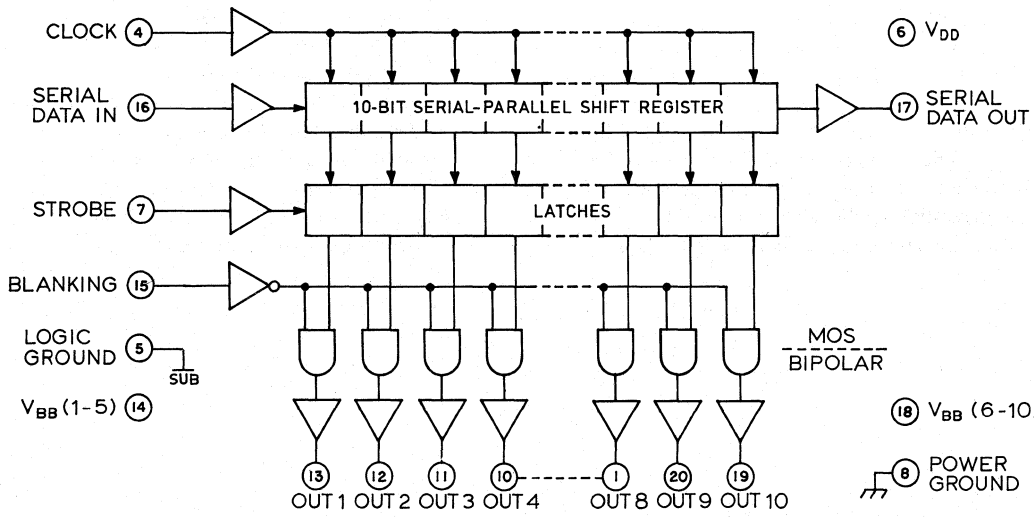
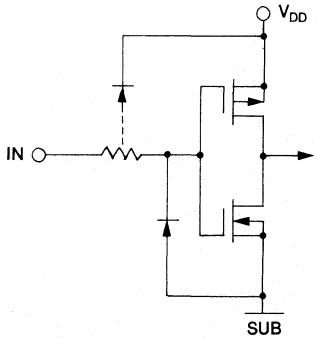
FUNCTIONAL BLOCK DIAGRAM



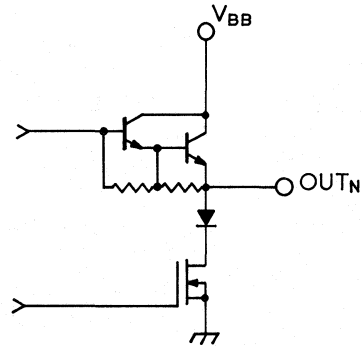
Dwg. No. A-14,214

TYPICAL INPUT CIRCUIT



Dwg. No. A-13,050

TYPICAL OUTPUT DRIVER

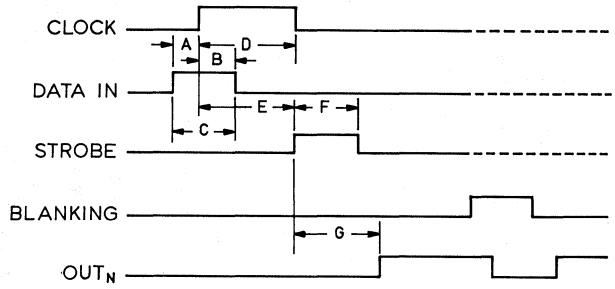


Dwg. No. A-14,219

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 135 V (UCN-5910A-2) or 150 V (UCN-5910A), unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 5 V			Limits @ V_{DD} = 12 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V, T_A = +70°C	—	−5.0	−15	—	−5.0	−15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = −40 mA, V_{BB} = 135 V	130	—	—	130	—	—	V
		I_{OUT} = −40 mA, V_{BB} = 150 V*	145	—	—	145	—	—	V
	$V_{OUT(0)}$	I_{OUT} = 5 mA	—	2.0	3.5	—	2.0	3.5	V
		I_{OUT} = 40 mA	—	—	—	—	15	25	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	10	—	—	—	—	—	mA
		V_{OUT} = 20 V to V_{BB}	—	—	—	25	—	—	mA
Input Voltage	$V_{IN(1)}$		3.5	—	5.3	10.5	—	12.3	V
	$V_{IN(0)}$		−0.3	—	+0.8	−0.3	—	+0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	0.05	0.5	—	0.1	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	—	−0.05	−0.5	—	−1.0	−1.0	µA
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = −200 µA	4.5	4.7	—	11.7	11.8	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	200	250	—	100	200	mV
Maximum Clock Frequency	f_{clk}		3.3	5.0	—	—	7.5	—	MHz
Supply Current	$I_{DD(1)}$	All Outputs High	—	350	500	—	700	850	µA
	$I_{DD(0)}$	All Outputs Low	—	350	500	—	700	850	µA
	$I_{BB(1)}$	Outputs High, No Load	—	1.0	2.0	—	1.0	2.0	mA
	$I_{BB(0)}$	Outputs Low	—	10	100	—	10	100	µA
Blanking to Output Delay	t_{PHL}	C_L = 30 pF	—	300	550	—	250	500	ns
	t_{PLH}	C_L = 30 pF	—	750	1000	—	750	1000	ns
Output Fall Time	t_f	C_L = 30 pF	—	500	750	—	300	550	ns
Output Rise Time	t_r	C_L = 30 pF	—	1100	1350	—	1100	1350	ns

Negative current is defined as coming out of (sourcing) the specified device pin.
*UCN-5910A only.



Dwg. No. A-12,649A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimun Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	750 ns

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H	⎍	$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L	⎍	$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X	⎍	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

RELIABILITY OF SERIES UCN-4800A AND UCN-5800A BiMOS DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series UCN-4800A and UCN-5800A BiMOS integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, burn-in, and accelerated-life tests:

1) Qualification testing is performed at an ambient temperature of +125°C, reduced so as to limit junction temperature to +150°C, for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure-rate data in a reasonable period of time.
2) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found that most failures are due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, are typically less than 0.1%.
3) Accelerated-life testing is performed at temperatures above +125°C and is used to generate failure-rate data.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution can be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminate level.

Table I contains data produced by life tests that were conducted at +150°C. The data include the number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C.

The data at the bottom of Table I are compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% fail-point. The median life at a junction temperature of +150°C is, in this case, 31,000 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1]

TABLE I
TEST RESULTS AT T_J = +150°C

		HOURS ON TEST											
TEST NUMBER	QTY.	48	90	150	300	600	1200	1800	2400	3000	5000	6000	7000
		NUMBER OF FAILURES											
1	35	0	0	0	0	0	0	0	0	0	0	5	7
2	25	0	0	3	0	1	6	—	—	—	—	—	—
3	21	0	1	—	—	—	—	—	—	—	—	—	—
4	30	0	0	4	9	—	—	—	—	—	—	—	—
5	17	0	0	0	0	2	0	0	0	0	1	0	2
6	20	0	0	3	10	0	—	—	—	—	—	—	—
7	20	0	0	0	0	0	2	0	1	0	0	—	—
8	25	0	0	1	0	2	0	2	0	0	0	1	—
9	25	0	0	0	1	0	0	0	0	0	2	—	—
10	25	0	0	0	0	0	0	—	—	—	—	—	—
11	30	0	0	0	0	0	0	0	—	—	—	—	—
12	30	0	0	0	0	0	0	0	—	—	—	—	—
13	30	0	0	0	5	0	0	0	0	0	—	—	—
14	30	0	0	0	0	0	1	0	2	—	—	—	—
15	26	0	0	0	—	—	—	—	—	—	—	—	—
16	30	0	0	0	0	—	—	—	—	—	—	—	—
17	20	1	0	0	1	0	0	—	—	—	—	—	—
18	25	0	0	0	0	0	0	—	—	—	—	—	—
19	28	0	0	0	0	0	0	—	—	—	—	—	—
20	45	0	0	0	0	0	0	—	—	—	—	—	—
21	25	0	0	0	0	0	—	—	—	—	—	—	—
TOTAL ON TEST		562	561	540	503	430	387	228	166	136	111	69	44
TOTAL FAILURES		1	1	11	26	5	9	2	3	0	3	6	9
TOTAL GOOD		561	560	529	477	425	378	226	163	136	108	63	35
P_s		.998	.998	.980	.948	.988	.977	.991	.982	1.00	.973	.913	.795
Cumulative P_s		.998	.996	.976	.926	.915	.894	.886	.870	.870	.846	.773	.615
$P_f = 1 - P_s$		.002	.004	.024	.074	.085	.106	.114	.130	.130	.154	.227	.385
% Failures		0.18	.036	2.39	7.43	8.51	10.6	11.4	13.0	13.0	15.4	22.7	38.5

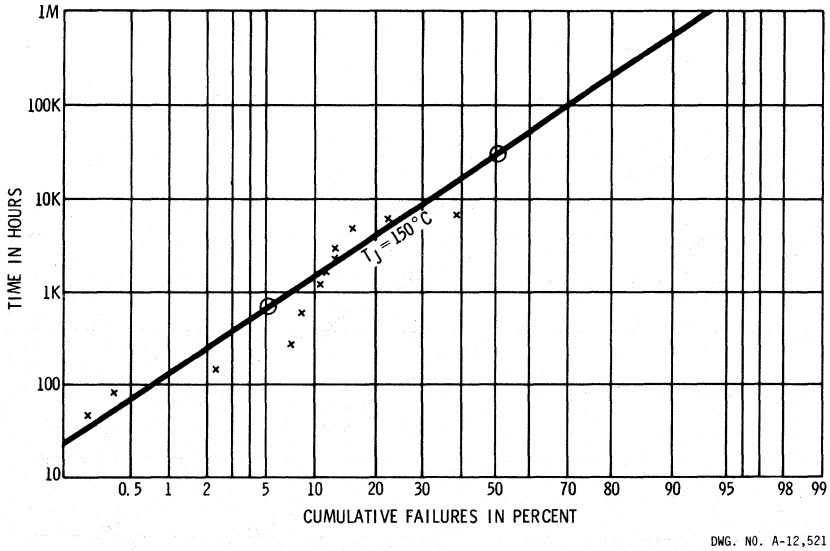


Figure 1
CUMULATIVE PERCENT FAILURES

The Arrhenius equation is:

$$V_r = V_r^o e^{-\epsilon/kT}$$

where V_r^o = a constant
ϵ = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5710M, and Series UDN-2980A devices at multiple temperatures. Failure analysis of devices rejected during that testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. The Arrhenius plot gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of ϵ = 1.0 eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life at reduced junction temperatures can now be determined using Figure 2. It must be emphasized that this is junction temperature and *not* ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\theta_{JA} + T_A \quad \text{or} \quad T_J = P_D\theta_{JC} + T_C$$

The median lifetime, or 50% fail-point, as graphically determined in Figure 2, is approximately 22 years at +125°C or 190 years at +100°C junction temperature.

The approximate failure rate (FR) may be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life line. The actual instantaneous failure rate can be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(1.7 \times 10^6 \text{ hours})$$
$$= 0.06\%/1000 \text{ hours} = 600 \text{ FIT}$$

where *FIT* = failures per 10^9 unit-hours

Other failure-rate values have been calculated and appear in Table II.

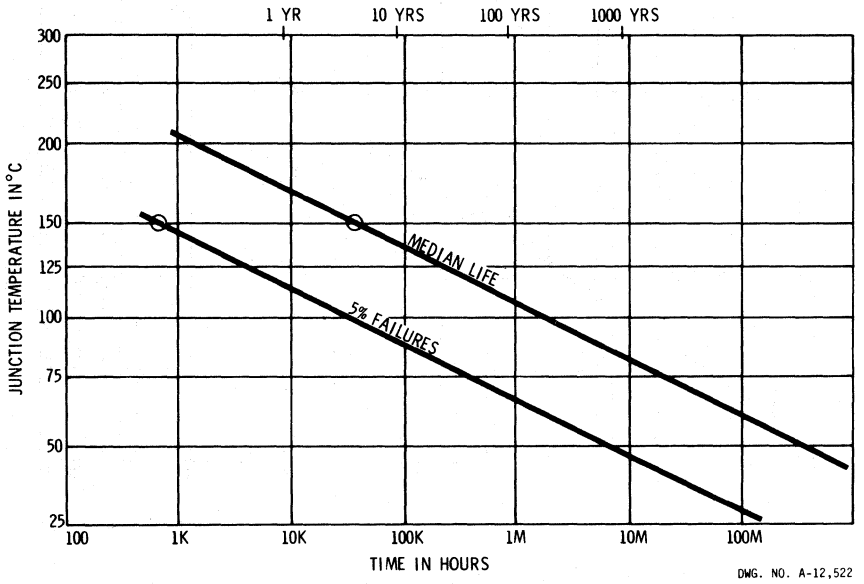


Figure 2
MEDIAN LIFE

TABLE II
SERIES UCN-4800A AND UCN-5800A FAILURE RATE

T_J (°C)	Median Life (h)	Failure Rate (%/1000h)	Failures In Time (No./10^9 unit-hours)
125	2×10^5	0.5	5000
100	1.7×10^6	0.06	600
75	1.7×10^7	0.006	60
50	3×10^8	0.0003	3

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides a failure rate within design objectives.

Figure 2 shows that a design with a continuous operating junction temperature of +100°C (internal power dissipation plus external ambient temperature) would reach the 5% failure point in 3.8 years. Lowering the junction temperature to +75°C increases the time to the 5% failure point to 42 years.

A complete sequence of environmental tests, including temperature cycle, pressure cooker, and biased humidity tests, are continuously monitored to ensure that assembly and package technology remain within established units.

The environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K.E., and Bird, D.W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208-213.

BiMOS II POWER DRIVERS

THE second generation of merged CMOS/bipolar integrated circuits extends the lead in innovative interface forged by Sprague Electric's original BiMOS power drivers.

Higher-density CMOS logic gives BiMOS II integrated circuits improved switching speeds at reduced costs. With a 5 V supply, second generation BiMOS typically operates at data input rates above 5 MHz; at 12 V, significantly higher speeds are obtainable. The BiMOS II series also offers new and improved functions.

Reliable, single-chip BiMOS II solutions are available for a wide variety of peripheral and power interface problems. Two or more devices are no longer required to interface low-level (TTL, CMOS, NMOS, PMOS) LSI or microprocessor functions with power loads such as LEDs, gas-discharge or vacuum-fluorescent displays, relays, solenoids, thermal printers, motors, impact printer hammers, and incandescent lamps. Since all BiMOS devices include logic and control in addition to power functions, they also free the microprocessor from many housekeeping tasks.

SERIES UCN-5900 BiMOS III
***HIGH-VOLTAGE* INTERFACE DRIVERS**

THE original UCN-4800 BiMOS interface integrated circuit designs evolved into high-speed UCN-5800 BiMOS II designs. Improvements continue with the new 150 V Sprague Series UCN-5900 *BiMOS III* designs.

Original BiMOS Type Number	BiMOS II Type Number	BiMOS III Type Number
UCN-4401A (50 V)	UCN-5800A (50 V)	UCN-5900A (150 V)
UCN-4801A (50 V)	UCN-5801A (50 V)	UCN-5901A (150 V)
UCN-4810A-1 (80 V)	UCN-5810A-1 (80 V)	UCN-5910A (150 V)

5

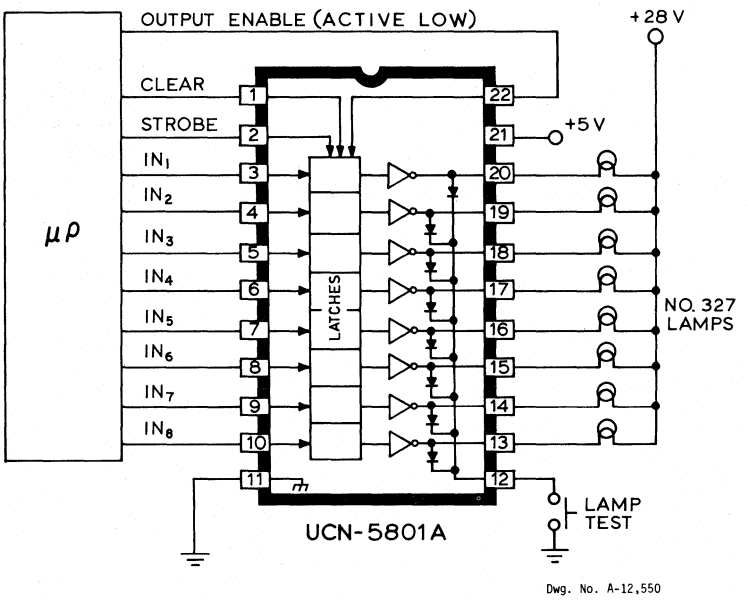
INCANDESCENT LAMP DRIVERS

EACH of the UCN-5800A or UCN-5801A open-collector Darlington outputs will sink up to 500 mA and will sustain at least 50 V in the OFF state. The high peak current rating of these devices allows their use with the high inrush (10×) currents normally associated with incandescent lamps. Internal diodes can be used to perform the lamp test function. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current: Either a reduction in output current or a suitable combination of duty cycle and number of active outputs is usually required.

The UCN-5800A is supplied in a standard 14-lead DIP. The UCN-5801A is furnished in a 22-lead DIP with 0.400″ row spacing.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . . 45 V
Logic Supply Voltage Range . . . . . 5.0 V to 12 V
Continuous Output Current . . . . . 350 mA



PLANAR GAS-DISCHARGE DISPLAY DRIVERS

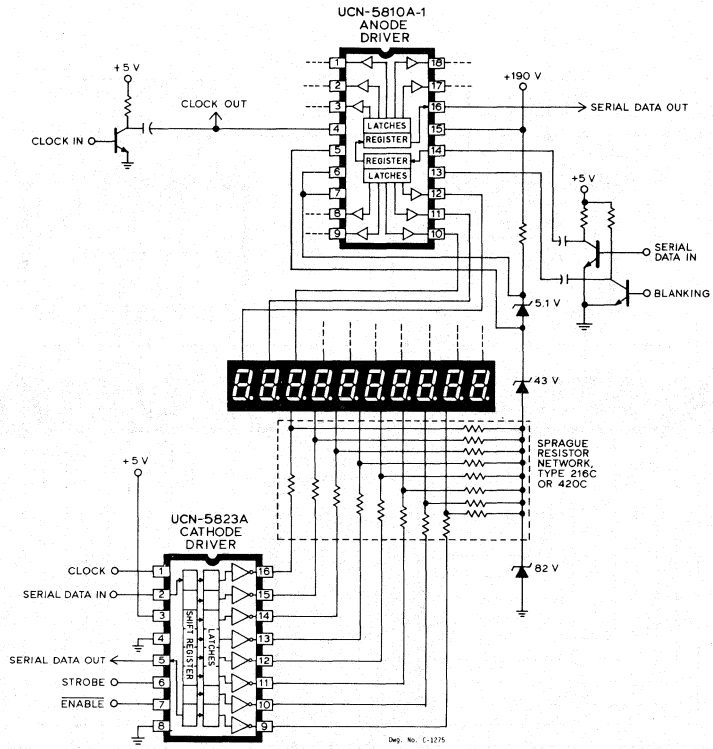
COMBINING the high-voltage UCN-5810A-1, UCN-5812A-1, or UCN-5818A-1 serial-input, latched source driver with the UCN-5823A serial-input, latched sink driver provides a simple way to drive multiplexed high-voltage planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 ..... 75 V
- UCN-5823A ..... 95 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 ..... −25 mA
- UCN-5823A ..... 350 mA



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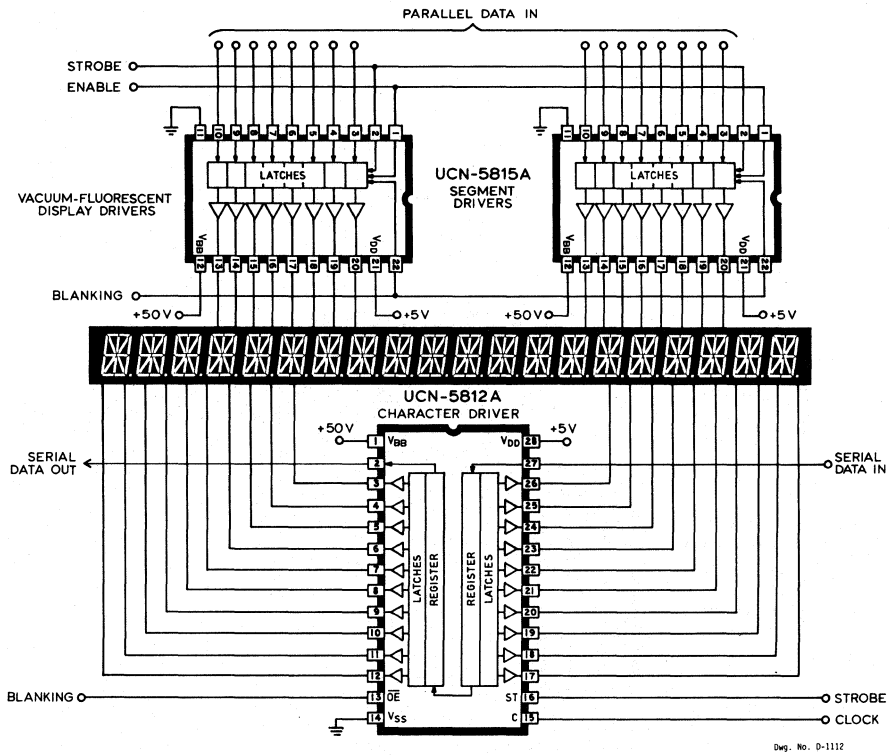
VACUUM-FLUORESCENT DISPLAY DRIVERS

THE UCN-5815A 8-bit, latched, source driver provides a practical means of driving the segments, dots (matrix panel), or bars of multiplexed high-voltage vacuum-fluorescent displays. The UCN-5810A (10-bit), UCN-5812A (20-bit), or UCN-5818A (32-bit) serial-input, latched source drivers are well-suited for use as character or digit drivers. The high-voltage versions (suffix -1) can also be used to drive the anodes of planar gas-discharge displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5810A, UCN-5812A, UCN-5818A ..... 55 V
- UCN-5810A-1, UCN-5812A-1, UCN-5818A-1 ..... 75 V

Logic Supply Voltage Range ..... 5.0 V to 12 V
Continuous Output Current ..... −25 mA



MULTIPLEXED INCANDESCENT LAMP DRIVERS

IN ORDER to obtain brightness equivalent to normal d-c operation, multiplexed incandescent displays must be operated at a voltage:

$$E_{MPX} = E_{DC}\sqrt{N}$$

where E_{MPX} = the recommended operating supply voltage,
E_{DC} = the rated d-c lamp voltage, and
N = the number of digits being multiplexed.

Multiplexed lamps also require isolation diodes to prevent sneak series/parallel paths to unaddressed elements.

Serial-input, latched source drivers provide simple, compact, and economical segment drivers for mutiplexed incandescent lamp applications. The UCN-5890A/B and UCN-5891A/B feature high-voltage, high-current (500 mA, peak) Darlington outputs. The UCN-5895A has saturated outputs for minimum voltage drop and will source up to 250 mA per driver. The drivers are supplied in an economical 16-pin "A" package or, for improved package power dissipation, a 22-pin "B" package. In either package style, UCN-5890, UCN-5891 and UCN-5895 are pin-compatible except for output ratings.

High-current UCN-5825B or UCN-5826B serial-input, latched sink drivers are used to drive the digits. Their high peak current rating is required to withstand the substantial inrush currents created by cold filaments. These BiMOS II power drivers also include internal thermal shutdown circuitry.

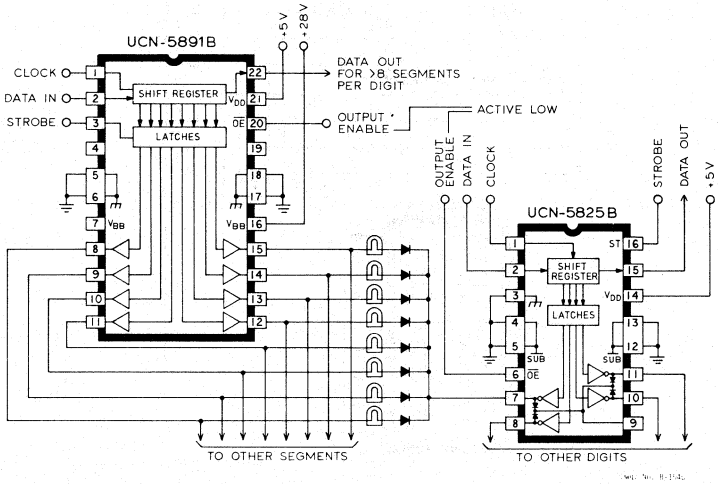
RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5825B ..... 55 V
- UCN-5826B ..... 75 V
- UCN-5890A/B ..... 75 V
- UCN-5891A/B ..... 45 V
- UCN-5895A ..... 45 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5825B ..... 1.75 A
- UCN-5826B ..... 1.75 A
- UCN-5890A/B ..... −350 mA
- UCN-5891A/B ..... −350 mA
- UCN-5895A ..... −120 mA

5



MULTIPLEXED LED DRIVERS

LATCHED source drivers are simple, compact, and economical segment drivers for multiplexed LED and incandescent lamp applications. The UCN-5895A features saturated outputs for minimum voltage drop. It sources a minimum of 120 mA per driver. The source driver is supplied in an economical 16-pin 'A' package.

A typical common-cathode LED display driver application is shown below. The high-current UCN-5821A, a latched sink driver, is used to drive the digits. Common-anode LED displays would require the use of the UCN-5891A source driver and UCN-5821A sink driver.

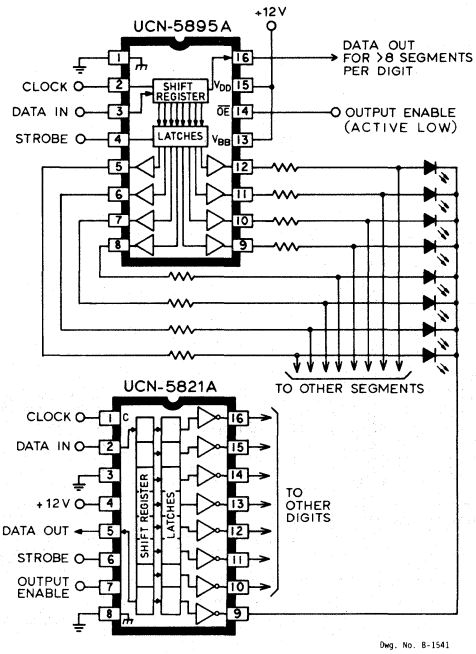
In order to obtain sufficient brightness, multiplexed LED displays must typically be operated at greatly increased current. Appropriate current limiting is required.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage
- UCN-5821A ..... 45 V
- UCN-5890A/B ..... 75 V
- UCN-5891A/B ..... 45 V
- UCN-5895A ..... 45 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5821A ..... 350 mA
- UCN-5890A/B ..... −350 mA
- UCN-5891A/B ..... −350 mA
- UCN-5895A ..... −120 mA



UNIPOLAR MOTOR DRIVERS

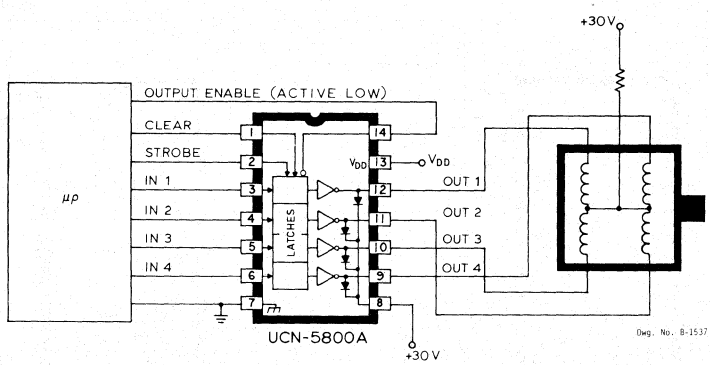
DRIVING unipolar motors is but one of the many successful applications for the UCN-5800A, UCN-5801A, UCN-5813B, and UCN-5814B BiMOS II latched sink drivers. The UCN-5801A is an eight-channel driver. The rest are four-channel drivers. The UCN-5814B includes CHIP ENABLE and CLEAR functions. Its larger 22-lead dual in-line package also allows increased package power dissipation without the use of an external heat sink. All devices contain CMOS data latches, CMOS control circuitry, and high-voltage, high-current bipolar Darlington outputs. Internal transient-protection diodes for use with inductive loads are included with all devices.

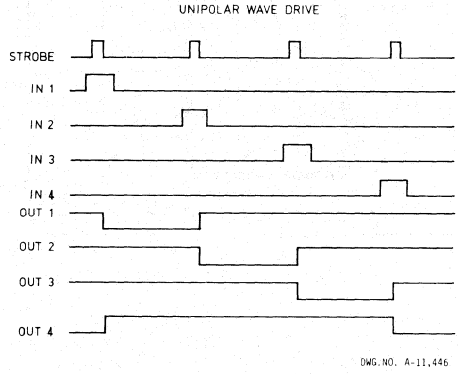
RECOMMENDED MAX. OPERATING CONDITIONS

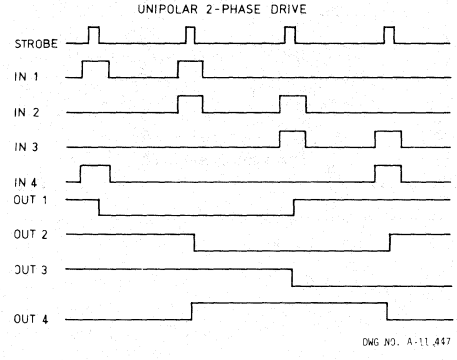
Output Voltage (Inductive Load)
- UCN-5800A, UCN-5801A, UCN-5813B, UCN-5814B ..... 35 V
- UCN-5813B-1, UCN-5814B-1 ..... 50 V

Logic Supply Voltage Range ..... 5.0 V to 12 V

Continuous Output Current
- UCN-5800A ..... 350 mA
- UCN-5801A ..... 350 mA
- UCN-5813B/B-1 ..... 1.5 A
- UCN-5814B/B-1 ..... 1.5 A







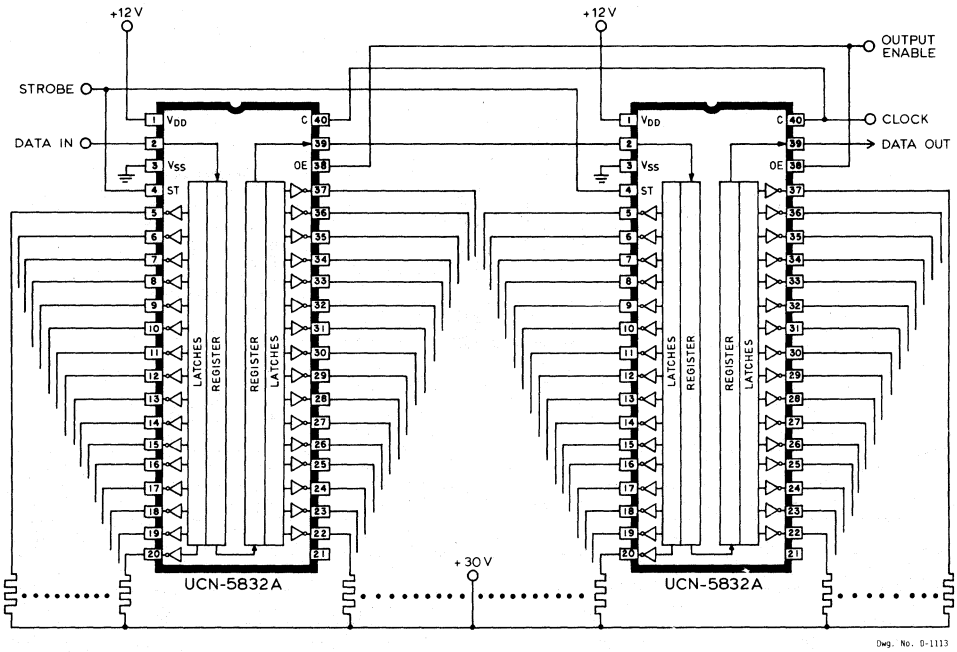
THERMAL PRINTHEAD DRIVER

DESIGNED primarily for use with thermal printheads, the UCN-5832A is optimized for low output-saturation voltage and high-speed operation. Each device has 32 bipolar, open-collector saturated outputs, a CMOS data latch for each driver, a 32-bit CMOS shift register, and CMOS control circuitry. A CMOS serial data output allows these devices to be cascaded in applications requiring more than 32 bits.

The UCN-5832A is supplied in a 40-pin DIP with 0.600" row spacing. Under normal conditions, all outputs will sustain 100 mA continuously without derating. They can also be supplied in unpackaged chip form or in a leaded chip carrier.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . . 40 V
Logic Supply Voltage Range . . . . . 5.0 V to 12 V
Continuous Output Current . . . . . 100 mA



IMPACT PRINT-HAMMER DRIVERS

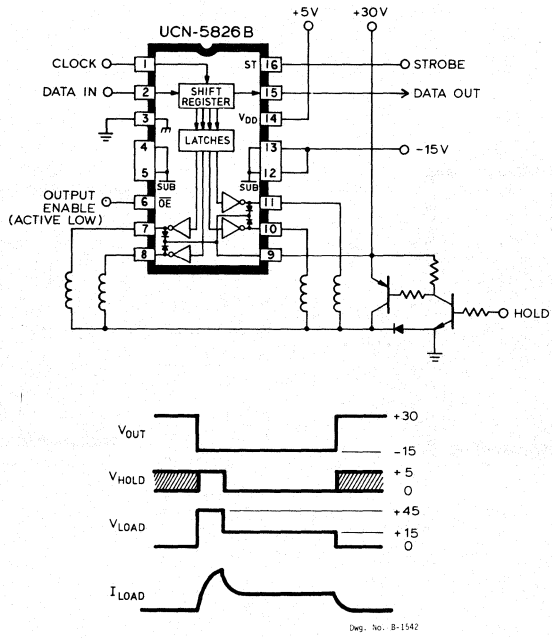
THE UCN-5825B and UCN-5826B 4-bit shift register/latched drivers are specifically designed for use with high-current inductive loads such as impact printers, solenoid, relays, and stepper motors. A CMOS serial data output allows cascading drivers where more than 4 bits is required. Except for output-voltage ratings, the two drivers are identical.

A bilevel current driver is shown. This application takes advantage of the split supply capability of the device. A relatively high turn-on current provides for high-speed operation and overcomes the inertia of a heavy solenoid or relay armature. The reduced holding current generates minimum heat and allows for improved power supply efficiency.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (Inductive Load)
- UCN-5825B ..... 35 V
- UCN-5826B ..... 60 V

Logic Supply Voltage Range ..... 5.0 V to 12 V
Continuous Output Current ..... 1.75 A



RELAY AND SOLENOID DRIVERS

BiMOS II DRIVERS provide an interface flexibility beyond the reach of standard logic buffers and power-driver arrays. Drivers with internal transient-suppression diodes are ideal for use with relay and solenoid loads.

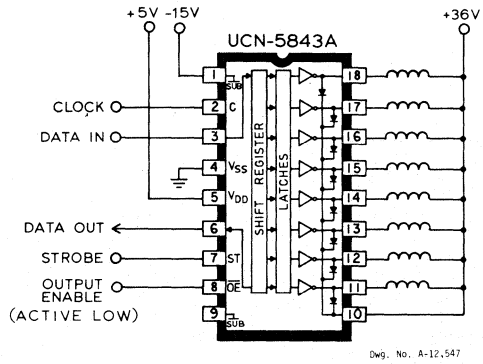
Series UCN-5840A sink drivers feature isolated logic and power grounds that allow split-supply operation or isolated grounds for reduction of transients and noise currents on common logic/load ground lines. The UCN-5890A and UCN-5890B source drivers require load supply voltages of at least 20 V. For lower-voltage operation, the UCN-5891A or UCN-5891B is recommended.

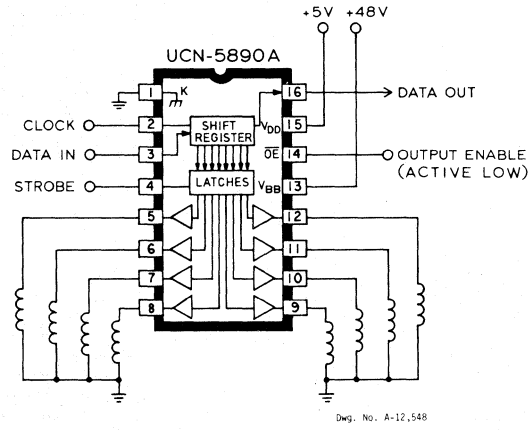
The serial DATA OUTPUT allows cascading for interface applications requiring additional drive lines. The OUTPUT ENABLE can also provide a CHIP ENABLE function that uses a minimum number of drive lines to control output from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (Inductive Load)
- UCN-5841A . . . . . 35 V
- UCN-5842A . . . . . 50 V
- UCN-5843A . . . . . 60 V
- UCN-5890A/B . . . . . 50 V
- UCN-5891A/B . . . . . 35 V

Logic Supply Voltage Range . . . . . 5.0 V to 12 V
Continuous Output Current . . . . . 350 mA



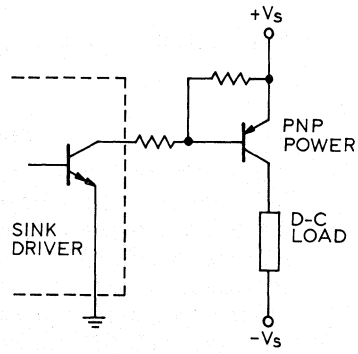


MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

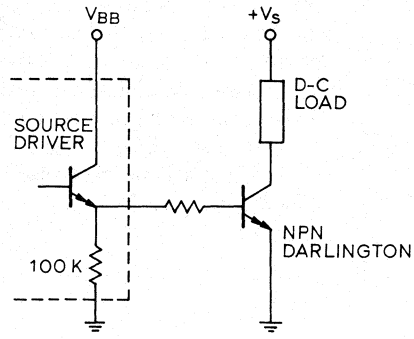
SPRAGUE BiMOS II power drivers can also be used as multi-channel pre-drivers for discrete high-current semiconductors, reducing the need for many discrete components. BiMOS II sink drivers provide enough switching current to the bases of discrete PNP power transistors for load currents of up to 20 A. Higher load currents can be obtained by using power Darlington devices. BiMOS II source drivers may require discrete Darlington power drivers for significant load currents, but have the advantage of allowing rather wide load-voltage swings.

Higher voltage requirements can be satisfied with discrete semiconductors or with the BiMOS III devices described below.

For a-c loads, source drivers can be used to provide gate current (with appropriate current limiting) to a power SCR or triac. This scheme can provide an economical approach to many applications such as driving incandescent lamps or a-c motors with current levels of up to 20 A.



Dwg. No. A-11,744A



Dwg. No. A-11,745A

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BiMOS ICs FOR ELECTROLUMINESCENT DISPLAYS

INTRODUCTION

Sprague Electric Company has introduced a new set of 32-channel EL driver chips that utilize the patented BiMOS process. BiMOS incorporates CMOS and high-voltage bipolar devices on the same junction-isolated substrate. Among the advantages of BiMOS technology are microprocessor compatability, low-power logic with superior noise immunity and supply voltage range, high-current bipolar output capability, and space-saving integration with its corresponding component-count reduction. A brief description of the BiMOS process and the ac TFEL drive scheme is followed by an analysis of the design and performance of the row and column driver chips, UCN-5851/52 and UCN-5853/54, respectively. The row driver chip incorporates a 32-bit shift register with OUTPUT ENABLE and STROBE together with 32 high-voltage open-drain DMOS transistors, each capable of withstanding 280 V and sinking 120 mA. The column driver chip is composed of a 32-bit shift register, 32-bit latch, OUTPUT ENABLE circuitry and 32 source-sink outputs rated at 80 V and ±20 mA. Each chip is pin-compatible with existing 32-channel EL drivers, and is available with clockwise or counter-clockwise output sequencing to facilitate layout of printed circuit boards.

THE EL SYSTEM

The electroluminescent display is a matrix of pixels, usually square, formed by the intersections of row and column electrodes that are bonded to the back and front, respectively, of the insulated active layer. The active region consists of an electroluminescent layer (ZnS doped with Mg) electrically isolated on both sides by an oxide dielectric. The intersection points of the row and column electrodes form capacitors that, when charged beyond a certain threshold voltage, provide sufficient electric field for photonic emission in the luminescent layer. Although the brightness vs. applied waveform characteristics of these pixel-capacitors are not fully understood, present refresh drive techniques produce a display with high readability, that is, good contrast under a variety of light conditions and an extremely wide viewing angle.

The threshold voltage for light emission is reached by driving the rows negative (− 140 V) and the columns positive (+ 40 V to + 80 V) relative to ground, resulting in a pixel voltage which equals the sum of both driving potentials. Individual pixel control is accomplished by selecting the rows one at a time and pulling high only those columns which correspond to ON pixels. (Figure 1).

After each complete scan, the entire display is refreshed by pulling all rows up to a high positive voltage through the row driver clamp diodes. This action reverses the applied pixel field, causing an additional light pulse and supplying the necessary bipolar drive waveform. The entire display is strobed about 60 times a second, resulting in a flicker-free image. The typical display size of 256 rows by 512 columns provides reasonable graphics capability and can display 25 lines of 80 characters each.

PROCESS TECHNOLOGY

The UCN-5851/4 EL driver chip set is fabricated using Sprague's highly adaptive BiMOS II process. Through this fusion of CMOS, bipolar and high-voltage DMOS technologies, Sprague enables the user to link microprocessors with high-voltage, high-current, and high-speed peripheral devices. The use of epitaxy permits the incorporation of high-performance, high-voltage bipolar devices while also maintaining controllable MOS thresholds. The up-down isolation that forms the device tubs permits the use of resurf field control, yielding N-channel DMOS devices that break down above 250 V. The up-down technique also reduces chip area by minimizing isolation-wall side diffusion.

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EL BLOCK DIAGRAM

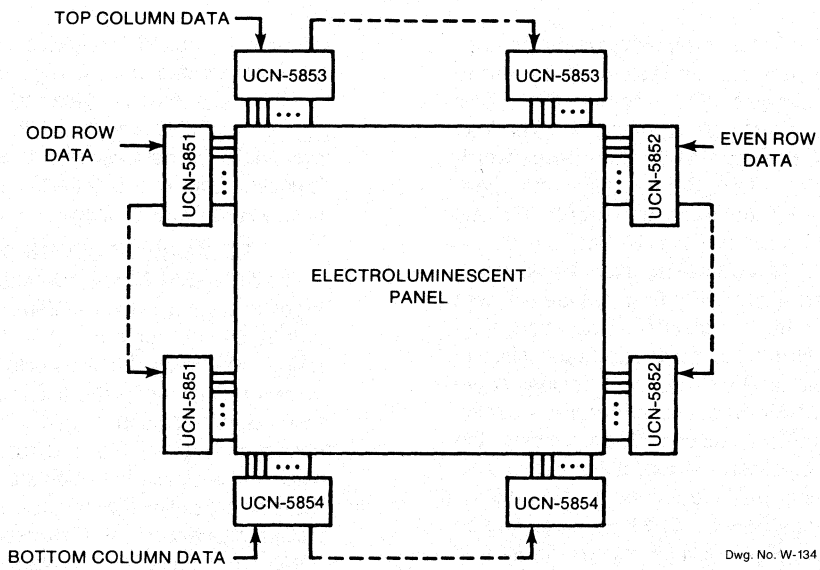
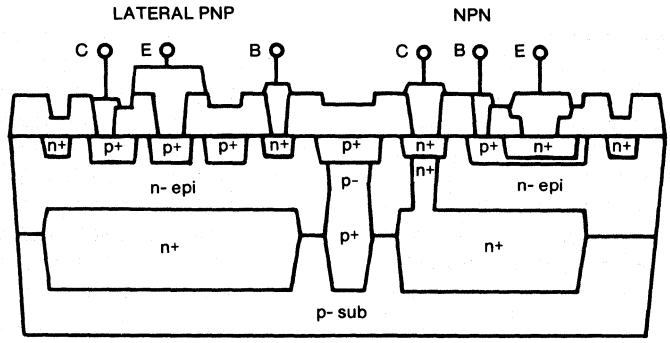


FIGURE 1

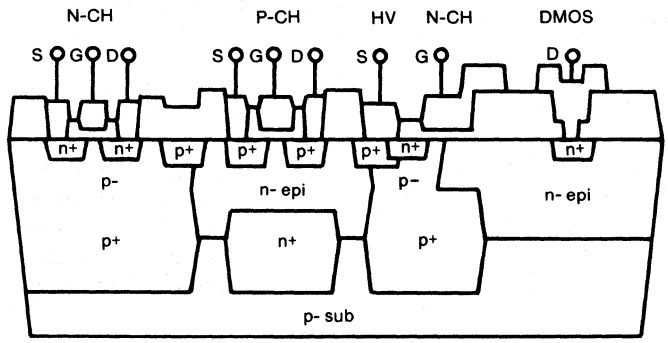
BIPOLAR PROCESS CROSS-SECTION



Dwg. No. W-135

FIGURE 2

MOS PROCESS CROSS-SECTION



Dwg. No. W-136

FIGURE 3

Figures 2 and 3 show process cross-sections for BiMOS II. The devices available are low-voltage PMOS, low-voltage NMOS, lateral PNP, vertical NPN and N-channel DMOS transistors. The low-voltage NMOS devices are built in the p-well, which also serves as the DMOS gate region and upper isolation. The P+ buried layer beneath the low-voltage NMOS prevents parasitic CMOS latch-up, and also serves as the lower isolation. The low-voltage PMOS and lateral PNP transistors are built with the same P+ diffusion, which is suitably controlled to provide the NPN base regions and low-resistivity diffused resistors. The shallow N+ regions serve as low-voltage NMOS sources and drains, and also as the NPN emitter diffusions. Also available to the designer are polysilicon resistors at 2kΩ per square.

The voltage capabilities of the NPN and PNP transistors range from 5 V to 100 V, depending on layout spacings. Higher voltage devices require N+ guard rings as shown in the bipolar cross-section. The high-voltage PNP requires field plating for reliability considerations. The high-voltage N-channel DMOS, field plated over drain and body regions, may be constructed to yield breakdowns from 100 V to over 300 V. Test devices are still being characterized to determine the effects of the P+ buried layer resurf shelf on breakdown voltage.

ROW DRIVER BLOCK DIAGRAM

The UCN-5851/52 row driver function is shown in the block diagram of Figure 4. The row driver consists of a 32-bit shift register with OUTPUT ENABLE and STROBE lines which can be used to turn all 32 outputs ON or OFF. Data enters the shift register on the high-to-low clock transition, a logic "1" input causing the corresponding DMOS output to pull low. Typically, a single "1" is clocked through the shift register and the rows are pulled low one at a time using OUTPUT ENABLE. After a complete scan the substrate common (GND) pin is pulled high, forward-biasing the body-

ROW DRIVER BLOCK DIAGRAM

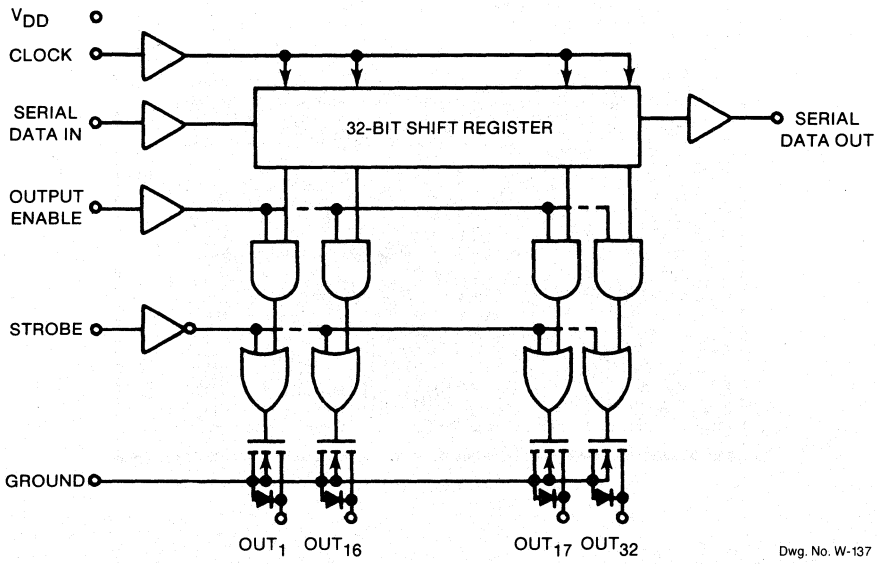


FIGURE 4

drain diodes present in each DMOS structure, and pulling all outputs high.

Since the DMOS gates switch between ground and V_{DD}, output current capability is strongly affected by the logic supply voltage. At V_{DD}, = 5 V, the output ON resistance is about 300Ω, decreasing to approximately 100Ω at V_{DD} = 12 V. A serial DATA OUT pin is provided for cascading the shift register.

COLUMN DRIVER BLOCK DIAGRAM

The block diagram of Figure 5 shows the UCN-5853/54 column driver. Like the row driver, the device contains a 32-bit shift register with a serial output for cascading additional drivers. However, data enters the shift register on the low-to-high clock transition, with a data "1" causing the corresponding output to turn ON. In this state the output sources

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COLUMN DRIVER BLOCK DIAGRAM

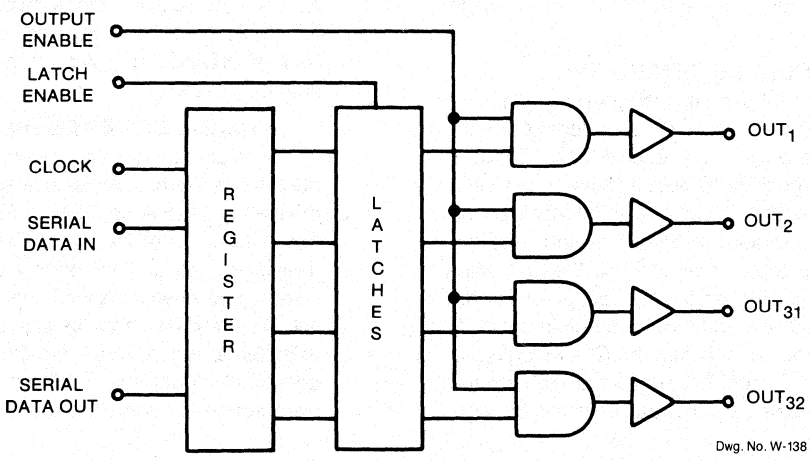


FIGURE 5

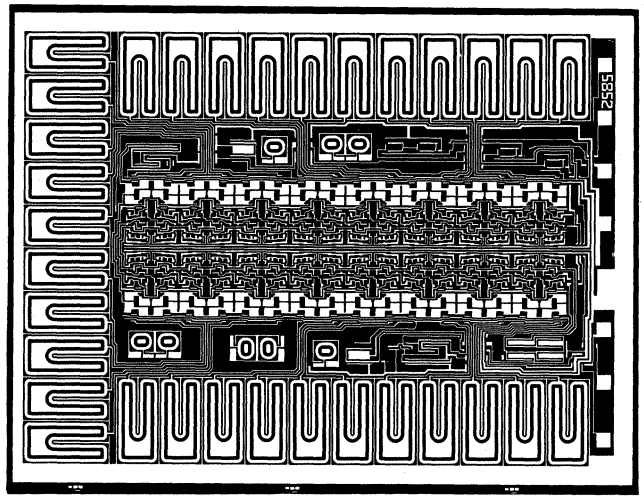


FIGURE 6

current from the high-voltage Darlington drive, causing an ON pixel. The column driver also contains a 32-bit latch that serves to hold currently displayed information while a new set of data is being clocked through the shift register. The transfer of data from shift register to latch is controlled by the LATCH ENABLE input. The shift register data present at the negative-going edge of the LATCH ENABLE signal is retained in the latch. An OUTPUT ENABLE "0" causes all outputs to pull low regardless of the data present in the latch. The ground-clamp diode shown is the inherent N-DMOS body/drain diode, while the supply rail diode is an added diffusion in the high-voltage pocket.

ROW DRIVER PHOTO

Figure 6 shows the row driver layout in silicon form. The 32-bit shift register and gating logic are contained in the center, and the large NMOS and PMOS transistors, which drive the output gates, can be seen on either side of the CMOS array. The 32 high-voltage N-channel outputs are lateral open-drain DMOS devices. These occupy three sides of the chip, while the remaining end is used for logic and ground pads. All front-end buffers and input protection are contained in the spaces between the CMOS logic and DMOS outputs. In addition, eight small high-voltage test devices can be seen in areas adjoining the logic buffers.

COLUMN DRIVER PHOTO

The silicon implementation of the column driver chip can be seen in Figure 7. As in the row driver, the center area contains the CMOS logic array, which is comprised of a 32-bit shift register, 32-bit latch, gating logic, and inverters to drive the source and sink sections of the output cells. All logic and supply pads are on one end of the chip flanked by their resective buffers and input protection. The other three sides of the chip contain the 32 sink-source outputs, 10 of which were relocated to the chip end to facilitate bonding. The Darlington source drivers can be seen just inside the high-voltage supply metal bus, while the output pads and lateral high-voltage N-channel DMOS sink transistors lie outside on the periphery of the chip.

COLUMN DRIVER OUTPUT SECTION

The column driver output section is shown in Figure 8. It consists of a bipolar level shift, bipolar source drive and lateral N-channel DMOS sink transistor. The level shift is driven by the CMOS logic through a resistor divider, which minimizes the static logic current (I_{DD}) when the source input is high. The level shift current, drawn from the high-voltage supply rail, is limited to about 60 μA per channel. This yields about 2.0 mA per chip, a 70 percent improvement over first generation EL column drivers. The level

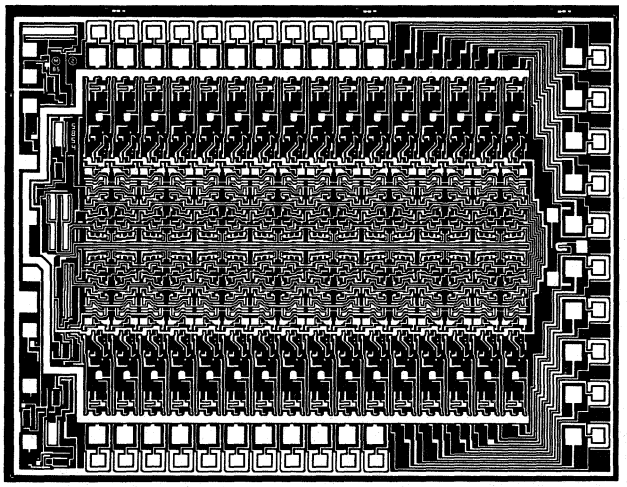


FIGURE 7

shift drives a high-voltage lateral PNP which in turn drives the Darlington output. The gate of the DMOS sink transistor is driven by the CMOS logic, out-of-phase with the source input.

The circuit configuration ensures minimum crossover current, because the DMOS transistor must turn OFF the source drive before any current may be pulled from the output. This feature also bypasses any turn-off delay associated with the slow lateral PNP transistor, enabling the output structure to switch at speeds greater than 400 kHz. The series diode does not add appreciably to the DMOS saturation voltage.

5

COLUMN DRIVER LEVEL SHIFT AND OUTPUT

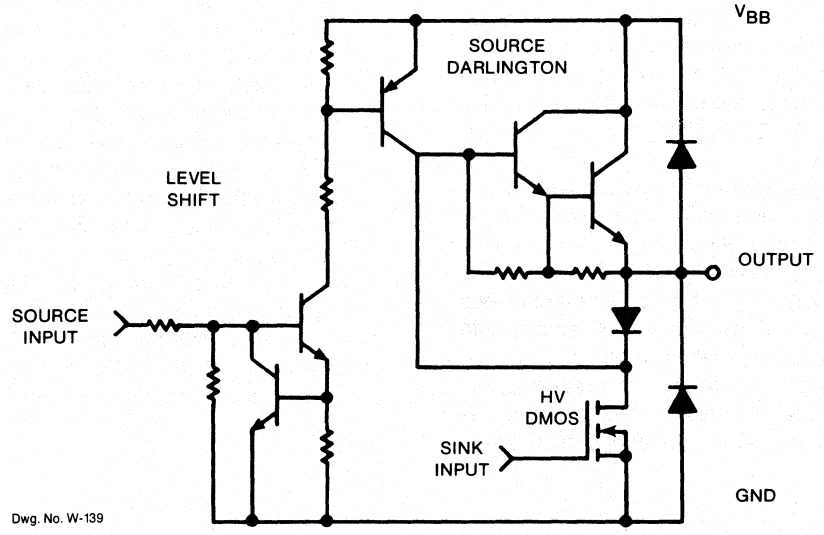


FIGURE 8

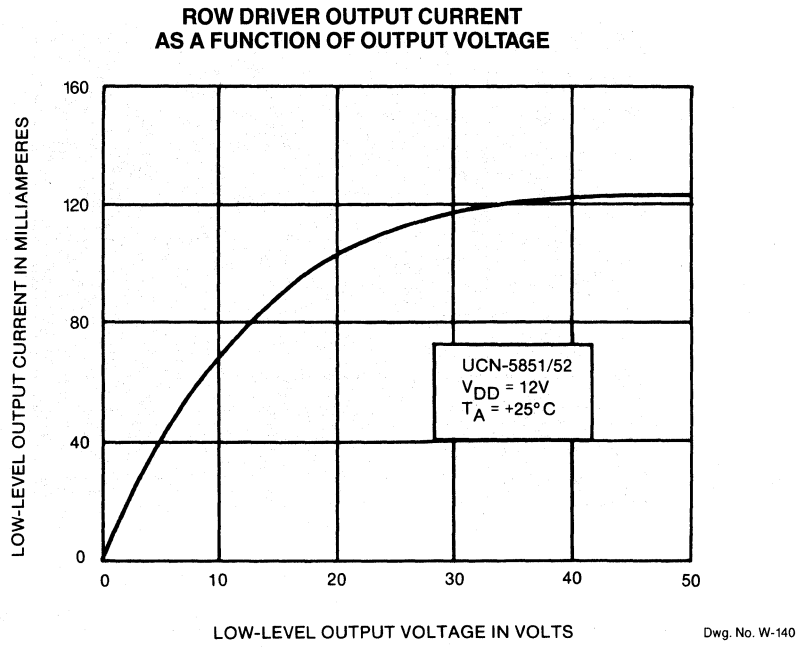


FIGURE 9

ROW DRIVER RESULTS

The current and voltage characteristics of the high-voltage open-drain DMOS device are shown in the graph of Figure 9. At +25°C, the typical ON resistance is 100Ω and the saturation current (taken at V_{DS} = 30 V) is about 120 mA, a 50 percent improvement over first generation devices. The saturation current varies with temperature from 87 mA at +125°C to 132mA at 0°C. At a sink current of 50mA, the voltage drop is 6.5 V at +25°C, increasing to 13.2 V at +125°C, yielding a temperature coefficient of 67mV/°C.

In the OFF state, leakage is typically below 0.1 μA and is constant until avalanche breakdown is encountered at about 280 V. The device can switch 250 V and 120 mA. No latching will occur, even if the load is decreased to 0Ω raising the instantaneous power dissipation to over 30 W. This square safe operating area enhances the reliability of the device while increasing the scope of possible applications. The switching speed, though probably limited by the CMOS output inverter current capability, exceeds 1MHz. The body-drain diode exhibits a voltage drop of 1.15 V at 100mA. Logic power dissipation is 0.1mW at f_{CLK} = 10kHz, increasing to 10mW at a 1MHz clock rate.

COLUMN DRIVER RESULTS

The capability of the column driver is determined by the sink and source current capability, and by the speed and efficiency of the push-pull output stage. The graph in Figure 10 illustrates the current capability of the bipolar Darlington source driver. The saturation voltage in the linear region, measuring 2.5 V at 20mA, is better than can be economically achieved using a MOS source device. This voltage is important because it represents power wasted in the column driver outputs each time a pixel is turned ON. A 1 V difference in source saturation voltage may lead to as much as 250mW of unnecessary power dissipation. At 20mA, the source saturation voltage varies from 2.05 V at 0°C to 1.9 V at +125°C, giving a temperature coefficient of −1.2m V/°C.

COLUMN DRIVER SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

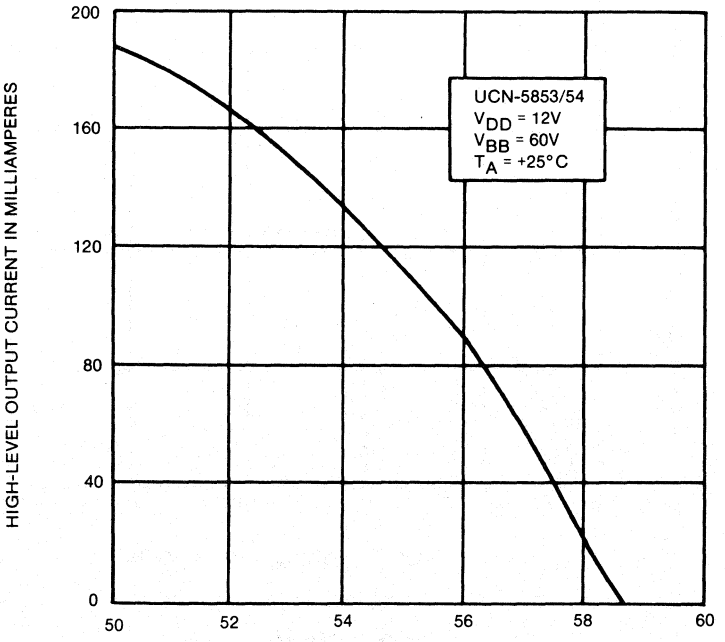


FIGURE 10

The voltage/current characteristic of the N-channel DMOS sink device is shown in Figure 11. At +25°C, the ON resistance is 305Ω. The saturation current is 41mA, measured at 25 V. At 20mA, V_{DS} varies from 6.6 V at 0°C to 8.2 V at +125°C, yielding a 12.8mV/°C temperature coefficient. The body/drain diode in the DMOS device shows a forward voltage drop of 1.18 V at 20mA (+25°C). The V_{BB} rail clamp diode drops 0.91 V at 20mA and +25°C. The actual breakdown voltage from the V_{BB} rail to ground exceeds 90 V.

The output switching speed exceeds 400kHz at 80 V with a 30pF load to ground. Investigation is currently underway to determine the output power dissipation due to switching losses and capacitive charging, which varies with output switching speed and duty cycle. Static leakage is very low during both high and low output states. The logic dissipation is about 0.1mW at f_{CLK} = 10kHz under typical conditions, increasing to 8.5mW at a 1 MHz clock rate.

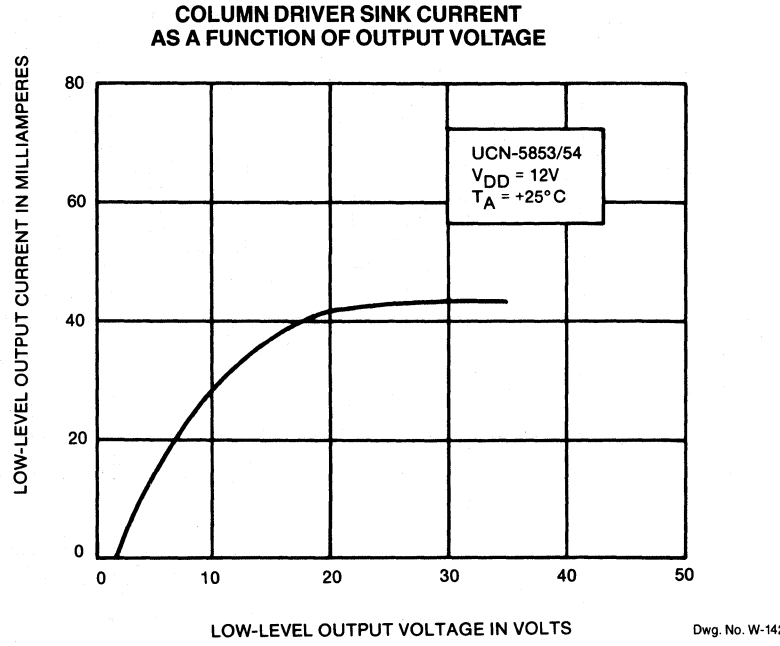


FIGURE 11

CONCLUSION

The Sprague UCN-5851/52 and UCN-5853/54 EL driver chip set offers increased performance and reliability, meeting the increasing demands of the display industry. Higher voltage column drivers mean increased display brightness and contrast, while giving the assurance of a larger safety margin in operation. Greater current capability minimizes pixel brightness variations, which can be caused by varying line resistances and changing electrode capacitances. The higher current and high speed also permit the use of larger panels as user needs increase. The ruggedness of these drivers is enhanced by the wide current and voltage margins, as well as by the square safe operating area of the sink devices, and the high-current clamp diodes. Both parts are available in 40-pin DIPs (plastic and cer-DIP), 44-pin plastic leadless chip carriers, 44-pin hermetic cer-quad packages, and in chip form for TAB installation.

References

Texas Instruments Display Driver Handbook, 1983.

Driving Large Matrix AC Thin-Film Electroluminescent Displays, by Greg Draper.

Thin-Film Electroluminescent Displays, by Christopher N. King, SID Seminar Digest, April-May 1985.

BiMOS: A MERGED TECHNOLOGY FOR CUSTOM AND SEMI-STANDARD POWER INTERFACE ICs

BiMOS power interface continues to advance its technological capability, expand to new applications and users, afford a growing product selection, provide cost-reduction solutions, and offer improved reliability and increased alternate sourcing. However, with the recent focus on other merged technologies, many have overlooked BiMOS. This paper highlights limits, relative merits, and newer developments in BiMOS power integrated circuits.

INTRODUCTION

Smart power interface ICs originated within Sprague Electric in 1977, and became a quiet revolution with an intuitive, innovative shaping of technology to satisfy a need. These power integrated circuits began with a creative evolution of power interface circuitry dating to 1970. The merging of bipolar (Bi) with CMOS (MOS) logic was driven by an exploding need for power interface compatible with microprocessors. Initially, it combined a quad "D" latch with four high-current/high-voltage Darlington outputs. Although not normally attempted, both a *new product* and a *new process* were *concurrently* and *successfully attempted.* The breakthrough spawned semi-standard BiMOS power interface.

Semi-standard power interface ICs were the response to applications-driven or market-driven developments that propelled BiMOS as a very important technology. This market (applications) driven strategy produced a variety of products targeted, increasingly, toward specific applications and multiple customer use. Expectations are for this to continue. However, other forces (particularly the focus on semi-custom ICs and the ability to simplify customizing) are stimulating an increased *diversity.* With a mature process, a CAD library and tools, *diversity* means keen interest in and heightened demand for custom BiMOS power integrated circuits.

Table 1 — BiMOS Evolution

BiMOS	CMOS Logic			Bipolar Power			Relative Traits	
	Dimension	Logic	Speed	Outputs and Ratings			Advances	Merit/$
I	8 μN/10 μP	5-18 V	1 MHz	NPN/PNP	<100 V	>500 mA	Oldest	Good
II	8 μN/10 μP	5-15 V	5 MHz	NPN/PNP	<100 V	>2 A	Speed/Size	Lower
III	8 μN/12 μP	5-15 V	5 MHz	+ DMOS	>200 V	>100 mA	High Voltage	Modest
IV	5.5 μN/7 μP	5-7 V	5 MHz	All	<100 V	>2 A	Density/$	Lowest

DIVERSITY: DRIVING FORCE

Forces of diversity include systems manufacturers striving for new products rapidly tailored for specific applications, an acute awareness of semi-custom and custom ICs, increased semiconductor supplier use of CAD design and chip layout, automated processing, manufacturing, and testing of ICs, and (everywhere) swift, fierce international competition. All of these factors (and more) are stimulating new demands for a competitive advantage. They are accelerating the need for semi-standard (applications-driven) and custom smart power BiMOS ICs.

Aiding movement toward greater diversity are expanded product offerings, a large number of new users, ever-broadening applications, and recent technological developments. From inception in 1977, BiMOS has become a mature, high-volume technology that has advanced and diversified with later generations. Second generation BiMOS provides size and chip-cost reductions and greatly improved switching speeds. Another later generation (BiMOS IV) cut chip size even further to reduce cost per output. BiMOS III provides high-voltage outputs (150-200 V).

More recent circuits often include functions not originally used. Added to the bipolar power/CMOS logic basics are analog functions (control and amplifiers) and protective circuitry (thermal, over-current). This potential for diversity is also enhanced by possible combinations of bipolar (power or analog), CMOS logic, power (vertical) DMOS outputs, high-voltage (lateral) DMOS outputs, and improved protection diodes.

The potential for further diversity involves a better awareness of the technology and a determination of whether a circuit should be custom or semi-standard. Many new IC programs have begun as discussions of custom devices, only to evolve into non-proprietary semi-standard ICs as volume criteria, design funding and decision delays preclude exclusive use.

TECHNOLOGY CHARACTERISTICS

Over the past several years BiMOS has followed an Olympian path (faster, higher, farther) as developments in process technology, increases in voltage, current, and power, and many new circuit functions and applications have formed an explosive, accelerating force dubbed "smart power." From the original quad latch/driver IC rated at 50 V/500 mA per output, BiMOS has expanded to 32-bit drivers (64-bit in the offing), 200 V levels, 2 A/output, and a variety of shift registers, latches, random logic, protection diodes, and protective circuitry such as thermal shutdown. Logic (shift register) speeds have climbed to over 5 MHz (from 1 MHz, 5 V logic) as CMOS was shrunk to improve performance and reduce cost. The conservative approach to BiMOS has resulted in 3.5-4 A peak ratings for 2 A driver outputs, and, often, the option of voltage selections that exceed nominal ratings at very little additional cost.

The evolutionary changes in circuit capabilities and specifications are listed in Table 1. Early concerns included faster shift register speeds, smaller and lower cost chips, and high-reliability military packaging and screening. Subsequently, concerns for higher current and power, considerably higher voltages (>100V), smaller packages (now SMD versions), and more outputs per chip (serial-input ICs) spurred further variations of BiMOS. The characteristics of BiMOS I through IV offer a technology choice based upon system design requirements, although the first generation (BiMOS I) is no longer used for new designs. The second generation (BiMOS II) will be superseded, primarily, by the smaller BiMOS IV versions.

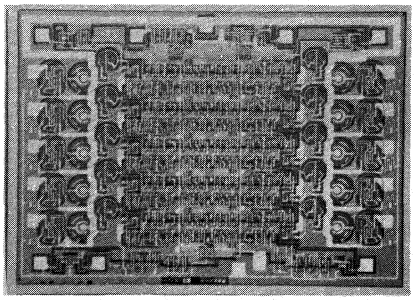


FIGURE 1
UCN-4810 10-Bit Driver — 60V, 50 mA
16050 sq. mils

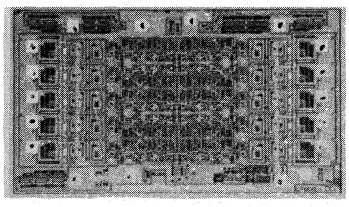


FIGURE 2
UCN-5810 10-Bit Driver — 60V, 50 mA
8885 sq. mils

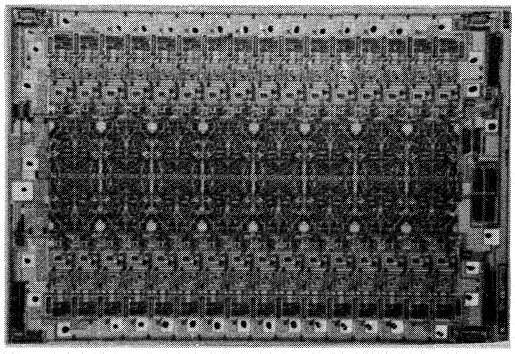


FIGURE 3
UCN-5818 32-Bit Driver — 60V, 50 mA
23495 sq. mils

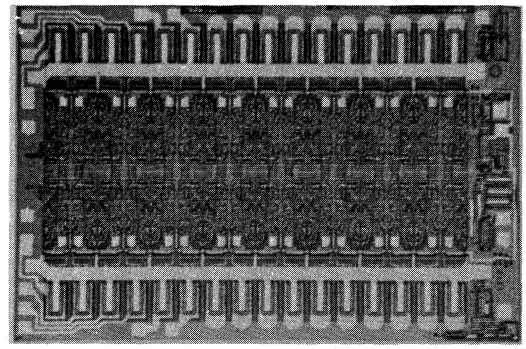


FIGURE 4
UCN-5832 32-Bit Driver — 40V, 150 mA
23250 sq. mils

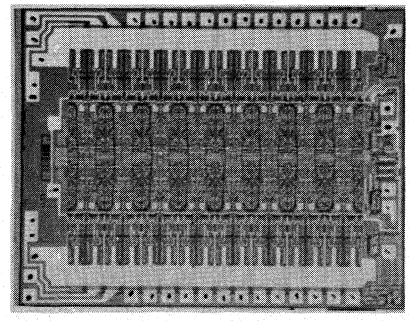


FIGURE 5
UCN-5833 32-Bit Driver — 40V, 100 mA
15873 sq. mils

5

All BiMOS versions now have metal-gate CMOS inputs; however, the use of silicon gate technology may further enhance BiMOS power interface. Current density requirements dictate use of heavy (thick) aluminum interconnect for the high-current circuitry, and the 25 kÅ metallization has complicated any early change to silicon gate CMOS. It should be noted that polysilicon is now used for high-value circuit resistors in a number of the present power integrated circuits, so a future conversion to silicon gate technology is anticipated. Also of concern is the increasing use of two-level metallization (now used for high-current bipolar power integrated circuits). As chip outputs increase in number and current, the two-level interconnect offers advantages of current density (per unit area) and positively affects both performance and cost.

EVOLUTION

An important comparison is shown in Figures 1 through 5. In Figure 1 is an early BiMOS interface IC, a 10-bit serial-to-parallel driver rated at 60V and 50 mA. In the second generation UCN-5810 (Figure 2), the chip area is reduced by *45 percent*, while logic speed

increased by about *500 percent*. The 32-bit UCN-5818 in Figure 3 (also BiMOS II), is only 46 percent larger than the chip in Figure 1, although it contains 32 rather than 10 outputs.

Another 32-bit BiMOS II power integrated circuit (UCN-5832, Figure 4) is approximately the same size, but contains 32 outputs each rated at 100 mA and 50 V. Compare this to a BiMOS IV version with similar ratings, the UCN-5833 shown in Figure 5. A BiMOS IV version of Figure 3 would be a chip with about the same dimensions as those of Figure 5.

The BiMOS evolution has produced much more complex power integrated circuits without increasing chip size. This increase in circuit density dramatically affects performance and cost while adding new prospects for single-chip interface ICs.

One BiMOS development is embodied in the larger, high-voltage UCN-5910 (not shown). This BiMOS III (150-200 V) 10-bit IC is a functional equivalent to Figures 1 and 2. The present high-voltage technology yields chips comparable in size to the original BiMOS ICs, although switching performance is far inferior to the BiMOS II and IV processes. The hybrid nature of the newer BiMOS, with its ability to provide high-voltage lateral DMOS, may allow shrinking of many future high-voltage smart power ICs, especially those with low to modest current outputs.

Another aspect of the evolution is illustrated by higher power ICs. The *original* BiMOS power integrated circuit was the UCN-4401, a quad latch/driver rated at 50 V (inductive, 35 V) and 500 mA per output. The much newer, high-power UCN-5826 is a four-bit serial-to-parallel IC with a 60 V (inductive) sustaining voltage rating and a conservative, continuous current rating of 2 A (peak, 3.5-4 A). Despite addition of a shift register, improvement of inductive voltage capability, and dramatically increased output current, the change in chip size was minimal (from 7200 to 19300 sq. mils). Future designs with bipolar outputs and two-level interconnect will further reduce the size of high-current chips and allow lower output ON impedance to minimize power dissipation. Merged chip designs, needing increased switching speed and improved safe operating area, will adopt increased use of high-current DMOS (vertical) outputs. BiMOS offers a mix-and-match technology that can combine vertical and lateral DMOS outputs with the older, proven bipolar types.

TECHNOLOGY COMPARISON

Distinguishing between competing power IC technologies is increasingly difficult, and especially so among the merged processes. BiMOS is based upon a bipolar process. Adding CMOS logic means additional process and masking steps beyond either linear bipolar or

Table 2 — Technology Comparison

	Output Characteristics			Logic Traits			Technological Merit		
Process	**Limits**	**Drive**	**Form**	**Density**	**Power**	**Speed**	**Complexity**	**Cost**	**Maturity**
Bipolar	8 A/60 V	High	PNP/NPN	Low	High	Slow	Low	Low	Oldest
I^2L	8 A/35 V	High	PNP/NPN	Medium	Modest	Modest	Low/Mild	Mid	Proven
BiMos	4 A/200 V	High	PNP/NPN	High	Very Low	Fast	High	High	Proven
C/VDMOS	2 A/60 V	Low	NMOS[1]	High	Very Low	Fast	High	High	Recent
C/LDMOS	0.5 A/300 V	Low	NMOS[2]	High	Very Low	Fast	High	High	Proven

NOTES:
1) Bootstrapping NMOS normally used for source outputs, although PNP can be implemented.
2) Bootstrapping required (charge-pump circuitry and emitter-follower scheme) for source outputs.
3) I^2L: Includes both single and double epitaxial process limits.
4) C/VDMOS = CMOS/Vertical DMOS
5) C/LDMOS = CMOS/Lateral (high-voltage) DMOS

I²L. Presently, BiMOS provides power and analog bipolar, CMOS logic (metal-gate, medium-density), high-voltage, medium-current lateral DMOS, high-current, medium-voltage vertical DMOS, improved (very low parasitic beta) flyback diodes, polysilicon or diffused resistors and protective functions:

Bipolar
- Power Outputs — NPN and PNP
- Analog Amplification and Control
- Diodes — Output Transient Protection

Merged Outputs
- P-Channel/NPN (Source)
- N-Channel/NPN (Sink)

MOS
- CMOS Logic (Analog Possible)
- Power Outputs — Vertical DMOS (N-Channel)
- High-Voltage Outputs — Lateral DMOS (NMOS)

Control/Protective
- Thermal Shutdown
- Over-Current
- Over-Voltage
- Power-On Reset

Passive Components
- Diffused Resistors 150 Ω /square
- Polysilicon Resistors — 2 kΩ/square

Compared to competing technologies, BiMOS offers a greater variety of output ratings and functions, speed and power advantages of CMOS logic, and competitive cost. It provides single-chip, complex, multiple output Smart Power ICs, proven military reliability, and a maturity unequaled by other alternatives.

The evolution of BiMOS semi-standard power interface started with a user need to combine a power array (bipolar) with an octal latch (CMOS) and continues to provide performance, size/space, reliability, and cost advantages. (One 32-bit IC approaches five cents an output.) Although these semi-standard, applications oriented power integrated circuits will endure, another potential and largely overlooked market exists in *custom* BiMOS power. With the tools listed previously, user/vendor partnerships can create new and superior products for nearly any system.

Highlighting the possibilities are recent activities with innovative leaders in:

Appliances
ATE/Instrumentation
Automotive
Brushless DC Motors
Flat Panel Displays
Military Avionics
Printers (Impact and Impactless)
Telecommunications

Many of these discussions have focused on design and development of generic or semi-standard BiMOS ICs. However, recent dialogue has, increasingly, been oriented toward custom programs. A particular system design might be optimized with a different combination or number of the ingredients listed earlier. Examples include a 24-bit driver, a 115 V line-operated brushless dc motor circuit, special ICs for telecom, MUX driver ICs for automotive, and CMOS logic readback for ATE and instrumentation.

CUSTOM BiMOS

Originally developed for specific applications and functions, BiMOS power integrated circuit technology is now a ready, mature, and cost-effective approach for *custom* programs. It must be noted that Sprague does *not* envision a workable semi-custom potential for BiMOS power ICs. The variables of voltage, current, logic, output lines, protection, packaging and testing tend to overwhelm any prospect of creating semi-custom chips. The established direction toward semi-standard ICs will continue but many new activities will branch into custom ICs.

The creation of a custom BiMOS power integrated circuit, optimized for a specific system, is quite straightforward and uses a proven CAD cellular library of functions (latch, S/R, thermal shutdown) and components (bipolar power cells, PNPs) to assemble a new circuit. However, despite this cellular design technique, new BiMOS power integrated circuits are much like other custom designs and take much longer than any conventional semi-custom design. The disadvantages of design funding and longer program schedules may be

balanced by the cost and performance advantages of an optimized, volume design. With improvements in logistics, the elapsed time for a custom BiMOS design is expected to diminish, and allow an early strategic advantage to the swift and sure.

APPLICATIONS EXAMPLES

As mentioned previously, opportunities abound for both custom and semi-standard BiMOS. Certain types of systems have a greater leverage factor (many power integrated circuits per design) than others. Impact and thermal printers, flat panel displays, and ATE (automated test equipment) represent types of uses with a high content of Smart Power ICs. To illustrate, typical printer examples are shown in Figures 6 and 7.

An example of a high-efficiency impact printer, using a split supply (bilevel current drive) is shown in Figure 6. Previously these printers have used vast quantities of TO-220 discretes. With this BiMOS design, both component count and cost are greatly reduced.

Another example is thermal printer drive. High-speed, high-resolution systems require a great many drive lines, as do flat panel, matrix displays. Space, package size, cost per output, and switching speed are important. Fig ure 7 is an example of a smart 32-bit driver (used both in chip and PLCC form) to meet space/resolution constraints. Newer BiMOS power integrated circuits dissipate considerable power, and high pin-count power packages are needed as output lines and currents escalate.

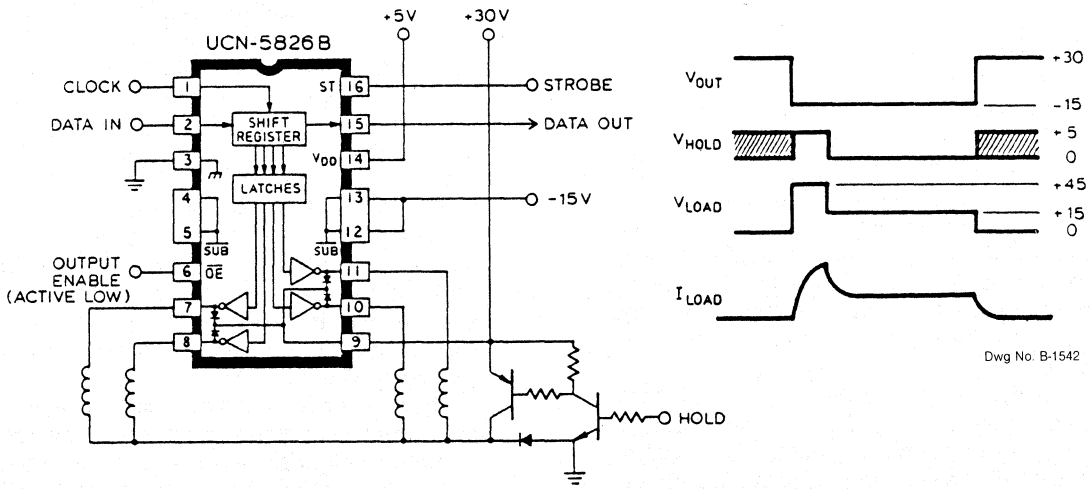


FIGURE 6
Serial-Input, High-Power (2 A) Impact Printer Driver

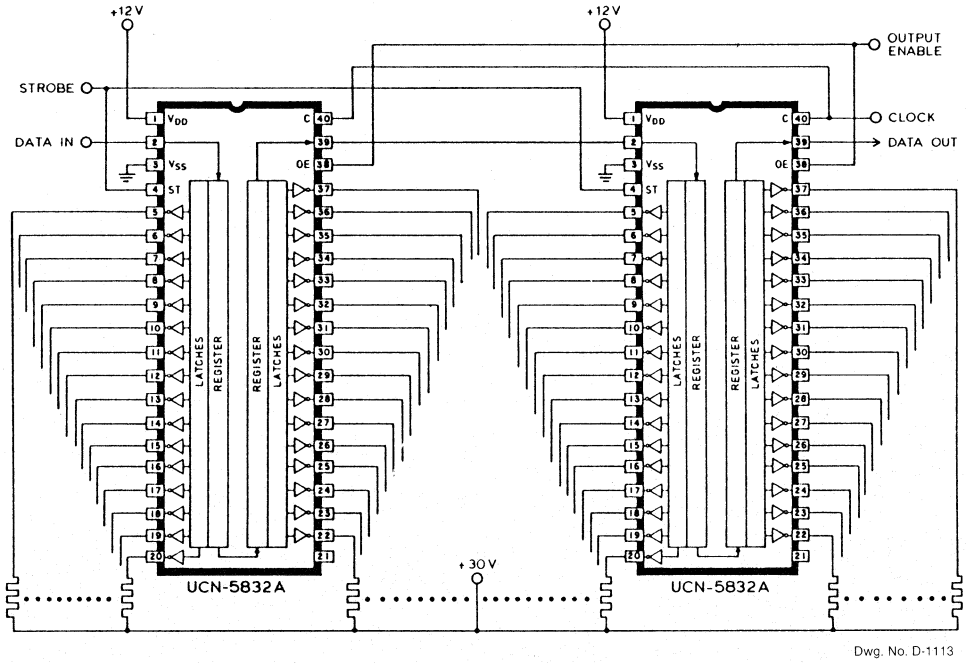


FIGURE 7
Serial-Input, 32-Bit Thermal Printhead Driver

CONCLUSION

Opportunities for custom BiMOS power interface are increasing. Users can take advantage of several years of evolution of design and process; a CAD library, automated testing, proven reliability, and cost and size reductions all gained through production experience. Technologically, BiMOS power affords an array of unsurpassed capabilities but lacks exploitation in custom ICs. Systems requiring many output lines are the most natural targets, although use is more limited by imagination than any other factor.

The increasing need for innovative products, rapidly executed and offering strategic advantages, focuses on greater diversity for system, function, and components. Key aspects of the increased use of custom BiMOS power ICs are maturity, technological advantages, innovation, swift execution, and diversity. Change and progress are relentless. BiMOS power is the ready-made technology for many of today's custom power ICs.

NOTES

NOTES

SECTION 6—MILITARY DEVICES

*QPL version of ULS-2003H-883.

6

SELECTION GUIDE TO HIGH-VOLTAGE/HIGH-CURRENT POWER DRIVERS TO MIL-STD-883

In order of (1) output current rating, (2) output voltage rating, and (3) number of drivers

Outputs*			Features					
mA	V	#	Serial Input	Latched Drivers	Diode Clamp	Sat. Out.	Internal Protect.	Part Number
SINK DRIVERS								
100	20	8	—	—	—	X	—	UDS-2595H/R ††
250	40	4	—	—	X	X	—	Series UHD-400
250	70	4	—	—	X	X	—	Series UHD-400-1
250	100	4	—	—	X	X	—	Series UHD-500
300	80	2	—	—	—	X	—	Series UDS-3610H†
300	80	2	—	—	—	X	—	Series UDS-5710H†
300	80	4	—	—	X	X	—	Series UDS-5700H
300	120	4	—		PIN Diode Driver		—	UDS-5791H
350	50	4	—	X	X	—	—	UCS-4801H
350	50	4	—	X	X	—	—	UCS-5800H
350	50	7	—	—	X	—	—	Series ULS-2000H/R
350	50	8	—	—	X	—	—	Series ULS-2800H/R
350	50	8	—	X	X	—	—	UCS-4801H
350	50	8	—	X	X	—	—	UCS-5801H
350	50	8	X	X	—	—	—	UCS-4821H
350	80	8	X	X	—	—	—	UCS-4822H
350	80	8	X	X	—	—	—	UCS-5822H
350	95	7	—	—	X	—	—	Series ULS-2020H/R
350	95	8	—	—	X	—	—	Series ULS-2820H/R
350	100	8	X	X	—	—	—	UCS-4823H
500	50	7	—	—	X	—	—	Series ULS-2010H/R
500	50	8	—	—	X	—	—	Series ULS-2810H/R
1250	50	4	—	—	X	—	—	Series ULS-2064H
1500	80	4	—	—	X	—	—	Series ULS-2065H
SOURCE DRIVERS								
−25	60	8	—	X	—	—	—	UCS-4815H
−25	60	8	—	X	—	—	—	UCS-5815H
−25	60	10	X	X	—	—	—	UCS-4810H
−25	60	10	X	X	—	—	—	UCS-5810H
−350	−50	8	—	—	X	—	—	UDS-2580/88H††
−350	50	8	—	—	X	—	—	UDS-2981/82H/R
−350	80	8	—	—	X	—	—	UDS-2983/84H/R
SOURCE/SINK DRIVERS								
±800	30	3	HALF-BRIDGE		X	X	—	UDS-2933/34H

*Current is maximum testing condition. Voltage is absolute maximum rating.
†NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.
††New product. Information on commercial version is given elsewhere in this data book as UDN

SELECTION GUIDE TO SMART POWER DRIVERS TO MIL-STD-883

Logic	Output Ratings*		Diode Clamps	Part Number
PARALLEL-INPUT LATCHED DRIVERS				
4-Bit	350 mA	50 V	X	UCS-4401H
4-Bit	350 mA	50 V	X	UCS-5800H
8-Bit	−25 mA	60 V	—	UCS-4815H
8-Bit	−25 mA	60 V	—	UCS-5815H
8-Bit	350 mA	50 V	X	UCS-4801H
8-Bit	350 mA	50 V	X	UCS-5801H
SERIAL-INPUT LATCHED DRIVERS				
8-Bit	350 mA	50 V	—	UCS-4821H
8-Bit	350 mA	80 V	—	UCS-4822H
8-Bit	350 mA	80 V	—	UCS-5822H
8-Bit	350 mA	100 V	—	UCS-4823H
10-Bit	−25 mA	60 V	—	UCS-4810H
10-Bit	−25 mA	60 V	—	UCS-5810H

*Current is maximum tested condition; voltage is absolute maximum rating.

SELECTION GUIDE TO 4000B SERIES CMOS LOGIC

Function	Description	Part Number				Package Style	Features
		MIL-STD-883	MIL-M-38510†		DESC Drawing		
Gates and Inverters	NAND	883C4011BC	/05001B	/05051B	—	14-Pin DIP	Quad 2-Input
		883C4011UBC	—	—	—	14-Pin DIP	Quad 2-Input (Unbuffered)
		883C4012BC	/05002B	/05052B	—	14-Pin DIP	Dual 4-Input
		883C4023BC	/05003B	/05053B	7901301	14-Pin DIP	Triple 3-Input
		883C4068BC	—	—	—	14-Pin DIP	8-Input
	AND	883C4073BC	/17003B	—	—	14-Pin DIP	Triple 3-Input
		883C4081BC	/17001B	—	—	14-Pin DIP	Quad 2-Input
		883C4082BC	/17002B	—	—	14-Pin DIP	Dual 4-Input
	NOR	883C4001BC	/05252B	—	—	14-Pin DIP	Quad 2-Input
		883C4001UBC	/05202B	—	—	14-Pin DIP	Quad 2-Input (Unbuffered)
		883C4002BC	/05203B	—	—	14-Pin DIP	Dual 4-Input
		883C4025BC	/05204B	—	—	14-Pin DIP	Triple 3-Input
		883C4078BC	—	—	7704401	14-Pin DIP	8-Input
	OR	883C4071BC	/17101B	—	—	14-Pin DIP	Quad 2-Input
		883C4072BC	/17102B	—	—	14-Pin DIP	Dual 4-Input
		883C4075BC	/17103B	—	—	14-Pin DIP	Triple 3-Input
	Complex	883C4000BC	/05201B	—	—	14-Pin DIP	Dual 3-Input NOR and Inverter
		883C4007UBC	/05301B	—	—	14-Pin DIP	Dual Complimentary Pair and Inverter
		883C4030BC	/05303B	/05353B	—	14-Pin DIP	Quad 2-Input Exclusive OR
		883C4070BC	/17203B	—	—	14-Pin DIP	Quad 2-Input Exclusive OR
		883C4077BC	/17204B	—	—	14-Pin DIP	Quad Input Exclusive NOR
		883C4085BC	/17201B	—	—	14-Pin DIP	Dual 2-Wide AND-OR Invert
		883C4086BC	/16202B	—	—	14-Pin DIP	4-Wide AND-OR Invert
		883C4019BC	/05302B	/05352B	—	16-Pin DIP	Quad AND-OR Select Gate
	Inverters	883C4069UBC	—	—	—	14-Pin DIP	Hex, Pin-Compatible with 74C04
		883C4449UBC	—	—	—	16-Pin DIP	Hex, Pin-Compatible with 4009, 4049
	Expandable Gates	883C4402BC	—	—	—	16-Pin DIP	Dual 4-Input NOR
		883C4412BC	—	—	—	16-Pin DIP	Dual 4-Input NAND
Schmitt Triggers	Quad	883C4093BC	/17701B	—	77046	14-Pin DIP	2-Input NAND
	Hex	883C4584BC	—	—	—	14-Pin DIP	Inverter
Buffers	Level Shifting	883C4009UBC	/05501B	—	—	16-Pin DIP	Hex Inverter, Dual Supply
		883C4010BC	/05502B	—	—	16-Pin DIP	Hex Non-Inverting, Dual Supply
		883C4049UBC	/05503B	—	7901401	16-Pin DIP	Hex Inverter, Single Supply
		883C4050BC	/05504B	—	—	16-Pin DIP	Hex Non-Inverting, Single Supply
		883C4504BC	—	—	—	16-Pin DIP	Hex Non-Inverting, Dual Supply
	High Current	883C4041UBC	—	—	—	14-Pin DIP	Quad True/Complement
		883C4441UBC	—	—	—	14-Pin DIP	Quad Driver
	3-State	883C4502BC	—	—	—	16-Pin DIP	Hex Strobed Inverting
Encoder	8-Bit Priority	883C4532BC	/17302B	—	—	16-Pin DIP	5 V, 10 V and 15 V Parallel Rating
Decoders	Logic Functions	883C4028BC	/05901B	/05951B	—	16-Pin DIP	BCD-to-Decimal
		883C4428BC	—	—	—	14-Pin DIP	Binary-to-Octal
		883C4514BC	—	—	7703501	24-Pin DIP	4-to-16 Line Decoder/Latch (Active High Output)
		883C4515BC	—	—	7703201	24-Pin DIP	4-to-16 Line Decoder/Latch (Active Low Output)
		883C4555BC	—	—	—	16-Pin DIP	Dual 2-to-4 Line (Active High Output)
		883C4556BC	—	—	7704801	16-Pin DIP	Dual 2-to-4 Line (Active Low Output)
	Display Functions	883C4026ABC	—	—	—	16-Pin DIP	Decade Counter, 7 Segment Output
		883C4426ABC	—	—	—	16-Pin DIP	4026 with Bipolar Drivers
		883C4033ABC	—	—	—	16-Pin DIP	Decade Counter, 7 Segment Output
		883C4433ABC	—	—	—	16-Pin DIP	4033 with Bipolar Drivers
		883C4511BC	—	—	—	16-Pin DIP	BCD to 7-Seg. Latch/Decoder, Bipolar Outputs
		883C4543BC	—	—	—	16-Pin DIP	BCD to 7-Seg. Latch/Decoder, LCD Outputs

†Complete Catalog Number is M38510/—Example: M38510/05001B.
Detailed technical information for 4000B Series CMOS logic is available on request.

Continued

SELECTION GUIDE TO 4000B SERIES CMOS LOGIC

Function	Description	Part Number			Package Style	Features
		MIL-STD-883	MIL-M-38510†	DESC Drawing		
Counters	Binary	883C4024BC	/05605B	—	14-Pin DIP	7-Stage
		883C4404BC	—	—	14-Pin DIP	8-Stage
		883C4040BC	—	77058	16-Pin DIP	12-Stage
		883C4020BC	/05603B	/05653B	16-Pin DIP	14-Stage
		883C4060BC	—	—	16-Pin DIP	14-Stage with Oscillator
		883C4161BC	—	—	16-Pin DIP	4-Stage with Asynchronous Clear
		883C4163BC	—	—	16-Pin DIP	4-Stage with Synchronous Clear
		883C4193BC	—	—	16-Pin DIP	4-Bit Up/Down
		883C4516BC	—	—	16-Pin DIP	4-Stage Programmable Up/Down
		883C4526BC	—	—	16-Pin DIP	4-Stage Programmable Down
	Binary/Decade	883C4029BC	—	—	81016	16-Pin DIP	Presettable Up/Down
	Decade	883C4520BC	—	—	77025	16-Pin DIP	Dual 4-Stage Up
		883C4192BC	—	—	—	16-Pin DIP	Presettable Up/Down
		883C4510BC	—	—	—	16-Pin DIP	Programmable Up/Down
		883C4160BC	—	—	—	16-Pin DIP	Counter with Asynchronous Clear
		883C4162BC	—	—	—	16-Pin DIP	Counter with Synchronous Clear
		883C4522BC	—	—	—	16-Pin DIP	4-Stage Programmable Down
		883C4518BC	—	—	—	16-Pin DIP	Dual Up
	Decoded Outputs	883C4017BC	/05601B	/05651B	—	16-Pin DIP	Decade Counter with 10 Outputs
		883C4022BC	/05604B	—	—	16-Pin DIP	Octal Counter with 8 Outputs
	Johnson	883C4018BC	/05602B	/05652B	—	16-Pin DIP	Presettable Divide-by-n
Dividers/Multipliers	÷ 21	883C4445BC	—	—	—	16-Pin DIP	On-Board Oscillator
	Rate Multiplier	883C4527BC	—	—	—	16-Pin DIP	BCD
	Phase-Locked Loops	883C4046BC	—	—	—	16-Pin DIP	Maximum Operating Freq. 3 MHz at 10 V
		883C4446BC	—	—	—	16-Pin DIP	Maximum Operating Freq. 4 MHz at 10 V
	Multivibrators	883C4528BC	—	—	77045	16-Pin DIP	Dual Monostable
		883C4047BC	—	—	81020	16-Pin DIP	Monostable/Astable
Arithmetic Logic	4-Bit	883C4582BC	—	—	—	16-Pin DIP	Look-Ahead Carry Block
		883C4585BC	—	—	77037	16-Pin DIP	Magnitude Comparator
		883C4008BC	/05401B	—	—	16-Pin DIP	Full Adder
		883C4581BC	—	—	—	24-Pin DIP	Arithmetic Logic Unit
	12-Bit	883C4531BC	—	—	—	16-Pin DIP	Parity Tree
Flip-Flops	Dual D Type	883C4013BC	/05101B	/05151B	79011	14-Pin DIP	16 MHz Toggle Rate
	Dual JK Type	883C4027BC	/05102B	—	—	16-Pin DIP	8 MHz Toggle Rate
	Quad D Type	883C4076BC	—	—	—	16-Pin DIP	3-State Outputs
	Hex D Type	883C4174BC	—	—	—	16-Pin DIP	Functional Equivalent to TTL
Latches	R-S Type	883C4043BC	/05103B	—	—	16-Pin DIP	Quad NOR with 3-State Outputs
		883C4044BC	—	—	—	16-Pin DIP	Quad NAND with 3-State Outputs
	Clocked	883C4042BC	—	—	81019	16-Pin DIP	Quad, Common Clock
		883C4508BC	—	—	—	24-Pin DIP	Dual 4-Bit With Three-State Outputs
	Addressable	883C4099BC	—	—	—	16-Pin DIP	8-Bit
Shift Registers	Serial In/Serial Out	883C4006BC	/05701B	/05751B	—	14-Pin DIP	18-Stage
	Serial In/Parallel Out	883C4015BC	/05703B	—	—	16-Pin DIP	Dual 4-Stage
	Parallel In/Serial Out	883C4014BC	—	—	—	16-Pin DIP	8-Stage, Synchronous Parallel Loading
		883C4021BC	/05704B	/05754B	79012	16-Pin DIP	8-Stage, Asynchronous Parallel Loading
	Parallel In/Parallel Out	883C4035BC	—	—	81017	16-Pin DIP	4-Stage
	Bus Registers	883C4034BC	—	—	—	24-Pin DIP	8-Stage Universal
		883C4094BC	—	—	77025	16-Pin DIP	8-Stage Shift and Store
		883C4517BC	—	—	—	16-Pin DIP	Dual 64-Bit Static
Multiplexers and Switches	Digital Mux.	883C4512BC	—	—	—	16-Pin DIP	8-Channel Data Selector
	Analog Multiplexers and Demultiplexers	883C4051BC	—	—	—	16-Pin DIP	8-Channel Analog Multiplexer
		883C4052BC	—	—	79015	16-Pin DIP	Differential 4-Channel Analog Mux./Demux.
		883C4053BC	—	—	81018	16-Pin DIP	Triple 2-Channel Analog Mux./Demux.
	Analog Switches	883C4016BC	/05801B	—	—	14-Pin DIP	Quad SPST Switch
		883C4066BC	/05802B	/05852B	—	14-Pin DIP	Quad SPST with Buffered Control Unit
		883C4416BC	—	—	—	14-Pin DIP	4016 Configured for DPDT

†Complete Catalog Number is M38510/—Example: M38510/05001B.
Detailed technical information for 4000B Series CMOS logic is available on request.

CUSTOM DEVICES FOR MILITARY APPLICATIONS

Sprague Electric Company's Semiconductor Group has broad experience in designing and manufacturing custom integrated circuits for a wide variety of military applications. Technologies ranging from high-speed, low-power CMOS to high-voltage, high-current bipolar and BiMOS provide low-cost, space-saving, custom silicon solutions for tough military system problems. Sprague Electric offers the custom design and manufacturing resources necessary to produce high-volume, military-grade, proprietary circuits in a secure environment with a timely schedule.

In addition to custom design services, Sprague Electric also provides for customer-owned tooling (COT), an economical manufacturing capability for customers who have already designed proprietary LSI circuits compatible with Sprague processes. Two wafer fabrication facilities are available with full JAN line qualifications to MIL-M-38510.

CUSTOM MANUFACTURING SERVICES

Custom devices are available with a variety of manufacturing services. Devices may be purchased as:

DICE IN WAFER FORM
- Without Device Electrical Testing
- With 100% Electrical Testing
- Expanded Wafers

DICE IN WAFFLE PACKS
- Tested, Sorted, Inspected

PACKAGED UNITS WITH FULL ELECTRICAL TESTING
- Hermetic Dual In-Line Packages
- Plastic Dual In-Line Packages
- Leadless and Leaded Hermetic Chip Carriers
- Specialty Packages (Plastic Flatpacks, Small Outline)

These choices give the customer the flexibility to select only the services needed, minimizing custom silicon solution costs. Full military screening per MIL-STD-883, with compliant fabrication, assembly, testing, and qualification, is standard.

SERIES UHD-400, UHD-400-1, AND UHD-500 POWER AND RELAY DRIVERS

MIL-STD-883 Compliant

FEATURES

- 500 mA Output Current-Sink Capability
- Four Logic Types
- Pinning Compatible with 54/74 Logic Series
- High-Voltage Output:
  100 V Series UHD-500
  70 V Series UHD-400-1
  40 V Series UHD-400

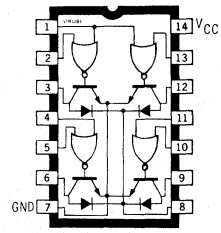
COMBINING LOGIC GATES and high-current switching transistors, these hermetically packaged, monolithic devices are used to drive incandescent or LED lamps, relays, solenoids, small dc motors, and other peripheral power loads in military and aerospace applications. Drivers with internal transient-suppression diodes are recommended for use with inductive loads.

Three minimum output-breakdown voltage ratings are available: 40 V (Series UHD-400), 70 V (Series UHD-400-1), and 100 V (Series UHD-500). All devices can sink 250 mA continuous, or 500 mA peak.

The inputs are compatible with standard TTL and CMOS logic levels. Four of eight available logic/output configurations are shown at right.

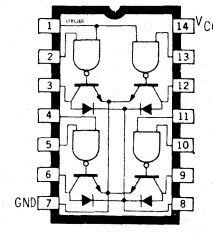
These devices are supplied in ceramic/metal side-brazed 14-pin hermetic packages. The package conforms to the dimensional requirements of MIL-M-38510 and is rated for operation over the full military temperature range of −55°C to +125°C. Power and relay drivers in flat-pack packages, Series UHC-400, UHC-400-1, and UHC-500, continue to be available on special order.

Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, is standard for all devices.



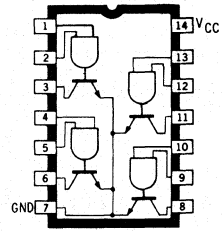
Dwg. No. A-9130B

UHD-403
UHD-403-1
UHD-503



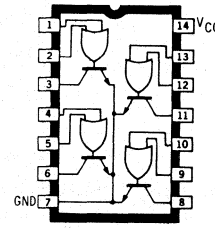
Dwg. No. A-7880B

UHD-406
UHD-406-1
UHD-506



Dwg. No. A-12,388

UHD-408
UHD-408-1
UHD-508



Dwg. No. A-12,389

UHD-432
UHD-432-1
UHD-532

Device Part Number Designation

Part Numbers*			Function
400	400-1	500	Quad 2-Input AND
402	402-1	502	Quad 2-Input OR
403	403-1	503	Quad OR for Inductive Loads
406	406-1	506	Quad AND for Inductive Loads
407	407-1	507	Quad NAND for Inductive Loads
408	408-1	508	Quad 2-Input NAND
432	432-1	532	Quad 2-Input NOR
433	433-1	533	Quad NOR for Inductive Loads

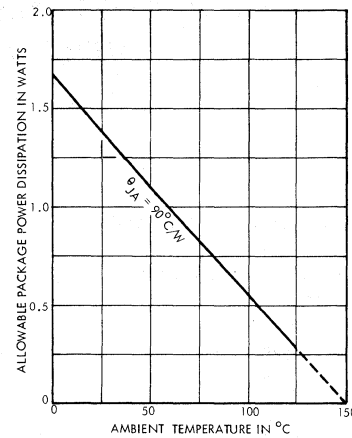
*Complete part number includes the prefix UHD.

6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . 7 V
Output Voltage, V_{IN} . . . . . 5.5 V
Output Off-State Voltage, V_{OFF}
  Series UHD-400 . . . . . 40 V
  Series UHD-400-1 . . . . . 70 V
  Series UHD-500 . . . . . 100 V
Output On-State Sink Current, I_{ON}
  (one driver) . . . . . 500 mA
  (total package) . . . . . 1 A
Suppression Diode Off-State Voltage, V_R
  Series UHD-400 . . . . . 40 V
  Series UHD-400-1 . . . . . 70 V
  Series UHD-500 . . . . . 100 V
Suppression Diode On-State Current, I_F . . . . . 500 mA
Operating Free-Air Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION



Dwg. No. A-10,884B

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into Any Output (ON State)	—	—	250	mA

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

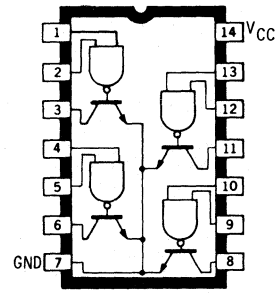
Characteristic	Series	Test Conditions (Note 3)	Limits			
			Min.	Typ.	Max.	Units
Turn-On Delay Time (t_{pd0})	UHD-400	V_S = 40 V, R_L = 265Ω (6 W)	—	200	500	ns
	UHD-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	200	500	ns
	UHD-500	V_S = 100 V, R_L = 670Ω (15 W)	—	200	500	ns
Turn-Off Delay Time (t_{pd1})	UHD-400	V_S = 40 V, R_L = 265Ω (6 W)	—	300	750	ns
	UHD-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	300	750	ns
	UHD-500	V_S = 100 V, R_L = 670Ω (15 W)	—	300	750	ns

NOTES:
1. Each input tested separately.
2. Voltage values shown in the test-circuit waveforms are with respect to network ground terminal.
3. C_L = 15 pF. Capacitance value specified includes probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0 V	$t_f \leq 7.0$ ns	t_p = 1.0 μs
$V_{in(1)}$ = 3.5 V	$t_r \leq 14$ ns	PRR = 500 kHz

UHD-400, UHD-400-1, UHD-500
Quad 2-Input AND Power Drivers

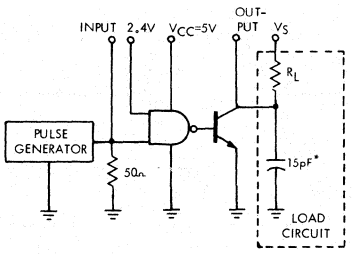


Dwg. No. A-7606

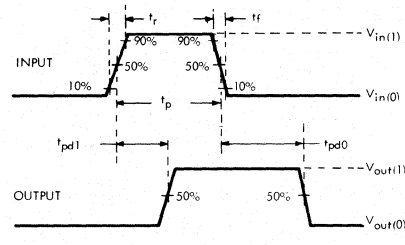
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-400	4.5 V	2.0 V	2.0 V	40 V	—	—	100	µA
			UHD-400-1	4.5 V	2.0 V	2.0 V	70 V	—	—	100	µA
			UHD-500	4.5 V	2.0 V	2.0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	17.5	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Each input is tested separately.



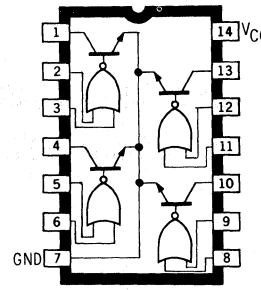
Dwg. No. A-7876E



Dwg. No. A-7628C

*Includes probe and test fixture capacitance.

UHD-402, UHD-402-1, UHD-502
Quad 2-Input OR Power Drivers

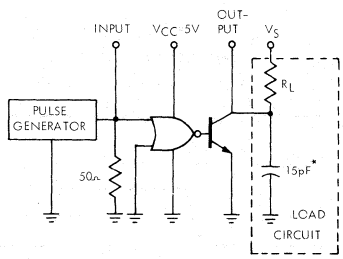


Dwg. No. A-7608

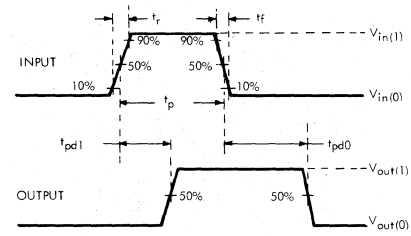
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-402	4.5 V	2.0 V	0 V	40 V	—	—	100	µA
			UHD-402-1	4.5 V	2.0 V	0 V	70 V	—	—	100	µA
			UHD-502	4.5 V	2.0 V	0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.1	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	18	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.



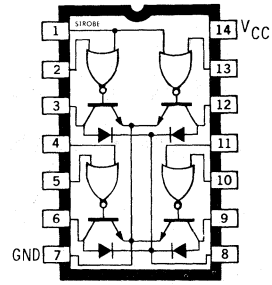
Dwg. No. A-7877C



Dwg. No. A-7628C

*Includes probe and test fixture capacitance.

UHD-403, UHD-403-1, UHD-503
Quad OR Relay Drivers

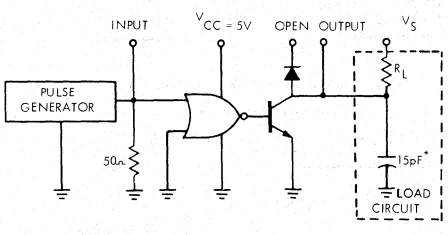


Dwg. No. A-9130B

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

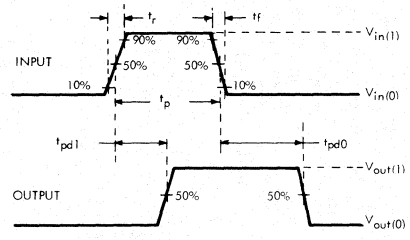
Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-403	4.5 V	2.0 V	0 V	40 V	—	—	100	µA
			UHD-403-1	4.5 V	2.0 V	0 V	70 V	—	—	100	µA
			UHD-503	4.5 V	2.0 V	0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	0.8 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	0.8 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



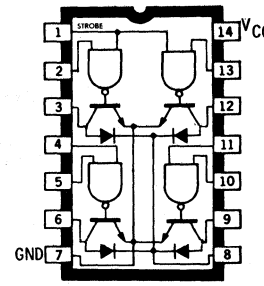
Dwg. No. A-9123C

*Includes probe and test fixture capacitance.



Dwg. No. A-7628C

UHD-406, UHD-406-1, UHD-506
Quad AND Relay Drivers

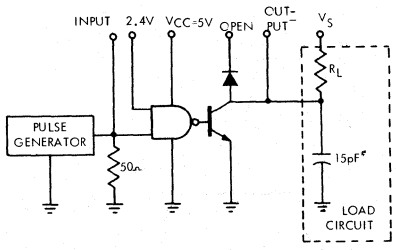


Dwg. No. A-7880B

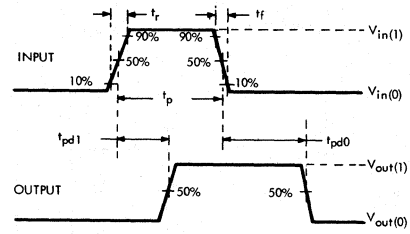
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-406	4.5 V	2.0 V	2.0 V	40 V	—	—	100	µA
			UHD-406-1	4.5 V	2.0 V	2.0 V	70 V	—	—	100	µA
			UHD-506	4.5 V	2.0 V	2.0 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.5	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	0.8 V	4.5 V	150 mA	—	—	0.6	V
				4.5 V	0.8 V	4.5 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	5.0 V	5.0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	4.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	0 V	0 V	—	—	17.5	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



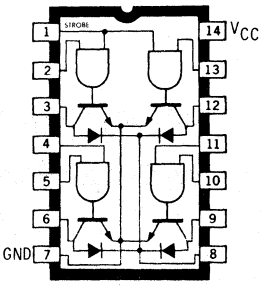
Dwg. No. A-7878C



Dwg. No. A-7628C

*Includes probe and test fixture capacitance.

UHD-407, UHD-407-1, UHD-507
Quad NAND Relay Drivers

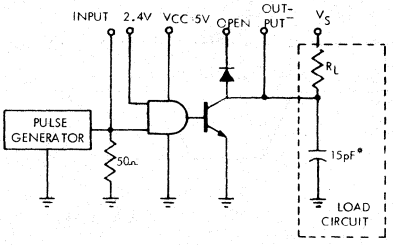


Dwg. No. A-7973B

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

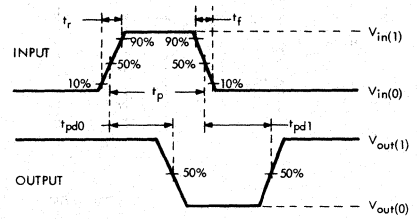
Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-407	4.5 V	0.8 V	4.5 V	40 V	—	—	100	µA
			UHD-407-1	4.5 V	0.8 V	4.5 V	70 V	—	—	100	µA
			UHD-507	4.5 V	0.8 V	4.5 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	5.0 V	5.0 V	Open	—	—	200	µA
Diode Forward Voltage	V_F	—	All	5.0 V	0 V	0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



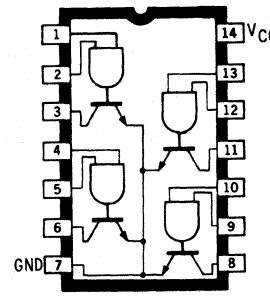
Dwg. No. A-7899C

*Includes probe and text fixture capacitance.



Dwg. No. A-7900A

UHD-408, UHD-408-1, UHD-508
Quad 2-Input NAND Power Drivers

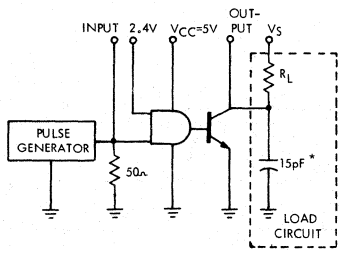


Dwg. No. 12,388

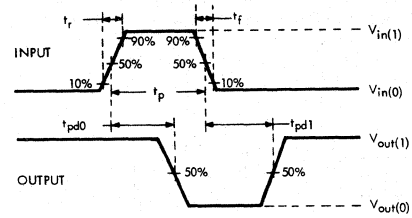
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-408	4.5 V	0.8 V	4.5 V	40 V	—	—	100	µA
			UHD-408-1	4.5 V	0.8 V	4.5 V	70 V	—	—	100	µA
			UHD-508	4.5 V	0.8 V	4.5 V	100 V	—	—	100	µA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	2.0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	2.0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	µA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	µA
				5.5 V	5.5 V	0 V	—	—	—	1000	µA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
2. Each input is tested separately.



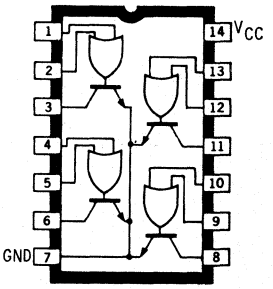
Dwg. No. A-9638A



Dwg. No. A-7900A

*Includes probe and test fixture capacitance.

UHD-432, UHD-432-1, UHD-532
Quad 2-Input NOR Power Drivers

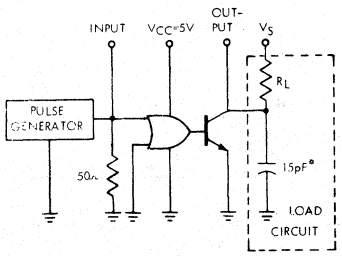


Dwg. No. A-12,389

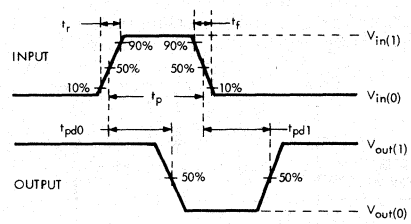
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions V_{CC}	Driven Input	Other Input	Output	Limits Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-432	4.5 V	0.8 V	0.8 V	40 V	—	—	100	μA
			UHD-432-1	4.5 V	0.8 V	0.8 V	70 V	—	—	100	μA
			UHD-532	4.5 V	0.8 V	0.8 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values are at $V_{CC} = 5.0$ V, $T_A = +25°C$.
2. Each input is tested separately.



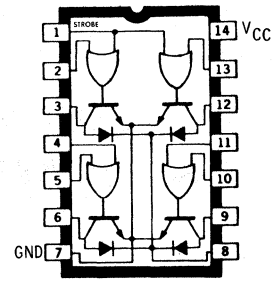
Dwg. No. A-7902C



Dwg. No. A-7900A

*Includes probe and test fixture capacitance.

UHD-433, UHD-433-1, UHD-533
Quad NOR Relay Drivers

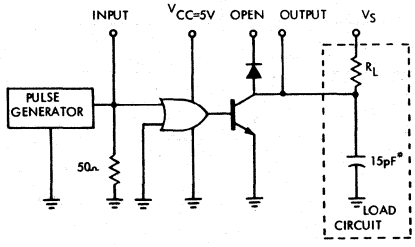


Dwg. No. A-12,390A

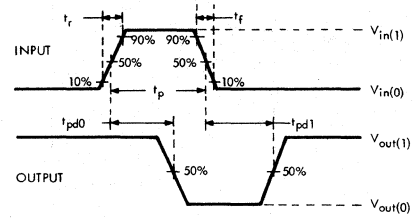
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices	Test Conditions				Limits			
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	—	UHD-433	4.5 V	0.8 V	0.8 V	40 V	—	—	100	μA
			UHD-433-1	4.5 V	0.8 V	0.8 V	70 V	—	—	100	μA
			UHD-533	4.5 V	0.8 V	0.8 V	100 V	—	—	100	μA
Output Voltage	$V_{CE(SAT)}$	−55°C to +25°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.5	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.7	V
		+125°C	All	4.5 V	2.0 V	0 V	150 mA	—	—	0.6	V
				4.5 V	2.0 V	0 V	250 mA	—	—	0.8	V
Input Voltage	$V_{IN(1)}$	—	All	4.5 V	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	—	All	4.5 V	—	—	—	—	—	0.8	V
Input Current (Note 2)	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−800	μA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	40	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Strobe Input Current	$I_{IN(0)}$	—	All	5.5 V	0.4 V	4.5 V	—	—	—	−1.6	mA
	$I_{IN(1)}$	—	All	5.5 V	2.4 V	0 V	—	—	—	100	μA
				5.5 V	5.5 V	0 V	—	—	—	1000	μA
Diode Leakage Current (Note 3)	I_R	—	All	5.0 V	5.0 V	5.0 V	Open	—	—	200	μA
Diode Forward Voltage	V_F	—	All	5.0 V	0 V	0 V	200 mA	—	1.5	1.75	V
Supply Current (Each Gate)	$I_{CC(1)}$	+25°C	All	5.5 V	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	+25°C	All	5.5 V	5.0 V	5.0 V	—	—	20	26.5	mA

NOTES:
1. All typical values at are V_{CC} = 5.0 V, T_A = +25°C.
2. Excluding strobe input; each input is tested separately.
3. All diodes tested simultaneously at pin 8 at rated V_{OFF}.



Dwg. No. A-9135C



Dwg. No. A-7900A

*Includes probe and test fixture capacitance.

SERIES ULS-2000H AND ULS-2000R HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

MIL-STD-883 Compliant

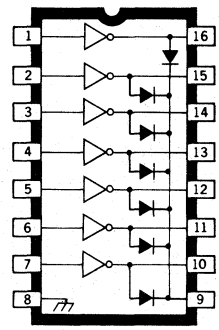
FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- Side-Brazed Hermetic Package
- Cer-DIP Hermetic Package
- High-Reliability Screening to MIL-STD-883, Class B
- −55°C to +125°C Temperature Range

COMPRISED OF SEVEN silicon NPN Darlington power drivers on a common monolithic substrate, Series ULS-2000H and ULS-2000R arrays drive relays, solenoids, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A of output current per package.

These devices are screened to MIL-STD-883, Class B and are supplied in either the popular ceramic/metal side-brazed 16-pin hermetic package (suffix 'H') or ceramic/glass cer-DIP hermetic package (suffix 'R'). Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of −55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 30 integrated circuits described in this bulletin permit the circuit designer to select the optimal device for any application. In addition to the two package styles, there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression.



Dwg. No. A-9594

Device Part Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	Part Number		
General Purpose PMOS, CMOS	ULS-2001*	ULS-2011*	ULS-2021*
14-25 V PMOS	ULS-2002*	ULS-2012*	ULS-2022*
5 V TTL, CMOS	ULS-2003*	ULS-2013*	ULS-2023*
6-15 V CMOS, PMOS	ULS-2004*	ULS-2014*	ULS-2024*
High-Output TTL	ULS-2005*	ULS-2015*	ULS-2025*

*Complete part number includes a final letter to indicate package (H = ceramic/metal size-brazed, R = ceramic/glass cer-DIP).

6

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
- (ULS-200X*, ULS-201X*) ..... 50 V
- (ULS-202X*) ..... 95 V

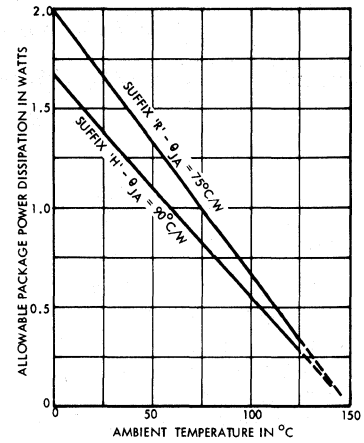
Input Voltage, V_{IN}
- (ULS-20X2, X3, X4*) ..... 30 V
- (ULS-20X5*) ..... 15 V

Peak Output Current, I_{OUT}
- (ULS-200X*, ULS-202X*) ..... 500 mA
- (ULS-201X*) ..... 600 mA

Ground Terminal Current, I_{GND} ..... 3.0 A
Continuous Input Current, I_{IN} ..... 25 mA
Power Dissipation, P_D
- (one Darlington pair) ..... 1.0 W
- (total package) ..... See Graph

Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

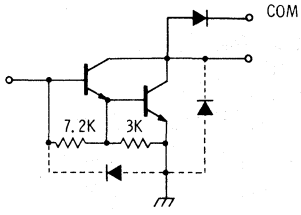
ALLOWABLE PACKAGE POWER DISSIPATION



Dwg. No. A-10,884A

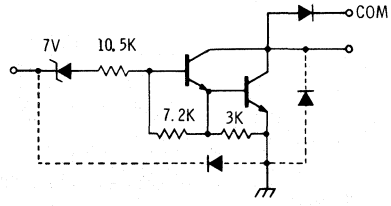
PARTIAL SCHEMATICS

ULS-20X1*
(Each Driver)



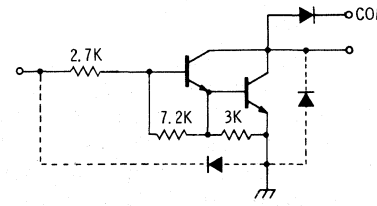
Dwg. No. A-9595

ULS-20X2*
(Each Driver)



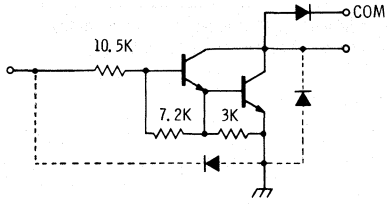
Dwg. No. A-9650

ULS-20X3*
(Each Driver)



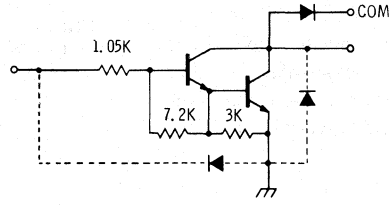
Dwg. No. A-9651

ULS-20X4*
(Each Driver)



Dwg. No. A-9898A

ULS-20X5*
(Each Driver)



Dwg. No. A-10,228

**Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP). X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.*

SERIES ULS-2000H AND ULS-2000R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	μA
		ULS-2002*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2004*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 μA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 μA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 μA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2002*		V_{IN} = 17 V	3	480	850	1300	μA
		ULS-2003*		V_{IN} = 3.85 V	3	650	930	1350	μA
		ULS-2004*		V_{IN} = 5.0 V	3	240	350	500	μA
				V_{IN} = 12 V	3	650	1000	1450	μA
		ULS-2005*		V_{IN} = 3.0 V	3	—	1500	2400	μA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2002*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2003*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2004*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2005*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2001*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ μs, see graph.

SERIES ULS-2010H AND ULS-2010R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2012*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2014*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS-2012*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2013*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2014*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2015*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2012*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
		ULS-2013*	−55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V
		ULS-2014*	−55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS-2015*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2011*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2020H AND ULS-2020R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS-2022*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2024*	25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2022*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2023*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2024*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2025*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2022*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2023*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2024*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2025*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2021*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

TEST FIGURES

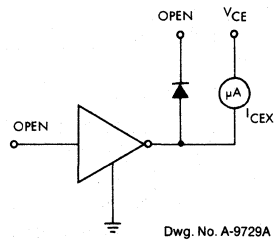


FIGURE 1A

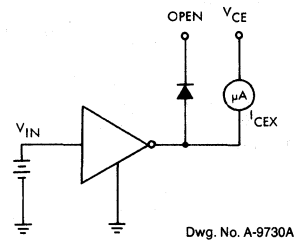


FIGURE 1B

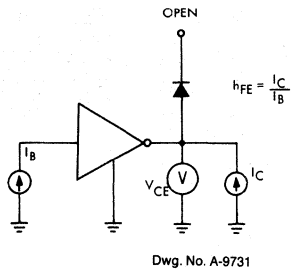


FIGURE 2

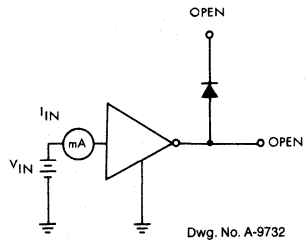


FIGURE 3

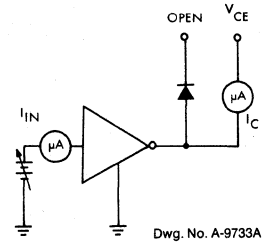


FIGURE 4

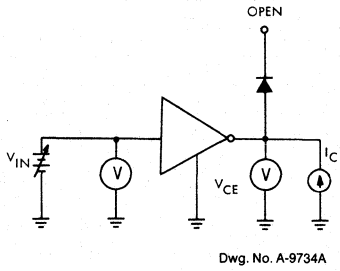


FIGURE 5

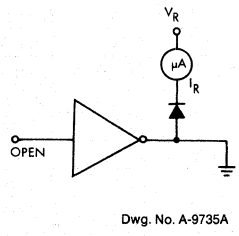


FIGURE 6

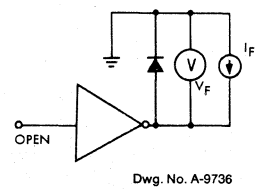
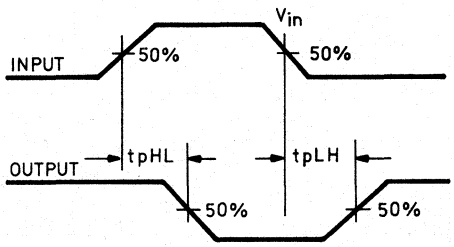
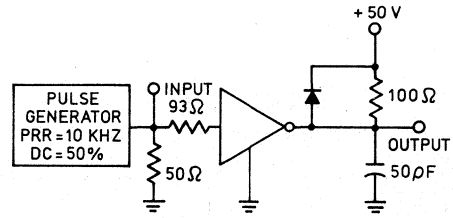


FIGURE 7

	V_{in}
ULS-20X1*	3.5 V
ULS-20X2*	13 V
ULS-20X3*	3.5 V
ULS-20X4*	12 V
ULS-20X5*	3.5 V



Dwg. No. A-13,272

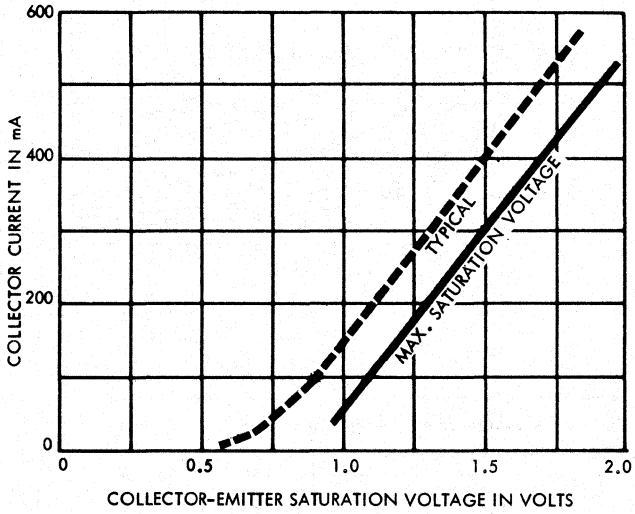


Dwg. No. A-13,273

* Complete part number includes a final letter to indicate package.
X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

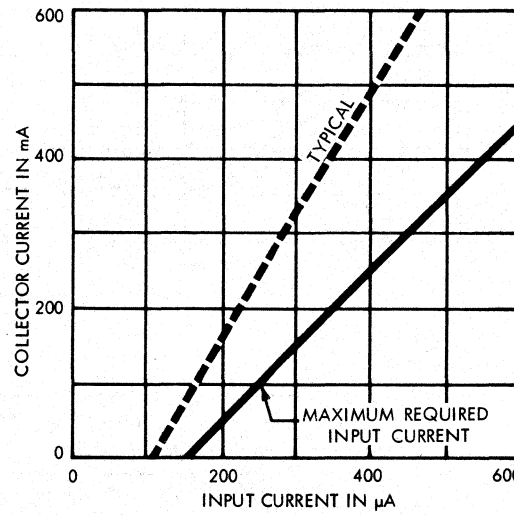
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

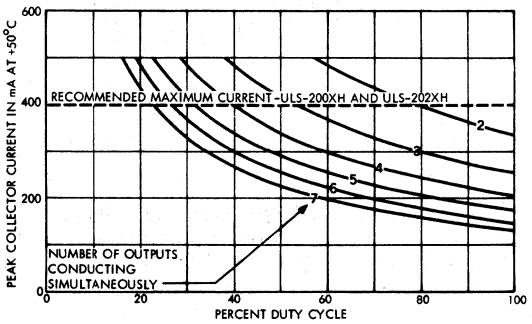


Dwg. No. A-10,872B

6

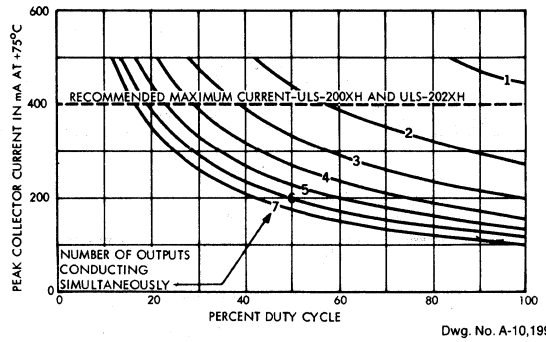
SERIES ULS-2000H

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



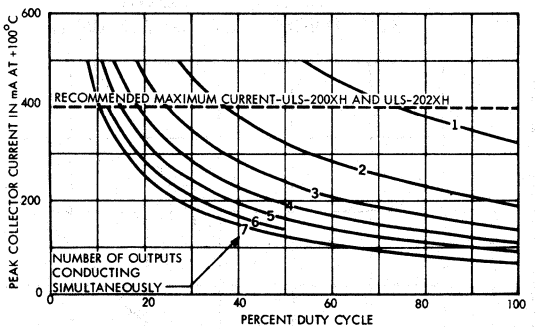
Dwg. No. A-10,197B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



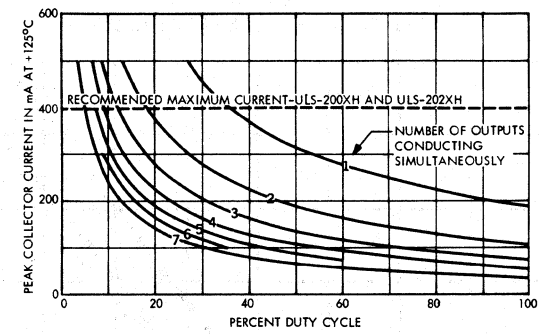
Dwg. No. A-10,199B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,200B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

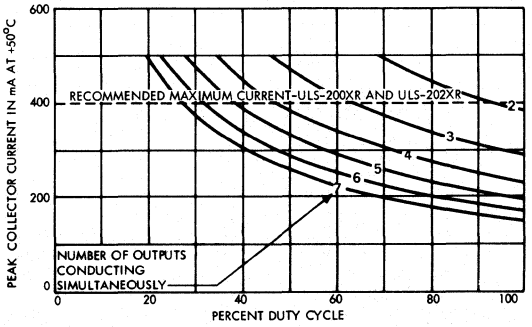


Dwg. No. A-10,201B

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

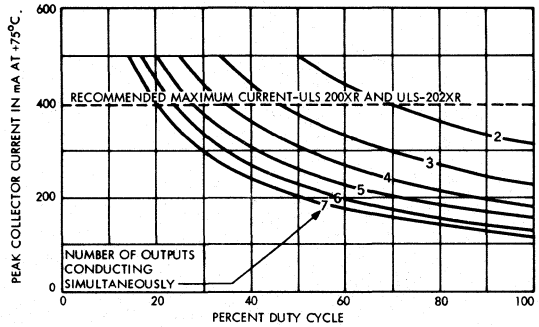
SERIES ULS-2000R

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



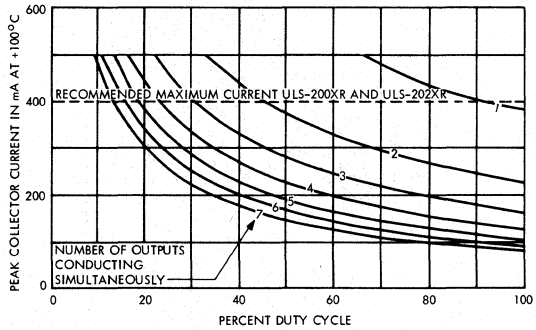
Dwg. No. A-10,883B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



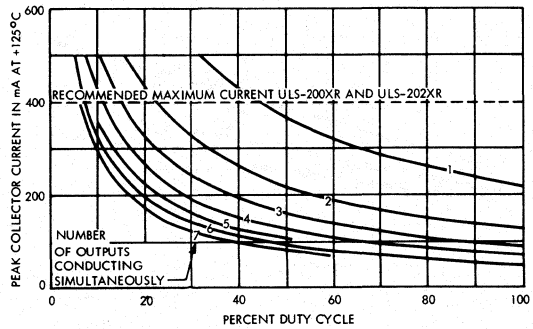
Dwg. No. A-10,887B

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,434

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

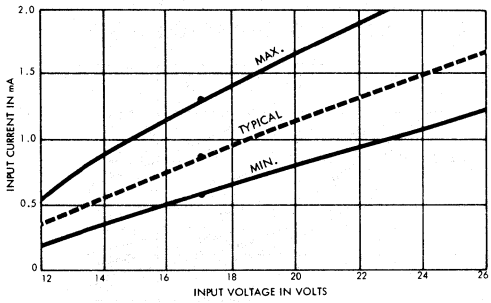


Dwg. No. A-12,435

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

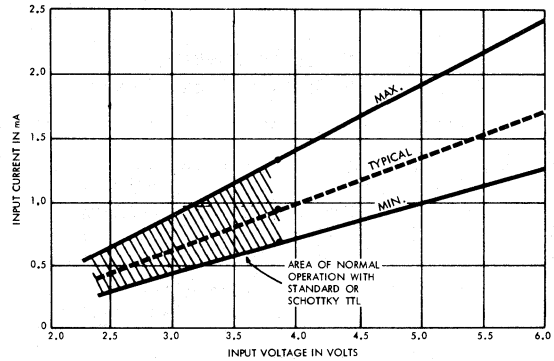
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS-20X2



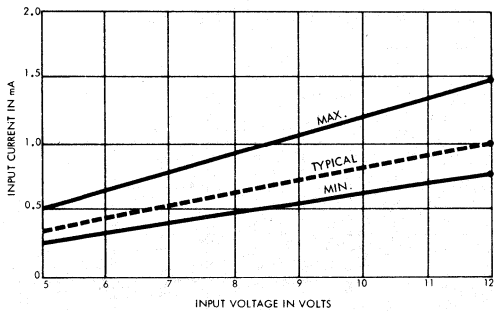
Dwg. No. A-10,225A

ULS-20X3



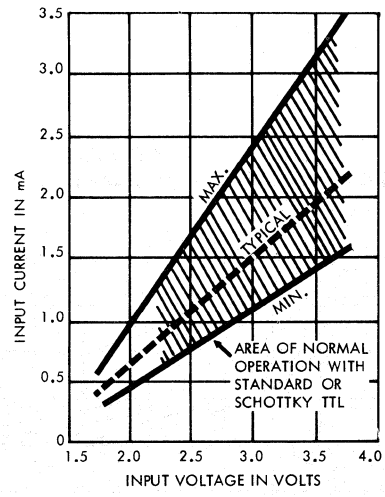
Dwg. No. A-10,224A

ULS-20X4



Dwg. No. A-10,226A

ULS-20X5



Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

ULS-2064H THROUGH ULS-2077H
1.25 A QUAD DARLINGTON SWITCHES
MIL-STD-883 Compliant

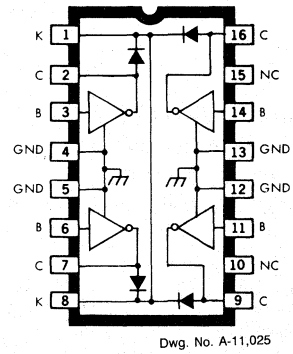
FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Units
- Transient-Protected Outputs
- Hermetically Sealed Packages
- High-Reliability Screening to MIL-STD-883, Class B

INTENDED FOR MILITARY, aerospace, and related applications, ULS-2064H through ULS-2077H quad Darlington switches interface between low-level logic and a variety of peripheral power loads such as relays, solenoids, dc and stepping motors, multiplexed LED and incandescent displays, heaters, and similar loads of up to 400 watts (1.25 A per output, 80 V, 12.5% duty cycle, +50°C). The devices are specified with a minimum output breakdown of 50 volts (35 volts sustaining at 100 mA) or 80 volts (50 volts sustaining), and a saturated output current specification of 1.25 A.

The ULS-2064/65/68/69H switches are designed for use with TTL, DTL, Schottky TTL, and 5 V CMOS logic. The ULS-2066/67/70/77H are intended for use with 6 V to 15 V CMOS and PMOS logic. These devices include integral transient-suppression diodes for use with inductive loads.

Types ULS-2068H and ULS-2069H incorporate a pre-driver stage operating from a low-current, 5 V supply. The pre-driver for the ULS-2070H and ULS-2071H operates from a low-current, 12 V supply. The input drive requirements for these devices are reduced, while still allowing the outputs to switch currents up to 1.5 A.



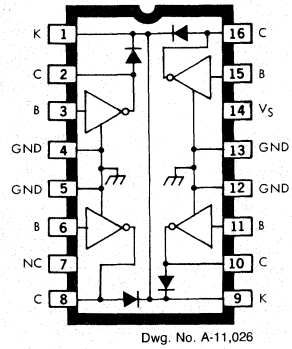
Dwg. No. A-11,025

ULS-2064H—ULS-2067H

The ULS-2074H through ULS-2077H switches are intended for use in emitter-follower applications. These circuits are identical with the ULS-2064H through ULS-2067H except for the uncommitted emitters and the omission of the suppression diodes.

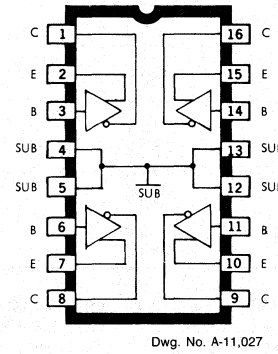
Reverse-bias burn-in and 100% high-reliability screening are standard for all side-brazed hermetic

Continued next page



Dwg. No. A-11,026

ULS-2068H—ULS-2071H



Dwg. No. A-11,027

ULS-2074H—ULS-2077H

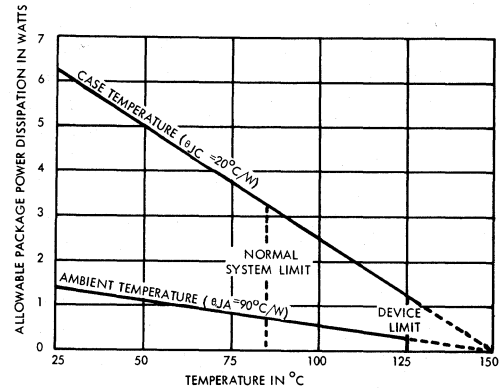
integrated circuits from Sprague Electric Company. Those devices previously manufactured as the ULS-2064H through ULS-2077H are now screened to the additional requirements of MIL-STD-883, Class B, and are so marked.

These quad Darlington switches are supplied in 16-pin ceramic/metal side-brazed hermetic packages. On special order, economical ceramic/glass cer-DIP hermetic packages can be specified by changing the part number suffix from 'H' to 'R'. Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the military temperature range of −55°C to +125°C.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature for any one driver (unless otherwise noted)

Output Voltage, V_{CEX} ..... See Below
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... See Below
Output Current, I_{OUT} (Note 1) ..... 1.5 A
Input Voltage, V_{IN} (Note 2) ..... See Below
Input Current, I_B (Note 3) ..... 25 mA
Supply Voltage, V_S (ULS-2068/69H) ..... 10 V
(ULS-2070/71H) ..... 20 V
Total Package Power Dissipation ..... See Graph
Power Dissipation, P_D/Output ..... 2.2 W
Operating Ambient Temperature Range, T_A . −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



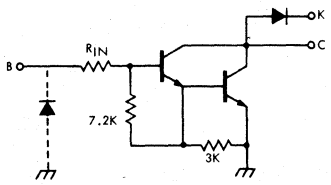
Dwg. No. A-10,198A

Type Number	V_{CEX} (Max.)	$V_{CE(SUS)}$ (Min.)	V_{IN} (Max.)	Application
ULS-2064H	50 V	35 V	15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULS-2065H	80 V	50 V	15 V	
ULS-2066H	50 V	35 V	30 V	6 to 15 V CMOS and PMOS
ULS-2067H	80 V	50 V	30 V	
ULS-2068H	50 V	35 V	15 V	TTL, DTL, Schottky TTL, and 5 V CMOS
ULS-2069H	80 V	50 V	15 V	
ULS-2070H	50 V	35 V	30 V	6 to 15 V CMOS and PMOS
ULS-2071H	80 V	50 V	30 V	
ULS-2074H	50 V	35 V	30 V	General-Purpose
ULS-2075H	80 V	50 V	60 V	
ULS-2076H	50 V	35 V	30 V	6 to 15 V CMOS and PMOS
ULS-2077H	80 V	50 V	60 V	

Notes:
1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is with reference to the substrate (no connection to any other pins) for the ULS-2074/75/76/77H, reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

ULS-2064H THROUGH ULS-2067H

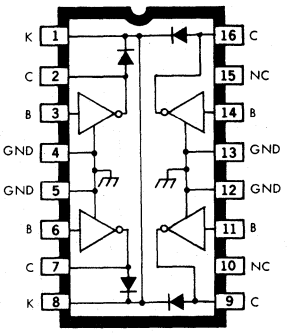
PARTIAL SCHEMATIC



Dwg. No. A-10,353

ULS-2064H
ULS-2065H $R_{IN} = 350\ \Omega$

ULS-2066H
ULS-2067H $R_{IN} = 3\ k\Omega$



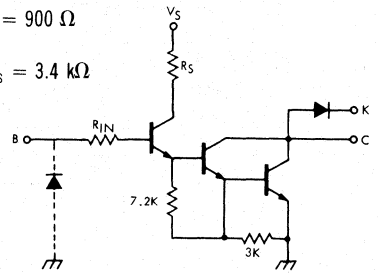
Dwg. No. A-11,025

ULS-2068H THROUGH ULS-2071H

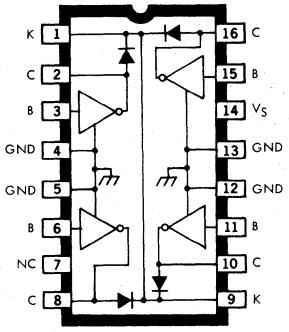
PARTIAL SCHEMATIC

ULS-2068H
ULS-2069H $R_{IN} = 2.5\ k\Omega$, $R_S = 900\ \Omega$

ULS-2070H
ULS-2071H $R_{IN} = 11.6\ k\Omega$, $R_S = 3.4\ k\Omega$



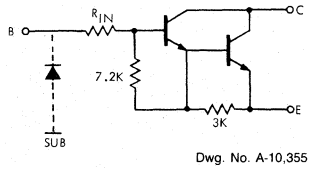
Dwg. No. A-10,354



Dwg. No. A-11,026

ULS-2074H THROUGH ULS-2077H

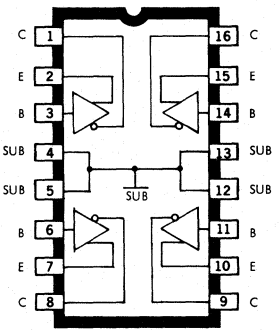
PARTIAL SCHEMATIC



Dwg. No. A-10,355

ULS-2074H
ULS-2075H $R_{IN} = 350\ \Omega$

ULS-2076H
ULS-2077H $R_{IN} = 3\ k\Omega$



Dwg. No. A-11,027

6

ULS-2064H THROUGH ULS-2067H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS-2064/66H		V_{CE} = 50 V	1	—	500	µA
		ULS-2065/67H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2064/66H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS-2065/67H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1.1 mA	3	—	1.35	V
				I_C = 750 mA, I_B = 1.7 mA	3	—	1.55	V
				I_C = 1.0 A, I_B = 2.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 3.75 mA	3	—	1.95	V
			+25°C	I_C = 500 mA, I_B = 625 µA	3	—	1.20	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.35	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.55	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.75	V
			+125°C	I_C = 500 mA, I_B = 625 µA	3	—	1.35	V
				I_C = 750 mA, I_B = 935 µA	3	—	1.55	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2064/65H		V_{IN} = 2.4 V	4	—	4.3	mA
				V_{IN} = 3.75 V	4	—	9.6	mA
		ULS-2066/67H		V_{IN} = 5.0 V	4	—	1.8	mA
				V_{IN} = 12 V	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$	ULS-2064/65H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.1	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.0	V
		ULS-2066/67H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	11.5	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	6.5	V
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS-2064/66H		V_R = 50 V	6	—	100	µA
		ULS-2065/67H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 1.25 A	7	—	2.1	V

ULS-2068H THROUGH ULS-2071H

ELECTRICAL CHARACTERISTICS over operating temperature range, V_S = 5.0 V (ULS-2068/69H) or V_S = 12 V (ULS-2070/71H), (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS-2068/70H		V_{CE} = 50 V	1	—	500	µA
		ULS-2069/71H		V_{CE} = 80 V	1	—	500	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2068/70H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS-2069/71H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ULS-2068/69H	−55°C	I_C = 500 mA, V_{IN} = 3.2 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 3.2 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 3.2 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 3.2 V	3	—	1.95	V
			+25°C	I_C = 500 mA, V_{IN} = 2.9 V	3	—	1.20	V
				I_C = 750 mA, V_{IN} = 2.9 V	3	—	1.35	V
				I_C = 1.0 A, V_{IN} = 2.9 V	3	—	1.55	V
				I_C = 1.25 A, V_{IN} = 2.9 V	3	—	1.75	V
			+125°C	I_C = 500 mA, V_{IN} = 2.8 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 2.8 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 2.8 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 2.8 V	3	—	1.95	V
		ULS-2070/71H	−55°C	I_C = 500 mA, V_{IN} = 5.5 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 5.5 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 5.5 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 5.5 V	3	—	1.95	V
			+25°C	I_C = 500 mA, V_{IN} = 5.1 V	3	—	1.20	V
				I_C = 750 mA, V_{IN} = 5.1 V	3	—	1.35	V
				I_C = 1.0 A, V_{IN} = 5.1 V	3	—	1.55	V
				I_C = 1.25 A, V_{IN} = 5.1 V	3	—	1.75	V
			+125°C	I_C = 500 mA, V_{IN} = 5.0 V	3	—	1.35	V
				I_C = 750 mA, V_{IN} = 5.0 V	3	—	1.55	V
				I_C = 1.0 A, V_{IN} = 5.0 V	3	—	1.75	V
				I_C = 1.25 A, V_{IN} = 5.0 V	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2068/69H	−55°C	V_{IN} = 3.2 V	4	—	600	µA
			+25°C	V_{IN} = 2.75 V	4	—	550	µA
			+125°C	V_{IN} = 2.75 V	4	—	850	µA
				V_{IN} = 3.75 V	4	—	1400	µA
		ULS-2070/71H	−55°C to +25°C	V_{IN} = 5.0 V	4	—	400	µA
				V_{IN} = 12 V	4	—	1250	µA
			+125°C	V_{IN} = 5.0 V	4	—	800	µA
				V_{IN} = 12 V	4	—	1600	µA
Input Voltage	$V_{IN(ON)}$	ULS-2068/69H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.2	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.75	V
		ULS-2070/71H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	5.0	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	5.0	V
Supply Current	I_S	ULS-2068/69H		I_C = 500 mA, V_{IN} = 3.2 V	8	—	6.0	mA
		ULS-2070/71H	−55°C to +25°C	I_C = 500 mA, V_{IN} = 5.0 V	8	—	4.5	mA
			+125°C	I_C = 500 mA, V_{IN} = 5.0 V	8	—	6.0	mA
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	µs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	µs
Clamp Diode Leakage Current	I_R	ULS-2068/70H		V_R = 50 V	6	—	100	µA
		ULS-2069/71H		V_R = 80 V	6	—	100	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 1.25 A	7	—	2.1	V

6

ULS-2074H THROUGH ULS-2077H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits		
			Temp.	Electrical Conditions	Fig.	Min.	Max.	Units
Output Leakage Current	I_{CEX}	ULS-2074/76H		V_{CE} = 50 V	1	—	500	μA
		ULS-2075/77H		V_{CE} = 80 V	1	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2074/76H		I_C = 100 mA, V_{IN} = 0.4 V	2	35	—	V
		ULS-2075/77H		I_C = 100 mA, V_{IN} = 0.4 V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1.1 mA	3	—	1.35	V
				I_C = 750 mA, I_B = 1.7 mA	3	—	1.55	V
				I_C = 1.0 A, I_B = 2.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 3.75 mA	3	—	1.95	V
			+25°C	I_C = 500 mA, I_B = 625 μA	3	—	1.20	V
				I_C = 750 mA, I_B = 935 μA	3	—	1.35	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.55	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.75	V
			+125°C	I_C = 500 mA, I_B = 625 μA	3	—	1.35	V
				I_C = 750 mA, I_B = 935 μA	3	—	1.55	V
				I_C = 1.0 A, I_B = 1.25 mA	3	—	1.75	V
				I_C = 1.25 A, I_B = 2.0 mA	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2074/75H		V_{IN} = 2.4 V	4	—	4.3	mA
				V_{IN} = 3.75 V	4	—	9.6	mA
		ULS-2076/77H		V_{IN} = 5.0 V	4	—	1.8	mA
				V_{IN} = 12 V	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$	ULS-2074/75H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	3.1	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	2.0	V
		ULS-2076/77H	−55°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	11.5	V
			+25°C	V_{CE} = 2.0 V, I_C = 1.0 A	5	—	6.5	V
Turn-On Delay	t_{pHL}	All	+25°C		9	—	1.0	μs
Turn-Off Delay	t_{pLH}	All	+25°C		9	—	1.5	μs

TEST FIGURES

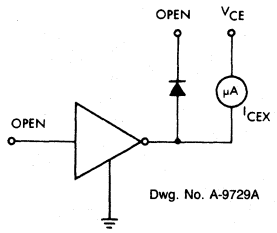


Figure 1

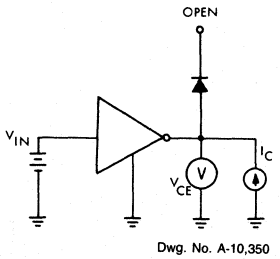


Figure 2

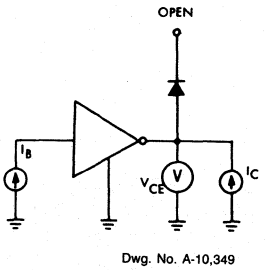


Figure 3

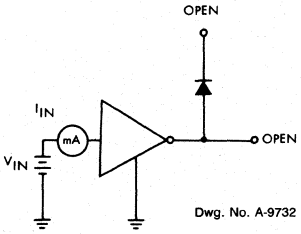


Figure 4

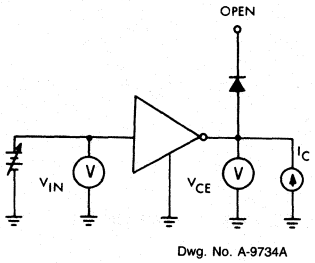


Figure 5

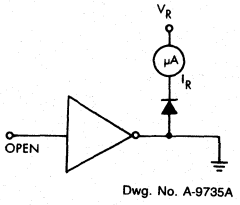


Figure 6

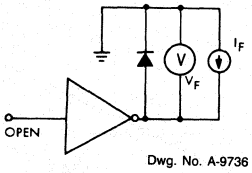


Figure 7

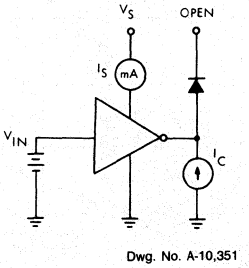
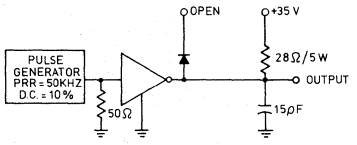


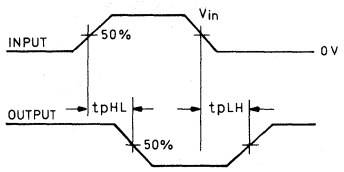
Figure 8

NOTE: Diodes not applicable to Types ULS-2074H through ULS-2077H.



Dwg. No. A-13,247

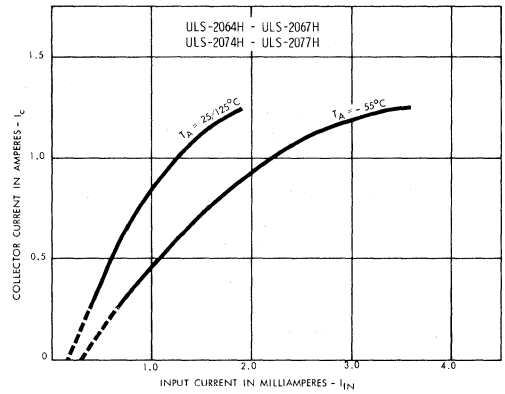
	V_{in}
ULS-2064/65/68/69/74/75H	2.4V
ULS-2066/67/70/71/76/77H	5.0V



Dwg. No. A-13,248

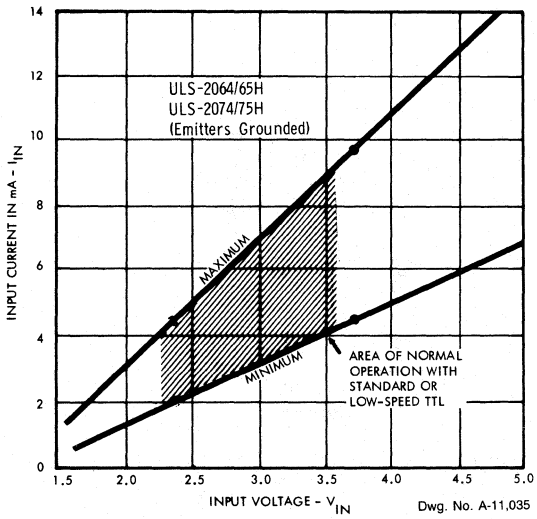
Figure 9

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



Dwg. No. A-11,030

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



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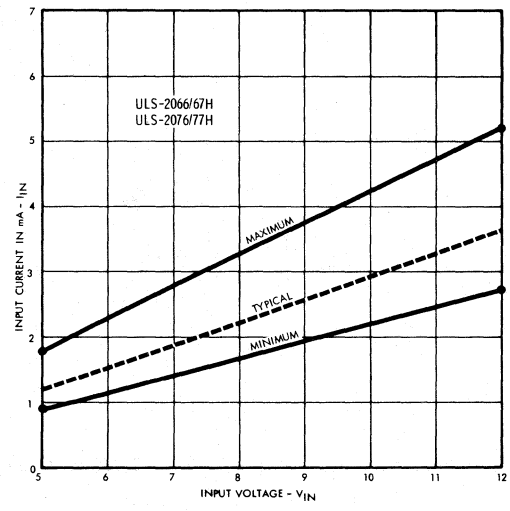
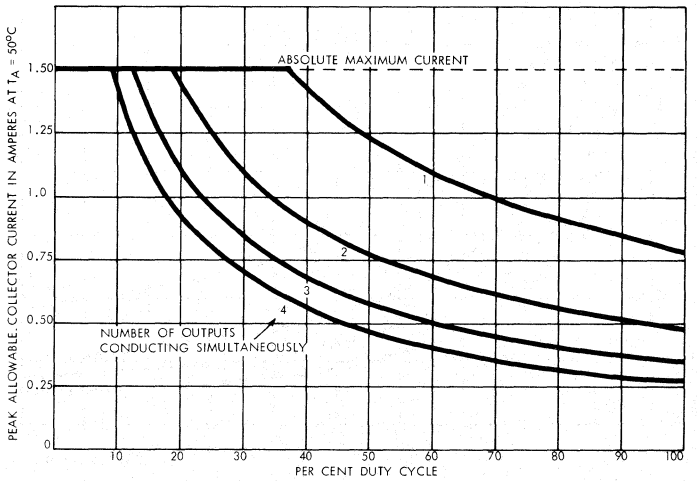


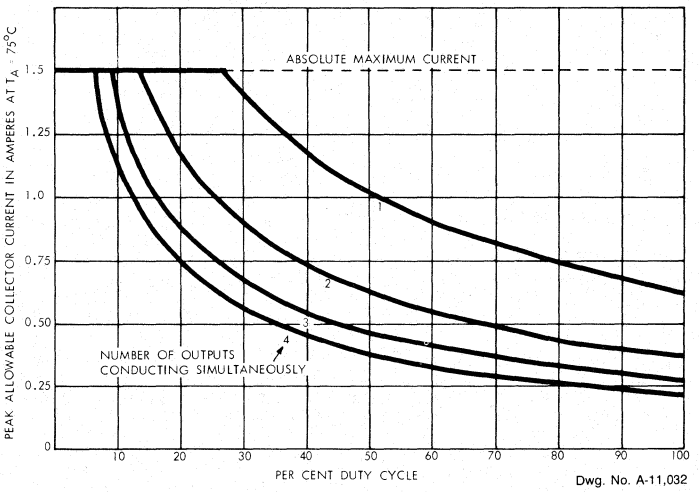
ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

AT T_A = +50°C



Dwg. No. A-11,031

AT T_A = +75°C

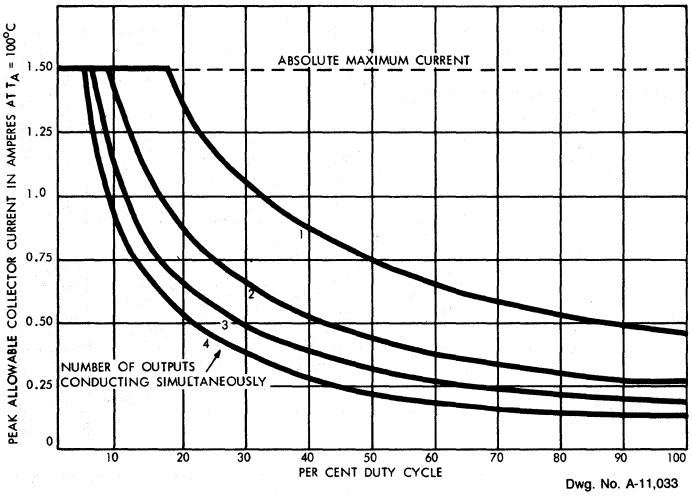


Dwg. No. A-11,032

6

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

AT T_A = +100°C



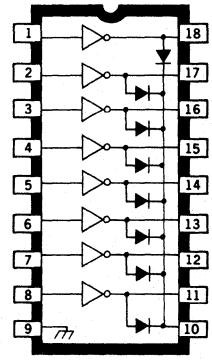
Dwg. No. A-11,033

SERIES ULS-2800H AND ULS-2800R HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

MIL-STD-883 Compliant

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- Side-Brazed Hermetic Package
- Cer-DIP Hermetic Package
- High-Reliability Screening to MIL-STD-883, Class B
- −55°C to +125°C Temperature Range



Dwg. No. A-10,322

DESIGNED TO SERVE as interface between low-level logic circuitry and high-power loads, Series ULS-2800H and ULS-2800R arrays consist of eight silicon NPN Darlington power drivers on a common monolithic substrate. They are ideally suited to driving relays, solenoids, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A output current per package.

These devices are screened to MIL-STD-883, Class B and are supplied in either the popular ceramic/metal side-brazed 18-pin hermetic package (suffix 'H') or ceramic/glass cer-DIP hermetic package (suffix 'R'). Both package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of −55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 30 integrated circuits described in this bulletin permit the circuit designer to select the optimal device for any application. In addition to the two package styles, there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression.

Device Part Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	Part Number		
General Purpose PMOS, CMOS	ULS-2801*	ULS-2811*	ULS-2821*
14-25 V PMOS	ULS-2802*	ULS-2812*	ULS-2822*
5 V TTL, CMOS	ULS-2803*	ULS-2813*	ULS-2823*
6-15 V CMOS, PMOS	ULS-2804*	ULS-2814*	ULS-2824*
High-Output TTL	ULS-2805*	ULS-2815*	ULS-2825*

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP)

6

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
- (ULS-280X*, ULS-281X*) . . . . . 50 V
- (ULS-282X*) . . . . . 95 V

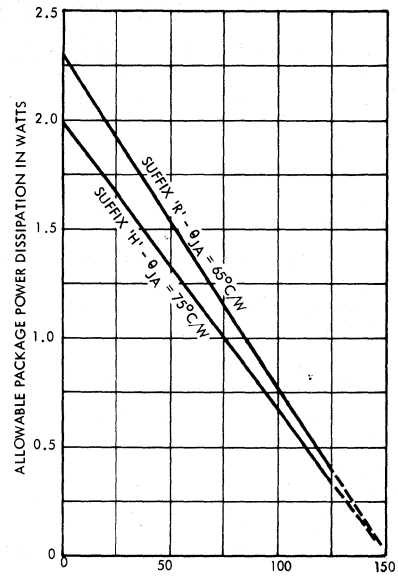
Input Voltage, V_{IN}
- (ULS-28X2, X3, X4*) . . . . . 30 V
- (ULS-28X5*) . . . . . 15 V

Peak Output Current, I_{OUT}
- (ULS-280X*, ULS-282X*) . . . . . 500 mA
- (ULS-281X*) . . . . . 600 mA

Ground Terminal Current, I_{GND} . . . . . 3.0 A
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D
- (one Darlington pair) . . . . . 1.0 W
- (total package) . . . . . See Graph

Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

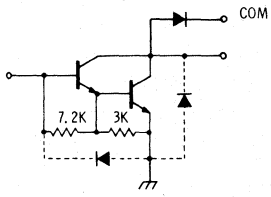
ALLOWABLE PACKAGE POWER DISSIPATION



Dwg. No. A-10,879A

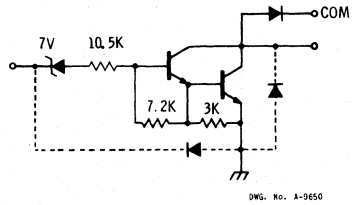
PARTIAL SCHEMATICS

ULS-28X1*
(Each Driver)



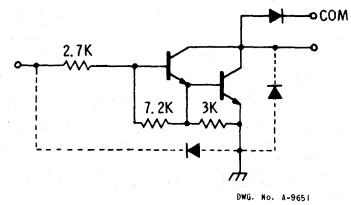
Dwg. No. A-9595

ULS-28X2*
(Each Driver)



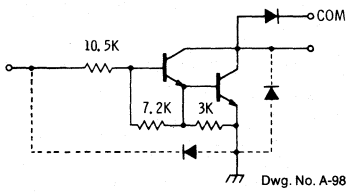
Dwg. No. A-9650

ULS-28X3*
(Each Driver)



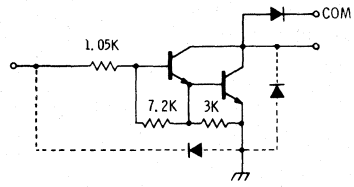
Dwg. No. A-9651

ULS-28X4*
(Each Driver)



Dwg. No. A-9898A

ULS-28X5*
(Each Driver)



Dwg. No. A-10,228

**Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP). X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.*

SERIES ULS-2800H AND ULS-2800R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2802*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2804*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2802*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2803*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2804*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2805*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2802*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2803*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2804*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2805*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2801*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2810H AND ULS-2810R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS-2812*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2814*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS-2812*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2813*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2814*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2815*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2812*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
		ULS-2013*	−55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V
		ULS-2814*	−55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS-2815*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2811*	−55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

SERIES ULS-2820H AND ULS-2820R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS-2822*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS-2824*	25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2822*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS-2823*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS-2824*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS-2825*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS-2822*	−55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	13	V
		ULS-2823*	−55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V
		ULS-2824*	−55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS-2825*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2821*	−55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_f	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

TEST FIGURES

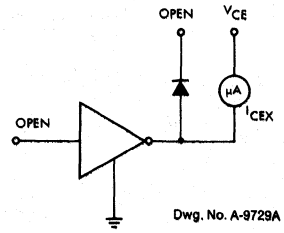


FIGURE 1A

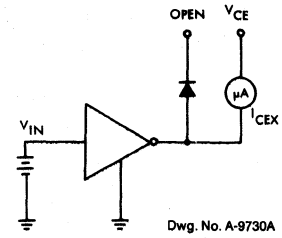


FIGURE 1B

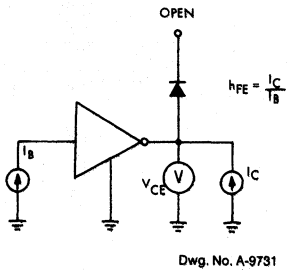


FIGURE 2

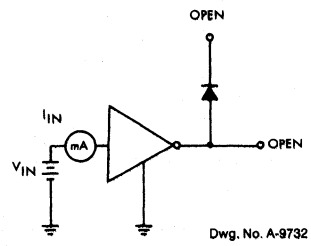


FIGURE 3

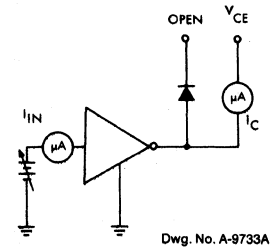


FIGURE 4

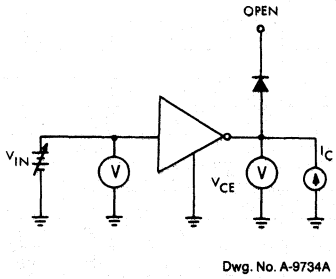


FIGURE 5

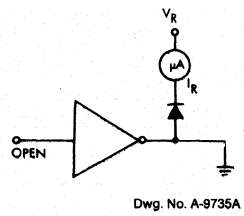


FIGURE 6

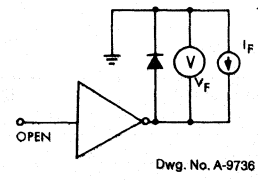
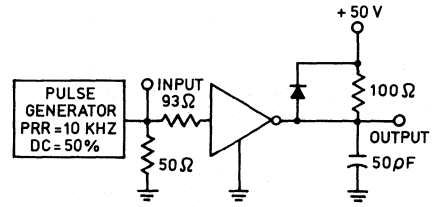
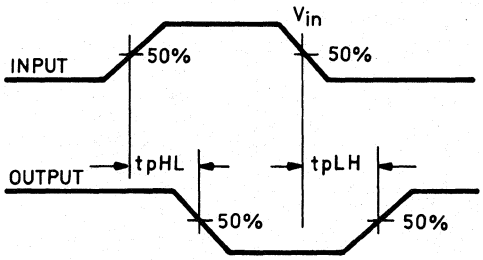


FIGURE 7

	V_{in}
ULS-28X1*	3.5 V
ULS-28X2*	13 V
ULS-28X3*	3.5 V
ULS-28X4*	12 V
ULS-28X5*	3.5 V



Dwg. No. A-13,273

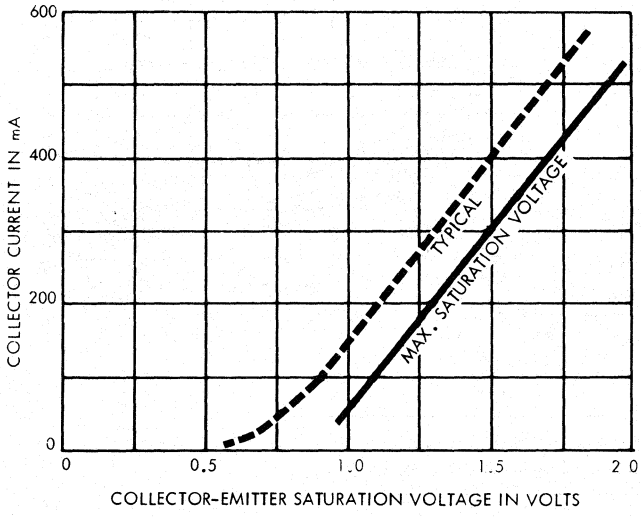


Dwg. No. A-13,272

* Complete part number includes a final letter to indicate package.
X = Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

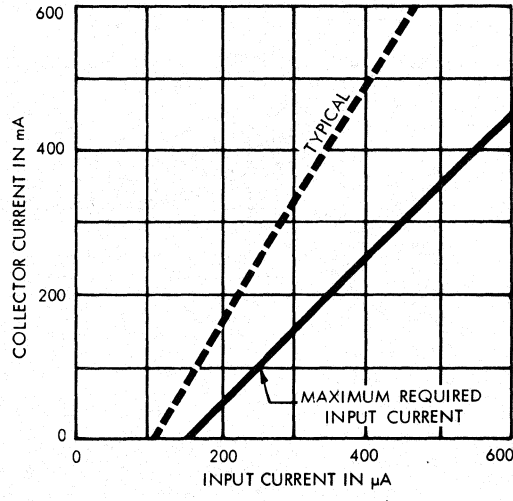
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg. No. A-9754C

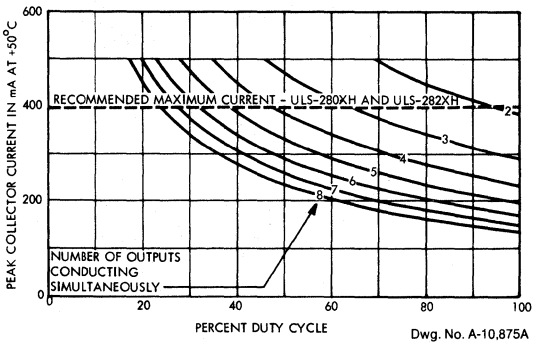
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



Dwg. No. A-10,872B

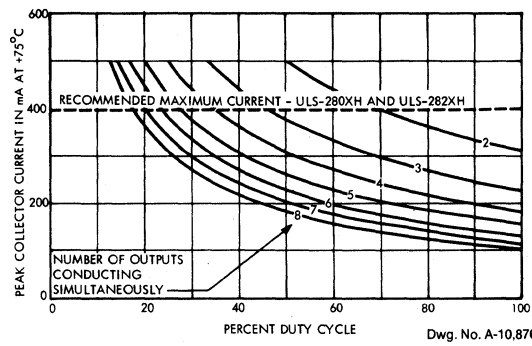
SERIES ULS-2800H

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



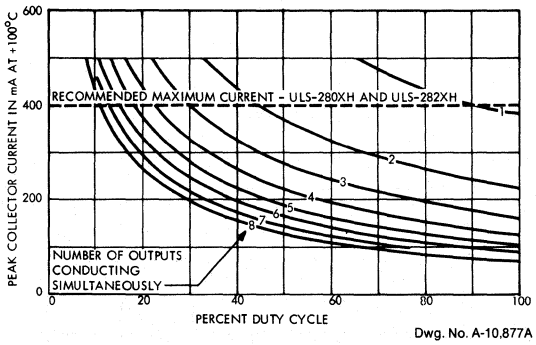
Dwg. No. A-10,875A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



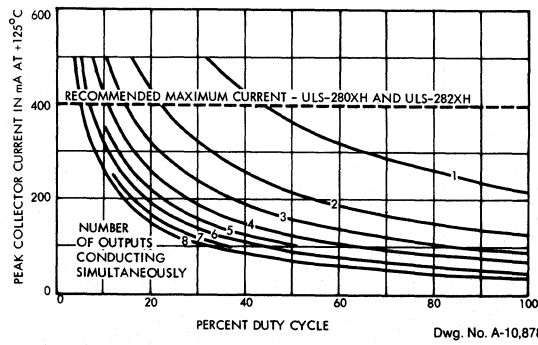
Dwg. No. A-10,876A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-10,877A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

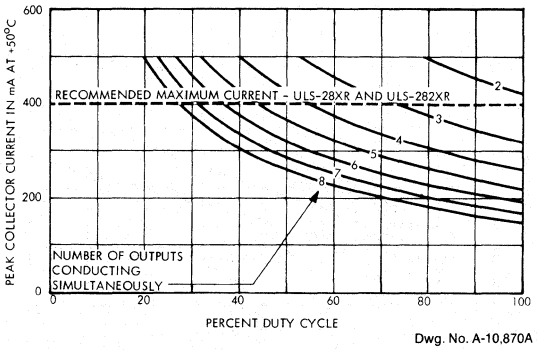


Dwg. No. A-10,878A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

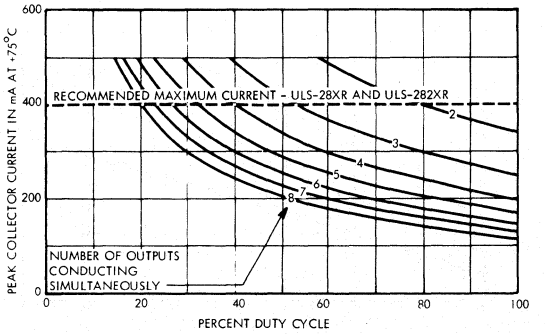
SERIES ULS-2800R

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



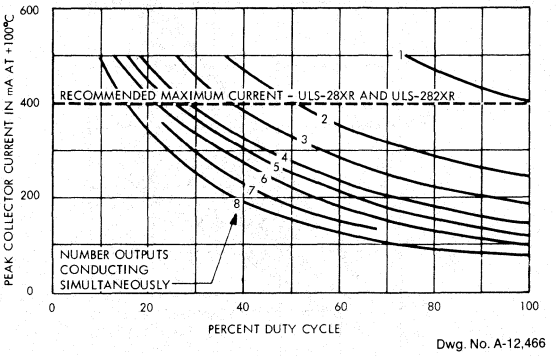
Dwg. No. A-10,870A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



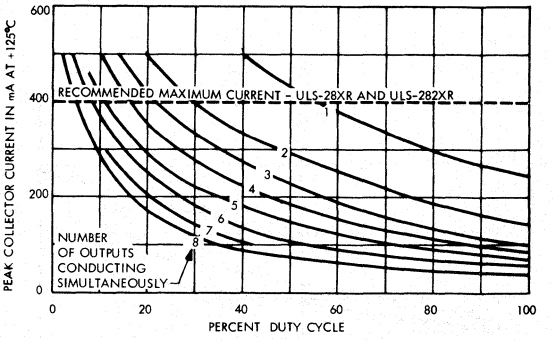
Dwg. No. A-10,871A

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg. No. A-12,466

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

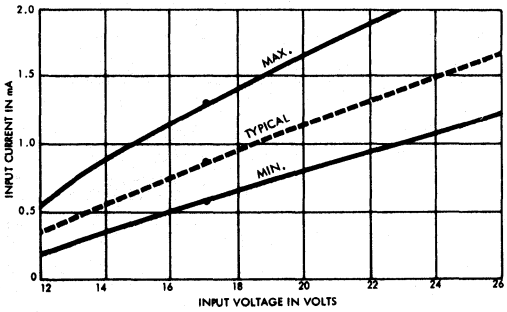


Dwg. No. A-12,467

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

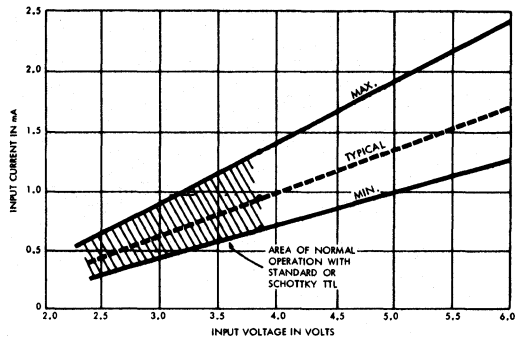
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS-28X2



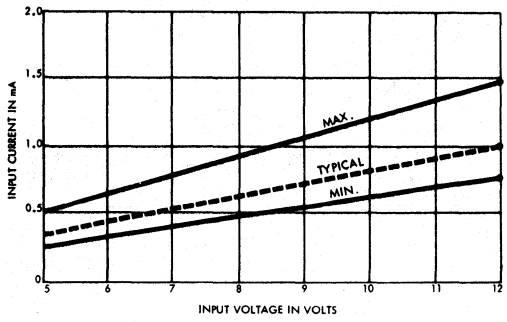
Dwg. No. A-10,225A

ULS-28X3



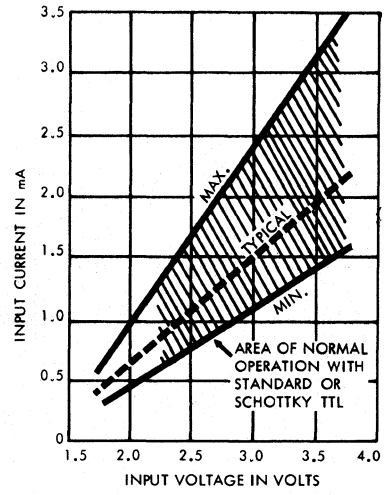
Dwg. No. A-10,224A

ULS-28X4



Dwg. No. A-10,226A

ULS-28X5



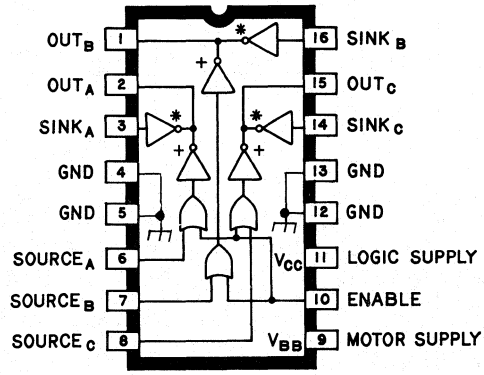
Dwg. No. A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

UDS-2933H AND UDS-2934H
HERMETIC 3-CHANNEL HALF-BRIDGE MOTOR DRIVERS
MIL-STD-883 Compliant

FEATURES

- Output Currents to 1 A
- Output Voltage to 30 V
- Low Output-Saturation Voltage
- Transient-Protected Outputs
- Tri-State Outputs
- TTL or CMOS Compatible Inputs
- High-Reliability Screening to MIL-STD-883, Class B



Dwg. No. A-13,059

Developed for use in 3-phase brushless dc motor applications, the UDS-2933H and UDS-2934H half-bridge drivers provide output capabilities to 0.6 A and 30 V. Saturated drivers provide for low output voltage drops at maximum rated current.

The two devices differ only in input logic and supply levels: the UDS-2933H is compatible with TTL and 5 V CMOS; the UDS-2934H is used with 12 V CMOS. An ENABLE input controls the source drivers and can be used for PWM operation. The chopper drive mode is characterized by low load power dissipation levels and maximum efficiency. Both ground clamp and flyback diodes for each output are provided.

Under normal operating conditions, the UDS-2933H and UDS-2934H will drive one pair of motor windings (1 source and 1 sink ON) continuously at 250 mA and an ambient temperature of +98°C or +73°C respectively.

Both devices are supplied in glass/metal side-brazed 16-pin hermetic packages conforming to the dimensional requirements of MIL-M-38510. They are rated for operation over a temperature range of −55°C to +125°C. Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

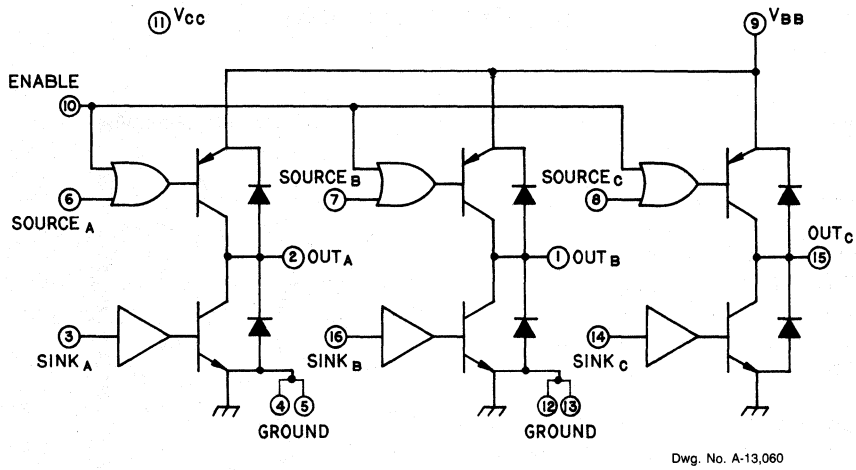
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Motor Supply Voltage Range, V_{BB} . . . . . 30 V
Logic Supply Voltage Range, V_{CC}
(UDS-2933H) . . . . . 4.5 V to 7.0 V
(UDS-2934H) . . . . . 10 V to 15 V
Logic Input Voltage, V_{IN} . . . . . V_{CC}
Output Current, I_{OUT} . . . . . ±0.6 A
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

NOTE: Output current rating will be limited by ambient temperature, number of outputs conducting, duty cycle, air flow, and adjacent heat sources. Under any set of conditions, do not exceed the ±0.6 A output current rating or a junction temperature of +150°C.

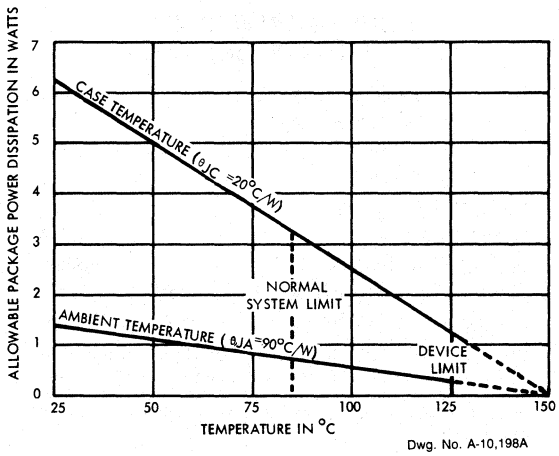
6

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,060

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,198A

TRUTH TABLE

Sink Driver Input	Source Driver Input	Enable Input	Output
Low	Low	Low	High
Low	High	Low	Open
High	Low	Low	Disallowed
High	High	Any	Low
High	Any	High	Low
Low	Any	High	Open

ELECTRICAL CHARACTERISTICS at $-55°C \leq T_A \leq +125°C$, $V_{BB} = 30\,V$, $V_{CC} = 5\,V$ (UDS-2933H) or $V_{CC} = 12\,V$ (UDS-2934H)

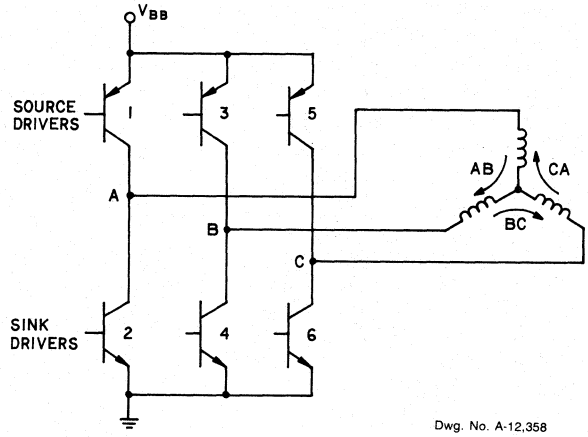
Characteristic	Symbol	Applicable Devices*	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	All Drivers OFF, $V_{OUT} = 0\,V$	—	−5.0	−500	µA
			All Drivers OFF, $V_{OUT} = 30\,V$	—	5.0	500	µA
Output Saturation Voltage	$V_{CE(SAT)}$	All	$I_{OUT} = -100\,mA$	—	—	1.1	V
			$I_{OUT} = 100\,mA$	—	—	0.2	V
			$I_{OUT} = -250\,mA$	—	—	1.2	V
			$I_{OUT} = 250\,mA$	—	—	0.3	V
			$I_{OUT} = -500\,mA$	—	—	1.5	V
			$I_{OUT} = 500\,mA$	—	—	0.6	V
Motor Supply Current	I_{BB}	All	All Drivers OFF	—	50	200	µA
			1 Source + 1 Sink ON, No Loads	—	1.0	1.3	mA
Clamp Diode Forward Voltage	V_F	All	$I_F = 500\,mA$	—	1.3	2.0	V
Logic Input Voltage	$V_{IN(1)}$	2933H		2.4	—	—	V
		2934H		8.0	—	—	V
	$V_{IN(0)}$	2933H		—	—	0.4	V
		2934H		—	—	4.0	V
Logic Input Current	$I_{IN(1)}$	2933H	$V_{IN} = 2.4\,V$	—	<1.0	10	µA
		2934H	$V_{IN} = 8.0\,V$	—	<1.0	10	µA
	$I_{IN(0)}$	All	$V_{IN} = 0.8\,V$	—	−50	−300	µA
Logic Supply Current	I_{CC}	All	All Drivers OFF	—	3.0	6.0	mA
			1 Source + 1 Sink ON	—	30	40	mA
Output Rise Time at $T_A = +25°C$	t_r	All	$I_{OUT} = -500\,mA$, $V_{BB} = 20\,V$	—	250	—	ns
			$I_{OUT} = 500\,mA$, $V_{BB} = 20\,V$	—	150	—	ns
Output Fall Time at $T_A = +25°C$	t_f	All	$I_{OUT} = -500\,mA$, $V_{BB} = 20\,V$	—	500	—	ns
			$I_{OUT} = 500\,mA$, $V_{BB} = 20\,V$	—	30	—	ns

NOTES: 1. Each driver is tested separately.
2. Positive (negative) current is defined as going into (coming out of) the specified device pin.
*Complete part number includes prefix UDS-

TYPICAL COMMUTATION SEQUENCE

Drivers ON*	Motor Current	Elec. Degrees
1 + 4	AB	0
1 + 6	−CA	60
3 + 6	BC	120
3 + 2	−AB	180
5 + 2	CA	240
5 + 4	−BC	300

*ENABLE input must be low; Source drivers are turned ON with a logic low, sink drivers are turned ON with a logic high.



Dwg. No. A-12,358

SERIES UDS-2980H AND UDS-2980R HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

MIL-STD-883 Compliant

FEATURES

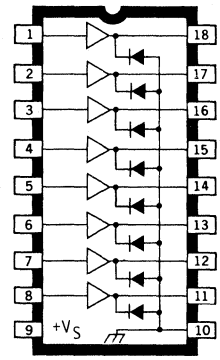
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C

SERIES UDS-2980H and UDS-2980R hermetically sealed source drivers link standard low-power digital logic and relays, solenoids, stepping motors, LEDs, and lamps in applications requiring separate logic and load grounds, load supply voltages to +80 V, and load currents to 500 mA.

Types UDS-2981H/R and UDS-2983H/R are intended for use with 5 V logic systems (TTL, Schottky TTL, DTL and 5 V CMOS). UDS-2982H/R and UDS-2984H/R integrated circuits are intended for MOS interface (PMOS and CMOS) operating from supply voltages of from 6 to 16 V.

Types UDS-2981H/R and UDS-2982H/R will withstand an output OFF voltage of 50 V. UDS-2983H/R and UDS-2984H/R drivers will withstand a maximum output OFF voltage of 80 V.

Under normal operating conditions, the devices will sustain 50 mA continuously on each of the eight outputs at an ambient temperature of +85°C and with a supply voltage of 15 V. All types include input current-limiting resistors and output transient-suppression diodes. In all cases, outputs are switched ON by an active high input level.



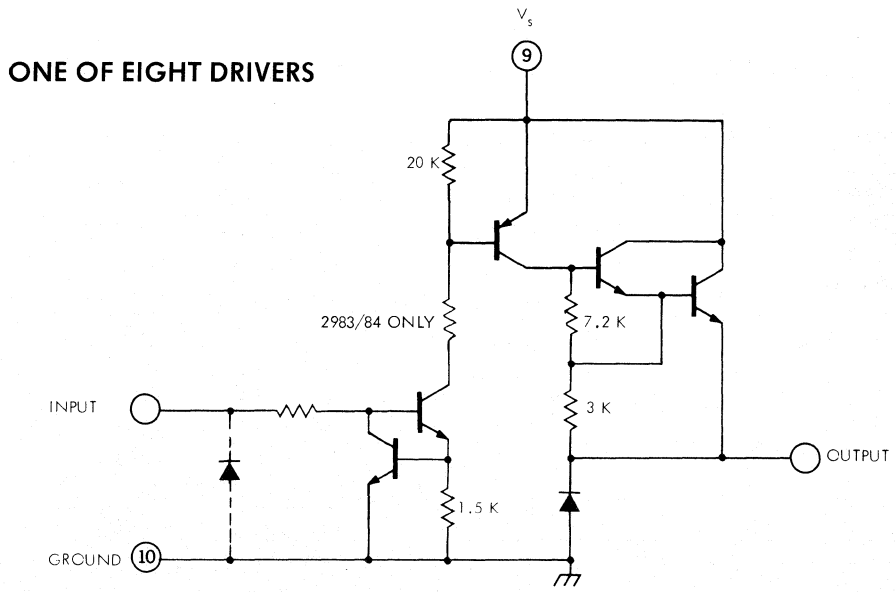
Dwg. No. A-10,243

Note that the maximum current rating may not be obtained at −55°C because of reduced beta, or at +125°C because of package power limitations.

Series UDS-2980H drivers are furnished in 18-pin ceramic/metal (side-brazed) hermetic dual in-line packages. Series UDS-2980R drivers are supplied in ceramic/glass (cer-DIP) hermetic packages. Both are processed to the requirements of MIL-STD-883, Class B.

The same circuits are also available in 18-pin plastic dual in-line packages (Series UDN-2980A) for operation over a limited temperature range, or where higher package power dissipation is needed.

Device Type	$V_{CE(MAX)}$	$V_{IN(MAX)}$	Applications
UDS-2981H/R	50 V	15 V	TTL, DTL, 5 V CMOS
UDS-2982H/R	50 V	30 V	6-15 V CMOS/PMOS
UDS-2983H/R	80 V	15 V	TTL, DTL, 5 V CMOS
UDS-2984H/R	80 V	30 V	6-15 V CMOS/PMOS



Dwg. No. A-10,242B

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

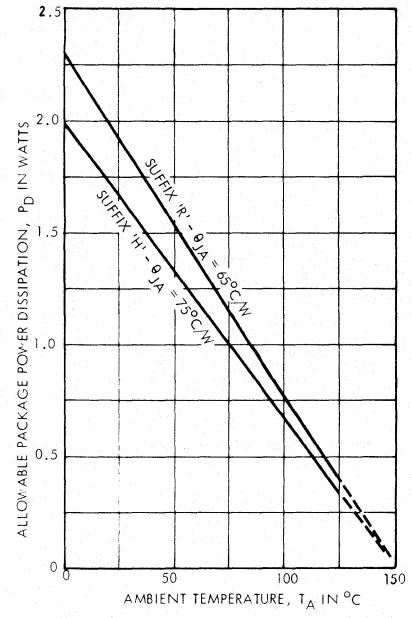
Output Voltage Range, V_{CE}
- (UDS-2981 and UDS-2982H/R) ..... +5 V to +50 V
- (UDS-2983 and UDS-2984H/R) ..... +35 V to +80 V

Input Voltage, V_{IN}
- (UDS-2981 and UDS-2983H/R) ..... +15 V
- (UDS-2982 and UDS-2984H/R) ..... +30 V

Output Current, I_{OUT} ..... −500 mA
Ground Terminal Current, I_{GND} ..... 3.0 A
Power Dissipation, P_D
- (any one driver) ..... 1.1 W
- (total package) ..... See Graph

Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,879A

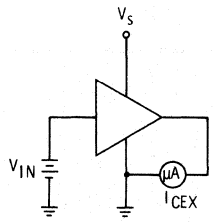
6

ELECTRICAL CHARACTERISTICS from −55°C to +125°C (unless otherwise specified)

Characteristic	Symbol	Applicable Devices†	Temp.	Test Conditions	Fig.	Limit
Maximum Output Leakage Current	I_{CEX}	UDS-2981/82		V_{IN} = 0.25 V*, V_S = 50 V	1	200 µA
		UDS-2983/84		V_{IN} = 0.25 V*, V_S = 80 V	1	200 µA
Maximum Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDS-2981/83	−55°C	V_{IN} = 2.4 V, I_{OUT} = −100 mA	2	2.0 V
				V_{IN} = 2.4 V, I_{OUT} = −200 mA	2	2.1 V
			+25°C	V_{IN} = 2.4 V, I_{OUT} = −350 mA	2	2.0 V
			+125°C	V_{IN} = 2.4 V, I_{OUT} = −100 mA	2	1.8 V
				V_{IN} = 2.4 V, I_{OUT} = −200 mA**	2	1.9 V
		UDS-2982/84	−55°C	V_{IN} = 5.0 V, I_{OUT} = −100 mA	2	2.0 V
				V_{IN} = 5.0 V, I_{OUT} = −200 mA	2	2.1 V
			+25°C	V_{IN} = 5.0 V, I_{OUT} = −350 mA	2	2.0 V
			+125°C	V_{IN} = 5.0 V, I_{OUT} = −100 mA	2	1.8 V
				V_{IN} = 5.0 V, I_{OUT} = −200 mA**	2	1.9 V
Maximum Input Current	$I_{IN(ON)}$	All		V_{IN} = 2.4 V	3	295 µA
				V_{IN} = 3.85 V	3	600 µA
				V_{IN} = 12 V	3	2.3 mA
	$I_{IN(OFF)}$	UDS-2981/82		V_{IN} = 0 V, V_S = 50 V	3	10 µA
		UDS-2983/84		V_{IN} = 0 V, V_S = 80 V	3	10 µA
Minimum Output Source Current	I_{OUT}	UDS-2981/83		V_{IN} = 2.4 V, V_{CE} = 2.2 V	2	−200 mA
		UDS-2982/84		V_{IN} = 5.0 V, V_{CE} = 2.2 V	2	−200 mA
Maximum Supply Current (Outputs Open)	I_S	UDS-2981	+25°C	V_{IN} = 2.4 V*, V_S = 50 V	4	10 mA
		UDS-2982		V_{IN} = 5.0 V*, V_S = 50 V	4	10 mA
		UDS-2983		V_{IN} = 2.4 V*, V_S = 80 V	4	10 mA
		UDS-2984		V_{IN} = 5.0 V*, V_S = 80 V	4	10 mA
Maximum Turn-ON Delay Time	t_{pHL}	UDS-2981/82	+25°C	V_S = 35 V, R_L = 175 Ω	7	2.0 µs
		UDS-2983/84		V_S = 50 V, R_L = 250 Ω	7	2.0 µs
Maximum Turn-OFF Delay Time	t_{pLH}	UDS-2981/82	+25°C	V_S = 35 V, R_L = 175 Ω	7	10 µs
		UDS-2983/84		V_S = 50 V, R_L = 250 Ω	7	10 µs
Maximum Clamp Diode Leakage Current	I_R	UDS-2981/82		V_S = 50 V (All Inputs V_{IN} = 0.25 V)	5	50 µA
		UDS-2983/84		V_S = 80 V (All Inputs V_{IN} = 0.25 V)	5	50 µA
Maximum Clamp Diode Forward Voltage	V_F	ALL		I_F = 200 mA	6	1.75 V

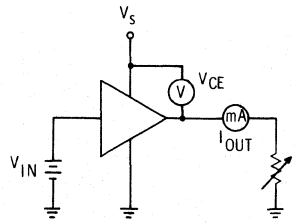
*All inputs simultaneously.
**Pulsed test.
†Complete part number includes a terminal letter that indicates package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).

TEST FIGURES



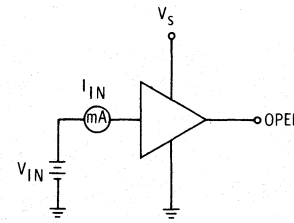
Dwg. No. A-11,083

Figure 1



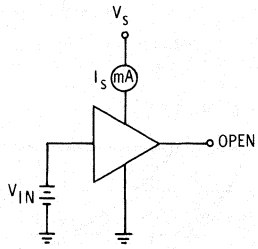
Dwg. No. A-11,084

Figure 2



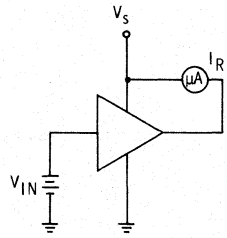
Dwg. No. A-11,085

Figure 3



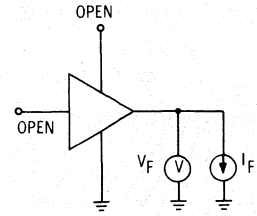
Dw.No. A-11,086

Figure 4

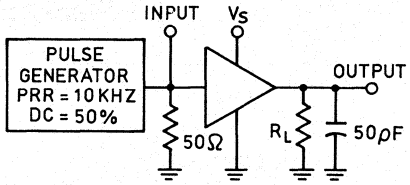


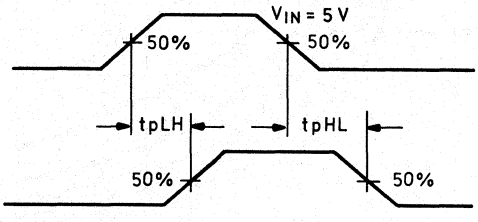
Dwg. No. A-11,087

Figure 5



Dwg. No. A-11,088

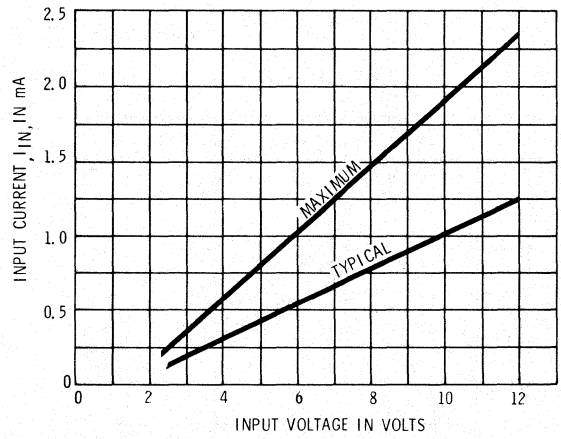




Dwg. No. A-13,263

Figure 7

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

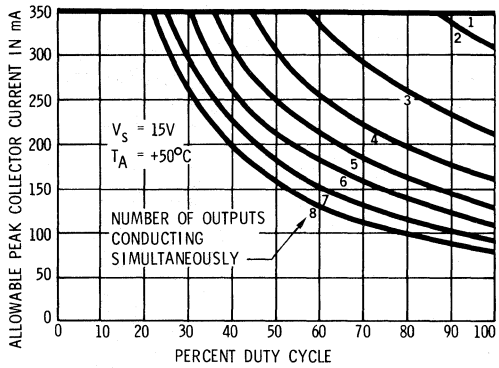


Dwg. No. A-11,115B

6

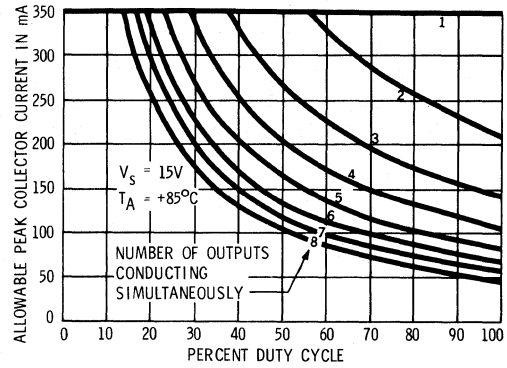
ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE SERIES UDS-2980H

UDS-2981/82H



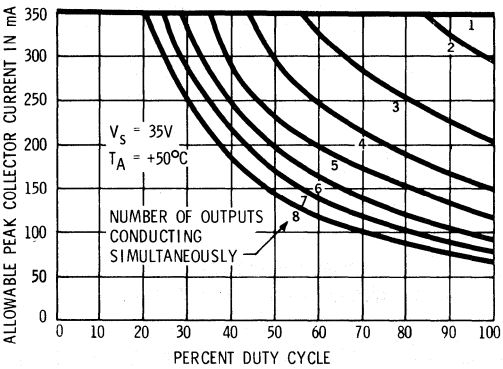
Dwg. No. A-11,078B

UDS-2981/82H



Dwg. No. A-11,076B

ALL DEVICES



Dwg. No. A-11,079B

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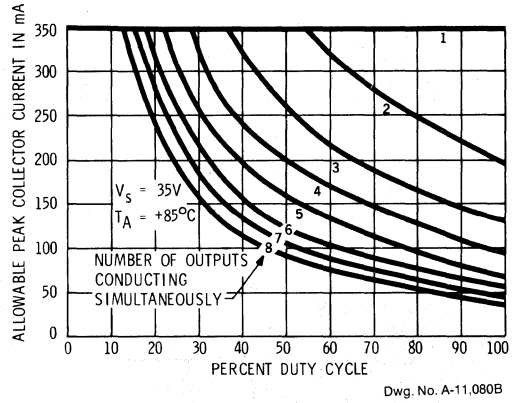
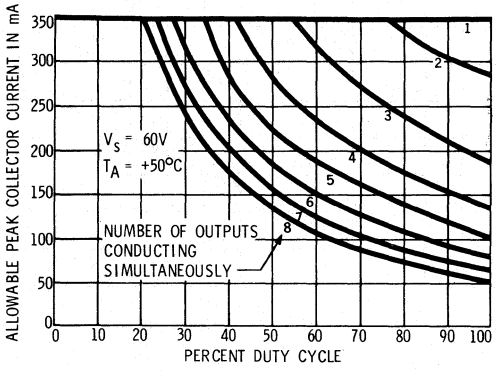


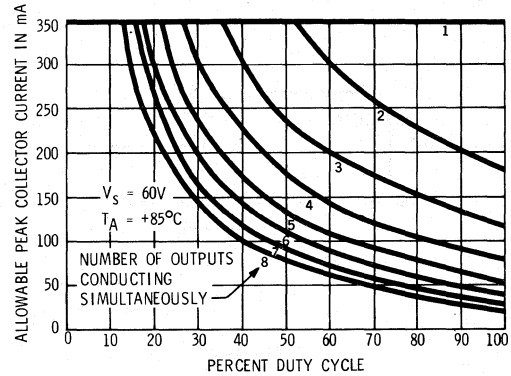
Dwg. No. A-11,080B

UDS-2983/84H



Dwg. No. A-11,077A

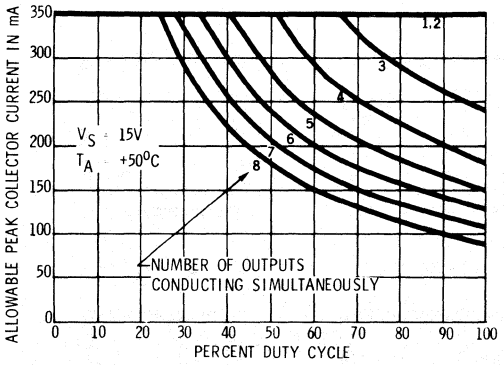
UDS-2983/84H



Dwg. No. A-11,081A

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE SERIES UDS-2980R

UDS-2981/82R



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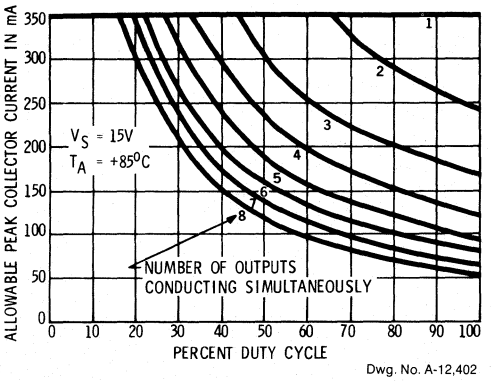
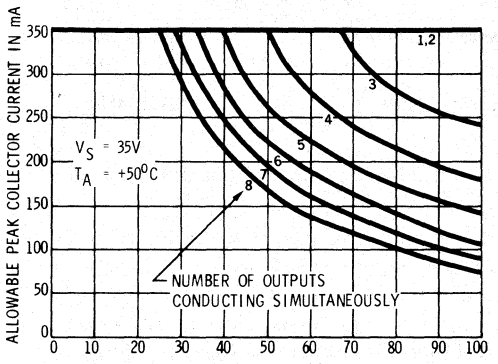
UDS-2981/82R



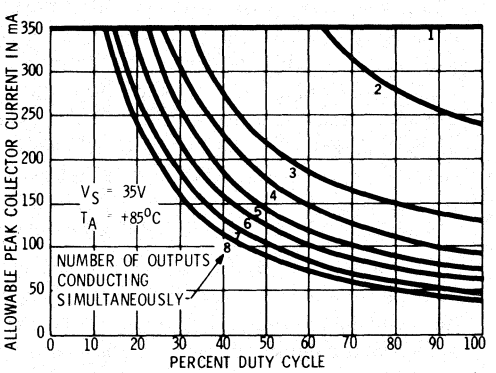
Dwg. No. A-12,402

ALL DEVICES



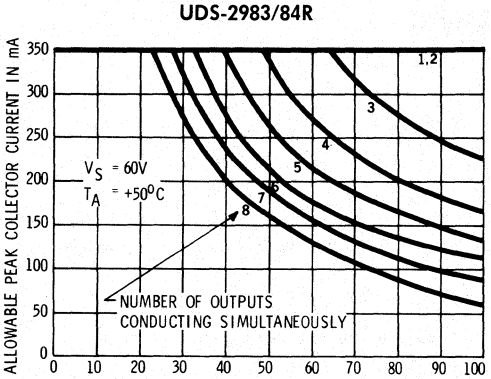
Dwg. No. A-12,403

ALL DEVICES



Dwg. No. A-12,404

UDS-2983/84R



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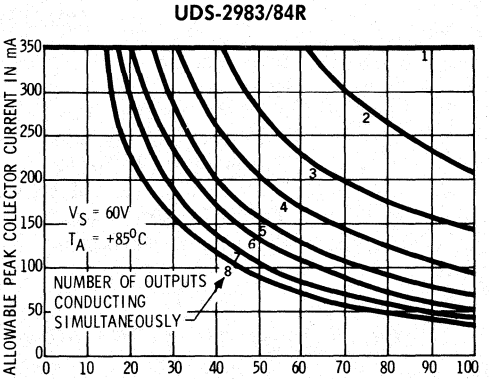
UDS-2983/84R



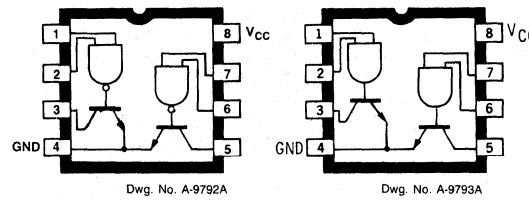
Dwg. No. A-12,406

6

SERIES UDS-3610H
DUAL 2-INPUT PERIPHERAL/POWER DRIVERS

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Hermetically Sealed Package
- High-Reliability Screening

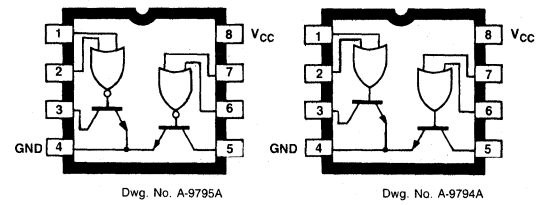


Dwg. No. A-9792A

UDS-3611H

Dwg. No. A-9793A

UDS-3612H



Dwg. No. A-9795A

UDS-3613H

Dwg. No. A-9794A

UDS-3614H

THESE mini-DIP dual 2-input peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 250 mA continuously at an ambient temperature of +75°C. In the OFF state, these drivers will withstand at least 80 V. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

The Series UDS-3610H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

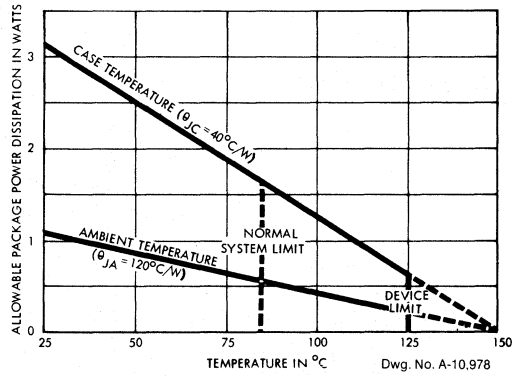
With appropriate external diode transient suppression, Series UDS-3610H drivers can also be used with inductive loads such as relays, solenoids, and stepping motors. Similar devices with integral transient suppression are in Series UDS-5710H.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Power Dissipation, P_D (One Output)	1.0 W
(Total Package)	See Graph
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

These devices are NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions			Limits				Notes
		V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{IN(1)}$	Min.	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	Min.	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−50	−100	μA	2
"1" Input Current	$I_{IN(1)}$	Max.	30 V	0 V	—	—	10	μA	2
Input Clamp Voltage	V_I	Min.	−12 mA	—	—	—	−1.5	V	—

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

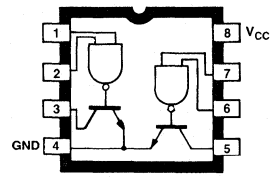
Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 W) C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 W) C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_r \leq$ 7 ns	t_p = 1 μs
$V_{IN(1)}$ = 3.5 V	$t_r \leq$ 14 ns	PRR = 500 kHz

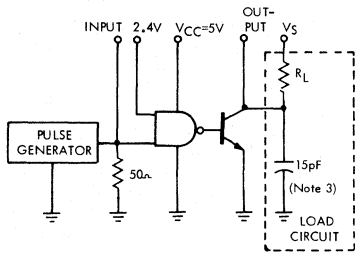
UDS-3611H
Dual AND Driver



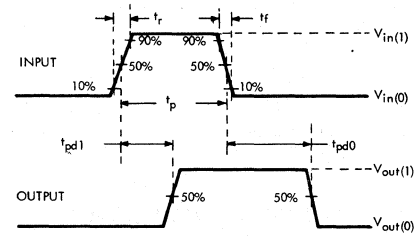
Dwg. No. A-9792A

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	2.0 V	80 V	—	—	100	μA	—
		—	Open	2.0 V	2.0 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	35	49	mA	1, 2



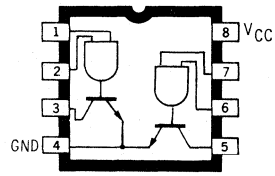
Dwg. No. A-7876D



Dwg. No. A-7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

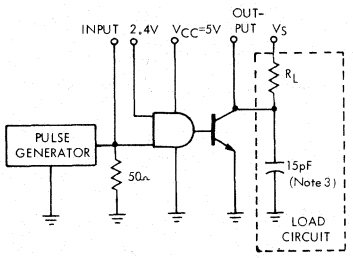
UDS-3612H
Dual NAND Driver



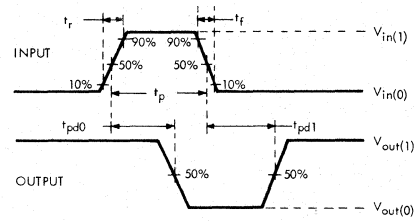
Dwg. No. A-9793A

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	80 V	—	—	100	μA	—
		—	Open	0.8 V	V_{CC}	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	53	mA	1, 2



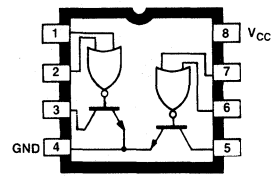
Dwg. No. A-9638



Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

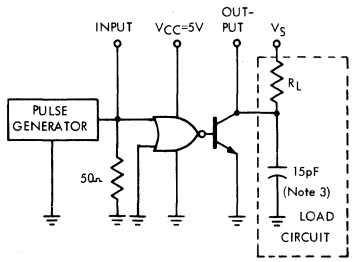
UDS-3613H
Dual OR Driver



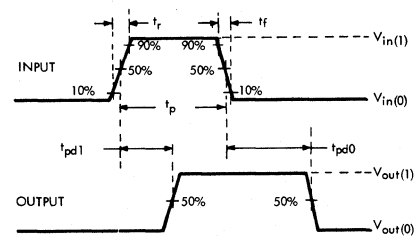
Dwg. No. A-9795A

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	36	50	mA	1, 2



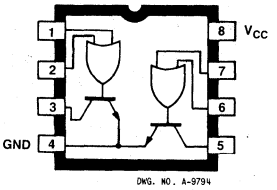
Dwg. No. A-7877B



Dwg. No. A-7628C

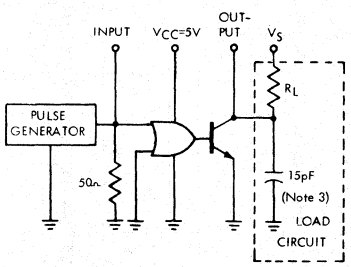
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

UDS-3614H
Dual NOR Driver

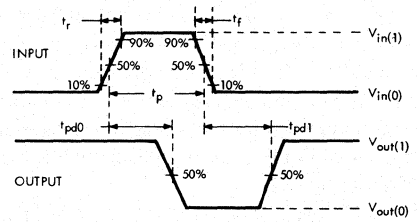


ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	0.8 V	80 V	—	—	100	μA	—
		—	Open	0.8 V	0.8 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	50	mA	1, 2



Dwg. No. A-9942



Dwg. No. A-7900A

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

UCS-4401H AND UCS-4801H
HERMETIC BiMOS LATCHED DRIVERS
MIL-STD-883 Compliant

FEATURES

- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- High-Reliability Screening to MIL-STD-883, Class B

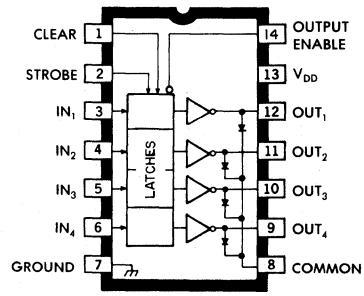
HIGH-VOLTAGE, HIGH-CURRENT interface for military, aerospace and related applications is supplied by these latched drivers. Type UCS-4401H contains four pairs of latches and drivers; Type UCS-4801H has eight pairs of latches and drivers.

The integrated circuits' CMOS inputs work with standard CMOS, PMOS and NMOS logic levels and (with appropriate pull-up resistors) with TTL or DTL circuits. The bipolar open-collector outputs can be used with relays, solenoids, motors, LED or incandescent displays, and other high-power loads.

The output transistors can sink 500 mA and will withstand a V_{CE} of 50 V in the OFF state. Outputs can be paralleled for higher current capability. Because of limitations on package power dissipation, simultaneous operation of all drivers at maximum rated current can only be accomplished with a reduction of duty cycle.

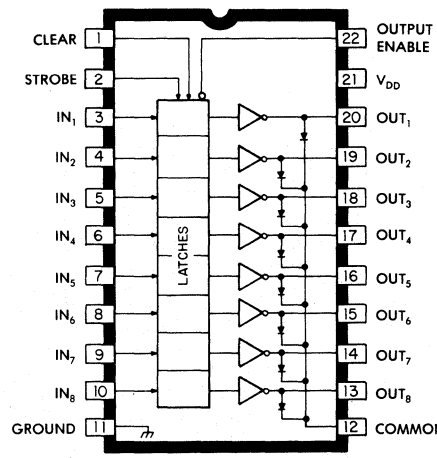
Type UCS-4401H, the four-latch device, is furnished in a standard 14-pin side-brazed hermetic package. Type UCS-4801H, the eight-latch device, is furnished in a 22-pin side-brazed hermetic package with row centers 0.400-inch (10.16 mm) apart.

Monolithic construction enables cost-effective and reliable systems design. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.



Dwg. No. A-10,499B

UCS-4401H



Dwg. No. A-10,498B

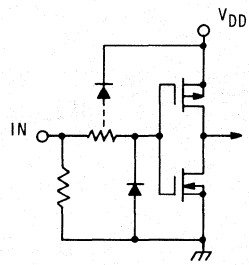
UCS-4801H

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 18 V
Input Voltage Range, V_{IN} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Continuous Collector Current, I_C . . . . . 500 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . . $-55°C$ to $+125°C$
Storage Temperature Range, T_S . . . . . $-65°C$ to $+150°C$

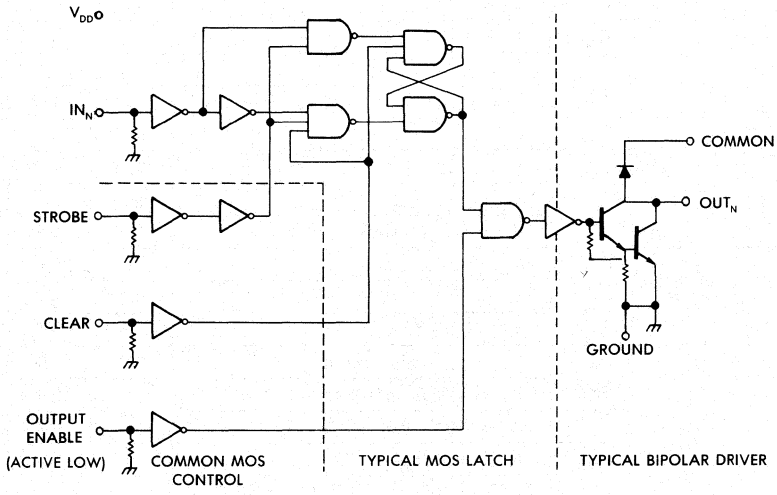
CAUTION: Sprague CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



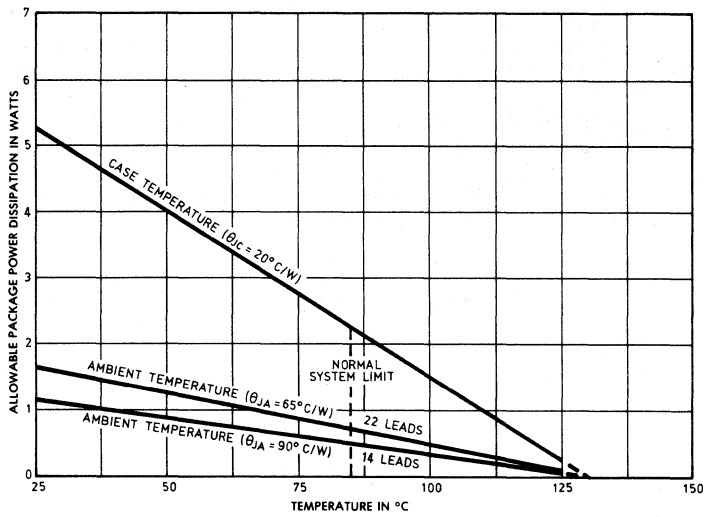
Dwg. No. A-12,520

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,495B

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,464

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 15 V	13.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 15 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	V_{DD} = 15 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	All Drivers OFF, V_{IN} = 0 V	—	50	100	µA
		All Drivers OFF, V_{IN} = 0 V, V_{DD} = 15 V	—	—	200	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\,V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\,V$	—	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\,mA$	—	—	1.3	V
		$I_C = 200\,mA$	—	—	1.5	V
		$I_C = 350\,mA$, $V_{DD} = 7.0\,V$	—	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15\,V$	14	—	—	V
		$V_{DD} = 10\,V$	9.0	—	—	V
		$V_{DD} = 5.0\,V$ (See note)	3.6	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15\,V$	35	—	—	kΩ
		$V_{DD} = 10\,V$	35	—	—	kΩ
		$V_{DD} = 5.0\,V$	35	—	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	$V_{DD} = 15\,V$, Outputs Open	—	1.0	2.5	mA
		$V_{DD} = 10\,V$, Outputs Open	—	0.9	1.9	mA
		$V_{DD} = 5.0\,V$, Outputs Open	—	0.7	1.2	mA
	$I_{DD(OFF)}$	All Drivers OFF, $V_{IN} = 0\,V$	—	50	100	μA
		All Drivers OFF, $V_{IN} = 0\,V$, $V_{DD} = 15\,V$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\,V$	—	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\,mA$	—	—	2.1	V

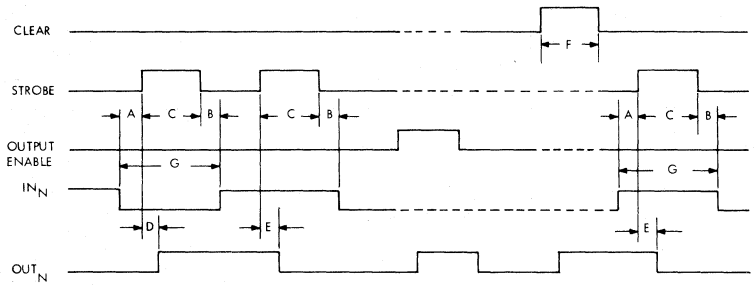
ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\,V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\,V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\,mA$*	—	—	1.3	V
		$I_C = 200\,mA$*	—	—	1.5	V
		$I_C = 350\,mA$, $V_{DD} = 7.0\,V$*	—	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15\,V$	13.5	—	—	V
		$V_{DD} = 10\,V$	8.5	—	—	V
		$V_{DD} = 5.0\,V$ (See note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15\,V$	50	—	—	kΩ
		$V_{DD} = 10\,V$	50	—	—	kΩ
		$V_{DD} = 5.0\,V$	50	—	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	$V_{DD} = 15\,V$, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10\,V$, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0\,V$, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	All Drivers OFF, $V_{IN} = 0\,V$	—	50	100	μA
		All Drivers OFF, $V_{IN} = 0\,V$, $V_{DD} = 15\,V$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\,V$	—	—	500	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\,mA$*	—	—	2.0	V

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1"
*Pulsed test.

TIMING CONDITIONS

T_A = +25°C; Logic Levels are V_{DD} and Ground



Dwg. No. A-10,895A

A. Minimum data active time before strobe enabled (data set-up time) . . . . . 100 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 100 ns
C. Minimum strobe pulse width . . . . . 300 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 500 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

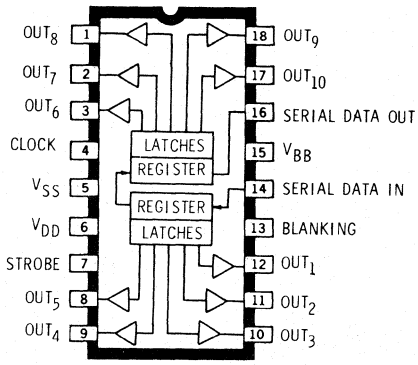
				OUT_N	
IN_N	STROBE	CLEAR	OUTPUT ENABLE	t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

UCS-4810H HERMETIC BiMOS
10-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,988

COMBINING low-power CMOS logic with bipolar source drivers, Type UCS-4810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input-logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C at a duty cycle of 61%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications in this bulletin.

Type UCS-4810H, when combined with Type UCS-4815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components. Type UCS-4801H is furnished in an 18-pin hermetic dual-in-line package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
and V_{SS} = 0 V

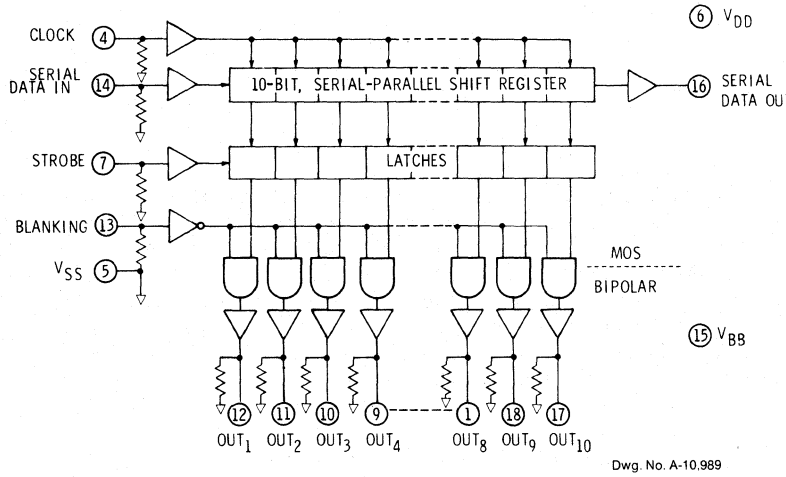
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... 1.4 W*
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at 13.3 mW/°C above +25°C.

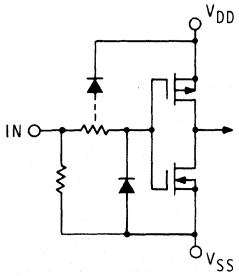
Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
10	81%	61%	34%
9	90%	68%	38%
8	98%	76%	43%
7	100%	87%	49%
6	100%	97%	57%
5	100%	100%	69%
4	100%	100%	86%
3	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM

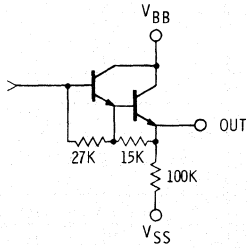


TYPICAL INPUT CIRCUIT



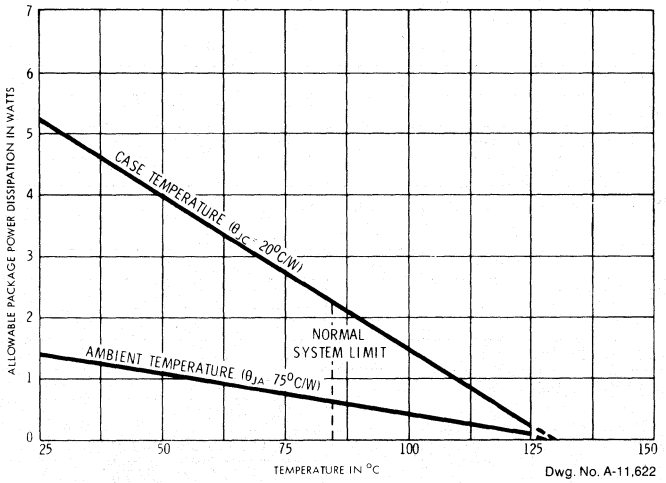
Dwg. A-12,517

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981B

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,622

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 15$ V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	μA
		$V_{DD} = V_{IN} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 15$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

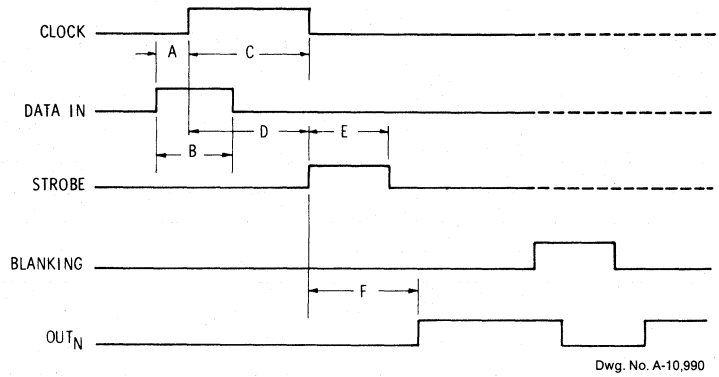
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 15$ V	14	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	μA
		$V_{DD} = V_{IN} = 15$ V	—	430	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 15$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = −25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	1400	μA
Output Leakage Current			—	−30	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 15 V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	μA
		V_{DD} = V_{IN} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	27	kΩ
		V_{DD} = 15 V	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



Dwg. No. A-10,990

TIMING CONDITIONS

T_A = +25°C; Logic Levels are V_{DD} and V_{SS}

	V_{DD} = 5.0 V	V_{DD} = 15 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

UCS-4810H TRUTH TABLE

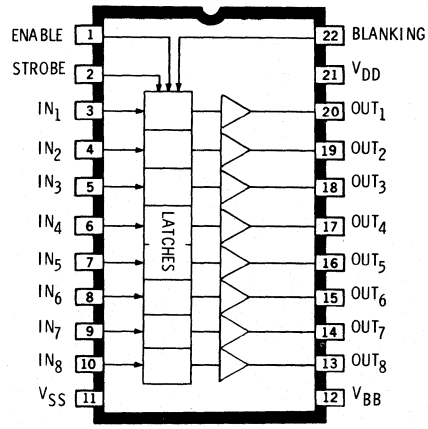
Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$	Blanking Input	Output Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$
H	⎍	H $R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
L	⎍	L $R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
X	⎍	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$	R_{10}				
		X X X ..... X X X	X	L	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$		
		$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	P_{10}	H	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	L	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$
					X X X ..... X X X	H	L L L ..... L L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCS-4815H
HERMETIC BiMOS LATCH/SOURCE DRIVER
MIL-STD-883 Compliant

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCS-4815H BiMOS integrated circuit has eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply-voltage range of 5 V to 15 V. When employed with either standard TTL or low-speed TTL, UCS-4815H may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C and a duty cycle of 89%. Other combinations of numbers of conducting outputs and duty cycle are shown in the specifications in this bulletin.

A minimum component display subsystem, requiring few or no discrete components, may be assembled by using a UCS-4815H BiMOS latch/source driver with a UCS-4810H serial-to-parallel latch/driver.

The UCS-4815H is furnished in 22-pin hermetic dual-in-line packages. To simplify printed wiring board layout, output pins on the package are opposite respective input pins.

Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

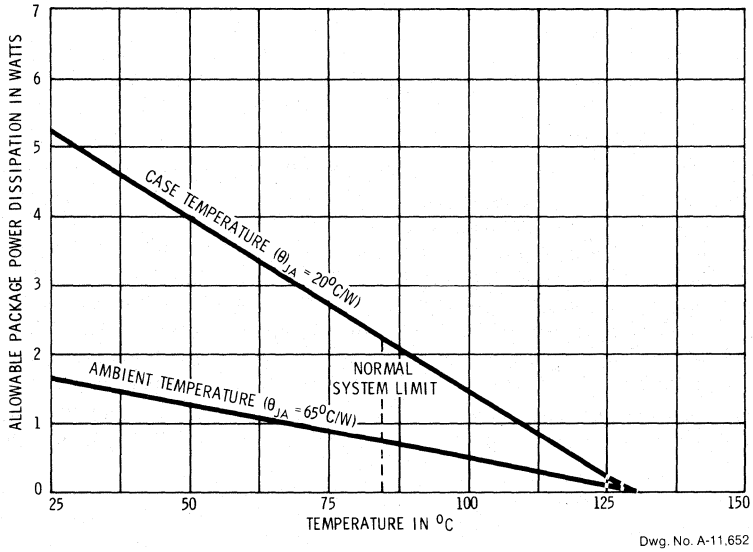
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... 1.6 W*
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at 15.4 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	100%	89%	56%
7	100%	98%	57%
6	100%	100%	66%
5	100%	100%	80%
4	100%	100%	100%

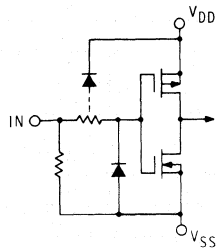
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



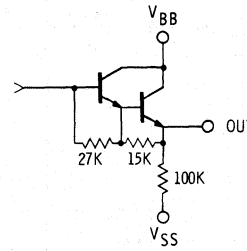
Dwg. No. A-11,652

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,517

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981B

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{ss} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 15$ V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	μA
		$V_{DD} = V_{IN} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

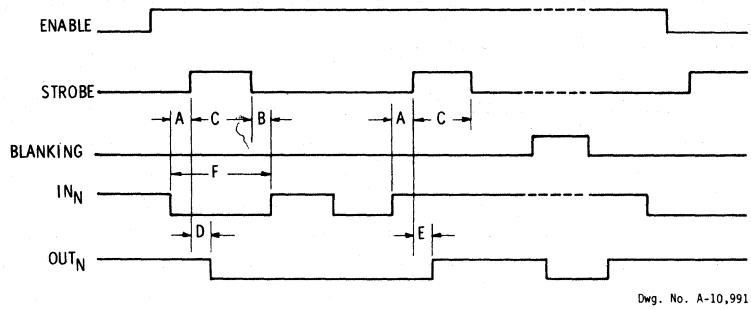
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 15$ V	14	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	μA
		$V_{DD} = V_{IN} = 15$ V	—	430	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = −25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	400	1400	μA
Output Leakage Current			—	−30	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 15 V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	μA
		V_{DD} = V_{IN} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	12	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



Dwg. No. A-10,991

TIMING CONDITIONS

T_A = +25°C; Logic Levels are V_{DD} and V_{SS}

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 100 ns
C. Typical Strobe Pulse Width For Power-Up Clear Disable ..... 500 ns
Minimum Strobe Pulse Width After Power-Up Clear Disabled ..... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition ..... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition ..... 1.0 μs
F. Minimum Data Pulse Width ..... 500 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

On first applying V_{DD} to the device, all latch outputs assume a low state (Power-Up Clear) resulting in all outputs being OFF. The latches will remain in the low condition until the Clear is disabled by a STROBE high input. Data may be entered into the latches during Power-Up Clear disable if the ENABLE input is also high.

UCS-4815H TRUTH TABLE

Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

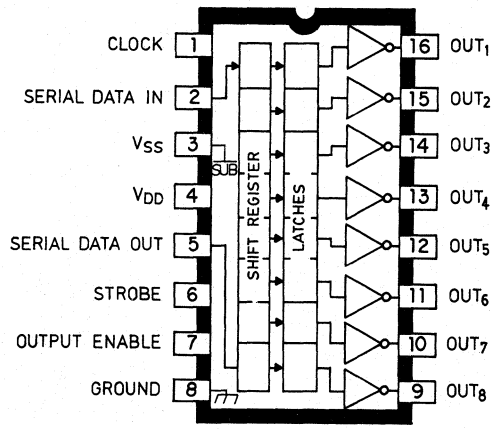
X = irrelevant
T-1 = previous output state
T = present output state

SERIES UCS-4820H HERMETIC BiMOS 8-BIT, SERIAL-INPUT, LATCHED DRIVERS

MIL-STD-883 Compliant

FEATURES

- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B



Dwg. No. A-11,388B

INTENDED FOR MILITARY, aerospace, and related applications, Series UCS-4820H 8-bit, serial-input, latched drivers combine bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays. Except for the maximum allowable driver output-voltage ratings, Types UCS-4821H (50 V), UCS-4822H (80 V), and UCS-4823H (100 V) are identical.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output allows cascading these devices for interface applications requiring additional drive lines.

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 50°C at a 42% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

Series UCS-4820H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, class B are standard.

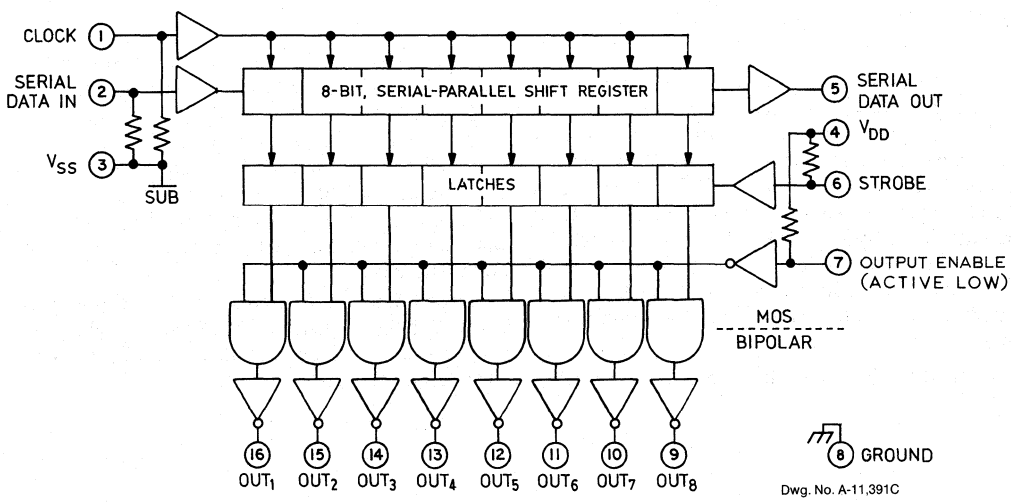
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} (UCS-4821H) ..... 50 V
(UCS-4822H) ..... 80 V
(UCS-4823H) ..... 100 V
Logic Supply Voltage, V_{DD} ..... 18 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 500 mA
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

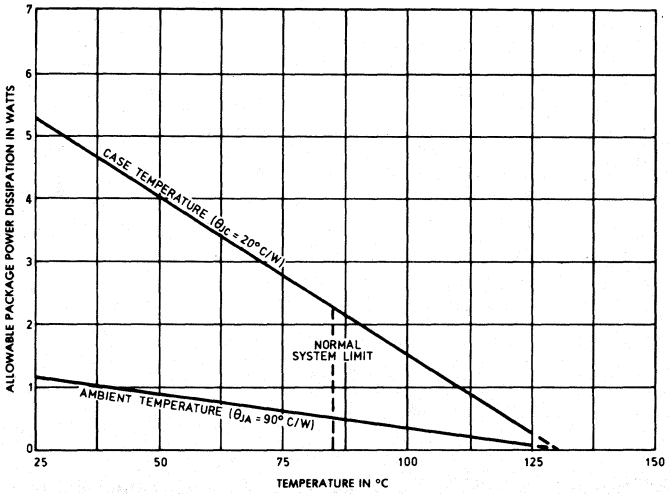
Number of Outputs ON (I_{OUT} = 200 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	50%	42%	18%
7	63%	48%	21%
6	74%	56%	25%
5	88%	67%	30%
4	100%	84%	37%
3	100%	100%	50%
2	100%	100%	75%
1	100%	100%	100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM



ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,677

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	V_{OUT} = 50 V	—	50	µA
		UCS-4822H	V_{OUT} = 80 V	—	50	µA
		UCS-4823H	V_{OUT} = 100 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA	—	1.1	V
			I_{OUT} = 200 mA	—	1.3	V
			I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 15 V	13.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 15 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, V_{STROBE} = V_{DD} = 15 V	—	2.0	mA
			One driver ON, V_{STROBE} = V_{DD} = 10 V	—	1.7	mA
			One driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	1.0	mA
	$I_{DD(OFF)}$	ALL	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	100	µA
			V_{ENABLE} = V_{STROBE} = V_{DD} = 15 V	—	200	µA

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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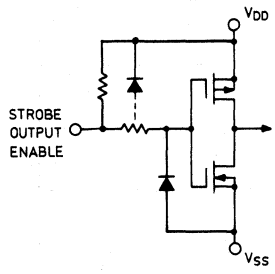
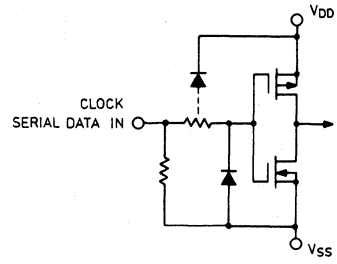
TYPICAL INPUT CIRCUITS



Dwg. No. A-12,658



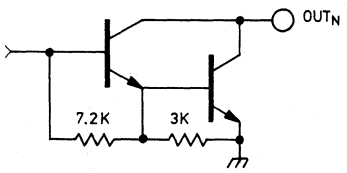
Dwg. No. A-12,659

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$, $V_{SS} = 0\ V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	$V_{OUT} = 50\ V$	—	50	µA
		UCS-4822H	$V_{OUT} = 80\ V$	—	50	µA
		UCS-4823H	$V_{OUT} = 100\ V$	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\ mA$	—	1.3	V
			$I_{OUT} = 200\ mA$	—	1.5	V
			$I_{OUT} = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15\ V$	14	—	V
			$V_{DD} = 10\ V$	9.0	—	V
			$V_{DD} = 5.0\ V$ (See Note)	3.6	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15\ V$	35	—	kΩ
			$V_{DD} = 10\ V$	35	—	kΩ
			$V_{DD} = 5.0\ V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, $V_{STROBE} = V_{DD} = 15\ V$	—	2.5	mA
			One driver ON, $V_{STROBE} = V_{DD} = 10\ V$	—	1.9	mA
			One driver ON, $V_{STROBE} = V_{DD} = 5.0\ V$	—	1.2	mA
	$I_{DD(OFF)}$	ALL	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\ V$	—	100	µA
			$V_{ENABLE} = V_{STROBE} = V_{DD} = 15\ V$	—	200	µA

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

TYPICAL OUTPUT DRIVER



Dwg. No. A-11,390A

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Limits Units
Output Leakage Current	I_{CEX}	UCS-4821H	V_{OUT} = 50 V	—	500	µA
		UCS-4822H	V_{OUT} = 80 V	—	500	µA
		UCS-4823H	V_{OUT} = 100 V	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	I_{OUT} = 100 mA*	—	1.3	V
			I_{OUT} = 200 mA*	—	1.5	V
			I_{OUT} = 350 mA*, V_{DD} = 7.0 V	—	1.8	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	V_{DD} = 15 V	13.5	—	V
			V_{DD} = 10 V	8.5	—	V
			V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	ALL	V_{DD} = 15 V	50	—	kΩ
			V_{DD} = 10 V	50	—	kΩ
			V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, V_{STROBE} = V_{DD} = 15 V	—	2.0	mA
			One driver ON, V_{STROBE} = V_{DD} = 10 V	—	1.7	mA
			One driver ON, V_{STROBE} = V_{DD} = 5.0 V	—	1.0	mA
	$I_{DD(OFF)}$	ALL	V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0 V	—	100	µA
			V_{ENABLE} = V_{STROBE} = V_{DD} = 15 V	—	200	µA

*Pulsed test.
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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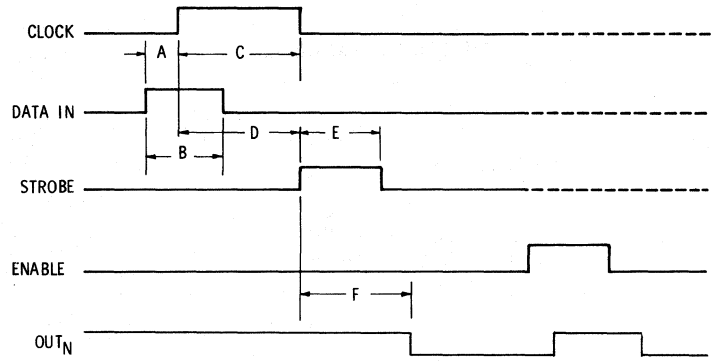


Dwg. No. A-10,990B

TIMING CONDITIONS

(T_A = +25°C; Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V	V_{DD} = 15 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

SERIES UCS-4820H TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_8$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_8$	Output Enable	Output Contents $I_1\ I_2\ I_3 \ldots I_8$
H	⎍	$H\ R_1\ R_2 \ldots R_7$	R_7				
L	⎍	$L\ R_1\ R_2 \ldots R_7$	R_7				
X	⎍	$R_1\ R_2\ R_3 \ldots R_8$	R_8				
		X X X ... X	X	L	$R_1\ R_2\ R_3 \ldots R_8$		
		$P_1\ P_2\ P_3 \ldots P_8$	P_8	H	$P_1\ P_2\ P_3 \ldots P_8$	L	$P_1\ P_2\ P_3 \ldots P_8$
					X X X ... X	H	H H H ... H

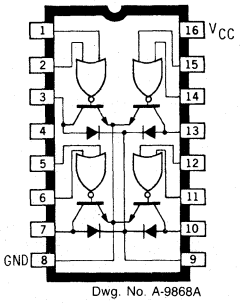
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

SERIES UDS-5700H QUAD 2-INPUT PERIPHERAL/POWER DRIVERS

MIL-STD-883 Compliant

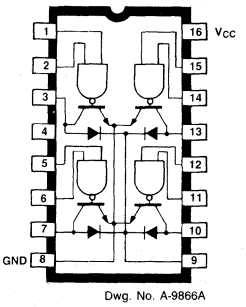
FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Hermetically Sealed Package to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B



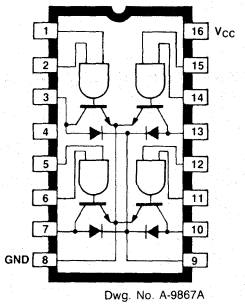
Dwg. No. A-9868A

UDS-5703H



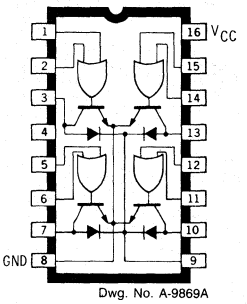
Dwg. No. A-9866A

UDS-5706H



Dwg. No. A-9867A

UDS-5707H



Dwg. No. A-9869A

UDS-5733H

THESE 16-LEAD QUAD 2-input peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, and NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 150 mA continuously at an ambient temperature of +70°C. In the OFF state, these drivers will withstand at least 80 V. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

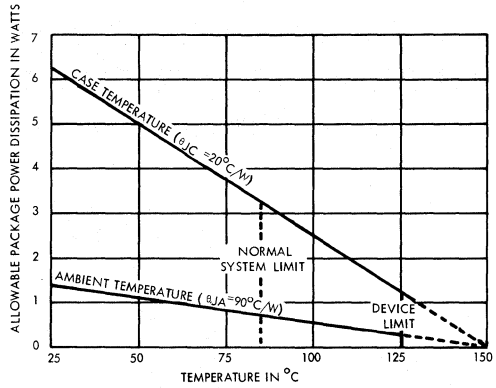
The Series UDS-5700H quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. For non-inductive loads, the diode common bus can be used as a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	80 V
Output On-State Sink Current, I_{ON}	600 mA
Suppression Diode Off-State Voltage, V_{OFF}	80 V
Suppression Diode On-State Current, I_{ON}	600 mA
Power Dissipation, P_D	1.0 W
Package Power Dissipation, P_D	See Graph
Ambient Temperature Range (operating), T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,198A

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

		Test Conditions			Limits				
Characteristic	Symbol	V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{IN(1)}$	Min.	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	Min.	—	—	—	—	0.8	V	—
"0" Input Current	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−50	−100	μA	2
"1" Input Current	$I_{IN(1)}$	Max.	30 V	0 V	—	—	10	μA	2
Input Clamp Voltage	V_I	Min.	−12 mA	—	—	—	−1.5	V	—

SWITCHING CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 5.0$ V

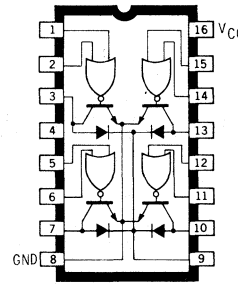
			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	$V_S = 70$ V, $R_L = 465\ \Omega$ (10 Watts) $C_L = 15$ pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	$V_S = 70$ V, $R_L = 465\ \Omega$ (10 Watts) $C_L = 15$ pF	—	300	750	ns	3

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{IN(0)} = 0$ V	$t_r \leq 7$ ns	$t_p = 1\ \mu s$
$V_{IN(1)} = 3.5$ V	$t_r \leq 14$ ns	PRR = 500 kHz

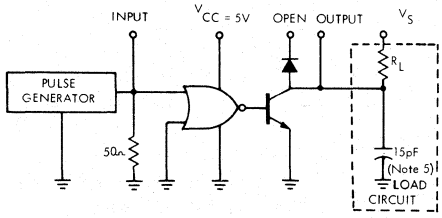
UDS-5703H QUAD OR DRIVER



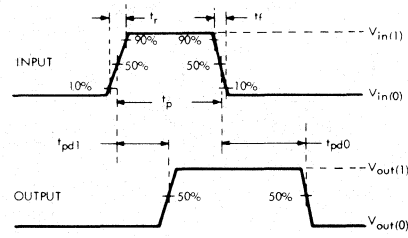
Dwg. No. A-9869A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	0 V	80 V	—	—	100	μA	—
		—	Open	2.0 V	0 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	μA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	72	100	mA	1, 2



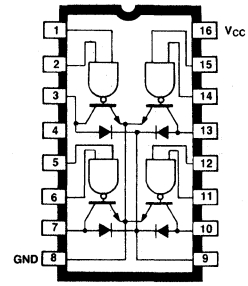
Dwg. No. A-9123A



Dwg. No. A-7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

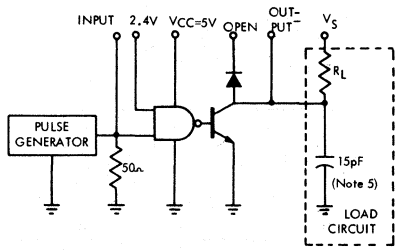
UDS-5706H QUAD AND DRIVER



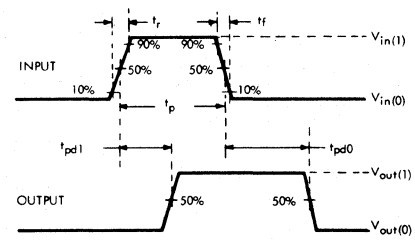
Dwg. No. A-9866A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	2.0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	2.0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	70	98	mA	1, 2



Dwg. No. A-7878A

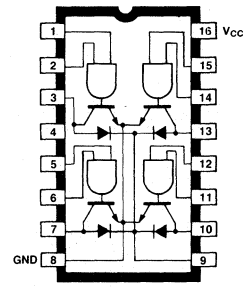


Dwg. No. A-7628C

NOTES:

1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Diode leakage current measured at $V_R = 80$ V.
4. Diode forward voltage drop measured at $I_f = 300$ mA.
5. Capacitance values specified include probe and test fixture capacitance.

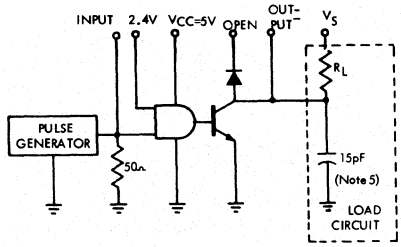
UDS-5707H QUAD NAND DRIVER



Dwg. No. A-9867A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	80 V	—	—	100	μA	—
		—	Open	0.8 V	V_{CC}	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	μA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	80	106	mA	1, 2



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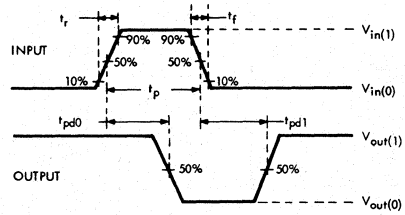
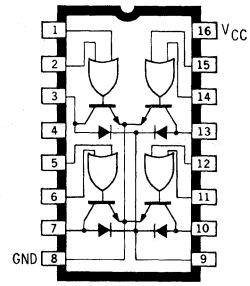


Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

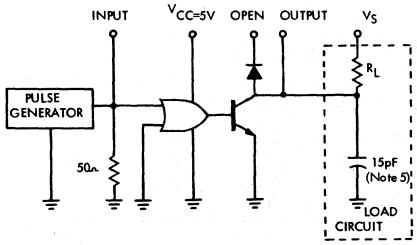
UDS-5733H QUAD NOR DRIVER



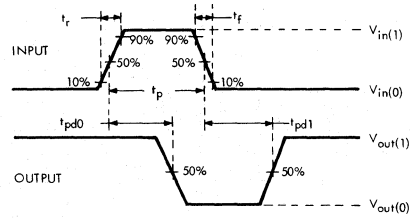
Dwg. No. A-9868A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	0.8 V	80 V	—	—	100	μA	—
		—	Open	0.8 V	0.8 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	μA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	80	100	mA	1, 2



Dwg. No. A-9135A



Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = 80 V.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDS-5710H
DUAL PERIPHERAL/POWER DRIVERS

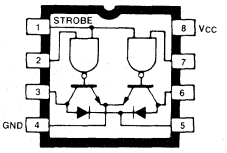
FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Standoff Voltage of 80 V
- Transient Protected Outputs
- High-Reliability Screening

THESE DUAL peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 200 mA continuously at ambient temperatures of up to +85°C. In the OFF state, these drivers will withstand at least 80 V. Units are supplied in 8-pin hermetically-sealed mini-DIP packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883 are standard.

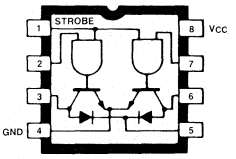
The Series UDS-5710H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to a 500 mA peak value.

The integral transient suppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode common bus can be used to perform the "lamp test" function. Similar devices with four drivers per package are the Series UDS-5700H.



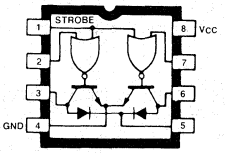
Dwg. No. A-9791B

UDS-5711H
Dual AND Driver



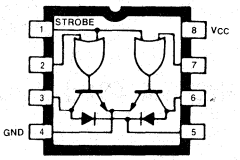
Dwg. No. A-9790B

UDS-5712H
Dual NAND Driver



Dwg. No. A-9789B

UDS-5713H
Dual OR Driver



Dwg. No. A-9788B

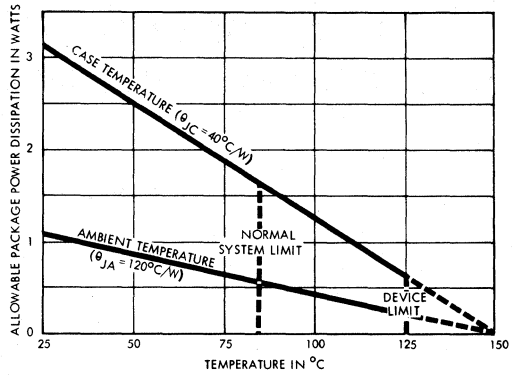
UDS-5714H
Dual NOR Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	500 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	500 mA
Power Dissipation, P_D (one output)	1.0 W
(total package)	See Graph
Ambient Temperature Range (operating), T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

These devices are NON-COMPLIANT regarding MIL-STD-883C because of package dimensions.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-10,978

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions			Limits			Units	Notes
		V_{CC}	Driven Input	Other Input	Min.	Typ.	Max.		
"1" Input Voltage	$V_{IN(1)}$	Min.		—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	Min.		—	—	—	0.8	V	—
"0" Input Current at all Inputs except Strobe	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−50	−100	μA	2
"0" Input Current at Strobe	$I_{IN(0)}$	Max.	0.4 V	30 V	—	−100	−200	μA	—
"1" Input Current at all Inputs except Strobe	$I_{IN(1)}$	Max.	30 V	0 V	—	—	10	μA	2
"1" Input Current at Strobe	$I_{IN(1)}$	Max.	30 V	0 V	—	—	20	μA	2
Input Clamp Voltage	V_I	Min.	−12 mA	—	—	—	−1.5	V	—

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

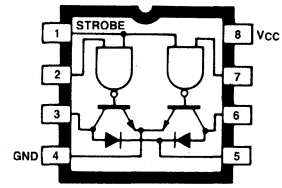
Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	T_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{IN(0)}$ = 0 V	$t_r \leq$ 7 ns	t_p = 1 μs
$V_{IN(1)}$ = 3.5 V	$t_r \leq$ 14 ns	PRR = 500 kHz

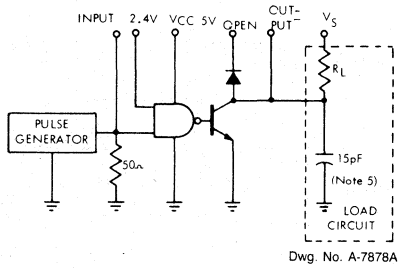
UDS-5711H DUAL AND DRIVER



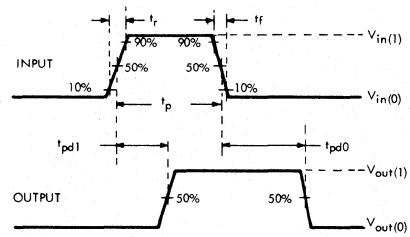
Dwg. No. A-9791B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	2.0 V	80 V	—	—	100	μA	—
		—	Open	2.0 V	2.0 V	80 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	V_{CC}	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	V_{CC}	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	μA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	35	49	mA	1, 2



Dwg. No. A-7878A

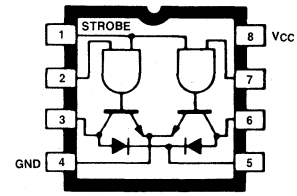


Dwg. No. A7628C

NOTES:

1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

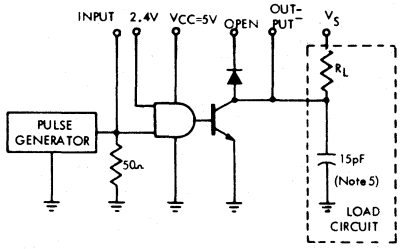
UDS-5712H DUAL NAND DRIVER



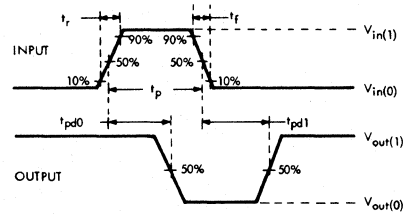
Dwg. No. A-9790B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	80 V	—	—	100	µA	—
		—	Open	0.8 V	V_{CC}	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	2.0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	53	mA	1, 2



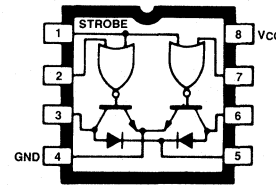
Dwg. No. A-7809A



Dwg. No. A-7900A

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

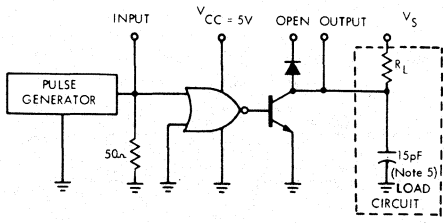
UDS-5713H DUAL OR DRIVER



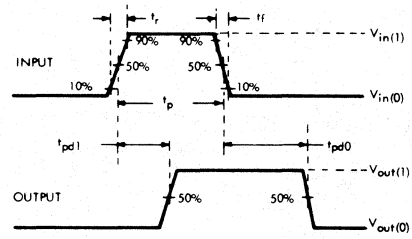
Dwg. No. A-9789B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	2.0 V	0 V	80 V	—	—	100	µA	—
		—	Open	2.0 V	0 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	0.8 V	0.8 V	150 mA	—	0.4	0.5	V	—
		—	Min.	0.8 V	0.8 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	0 V	0 V	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	V_{CC}	V_{CC}	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	5.0 V	5.0 V	—	—	8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	0 V	0 V	—	—	36	50	mA	1, 2



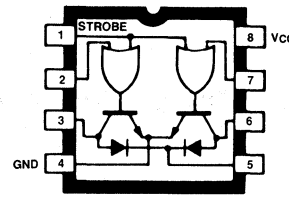
Dwg. No. A-9123A



Dwg. No. A-7628C

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

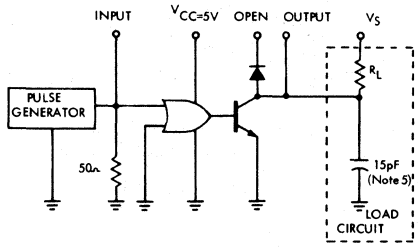
UDS-5714H DUAL NOR DRIVER



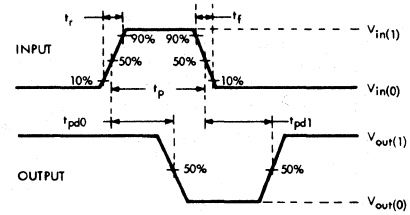
Dwg. No. A-9788B

ELECTRICAL CHARACTERISTICS over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	0.8 V	80 V	—	—	100	µA	—
		—	Open	0.8 V	0.8 V	80 V	—	—	100	µA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	0 V	150 mA	—	0.4	0.5	V	—
		—	Min.	2.0 V	0 V	300 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_{LK}	Nom.	Nom.	V_{CC}	V_{CC}	Open	—	—	200	µA	3
Diode Forward Voltage Drop	V_D	Nom.	Nom.	0 V	0 V	—	—	1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	Nom.	Max.	0 V	0 V	—	—	12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	Nom.	Max.	5.0 V	5.0 V	—	—	40	50	mA	1, 2



Dwg. No. A-9135A



Dwg. No. A-7900A

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at $I_f = 300$ mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDS-5791H
QUAD PIN DIODE POWER DRIVER
MIL-STD-883 Compliant

FEATURES

- Low Input Current
- TTL, DTL, MOS Compatible
- Wide Operating Voltage Range
- High Output Breakdown Voltage
- High-Reliability Screening to MIL-STD-883, Class B

CONSISTING of four high-voltage NPN output stages and associated logic and level shifting, this monolithic, planar integrated circuit offers an easy solution to many PIN diode driving applications.

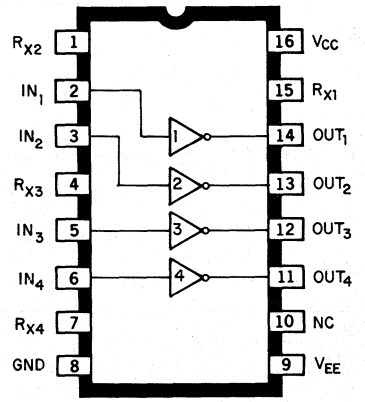
The UDS-5791H quad power driver is designed to replace discrete or hybrid PIN diode drivers. It provides significant reductions in cost and space with improved reliability. The device is capable of sustaining OFF voltages of 120 V and will switch currents to 500 mA.

The input buffer circuitry has been designed to utilize external discrete resistors. The one-resistor-per-driver effectively reduces total package power dissipation and junction temperature while allowing user selection of output base drive current, power supply voltages, and output current.

All devices are rated for operation over an extended temperature range of −55°C to +125°C. It is customarily supplied in 16-pin hermetic dual in-line packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
over free-air operating temperature range

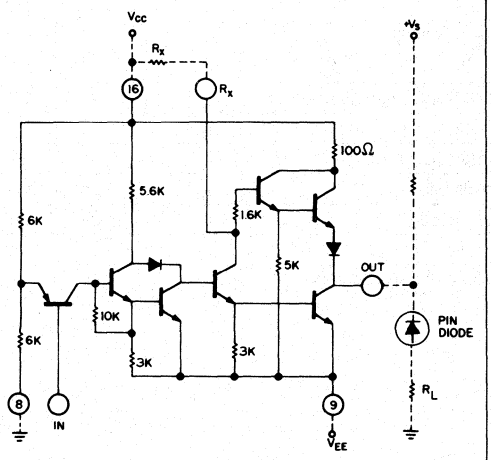
Supply Voltage, V_{CC}	+6.0 V
Supply Voltage, V_{EE}	−6.0 V
Input Voltage, V_{IN}	V_{CC}
Output OFF-State Voltage, V_{OFF} (ref. V_{EE})	+120 V
Output ON-State Current, I_{ON}	500 mA
Package Power Dissipation, P_D	See Graph
Operating Ambient Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C



Dwg. No. A-10,478

PARTIAL SCHEMATIC

ONE OF FOUR DRIVERS



Dwg. No. A-10,480

6

RECOMMENDED OPERATING CONDITIONS

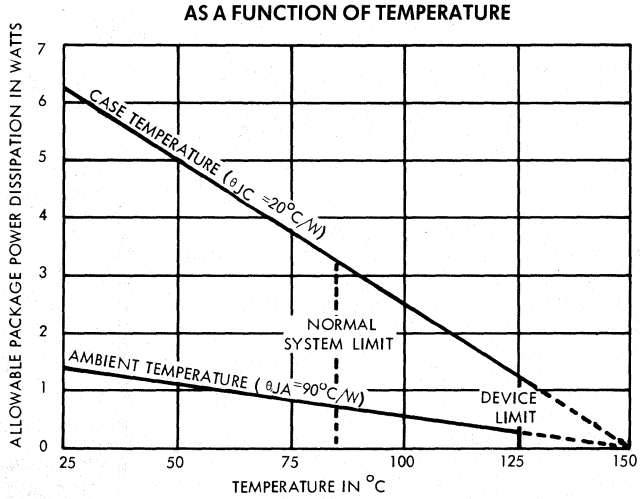
	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
Supply Voltage, V_{EE}	−1.5	−3.0	−5.5	V
Output ON-State Current, I_{ON}			300	mA
Operating Ambient Temperature Range, T_A	−55	+25	+125	°C

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp. (°C)	V_{CC} (+V)	V_{EE} (−V)	V_{IN} (+V)	V_{OFF} (+V)	or I_{ON} (mA)	R_X (Ω)	Limits Min.	Limits Max.	Units
"1" Input Voltage	$V_{IN(1)}$	—	4.5	—	—	—	—	—	2.0	4.0	V
"0" Input Voltage	$V_{IN(0)}$	—	4.5	—	—	—	—	—	—	0.8	V
"1" Input Current	$I_{IN(1)}$	—	5.5	3.0	5.0	—	—	—	—	50	μA
"0" Input Current	$I_{IN(0)}$	—	5.5	3.0	0.4	—	—	—	—	1.0	mA
OFF-State Reverse Current	I_{OFF}	+25	4.5	3.0	0.4	115	—	—	—	50	μA
		+125	4.5	3.0	0.4	115	—	—	—	100	μA
ON-State Output Voltage* (Ref. V_{EE})	V_{ON}	−55	4.5	1.5	2.4	—	150	720	—	400	mV
						—	300	360	—	600	mV
		+25	4.5	1.5	2.4	—	150	720	—	400	mV
						—	300	360	—	700	mV
		+125	4.5	1.5	2.4	—	150	720	—	500	mV
						—	300	360	—	850	mV
Predriver Collector Voltage* (Ref. V_{EE})	V_X	—	4.5	1.5	2.4	—	150	720	—	1.3	V
						—	300	360	—	1.5	V
			5.5	3.3	2.4	—	300	270	—	1.7	V
Output Short-Circuit Current*	I_{OS}	—	4.5	3.0	0.4	−2.3	—	510	20	50	mA
OFF-State Supply Current	I_{CC}	—	5.5	5.5	0.4	—	—	—	—	4.1	mA
ON-State Supply Current	I_{CC}	—	5.5	5.5	2.4	—	—	—	—	3.4	mA
Turn-On Delay	t_{on}	+25	5.0	3.0	—	—	—	510	—	500	ns
Storage Delay	t_s	+25	5.0	3.0	—	—	—	510	—	5.0	μs
Fall Time	t_f	+25	5.0	3.0	—	—	—	510	—	100	ns

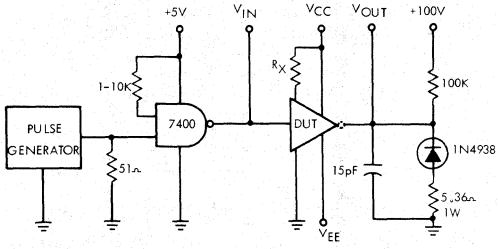
*Each output tested separately.

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

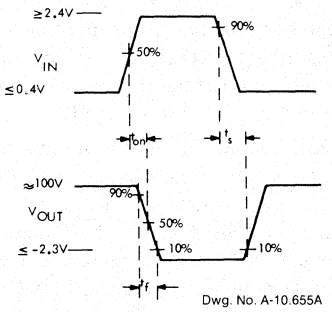


Dwg. No. A-10,198A

SWITCHING TEST CIRCUIT AND WAVEFORMS



Dwg. No. A-10.654



Dwg. No. A-10.655A

GENERAL DESIGN NOTES

$$I_{RX} = \frac{I_{ON}}{B} \qquad R_X = \frac{B(V_{CC} - V_{EE} - V_X)}{I_{ON}}$$

where:

B = 30, the minimum output current gain over the operating temperature range

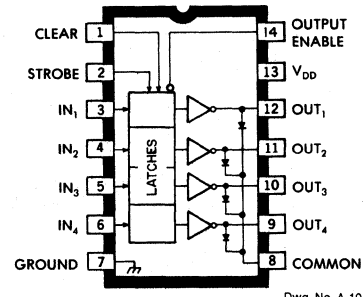
V_X = 1.5, the maximum predriver voltage

It is recommended that a minimum overdrive of 25% to be used (1.25 I_{RX} or 0.8R_X).

UCS-5800H AND UCS-5801H
HERMETIC BiMOS II LATCHED DRIVERS
MIL-STD-883 Compliant

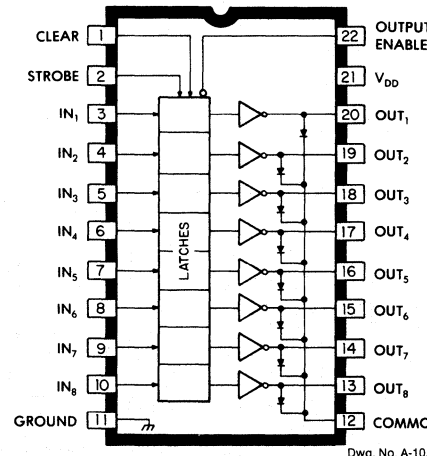
FEATURES

- 4.4 MHz Minimum Data Input Rate
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Control and Latches
- High-Voltage, High-Current Outputs
- Transient-Protected Outputs
- Operating Temperature −55°C to +125°C
- High-Reliability Screening to MIL-STD-883, Class B



Dwg. No. A-10,499B

UCS-5800H



Dwg. No. A-10,498B

UCS-5801H

SIMPLIFYING INTERFACE between LSI and peripheral power loads, the hermetically sealed UCS-5800H (4-bit) and UCS-5801H (8-bit) latched drivers combine the advantages of CMOS logic and control and high-voltage, high-current bipolar output buffers. Typical applications include microprocessor interface to relays, solenoids, dc and stepper motors, printers, LED or incandescent displays requiring hermetic packaging and an operating temperature range of −55°C to +125°C.

BiMOS II latched drivers have data input rates faster than those of the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors.

The Darlington open-collector outputs will drive power loads rated to 50 V and 350 mA (500 mA, maximum). Integral diodes for inductive load transient suppression are included. Because of limitations on package power dissipation, the simultaneous operation of all drivers at high current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load-current capability.

The 4-bit, UCS-5800H is furnished in a standard 14-pin side-brazed hermetic package. The 8-bit, UCS-5801H is supplied in a 22-pin side-brazed hermetic package with row spacing on 0.400″ (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs. Both packages conform to the dimensional requirements of MIL-M-38510. High-temperature reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B are standard.

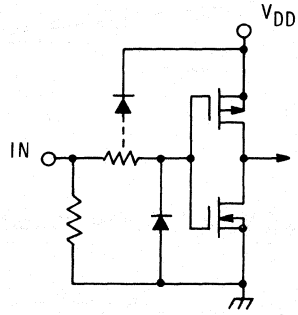
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE} . . . . . 50 V
Supply Voltage, V_{DD} . . . . . 15 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . . 500 mA
Package Power Dissipation, P_D . . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

NOTE: Output current rating may be limited by duty cycle, ambient temperature, air flow, and number of outputs conducting. Under any set of conditions, do not exceed a maximum junction temperature of +130°C.

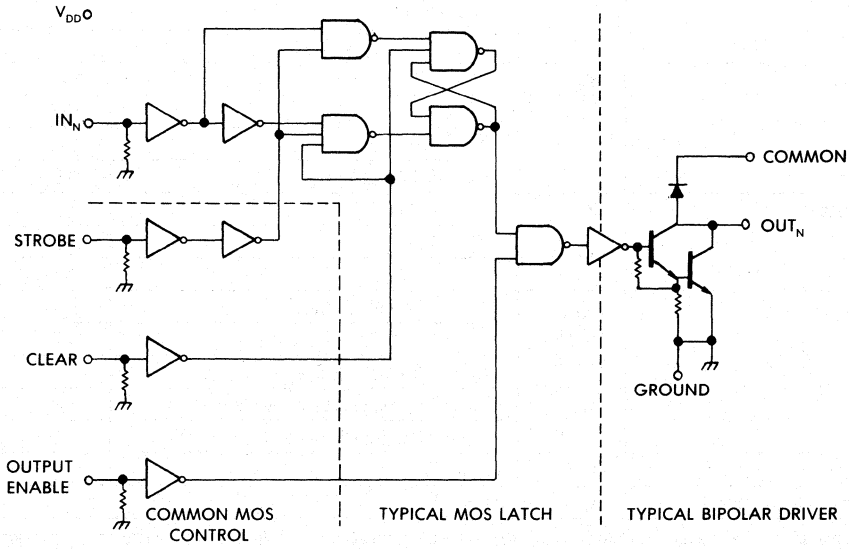
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



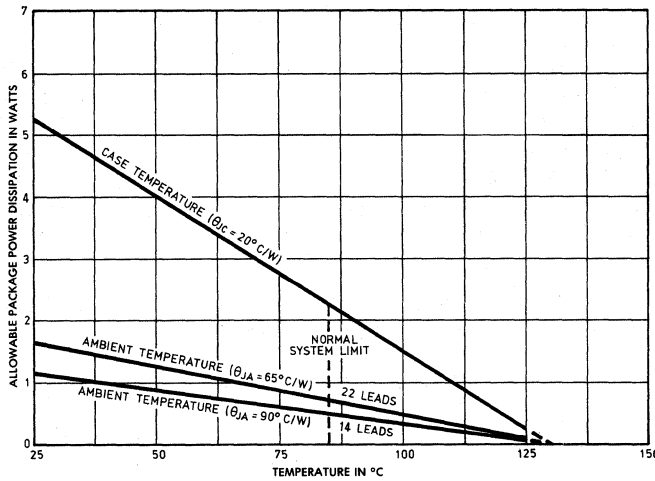
Dwg. No. A-12,520

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,495A

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,464

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V	—	50	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	1.1	V
		I_C = 200 mA	—	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 10 V	8.5	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	V
Input Resistance	R_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 10 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."

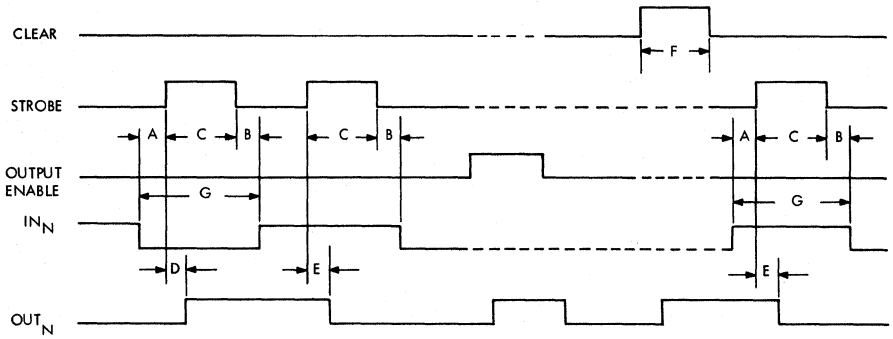
ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	1.3	V
		$I_C = 200\ mA$	—	1.5	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	11	—	V
		$V_{DD} = 10\ V$	9.0	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.6	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	35	—	kΩ
		$V_{DD} = 10\ V$	35	—	kΩ
		$V_{DD} = 5.0\ V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	2.5	mA
		$V_{DD} = 10\ V$, Outputs Open	—	1.9	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	200	μA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	2.1	V

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\ V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V$	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	1.3	V
		$I_C = 200\ mA$	—	1.5	V
		$I_C = 350\ mA$, $V_{DD} = 7.0\ V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	V
		$V_{DD} = 10\ V$	8.5	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	—	kΩ
		$V_{DD} = 10\ V$	50	—	kΩ
		$V_{DD} = 5.0\ V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	200	μA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	100	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V$	—	100	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1."



Dwg. No. A-10,895A

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and Ground)

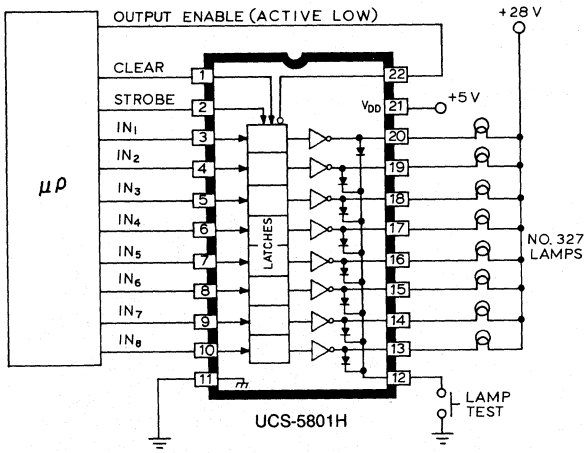
A. Minimum data active time before strobe enabled (data set-up time) . . . . . 50 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 50 ns
C. Minimum strobe pulse width . . . . . 125 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 225 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

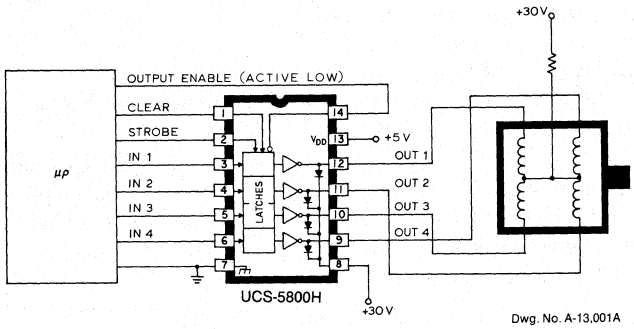


Dwg. No. A-13,000A

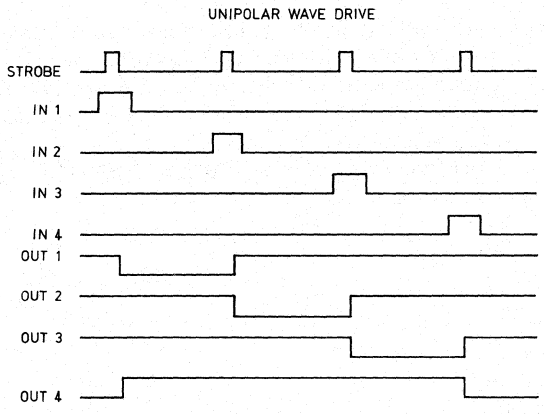
TYPICAL APPLICATIONS

INCANDESCENT LAMP DRIVER

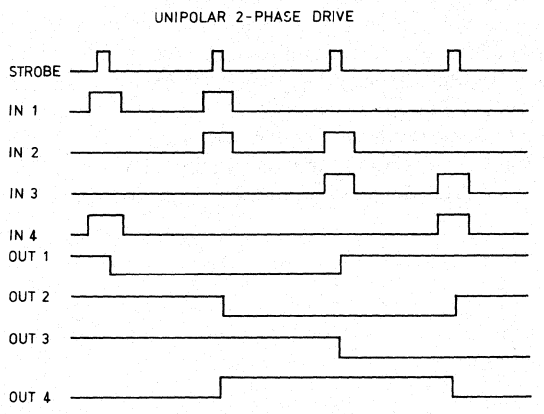
UNIPOLAR STEPPER-MOTOR DRIVE



Dwg. No. A-13,001A



Dwg. No. A-11,446



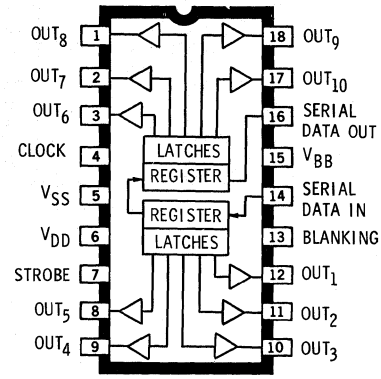
Dwg. No. A-11,447

6

UCS-5810H HERMETIC BiMOS II
10-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

FEATURES

- 5 MHz Minimum Data Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,988

COMBINING low-power CMOS logic with bipolar source drivers, Type UCS-5810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input-logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C at a duty cycle of 61%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications in this bulletin.

Type UCS-5810H, when combined with Type UCS-5815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components. Type UCS-5810H is furnished in an 18-pin hermetic dual-in-line package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

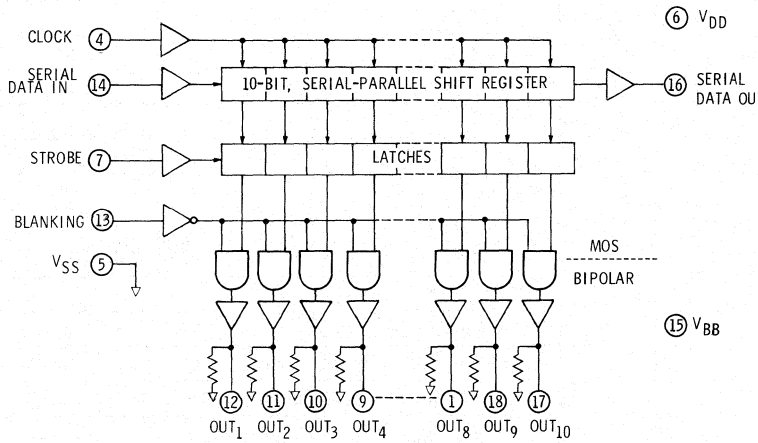
Output Voltage, V_{OUT} . . . . . 60 V
Logic Supply Voltage Range, V_{DD} . . . . . 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB} . . . . . 5.0 V to 60 V
Input Voltage Range, V_{IN} . . . . . −0.3 V to V_{DD} +0.3 V
Continuous Ouput Current, I_{OUT} . . . . . −40 mA
Package Power Dissipation, P_D . . . . . 1.4 W*
Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

*Derate at 13.3 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
10	81%	61%	34%
9	90%	68%	38%
8	98%	76%	43%
7	100%	87%	49%
6	100%	97%	57%
5	100%	100%	69%
4	100%	100%	86%
3	100%	100%	100%

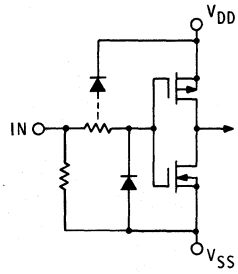
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM

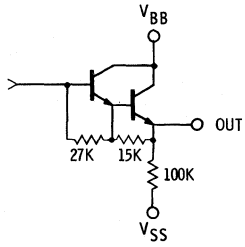


Dwg. No. A-10,989

TYPICAL INPUT CIRCUIT

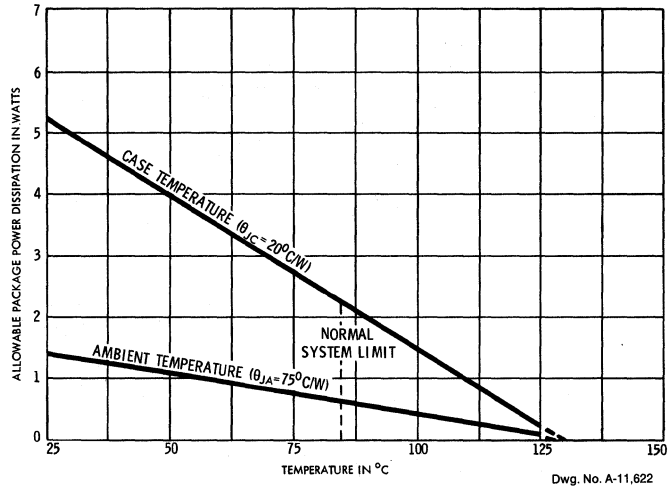


TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981B

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,622

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60\ V$, $V_{DD} = 5\ V$ to $12\ V$, $V_{SS} = 0\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25\ mA$	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\ V$	3.5	—	V
		$V_{DD} = 12\ V$	10.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\ V$	—	100	µA
		$V_{DD} = V_{IN} = 12\ V$	—	240	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\ V$	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0\ V$	—	20	kΩ
		$V_{DD} = 12\ V$	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	200	µA
	I_{DD}	$V_{DD} = 5.0\ V$, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12\ V$, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0\ V$, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12\ V$, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60\ V$, $V_{DD} = 5\ V$ to $12\ V$, $V_{SS} = 0\ V$ (unless otherwise noted)

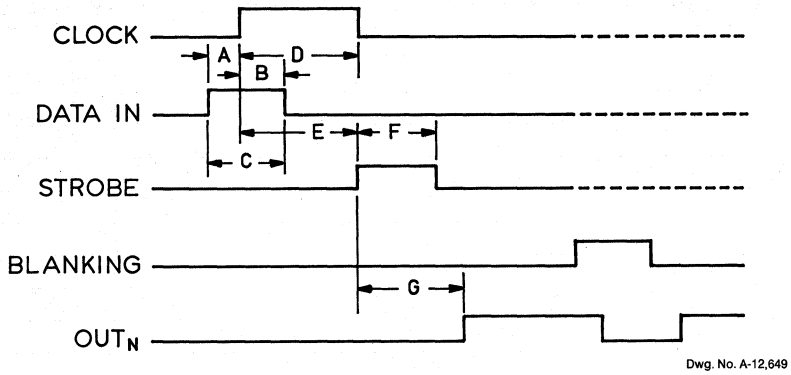
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25\ mA$	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\ V$	3.6	—	V
		$V_{DD} = 12\ V$	11.0	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\ V$	—	145	µA
		$V_{DD} = V_{IN} = 12\ V$	—	430	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\ V$	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0\ V$	—	20	kΩ
		$V_{DD} = 12\ V$	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0\ V$, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12\ V$, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0\ V$, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12\ V$, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{BB} = 60\ V$, $V_{DD} = 5\ V$ to $12\ V$, $V_{SS} = 0\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25\ mA$	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	µA
Output Leakage Current			—	−30	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\ V$	3.5	—	V
		$V_{DD} = 12\ V$	10.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\ V$	—	100	µA
		$V_{DD} = V_{IN} = 12\ V$	—	300	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\ V$	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0\ V$	—	27	kΩ
		$V_{DD} = 12\ V$	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0\ V$, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12\ V$, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0\ V$, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12\ V$, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



Dwg. No. A-12,649

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

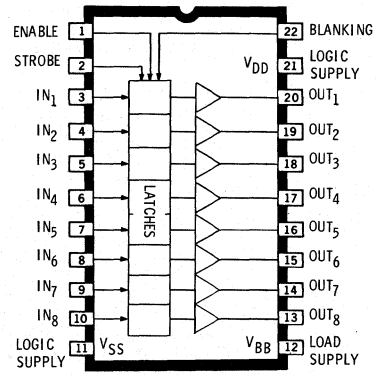
Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking Input	Output Contents
		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$			$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$		$I_1\ I_2\ I_3\ \ldots I_{N-1}\ I_N$
H		$H\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
L		$L\ R_1\ R_2\ \ldots R_{N-2} R_{N-1}$	R_{N-1}				
X		$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$	R_N				
		X X X ... X X	X	L	$R_1\ R_2\ R_3\ \ldots R_{N-1} R_N$		
		$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	P_N	H	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$	L	$P_1\ P_2\ P_3\ \ldots P_{N-1} P_N$
					X X X ... X X	H	L L L ... L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCS-5815H
HERMETIC BiMOS II LATCH/SOURCE DRIVER
MIL-STD-883 Compliant

FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C



Dwg. No. A-10,987A

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the UCS-5815H BiMos integrated circuit has eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common STROBE, BLANKING, and ENABLE functions.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 12 V. When employed with either standard TTL or low-speed TTL UCS-5815H may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C and a duty cycle of 89%. Other combinations of numbers of conducting outputs and duty cycle are shown in the specifications in this bulletin.

A minimum component display subsystem, requiring few or no discrete components, may be assembled by using a UCS-5815H BiMOS latch/source driver with a UCS-5810H serial-to-parallel latch/driver.

The UCS-5815H is furnished in 22-pin hermetic dual-in-line packages. To simplify printed wiring board layout, output pins on the package are opposite respective input pins.

Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

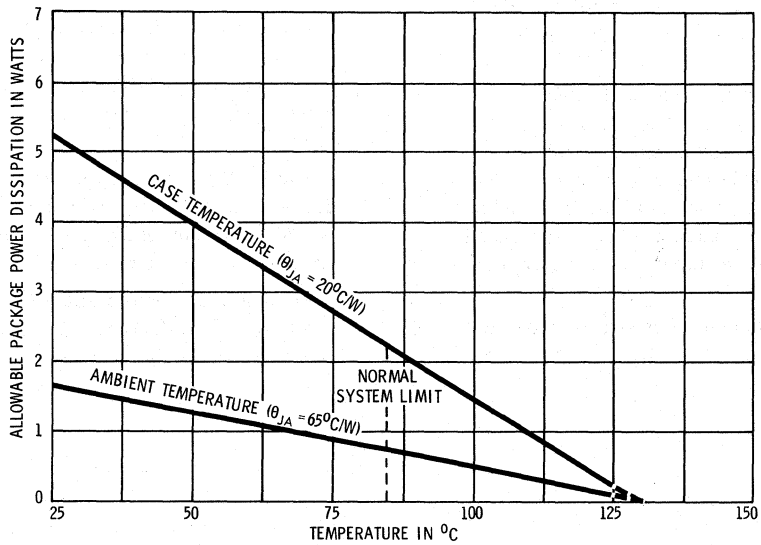
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 15 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... −40 mA
Package Power Dissipation, P_D ..... 1.6 W*
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at 15.4 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	100%	89%	56%
7	100%	98%	57%
6	100%	100%	66%
5	100%	100%	80%
4	100%	100%	100%

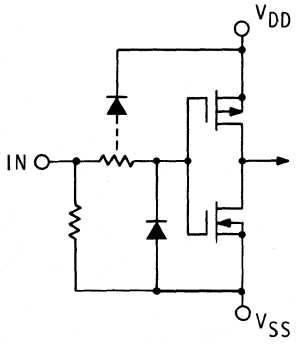
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



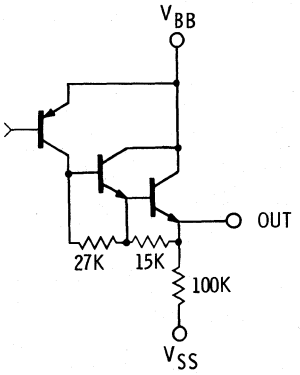
Dwg. No. A-11,652

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,517

TYPICAL OUTPUT DRIVER



Dwg. No. A-12,546

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 5$ V to 12 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 12$ V	10.5	12.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	µA
		$V_{DD} = V_{IN} = 12$ V	—	240	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, All Outputs open	—	10.5	mA
		All outputs OFF, All Outputs open	—	200	µA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12$ V, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

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ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60\,V$, $V_{DD} = 5\,V$ to $12\,V$, $V_{SS} = 0\,V$ (unless otherwise noted)

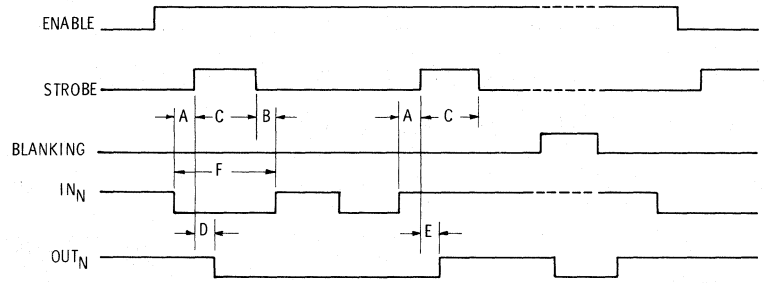
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	µA
Output Leakage Current			—	−15	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\,V$	3.6	—	V
		$V_{DD} = 12\,V$	11.0	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\,V$	—	145	µA
		$V_{DD} = V_{IN} = 12\,V$	—	430	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\,V$	35	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0\,V$, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12\,V$, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0\,V$, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12\,V$, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{BB} = 60\,V$, $V_{DD} = 5\,V$ to $12\,V$, $V_{SS} = 0\,V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	µA
Output Leakage Current			—	−30	µA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\,V$	3.5	—	V
		$V_{DD} = 12\,V$	10.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\,V$	—	100	µA
		$V_{DD} = V_{IN} = 12\,V$	—	300	µA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\,V$	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	12	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	$V_{DD} = 5.0\,V$, All outputs OFF, All inputs = 0 V	—	100	µA
		$V_{DD} = 12\,V$, All outputs OFF, All inputs = 0 V	—	200	µA
		$V_{DD} = 5.0\,V$, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 12\,V$, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.



Dwg. No. A-10,991

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	50 ns
B. Minimum Data Active time After Strobe Disabled (Data Hold Time)	50 ns
C. Minimum Strobe Pulse Width	125 ns
D. Typical Time Between Strobe Activation and Output ON to OFF Transition	500 ns
E. Typical Time Between Strobe Activation and Output OFF to ON Transition	500 ns
F. Minimum Data Pulse Width	225 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

The timing conditions shown above guarantee a 4.4 MHz, minimum data input rate (50% duty cycle) with a 5 V supply. Typically, input rates above 5 MHz are permitted. With a 12 V supply, rates in excess of 10 MHz are possible.

UCS-5815H TRUTH TABLE

Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

6

UCS-5822H HERMETIC BiMOS II
8-BIT, SERIAL-INPUT, LATCHED DRIVER
MIL-STD-883 Compliant

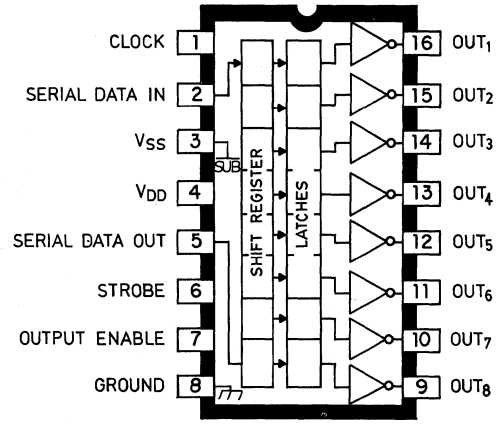
FEATURES

- 3.3 MHz Minimum Data Input Rate
- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Intended for military, aerospace, and related applications. The UCS-5822H 8-bit, serial-input, latched driver combines bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output alows cascading these devices for interface applications requiring additional drive lines.



Dwg. No. A-11,388B

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions, and without heat sinking, these devices can sustain 200 mA per output at 50°C at a 42% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

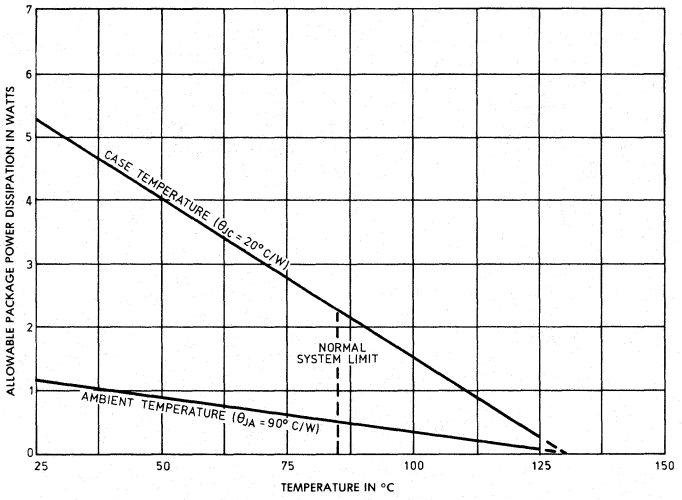
The UCS-5822H is furnished in 16-pin side-brazed dual in-line hermetic packages. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, class B are standard.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} ..... 80 V
Logic Supply Voltage, V_{DD} ..... 15 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... 500 mA
Package Power Dissipation, P_D ..... See Graph
Operating Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

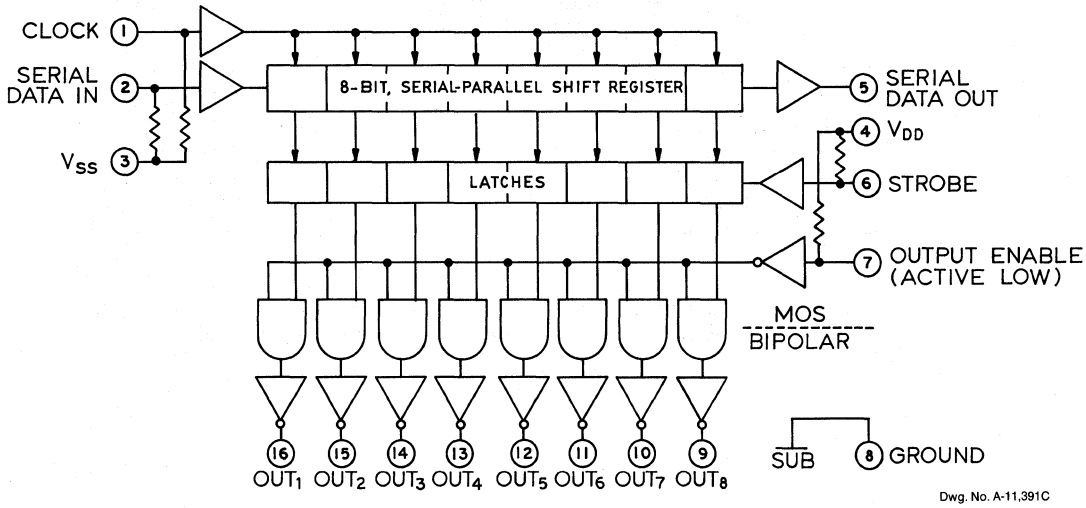
Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



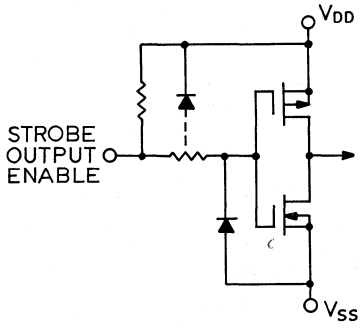
Dwg. No. A-11,677

FUNCTIONAL BLOCK DIAGRAM

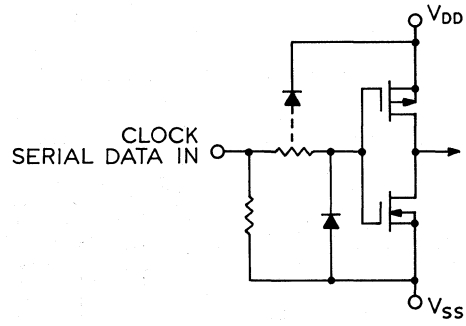


Dwg. No. A-11,391C

TYPICAL INPUT CIRCUITS

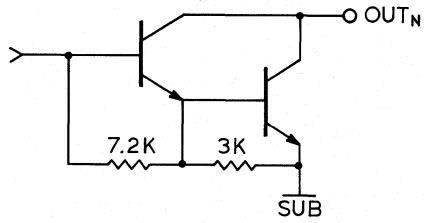


Dwg. No. A-12,658



Dwg. No. A-12,659

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,229

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\,V$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\,mA$	—	1.1	V
		$I_{OUT} = 200\,mA$	—	1.3	V
		$I_{OUT} = 350\,mA$, $V_{DD} = 7.0\,V$	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\,V$	10.5	—	V
		$V_{DD} = 5.0\,V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\,V$	50	—	kΩ
		$V_{DD} = 10\,V$	50	—	kΩ
		$V_{DD} = 5.0\,V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\,V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\,V$	—	3.9	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\,V$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\,V$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\,V$	—	2.9	mA

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

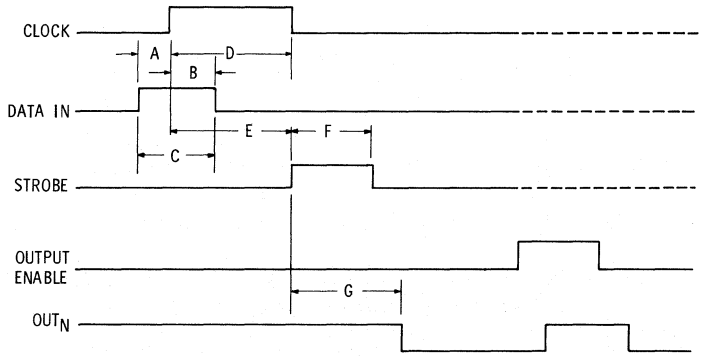
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\,V$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\,mA$	—	1.3	V
		$I_{OUT} = 200\,mA$	—	1.5	V
		$I_{OUT} = 350\,mA$, $V_{DD} = 7.0\,V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\,V$	10.5	—	V
		$V_{DD} = 5.0\,V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\,V$	35	—	kΩ
		$V_{DD} = 10\,V$	35	—	kΩ
		$V_{DD} = 5.0\,V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\,V$	—	5.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\,V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\,V$	—	3.0	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\,V$	—	2.0	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\,V$	—	3.5	mA

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\,V$	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\,mA$*	—	1.3	V
		$I_{OUT} = 200\,mA$*	—	1.5	V
		$I_{OUT} = 350\,mA$*, $V_{DD} = 7.0\,V$	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\,V$	10.5	—	V
		$V_{DD} = 5.0\,V$ (See Note)	3.5	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\,V$	50	—	kΩ
		$V_{DD} = 10\,V$	50	—	kΩ
		$V_{DD} = 5.0\,V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One driver ON, $V_{STROBE} = V_{DD} = 12\,V$	—	4.5	mA
		One driver ON, $V_{STROBE} = V_{DD} = 10\,V$	—	3.9	mA
		One driver ON, $V_{STROBE} = V_{DD} = 5.0\,V$	—	2.4	mA
	$I_{DD(OFF)}$	$V_{ENABLE} = V_{STROBE} = V_{DD} = 5.0\,V$	—	1.6	mA
		$V_{ENABLE} = V_{STROBE} = V_{DD} = 12\,V$	—	2.9	mA

*Pulsed test.
NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

Number of Outputs ON ($I_{OUT} = 200\,mA$)	Max. Allowable Duty Cycle at $V_{DD} = 5\,V$ and T_A of:		
	+25°C	+50°C	+85°C
8	50%	42%	18%
7	63%	48%	21%
6	74%	56%	25%
5	88%	67%	30%
4	100%	84%	37%
3	100%	100%	50%
2	100%	100%	75%
1	100%	100%	100%



Dwg. No. A-12,627

TIMING CONDITIONS

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS})

	V_{DD} = 5.0 V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	1.0 µs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

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UCS-5822H TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H		H R_1 R_2 ..... R_7	R_7				
L		L R_1 R_2 ..... R_7	R_7				
X		R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

MIL-STD-883 CLASS B HIGH-RELIABILITY SCREENING

All full-temperature hermetic devices are produced on a production line that is JAN Class B certified and are processed to the production screen inspections and tests in accordance with the latest requirements of MIL-STD-883. Applicable devices are marked to indicate compliance to the latest revision (at time of manufacture) of MIL-STD-883. For example: UCS5822H-883.

100% Production and High Reliability Screen Tests MIL-STD-883, Method 5004, Class B

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Temperature Cycle	1010, Cond. C	—
Constant Acceleration	2001, Cond. E	30,000 Gs, Y1 Plane
Interim Electrical	5005, Gp A, Subgp. 1	25°C per Specification
Burn-In	1015, Cond. A.	125°C, 160 Hrs or 150°C, 80 Hrs
Static Electrical	5005, Gp A, Subgp. 1	25°C per Specification
	5005, Gp A, Subgp. 2 & 3	−55°C & +125°C per Specification
Dynamic & Functional Electrical	5005, Gp A, Subgp. 4, 7 & 9	25°C per Specification
Fine Seal	1014, Cond. A_1	5×10^{-8} atm × cm³/s Max.
Gross Seal	1014, Cond. C	—
Marking	—	Sprague logo and part number, date code, lot identification, and ESD warning symbol when applicable.
External Visual	2009	—

Quality Conformance Inspection MIL-STD-883, Method 5005, Class B

Test	MIL-STD-883 Test Method	Description
Group A, Subgp. 1-4, 7 & 9	5005, Table I	Each Inspection Lot
Group B	5005, Table II	Alternate Gp. B on Weekly Basis
Group C	5005, Table III	End Points, Gp. A, Subgp. 1, as required
Group D	5005, Table IV	End Points, Gp. A, Subgp. 1, as required

NOTE: Devices using an 8-leaded side-brazed package are NON-COMPLIANT regarding MIL-STD-883. Military specification MIL-M-38510, case outline D-4, configuration 3 defines the package length as 0.405" (10.29 mm) maximum. Sprague Electric packages are 0.528" (13.41 mm) maximum. These devices (Series UDS-3610H and UDS-5710H) are therefore marked to indicate conformance only to MIL-STD-883B. For example: UDS-3611H-MIL.

BiMOS II POWER DRIVERS TO MIL-STD-883

BiMOS monolithic smart power drivers combine CMOS logic and control functions with bipolar and/or DMOS power drivers. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL, LSTTL, or DTL circuits may require appropriate pull-up resistors to ensure a logic high. The power driver outputs are used with VF, LED, and incandescent displays, dc and stepper motors, relays, solenoids, and thermal or electrosensitive print heads. With BiMOS integrated circuit, reliable, single-chip solutions are provided for a wide variety of peripheral power interface problems.

The high-current and high-voltage BiMOS drivers shown here are processed to MIL-STD-883. They furnish a higher level of interface flexibility and versatility for military, aerospace, avionics, than is provided with standard logic or discrete power drivers. They are supplied in ceramic/metal side-brazed hermetic packages (Sprague suffix letter 'H'). All devices are rated for operation over the full military temperature range of −55°C to +125°C.

8-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED DRIVERS

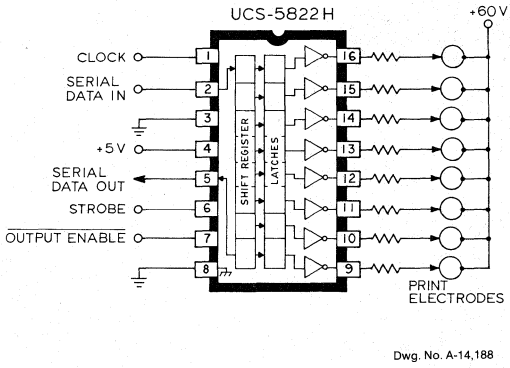
The UCS-5822H and UCS-5842H BiMOS 8-Bit Serial-In/Parallel-Out Latched Drivers augment the original UCS-4401H and UCS-4801H devices. Both of the devices contain an octal shift register, octal latch, and octal high-current, open-collector Darlington outputs. They improve systems designs through a reduced package count and a reduction in I/O line requirements. By using the serial data output, the drivers can be cascaded for interface applications requiring more than eight drive lines.

The bipolar outputs are suitable for a variety of peripheral loads, including incandescent lamps, LEDs, and thermal or electrosensitive printers. The UCS-5842H is recommended for relays, solenoids, and other high-power inductive loads.

RECOMMENDED MAX. OPERATING CONDITIONS

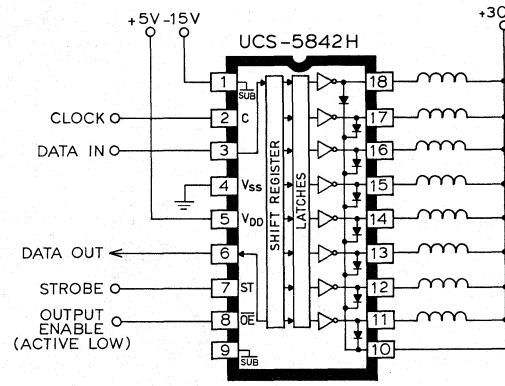
Output Sustaining Voltage (UCS-5842H)	50 V
Output Voltage	75 V
Logic Supply Voltage	12 V
Continuous Output Current	350 mA

ELECTROSENSITIVE PRINTER



Dwg. No. A-14,188

RELAY/SOLENOID DRIVER



Dwg. No. A-14,266

10-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED SOURCE DRIVER

The UCS-5810H BiMOS 10-Bit Serial-In/Parallel-Out Latched Source Driver is primarily designed as interface between logic circuitry and vacuum-fluorescent displays but may also be used with LED displays or thermal printers within its output limitations of 60 V and −40 mA per driver.

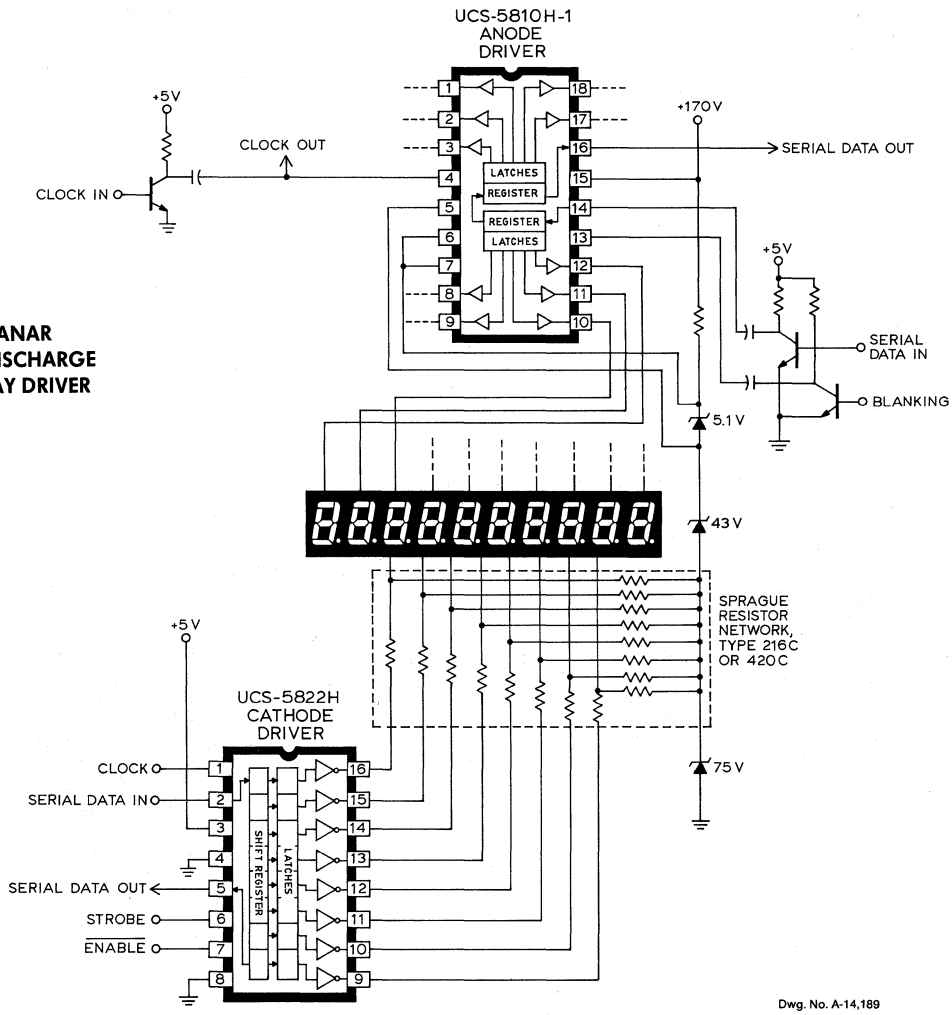
The CMOS shift register and latches will operate over a wide supply-voltage range and is compatible with standard MOS logic families. When used with TTL or low-speed TTL, pull-up resistors may be needed to ensure an input-logic high.

The 10 high-voltage outputs are used to switch the anodes (segments or dots) and/or grids (character or digit) of typical vacuum-fluorescent panels.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage ..... 55 V
Logic Supply Voltage Range..... 5.0 V to 12 V
Continuous Output Current ..... −25 mA

PLANAR GAS-DISCHARGE DISPLAY DRIVER



Dwg. No. A-14,189

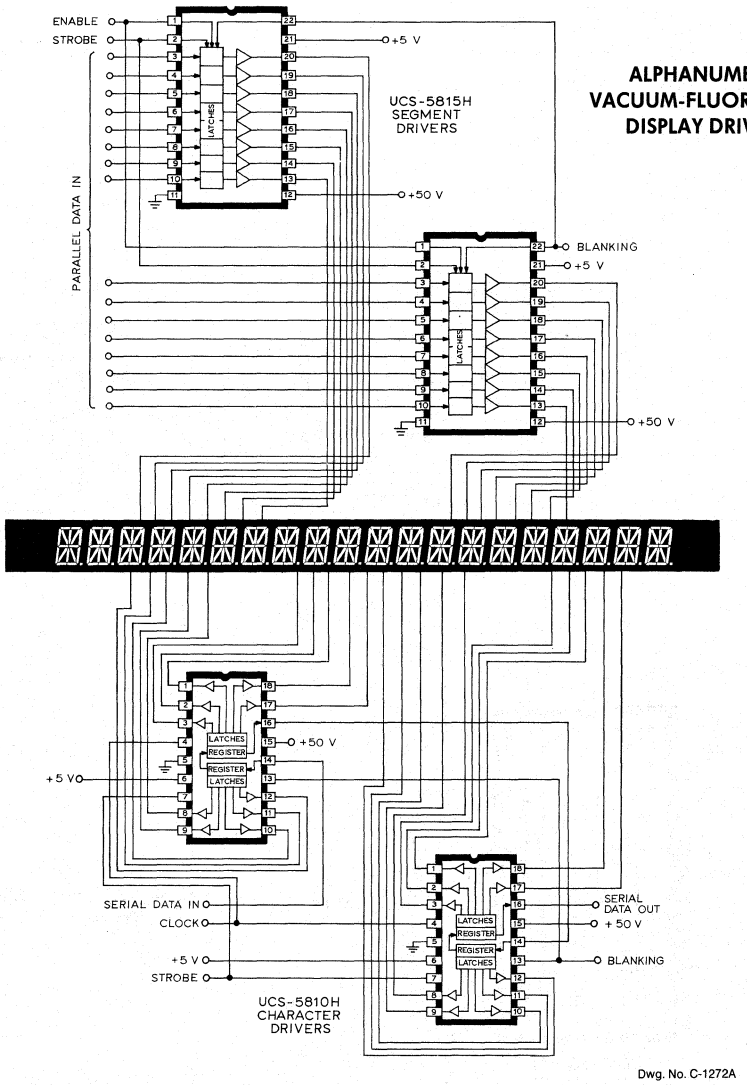
8-BIT LATCHED SOURCE DRIVER

The UCS-5815H BiMOS 8-Bit Latched Source Driver is designed primarily for use with high-voltage vacuum-fluorescent displays. It contains an 8-bit type D latch and eight source outputs with pull-down resistors, a common strobe, blanking, and enable functions.

The eight high-voltage outputs are generally used to drive the segments, dots (matrix panel), bars, or digits of vacuum-fluorescent displays. Type UCS-5815H is often used in combination with the Type UCS-5810H 10-Bit Serial Input, Latched Driver.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	55 V
Logic Supply Voltage Range	5.0 V to 12 V
Continuous Output Current	−25 mA



Dwg. No. C-1272A

4- AND 8-BIT LATCHED DRIVERS

The UCS-5800H and UCS-5801H are evolutionary improvements to the original BiMOS integrated circuits. They are used successfully in many applications. These high-voltage, high-current latched drivers have four or eight MOS data latches, a bipolar driver for each latch, and MOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Type UCS-5800H contains four latched drivers while Type UCS-5801H contains eight latched drivers.

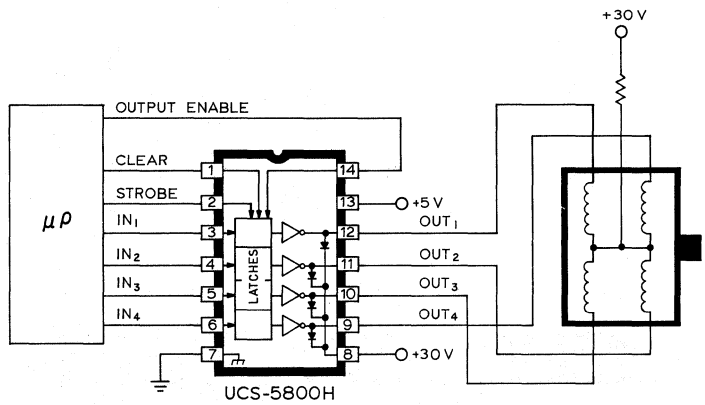
Each of the open-collector Darlington outputs can sink up to 500 mA and will sustain at least 50 V in the OFF state. Internal diodes suppress transients and allow these devices to be used with inductive loads. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current, and usually dictate either a reduction in output current or a suitable combination of duty cycle and number of active outputs.

The UCS-5800H is supplied in a standard 14-lead side-brazed hermetic package. The UCS-5801H is furnished in a 22-lead side-brazed hermetic package with lead centers on 0.400-inch spacing.

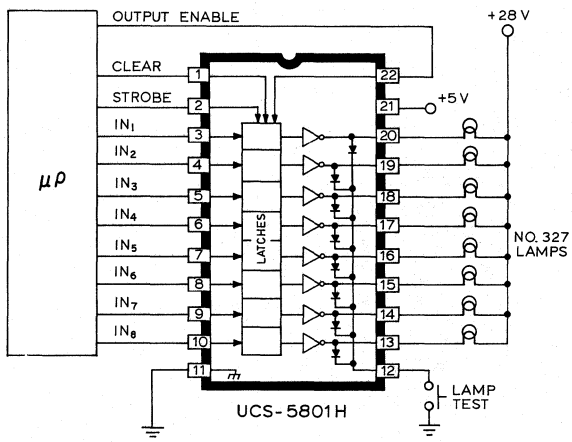
RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage	45 V
Logic Supply Voltage	12 V
Continuous Output Current	350 mA

UNIPOLAR BIFILAR MOTOR DRIVE



Dwg. No. B-1491A



Dwg. No. A-11,743A

INCANDESCENT LAMP DRIVER

NOTES

SECTION 7—LINEAR INTEGRATED CIRCUITS

®C-QUAM (Compatible Quadrature Amplitude Modulation) is a registered trademark of Motorola, Inc.

Continued

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*Complete information is provided in Data Book CN-250, Discrete Semiconductors.
†Complete information is provided in Data Book SN-500, IC Sensors.

SELECTION GUIDE TO AM AND FM RADIO CIRCUITS

Device Type	RF Mixer	FM IF	FM Det.	Mute/ Squelch	Δf Mute	Stereo Decode	AM Radio	Audio Amp	Supply Voltage Range
NE564N/F	—	—	X	—	—	—	—	—	4.5-5.5 V
ULN-2111A	—	X	X	—	—	—	—	—	8.0-14 V
ULN-2204A	—	X	X	—	—	—	X	X	2.0-12 V
ULN-2241A	—	X	X	—	—	—	X	—	10-16 V
ULN-2243A	X	X	—	—	—	—	—	—	8.0-12 V
ULN-3803A	—	X	X	—	—	—	X	—	3.0-12 V
ULN-3809A	—	—	—	—	—	X	—	—	9.0-16 V
ULN-3820A	—	—	—	—	—	X†	—	—	6.0-12 V
ULN-3821A	—	—	—	—	—	—	XX††	—	6.0-12 V
ULN-3823A	—	—	—	—	—	X	—	—	1.8-9.0 V
ULN-3839A	—	—	—	—	—	—	X	X	1.8-9.0 V
ULN-3840A	—	X	X	X	X	—	X	—	8.5-16 V
ULN-3841A	—	—	—	—	—	—	X	—	6.5-16 V
ULN-3842A	X	X	X	X	X	—	X	—	8.5-16 V
ULN-3859A	X	X	X	X	—	—	—	—	4.0-9.0 V
ULN-3862A	X	X	X	X	—	—	—	—	2.0-8.0 V
ULN-3869M	X	—	—	—	—	—	—	—	1.5-6.0 V
ULN-3883A	X	X	X	X	—	—	—	X	3.0-9.0 V

Detailed technical information is available from any Sprague sales office or sales representative.
†C-QUAM® AM stereo decoder (®Motorola, Inc.).
††Tuning stabilizer for AM radio.

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SELECTION GUIDE TO AUDIO POWER AMPLIFIERS

Device Type	Monophonic	Stereo	P_{OUT}	@	R_L	and	V_{CC}	Supply Voltage Range
ULN-2280B	X	—	2.5 W		8Ω		18 V	8.0-26 V
			2.5 W		16Ω		24 V	
ULN-3718M†	X	—	80 mW		8Ω		3.0 V	1.8-9.0 V
			125 mW		32Ω		6.0 V	
			430 mW		8Ω		6.0 V	
ULN-3725M†	X	—	0.9 W		4Ω		6.0 V	3.0-14 V
			1.3 W		8Ω		9.0 V	
			2.3 W		8Ω		12 V	
ULN-3750B	—	X	0.9 W		4Ω		6.0 V	3.0-14 V
			1.3 W		8Ω		9.0 V	
			2.3 W		8Ω		12 V	
ULN-3782M†	—	X	220 mW		8Ω		3.0 V	1.8-9.0 V
			430 mW		8Ω		6.0 V	
ULN-3784B	X	—	5.0 W		8Ω		24 V	9.0-28 V
			4.8 W		16Ω		28 V	
ULN-3793/94W	X	—	18 W		4Ω		13.2 V	8.0-16 V
			11 W		8Ω		13.2 V	

Detailed technical information is available from any Sprague sales office or sales representative.
†New product. Contact factory for information.

SELECTION GUIDE TO POWER SUPPLY CIRCUITS

Device Type	Description	Page
NE5560N/F	General-purpose, full-feature, primary side PWM controller with feed-forward control for single-ended power converter applications	§
NE5561N	Low-cost, basic PWM controller for dc-to-dc systems	§
NE5568N	Similar to NE5561N with trimmed ±2% reference	§
SG3525AJ/AN	High-frequency PWM controller with dual NOR outputs for single- or double-ended systems	§
SG3526J/N	High-frequency full-feature PWM controller for single- or double-ended systems	§
SG3527AJ/AN	Similar to SG3525AJ/AN with dual OR outputs	§
TL594CN	Universal PWM controller featuring dual analog inputs and pin-programmable dual outputs	§
TL594IN	Similar to TL594C for operation over temperature range of −40°C to +85°C	§
TL595CN	Similar to TL594CN with added 39 V shunt regulator and output logic steering input	§
TL595IN	Similar to TL595CN for operation over temperature range of −40°C to +85°C	§
ULN-8130A	Versatile precision voltage monitoring system featuring a ±1% trimmed reference. Monitors four positive *or* two positive and two negative power supply outputs and power line	7-23
ULN-8131A	Similar to ULN-8130A. Can also monitor three positive outputs and one negative power supply output and power line	7-28
ULN-8163A/R	Full-feature, precision (trimmed to ±1%), low-voltage primary-side controller with pulse-by-pulse current limiting for single-ended applications	7-33

§Detailed technical information is available from any Sprague sales office or sales representative.

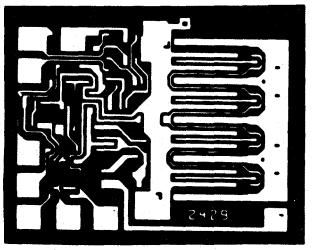
SELECTION GUIDE TO MISCELLANEOUS LINEAR ICs

§Detailed technical information is available from any Sprague sales office or sales representative.
†New product. Contact factory for information.
*Refer to Data Book SN-500, Integrated Sensors.

ULN-2429A FLUID DETECTOR

FEATURES

- High Output Current
- A-C or D-C Output
- Single-Wire Probe
- Low External Parts Count
- Internal Voltage Regulator
- Reverse Voltage Protection
- 14-Pin Dual In-Line Plastic Package



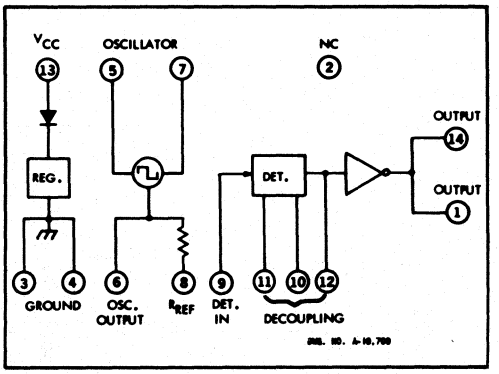
PRIMARILY DESIGNED for use as an automotive low coolant detector, the ULN-2429A monolithic bipolar integrated circuit is ideal for detecting the presence or absence of many different types of liquids in automotive, home, or industrial applictions. Especially useful in harsh environments, reverse voltage protection, internal voltage regulation, temperature compensation, and high-frequency noise immunity are all incorporated in the design.

A simple probe, immersed in the fluid being monitored, is driven with an a-c signal to prevent plating problems. The presence, absence, or condition of the fluid is determined by comparing the loaded probe resistance with an internal (pin 8) or external (pin 6) resistance. Typical conductive fluids which can be sensed are tap water, sea water, weak acids and bases, wet soil, wine, beer, and coffee. Non-conductive fluids include most petroleum products, distilled water, dry soil, and vodka. The probe can be replaced with any variable-resistance element such as a photodiode or photoconductive cell, rotary or linear position sensor, or thermistor for detecting solids, non-conducting liquids, gases, etc.

The high-current output is typically a square wave signal for use with an LED, incandescent lamp, or loudspeaker. A capacitor can be connected (pin 12) to provide a d-c output for use with inductive loads such as relays and solenoids.

The ULN-2429A is rated for operation with a load voltage of up to 30 volts. Selected devices, for operation up to 50 V are available as the ULN-2429A-1. In all other respects, the ULN-2429A and the ULN-2429A-1 fluid detectors are identical.

These devices are furnished in an improved 14-lead dual in-line plastic package with a copper alloy lead frame for superior thermal characteristics. However, in order to realize the maximum current-handling capability of these devices, both of the output pins (1 and 14) and both ground pins (3 and 4) should be used.



FUNCTIONAL BLOCK DIAGRAM

7

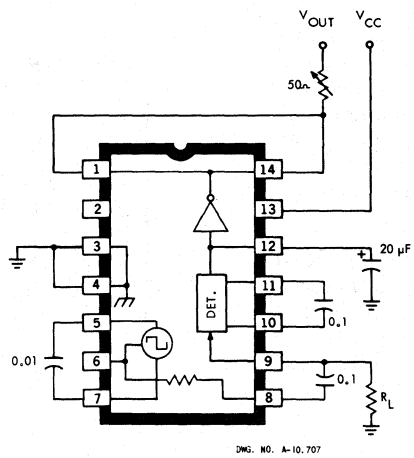
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (continuous) . . . . . +16 V, −50 V
(1 hr. at +25°C) . . . . . +24 V
(10 μs) . . . . . +50 V
Output Voltage, V_{OUT} (ULN-2429A) . . . . . +30 V
(ULN-2429A-1) . . . . . +50 V
Output Current, I_{OUT} (continuous) . . . . . 700 mA
(1 hr. at +25°C) . . . . . 1.0 A
Package Power Dissipation, P_D . . . . . 1.33 W*
Operating Temperature Range, T_A . . . . . −40°C to +85°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C
*Derate at the rate of 16.67 mW/°C above T_A = +70°C.

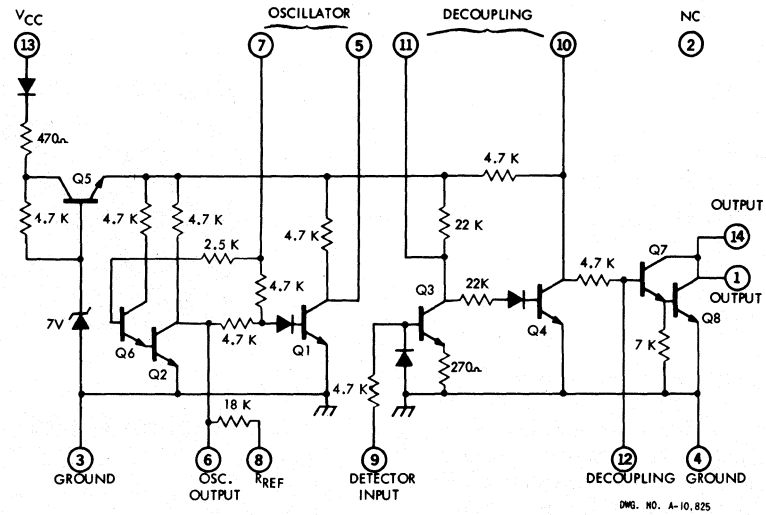
ELECTRICAL CHARACTERISTICS at T_A = −25°C, V_{CC} = V_{OUT} = +12 V (unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	13	—	10	—	16	V
Supply Current	I_{CC}	13	V_{CC} = +16V	—	—	10	mA
Oscillator Output Voltage	V_{osc}	6	R_L = 18 kΩ	—	3.0	—	V_{PP}
Output ON Voltage	V_{OUT}	1,14	$R_L \geq$ 30 kΩ, I_{OUT} = 500 mA	—	0.9	1.5	V
Output OFF Current	I_{OUT}	1,14	$R_L \leq$ 10 kΩ, V_{OUT} = V_{OUT}(max)	—	—	100	μA
Oscillator Frequency	f_{osc}	6	R_L = 18 kΩ	—	2.4	—	kHz

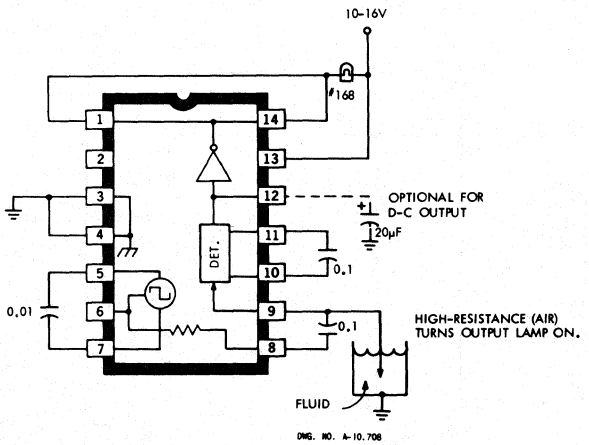
TEST CIRCUIT

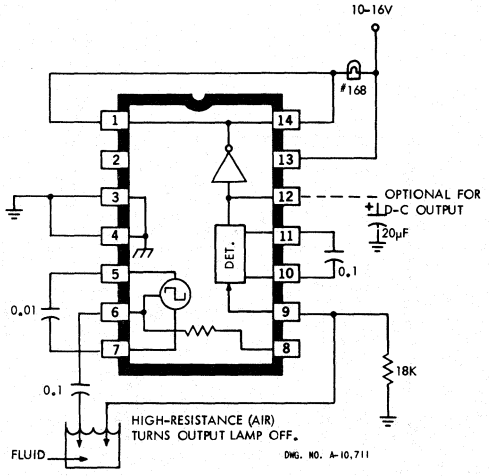


CIRCUIT SCHEMATIC



TYPICAL APPLICATIONS



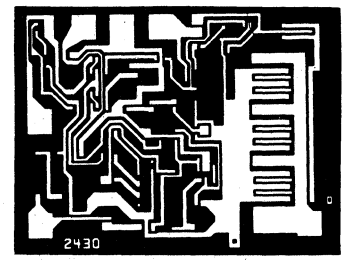


7

ULN-2430M TIMER

FEATURES

- Microseconds to Minutes
- Temperature Compensated
- 400 mA Output
- 8-Pin Dual In-Line Plastic Package

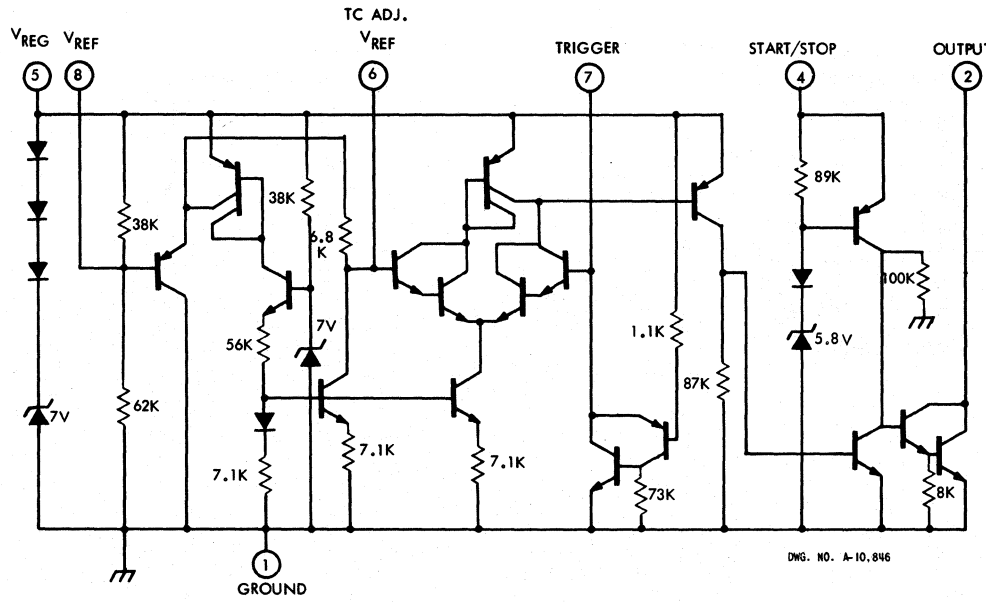


PROVIDING time delays from several microseconds to approximately 10 minutes, the ULN-2430M timer was originally designed for use as a rear window heater timer in automotive applications. In typical system designs, this device will meet all of the stringent automotive environmental and transient requirements, including "load dump". The rugged design, the high output current rating, and an internal voltage regulator and reference allow the ULN-2430M timer to be used in many industrial applications.

ABSOLUTE MAXIMUM RATINGS

Regulator Current, I_{REG} ..... 15 mA
Latch Current, I_4 ..... 3 mA
Output Current, I_{OUT} ..... 400 mA
Package Power Dissipation, P_D ..... 330 mW*
Operating Temperature Range, T_A ..... −40°C to +85°C
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at the rate of 4.2 mW/°C above T_A = +70°C.



ELECTRICAL CHARACTERISTICS at T_A = +25°C (unless otherwise noted), Fig. 1

Characteristic	Test Pin	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operating Voltage Range			10	—	16	V
Regulator Voltage	5		8.4	9.0	10.1	V
Output Breakdown Voltage	2	I_{LEAK} = 100 μA	30	—	—	V
Output Saturation Voltage	2	I_{OUT} = 400 mA	—	—	2.5	V
		I_{OUT} = 250 mA	—	—	1.3	V
Latch Voltage	4	Over Op. Temp. Range	5.5	7.0	8.0	V
Trigger Threshold	7	V_7/V_5	0.60	0.63	0.67	
Reference	8	V_8/V_5	0.58	0.63	0.68	
Temp. Coeff. of Trigger Threshold	7		−2.0	—	−4.0	mV/°C
Trigger Input Current	7		—	20	200	nA
Capacitor Discharge Time	7	C_1 = 220 μF, ±10%	—	—	2.0	s
Supply Current	5	V_{CC} = 16 V	—	—	10	mA

CIRCUIT OPERATION

The basic system shown in Figure 1 provides power for the timer after the momentary closure of the "rear window heater switch" S_1. Momentary closure provides an input to pin 4 which turns ON the output driver, energizes the relay, and (through the relay contacts) provides power to the timer and the heater element. Waveforms are shown in Figure 2.

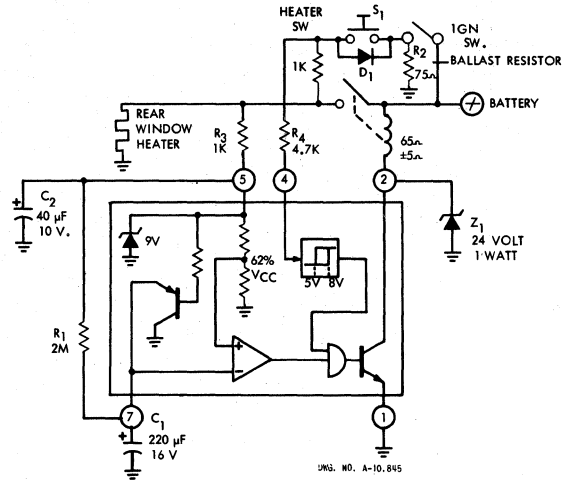
The output remains ON, supplying power to the heater until V_7 = 62% V_5, which occurs at time t = R_1 x C_1. The time delay can be adjusted from several microseconds to approximately 10 minutes by the choice of R_1 and C_1. When t = R_1 x C_1, the comparator changes state and the relay de-energizes, returning the circuit to the quiescent condition.

Timing accuracy is primarily a function of capacitor leakage for long time delays. Hard switching of the comparator necessitates low input bias currents on the comparator and low capacitor leakage current. The worst case comparator input is 200 nA and the charge current at V_7 = 62% V_5 is approximately 1.7 μA for R_1 = 2 MΩ. For these reasons, it is recommended that R_1 not exceed 2 MΩ and C_1 leakage be less than 500 nA.

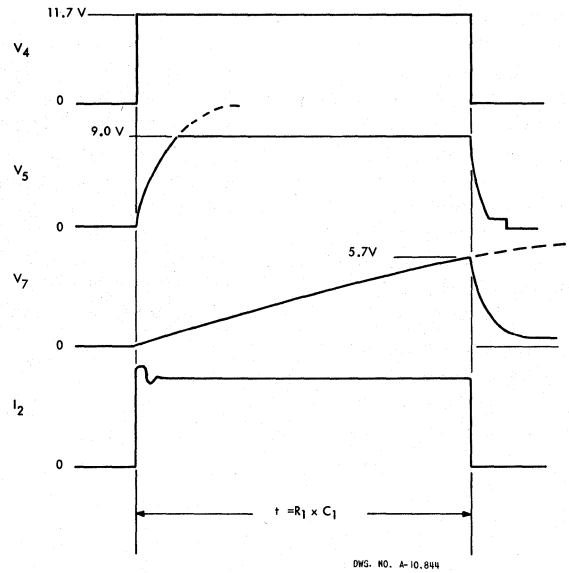
Diode D_1 and the circuitry associated with pin 4 provide start-stop capability for the timer. When the voltage at pin 4 is larger than 8 V timing is initiated. When less than 5.5 V, timing is stopped. Transient protection against load dump and other automotive environmental hazards is provided by the integrated circuit design and discrete components Z_1, C_2, R_3, R_4, and D_1.

TYPICAL APPLICATION

(Figure 1)



TIMER WAVEFORMS



ULN-2435A, ULN-2445A, AND ULN-2455A AUTOMOTIVE LAMP MONITORS

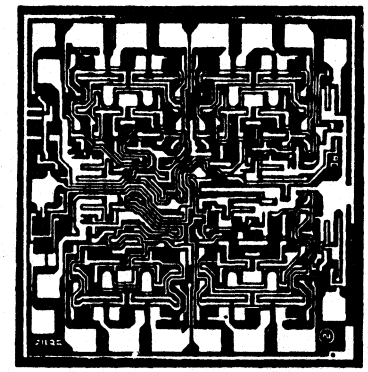
FEATURES

- No Standby Power
- Integral to Wiring Assembly
- Fail-Safe
- Reverse Voltage Protected
- Internal Transient Protection
- Dual In-Line Plastic Packages

CAPABLE of monitoring all types of automotive lamps, Type ULN-2435A, ULN-2445A, and ULN-2455A lamp monitors provide multiple LED outputs to pinpoint the area in which a lamp has failed. Types ULN-2435A and ULN-2445A feature an additional output that triggers an alarm if any of the comparators detects a lamp failure. This output can be used to drive an audible signaling device or centrally located warning indicator.

The Type ULN-2435A lamp monitor has interconnected comparator ouputs and logic to monitor the ignition circuit and fuses, making it uniquely applicable to automotive applications. Type ULN-2445A is similar, but has no interconnected comparators. Type ULN-2455A is a general-purpose quad comparator that can be used to monitor automotive lamps, multiple low-voltage power supplies, or, with appropriate sensors, industrial processes.

Installation and operation of these quad lamp monitors has no effect on normal lamp operation. Comparators sense the normal voltage drop in the lamp wiring (approximately 20 mV) for each of the monitored lamp circuits. Little additional wiring is necessary for installation because the system can be completely integral to the wiring assembly. No standby power is required: The operating voltage is obtained from the sense leads; the system is energized only when the lamps are turned ON.



All three integrated circuits are designed for use in the severe automotive environment. Lateral PNP transistors provide high-frequency noise immunity and differential transient-voltage protection. Reverse voltage protection, internal regulators, and temperature compensation are all embodied in the circuit design. A failure within the device will not affect lamp operation.

Types ULN-2435A and ULN-2445A are supplied in 18-pin dual in-line plastic packages. The Type ULN-2455A lamp monitor is supplied in a 14-pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Supply Voltage, V_{CC}	30 V
Peak Supply Voltage, V_{CC} (0.1 s)	80 V
Peak Reverse Voltage, V_R	30 V
Output Current, I_{OUT}	35 mA
Package Power Dissipation, P_D (ULN-2435/45A)	2.3 W*
(ULN-2455A)	2.0 W**
Operating Temperature Range, T_A	−40°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate at the rate of 18.18 mW/°C above T_A = +25°C.
**Derate at the rate of 16.67 mW/°C above T_A = +25°C.

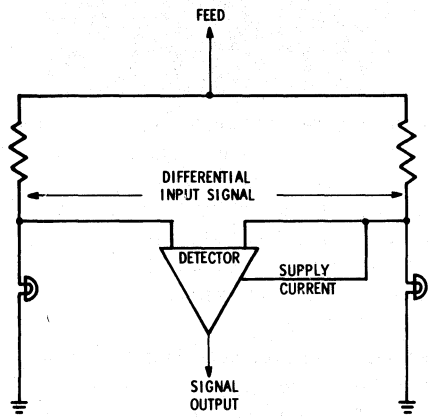
7

PRINCIPLE OF OPERATION

Operation of these lamp monitors is similar to that of a simple bridge circuit in which the top two legs of the bridge are formed by the wiring assembly resistance or discrete low-value resistors. The bottom legs of the bridge are the monitored lamps. Four differential amplifier circuits sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

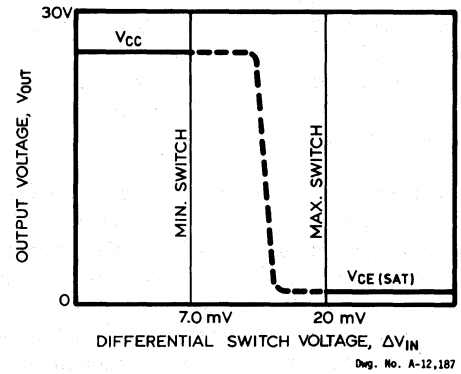
Sprague Electric Technical Paper TP 81-7 discusses the requirements of automotive lamp monitoring systems and presents a more detailed description of the operation of these differential sense amplifiers (page 10-56).

BASIC BRIDGE MONITORING SYSTEM



Dwg. No. A-11,473A

TYPICAL SWITCH CHARACTERISTICS

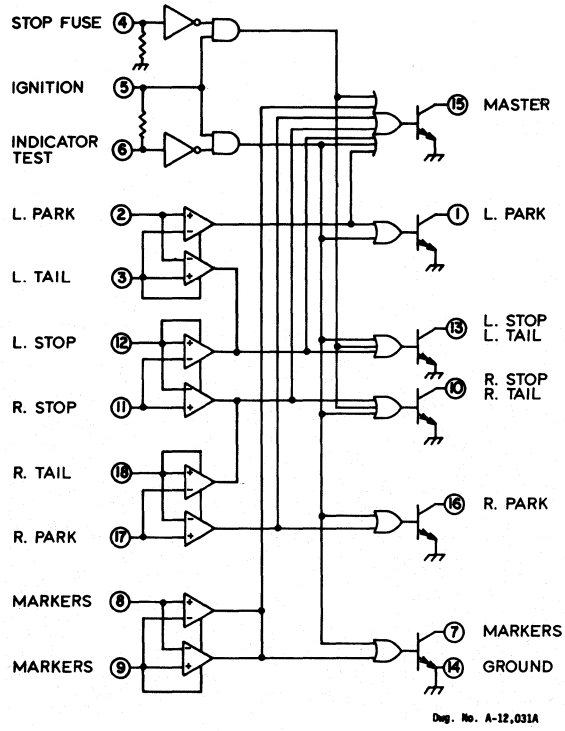


Dwg. No. A-12,187

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{IN} = 10 to 16 V (unless otherwise shown)

Characteristic	Test Pins		Test Conditions	Limits			
	ULN-2435/45A	ULN-2455A		Min.	Typ.	Max.	Units
Output Leakage Current	1, 7, 10, 13, 15, 16	1, 4, 8, 11	V_{OUT} = 80 V, $\Delta V_{IN} < 7$ mV	—	—	100	µA
Output Saturation Voltage	1, 7, 10, 13, 15, 16	1, 4, 8, 11	I_{OUT} = 5 mA, $\Delta V_{IN} > 20$ mV	—	0.8	1.0	V
			I_{OUT} = 30 mA, $\Delta V_{IN} > 20$ mV	—	1.4	2.0	V
Differential Switch Voltage	2-3, 8-9, 11-12, 17-18	2-3, 5-6, 9-10, 12-13	Absolute Value $V_{(2)} - V_{(3)}$	7.0	13	20	mV
Input Current	4	NA	$V_{IN} = V_{CC}$ = 16 V	—	—	500	µA
	5	NA	$V_{IN} = V_{CC}$ = 16 V	—	—	15	mA
	6	NA	V_{IN} = 0 V, V_{CC} = 16 V	—	—	−1.0	mA
	2, 8, 11, 17	2, 5, 9, 12	$\Delta V_{IN} = V_{(2)} - V_{(3)} = +30$ mV	150	300	800	µA
	3, 9, 12, 18	3, 6, 10,1 3	$\Delta V_{IN} = V_{(2)} - V_{(3)} = -30$ mV	0.5	1.7	3.5	mA

ULN-2435A
FUNCTIONAL BLOCK DIAGRAM

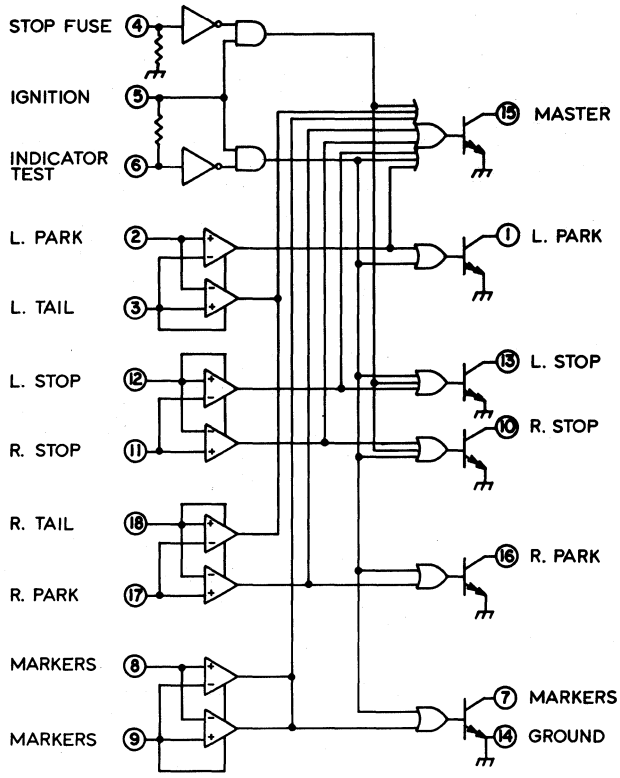


ULN-2435A and ULN-2445A TRUTH TABLES

	INPUT PINS							OUTPUT PINS											
								ULN-2435A						ULN-2445A					
CONDITIONS	2/3	8/9	11/12	17/18	6	4	5	1	7	10	13	15	16	1	7	10	13	15	16
Normal	=	=	=	=	0	H	X	H	H	H	H	H	H	H	H	H	H	H	H
L. Park Lamp Failure	>	=	=	=	0	H	X	L	H	H	H	L	H	L	H	H	H	L	H
L. Tail Lamp Failure	<	=	=	=	0	H	X	H	H	H	**L**	L	H	H	H	H	**H**	L	H
Marker Lamp Failure	=	>	=	=	0	H	X	H	L	H	H	L	H	H	L	H	H	L	H
Marker Lamp Failure	=	<	=	=	0	H	X	H	L	H	H	L	H	H	L	H	H	L	H
R. Stop Lamp Failure	=	=	>	=	0	H	X	H	H	L	H	L	H	H	H	L	H	L	H
L. Stop Lamp Failure	=	=	<	=	0	H	X	H	H	H	L	L	H	H	H	H	L	L	H
R. Park Lamp Failure	=	=	=	>	0	H	X	H	H	H	H	L	L	H	H	H	H	L	L
R. Tail Lamp Failure	=	=	=	<	0	H	X	H	H	**L**	H	L	H	H	H	**H**	H	L	H
Stop Lamp Fuse Failure	=	=	=	=	0	L	H	H	H	L	L	L	H	H	H	L	L	L	H
Indicator Lamp Test	X	X	X	X	L	X	H	L	L	L	L	L	L	L	L	L	L	L	L

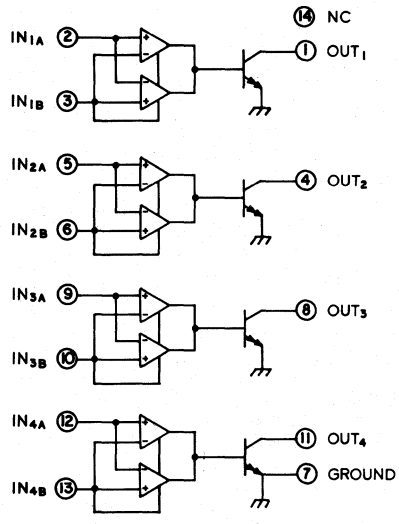
= — Less than 7 mV offset between a pair of input pins
> — Greater than +20 mV differential between a pair of input pins [$V_{(2)} - V_{(3)}$]
< — Greater than −20 mV differential between a pair of input pins [$V_{(2)} - V_{(3)}$]
H — V_{CC}
L — V_{SAT} (outputs) or GROUND (inputs)
0 — Open or V_{CC}
X — Irrelevant

ULN-2445A FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,032A

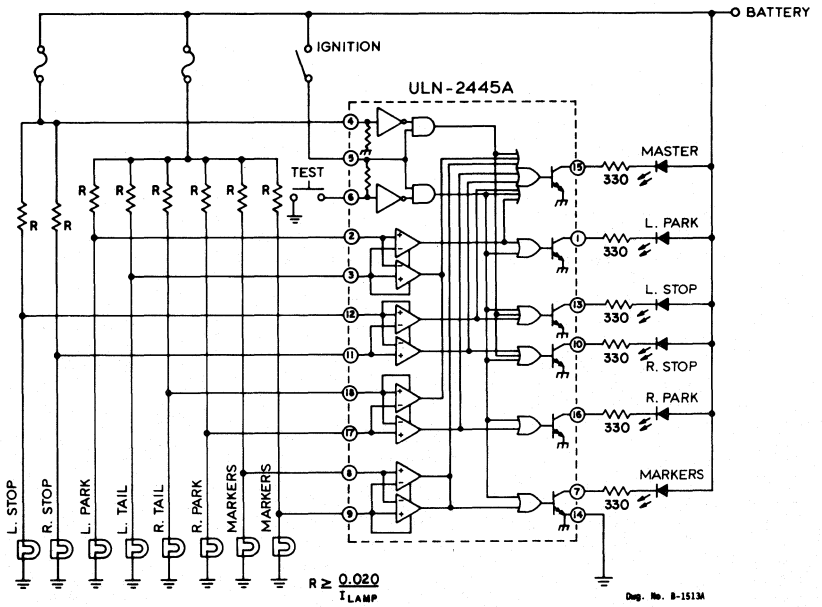
ULN-2455A FUNCTIONAL BLOCK DIAGRAM



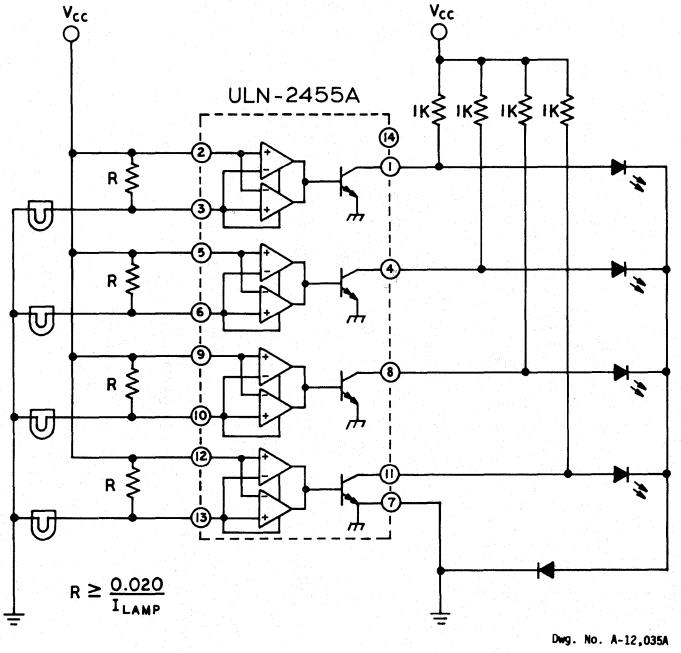
Dwg. No. A-12,033A

TYPICAL APPLICATIONS

AUTOMOTIVE LAMP MONITOR

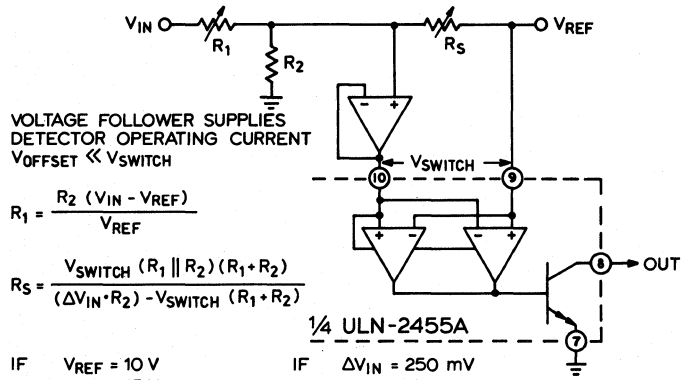


QUAD LAMP MONITOR



TYPICAL APPLICATIONS (Continued)

POWER SUPPLY SUPERVISORY CIRCUIT



$$R_1 = \frac{R_2\,(V_{IN} - V_{REF})}{V_{REF}}$$

$$R_S = \frac{V_{SWITCH}\,(R_1 \parallel R_2)(R_1 + R_2)}{(\Delta V_{IN} \cdot R_2) - V_{SWITCH}\,(R_1 + R_2)}$$

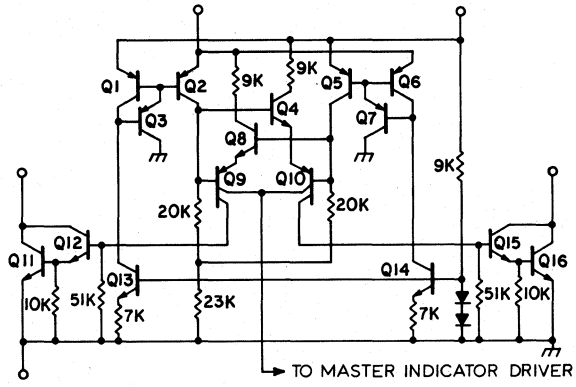
IF V_{REF} = 10 V
V_{IN} = 15 V
R_2 = 15 kΩ
THEN R_1 = 7.5 kΩ

IF ΔV_{IN} = 250 mV
V_{SWITCH} = 13 mV
THEN R_S = 423 Ω

Dwg. No. B-1524

SIMPLIFIED SCHEMATIC

(One of 4 differential sense amplifiers)

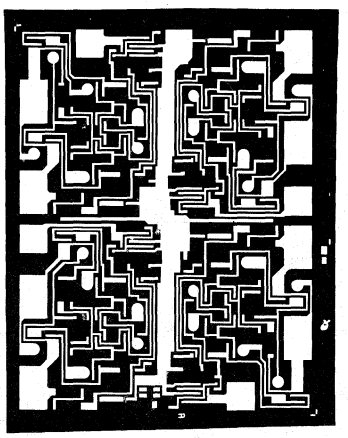


Dwg.No. A-12,036

ULN-2457A AND ULN-2457L
QUAD LAMP MONITORS FOR 24 V SYSTEMS

FEATURES

- 18 to 32 V Operation
- No Standby Power
- Integral to Wiring Assembly
- Fair-Safe
- Reverse-Voltage Protected
- Internal Transient Protection



CAPABLE of monitoring lamps in truck or bus, railroad, marine, and other applications using 24 V power systems, the ULN-2457A and ULN-2457L lamp monitors provide LED outputs (to 35 mA) to indicate the circuit in which a lamp failure has occurred. Differential amplifiers sense the voltage drops in the wiring assemblies (approximately 20 mV) for similar lamps. When the monitor detects a difference in voltage due to an open filament or lamp socket, the appropriate output driver is turned ON. Both devices are general-purpose quad comparators that can also be used to monitor multiple low-voltage power supplies and, with appropriate sensors, industrial processes.

The installation and operation of these quad lamp monitors has negligible effect on normal lamp operation. Comparators sense the normal voltage drop in the lamp wiring for each of the monitored lamp circuits. Little additional wiring is necessary for installation because the system can be completely integral to the wiring assembly. No standby power is required. The operating voltage is obtained from the sense leads; the system is energized only when the lamps are turned ON.

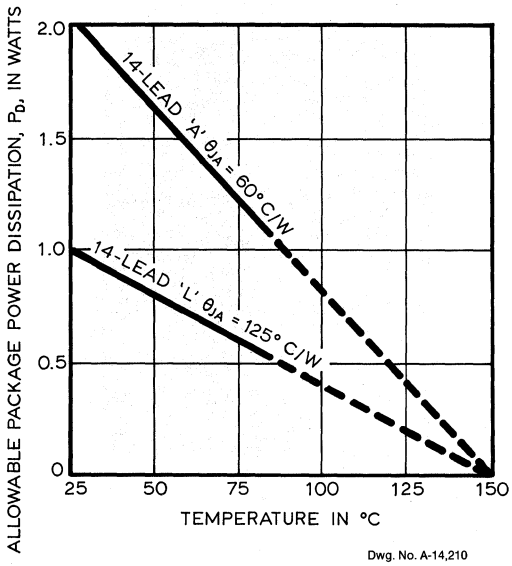
These integrated circuits were designed to withstand the severe environment of heavy-duty automotive applications. Lateral PNP transistors and thin-film resistors provide high-frequency noise immunity, transient-voltage protection, and reverse voltage protection. Internal regulators and temperature compensation are included in the circuit design. A failure within the device will not affect lamp operation. For low-voltage applications (10 to 16 V) the pin-compatible ULN-2455A is suggested.

The ULN-2457A is supplied in a standard 14-pin dual in-line plastic package. The ULN-2457L is supplied in a surface-mount 14-lead SOIC plastic package. Both devices are rated for operation over the temperature range of −40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

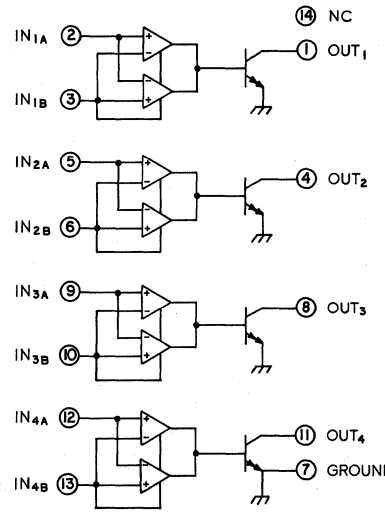
Supply Voltage, V_{CC}	34 V
Peak Supply Voltage, V_{CC} (0.1 s)	80 V
Peak Reverse Voltage, V_R	30 V
Output Current, I_{OUT}	35 mA
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−40°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C

ALLOWABLE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-14,210

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-12,033A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = V_{IN} = 18$ to 32 V (unless otherwise shown)

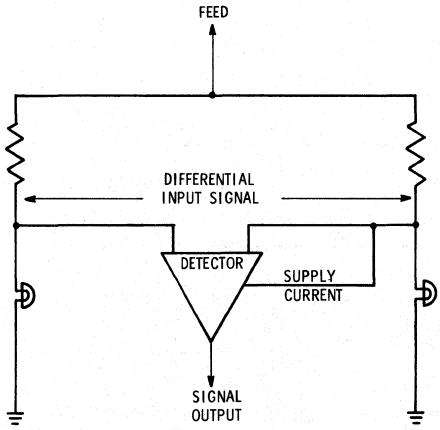
Characteristic	Test Pins	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	1, 4, 8, 11	$V_{OUT} = 80$ V, $\Delta V_{IN} < 7$ mV	—	—	100	μA
Output Saturation Voltage	1, 4, 8, 11	$I_{OUT} = 5$ mA, $\Delta V_{IN} > 20$ mV	—	0.8	1.0	V
		$I_{OUT} = 30$ mA, $\Delta V_{IN} > 20$ mV	—	1.4	2.0	V
Differential Switch Voltage	2-3, 5-6, 9-10, 12-13	Absolute Value $V_{(2)} - V_{(3)}$	7.0	13	20	mV
Input Current	2, 5, 9, 12	$\Delta V_{IN} = V_{(2)} - V_{(3)} = +30$ mV	150	300	800	μA
	3, 6, 10, 13	$\Delta V_{IN} = V_{(2)} - V_{(3)} = -30$ mV	0.5	1.7	3.5	mA

PRINCIPLE OF OPERATION

Operation of these lamp monitors is similar to that of a simple bridge circuit in which the top two legs of the bridge are formed by the wiring assembly resistance or discrete low-value resistors. The bottom legs of the bridge are the monitored lamps. Four differential amplifier circuits sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

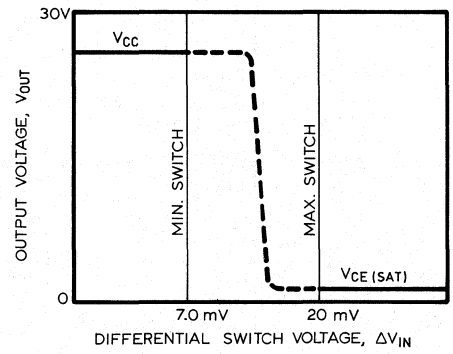
Sprague Technical Paper TP 81-7 discusses the requirements of automotive lamp monitoring systems and presents a more detailed description of the operation of these differential sense amplifiers.

BASIC BRIDGE MONITORING SYSTEM



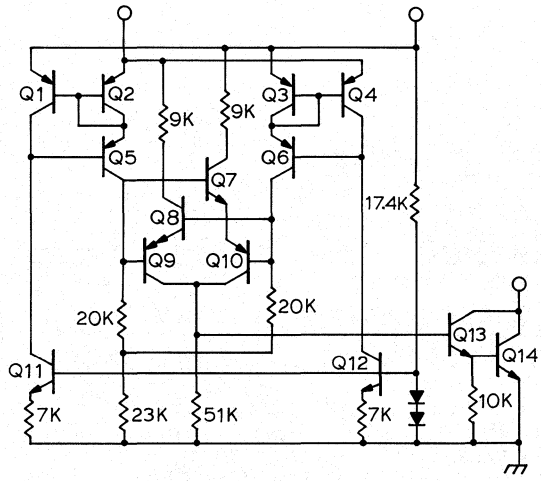
Dwg. No. A-11,473A

TYPICAL SWITCH CHARACTERISTICS



Dwg. No. A-12,187

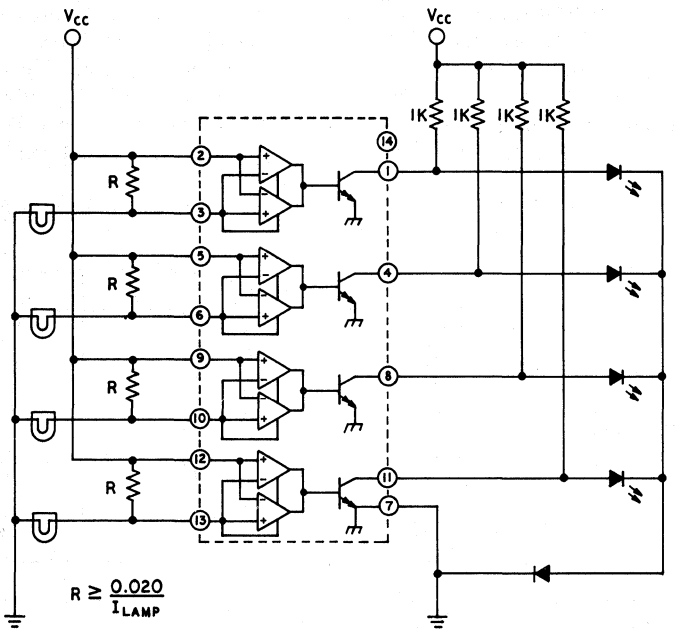
SIMPLIFIED SCHEMATIC
(One of 4 differential sense amplifiers)



Dwg. No. A-14,212

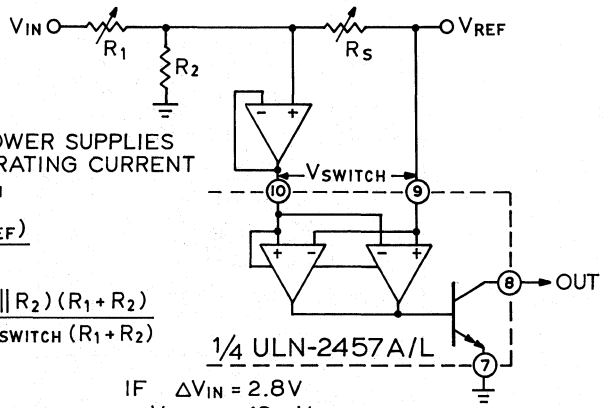
TYPICAL APPLICATIONS

QUAD LAMP MONITOR



Dwg. No. A-14,209

POWER SUPPLY SUPERVISORY CIRCUIT



VOLTAGE FOLLOWER SUPPLIES DETECTOR OPERATING CURRENT

$V_{OFFSET} \ll V_{SWITCH}$

$$R_1 = \frac{R_2 (V_{IN} - V_{REF})}{V_{REF}}$$

$$R_S = \frac{V_{SWITCH} (R_1 \| R_2)(R_1 + R_2)}{(\Delta V_{IN} \cdot R_2) - V_{SWITCH} (R_1 + R_2)}$$

IF $V_{REF} = 20V$
$V_{IN} = 28V$
$R_2 = 15k\Omega$

THEN $R_1 = 6.0k\Omega$

IF $\Delta V_{IN} = 2.8V$
$V_{SWITCH} = 13mV$

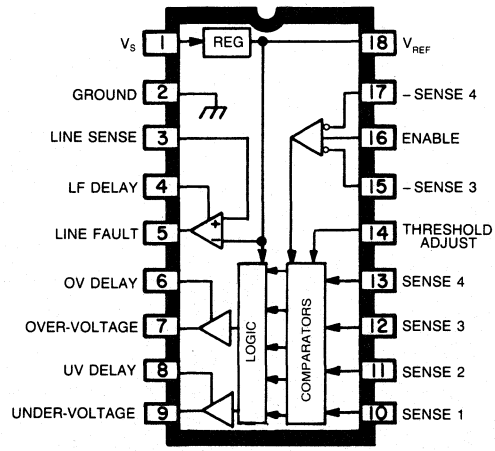
THEN $R_S = 28\Omega$

Dwg. No. A-14,211

ULN-8130A
PRECISION SUPERVISORY SYSTEMS MONITOR
Quad Voltage and Line Monitor

FEATURES

- 10 V to 35 V Operation
- Low Standby Current
- Reference Trimmed to 1%
- Monitors 4 Separate DC Levels
- Separate Under-Voltage Comparators
- Fixed Under-Voltage Threshold
- Line Sense Input
- Pull-Up Clamped Outputs
- Programmable Output Delays
- V_S Under-Voltage Lockout



Dwg. No. A-13,221

Capable of monitoring four dc power lines, the ULN-8130A is a power fault monitor for both under-voltage and over-voltage conditions. Two of the four inputs are designed to monitor positive voltages while the other two inputs can be used to monitor two positive or two negative voltages. An additional comparator is used to monitor the primary power line and will provide early warning of line voltage drop-out.

An under-voltage lockout, monitoring the ULN-8130A internal supply, prevents false outputs from occurring during low supply-voltage operation. The logic outputs can be used to operate LEDs or other low-voltage indicators.

The circuit configuration of the ULN-8130A allows easy programming of over-voltage thresholds which are referenced to a 1% trimmed 2.5 V bandgap reference. The UV FAULT (pin 9) is initiated by one or more of the four sense inputs falling below the UV trip point (the internal reference voltage). The OV FAULT (pin 7) is activated by one or more of the sense inputs rising above the externally set (pin 14) OV trip point. The LINE OK output (pin 5) will remain high as long as the LINE SENSE input (pin 3) is above the internal reference voltage. The LINE SENSE will accept a positive dc voltage proportional to either the high-voltage master bus or the ac line.

Output delays can be introduced by adding capacitors from the appropriate DELAY pins to ground. The LINE FAULT DELAY capacitor value should be large enough to prevent false shutdowns due to short line transients.

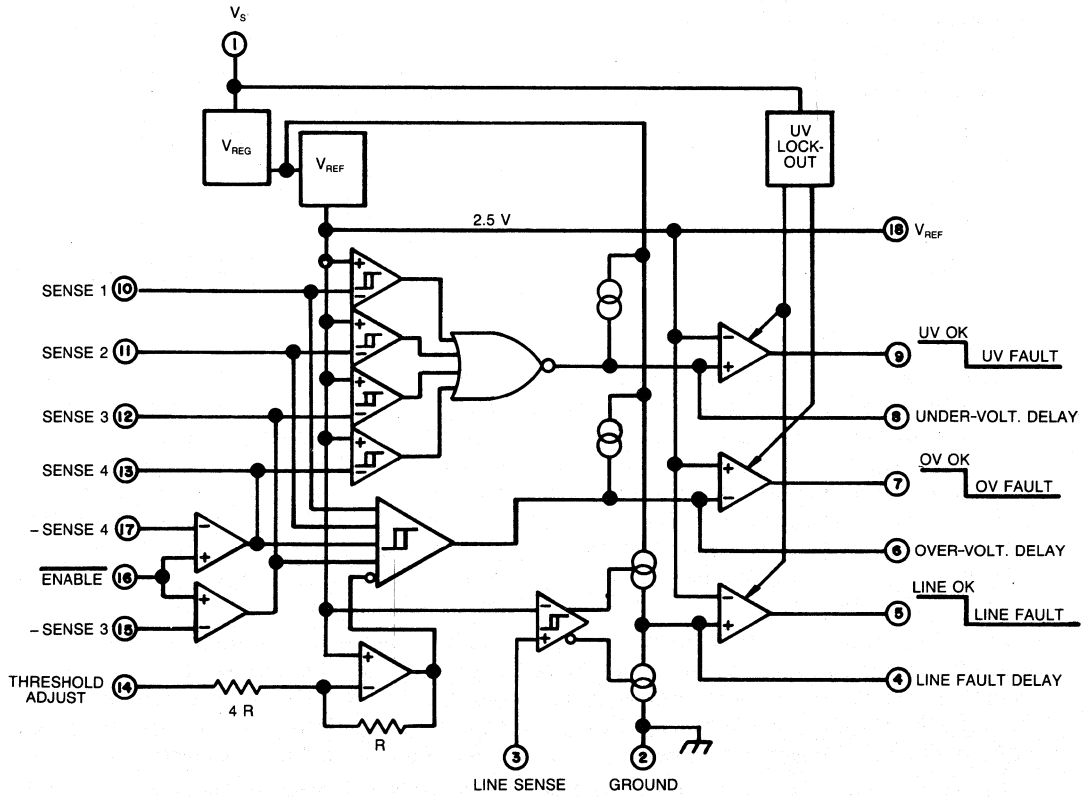
The ULN-8130A is supplied in an 18-pin dual in-line plastic package with a copper lead frame that gives it enhanced power dissipation ratings. It is rated for continuous operation over the temperature range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Supply Voltage, V_{CC} ..... 35 V
Power Dissipation, P_D ..... 2.3 W*
Operating Temperature, T_A ..... 0°C to +70°C
Storage Temperature, T_S ..... −65°C to +150°C
Junction Temperature, T_J ..... +150°C

*Derate at the rate of 18.2 mW/°C above T_A = 25°C

FUNCTIONAL BLOCK DIAGRAM



DWG A-13,002

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 15\,V$

Characteristic	Test Pin	Test Conditions	Limits		
			Min.	Max.	Units
Functional V_S Range	1		10	35	V
Quiescent Current	1	$V_S = 35\,V$, $V_{16} = V_{18}$, No Fault	—	15	mA
REFERENCE VOLTAGE SECTION					
Reference Voltage	18	No Load, $T_A = +25°C$	2.47	2.53	V
		No Load, Change Over Temp.	—	25	mV
Load Regulation	18	$I_{REF} = 0$ to 10 mA	—	20	mV
Line Regulation	18	$V_S = 10$ to 35 V	—	10	mV
Ripple Rejection	18	f = 120 Hz	60	—	dB
Short-Circuit Current Protection	18		—	40	mA
COMPARATOR SECTION					
Under-Voltage Trip Points	10-13*	$T_A = +25°C$	2.47	2.53	V
		Over Temperature	2.46	2.54	V
Under-Voltage Trip Hysteresis	10-13*	Over Temperature	10	25	mV
Over-Voltage Trip Points	10-13*	$V_{14} = 0$	3.08	3.17	V
Over-Voltage Trip Hysteresis	14	$V_{14} = 0$ to 2.5 V, Over Temp.	10	25	mV
Line Monitor Trip Threshold	3		2.40	2.54	V
Under-Voltage Lockout Enable	1	V_S Decreasing	8.5	—	V
Under-Voltage Lockout Disable	1	V_S Increasing	—	10.5	V
Input Bias Current	3, 10, 11	$V_{IN} = 2.0\,V$	—	−6.0	μA
		$V_{IN} = 3.0\,V$	—	6.0	μA
	14	$V_{IN} = 0$	—	−50	μA
	15, 17	$V_{IN} = -2.0\,V$, $V_{16} = 0\,V$	—	−2.0	μA
OUTPUT DRIVERS					
Output Saturation Voltage	5, 9	$I_{SINK} = 5.0$ mA	—	0.5	V
	7	$I_{SINK} = 10$ mA	—	0.5	V
	5, 7, 9	$I_{SOURCE} = 500\,\mu A$	4.0	5.25	V
Output Leakage Current	5, 7, 9	$V_{OUT} = 35\,V$	—	50	μA
Line Fault Delay Current Source	4	$V_4 = 2.0\,V$	160	350	μA
Line Fault Delay Current Sink	4	$V_4 = 2.0\,V$	3.2	7.0	mA
Over-Voltage Delay Current Source	6	$V_6 = 2.0\,V$	160	300	μA
Under-Voltage Delay Current Source	8	$V_8 = 2.0\,V$	35	75	μA

*All inputs connected to 2.75 V except input being tested.

APPLICATIONS

The basic voltage monitors are based on a 2.5 V precision bandgap reference. External resistive dividers are used to present a nominal 2.5 V level to each under-voltage comparator at the minimum allowable under-voltage condition. The over-voltage reference is set up by another resistive divider at pin 14 determined by the tightest over-voltage tolerance requirement.

BASIC FORMULAS:

(1) An under-voltage fault is detected, (pin 9 goes low), when the positive input voltage being monitored is less than:

$$V_{MON(LO)} = 2.5\ (R_1 + R_2)/R_2$$

(2) The internal over-voltage threshold is defined as:

$$V_{OVT} = 2.5 \left[1 + \frac{R_A}{4(R_A + R_B)}\right]$$

where $R_A \,//\, R_B << 100\ k\Omega$.

(3) An over-voltage fault is detected when the positive input voltage being monitored exceeds:

$$V_{MON(HI)} = V_{OVT}\ (R_1 + R_2)/R_2$$

(4) Individual over-voltage thresholds can be increased by the addition of R_X with

$$R_X = R_1 \left[\frac{V_{OVT} - 2.5}{V_{MON(HI)} - V_{OVT}\left(\frac{R_1 + R_2}{R_2}\right)}\right]$$

(5) To monitor negative supplies at SENSE 3 and SENSE 4, pin 16 is connected to ground. In this condition, an under-voltage fault indication will occur when either negative supply being monitored falls below:

$$V_{MON(LO)} = 2.5\ R_3/R_4$$

Note that for monitor purposes, under-voltage means the negative supply is actually going net positive, or toward ground.

(6) For negative supplies, an over-voltage fault indication will occur when:

$$V_{MON(HI)} = V_{OVT}\ R_3/R_4$$

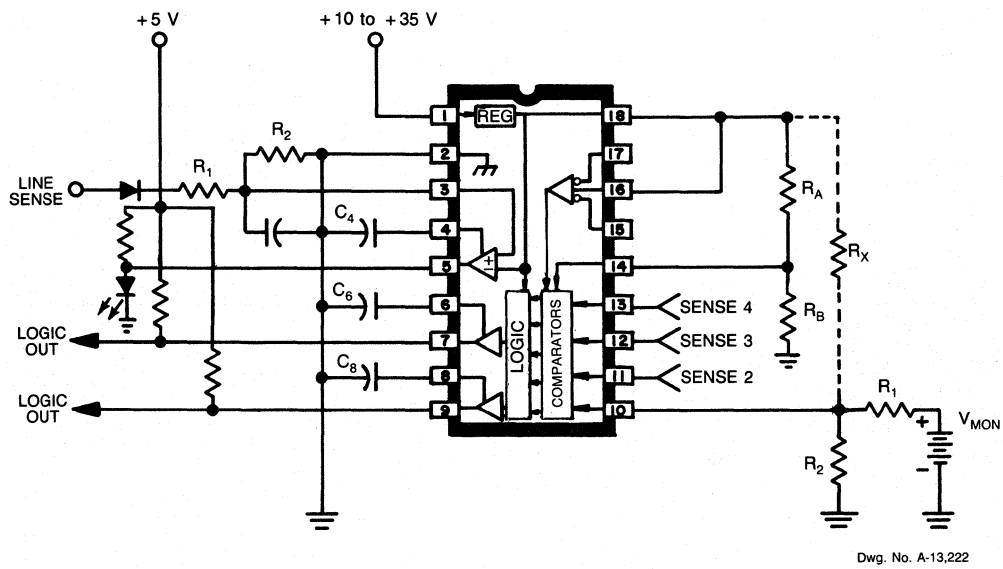
(7) Fault delay capacitor values are determined by:

$$C_4 \text{ or } C_6 = \frac{200 \times 10^{-6} \times t}{2.5}$$

$$C_9 = \frac{55 \times 10^{-6} \times t}{2.5}$$

where t is the output delay in seconds.

LINE SENSE AND POSITIVE SUPPLY MONITORING
(SENSE 1, 2, 3, and 4)



Dwg. No. A-13,222

UNUSED INPUTS

Unused positive sense channel inputs (pins 3, 10-13) must not be left unconnected. Neither can they be tied high (over-voltage fault indication), tied low (under-voltage fault indication), or tied to the internal reference (susceptible to noise and voltage offsets). Unused sense channel inputs should be connected to any operating sense channel input. For example, if channels 1, 2, and 4 are being used, the unused channel 3 sense input (pin 12) should be connected to the sense 2 or sense 4 input.

Unused negative sense channel inputs (pins 15 and 17) can be left open-circuited *provided* the associated enable input (pin 16) is tied high and the associated positive sense channel inputs (pins 12 and 13) are utilized to monitor positive supplies or are connected as described above.

DESIGN EXAMPLE

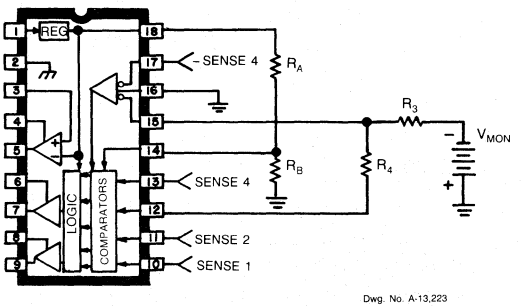
As an example, consider the following set of monitoring conditions:

V_1 = +5 V +10%, −5%
V_2 = +12 V ±10%
V_3 = +15 V ±5%
V_4 = +24 V ±10%

The required input dividers are calculated per (1) to yield the resistor divider ratios, R_2 (R_1 + R_2), of: 0.5263, 0.2315, 0.1754 (Note 1), and 0.1157 respectively. The over-voltage threshold, V_{OVT}, would be dictated by the tightest tolerance supply which gives the lowest V_{OVT} from (3). Therefore, $V_{MON(HI)}$ = 15 x 1.05 = 15.75 volts and V_{OVT} = 15.75 x 0.1754 = 2.763 volts[1]. This is the voltage appearing at the SENSE terminal and is equal to the over-voltage threshold to be set via the resistor ratio at pin 14. From (2), $R_A/(R_A + R_B)$ is calculated to be 0.4096. It is good practice to keep the equivalent external impedances as low as possible, in order to minimize bias current and offset errors. For the purpose of this example, all resistor dividers will be taken to have an equivalent impedance of 1000 ohms. This being the case, the final values are: R_A = 1.7 kΩ and R_B = 2.44 kΩ.

In order to provide accurate over-voltage sensing for the V_1, V_2, and V_4 supplies, resistors are connected from the respective input sense nodes and returned to the 2.5 V reference. Calculation is made by first picking values for the input dividers and then calculating the required value of R_X from (4). Again, assuming 1 kΩ equivalent divider impedances and making the calculations, a summary of results is given below.

NEGATIVE SENSE MONITORING
SENSE 3 and 4 Only



Dwg. No. A-13,223

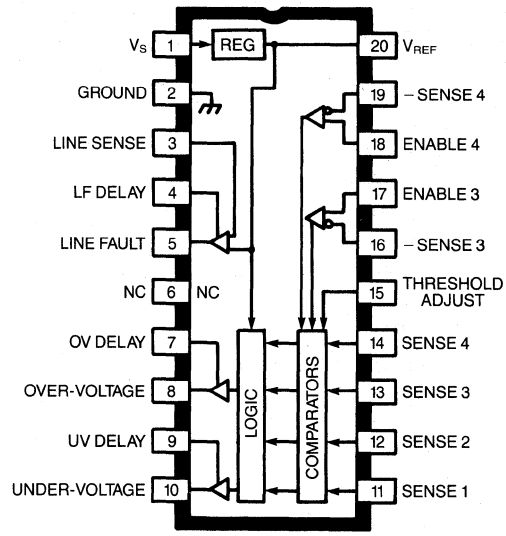
MONITORED SUPPLY	$V_{MON(HI)}$	$V_{MON(LO)}$	R_1	R_2	R_X
+5 V (+10%, −5%)	5.5 V	4.75 V	1.90 kΩ	2.11 kΩ	2.0 kΩ
+12 V (±10%)	13.2 V	10.8 V	4.32 kΩ	1.30 kΩ	900 Ω
+15 V (±5%)	15.75 V	14.25 V	5.70 kΩ	1.21 kΩ	∞
+24 V (±10%)	26.4 V	21.6 V	8.64 kΩ	1.13 kΩ	900 Ω

1. Note that the number 0.1754 is rounded off. Due to required accuracies in the external dividers, round off numbers only after final resistor values are calculated. For the same reason, use stable high-accuracy metal film resistors. Many applications may benefit from combining the ULN-8130A and functionally trimmed Sprague resistor-capacitor networks.

ULN-8131A
PRECISION SUPERVISORY SYSTEMS MONITOR
Quad Voltage and Line Monitor

FEATURES

- Reference Trimmed to 1%
- Monitors Four DC Supplies
- 10 to 35 Volts Operation
- Low Standby Current
- Separate Under-Voltage Comparators
- Fixed Under-Voltage Threshold
- Programmable Over-Voltage Threshold
- Line Sense Input
- Full-Up Clamped Outputs
- Programmable Output Delays
- V_S Under-Voltage Lockout



Dwg. No. W-185

Capable of monitoring four dc power lines, the ULN-8131A is a power-fault monitor for both under-voltage and over-voltage conditions. Two of the four inputs are designed to monitor positive voltages, while the other two inputs can be used to monitor positive or negative voltages. Typical examples might be a +5 V logic supply, +15 V and −15 V analog supplies, and a positive peripheral power load supply. The primary power line is monitored by an additional comparator and will provide early warning of line voltage drop-out.

During low-supply voltage operations, an under-voltage lockout which monitors the ULN-8131A internal supply, prevents false outputs from occurring. The logic outputs can be used to operate LEDs or other low-voltage indicators.

The circuit configuration of the ULN-8131A allows easy programming of over-voltage thresholds which are referenced to a 1% trimmed 2.5 V bandgap reference. The UV FAULT (pin 10) is initiated by one or more of the four sense inputs falling below the UV trip point (the internal reference voltage). The OV FAULT (pin 8) is activated by one or more of the sense inputs rising above the externally set (pin 15) OV trip point. The LINE OK output (pin 5) will remain high as long as the LINE SENSE input (pin 3) is above the internal reference voltage. The LINE SENSE will accept a positive dc voltage proportional to either the high-voltage master bus or the ac line.

Output delays can be introduced by adding capacitors from the appropriate DELAY pins to ground. The LINE FAULT DELAY capacitor value should be large enough to prevent false shutdowns due to short line transients.

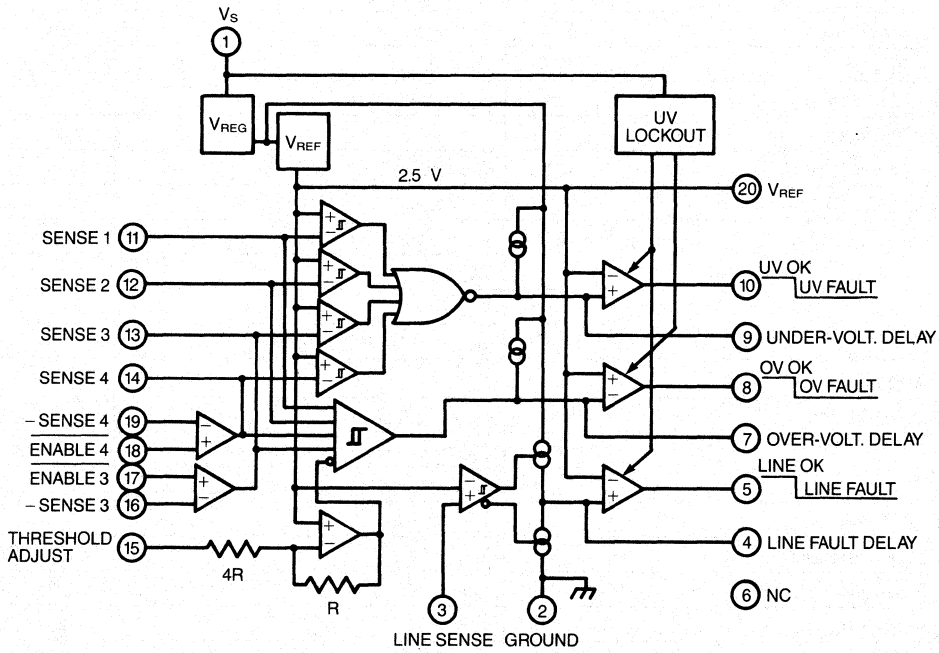
The ULN-8131A is supplied in a 20-pin dual in-line plastic package with a copper lead frame that gives it enhanced power dissipation ratings. The similar ULN-8130A is intended for monitoring four positive supplies, or two positive and two negative supplies. It is supplied in an 18-pin DIP.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Supply Voltage, V_{CC} 35V
Power Dissipation, P_D 2.3W*
Operating Temperature, T_A ..... 0°C to +70°C
Storage Temperature, T_S ..... −65°C to +150°C
Junction Temperature, T_J ..... +150°C

*Derate at the rate of 18.2 mW/°C above $T_A = 25°C$

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. W-186

7

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 15\,V$

Characteristic	Test Pin	Test Conditions	Limits Min.	Limits Max.	Units
Functional V_S Range	1		10	35	V
Quiescent Current	1	$V_S = 35V$, $V_{17} = V_{18} = V_{20}$ No Fault	—	15	mA
REFERENCE VOLTAGE SECTION					
Reference Voltage	20	No Load, $T_A = +25°C$	2.47	2.53	V
		No Load, Change Over Temp.	—	25	mV
Load Regulation	20	$I_{REF} = 0$ to 10mA	—	20	mV
Line Regulation	20	$V_S = 10$ to 35V	—	10	mV
Ripple Rejection	20	f = 120Hz	60	—	dB
Short-Circuit Current Protection	20		—	40	mA
COMPARATOR SECTION					
Under-Voltage Trip Points	11-14*	$T_A = +25°C$	2.47	2.53	V
		Over Temperature	2.46	2.54	V
Under-Voltage Trip Hysteresis	11-14*	Over Temperature	10	25	mV
Over-Voltage Trip Points	11-14*	$V_{15} = 0$	3.08	3.17	V
Over-Voltage Trip Hysteresis	15	$V_{15} = 0$ to 2.5V, Over Temp.	10	25	mV
Line Monitor Trip Threshold	3		2.40	2.54	V
Under-Voltage Lockout Enable	1	V_S Decreasing	8.5	—	V
Under-Voltage Lockout Disable	1	V_S Increasing	—	10.5	V
Input Bias Current	3, 11, 12	$V_{IN} = 2.0V$	—	−6.0	μA
		$V_{IN} = 3.0V$	—	6.0	μA
	15	$V_{IN} = 0$	—	−50	μA
	16, 19	$V_{IN} = -2.0V$, $V_{17} = V_{18} = 0V$	—	−2.0	μA
OUTPUT DRIVERS					
Output Saturation Voltage	5, 10	$I_{SINK} = 5.0mA$	—	0.5	V
	8	$I_{SINK} = 10mA$	—	0.5	V
	5, 8, 10	$I_{SOURCE} = 500\,\mu A$	4.0	5.25	V
Output Leakage Current	5, 8, 10	$V_{OUT} = 35V$	—	50	μA
Line Fault Delay Current Source	4	$V_4 = 2.0V$	160	350	μA
Line Fault Delay Current Sink	4	$V_4 = 2.0V$	3.2	7.0	mA
Over-Voltage Delay Current Source	7	$V_7 = 2.0V$	160	300	μA
Under-Voltage Delay Current Source	9	$V_9 = 2.0V$	35	75	μA

**All inputs connected to 2.75 V except input being tested.*

APPLICATIONS

The basic voltage monitors are based on a 2.5 V precision bandgap reference. External resistive dividers are used to present a nominal 2.5 V level to each under-voltage comparator at the minimum allowable under-voltage condition. The over-voltage reference is set up by another resistive divider at pin 15 determined by the tightest over-voltage tolerance requirement.

BASIC FORMULAS:

(1) An under-voltage fault is detected, (pin 10 goes low), when the positive input voltage being monitored is less than:

$$V_{MON(LO)} = 2.5\,(R_1 + R_2)/R_2$$

(2) The internal over-voltage threshold is defined as:

$$V_{OVT} = 2.5\left[1 + \frac{R_A}{4(R_A + R_B)}\right]$$

where $R_A \,//\, R_B << 100\ k\Omega$.

(3) An over-voltage fault is detected when the positive input voltage being monitored exceeds:

$$V_{MON(HI)} = V_{OVT}\,(R_1 + R_2)/R_2$$

(4) Individual over-voltage thresholds can be increased by the addition of R_X with

$$R_X = R_1\left[\frac{V_{OVT} - 2.5}{V_{MON(HI)} - V_{OVT}\left(\frac{R_1 + R_2}{R_2}\right)}\right]$$

(5) To monitor negative supplies at SENSE 3 or SENSE 4, pin 17 or 18, respectively, is connected to ground. In this condition, an under-voltage fault indication will occur when the negative supply being monitored falls below:

$$V_{MON(LO)} = 2.5\,R_3/R_4$$

Note that for monitor purposes, under-voltage means the negative supply is actually going net positive, or toward ground.

(6) For negative supplies, an over-voltage fault indication will occur when:

$$V_{MON(HI)} = V_{OVT}\,R_3/R_4$$

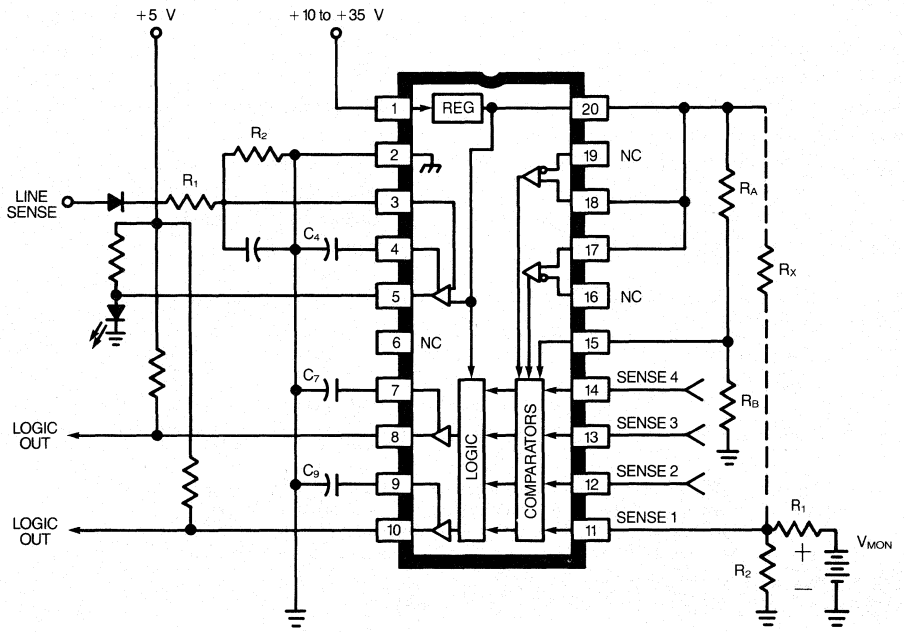
(7) Fault delay capacitor values are determined by:

$$C_4 \text{ or } C_7 = \frac{200 \times 10^{-6} \times t}{2.5}$$

$$C_9 = \frac{55 \times 10^{-6} \times t}{2.5}$$

where t is the output delay in seconds.

LINE SENSE AND POSITIVE SUPPLY MONITORING
(SENSE 1, 2, 3, and 4)



Dwg. No. W-157

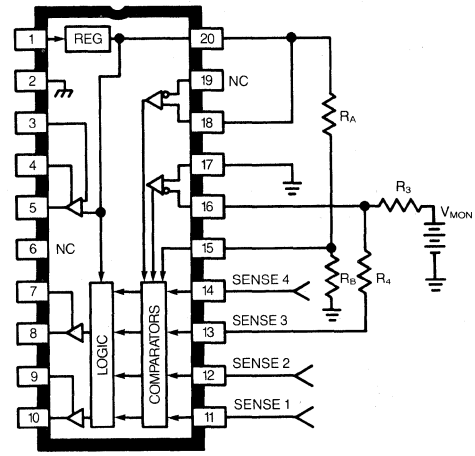
7

UNUSED INPUTS

Unused positive sense channel inputs (pins 3, 11-14) must not be left unconnected. They cannot be tied high (over-voltage fault indication), tied low (under-voltage fault indication), or tied to the internal reference (susceptible to noise and voltage offsets). Unused sense channel inputs should be connected to any operating sense channel input. For example, if channels 1, 2, and 4 are being used, the unused channel 3 sense input (pin 13) should be connected to the SENSE 2 or SENSE 4 input.

Unused negative sense channel inputs (pins 16 and 19) can be left open-circuited *provided* the associated ENABLE inputs (pins 17 and 18) are tied high and the associated positive sense channel inputs (pins 13 and 14) are utilized to monitor positive supplies or are connected as described above.

NEGATIVE SENSE MONITORING
SENSE 3 and 4 Only



Dwg. No. W-187

DESIGN EXAMPLE

As an example, consider the following set of monitoring conditions:

$V_1 = +5\,V\ (+10\%, -5\%)$
$V_2 = +12\,V\ (\pm 10\%)$
$V_3 = +15\,V\ (\pm 5\%)$
$V_4 = +24\,V\ (\pm 10\%)$

The required input dividers are calculated per (1) to yield the resistor divider ratios, $R_2/(R_1 + R_2)$, of: 0.5263, 0.2315, 0.1754 (Note 1), and 0.1157 respectively. The over-voltage threshold, V_{OVT}, would be dictated by the tightest tolerance supply which gives the lowest V_{OVT} from (3). Therefore, $V_{MON(HI)} = 15 \times 1.05 = 15.75\,V$ and $V_{OVT} = 15.75 \times 0.1754 = 2.763\,V$[1]. This is the voltage appearing at the SENSE terminal and is equal to the over-voltage threshold to be set via the resistor ratio at pin 15. From (2), $R_A/(R_A + R_B)$ is calculated to be 0.4096. It is good practice to keep the equivalent external impedances as low as possible, in order to minimize bias current and offset errors. For the purpose of this example, all resistor dividers will be taken to have an equivalent impedance of 1000 ohms. This being the case, the final values are: $R_A = 1.7\,k\Omega$ and $R_B = 2.44\,k\Omega$.

In order to provide accurate over-voltage sensing for the V_1, V_2, and V_4 supplies, resistors are connected from the respective input sense nodes and returned to the 2.5 V reference. Calculation is made by first picking values for the input dividers and then calculating the required value of R_X from (4). Again, assuming 1 kΩ equivalent divider impedances and making the calculations, a summary of results is given below.

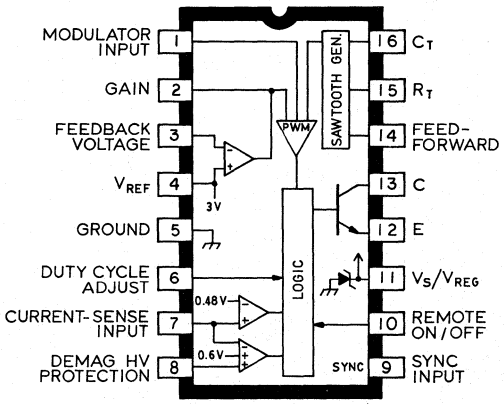
MONITORED SUPPLY	$V_{MON(HI)}$	$V_{MON(LO)}$	R_1	R_2	R_X
+5V(+10%, −5%)	5.5V	4.75V	1.90kΩ	2.11kΩ	2.0kΩ
+12V(±10%)	13.2V	10.8V	4.32kΩ	1.30kΩ	900Ω
+15V(±5%)	15.75V	14.25V	5.70kΩ	1.21kΩ	∞
+24V(±10%)	26.4V	21.6V	8.64kΩ	1.13kΩ	900Ω

1. Note that the number 0.1754 is rounded off. Due to required accuracies in the external dividers, round off numbers only after final resistor values are calculated. For the same reason, use stable high-accuracy metal film resistors. Many applications may benefit from combining the ULN-8131A and functionally trimmed Sprague resistor-capacitor networks.

ULN-8163A AND ULN-8163R
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUITS

FEATURES

- Supply Range of 4.5 V to 14 V; Internal Shunt Regulator for Higher-Voltage Source Operation
- Low Standby Current
- 300 kHz Sawtooth Generator
- Improved Feed-forward Control (4:1 Range)
- Precision Current-Limit Threshold
- Precision (1%) Bandgap Voltage Reference
- Improved Stability Over Temperature
- Direct Pulse-Width Modulator Access
- External TTL-Compatible Synchronization
- Precision Over-Voltage Threshold
- TTL-Compatible Shutdown



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The ULN-8163A and ULN-8163R are switched-mode power supply control circuits featuring low-voltage operation, precision reference, and protective features. Both have a temperature-compensated bandgap reference, an internal error amplifier, wide-range feedforward capability, a high-frequency 300 kHz sawtooth waveform generator, a pulse-width modulator, a variety of protection circuitry, and a 200 mA output driver.

Low-voltage operation and low quiescent current drain make them suitable for automotive and other general SMPS applications such as dc-to-dc converters operating directly from 5 V or 12 V supplies and off-line primary-side control.

The ULN-8163A is supplied in a 16-pin dual in-line package with a copper lead frame for enhanced power dissipation ratings for operation over a temperature range of −20°C to +85°C. The ULN-8163R is furnished in a 16-pin hermetically sealed glass/ceramic package which will withstand severe environmental contamination.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

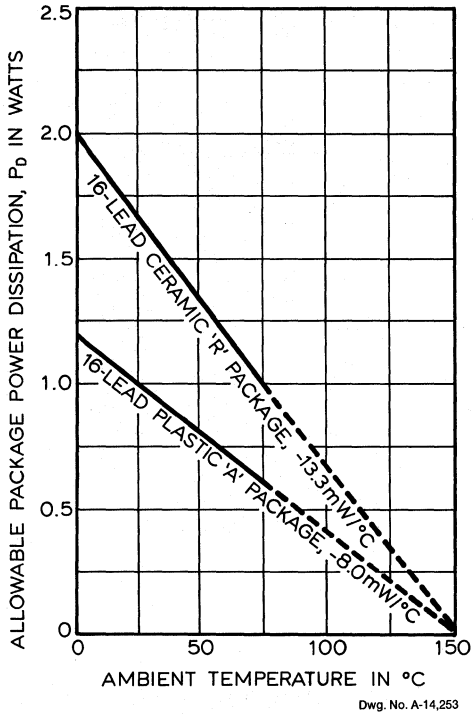
Supply Voltage, V_S	(See Note)
Supply Current, I_{REG}	30 mA
Output Current, I_C (peak)	200 mA
(continuous)	100 mA
Reference Output Current, I_{REF}	10 mA
Logic Input Voltage, V_9, V_{10}	8.0 V
Package Power Dissipation, P_D	
(ULN-8163A)	2.1 W*
(ULN-8163R)	1.7 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate linearity to 0 W at T_A = +150°C

NOTE: Maximum allowable supply voltage is dependent on value of external current limiting resistor: 14 V at 0 Ω.

7

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



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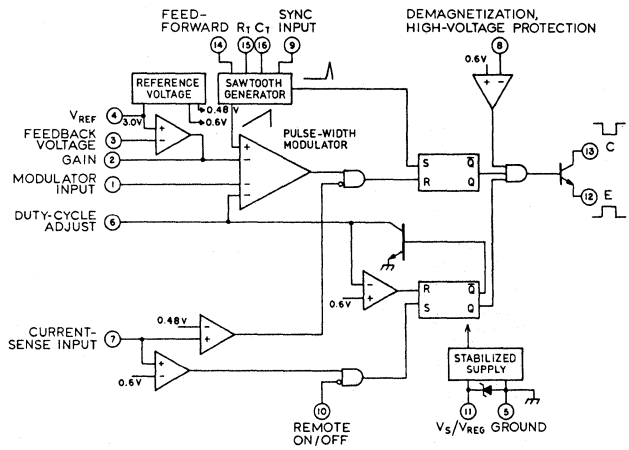
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = 12 V, f_o = 40 kHz (unless otherwise specified).

Characteristic	Test Pin	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Clamp Voltage	11	I_S = 10 mA	14	—	18	V
	11	I_S = 30 mA	15	—	19	V
Supply Current	11	$V_{12} = V_{13} = 0$	2.0	5.5	7.0	mA
REFERENCE SECTION						
Internal Reference, V_{REF}	4	T_A = +25°C	2.97	3.00	3.03	V
	4	Over Operating Temp. Range†	2.94	—	3.06	V
Temperature Coefficient of V_{REF}	4		—	±100	—	ppm/°C
Line Regulation	4	6 V < V_S < 12 V	—	1.0	3.0	mV/V
Load Regulation	4	0 < I_{REF} < 5 mA	—	3.0	10	mV

Note: Negative current is defined as coming out of (sourcing) the specified device pin.
†These parameters, although guaranteed over the operating temperature range, are tested at T_A = +25°C only.
*These parameters are tested to a lot sample plan only.
°Any output other than zero is not allowed.

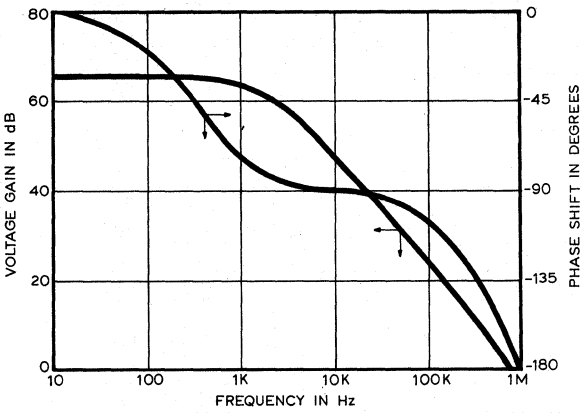
ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_S = 12\ V$, $f_o = 40\ kHz$ (unless otherwise specified).

Characteristic	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
OSCILLATOR SECTION						
Min. Oscillator Frequency*	15, 16	$R_T = 5\ M\Omega$, $C_T = 15000\ pF$	—	—	50	Hz
Max. Oscillator Frequency	15, 16	$R_T = 2.3\ k\Omega$, $C_T = 500\ pF$	200	300	—	kHz
Initial Oscillator Accuracy	15, 16	$R_T = 5\ k\Omega$	—	±2.0	—	%
Voltage Stability	15, 16	$5\ V < V_S < 12\ V$	—	0.2	0.5	kHz/V
Temperature Stability			—	30	100	ppm/°C
MODULATOR/COMPARATOR SECTION						
Modulator Input Current	1	$V_1 = 1.0\ V$	—	−1.0	−3.0	μA
Maximum Duty Cycle	12	$V_6 < 3.0\ V$	95	—	99	%
Minimum Duty Cycle•	12	$V_6 > 0.9\ V$	—	—	0	%
Duty Cycle Accuracy	12	$V_6 = 2.0\ V$	44	47	50	%
Propagation Delay	6-12		—	200	—	ns
Input Current, Duty Cycle Control	6		—	−1.0	−3.0	μA
PROTECTIVE FUNCTIONS						
Under-Voltage Lockout	11-12		3.80	4.0	4.25	V
Start Threshold	11-12		4.25	4.5	4.75	V
Over-Voltage Threshold	8-12		570	600	630	mV
Over-Voltage Delay	8-12		—	200	500	ns
Over-Voltage Input Current	8		—	2.0	5.0	μA
EXTERNAL SYNCHRONIZATION						
Sync Input OFF Voltage	9		0	—	0.8	V
Sync Input ON Voltage	9		2.0	—	—	V
Sync Input Current	9	$V_9 = 0\ V$, $T_A = +25°C$	—	−85	−125	μA
	9	$V_9 = 0\ V$, Over Operating Temp. Range†	—	—	−125	μA
REMOTE						
Remote OFF Voltage	10		0	—	0.8	V
Remote ON Voltage	10		2.0	—	—	V
Remote Input Current	10	$T_A = +25°C$	—	−85	−125	μA
	10	Over Operating Temp. Range†	—	—	−125	μA
CURRENT LIMITING						
Input Current	7	$V_7 < 450\ mV$	—	−5.0	−20	μA
Inhibit Delay*	7	One Pulse, 20% Overdrive at $I_C = 40\ mA$	—	400	600	ns
Trip Levels	7	Shutdown/Slow Start	570	600	630	mV
	7	Current Limit	455	480	505	mV
Shutdown/Current Limit Ratio	—		1.15	1.25	1.40	—
ERROR AMPLIFIER						
Error-Amplifier Gain	3-2	Open Loop	60	66	—	dB
Error-Amplifier Feedback Resistance	2		10	—	—	kΩ
Small-Signal Bandwidth	3-2		700	—	—	kHz
Input Offset Voltage	3		−10	—	10	mV
Input Current	3		—	0.1	1.0	μA
Power Supply Rejection			60	70	—	dB
OUTPUT STAGE						
Output-Saturation Voltage	13	$V_{CE(SAT)}$ at $I_C = 10\ mA$, $V_E = 0$	—	—	750	mV
		$V_{CE(SAT)}$ at $I_C = 100\ mA$, $V_E = 0$	—	—	1.0	V
Output Voltage	12		—	—	30	V
Output Source Compliance	11	$5\ V < V_S < 14\ V$	$V_S - 3$	—	—	V

Note: Negative current is defined as coming out of (sourcing) the specified device pin.
†These parameters, although guaranteed over the operating temperature range, are tested at $T_A = +25°C$ only.
*These parameters are tested to a lot sample plan only.
•Any output other than zero is not allowed.

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER VOLTAGE GAIN AND PHASE SHIFT AS FUNCTIONS OF FREQUENCY



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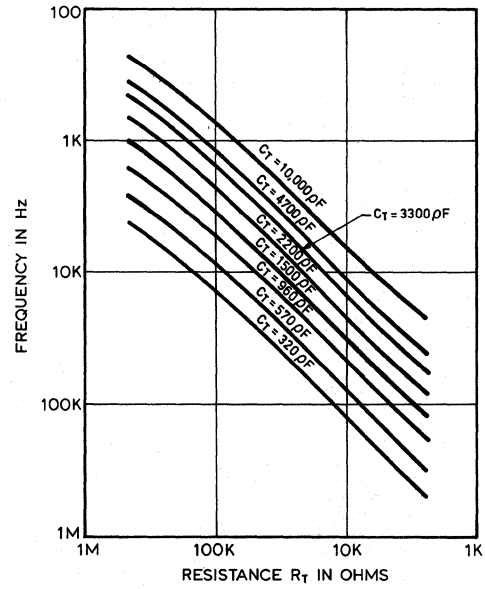
FREQUENCY AS A FUNCTION OF R_T



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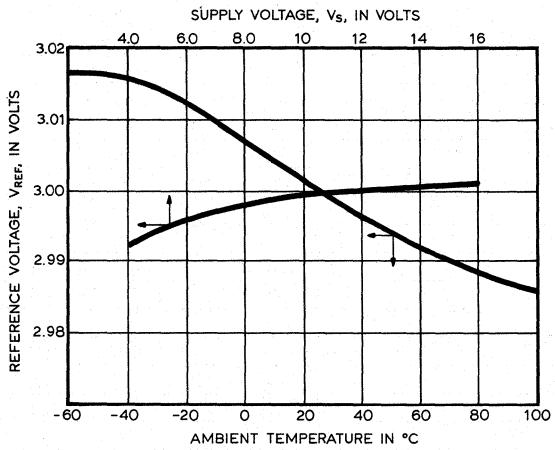
REFERENCE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



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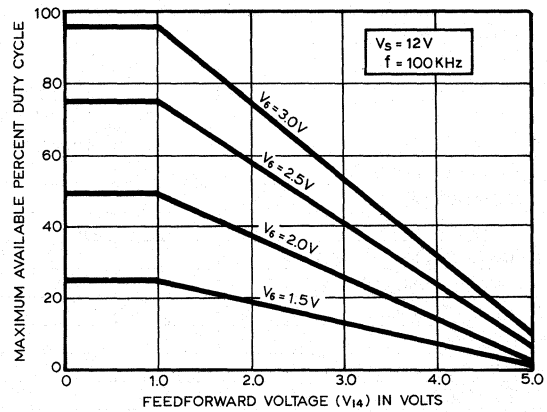
MAXIMUM DUTY CYCLE AS A FUNCTION OF FEED FORWARD VOLTAGE



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TYPICAL APPLICATION

The boost converter shown in Figure 1 is an example of a step-up type dc-to-dc converter that might be used in an automotive application. The ULN-8163A is used due to its wide supply operating range, over-voltage protection, and current-limiting circuits. The application shown will produce an output of 30 V from an input source which varies from 8 V to 24 V (typical of automotive requirements). By changing the feedback, the output switch, and the storage inductor, a wide range of output voltages and power levels can be produced.

The IC supply requirements allow powering the controller through a 470 Ω current-limiting resistor. A 0.1 μF capacitor provides adequate supply bypassing. Over the normal operating range of 8 V to 16 V, the ULN-8163A is voltage driven. The low quiescent current of the circuit, coupled with the low dc current required to drive the power FET switch, results in an IR drop of typically 2 V in the supply resistor, which means that the circuit will remain active at input supply levels as low as 6.5 V. The output regulation may be compromised at these low voltages, depending on the load requirements. At supply voltages above approximately 16 V, the controller will operate in the current-driven mode. The usual maximum supply voltage of 18 V results in a power dissipation requirement of only 10 mW in the supply resistor. With a 24 V supply, the supply resistor dissipation rises to 136 mW, worst case, suggesting the 250 mW resistor. The internal Zenor diode, plus external RC network, provides the additional benefit of excellent protection against over-voltage transients.

The output voltage is set by the feedback resistor divider R_1, R_2. Error amplifier compensation is provided by the RC network connected between pins 2 and 3.

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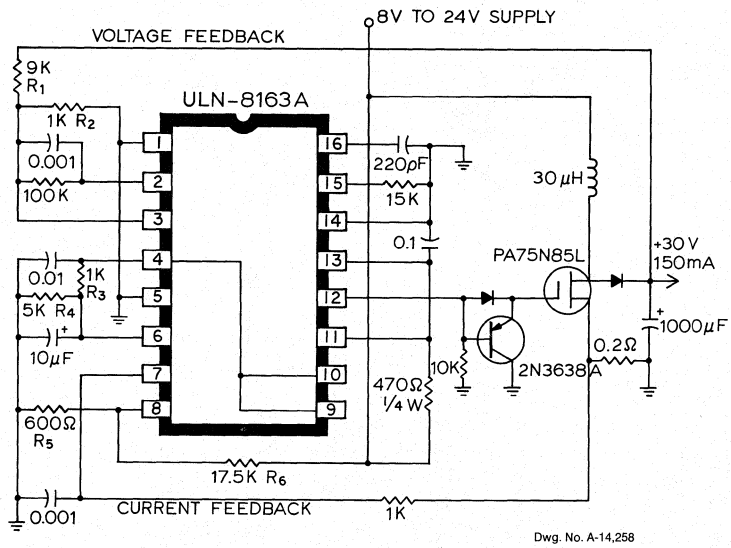

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FIGURE 1
BOOST CONVERTER

The supply operates at a frequency of 100 kHz, set by the timing components at pins 15 and 16. The maximum available duty cycle is set up by the resistor ratio R_3:R_4. The setting is determined by the output voltage and required minimum supply input and in this application is set at 75 percent by a 5:1 resistor divider producing 2.5 V at pin 6.

The over-voltage function provides protection to the power switch during over-voltage transients. This is accomplished by setting the R_5, R_6 divider so that, at some supply voltage, a pin 8 voltage of 600 mV disables the circuit. In this example, the over-voltage trip threshold is at a supply voltage of 18 V. Adjustment of the divider ratio allows the threshold to be adjusted as required.

The output switch is a G.I. PA75N85L n-channel power FET. Alternatively, an IR520 or MTP10N10 can be substituted. The power FET switch results in very low current drive requirements, which significantly eases the supply requirements on the control circuitry. The gate turn-ON is done directly by the sourcing output of the ULN-8163A through the diode. The 2N3638A PNP provides a very simple, low-cost, and effective means of providing rapid (<50 ns) turn-OFF. The value of the storage inductor is determined by the output power requirement and frequency of operation.

For increased output current requirements, a Darlington bipolar power switch can be implemented by using the output drive circuit of Figure 2. In this case, the output collector requires a separate supply return from pin 13 to the input supply.

Additionally, the output connection for a voltage buck converter is shown in Figure 3. With the same 8 V to 24 V supply, the buck converter can be used to provide a high-efficiency 2.5 V to 5 V supply. Considerable literature exists that analyzes both the buck and boost converters.

FIGURE 2
HIGH-CURRENT BOOST CONVERTER

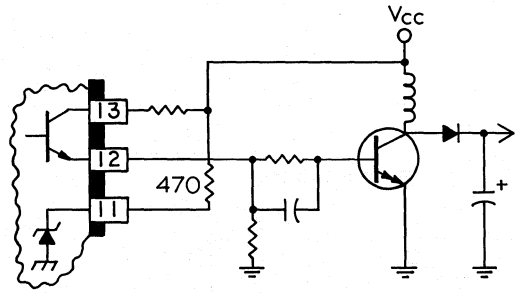

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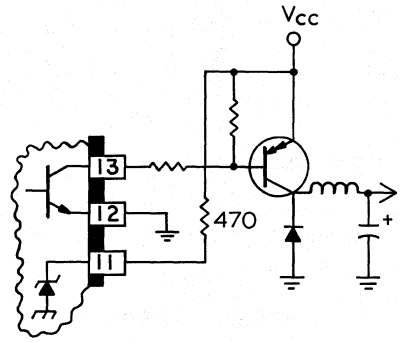
FIGURE 3
BUCK CONVERTER



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AN ELECTRONIC LAMP MONITOR

REQUIREMENTS

There are several requirements for a lamp monitoring system. The system should be able to monitor all types of exterior lamps on the automobile; the number of lamps must not be critical to the design. The system must be easy to assemble; it should be simple in design so that it can be repaired in the field with minimal training of personnel; it must be reliable and must be able to withstand the electrical and environmental conditions to which the vehicle is subjected. There should be minimal change from one car line to another, and from one model year to another. Most importantly, the unit cost should be reasonable.

LAMP MONITORING METHODS

Several methods of detecting lamp failure have been examined by the automotive industry. In one, reed relays mounted close to the wiring harness are closed by the electromagnetic force produced by the lamp current. If a lamp fails, the relay opens, resulting in an indication on the dashboard. The system has inherent problems, including a lack of uniformity of the relays, tight tolerances on the proximity of the relays to the wiring assemblies, and the effects of vibration in the automobile.

Another method of monitoring lamps involves the use of phototransistors (Figure 1). These light-sensitive solid-state devices detect the presence of light at each monitored lamp. The signals from each lamp are brought to a common switch, which controls the operation of an indicator on the dash. This monitoring system is unattractive to the user because of cost, difficulty in placement of the sensing devices, inability to detect a single failure in a dual filament lamp, and the need for calibration of devices for various types of lamps.

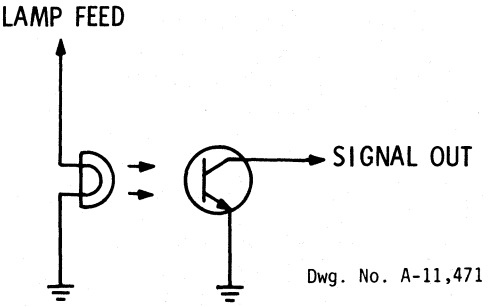


Figure 1
PHOTOTRANSISTOR SYSTEM

One of the more frequently used systems employs fiber optics (Figure 2). The fiber-optic system uses a plastic or glass fiber that transmits light and gives a positive-function indication for each of the lamps monitored. However, this system is used only in applications requiring the monitoring of a small number of lamps, since the cost of materials and of routing fiber optics is prohibitively expensive.

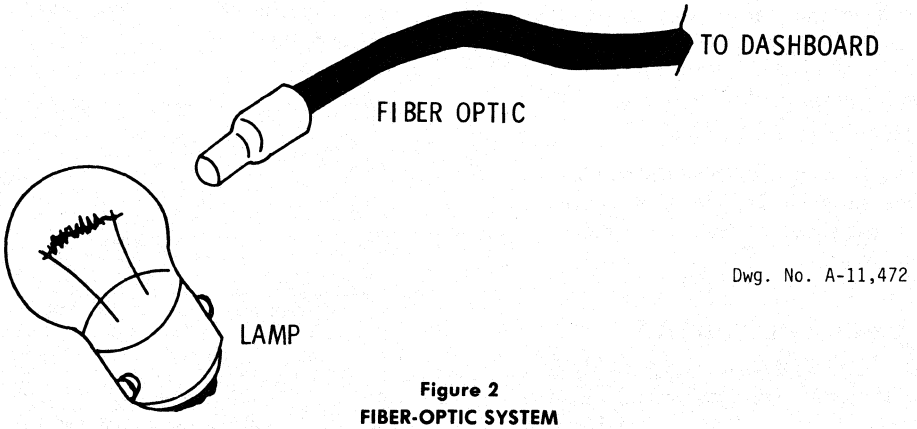


Figure 2
FIBER-OPTIC SYSTEM

SOLUTION

The Sprague Type ULN-2435A electronic lamp monitor overcomes technical problems discussed above while taking advantage of the low cost of integrated circuits. This integrated circuit monitors all types of exterior lamps and provides five outputs capable of driving light-emitting diodes that indicate the location of automotive lamp failure.

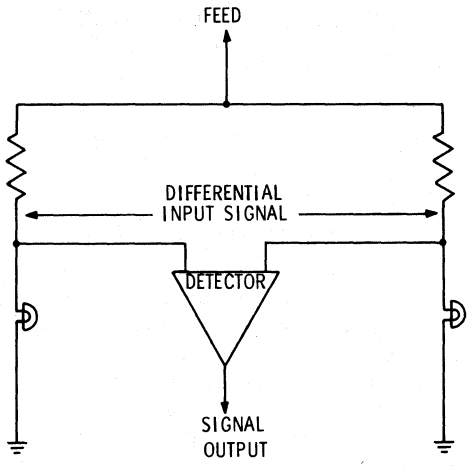


Figure 3
BRIDGE MONITORING SYSTEM

The principle of operation is that of a simple bridge circuit (Figure 3) in which the top two legs of the bridge are the wiring-assembly resistance or discrete resistors. The bottom legs of the bridge circuit are the monitored lamps. Four differential amplifiers sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the various lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

A sixth output driver gives an indication if any of the monitored lamps fail. This output can be used to drive an audible signaling device or a centrally-located warning lamp.

CIRCUIT DESCRIPTION

A simplified detector is shown in Figure 4. Q1 and Q2 form a differential amplifier. The amplified differential signal is applied at Point A-B to threshold

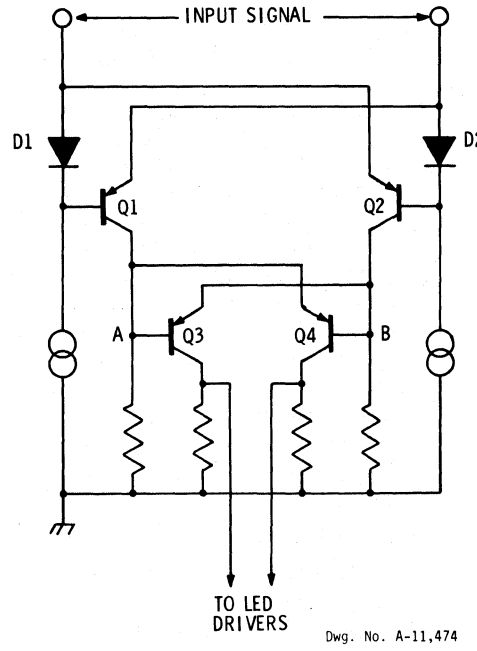


Figure 4
SIMPLIFIED DETECTOR

detectors Q3 and Q4, which drive the LED driver transistors. D1 and D2 perform the dual function of level-shifting the input signal and establishing required bias currents for Q1 and Q2. Since the supply current is derived from the lamp lines, standby current is reduced to zero when the lamps are turned off.

The use of PNPs in the detectors reduces the system's susceptibility to high-frequency noise. Figure 5 shows a comparison of frequency response for a monolithic NPN transistor and a monolithic PNP transistor.

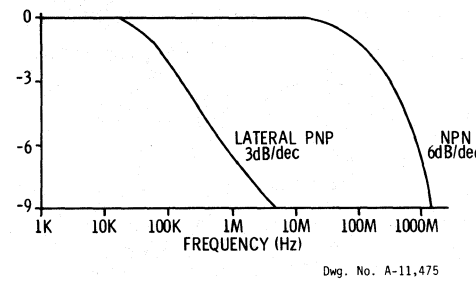


Figure 5
FREQUENCY RESPONSE

A block diagram of a typical application of Type ULN-2435A is depicted in Figure 6. In this application, eight lamps and three fuses are monitored. The stop-lamp fuse (A) is monitored by the circuitry at Pin 4. If the fuse blows, the LEDs connected to pins 10 and 13 turn ON. By using separate fuses for the park lamps and tail/marker-lamp circuits, detectors 1 and 2 can double as fuse monitors. If, for example, fuse B blows, detectors 1 and 2 turn on the LEDs connected to pins 1 and 16. An additional input, pin 6, is used to test the LEDs and the master indicator during cranking.

The simplistic design of this system enables easy installation in an automobile. No external components are required, other than the LED indicators and the voltage-dropping resistors, to complete the system. The integrated circuit may be mounted on a printed wiring board. Depending on lamp current, the copper runs of a printed wiring board might be used as the top legs of the bridge circuit. A failure within the integrated circuit will not affect lamp operation or other automotive functions.

TRANSIENT PROTECTION

In laying out the integrated circuit, careful consideration was given to providing on-chip voltage-transient protection. The LED driver transistors, for example, were designed to withstand an 80-volt load-dump transient. The detector inputs are also designed to withstand 80 volts. In addition, the inputs to the detectors are essentially grounded through the low-resistance lamps being monitored, which further protects the integrated circuit from transients. Reverse-battery protection is included on the chip. In the event of a battery reversal, the PNPs provide inherent protection, while the dielectrically-isolated resistors provide additional safeguards.

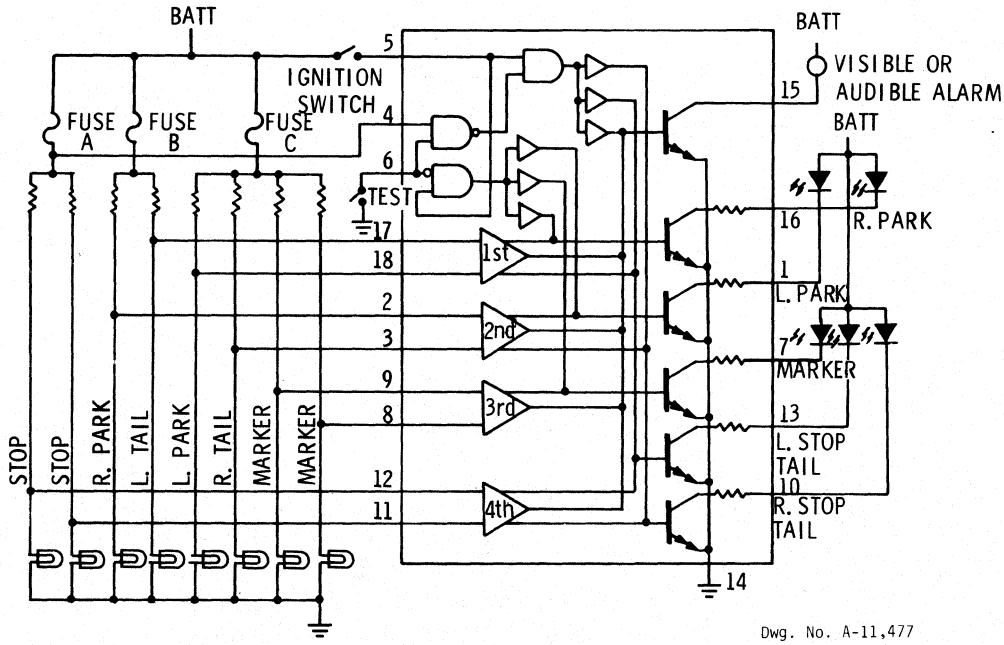


Figure 6
TYPICAL APPLICATION

SECTION 8—PACKAGE INFORMATION

Package Thermal Characteristics

Package Designator	Package Type	Lead Material	$R\Theta_{JA}$† (°C/W)	$R\Theta_{JC}$† (°C/W)
A	14-Pin Plastic DIP	Copper	60	38
A	16-Pin Plastic DIP	Copper	60	38
A	18-Pin Plastic DIP	Copper	55	25
A	20-Pin Plastic DIP	Copper	55	25
A	22-Pin Plastic DIP	Copper	50	21
A	28-Pin Plastic DIP	Copper	40	16
A	40-Pin Plastic DIP	Copper	36	—
B	8-Pin Semi-Tab Plastic DIP	Copper	75	13*
B	14-Pin Semi-Tab Plastic DIP	Copper	45	13*
B	16-Pin Semi-Tab Plastic DIP	Copper	45	13*
B	22-Pin Semi-Tab Plastic DIP	Copper	40	13*
EK	20-Contact Sq. Hermetic LCC	N.A.	110	14-19
EK	28-Contact Sq. Hermetic LCC	N.A.	100	10-19
EK	44-Contact Sq. Hermetic LCC	N.A.	—	7.5-19
EL	18-Contact Rect. Hermetic LCC	N.A.	—	—
EP	20-Lead Square Plastic LCC	Copper	75	28
EP	28-Lead Square Plastic LCC	Copper	65	16
EP	44-Lead Square Plastic LCC	Copper	50	15
H	8-Pin Hermetic DIP	Kovar	120	40
H	14-Pin Hermetic DIP	Kovar	90	20
H	16-Pin Hermetic DIP	Kovar	90	20
H	18-Pin Hermetic DIP	Kovar	75	20
H	22-Pin Hermetic DIP	Kovar	65	20
L	8-Lead SOIC	Copper	165	45
L	14-Lead SOIC	Copper	118	29
L	16-Lead SOIC	Copper	110	27
LB	20-Lead Semi-Tab SOIC	Copper	46	7.9*
LW	16-Lead SOIC	Copper	97	—
LW	18-Lead SOIC	Copper	97	—
LW	20-Lead SOIC	Copper	87	17
M	8-Pin Mini DIP	Copper	80	55
R	14-Pin CerDIP	Kovar	75	—
R	16-Pin CerDIP	Kovar	75	—
R	18-Pin CerDIP	Kovar	65	—
W	12-Lead Power Tab SIP	Copper	24	3.0*
Z	5-Lea i Power Tab SIP	Copper	40	4.5*

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods. Where differences exist, the detail specificatior takes precedence.

†$G\Theta_{JA} = 1/R\Theta_{JA}$ and $G\Theta_{JC} = 1/R\Theta_{JC}$

*$R\Theta_{JT}$

Interface and Linear ICs

For Surface-Mount Applications

The Sprague Semiconductor Group offers many of its peripheral power interface and linear integrated circuits in small-outline packages and leaded or leadless chip carriers for use in high-density surface-mount applications. Popular products presently available include industry-standard Series ULN-2000, ULN-2060/70, ULN-2800, UDN-2980, and Series UCN-5800 peripheral power drivers for printers, displays, motors, solenoids, relays, and other power interface; Series UDS-5790 PIN-diode drivers; and custom telecommunications circuits. Additional devices will become available as needs are developed.

SURFACE-MOUNT PACKAGE AVAILABILITY

Leads	Package Style	Industry Pkg. Outline	Tape & Reel Width × Pitch (mm)	Sprague P/N Suffix
8	SO-8	MS-012AA	12 × 8	L
14	SO-14	MS-012AB	16 × 8	L
16	SO-16	MS-012AC	16 × 8	L
	SOL-16	MS-013AA	16 × 12	LW
18	SOL-18	MS-013AB	—	LW
	LCC-18	M38510/C-9	24 × 12	EL
20	SOL-20	MS-013AC	24 × 12	LW
	SOL-20B	MS-013AC	24 × 12	LB
	LCC-20	M38510/C-3	16 × 12	EK
	PLCC-20	MO-047AA	16 × 12	EP
28	LCC-28	M38510/C-4	24 × 16	EK
	PLCC-28	MS-007AA	24 × 16	EP
44	LCC-44	M38510/C-5	32 × 44	EK
	PLCC-44	MS-007AB	32 × 44	EP

LCC = Hermetic Leadless Chip Carrier.
PLCC = Plastic Leaded Chip Carrier.
SO = Small Outline IC, 0.15" Gull-Wing.
SOL = Small Outline IC, 0.30" Gull-Wing.

The SOL-20B package is a miniature "bat wing" package (12 active connections plus eight tab/ground connections) for use in surface-mount, high package-power dissipation requirements. Similar designs are being addressed for use with plastic leaded-chip carriers to provide multi-pin packages with minimized board space requirements and with junction-to-tab thermal resistances of less than 5°C/W. The unique Sprague PLCC power package construction will be compatible with other PLCC products and will allow the easy attachment of external heat sinks for highest package power dissipation. Except for the SOL-18 package, all devices can be supplied in tape and reel to EIA 481A.

SURFACE-MOUNT PACKAGING FOR ICs

Part Number	Package	Description
ULN-2001 through 2005L	SO-16	7 Darlingtons, 50 V/350 mA
ULN-2021L through 2025L	SO-16	7 Darlingtons, 95 V/350 mA
ULS-2001EK through 2005EK	LCC-20	7 Darlingtons, 50 V/350 mA
ULN-2046L	SO-14	5 NPN Transistors
ULN-2061L	SO-8	2 Darlingtons, 50 V/1.25 A
ULN-2064/68/74LB	SOL-20B	4 Darlingtons, 50 V/1.25 A
ULN-2081L	SO-16	7 NPN Transistors, Common Emitter
ULN-2082L	SO-16	7 NPN Transistors, Common Emitter
ULN-2083L	SO-16	5 Independent NPN Transistors
ULN-2086L	SO-14	5 NPN Transistors
ULN-2204LW	SOL-16	AM/FM Radio System
UDN-2580EP	PLCC-20	8 Darlingtons, 50 V*/ – 350 mA
UDN-2580LW	SOL-18	8 Darlingtons, 50 V*/ – 350 mA
UDN-2585EP	PLCC-20	8 Drivers, 25 V/ – 120 mA
UDN-2585LW	SOL-18	8 Drivers, 25 V/ – 120 mA
UDN-2595EP	PLCC-20	8 Drivers, 20 V/100 mA
UDN-2595LW	SOL-18	8 Drivers, 20 V/100 mA
ULN-2801LW through 2804LW	SOL-18	8 Darlingtons, 50 V/350 mA
ULN-2821LW through 2825LW	SOL-18	8 Darlingtons, 95 V/350 mA
ULS-2803EK and 2804EK	LCC-20	8 Darlingtons, 50 V/350 mA
UDN-2933LB	SOL-20B	3-Channel Half-Bridge, 30 V/ ± 800 mA
UDS-2982EK	LCC-20	8 Darlingtons, 50 V/ – 350 mA
UDN-2982EP	PLCC-20	8 Darlingtons, 50 V/ – 350 mA
UDN-2982LW	SOL-18	8 Darlingtons, 50 V/ – 350 mA
UDS-2984EK	LCC-20	8 Darlingtons, 80 V/ – 350 mA
UDN-2984EP	PLCC-20	8 Darlingtons, 80 V/ – 350 mA
UDN-2984LW	SOL-18	8 Darlingtons, 80 V/ – 350 mA
UDN-2993LB	SOL-20B	Dual 40 V/500 mA H-Bridge
ULN-3781L	SO-8	Low-Voltage Audio Power Amplifier
ULN-3782L	SO-8	Dual Audio Power Amplifier
ULN-3820LW	SOL-20	C-QUAM® AM Stereo Decoder
ULN-3839LW	SOL-16	AM Radio System
ULN-3841LW	SOL-20	AM Signal Processor
ULN-3842LW	SOL-20	AM/FM Signal Processor
ULN-3859EP	PLCC-20	Low-Power, Narrow-Band FM IF

*Increased voltage ratings available.
®Registered trademark of Motorola, Inc.

SURFACE-MOUNT PACKAGING FOR ICs

Part Number	Package	Description
ULN-3862LW	SOL-16	FM IF System
ULN-3883LW	SOL-18	FM Communications IF/Audio System
UCN-4807EP and 4808EP	PLCC-20	Addressable, 8-Channel Latched Drivers
UDN-5707EP	PLCC-20	Quad NAND Driver, 80 V/300 mA
UDN-5725L	SO-14	Dual Power Driver, 70 V/1 A
UCS-5791EK	LCC-18	Quad PIN Diode Driver, 120 V/300 mA
UCN-5800L	SO-14	4-Bit Latch, 50 V/350 mA
UCN-5801EP	PLCC-28	8-Bit Latch, 50 V/350 mA
UCN-5810EP	PLCC-20	10-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5810LW	SOL-18	10-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5812EP	PLCC-28	20-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5815EP	PLCC-28	8-Bit Latch, 60 V/ – 25 mA
UCN-5816EP	PLCC-28	4-Bit Decoder/Latch, 60 V/350 mA
UCN-5818EP	PLCC-44	32-Bit SR/Latch, 60 V*/ – 25 mA
UCN-5821EP through 5823EP	PLCC-20	8-Bit SR/Latch, to 100 V/350 mA
UCN-5832EP	PLCC-44	32-Bit SR/Latch, 40 V/100 mA
UCN-5833EP	PLCC-44	32-Bit SR/Latch, 30 V/100 mA
UCN-5841EP through 5843EP	PLCC-20	8-Bit SR/Latch, to 100 V/350 mA
UCN-5851EP and 5852EP	PLCC-44	32-Bit Serial-In, 225 V/100 mA
UCN-5853EP and 5854EP	PLCC-44	32-Bit SR/Latch, 60 V*/ ± 20 mA
UCN-5881EP	PLCC-44	Dual 8-Bit Latch, 20 V/25 mA
UCN-5895EP	PLCC-20	8-Bit SR/Latch, 50 V/ – 120 mA
UCN-5895LW	SOL-18	8-Bit SR/Latch, 50 V/ – 120 mA
UDN-6118LW	SOL-18	8 Drivers, 80 V*/ – 25 mA
ULN-8130LW	SOL-18	Supervisory Systems Monitor
ULN-8131LW	SOL-20	Supervisory Systems Monitor
ULN-8163LW	SOL-16	SMPS Controller
NE5560D	SOL-16	SMPS Controller
NE5568D	SO-8	SMPS Controller
SG3525A	SOL-16	SMPS Controller
SG3526	SOL-18	SMPS Controller
SG3527A	SOL-16	SMPS Controller
TL594CDW	SOL-16	SMPS Controller
TL595CDW	SOL-18	SMPS Controller

*Increased voltage ratings available.

OPERATING AND HANDLING PRACTICES FOR MOS INTEGRATED CIRCUITS

Handling Practices — Packaged Devices

Sprague Electric incorporates input protection diodes in all of its MOS/CMOS devices. Because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.
2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.
3. Devices should not be inserted into or removed from test stations unless the power is off.
4. Neither should signals be applied to the inputs while the device power supply is in an off condition.
5. Unused input leads should be committed to either V_{SS} or V_{DD}.

Handling Practices — Die

A conductive carrier should be used in order to avoid differences in voltage potential.

Automatic Handling Equipment

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aid here and are available commercially. This method is very effective in eliminating static electricity problems.

Ambient Conditions

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

Alert Failure Modes

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.
2. Shorted or 'blown' open gates.
3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

MOUNTING POWER TAB DEVICES

Power-tab packages are efficient thermal dissipators when properly utilized. In application, the following precautions should be taken:

1. Always fasten the tab to the heat sink before the leads are soldered to fixed terminals.
2. Strain relief must be provided if there is any probability of axial stress to the leads.
3. Thermal grease (Dow Corning 340 or equivalent) should always be used. Thermal compounds are better heat conductors than air but not a good substitute for flat mating surfaces.
4. The mounting surface should be flat to within 0.002 inch/inch (0.05 mm/mm).
5. "Brute Force" mounting to poorly finished heat sinks can cause internal stresses which damage silicon chips and insulation parts. Mounting torque should be between 4 and 8 inch pounds (0.45 to 0.90 Nm.)
6. The mounting holes should be as clean as possible with no burrs or ridges.
7. Use appropriate hardware including a lock washer or torque washer.
8. If insulating bushings are used, they should be of dialylphthalate, fiberglass-filled polycarbonate, or fiberglass-filled nylon. Unfilled nylon should be avoided.

THERMAL DESIGN FOR PLASTIC INTEGRATED CIRCUITS

PROPER THERMAL DESIGN is essential for reliable operation of many electronic circuits. Under severe thermal stress, leakage currents increase, materials decompose, and components drift in value or fail. Present-day linear integrated circuits are capable of delivering 5 to 10 watts of continuous power. Previously, such power levels came only with discrete metal can power transistors. It was relatively easy to determine the thermal resistance of these devices and attach a massive heat sink. However, in many markets, economic factors now dictate the use of molded dual in-line plastic packaged monolithic circuits. The guidelines to be discussed will provide the circuit design engineer with information on maintaining junction temperature below a safe limit under worst case conditions.

Design Considerations

Four factors must be considered before the required heat-sinking can be determined. These are:

1. Maximum ambient temperature
2. Maximum allowable chip temperature
3. Junction-to-ambient thermal resistance
4. Continuous chip power dissipation

Maximum ambient temperature for the integrated circuit is normally between +70°C and +85°C and is usually dependent on the case material. In most applications, however, the limiting factor is the associated discrete components and a limit of about +50°C is specified. The maximum allowable chip temperature is usually +150°C for silicon.

Thermal resistance is the all-important design factor. It is composed of several individual elements, some of which are determined by the integrated circuits manufacturer, and some by the user.

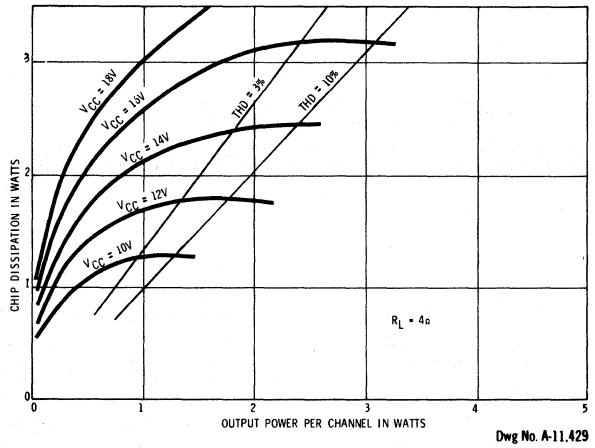
Chip Power Dissipation

The chip power dissipation should be obtainable from the manufacturer's specifications. In most applications it is a variable and determined by the user when he specifies the circuit variables.

A typical example is a dual 2-watt audio power amplifier. Power dissipation is determined by the load impedance, the required peak output power, the acceptable amount of total harmonic distortion (THD), and the supply voltage (V_{CC}). This is illustrated in Figures 1-3. Note that for a given supply voltage, the chip dissipation may be greatest at some point below the peak output power rating and must be considered.

As shown in the figures, a peak output power of 2 watts per channel with 3% maximum THD would mean a chip power dissipation of about 2.7 W and a V_{CC} of 15 V with a load impedance of 4Ω, or 1.8 W and 15 V at 8Ω, or 1.4 W and 19 V at 16Ω. In general, the highest load impedance for a given output power is the most desirable (within the output voltage capability of the device).

PACKAGE INFORMATION



Dwg No. A-11,429

Figure 1

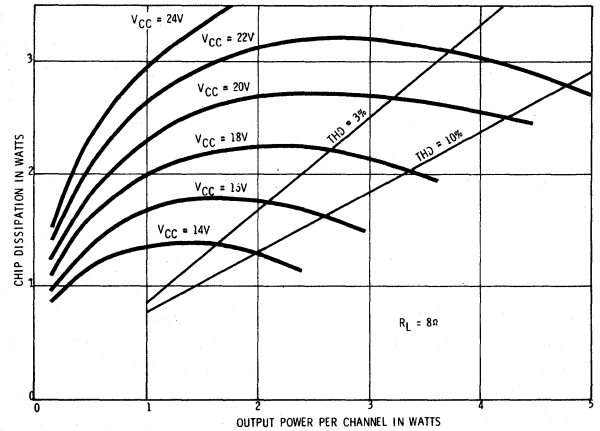


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Figure 2

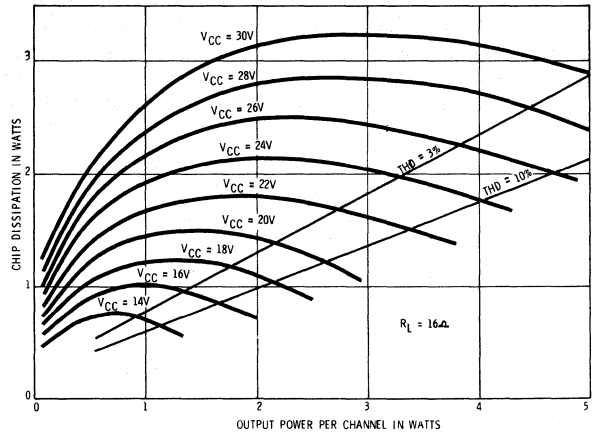

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Figure 3

Heat Dissipation

In any circuit involving power, a major design objective is to reduce the temperature of the components in order to improve reliability, reduce cost, or improve operation. The logical place to start is with the heat-producing component itself. First, keep the amount of heat generated to a minimum. Second, get rid of the heat that must be generated.

Heat generation can be minimized through proper circuit design. Heat dissipation is a function of thermal resistance.

With the typical discrete component, heat dissipation can be accomplished by fastening it directly to the chassis. Dual in-line plastic packaged integrated circuits, however, are quite a bit different. Their shape is not conducive to fastening directly to the chassis, they are normally installed in a plastic socket or on a printed wiring board, and the heat producing chip is not readily accessible.

Some users specify unusual packages so as to get the heat sink as close as possible to the chip and/or provide an attachment point for an external heat sink. A common factor in many of these special designs is that the lead frame is an integral part of the heat sink.

Since the plastic package may have a thermal resistance of between 50 and 100°C/W and the lead frame a thermal resistance of only 10 to 20°C/W, this would seem like the best route to go.

Standard Packages

The most common lead frame material has been Kovar (an iron-nickel-cobalt alloy). Its coefficient of expansion is close to that of silicon thereby minimizing mechanical stresses. However, Kovar has a relatively high thermal resistance and consequently is not suitable for standard lead frames in high power dissipation circuits. For these applications, copper or copper-alloy lead frames should be used. Additionally, some type of added heat sinking may be necessary. Thus lead frame configurations are being altered from the standard 14-pin or 16-pin designs.

Rapidly becoming an industry standard is the "bat-wing" package. This package is the same size as a 14-pin dual in-line package, but the center portion of the frame is left as tabs, measuring about ¼" square. These tabs can be soldered, welded, or bolted to a heat sink, or inserted directly into some sockets. The worst case thermal resistance of various lead frames (Θ_{JC}) is given below.

Lead Frame	Thermal Resistance
14-pin Kovar	47°C/W
14-pin copper	19°C/W
"Bat-wing"	11°C/W

Which Heat Sink?

If the integrated circuit manufacturer has done his job well, the chip-to-ambient thermal resistance will be minimized for maximum chip power dissipation. It would appear that even the Kovar lead frame would be adequate for most applications. However, the total thermal resistance (Θ_{JA}) is also dependent on a stagnant layer of air at the lead frame-ambient interface which will support a temperature gradient. The total thermal resistance of a non-heat sinked dual in-line plastic package is therefore much higher. Since air is a natural thermal insulator, maximum heat transfer is through convection and the total thermal resistance will decrease some at high power levels.

Lead Frame	Total Thermal Resistance	Max. Power Diss. (W) at 50°C T_A, 150°C T_J
14-Pin Kovar	120°C/W	0.83
14-Pin Copper	72°C/W	1.39
"Bat-Wing"	50°C/W	2.0

Ignoring any safety margin and device performance, even the "bat-wing" is now only barely adequate for most applications. The obvious solution is the use of an external heat sink.

Referring to Figures 4 and 5, the thermal resistance requirement of the heat sink is found at the junction of the specified chip power dissipation and maximum ambient temperature. These curves are typical of those furnished in many monolithic integrated circuit data sheets. Actual performance in a specific situation depends on factors such as the proximity of objects interfering with air flow, heat radiated or convected from other components, atmospheric pressure, and humidity. A good safety factor is therefore in order.

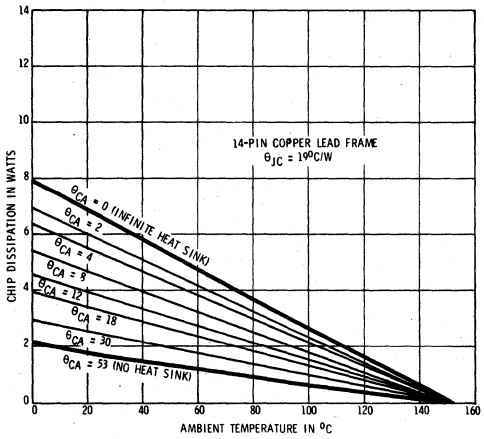


Figure 4

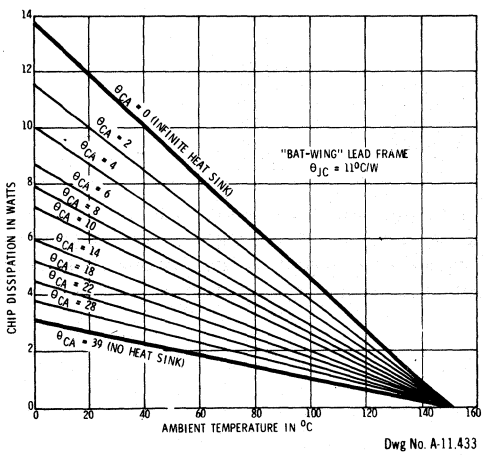


Figure 5

Heat sinks for plastic dual in-line packages can be of almost unlimited variety in design, material, and finish. Economics will normally play a very important role in the selection of any heat sink.

The least expensive and easiest to fabricate heat sink is the plain copper sheet. It is also very effective in reducing the total thermal resistance. The necessary dimensions can be obtained from Figure 6. These heat sinks are square in geometry, 0.015 inches thick, mounted vertically on each side of the lead frame, and with a dull or painted surface (Figure 7). The heat sinks should be soldered directly to the lead frame (approximately 0.3°C/W interface thermal resistance).

The plain copper sheet heat sink is also available commercially and may be less expensive than in-house manufacture. Two standard types are the Staver V7 and V8.

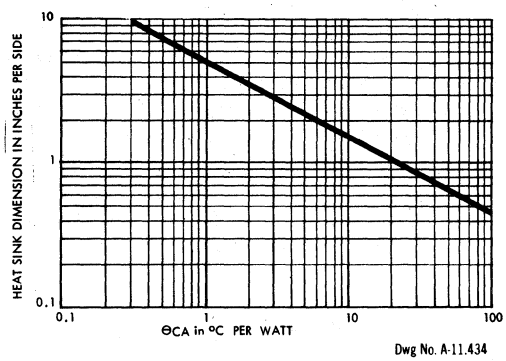


Figure 6

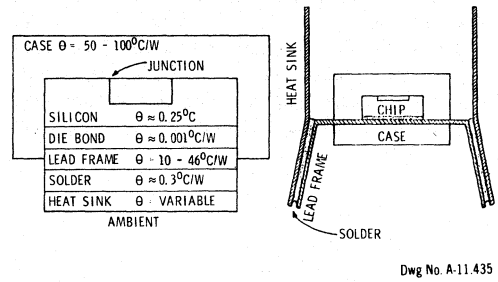


Figure 7

Heat Sink Finishes

Although plain copper is an effective heat sink, it is sometimes desirable to have something that is more appealing to the eye. For this reason, and others, many heat sinks are either painted or anodized.

The most common finish is probably black anodizing. It is economical and offers a good appearance. The black finish will also increase the performance of the heat sink, due to radiation, by as much as 25%. However, since anodizing is an electrical and thermal insulator, the heat sink should have an area free of anodize where the heat-generating device is attached.

Other popular finishes for heat sinks are irridite and chromic acid dips. They are economical and have negligible thermal and electrical resistances. These finishes, however, do not enjoy the 25% increase in performance that a dull black finish has.

Forced Air Cooling

The performance of many heat sinks can be increased by as much as 100% by forcing air over the fins. Where space is a problem, the cost of a small fan can often be justified. If a fan is required for other purposes, it is advantageous to place the semiconductor heat source in the air flow. A rule-of-thumb is that semiconductor failure rate is halved for each 10°C reduction in junction operating temperature.

Chip Design

Proper thermal design by the integrated circuit user can reduce the operating temperature of the semiconductor junction. However, the minimum chip temperature at any power level is determined solely by the device manufacturer. For this reason, care must be taken in choosing the manufacturer. "Exact equivalent" integrated circuits are not necessarily identical. Electrically and mechanically they may be the same, but thermal differences can mean that "identical" audio power amplifiers will not put out the same power without exceeding the rated junction temperature.

The circuit manufacturer must optimize his chip design so that component drift is minimized and/or equalized so that rated performance can actually be obtained under maximum thermal stress.

Note in Figures 8 and 9 that the Darlington input differential pairs are cross-connected so as to minimize differences in gain as a function of output transistor power dissipation. Transistor Q_4, being closest to the output power transistors, is naturally the hottest; Q_3 is a degree or two cooler; Q_1 and Q_2 are about equal and midway between Q_3 and Q_4. The gain of the Q_1-Q_2 Darlington pair is about equal to the gain of Q_3-Q_4 at all output power levels because of careful thermal design.

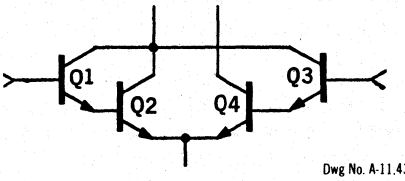


Figure 8

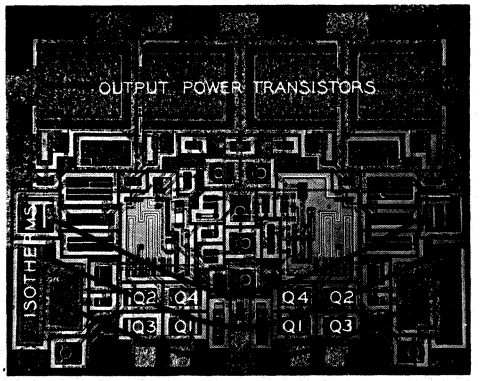


Figure 9

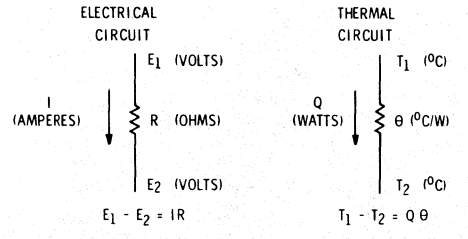
In certain specialized applications, thermal coupling can be used to a distinct advantage. Experimentally, thermal coupling has been used to provide a low-pass feedback network which otherwise could be obtained only with very large values of capacitance.

The foregoing discussion has covered the average thermal characteristics of today's dual in-line plastic integrated circuits. The specific devices will vary with the different packages and bonding techniques employed, but the concepts will remain the same.

APPENDIX

The following is intended to review terminology and compare thermal circuits with the more familiar electrical quantities.

The first law of thermodynamics states that energy cannot be created or destroyed but can be converted from one form to another. The second law of thermodynamics states that energy transfer will occur only in the direction of lower energy. In the semiconductor junction, the electrical energy is converted to thermal energy. Since no heat will be stored at the junction, the heat will flow to a lower temperature medium, air. The rate of heat flow is dependent on the resistance to that flow and the temperature difference between the source and the sink.



Dwg No. A-11,437

Figure 10

This thermal electrical analogy is convenient only for conduction problems where heat flow and temperature obey linear equations. The analogy becomes much more complex for situations involving heat flow by convection and radiation. Where these two modes are not negligible, they can be approximated by an equivalent thermal resistance. If ignored, the error introduced will only improve the device reliability.

A simplified thermal flow diagram of a molded dual in-line package and heat sink is shown. The thermal resistance of the lead frame-heat sink-ambient is shown as a variable resistor, because this is under the control of the user and may be varied over a considerable range.

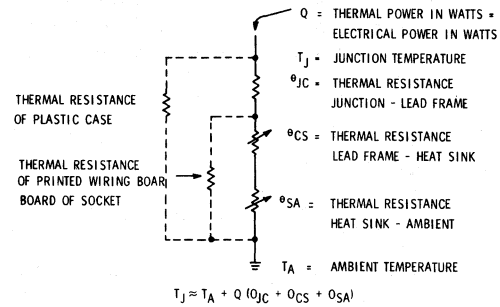


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Figure 11

Material	Thermal Resistance in °C/W for Unit Area/Unit Length
Silver	0.09
Copper, Annealed	0.10
Gold	0.12
Beryllia Ceramic	0.20
Aluminum	0.20
Brass (66 Cu, 34 Zn)	0.40
Silicon	0.50
Germanium	0.70
Steel, SAE 1045	0.80
Solder (60 Sn, 40 Pb)	1.5
Alumina Ceramic	2.0
Kovar (54 Fe, 29 Ni, 17 Co)	3.0
Glass	40
Epoxy	40
Mica	50
Teflon PTFE	200
Air	2000

Computing IC Temperature Rise

Heat is the enemy of integrated circuits—particularly power devices. Here's how to use thermal ratings to determine safe IC operation.

EXCESSIVE heat shortens the life of an IC and reduces its operating capability. Until recently, ICs were capable of operating only in low-power applications requiring perhaps a few milliwatts of power. But now, new ICs handle several hundred milliamperes and drive devices such as relays, solenoids, stepping motors, and incandescent lamps. These high power levels may increase IC temperatures substantially and are capable of destroying devices unless appropriate precautions are taken.

Thermal Characteristics

The thermal characteristics of any IC are determined by four parameters. Maximum allowable IC chip junction temperature T_J and thermal resistance R_θ are specified by the IC manufacturer. Ambient temperature T_A and the power dissipation P_D are determined by the user. Equation 1 expresses the relation of these parameters.

$$T_J = T_A + P_D R_\theta \qquad (1)$$

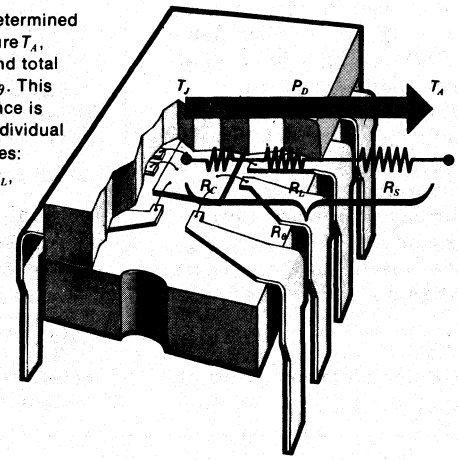
Junction temperature T_J usually is limited to 150°C for silicon ICs. Devices may operate momentarily at slightly higher temperatures, but device life expectancy decreases exponentially for extended high-temperature operation. Usually, the lower the junction operating temperature, the greater the anticipated life of the IC.

Ambient temperature T_A is traditionally limited either to 70°C or 85°C for plastic dual in-line packages (DIPs) or 125°C for hermetic devices. Again, the objective is to operate at as low a junction temperature as practical.

Thermal resistance R_θ is the basic thermal characteristic for ICs. It is usually expressed in terms of °C/W and represents the rise in junction temperature with a unit of power applied in still air. (The reciprocal of thermal resistance is thermal conductance, or derating factor,

Why IC Temperatures Rise

IC temperature T_J is determined by ambient temperature T_A, heat dissipated P_D, and total thermal resistance R_θ. This total thermal resistance is comprised of three individual component resistances: chip R_C, lead frame R_L, and heat sink R_S.



G_θ expressed as W/°C.) Thermal resistance of an IC consists of several distinct components, the sum of which is the specified thermal resistance. For a typical IC, these components of thermal resistance are 0.5°C/W per unit thickness of the silicon chip, 0.1 to 3°C/W per unit length of the lead frame, and up to 2,000°C/W per unit thickness of still air surrounding the IC. DIPs are used more than any other type of packaging for ICs and newer copper-alloy lead frames provide a superior thermal rating over the standard iron-nickel-cobalt alloy (Kovar) lead frames. However, power ICs are also available in other packages such as flat-packs and TO-type cans.

The power P_D that an IC can safely dissipate usually depends on the size of the IC chip and the type of packaging. Most common copper-frame DIPs can dissipate about 1.5 W, although some special-purpose types have ratings as high as 5 W.

Total IC power to be dissipated depends on input current, output current, voltage drop, and duty cycle. Thus, for many industrial digital-control ICs, logic-gate power P_l (typically less than 0.1 W) and output power P_o must be determined to find the total power to be dissipated. Total power dissipation for these logic devices is the sum of P_l and P_o.

$$P_l = n(V_{CC}I_{CC}) \quad (2)$$

$$P_o = n(V_{CE(SAT)}I_C) \quad (3)$$

where V_{CC} = logic-gate supply voltage, I_{CC} = logic-gate ON current, $V_{CE(SAT)}$ = output saturation voltage, I_C = output

Finding Safe Operating Limits

Here's how to calculate the safe operating limits for an IC. The first two examples are simple calculations involving maximum allowable power and are straightforward. The third and fourth examples are more complex and involve logic power, output power, and duty cycle.

Problem: Determine the maximum allowable power dissipation that can be handled safely by a 16-lead Kovar DIP with an R_θ of 125°C/W in an ambient temperature of 70°C.

Solution: From Equation 1, the maximum allowable power dissipation P_D for this IC is

$$P_D = \frac{150°C - 70°C}{125°C/W}$$
$$= 0.64\ W$$

Problem: Determine the maximum allowable power dissipation that can be handled by a 14-lead copper DIP with a derating factor G_θ of 16.67 mW/°C in an ambient of 70°C.

Solution: Since the derating factor G_θ is the reciprocal of thermal resistance R_θ, the maximum allowable power dissipation P_D from Equation 1 is

$$P_D = (150°C - 70°C) \times (16.67\ mW/°C)$$
$$= 1.33\ W$$

Problem: Calculate the maximum junction temperature for a quad power driver with a thermal resistance of 60°C/W in an ambient of 70°C and which is controlling a 250 mA load on each of the four outputs.

Solution: To determine the maximum (worst case) junction temperature for this IC, the maximum total power dissipation must be determined from the data listed on the IC data sheet. The specifications are usually listed as typical and minimum or maximum values. It is important to use maximum voltage and current limits to insure an adequate design. Common maximum values for an

Measuring IC Temperature

Sometimes IC junction temperature cannot be calculated readily and instead must be measured. Measurement should be made when there is insufficient data with which to calculate, when the effects of external variables such as forced-air cooling or enclosure size must be determined, or as a check on the manufacturer's specifications regarding package thermal resistance.

The most popular technique for measuring IC temperature uses the characteristic of a diode to reduce its forward voltage with temperature. Many IC chips have some sort of accessible diode—parasitic, input protection, base-emitter junction, or output clamp. With this technique, a "sense" diode is calibrated so that forward voltage is a direct indicator of diode junction temperature. Then, current is applied to some other component on the chip to simulate operating conditions and to produce a temperature rise. Since the thermal resistance of the silicon chip is low, the temperature of the sense diode is assumed to be the same as the rest of the monolithic chip.

The sense diode should be calibrated over at least the expected junction operating temperature chamber. Apply an accurately measured, low current of about 1 mA through the sense diode and measure the forward voltage in 25°C increments after stabilization at each temperature. This calibration provides enough data for at least six points to construct a diode-forward-voltage versus junction-temperature graph at the specified forward current. A typical 25°C forward voltage is between 600 and 750 mV and decreases 1.6 to 2.0 mV/°C.

For power levels above 2 W, it may be necessary to use more than a single transistor if only the device saturation voltage and sink current are used. When higher power is desired, keep the output out of saturation.

Measuring the sense-diode forward voltage may require a considerable waiting period (10 to 15 minutes) for thermal equilibrium. In any event, at the instant of measurement, the heating power may have to be disconnected since erroneous readings may result from IR drop in circuit common leads. Various circuit connections (such as four-point Kelvin) may be arranged to reduce or eliminate this source of error.

The IC junction temperature can be determined by comparing the voltage measurement with the internal power source against the voltage measurement with the temperature chamber.

industrial power driver are $V_{CC} = 5.25$ V, $I_{CC} = 25$ mA, and $V_{CE(SAT)} = 0.7$V, and $I_c = 250$ mA. From Equations 2 and 3, worst case logic and output power dissipation are

$$P_l = 4(5.25\text{ V} \times 25\text{ mA}) = 525\text{ mW}$$

$$P_o = 4(0.7\text{ V} \times 250\text{ mA}) = 700\text{ mW}$$

Thus, the total worst case power dissipation P_D is 525 mW plus 700 mW, or 1.225 W. From Equation 1, maximum junction temperature T_J is

$$T_J = 70°\text{C} + (1.225\text{ W}) \times (16.67\text{ mW/°C}) = 143.5°\text{C}$$

Problem: Determine the acceptable duty cycle for a hermetic power driver with a thermal resistance of 100°C/W in an ambient of 85°C and which is controlling load currents of 250 mA on each of four outputs.

Solution: From Equation 1, the allowable average power dissipation P_D for this IC is

$$P_D = \frac{150°\text{C} - 85°\text{C}}{100°\text{C/W}} = 0.65\text{ W}$$

This means that there is 0.65 W limit on average power, but, not instantaneous power. If the duty cycle is low enough, and the ON time is not more than about 0.5 sec, the average power dissipation can be considerably lower than the peak power. The ON, or peak power, is determined from the data sheet maximum values of V_{CC}, I_{CC}, and $V_{CE(SAT)}$ at the specified load current of 250 mA. From Equations 2 and 3, logic-gate power P_l and output power P_o for the ON state are

$$P_l = 4(5.5\text{ V} \times 26.5\text{ mA}) = 583\text{ mW}$$

$$P_o = 4(0.7\text{ V} \times 250\text{ mA}) = 700\text{ mW}$$

Instantaneous ON power P_{ON} is the sum of P_l and P_o for the ON state, or 1.283 W. The OFF power is primarily the power dissipated by the logic in the OFF state, and is found by using the I_{CC} maximum rated current listed on the specification sheet. The power dissipated in the output stage can be calculated from the leakage current I_C and supply voltage V_{CE}. From Equations 2 and 3, logic-gate power P_l and output power P_o for the OFF state are

$$P_l = 4(5.5\text{ V} \times 7.5\text{ mA}) = 165\text{ mW}$$

$$P_o = 4(100\text{ V} \times 0.1\text{ mA}) = 40\text{ mW}$$

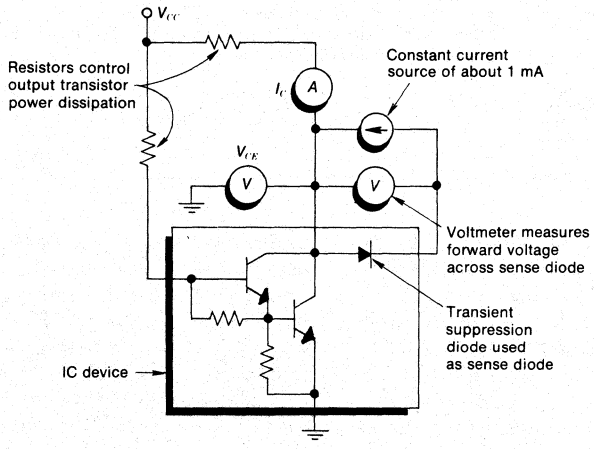
Instantaneous OFF power P_{OFF} is the sum of P_l and P_o for the OFF state, or 205 mW. From Equation 4, acceptable duty cycle D is

$$D = \frac{P_D - P_{OFF}}{P_{ON} - P_{OFF}} = \frac{0.65\text{ W} - 0.205\text{ W}}{1.283\text{ W} - 0.205\text{ W}}$$

load current, and n = number of logic gates. Manufacturers usually list typical and maximum values for these voltages and currents. For thermal considerations it is best to use the maximum values so that worst-case power dissipation is determined.

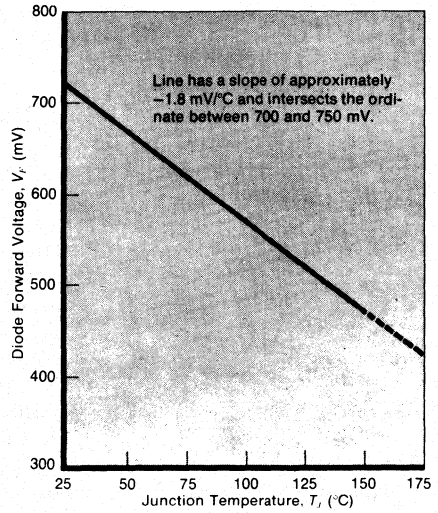
If the duty cycle of the device is longer than 0.5 sec, the peak power dissipation is the sum of the logic-gate power P_l and output power P_o for the logic ON state alone. If the ON time is less than 0.5 sec, however, average power dissipation must be calculated from instantaneous

Setting Up the Circuit



Input power is negligible compared to output power and is therefore not measured.

Calibrating the Sense Diode



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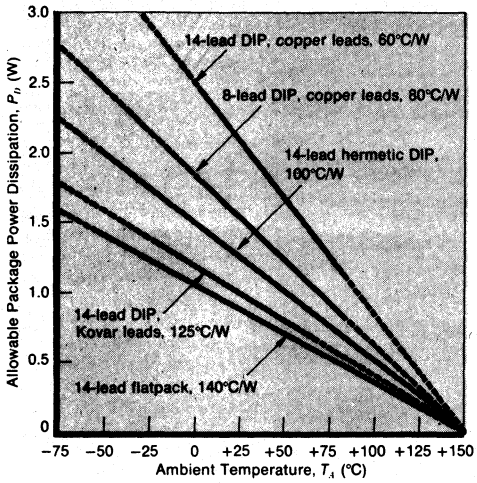
What the Curves Show

The junction temperature of an IC depends on several factors, including the thermal resistance of the IC and the operating duty cycle. Graphs showing the relationship of these factors are often useful in specifying an IC.

Thermal Ratings

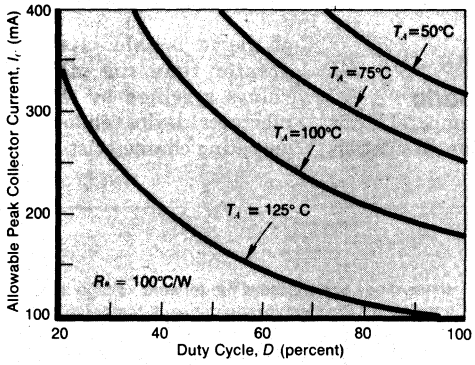


Typical thermal-resistance ratings for ICs in still air range from 60°C/W to 140°C/W. The slope of each curve on this graph is equal to the derating factor $G\theta$, which is the reciprocal of thermal resistance $R\theta$. For an ambient temperature of 50°C, a typical 14-lead flatpack with an $R\theta$ of 140°C/W can dissipate about 0.7 W. A typical DIP, however, with 14 copper-alloy leads can dissipate almost 1.7 W at 50°C.

The highest allowable package power dissipation shown here is 2.5 W. Other special-purpose DIP packages are available with power dissipation ratings as high as 3.3 W at 0°C ($R\theta$ = 45°C/W). If not for package limitations, IC chip dissipation might be greater than 9 W at an ambient temperature of up to 70°C.

Although the curve for plastic DIPs goes all the way to 150°C, they ordinarily are not used in ambients above 85°C because of traditional package limitations. Hermetic DIPs are specified to temperatures of 125°C, and at 150°C the device should be derated to 0 W. The higher specification limits for hermetic devices is the result of their design for use in rigorous, high-reliability military applications.

Duty Cycle



Duty cycle is important in calculating IC junction temperature because average power—not instantaneous power—is responsible for heating the IC. To convert from peak power to average power, multiply the peak power dissipation by the duty cycle. The average-power rating is then used with the thermal-resistance rating to calculate the IC junction temperature. Thus, short duty cycles allow peak power to be high without exceeding the 150°C junction-temperature limit. However, this consideration applies only to ON times of less than 0.5 sec.

ON and OFF power P_{ON} and P_{OFF} from

$$P_D = DP_{ON} + (1 - D)P_{OFF} \quad (4)$$

Corrective Actions

If the junction temperature or the required power dissipation of the IC is calculated to be greater than the maximum values specified by the manufacturer, device reliability and operating characteristics possibly will be reduced. Possible solutions are: 1. Modify or partition the circuit design so the IC is not required to dissipate as much power. 2. Reduce the thermal resistance of the IC by using a heat sink or forced-air cooling. 3. Reduce the ambient temperature by moving heat-producing components such as transformers and resistors away from the IC. 4. Specify a different IC with improved thermal or electrical characteristics (if available).

THERMAL RESISTANCE— A RELIABILITY CONSIDERATION

More and more the semiconductor component supplier and the ultimate system user are becoming aware of the need for reliable components. Most failure mechanisms responsible for reliability failures are temperature dependent and the kinetics of the failure reaction are normally described by an Arrhenius function. This dependence, therefore, demands the capability of measuring the mean temperature which an integrated circuit die will attain during operation to realistically assess the reliability of the part.

The problem addressed by this paper is the inconsistency of the measurement techniques and the results used by manufacturers and users to determine the thermal characteristics of packaged semiconductor components. Our objective is to provide insight into the considerations which must be applied when evaluating these thermal properties of the packaged component. These considerations are materials, geometry and environment.

Furthermore, we wish to instill uniformity in the method of determining thermal properties of packaged semiconductors through understanding of the variables involved which can lead to a useable industry standard.

Reliability—The Temperature Function

The recognition of the problems one encounters in measuring the mean temperature of a die has been directly related to our experiences at the Sprague Electric Co. in our Reliability Assurance Programs. The large number of device types manufactured require an equally large number of burn-in boards having different functions and geometry for the individual reliability studies. The variations in board density and thermal environment for a device under test have provided considerable junction temperature data from which we conclude that a "thermal resistance" measured in one oven with its set of conditions is not transferable to another oven with different boards, loading, etc. when the reference temperature for the measurement is the oven control temperature. Furthermore, it has become obvious that these same problems in measuring a mean die temperature exist in a system environment.

Most reactions which can cause a failure in an electrical parameter of an integrated circuit are chemical in nature and are influenced by temperature. The temperature dependence of these reactions has been described very well by S. Arrhenius in his treatment of reaction kinetics.[1] In his treatment, the reaction velocity or rate is given by the equation.

$$d\ln V_r/dT = E/RT^2$$

here V_r is the specific reaction rate, T is the absolute temperature, R is the Molar Gas Constant, and E is the energy difference between a mole of active molecules and a mole of normal molecules.

This equation integrates to

$$\ln V_r = E/RT + A$$

where A is a constant which is the value of $\ln V_r$ at $1/T = 0$, $(\ln V_r)$. A more familiar expression is

$$\ln V_r = \ln V_r^0 - \epsilon/kT$$

or

$$V_r = V_r^0 e - \epsilon/kT$$

where ϵ is the activation energy per molecule $(= E/N)$, N = Avagado's number and k is the gas constant per molecule $(= R/N)$, which is generally known as the Boltzmann constant. It has the value 8.6×10^{-5} eV/°K.

V_E, the time rate of change of the electrical parameter is proportional to V_r, i.e., $V_E = BV_r$. The amount of change in the electrical parameter necessary to cause a normal device to fail, ΔP_f, is $V_E t_f$ where t_f is the time of failure.

Recalling that $V_E = BV_r$, then

$$\Delta P_f = BV_r t_f$$

For a given device ΔP_F is a constant, therefore,

$$t_f = \Delta P_f B^{-1}/V_r$$

but

$$V_r = V_r^0 e\, \epsilon/kT$$

therefore

$$t_f = (B^{-1}\Delta P_f/V_r^0 e^{\epsilon/kT} = \delta e^{\epsilon/kT}$$

where

$$\delta = B^{-1}\Delta P_f/V_r^0$$

The acceleration factor ($\overline{AF}$) between any two temperatures is derived from this equation, when the activation energy for the failure reaction is known:

$$\overline{AF} = t_{f_1}/t_{f_2} = e^{e/k(1/T_1 - 1/T_2)}$$

Activation energies of most reactions responsible for random failures in a normal operating period (beyond infant mortality) are nominally

$$(0.4 - 1.0)\,eV.$$

The importance of accurately determining the die temperature is now clear if one considers a not unrealistic situation where a device is thought to be operating with a die temperature of 120° and the actual temperature is 150°C. If the failure reaction has an activation energy of 0.7 eV, then the acceleration factor is 4.3 which means the device would fail in less than one quarter of the time it would have taken if the device actually operated at 120°C.

Thermal Resistance – θ_{JA}

Quite frequently applications engineers have made attempts to identify the temperature attained by a die when a steady state rate of heat is being generated by the die by applying the term called "Thermal Resistance." This "constant," designated $R\theta_{JA}$ or simply θ_{JA}, relates the temperature rise of a packaged integrated circuit die above an ambient temperature when a known constant power is generated in the die. This term is normally defined as

$$\theta_{JA} = (T_J - T_A)/P_D$$

where T_J is the mean junction or die temperature, T_A is an ambient temperature, and P_D is the power generated within the die which must be conducted from the die to the ambient. This is occasionally designated Q_T, the time rate of heat generation in the die. Thermal resistance data supplied by manufacturers may be referenced to a cubic foot of free or still air, flowing air at some velocity, or simply no reference. These are some of the definitions of "ambient" from which one must determine where to measure T_A.

Thermal resistance as defined by θ_{JA} is not constant. It is made up of a constant term (or terms) in series with a number of variable terms. The constant terms relate to the package materials and geometry, which we will designate θ_{JC_i} and the variable terms relate to the heat paths from the package boundary to some isothermal envelope in the system which has the temperature T_A. Even if the system for measuring θ_{JA} is defined, it is virtually impossible to reproduce that system in an application since the external thermal paths are determined by the method of mounting, the printed wiring board if used, other heat generating components on the board or in the vicinity, air flow patterns, etc. These are all variable for each application. We have measured values of θ_{JA} for the same device which vary by a factor of two when the mounting and environmental conditions are changed. The values in the θ_{JA} column in Tables 2 and 3 are indicative of the variation.

One is tempted to partition θ_{JA} into two thermal terms,

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{JC} is defined as the thermal resistance from the source of power at T_J to the boundary of the package not including the external legs, and θ_{CA} is the thermal resistance from the package boundary to that isothermal envelope at T_A. However, when one examines the thermal profile along the surface of a plastic dual-in-line package such as shown in Figure 1, it is immediately obvious that a definition of θ_{JC}

$$\theta_{JC} = (T_J - T_C)/P_D$$

cannot be applied because T_C varies with position. Similarly, the term θ_{CA} defined by

$$\theta_{CA} = (T_C - T_A)/P_D$$

suffers from the same variability in T_C. This being the case it is invalid to partition θ_{JA} when operating on the *total* power to be dissipated, P_D.

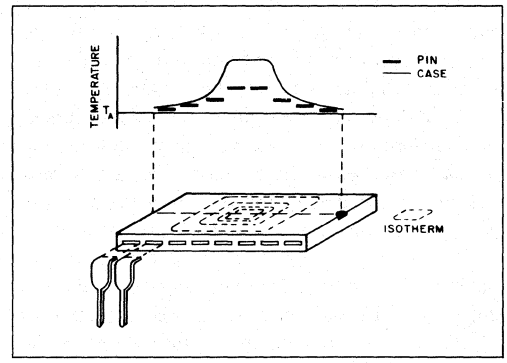


Figure 1

The Thermal Model

When one examines a plastic package supplied by an individual manufacturer it is found that the geometry of the lead frame, its position within the package boundary, its composition, the composition of the plastic and its filler, the internal wire bonding are very carefully controlled and constant in time. This being the case one can readily build a model of the package which can be as invariant as the package material properties. If one considers all possible heat flows, a very complex model emerges. However, if the thermal conductivities of the package materials and the orders of magnitude difference in the values of these conductivities are considered, a simplified workable model can be generated by neglecting heat paths where heat flows are minimal. The simplified model shown in Figure 2 has ignored the heat flow between leads and assumes that the large difference between the thermal conductivity of the loaded plastic and the metals in the package define the specified heat paths. For example, the heat flow between leads would be a shunting resistor between heat paths in the model. The thermal conductivity of most plastics range between 1.5 and 3 $\times$ 10^{-3} calories/cm – °C while copper based materials range between 0.5 and 0.82 calories/cm – °C and nickel based alloys are about 0.03 calories/cm – °C.

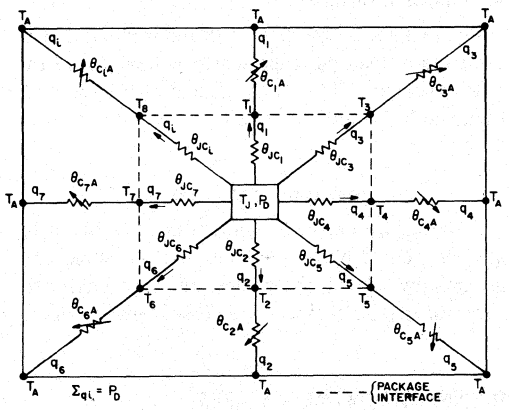


Figure 2

The heat paths defined by θ_{JC_i}, where i refers to a particular path, radiate from the chip to an area on the package periphery defined by the projected chip or pad area as well as the mean cross-sectional area of each of the leads within the plastic package boundary (see Figure 1). Because of package symmetry, a 16 lead isolated pad package may have seven different heat paths which can be characterized. The thermal resistance, θ_{JC_i}, can be calculated for each path from the geometry and material properties. For example θ_{JC_1} is the resistance from the top of the chip to the projected area on the package surface. The value of θ_{JC_1} is given by

$$\theta_{JC_1} = (T_J - T_{C_i})/q_1 = L/K_pA$$

where L is the length of the heat path (thickness of the plastic above the die), A is the cross-sectional area of the heat path (are of the die or the pad), K_p is the thermal conductivity of the loaded plastic and q_1 is the heat/second flowing in the path defined by A and L.

θ_{JC_2} is the thermal resistance from the top of the die through the silicon, through the pad and through the plastic to the bottom surface. The value of θ_{JC_2} is given by

$$\theta_{JC_2} = (T_J - T_{C_2})/q_2 = [1/A] \sum L_n/K_n$$
$$n = \text{Si, Metal, Plastic}$$

Similar expressions can be derived for each of the leads and they have the form

$$\theta_{JC_i} = (T_J - T_{C_i})/q_i = [1/t]\,[(L/K_PW_P) + (1/K_M) \sum L_n/W_n]$$
$$n = 1, 2 \ldots\ldots$$

where t is the thickness of the lead frame, K_p is the thermal conductivity of the loaded plastic, K_M is the thermal conductivity of the frame metal, L_n is the mean length of each connected portion of a leg segment having a mean width, W_n. In accord with the model, each internal path characterized by a thermal resistance, θ_{JC_i}, is in series with an external thermal resistance, θ_{CiA}, which completes the path to T_A. The value of θ_{C_iA} can be calculated from the amount of heat, q_i, flowing through the internal package path and the temperature difference, $(T_{C_i} - T_A)$, with the equation

$$\theta_{C_iA} = (T_{C_i} - T_A)\,/\,q_i.$$

Values of θ_{CiA} are variable and depend upon the specific environment.

We at Sprague Electric Company identify the heat paths in our calculations and data as follows: a) when i = 1 the path is from die to case surface directly above, b) when i = 2 the path is from die to the case surface directly below and c) when i = 3, 4, 5 . . . the path is from die through an identified metal lead to the intersection with the plastic surface.

Verification of Model

From the model one can derive the minimum thermal resistance which is characteristic of the package. This can be calculated for the condition when all case temperatures are equal and at T_A. This is equivalent to shorting all external thermal resistances so that $T_{C_i} = T_A$. When all T_{C_i} are equal, the reciprocal of the sum of the reciprocals of all θ_{JC_i} is the minimum thermal resistance for the package. This is realized experimentally by placing the unit in an infinite heat sink such as a rapidly stirred, low-viscosity controlled temperature bath. The case temperature is now forced to be the same over all surfaces and by definition it is T_A. θ_{JC} is the minimum limit of θ_{JA}. Table 1 shows the agreement between the values of θ_{JC} calculated from the model when the case temperatures are shorted together and the values experimentally measured in a controlled temperature liquid bath. The agreement between calculated and experimental values for packages constructed from different materials enhance the validity of the model.

Applying The Model To Measure T_J

Having verified the model, any one of the identified heat paths, which has a constant thermal resistance, o_{JC_i}, can now be used to determine quite accurately the die temperature, T_J. If one chooses to measure the case temperature directly above the die, the difference between die temperature and case temperature is related to the heat flow, q_i, through that path by the thermal conductivity equation:

$$q_i = K_p A (T_J - T_{C_1})/L_1.$$

Rearranging this equation to

$$(T_J - T_{C_1})/q_1 = L_1/k_p A_1 = \theta_{JC_1}$$

Then

$$T_J = T_{C_1} + q_i\theta_{JC_1}$$

If the fraction of total heat, P_D generated by the die which passes through path 1 is defined as k, then

$$q_1 = k_1 P_D$$

Substituting into the previous equation, T_J is now referenced to T_{C_1} by

$$T_J = T_{C_1} + k_1\theta_{JC_1}P_D$$

where T_J, T_{C_1}, and P_D are experimentally measureable quantities. Values of $k_1\theta_{JC_1}$ can be determined. This term can be used to determine T_J in any environment by measuring T_{C1} and the total heat generated by the die. This equation applies for any path, i., i, e.

$$T_J = T_{C_1} + k_i\theta_{JC_i}P_D$$

Experimental results are presented in Table 2 which establish that $k_i\theta_{JC_i}$ is a constant, the magnitude of which is determined by the heat path chosen.

In our notation, $k_4\theta_{JC_4}$ is the thermal resistance of the path determined by measuring the temperature of pin 4 at the point of intersection with the case body. Further data are presented in Table 3 for a copper tab package where the pad on which the die is mounted extends to the outside of the package. The values of $k_5\theta_{JC_5}$ remain constant over a large change in environment. When i = 5, the heat path is from the die through the heat tab to the intersection with the case surface.

Figure 3 shows the outline of the frame in the 16 pin isolated pad package which is designated the "A" package. The "B" package or tab package frame outline is also shown.

Measurement of $k_i\theta_{JC_i}$

Although the derived equations indicate that $k_i\theta_{JC_i}$ are determined by two temperature measurements at one power level, the values are more accurately determined from temperature versus power plots.

TABLE 1
COMPARISON OF CALCULATED AND EXPERIMENTAL VALUES OF $[\theta_{JC}]\ T_{C_i} = T_A$
(All measurements in °C/W)

Package Type	Frame Material	$[\theta_{JC}]\ T_{C_i} = T_A$ Experimental	Calculated
16 pin, isolated pad, Epoxy I	copper	41 ± 3	43
16 pin, isolated pad, Epoxy I	Kovar	100 ± 4	93
16 Pin Tab	copper	8.6 ± .7	8.5

TABLE 2
THERMAL RESISTANCE VALUES—ISOLATED PAD—EPOXY PACKAGE
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_4\theta_{C_4A}$	$k_1\theta_{C1A}$	$k_1\theta_{JC_1}$	$k_4\theta_{JC_4}$
ULN-2003A 16-Pin Copper Frame. "A" Package	1 ft.^{3} still air, socket mount	84.7	39.1	48.1	36.6	45.6
ULN-2003A 16-Pin Copper Frame. "A" Package	Oven #1 60 CFM, pin connectors	60.0	17.0	25.2	34.8	42.3
ULN-2003A 16-Pin Copper Frame. "A" Package	AAVID E type 5010 heat sink Oven #1 60 CFM	50.4	11.4	15.2	35.2	39
ULN-2003A 16-Pin Copper Frame. "A" Package	Fluorocarbon Bath, pin connectors	41.3	3.3	2.9	38.4	38

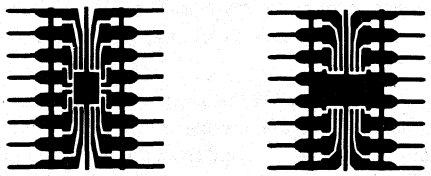


Figure 3
Plastic Package Frame Geometry

If one considers any one path, i, in the model, that path is described by:

$$T_J - T_A = q_i (\theta_{JC_i} + \theta_{C_iA})$$

Here again if k_i is the fraction of the total heat (P_D) which traverses path i then the previous equation can be written

$$T_J - T_A = k_i P_D (\theta_{JC_i} + \theta_{C_iA})$$

or rearranging terms

$$(T_J - T_A)/P_D = k_i\theta_{JC_i} + k_i\theta_{C_iA}$$

TABLE 3
THERMAL RESISTANCE VALUES—TAB PAD—EPOXY PACKAGE
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$K_5\theta_{C5}A$	K_5J_{C5}
Test Chip "B" Package	oven #1, T_A = 50°, 60 CFM	32.8	25.0	7.8
ULN-2068 "B" Package	oven #1, T_A = 50°, 60 CFM	34.9	26.4	8.5
ULN-2068 "B" Package	Socket mount, FC-40 Bath	23.2	13.5	9.7
ULN-2068 "B" Package	Socket mounted on board, FC-40 Bath	26.8	17.4	9.4
Test Die "B" Package	oven #1, soldered on test board, 60 CFM	31.2	22.8	8.4
Test Die "B" Package	oven #1, soldered in test board w/Staver heat sink	22.3	14.2	8.1

By definition $(T_J - T_A)/P_D = \theta_{JA}$, therefore by substitution and rearrangement

$$k_i\theta_{JC_i} = \theta_{JA} - k_i\theta_{C_iA}$$

where experimentally θ_{JA} is the slope of a plot of T_J versus P_D and $K_i\theta_{C_iA}$ is the slope of the plot of T_{C_i}, versus P_D. Figures 4, 5, and 6 are representative of the experimental plots for evaluation of $k_i\theta_{JC_i}$.

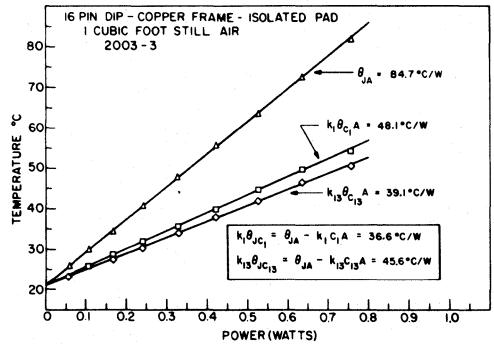


Figure 4

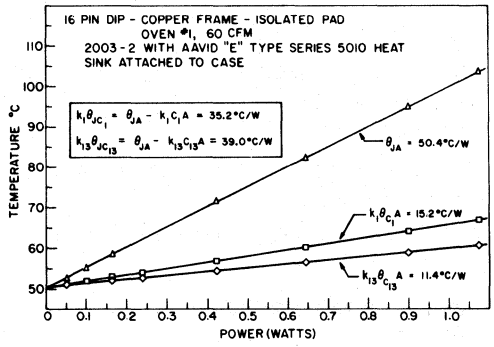


Figure 5

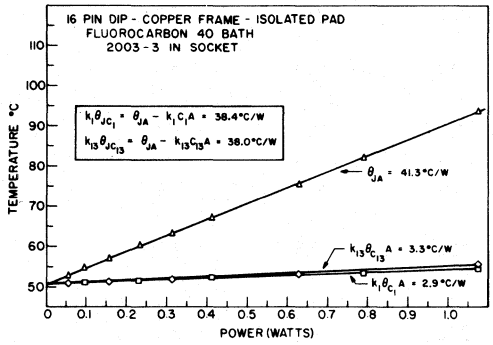


Figure 6

T_{C_i} Measurement

The numerical values of $k_i\theta_{JC_i}$ which we have shown experimentally to be constant over a large variation in environmental conditions are functions of the measuring system for determining the case or leg temperature, T_{C_i}. This can be shown by considering heat path 1 in the Model shown in Figure 2. In this case $q_1 = (T_J - T_A)/(\theta_{JC_1} + \theta_{C_1A})$. θ_{JC_1} is defined as L_l/k_pA_1 where A_1 is determined by the die area. When a thermocouple is attached to the surface directly over the die it also functions as a heat sink. This changes the effective area A of the internal heat path and also changes the external thermal resistance, θ_{C_1A}. The changes are functions of the thermocouple composition and size. The value of θ_{JC_1} is now determined by the effective area of contact of the thermocouple and its value remains constant when the attached thermocouple's size is held constant. k_1, $(= q_1/Q_t)$, also changes because q_1 is determined by the sum of θ_{JC_1} and θ_{C_1A}. The term $(T_J - T_A)$ is essentially constant within experimental error because q_1 is small compared to Q_t and the variations in q_1 do not measureably change the die temperature.

θ_{C_1A} decreases as the wire size of a copper-constantan thermocouple increases and it increases as the composition is changed from copper-constantan to iron constantan. The thermal conductivities of copper, iron, and constantan are respectively 0.9, 0.16, and 0.054 cal/°C-cm.

Data in Table 4 confirm the direction and change in $k_1\theta_{JC_1}$ with change in measuring system. Data were taken in the same oven ambient.

When the physical system for T_C measurement and the conditions for measurement are specified and held constant, values for $k_1\theta_{JC_1}$ are constants.

T_J Measurement For $k_i\theta_{JC_i}$ Determination

An accurate measurement of the value of $k_i\theta_{JC_i}$ requires a method of measuring the mean temperature of the die, T_J. Techniques to make this measurement have been discussed elsewhere. (See Ref. 2, 3, 4) They involve measurement of a temperature sensitive parameter of an element on the die. The forward voltage drop across a diode measured at constant current is a commonly used parameter. One must observe caution when applying the cali-

TABLE 4
VARIATIONS IN $k_i\theta_{JC_1}$ WITH MEASUREMENT SYSTEM
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_1\theta_{C_1A}$	$k_1\theta_{JC_1}$
Test device	.005" Type "J" thermocouple	127.6	52.2	75.4
Test device	.012" Type "J" thermocouple	123.5	31.5	92.0
2125-Linear TV Circuit	.005" Type "T" thermocouple	123.3	75.0	48.3

bration data for an element in an unpowered die to the measured values of that element when the die is powered. It is rather unique if a parasitic voltage or current from the powered portion of the die does not interact with the temperature measuring element. This interaction leads to an inaccurate indication of the true temperature.

A test chip with a number of temperature sensitive elements is valuable. Figure 7 is a photo micrograph of a test chip designed by personnel at the Sprague Electric Company to evaluate thermal resistance values for various packages as well as package-surface interactions. The die contains 3 heat generators, and 6 primary temperature sensors, which are either diodes or special resistors. Parasitics normally interact differently with different elements because of location or structure variations. Agreement in the value of temperatures measured simultaneously for different elements on the chip normally indicates a correct measurement.

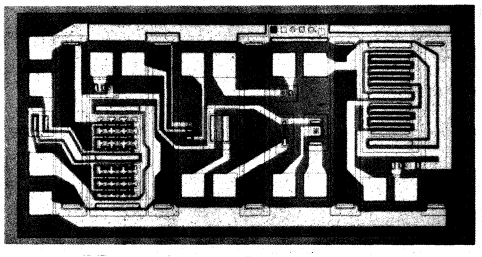


Figure 7

Figure 8 illustrates errors which can be introduced when making static steady state measurements of temperature during power application. Observe the plots of T_j (from V_{eb} calibration) versus P_D for three different diodes on the chip. Although the slopes of the plots after initial power agree within 10%, the initial portion of the curve indicates a negative thermal resistance and the offsets of the curves indicate a varying interaction at different power levels. Although calculation of thermal resistance by the slope method would introduce a similar error for all three diodes, the single power point method for calculating $k_i\theta_{JC_i}$, where $k_i\theta_{JC_i} = (T_J - T_{C_i})/P_D$, would introduce considerable and different levels of error in the calculated values for each diode measurement.

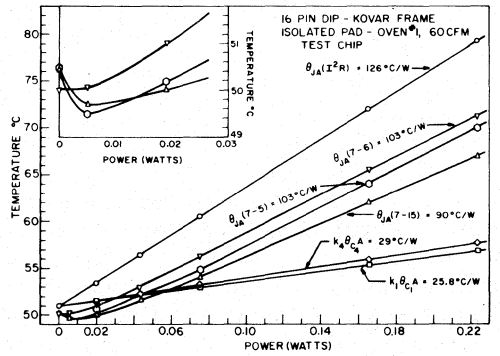


Figure 8

For example, if temperature measurements were made at a power level of 0.22 Watts, one would calculate a value of 44.6°C/W for $k_1\theta_{JC_1}$ using T_J from diode 7-15. 57.1°C/W using T_J from diode 7-5, and 63.8°C/W using T_J from diode 7-6. The true value which was verified by pulsed measurements was 97°C/W.

To eliminate interactions between the powered portion of a circuit and the temperature sensing element during measurement, the circuit shown in Figure 9 was developed. This circuit was designed for thermal evaluation of packages in which the function could be a linear circuit, a digital circuit, or the standard test chip which has a number of different power sources and temperature sensing elements.

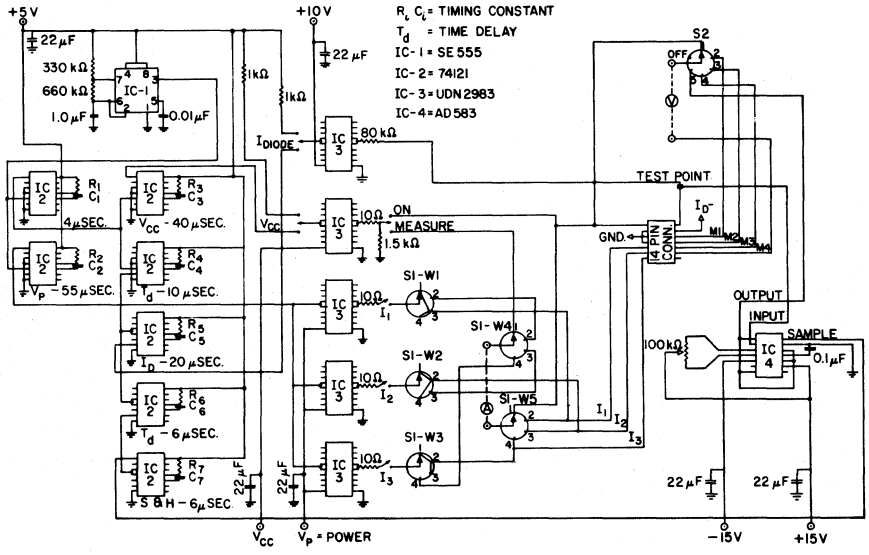


Figure 9

In operation, the circuit applies power at a measured level to the device under test for approximately one second, interrupts power for 40 microseconds, and continues this cycle throughout the test period. At the beginning of the 40-microsecond power off interval, a 10-microsecond delay allows circuit transients to decay before the diode current is activated. A 6-microsecond delay allows the current to settle before a sample and hold circuit samples the diode voltage to determine the chip temperature. This sequence allows the package under test to come to thermal equilibrium with the environment which approaches that for continuous power input. The power down sequence and temperature measurement interval are short enough to insure that the actual temperature drop when power is removed is less than the sensitivity of the temperature sensitive element.

The case temperature measurements, T_{C_i}, can be made by thermocouple or by infra-red measurements.[4] In theory the infra-red measurements would be preferred since a conductive contact is not made to the surface which is to be measured. In practice a number of difficulties with I.R. measurements are encountered. The emissivity of the surface to be measured must be controlled to give accurate measurements. This normally requires painting the surface with a "proprietary" film. When the emissivity is mastered, two larger difficulties must be overcome; a) physically placing the infra-red measuring instrument into the system to view a package surface when the unit may be buried in a maze of printed wiring boards and circuitry and b) the cost of available instrumentation.

The thermocouple technique to measure case temperature is a practical and reliable method when the composition of the thermocouples, its physical size, its location on the package, and the method of its attachment are defined. The method of measurement can be standardized and provides an accurate, inexpensive method for the applications engineer or the reliability engineer to determine a reference temperature to which the temperature rise across the package path, $(k_i\theta_{JC_i})P_D$, can be applied in order to determine a true T_J.

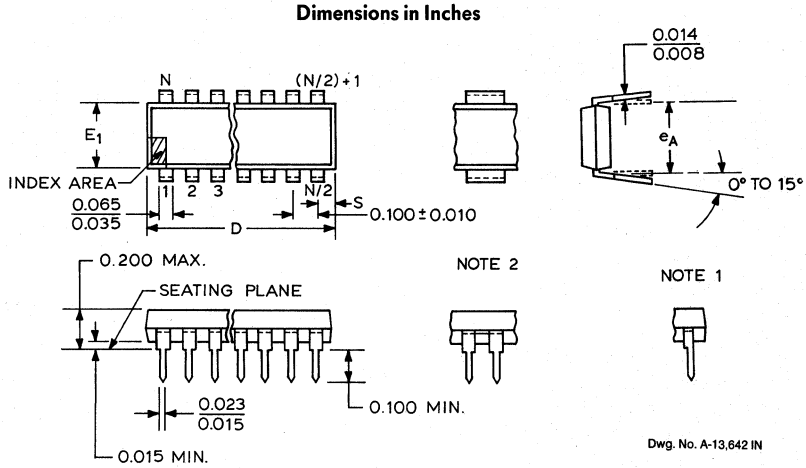
REFERENCES

1. S. Glasstone, *Textbook of Physical Chemistry,* 2nd Edition, D. Van Nostrand Co. Inc., New York, 1946
2. P. E. Roughan, *Thermal Resistance of Integrated Circuit Packages,* Technical Paper TP72-7, Sprague Electric Co., 1972
3. F. R. Dewey and P. R. Emerald, *Computing IC Temperature Rise,* Machine Design, pp 98-101, June 1977
4. C. A. Lidback, *Scanning I. R. Microscopy Techniques for Semiconductor Thermal Analysis.* 17th Annual Proceedings Reliability Physics 1979 IEEE Catalog No. 79CH1425-8 Phy.

PLASTIC DIP

SPRAGUE PACKAGE DESIGNATOR A, B, OR M

Dimensions in Inches



N	Leads Pkg. Designator	8 B	8 M	14 A	16 A	16 B	18 A
D	Body Length	0.360/0.390	0.360/0.390	0.735/0.785	0.735/0.785	0.735/0/785	0.885/0.915
E_1	Body Width	0.240/0.260	0.240/0.260	0.240/0.260	0.240/0.260	0.240/0.260	0.240/0.260
e_A	Row Spacing	0.300 BSC	0.300 BSC	0.300 BSC	0.300 BSC	0.300 BSC	0.300 BSC
S	Lead CL to End	0.040 REF	0.040 REF	0.075 REF	0.025 REF	0.025 REF	0.050 REF
Notes	(Leads Affected)	1 (1, 4, 5, 8) 2 (2, 3, 6, 7)	1 (1, 4, 5, 8) —	— —	1 (1, 8, 9, 16) —	1 (1, 8, 9, 16) 2 (4, 5, 12, 13)	— —

N	Leads Pkg. Designator	20 A	22 A	22 B	28 A	40 A
D	Body Length	0.990/1.040	1.050/1.120	1.050/1.120	1.380/1.460	1.980/2.060
E_1	Body Width	0.240/0.260	0.300/0.390	0.300/0.390	0.480/0.560	0.480/0.560
e_A	Row Spacing	0.300 BSC	0.400 BSC	0.400 BSC	0.600 BSC	0.600 BSC
S	Lead CL to End	0.060 REF	0.050 REF	0.050 REF	0.075 REF	0.075 REF
Notes	(Leads Affected)	— —	— —	2 (5, 6, 17, 18) —	— —	— —

NOTES:

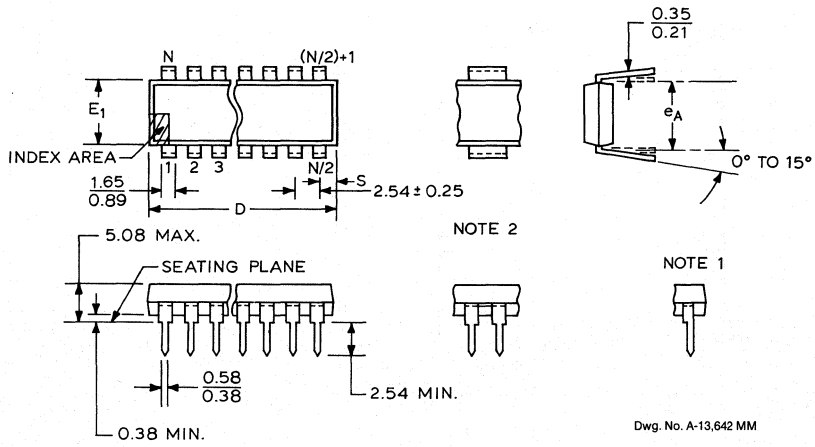
1. Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC DIP

SPRAGUE PACKAGE DESIGNATOR A, B, OR M

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,642 MM

N	Leads Pkg. Designator	8 B	8 M	14 A	16 A	16 B	18 A
D	Body Length	9.14/9.91	9.14/9.91	18.67/19.93	18.67/19.93	18.67/19.93	22.48/23.24
E_1	Body Width	6.10/6.60	6.10/6.60	6.10/6.60	6.10/6.60	6.10/6.60	6.10/6.60
e_A	Row Spacing	7.62 BSC	7.62 BSC	7.62 BSC	7.62 BSC	7.62 BSC	7.62 BSC
S	Lead CL to End	1.02 REF	1.02 REF	1.90 REF	0.64 REF	0.64 REF	1.27 REF
Notes	(Leads Affected)	1 (1, 4, 5, 8) 2 (2, 3, 6, 7)	1 (1, 4, 5, 8) —	— —	1 (1, 8, 9, 16) —	1 (1, 8, 9, 16) 2 (4, 5, 12, 13)	— —

N	Leads Pkg. Designator	20 A	22 A	22 B	28 A	40 A
D	Body Length	25.15/26.42	26.67/28.45	26.67/28.45	35.05/37.08	50.29/52.32
E_1	Body Width	6.10/6.60	7.62/9.91	7.62/9.91	12.19/14.22	12.19/14.22
e_A	Row Spacing	7.62 BSC	10.16 BSC	10.16 BSC	15.24 BSC	15.24 BSC
S	Lead CL to End	1.52 REF	1.27 REF	1.27 REF	1.90 REF	1.90 REF
Notes	(Leads Affected)	— —	— —	2 (5, 6, 17, 18) —	— —	— —

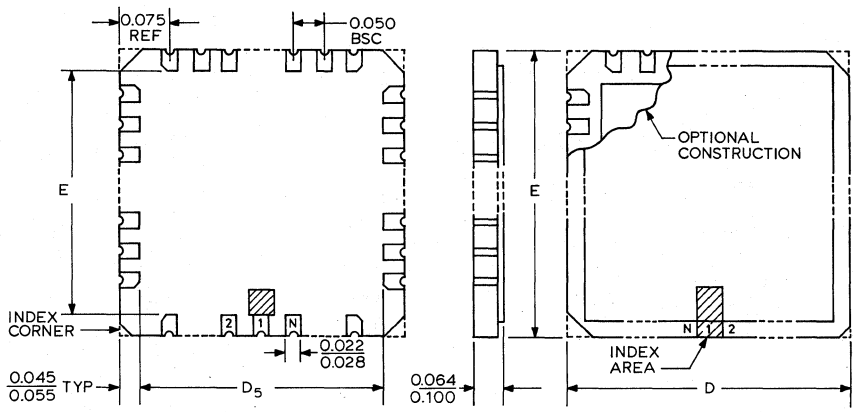
NOTES:
1. Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.
2. Webbed lead frame. Leads indicated are internally one piece.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

CERAMIC LEADLESS CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EK OR EL

Dimensions in Inches



Dwg. No. A 14,156

N	Leads Pkg. Designator	18 EL	20 EK	24 EK	28 EK	32 EL	44 EK
N_D	Leads per Side	4	5	6	7	7	11
N_E	Leads per Side	5	5	6	7	9	11
D	Overall Length	0.280/0.290	0.342/0.358	0.395/0.410	0.442/0.460	0.442/0.458	0.640/0.662
D_5	Contact Spacing	0.185 REF	0.250 REF	0.300 REF	0.350 REF	0.350 REF	0.550 REF
E	Overall Width	0.345/0.365	0.342/0.358	0.395/0.410	0.442/0.460	0.540/0.560	0.640/0.662
E_5	Contact Spacing	0.250 REF	0.250 REF	0.300 REF	0.350 REF	0.450 REF	0.550 REF
M38510F Case Outline		C-9	C-2	C-3	C-4	C-12	C-5

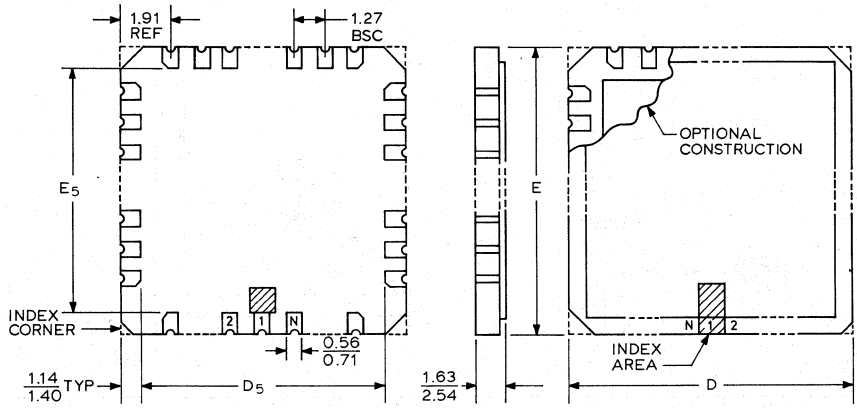
NOTE: Index is centered on D side. Corner shape (square, notch, radius) optional.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

CERAMIC LEADLESS CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EK OR EL

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-14,157

N	Leads Pkg. Designator	18 EL	20 EK	24 EK	28 EK	32 EL	44 EK
N_D		4	5	6	7	7	11
N_E		5	5	6	7	9	11
D	Overall Length	7.11/7.37	8.69/9.09	10.03/10.41	11.23/11.68	11.23/11.63	16.26/16.81
D_5	Contact Spacing	4.70 REF	6.35 REF	7.62 REF	8.89 REF	8.90 REF	13.97 REF
E	Overall Width	8.76/9.27	8.69/9.09	10.03/10.41	11.23/11.68	13.72/14.22	16.26/16.81
E_5	Contact Spacing	6.35 REF	6.35 REF	7.62 REF	8.89 REF	11.43 REF	13.97 REF
M38510F Case Outline		C-9	C-2	C-3	C-4	C-12	C-5

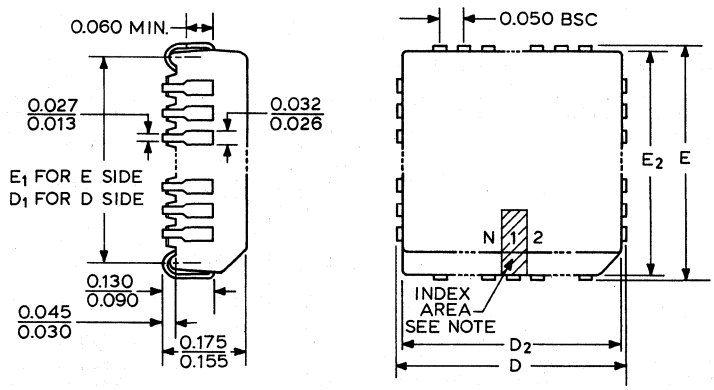
NOTE: Index is centered on D side. Corner shape (square, notch, radius) optional.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC LEADED CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EP

Dimensions in Inches



Dwg. No. A-13,644 IN

N	Leads Pkg. Designator	20 EP	24 EP	28 EP	44 EP
N_D	Leads per Side	5	6	7	11
N_E	Leads per Side	5	6	7	11
D	Overall Length	0.385/0.395	0.370/0.410	0.470/0.510	0.670/0.710
D_1	Row Spacing	0.290/0.330	0.332 REF	0.390/0.430	0.590/0.630
D_2	Body Length	0.350/0.356	0.360/0.380	0.440/0.460	0.640/0.660
E	Overall Width	0.385/0.395	0.370/0.410	0.470/0.510	0.670/0.710
E_1	Row Spacing	0.290/0.330	0.332 REF	0.390/0.430	0.590/0.630
E_2	Body Width	0.350/0.356	0.360/0.380	0.440/0.460	0.640/0.660
JEDEC Designation		MO-047AA	MS-006AA	MS-007AA	MS-007AB

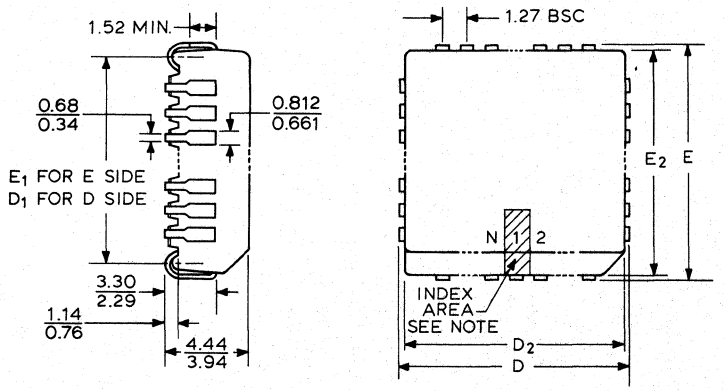
NOTE: Index is centered on "D" side.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC LEADED CHIP CARRIER

SPRAGUE PACKAGE DESIGNATOR EP

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,644 MM

N	Leads Pkg. Designator	20 EP	24 EP	28 EP	44 EP
N_D	Leads per Side	5	6	7	11
N_E	Leads per Side	5	6	7	11
D	Overall Length	9.78/10.03	9.40/10.41	11.94/12.95	17.02/18.03
D_1	Row Spacing	7.37/8.38	8.43 REF	9.91/10.92	15.00/16.00
D_2	Body Length	8.89/9.042	9.15/9.65	11.18/11.68	16.26/16.76
E	Overall Width	9.78/10.03	9.40/10.41	11.94/12.95	17.02/18.03
E_1	Row Spacing	7.37/8.38	8.43 REF	9.91/10.92	15.00/16.00
E_2	Body Width	8.89/9.042	9.15/9.65	11.18/11.68	16.26/16.76
JEDEC Designation		MO-047AA	MS-006AA	MS-007AA	MS-007AB

NOTE: Index is centered on "D" side.

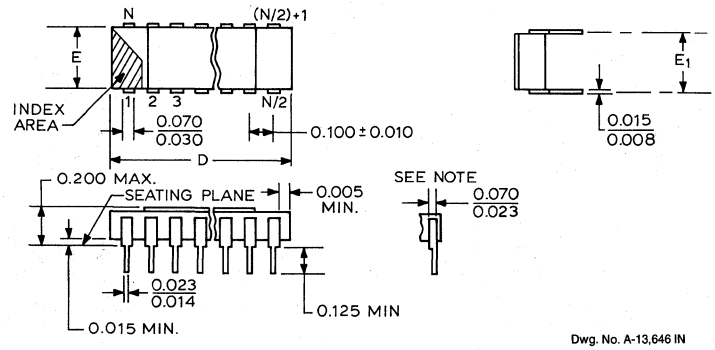
A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

8

HERMETIC DIP

SPRAGUE PACKAGE DESIGNATOR H

Dimensions in Inches



Dwg. No. A-13,646 IN

N	Leads Pkg. Designator	8 H	14 H	16 H	18 H	22 H
D E E_1	Body Length Body Width Row Spacing	0.528 Max. 0.220/0.310 0.290/0.320	0.785 Max. 0.220/0.310 0.290/0.320	0.840 Max. 0.220/0.310 0.290/0.320	0.960 Max. 0.220/0.310 0.290/0.320	1.260 Max. 0.350/0.390 0.390/0.420
Notes	(Leads Affected)	—	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		—	D-1 Configuration 3	D-2 Configuration 3	D-6 Configuration 3	D-7 Configuration 3

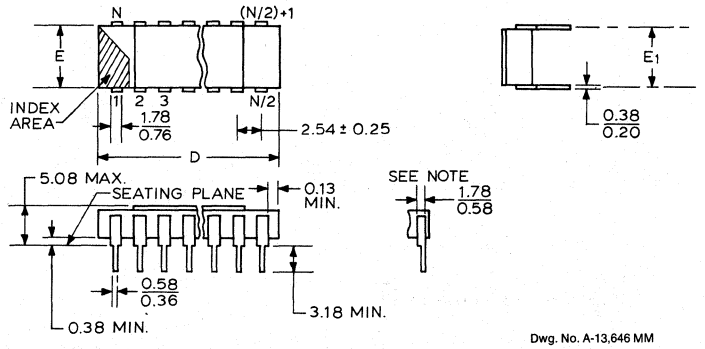
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

HERMETIC DIP

SPRAGUE PACKAGE DESIGNATOR H

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,646 MM

N	Leads Pkg. Designator	8 H	14 H	16 H	18 H	22 H
D	Body Length	13.41 Max.	19.94 Max.	21.34 Max.	24.38 Max.	32.00 Max.
E	Body Width	5.59/7.87	5.59/7.87	5.59/7.87	5.59/7.87	8.89/9.91
E_1	Row Spacing	7.37/8.13	7.37/8.13	7.37/8.13	7.37/8.13	9.91/10.67
Notes	(Leads Affected)	—	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		—	D-1 Configuration 3	D-2 Configuration 3	D-6 Configuration 3	D-7 Configuration 3

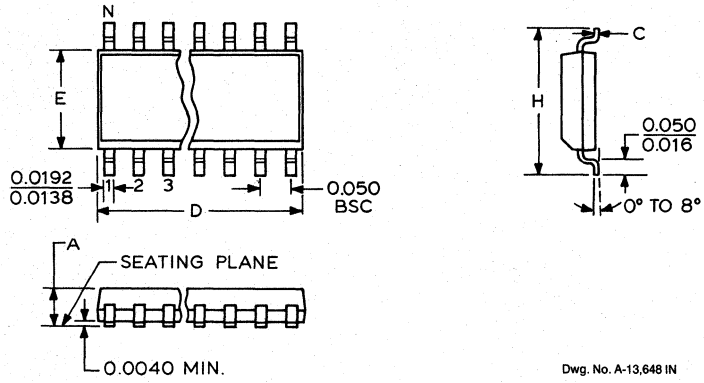
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC SOIC

SPRAGUE PACKAGE DESIGNATOR L, LB, OR LW

Dimensions in Inches
(Based on 1 mm = 0.03937")



Dwg. No. A-13,648 IN

N	Leads Pkg. Designator	8 L	14 L	16 L	16 LW	18 LW
A	Seated Height	0.0532/0.0688	0.0532/0.0688	0.0532/0.0688	0.0926/0.1043	0.0926/0.1043
C	Lead Thickness	0.0075/0.0098	0.0075/0.0098	0.0075/0.0098	0.0091/0.0125	0.0091/0.0125
D	Body Length	0.1890/0.1968	0.3367/0.3444	0.3859/0.3937	0.3977/0.4133	0.4469/0.4625
E	Body Width	0.1497/0.1574	0.1497/0.1574	0.1497/0.1574	0.2914/0.2992	0.2914/0.2992
H	Overall Width	0.2284/0.2440	0.2284/0.2440	0.2284/0.2440	0.394/0.419	0.394/0.419
Notes	(Leads Affected)	—	—	—	—	—
JEDEC Designation		MS-012AA	MS-012AB	MS-012AC	MS-013AA	MS-013AB

N	Leads Pkg. Designator	20 LB	20 LW
A	Seated Height	0.0926/0.1043	0.0926/0.1043
C	Lead Thickness	0.0091/0.0125	0.0091/0.0125
D	Body Length	0.4961/0.5118	0.4961/0.5118
E	Body Width	0.2914/0.2992	0.2914/0.2992
H	Overall Width	0.394/0.419	0.394/0.419
Notes	(Leads Affected)	(4-7, 14-17)	—
JEDEC Designation		MS-013AC	MS-013AC

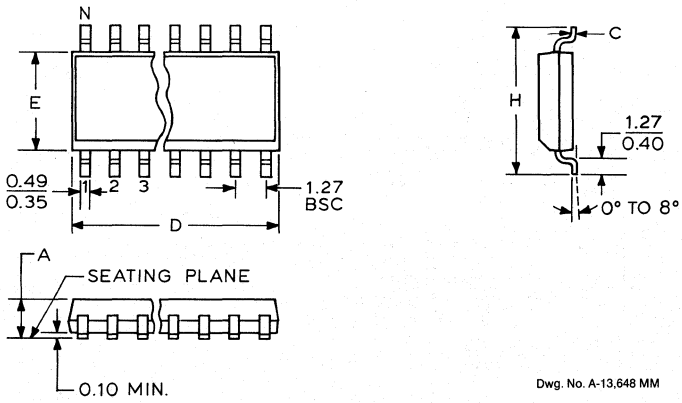
NOTE: Webbed lead frame. Leads indicated are internally one piece.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC SOIC

SPRAGUE PACKAGE DESIGNATOR L, LB, OR LW

Dimensions in Millimeters



Dwg. No. A-13,648 MM

N	Leads Pkg. Designator	8 L	14 L	16 L	16 LW	18 LW
A	Seated Height	1.35/1.75	1.35/1.75	1.35/1.75	2.35/2.65	2.35/2.65
C	Lead Thickness	0.19/0.25	0.19/0.25	0.19/0.25	0.23/0.32	0.23/0.32
D	Body Length	4.80/5.00	8.55/8.75	9.80/10.0	10.10/10.50	11.35/11.75
E	Body Width	3.80/4.00	3.80/4.00	3.80/4.00	7.40/7.60	7.40/7.60
H	Overall Width	5.80/6.20	5.80/6.20	5.80/6.20	10.0/10.65	10.0/10.65
Notes	(Leads Affected)	—	—	—	—	—
JEDEC Designation		MS-012AA	MS-012AB	MS-012AC	MS-013AA	MS-013AB

N	Leads Pkg. Designator	20 LB	20 LW
A	Seated Height	2.35/2.65	2.35/2.65
C	Lead Thickness	0.23/0.32	0.23/0.32
D	Body Length	12.60/13.00	12.60/13.00
E	Body Width	7.40/7.60	7.40/7.60
H	Overall Width	10.0/10.65	10.0/10.65
Notes	(Leads Affected)	(4-7, 14-17)	—
JEDEC Designation		MS-013AC	MS-013AC

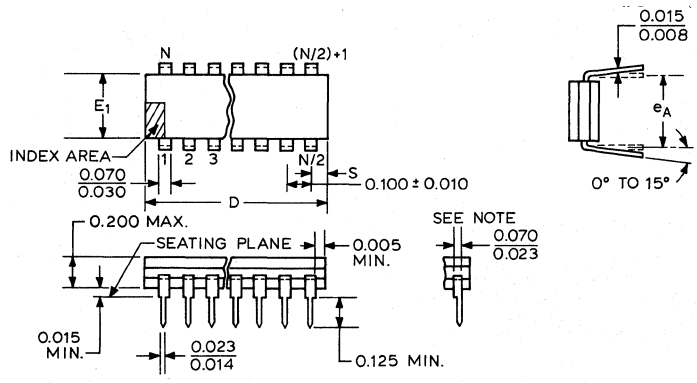
NOTE: Webbed lead frame. Leads indicated are internally one piece.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

HERMETIC CERDIP

SPRAGUE PACKAGE DESIGNATOR R

Dimensions in Inches



Dwg. No. A-13,650 IN

N	Leads Pkg. Designation	14 R	16 R	18 R	22 R
D	Body Length	0.785 Max.	0.840 Max.	0.960 Max.	1.260 Max.
E_1	Body Width	0.220/0.310	0.220/0.310	0.220/0.310	0.350/0.390
e_A	Row Spacing	0.300 BSC	0.300 BSC	0.300 BSC	0.400 BSC
S	Lead CL to End	0.075 Ref.	0.025 Ref.	0.050 Ref.	0.025 Ref.
Notes	(Leads Affected)	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		D-1 Configuration 1	D-2 Configuration 1	D-6 Configuration 1	D-7 Configuration 1

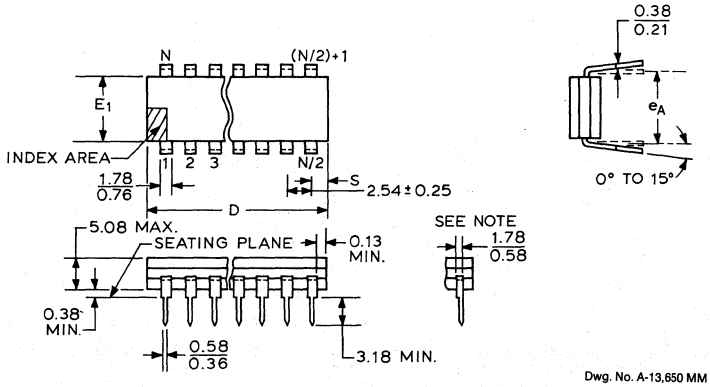
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

HERMETIC CERDIP

SPRAGUE PACKAGE DESIGNATOR R

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,650 MM

N	Leads Pkg. Designation	14 R	16 R	18 R	22 R
D	Body Length	19.94 Max.	21.34 Max.	24.38 Max.	32.00 Max.
E_1	Body Width	5.59/7.87	5.59/7.87	5.59/7.87	8.89/9.91
e_A	Row Spacing	7.62 BSC	7.62 BSC	7.62 BSC	10.16 BSC
S	Lead CL to End	1.91 REF	0.64 REF	1.27 REF	1.27 REF
Notes	(Leads Affected)	—	(1, 8, 9, 16)	—	—
M38510F Case Outline		D-1 Configuration 1	D-2 Configuration 1	D-6 Configuration 1	D-7 Configuration 1

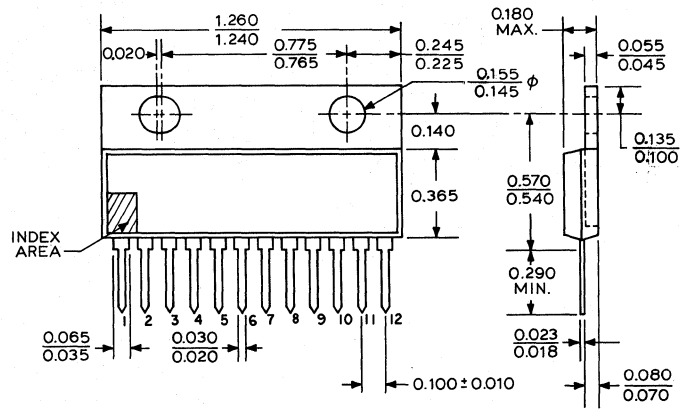
NOTE: Leads 1, N/2, (N/2) + 1, and N may be half-leads at vendor's option.

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall.also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR W

Dimensions in Inches



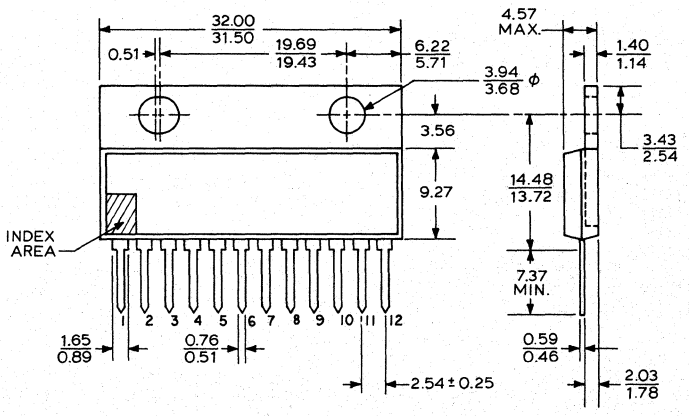
Dwg. No. A-13,652 IN

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR W

Dimensions in Millimeters
(Based on 1" = 25.40 mm)



Dwg. No. A-13,652 MM

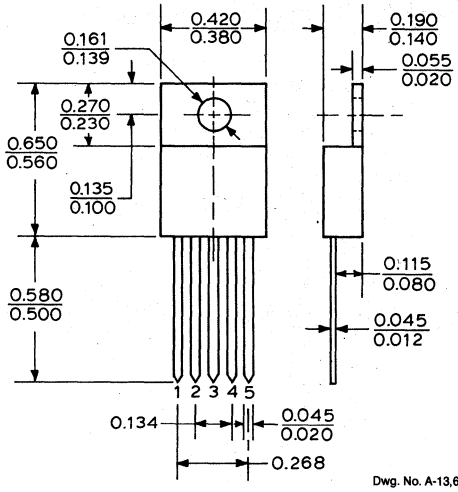
A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR Z, ZH OR ZV

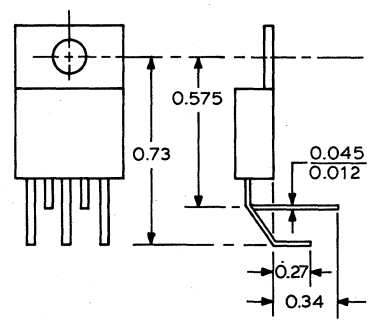
Dimensions in Inches

DESIGNATOR Z
(JEDEC Designation TO-220AB)



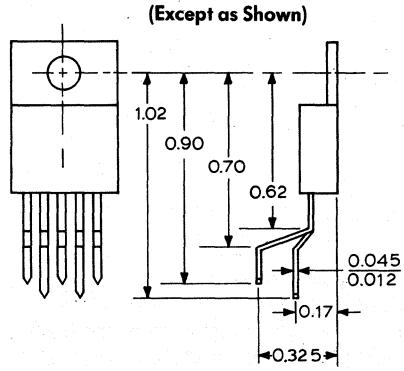
Dwg. No. A-13,654 IN

DESIGNATOR ZH
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,655 IN

DESIGNATOR ZV
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,656 IN

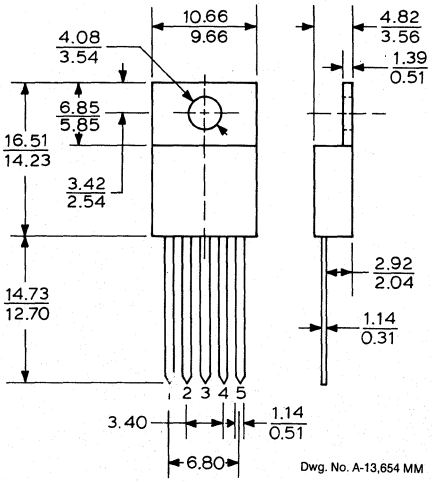
A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 0.030" max. below seating plane.

PLASTIC SIP

SPRAGUE PACKAGE DESIGNATOR Z, ZH OR ZV

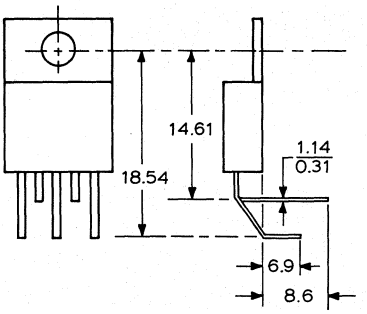
Dimensions in Millimeters
(Based on 1" = 25.40 mm)

DESIGNATOR Z
(JEDEC Designation TO-220AB)



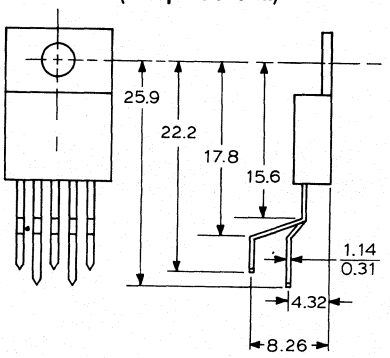
Dwg. No. A-13,654 MM

DESIGNATOR ZH
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,655 MM

DESIGNATOR ZV
PACKAGE Z
(Except as Shown)



Dwg. No. A-13,656 MM

A. Dimensions shown as ——/——are Min./Max.
B. Lead thickness is measured at seating plane or below.
C. Lead spacing tolerance is non-cumulative.
D. Exact body and lead configuration at vendor's option within limits shown.
E. Leads missing from their designated positions shall also be counted when numbering leads.
F. Lead gauge plane is 7.62 mm max. below seating plane.

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

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SPRAGUE

THE MARK OF RELIABILITY

E/EOBA

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