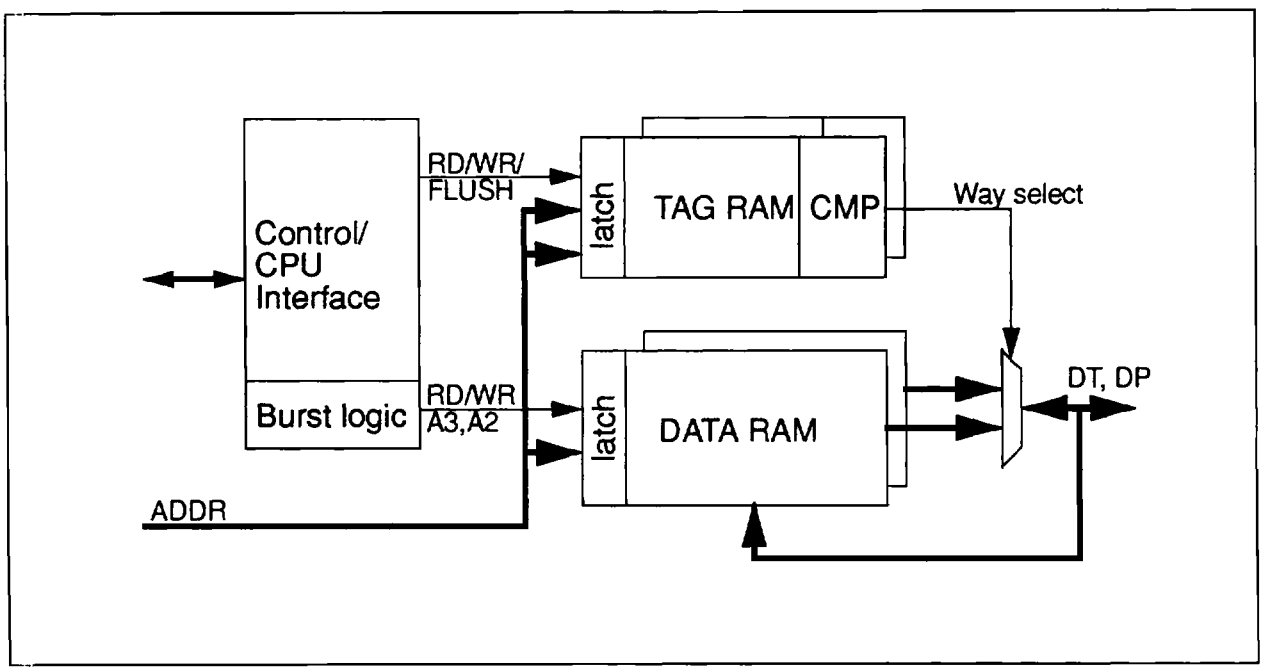
FEATURES

- Single Chip Cache Subsystem for 486 CPU
- Look-aside Architecture
- Write-through Cache Operation
- 33 and 50 MHz Operating Frequency
- 256k byte Two-way-set Associativity
- Cascadable up to 1M bytes
- Enhanced Cascade Mode
- Zero Wait State Burst (2-1-1-1)
- PC compatible
- 160-pin PQFP package

DESCRIPTION

The SONY Cache-2 is a single chip cache subsystem designed to work with the 486SX/DX/DX2 microprocessors at frequencies up to 50MHz. This device is designed utilizing SONY's proprietary Memory-intensive ASIC (MASIC™) technology. Using MASIC, the SONY Cache-2 integrates 256k bytes of cache memory, tag ram and associated control logic on a single chip. As a look-aside secondary cache, this device can be incorporated into various systems using different core-logic chipsets. This device can be designed onto a motherboard as a standard or an upgradeable feature. Multiple SONY Cache-2 chips can be cascaded to provide different levels of cache sizes and performances. A proprietary Enhanced Cascade Mode allows cascading at high speed without using external glue logic. High performance, high integration and low power characteristics render this device ideal for high performance desktop and mobile computing applications.

SONY Cache-2 BLOCK DIAGRAM



1 SONY Cache-2 Pinout

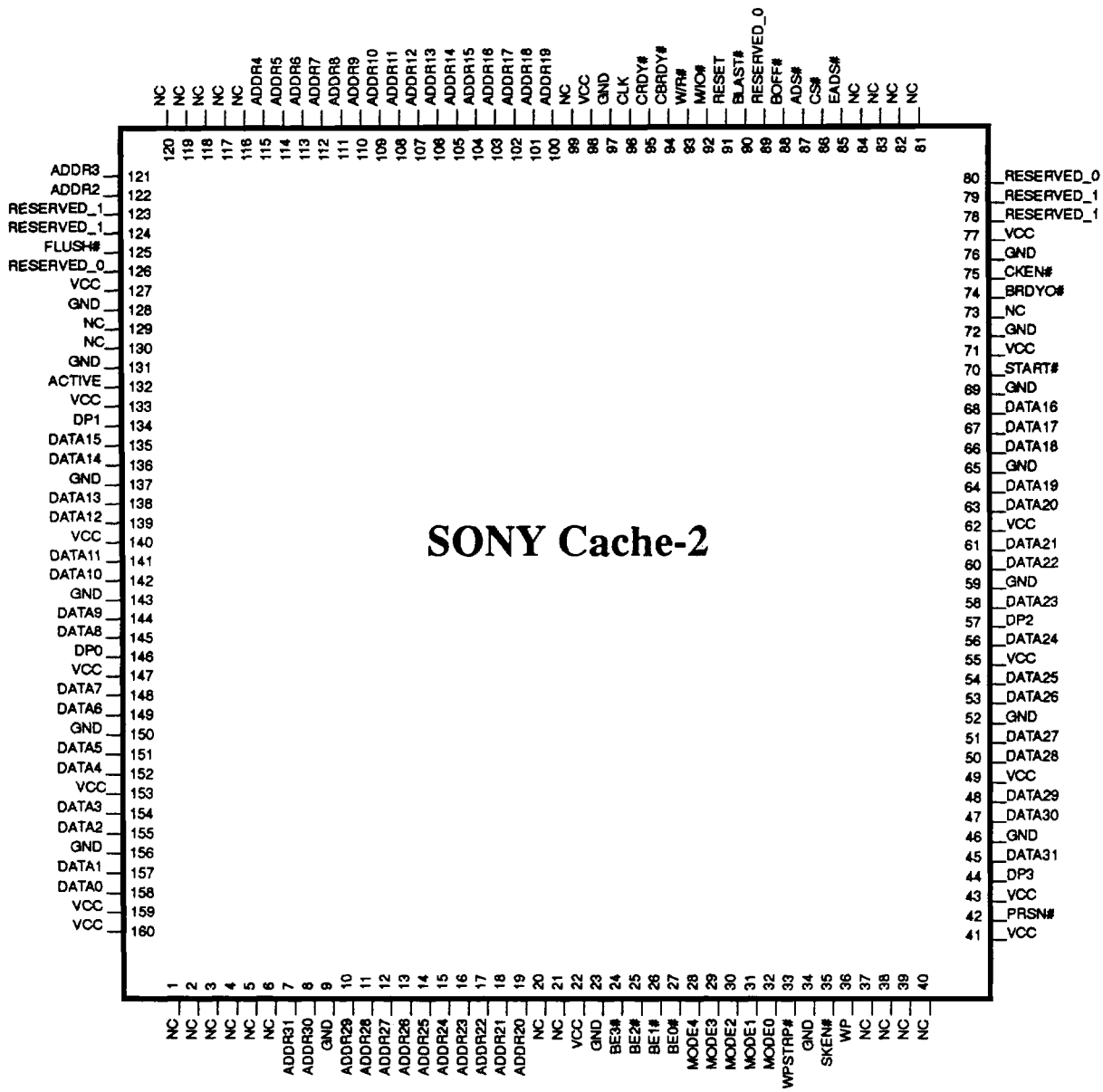


Figure 1.1 160-pin PQFP package pinout

Notes: "RESERVED_0" pins should be connected to Gnd through resistive pull-down.
"RESERVED_1" pins should be connected to Vcc through resistive pull-up.
"NC" pins should not be connected externally. Some of these pins may be driven by the SONY Cache-2.

1.1 Table of package pin number and pin names

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	NC	41	VCC	81	NC	121	ADDR3
2	NC	42	PRSN#	82	NC	122	ADDR2
3	NC	43	VCC	83	NC	123	RESERVED_1
4	NC	44	DP3	84	NC	124	RESERVED_1
5	NC	45	DATA31	85	EADS#	125	FLUSH#
6	NC	46	GND	86	CS#	126	RESERVED_0
7	ADDR31	47	DATA30	87	ADS#	127	VCC
8	ADDR30	48	DATA29	88	BOFF#	128	GND
9	GND	49	VCC	89	RESERVED_0	129	NC
10	ADDR29	50	DATA28	90	BLAST#	130	NC
11	ADDR28	51	DATA27	91	RESET	131	GND
12	ADDR27	52	GND	92	M/IO#	132	ACTIVE
13	ADDR26	53	DATA26	93	W/R#	133	VCC
14	ADDR25	54	DATA25	94	CBRDY#	134	DP1
15	ADDR24	55	VCC	95	CRDY#	135	DATA15
16	ADDR23	56	DATA24	96	CLK	136	DATA14
17	ADDR22	57	DP2	97	GND	137	GND
18	ADDR21	58	DATA23	98	VCC	138	DATA13
19	ADDR20	59	GND	99	NC	139	DATA12
20	NC	60	DATA22	100	ADDR19	140	VCC
21	NC	61	DATA21	101	ADDR18	141	DATA11
22	VCC	62	VCC	102	ADDR17	142	DATA10
23	GND	63	DATA20	103	ADDR16	143	GND
24	BE3#	64	DATA19	104	ADDR15	144	DATA9
25	BE2#	65	GND	105	ADDR14	145	DATA8
26	BE1#	66	DATA18	106	ADDR13	146	DP0
27	BE0#	67	DATA17	107	ADDR12	147	VCC
28	MODE4	68	DATA16	108	ADDR11	148	DATA7
29	MODE3	69	GND	109	ADDR10	149	DATA6
30	MODE2	70	START#	110	ADDR9	150	GND
31	MODE1	71	VCC	111	ADDR8	151	DATA5
32	MODE0	72	GND	112	ADDR7	152	DATA4
33	WPSTRP#	73	NC	113	ADDR6	153	VCC
34	GND	74	BRDYO#	114	ADDR5	154	DATA3
35	SKEN#	75	CKEN#	115	ADDR4	155	DATA2
36	WP	76	GND	116	NC	156	GND
37	NC	77	VCC	117	NC	157	DATA1
38	NC	78	RESERVED_1	118	NC	158	DATA0
39	NC	79	RESERVED_1	119	NC	159	VCC
40	NC	80	RESERVED_0	120	NC	160	VCC

2 Pin Descriptions

2.1 Address:

ADDR[31:2]	I/O	Address pins shared by the CPU and the cache subsystem on the host bus.
BE#[3:0]	I/O	Byte Enable. These signals allow individual bytes within a doubleword to be updated independently. They are ignored in all read cycles.

2.2 Data:

DATA[31:0]	I/O	Data pins on the host bus.
DP[3:0]	I/O	Data parity. One parity bit for each data byte. The SONY Cache-2 does not perform parity check. These bits are read and written like other data bits.

2.3 Control:

ACTIVE	O	This signal serves as an indicator in Enhanced Cascade mode to indicator which one of the SONY Cache-2 chip has been selected to handle memory access. This pin should be used for debugging purpose only and should not be used during normal operation.
ADS#	I/O	Address Strobe. It is an input from the CPU to indicate the start of an access cycle. The ADDR[31:2], BE#[3:0], CS#, M/IO# and W/R# signals must be valid when ADS# is active.
BLAST#	I/O	End-of-Burst indicator. Driven by the CPU to indicate the end of a burst cycle.
BOFF#	I	BOFF# is an input generated by the system logic to back-off the CPU and the SONY Cache-2 from the host bus. Any on-going bus access is aborted in the next cycle when BOFF# is active.

BRDYO#	I/O	Burst ready is generated by the SONY Cache-2 to indicate that a read hit has occurred and that data is being returned on the data bus. It also indicates that the SONY Cache-2 can transfer the entire cache line by using burst mode. Burst ready is normally tri-stated. During read hit, it is asserted by the SONY Cache-2 until the read cycle is terminated, and then driven high for one cycle before being tri-stated. It is an I/O pin during Enhanced Cascade mode.
CBRDY#	I	Cache data burst ready. Generated by the system logic to indicate that one cycle of data transfer has been completed and that burst mode can be used to transfer more data. This pin can be connected externally to BRDYO# to form an I/O pin that can be directly connected to the BRDY# input of the CPU. See appendix for more detail.
CKEN#	O	Cache Enable. This pin is driven by the SONY Cache-2 to indicate to the CPU if the read hit data from the SONY Cache-2 is cacheable in the CPU's internal cache. It can be sampled by the CPU in the same way as it samples KEN#. A line that is in the SONY Cache-2 is not cacheable in the CPU only if it is write protected and the write protect strap option is on.
CLK	I	System clock. Same as the 486 1X clock.
CRDY#	I	Cache data ready. Generated by the system logic to terminate the current bus cycle and to stop the burst transfer. CRDY# can be connected externally to RDYO# to form an I/O pin. See appendix for more detail.
CS#	I	Chip Select. This signal is must be asserted with ADS# and EADS#; otherwise ADS# and EADS# are ignored. When Enhanced Cascade Mode is used, CS# must be tied low.
EADS#	I	External Address Strobe. The SONY Cache-2 performs a snoop cycle when EADS# is active. The snoop address is sampled at the same time as EADS# is sampled low. If the snoop address hits a cache line, that cache line is invalidated internally.
FLUSH#	I	FLUSH# invalidates all the cache lines in the SONY Cache-2. This can be used to ensure that any stale data, if present, will be purged from the cache.
M/IO#	I/O	Memory and I/O selector. Memory is selected if this signal is high, otherwise I/O is selected.

MODE[4:0]	I	Operation mode selector. Static input pins. Selects between normal mode, Enhanced Cascade mode and test mode. MODE4:0] Description 00000 Normal mode, 256K byte 00100 Enhanced Cascade mode, 1024K, chip0 00101 Enhanced Cascade mode, 1024K, chip1 00110 Enhanced Cascade mode, 1024K, chip2 00111 Enhanced Cascade mode, 1024K, chip3 01100 Enhanced Cascade mode, 512K, chip0 01101 Enhanced Cascade mode, 512K, chip1 all other mode pin combinations are reserved.
NC	--	These pins must be left unconnected to any external signal. Some of these signal may be driven by the SONY Cache-2
PRSN#	O	This is a static output pin that always drives low. It allows the system logic to detect the presence of the SONY Cache-2 chip.
RESET	I	Resets the SONY Cache-2 to the initial state and invalidates all the tag entries. The SONY Cache-2 must be reset after power-up or after mode pin changes.
RESERVED_0	I	These pins must be tied low through pull-down resistors.
RESERVED_1	I	These pins must be tied high through pull-up resistors.
SKEN#	I	Cacheability indicator. This signal is sampled by the SONY Cache-2 to determine if a line fill is cacheable. It is sampled twice during a line fill. It is first sampled one clock cycle before the first CBRDY#. It is sampled again one clock cycles before the last CBRDY# of the line fill. SKEN# must be active during both sampling points; otherwise the line fill is not cacheable.
START#	I/O	The START# pin indicates to the system memory that a read miss or memory write has occurred. The system memory is required to handle these cycles.
W/R#	I/O	Read/Write select. High indicates a write cycle and low indicates a read cycle.
WP	I	The Write Protect signal indicates if a cache line is write protected. It is sampled at the third cycle of a cache line fill. If WP is high and the write protect strap option is on, the line is write protected and any further attempts to write to this location will be ignored.
WPSTRP#	I	Write Protect Strap. It is sampled at the falling edge of RESET. It must be stable for two clocks before and after the falling edge of RESET. If WPSTRP# is sampled active, the write protect strap option is turned on. The SONY Cache-2 will use the WP pin to determine the write protection of the cache line. If WPSTRP# is sample inactive, the WP input will have no effect.

3 Functional Descriptions

3.1 Introduction

The SONY Cache-2 is designed to work with the 486 microprocessor in a "look aside" configuration. Data and address buses from the CPU are routed to the system memory and the SONY Cache-2 in parallel. If data read by the CPU is present in the SONY Cache-2, i.e. cache hit, the SONY Cache-2 returns its cache data to the CPU without requiring services from the system memory.

If data needed by the CPU is not in the SONY Cache-2, the it will start a memory cycle. The SONY Cache-2 will monitor the transactions between the CPU and memory. Data returned from the memory is captured by the CPU and the SONY Cache-2 at the same time. The control logic within the SONY Cache-2 caches the newly returned data automatically. Future references to the same data will produce a cache hit in the SONY Cache-2 so that data can be transferred to the CPU with zero wait state.

The SONY Cache-2 is a write-through cache so that all write data will be written into the system memory and, for write hit, to the SONY Cache-2 simultaneously. The write-through design guarantees data consistency between the cache and system memory whenever data is written by the CPU.

The SONY Cache-2 interface logic understands the CPU bus cycles for memory accesses. It monitors all the transactions between the CPU and external cache/memory but does not generate bus transactions of its own. This near-transparent design minimizes overheads for cache fill and allows the SONY Cache-2 to be incorporated into any motherboard design with minimum design changes. A motherboard can be designed with the SONY Cache-2 as a plug-in option to offer different levels of performance. Figure 3.1 shows a typical system configuration with the SONY Cache-2.

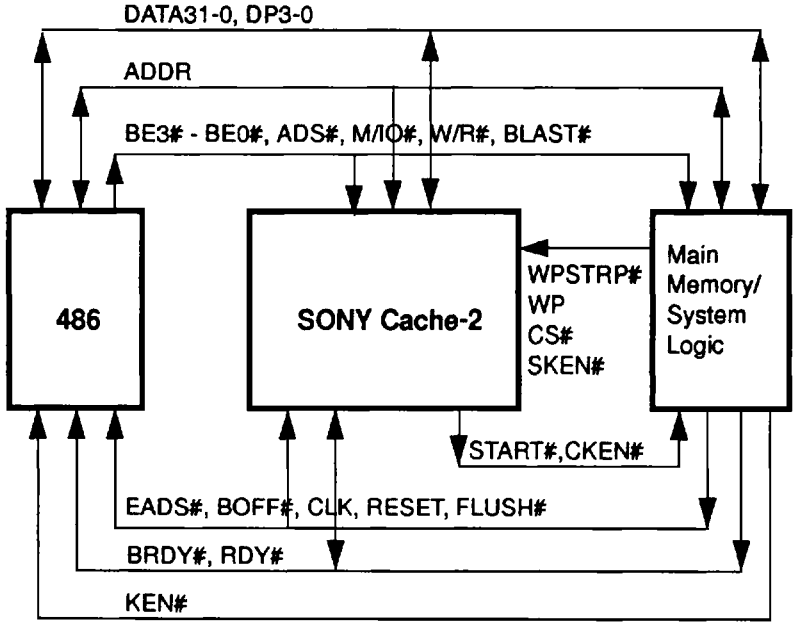


Figure 3.1 Typical System Configuration

3.2 Internal Architecture

The SONY Cache-2 is a 256k byte 2-way-set-associative cache system with line size of 16 bytes. Each WAY contains 4k tags and each tag controls two lines of cache memory. The upper address bits, ADDR[31:17] are stored in the tag when data is written into the cache. The next lower address bits, ADDR[16:5] select one of the 4k tags and the address bits ADDR[4:2] select the line and the doubleword within the cache line.

Since the cache is 2-way-set-associative, there are two possible locations for each data line to be stored in the cache. During a read, address bits 16 to 5 access the two tag entries simultaneously and the two tags are compared with the address bits 31 to 17. The matched tag indicates the corresponding data are stored in the cache; thus a cache hit is generated. Once a cache hit is detected, memory reads for any of the bytes within the cache line can be read from the cache. If neither of the tags matches the address bits or the tags are invalid then a cache miss is generated and data must be read from system memory.

When a data line is read from system memory it is cached into the SONY Cache-2 and the CPU at the same time. A Least Recently Used (LRU) algorithm is used to select one of the two WAYs to store the new data. An LRU bit is maintained for each of the 4k tags for cache update. Since the SONY Cache-2 is a write-through cache, there is no need to copy the existing data to the system memory during cache replacement.

3.3 Interface to CPU

The SONY Cache-2 is designed specifically for a 486-based motherboard and it understands the memory access cycles generated by the CPU. It monitors ADS#, CS#, M/IO#, W/R#, and ADDR to initiate a cache read. If the read address produces a cache hit, the SONY Cache-2 returns data with zero wait states. Since the entire cache line is valid in the SONY Cache-2, it transfers data to the CPU using burst mode by asserting BRDYO#. If the CPU indicates it is also ready to accept more data by de-asserting BLAST#, the burst sequence will continue and the remaining doublewords of the cache line will be sent to the CPU with zero wait state until BLAST# is asserted. Data returned from the SONY Cache-2 is cacheable in the CPU's internal cache unless the WP (write protect) bit of the cache tag is set and the WSTRP option is on. Figure 3.2 is a timing diagram of a read hit cycle.

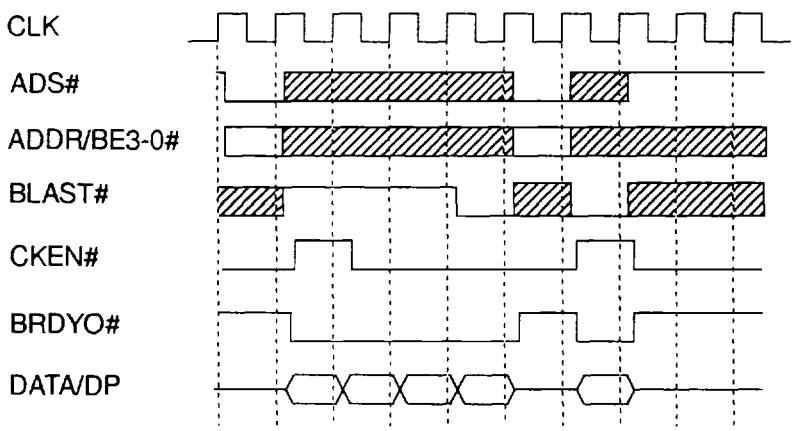


Figure 3.2 Cache hit with CPU reading four words followed by cache hit with CPU reading one word.

3.4 Interface to system memory

If a memory read produces a cache hit, the SONY Cache-2 will return data directly to the CPU without alerting the system memory, However, if the read access produces a cache miss, system memory is activated by the SONY Cache-2 to serve the memory read. It indicates a cache miss to the system memory by asserting START#. Other control signals such as M/IO#, W/R# and ADDR are available to the system memory directly from the CPU. The SONY Cache-2 monitors the ready signals, CRDY# and CBRDY#, from system memory to read data from the DATA bus. The system memory can use burst or non-burst mode to return data to the CPU and the SONY Cache-2. Data from the system memory is cacheable in the SONY Cache-2 only if the SKEN# input is driven active one clock cycle before the first data returns from the system memory and one clock cycle before the last data. If a cache line fill is aborted before it is completed, the SONY Cache-2 will not update its cache line. Figure 3.3 and Figure 3.4 show the interactions between the SONY Cache-2, system memory and the CPU during cache misses.

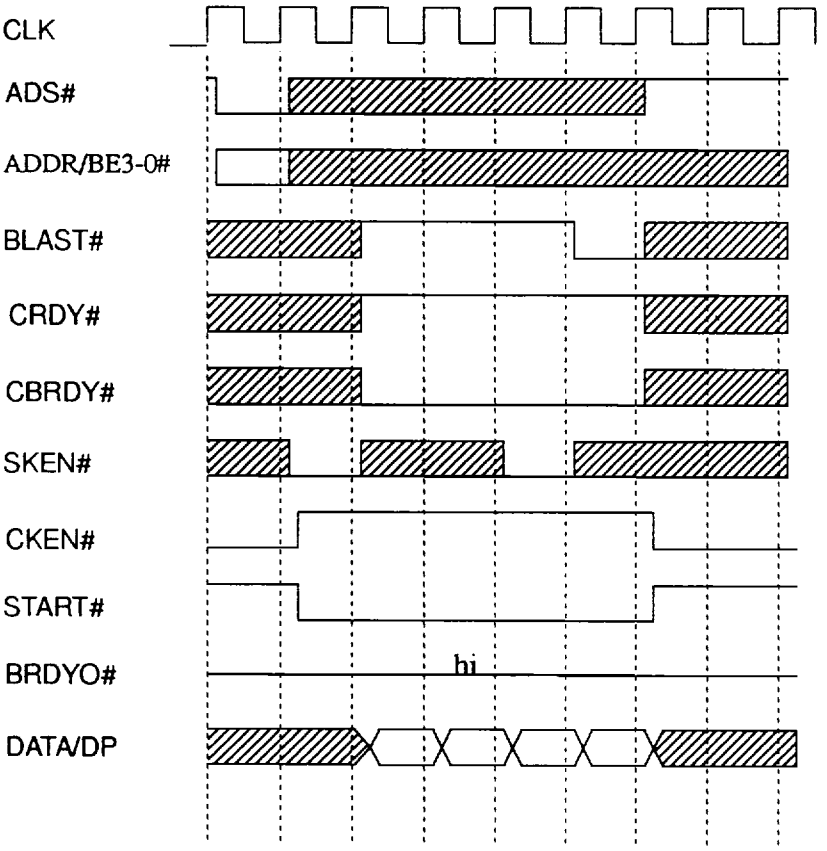


Figure 3.3 Line fill with burst mode and no wait state

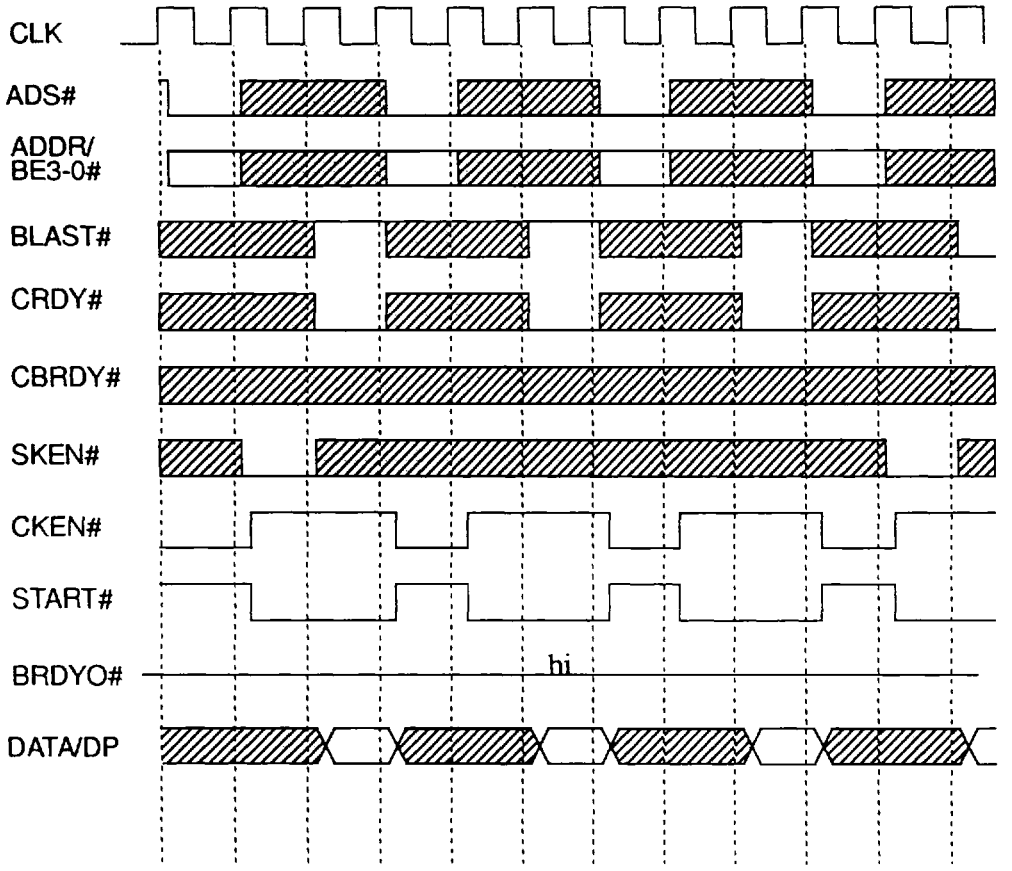


Figure 3.4 Read miss with non-burst line fill

3.5 Write sequences

A write-through cache design implies that every time the CPU writes data into memory, the cache and the system memory are updated at the same time. If the write data is already in the cache (write hit), the SONY Cache-2 updates its cache line and activates START# to initiate the memory update. If the write data is not in the cache (write miss), the SONY Cache-2 activates START# but does not operate on the data. Figure 3.5 shows the timing sequences of write cycles.

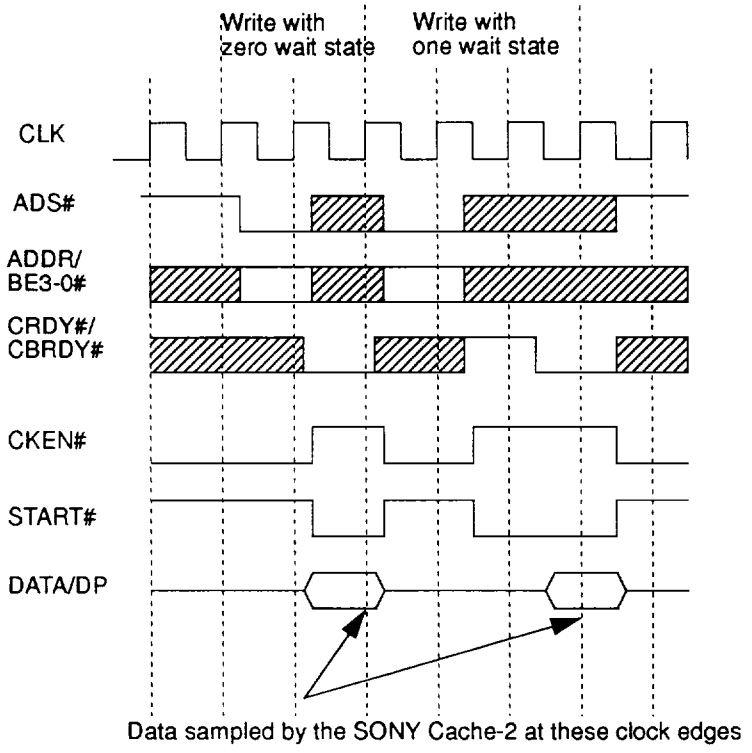


Figure 3.5 Write hit cycle

3.6 Cache Line Snoop

In order to support external bus master and DMA transfers efficiently, the SONY Cache-2 has the capability of invalidating an individual cache line when the line is updated by a master other than the CPU. To invalidate a cache line, the external master performs a snoop cycle by asserting EADS# and drives the valid address on to ADDR[31:4]. The SONY Cache-2 checks its tags for a cache hit. The line is invalidated if it is found in the cache.

The SONY Cache-2 can be snooped once every two clock cycles. It requires one cycle for reading the tag entries and one cycle for invalidating the tag. Invalidation can run at the same time the SONY Cache-2 is doing a line fill since ADDR[31:4] and EADS# are not used during a line fill. A cache access after the current line fill, however, can be delayed if the line fill and invalidation cycles are running in parallel. Figure 3.6 illustrate the timing sequences.

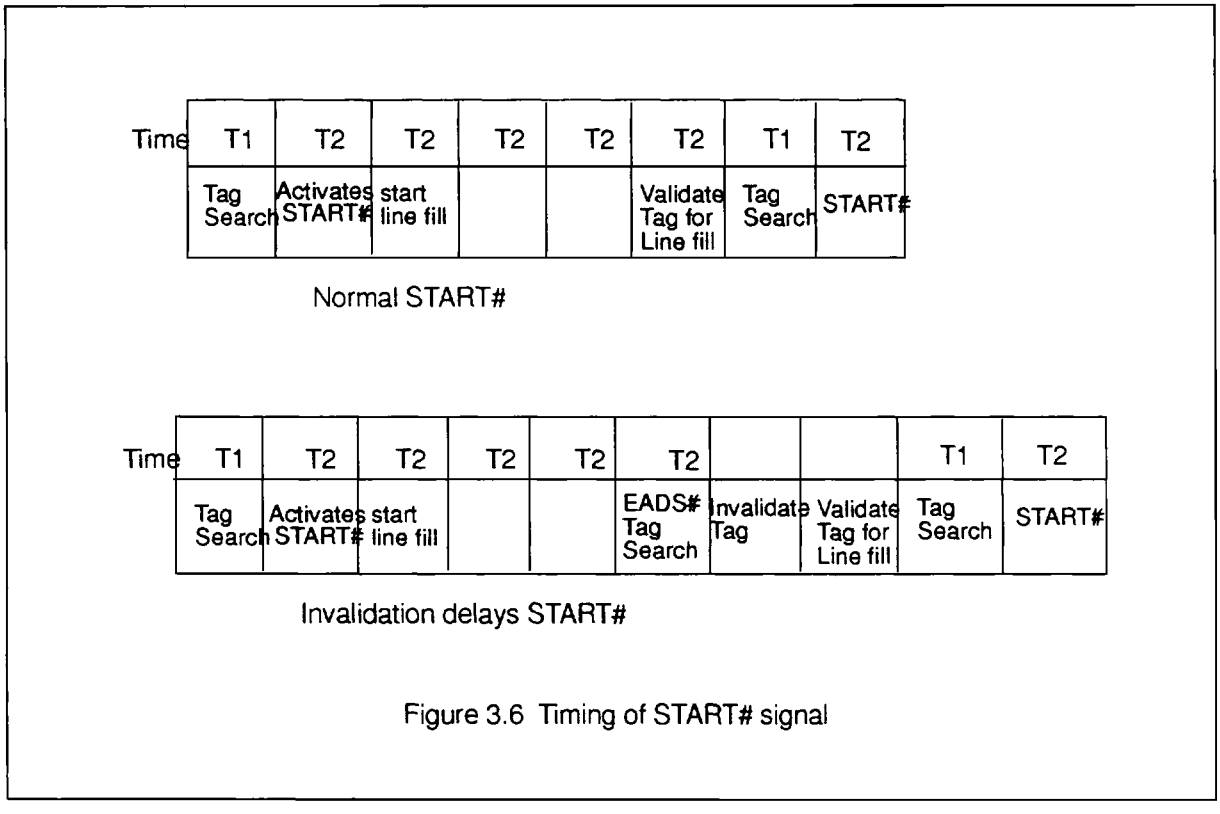


Figure 3.6 Timing of START# signal

3.7 Backoff

To further support multiple bus master systems and to avoid deadlock, a backoff feature is incorporated. With this feature, the external master can assert the BOFF# input to the SONY Cache-2 anytime during operation. The SONY Cache-2 immediately relinquish the bus and abort any read or write cycle it may be running at the time. After BOFF# has been de-asserted, it waits for the CPU to start a new operation. Figure 3.7 is an example of asserting BOFF# during read hit.

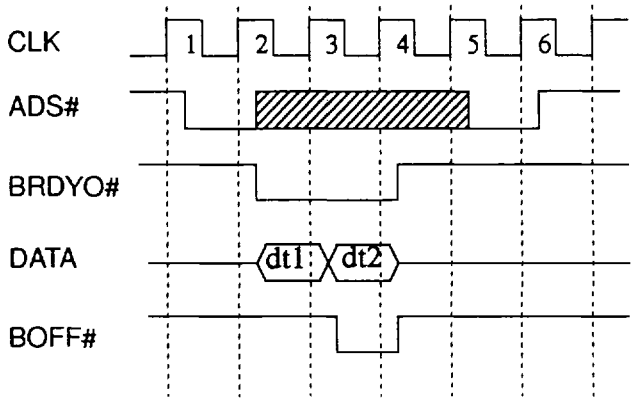


Figure 3.7 BOFF# asserted during read hit

Notes:

1. BOFF# may be asserted at any cycle. Current memory access is aborted and will not be restarted after BOFF# is de-asserted.
2. Asserting ADS# at cycle 5 starts a new memory access.

3.8 Enhanced Cascade Modes

Multiple SONY Cache-2 chips can be cascaded together to increase cache size. A special cascading method, called the Enhanced Cascade Mode, was developed to cascade multiple SONY Cache-2 chips together without using any external glue logic. Under this mode, each SONY Cache-2 chip in the system decodes the address internally and responds to a specific address range for read, write and snoop cycles. In 2-chip cascade mode, ADDR17 is used as internal select. In 4-chip cascade mode, ADDR[18:17] are both used to decode the internal select. The chips that are not selected for read or write are disabled. Outputs from all 2 or 4 SONY Cache-2 chips can be wired together since only one chip is actively driving during normal operation. Figure 3.8 illustrates the Enhanced Cascade mode used in a four chip cascade design.

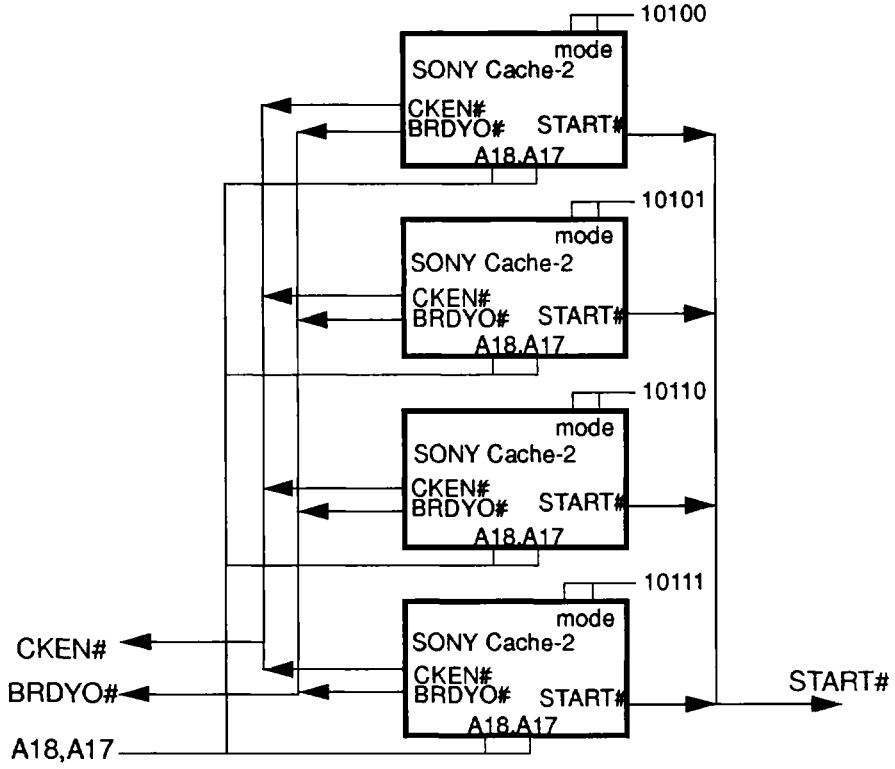


Figure 3.8 Enhanced Cascade Mode with no external glue logic.

4 Electrical Specifications

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	VCC	-1.0 to +7	V
Input Voltage	VIN	-0.5 to + VCC + 0.5	V
Power Dissipation	PDmax	1.8	W
Ambient(Operating) Temperature	TOPR	0 to +70	°C
Storage Temperature	TSTG	-65 to +150	°C

D. C. Characteristics

Item	Symbol	Min	Max	Unit
Supply Voltage	Vcc	4.75	5.25	V
Input low voltage	VIL	-0.3	+0.8	V
Input high voltage	VIH	2.2	Vcc + 0.3	V
Output low voltage @4.5mA	VOL		0.4	V
Output high voltage @-1.0mA	VOH	2.4		V
Input leakage current	ILI	-1	1	µA
Output leakage current	ILO	-1	1	µA
Capacitance: PQFP Clock pin Other input pins Output pins I/O pins	Cin		 9 7 9 9	 pF pF pF pF

Package Thermal Resistance

Parameter	Air Flow (Meters/Second)			
	0	1 m/s	2 m/s	3 m/s
$Ø_{JA}$ (°C/W)	30.5	22.6	20.4	17.7
$Ø_{JC}$ (°C/W)	6.3			

5 A.C. Specifications

Operating Conditions: 5V Vcc, ± 5%, 0 to 70°C

Symbol	Parameter	50MHz		33MHz		Fig
		Min(ns)	Max(ns)	Min(ns)	Max(ns)	
t_1	CLK Period	20		30		5.1
t_2	CLK High Time	6		11		5.1
t_3	CLK Low Time	6		11		5.1
t_{4a}	CLK Fall Time		3		3	5.1
t_{4b}	CLK Rise Time		3		3	5.1
t_{5a}	ADDR, BE0#-BE3# Setup (Non-Snoop)	5		13		5.2
t_{5b}	ADDR, BE# - BE3# Hold (Non-Snoop)	3		4		5.2
t_{6a}	ADS#, M/IO#, W/R# Setup	5		13		5.2
t_{6b}	ADS#, M/IO#, W/R# Hold	3		4		5.2
t_{7a}	BLAST# Setup	5		9		5.2
t_{7b}	BLAST# Hold	3		4		5.2
t_{8a}	CRDY#, CBRDY# Setup	4		5		5.2
t_{8b}	CRDY#, CBRDY# Hold	3		4		5.2
t_{9a}	SKEN# Setup	4		5		5.2
t_{9b}	SKEN# Hold	3		4		5.2
t_{10a}	DATA, DP0-DP3 Setup	4		5		5.2
t_{10b}	DATA, DP0-DP3 Hold	3		4		5.2
t_{11a}	WP Setup	5		8		5.2
t_{11b}	WP Hold	3		4		5.2
t_{12a}	BOFF# Setup	5		8		5.2
t_{12b}	BOFF# Hold	3		4		5.2
t_{13a}	EADS# Setup	4		5		5.2
t_{13b}	EADS# Hold	3		4		5.2
t_{14a}	ADDR Setup(Invalidation)	4		5		5.2
t_{14b}	ADDR Hold (Invalidation)	3		4		5.2
t_{15a}	RESET, FLUSH# Setup	4		5		5.2
t_{15b}	RESET, FLUSH# Hold	3		4		5.2
t_{16}	BRDYO# Valid	3	13	3	16	5.3
t_{17}	CKEN# Valid	3	9	3	15	5.3

Symbol	Parameter	50MHz		33MHz		Fig
		Min(ns)	Max(ns)	Min(ns)	Max(ns)	
t_{18}	START# Valid	3	15	3	18	5.3
t_{19}	DATA Valid (Read Hit)	4	13	3	20	5.3
t_{20a}	CS# Setup	4		6		5.2
t_{20b}	CS# Hold	3		4		5.2
t_{22a}	BRDYO# enable		13		16	5.3
t_{22b}	BRDYO# disable		13		16	5.5

* All A.C. measurement are made with input switching from 0V to 3V. Input and output reference points are at 1.5V.

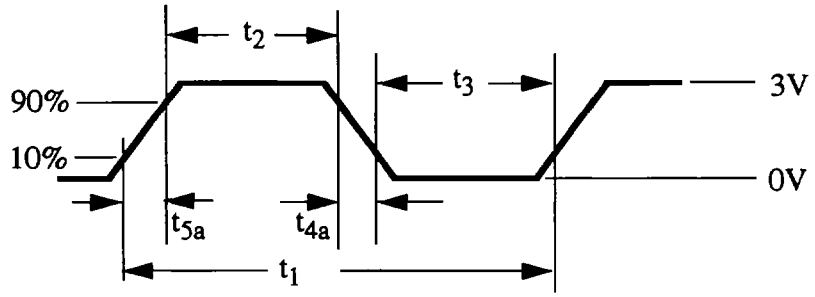
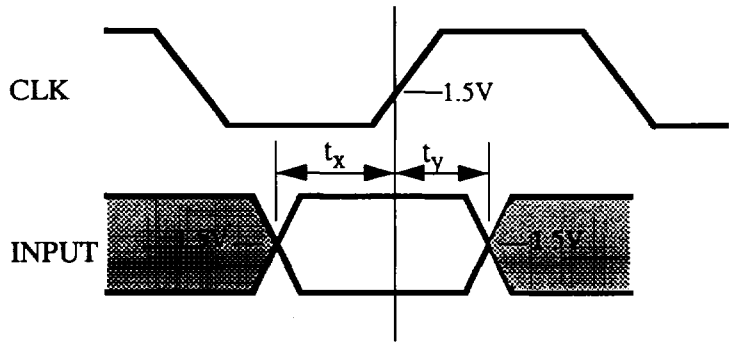


Figure 5.1. Clk Waveform



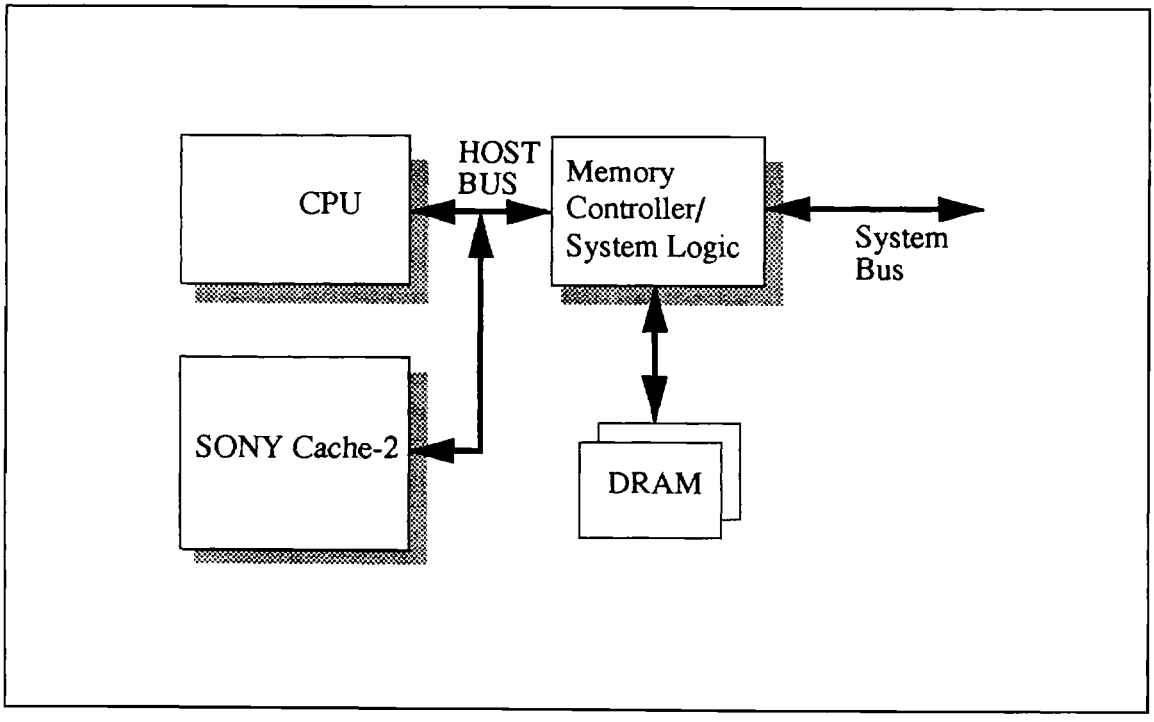
$t_x = t_{5a,6a,7a,8a,9a,10a,11a,12a,13a,14a,15a,20a}$
$t_y = t_{5b,6b,7b,8b,9b,10b,11b,12b,13b,14b,15b,20b}$

Figure 5.2. Setup and Hold Timings

Appendix

This appendix is organized as a design guide of using the SONY Cache-2 in typical system design. It first describes the special features such as Enhanced Cascade Mode and the usage of the mode pins. The next section describes typical design issues. Due to the simplicity of the look-aside architecture, the SONY Cache-2 can work with most PC systems without major design changes. However, some of the interface signals between the CPU and the system logic may be affected by the presence of the SONY Cache-2. This section describes how some these signals should be connected. The last section describes the restrictions in snoop cycle.

A.1 System Block Diagram



A.2 Mode Pins usage

The mode pins define the operation mode of the SONY Cache-2. These pins are static input pins tied to either logic-1 or logic-0 according to the desired operation mode. The mode pins are defined as the following:

MODE[4]:

This pin can be defined independent of the other mode pins. If this pin is tied to logic-0, the BRDYO# output will be tri-stated one cycle after each low-to-high transition. BRDYO# is enabled automatically when it drives low.

If MODE[4] is tied to logic-1. The BRDYO# and output is always enabled regardless of output state.

MODE[3:0]

MODE[3]	MODE[2]	MODE[1]	MODE[0]	Operation Mode
0	0	0	0	256K byte normal mode
1	0	0	0	Data ram test mode
1	0	0	1	Tag ram test mode
0	1	0	0	Enhanced cascade mode, 1024K, chip0
0	1	0	1	Enhanced cascade mode, 1024K, chip1
0	1	1	0	Enhanced cascade mode, 1024K, chip2
0	1	1	1	Enhanced cascade mode, 1024K, chip3
1	1	0	0	Enhanced cascade mode, 512K, chip0
1	1	0	1	Enhanced cascade mode, 512K, chip1
1	1	1	1	128K byte scale-down mode

The test modes are used for production testing and should not be used in the system. The 256K byte normal mode should be used in normal non-cascade design. If MODE[3:0] are all connected to 1, the SONY Cache-2 emulates a 128K-byte cache system. Internally half of the data ram and the tag ram are disabled so it would have the same performance as a 128K-byte cache. No address scrambling is required.

If two or four SONY Cache-2 chips are cascaded in a system to form a larger cache using enhanced cascade mode, all the SONY Cache-2 chips on the system should have MODE[3:0] tied to cascade mode setting. For example, if two SONY Cache-2 chips are cascaded in a system to form a 512K-byte cache, one of the SONY Cache-2 should be designated as chip0 and its MODE[3:0] pins tied to "1100". The other SONY Cache-2 should have MODE[3:0] tied to "1101".

A.3 Enhanced Cascade Mode

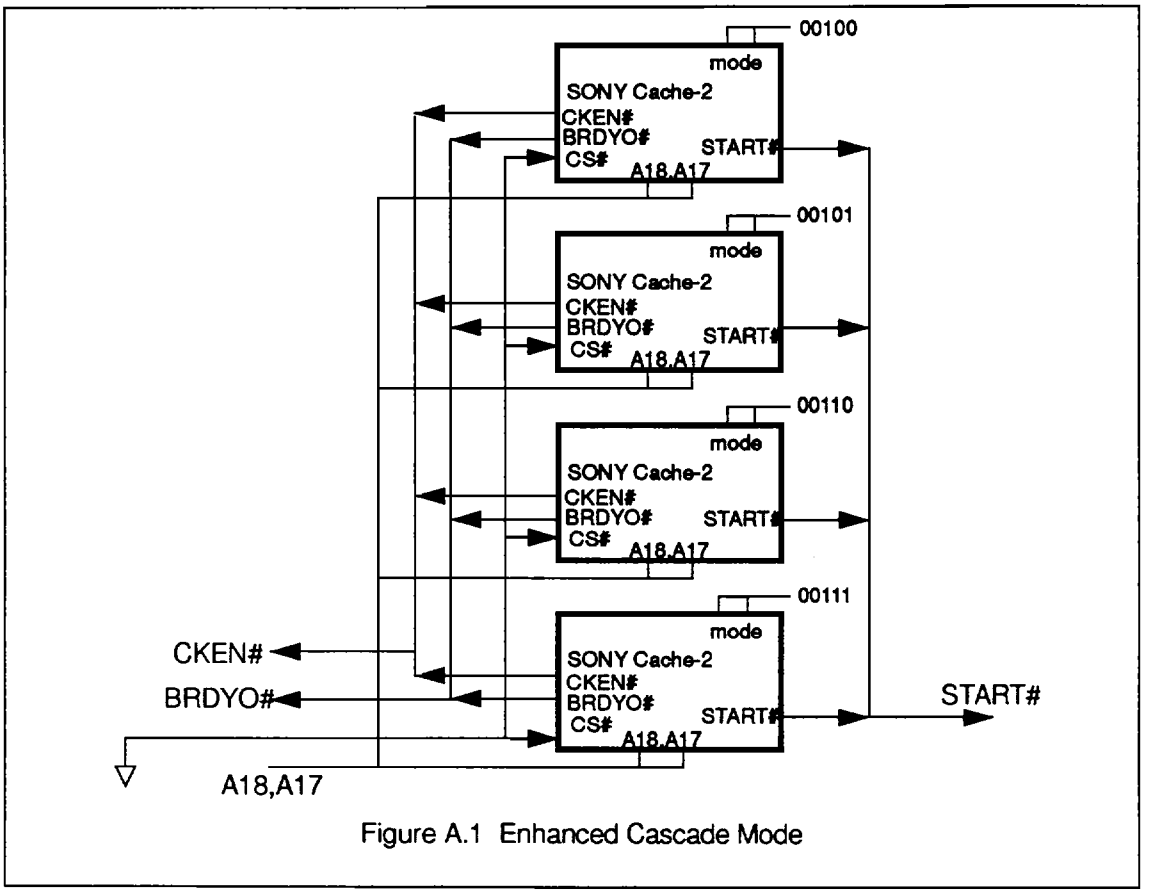


Figure A.1 Enhanced Cascade Mode

The Enhanced Cascade mode allows 2 or 4 SONY Cache-2 to work together to form a larger cache without using any external logic gates. When used in enhanced cascade mode, most of the inputs (except the MODE pins) and outputs (except the ACTIVE pin) are wired to all the SONY Cache-2 chips in parallel. For example, the BRDYO# pin from all the SONY Cache-2 chips on the system are wired together to form the BRDYO# signal.When the system is power-on or after reset, all the SONY Cache-2 chips on the system drive the outputs to the idle states. Since each output is driven to the same value by all the SONY Cache-2 chips, there is no signal conflict. Each memory access from the CPU would select one of the SONY Cache-2 as the active chip based on the value of ADDR18 and ADDR17. The un-selected chips tri-state their outputs so that the active chip has total control of the output and IO signals. The selected chip remains active until the next memory access which will start the select process again.

The ACTIVE output pin from each SONY Cache-2 should not be wired together. This pin is used for debugging only. When a SONY Cache-2 chip is selected, its asserts its ACTIVE output signal. If a chip is not selected, its ACTIVE pin is driven low.

The CS# input cannot be used during cascade mode. The CS# input to all the SONY Cache-2 chips must be connected to logic-0.

A.4 Interface Signal Generation

CKEN# and SKEN#

SKEN# is driven by the system logic and received by the SONY Cache-2 to determine cacheability of a line fill. CKEN# is driven by the SONY Cache-2 to determine cacheability of a CPU line fill when data is provided by the SONY Cache-2 (read hit). Data provided by the SONY Cache-2 is normally cacheable internal to the CPU with the exception for write protected lines. There are two methods to generate KEN# to the CPU through SKEN# and CKEN#.

The first method uses an external AND gate as shown in figure A.2. SKEN# is driven by the system logic according to data cacheability during read miss cycles. During read hit cycles, the SKEN# signal should be high so that the KEN# input of the CPU is controlled by the CKEN# output.

The alternative method is shown in figure 3.3 The method is applicable if the write-protect feature of the SONY Cache-2 is not used. In the absence of write-protected data, all read hit on SONY Cache-2 are cacheable in the CPU. The system logic should always drive KEN# low except during read miss or write cycles. KEN# should be driven according to the cacheability of the data during read miss cycles.

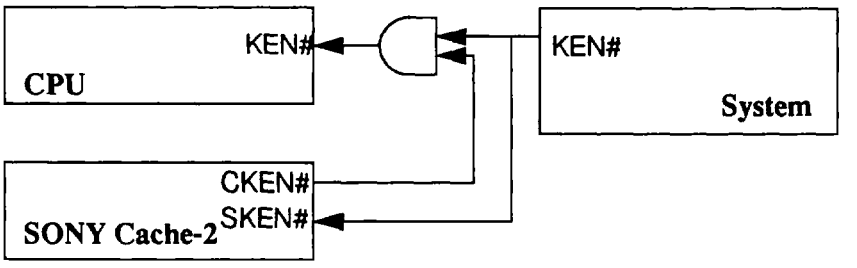


Figure A.2 Figure 3.2 KEN# generation

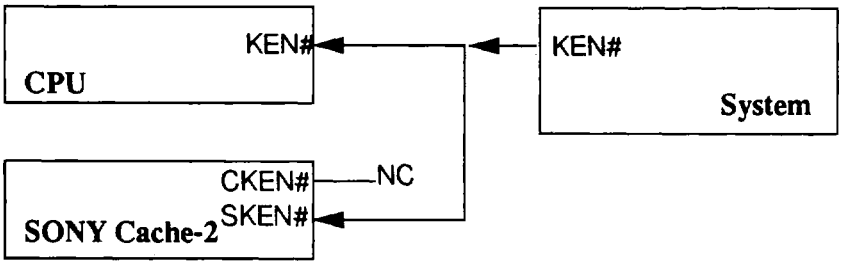


Figure A.3 Figure 3.3 KEN# generation, alternative method

BRDY#

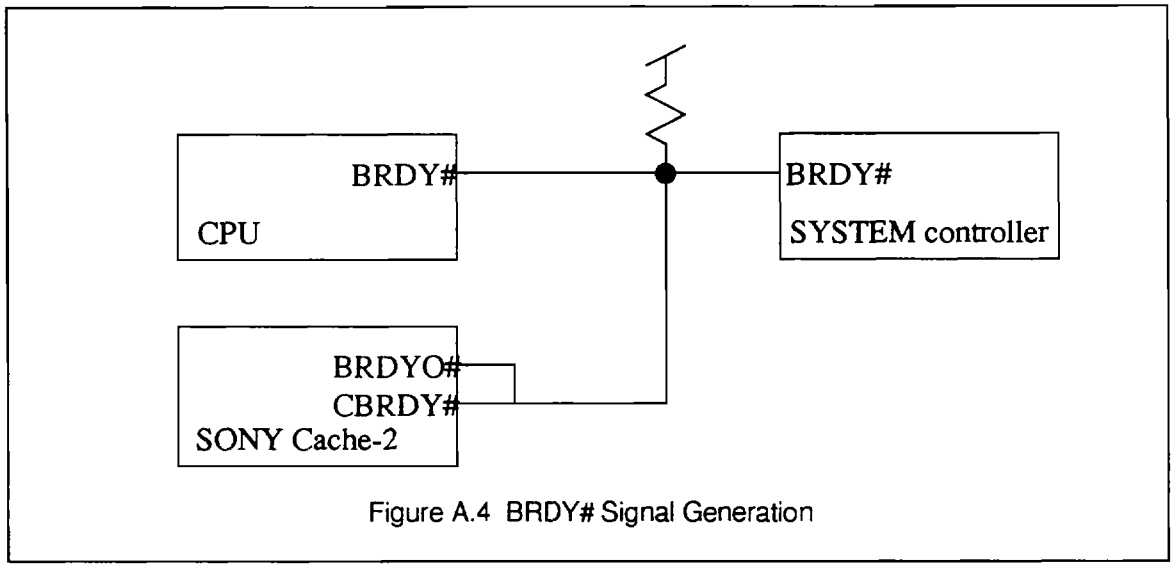


Figure A.4 BRDY# Signal Generation

If MODE[4] pin is tied to "0", BRDYO# from the SONY Cache-2 is normally tri-stated except during read hit cycle when the SONY Cache-2 drives this signal active (low). In the clock cycle after read hit is finished, the SONY Cache-2 drives BRDYO# high for one cycle and then it is tri-stated. A pull up resistor should be used to maintain BRDYO# at high level when it is tri-stated. The BRDY# signal from the system should be driven low only during read miss, write and I/O cycles. In all other cycles it should be driven high and then tri-stated. The CPU's BRDY# input can be generated by wire_AND the BRDYO# signal from the system and from the SONY Cache-2. CBRDY# and BRDYO# of the SONY Cache-2 can also be wired together to form an I/O pin.

START#

START# is used by the SONY Cache-2 to signal any cycle that requires services from the system memory. These cycles are read miss, write miss and write through cycles. The system memory controller can monitor this signal instead of the ADS# signal from the CPU to activate the system memory. The system logic should still monitor the ADS# signal from the CPU to detect I/O cycles.

CS#

The Chip Select signal should be tied low (active) during normal operation. If CS# is driven high, the SONY Cache-2 does not responds to any memory access or snoop cycle.

A.5 EADS# during line fill

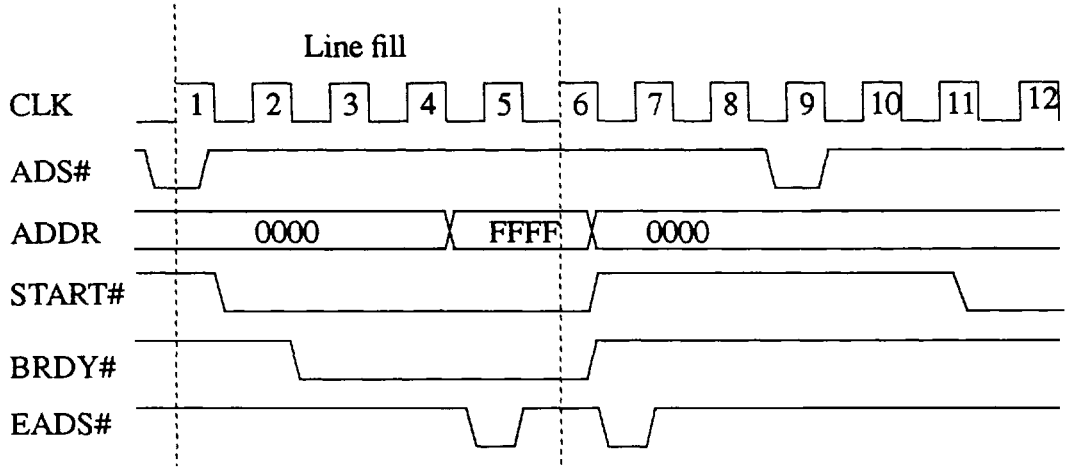


Figure A.5 EADS# causing problem during line fill

Invalidation by EADS# during line fill may cause problem if not handled properly. The above diagram is one example that invalidation will fail. The line fill completes at cycle 6 and validation of the cache line is supposed to take place at the same cycle. But since EADS# request has higher priority, the validation of the cache line at 0000 is delayed until cycle 9, after the completion of EADS# at cycle 5 and 7. The EADS# request at cycle 7, even tough it specifies address 0000, failed to invalidated the cache line at 0000 because it has taken place before the validation is performed. Furthermore, because internal tag ram is used for invalidation, the ADS# at cycle 9 is delayed until cycle 11 before the corresponding START# is generated.

The EADS# problem also exist in the following case:

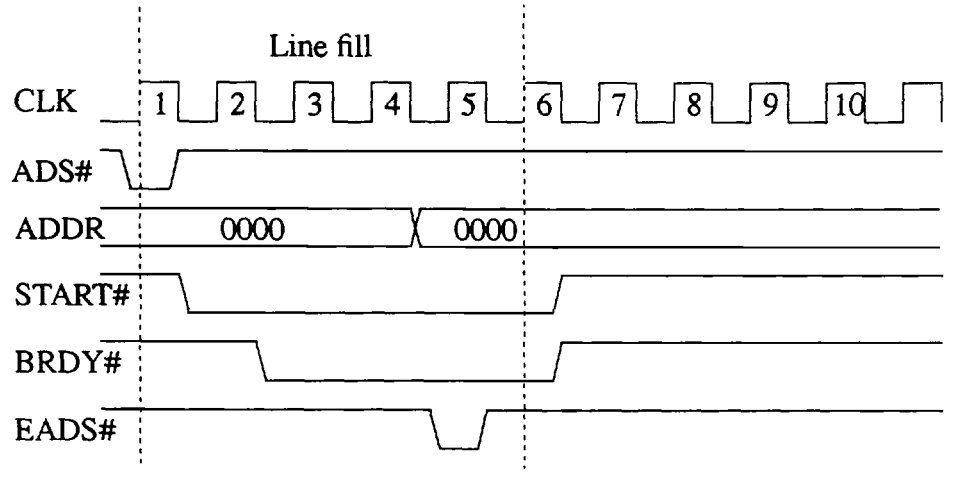


Figure A.6 EADS# causing problem during line fill

There are three different ways to avoid the problems shown in figure A.5 and A.6:

1 Do not allow EADS# from the cycle that line fill has started until the last doubleword has returned. This applies even if the line fill is of non-burst type.

2 If EADS# is activated during line fill, do not assert SKEN# before the last doubleword of the line fill. This way the cache line will not be validated.

3 Activate EADS# request only during back-off. The back-off cycle aborts all line fill in progress.