Power Products
1994

Siliconix
A Member of the TEMIC Group

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Power Products Data Book

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About Siliconix

Siliconix designs and manufactures semiconductor products that regulate and manage power supplies and enable the digitally-operated microprocessor to interface with real-world analog signals. The company's power transistors and integrated circuits are mainly used for power management and motion control in computers, hard disk drives, automobiles, and telecom systems. The company's analog switches, multiplexers, and low-power transistors are used to sense, switch, and route signals in video, multimedia, instrumentation, and test equipment in both the industrial and hi-rel environments.

Siliconix provides products and technologies that directly answer the market's demand for smaller, more efficient, and more cost-effective components. The company's LITE FOOT™ discrete power transistors are the industry's most compact solution for motion control in hard disk drives and for load management in portable computers. These miniaturized products can be mounted directly to the printed circuit board and are the first such products thin enough to fit inside any standard PCMCIA card. Siliconix introduced the first true surface-mount power transistor on the market with its LITTLE FOOT® product line. Besides computer and computer peripheral products, LITTLE FOOT has been designed into telecom systems, automotive air bag triggers, and numerous other applications where space-savings and efficiency are at a premium.

Siliconix power integrated circuits combine interface circuitry with power functions. A family of regulator and controller ICs designed for use with LITTLE FOOT discretes offers the optimal level of integration for dc-to-dc conversion in battery-operated equipment, including laptop and notebook computers. For data storage customers the company has produced highly integrated chips for voice coil and spindle motor control. New products include power ICs for computers equipped with dual battery packs or PCMCIA slots, and power ICs for bus control in automobiles.

Siliconix is a member of TEMIC, the microelectronics enterprise of AEG within the Daimler-Benz Group. The company now shares the technologies and applications expertise of its sister companies and takes advantage of a combined international sales network.

TEMIC

Siliconix

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General Information

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About This Data Book

The products detailed in this data book include both discrete and integrated devices for power control, conversion, and switching in computers, automobiles, data storage, communications, industrial, and hi-rel systems.

Siliconix' power MOSFET offerings include its LITTLE FOOT® and LITE FOOT™ families of small-outline devices, plus a distinguished selection of low-on-resistance products in other packages rated for both the industrial and military temperature ranges. Devices available in TO-220 and TO-263 packages include the company's 60-V TrenchFETs, the first power MOSFETs on the market to offer a *maximum* on-resistance as low as 8 mΩ at 10-V gate drive.

Siliconix power ICs for power management and motor control serve applications ranging from load switching in battery-operated portable computers to dc-to-dc conversion in communications systems. Bus interface ICs include devices designed for such protocols as ABUS and ISO 9141.

For More Information

To request additional literature, please call your local TEMIC Sales Representative. Office listings with phone and fax numbers are available in Section 8. In North America, you may also request information directly from Siliconix at 1-800-554-5565.

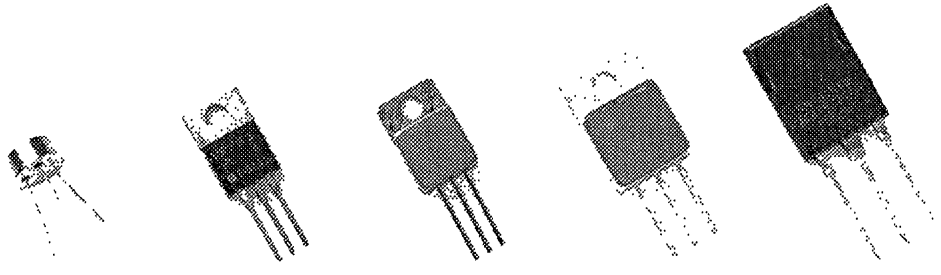
For Technical Support

In addition to the individual data sheets, Siliconix offers a number of Application Notes to help you with your designs. Please refer to the Application Note listing in Section 7, and use our FaxBack system at 1-408-970-5600 to obtain copies.

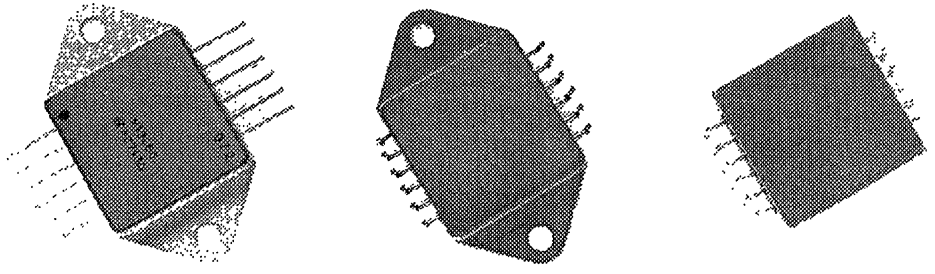
TSSOP SO-8 SO-14 SO-16 SO-16WB SO-24WB

4-Pin DIP 8-Pin DIP 14-Pin DIP 16-Pin DIP

SQFP-48 LCC-20 PLCC-20 TO-252 (DPAK) TO-251 TO-263 (D^2PAK)



TO-205AF (TO-39) TO-220 TO-257 TO-254 TO-247



MOD (Straight Lead) MOD (Bent-Up Lead) MOD (Bent-Down Lead)

N-Channel MOSFETs

Maximum Ratings					Configuration	Packages			
	$r_{DS(on)}$ (Ω)								
V_{DS} (V)	V_{GS} = 10 V	V_{GS} = 4.5 V	V_{GS} = 2.7 V	I_D (A)		8-Pin SOIC	Page	16-Pin SOIC	Page
20		0.05	0.08	±5	Dual	Si9925DY	1-37		
	0.1	0.2		±3.5	Dual	Si9956DY	1-113		
30	0.03	0.05		±7	Single	Si9410DY	1-13		
	0.05	0.08		±5	Dual	Si9936DY	1-51		
50	0.05	0.07		±5.3	Dual			Si9940DY	1-61
	0.13	0.2		±3	Dual	Si9955DY	1-109		
	0.3			±2	Dual	Si9959DY	1-123		
60	0.1	0.2		±3.3	Dual	Si9945DY	1-81		
200	1			±1	Single	Si9420DY	1-17		
240	6	8		±0.4	Dual	Si9944DY	1-77		

P-Channel MOSFETs

Maximum Ratings						Configuration	Packages	
	$r_{DS(on)}$ (Ω)							
V_{DS} (V)	V_{GS} = −10 V	V_{GS} = −6 V	V_{GS} = −4.5 V	V_{GS} = −2.7 V	I_D (A)		8-Pin SOIC	Page
−12			0.04		±6.4	Single	Si9434DY	1-29
−20			0.065	0.1	±5.4	Single	Si9433DY	1-25
			0.11	0.19	±3.4	Dual	Si9933DY	1-47
	0.05	0.065	0.09		±5.8	Single	Si9430DY	1-21
	0.1		0.16		±4.3	Single	Si9405DY	1-5
			0.19		±3.5	Dual	Si9947DY	1-85
	0.25		0.4		±2.3	Dual	Si9953DY	1-105
					±2.5	Single	Si9400DY	1-1
−30	0.055	0.07	0.105		±5.1	Single	Si9435DY	1-33
−60	0.15		0.24		±3	Single	Si9407DY	1-9
	0.28		0.5		±2	Dual	Si9948DY	1-89

Complementary MOSFETs

Maximum Ratings						Configuration	Packages			
	$r_{DS(on)}$ (Ω)									
V_{DS} (V)	V_{GS} = ±10 V	V_{GS} = ±6 V	V_{GS} = ±4.5 V	V_{GS} = ±2.7 V	I_D (A)		8-Pin SOIC	Page	16-Pin SOIC	Page
20			0.05	0.08	±5	N-Channel	Si9928DY	1-41		
−20			0.13	0.19	±3.2	P-Channel				
20	0.1	0.12	0.15		±3.5	N-Channel	Si9958DY	1-117		
−20			0.19		±3.5	P-Channel				
20	0.125		0.25		±3	N-Channel	Si9943DY	1-71		
−20	0.16		0.3		±2.8	P-Channel				
20	0.125		0.25		±3	N-Channel	Si9942DY	1-65		
−20	0.2		0.35		±2.5	P-Channel				
25	0.1		0.15		±3.5	N-Channel	Si9952DY	1-99		
−25	0.25		0.4		±2.3	P-Channel				
30	0.05	0.07	0.08		±3.5	N-Channel	Si9939DY	1-55		
−30	0.1	0.12	0.16		±3.5	P-Channel				
50	0.3		1		±2	N-/P-Channel Half-Bridge			Si9950DY	1-93

N-Channel MOSFETs

Maximum Ratings				Configuration	Packages	
	$r_{DS(on)}$ (Ω)					
V_{DS} (V)	V_{GS} = 10 V	V_{GS} = 4.5 V	I_D (A)		8-Pin TSSOP	Page
20	0.100	0.200	±2.5	Dual	Si6956DQ	2-23
30	0.050	0.080	±4.2	Single	Si6436DQ	2-3

P-Channel MOSFETs

Maximum Ratings					Configuration	Packages	
	$r_{DS(on)}$ (Ω)						
V_{DS} (V)	V_{GS} = −10 V	V_{GS} = −4.5 V	V_{GS} = −2.7 V	I_D (A)		8-Pin TSSOP	Page
−12		0.075	0.110	±3.5	Single	Si6433DQ	2-1
−20	0.100	0.190		±3.0	Single	Si6447DQ	2-5
	0.200	0.350		±1.7	Dual	Si6953DQ	2-15

Complementary MOSFETs

Maximum Ratings				Configuration	Packages	
	$r_{DS(on)}$ (Ω)					
V_{DS} (V)	V_{GS} = ±10 V	V_{GS} = ±4.5 V	I_D (A)		8-Pin TSSOP	Page
20	0.100	0.200	±2.5	N-Channel	Si6542DQ	2-7
−20	0.350	0.200	±1.7	P-Channel		

Power Conversion, PCMCIA Interface and Battery Management

Function	Recommended Operating Range		Part Number	Packages	Page
	Peak Output Current (A)	Voltage Range (V)			
3-W High-Voltage Switchmode Regulator	2.5	10 – 70	Si9100	14-Pin Plastic DIP 20-Pin PLCC	3-1
3-W High-Voltage Switchmode Regulator	2	10 – 120	Si9102	14-Pin Plastic DIP 20-Pin PLCC	3-9
High-Voltage Switchmode Regulator	2	10 – 120	Si9104	14-Pin Plastic DIP 16-Pin Widebody SOIC 20-Pin PLCC	3-16
1-W High-Voltage Switchmode Regulator	2	10 – 120	Si9105	14-Pin Plastic DIP 16-Pin Widebody SOIC 20-Pin PLCC	3-24
High-Voltage Switchmode Controller	±0.25[a]	10 – 120	Si9110	14-Pin Plastic DIP 14-Pin SOIC 14-Pin CerDIP	3-31
High-Voltage Switchmode Controller	±0.25[a]	10 – 120	Si9111	14-Pin Plastic DIP 14-Pin SOIC 14-Pin CerDIP	3-31
High-Voltage Switchmode Controller	±0.25[a]	9 – 80	Si9112	14-Pin Plastic DIP 14-Pin SOIC	3-38
High-Frequency Switchmode Controller	±0.4[a]	15 – 200	Si9114	14-Pin Plastic DIP 14-Pin SOIC	3-44
Universal Input Switchmode Controller	±0.25[a]	10 – 450	Si9120	16-Pin Plastic DIP 16-Pin SOIC	3-49
Low-Voltage Switchmode Controller	±0.2[a]	2.7 – 7	Si9145	16-Pin SOIC 16-Pin TSSOP	3-55
Synchronous Buck Converter Controller	±0.25[a]	6.0 – 16.5	Si9150	14-Pin SOIC	3-62
PCMCIA Interface Switch	1.0[b]	N. A.	Si9710CY	16-Pin SOIC	3-68
PCMCIA Interface Switch	1.0[b]	N. A.	Si9711CY	16-Pin SOIC	3-72
Battery Disconnect Switch	3.5	6 – 18	Si9717CY	16-Pin SOIC	3-76
Battery Disconnect Switch	3.5	6 – 18	Si9718CY	16-Pin SOIC	3-79

Notes
a. Driver output
b. Multiple outputs

Motor Control and MOSFET Drivers

Function	Recommended Operating Range		Part Number	Packages	Page
	Peak Output Current (A)	Voltage Range (V)			
Quad High-Current Power Driver	1.5[a]	12 – 15	D469A	14-Pin Plastic DIP 14-Pin Sidebraze	4-1
Adaptive Power MOSFET Driver	±1[a]	10.8 – 16.5	Si9910	8-Pin Plastic DIP 8-Pin SOIC	4-5
12-V Voice Coil Motor Driver	1.8	16	Si9961	24-Pin SOIC	4-10
N-Channel Half-Bridge Driver	±0.5[a]	20 – 40	Si9976	14-Pin SOIC	4-17
Configurable H-Bridge Driver	±0.5[a]	20 – 40	Si9978	24-Pin SOIC	4-22
3-Phase Brushless DC Motor Controller	±0.5[a]	20 – 40	Si9979	48-Pin SQFP	4-28

Notes
a. Driver output

Bus Interface

Function	Recommended Operating Range		Part Number	Packages	Page
	Peak Output Current (A)	Voltage Range (V)			
Single-Ended Bus Driver	N. A.	5 V, 8 – 35 V	Si9241	8-Pin SOIC	5-1
Single-Ended Bus Driver	N. A.	5 V, 8 – 35 V	Si9243	8-Pin SOIC	5-5

N-Channel

Maximum Ratings				Packages											
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	P_D (W)	TO-220AB	Page	D^2PAK TO-263	Page	DPAK TO-252	Page	TO-251	Page	TO-247AD	Page	4-Pin DIP TO-250	Page
30	0.03	30	50					SMD30N03-30L	6-93	SMU30N03-30L	6-93				
	0.01	60	105	SMP60N03-10L	6-121										
50	0.04	30	75	BUZ11	6-1										
	0.045	25	50					SMD25N05-45L	6-89	SMU25N05-45L	6-89				
	0.045	25	70	SMP25N05-45L	6-101										
	0.1	2.4	1											IRFD020	6-33
	0.1	14	40	BUZ71	6-5										
	0.1	15	40					SMD15N05	6-83	SMU15N05	6-83				
	0.12	13	40	BUZ71A	6-5										
60	0.008	60	150	SUP60N06-08	6-157	SUB60N06-08	6-153								
	0.014	60	100	SUP60N06-14	6-161	SUB60N06-14	6-161								
	0.014	60	150	SMP60N06-14	6-125										
	0.014	70	150									SMW70N06-14	6-149		
	0.018	48	83	SUP50N06-18	6-155	SUB50N06-18	6-155								
	0.018	60	105									SMW60N06-18	6-141		
	0.018	60	125	SMP60N06-18	6-129										
	0.025	46	105	SMP50N06-25	6-117										
	0.1	15	40					SMD15N06	6-87						
	0.4	1.1	1											IRFD123	6-41
100	0.025	60	180									SMW60N10	6-145		
	0.04	40	125	SMP40N10	6-109										
	0.04	45	150									SMW45N10	6-137		
	0.06	30	100	SMP30N10	6-105										
	0.085	27	125	IRF540	6-25										
	0.18	14	75	IRF530	6-21										
	0.3	1.3	1											IRFD120	6-41
	0.3	8	40	IRF520	6-17										
	0.6	1	1											IRFD110	6-37
	0 6	4	20	IRF510	6-13										

P-Channel

Maximum Ratings				Packages											
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	P_D (W)	TO-220AB	Page	D^2PAK TO-263	Page	DPAK TO-252	Page	TO-251	Page	TO-247AD	Page	4-Pin DIP TO-250	Page
−50	0.4	−7	40	BUZ171	6-9										
	0.28	−1.6	1											IRFD9020	6-45
	0.28	−10	40					SMD10P05	6-73	SMU10P05	6-73				
−60	0.02	−60	150	SUP60P06-20	6-163	SUB60P06-20	6-163								
	0.045	−40	125	SMP40P06	6-113										
	0.28	−10	40					SMD10P06L	6-79						
	0.28	−10	42					SMD10P06	6-77						
	0.8	−0.8	1											IRFD9123	6-49
−100	0.2	−20	125	SMP20P10	6-97										
	0.2	−20	150									SMW20P10	6-133		
	0.3	−12	75	IRF9530	6-29										
	0.6	−1	1											IRFD9120	6-49

N-Channel Hermetic Packages and Industry-Standard Military MOSFETs

Maximum Ratings				Packages								Equivalent Commercial Part	QPL Product in Accordance With 19500/
				Hermetic Power Module				TO-254AA	Page	TO-257AB	Page		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	P_D (W)	Lead Bent Down	Page	Lead Bent Up	Page						
100	0.065	30	150					2N7075	6-173			IRFM150	
	0 075	20	60							2N7085	6-201	2N7085	
	0.08	21	150	MOD100B	6-53	MOD100C	6-53					MOD100B/C	
	0 081	34	150					2N7224	6-221			IRFM150	592
	0.15	13	50							2N7081	6-197	2N7081	
200	0.1	28	150					2N7076	6-177			IRFM250	
	0.105	27.4	150					2N7225	6-223			IRFM250	592
	0.11	21	150	MOD200B	6-57	MOD200C	6-57					MOD200B/C	
	0.16	14	60							2N7086	6-206	2N7086	
400	0.3	15	150					2N7077	6-181			IRFM350	
	0.35	15	150	MOD400B	6-61	MOD400C	6-61					MOD400B/C	
	0.415	14	150					2N7227	6-225			IRFM350	592
500	0.4	13	150					2N7078	6-185			IRFM450	
	0.43	13	150	MOD500B	6-65	MOD500C	6-65					MOD500B/C	
	0.515	12	150					2N7228	6-227			IRFM450	592

20	0.1	0.5	3	Quad	LCC-20	Si8956AZ/883	6-69		

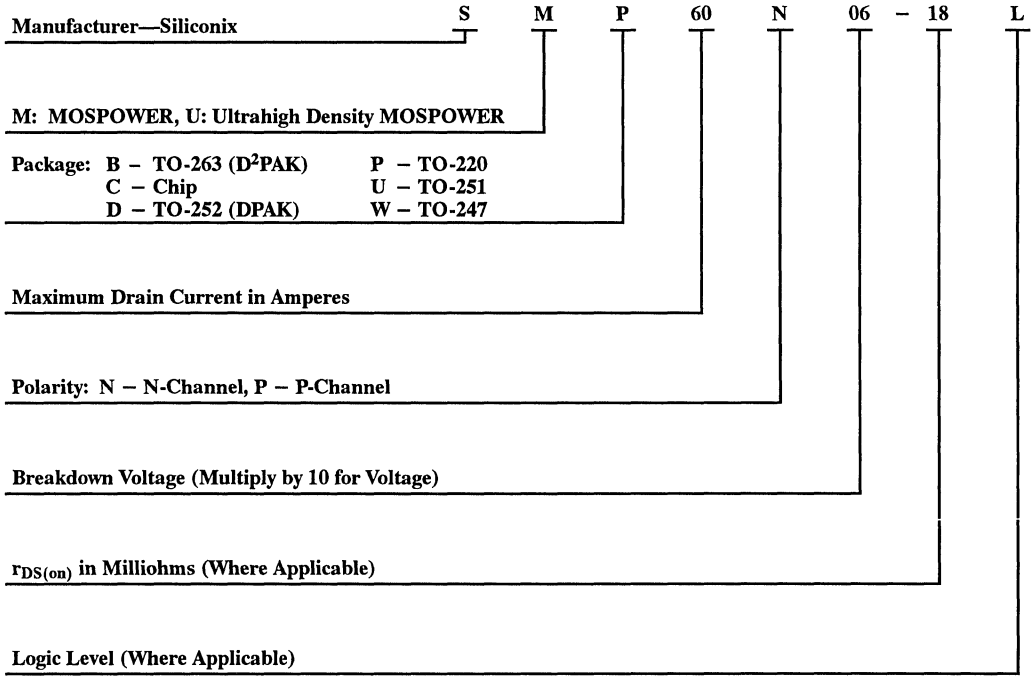
P-Channel Hermetic Packages and Industry-Standard Military MOSFETs

Maximum Ratings				Packages						Equivalent Commercial Part	QPL Product in Accordance With 19500/
				TO-205AF	Page	TO-254AA	Page	TO-257AB	Page		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)	P_D (W)								
−100	0.2	−14	70					2N7091	6-217	2N7091	
	0.21	−17	100			2N7079	6-189			2N7079	
	0.3	−6.5	25	2N6849	6-165					IRFF9130	564
	0.3	−10	60					2N7089	6-209	2N7089	
−200	0.5	−9.5	100			2N7080	6-193			2N7080	
	0.8	−5.7	60					2N7090	6-213	2N7090	
	0.8	−4	25	2N6851	6-169					IRFF9230	564

Ordering Information

Power Products Nomenclature

For Power MOSFETs



LITTLE FOOT®

1

About LITTLE FOOT

Siliconix' LITTLE FOOT® is the industry's first and largest family of small-outline, surface-mount power MOSFETs for motion control and load management in space-sensitive applications from the portable computer to the automobile. LITTLE FOOT products come in single and dual versions and can be mounted directly to printed circuit boards, where they are fully compatible with other surface-mounted components. First designed for computers and computer peripheral products, LITTLE FOOT is now widely used in telecom systems, automotive air bag triggers, and numerous other applications where space-savings and efficiency are at a premium.

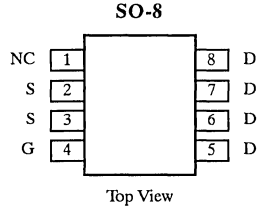
Siliconix

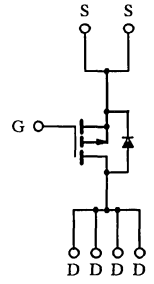
Si9400DY

P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.25 @ V_{GS} = −10 V	±2.5
	0.40 @ V_{GS} = −4.5 V	±2.0





P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.5	A
	T_A = 70°C		±2.0	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	−2.0	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

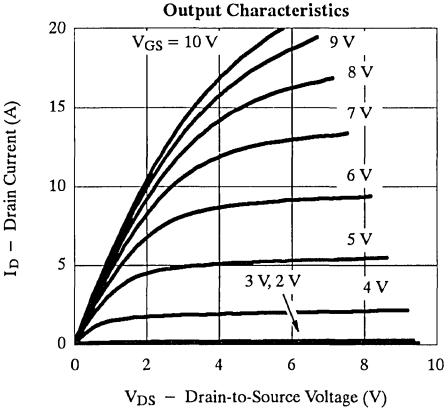
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

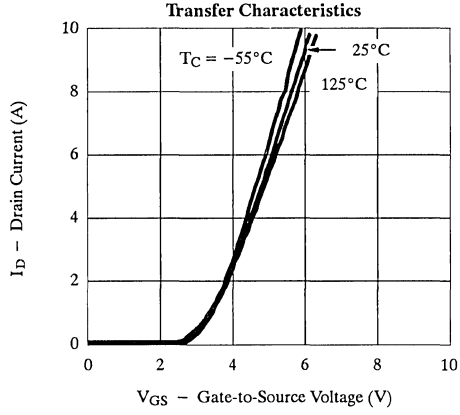
Specifications (T_J = 25°C Unless Otherwise Noted)

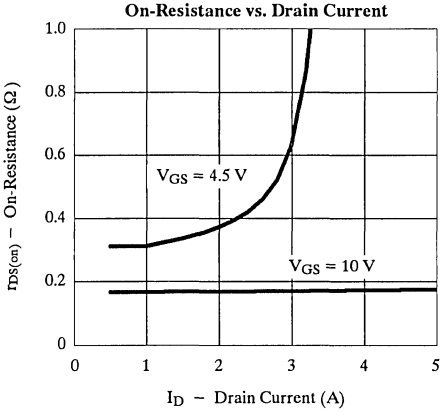
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −10 V	−10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 1 A		0.16	0.25	Ω
		V_{GS} = −4.5 V, I_D = 0.5 A		0.30	0.40	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −2.5 A		2.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = −1.25 A, V_{GS} = 0 V		−0.9	−1.6	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −2.0 A		5.4	25	nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		10	40	ns
Rise Time	t_r			10	40	
Turn-Off Delay Time	$t_{d(off)}$			38	90	
Fall Time	t_f			27	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs		69	100	

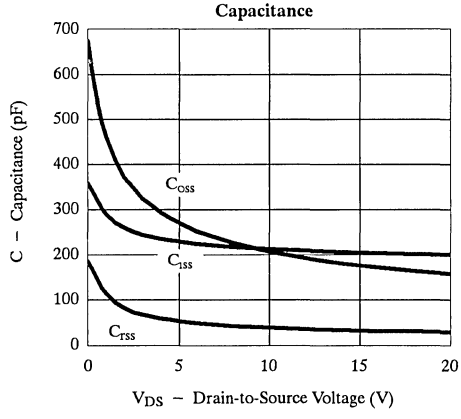
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

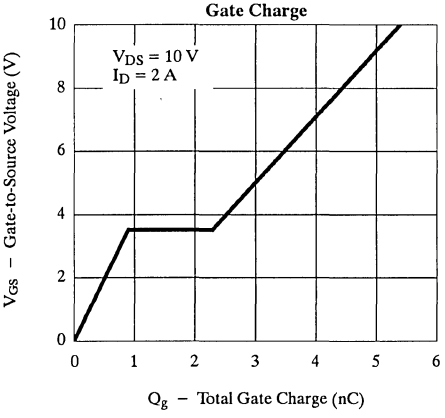
Typical Characteristics (25°C Unless Otherwise Noted)

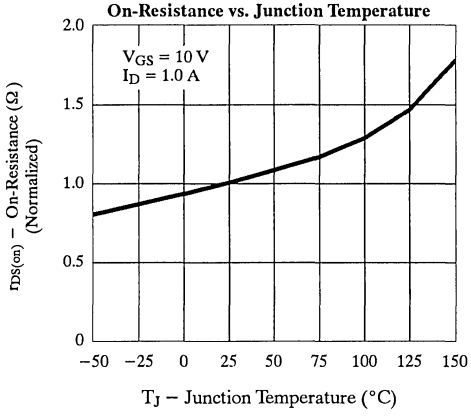




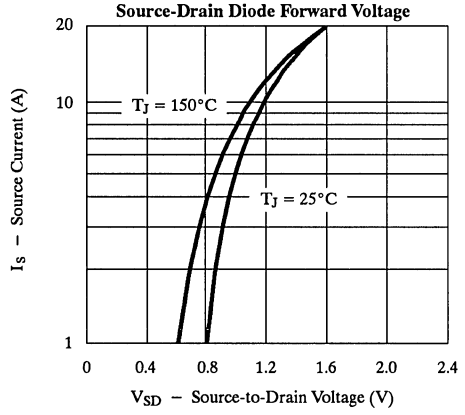


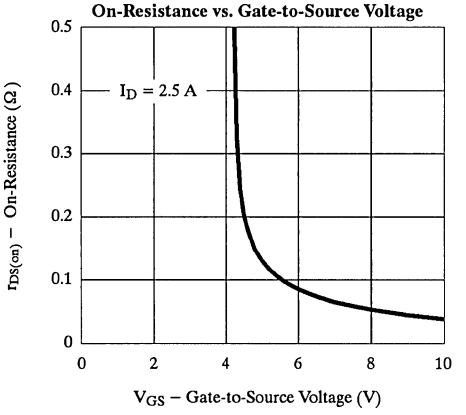


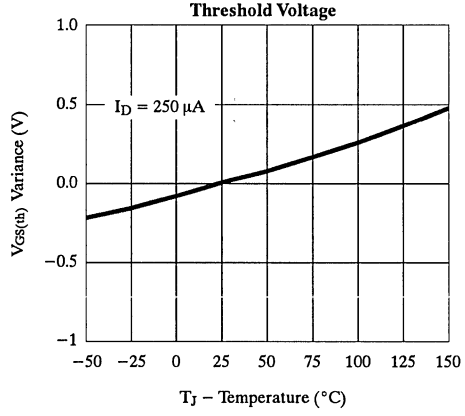


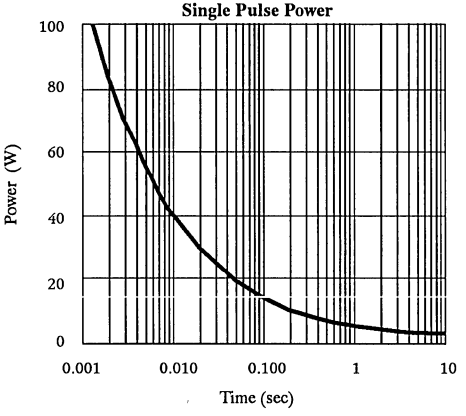


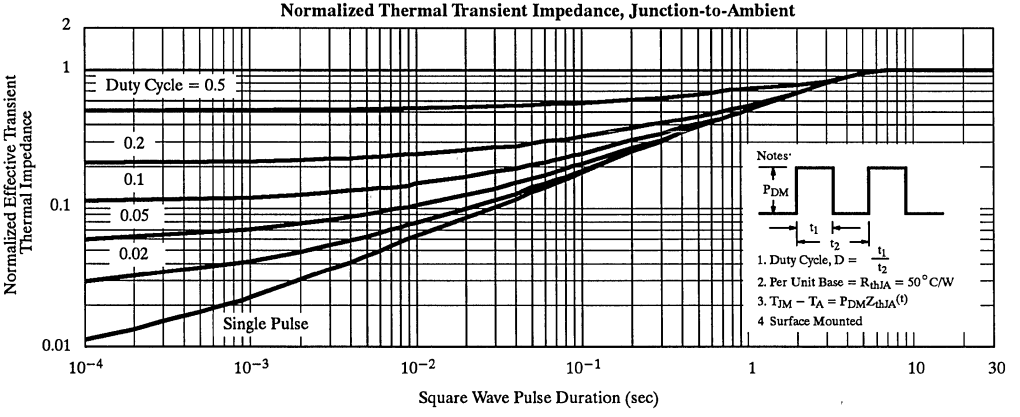
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

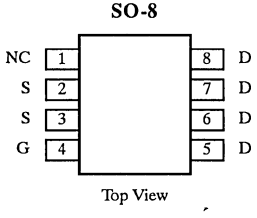
Si9405DY

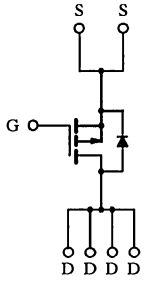
P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.10 @ V_{GS} = −10 V	±4.3
	0.16 @ V_{GS} = −4.5 V	±3.4

Recommended upgrade: Si9430DY
Lower profile/smaller size—see LITE FOOT™ equivalent: Si6447DQ





P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±4.3	A
	T_A = 70°C		±3.3	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	−2.2	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

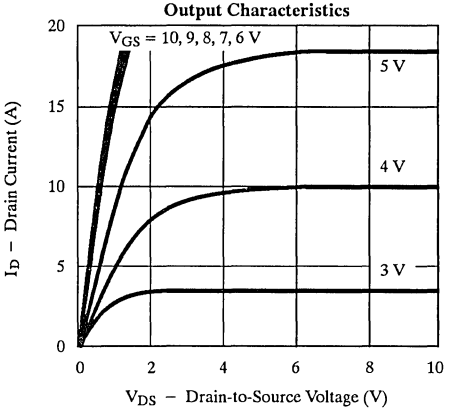
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−0.5			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −10 V	−20			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 2.0 A		0.07	0.10	Ω
		V_{GS} = −4.5 V, I_D = 2.0 A		0.11	0.16	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −4.3 A		6		S
Diode Forward Voltage[b]	V_{SD}	I_S = −1.25 A, V_{GS} = 0 V		−0.8	−1.6	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −2.0 A		29	40	nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			14		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		15	30	ns
Rise Time	t_r			30	80	
Turn-Off Delay Time	$t_{d(off)}$			142	200	
Fall Time	t_f			130	200	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		70		

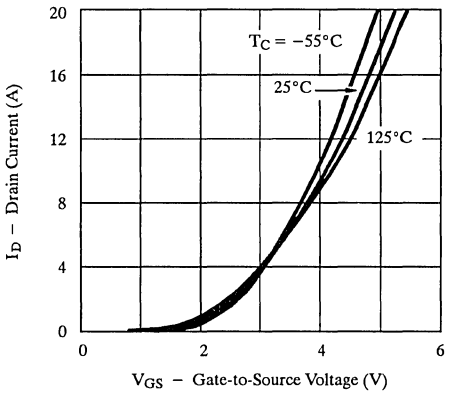
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

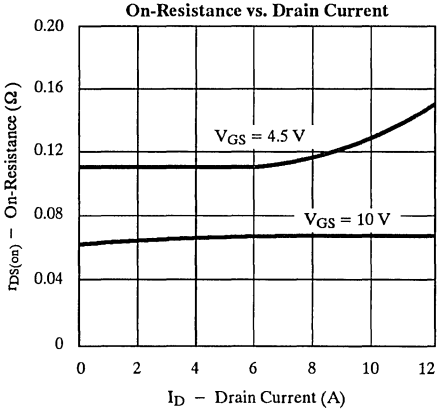
Output Characteristics



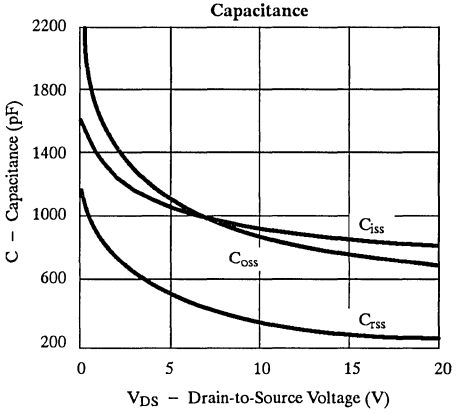
Transfer Characteristics



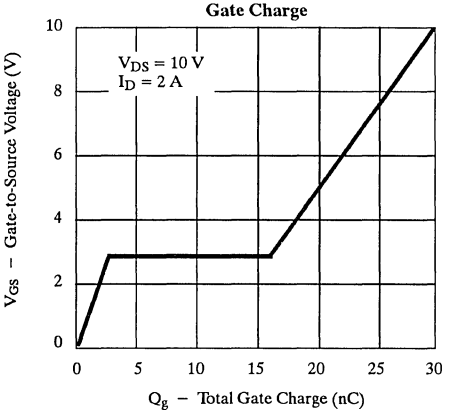
On-Resistance vs. Drain Current



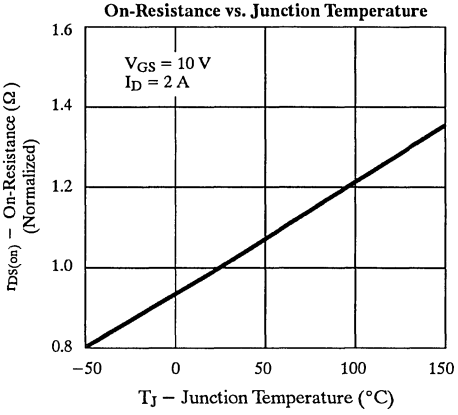
Capacitance



Gate Charge

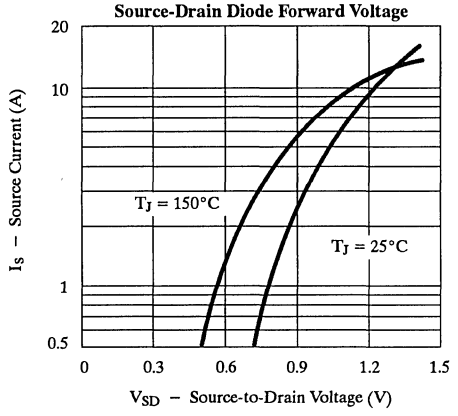


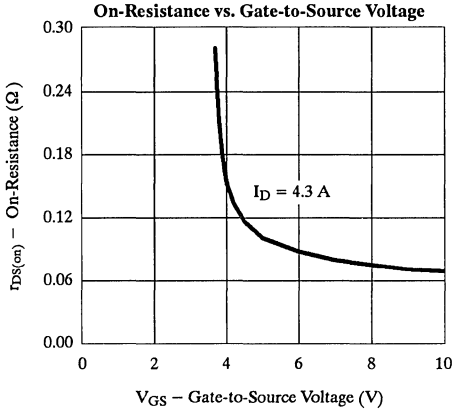
On-Resistance vs. Junction Temperature

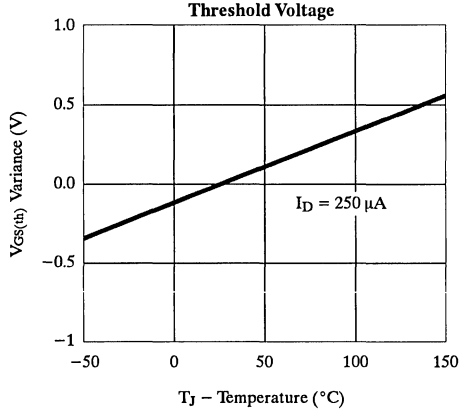


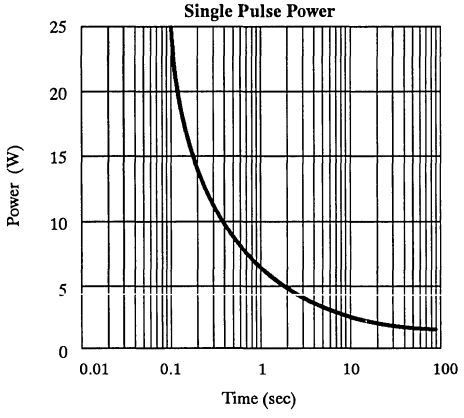
1 LITTLE FOOT

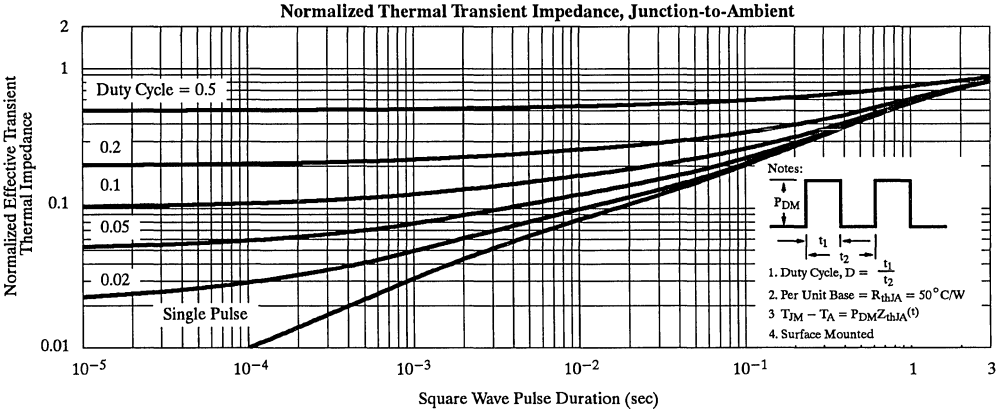
Typical Characteristics (25°C Unless Otherwise Noted)









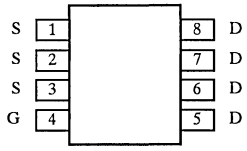


P-Channel Enhancement-Mode MOSFET

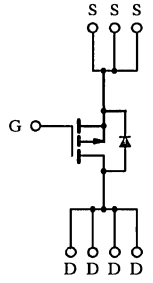
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−60	0.150 @ V_{GS} = −10 V	±3.0
	0.240 @ V_{GS} = −4.5 V	±2.4

SO-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.0	A
	T_A = 70°C		±2.4	
Pulsed Drain Current		I_{DM}	±12	
Continuous Source Current (Diode Conduction)		I_S	−2.5	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

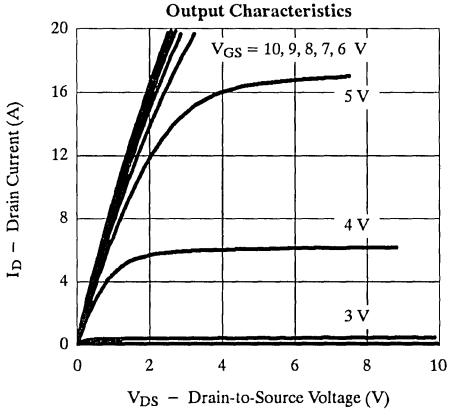
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

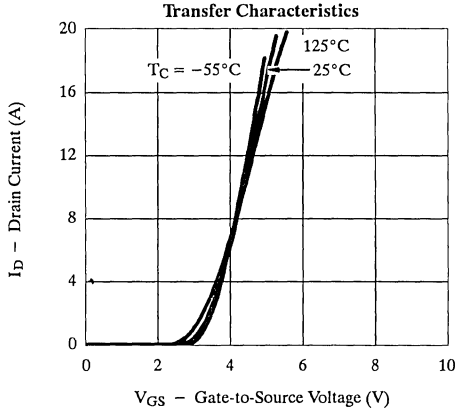
Specifications (T_J = 25°C Unless Otherwise Noted)

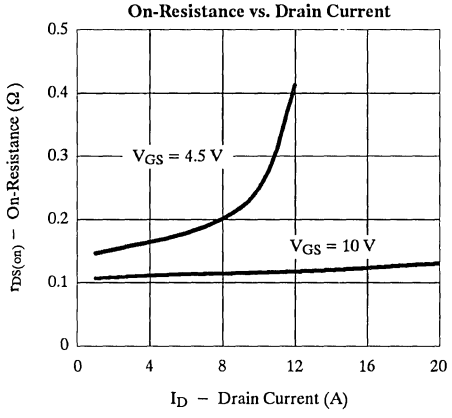
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	−1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V$, $V_{GS} = \pm 20\ V$			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48\ V$, $V_{GS} = 0\ V$			−1	µA
		$V_{DS} = -48\ V$, $V_{GS} = 0\ V$, $T_J = 55°C$			−10	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \le -5\ V$, $V_{GS} = -10\ V$	−12			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = -10\ V$, $I_D = 3.0\ A$		0.11	0.150	Ω
		$V_{GS} = -4.5\ V$, $I_D = 1.6\ A$		0.15	0.24	
Forward Transconductance[b]	g_{fs}	$V_{DS} = -15\ V$, $I_D = -3.0\ A$		5.5		S
Diode Forward Voltage[b]	V_{SD}	$I_S = -2.5\ A$, $V_{GS} = 0\ V$		−0.9	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = -30\ V$, $V_{GS} = -10\ V$, $I_D = -3.0\ A$		24.6	50	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			7.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -25\ V$, $R_L = 25\ \Omega$ $I_D \cong -1\ A$, $V_{GEN} = -10\ V$, $R_G = 6\ \Omega$		11	30	ns
Rise Time	t_r			13	40	
Turn-Off Delay Time	$t_{d(off)}$			55	100	
Fall Time	t_f			20	45	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -3.0\ A$, di/dt = 100 A/µs		80	120	

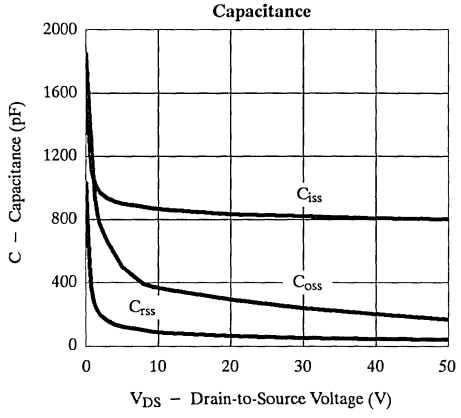
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

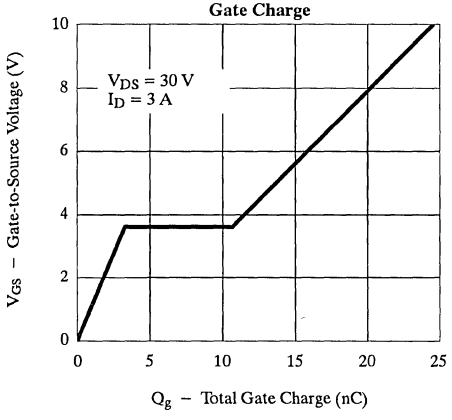
Typical Characteristics (25°C Unless Otherwise Noted)

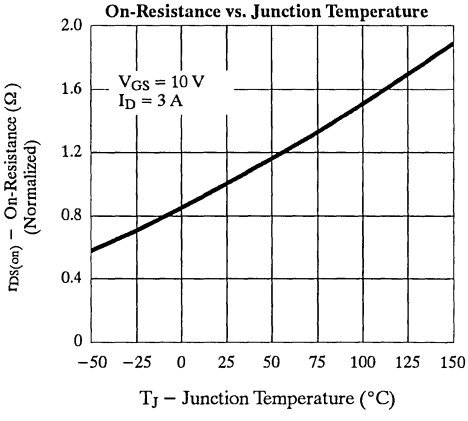




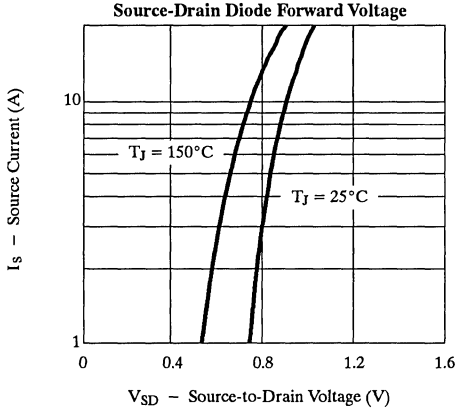


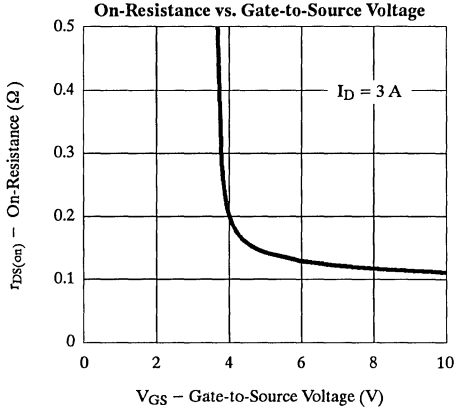


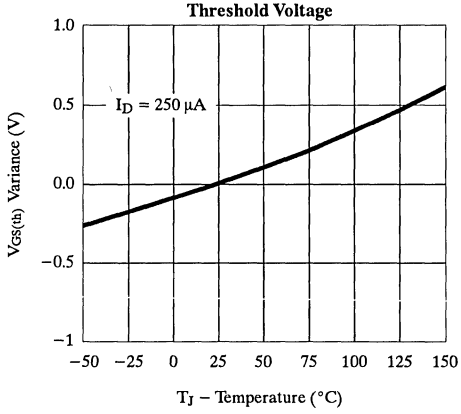


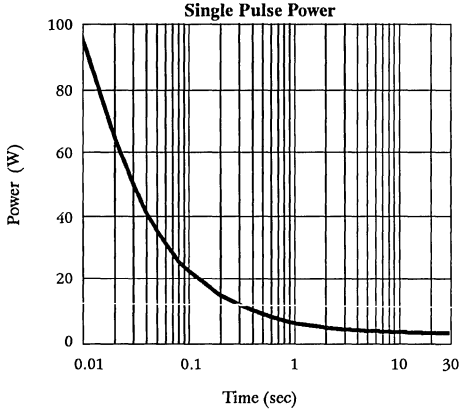


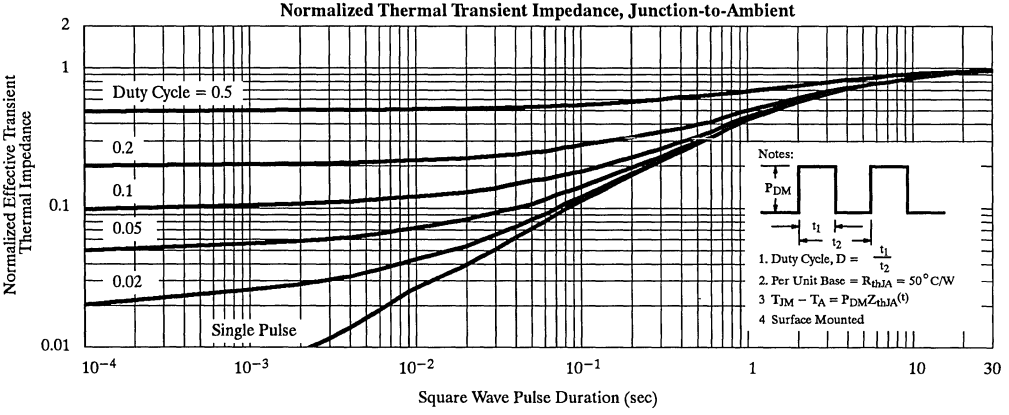
Typical Characteristics (25°C Unless Otherwise Noted)











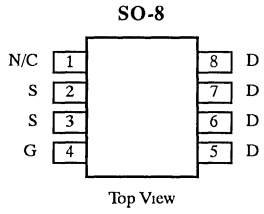
Siliconix

Si9410DY

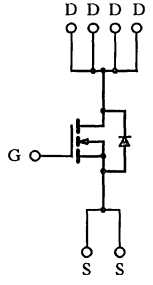
N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.030 @ V_{GS} = 10 V	±7.0
	0.040 @ V_{GS} = 5 V	±6.0
	0.050 @ V_{GS} = 4.5 V	±5.4



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±7.0	A
	T_A = 70°C		±5.8	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	2.8	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

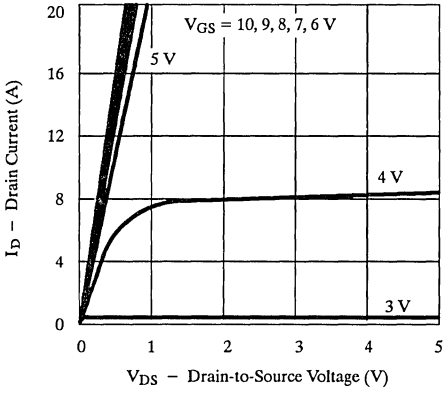
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D =7.0 A		0.026	0.030	Ω
		V_{GS} = 5 V, I_D = 4.0 A		0.034	0.040	
		V_{GS} = 4.5 V, I_D = 3.5 A		0.042	0.050	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 7.0 A		14		S
Diode Forward Voltage[b]	V_{SD}	I_S = 2 A, V_{GS} = 0 V		0.75	1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 2 A		30	50	nC
Gate-Source Charge	Q_{gs}			3.4		
Gate-Drain Charge	Q_{gd}			10.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		13	30	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			95	150	
Fall Time	t_f			80	140	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs		100		

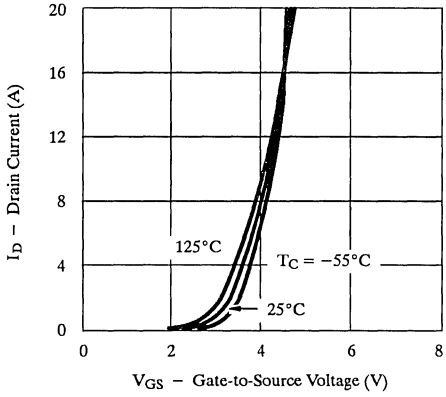
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

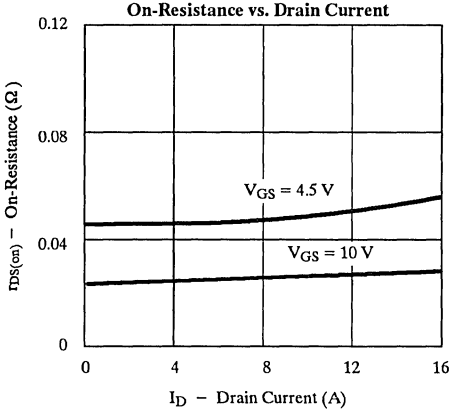
Output Characteristics



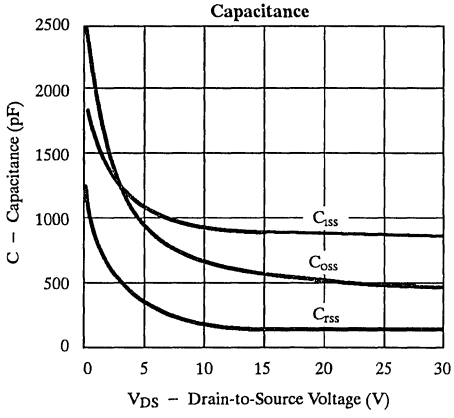
Transfer Characteristics



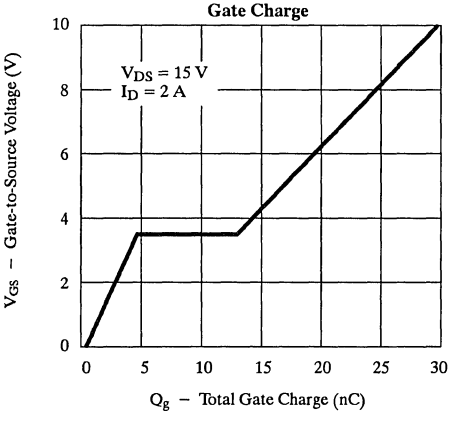
On-Resistance vs. Drain Current



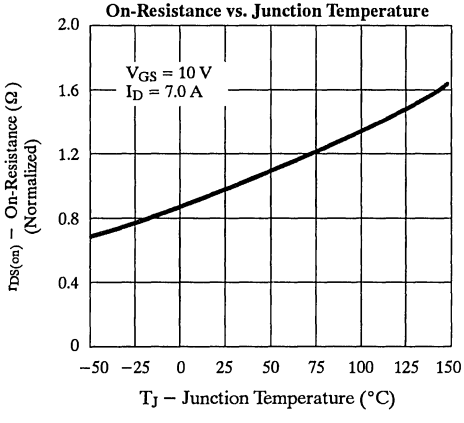
Capacitance



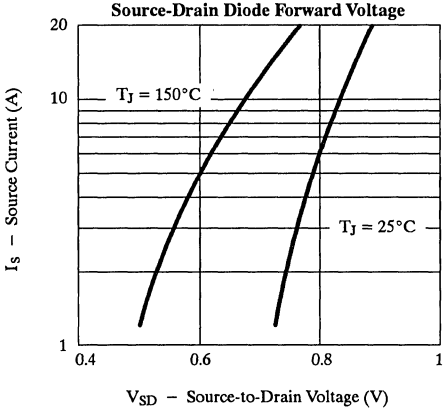
Gate Charge

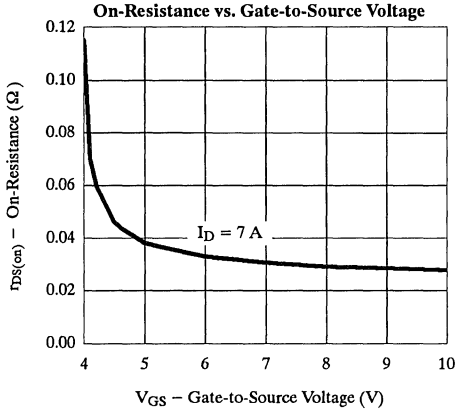


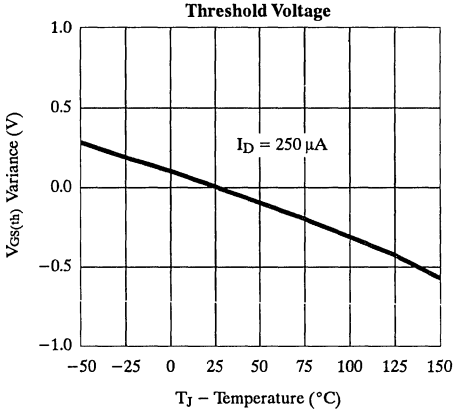
On-Resistance vs. Junction Temperature

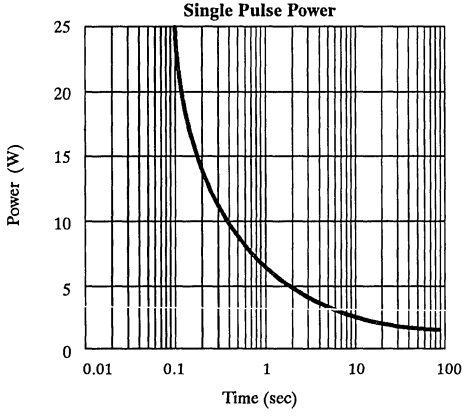


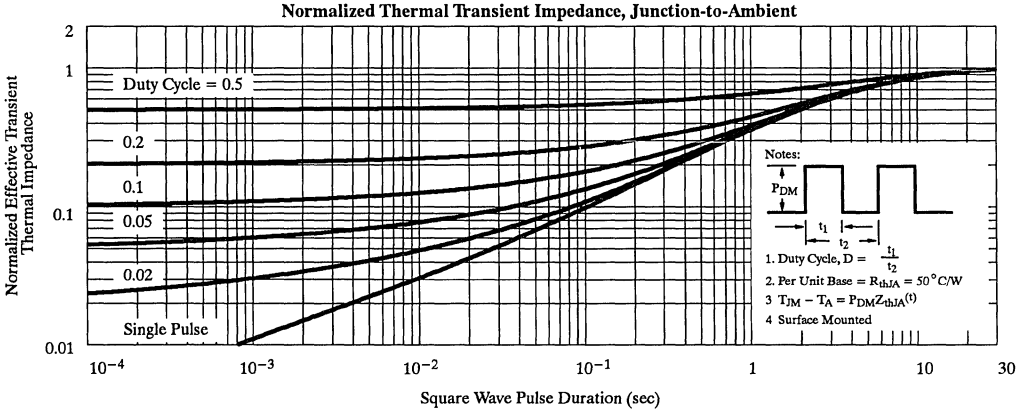
Typical Characteristics (25°C Unless Otherwise Noted)











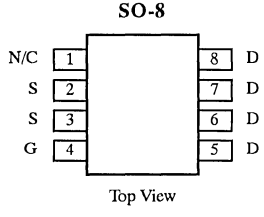
Siliconix

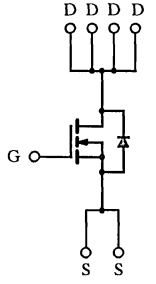
Si9420DY

N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	1.0 @ V_{GS} = 10 V	±1.0





N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±1.0	A
	T_A = 70°C		±0.8	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	1.0	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

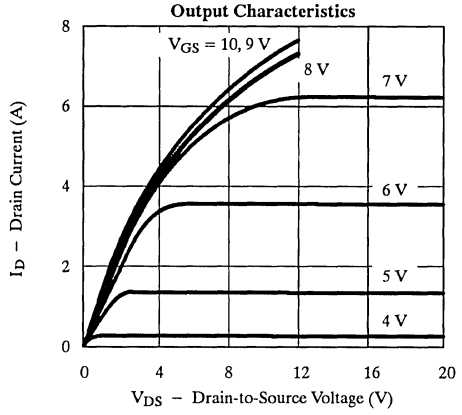
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

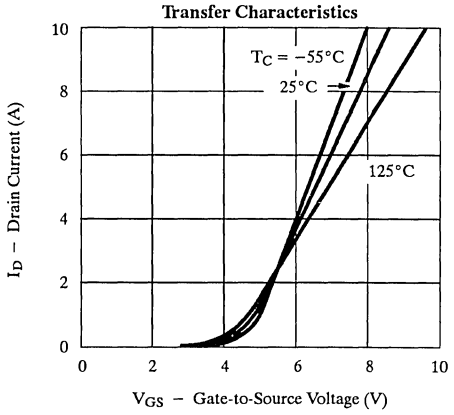
Specifications (T_J = 25°C Unless Otherwise Noted)

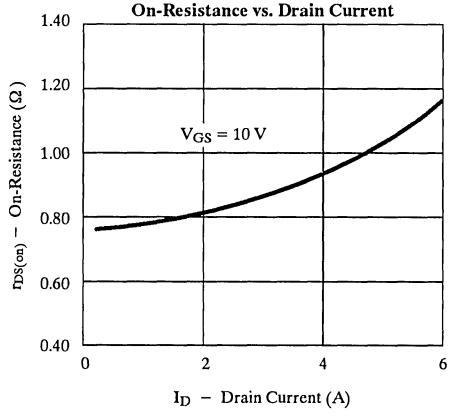
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			2	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 10 V, V_{GS} = 10 V	5.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.0 A		0.8	1.0	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 1.0 A		1.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.0 A, V_{GS} = 0 V		0.7	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 1.0 A		8.6	16	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 100 Ω I_D ≅ 1.0 A, V_{GEN} = 10 V, R_G = 6 Ω		7	14	ns
Rise Time	t_r			12	24	
Turn-Off Delay Time	$t_{d(off)}$			26	50	
Fall Time	t_f			15	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.0 A, di/dt = 100 A/µs		130		

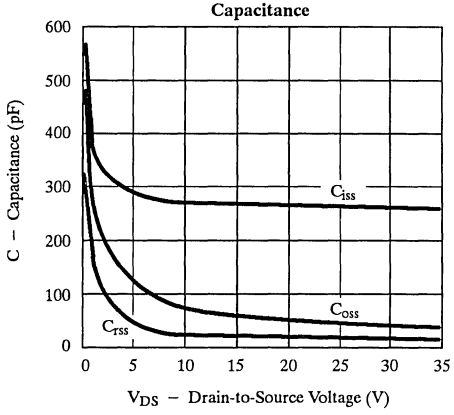
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

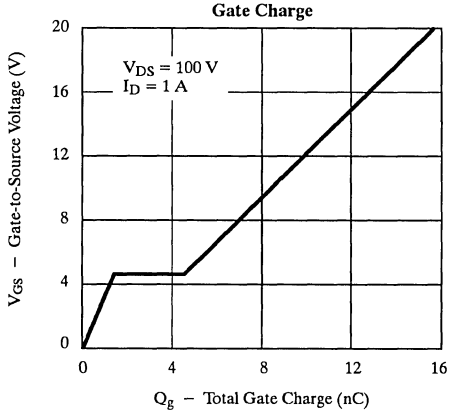
Typical Characteristics (25°C Unless Otherwise Noted)

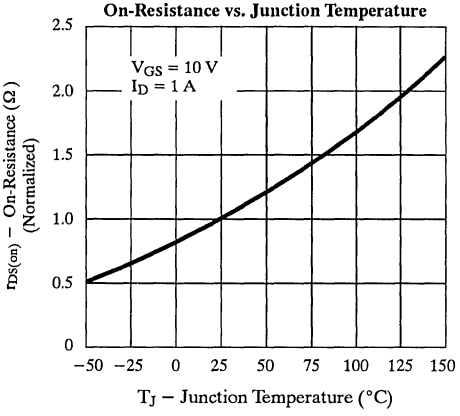




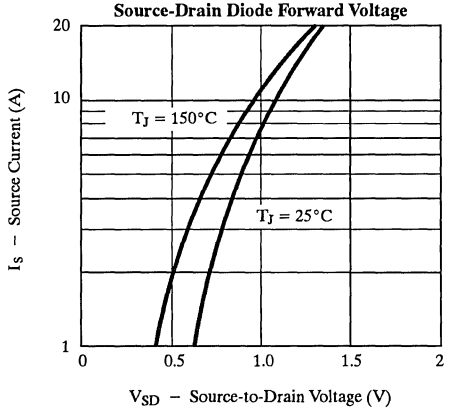


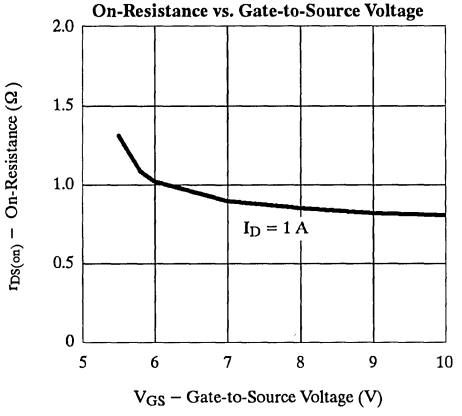


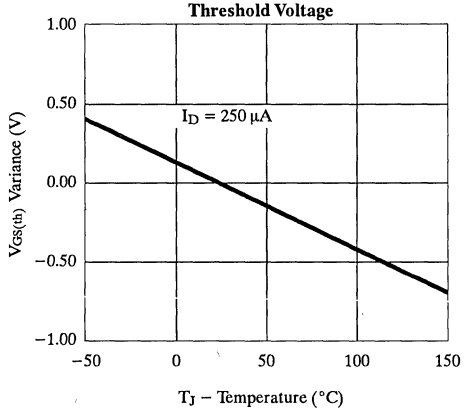


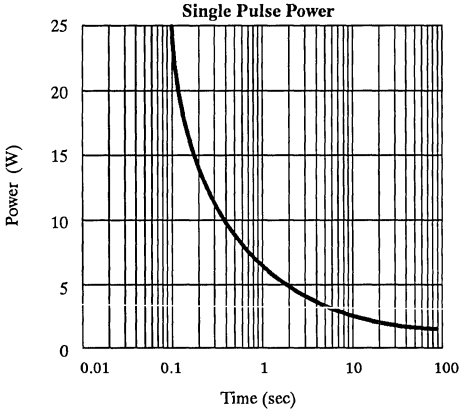


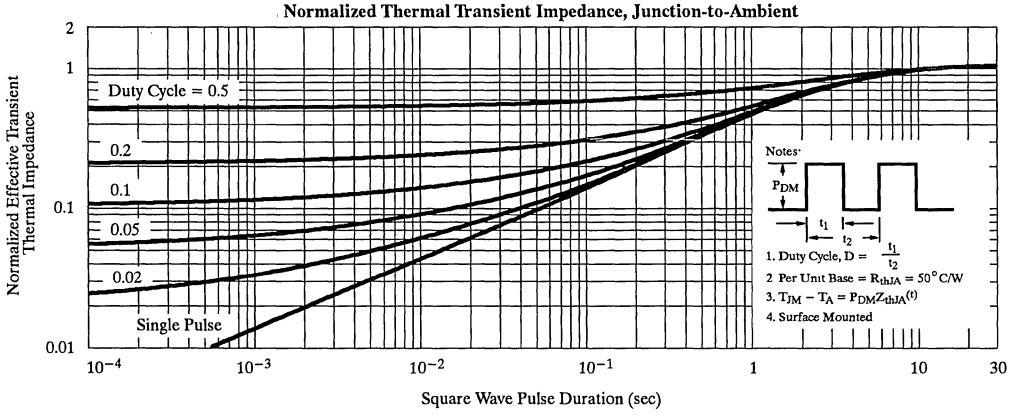
Typical Characteristics (25°C Unless Otherwise Noted)











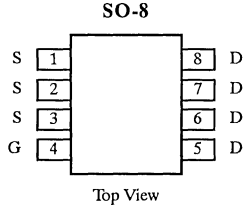
Siliconix

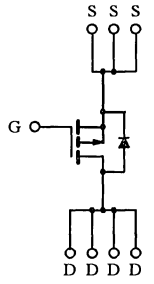
Si9430DY

P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.050 @ V_{GS} = −10 V	±5.8
	0.065 @ V_{GS} = −6 V	±4.9
	0.090 @ V_{GS} = −4.5 V	±4.0





P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.8	A
	T_A = 70°C		±4.6	
Pulsed Drain Current		I_{DM}	±15	
Continuous Source Current (Diode Conduction)		I_S	−2.4	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

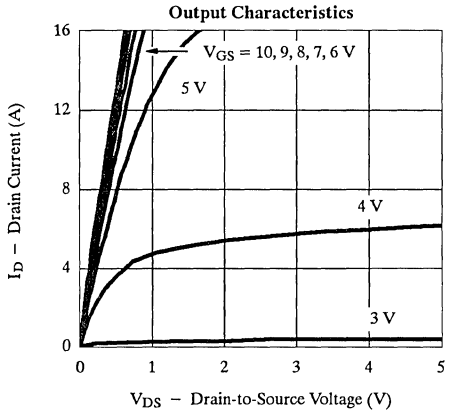
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

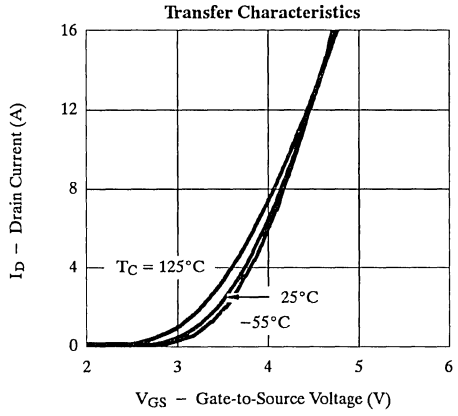
Specifications (T_J = 25°C Unless Otherwise Noted)

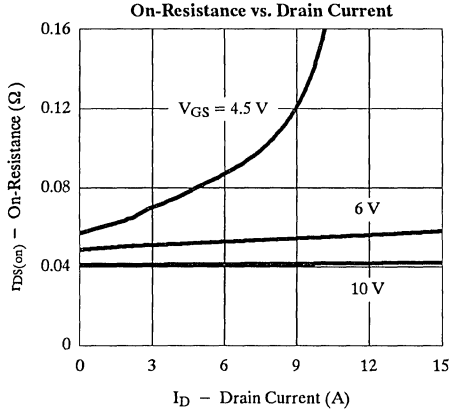
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −10 V	−15			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−3.6			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −5.3 A		0.040	0.050	Ω
		V_{GS} = −6 V, I_D = −3.6 A		0.055	0.065	
		V_{GS} = −4.5 V, I_D = −2.0 A		0.070	0.090	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −5.3 A		8.0		S
Diode Forward Voltage[b]	V_{SD}	I_S = −2.4 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −5.3 A		25	50	nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			8		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		14	30	ns
Rise Time	t_r			22	60	
Turn-Off Delay Time	$t_{d(off)}$			50	120	
Fall Time	t_f			25	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2.4 A, di/dt = 100 A/µs		85	100	

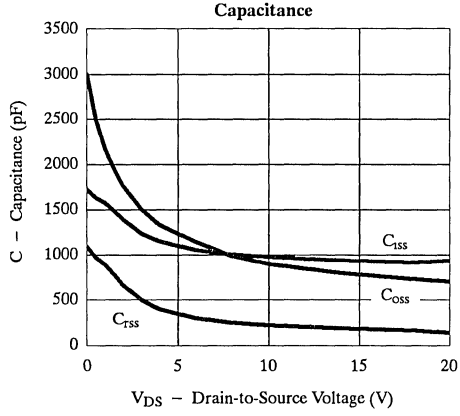
Notes
a Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

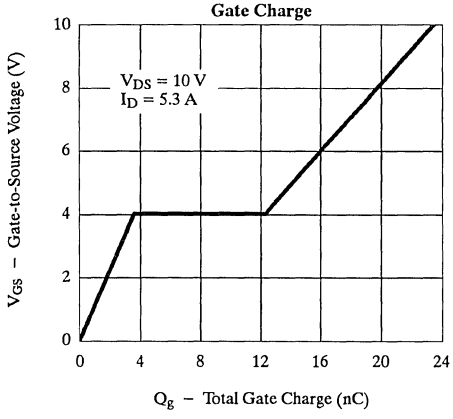
Typical Characteristics (25°C Unless Otherwise Noted)

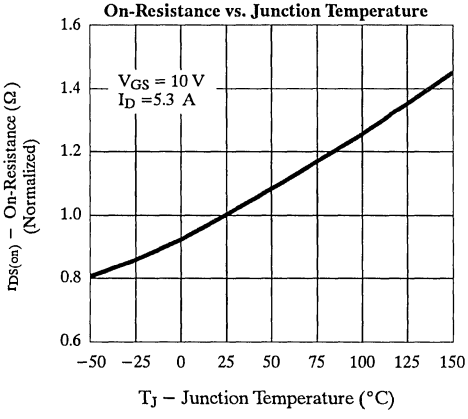




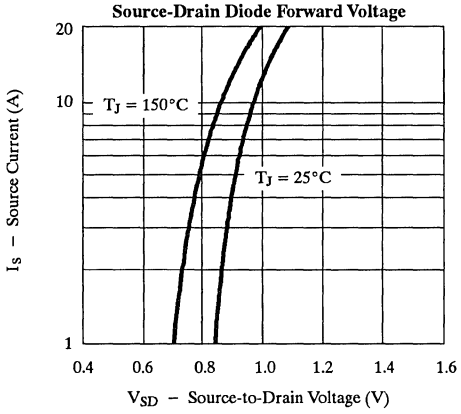


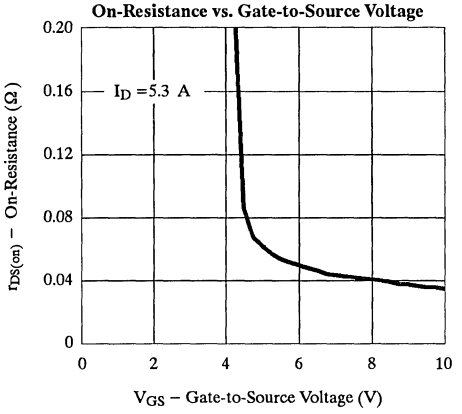


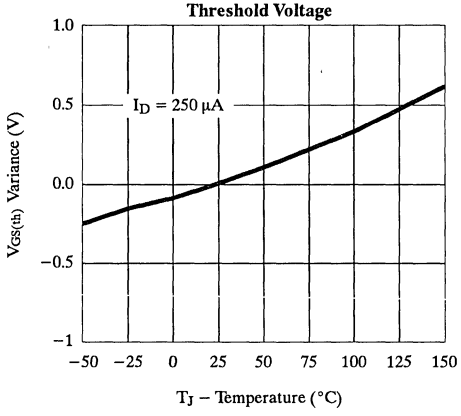


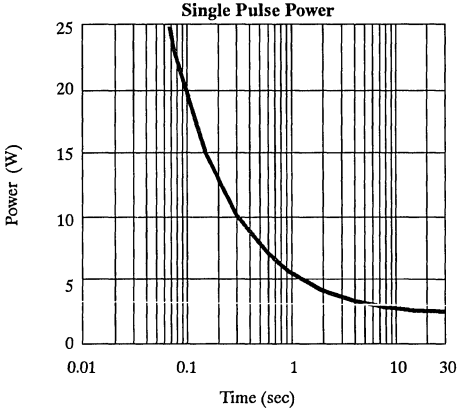


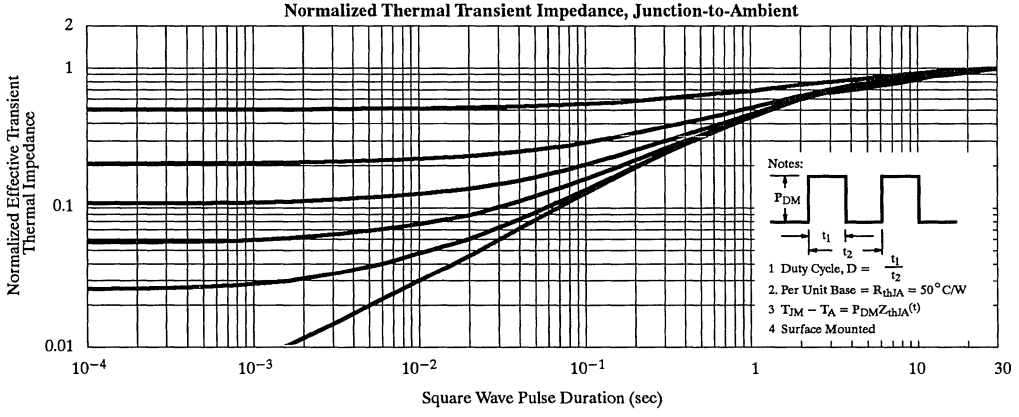
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

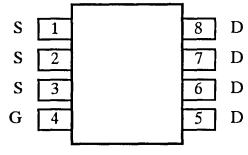
Si9433DY

P-Channel Enhancement-Mode MOSFET

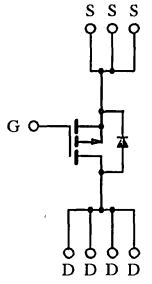
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.065 @ V_{GS} = −4.5 V	±5.4
	0.100 @ V_{GS} = −2.7 V	±4.2

SO-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.4	A
	T_A = 70°C		±4.4	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	−2.6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

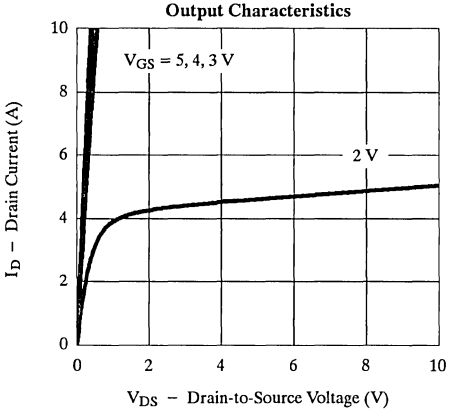
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−0.8			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−10			A
		V_{DS} ≤ −5 V, V_{GS} = −2.7 V	−4			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −5.1 A		0.045	0.065	Ω
		V_{GS} = −2.7 V, I_D = −2.0 A		0.060	0.100	
Forward Transconductance[b]	g_{fs}	V_{DS} = −9 V, I_D = −5.1 A		11		S
Diode Forward Voltage[b]	V_{SD}	I_S = −2.6 A, V_{GS} = 0 V		−1.0	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −5.1 A		20	60	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			10		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −6 V, R_L = 6 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω		30	60	ns
Rise Time	t_r			55	100	
Turn-Off Delay Time	$t_{d(off)}$			80	180	
Fall Time	t_f			50	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2.6, di/dt = 100 A/µs		60	80	

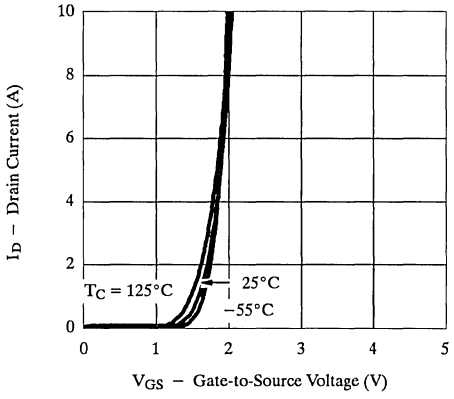
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

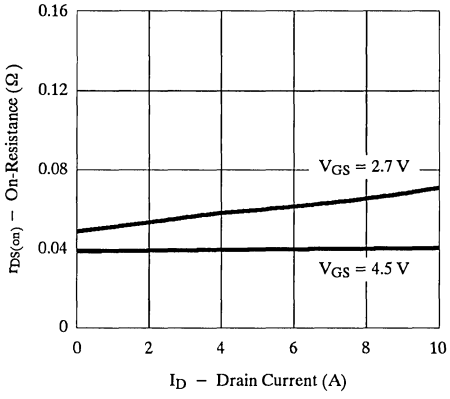
Output Characteristics



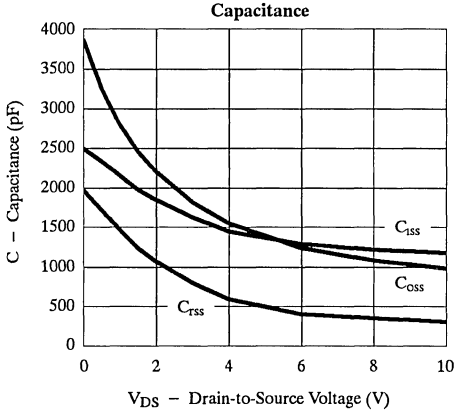
Transfer Characteristics



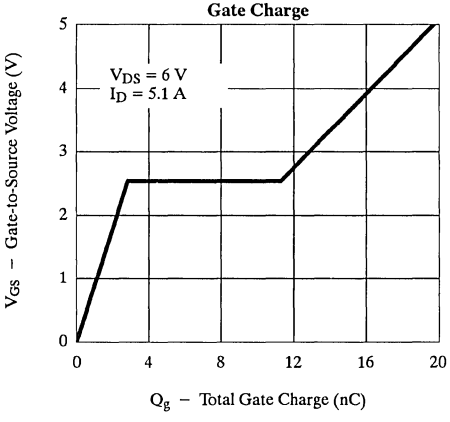
On-Resistance vs. Drain Current



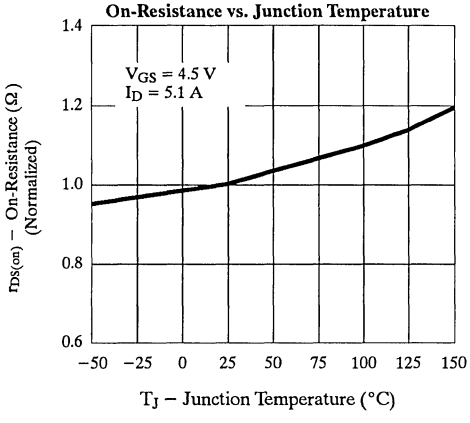
Capacitance



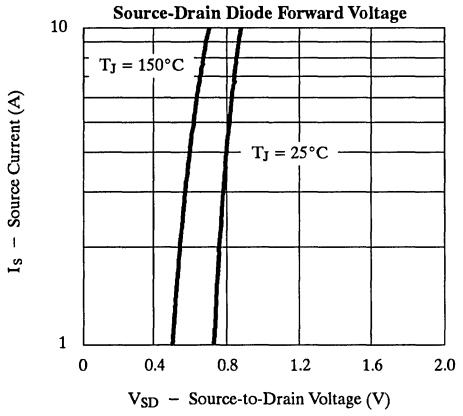
Gate Charge

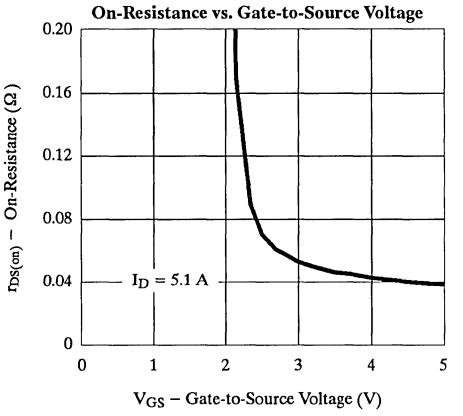


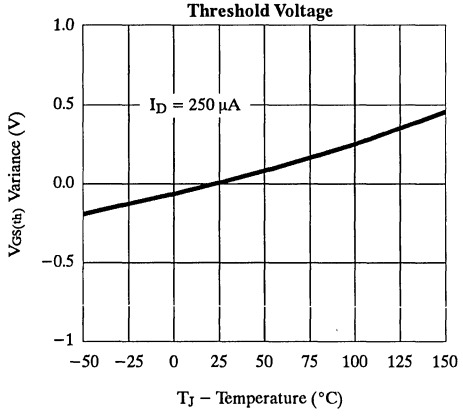
On-Resistance vs. Junction Temperature

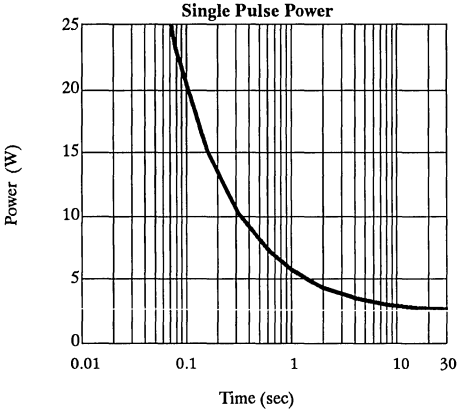


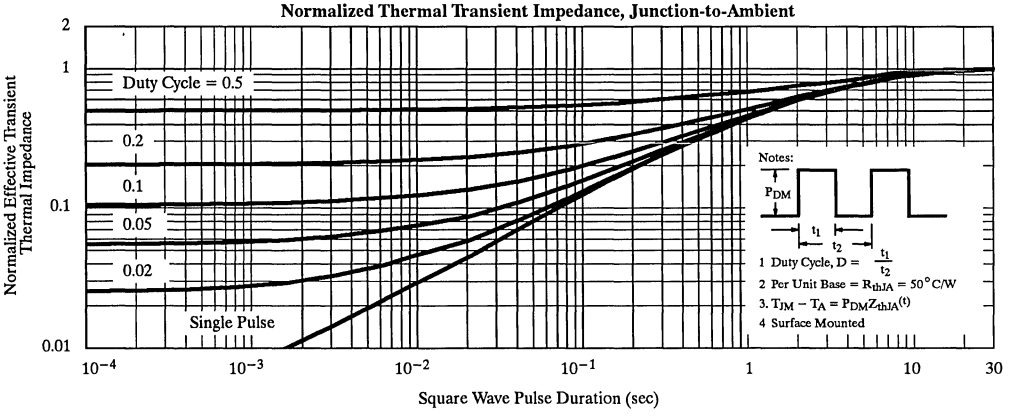
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

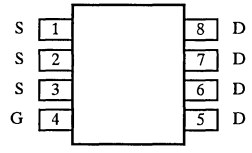
Si9434DY

P-Channel Enhancement-Mode MOSFET

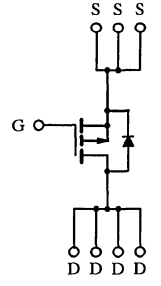
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−12	0.040 @ V_{GS} = −4.5 V	±6.4
	0.060 @ V_{GS} = −2.7 V	±5.1

SO-8



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±6.4	A
	T_A = 70°C		±5.1	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	−2.5	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

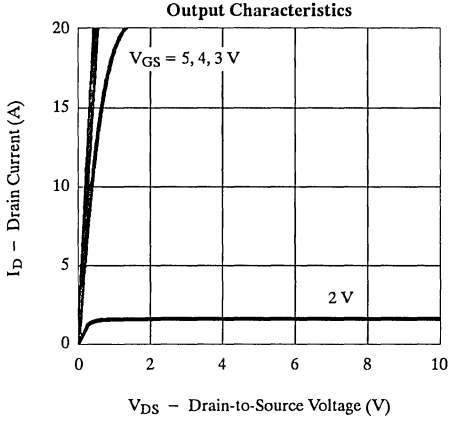
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−0.7			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −9.6 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −6.0 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−10			A
		V_{DS} ≤ −5 V, V_{GS} = −2.7V	−8			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −6.4 A			0.040	Ω
		V_{GS} = −2.7 V, I_D = −5.1 A			0.060	
Forward Transconductance[a]	g_{fs}	V_{DS} = −9 V, I_D = −6.4 A		14		S
Diode Forward Voltage[a]	V_{SD}	I_S = −2.5 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −6.4 A		36	80	nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			17		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −6 V, R_L = 6 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω		60	150	ns
Rise Time	t_r			90	200	
Turn-Off Delay Time	$t_{d(off)}$			150	300	
Fall Time	t_f			110	200	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2.5 A, di/dt = 100 A/µs		50	100	

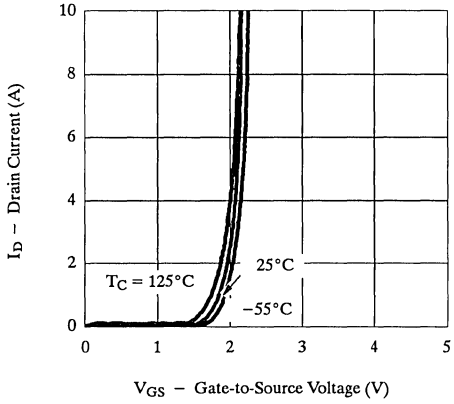
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

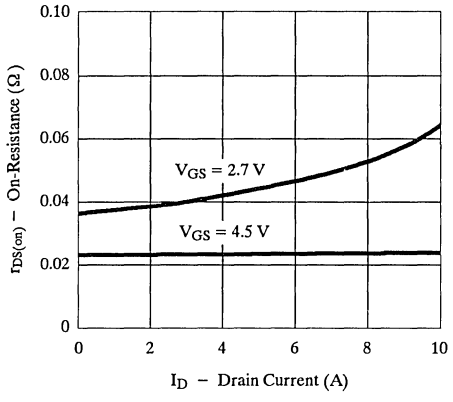
Output Characteristics



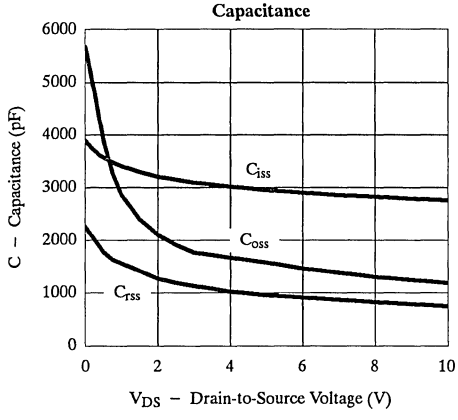
Transfer Characteristics



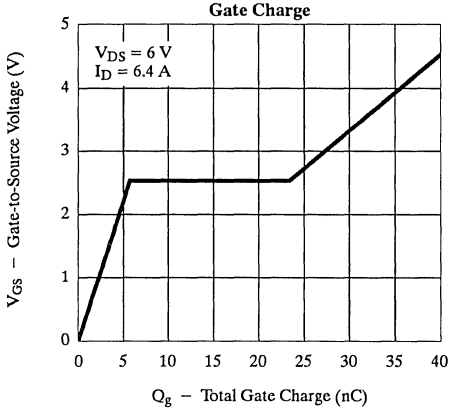
On-Resistance vs. Drain Current



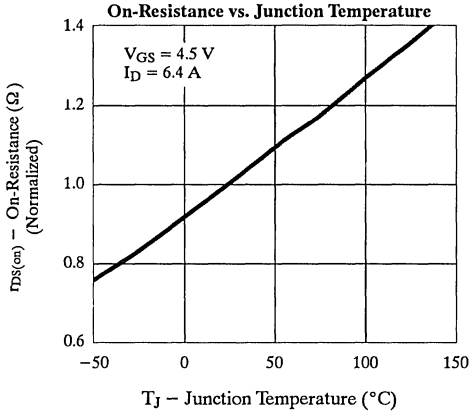
Capacitance



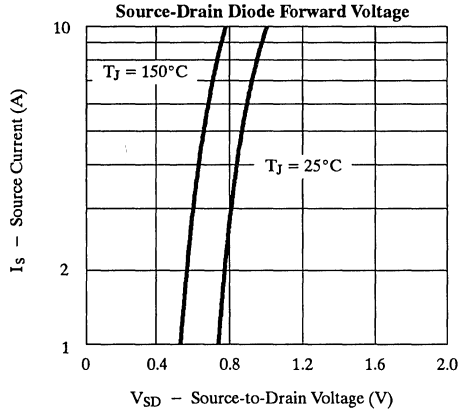
Gate Charge

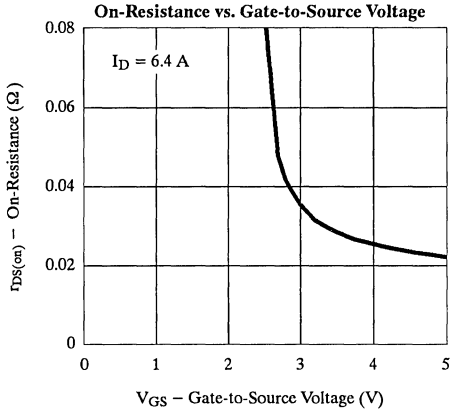


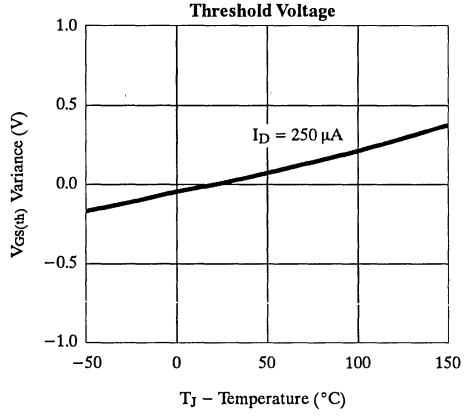
On-Resistance vs. Junction Temperature

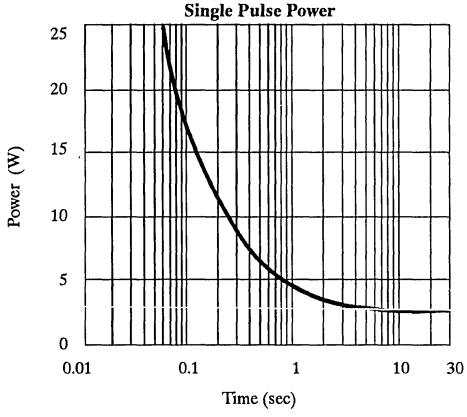


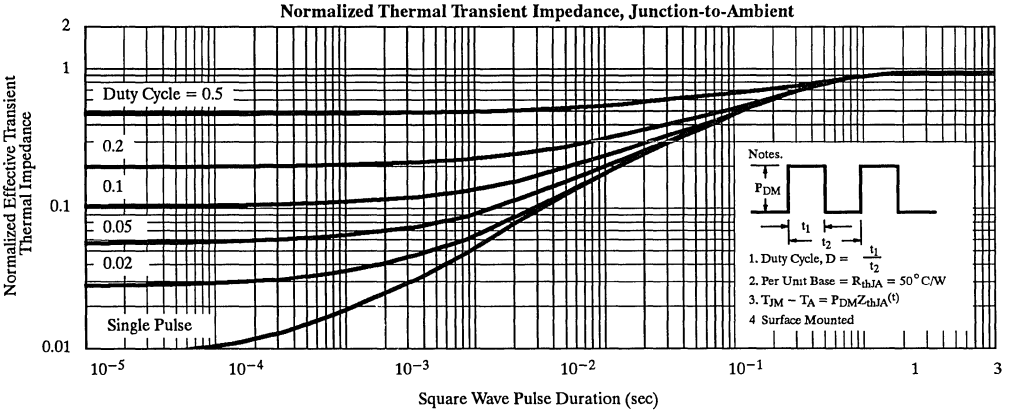
Typical Characteristics (25°C Unless Otherwise Noted)











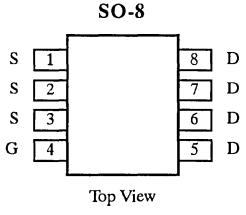
Siliconix

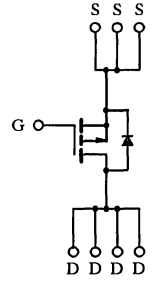
Si9435DY

P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−30	0.055 @ V_{GS} = −10 V	±5.1
	0.07 @ V_{GS} = −6 V	±4.6
	0.105 @ V_{GS} = −4.5 V	±3.6





P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.1	A
	T_A = 70°C		±4.6	
Pulsed Drain Current		I_{DM}	±15	
Continuous Source Current (Diode Conduction)		I_S	−2.6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

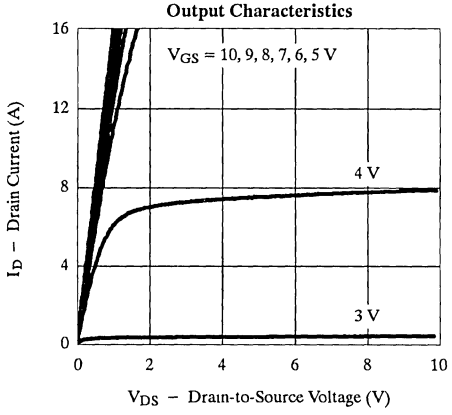
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −24 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −15 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −10 V, V_{GS} = −10 V	−15			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−4			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −4.6 A		0.045	0.055	Ω
		V_{GS} = −6 V, I_D = −4.1 A		0.060	0.07	
		V_{GS} = −4.5 V, I_D = −2.0 A		0.075	0.105	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −4.6 A		7.0		S
Diode Forward Voltage[b]	V_{SD}	I_S = −2.6 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −15 V, V_{GS} = −10 V, I_D = −4.6 A		23	40	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −15 V, R_L = 15 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		12	30	ns
Rise Time	t_r			21	60	
Turn-Off Delay Time	$t_{d(off)}$			45	120	
Fall Time	t_f			27	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.6 A, di/dt = 100 A/µs		70	100	

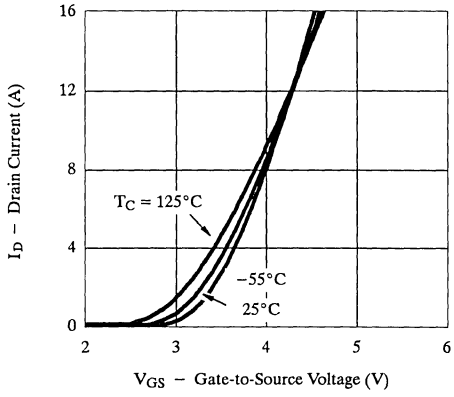
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

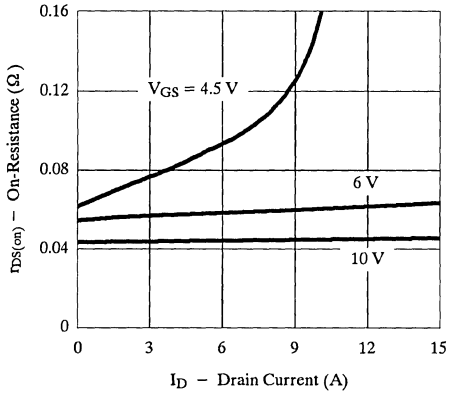
Output Characteristics



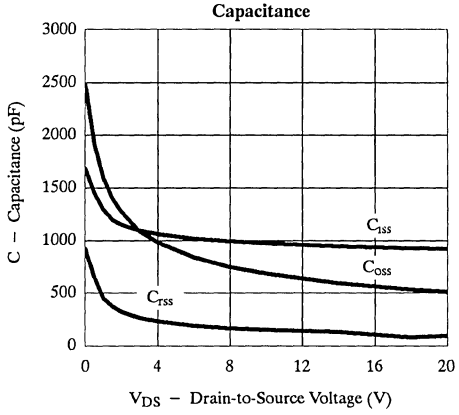
Transfer Characteristics



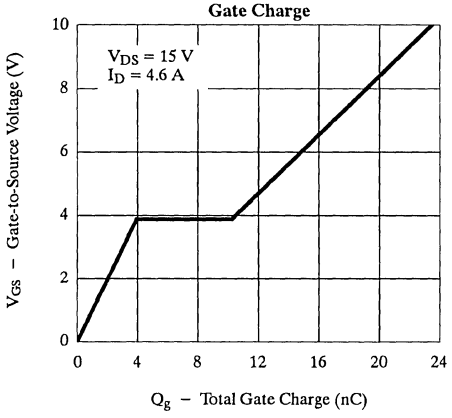
On-Resistance vs. Drain Current



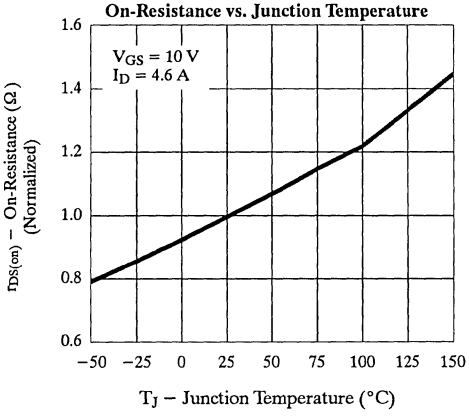
Capacitance



Gate Charge

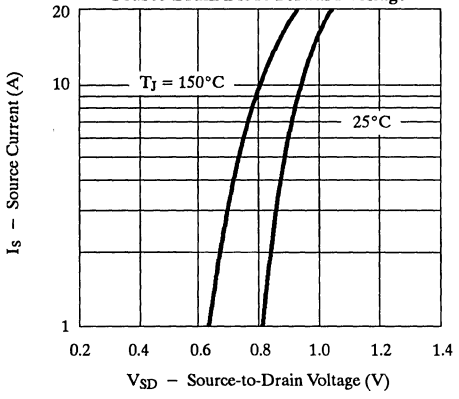


On-Resistance vs. Junction Temperature

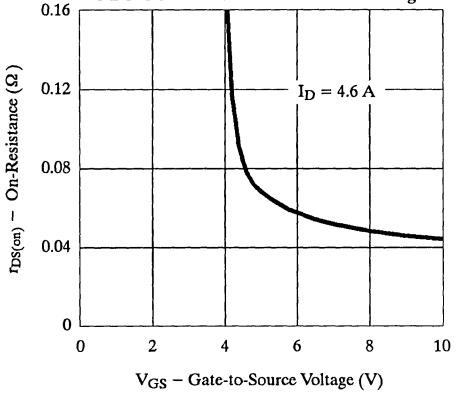


Typical Characteristics (25°C Unless Otherwise Noted)

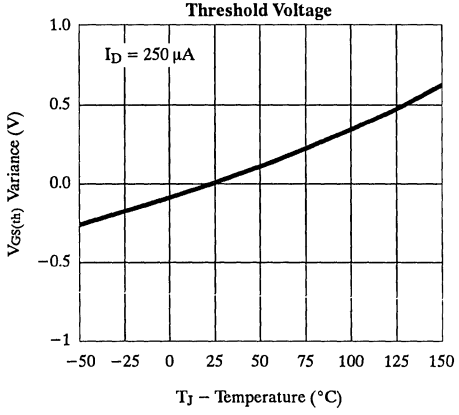
Source-Drain Diode Forward Voltage



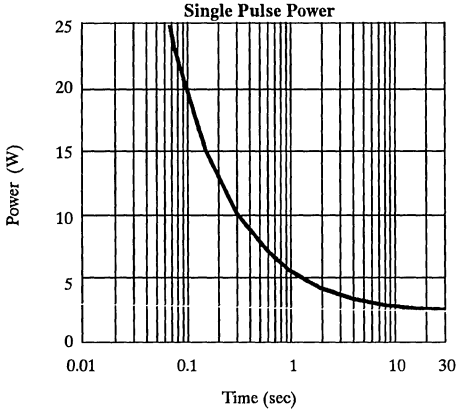
On-Resistance vs. Gate-to-Source Voltage



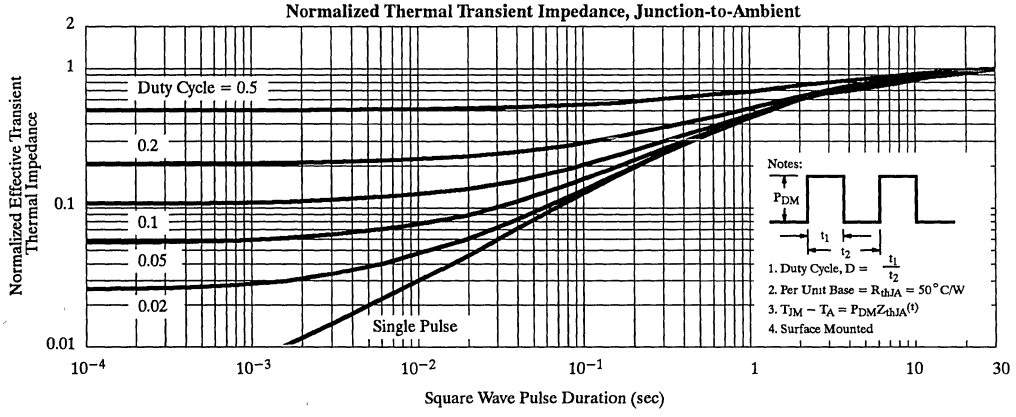
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

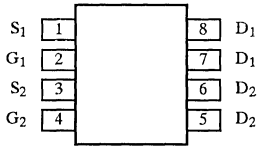
Si9925DY

Dual N-Channel Enhancement-Mode MOSFET

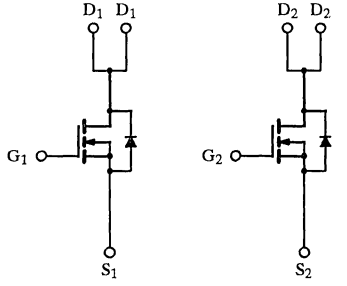
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.05 @ V_{GS} = 4.5 V	±5.0
	0.06 @ V_{GS} = 3.0 V	±4.2
	0.08 @ V_{GS} = 2.5 V	±3.6

SO-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.0	A
	T_A = 70°C		±4.0	
Pulsed Drain Current (10 µs Pulse Width)		I_{DM}	±48	
Continuous Source Current (Diode Conduction)		I_S	1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

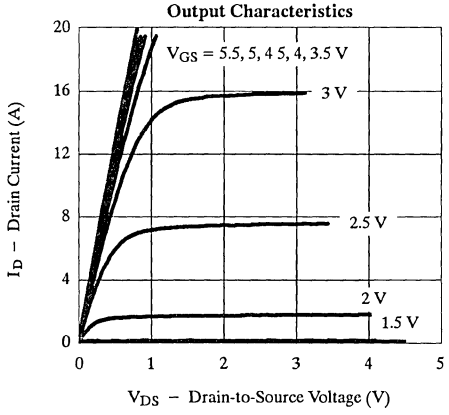
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.8			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V			1	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 5 V	10			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 7.2 V, I_D = 5.0 A	0.025	0.036	0.045	Ω
		V_{GS} = 4.5 V, I_D = 5.0 A		0.041	0.05	
		V_{GS} = 3.0 V, I_D = 3.9 A		0.050	0.07	
		V_{GS} = 2.5 V, I_D = 1 A		0.060	0.08	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 5.0 A		13		S
Diode Forward Voltage[a]	V_{SD}	I_S =5.0 A, V_{GS} = 0 V		0.9	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 5.0 A		10	20	nC
Gate-Source Charge	Q_{gs}			2.6		
Gate-Drain Charge	Q_{gd}			3.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 6 V, R_L = 6 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		13	40	ns
Rise Time	t_r			9	30	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			9	30	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 5.0 A, di/dt = 100 A/µs		100	150	

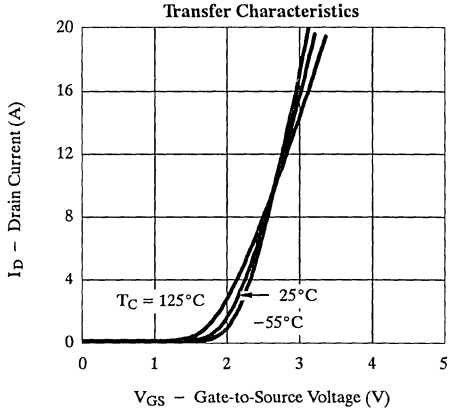
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)

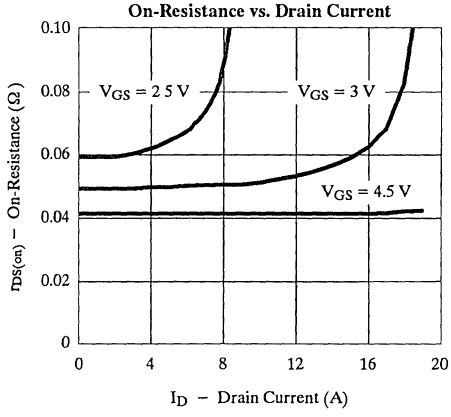
Output Characteristics



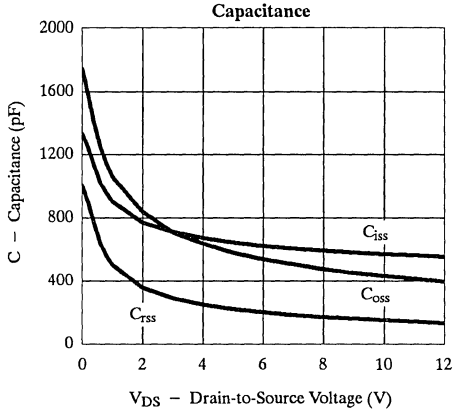
Transfer Characteristics



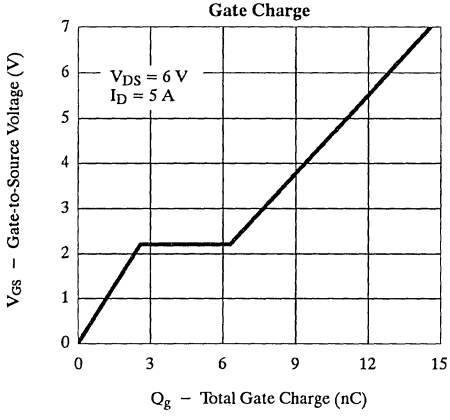
On-Resistance vs. Drain Current



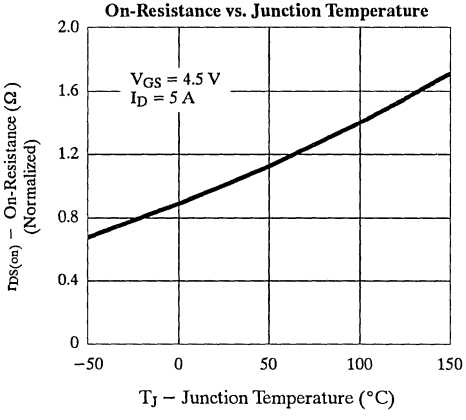
Capacitance



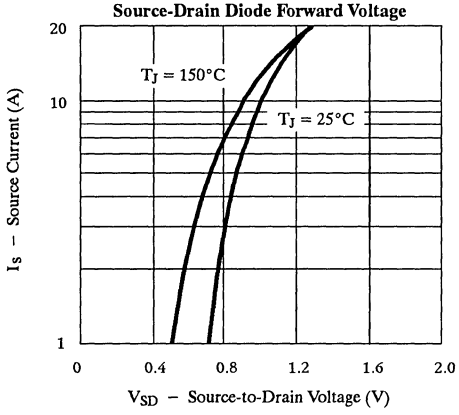
Gate Charge

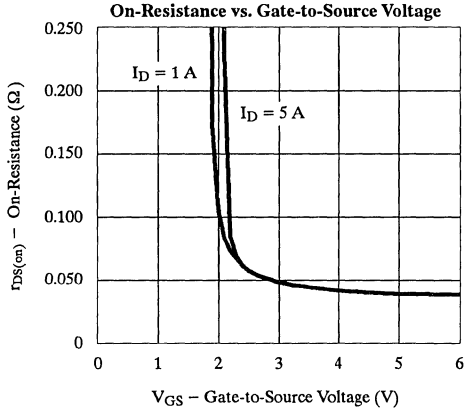


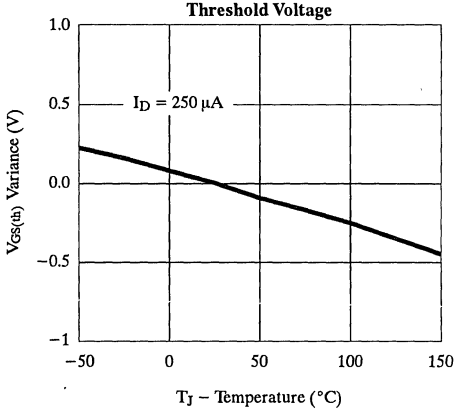
On-Resistance vs. Junction Temperature

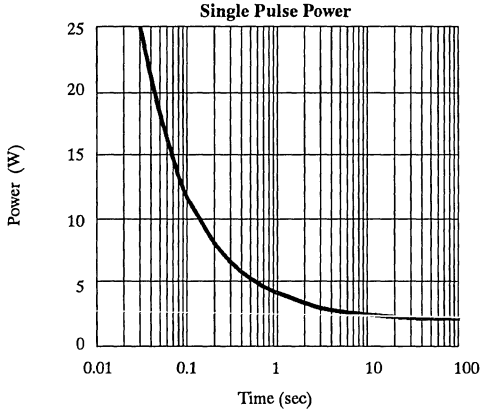


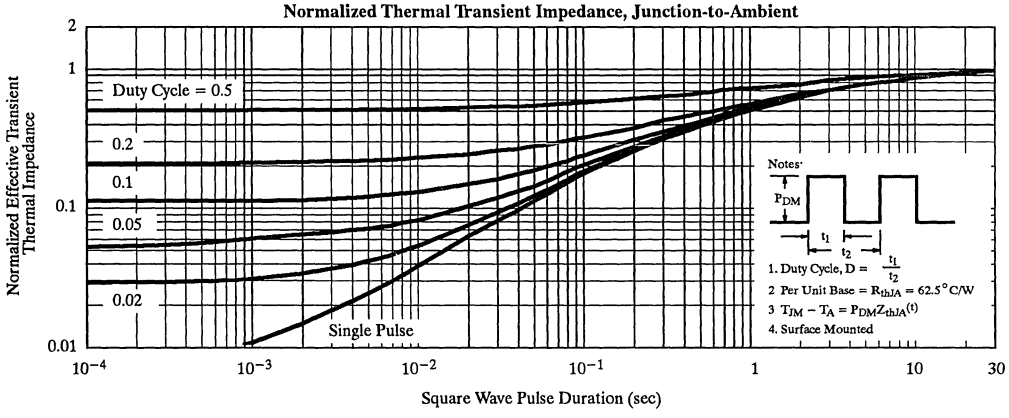
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

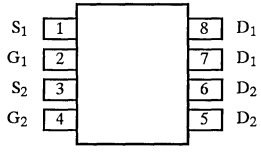
Si9928DY

Dual Enhancement-Mode MOSFETs (N- and P-Channel)

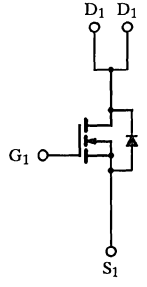
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.05 @ V_{GS} = 4.5 V	±5.0
		0.06 @ V_{GS} = 3.0 V	±4.2
		0.08 @ V_{GS} = 2.7 V	±3.6
P-Channel	−20	0.11 @ V_{GS} = −4.5 V	±3.4
		0.15 @ V_{GS} = −3.0 V	±2.9
		0.19 @ V_{GS} = −2.7 V	±2.6

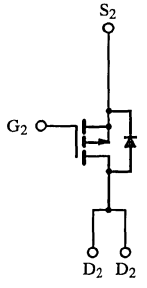
SO-8



Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	−20	V
Gate-Source Voltage		V_{GS}	±12	±12	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.0	±3.4	A
	T_A = 70°C		±4.0	±2.8	
Pulsed Drain Current		I_{DM}	±10	±10	
Continuous Source Current (Diode Conduction)		I_S	2.0	−2.0	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	2.0	W
	T_A = 70°C		1.3	1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.8	1.2		V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−0.8	−1.1		
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = − 16 V, V_{GS} = 0 V	P-Ch			−1	
		V_{DS} = 10 V, V_{GS} = 0 V, T_J = 70°C	N-Ch			5	
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C	P-Ch			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	10			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−10			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 5.0 A	N-Ch		0.041	0.05	Ω
		V_{GS} = −4.5 V, I_D = −3.2 A	P-Ch		0.087	0.11	
		V_{GS} = 3.0 V, I_D = 3.9 A	N-Ch		0.052	0.06	
		V_{GS} = −3.0 V, I_D = −2.0 A	P-Ch		0.120	0.15	
		V_{GS} = 2.7 V, I_D = 1.0 A	N-Ch		0.060	0.08	
		V_{GS} = −2.7 V, I_D = −1.0 A	P-Ch		0.135	0.19	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 5.0 A	N-Ch		13		S
		V_{DS} = −9 V, I_D = −3.2 A	P-Ch		8		
Diode Forward Voltage[b]	V_{SD}	I_S = 5.0 A, V_{GS} = 0 V	N-Ch		0.9	1.2	V
		I_S = −2.0 A, V_{GS} = 0 V	P-Ch		−0.9	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 5.0 A; P-Channel V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −3.2 A	N-Ch		10	20	nC
			P-Ch		8	20	
Gate-Source Charge	Q_{gs}		N-Ch		2.6		
			P-Ch		1.6		
Gate-Drain Charge	Q_{gd}		N-Ch		3.7		
			P-Ch		3.5		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 6 V, R_L = 6 Ω, I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω; P-Channel V_{DD} = −6 V, R_L = 6 Ω, I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω	N-Ch		13	30	ns
			P-Ch		22	40	
Rise Time	t_r		N-Ch		9	40	
			P-Ch		43	80	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		30	60	
			P-Ch		35	70	
Fall Time	t_f		N-Ch		9	30	
			P-Ch		20	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 5.0 A, di/dt = 100 A/µs	N-Ch		100	150	
		I_F = −2.0 A, di/dt = 100 A/µs	P-Ch		75	100	

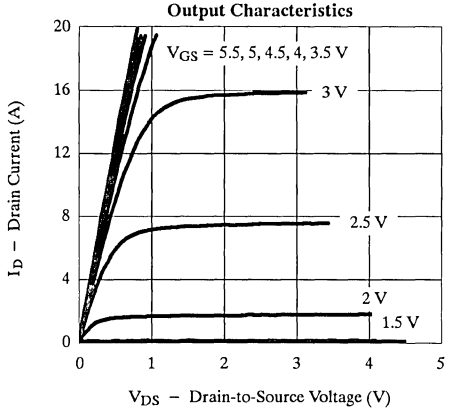
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics

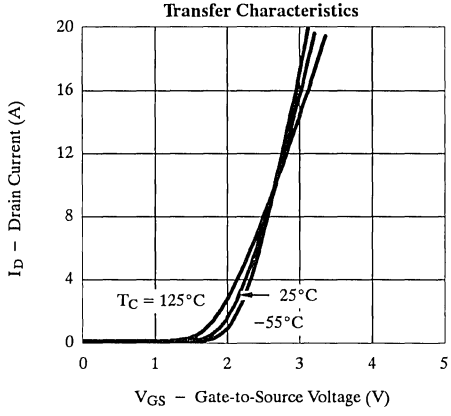
N-Channel

(25°C Unless Otherwise Noted)

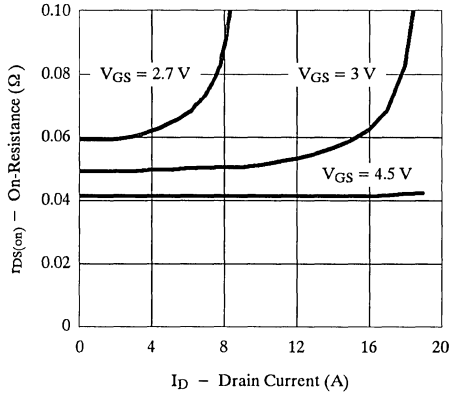
Output Characteristics



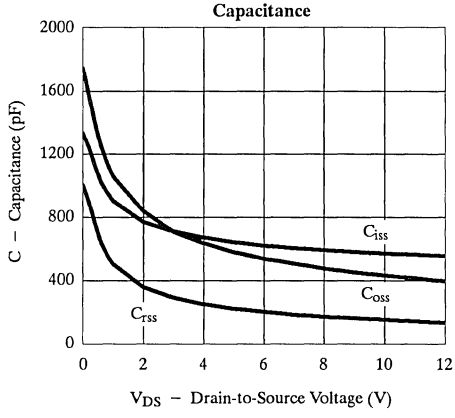
Transfer Characteristics



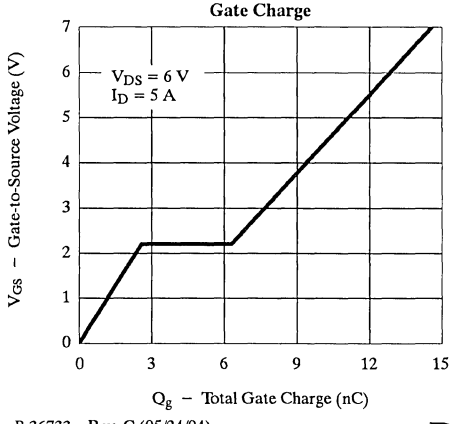
On-Resistance vs. Drain Current



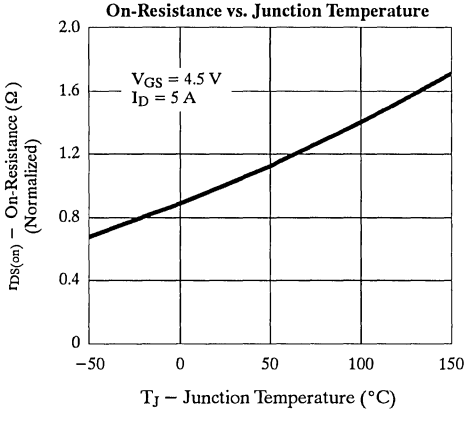
Capacitance



Gate Charge



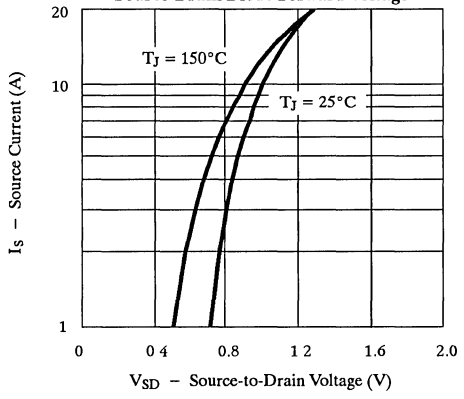
On-Resistance vs. Junction Temperature



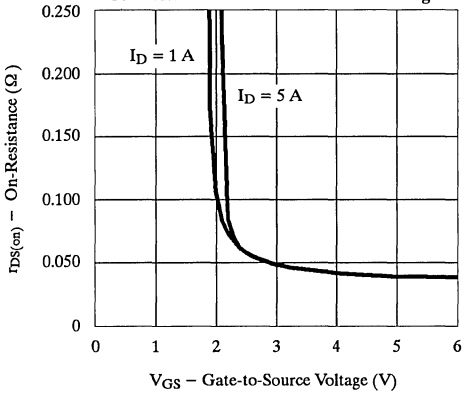
Typical Characteristics

(25°C Unless Otherwise Noted)

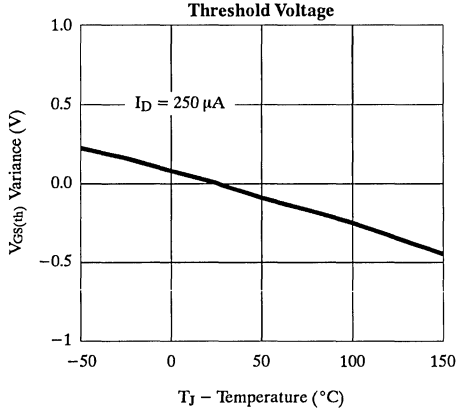
Source-Drain Diode Forward Voltage



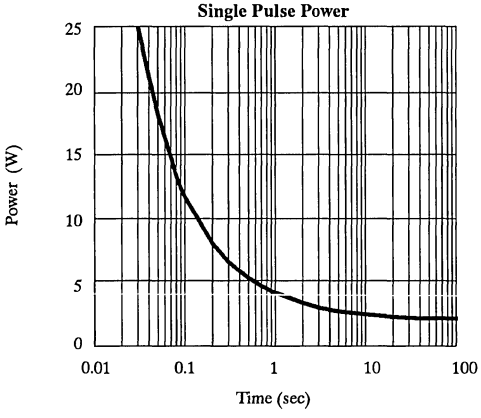
On-Resistance vs. Gate-to-Source Voltage



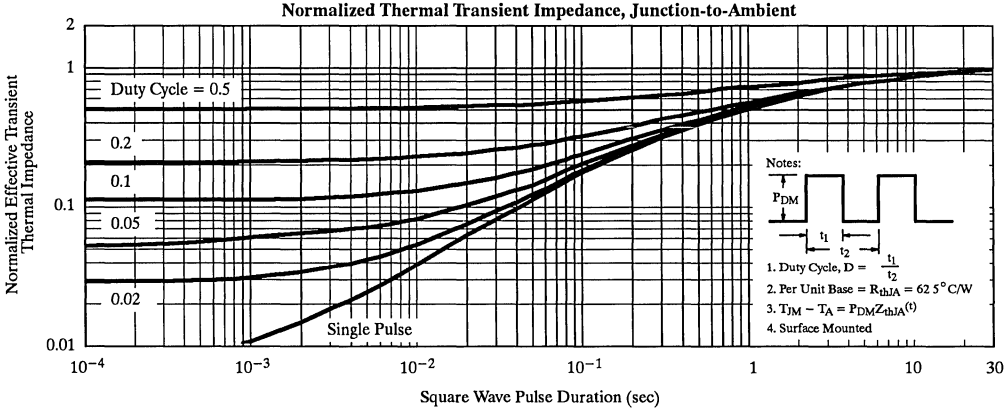
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

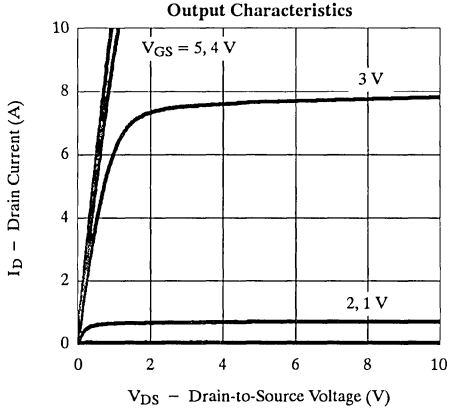


Typical Characteristics

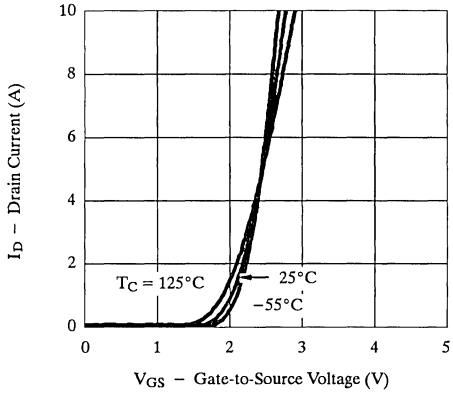
P-Channel

(25°C Unless Otherwise Noted)

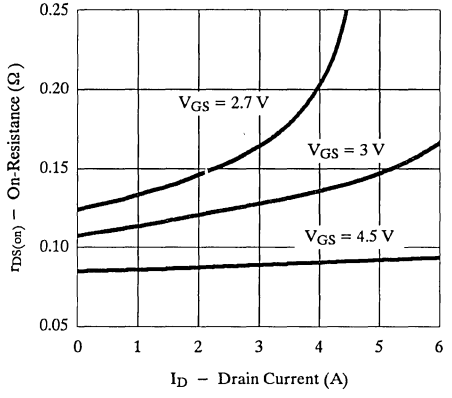
Output Characteristics



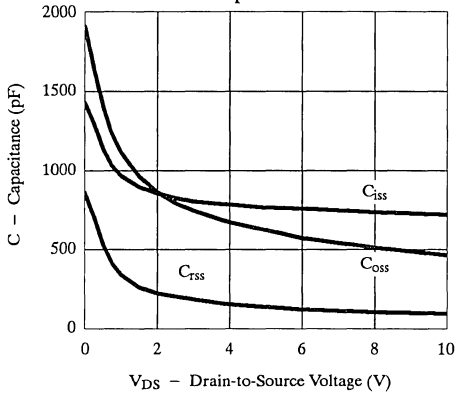
Transfer Characteristics



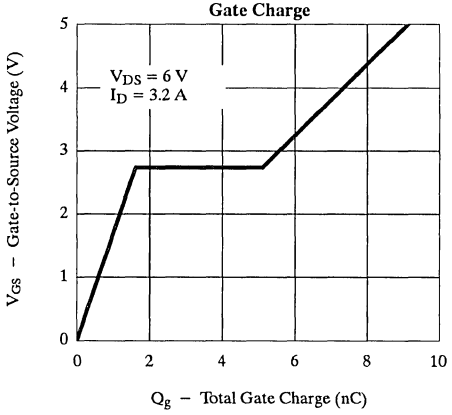
On-Resistance vs. Drain Current



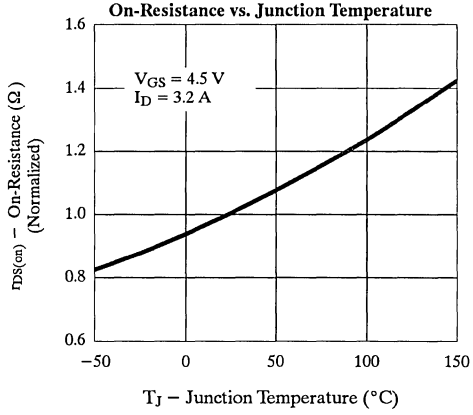
Capacitance



Gate Charge



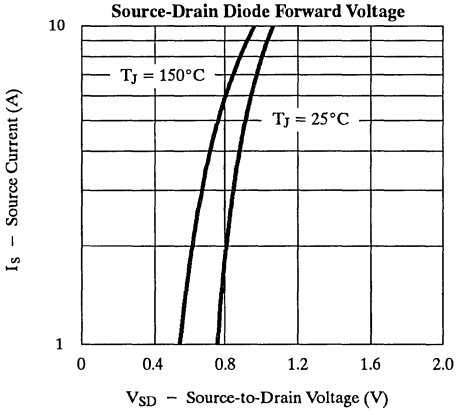
On-Resistance vs. Junction Temperature



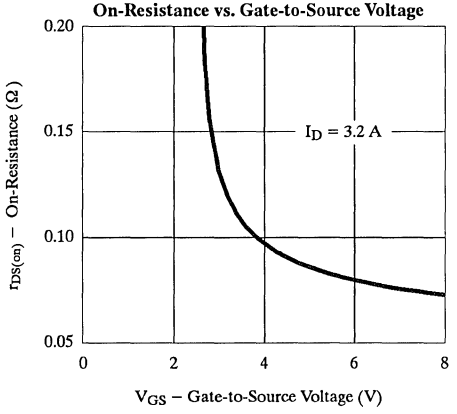
Typical Characteristics

(25°C Unless Otherwise Noted)

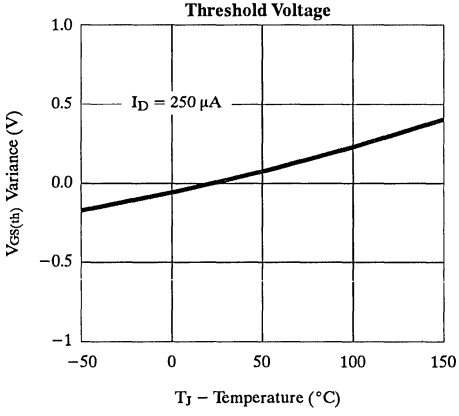
Source-Drain Diode Forward Voltage



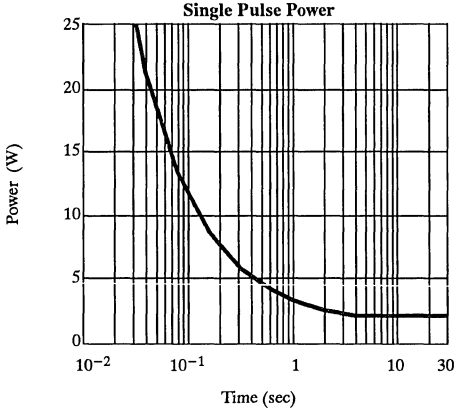
On-Resistance vs. Gate-to-Source Voltage



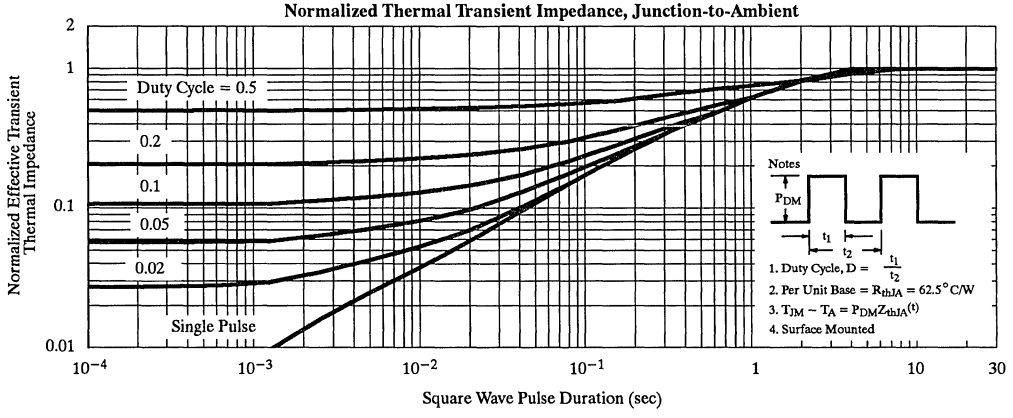
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

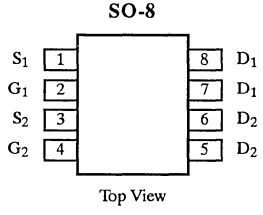


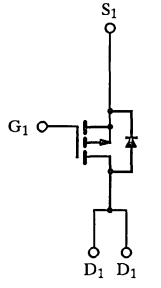
Si9933DY

Dual P-Channel Enhancement-Mode MOSFET

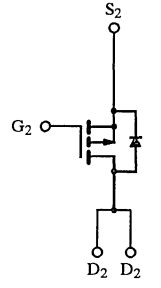
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.11 @ V_{GS} = −4.5 V	±3.4
	0.15 @ V_{GS} = −3.0 V	±2.9
	0.19 @ V_{GS} = −2.7 V	±2.6





P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.4	A
	T_A = 70°C		±2.7	
Pulsed Drain Current		I_{DM}	±8	
Continuous Source Current (Diode Conduction)		I_S	−2.0	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

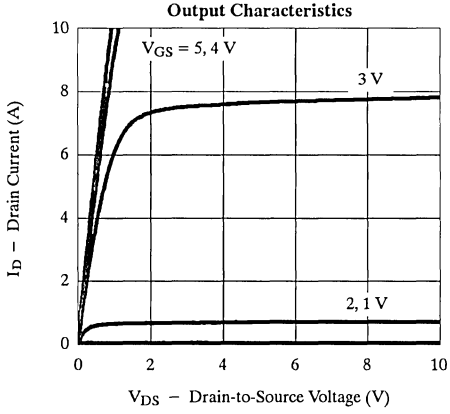
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−0.8			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−8			A
		V_{DS} ≤ −5 V, V_{GS} = −2.7 V	−2			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −3.2 A		0.09	0.11	Ω
		V_{GS} = −3.0 V, I_D = −2.0 A		0.120	0.15	
		V_{GS} = −2.7 V, I_D = −1 A		0.135	0.19	
Forward Transconductance[b]	g_{fs}	V_{DS} = −9 V, I_D = −3.4 A		8		S
Diode Forward Voltage[b]	V_{SD}	I_S = −2.0 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −3.2 A		8	20	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −6 V, R_L = 6 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω		22	40	ns
Rise Time	t_r			43	80	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2.0 A, di/dt = 100 A/µs		75	100	

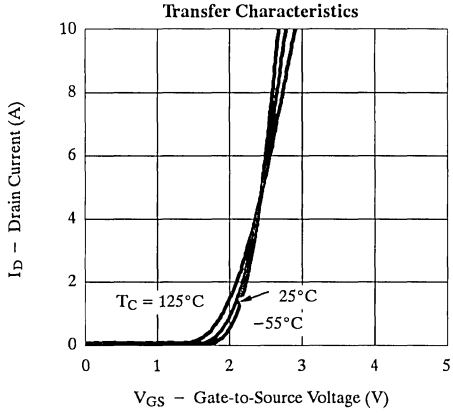
Notes
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

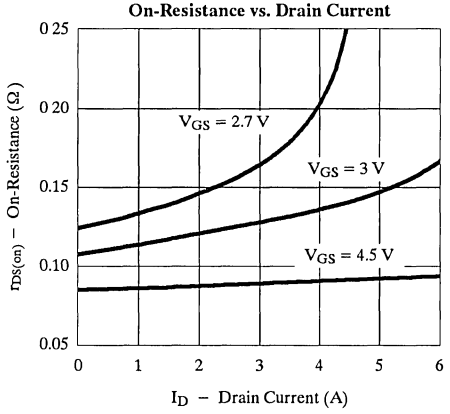
Output Characteristics



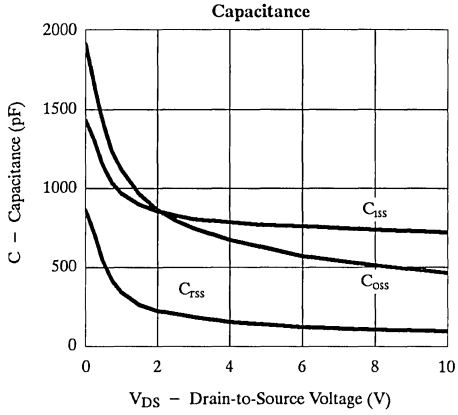
Transfer Characteristics



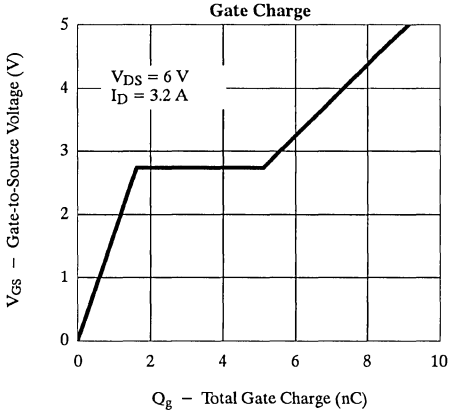
On-Resistance vs. Drain Current



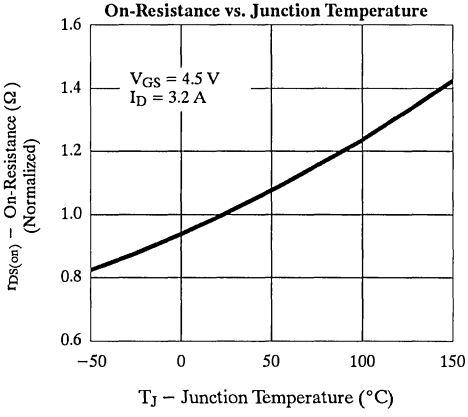
Capacitance



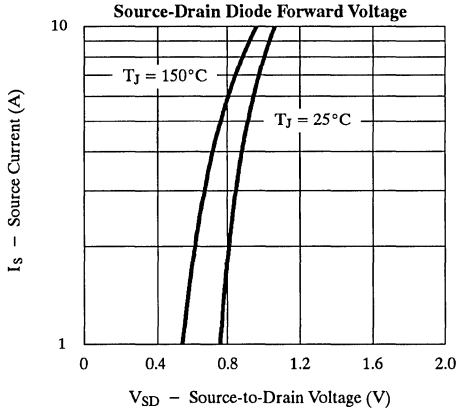
Gate Charge

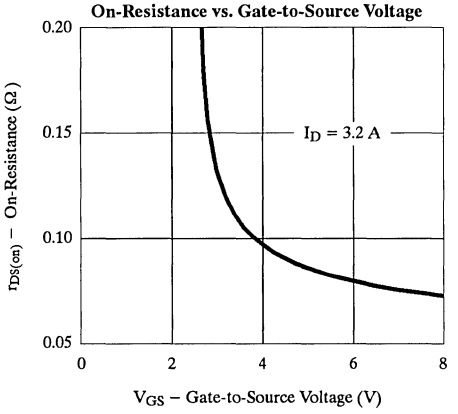


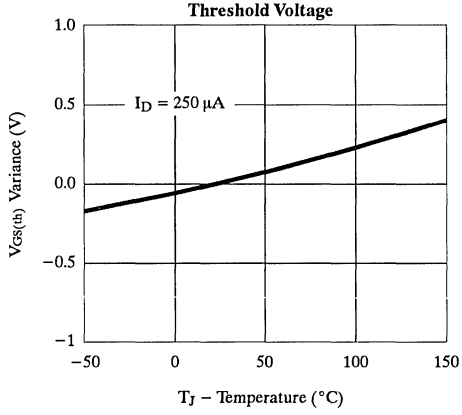
On-Resistance vs. Junction Temperature

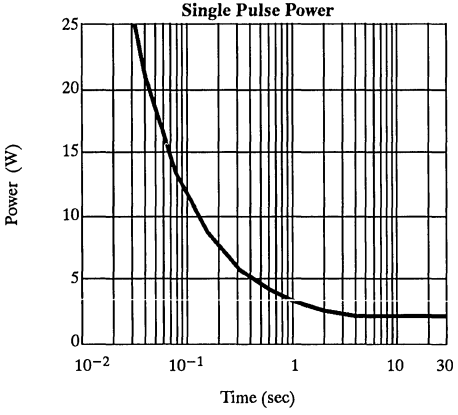


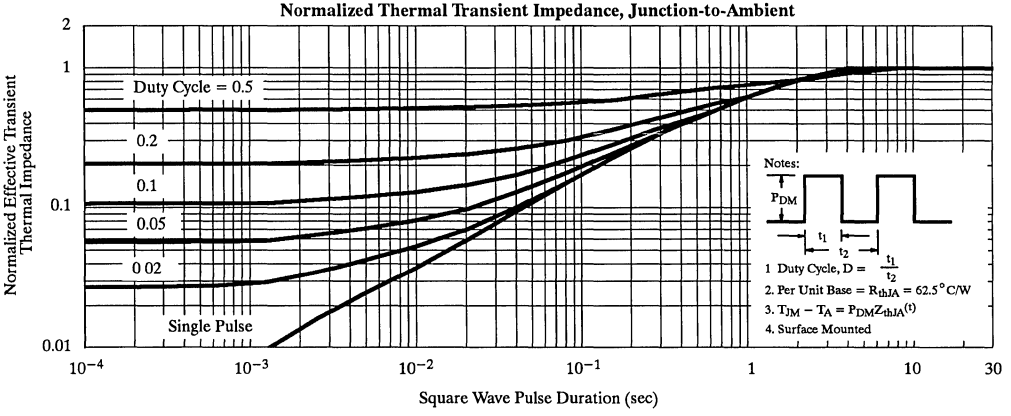
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

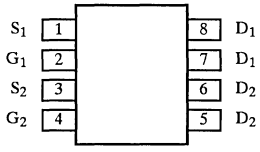
Si9936DY

Dual N-Channel Enhancement-Mode MOSFET

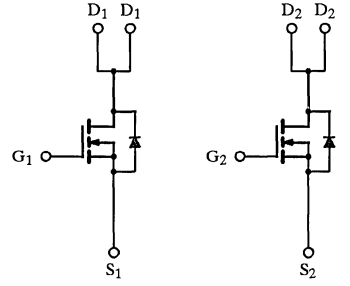
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.050 @ V_{GS} = 10 V	±5.0
	0.080 @ V_{GS} = 4.5 V	±3.9

SO-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.0	A
	T_A = 70°C		±4.0	
Pulsed Drain Current		I_{DM}	±40	
Continuous Source Current (Diode Conduction)		I_S	1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

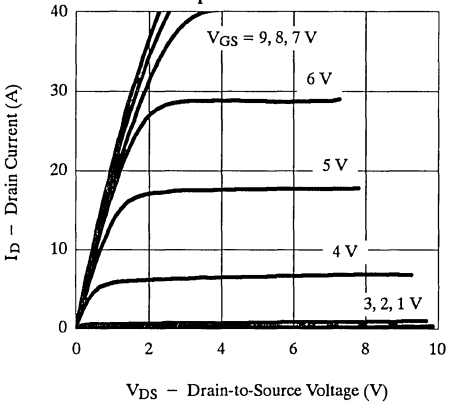
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			20	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5.0 A		0.04	0.050	Ω
		V_{GS} = 4.5 V, I_D = 3.9 A		0.06	0.080	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 5.0 A		8		S
Diode Forward Voltage[b]	V_{SD}	I_S =1.7 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 5.0 A		13	35	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		12	30	ns
Rise Time	t_r			10	25	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			10	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 5.0 A, di/dt = 100 A/µs		120	160	

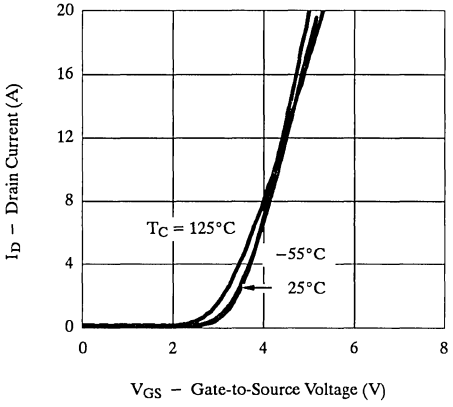
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

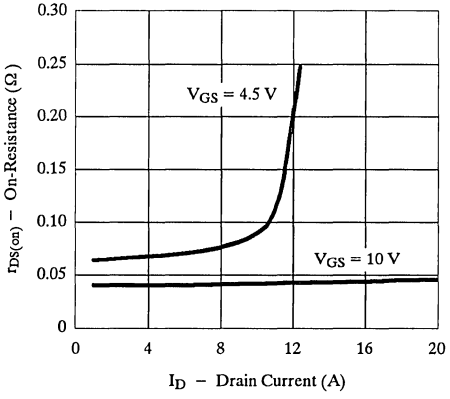
Output Characteristics



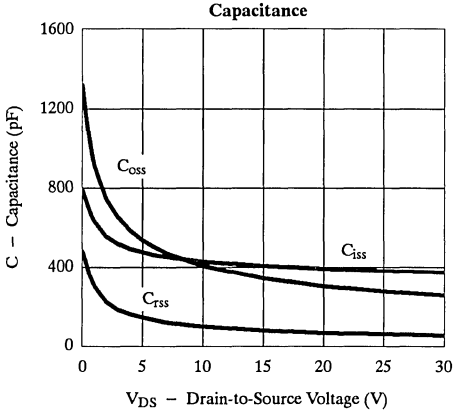
Transfer Characteristics



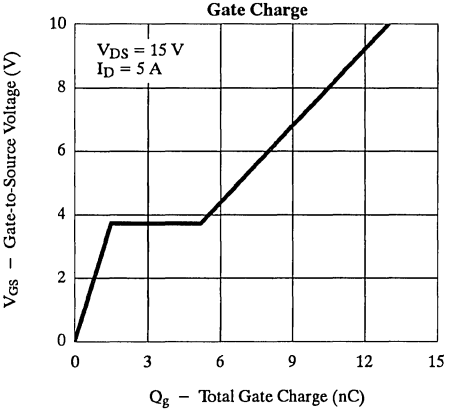
On-Resistance vs. Drain Current



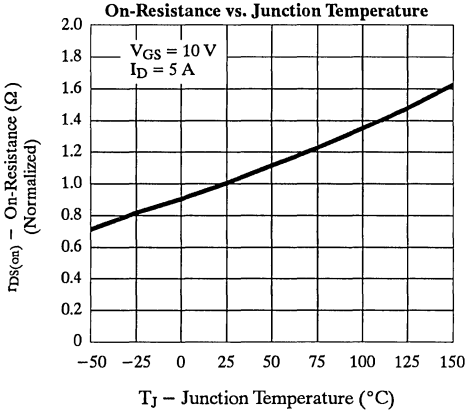
Capacitance



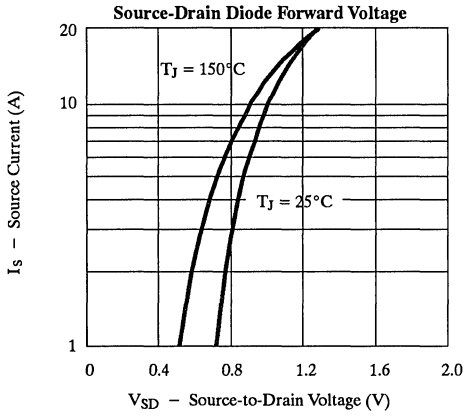
Gate Charge

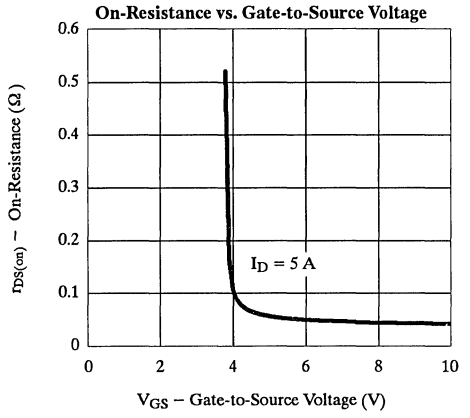


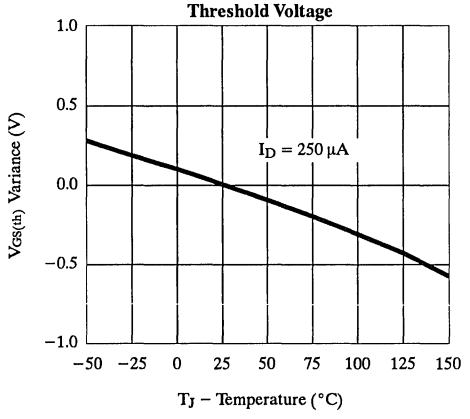
On-Resistance vs. Junction Temperature

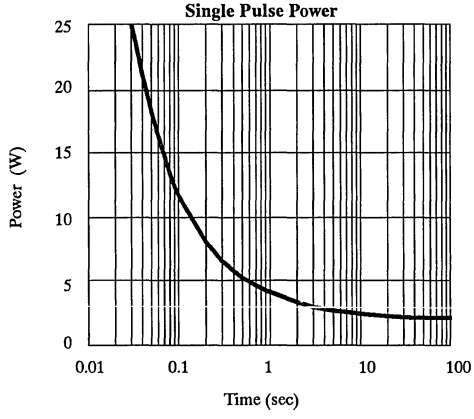


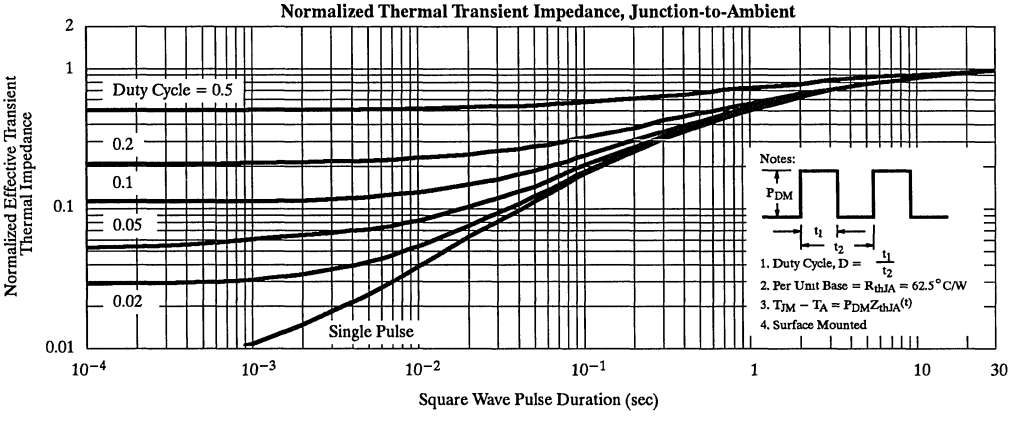
Typical Characteristics (25°C Unless Otherwise Noted)











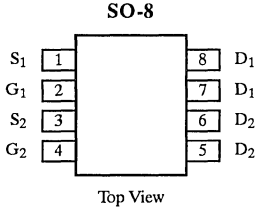
Siliconix

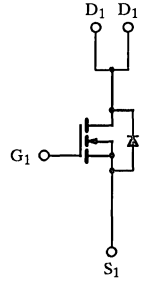
Si9939DY

Dual Enhancement-Mode MOSFETs (N- and P-Channel)

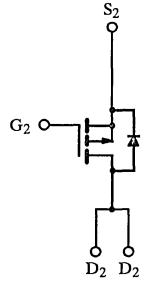
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	30	0.05 @ V_{GS} = 10 V	±3.5
		0.07 @ V_{GS} = 6 V	±3
		0.08 @ V_{GS} = 4.5 V	±2.5
P-Channel	−30	0.10 @ V_{GS} = −10 V	±3.5
		0.12 @ V_{GS} = −6V	±3
		0.16 @ V_{GS} = −4.5 V	±2.5





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	30	−30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.5	±3.5	A
	T_A = 70°C		±2.8	±2.8	
Pulsed Drain Current		I_{DM}	±14	±14	
Continuous Source Current (Diode Conduction)		I_S	1.7	−1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

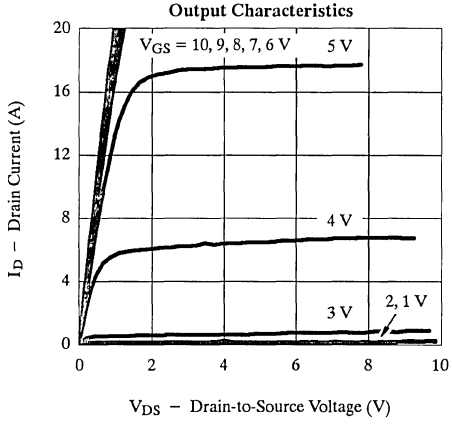
Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

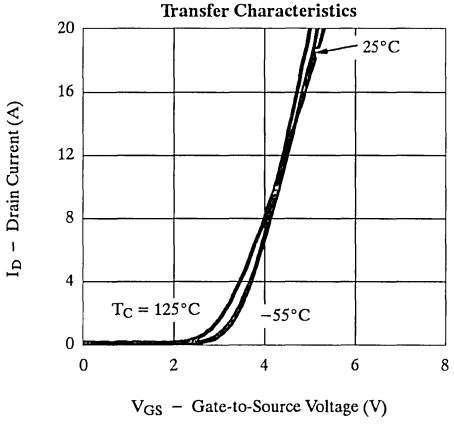
Specifications (T_J = 25°C Unless Otherwise Noted)

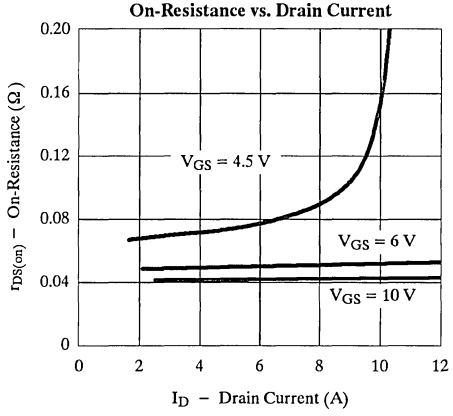
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = −24 V, V_{GS} = 0 V	P-Ch			−1	
		V_{DS} = 15 V, V_{GS} = 0 V, T_J = 70°C	N-Ch			5	
		V_{DS} = −15 V, V_{GS} = 0 V, T_J = 70°C	P-Ch			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	14			A
		V_{DS} ≤ −5 V, V_{GS} = −10 V	P-Ch	−14			
		V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	3.5			
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−2.5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.5 A	N-Ch		0.04	0.05	Ω
		V_{GS} = −10 V, I_D = 3.5 A	P-Ch		0.08	0.10	
		V_{GS} = 6 V, I_D = 3 A	N-Ch		0.05	0.07	
		V_{GS} = − 6 V, I_D = 3 A	P-Ch		0.10	0.12	
		V_{GS} = 4.5 V, I_D = 2.5 A	N-Ch		0.06	0.08	
		V_{GS} = −4.5 V, I_D = 2 A	P-Ch		0.13	0.16	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.5 A	N-Ch		8		S
		V_{DS} = −15 V, I_D = −3.5 A	P-Ch		5		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V	N-Ch		0.80	1.2	V
		I_S = −1.7 A, V_{GS} = 0 V	P-Ch		−0.80	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 10 V, I_D = 3.5 A P-Channel V_{DS} = −10 V, V_{GS} = −10 V I_D = −3.5 A	N-Ch		13	35	nC
			P-Ch		13	35	
Gate-Source Charge	Q_{gs}		N-Ch		2.1		
			P-Ch		2.8		
Gate-Drain Charge	Q_{gd}		N-Ch		5.3		
			P-Ch		4.1		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −15 V, R_L = 15 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		11	30	ns
			P-Ch		10	30	
Rise Time	t_r		N-Ch		17	40	
			P-Ch		21	40	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		26	50	
			P-Ch		24	50	
Fall Time	t_f		N-Ch		11	50	
			P-Ch		9	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 3.5 A, di/dt = 100 A/µs	N-Ch		70	120	
			P-Ch		40	100	

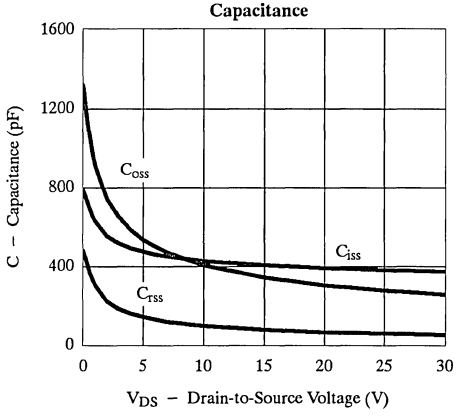
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

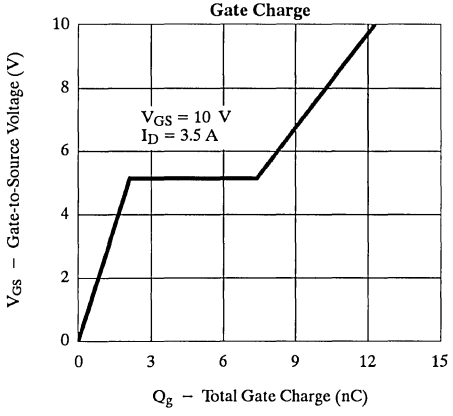
Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

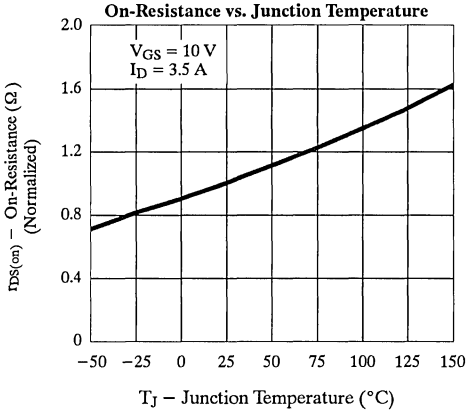






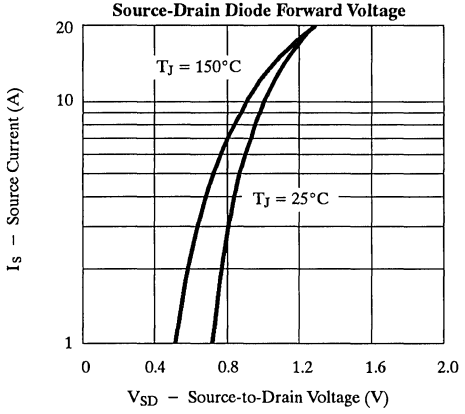




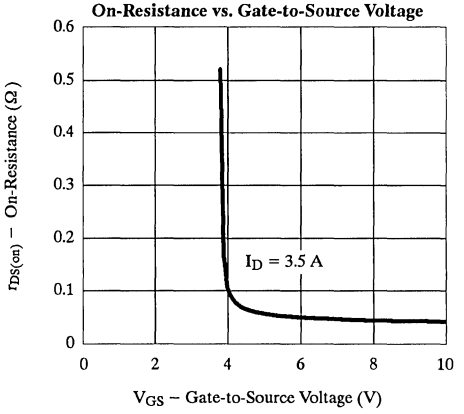


Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

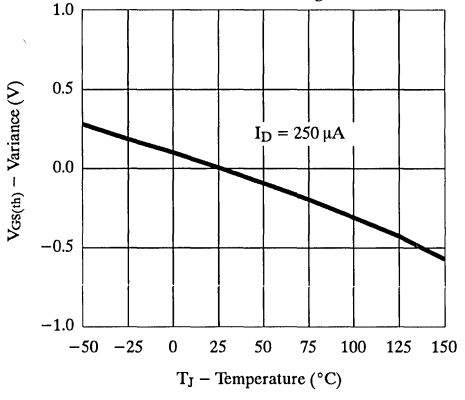
Source-Drain Diode Forward Voltage



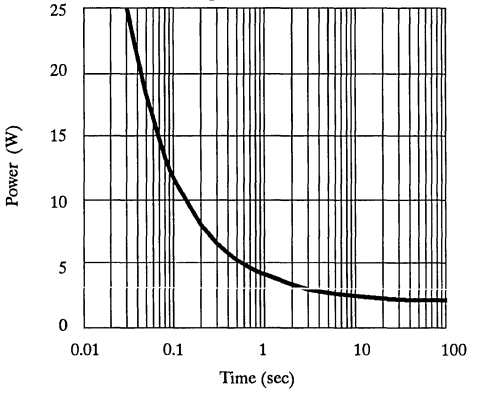
On-Resistance vs. Gate-to-Source Voltage



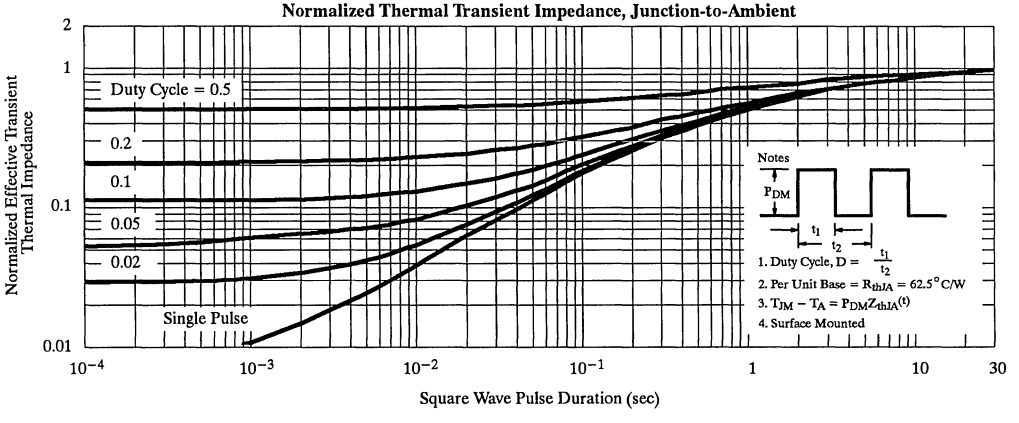
Threshold Voltage



Single Pulse Power

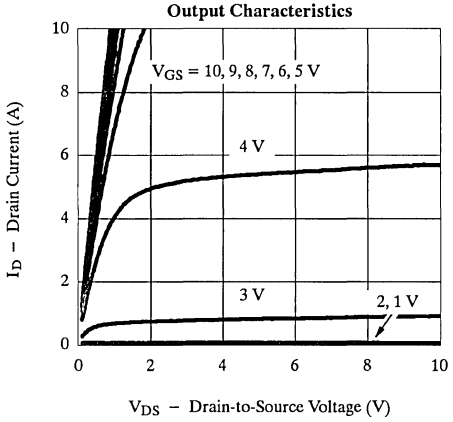


Normalized Thermal Transient Impedance, Junction-to-Ambient

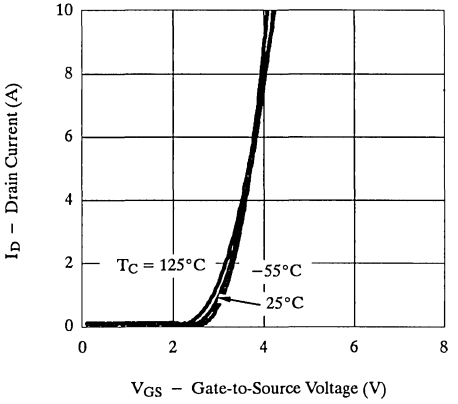


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

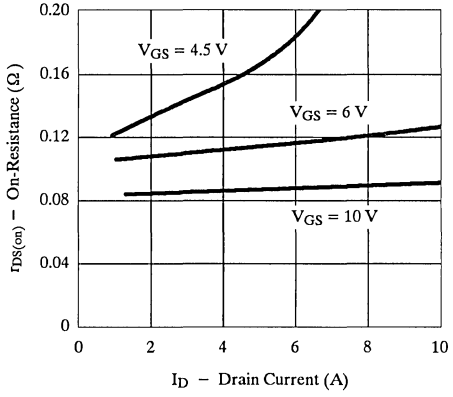
Output Characteristics



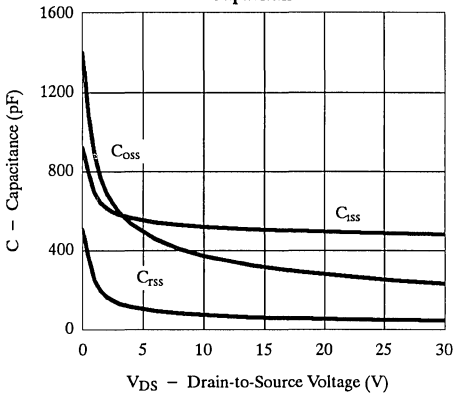
Transfer Characteristics



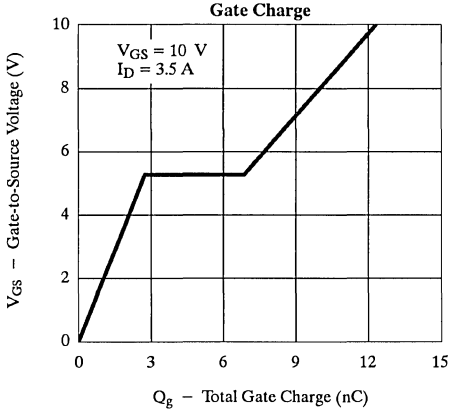
On-Resistance vs. Drain Current



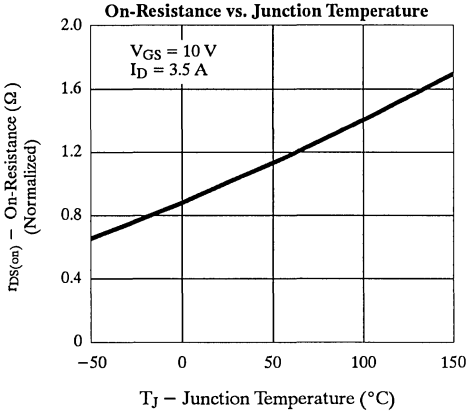
Capacitance



Gate Charge

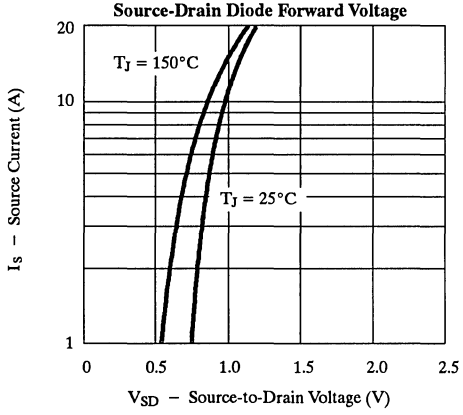


On-Resistance vs. Junction Temperature

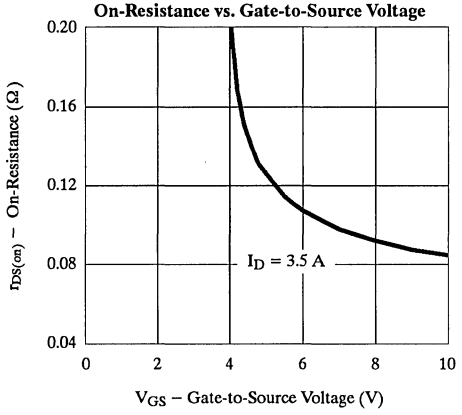


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

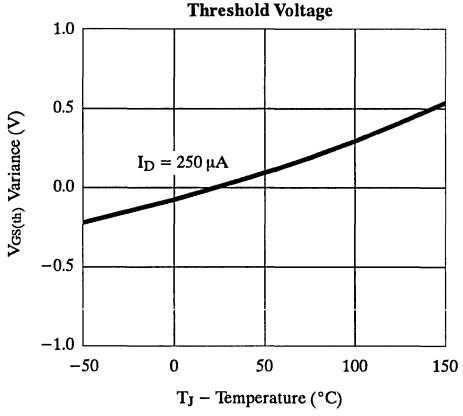
Source-Drain Diode Forward Voltage



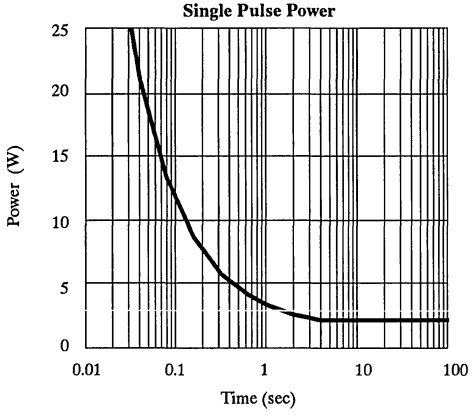
On-Resistance vs. Gate-to-Source Voltage



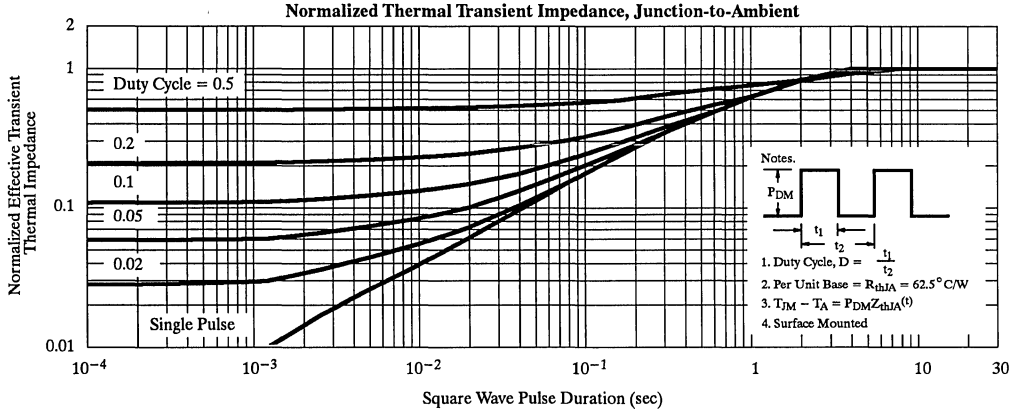
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

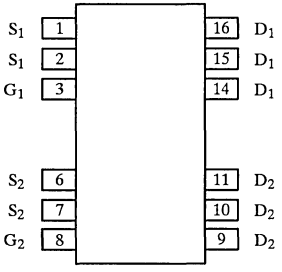
Si9940DY

Dual N-Channel Enhancement-Mode MOSFET

Product Summary

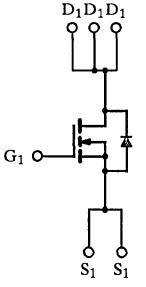
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.05 @ V_{GS} = 10 V	±5.3
	0.07 @ V_{GS} = 4.5 V	±4.5

SO-16*

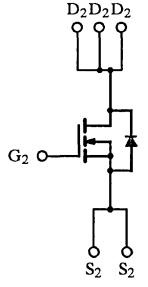


Top View

*Conforms to standard SO-16 dimensions



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±5.3	A
	T_A = 70°C		±4.2	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	2.5	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

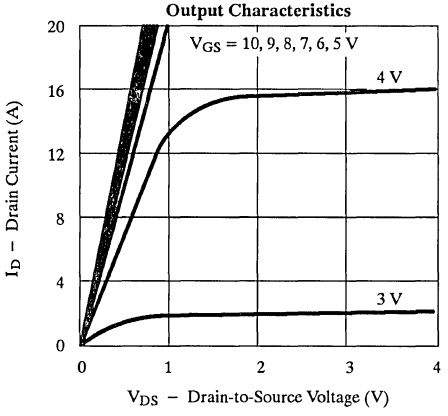
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	50	°C/W

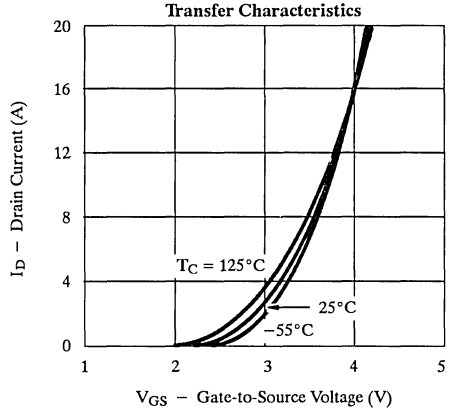
Specifications (T_J = 25°C Unless Otherwise Noted)

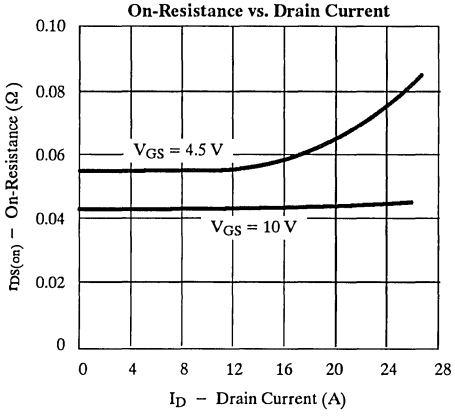
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5.3 A		0.042	0.05	Ω
		V_{GS} = 4.5 V, I_D = 4.5 A		0.055	0.07	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 5.3 A		11		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.5 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 2 A		30	50	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			9.4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		17	40	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			95	150	
Fall Time	t_f			55	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.5 A, di/dt = 100 A/µs		130		

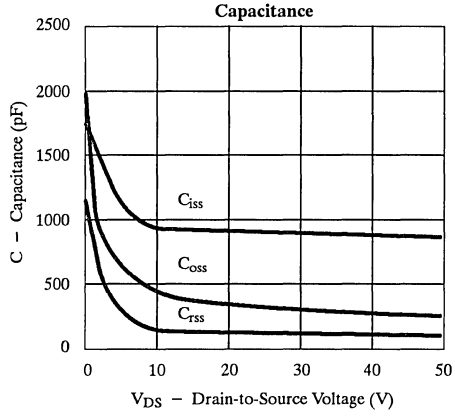
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

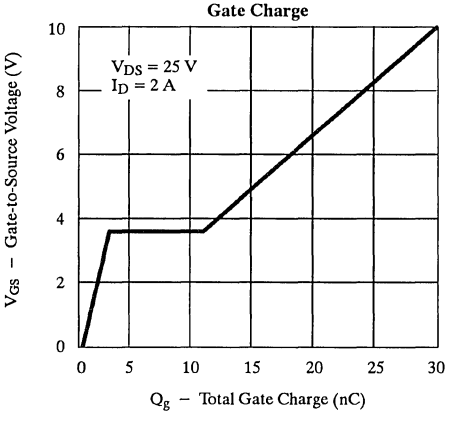
Typical Characteristics (25°C Unless Otherwise Noted)

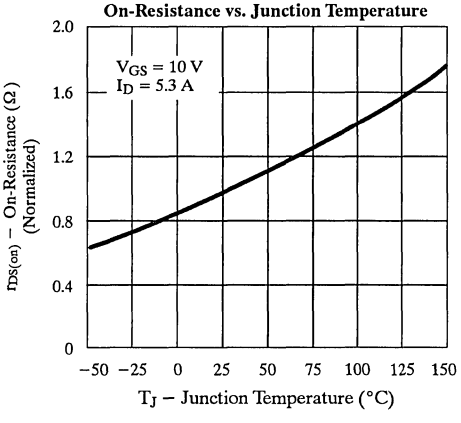






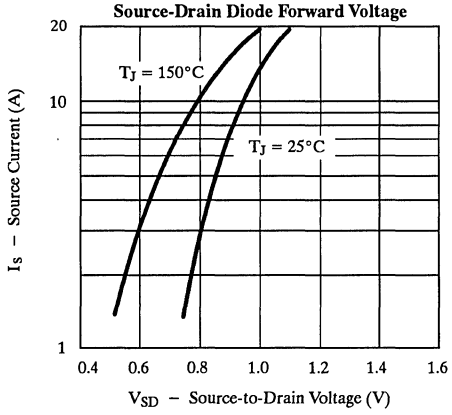




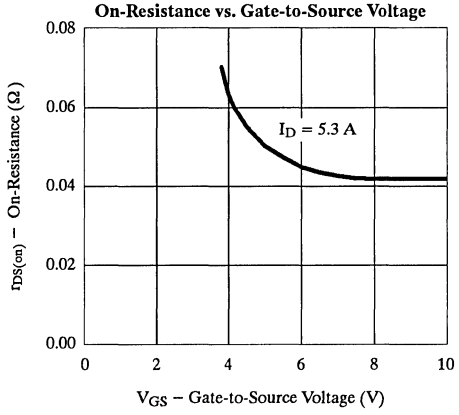


Typical Characteristics (25°C Unless Otherwise Noted)

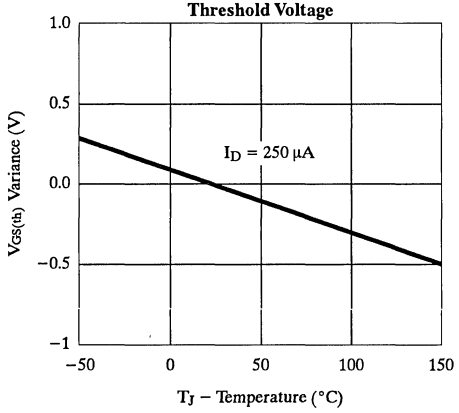
Source-Drain Diode Forward Voltage



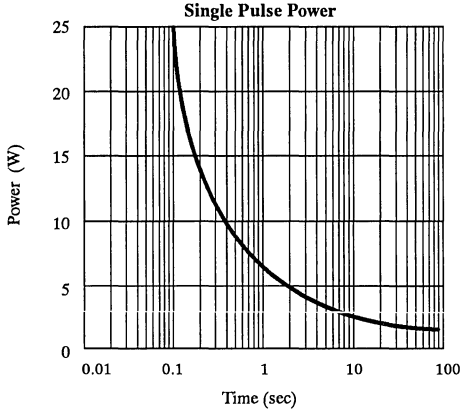
On-Resistance vs. Gate-to-Source Voltage



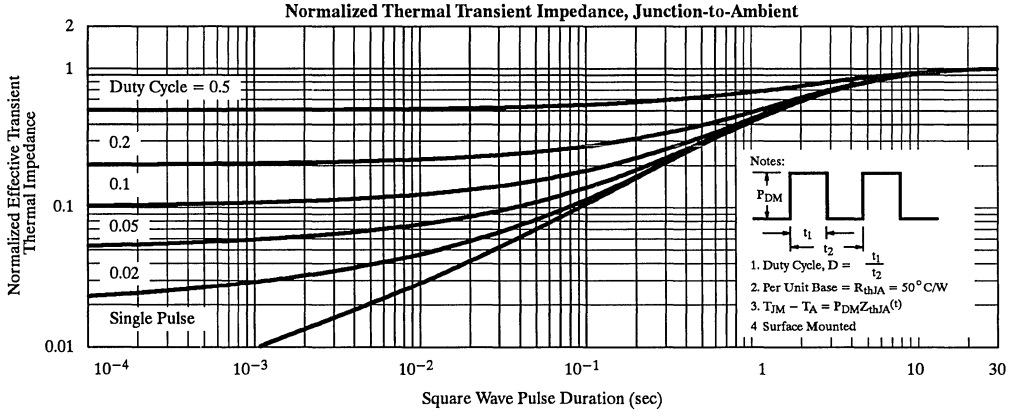
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

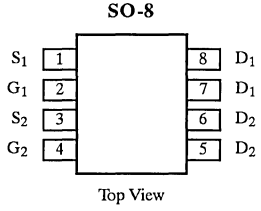
Si9942DY

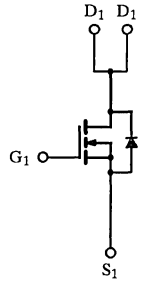
Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

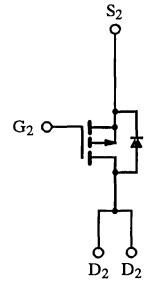
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.125 @ V_{GS} = 10 V	±3.0
		0.250 @ V_{GS} = 4.5 V	±2.0
P-Channel	−20	0.200 @ V_{GS} = −10 V	±2.5
		0.350 @ V_{GS} = −4.5 V	±2.0

Recommended upgrade: Si9939
Lower profile/smaller size—see LITE FOOT™ equivalent: Si6942DQ





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	−20	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.0	±2.5	A
	T_A = 70°C		±2.5	±2.0	
Pulsed Drain Current		I_{DM}	±10	±10	
Continuous Source Current (Diode Conduction)		I_S	1.6	−1.6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

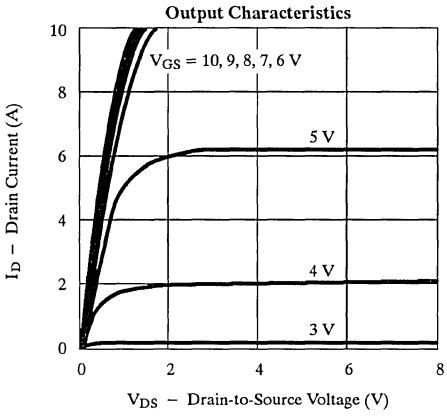
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

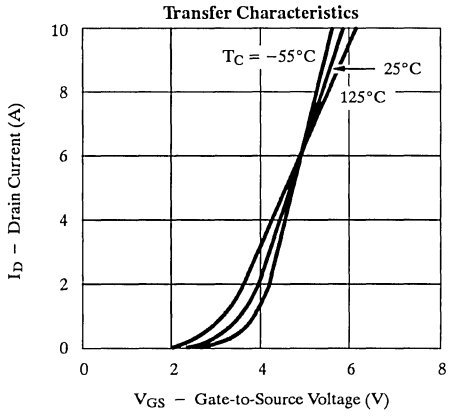
Specifications (T_J = 25°C Unless Otherwise Noted)

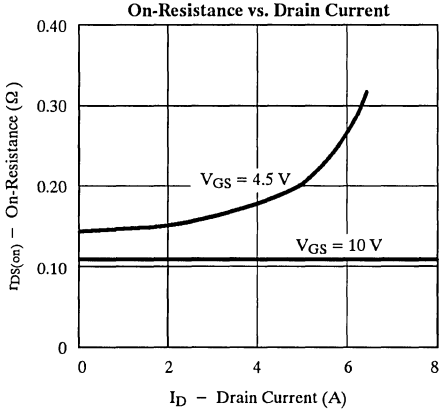
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = −16 V, V_{GS} = 0 V	P-Ch			−2	
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	10			A
		V_{DS} ≤ −5 V, V_{GS} = −10 V	P-Ch	−10			
		V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	2			
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−2			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.0 A	N-Ch		0.11	0 125	Ω
		V_{GS} = −10 V, I_D = 1.0 A	P-Ch		0.16	0.200	
		V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch		0.15	0.250	
		V_{GS} = −4.5 V, I_D = 0.5 A	P-Ch		0.30	0.350	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.0 A	N-Ch		3.7		S
		V_{DS} = −15 V, I_D = −3.0 A	P-Ch		3 0		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V	N-Ch		0.9	1.2	V
		I_S = −1.25 A, V_{GS} = 0 V	P-Ch		−0.9	−1.6	
Dynamic[a]							
Total Gate Charge	Q_g	N Channel V_{DS} = 10 V, V_{GS} = 10 V, I_D = 2.3 A P-Channel V_{DS} = −10 V, V_{GS} = −10 V, I_D = −2.3 A	N-Ch		5.2	25	nC
			P-Ch		5.4	25	
Gate-Source Charge	Q_{gs}		N-Ch		0.8		
			P-Ch		0.9		
Gate-Drain Charge	Q_{gd}		N-Ch		2.0		
			P-Ch		1.4		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 20 V, R_L = 20 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −20 V, R_L = 20 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		5	15	ns
			P-Ch		10	40	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		10	40	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		25	50	
			P-Ch		38	90	
Fall Time	t_f		N-Ch		22	50	
			P-Ch		27	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs	N-Ch		69	100	
			P-Ch		69	100	

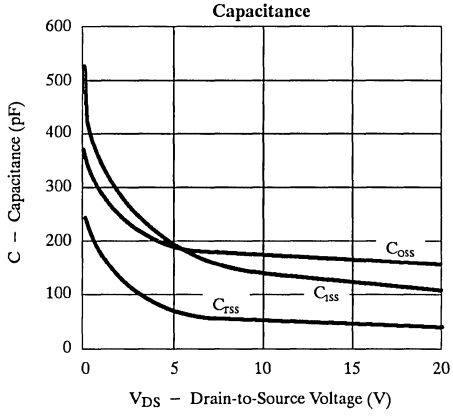
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

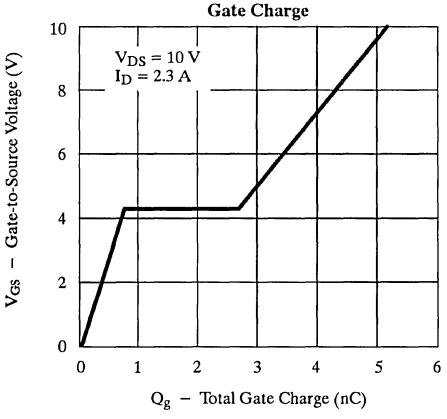
Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

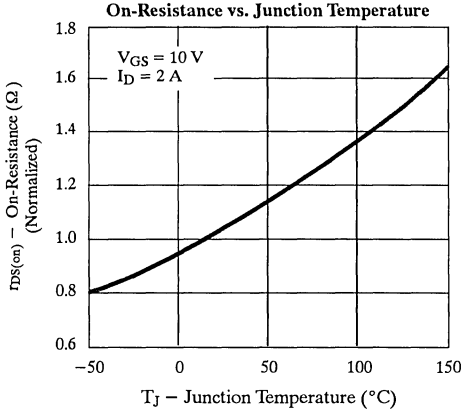








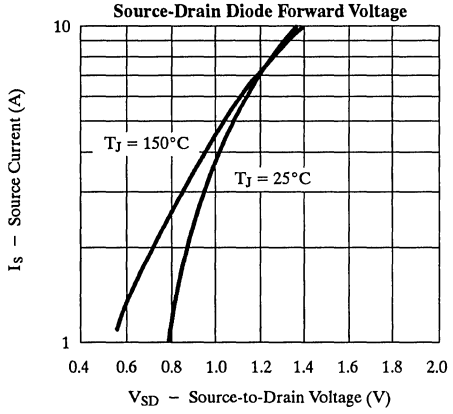




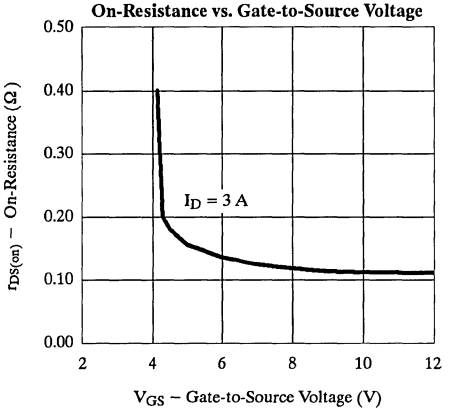
Typical Characteristics (25°C Unless Otherwise Noted)

N-Channel

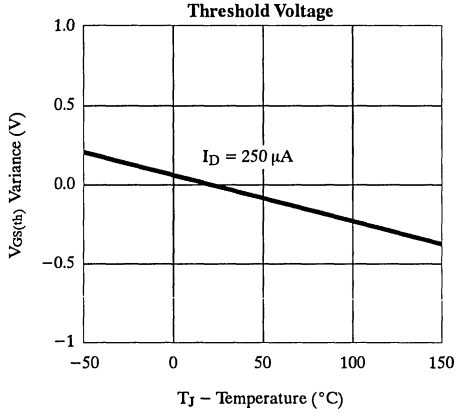
Source-Drain Diode Forward Voltage



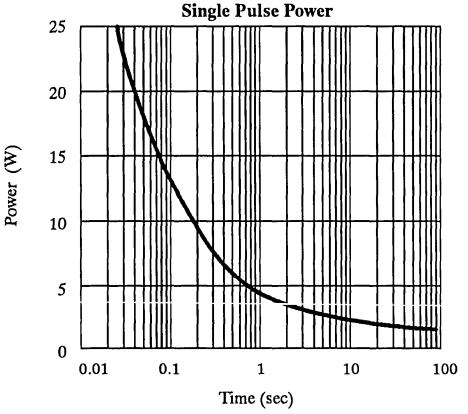
On-Resistance vs. Gate-to-Source Voltage



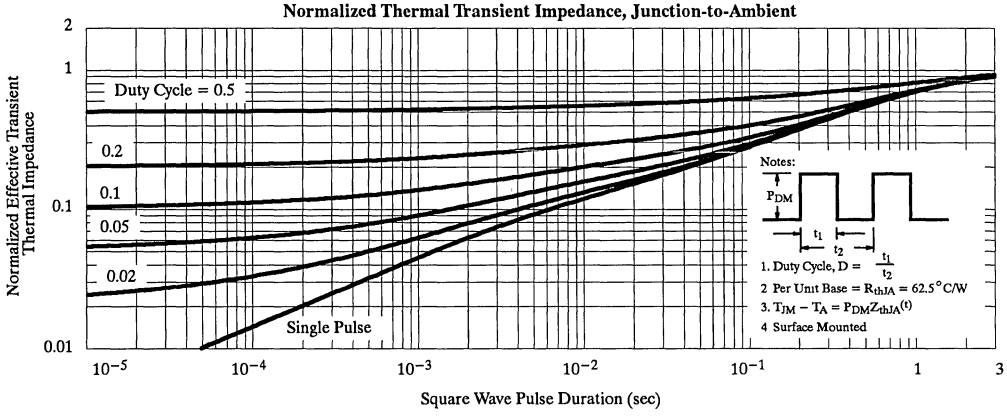
Threshold Voltage



Single Pulse Power

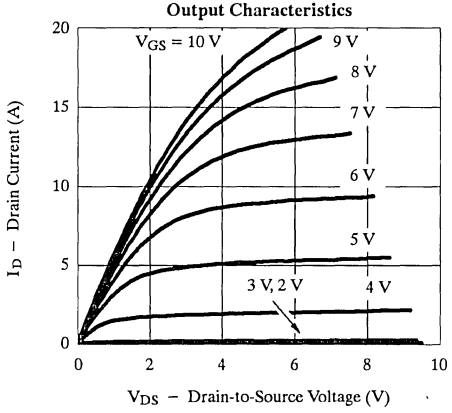


Normalized Thermal Transient Impedance, Junction-to-Ambient

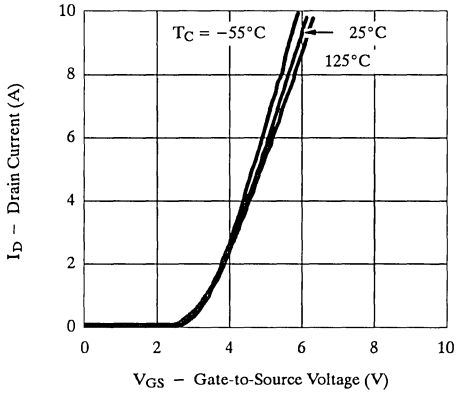


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

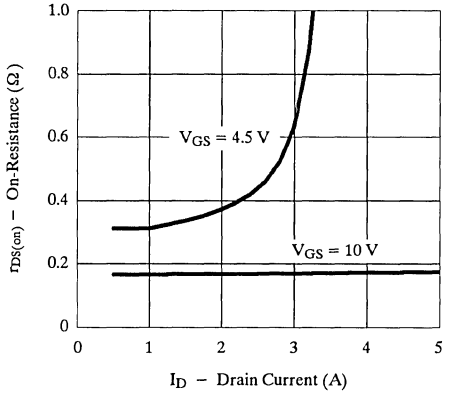
Output Characteristics



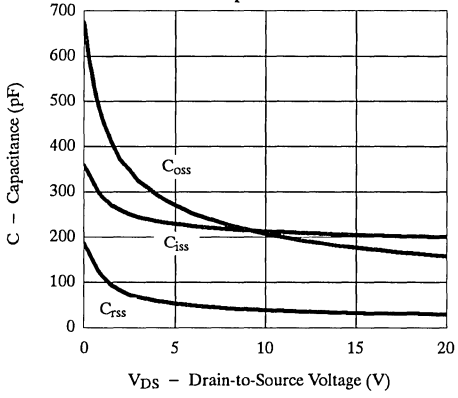
Transfer Characteristics



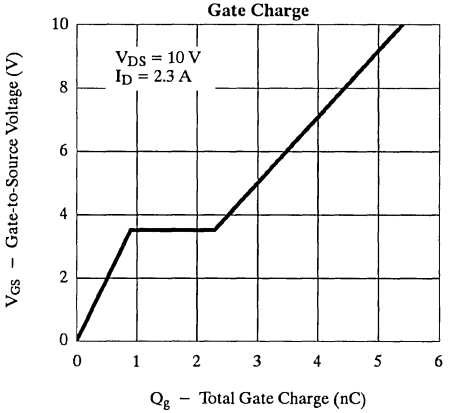
On-Resistance vs. Drain Current



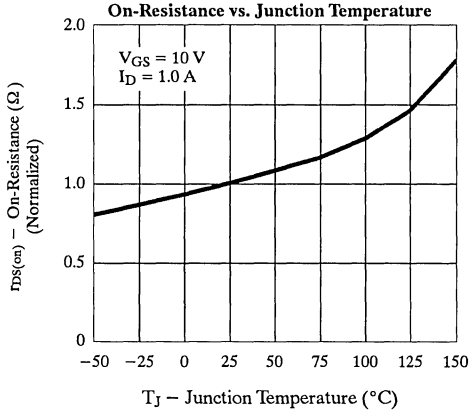
Capacitance



Gate Charge



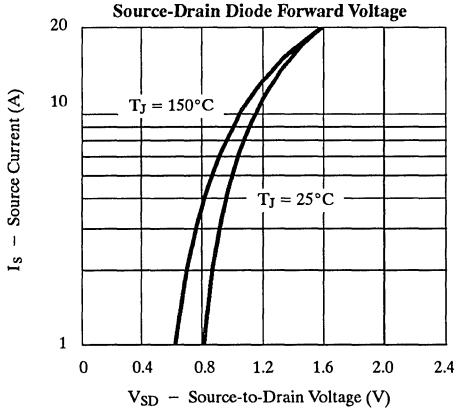
On-Resistance vs. Junction Temperature

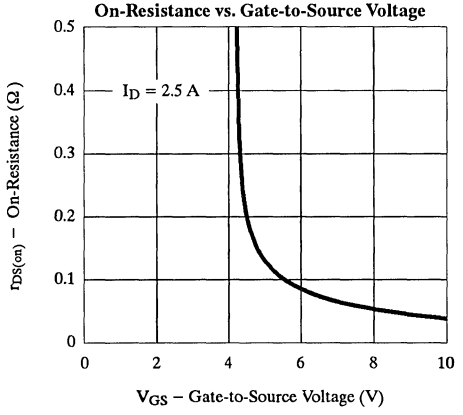


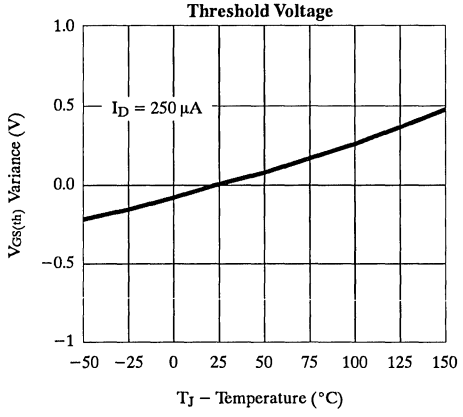
1 LITTLE FOOT

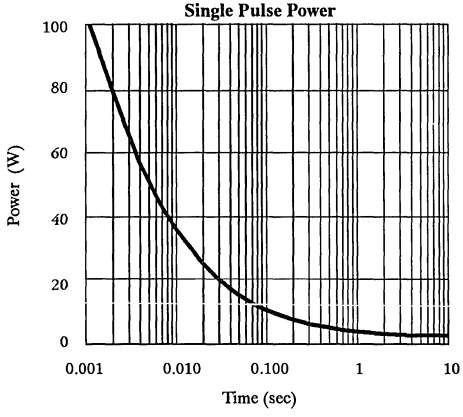
Typical Characteristics (25°C Unless Otherwise Noted)

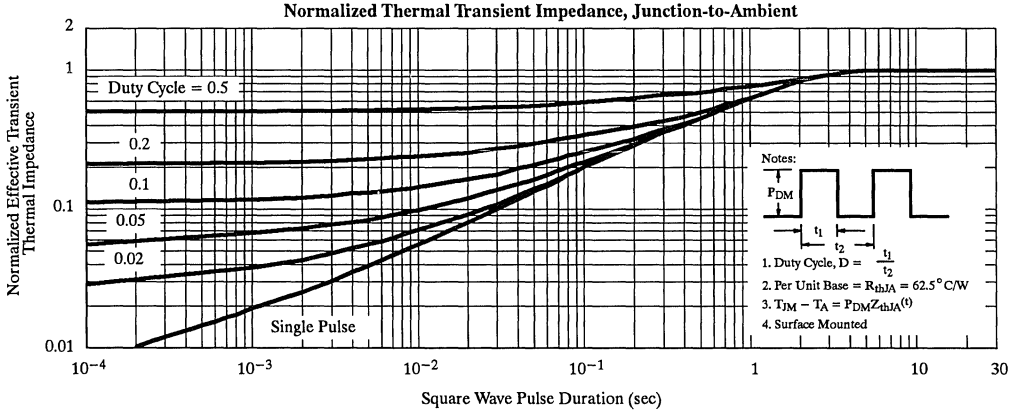
P-Channel







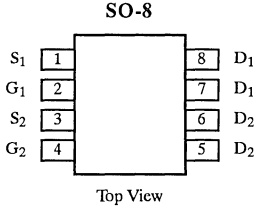


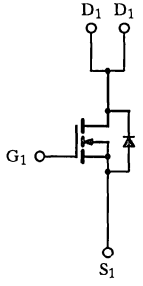


Dual Enhancement-Mode MOSFET (N- and P-Channel)

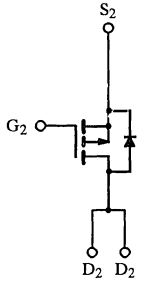
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.125 @ V_{GS} = 10 V	±3.0
		0.250 @ V_{GS} = 4.5 V	±2.0
P-Channel	−20	0.160 @ V_{GS} = −10 V	±2.8
		0.300 @ V_{GS} = −4.5 V	±2.0





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	−20	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.0	±2.8	A
	T_A = 70°C		±2.5	±2.3	
Pulsed Drain Current		I_{DM}	±10	±10	
Continuous Source Current (Diode Conduction)		I_S	1.6	−1.6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

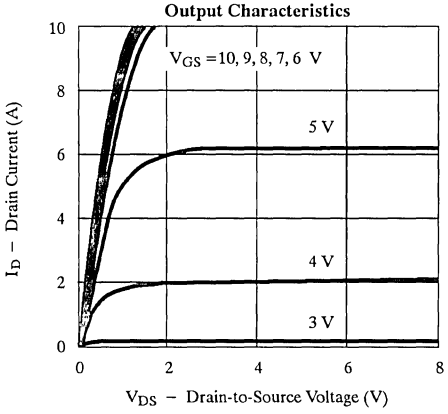
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

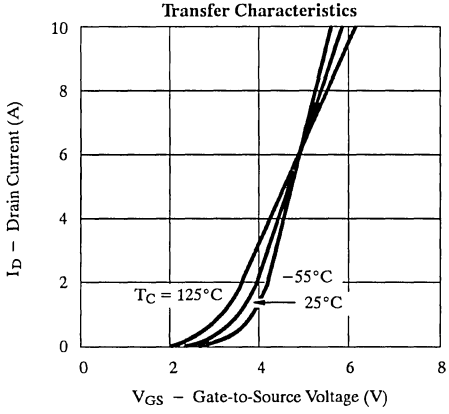
Specifications (T_J = 25°C Unless Otherwise Noted)

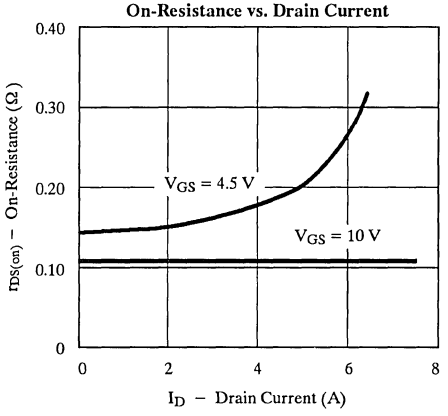
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = −16 V, V_{GS} = 0 V	P-Ch			−2	
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	10			A
		V_{DS} ≤ −5 V, V_{GS} = −10 V	P-Ch	−10			
		V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	2			
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−2			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.0 A	N-Ch		0.100	0.125	Ω
		V_{GS} = −10 V, I_D = 3.0 A	P-Ch	0.100	0.130	0.160	
		V_{GS} = 6 V, I_D = 2.0 A	N-Ch		0.120	0.160	
		V_{GS} = − 6 V, I_D = 2.0 A	P-Ch	0.120	0.160	0.200	
		V_{GS} = 4.5 V, I_D = 1.5 A	N-Ch		0.160	0.250	
		V_{GS} = −4.5 V, I_D = 1.5 A	P-Ch		0.20	0.300	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.0 A	N-Ch		3.7		S
		V_{DS} = −15 V, I_D = −3.0 A	P-Ch		3.0		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V	N-Ch		0.9	1.2	V
		I_S = −1.25 A, V_{GS} = 0 V	P-Ch		−1.4	−1.6	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 10 V, I_D = 2.3 A P-Channel V_{DS} = −10 V, V_{GS} = −10 V, I_D = −2.3 A	N-Ch		5.2	25	nC
			P-Ch		9.4	25	
Gate-Source Charge	Q_{gs}		N-Ch		0.8		
			P-Ch		1.3		
Gate-Drain Charge	Q_{gd}		N-Ch		2.0		
			P-Ch		2.0		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 20 V, R_L = 20 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −20 V, R_L = 20 Ω, I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		5	15	ns
			P-Ch		12	40	
Rise Time	t_r		N-Ch		10	20	
			P-Ch		19	40	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		25	50	
			P-Ch		42	90	
Fall Time	t_f		N-Ch		22	50	
			P-Ch		27	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs	N-Ch		69	100	
			P-Ch		69	100	

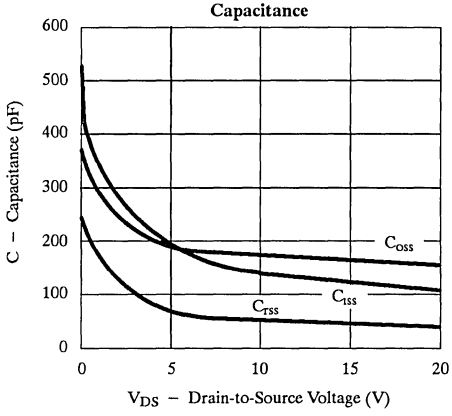
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

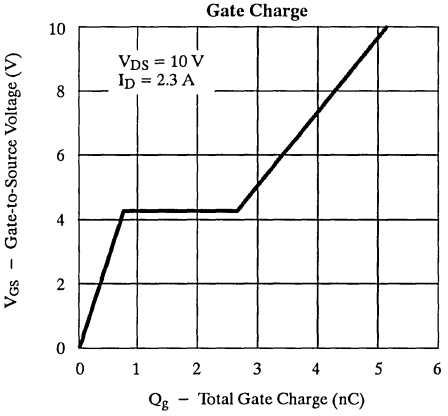
Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

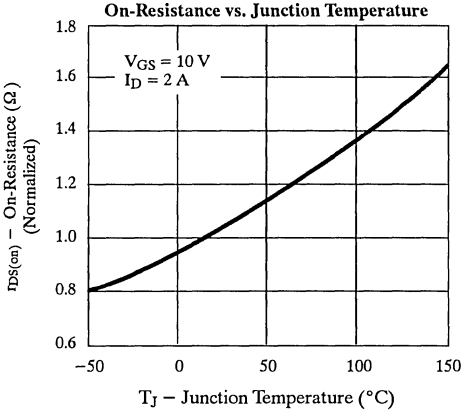






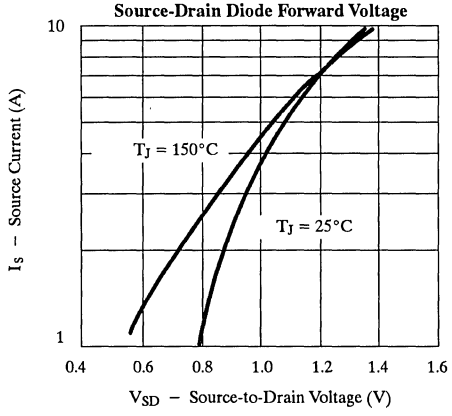




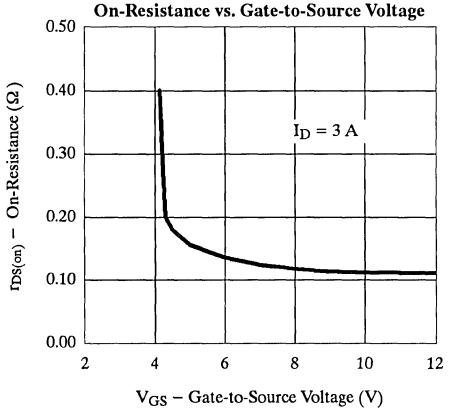


Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

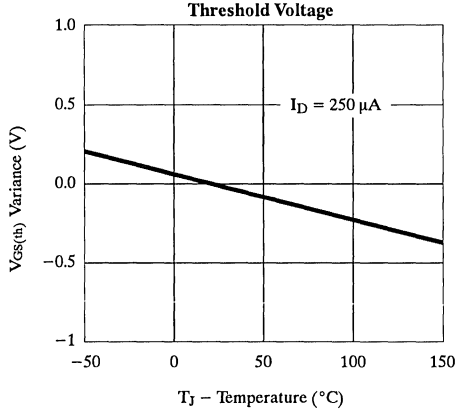
Source-Drain Diode Forward Voltage



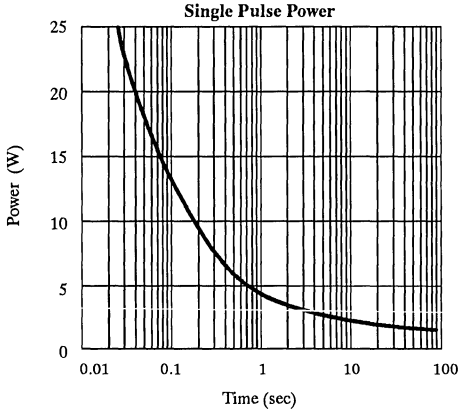
On-Resistance vs. Gate-to-Source Voltage



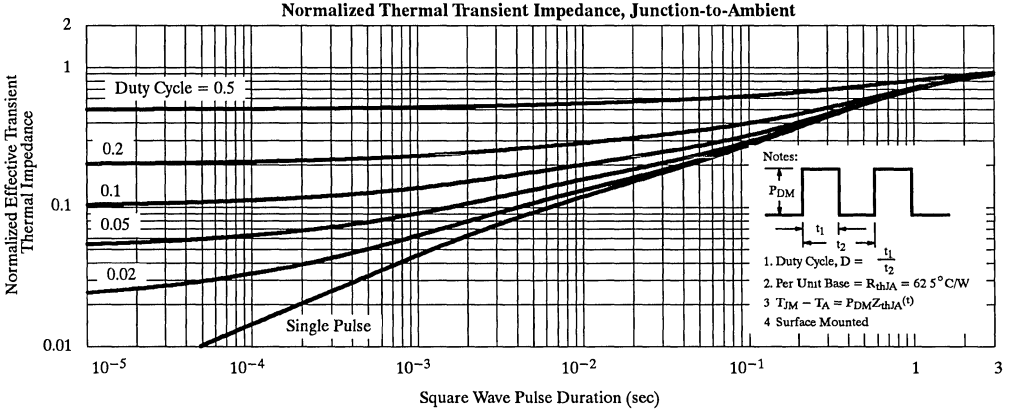
Threshold Voltage



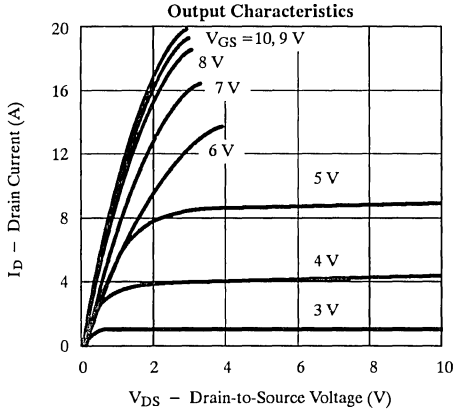
Single Pulse Power

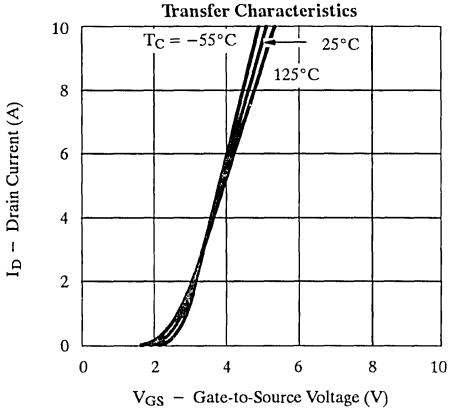


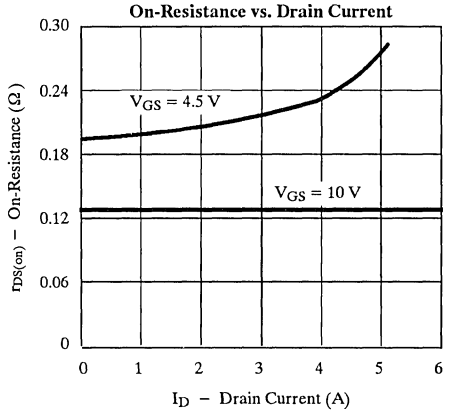
Normalized Thermal Transient Impedance, Junction-to-Ambient

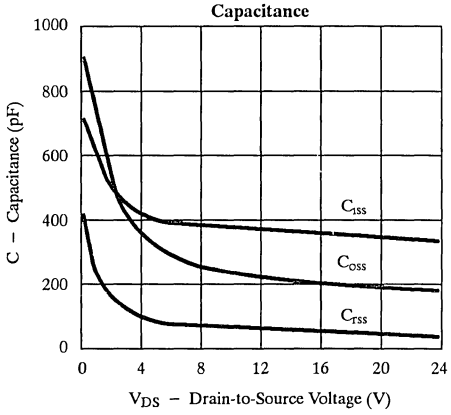


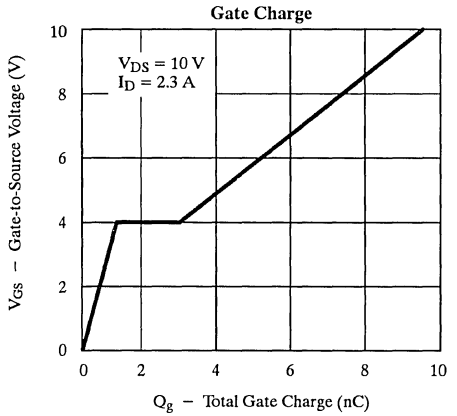
Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

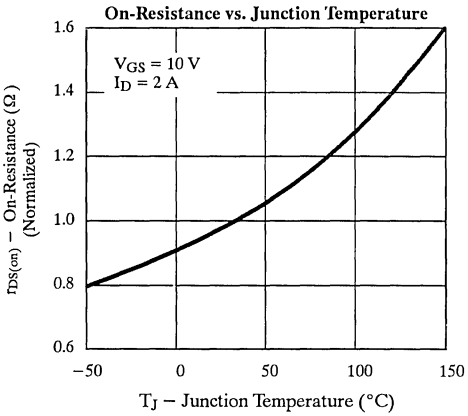








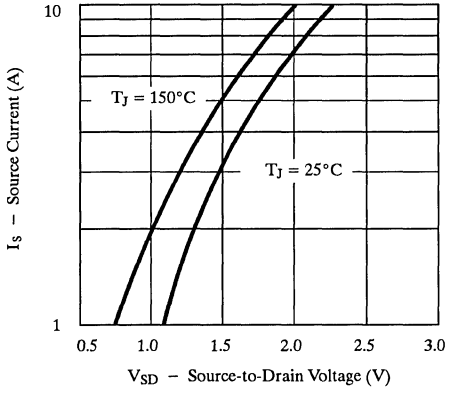




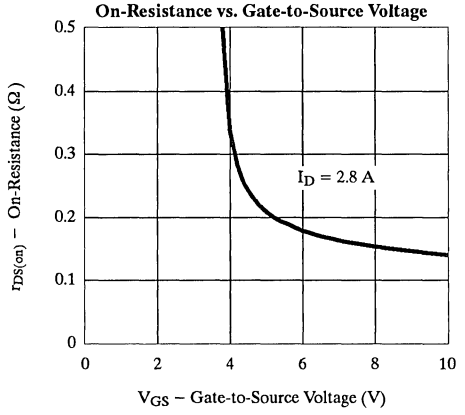
Typical Characteristics (25°C Unless Otherwise Noted)

P-Channel

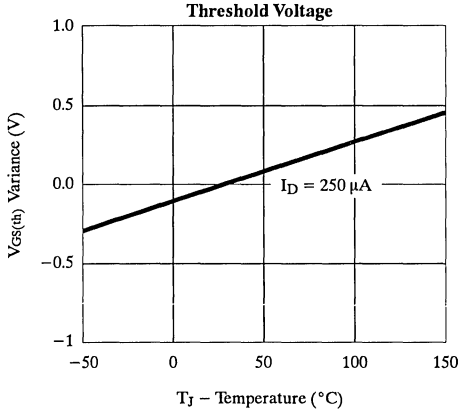
Source-Drain Diode Forward Voltage



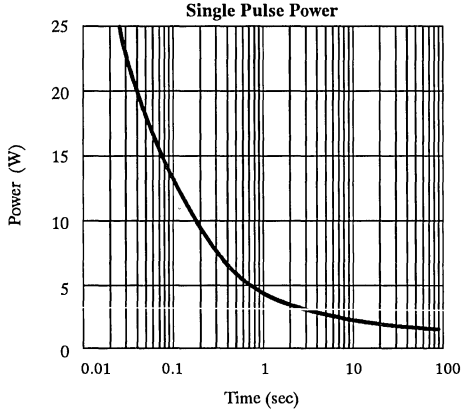
On-Resistance vs. Gate-to-Source Voltage



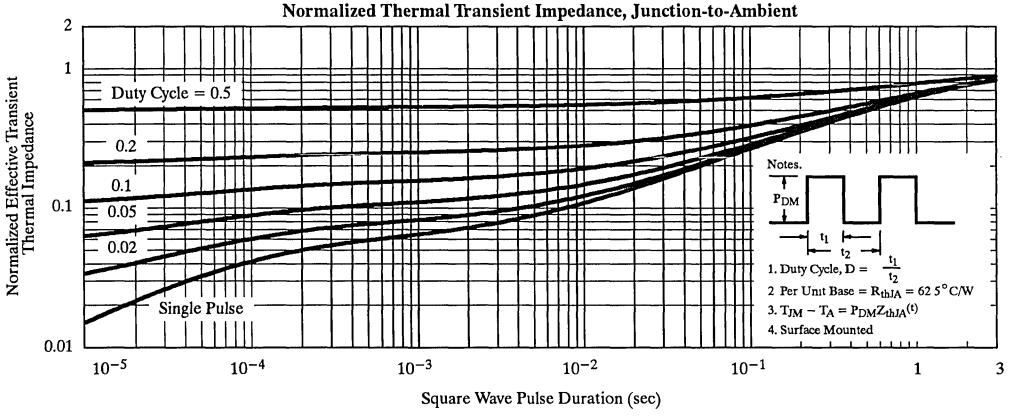
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

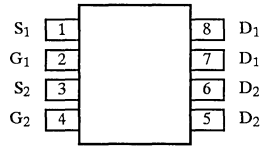
Si9944DY

Dual N-Channel Enhancement-Mode MOSFET

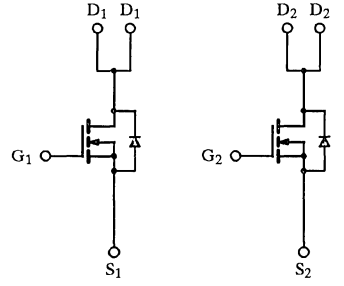
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
240	6 @ V_{GS} = 10 V	±0.4
	8 @ V_{GS} = 4.5 V	±0.3

SO-8



Top View



N-Channel MOSFET N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	240	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±0.4	A
	T_A = 70°C		±0.3	
Pulsed Drain Current		I_{DM}	±1.8	
Continuous Source Current (Diode Conduction)		I_S	0 4	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

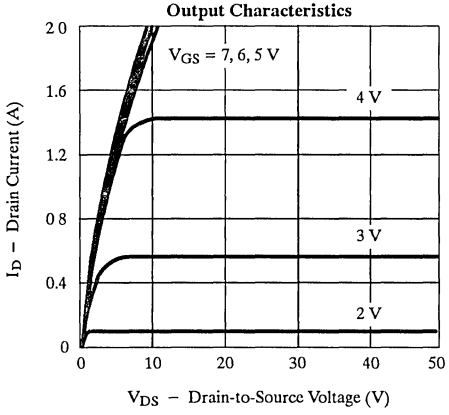
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.5			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 190 V, V_{GS} = 0 V			1	µA
		V_{DS} = 190 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 25 V, V_{GS} = 10 V	1.8			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.4 A		2.8	6	Ω
		V_{GS} = 4.5 V, I_D = 0.3 A		3.1	8	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 0.4 A		0.6		S
Diode Forward Voltage[b]	V_{SD}	I_S =0.4 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 60 V, V_{GS} = 10 V, I_D = 0.4 A		4.6	6.0	nC
Gate-Source Charge	Q_{gs}			0.17		
Gate-Drain Charge	Q_{gd}			1.75		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 60 V, R_L = 150 Ω I_D ≃ 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω		5	10	ns
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			14	20	

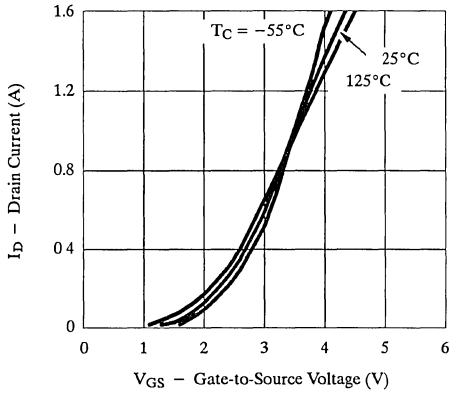
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

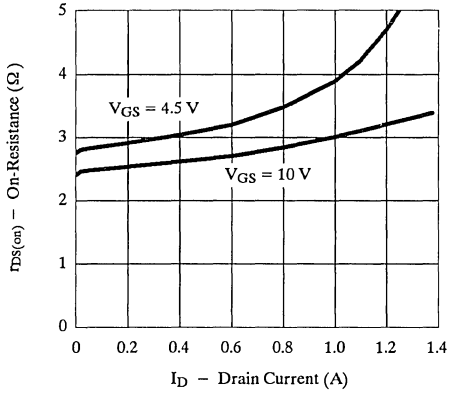
Output Characteristics



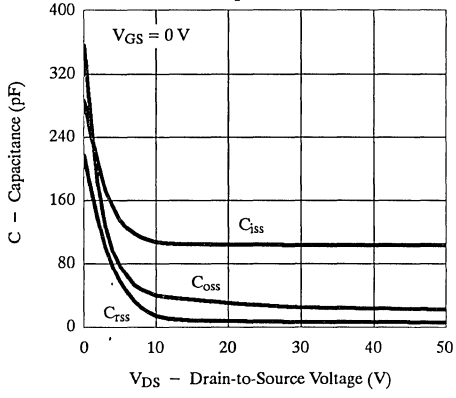
Transfer Characteristics



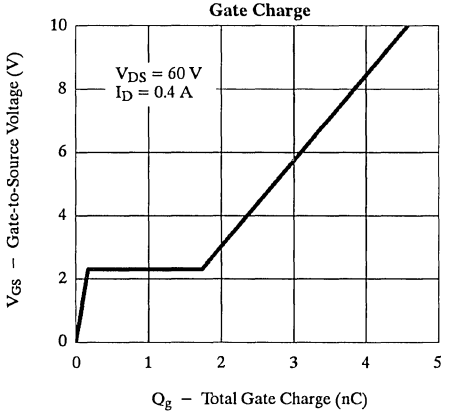
On-Resistance vs. Drain Current



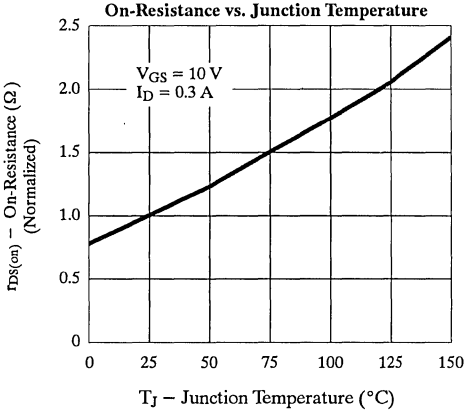
Capacitance



Gate Charge

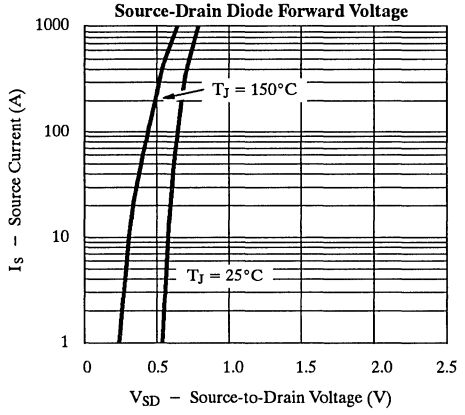


On-Resistance vs. Junction Temperature

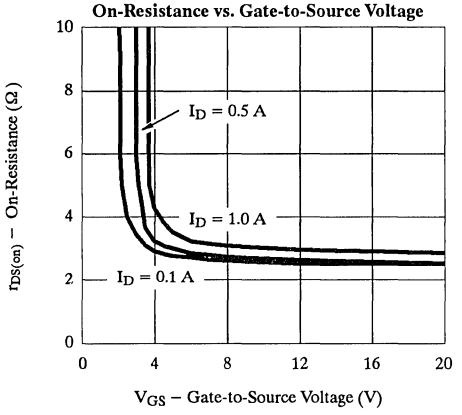


Typical Characteristics (25°C Unless Otherwise Noted)

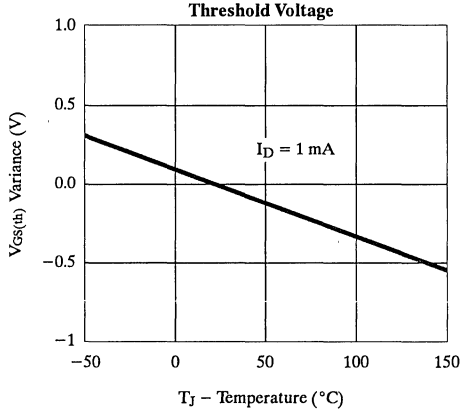
Source-Drain Diode Forward Voltage



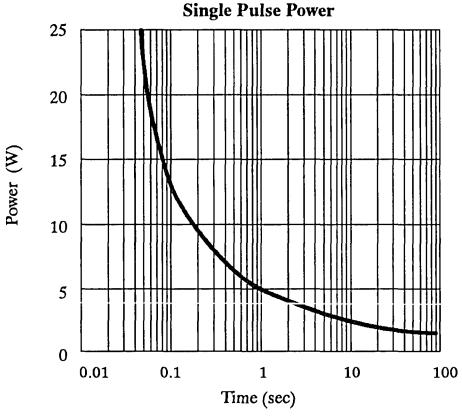
On-Resistance vs. Gate-to-Source Voltage



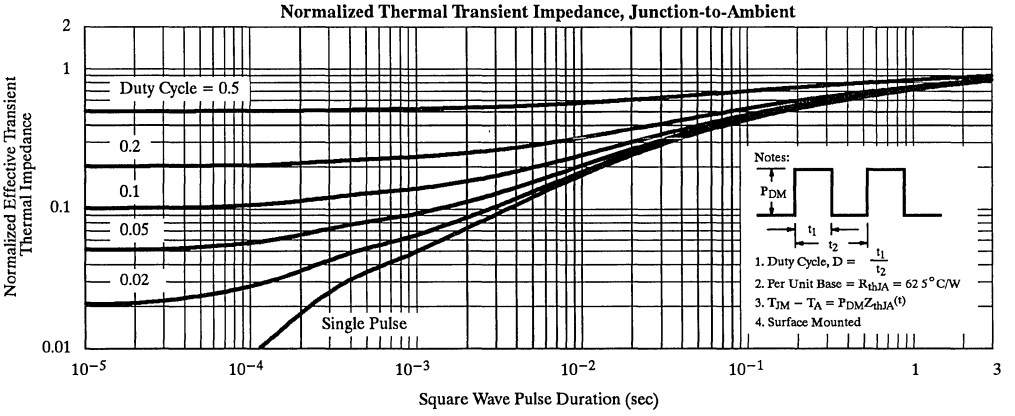
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

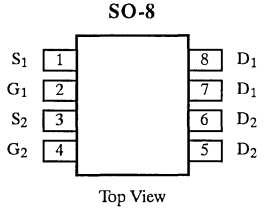


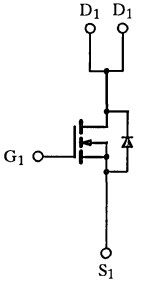
Si9945DY

Dual N-Channel Enhancement-Mode MOSFET

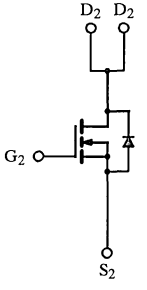
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.10 @ V_{GS} = 10 V	±3.3
	0.20 @ V_{GS} = 4.5 V	±2.5





N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.3	A
	T_A = 70°C		±2.6	
Pulsed Drain Current		I_{DM}	10	
Continuous Source Current (Diode Conduction)		I_S	1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

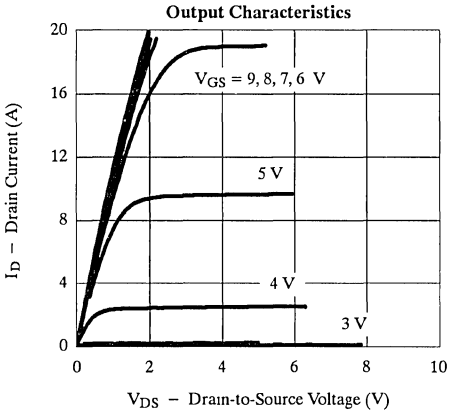
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

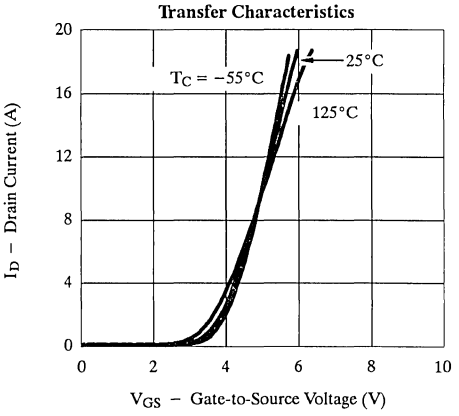
Specifications (T_J = 25°C Unless Otherwise Noted)

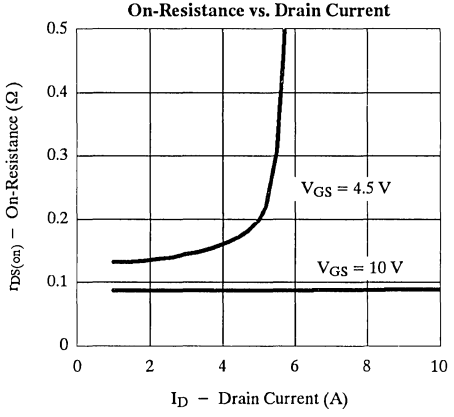
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.3 A			0.10	Ω
		V_{GS} = 4.5 V, I_D = 2.5 A			0.20	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.3 A		7.0		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 3.3 A		15	30	nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			4.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		9	25	ns
Rise Time	t_r			10	30	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			14	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/µs		70	100	

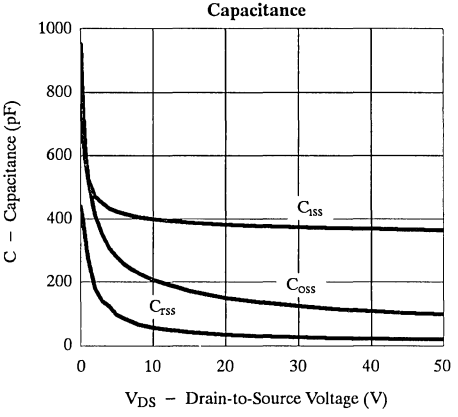
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

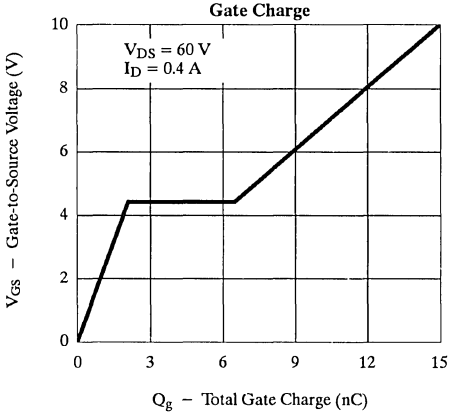
Typical Characteristics (25°C Unless Otherwise Noted)

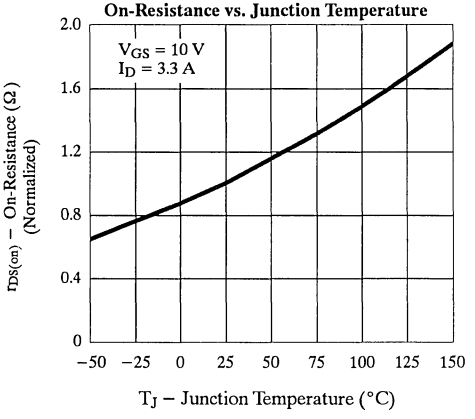






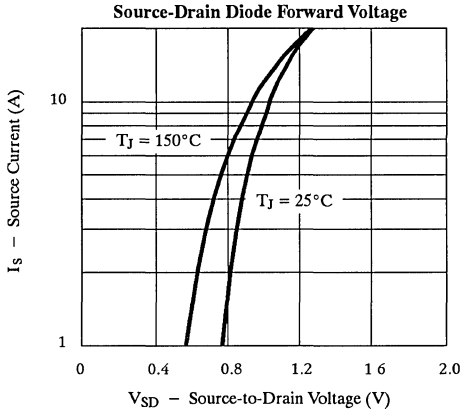


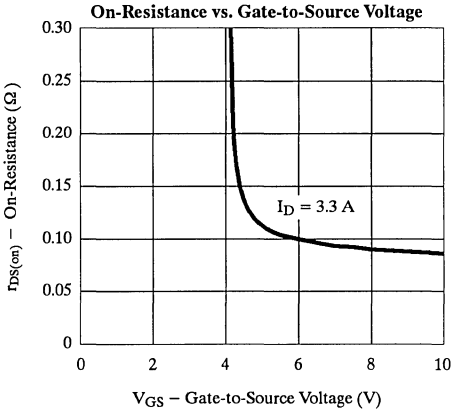


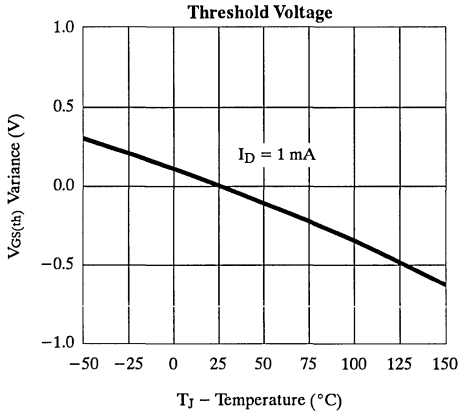


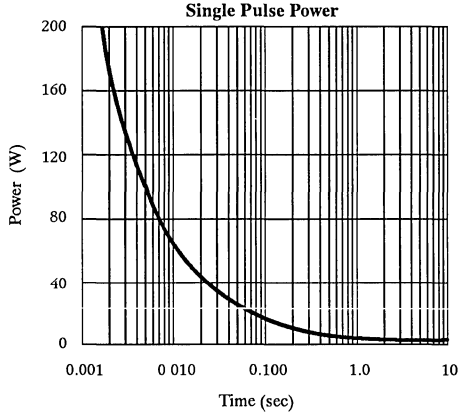
1 LITTLE FOOT

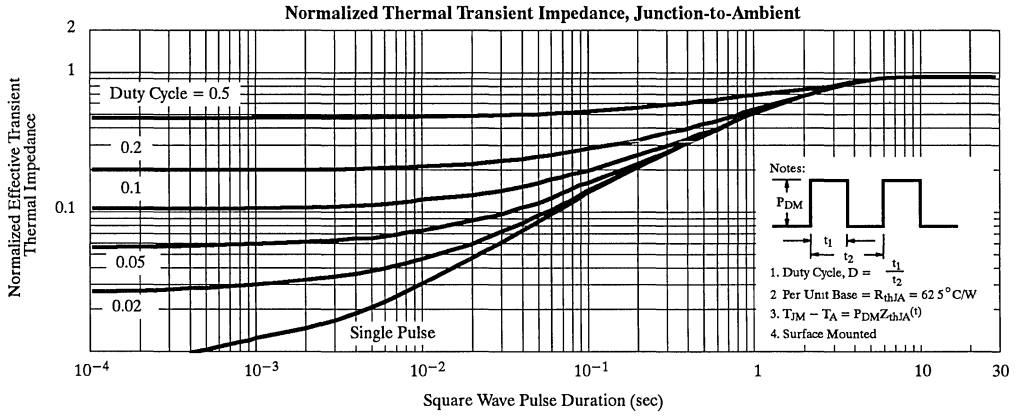
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

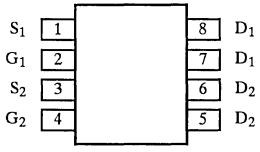
Si9947DY

Dual P-Channel Enhancement-Mode MOSFET

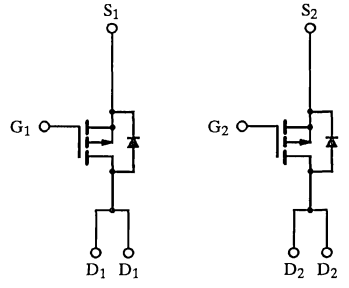
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.10 @ V_{GS} = −10 V	±3.5
	0.19 @ V_{GS} = −4.5 V	±2.5

SO-8



Top View



P-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.5	A
	T_A = 70°C		±2.5	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	−1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

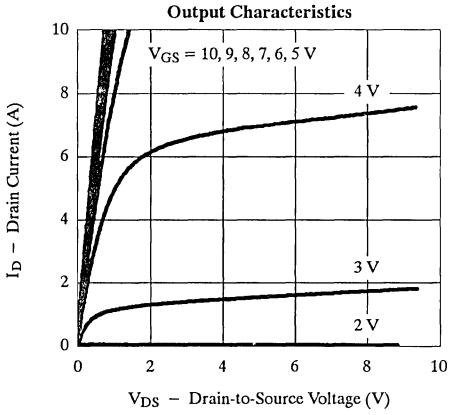
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

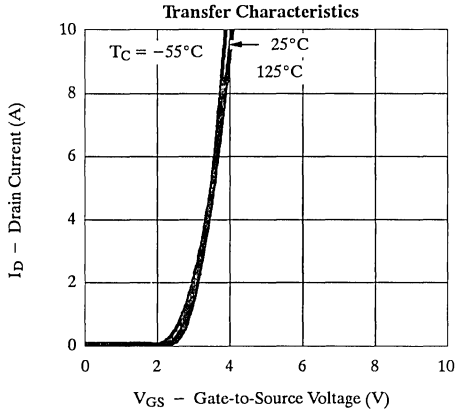
Specifications (T_J = 25°C Unless Otherwise Noted)

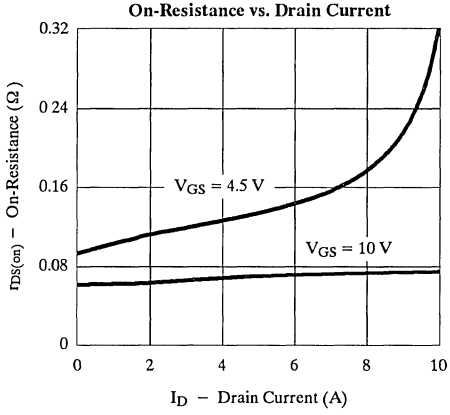
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −10 V	−14			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−2.5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 3.5 A			0.10	Ω
		V_{GS} = −4.5 V, I_D = 2 A			0.19	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −3.5 A		4.0		S
Diode Forward Voltage[b]	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −3.5 A		13	30	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		21	40	ns
Rise Time	t_r			12	25	
Turn-Off Delay Time	$t_{d(off)}$			12	30	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −3.5 A, di/dt = 100 A/µs		50	100	

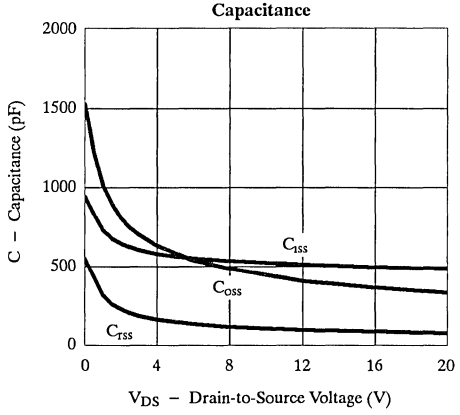
Notes
a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

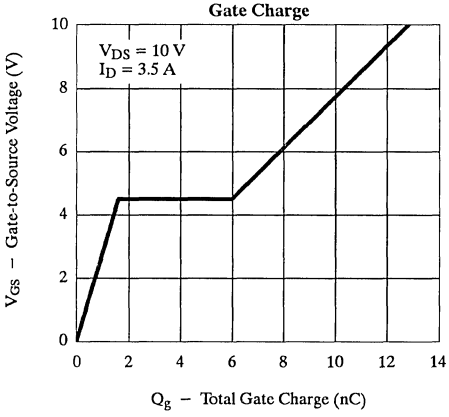
Typical Characteristics (25°C Unless Otherwise Noted)

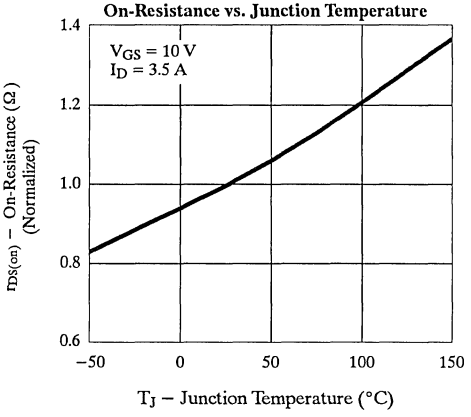




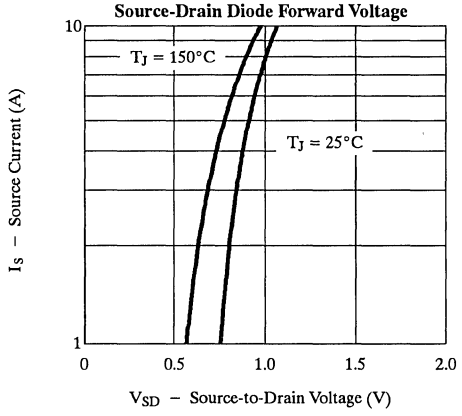


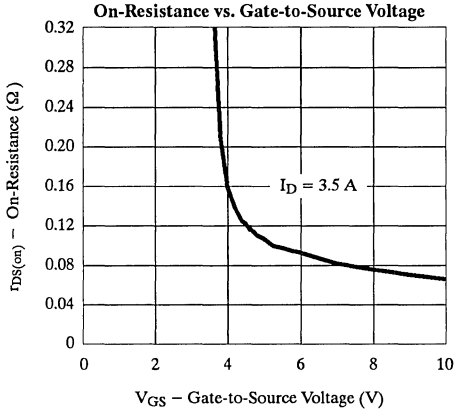


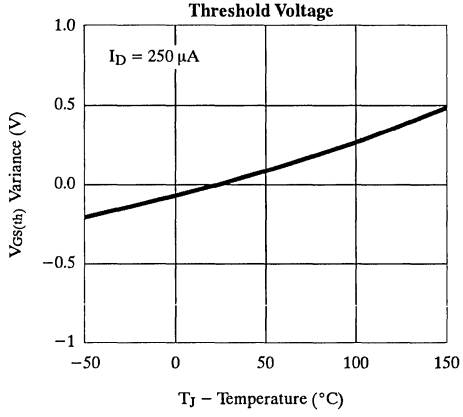


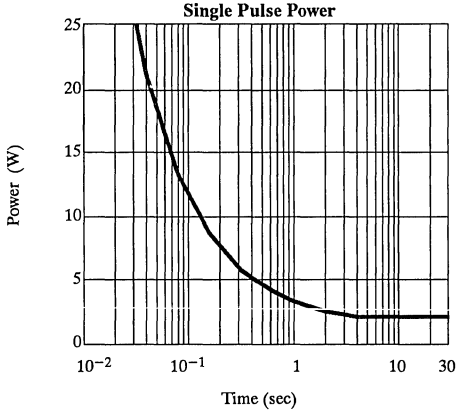


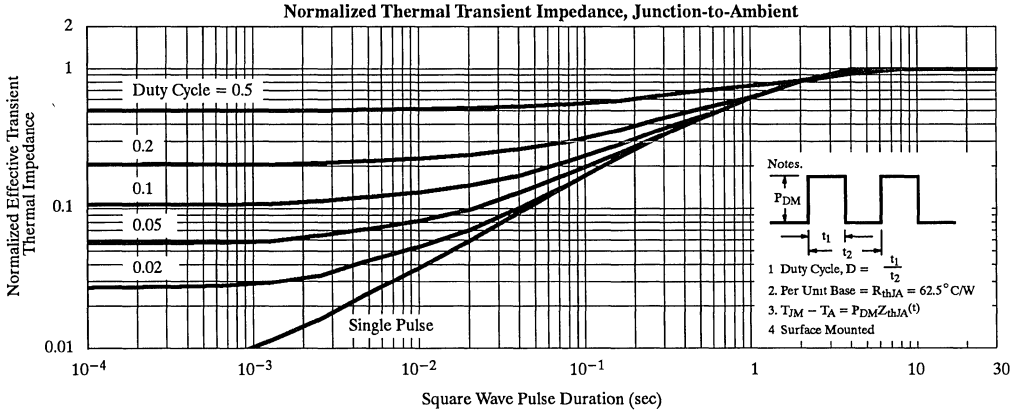
Typical Characteristics (25°C Unless Otherwise Noted)







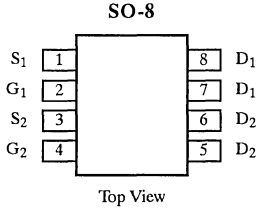


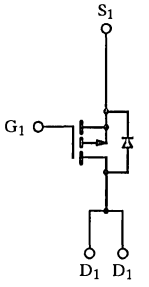


Dual P-Channel Enhancement-Mode MOSFET

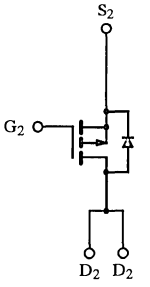
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−60	0.28 @ V_{GS} = −10 V	±2.0
	0.50 @ V_{GS} = −4.5 V	±1.6





P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.0	A
	T_A = 70°C		±1.6	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	−2.0	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

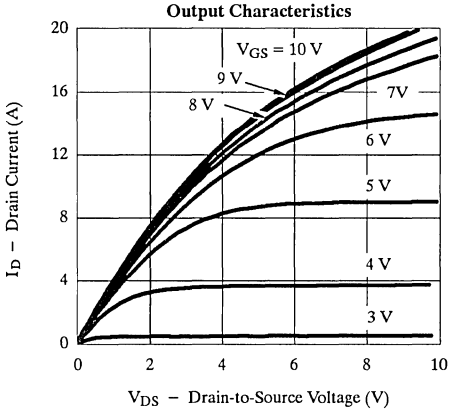
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62 5	°C/W

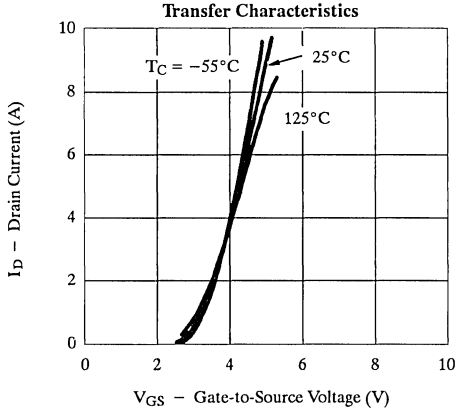
Specifications (T_J = 25°C Unless Otherwise Noted)

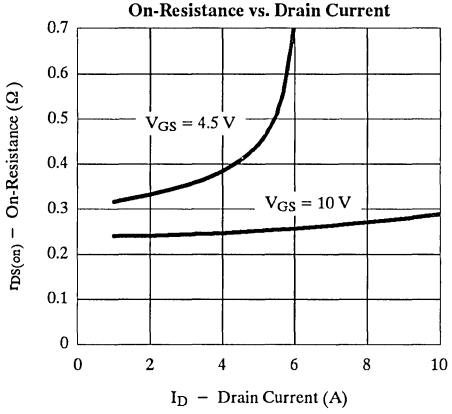
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −40 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −40 V, V_{GS} = 0 V, T_J = 55°C			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −10 V	−10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −2.0 A			0.28	Ω
		V_{GS} = −4.5 V, I_D = −1.6 A			0.50	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −2.0 A		5.0		S
Diode Forward Voltage[b]	V_{SD}	I_S = −2.0 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −30 V, V_{GS} = −10 V, I_D = −2.0 A		16	30	nC
Gate-Source Charge	Q_{gs}			2.0		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −30 V, R_L = 30 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		8	25	ns
Rise Time	t_r			11	30	
Turn-Off Delay Time	$t_{d(off)}$			28	60	
Fall Time	t_f			14	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2.0 A, di/dt = 100 A/µs		65	100	

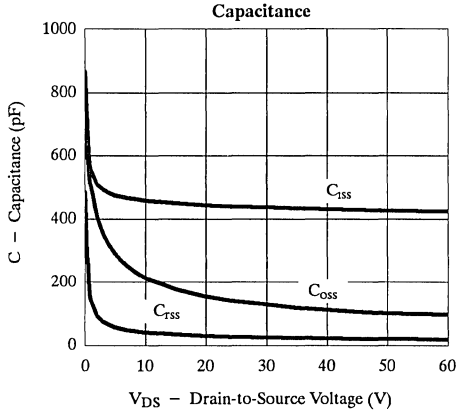
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

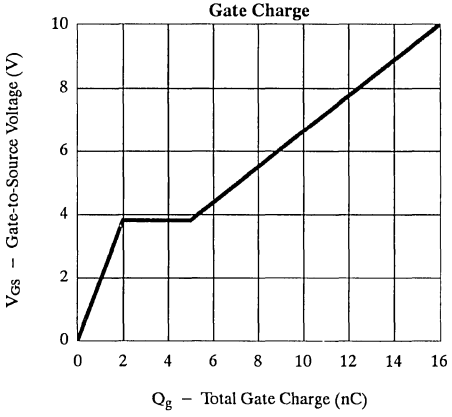
Typical Characteristics (25°C Unless Otherwise Noted)

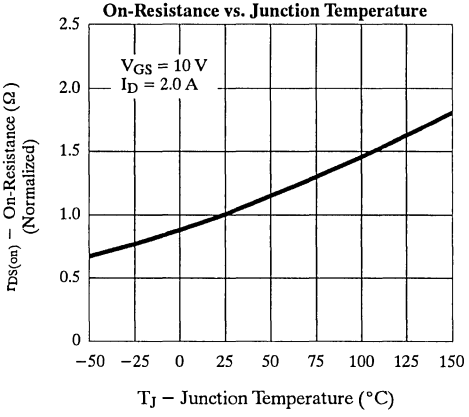




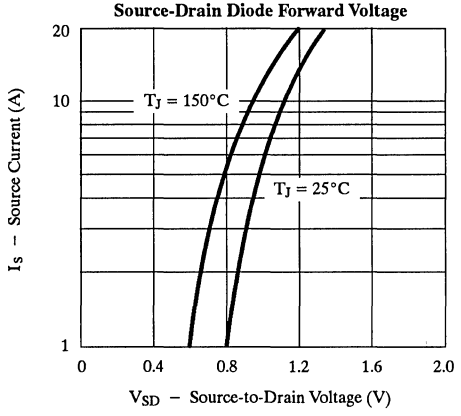


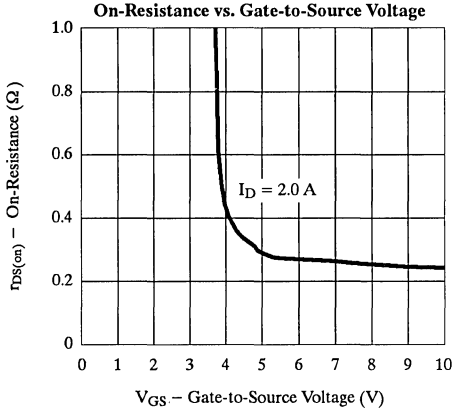


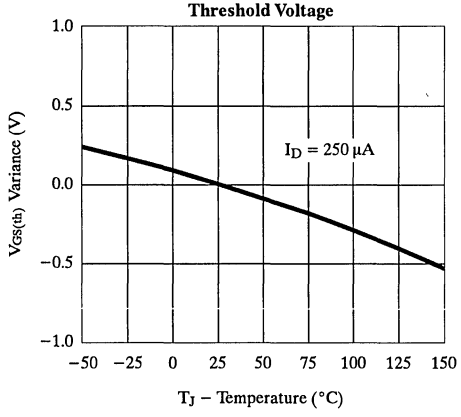


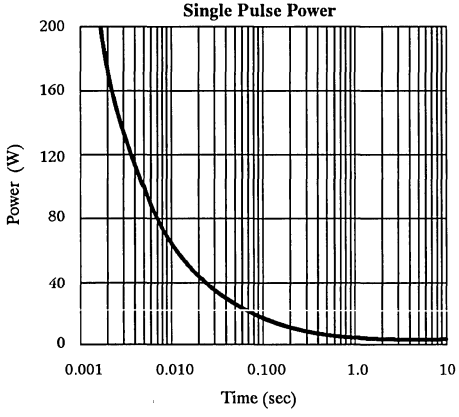


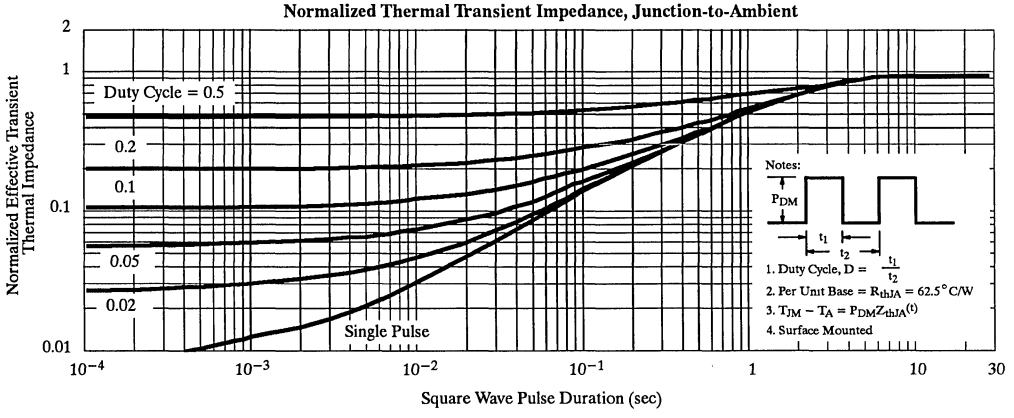
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

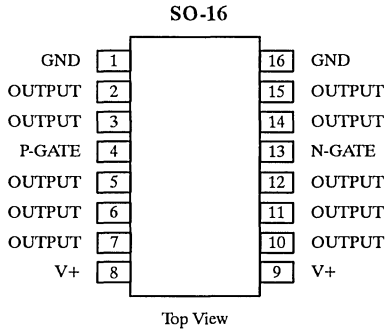
Si9950DY

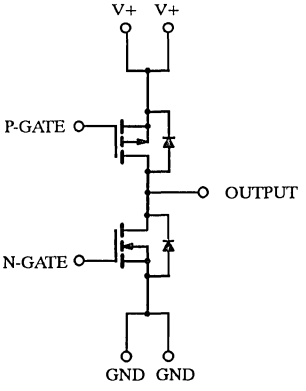
Complementary MOSFET Half-Bridge

Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N- or P-Channel	50	0.3 @ V_{GS} = 10 V	±2.0
		1.0 @ V_{GS} = 5 V	±1.2

Alternate Solution: one Si9948DY and one Si9945DY





Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N- or P-Channel	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.0	A
	T_A = 70°C		±1.7	
Pulsed Drain Current		I_{DM}	±8	
Continuous Source Current (Diode Conduction)		I_S	2.8	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.3	W
	T_A = 70°C		1.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	55	°C/W

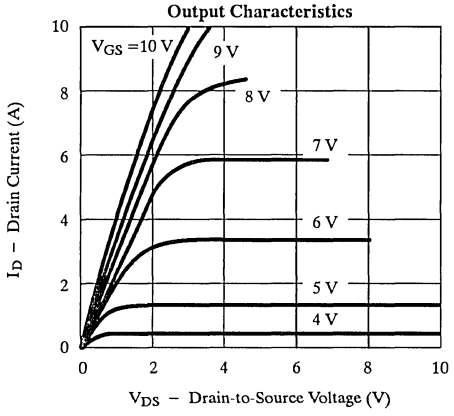
Specifications (T_J = 25°C Unless Otherwise Noted)

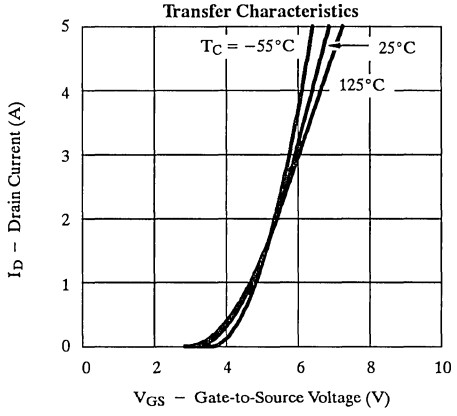
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	2.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.5			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = −40 V, V_{GS} = 0 V	P-Ch			−2	
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = −40 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	8			A
		V_{DS} ≤ −5 V, V_{GS} = −10 V	P-Ch	−8			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1 A				0.3	Ω
		V_{GS} = 5 V, I_D = 0.5 A				1.0	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 1 A	N-Ch		1.1		S
		V_{DS} = −15 V, I_D = −1 A	P-Ch		1.4		
Diode Forward Voltage[b]	V_{SD}	I_S = 2 A, V_{GS} = 0 V	N-Ch		0.9	1.2	V
		I_S = −2 A, V_{GS} = 0 V	P-Ch		−1.0	−1.3	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 25 V, V_{GS} = 10 V, I_D = 2 A P-Channel V_{DS} = −25 V, V_{GS} = −10 V, I_D = −2 A	N-Ch		3.7	6.0	nC
			P-Ch		17.0	26.0	
Gate-Source Charge	Q_{gs}		N-Ch		1.0		
			P-Ch		2.3		
Gate-Drain Charge	Q_{gd}		N-Ch		1.2		
			P-Ch		8.5		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 25 V, R_L = 25 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −25 V, R_L = 25 Ω, I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		7	20	ns
			P-Ch		10	30	
Rise Time	t_r		N-Ch		13	30	
			P-Ch		25	50	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		18	40	
			P-Ch		65	100	
Fall Time	t_f		N-Ch		13	25	
			P-Ch		60	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/µs	N-Ch		70	100	
			P-Ch		70	100	

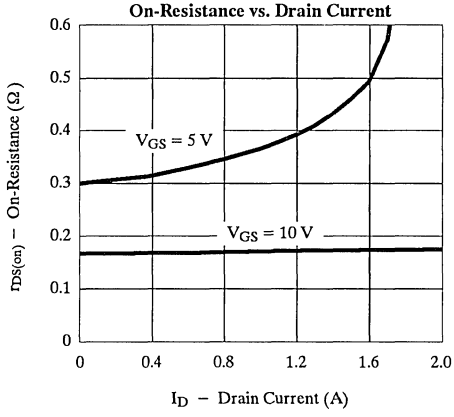
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

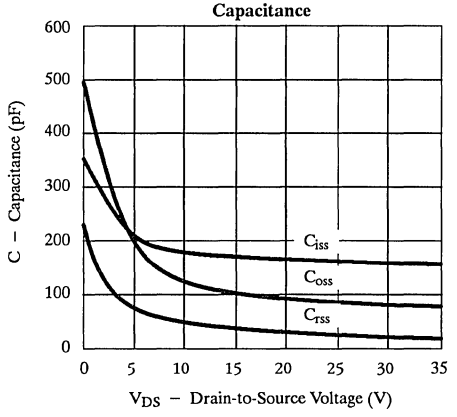
Typical Characteristics

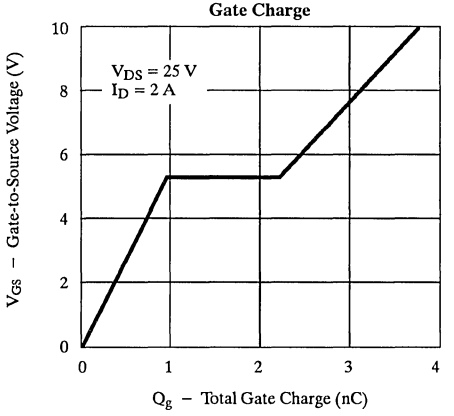
(25°C Unless Otherwise Noted)

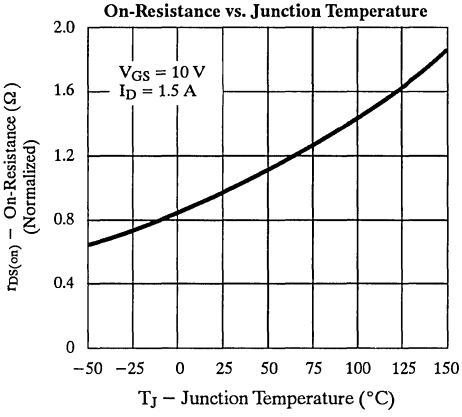








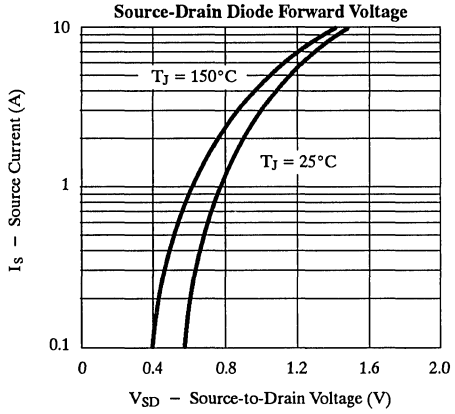


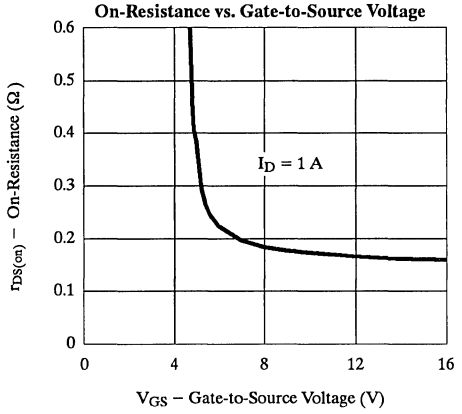


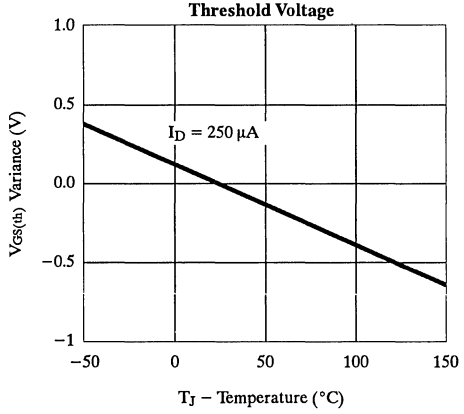
Typical Characteristics

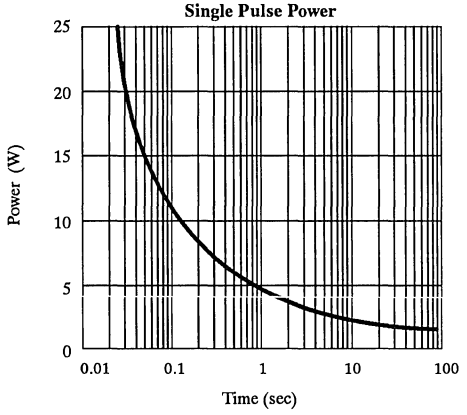
N-Channel

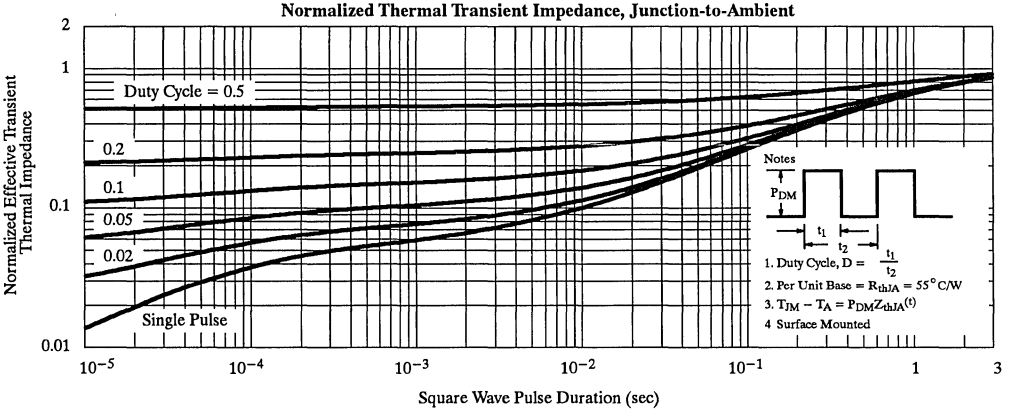
(25°C Unless Otherwise Noted)









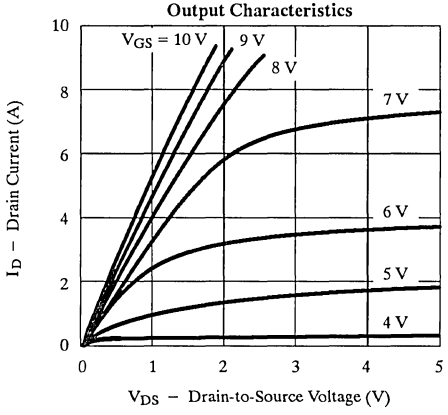


Typical Characteristics

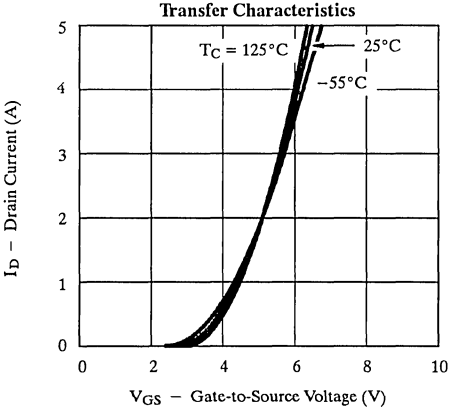
P-Channel

(25°C Unless Otherwise Noted)

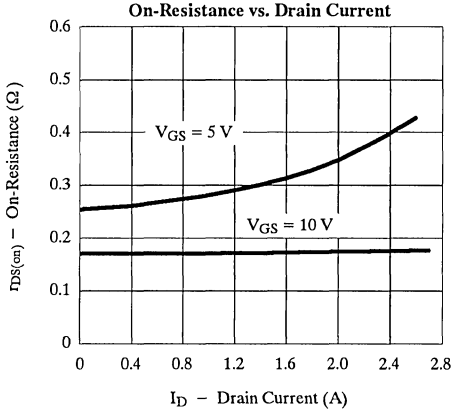
Output Characteristics



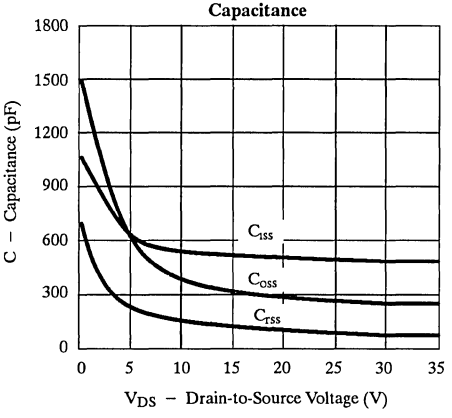
Transfer Characteristics



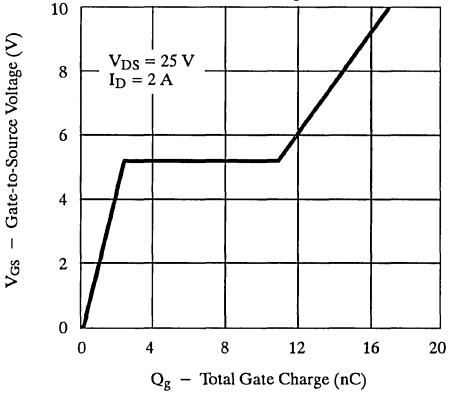
On-Resistance vs. Drain Current



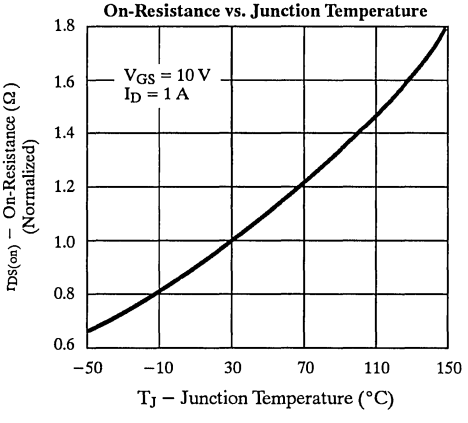
Capacitance



Gate Charge

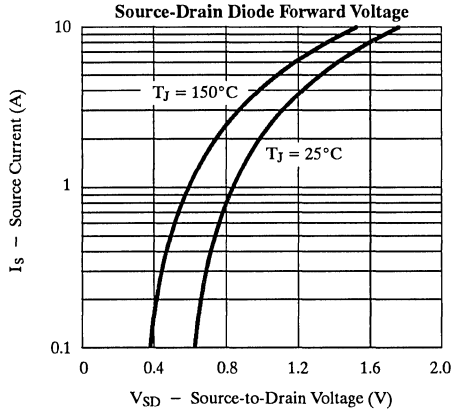


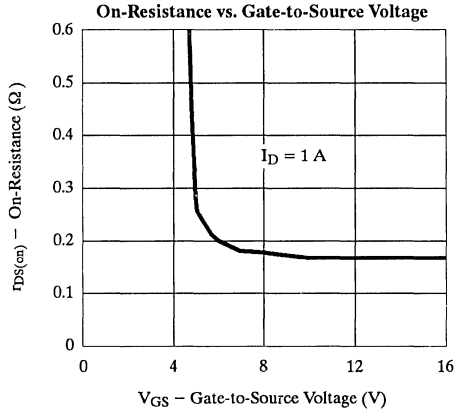
On-Resistance vs. Junction Temperature

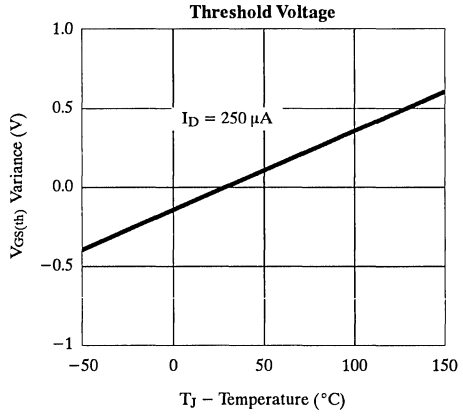


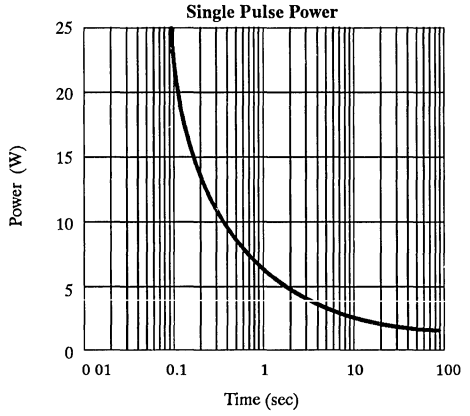
Typical Characteristics

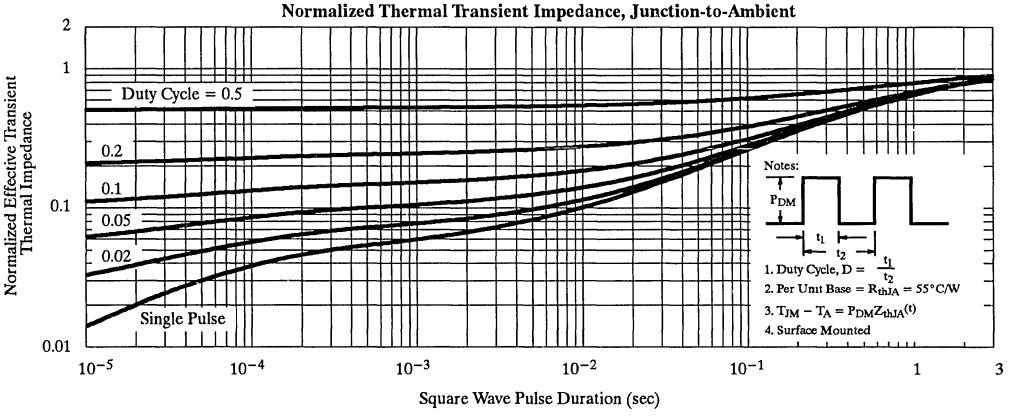
(25°C Unless Otherwise Noted)











Siliconix

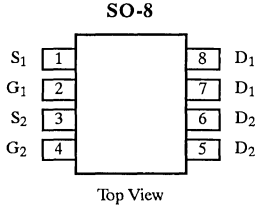
Si9952DY

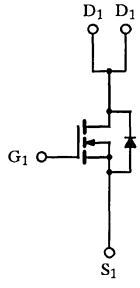
Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

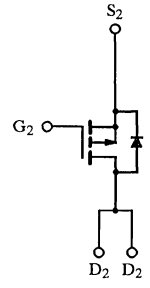
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	25	0.10 @ V_{GS} = 10 V	±3.5
		0.15 @ V_{GS} = 4.5 V	±2.0
P-Channel	−25	0.25 @ V_{GS} = −10 V	±2.3
		0.40 @ V_{GS} = −4.5 V	±1.8

Recommended upgrade: Si9939DY or Si9943DY
Lower profile/smaller size—see LITE FOOT™ equivalent: Si6942DQ





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	25	−25	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.5	±2.3	A
	T_A = 70°C		±2.8	±1.9	
Pulsed Drain Current		I_{DM}	±14	±9.2	
Continuous Source Current (Diode Conduction)		I_S	1.7	−1 6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = −20 V, V_{GS} = 0 V	P-Ch			−2	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	3.5			A
		V_{DS} ≤ −5 V, V_{GS} = −10 V	P-Ch	−2.3			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1 A	N-Ch		0.08	0.10	Ω
		V_{GS} = −10 V, I_D = 1 A	P-Ch		0.13	0.25	
		V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch		0.12	0.15	
		V_{GS} = −4.5 V, I_D = 0.5 A	P-Ch		0.20	0.40	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.5 A	N-Ch		5.0		S
		V_{DS} = −15 V, I_D = −3.5 A	P-Ch		3.2		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V	N-Ch		1.1	1.4	V
		I_S = −1.25 A, V_{GS} = 0 V	P-Ch		−1.2	−1.6	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 12.5 V, V_{GS} = 10 V, I_D = 2.3 A P-Channel V_{DS} = −12.5 V, V_{GS} = −10 V, I_D = −2.3 A	N-Ch		9.4	27	nC
			P-Ch		8.4	25	
Gate-Source Charge	Q_{gs}		N-Ch		1.6		
			P-Ch		1.3		
Gate-Drain Charge	Q_{gd}		N-Ch		3.1		
			P-Ch		3.0		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −25 V, R_L = 25 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		9	20	ns
			P-Ch		12	40	
Rise Time	t_r		N-Ch		8	20	
			P-Ch		19	40	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		45	90	
			P-Ch		42	90	
Fall Time	t_f		N-Ch		25	50	
			P-Ch		27	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs	N-Ch			75	
			P-Ch		69	100	

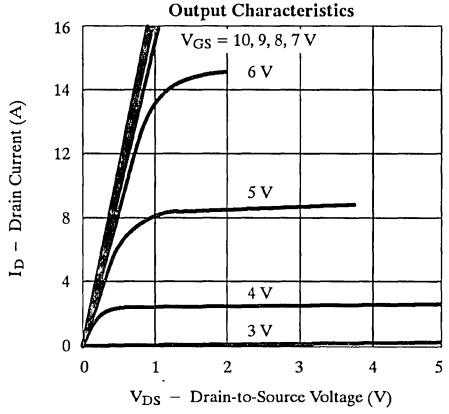
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics

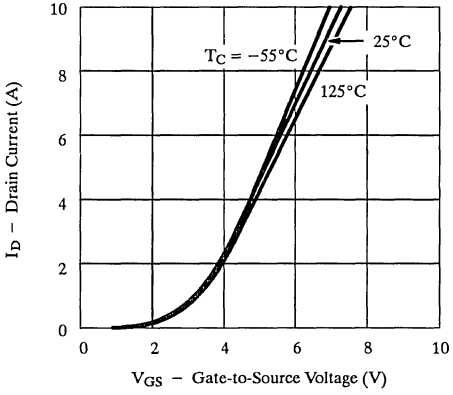
N-Channel

(25°C Unless Otherwise Noted)

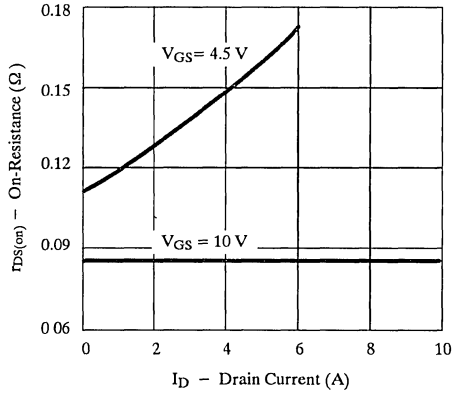
Output Characteristics



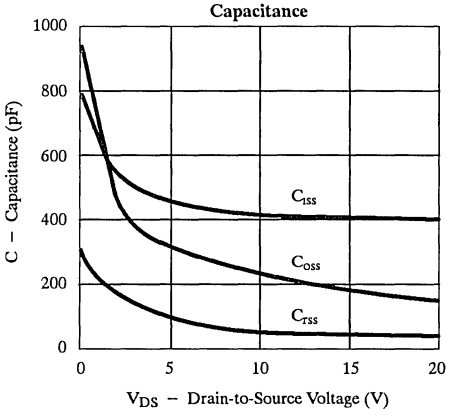
Transfer Characteristics



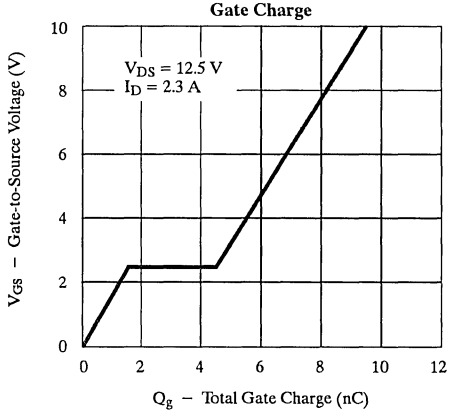
On-Resistance vs. Drain Current



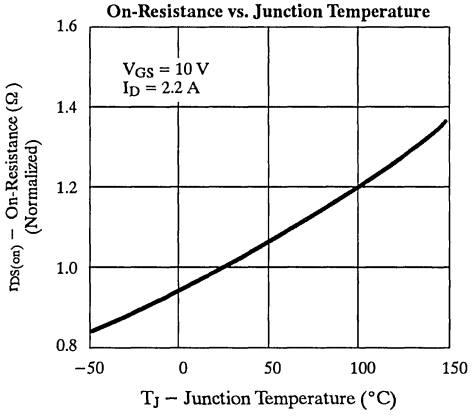
Capacitance



Gate Charge



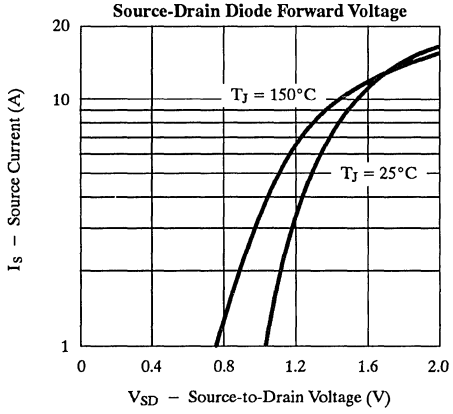
On-Resistance vs. Junction Temperature



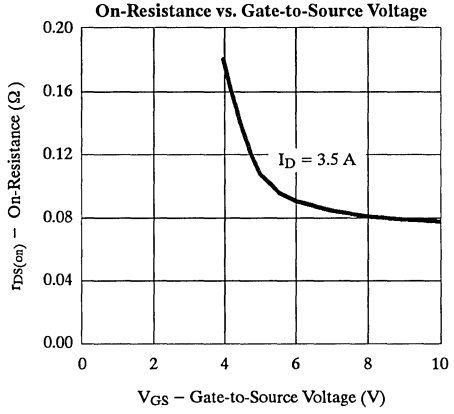
Typical Characteristics

(25°C Unless Otherwise Noted)

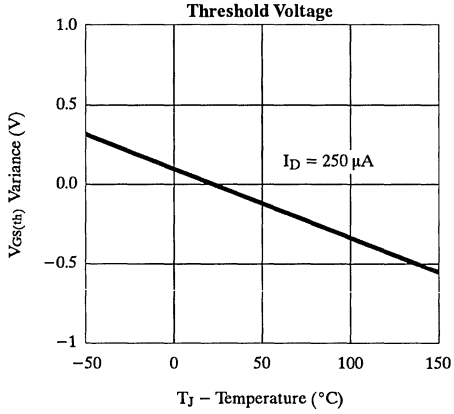
Source-Drain Diode Forward Voltage



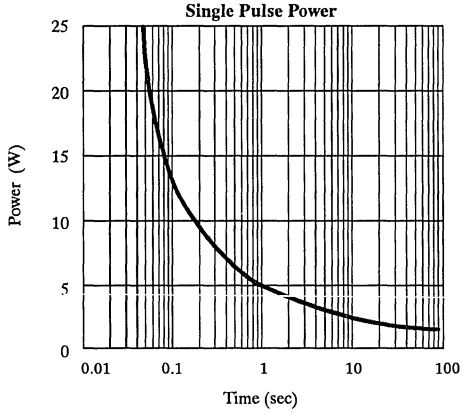
On-Resistance vs. Gate-to-Source Voltage



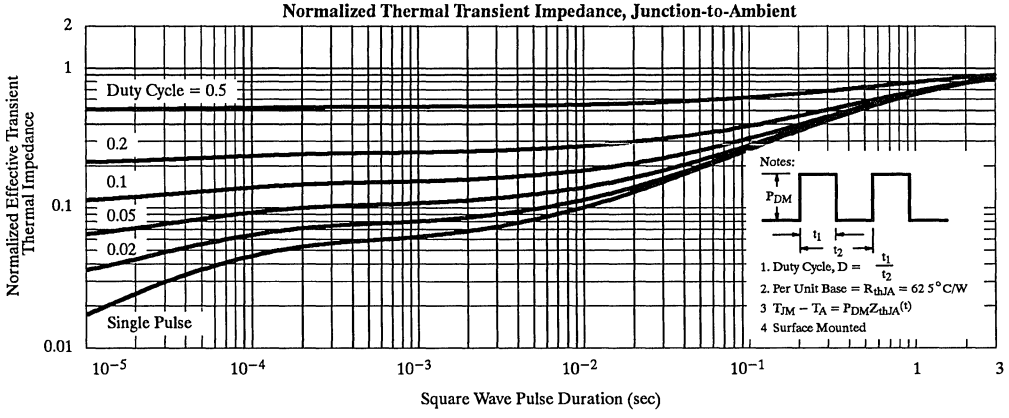
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

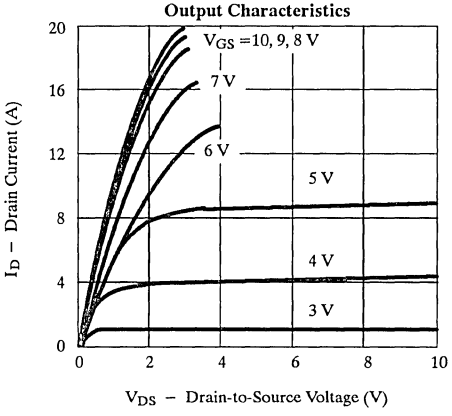


Typical Characteristics

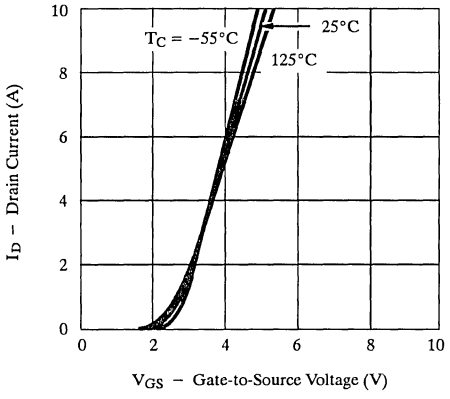
P-Channel

(25°C Unless Otherwise Noted)

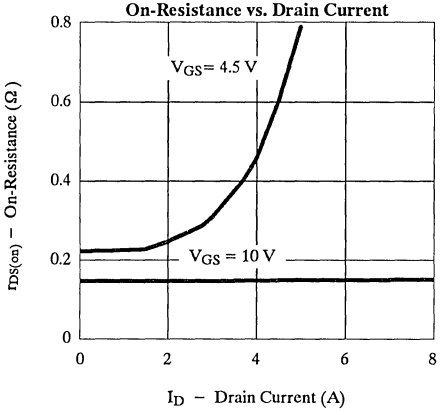
Output Characteristics



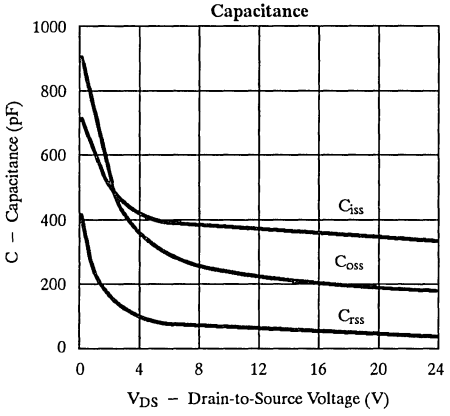
Transfer Characteristics



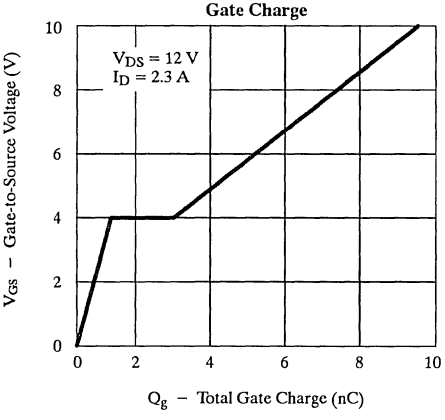
On-Resistance vs. Drain Current



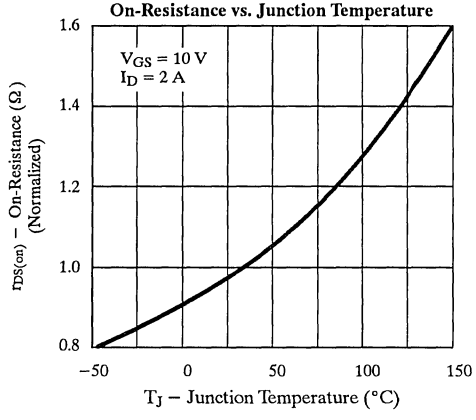
Capacitance



Gate Charge



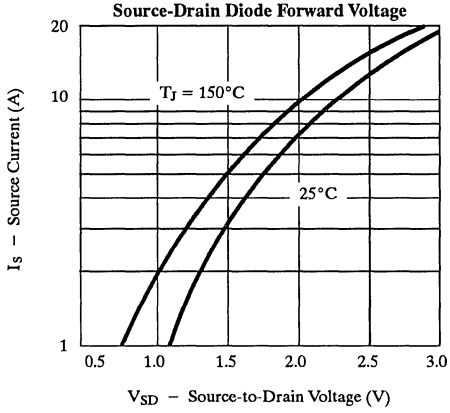
On-Resistance vs. Junction Temperature



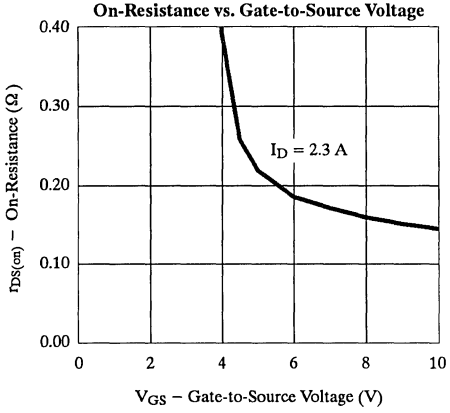
Typical Characteristics

(25°C Unless Otherwise Noted)

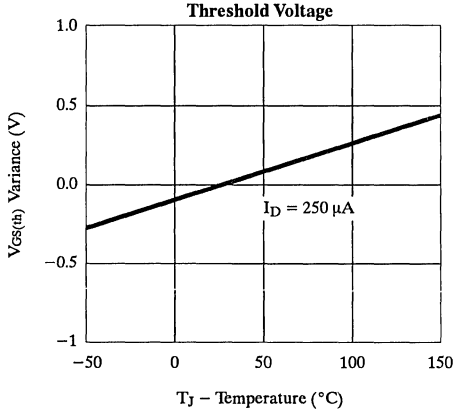
Source-Drain Diode Forward Voltage



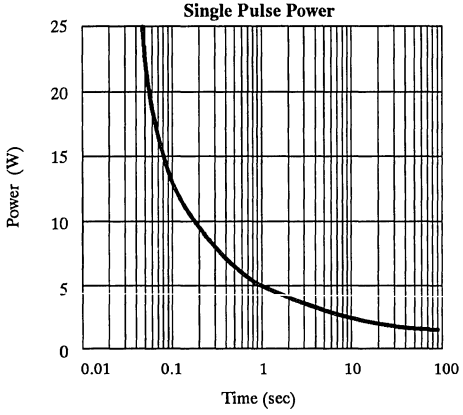
On-Resistance vs. Gate-to-Source Voltage



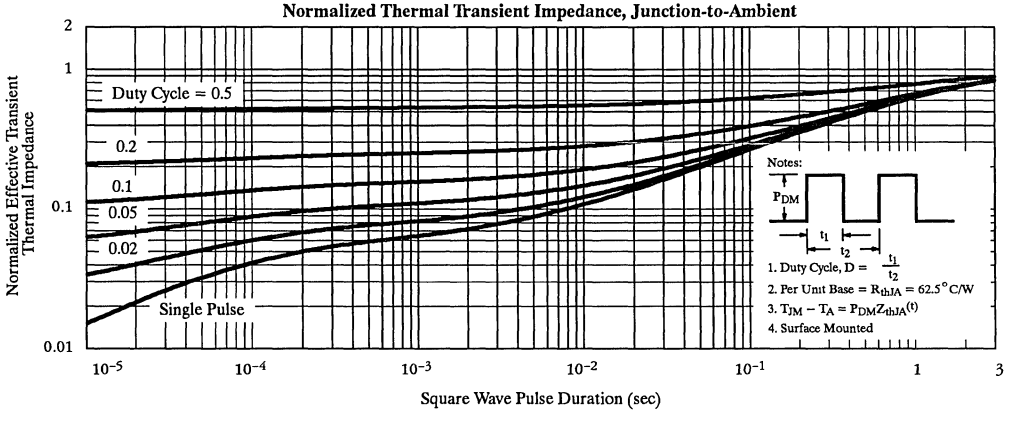
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

Si9953DY

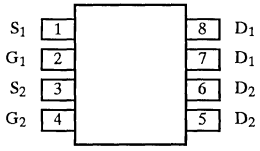
Dual P-Channel Enhancement-Mode MOSFET

Product Summary

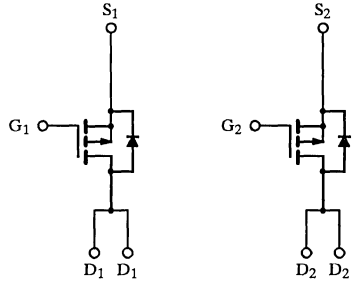
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.25 @ V_{GS} = −10 V	±2.3
	0.40 @ V_{GS} = −4.5 V	±1.5

Lower profile/smaller size—see LITE FOOT™ equivalent: Si6953DQ

SO-8



Top View



P-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.3	A
	T_A = 70°C		±1.8	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	−1.6	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

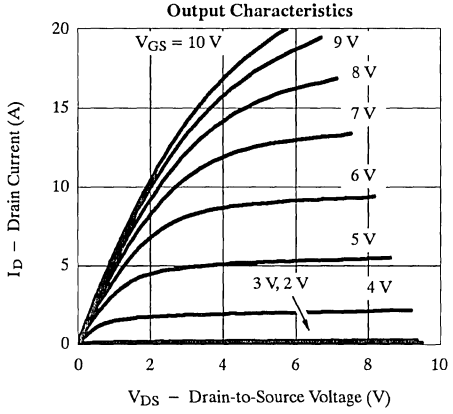
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

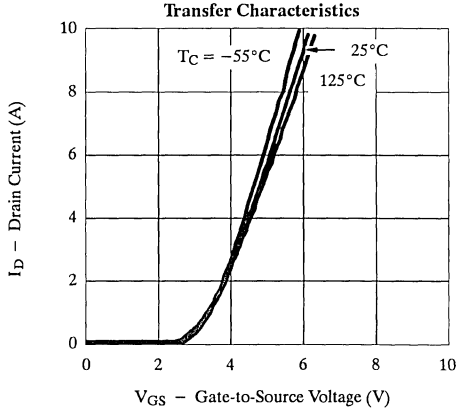
Specifications (T_J = 25°C Unless Otherwise Noted)

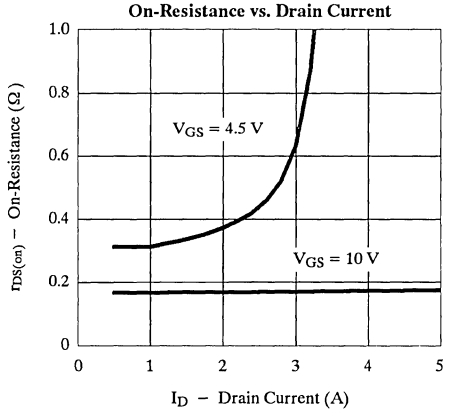
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C			−25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −10 V	−10			A
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−1.5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 1 A		0.16	0.25	Ω
		V_{GS} = −4.5 V, I_D = 0.5 A		0.30	0.40	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −2.3 A		2.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = −1.25 A, V_{GS} = 0 V		−0.9	−1.6	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −2.3 A		5.4	25	nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		10	40	ns
Rise Time	t_r			10	40	
Turn-Off Delay Time	$t_{d(off)}$			38	90	
Fall Time	t_f			27	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		69	100	

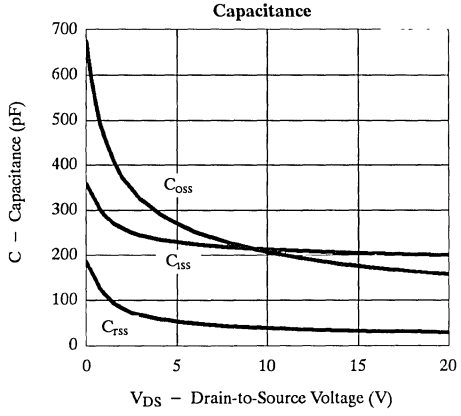
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

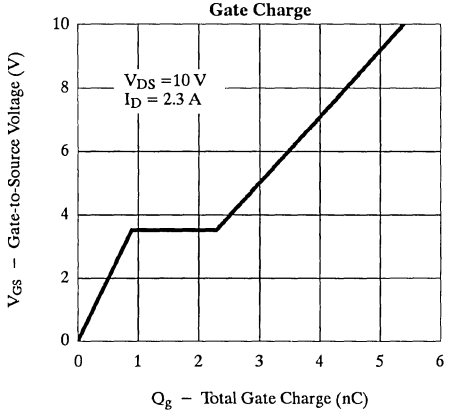
Typical Characteristics (25°C Unless Otherwise Noted)

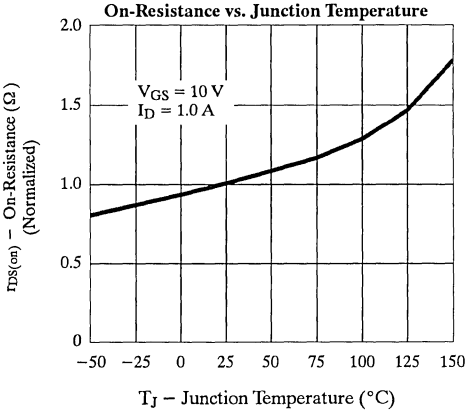




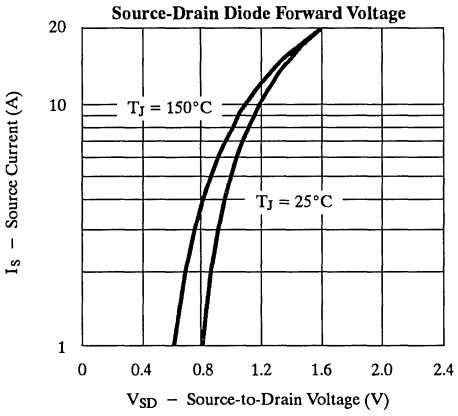


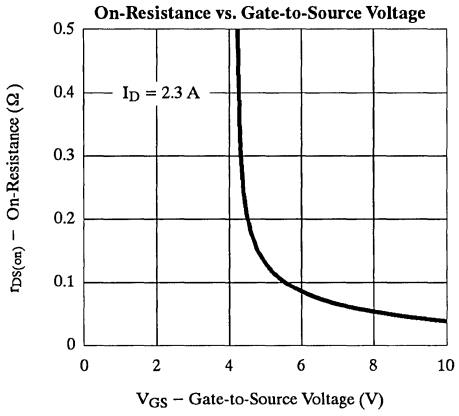


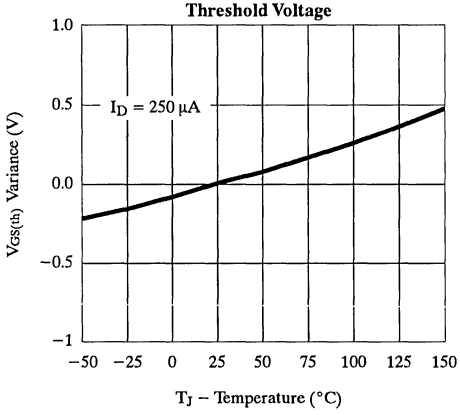


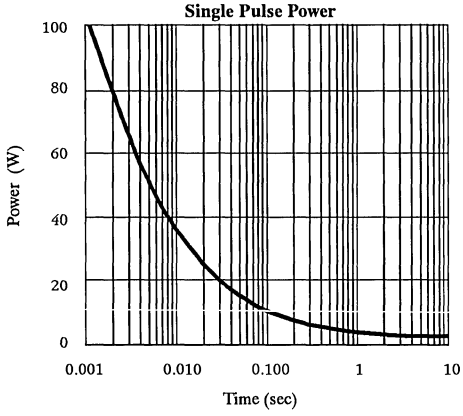


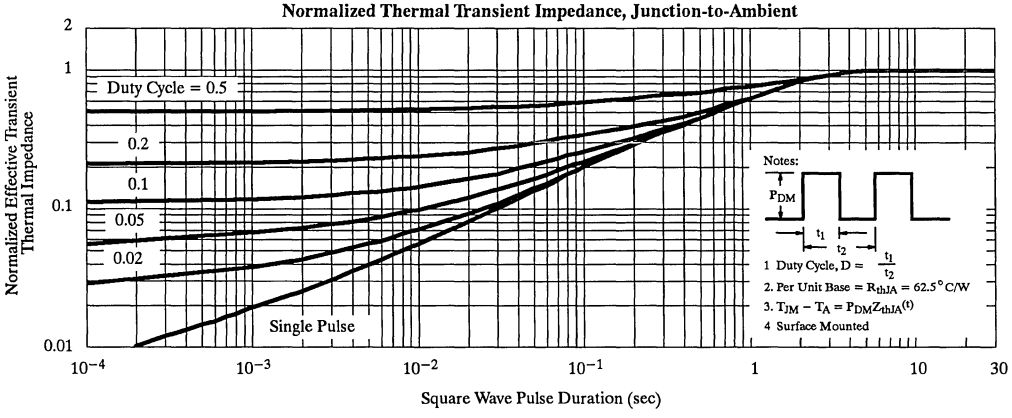
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

Si9955DY

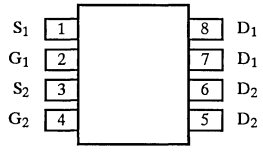
Dual N-Channel Enhancement-Mode MOSFET

Product Summary

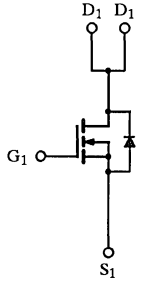
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.13 @ V_{GS} = 10 V	±3.0
	0.20 @ V_{GS} = 4.5 V	±1.5

Recommend upgrade: Si9945DY

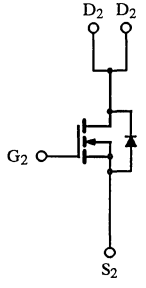
SO-8



Top View



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.0	A
	T_A = 70°C		±2.3	
Pulsed Drain Current		I_{DM}	±10	
Continuous Source Current (Diode Conduction)		I_S	2.0	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

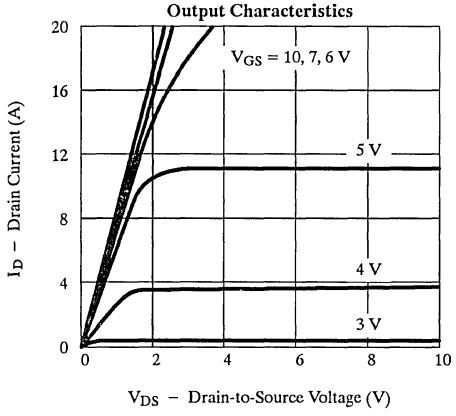
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

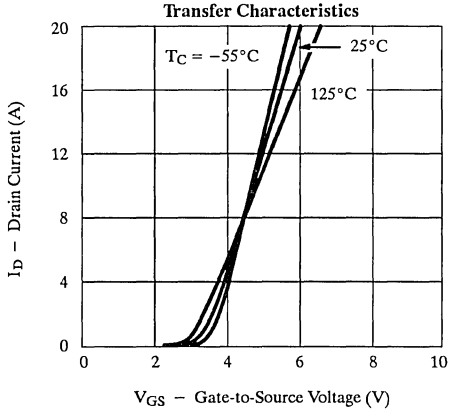
Specifications (T_J = 25°C Unless Otherwise Noted)

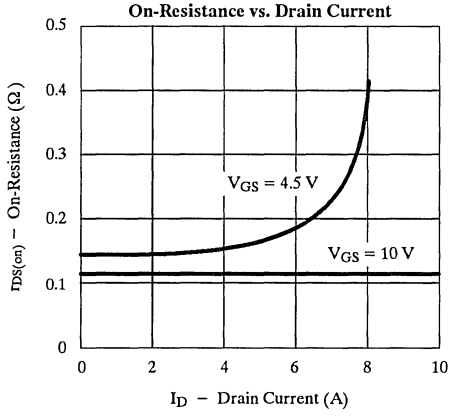
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.0 A		0.11	0.13	Ω
		V_{GS} = 4.5 V, I_D = 1.5 A		0.15	0.20	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.0 A		5.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.5 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 2 A		8.0	30	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			2.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		9	20	ns
Rise Time	t_r			8	20	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			25	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.5 A, di/dt = 100 A/µs		70	100	

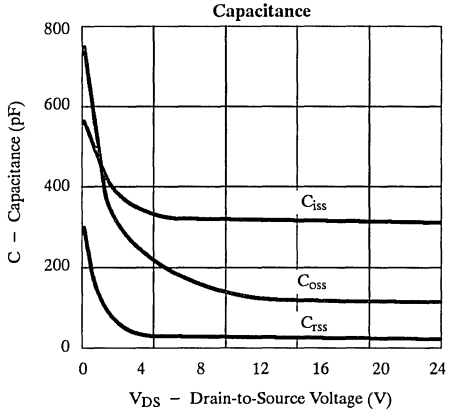
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

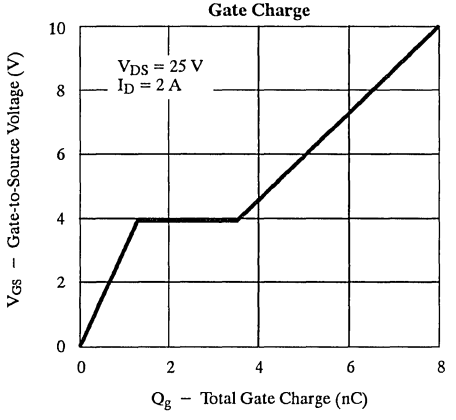
Typical Characteristics (25°C Unless Otherwise Noted)

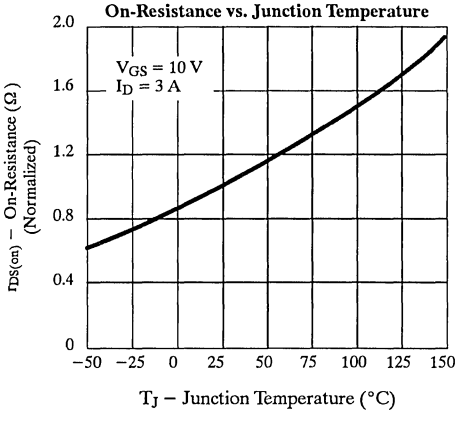




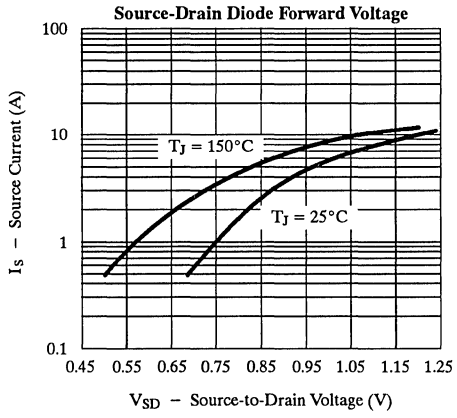


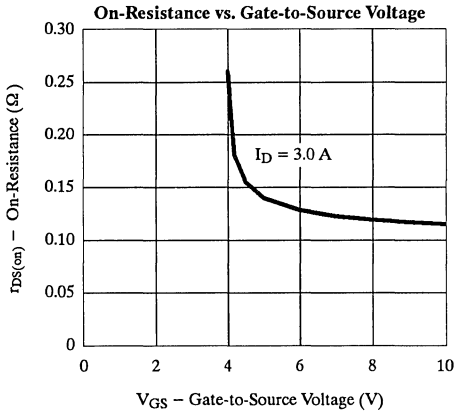


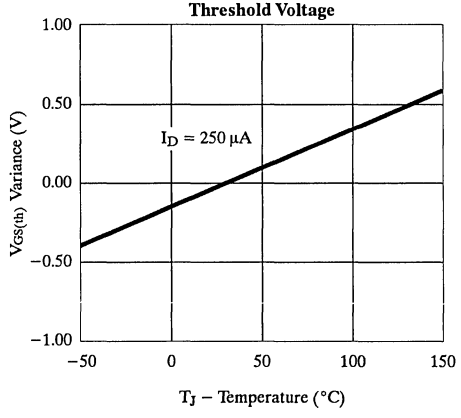


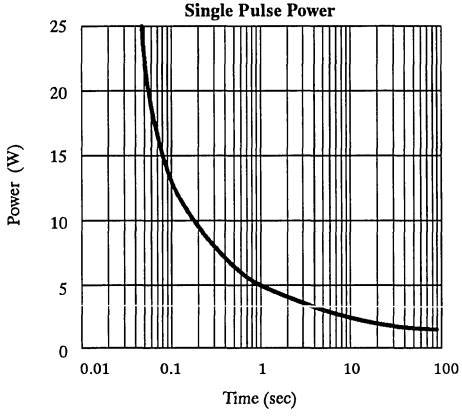


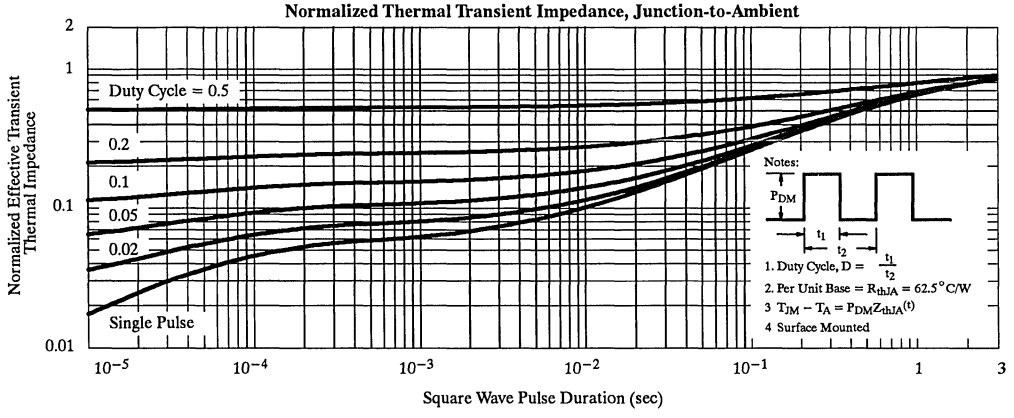
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

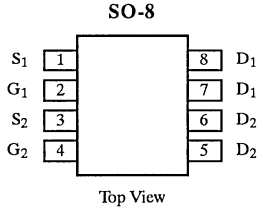
Si9956DY

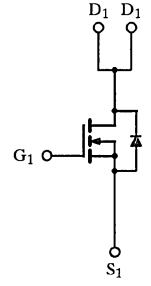
Dual N-Channel Enhancement-Mode MOSFET

Product Summary

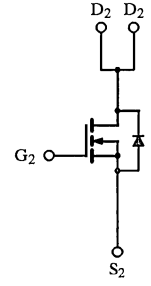
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.10 @ V_{GS} = 10 V	±3.5
	0.20 @ V_{GS} = 4.5 V	±2.0

Recommended upgrade: Si9936DY
Lower profile/smaller size—see LITE FOOT™ equivalent: Si6956DQ





N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.5	A
	T_A = 70°C		±2.8	
Pulsed Drain Current		I_{DM}	±14	
Continuous Source Current (Diode Conduction)		I_S	1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

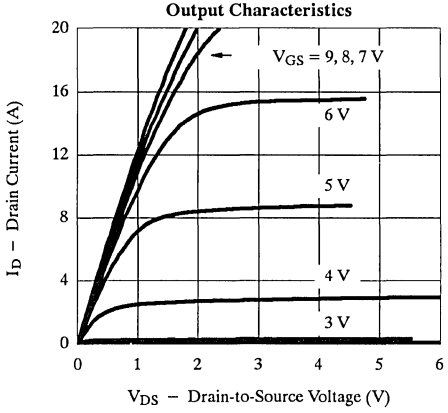
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			2	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	14			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.2 A		0.08	0.10	Ω
		V_{GS} = 4.5 V, I_D = 1 A		0.12	0.20	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.5 A		5.2		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.9	1.4	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 1.8 A		9	30	nC
Gate-Source Charge	Q_{gs}			0.7		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		5	20	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			18	90	
Fall Time	t_f			10	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		60	100	

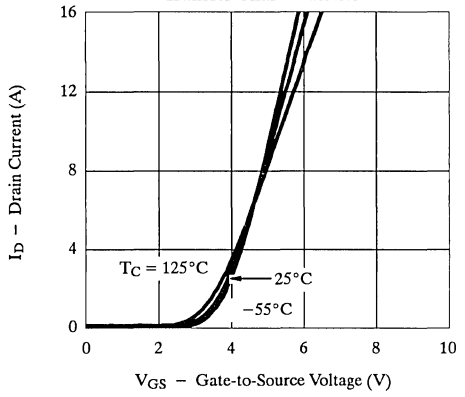
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

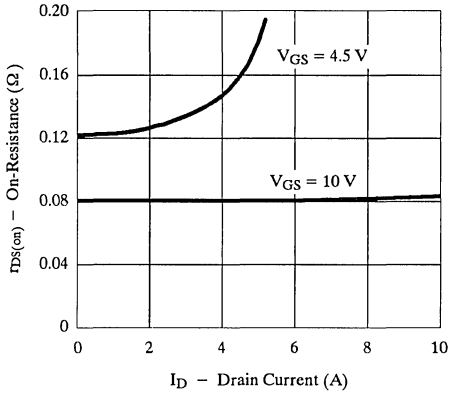
Output Characteristics



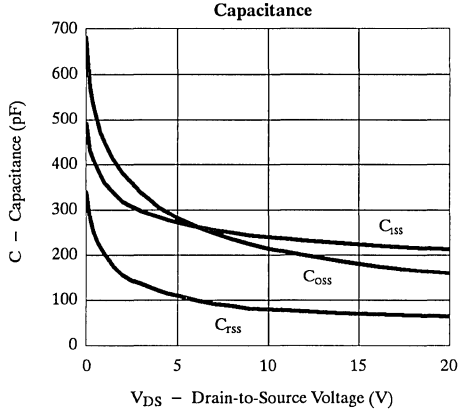
Transfer Characteristics



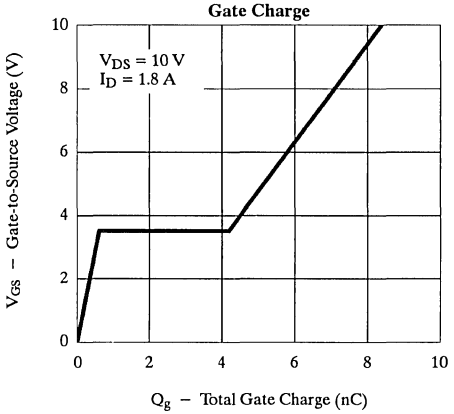
On-Resistance vs. Drain Current



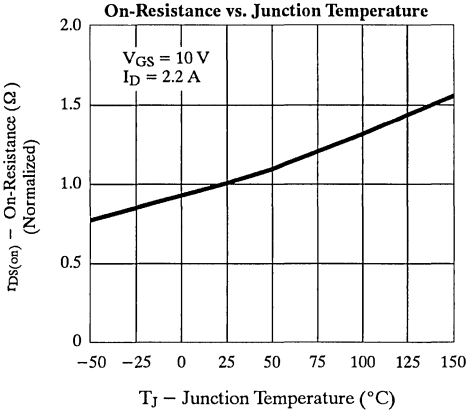
Capacitance



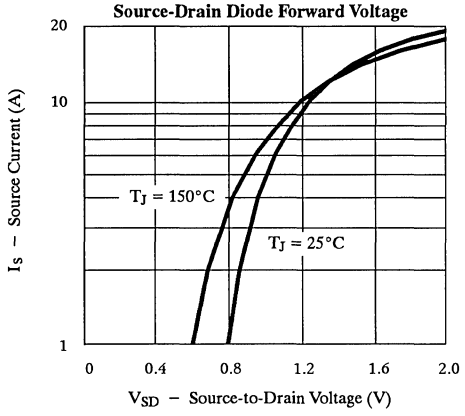
Gate Charge

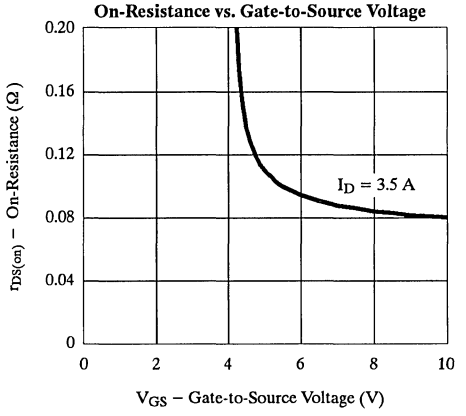


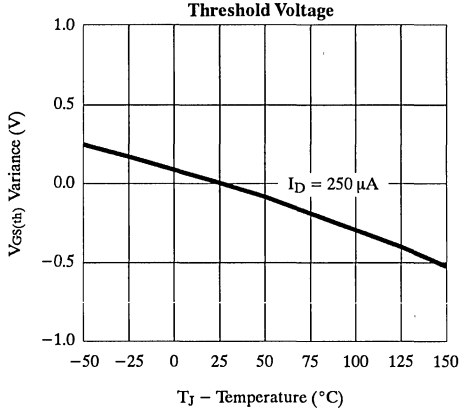
On-Resistance vs. Junction Temperature

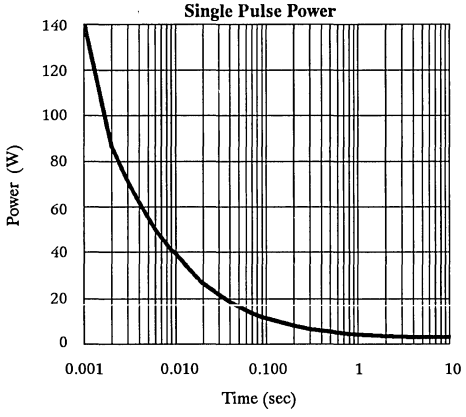


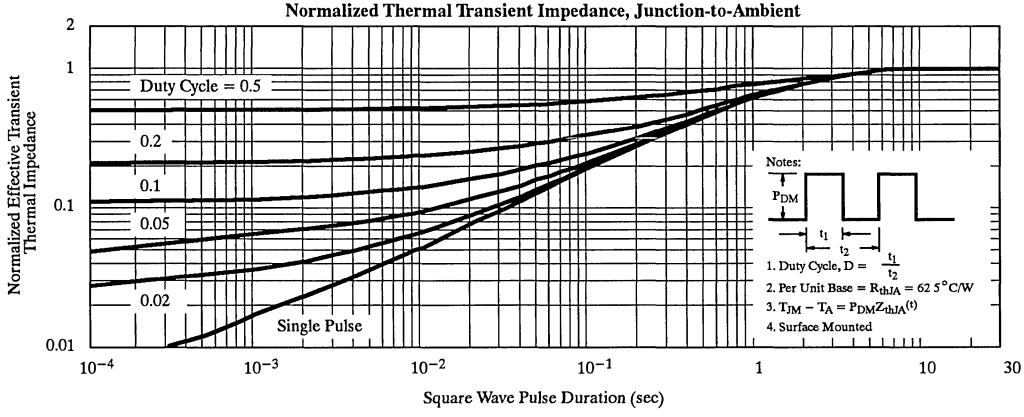
Typical Characteristics (25°C Unless Otherwise Noted)











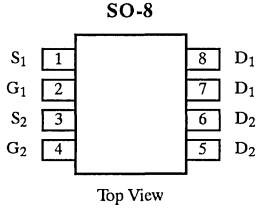
Siliconix

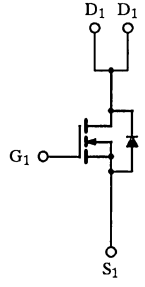
Si9958DY

Dual Enhancement-Mode MOSFETs (N- and P-Channel)

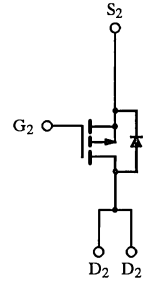
Product Summary

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.10 @ V_{GS} = 10 V	±3.5
		0.12 @ V_{GS} = 6 V	±3
		0.15 @ V_{GS} = 4.5 V	±2.5
P-Channel	−20	0.10 @ V_{GS} = −10 V	±3.5
		0.12 @ V_{GS} = −6V	±3
		0.19 @ V_{GS} = −4.5 V	±2.5





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	−20	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.5	±3.5	A
	T_A = 70°C		±2.8	±2.8	
Pulsed Drain Current		I_{DM}	±14	±14	
Continuous Source Current (Diode Conduction)		I_S	1.7	−1.7	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2.0		W
	T_A = 70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

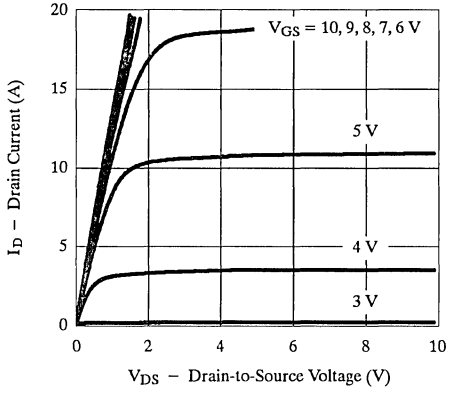
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = −16 V, V_{GS} = 0 V	P-Ch			−1	
		V_{DS} = 10 V, V_{GS} = 0 V, T_J = 70°C	N-Ch			5	
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C	P-Ch			−5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	14			A
		V_{DS} ≤ −5 V, V_{GS} = −10 V	P-Ch	−14			
		V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	3.5			
		V_{DS} ≤ −5 V, V_{GS} = −4.5 V	P-Ch	−2.5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.5 A	N-Ch			0.10	Ω
		V_{GS} = −10 V, I_D = 3.5 A	P-Ch	0.05		0.10	
		V_{GS} = 6 V, I_D = 3 A	N-Ch			0.12	
		V_{GS} = − 6 V, I_D = 3 A	P-Ch	0.08		0.12	
		V_{GS} = 4.5 V, I_D = 2 A	N-Ch			0.15	
		V_{GS} = −4.5 V, I_D = 2 A	P-Ch			0.19	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3.5 A	N-Ch		5.6		S
		V_{DS} = −15 V, I_D = −3.5 A	P-Ch		4.0		
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V	N-Ch		0.9	1.2	V
		I_S = −1.7 A, V_{GS} = 0 V	P-Ch		−0.9	−1.2	
Dynamic[a]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 10 V, I_D = 3.5 A P-Channel V_{DS} = −10 V, V_{GS} = −10 V, I_D = −3.5 A	N-Ch		9	30	nC
			P-Ch		13	30	
Gate-Source Charge	Q_{gs}		N-Ch		1.0		
			P-Ch		2.0		
Gate-Drain Charge	Q_{gd}		N-Ch		3.1		
			P-Ch		5.4		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −10 V, R_L = 10 Ω, I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch		5	10	ns
			P-Ch		21	40	
Rise Time	t_r		N-Ch		12	25	
			P-Ch		12	25	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		17	30	
			P-Ch		12	30	
Fall Time	t_f		N-Ch		9	20	
			P-Ch		11	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 3.5 A, di/dt = 100 A/µs	N-Ch		60	100	
			P-Ch		50	100	

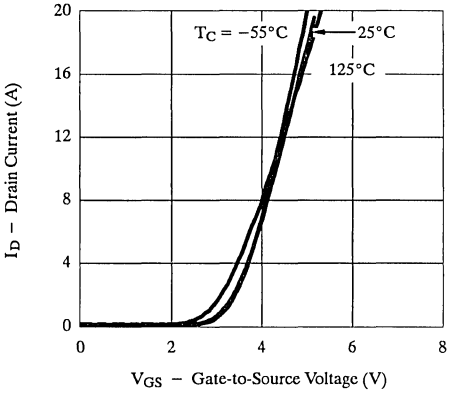
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

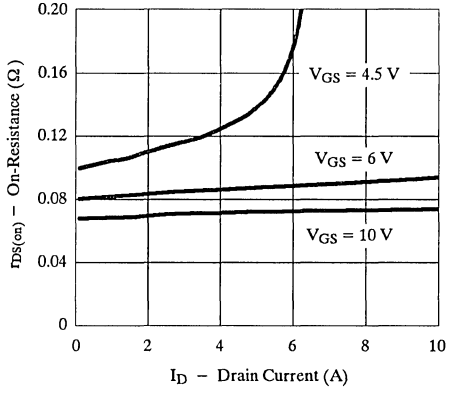
Output Characteristics



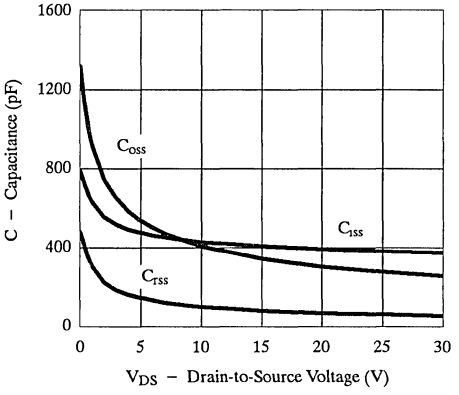
Transfer Characteristics



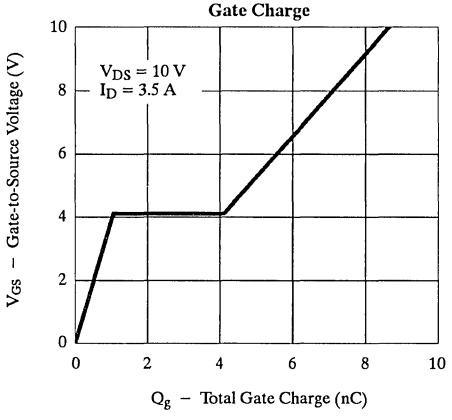
On-Resistance vs. Drain Current



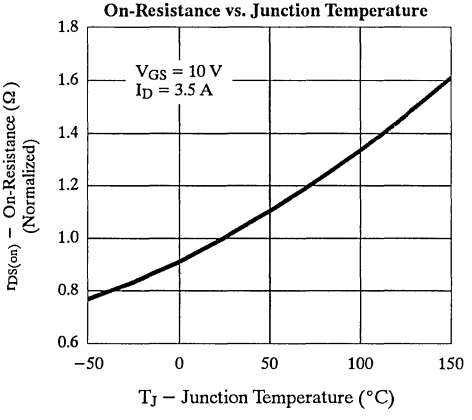
Capacitance



Gate Charge

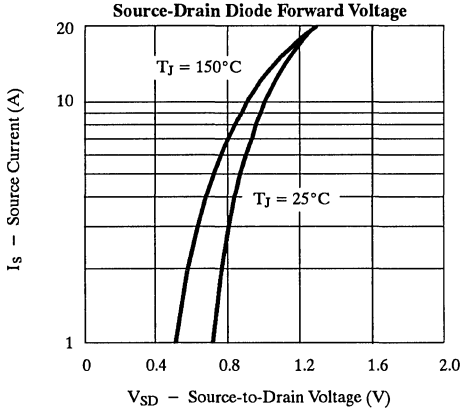


On-Resistance vs. Junction Temperature

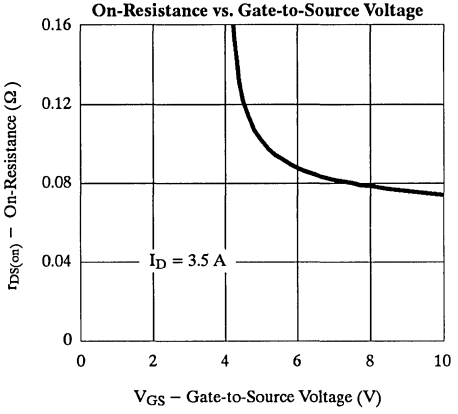


Typical Characteristics (25°C Unless Otherwise Noted)

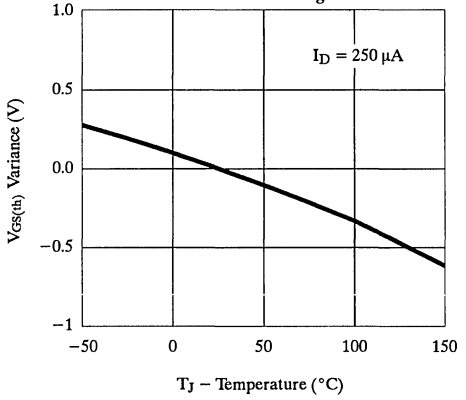
Source-Drain Diode Forward Voltage



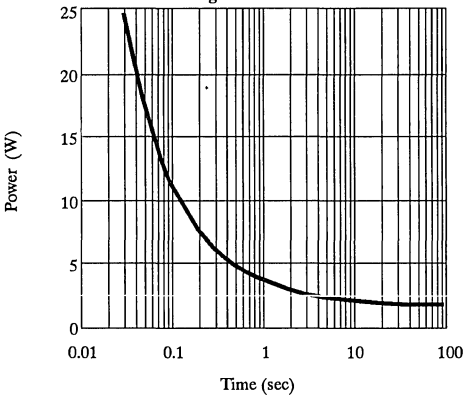
On-Resistance vs. Gate-to-Source Voltage



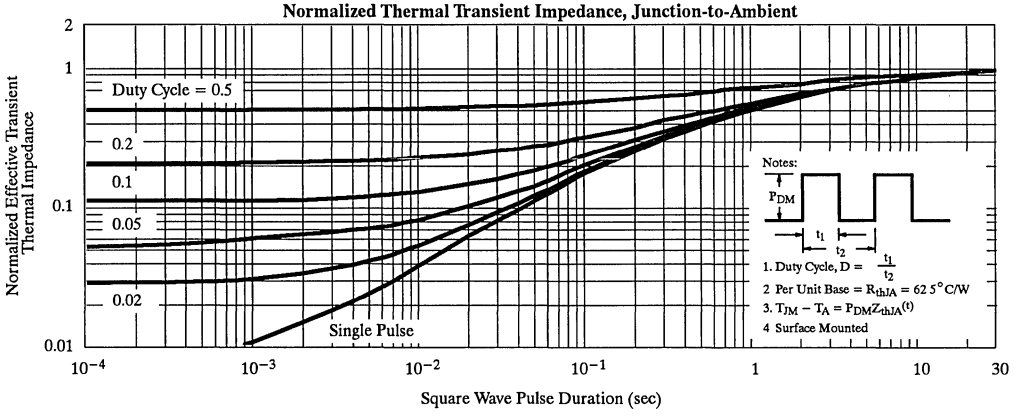
Threshold Voltage



Single Pulse Power

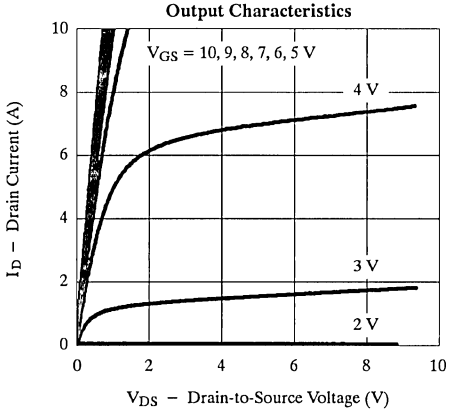


Normalized Thermal Transient Impedance, Junction-to-Ambient

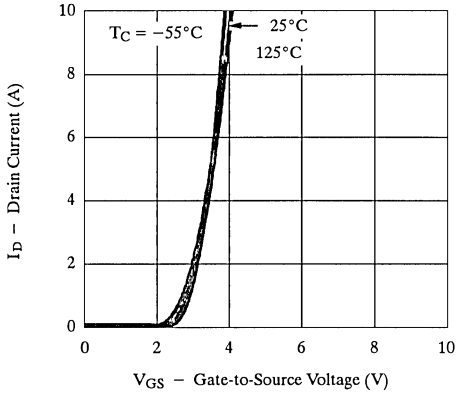


Typical Characteristics (25°C Unless Otherwise Noted) P-Channel

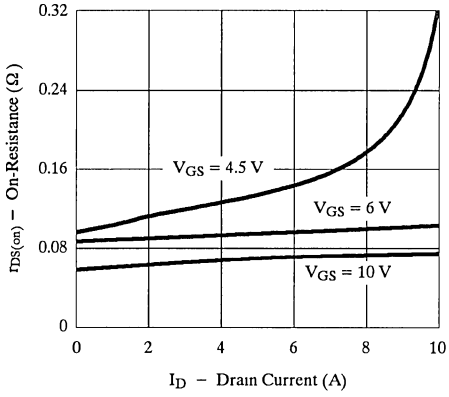
Output Characteristics



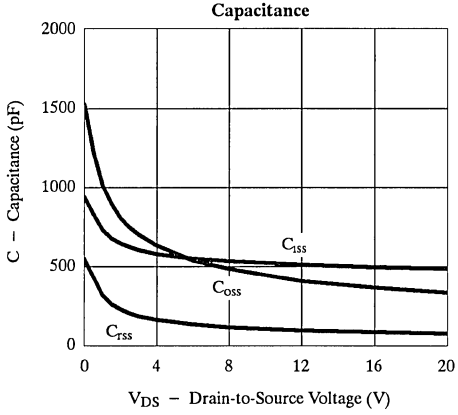
Transfer Characteristics



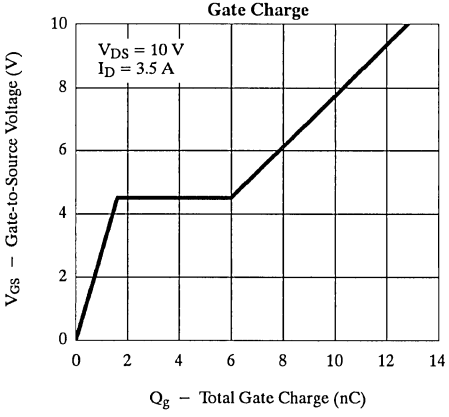
On-Resistance vs. Drain Current



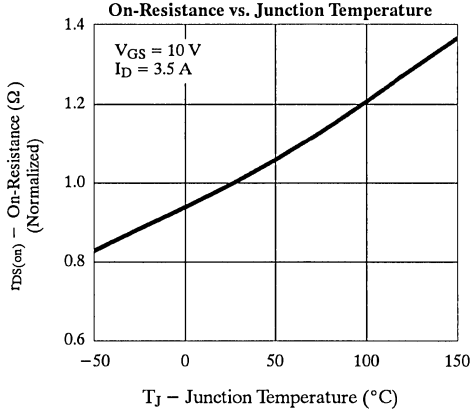
Capacitance



Gate Charge

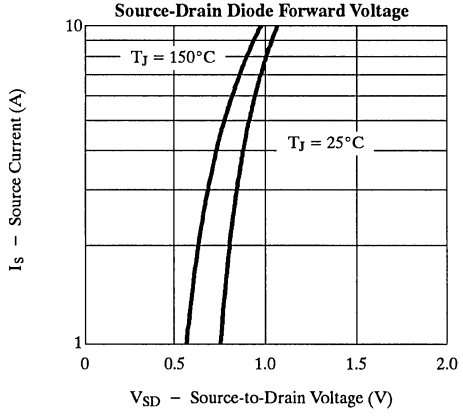


On-Resistance vs. Junction Temperature

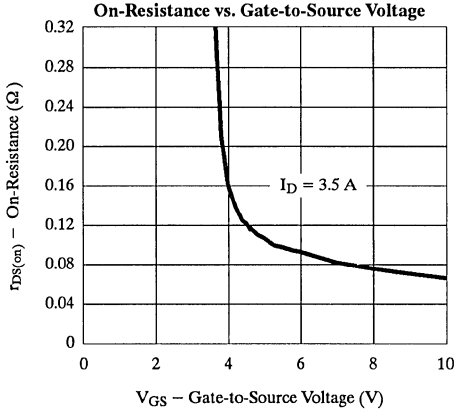


Typical Characteristics (25°C Unless Otherwise Noted)

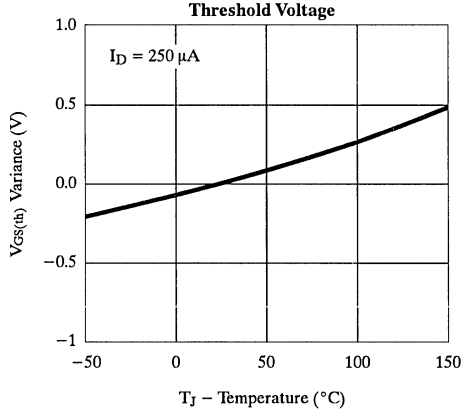
Source-Drain Diode Forward Voltage



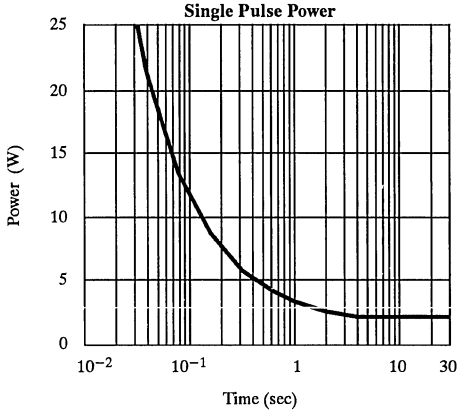
On-Resistance vs. Gate-to-Source Voltage



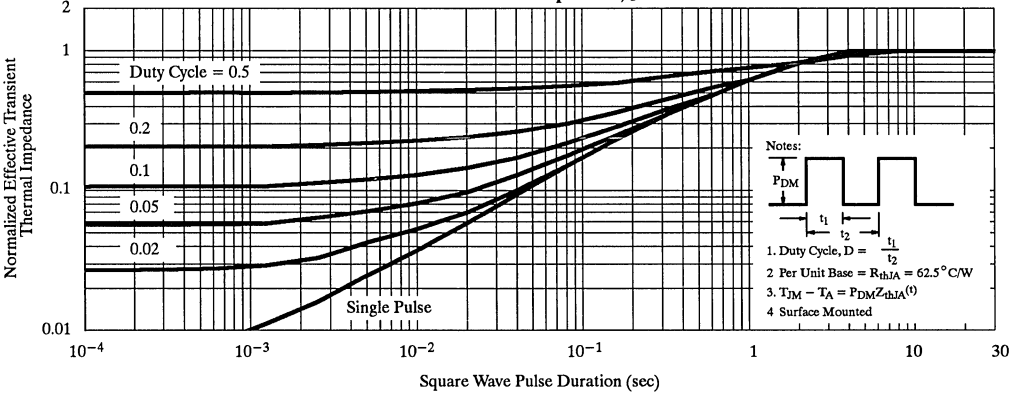
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

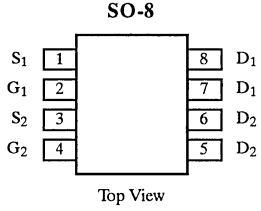
Si9959DY

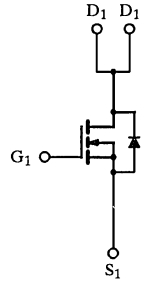
Dual N-Channel Enhancement-Mode MOSFET

Product Summary

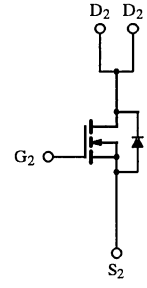
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.30 @ V_{GS} = 10 V	±2.0
	0.50 @ V_{GS} = 5 V	±0.6

For higher performance see Si9945DY





N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.0	A
	T_A = 70°C		±1.6	
Pulsed Drain Current		I_{DM}	±8	
Continuous Source Current (Diode Conduction)		I_S	1.8	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	2	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

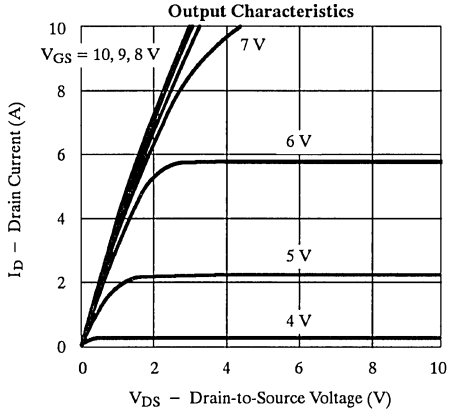
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board)	R_{thJA}	62.5	°C/W

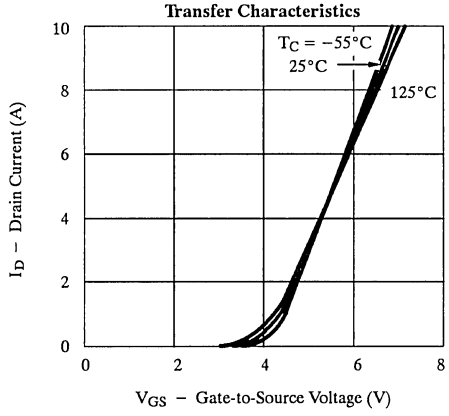
Specifications (T_J = 25°C Unless Otherwise Noted)

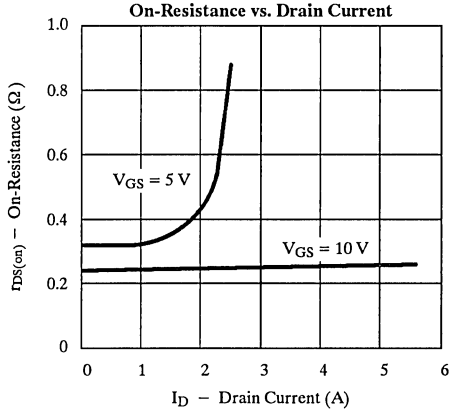
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	8			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.5 A		0.23	0.30	Ω
		V_{GS} = 5 V, I_D = 0.6 A		0.32	0.50	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 2.0 A		2.5		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.85	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 1.3 A		5	15	nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 50 Ω I_D ≅ 0.6 A, V_{GEN} = 10 V, R_G = 6 Ω		7	40	ns
Rise Time	t_r			18	70	
Turn-Off Delay Time	$t_{d(off)}$			40	100	
Fall Time	t_f			23	70	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		70	100	

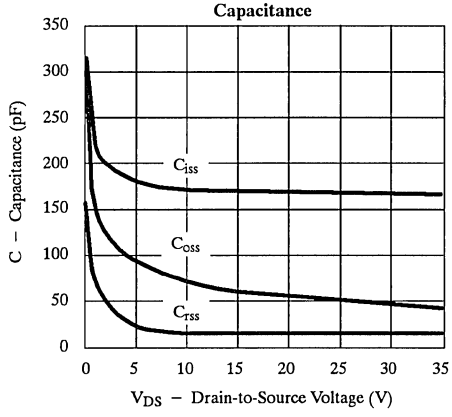
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

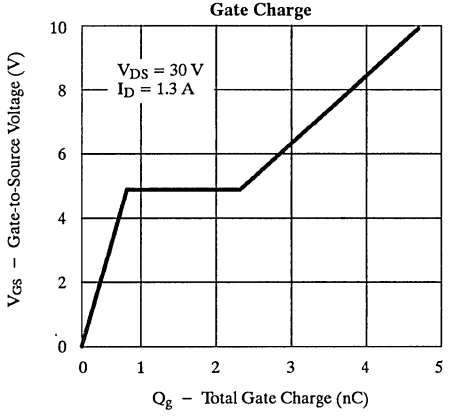
Typical Characteristics (25°C Unless Otherwise Noted)

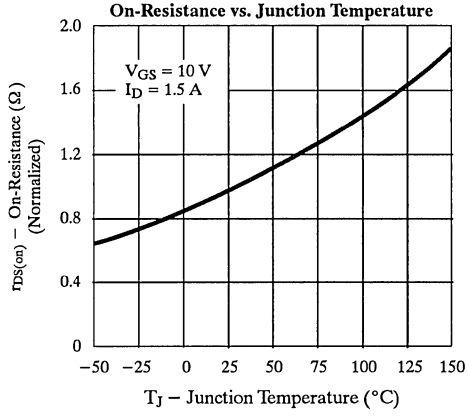




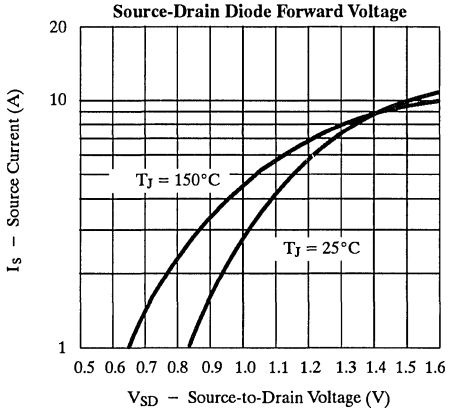


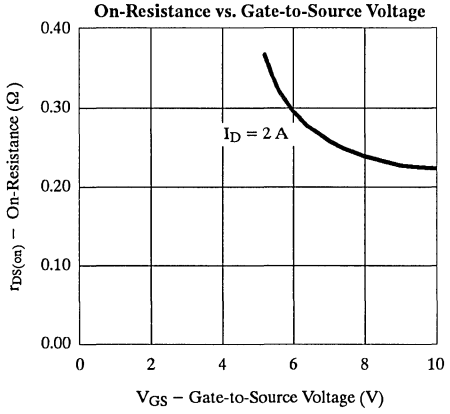


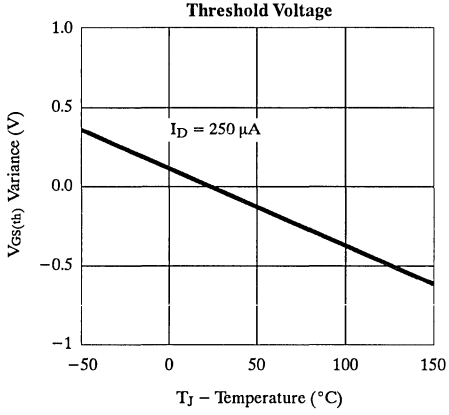


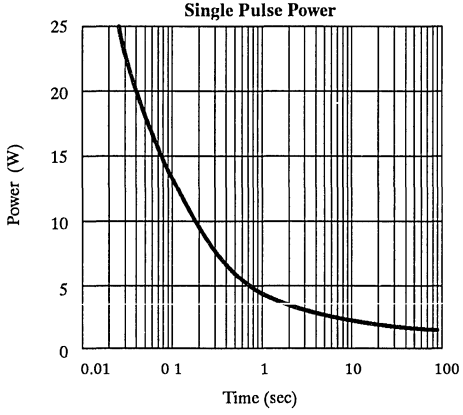


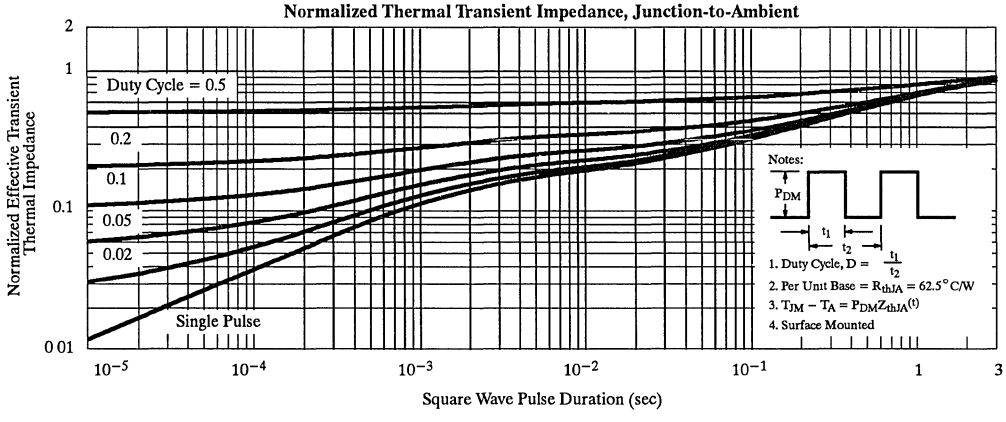
Typical Characteristics (25°C Unless Otherwise Noted)











LITE FOOT™ 2

About LITE FOOT

Combining a TSSOP package with high-density transistor cell technology, Siliconix LITE FOOT™ is the industry's most advanced product for space-sensitive and/or battery operated applications. New LITE FOOT power MOSFETs occupy a mere 6.4 x 3.0 mm of board space and are 30% thinner than the smallest standard power package on the market. With a minuscule height of 1.1 mm, LITE FOOT can slip into even the tightest layouts. LITE FOOT eases design of double-sided circuit boards and is the first family of power MOSFETs thin enough to fit into any standard PCMCIA card.

Siliconix

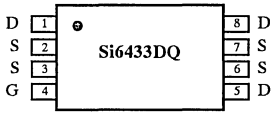
Si6433DQ

P-Channel Enhancement-Mode MOSFET

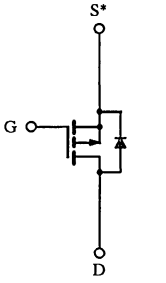
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−12	0.075 @ V_{GS} = −4.5 V	±3.5
	0.110 @ V_{GS} = −2.7 V	±2.9

TSSOP-8



Top View



P-Channel MOSFET

*Source Pins 2, 3, 6 and 7 must be tied common.

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.5	A
	T_A = 70°C		±2.8	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	−1.5	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, t ≤ 10 sec.)	R_{thJA}	83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	−0.7			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −9.6 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −6.0 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−10			A
		V_{DS} ≤ −5 V, V_{GS} = −2.7 V	−4			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4 5 V, I_D = 3 5 A			0 075	Ω
		V_{GS} = −2.7 V, I_D = 2.0 A			0.110	
Forward Transconductance[a]	g_{fs}	V_{DS} = −9 V, I_D = −3.5 A		11		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.5 A, V_{GS} = 0 V		−1.0	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −6 V, V_{GS} = −4.5 V, I_D = −3.5 A			60	nC
Gate-Source Charge	Q_{gs}					
Gate-Drain Charge	Q_{gd}					
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −6 V, R_L = 6 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω			60	ns
Rise Time	t_r				100	
Turn-Off Delay Time	$t_{d(off)}$				180	
Fall Time	t_f				100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.5 A, di/dt = 100 A/µs			100	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

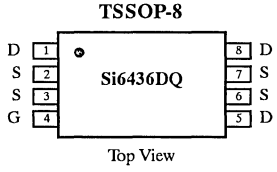
Siliconix

Si6436DQ

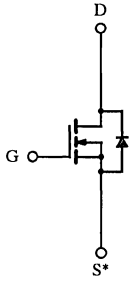
N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.05 @ V_{GS} = 10 V	±4.2
	0.08 @ V_{GS} = 4.5 V	±3.3



Top View



N-Channel MOSFET

*Source Pins 2, 3, 6 and 7 must be tied common.

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±4.2	A
	T_A = 70°C		±3.4	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)		I_S	1.25	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, t ≤ 10 sec.)	R_{thJA}	83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

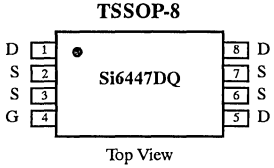
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			20	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.2 A		0.03	0.05	Ω
		V_{GS} = 4.5 V, I_D = 3.3 A		0.06	0.08	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 4.2 A		8		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 4.2 A		13	35	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		12	30	ns
Rise Time	t_r			10	25	
Turn-Off Delay Time	$t_{d(off)}$			25	30	
Fall Time	t_f			10	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		120	160	

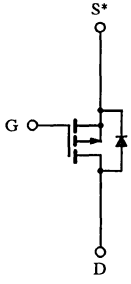
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.10 @ V_{GS} = −10 V	±3.0
	0.19 @ V_{GS} = −4.5 V	±2.2





P-Channel MOSFET

*Source Pins 2, 3, 6 and 7 must be tied common.

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±3.0	A
	T_A = 70°C		±2.4	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	−1.25	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	1.5	W
	T_A = 70°C		1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, t ≤ 10 sec.)	R_{thJA}	83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −10 V, V_{GS} = 0 V, T_J = 70°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ −5 V, V_{GS} = −10 V	−14			A
		V_{DS} ≥ −5 V, V_{GS} = −4.5 V	−2.5			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 3.0 A			0.10	Ω
		V_{GS} = −4.5 V, I_D = 2.0 A			0.19	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −3.0 A		4.0		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.25 A, V_{GS} = 0 V		−0.9	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −3.0 A		13	30	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω		21	40	ns
Rise Time	t_r			12	25	
Turn-Off Delay Time	$t_{d(off)}$			12	30	
Fall Time	t_f			11	20	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.25 A, di/dt = 100 A/µs		50	100	

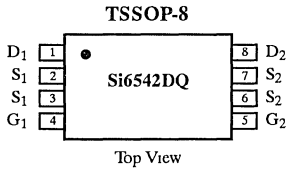
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Si6542DQ

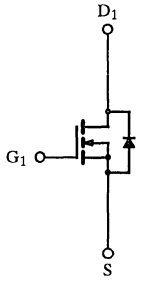
Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

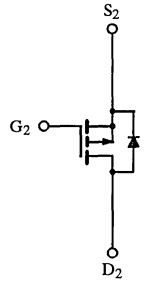
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.100 @ V_{GS} = 10 V	±2.5
		0.200 @ V_{GS} = 4.5 V	±1.7
P-Channel	−20	0.200 @ V_{GS} = −10 V	±1.7
		0.350 @ V_{GS} = −4.5 V	±1.3



Top View



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	−20	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.5	±1.7	A
	T_A = 70°C		±2.0	±1.3	
Pulsed Drain Current		I_{DM}	±20	±15	
Continuous Source Current (Diode Conduction)		I_S	1.25	−1.25	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	1.0		W
	T_A = 70°C		0.64		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, t ≤ 10 sec.)	R_{thJA}	125	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.0			V
		V_{DS} = V_{GS}, I_D = −250 µA	P-Ch	−1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = −16 V, V_{GS} = 0 V	P-Ch			−2	
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C	N-Ch			25	
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C	P-Ch			−25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	N-Ch	14			A
		V_{DS} ≥ −5 V, V_{GS} = −10 V	P-Ch	−10			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A	N-Ch			0.100	Ω
		V_{GS} = −10 V, I_D = 1.7 A	P-Ch			0.200	
		V_{GS} = 4.5 V, I_D = 1.7 A	N-Ch			0.200	
		V_{GS} = −4.5 V, I_D = 1.3 A	P-Ch			0.350	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 2.5 A	N-Ch				S
		V_{DS} = −15 V, I_D = − 1.7 A	P-Ch				
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V	N-Ch			1.2	V
		I_S = −1.25 A, V_{GS} = 0 V	P-Ch			−1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 10 V, I_D = 2.5 A P-Channel V_{DS} = −10 V, V_{GS} = −10 V, I_D = −1.7 A	N-Ch			50	nC
			P-Ch			25	
Gate-Source Charge	Q_{gs}		N-Ch				
			P-Ch				
Gate-Drain Charge	Q_{gd}		N-Ch				
			P-Ch				
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω, I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω P-Channel V_{DD} = −10 V, R_L = 10 Ω, I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω	N-Ch			20	ns
			P-Ch			40	
Rise Time	t_r		N-Ch			20	
			P-Ch			40	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch			90	
			P-Ch			90	
Fall Time	t_f		N-Ch			50	
			P-Ch			50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs	N-Ch			100	
		I_F = −1.25 A, di/dt = 100 A/µs	P-Ch			100	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

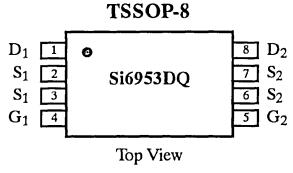
Siliconix

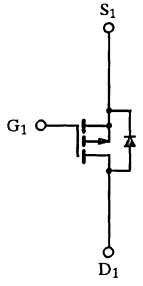
Si6953DQ

Dual P-Channel Enhancement-Mode MOSFET

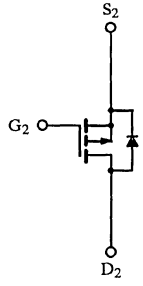
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.200 @ V_{GS} = −10 V	±1.7
	0.350 @ V_{GS} = −4.5 V	±1.3





P-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±1.7	A
	T_A = 70°C		±1.3	
Pulsed Drain Current		I_{DM}	±15	
Continuous Source Current (Diode Conduction)		I_S	−1.25	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, t ≤ 10 sec.)	R_{thJA}	125	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −16 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C			−25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ −5 V, V_{GS} = −10 V	−10			A
		V_{DS} ≥ −5 V, V_{GS} = −4.5 V	−1.5			
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = 1.7 A			0.200	Ω
		V_{GS} = −4.5 V, I_D = 1.3 A			0.350	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −1.7 A				S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.7 A, V_{GS} = 0 V			−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −10 V, I_D = −1.7 A			25	nC
Gate-Source Charge	Q_{gs}					
Gate-Drain Charge	Q_{gd}					
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −10 V, R_G = 6 Ω			40	ns
Rise Time	t_r				40	
Turn-Off Delay Time	$t_{d(off)}$				90	
Fall Time	t_f				50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.7 A, di/dt = 100 A/µs			100	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

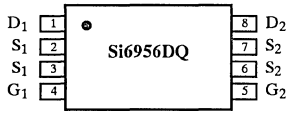
Si6956DQ

Dual N-Channel Enhancement-Mode MOSFET

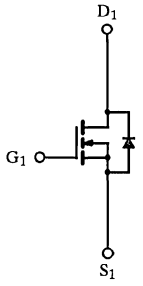
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.10 @ V_{GS} = 10 V	±2.5
	0.20 @ V_{GS} = 4.5 V	±1.7

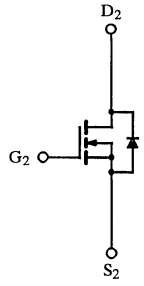
TSSOP-8



Top View



N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_A = 25°C	I_D	±2.5	A
	T_A = 70°C		±2.0	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)		I_S	1.25	
Maximum Power Dissipation (Surface Mounted on FR4 Board)	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient (Surface Mounted on FR4 Board, t ≤ 10 sec.)	R_{thJA}	125	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			2	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	14			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A			0.10	Ω
		V_{GS} = 4.5 V, I_D = 1.7 A			0 20	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 2.5 A				S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V			1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 2.5 A			50	nC
Gate-Source Charge	Q_{gs}					
Gate-Drain Charge	Q_{gd}					
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω			20	ns
Rise Time	t_r				20	
Turn-Off Delay Time	$t_{d(off)}$				90	
Fall Time	t_f				50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs			100	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Power Conversion, PCMCIA Interface & Battery Management

3

About Power Management

Siliconix IC products for power control, conversion, and switching combine the functions of two or more discretes in the same package and add useful protection features to ensure the reliability of designs. A popular series of switchmode control ICs designed especially for the communications market simplifies the design of line cards, network terminators, battery adapters, and cable television repeaters. A family of regulator and controller ICs designed for use with LITTLE FOOT discretes offers the optimal level of integration for dc-to-dc conversion in battery-operated equipment, including laptop and notebook computers. Highly-integrated products for the PCMCIA slot interface and for multiple battery-pack designs reduce parts count significantly, and simplify both design and user operation.

Siliconix

Si9100

3-W High-Voltage Switchmode Regulator

Features

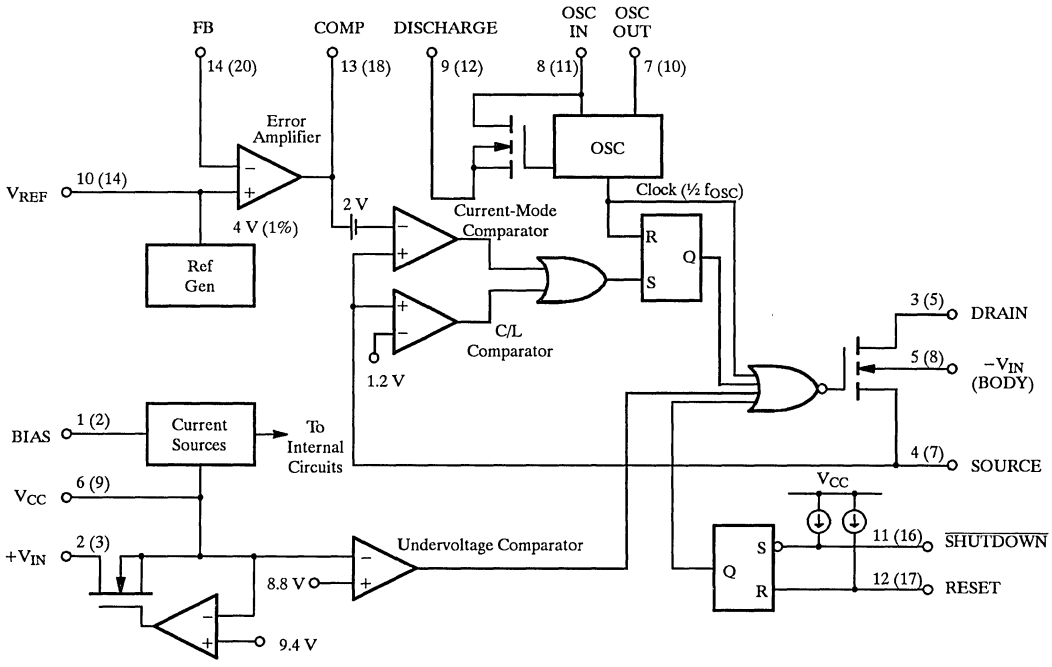
- 10- to 70-V Input Range
- Current-Mode Control
- On-Chip 150-V, 5-Ω MOSFET Switch
- Reference Selection
  Si9100 – ±1%
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

Description

The Si9100 high-voltage switchmode regulators are monolithic BiC/DMOS integrated circuits which contain most of the components necessary to implement high-efficiency dc-to-dc converters up to 3 watts. They can either be operated from a low-voltage dc supply, or directly from a 10- to 70-V unregulated dc power source. The Si9100 may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward), or by using a level shift circuit can generate a +5-V or a −5-V non-isolated output from a −48-V source.

The Si9100 is available in 14-pin plastic DIP and 20-pin PLCC packages. It is specified over the industrial, D suffix (−40 to 85°C) temperature ranges.

Functional Block Diagram



Note: Figures in parenthesis represent pin numbers for 20-pin package.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 70 V
V_{DS} ..... 150 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2.5 A
I_D (rms) ..... 350 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 3 mA
Storage Temperature ..... -65 to 125°C
Operating Temperature ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
20-Pin PLCC (N Suffix)[c] ..... 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 11.2 mW/°C above 25°C

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 70 V
t_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 24 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified $\overline{\text{DISCHARGE}} = -V_{IN} = 0$ V $V_{CC} = 10$ V, $+V_{IN} = 48$ V $R_{BIAS} = 390$ kΩ, $R_{OSC} = 330$ kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) $R_L = 10$ MΩ	Room	3.92	4.0	4.08	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	$R_{OSC} = 0$	Room	1	3		MHz
Initial Accuracy	f_{OSC}	$R_{OSC} = 330$ kΩ, See Note f	Room	80	100	120	kHz
		$R_{OSC} = 150$ kΩ, See Note f	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f = f(13.5\text{ V}) - f, (9.5\text{ V})/f(9.5\text{ V})$	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC In = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, $V_{FB} = 4$ V	Room		25	500	nA

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	D Suffix D Suffix −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Error Amplifier (Cont'd)							
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$, (OSC Disabled)	Room		±15	±40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room		1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	SOURCE (V_{FB} = 3.4 V)	Room		−2.0	−1.4	mA
		SINK (V_{FB} = 4.5 V)	Room	0.12	0.15		
Power Supply Rejection	PSRR	OSC IN = $-V_{IN}$, (OSC Disabled)	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC}, V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC}, V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room			70	V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = V_{UVLO}	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC}, See Detailed Description	Room	7.0	8.8	9.2	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width[e] $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	D Suffix D Suffix −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
MOSFET Switch							
Breakdown Voltage	$V_{(BR)DSS}$	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V, I_{DRAIN} = 100 µA	Full	150	180		V
Drain-Source On Resistance[g]	$r_{DS(on)}$	V_{SOURCE} = 0 V, I_{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I_{DSS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V, V_{DRAIN} = 100 V	Room			10	µA
Drain Capacitance	C_{DS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V	Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF
g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

Timing Waveforms

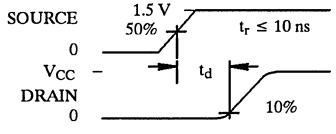


Figure 1.

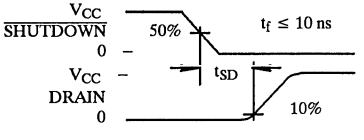


Figure 2.

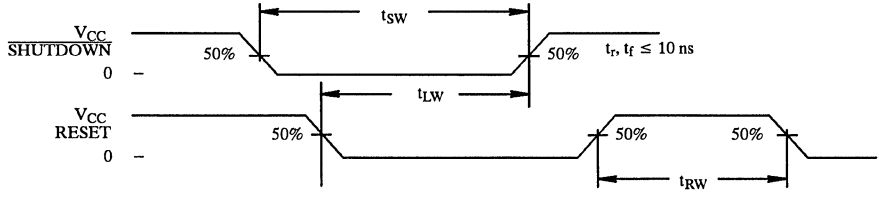
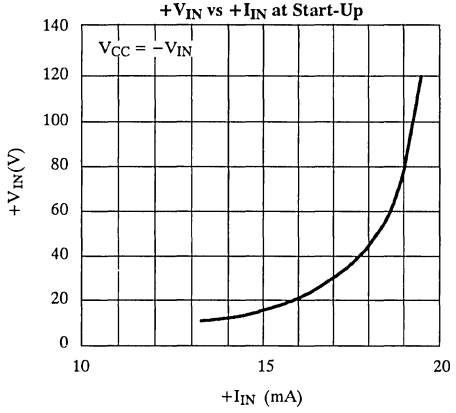
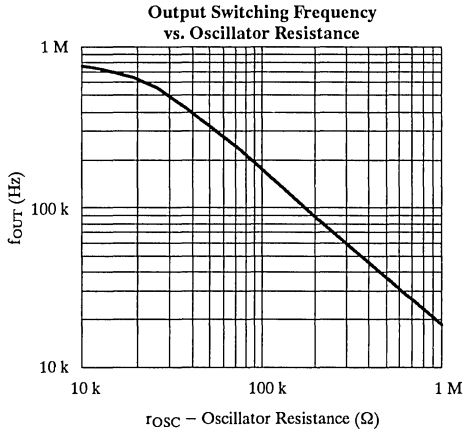


Figure 3.

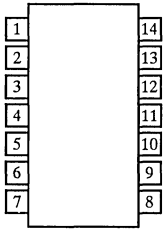
Typical Characteristics





Pin Configurations

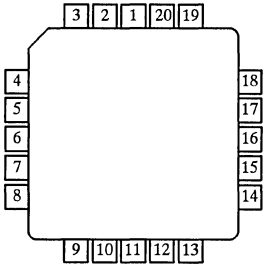
PDIP-14



Top View

Order Number
Plastic DIP: Si9100DJ

PLCC-20



Top View

Order Number
Plastic PLCC: Si9100DN

Function	Pin	
	14-Pin DIP	20-Pin PLCC*
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20
*Pins 1, 4, 6, 13, 15, and 19 = N/C		

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9100, a 390-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Reference Section

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. During the reference trimming procedure the error amplifier is connected for unity gain in order to compensate for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-μs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

Detailed Description (Cont'd)

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

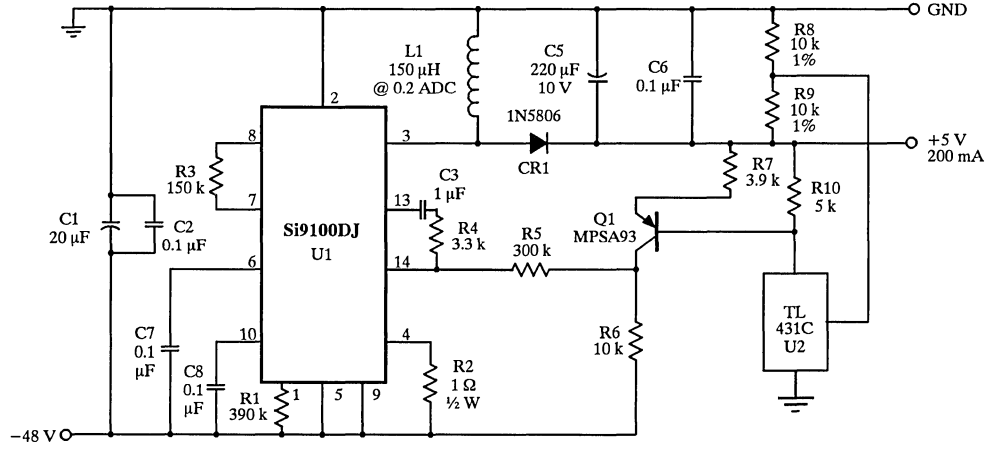
$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	↿	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
∫	L	Off (Latched, No Change)

Output Switch

The output switch is a 5-Ω, 150-V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

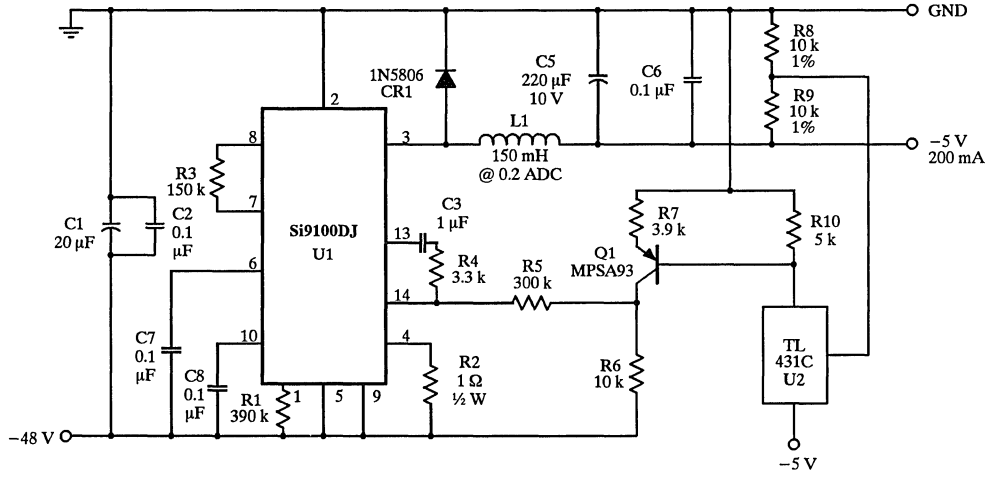
Applications

Buck–Boost
Non-Isolated 1-W Supply

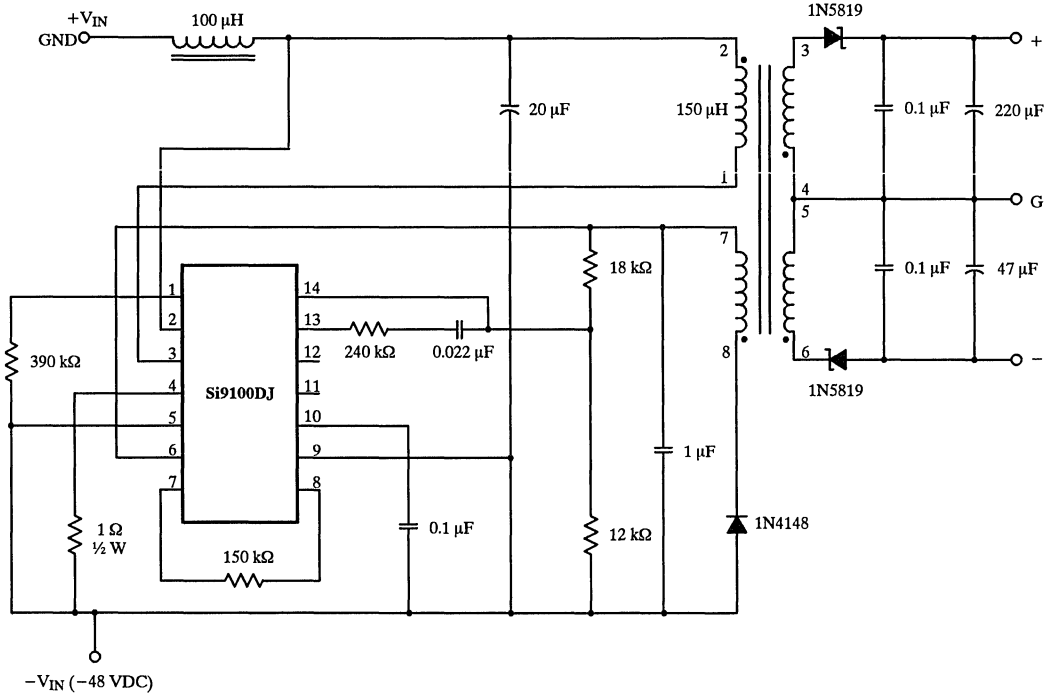


Applications (Cont'd)

Non-Isolated 1-W Supply (Buck)



One-Watt Flyback Converter for Telecommunications Power Supplies*



* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN713 and AN702.

Siliconix

Si9102

3-W High-Voltage Switchmode Regulator

Features

- 10- to 120-V Input Range
- Current-Mode Control
- On-chip 200-V, 7-Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

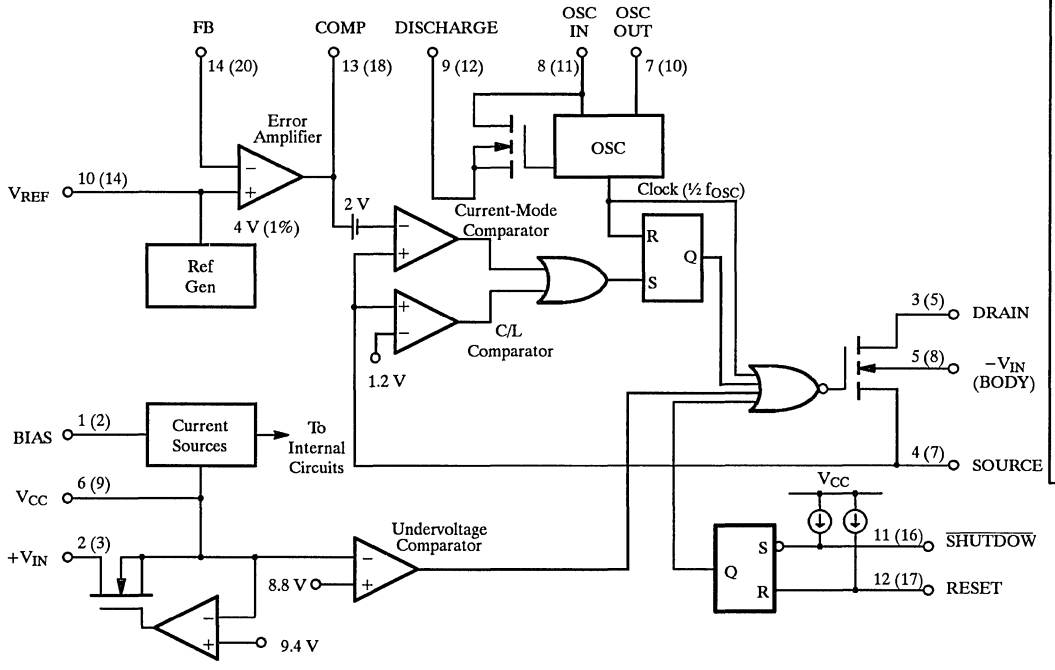
Description

The Si9102 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9102 is available in 14-pin plastic DIP and 20-pin PLCC packages, and is specified over the D suffix (−40 to 85°C) temperature range.

Functional Block Diagram



Note: Figures in parenthesis represent pin numbers for 20-pin package.

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (Note: 300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 3 mA
Storage Temperature ..... -65 to 125°C
Operating Temperature ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)a
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
20-Pin PLCC (N Suffix)[c] ..... 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 11.2 mW/°C above 25°C

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full	3.92 3.86	4.0	4.08 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ[g]	Room	80	100	120	kHz
		R_{OSC} = 150 kΩ[g]	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) − f(9.5 V)/f(9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V, OSC IN = $-V_{IN}$ (OSC Disabled)	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room	0.7	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Error Amplifier (Cont'd)							
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		−2.0	−1.4	mA
Input OFFSET Voltage	V_{OS}	OSC IN = − V_{IN} (OSC Disabled)	Room		±15	±40	mV
Output Current	I_{OUT}	Sink (V_{FB} = 4.5 V)	Room	0.12	0.15		mA
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room			120	V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.2	
V_{REG}, $-V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Widthe $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
MOSFET Switch							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On Resistance[f]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room			7	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	Room		5	10	µA
Drain Capacitance	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.
g. C_{STRAY} Pin 8 = ≤ 5 pF

Timing Waveforms

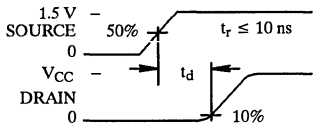


Figure 1.

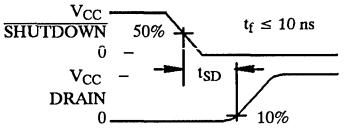


Figure 2.

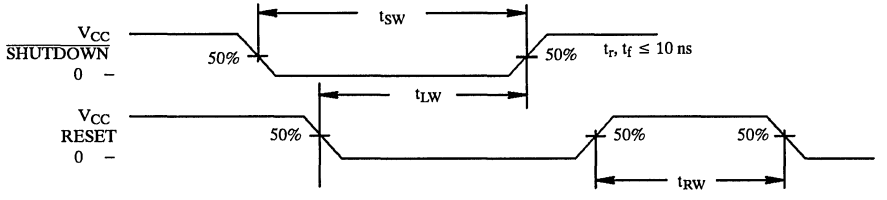
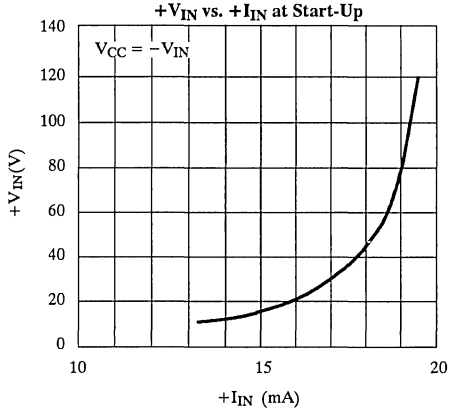
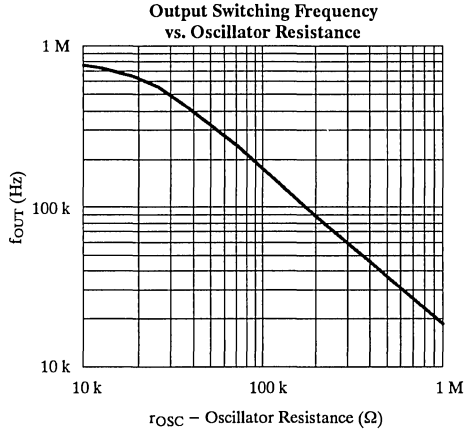


Figure 3.

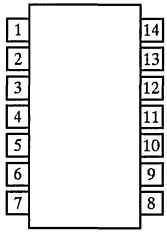
Typical Characteristics





Pin Configurations

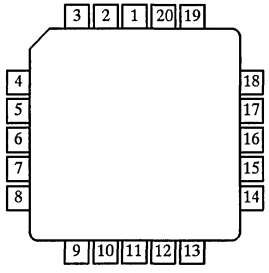
PDIP-14



Top View

Order Number
Plastic DIP: Si9102DJ

PLCC-20



Top View

Order Number
Plastic PLCC: Si9102DN

Function	Pin	
	14-Pin DIP	20-Pin PLCC*
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20
*Pins 1, 4, 6, 13, 15, and 19 = N/C		

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current

is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8-V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4-V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at start-up as a function of input voltage.

BIAS

To properly set the bias for the Si9102, a 390-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC in and OSC out pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

Detailed Description (Cont'd)

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET. $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

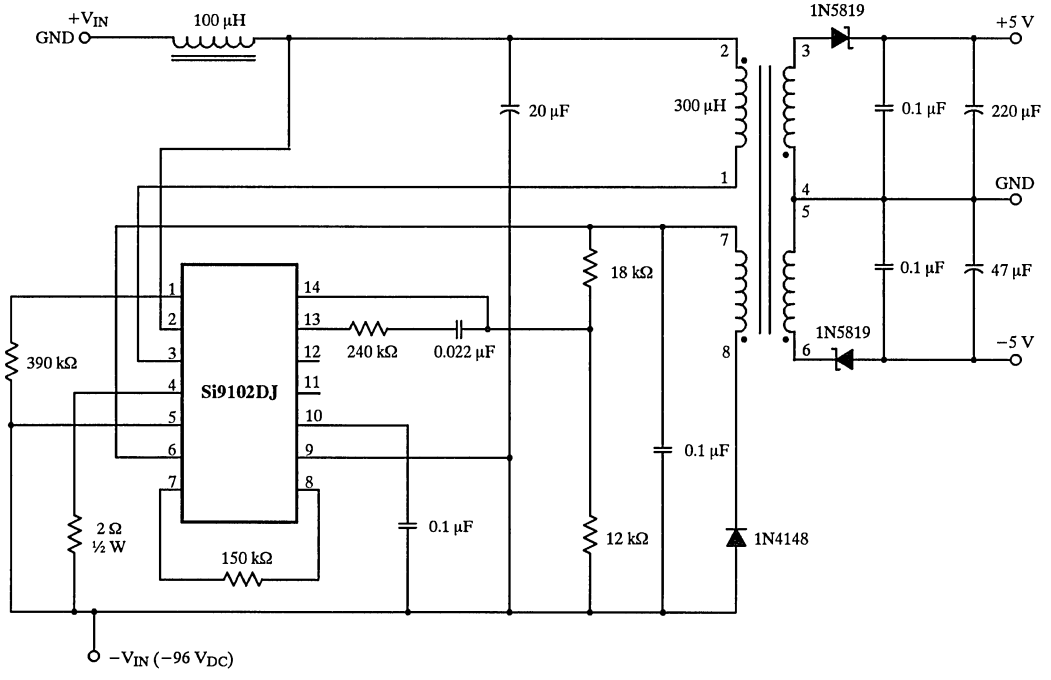
$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	⌐	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌐	L	Off (Latched, No Change)

Output Switch

The output switch is a 7-Ω , 200-V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Applications

Flyback Converter for Double Battery Telecommunications Power Supplies



Si9104

High-Voltage Switchmode Regulator

Features

- 10- to 120-V Input Range
- Current-Mode Control
- On-Chip 200-V, 5-Ω MOSFET Switch
- $\overline{\text{SHUTDOWN}}$ and RESET
- High Efficiency Operation (>80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

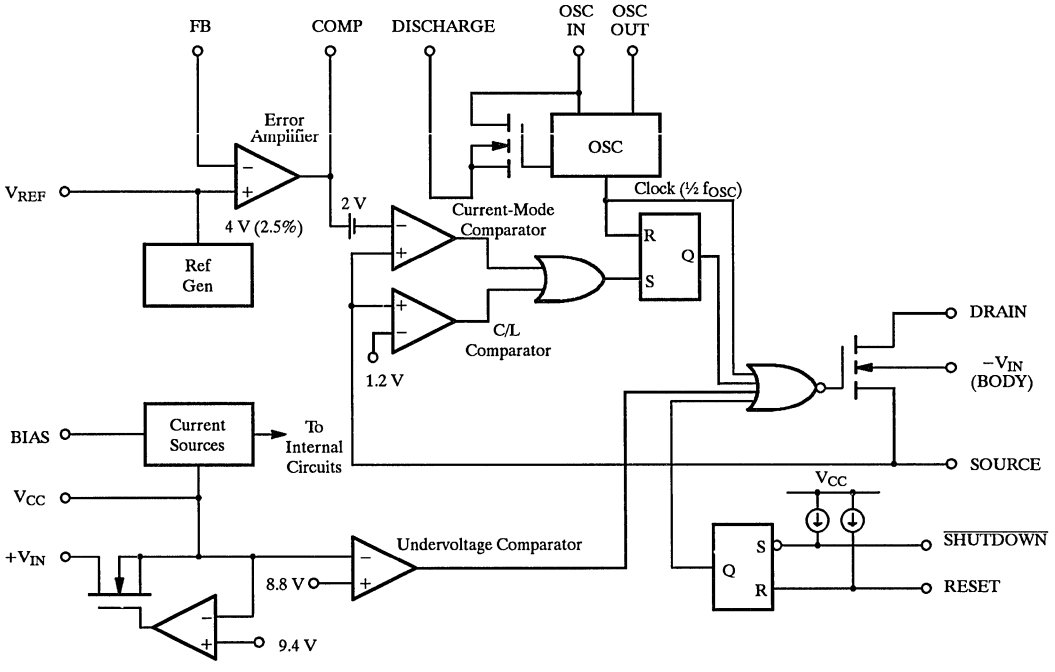
Description

The Si9104 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9104 is available in a 16-pin wide-body SOIC, 14-pin plastic DIP, and 20-pin PLCC, and are specified over the D suffix (−40 to 85°C) temperature range.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (300 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 3 mA
Storage Temperature ..... -65 to 125°C
Operating Temperature ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[a]
14-Pin Plastic DIP[b] ..... 750 mW
16-Pin Plastic Wide-Body SOIC[c] ..... 900 mW
20-Pin PLCC[d] ..... 1400 mW
Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
16-Pin Plastic Wide-Body SOIC ..... 140°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.
d. Derate 11.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 10 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to 7 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full	3.92 3.85	4.0	4.08 4.15	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.25	1.0	mV/°C
Long Term Stability[e]		t = 1000 hrs., T_A = 125°C	Room		5	25	mV
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 kΩ [f]	Room	80	100	120	kHz
		R_{OSC} = 150 kkΩ [f]	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) − f(10 V) / f(10 V)	Room	4	10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room		±15	±40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	60	80		dB
Unity Gain Bandwidth[e]	BW		Room	0.7	1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room		1000	2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		−2.0	−1.4	mA
		Sink (V_{FB} = 4.5 V)	Room	0.12	0.15		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC}, V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		100	200	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room	120			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	9.4	9.8	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.8	9.3	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}		Room	0.45	0.6	1.0	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width[e] $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Logic (Cont'd)							
Input Current Input Voltage High	I_{IH}	$V_{IN} = V_{CC}$	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		µA
MOSFET Switch							
Breakdown Voltage	$V_{BR(DSS)}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On-Resistance[g]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 150 V	Room		5	10	µA
Drain Capacitance[e]	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} @ OSC IN ≤ 5 pF.
g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

Timing Waveforms

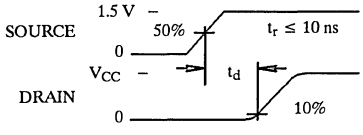


Figure 1.

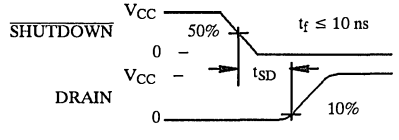


Figure 2.

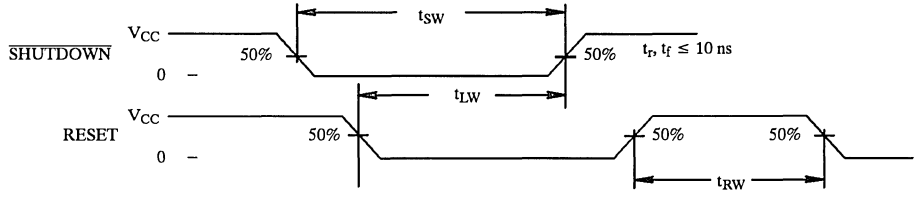
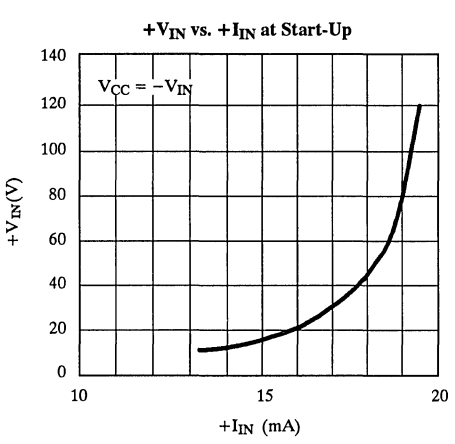
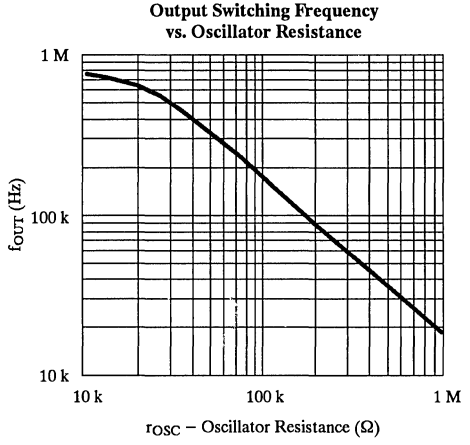


Figure 3.

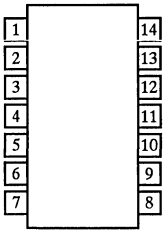
Typical Characteristics





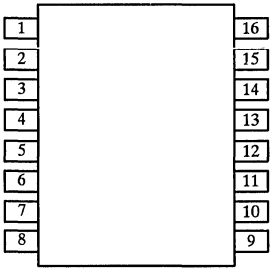
Pin Configurations

PDIP-14



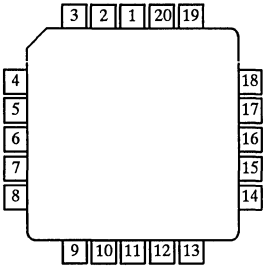
Top View
Order Number: Si9104DJ

SO-16
(Wide-Body)



Top View
Order Number: Si9104DW

PLCC-20



Top View
Order Number: Si9104DN

Pin Configurations (Cont'd)

Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
$-V_{IN}$	5	2	8
V_{CC}	6	4	9
OSC_{OUT}	7	5	10
OSC_{IN}	8	6	11
DISCHARGE	9	7	12
V_{REF}	10	8	14
$\overline{SHUTDOWN}$	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
$+V_{IN}$	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9104 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.4 V. If V_{CC} is not forced to exceed the 9.4-V threshold, then V_{CC} will be regulated to a nominal value of 9.4 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.8 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: During start-up or when V_{CC} drops below 9.4-V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. For typical pre-regulator current at start-up as a function of input voltage see Typical Characteristics, "$+V_{IN}$ vs. $+I_{IN}$ at Start-Up" (page 3-20).

BIAS

To properly set the bias for the Si9104, a 390-k Ω resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{SHUTDOWN}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

Detailed Description (Cont'd)

Reference Section

The reference section of the Si9104 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9104 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1.0% of 4 V. This compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with negative feedback compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a capacitor to ground (0.1 µF typically).

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between OSC IN and OSC OUT. (See Applications section for details of resistor value vs. frequency.) The DISCHARGE should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	⌝L	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌟	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Output Switch

The output switch is a 5-Ω, 200-V lateral DMOS device. Like discrete power MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9104 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Applications

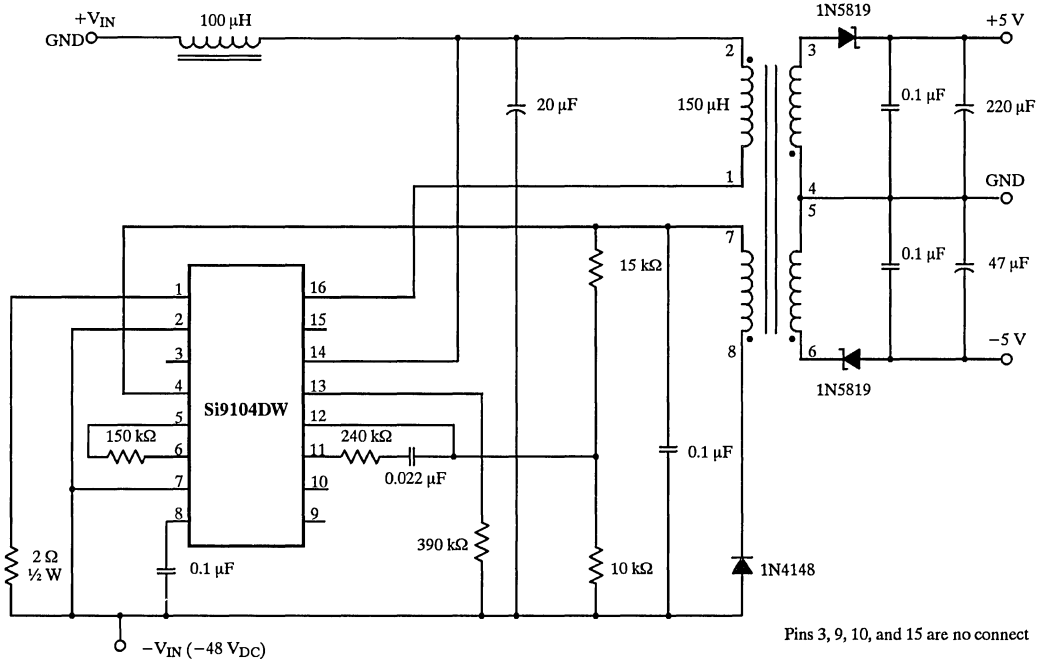


Figure 4. One-Watt Flyback Converter for Telecommunications Power Supplies

Si9105

1-W High-Voltage Switchmode Regulator

Features

- CCITT Compatible
- Current-Mode Control
- Low Power Consumption (less than 5 mW)
- 10- to 120-V Input Range
- 200-V, 250-mA MOSFET
- Internal Start-Up Circuit
- Current-Mode Control
- $\overline{\text{SHUTDOWN}}$ and RESET

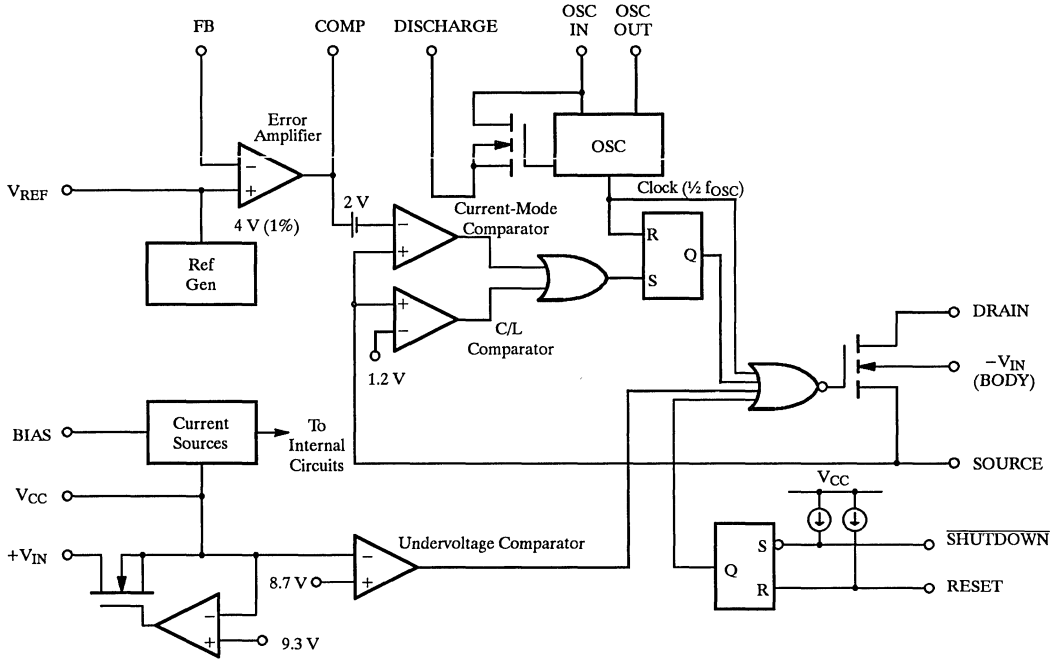
Description

The Si9105 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc/dc converter in ISDN terminals up to 3 watts. A 0.5-mA max supply current makes possible the design of a dc/dc converter with 60% efficiency at 25 mW, therefore meeting the recommended performance under the CCITT I.430 specifications.

This device may be used with an appropriate transformer to implement isolated flyback power converter topologies to provide single or multiple regulated dc outputs (i.e., ±5 V).

The Si9105 is available in 16-pin wide-body SOIC, 14-pin plastic, and 20-pin PLCC packages, and is specified over the industrial, D suffix (−40 to 85°C) temperature range.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
V_{DS} ..... 200 V
I_D (Peak) (200 µs pulse, 2% duty cycle) ..... 2 A
I_D (rms) ..... 250 mA
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) ..... −0.3 V to V_{CC} + 0.3 V
Linear Inputs (FEEDBACK, SOURCE) ..... −0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 5 mA
Storage Temperature ..... −65 to 125°C
Operating Temperature ..... −40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[a]
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
16-Pin Plastic Wide-Body SOIC (W Suffix)[c] ..... 900 mW
20-Pin PLCC (N Suffix)[d] ..... 1400 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
16-Pin Plastic Wide-Body SOIC ..... 140°C/W
20-Pin PLCC ..... 90°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C
c. Derate 7.2 mW/°C above 25°C
d Derate 11.2 mW/°C above 25°C

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 10 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to V_{CC} − 3 V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Reference							
Output Voltage	V_R	OSC IN = V_{IN} (OSC Disabled) R_L = 10 MΩ	Room	3.92	4.00	4.08	V
Output Impedance[e]	Z_{OUT}	OSC IN = $-V_{IN}$	Room	15	300	45	kΩ
Short Circuit Current	I_{SREF}	OSC IN = $-V_{IN}$, $V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}	OSC IN = $-V_{IN}$	Full		0.25	1.0	mV/°C
Long Term Stability[e]		t = 1000 hrs, T_A = 125°C	Room		5.00	25.00	mV
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	See Note e	Room	32	40	48	kHz
Voltage Stability	Δf/f	Δf/f = f (13.5 V) − f (9.5 V)/f (9.5 V)	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4	4.04	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room	60	80		dB

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
Error Amplifier (Cont'd)							
Input Offset Voltage	V_{OS}	OSC IN = $-V_{IN}$	Room		±15	±40	mV
Unity Gain Bandwidth[e]	BW		Room	0.5	0.8		MHz
Dynamic Output Impedance	Z_{OUT}		Room		1		kΩ
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room		−1.2	−0.32	mA
		Sink (V_{FB} = 4.5 V)	Room	0.05	0.08		
Power Supply Rejection	PSRR	10 V ≤ V_{CC} ≤ 13.5 V	Room		70		dB
Current Limit							
Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC} V_{FB} = 0 V	Room	0.8	1.0	1.2	V
Delay to Output[e]	t_d	R_L = 100 Ω from DRAIN to V_{CC} V_{SOURCE} = 1.5 V, See Figure 1	Room		200	300	ns
Input Voltage	$+V_{IN}$	I_{IN} = 100 µA	Room	120			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 10 V	Room			10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = 7 V	Room	8	15		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.5	9.3	9.7	V
Undervoltage Lockout	V_{UVLO}	R_L = 100 Ω from DRAIN to V_{CC} See Detailed Description	Room	7.0	8.7	9.2	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.25	0.5		
Suppiy							
Supply Current	I_{CC}		Room		0.35	0.5	mA
Bias Current	I_{BIAS}		Room		7.5		µA
$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width	t_{RW}		Room	50			
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 820 kΩ, R_{OSC} = 910 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[d]	Unit
MOSFET Switch							
Breakdown Voltage	$V_{(BR)DSS}$	I_{DRAIN} = 100 µA	Full	200	220		V
Drain-Source On Resistance[g]	$r_{DS(on)}$	I_{DRAIN} = 100 mA	Room		5	7	Ω
Drain Off Leakage Current	I_{DSS}	V_{DRAIN} = 100 V	Room			10	µA
Drain Capacitance	C_{DS}		Room		35		pF

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF
g. Temperature coefficient of $r_{DS(on)}$ is 0.75% per °C, typical.

Timing Waveforms

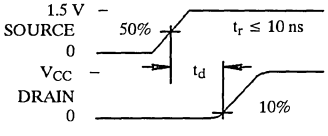


Figure 1.

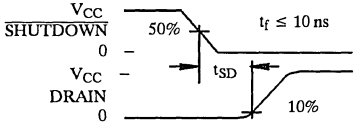


Figure 2.

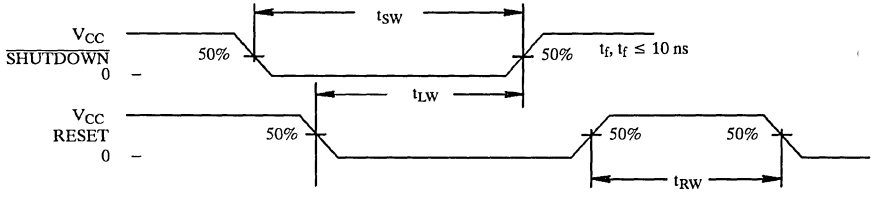
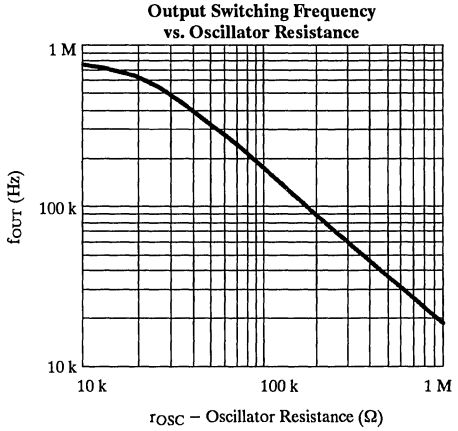


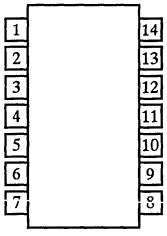
Figure 3.

Typical Characteristics



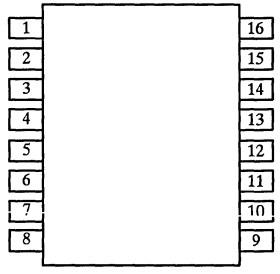
Pin Configurations

PDIP-14



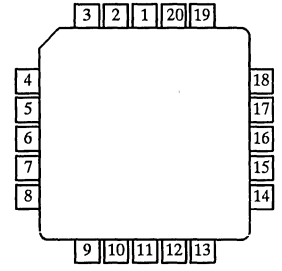
Top View
Order Number: Si9105DJ

SO-16 (Wide-Body)



Top View
Order Number: Si9105DW

PLCC-20



Top View
Order Number: Si9105DN

Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
$-V_{IN}$	5	2	8
V_{CC}	6	4	9
OSC_{OUT}	7	5	10
OSC_{IN}	8	6	11
DISCHARGE	9	7	12
V_{REF}	10	8	14
SHUTDOWN	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
$+V_{IN}$	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9105 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC}. This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 9.3 V. If V_{CC} is not forced to exceed the 9.3-V threshold, then V_{CC} will be regulated to a nominal value of 9.3 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.7 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will not exceed the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

BIAS

To properly set the bias for the Si9105, a 820-kΩ resistor should be tied from BIAS to $-V_{IN}$. This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 7.5 µA.

Reference Section

The reference section of the Si9105 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9105 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, whose 1-kΩ dynamic output impedance enables it to be used with feedback compensation (unlike transconductance amplifiers). A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics graph of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to a maximum of 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to OSC IN.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ and RESET are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ pin to provide variable shutdown time.

Detailed Description (Cont'd)

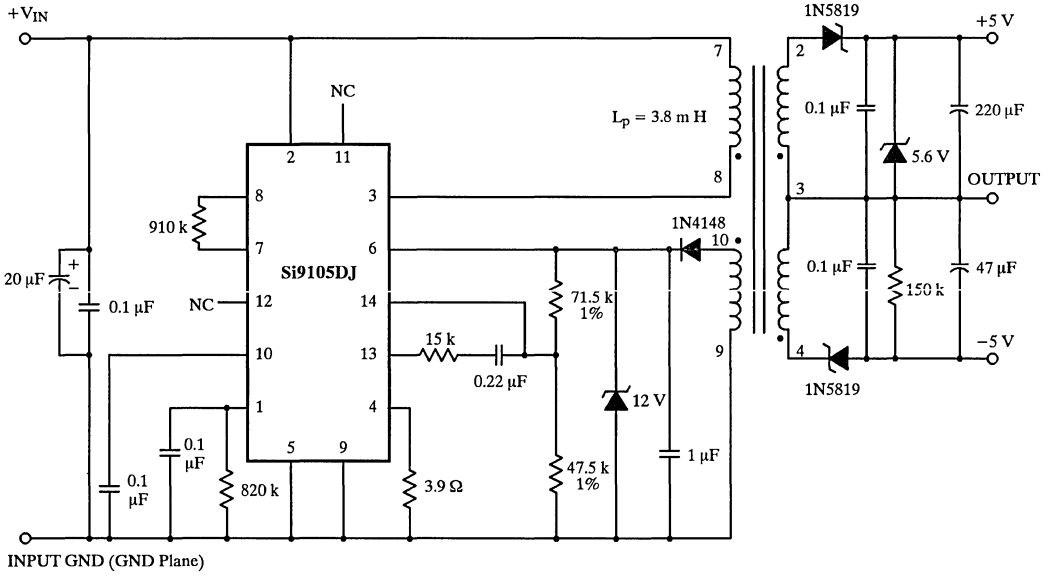
Output Switch

The output switch is a 7-Ω, 200-V lateral DMOS transistor. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9105 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

Table Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	⌝L	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌟H	L	Off (Latched, No Change)

Applications



CCITT Compatible ISDN Terminal Power Supply

High-Voltage Switchmode Controllers

Features

- 10- to 120-V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET
- Reference Selection
  Si9110 – ±1%
  Si9111 – ±10%

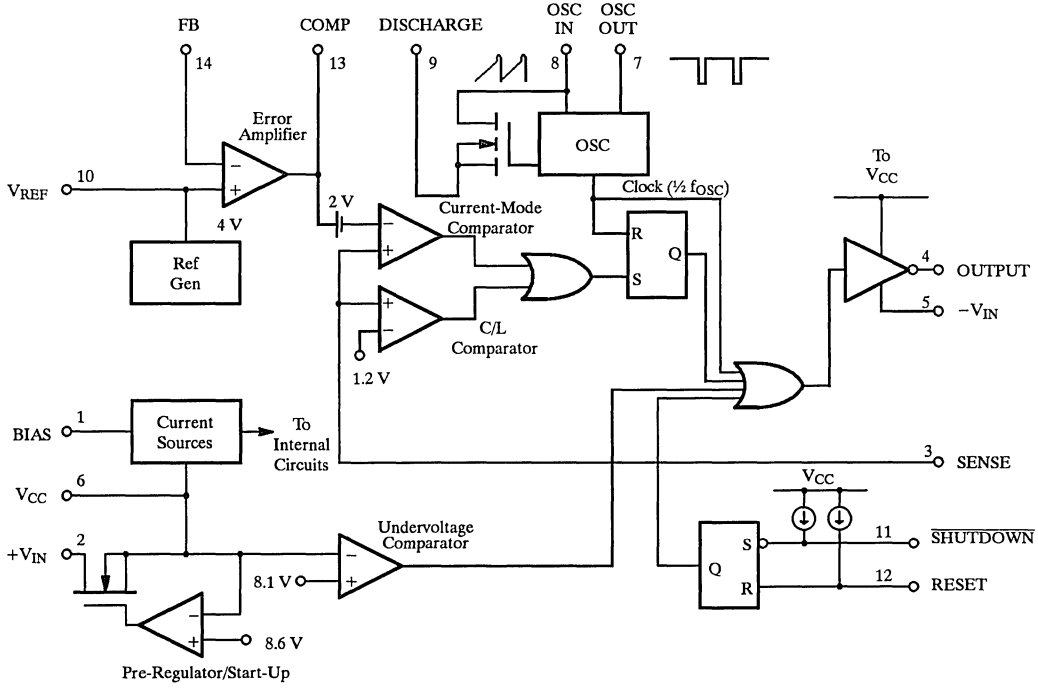
Description

The Si9110/9111 are BiC/DMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9110/9111 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9110/9111 is available in 14-pin plastic DIP, SOIC and CerDIP packages, and are specified over the military, A suffix (−55 to 125°C) and industrial, D suffix (−40 to 85°C) temperature ranges.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 120 V
Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN, OSC OUT) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SENSE, BIAS, V_{REF}) ..... -0.3 V to $V_{CC} + 0.3$ V
HV Pre-Regulator Input Current (continuous) ..... 5 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)a
14-Pin CerDIP (K Suffix)[b] ..... 1000 mW
14-Pin Plastic DIP (J Suffix)[c] ..... 750 mW
14-Pin SOIC (Y Suffix)[d] ..... 900 mW
Thermal Impedance (Θ_{JA})
14-Pin CerDIP ..... 100°C/W
14-Pin Plastic DIP ..... 167°C/W
14-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 10 mW/°C above 50°C.
c. Derate 6 mW/°C above 25°C.
d. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 120 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to $V_{CC} - 3$ V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Reference										
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Si9110	Room	4.0	3.92	4.08	3.92	4.08	V
			Si9111	Room	4.0	3.60	4.40	3.60	4.40	
			Si9110	Full		3.82	4.16	3.86	4.14	
			Si9111	Full		3.50	4.48	3.52	4.46	
Output Impedance[e]	Z_{OUT}			Room	30	15	45	15	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		Room	100	70	130	70	130	µA
Temperature Stability[e]	T_{REF}			Full	0.50		1.0		1.0	mV/°C
Oscillator										
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0		Room	3	1		1		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note f		Room	100	80	120	80	120	kHz
		R_{OSC} = 150 k, See Note f		Room	200	160	240	160	240	
Voltage Stability	Δf/f	Δf/f=f(13.5 V) − f(9.5 V)/ f(9.5 V)		Room	10		15		15	%
Temperature Coefficient[e]	T_{OSC}			Full	200		500		500	ppm/°C
Error Amplifier										
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Si9110	Room	4.00	3.96	4.04	3.96	4.04	V
			Si9111	Room	4.00	3.60	4.40	3.60	4.40	
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V		Room	25		500		500	nA

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Error Amplifier (Cont'd)									
Input OFFSET Voltage	V_{OS}	OSC IN = − V_{IN} (OSC Disabled)	Room	±15		±40		±40	mV
Open Loop Voltage Gain[e]	A_{VOL}		Room	80	60		60		dB
Unity Gain Bandwidth[e]	BW		Room	1.3	1		1		MHz
Dynamic Output Impedance[e]	Z_{OUT}		Room	1000		2000		2000	Ω
Output Current	I_{OUT}	Source (V_{FB} = 3.4 V)	Room	−2.0		−1.4		−1.4	mA
		Sink (V_{FB} = 4 5 V)	Room	0.15	0.12		0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	70	50		50		dB
Current Limit									
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.2	1.0	1.4	1.0	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room	100		150		150	ns
Pre-Regulator/Start-Up									
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room		120		120		V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	Room			10		10	µA
Pre-Regulator Start-Up Current	I_{START}	Pulse Width ≤ 300 µs, V_{CC} = V_{ULVO}	Room	15	8		8		mA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	8 6	7.8	9.4	7.8	9.4	V
Undervoltage Lockout	V_{UVLO}		Room	8.1	7.0	8.9	7.0	8.9	
V_{REG} − V_{UVLO}	V_{DELTA}		Room	0.6	0.3		0 3		
Supply									
Supply Current	I_{CC}	C_{LOAD} < 75 pF (Pin 4)	Room	0.6	0.45	1.0	0.45	1.0	mA
Bias Current	I_{BIAS}		Room	15	10	20	10	20	µA
Logic									
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF, V_{SENSE} − V_{IN} See Figure 2	Room	50		100		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room		50		50		
RESET Pulse Width[e]	t_{RW}		Room		50		50		
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}	See Figure 3	Room		25		25		
Input Low Voltage	V_{IL}		Room			2.0		2.0	V
Input High Voltage	V_{IH}		Room		8		8		

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Logic (Cont'd)									
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room	1		5		5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−25	−35		−35		µA
Output									
Output High Voltage	V_{OH}	I_{OUT} = −10 mA	Room Full		9.7 9.5		9.7 9.5		V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.30 0.50		0.30 0.50	V
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full	20 25		30 50		30 35	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room	40		75		75	ns
Fall Time[e]	t_f		Room	40		75		75	ns

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF.

Timing Waveforms

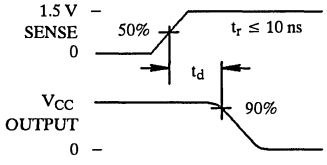


Figure 1.

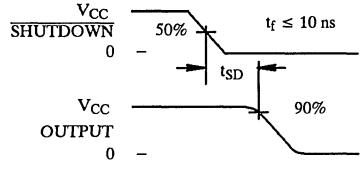


Figure 2.

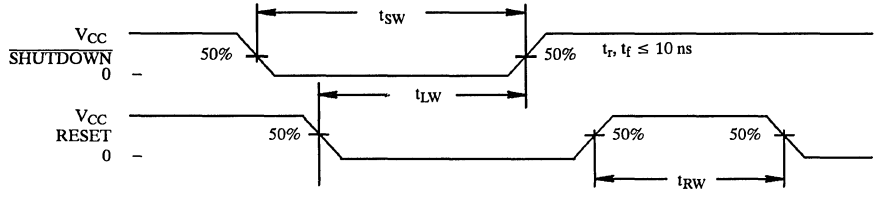
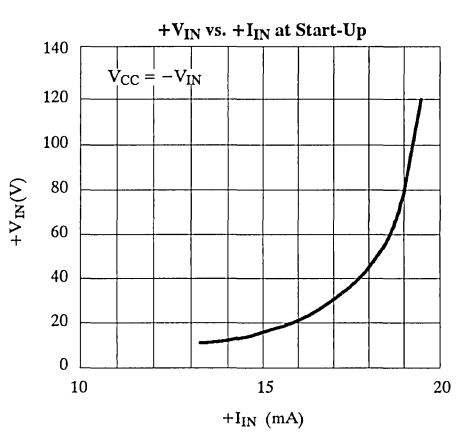
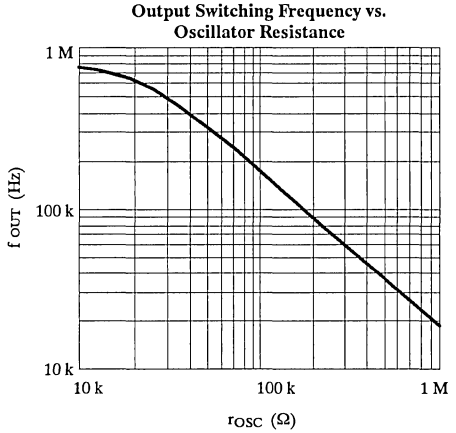


Figure 3.

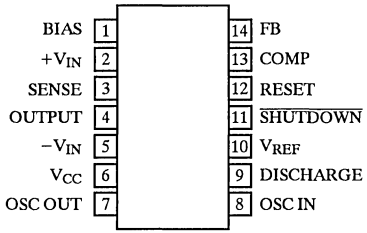
Typical Characteristics





Pin Configurations

Dual-In-Line and SOIC



Top View

Order Numbers

CerDIP: Si9110AK
Plastic DIP: Si9110DJ, Si9111DJ
SOIC: Si9110DY, Si9111DY

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9110/9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6-V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Detailed Description (Cont'd)

Note: During start-up or when V_{CC} drops below 8.6 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the V_{CC} supply can result in device damage. Figure 4 gives the typical pre-regulator current at BiC/DMOS as a function of input voltage.

BIAS

To properly set the bias for the Si9110/9111, a 390-kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to ≤ 50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	⌝⌞	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌟⌜	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Detailed Description (Cont'd)

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500-pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469A. The D469A can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

Applications

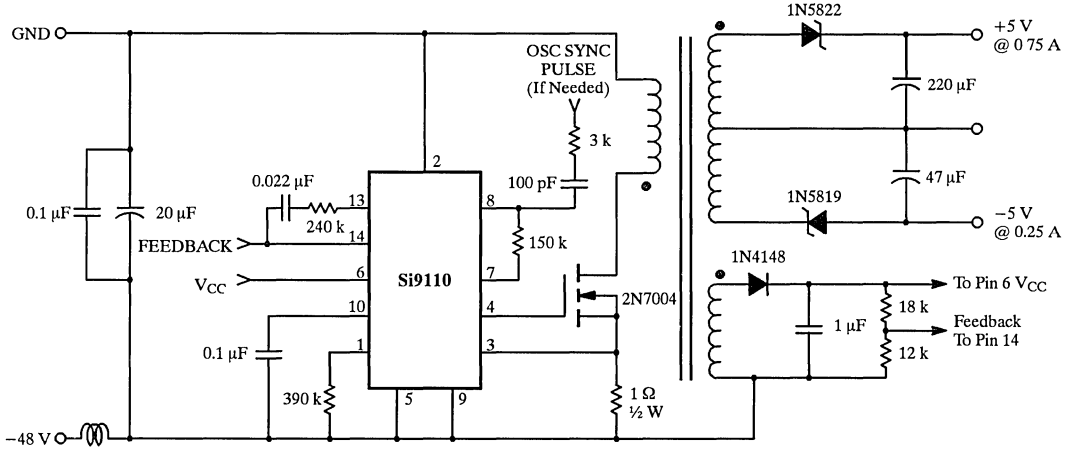


Figure 4. 5-Watt Power Supply for Telecom Applications

Si9112

High-Voltage Switchmode Controller

Features

- 9- to 80-V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

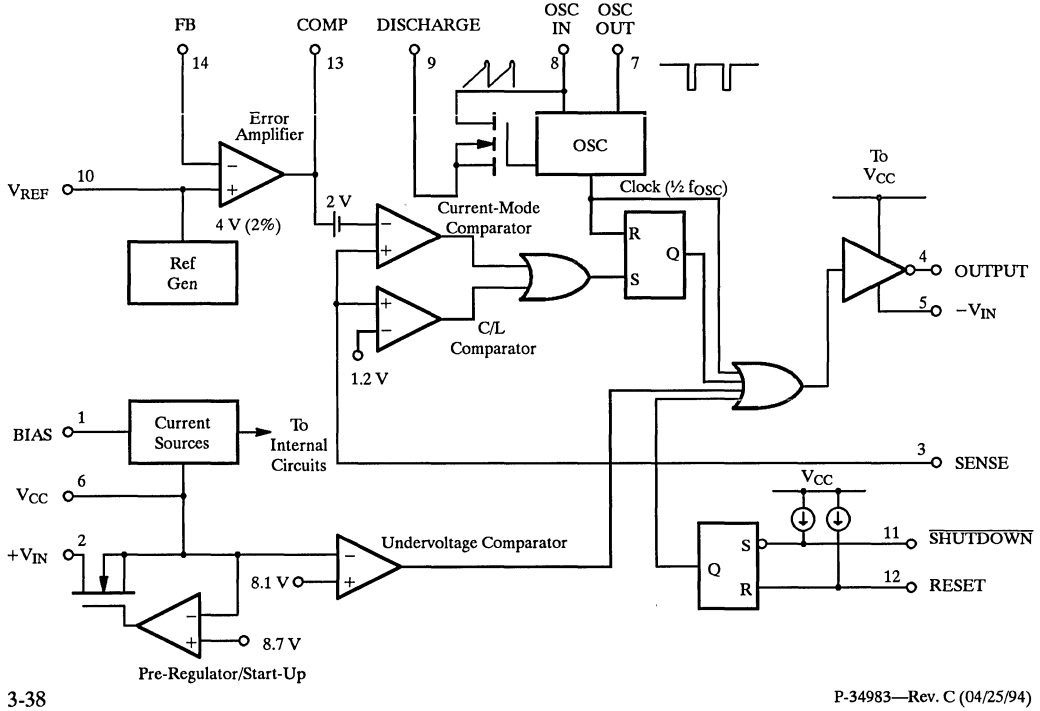
Description

The Si9112 is a BiC/DMOS integrated circuit designed for use in high-efficiency switchmode power converters. A high-voltage DMOS input allows this controller to work over a wide range of input voltages (9- to 80-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

A CMOS output driver provides high-speed switching of MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9112 can be used to implement single-ended power converter topologies (i.e., flyback, forward, and cuk).

The Si9112 is available in 14-pin plastic DIP, and SOIC packages, and is specified over the industrial, D suffix (−40 to 85°C) temperature range.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ ($V_{CC} < +V_{IN} + 0.3$ V)

V_{CC} ..... 15 V

$+V_{IN}$ ..... 80 V

Logic Inputs
(RESET, SHUTDOWN, OSC IN) ..... −0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SENSE) ..... −0.3 V to V_{CC} to 0.3 V

HV Pre-Regulator Input Current (continuous) ..... 25 mA
(Power Dissipation Limited)

Storage Temperature ..... −65 to 150°C

Operating Temperature ..... −40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)a
14-Pin Plastic DIP (J Suffix)[b] ..... 750 mW
14-Pin SOIC (Y Suffix)[c] ..... 900 mW

Thermal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 167°C/W
14-Pin SOIC ..... 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9 V to 13.5 V

$+V_{IN}$ ..... 9 V to 80 V

f_{OSC} ..... 40 kHz to 1 MHz

R_{OSC} ..... 25 kΩ to 1 MΩ

Linear Inputs ..... 0 to V_{CC} − 3 V

Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[d]	Typ[c]	Max[e]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full[e]	3.88 3.82	4.0	4.12 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	μA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	R_{OSC} = 330 k, See Note f	Room	80	100	120	kHz
		R_{OSC} = 150 k, See Note f	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = f(13.5 V) − f(9.5 V) / f(9.5 V)	Room		9	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.92	4.00	4.08	V
Input Offset Voltage	V_{OS}	OSC IN = $-V_{IN}$ (OSC Disabled)	Room		±15	±40	mV
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = $-V_{IN}$	Room	60	80		dB
Unity Gain Bandwidth[e]	BW	OSC IN = $-V_{IN}$ (OSC Disabled)	Room	1	1.5		MHz
Dynamic Output Impedance[e]	Z_{OUT}	Error Amp Configured for 60 dB gain	Room		1000	2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	Room		−2.0	−1.4	mA
		Sink V_{FB} = 4.5 V	Room	0.12	0.15		
Power Supply Rejection[e]	PSRR	9 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 9 V, $+V_{IN}$ = 12 V R_{BIAS} = 270 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[f]	Typ[c]	Max[g]	Unit
Current Limit							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room		100	150	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room	80			V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq$ 9.4 V	Room			10	µA
Pre-Regulator Dropout Voltage	V_{CC}	$+V_{IN}$ = 10 V, R_{LOAD} = 4 k at Pin 6	Room	V_{UVLO} +0.1			V
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	8.0	8.7	9.4	V
Undervoltage Lockout	V_{UVLO}	See Detailed Description	Room	7.2	8.1	8.9	V
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		V
Supply							
Supply Current	I_{CC}	$C_L \leq$ 75 pF (Pin 4)	Room		0.6	1.0	mA
Bias Current	I_{BIAS}		Room		15		µA
Logic							
$\overline{\text{SHUTDOWN}}$ Delay[e]	t_{SD}	C_L = 500 pF $V_{SENSE} = -V_{IN}$, See Figure 2	Room		50	100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			ns
RESET Pulse Width[e]	t_{RW}		Room	50			ns
Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET Low[e]	t_{LW}		Room	25			ns
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	7.0			V
Input Current Input Voltage High	I_{IH}	$V_{LOGIC} = V_{CC}$	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	25		µA
Output							
Output High Voltage	V_{OH}	I_{OUT} = −10 mA	Room Full	8.7 8.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	V
Output Resistance[e]	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full		20 25	30 35	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room		40	75	ns
Fall Time[e]	t_f		Room		40	75	ns

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF.

Timing Waveforms

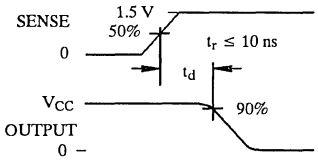


Figure 1.

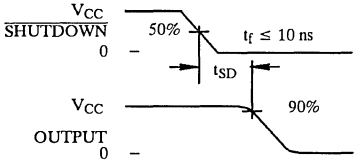


Figure 2.

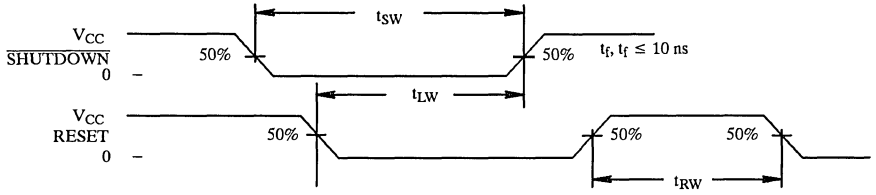
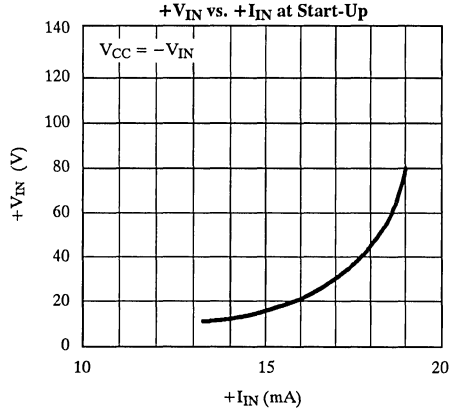
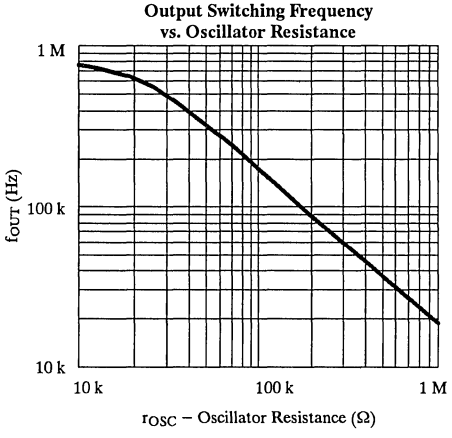


Figure 3.

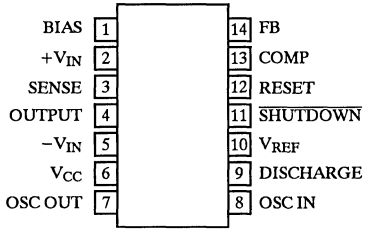
Typical Characteristics





Pin Configurations

Dual-In-Line and SOIC



Top View

Order Numbers
Plastic DIP: Si9112DJ
SOIC: Si9112DY

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9112 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The charging current is disabled when V_{CC} exceeds 8.7 V. If V_{CC} is not forced to exceed the 8.7-V threshold, then V_{CC} will be regulated to a nominal value of 8.7 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the UV lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the pre-regulator circuit is disabled.

BIAS

To properly set the bias for the Si9112, a 270-k Ω resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9112 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9112 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±2% of 4 V. This automatically compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Error Amplifier

Closed-loop regulation is provided by the error amplifier. The emitter follower output has a typical dynamic output impedance of 1000 Ω, and is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides low input leakage current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

P-34983—Rev. C (04/25/94)

Detailed Description (Cont'd)

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq 50\%$ by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5-µs pulse width, typical values would be 100 pF in series with 3 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	⌝⌞	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
⌟⌜	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive 60-V, 25-A MOSFETs. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

For applications information refer to AN703.

Si9114

Siliconix

High-Frequency Switchmode Controller

Features

- 15- to 200-V Input Range
- Current-Mode Control
- Internal Start-Up Circuit
- Latched $\overline{\text{SHUTDOWN}}$
- Soft-Start
- 1.5-MHz Error Amp

Description

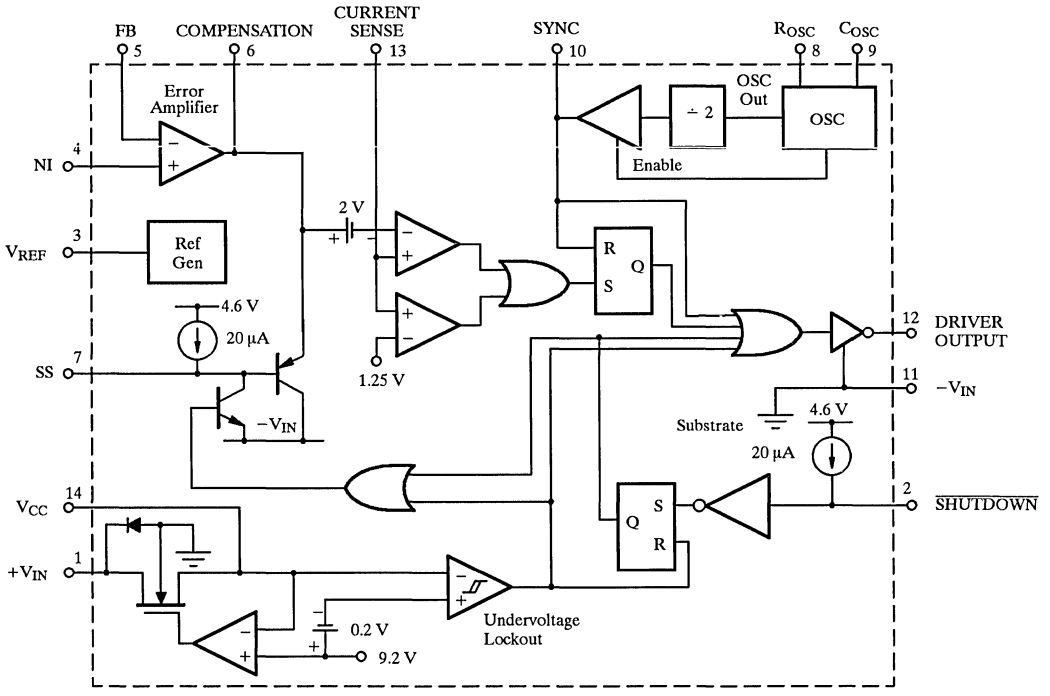
The Si9114 is a BiC/DMOS current-mode pulse width modulation (PWM) controller IC for high-frequency dc/dc converters. Single-ended topologies (forward and flyback) can be implemented at frequencies up to 1 MHz. The oscillator has an internal divide-by-two that limits the duty ratio to 50%. An oscillator sync output allows converters to be synchronized in phase as well as in frequency, in a master/slave configuration.

The output inverter can typically source 500 mA and sink 700 mA. Shoot-through current is all but eliminated to minimize supply current requirements.

The high-voltage DMOS transistor allows the IC to interface directly to bus voltages up to 200 V. Other features include a 1.5% accurate voltage reference, 1.5-MHz (min) bandwidth error amplifier, shutdown logic control, soft-start and undervoltage lockout circuits.

The Si9114 is available in 14-pin plastic DIP and SOIC packages, and is specified over the industrial, D suffix (−40°C to 85°C) temperature range.

Functional Block Diagram



Preliminary

Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 18 V

$+V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V) ..... 200 V

Logic Input ($\overline{SHUTDOWN}$, SYNC) ..... −0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SENSE, SOFT-START) ..... −0.3 V to V_{CC} + 0.3 V

HV Pre-Regulator Input Current (continuous) ..... 5 mA

Storage Temperature ..... −65 to 150°C

Operating Temperature ..... −40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[a]

14-Pin Plastic Dip (J Suffix)[b] ..... 750 mW

14-Pin SOIC (Y Suffix)[c] ..... 900 mW

Thermal Impedance (Θ_{JA})

14-Pin Plastic Dip ..... 167°C/W

14-Pin SOIC ..... 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.
b. Derate 6 mW/°C above 25°C.
c. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$

V_{CC} ..... 9.5 V to 16.5 V

$+V_{IN}$ ..... 15 V to 200 V

f_{OSC} ..... 20 kHz to 2 MHz

R_{OSC} ..... 56 kΩ to 1 MΩ

C_{OSC} ..... 47 pF to 200 pF

Linear Inputs ..... 0 to V_{CC} − 4 V

Digital Inputs ..... 0 to V_{CC}

Specifications

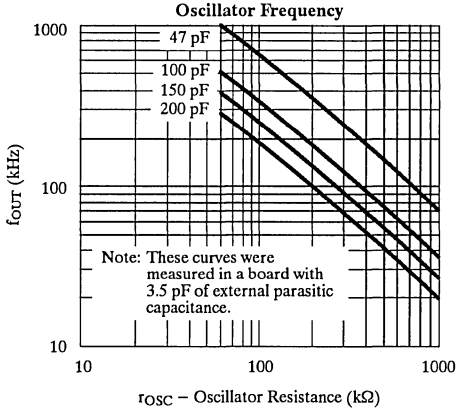
Parameter	Symbol	Test Conditions Unless Otherwise Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V	Limits D Suffix −40 to 85°C Min[b]	Typ[a]	Max[b]	Unit
Reference						
Output Voltage	V_R	OSC Disabled, T_A = 25°C	3.94	4.0	4.06	V
		OSC Disabled Over Voltage and Temperature Ranges[c]	3.88	4.0	4.12	
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		−15	−5	mA
Load Regulation	$\Delta V_R/\Delta I_R$	I_{REF} = 0 to −3 mA		3	40	mV
Oscillator						
Initial Accuracy	f_{OSC}[d]	R_{OSC} = 374 kΩ, C_{OSC} = 200 pF	90	100	110	kHz
		R_{OSC} = 133 kΩ, C_{OSC} = 100 pF	450	500	550	
Voltage Stability[c]	Δf/f	R_{OSC} = 133 kΩ, C_{OSC} = 100 pF Δf/f = [f(16.5 V) − f(9.5 V)] / f(9.5 V)		1	2	%
Temperature Coefficient[c]	OSC TC	$-40 \le T_A \le 85$°C, f_{OSC} = 100 kHz		200	500	ppm/°C
Sync Output Current (Master Mode)	$I_{SYNC(M)}$	$V_{ROSC} \le 5$ V	±1.0	±3.0		mA
Sync Output Current (Slave Mode)	$I_{SYNC(S)}$	$V_{ROSC} = V_{CC}$		±1	±500	nA

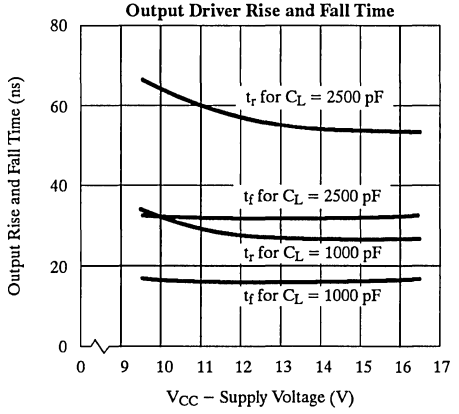
Specifications[a]

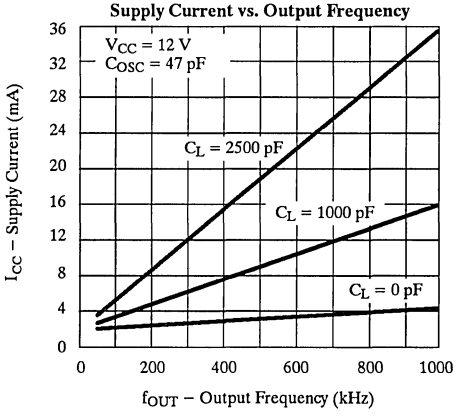
Parameter	Symbol	Test Conditions Unless Otherwise Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V		Limits D Suffix −40 to 85°C Min[b]	Typ[a]	Max[b]	Unit
Error Amplifier (C_{OSC} = $-V_{IN}$ OSC Disabled)							
Input BIAS Current	I_{FB}	V_{FB} = 5 V, NI = V_{REF}			±25	±200	nA
Input OFFSET Voltage	V_{OS2}				±5	±25	mV
Open Loop Voltage Gain[c]	A_{VOL}			65	88		dB
Unity Gain Bandwidth[c]	BW			1.5	2.3		MHz
Output Current	I_{OUT}	Source (V_{FB} = 3.5 V, NI = V_{REF})			−2.0	−1.0	mA
		Sink (V_{FB} = 4.5 V, NI = V_{REF})		1.0	4.0		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 16.5 V		50	88		dB
Pre-Regulator/Start-Up							
Input Leakage Current	$+I_{IN}$	$+V_{IN}$ = 200 V, V_{CC} ≥ 10 V			<1	10	µA
Pre-Regulator Start-Up Current	I_{START}	$+V_{IN}$ = 48 V, t_{PW} ≤ 300 µs, V_{CC} = V_{UVLO}		8	20		mA
V_{CC} Pre-Regulator Voltage	V_{PR}	$+V_{IN}$ = 48 V		8.8	9.1	9.4	V
V_{PR} − V_{UVLO} (Turn-On)	V_{DELTA}			0.1	0.2	0.7	
Undervoltage Lockout Hysteresis	V_{HYST}			0.18	0.3	0.4	
Supply							
Supply Current	I_{CC}	C_{LOAD} ≤ 50 pF	f_{OSC} = 100 kHz		1.3	2.5	mA
			f_{OSC} = 500 kHz		1.8	3.0	
Protection							
Current Limit Threshold Voltage	V_{SENSE}	V_{FB} = 0 V, NI = V_{REF}		1.15	1.23	1.30	V
Current Limit Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1			70	100	ns
$\overline{\text{SHUTDOWN}}$ Logic Threshold	V_{SD}				2.5	0.5	V
$\overline{\text{SHUTDOWN}}$ Delay to Latched Output[c]	t_{SD}	See Figure 2			0.30	1.0	µs
$\overline{\text{SHUTDOWN}}$ Pull-Up Current	I_{SD}	V_{SD} = 0 V		12	17	30	µA
Soft-Start Current	I_{SS}			12	17	30	
Output Inhibit Voltage	$V_{SS(off)}$	Soft-Start Voltage to Disable Driver Output			1.7	0.5	V
MOSFET Driver							
Output High Voltage	V_{OH}	I_{OUT} = −10 mA		9.85	9.9		V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA			0.05	0.15	
Peak Output Current[c]	I_{SOURCE}	V_{OUT} = 0 V			−400	−200	mA
	I_{SINK}	V_{OUT} = V_{CC}		500	700		

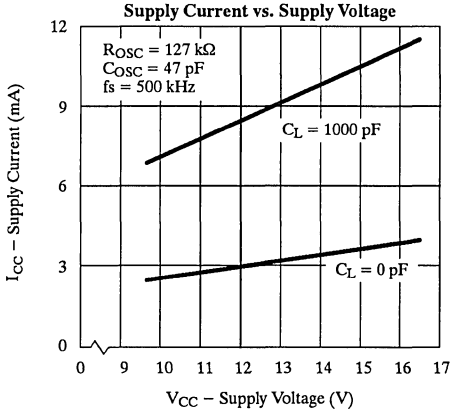
Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Guaranteed by design, not subject to production test.
d. C_{STRAY} ≤ 5 pF on C_{OSC}.

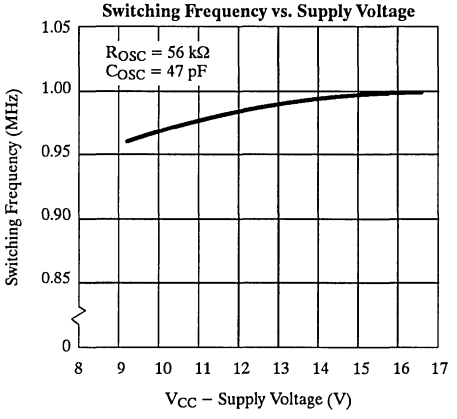
Typical Characteristics (25°C Unless Otherwise Noted)











Timing Waveforms

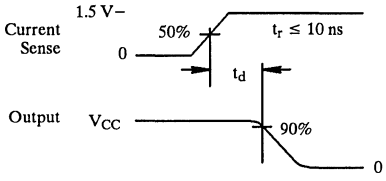


Figure 1.

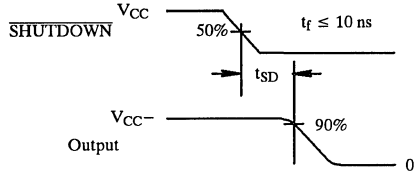
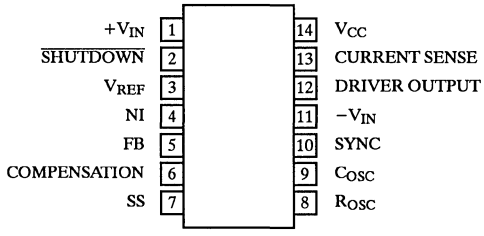


Figure 2.

Pin Configurations

Dual-In-Line and SOIC



Top View

Order Numbers
Plastic DIP: Si9114DJ
SOIC: Si9114DY

Applications

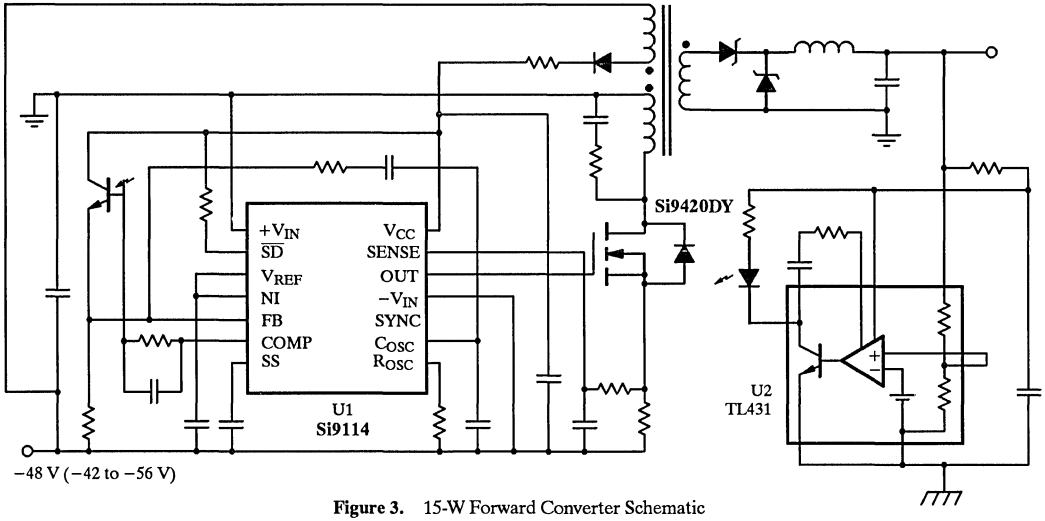


Figure 3. 15-W Forward Converter Schematic

Universal Input Switchmode Controller

Features

- 10- to 450-V Input Range
- Current-Mode Control
- 125-mA Output Drive
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)
- $\overline{\text{SHUTDOWN}}$ and RESET

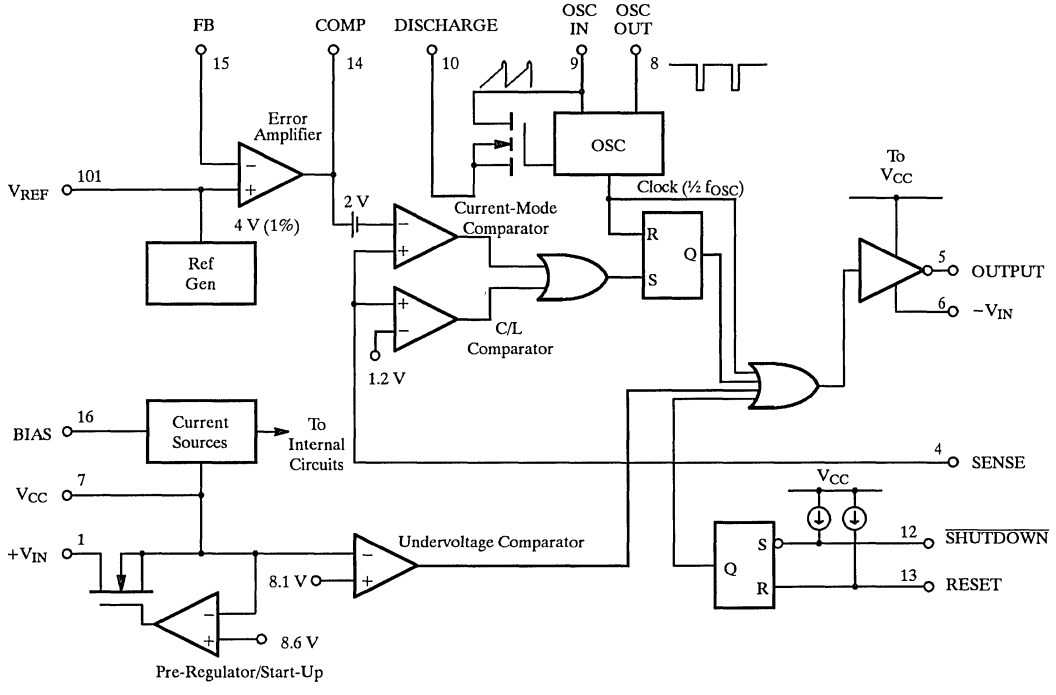
Description

The Si9120 is a BiC/DMOS integrated circuit designed for use in low-power, high-efficiency off-line power supplies. High-voltage DMOS inputs allow the controller to work over a wide range of input voltages (10- to 450-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce quiescent current to less than 1.5 mA.

A CMOS output driver provides high-speed switching for MOSFET devices with gate charge, Q_g, up to 25 nC, enough to supply 30 W of output power at 100 kHz. These devices, when combined with an output MOSFET and transformer, can be used to implement single-ended power converter topologies (i.e., flyback and forward).

The Si9120 is available in a 16-pin plastic DIP and SOIC packages, and is specified over the industrial, D suffix (−40 to 85°C) temperature range.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to $-V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V)
V_{CC} ..... 15 V
$+V_{IN}$ ..... 450 V
Logic Inputs (RESET
$\overline{\text{SHUTDOWN}}$, OSC IN, OSC OUT) ..... -0.3 V to $V_{CC} + 0.3$ V
Linear Input
(FEEDBACK, SENSE, BIAS, V_{REF}) ..... -0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) ..... 5 mA[a]
Continuous Output Current (Source or Sink) ..... 125 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature ..... -40 to 85°C
Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[b]
16-Pin Plastic DIP (J Suffix)[c] ..... 750 mW
16-Pin SOIC (Y Suffix)[d] ..... 900 mW
Thermal Impedance (Θ_{JA})
16-Pin Plastic DIP ..... 167°C/W
16-Pin SOIC ..... 140°C/W

Notes
a. Continuous current may be limited by the applications maximum input voltage and the package power dissipation.
b. Device mounted with all leads soldered or welded to PC board.
c. Derate 6 mW/°C above 25°C.
d. Derate 7.2 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to $-V_{IN}$
V_{CC} ..... 9.5 V to 13.5 V
$+V_{IN}$ ..... 10 V to 450 V
f_{OSC} ..... 40 kHz to 1 MHz
R_{OSC} ..... 25 kΩ to 1 MΩ
Linear Inputs ..... 0 to $V_{CC} - 3$ V
Digital Inputs ..... 0 to V_{CC}

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V $+V_{IN}$ = 300 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Reference							
Output Voltage	V_R	OSC IN = $-V_{IN}$ (OSC Disabled) R_L = 10 MΩ	Room Full	3.88 3.82	4.0	4.12 4.14	V
Output Impedance[e]	Z_{OUT}		Room	15	30	45	kΩ
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$	Room	70	100	130	µA
Temperature Stability[e]	T_{REF}		Full		0.5	1.0	mV/°C
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	1	3		MHz
Initial Accuracy	f_{OSC}	C_{STRAY} Pin 9 ≤ 5 pF, R_{OSC} = 330 kΩ	Room	80	100	120	kHz
		C_{STRAY} Pin 9 ≤ 5 pF, R_{OSC} = 150 kΩ	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f = f(13.5\text{ V}) - f(9.5\text{ V}) / f(9.5\text{ V})$	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		200	500	ppm/°C
Error Amplifier							
Feedback Input Voltage	V_{FB}	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.92		4.08	V
Input BIAS Current	I_{FB}	OSC IN = $-V_{IN}$, V_{FB} = 4 V	Room		25	500	nA
Input OFFSET Voltage	V_{OS}	OSC IN = $-V_{IN}$	Room		±15	±40	mV
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = $-V_{IN}$	Room	60	80		dB
Unity Gain Bandwidth[e]	BW	OSC IN = $-V_{IN}$	Room	1.0	1.5		MHz
Dynamic Output Impedance[e]	Z_{OUT}	Error Amp configured for 60 dB gain	Room		1000	2000	Ω
Output Current	I_{OUT}	Source V_{FB} = 3.4 V	Room		−2.0	−1.4	mA
		Sink V_{FB} = 4.5 V	Room	0.12	0.15		
Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	Room	50	70		dB

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V + V_{IN} = 300 V R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	Temp[b]	Limits D Suffix −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Current Limit							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Room	1.0	1.2	1.4	V
Delay to Output[e]	t_d	V_{SENSE} = 1.5 V, See Figure 1	Room		100	150	ns
Pre-Regulator/Start-Up							
Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	Room	450			V
Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	Room			10	µA
V_{CC} Pre-Regulator Turn-Off Threshold Voltage	V_{REG}	$I_{PRE-REGULATOR}$ = 10 µA	Room	7.8	8.6	9.4	V
Undervoltage Lockout	V_{UVLO}		Room	7.0	8.1	8.9	
$V_{REG} - V_{UVLO}$	V_{DELTA}		Room	0.3	0.6		
Supply							
Supply Current	I_{CC}	C_L = 500 pF at Pin 5	Room		0.85	1.5	mA
Bias Current	I_{BIAS}		Room	10	15	20	µA
Logic							
$\overline{SHUTDOWN}$ Delay[e]	t_{SD}	C_L = 500 pF, $V_{SENSE} = -V_{IN}$ See Figure 2	Room		50	100	ns
$\overline{SHUTDOWN}$ Pulse Width[e]	t_{SW}	See Figure 3	Room	50			
RESET Pulse Width[e]	t_{RW}		Room	50			
Latching Pulse Width $\overline{SHUTDOWN}$ and RESET Low[e]	t_{LW}		Room	25			
Input Low Voltage	V_{IL}		Room			2.0	V
Input High Voltage	V_{IH}		Room	8.0			
Input Current Input Voltage High	I_{IH}	V_{IN} = 10 V	Room		1	5	µA
Input Current Input Voltage Low	I_{IL}	V_{IN} = 0 V	Room	−35	−25		
Output							
Output High Voltage	V_{OH}	I_{OUT} = −10 mA	Room Full	9.7 9.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	
Output Resistance	R_{OUT}	I_{OUT} = 10 mA, Source or Sink	Room Full		20 25	30 35	Ω
Rise Time[e]	t_r	C_L = 500 pF	Room		40	75	ns
Fall Time[e]	t_f		Room		40	75	

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
e. Guaranteed by design, not subject to production test.

Timing Waveforms

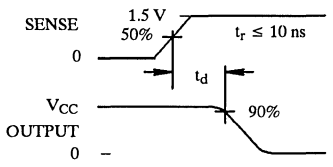


Figure 1.

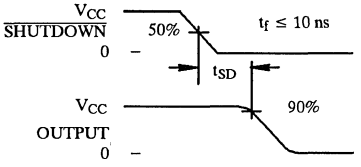


Figure 2.

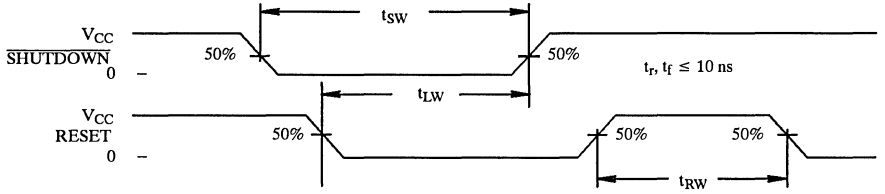
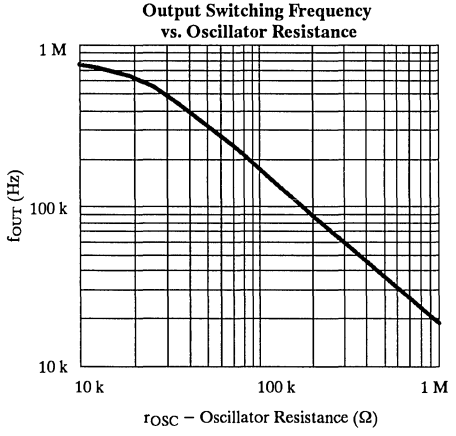


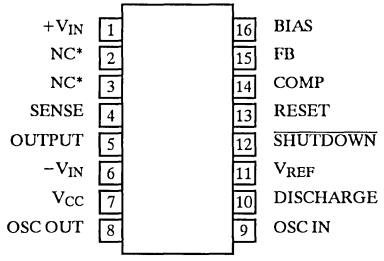
Figure 3.

Typical Characteristics



Pin Configurations

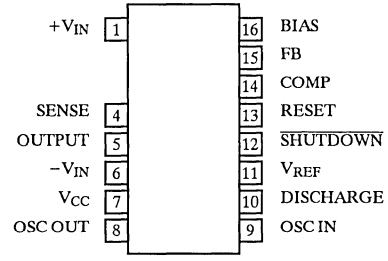
Dual-In-Line



Top View

Order Number: Si9120DJ

SOIC



Top View

Order Number: Si9120DY
Note: Pins 2 and 3 are removed

Detailed Description

Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9120 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, $+V_{IN}$ (pin 1) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET which is connected between $+V_{IN}$ and V_{CC} (pin 7). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6-V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

Note: When driving large MOSFETs at high frequency without a bootstrap V_{CC} supply, power dissipation in the pre-regulator may exceed the power rating of the IC package.

BIAS

To properly set the bias for the Si9120, a 390-kΩ resistor should be tied from BIAS (pin 16) to $-V_{IN}$ (pin 6). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

Reference Section

The reference section of the Si9120 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9120 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±2% of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Detailed Description (Cont'd)

Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for high input impedance. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Typical Characteristics for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$ 50% by locking the switching frequency to one half of the oscillator frequency.

$\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$ (pin 12) and RESET (pin 13) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched or unlatched input. The output is off whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. See Table 1.

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

Table 1: Truth Table for the $\overline{\text{SHUTDOWN}}$ and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
↑	L	Off (Latched—No Change)

Output Driver

The push-pull driver output has a typical on-resistance of 20 Ω maximum switching times are specified at 75 ns for a 500-pF load. This is sufficient to directly drive MOSFETs such as the IRF820, BUZ78 or BUZ80. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses.

For applications information refer to AN707 and AN708.

Siliconix

Si9145

Low-Voltage Switchmode Controller

Features

- 2.7-V to 7-V Input Operating Range
- PWM Control
- High-Speed, Source-Sink Output Drive (200 mA)
- Internal Oscillator (up to 2 MHz)
- Standby Mode
- 50–100% Duty-Cycle Controllable Maximum

Benefits

- Cellular Telephones
- Portable Computers
- Handheld Instruments
- Distributed Power Systems
- Palmtop/PDA Terminals

Applications

- DC/DC Converters

Description

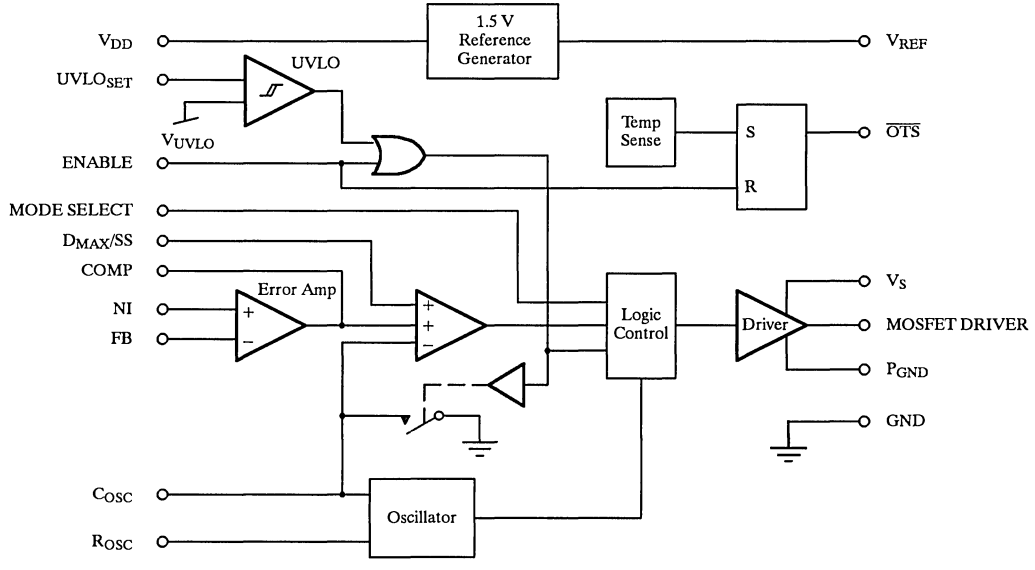
The Si9145 switchmode controller IC is ideally suited for high efficiency dc/dc converters in battery input powered systems. Operation is guaranteed down to 2.7 V, with a minimum start-up voltage of 3.0 V making the Si9145 ideal for use with NiCd, NMH, and lithium ion battery packs. A mode select pin allows the output driver polarity to be programmed allowing the device to function as a step-up or step-down converter.

Features include a precision bandgap reference, a wide bandwidth error amplifier, a 2-MHz oscillator, an input voltage monitor with standby mode and a 200-mA output driver. Supply current in normal operation is typically 1 mA and 250 µA in standby mode.

The Si9145 implements conventional voltage mode control. The maximum duty cycle can be limited by voltage on D_{MAX}/SS pin and frequency can be externally programmed by selection of R_{OSC} and C_{OSC}.

The Si9145 is available in 16-pin SOIC and TSSOP packages and is specified over the industrial temperature range (−25°C to +85°C).

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to GND.

V_{DD}, V_S ..... 8 V
P_{GND} ..... ±0.3 V
V_{DD} to V_S ..... −0.3 V
Linear Inputs ..... −0.3 V to V_{DD} to +0.3 V
Logic Inputs ..... −0.3 V to V_{DD} to +0.3 V
Continuous Output Current ..... 100 mA
Storage Temperature ..... −65 to 125°C
Operating Junction Temperature ..... 150°C

Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] ..... 900 mW
16-Pin TSSOP (Q Suffix)[c] ..... 925 mW
Thermal Impedance (Θ_{JA})
16-Pin SOIC ..... 140°C/W
16-Pin TSSOP ..... 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.
c. Derate 7.4 mW/°C above 25°C.

Recommended Operating Range

Voltages Referenced to GND.

V_{DD} ..... 2.7 V to 7 V
V_S ..... 2.7 V to 7 V
f_{OSC} ..... 2 kHz to 2 MHz
R_{OSC} ..... 5 kΩ to 250 kΩ
C_{OSC} ..... 47 pF to 200 pF
Linear Inputs ..... 0 to V_{DD}
Digital Inputs ..... 0 to V_{DD}
V_{REF} Load Resistance ..... >150 kΩ

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.7 V ≤ V_{DD} ≤ 7 V, V_{DD} = V_S GND = P_{GND}, −25°C ≤ T_A ≤ 85°C		Limits B Suffix − 25 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Reference							
Output Voltage	V_{REF}	I_{REF} = −10 µA		1.455		1.545	V
			T_A = 25°C	1.485	1.50	1 515	
Oscillator							
Maximum Frequency[d]	f_{MAX}	V_{CC} = 3.0 V, C_{OSC} = 47 pF, R_{OSC} = 5.0 kΩ		2.0			MHz
Initial Accuracy	f_{OSC}	V_{CC} = 3.0 V C_{OSC} = TBD pF, R_{OSC} = TBD kΩ	T_A = 25°C	0.9	1.0	1.1	
R_{OSC} Voltage	V_{ROSC}				1.0		V
Oscillator Start Voltage				3.0			
50% D_{MAX}/SS	V_{DMAX} 50%	MODE SELECT = V_{DD}			1.25		
100% D_{MAX}/SS	V_{DMAX} 100%				1.54		
D_{MAX}/SS Input Current	I_{DMAX}	D_{MAX} = 0 to V_{DD}		−100		100	nA
Voltage Stability	Δf/f/ΔV	2.7 V ≤ V_{DD} ≤ 7 V, Ref to 4.8 V	T_A = 25°C	−16		+16	%
		2.7 V ≤ V_{DD} ≤ 4.2 V, Ref to 3.5 V		−6		+6	
		3.8 V ≤ V_{DD} ≤ 5.6 V, Ref to 4.7 V		−7		+7	
Temperature Stability[d]	Δf/Δt	Referenced to 25°C		−5	±3	+5	

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified 2.7 V ≤ V_{DD} ≤ 7 V, V_{DD} = V_S GND = P_{GND}, −25°C ≤ T_A ≤ 85°C	Limits B Suffix − 25 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Error Amplifier (C_{OSC} = GND, OSC DISABLED)						
Input Bias Current	I_{FB}	V_{NI} = V_{REF}, V_{FB} = 1.0 V	−1.0			µA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	V_{NI} = V_{REF}	−15	0	+15	mV
Unity Gain Bandwidth[d]	BW			10		MHz
Output Current	I_{EA}	Source (V_{FB} = 1 V, NI = V_{REF})			−1.0	mA
		Sink (V_{FB} = 2 V, NI = V_{REF})	0 8			
Power Supply Rejection	P_{SRR}		50	60		dB
Input Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	V_{DD} High to Low	TBD	1.0	TBD	V
	V_{UVLOLH}	V_{DD} Low to High		1 2		
Hysterisis	V_{HYS}	V_{UVLOLH} − V_{UVLOHL}		200		mV
UVLO Input Current	I_{UVLO}	V_{UVLO} = 0 to V_{DD}	−100		100	nA
MOSFET Driver						
Output High Voltage	V_{OH}	V_{DD} = 2.7 V, I_{OUT} = −10 mA	2.55	2.60		V
Output Low Voltage	V_{OL}	V_{DD} = 2.7 V, I_{OUT} = 10 mA		0.06	0 15	
Peak Output Current	I_{SOURCE}	V_{DD} = 2.7 V, V_{OUT} = 0 V		−180	−130	mA
Peak Output Current	I_{SINK}	V_{DD} = 2.7 V, V_{OUT} = 2.7 V	150	200		
Logic						
ENABLE Delay to Output	td_{EN}			35		ns
ENABLE Logic Low	V_{ENL}				0.2 V_{DD}	V
ENABLE Logic High	V_{ENH}		0.8 V_{DD}			
ENABLE Input Current	I_{EN}	ENABLE = 0 to V_{DD}	−1 0		1.0	µA
MODE SELECT Logic Low	V_{MODEL}				0.2 V_{DD}	V
MODE SELECT Logic High	V_{MODEH}		0.8 V_{DD}			
MODE SELECT Input Current	I_{MODE}	MODE SELECT = 0 to V_{DD}	−1 0		1 0	µA
Over Temperature Sense						
Trip Point	T_{TRIP}			150		°C
Output Low	V_{OTSL}	V_{DD} = 2.7 V, I_{OUT} = 1 µA		0.06	0.15	V
Output High	V_{OTSH}	V_{DD} = 2.7 V, I_{OUT} = −1 µA	2 55	2.6		
Supply						
Supply Current − Normal	I_{DD}	V_{DD} = 2.7 V, f_{OSC} = 1 MHz, R_{OSC} = 7.5 kΩ		1.1	TBD	mA
		V_{DD} = 7 V, f_{OSC} = 1 MHz, R_{OSC} = 7.5 kΩ		1.4	TBD	
Supply Current − Shutdown		ENABLE = Low		250	TBD	µA

Notes
a. C_{STRAY} < 5 pF on C_{OSC}.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production testing.

Timing Waveforms

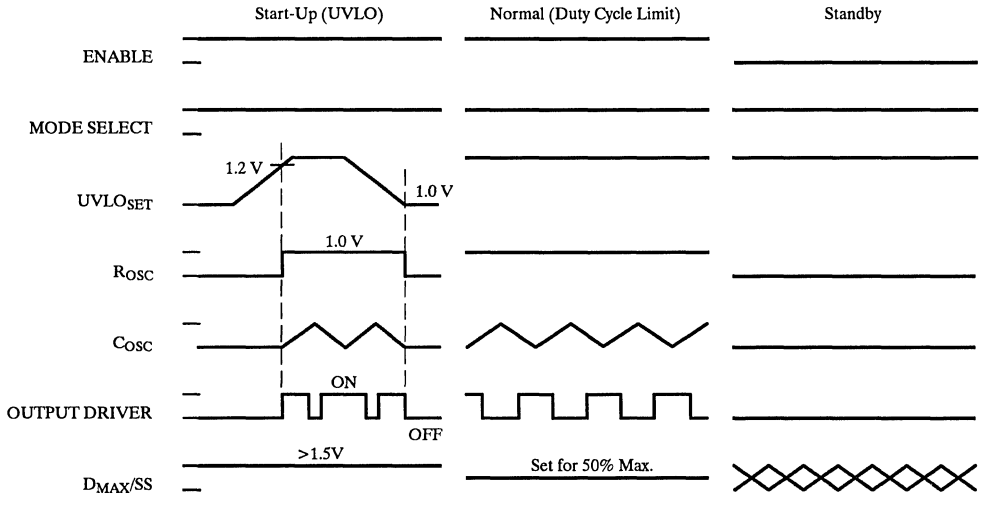


Figure 1. Si9145 Timing Diagram (MODE SELECT = High)

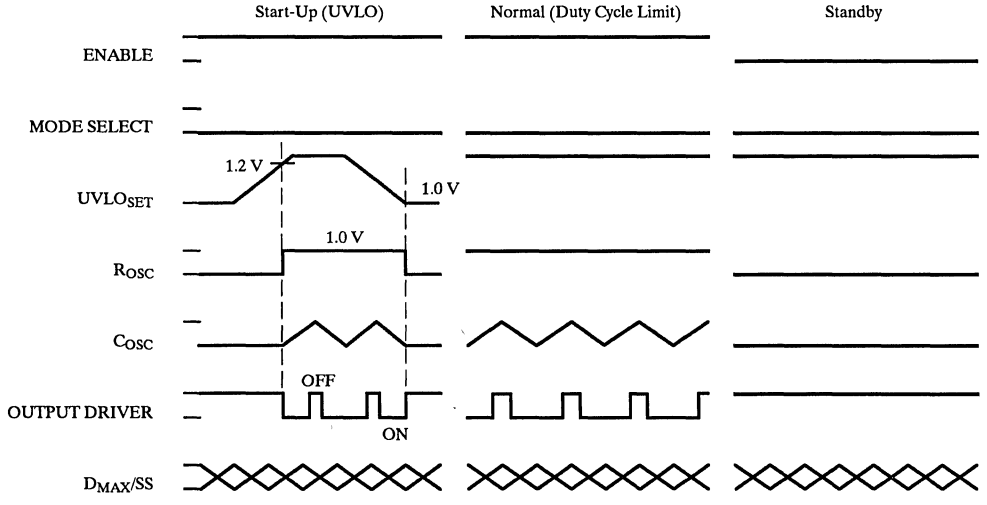
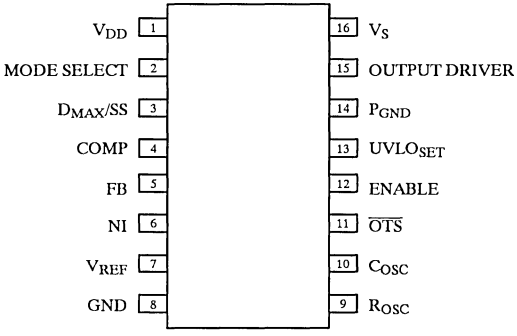


Figure 2. Si9145 Timing Diagram (MODE SELECT = Low)

Pin Configurations

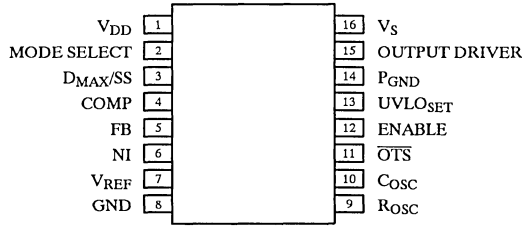
SO-16



Top View

Order Number: Si9145BY

SO-16 (TSSOP)



Top View

Order Number: Si9145BQ

Pin Description

Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor is required.

Pin 2: MODE SELECT

Pin used to enable max duty cycle limit and set output polarity of controller. When connected to V_{DD}, the max duty cycle function is enabled by using the D_{MAX}/SS pin. The max duty cycle limit is usually for forward, flyback, and boost converters. The output polarity is high when the PWM circuitry wants the external device "on".

When connected to GND, the max duty cycle is not limited usually for buck converters driving a p-channel MOS. The output polarity is low when the PWM circuitry wants the external PMOS "on".

Pin 3: D_{MAX}/SS

When max duty cycle function is enabled (MODE SELECT = V_{DD}), the voltage on this pin limits the max duty cycle. Below 1.0 V the duty cycle is 0 and above 1.5 V the duty cycle is not limited, and can be 100% depending on the PWM circuitry. The addition of external components can implement a soft start function.

Pin 4: COMP

Output of error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin 5: FB

The inverting input of the error amplifier. External resistors are connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to the V_{REF} pin.

Pin 7: V_{REF}

This pin supplies 1.5 V trimmed to ± 1%. The reference voltage is generated by a band-gap reference.

Pin 8: GND

Negative return for V_{DD}.

Pin 9: R_{OSC}

This pin is the equivalent of a 1.0-V source derived from the on-chip V_{REF}. When a low T.C. resistor is externally connected from this pin to GND, a temperature independent current is generated internally. This current is used as the charging current source connected to the C_{OSC} pin. The current is internally multiplied by 2 and is used as the discharging current source connected to the C_{OSC} pin. Therefore, the external resistor is one of the factors that determine the oscillator frequency.

Pin Description

Pin 10: C_{OSC}

An external capacitor is connected to this pin to set the oscillator frequency. Internal current sources alternately charge and discharge the external capacitor. The oscillator waveform is a symmetrical triangular type with a typical voltage swing between 1.0 V and 1.5 V.

Pin 11: $\overline{OTS}$

This pin indicates an over-temperature condition on the chip. An output low indicates an over-temperature fault. The output is latched low and must be set with the ENABLE pin going low then high, or by turning power off and on.

Pin 12: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode normal operation is disabled, supply current is reduced, the oscillator stops and the output is high for MODE SELECT = low, and low for MODE SELECT = high.

Pin 13: $UVLO_{SET}$

This pin will place the chip in the standby mode if the UVLO voltage is below 1.2 V. Once the UVLO voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV, the UVLO pin must drop below 1.0 V before the chip enters the standby mode.

Pin 14: P_{GND}

The negative return for the V_S supply.

Pin 15: OUTPUT DRIVER

CMOS push-pull output. This pin drives the external MOSFET and is capable of sinking 200 mA or sourcing 180 mA with V_S equal to 2.7 V.

Pin 16: V_S

The positive terminal of an external battery or power supply. The voltage on this pin powers the CMOS output driver. A bypass capacitor is required.

Applications

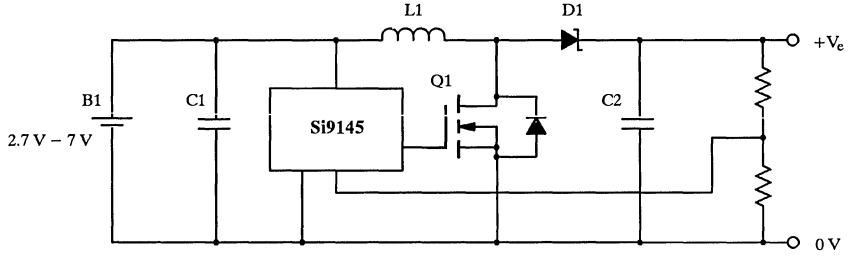


Figure 3. Non-Isolated Step Up Boost Converter for $V_{OUT} > V_{IN}$

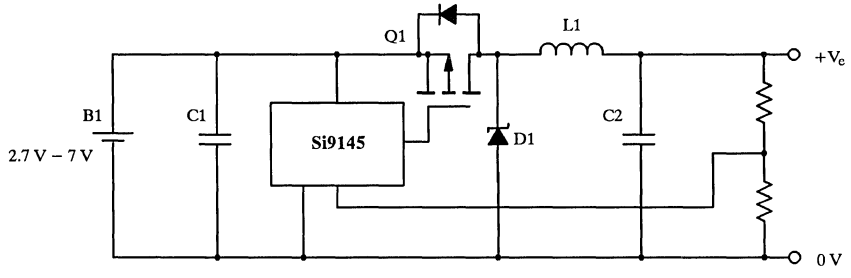


Figure 4. Non-Isolated Step Down Buck Converter for $V_{OUT} < V_{IN}$

Application Examples (Cont'd)

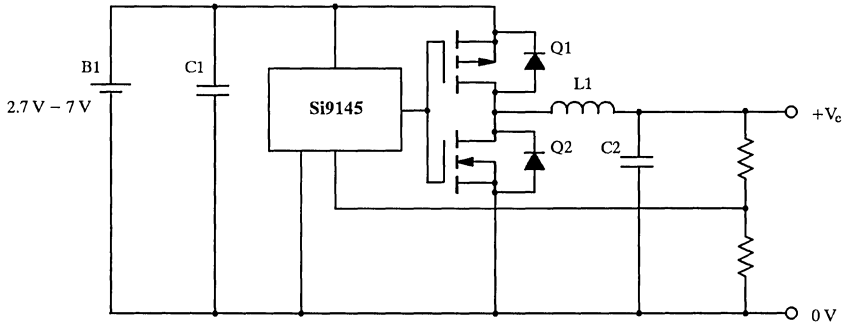


Figure 5. Non-Isolated Synchronous Buck Converter for $V_{OUT} < V_{IN}$

Si9150

Siliconix

Synchronous Buck Converter Controller

Features

- 6- to 16.5-V Input Range (Si9150CY)
- Voltage-Mode PWM Control
- Low-Current Standby Mode
- Enable Control
- Dual 100-mA Output Drivers
- 2% Band Gap Reference
- Multiple Converters Easily Synchronized
- Over-Current Protection

Description

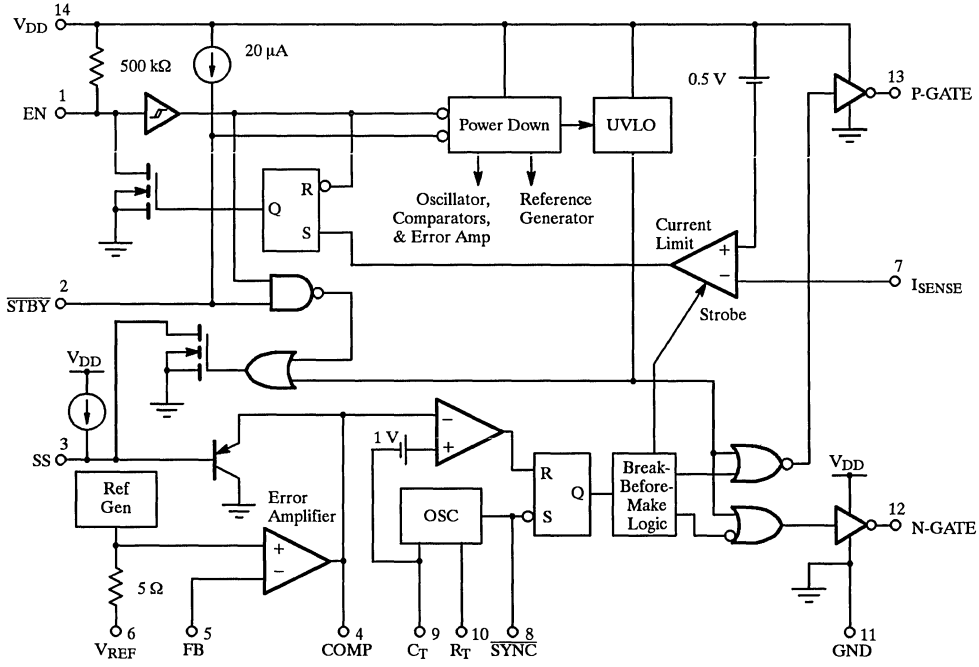
The Si9150 synchronous buck regulator controller is ideally suited for high-efficiency step down converters in battery-powered equipment. Combined with the Si9943DY MOSFET half-bridge, a 90% efficient, 7.5-W, 3.3-V or 5-V power supply can be implemented using standard surface-mount assembly techniques. The wide input range allows operation from NiCd or NiMH battery packs using six to ten cells.

Over-current protection is achieved by sensing the on-state voltage drop across the high side p-channel MOSFET, which eliminates the need for a current sense resistor.

Duty ratios of 0 to 100% and switching frequencies up to 300 kHz are possible. The IC can be disabled by pulling EN low (I_{DD} = 100 µA), or the 2.5-V reference can be maintained, with all other functions disabled, by pulling $\overline{STBY}$ low (I_{DD} = 500 µA).

The Si9150 is available in a 14-pin SOIC and rated for the commercial temperature range of 0 to 70°C.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to GND.

V_{DD} ..... 18 V

I_{SENSE} Input ..... −2 V to V_{DD} +2 V

All Other Inputs ..... −0.3 to V_{DD} + 0.3 V

P-Gate, N-Gate Continuous Source/Sink Current ..... 50 mA

Storage Temperature ..... −65 to 125°C

Operating Junction Temperature ..... 150°C

Power Dissipation (Package)a

14-Pin SOIC (Y Suffix)[b] ..... 900 mW

Thermal Impedance (Θ_{JA})

14-Pin SOIC ..... 140°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 7.2 mW/°C.

Specifications[a]

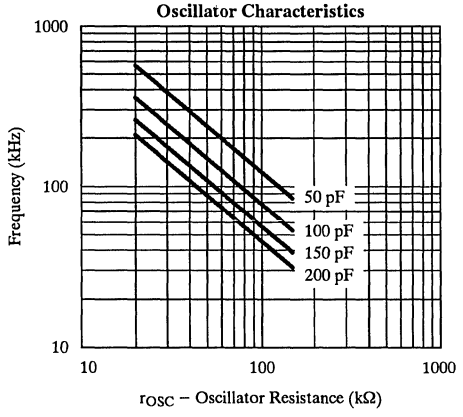
Parameter	Symbol	Test Conditions Unless Otherwise Specified 6.0 ≤ V_{DD} ≤ 16.5 V	Limits C Suffix – 0 to 70°C Min[b]	Typ[c]	Max[b]	Unit
Reference						
Output Voltage	V_{REF}	T_A = 25°C, Measured at Feedback[e], Pin 5	2.45	2.50	2.55	V
		T_{MIN} to T_{MAX}[d]	2.425	2.500	2.575	
Oscillator						
Maximum Frequency	f_{MAX}	C_{OSC} =94.3 pF, R_{OSC} = 28.7 k, T_A = 25°C[f]	255	300	345	kHz
Initial Accuracy	f_{OSC}	C_{OSC} =212 pF, R_{OSC} = 41.2 k, T_A = 25°C[f]	85	100	115	
Oscillator Ramp Amplitude	V_{OSC}	T_A = 25°C, 100 kHz	2.05	2.65	2.85	V
Temperature Stability[d]	f_{TEMP}	V_{DD} = 10 V, T_{MIN} to T_{MAX}	−5	±3	+5	%
Error Amplifier						
Input BIAS Current	I_B	V_{FB} = V_{REF}		25	500	nA
Open Loop Voltage Gain[d]	A_{VOL}		60	72		dB
Offset Voltage	V_{OS}			10	25	mV
Unity Gain Bandwidth[d]	BW		1	1.5		MHz
Output Current	I_{OUT}	Source, V_{COMP} = 2.50 V		−0.30	−0.20	mA
		Sink, V_{COMP} = 1.0 V	1	2.5		
Power Supply Rejection	PSRR		50	70		dB
Protection						
Current Limit Threshold Voltage	V_{CL}	T_A = 25°C, V_{DD} = 10 V	0.43	0.49	0.55	V
Current Limit Delay to Output[d]	t_d	T_A = 25°C		500	1000	ns
Undervoltage Lockout Voltage	V_{UVLO}	Upper Threshold	5.4	5.7	6.0	V
Undervoltage Hysteresis	V_{HYS}		0.10	0.17	0.25	
Softstart Pull-Up Current	I_{SS}			20		µA
Supply						
Supply Current – Enable Low	I_{OFF}			60	100	µA
Supply Current – Enable High	I_{CC}	C_L = 0 pF, f_{OSC} = 100 kHz, V_{DD} = 10 V		2.2	3.0	mA
Supply Current – $\overline{STBY}$ Low	I_{SB}			300	500	µA

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified 6.0 ≤ V_{DD} ≤ 16.5 V	Limits C Suffix – 0 to 70°C Min[b]	Typ[c]	Max[b]	Unit
Output						
Output High Voltage	V_{OH}	I_{OUT} = 10 mA, V_{DD} = 10 V	9.75			V
Output Low Voltage	V_{OL}	I_{OUT} = −10 mA, V_{DD} = 10 V			0.25	V
Output Resistance	R_{OUT}	I_{OUT} = 100 mA, V_{DD} = 10 V		10	20	Ω
Rise Time[d]	t_r	C_L = 800 pF, V_{DD} = 10 V		30	60	ns
Fall Time[d]	t_f			30	60	ns
Logic						
Delay to Output	$t_{d(EN)}$	Transition High to Low		0.25	1	µs
Enable Pull-Up Resistance	R_{EN}			500		kΩ
$\overline{STBY}$ Pull-Up Current	$I_{\overline{STBY}}$	T_A = 25°C, $V_{\overline{STBY}}$ = 0 V, V_{DD} = 10 V	−25	−20	−15	µA
Turn-On Threshold	V_{ENH}	V_{DD} = 10 V, Rising Input Voltage	6	6.8	8	V
Turn-Off Threshold	V_{ENL}	V_{DD} = 10 V, Falling Input Voltage	2	3.75	5	V

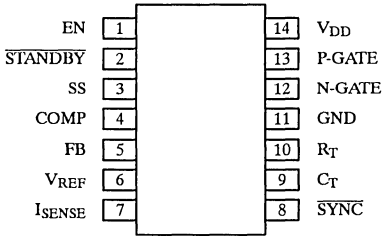
Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. The voltage reference is trimmed with the feedback (Pin 5) connected to compensation (Pin 4) so that the effect of the error amplifier's input offset voltage is eliminated.
f. C_{OSC} includes the PC board's parasitic capacitance.

Typical Characteristics



Pin Configuration

SOIC



Top View

Order Number: Si9150CY

Pin Description

Pin 1: EN

When this pin is low, the IC is shut down. After a low signal is applied to EN, then COMP, REF, R_T, and C_T settle toward ground; N-GATE, $\overline{\text{STBY}}$ and Soft-Start are grounded; and P-GATE is pulled high. The current consumption is no more than 100 µA in this state. This input's threshold has substantial hysteresis so that a capacitor to GND can be used to delay restart after the current limit is activated. After V_{ENH} is exceeded, one clock cycle elapses before N-GATE and P-GATE are enabled. EN is pulled up to V_{DD} through a 500-k resistor and is pulled down internally when the current limit is triggered.

Pin 2: $\overline{\text{STBY}}$

Has a function similar to EN. The differences are that the EN pin is unaffected, that the reference is still available, that bias currents are still present internally, and that this pin's pull up current is present. This pin should be used to disable an application if the reference voltage is still needed.

Pin 3: Soft-Start (SS)

This pin limits the maximum voltage that the error amplifier can output. A capacitor between this pin and ground will limit the rate at which the duty factor can increase during initial power up, during a restart when EN or $\overline{\text{STBY}}$ goes high, or after the current limit is triggered. A capacitor here can prevent an application from triggering the Si9150's current limit during startup. Soft-Start is pulled low if either EN or $\overline{\text{STBY}}$ is low.

Pin 4: Compensation (COMP)

This pin is tied directly to the output of the error amplifier. The feedback network which insures the stability of an application uses this pin. COMP settles low when either EN or $\overline{\text{STBY}}$ is pulled low.

Pin 5: Feedback (FB)

This pin is attached directly to the inverting input of the error amplifier. This pin is used to regulate the power supply's output voltage.

Pin 6: Reference (V_{REF})

The internal 2.5-V reference generator is attached to this pin through a 5-Ω resistor. A 0.1-µF bypass capacitor is needed to suppress noise. Also note that the generator has an open emitter; it will not pull down. The maximum current that the generator will source before it current limits is about 10 mA. Many parts of the IC use this voltage, so it is important not to overload the reference generator.

Pin 7: I_{SENSE}

This pin should be attached to the switched node (the drains of the application's p-channel and n-channel MOSFETs). If the voltage between V_{DD} and this pin is more then 0.46 V while the P-GATE is low, the current limit is activated. The current limit is relatively slow to prevent false triggering due to noise. Activating the current limit causes EN to be pulled to GND. I_{SENSE} may be operated from V_{DD} + 2 V to GND − 2 V.

Pin Description (Cont'd)

Pin 8: $\overline{\text{SYNC}}$

This pin forces the clock to reset when low, and is also pulled low when the clock resets itself. Thus if several Si9150's have their sync pins shorted together, they will be synchronized; the shortest duration clock will control the other clocks.

Pin 9: C_T

A capacitor from this pin to ground is charged until it reaches 2.5 V, at which point the capacitor is rapidly discharged. The resulting sawtooth with about 1 V added is compared to the input voltage at COMP to determine whether P-GATE and N-GATE should be high or low. The maximum recommended value for C_{OSC} is 200 pF (See Typical Characteristics). The capacitor's charging current is controlled by Pin 10, R_T.

Pin 10: R_T

The IC applies 2.5 V to this pin, and the current is mirrored and applied to Pin 9 while charging the capacitor. The minimum recommended value of R_{OSC} is 20 kΩ (Figure 1).

Pin 11: GND

Since the Si9150 has a high-side current limit, it is important that V_{DD} track the voltage on the source of the p-channel power MOSFET. For noise immunity, it is best to separate the logic ground from the power ground. The logic ground should be decoupled to V_{DD} through at least a 1-µF capacitor. The two grounds may be connected by a path that is long compared to the the path from V_{DD} to the source of the application's p-channel MOSFET.

Pin 12: N-GATE

This pin is used to drive the application's n-channel MOSFET. When turning the n-channel MOSFET off, the p-channel MOSFET will not be turned on until N-GATE is within a few volts of ground. This pin is low while either EN or $\overline{\text{STBY}}$ is low.

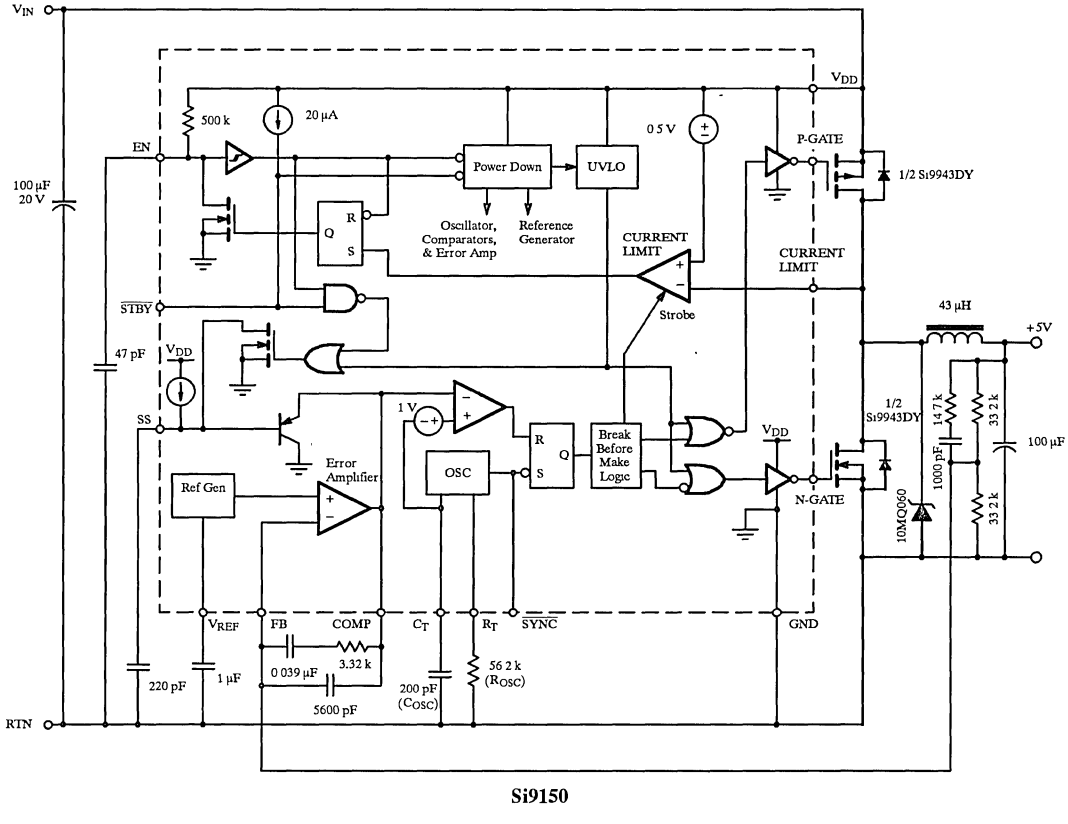
Pin 13: P-GATE

This pin is used to drive the application's p-channel MOSFET. The break before make circuitry for the P-GATE is complimentary to that for the N-GATE. This pin is high while either EN or $\overline{\text{STBY}}$ is low.

Pin 14: V_{DD}

This pin powers the IC. The connection between this pin and the source of the p-channel FET should be as short as practical. Read Pin 11's description for bypassing suggestions.

Applications



Si9150

Figure 1. Typical Application Circuit

Si9710CY

Siliconix

PCMCIA Interface Switch

Features

- Single SO-16 Package
- CMOS Inputs with Hysteresis
- Extremely Low R_{ON}
- Reverse Blocking Switches
- HiZ Outputs in the Off-State
- Low Power Consumption
- Safe Power-Up

Description

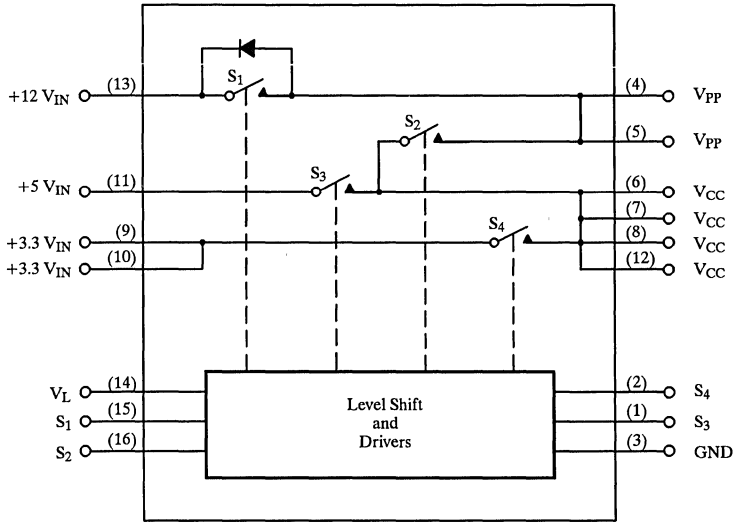
The Si9710CY switch is a monolithic switch designed to meet the needs of the PCMCIA interface. The inputs are fully CMOS compatible and incorporate all the level shift and interface required to be driven by any CMOS driver. The external inputs can be driven to 3.3-V or 5-V by setting V_L at the appropriate level. The switches are low R_{ON} and can carry the maximum currents found on the PCMCIA interface.

The 5-V and 3.3-V switches do not have the parasitic diode found in vertical DMOS power switches.

Low R_{ON} is achieved by using MOSFETs driven off the $+12\text{-}V_{IN}$ input. All level shifting is built into the PCMCIA switch.

The Si9710CY is available in an SO-16 package and is rated over the commercial temperature range 0 to 70°C.

Functional Block Diagram



Truth Table – S_1 through S_4

Logic	Switch
0	OFF
1	ON

Absolute Maximum Ratings

Voltages Referenced to Ground

V_L ..... 7 V
+12 V_{IN} ..... 15 V
+5 V_{IN} ..... 7 V
+3.3 V_{IN} ..... 7 V
S_1 through S_4 (CMOS Inputs) ..... V_L + 0.5 V
I_{OUT} V_{PP} ..... 300 mA
V_{CC} ..... 7 V
V_{PP} ..... 15 V
All Pins ..... −0.5 V
I_{OUT} V_{CC} ..... 1500 mA
PD Max: (T_A = 25°C) ..... 710 mW
(T_A = 70°C) ..... 390 mW
Junction Temperature ..... 125°C

Thermal Ratings

$R_{\Theta JA}$ ..... 140 °C/W

Recommended Operating Conditions

+12 V_{IN} ..... 12 V ± 10%
+5 V_{IN} ..... 5 V ± 10%
+3.3 V_{IN} ..... 3.3 V ± 10%
I_{OUT} V_{CC} ..... 1000 mA
I_{OUT} V_{PP} ..... 150 mA
V_L ..... 5.0 V ± 10%

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified +5 V_{IN} = 5 V, +3.3 V_{IN} = 3.3 V +12 V_{IN} = 12 V, V_L = 5.0 V, GND = 0 V		Limits C Suffix, 0 to 70°C Min[a]	Typ	Max[a]	Unit
Switch 1							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 10.8 V S_1 = V_L, S_2 = GND	T_A = 25°C			200	mΩ
			T_A = 70°C			250	
Off Current (+12 V_{IN} to V_{PP})	I_{OFF}	+12 V_{IN} = 13.2 V, V_{PP} = 0 V S_1 = GND	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S1(on)}$	C_L = 0.1 µF, S_2 = Low, R_L = 100 Ω, See Figure 1		0.1		1	µs
	$t_{S1(off)}$			0.5		4	
Switch 2							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 10.8 V S_2 = S_3 = V_L	T_A = 25°C			300	mΩ
			T_A = 70°C			350	
Off Current	I_{OFF}	V_{PP} = 13.2 V, V_{CC} = 0 V +12 V_{IN} = 13.2 V	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S2(on)}$	C_L = 0.1 µF, R_L = 100 Ω, S_1 = S_4 = GND S_3 = V_L, See Figure 1		0.1		1	µs
	$t_{S2(off)}$			0.5		4	
Switch 3							
On-Resistance	R_{ON}	I = 500 mA, +12 V_{IN} = 10.8 V S_3 = V_L	T_A = 25°C			200	mΩ
			T_A = 70°C			250	
Off Current	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S3(on)}$	+5 V_{IN} = 5 V, C_L = 0.1 µF, V_{CC} to GND R_L = 100 Ω, V_{CC} to GND, See Figure 2		0.1		1	µs
	$t_{S3(off)}$			0.5		4	

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified +5 V_{IN} = 5 V, +3.3 V_{IN} = 3.3 V +12 V_{IN} = 12 V, V_L = 5.0 V, GND = 0 V		Limits C Suffix, 0 to 70°C Min[a]	Typ	Max[a]	Unit
Switch 4							
On-Resistance	R_{ON}	I = 500 mA, +12 V_{IN} = 10.8 V S_4 = V_L	T_A = 25°C			150	mΩ
			T_A = 70°C			185	
Off Current	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V S_2 = S_3 = S_4 = GND	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S4(on)}$	+3.3 V_{IN} = 3.3 V, C_L = 0.1 µF, S_3 = GND R_L = 100 Ω, See Figure 2		0.1		1	µs
	$t_{S4(off)}$			0.5		4	
Power Supply							
+12 V_{IN} Current	$I_{+12VIN(1)}$	S_1 = S_4 = GND, S_2 = S_3 = V_L				10	µA
	$I_{+12VIN(2)}$	S_1 = S_4 = V_L, S_2 = S_3 = GND				10	
V_L Current	$I_{VL(1)}$	S_1 = S_4 = GND, S_2 = S_3 = V_L				10	
	$I_{VL(2)}$	S_1 = S_4 = V_L, S_2 = S_3 = GND				10	
Switch Control Inputs							
Input Voltage High	$V_{I(H)}$		V_L = 3.3 V	2.8	2.4		V
			V_L = 5 V	4.0	3.3		
Input Voltage Low	$V_{I(L)}$		V_L = 3.3 V		1.1	0.4	
			V_L = 5 V		1.5	0.8	
Input Hysteresis[b]	$V_{I(H)}-V_{I(L)}$		V_L = 3.3 V	0.5	1.3		
			V_L = 5 V	0.8	1.8		
Input Current High	$I_{I(H)}$	S_1 through S_4 = V_L, V_L = 5 V				1.0	µA
Input Current Low	$I_{I(L)}$	S_1 through S_4 = GND, V_L = 5 V		−1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Guaranteed by design, not subject to production testing.

Timing Waveforms

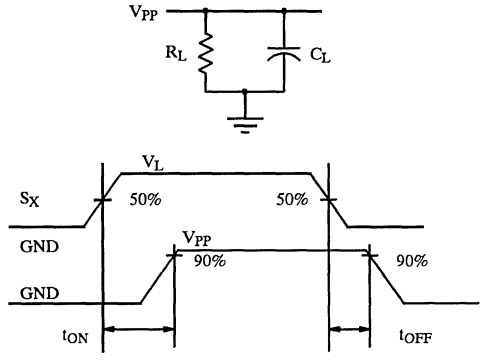


Figure 1.

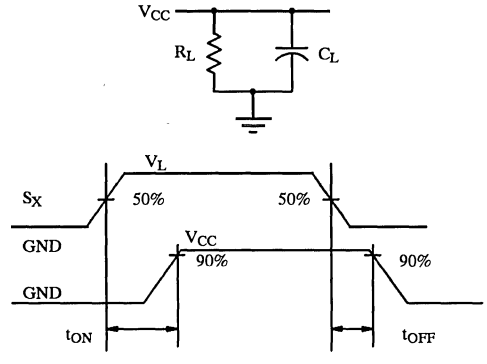
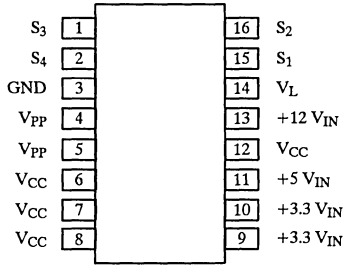


Figure 2.

Pin Configuration

SOIC-16



Top View

Order Number Si9710CY

Pin Description

Pin Number	Symbol	Description
1	S_3	Control input for selecting +5 V_{IN} to V_{CC}. The PCMCIA terminology for this pin is $V_{CC}\_EN_1$.
2	S_4	Control input for selecting +3.3 V_{IN} to V_{CC}. The PCMCIA terminology for this pin is $V_{CC}\_EN_0$.
3	GND	Ground connection.
4, 5	V_{PP}	Program and peripheral voltage to PCMCIA slot.
6, 7, 8, 12	V_{CC}	Supply voltage to slot.
9, 10	+3.3 V_{IN}	+3.3-V supply.
11	+5 V_{IN}	+5-V supply.
13	+12 V_{IN}	+12-V supply.
14	V_L	Rail voltage for switch control inputs, selectable to 5-V or 3.3-V.
15	S_1	Control input for selecting +12 V_{IN} to V_{PP}. The PCMCIA terminology for this pin is $V_{PP}\_EN_1$.
16	S_2	Control input for selecting V_{CC} to V_{PP}. The PCMCIA terminology for this pin is $V_{PP}\_EN_0$.

Si9711CY

Siliconix

PCMCIA Interface Switch

Features

- Single SO-16 Package
- CMOS Inputs with Hysteresis
- Extremely Low R_{ON}
- Reverse Blocking Switches
- Hi-Z Outputs in the Off-State
- Low Power Consumption
- Safe Power -Up

Description

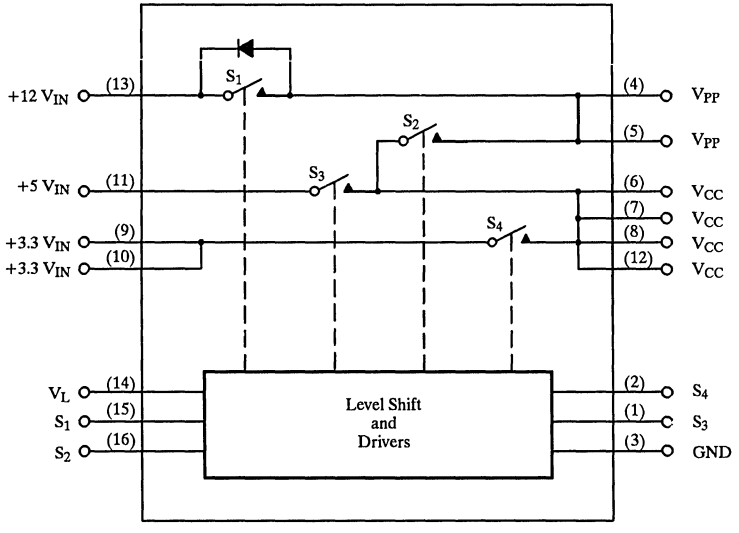
The Si9711CY is a monolithic switch designed to meet the needs of the PCMCIA interface. The inputs are fully CMOS compatible and incorporate all the level shift and interface required to be driven by any CMOS driver. The external inputs can be driven to 3.3-V or 5-V by setting V_L at the appropriate level. The switches are low R_{ON} and can carry the maximum currents found on the PCMCIA interface.

The 5-V and 3.3-V switches do not have the parasitic diode found in vertical DMOS power switches.

Low R_{ON} is achieved by using MOSFETs driven off the +12-V_{IN} input. All level shifting is built into the Si9711CY.

The Si9711CY is packaged in an SO-16 package and is rated over the commercial temperature range 0 to 70°C.

Functional Block Diagram



Truth Table – S_1 through S_4

Logic	Switch
0	OFF
1	ON

Preliminary

Absolute Maximum Ratings

Voltages Referenced to Ground

V_L ..... 7 V
+12 V_{IN} ..... 15 V
+5 V_{IN} ..... 7 V
+3.3 V_{IN} ..... 7 V
S_1 through S_4 (CMOS Inputs) ..... V_L + 0.5 V
I_{OUT} V_{PP} ..... 300 mA
V_{CC} ..... 7 V
V_{PP} ..... 15 V
All Pins ..... −0.5 V
I_{OUT} V_{CC} ..... 1.5 A
PD Max: (T_A = 25°C) ..... 710 mW
(T_A = 70°C) ..... 390 mW
Junction Temperature ..... 125°C
Thermal Ratings
$R_{\Theta JA}$ ..... 140 °C/W

Recommended Operating Conditions

+12 V_{IN} ..... 12 V ± 10%
+5 V_{IN} ..... 5 V ± 10%
+3.3 V_{IN} ..... 3.3 V ± 10%
I_{OUT} V_{CC} ..... 1 A
I_{OUT} V_{PP} ..... 150 mA
V_L ..... 5.0 V ± 10%

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified +5 V_{IN} = 5 V, +3.3 V_{IN} = 3.3 V +12 V_{IN} = 12 V, V_L = 5.0 V, GND = 0 V		Limits C Suffix, 0 to 70°C Min[a]	Typ	Max[a]	Unit
Switch 1							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 10.8 V S_1 = V_L, S_2 = GND	T_A = 25°C			200	mΩ
			T_A = 70°C			250	
Off Current (+12 V_{IN} to V_{PP})	I_{OFF}	+12 V_{IN} = 13.2 V, V_{PP} = 0 V S_1 = GND	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S1(on)}$	C_L = 0.1 µF, S_2 = Low, R_L = 100 Ω, See Figure 1		0.1		1	µs
	$t_{S1(off)}$			0.5		4	
Switch 2							
On-Resistance	R_{ON}	I = 120 mA, +12 V_{IN} = 10.8 V S_2 = S_3 = V_L	T_A = 25°C			300	mΩ
			T_A = 70°C			350	
Off Current	I_{OFF}	V_{PP} = 13.2 V, V_{CC} = 0 V +12 V_{IN} = 13.2 V	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{S2(on)}$	C_L = 0.1 µF, R_L = 100 Ω, S_1 = S_4 = GND, S_3 = V_L, See Figure 1		0.1		1	µs
	$t_{S2(off)}$			0.5		4	
Switch 3							
On-Resistance	R_{ON}	I = 500 mA, +12 V_{IN} = 10.8 V S3 = V_L	T_A = 25°C			200	mΩ
			T_A = 70°C			250	
Off Current	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{d(on)}$	+5 V_{IN} = 5 V, C_L = 0.1 µF, V_{CC} to GND R_L = 100 Ω, V_{CC} to GND, See Figure 2		1			µs
	$t_{ramp(on)}$			200			
	$t_{S3(off)}$			0.5		4	

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified +5 V_{IN} = 5 V, +3.3 V_{IN} = 3.3 V +12 V_{IN} = 12 V, V_L = 5.0 V, GND = 0 V		Limits C Suffix, 0 to 70°C Min[a]	Typ	Max[a]	Unit
Switch 4							
On-Resistance	R_{ON}	I = 500 mA, +12 V_{IN} = 10.8 V $S_4 = V_L$	T_A = 25°C			150	mΩ
			T_A = 70°C			185	
Off Current	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V $S_2 = S_3 = S_4$ = GND	T_A = 25°C			1	µA
			T_A = 70°C			10	
Switching Time	$t_{d(on)}$	+3.3 V_{IN} = 3.3 V, C_L = 0.1 µF, S_3 = GND R_L = 100 Ω, See Figure 2		1			µs
	$t_{ramp(on)}$			200			
	$t_{S4(off)}$			0.5		4	
Power Supply							
+12 V_{IN} Current	$I_{+12VIN(1)}$	$S_1 = S_4$ = GND, $S_2 = S_3 = V_L$				10	µA
	$I_{+12VIN(2)}$	$S_1 = S_4 = V_L$, $S_2 = S_3$ = GND				10	
V_L Current	$I_{VL(1)}$	$S_1 = S_4$ = GND, $S_2 = S_3 = V_L$				10	
	$I_{VL(2)}$	$S_1 = S_4 = V_L$, $S_2 = S_3$ = GND				10	
Switch Control Inputs							
Input Voltage High	$V_{I(H)}$		V_L = 3.3 V	2.8	2.4		V
			V_L = 5 V	4.0	3.3		
Input Voltage Low	$V_{I(L)}$		V_L = 3.3 V		1.1	0.4	
			V_L = 5 V		1.5	0.8	
Input Hysteresis[b]	$V_{I(H)}-V_{I(L)}$		V_L = 3.3 V	0.5	1.3		
			V_L = 5 V	0.8	1.8		
Input Current High	$I_{I(H)}$	S_1 through $S_4 = V_L$, V_L = 5 V				1.0	µA
Input Current Low	$I_{I(L)}$	S_1 through S_4 = GND, V_L = 5 V		−1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Guaranteed by design, not subject to production testing.

Timing Waveforms

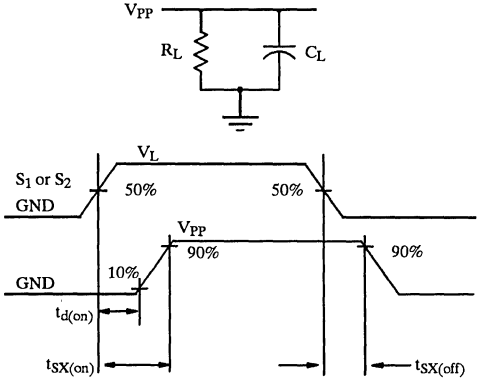


Figure 1. $t_{d(on)}$ and $t_{SX(on)}$

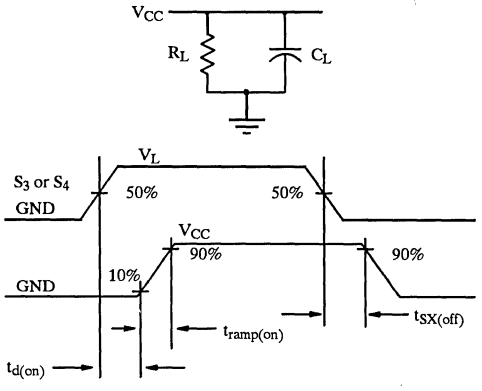
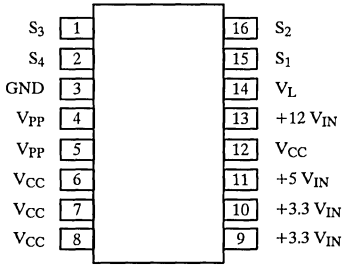


Figure 2. $t_{ramp(on)}$

Pin Configuration

SO-16



Top View

Order Number: Si9711CY

Pin Description

Pin Number	Symbol	Description
1	S_3	Control input for selecting +5 V_{IN} to V_{CC}. The PCMCIA terminology for this pin is $V_{CC}\_EN_1$.
2	S_4	Control input for selecting +3.3 V_{IN} to V_{CC}. The PCMCIA terminology for this pin is $V_{CC}\_EN_0$.
3	GND	Ground connection.
4, 5	V_{PP}	Program and peripheral voltage to PCMCIA slot.
6, 7, 8, 12	V_{CC}	Supply voltage to slot.
9, 10	+3.3 V_{IN}	+3.3-V supply.
11	+5 V_{IN}	+5-V supply.
13	+12 V_{IN}	+12-V supply.
14	V_L	Rail voltage for switch control inputs, selectable to 5-V or 3.3-V.
15	S_1	Control input for selecting +12 V_{IN} to V_{PP} . The PCMCIA terminology for this pin is $V_{PP}\_EN_1$.
16	S_2	Control input for selecting V_{CC} to V_{PP} . The PCMCIA terminology for this pin is $V_{PP}\_EN_0$.

1326

TEMIC

Si9717CY

Siliconix

Battery Disconnect Switch

Features

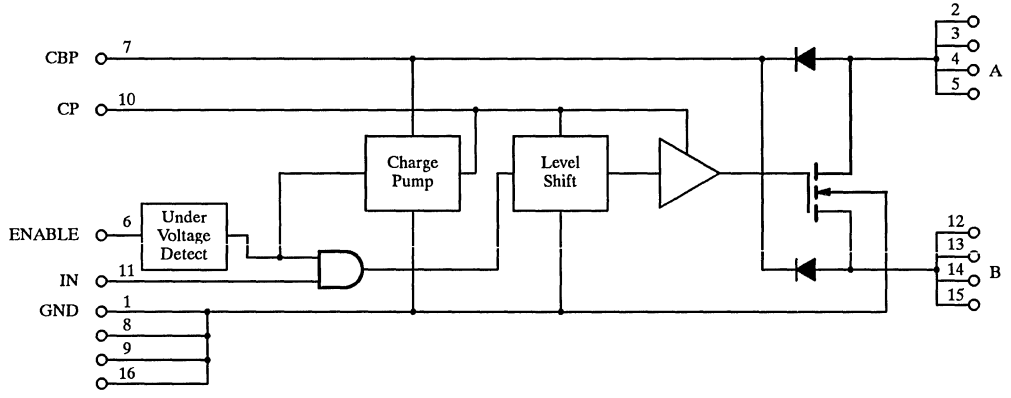
- 6- to 18-V Operation
- Separate Logic Voltage Input
- Undervoltage Lockout (UVL) @ V_L = 3 V
- Shutdown Control Capability
- Safe Power Down

Description

The Si9717CY is a reverse blocking switch for battery disconnect applications. It is an integrated solution for multiple battery technology designs or designs that require isolation from the power bus during charging.

The Si9717CY is available in a 16-pin SOIC package and is rated for the commercial temperature range of 0 to 70°C.

Functional Block Diagram



Absolute Maximum Ratings

Voltage Referenced to GND

V_A, V_B ..... −0.3 to 20 V
V_{IN} ..... −0.3 to 10 V
V_{ENABLE} ..... −0.3 to 10 V

Storage Temperature ..... −65 to 125°C
Power Dissipation ..... 2 W

Notes: Device mounted with all leads soldered to PC board.

Recommended Operating Range

V_A, V_B (see note) ..... 6 to 18 V
V_{IN} ..... 0 to 5 V
I_{AB} (continuous) ..... 0 to 4 A
I_{AB} x V_A (continuous) ..... 0 to 40 W
Minimum Cycle Time (turn-on to turn-on) ..... 10 ms
V_{ENABLE} ..... 0 to 5 V

Operating Temperature ..... 0 to 70°C
Junction Temperature ..... 0 to 150°C

Notes:
a. Si9717CY is functional at V_A, V_B = 5 to 6 V with higher supply current. See $I_{A(on)}$ specification.

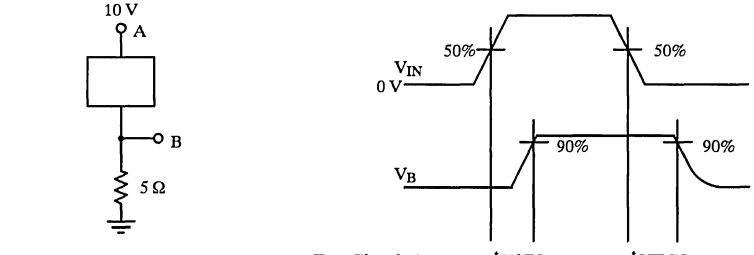
Advance Information

Specifications

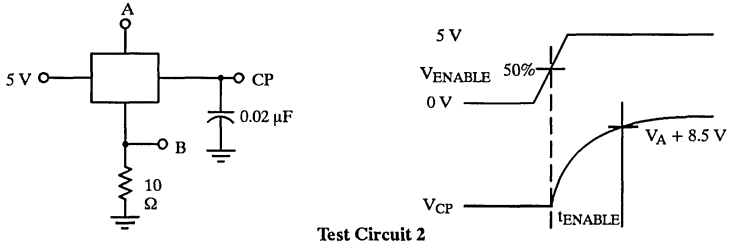
Parameter	Symbol	Test Conditions Unless Otherwise Specified $6\ V \leqq V_A \leqq 18\ V$ $C_{VDD} = 0.1\ \mu F$, CP = 0.02 µF	Temp[a]	Limits[d] Min[b]	Typ[c]	Max[b]	Unit
On-Resistance	R_{AB}	$V_A = 10\ V, I_A = 1\ A$	Room			0.06	Ω
Leakage Current	$I_{AB(off)}$	$V_A = 16\ V, V_B = 0\ V$	Room			10	µA
IN Low Threshold	$V_{IN(L)}$		Full			1	V
IN High Threshold	$V_{IN(H)}$		Full	4.0			
IN Input Current	$I_{IN(H)}$	$V_{IN} = 5.0\ V$	Full			1	µA
Turn-On Delay IN to A or B	$t_{ON(IN)}$	ENABLE = 5 V, $V_A = 10\ V, R_L = 5\ \Omega$ Test Circuit 1	Full			10	µs
Turn-Off Delay IN to A or B	$t_{OFF(IN)}$		Full			10	
ENABLE Low Threshold	$V_{ENABLE(L)}$		Full			3.0	V
ENABLE High Threshold	$V_{ENABLE(H)}$		Full	4.4			
ENABLE Input Current	$I_{ENABLE(H)}$	$V_{ENABLE} = 5\ V$	Full			50	µA
Setup Time from ENABLE to Switch	$t_{ENABLE(H)}$	$V_A = 10\ V, V_{IN} = 0\ V$, Test Circuit 2	Room			2.0	ms
		$V_A = 6\ V, V_{IN} = 0\ V$, Test Circuit 2	Full			10	
On-State Drain	$I_{A(on)}$	AB Shorted, $V_A = 10\ V, V_{ENABLE} = 5\ V$	Full			60	µA
		AB Shorted, $V_A = 5\ V, V_{ENABLE} = 5\ V$	Full			300	
Off-State Drain	$I_{A(off)}$	AB Shorted, $V_A = 10\ V, V_{ENABLE} = 0\ V$	Full			10	

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Tested at room temperature, high temperature guaranteed by statistical data correlation techniques.

Test Circuit



Test Circuit 1

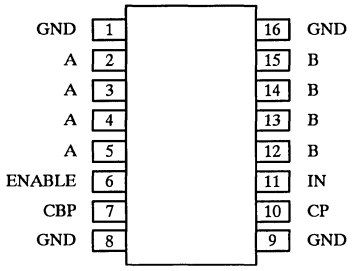


Test Circuit 2

Pin Configuration and Truth Table

ENABLE	IN	Switch Controller State	Switch
0	0	Inactive	X
0	1	Inactive	X
1	0	Set-Up	Off
1	1	Active	On

SO-16



Top View

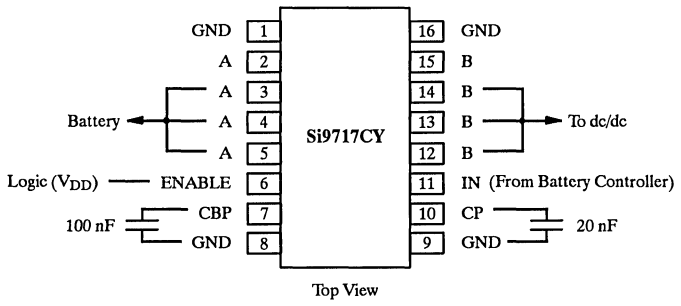
Order Number: Si9717CY

Pin Description

Pin Number	Symbol	Description
1, 8, 9, 16	GND	Common connection for negative battery terminals.
2, 3, 4, 5	A	A-terminal of the battery switch, bidirectional.
6	ENABLE	Logic input, ENABLE. Activates charge pump and switch drive logic.
7	CBP	Internally generated logic power supply, V_{DD}. Requires external bypass capacitor connected to pin 8.
10	CP	Charge pump output terminal. Requires external capacitor connected to pin 9.
11	IN	Logic input, IN. A high level turns on the switch.
12, 13, 14, 15	B	B-terminal of the battery switch, bidirectional.

Applications Diagram

SO-16



Top View

Battery Disconnect Switch

Features

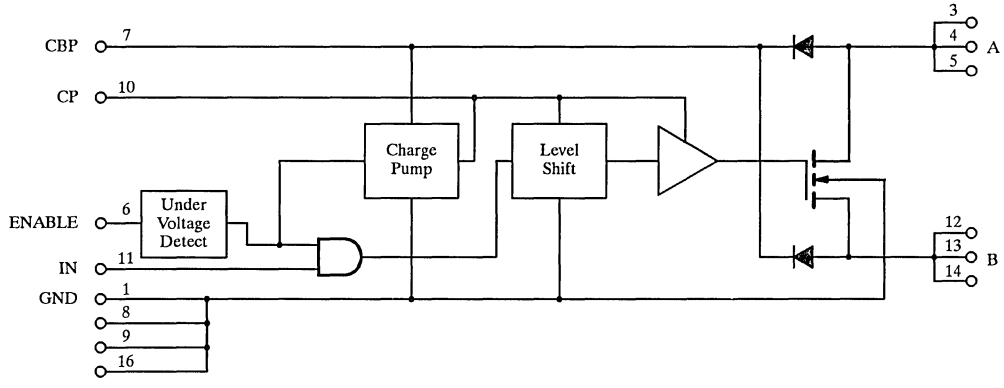
- 6- to 18-V Operation
- Separate Logic Voltage Input
- Undervoltage Lockout (UVL) @ V_L = 3 V
- Shutdown Control Capability
- Safe Power Down

Description

The Si9718CY is a reverse blocking switch for battery disconnect applications. It is an integrated solution for multiple battery technology designs or designs that require isolation from the power bus during charging.

The Si9718CY is available in a 16-pin SOIC package and is rated for the commercial temperature range of 0 to 70°C.

Functional Block Diagram



Absolute Maximum Ratings

Voltage Referenced to GND

V_A, V_B ..... −0.3 to 20 V

V_{IN} ..... −0.3 to 10 V

V_{ENABLE} ..... −0.3 to 10 V

Storage Temperature ..... −65 to 125°C

Power Dissipation ..... 2 W

Notes: Device mounted with all leads soldered to PC board.

Recommended Operating Range

V_A, V_B (See note a) ..... 6 to 18 V

V_{IN} ..... 0 to 5 V

I_{AB} (continuous) ..... 0 to 3.5 A

I_{AB} x V_A (continuous) ..... 0 to 35 W

Minimum Cycle Time (turn-on to turn-on) ..... 10 ms

V_{ENABLE} ..... 0 to 5 V

Operating Temperature ..... 0 to 70°C

Junction Temperature ..... 0 to 150°C

Notes:

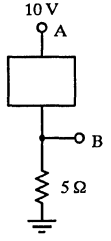
a. Si9718CY is functional at V_A, V_B = 5 to 6 V with higher supply current. See $I_{A(on)}$ specification.

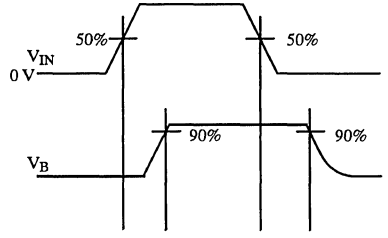
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified 6 V ≦ V_A ≦ 18 V C_{VDD} = 0.1 µF, CP = 0.02 µF	Temp[a]	Limits[d] Min[b]	Typ[c]	Max[b]	Unit
On-Resistance	R_{AB}	V_A = 10 V, I_A = 1 A	Room			0.08	Ω
Leakage Current	$I_{AB(off)}$	V_A = 16 V, V_B = 0 V	Room			10	µA
IN Low Threshold	$V_{IN(L)}$		Full			1	V
IN High Threshold	$V_{IN(H)}$		Full	4.0			
IN Input Current	$I_{IN(H)}$	V_{IN} = 5.0 V	Full			1	µA
Turn-On Delay IN to A or B	$t_{ON(IN)}$	ENABLE = 5 V, V_A = 10 V, R_L = 5 Ω Test Circuit 1	Full			10	µs
Turn-Off Delay IN to A or B	$t_{OFF(IN)}$		Full			10	
ENABLE Low Threshold	$V_{ENABLE(L)}$		Full			3.0	V
ENABLE High Threshold	$V_{ENABLE(H)}$		Full	4.4			
ENABLE Input Current	$I_{ENABLE(H)}$	V_{ENABLE} = 5 V	Full			50	µA
Setup Time from ENABLE to Switch	$t_{ENABLE(H)}$	V_A = 10 V, V_{IN} = 0 V, Test Circuit 2	Room			2.0	ms
		V_A = 6 V, V_{IN} = 0 V, Test Circuit 2	Full			10	
On-State Drain	$I_{A(on)}$	AB Shorted, V_A = 10 V, V_{ENABLE} = 5 V	Full			60	µA
		AB Shorted, V_A = 5 V, V_{ENABLE} = 5 V	Full			300	
Off-State Drain	$I_{A(off)}$	AB Shorted, V_A = 10 V, V_{ENABLE} = 0 V	Full			10	

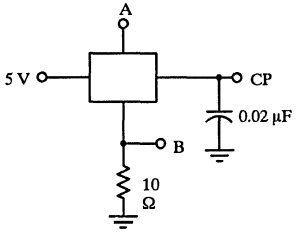
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Tested at room temperature, high temperature guaranteed by statistical data correlation techniques.

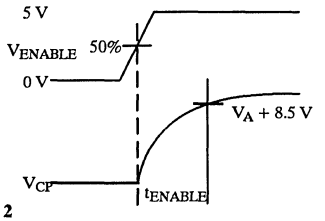
Test Circuit





Test Circuit 1



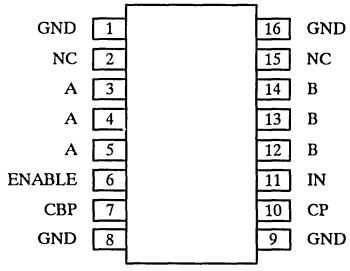


Test Circuit 2

Pin Configuration and Truth Table

ENABLE	IN	Switch Controller State	Switch
0	0	Inactive	X
0	1	Inactive	X
1	0	Set-Up	Off
1	1	Active	On

SO-16



Top View

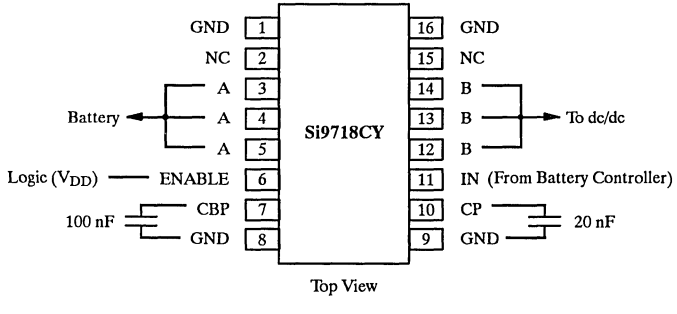
Order Number: Si9718CY

Pin Description

Pin Number	Symbol	Description
1, 8, 9, 16	GND	Common connection for negative battery terminals.
2, 15	NC	No internal connection.
3, 4, 5	A	A-terminal of the battery switch, bidirectional.
6	ENABLE	Logic input, ENABLE. Activates charge pump and switch drive logic.
7	CBP	Internally generated logic power supply, V_{DD}. Requires external bypass capacitor connected to pin 8.
10	CP	Charge pump output terminal. Requires external capacitor connected to pin 9.
11	IN	Logic input, IN. A high level turns on the switch.
12, 13, 14	B	B-terminal of the battery switch, bidirectional.

Applications Diagram

SO-16



Top View

Motor Control & MOSFET Drivers

4

About Motor Control

Siliconix power ICs for motor control serve a range of applications from hard disk drives to machine tools. All products in this category eliminate the need for several discrete components, and most are available in surface-mount packages. In every case, they have been designed to integrate key functions—like voice coil motor control in disk drives, three-phase brushless motor control in photocopiers and printers, and high-voltage motor control in water pumps and household appliances—while promoting efficiency, manufacturability, and cost-effectiveness.

Siliconix

D469A

Quad High-Current Power Driver

Features

- Wide Voltage Range
- High Current Drive
- Fast Rise and Fall Times
- Low Power Consumption
- Single Power Supply
- Low Output Impedance
- TTL/CMOS Inputs
- ESD Protection

Applications

- Motor Drives
- Power Supplies
- dc/dc Converters

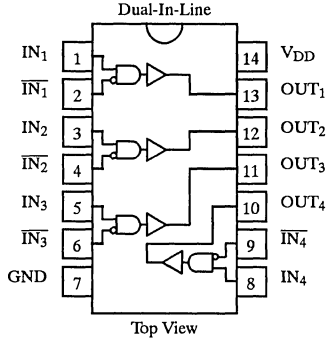
End Products

- Computers
- Printers
- Avionics
- Industrial Controllers
- Robotics
- Central Office Equipment

Description

The D469A is a quad monolithic high-current and high-speed driver designed to interface logic level signals to power MOSFETs, at voltages up to 15 V, in motor controls and other power control applications. This 4-channel power driver can source or sink up to 1.5 A.

Pin Configuration, Functional Block Diagram and Truth Table



Truth Table

IN_X	$\overline{IN_X}$	OUT_X
0	0	Low
0	1	Low
1	0	High
1	1	Low

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	14-Pin Plastic DIP	D469ADJ
−55 to 125°C	14-Pin Sidebraze	D469AAP
		D469AAP/883
		5962-9098301MCA

Absolute Maximum Ratings

Ambient Temperature Under Bias ..... −55 to 125°C
Voltage on Any Pin with Respect to Ground ... −0.3 to V_{DD} +0.3 V
Supply Voltage, V_{DD} ..... −0.3 to 18 V
Peak Output Current ..... ±1.5 A
DC Continuous Current (Any Output) ..... 100 mA
AC Time Average Current ..... 100 mA
Storage Temperature ..... −65 to 150°C
Operating Temperature (A Suffix) ..... −55 to 125°C
(D Suffix) ..... −40 to 85°C
Junction Temperature ..... 150°C

Power Dissipation (Package)[a]
14-Pin Plastic DIP[b] ..... 1000 mW
14-Pin Sidebraze[c] ..... 750 mW
Themal Impedance (Θ_{JA})
14-Pin Plastic DIP ..... 100°C/W (No Airflow)
14-Pin Sidebraze ..... 167°C/W(No Airflow)

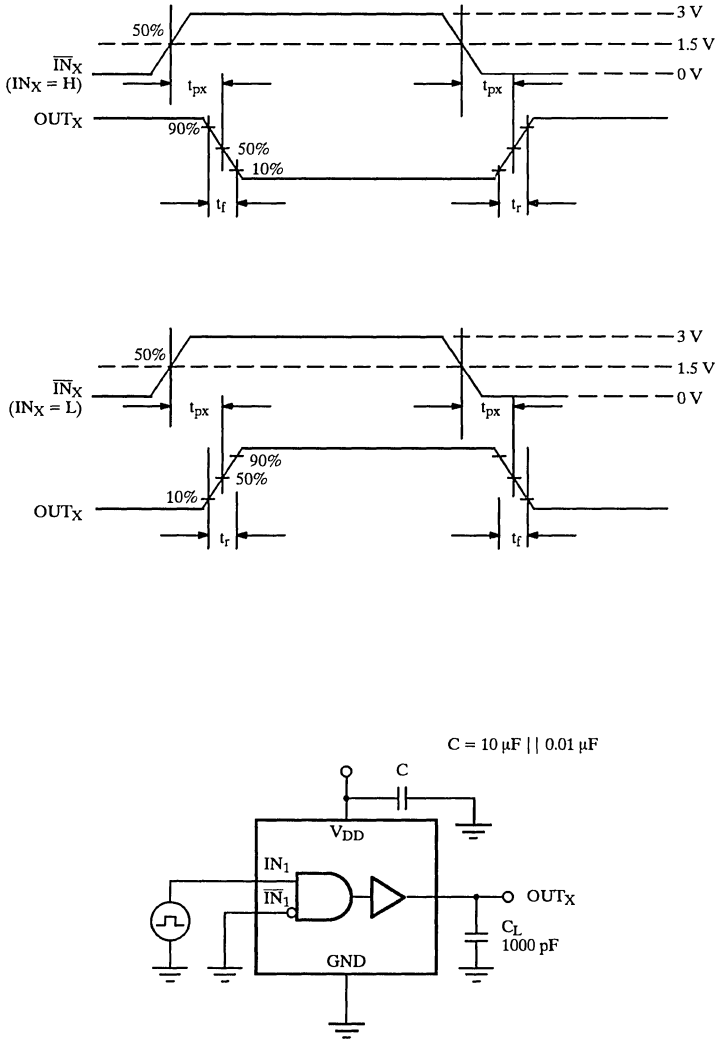
Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 10 mW/°C above 50°C.
c. Derate 6 mW/°C above 25°C.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 15 V T_A = Operating Temperature Range	Limit Min[a]	Typ[b]	Max[a]	Unit
Input						
Input Voltage High	V_{INH}		2.4			V
Input Voltage Low	V_{INL}				0.8	
Input Current, Input Voltage High	I_{INH}	$V_{IN} = V_{DD}$		0.001	10	µA
Input Current, Input Voltage Low	I_{INL}	V_{IN} = 0 V	−10	−0.001		
Output						
Output Voltage High	V_{OUTH}	I_{OUT} = −100 mA, One Output at a Time	13	14.44		V
		I_{OUT} = −10 mA	14.8	14.95		
Output Voltage Low	V_{OUTL}	I_{OUT} = 100 mA, One Output at a Time		0.33	1	
		I_{OUT} = 10 mA		0.033	0.1	
Output Source Current	I_{OS+}			1.5		A
Output Sink Current	I_{OS1}			−1.5		
Output Resistance	R_{OUT}	I_{OUT} = 10 mA		3.5		Ω
		I_{OUT} = −10 mA		5.5		
Dynamic						
Propagation Delay	t_{px}	C_L = 1000 pF (See Figure 1)		30	80	ns
Rise Time	t_r			10		
Fall Time	t_f			10		
Input Capacitance	C_{in}			5		pF
Supply						
Supply Current	I_{DD}	$IN_X = \overline{IN_X}$ = 0 V, V_{DD} = 15.75 V		1.4	20	mA
		$IN_X = \overline{IN_X}$ = 3 V, V_{DD} = 15.75 V		1.4	30	
		f = 100 kHz, V_{DD} = 15.75 V, C_L = 1000 pF One Output at a Time		7	20	

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

AC Test Conditions

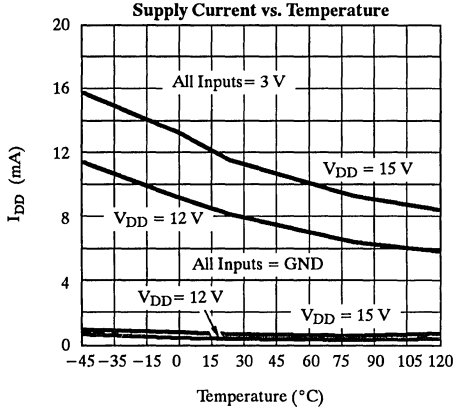


Note: Test repeated for inverting input.

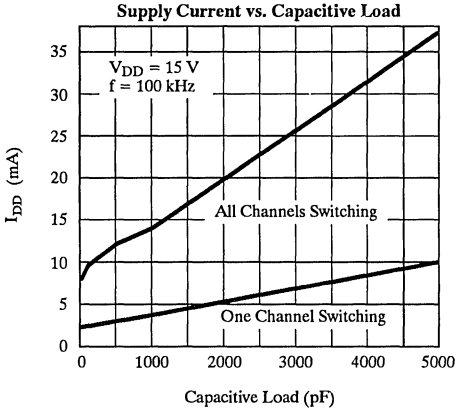
Figure 1. Switching Time Test Circuit

Typical Characteristics

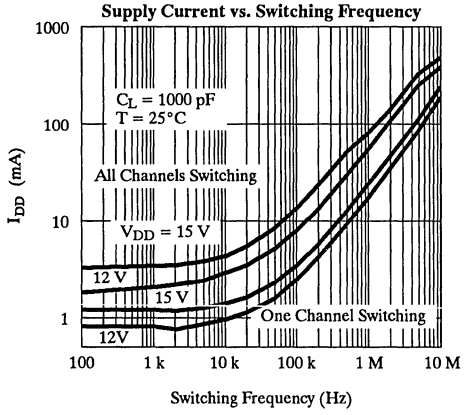
Supply Current vs. Temperature



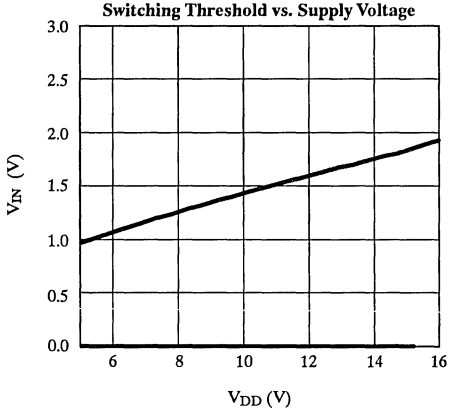
Supply Current vs. Capacitive Load



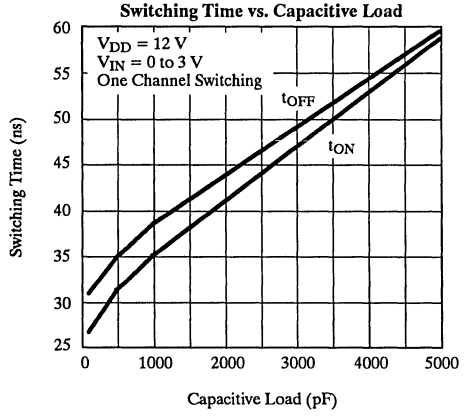
Supply Current vs. Switching Frequency



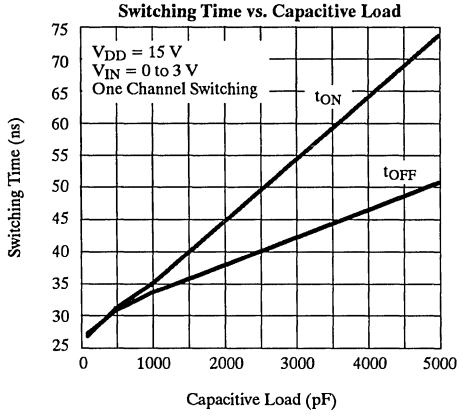
Switching Threshold vs. Supply Voltage



Switching Time vs. Capacitive Load



Switching Time vs. Capacitive Load



Siliconix

Si9910

Adaptive Power MOSFET Driver[1]

Features

- dv/dt and di/dt Control
- Undervoltage Protection
- Short-Circuit Protection
- t_{rr} Shoot-Through Current Limiting
- Low Quiescent Current
- CMOS Compatible Inputs
- Compatible with Wide Range of MOSFET Devices
- Bootstrap and Charge Pump Compatible (High-Side Drive)

Description

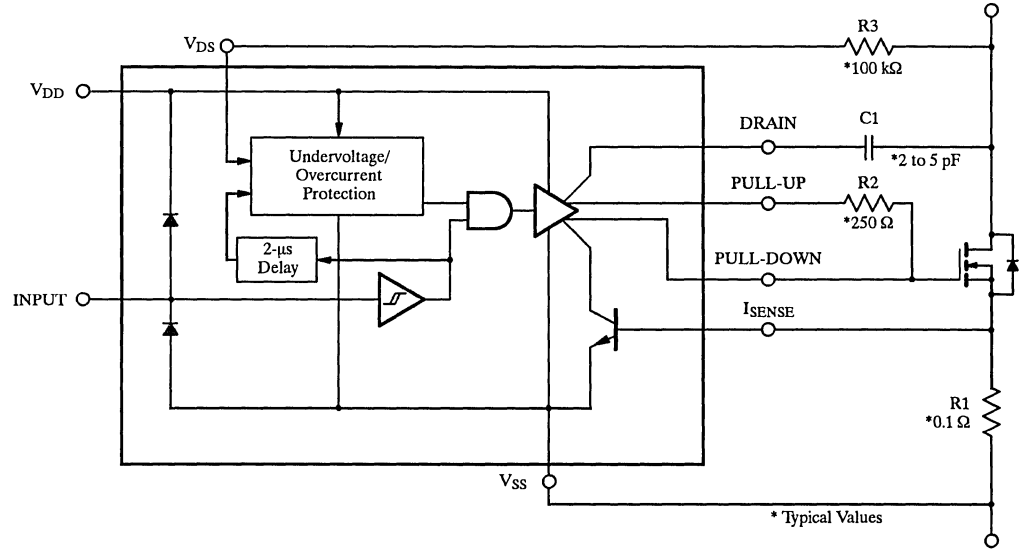
The Si9910 Power MOSFET driver provides optimized gate drive signals, protection circuitry and logic level interface. Very low quiescent current is provided by a CMOS buffer and a high-current emitter-follower output stage. This efficiency allows operation in high-voltage bridge applications with "bootstrap" or "charge-pump" floating power supply techniques.

The non-inverting output configuration minimizes current drain for an n-channel "on" state. The logic input is internally diode clamped to allow simple pull-down in high-side drives.

Fault protection circuitry senses an undervoltage or output short-circuit condition and disables the power MOSFET. Addition of one external resistor limits maximum di/dt of the external Power MOSFET. A fast feedback circuit may be used to limit shoot-through current during t_{rr} (diode reverse recovery time) in a bridge configuration.

The Si9910 is available in 8-pin plastic DIP and SOIC packages, and are specified over the industrial, D suffix (−40 to 85°C) temperature range.

Functional Block Diagram



1. Patent Number 484116.

Absolute Maximum Ratings

Voltages Referenced to V_{SS} Pin
V_{DD} Supply Range ..... −0.3 V to 18 V
Pin 1, 4, 5, 7, 8 ..... −0.3 V to V_{DD} + 0.3 V
Pin 2 ..... −0.7 V to V_{DD} + 0.3 V
Input Current ..... ±20 mA
Peak Current (I_{pk}) ..... 1 A
Storage Temperature ..... −65 to 150°C
Operating Temperature ..... −40 to 85°C

Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
8-Pin SOIC (Y Suffix)[b] ..... 700 mW
8-Pin Plastic DIP (J Suffix)[b] ..... 700 mW

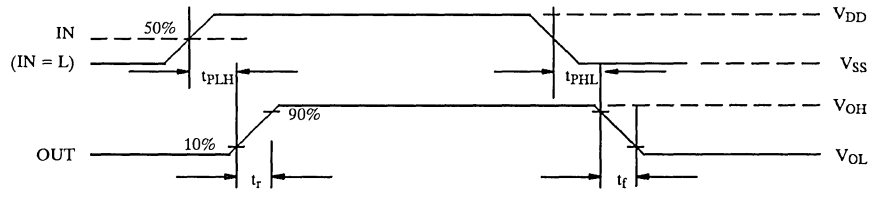
Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 5.6 mW/°C above 25°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} 10.8 V to 16.5 V T_A = Operating Temperature Range	Limits Min[c]	Limits Typ[b]	Limits Max[c]	Unit
Input						
High Level Input Voltage	V_{IH}		0.70 x V_{DD}	7.4		V
Low Level Input Voltage	V_{IL}			6.0	0.35 x V_{DD}	
Input Voltage Hysteresis	V_h		0.90	2.0	3.0	
High Level Input Current	I_{IH}	V_{IN} = V_{DD}			±1	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V			±1	
Output						
High Level Output Voltage	V_{OH}	I_{OH} = −200 mA	V_{DD} −3	10.7		V
Low Level Output Voltage	V_{OL}	I_{OL} = 200 mA		1.3	3	
Undervoltage Lockout	V_{UVLO}		8.3	9.2	10.6	
I_{SENSE} Pin Threshold	V_{TH}	Max I_S = 2 mA, Input High 100 mV Change on Drain	0.5	0.66	0 8	
Voltage Drain-Source Maximum	V_{DS}	Input High	8.3	9.1	10.2	
Input Current for V_{DS} Input	I_{VDS}			12	20.0	µA
Peak Output Source Current	I_{OS+}			1		A
Peak Output Sink Current	I_{OS-}			−1		
Supply						
Supply Range	V_{DD}		10.8		16.5	V
Supply Current	I_{DD1}	Output High, No Load		0.1	1	µA
	I_{DD2}	Output Low, No Load		100	500	
Dynamic						
Propagation Delay Time Low to High Level	t_{PLH}	C_L = 2000 pF		120		ns
Propagation Delay Time High to Low Level	t_{PHL}			135		
Rise Time	t_r			50		
Fall Time	t_f			35		
Overcurrent Sense Delay (V_{DS})	t_{DS}			1		µS
Input Capacitance	C_{in}			5		pF

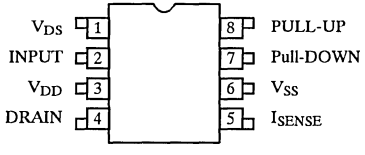
Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

AC Testing Conditions



Pin Configurations

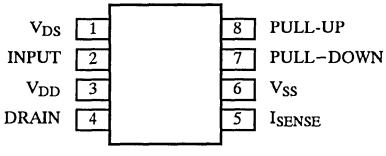
PDIP-8



Top View

Order Number:
SI9910DJ

SO-8



Top View

Order Number:
SI9910DY

Pin Description

Pin 1: V_{DS}

Pin 1 or V_{DS} is a sense input for the maximum source-drain voltage limit. Two microseconds after a high transition on input pin 2, an internal timer enables the $V_{DS(max)}$ sense circuitry. A catastrophic overcurrent condition, excessive on-resistance, or insufficient gate-drive voltage can be sensed by limiting the maximum voltage drop across the power MOSFET. An external resistor (R3) is required to protect pin 1 from overvoltage during the MOSFET "off" condition. Exceeding $V_{DS(max)}$ latches the Si9910 "off." Drive is re-enabled on the next positive- going input on pin 2. If pin 1 is not used, it must be connected to pin 6 (V_{SS}).

Pin 2: INPUT

A non-inverting, Schmidt trigger input controls the state of the MOSFET gate-drive outputs and enables the protection logic. When the input is low ($\leq V_{IL}$), V_{DD} is monitored for an undervoltage condition (insufficiently charged bootstrap capacitor). If an undervoltage ($\leq V_{DD(min)}$) condition exists, the driver will ignore a turn-on input signal. An undervoltage ($\leq V_{DD(min)}$) condition during an "on" state will not be sensed.

Pin 3: V_{DD}

V_{DD} supplies power for the driver's internal circuitry and charging current for the power MOSFET's gate capacitance. The Si9910 minimizes the internal I_{DD} in the "on" state (gate-drive outputs high) allowing a "floating" power supply to be provided by charge pump or bootstrap techniques.

Pin 4: DRAIN

Drain is an analog input to the internal dv/dt limiting circuitry. An external capacitor (C1) must be used to protect the input from exposure to the high-voltage ("off" state) drain and to set the power MOSFET's maximum rate of dv/dt. If dv/dt feedback is not used, pin 4 must be left open.

Pin Description (Cont'd)

Pin 5: I_{SENSE}

I_{SENSE} in combination with an external resistor (R_1) protects the power MOSFET from potentially catastrophic peak currents. I_{SENSE} is an analog feedback that limits current during the power MOSFET's transition to an "on" state. It is intended to protect power MOSFETs (in a half-bridge arrangement) from "shoot-through" current, resulting from excess di/dt and t_{rr} of flyback diodes or from logic timing overlap. An 0.8-V drop across (R1) should indicate a current level that is approximately four times the maximum allowable load current. When the I_{SENSE} input is not used, it should be tied to pin 6 (V_{SS}).

Pin 6: V_{SS}

V_{SS} is the driver's ground return pin. The applications diagram illustrates the connection of V_{SS} for source-referenced "floating" applications (half-bridge, high-side) and ground-referenced applications (half-bridge, low-side).

Pin 7: PULL-DOWN
Pin 8: PULL-UP

Pull-up and pull-down outputs collectively provide the power MOSFET gate with charging and discharging currents. Turn "on" or "off" di/dt can be limited by adding resistance (R_2) in series with the appropriate output.

Applications

"Floating" High-Side Drive Applications

As demonstrated in Figure 1, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 permit its use in half-bridge high-side drive applications.

A simple and inexpensive method of isolating a floating supply to power the Si9910 in high-side driver applications had to be provided. Therefore, the Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses and the charge pump circuit provides static operation.

The Si9910 is configured to take advantage of either floating supply technique if the application is not sensitive to their particular limitations, or both techniques if switching losses must be minimized and static operation is necessary. The schematic above illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

Input signal level shifting is accomplished with a passive pull-up (R4) and the Siliconix VN50300 (500-V/300-Ω) MOSFET for pull-down in applications below 500 V. Complete specifications for the VN50300 can be found in the Siliconix Low-Power Discretes Data Book. One of the VN50300's most important features in this application is its extremely low C_{oss} (output or drain) capacitance. C_{oss} (typically 5 pF), plus the Si9910's input capacitance (also typically 5 pF) plus any stray board capacitance. Total node capacitance defines the value of R4 needed to guarantee an input transition rate which safely exceeds the maximum dv/dt rate of the output half-bridge. Another feature of the VN50300 is its inherently low saturation current. Using level-shift devices with higher current capabilities may necessitate the addition of current-limiting components such as R5.

Bootstrap Undervoltage Lockout

When using a bootstrap capacitor as a high-side floating supply, care must be taken to ensure time is available to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As a catastrophic protection against abnormal conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate. For more details, please refer to Application Note AN705.

Applications (Cont'd)

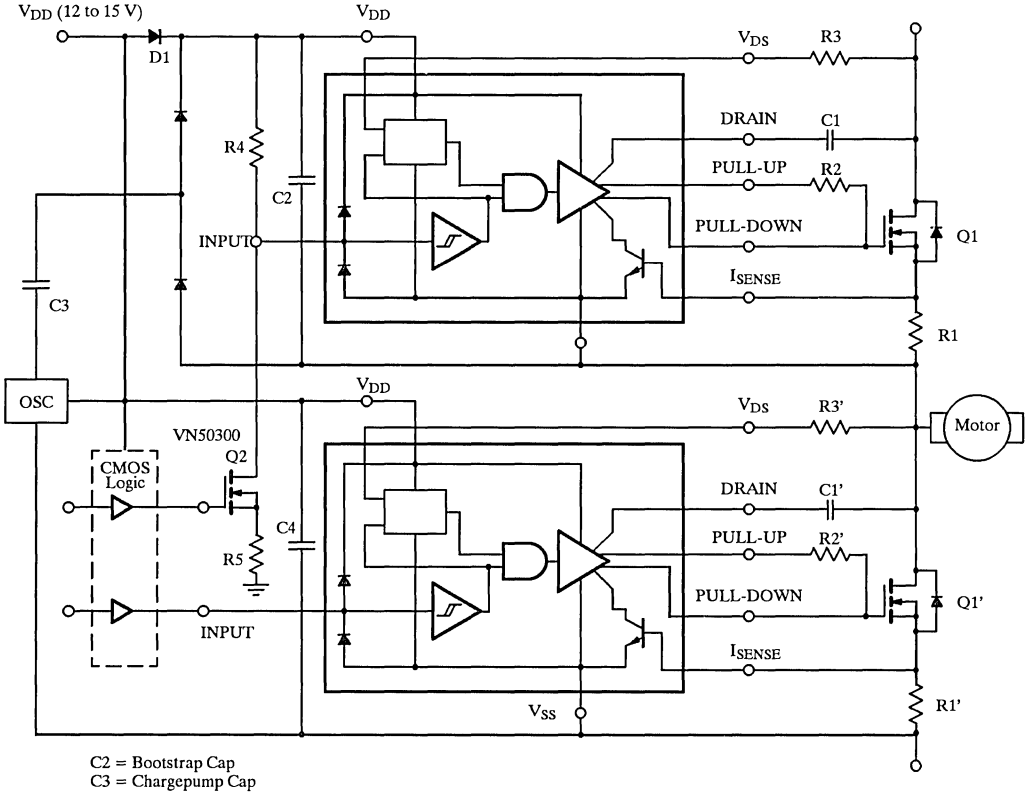


Figure 1. High-Voltage Half-Bridge with Si9910 Drivers

Si9961

12-V Voice Coil Motor Driver

Features

- 1.8-A H-Bridge Output
- Class B Linear Operation
- Externally Programmable Gain and Bandwidth
- Undervoltage Head Retract
- Programmable Retract Current
- Low Standby Current
- Rail-to-Rail Output Swing
- Single 12-V Supply
- System Voltage Monitor with Fault Output

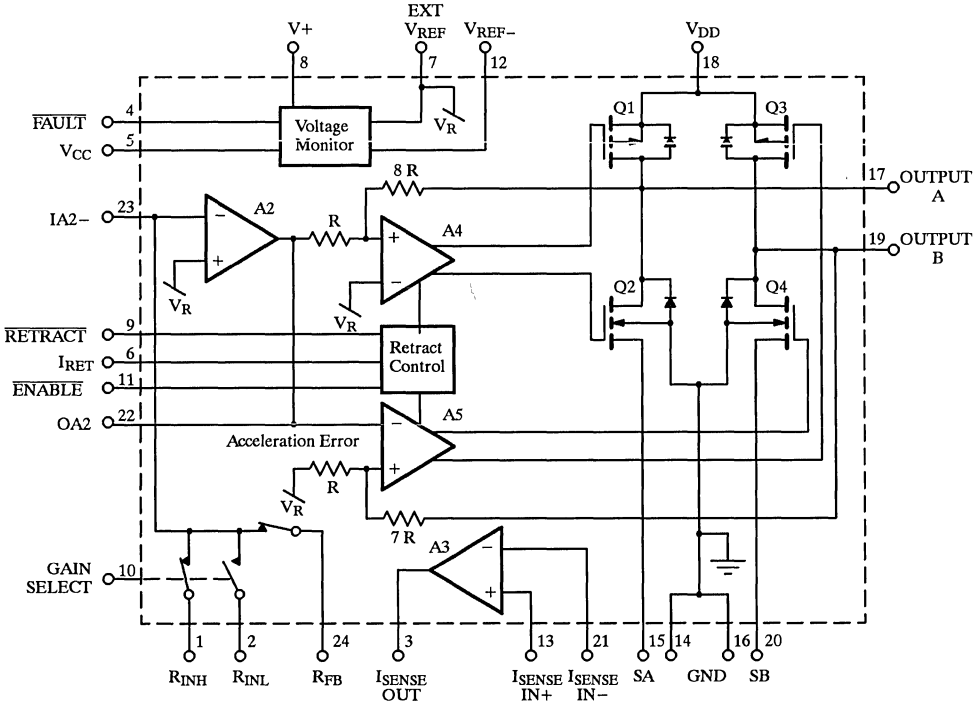
Description

The Si9961 is a linear actuator (voice coil motor) driver suitable for use in disk drive head positioning systems. The Si9961 contains all of the power and control circuitry necessary to drive the VCM that is typically found in 3½-inch hard disk drives and optical disk drives. The driver is capable of delivering 1.8 A at a nominal supply of 12 V.

The Si9961 provides all necessary functions including a motor current sense amplifier, a loop compensation amplifier and a power amplifier featuring four complementary MOSFETs in a H-bridge configuration. The output crossover protection ensures no cross-conducting current and true Class B operation during linear tracking. Externally programmable gain switch at the input summing junction increases the resolution and dynamic range for a given DAC. The head retract circuitry can be activated by either an undervoltage condition or an external command. An external resistor is required to set the VCM current during retract.

The Si9961 is constructed on a self-isolated BiC/DMOS power IC process. The IC is available in 24-pin SO package for operation over the commercial, C suffix (0 to 70°C) temperature range.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to Common Pin
V+ Supply Range ..... −0.3 V to 16 V
Pin ($\overline{FAULT}$) ..... −0.3 V to V_{CC} + 0.3 V
Pin (Output A & B, Source A & B) ..... −0.3 V to V_{DD} + 0.3 V
Pin (All Others) ..... −0.3 V to V+ + 0.3 V
Maximum Clamp Current
Output A, Output B (Pulsed 10 ms at 10% duty cycle) ..... ±1.8 A
Pin (All Others) ..... ±20 mA
Storage Temperature ..... −65 to 150°C

Operating Temperature ..... 0 to 70°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (Package)[a]
24-Pin SOIC[b] ..... 3.125 W
Thermal Impedance (Θ_{JA})[a]
24-Pin SOIC ..... 40°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 25 mW/°C above 25°C.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V ±10%, V_{DD} = 11.6 V ±10% V_{CC} = 5 V ±10%, V_{REF-} = GND = 0 V V_{REF} = 5 V ±5%	Limits C Suffix 0 to 70°C Min[b]	Typ[a]	Max[b]	Unit
Bridge Outputs (A_4, A_5)						
High Level Output Voltage	V_{OH}	I_{OH} = 1.0 A, V_{DD} = 10.2 V, OA_2= V_{REF} ±1 V	8.0	9.1		V
Low Level Output Voltage	V_{OL}	I_{OL} = −1.0 A, OA_2 = V_{REF} ±1 V		0.6	1.1	
Clamp Diode Voltage	V_{CL}	I_F = 1.0 A, $\overline{ENABLE}$ = High			2.5	
Amplifier Gain		Output V_{RANGE} = V_{REF} ±2 V	12	16	18	V/V
Dynamic Crossover Current		Measured at V_{DD}		10		mA
Slew Rate	SR		1			V/µS
Small Signal Bandwidth (−3 dB)				0.2		MHz
Input Deadband			−60		60	mV
A_2, Loop Compensation Amplifier						
Input Offset Voltage	V_{OS}		−8		8	mV
Input Bias Current	I_B	Gain Select = High, IA_2^- = 5 V	−50		50	nA
Unity Gain Bandwidth		R_{LOAD} = 10 kΩ C_{LOAD} = 100 pF to V_{REF}		1		MHz
Slew Rate	SR		1			V/µs
Power Supply Rejection Ratio	PSRR	@ 10 kHz		50		dB
Open Loop Voltage Gain	A_{VOL}			80		
Output Voltage Swing	V_O	R_{LOAD} = 10 kΩ to V_{REF}	V_{REF} −2		V_{REF} +2	V
A_3, Current Sense Amplifier						
Input Offset Voltage	V_{OS}		−5		5	mV
Input Impedance	R_{IN}	I_{SENSE}IN+ to I_{SENSE}IN−		5		kΩ
Small Signal Bandwidth (−3 dB)		R_{LOAD} = 10 kΩ C_{LOAD} = 100 pF to V_{REF}		1		MHz
Common Mode Rejection Ratio	CMRR	@ 5 kHz		50		dB
Slew Rate	SR		2			V/µs
Gain			3.9	4	4.1	V/V

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V ±10%, V_{DD} = 11.6 V ±10% V_{CC} = 5 V ±10%, V_{REF-} = GND = 0 V V_{REF} = 5 V ±5%	Limits C Suffix 0 to 70°C Min[b]	Typ[a]	Max[b]	Unit
A_3, Current Sense Amplifier (Cont'd)						
Input Common-Mode Voltage Range	V_{CM}	To GND	−0.3		2	V
Output Voltage Swing	V_O	R_{LOAD} = 10 kΩ, C_{LOAD} = 100 pF to V_{REF}	V_{REF} −2		V_{REF} +2	V
Supply						
Supply Current (Normal)	I_{CC}	Static, No Load $\overline{RETRACT}$ = High $\overline{ENABLE}$ = Low			0.01	mA
	I_{V+}			2	5	
	I_{DD}			5	13	
Supply Current (Standby)	I_{CC}	Static, No Load $\overline{RETRACT}$ = High $\overline{ENABLE}$ = High			0.01	mA
	I_{V+}			0.2	0.4	
	I_{DD}			0.8	1.6	
V_{DD} Range	V_{DD}	Normal Mode	10.2	11.6	13.2	V
		Retract Mode	2.0		14	
V_{CC} Range	V_{CC}		4.5	5	5.5	V
V+ Range	V+		10.8	12	13.2	V
Gain Select Switch						
R_{FB} Switch Resistance		IA2− = 5 V		108	240	Ω
R_{INH} Switch Resistance				135	300	Ω
R_{INL} Switch Resistance				810	1800	Ω
V_{REF} (EXT)						
Input Current	I_{REF}	OA2 = V_{REF}	0.15	0.40	0.65	mA
External Voltage Range	V_{REF}		4.75	5	5.25	V
Power Supply Monitor						
V_{CC} Undervoltage Threshold		V_{REF} = 5.0 V	3.82	4.12	4.42	V
Hysteresis				40		mV
V+ Undervoltage Threshold		V_{REF} = 5.0 V	9.1	9.8	10.6	V
Hysteresis				100		mV
Gain Select, $\overline{RETRACT}$, $\overline{ENABLE}$ Input						
Input High Voltage	V_{IH}		3.5			V
Input Low Voltage	V_{IL}				1.5	V
Input High Current	I_{IH}	V_{IN} = 5 V	−1		1	µA
Input Low Current	I_{IL}	V_{IN} = 0 V	−1		1	µA

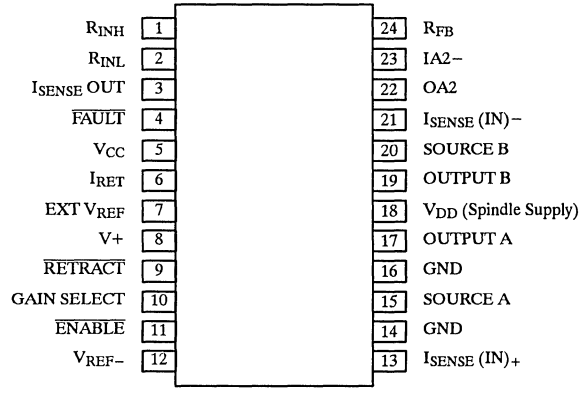
Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V ±10%, V_{DD} = 11.6 V ±10% V_{CC} = 5 V ±10%, V_{REF-} = GND = 0 V V_{REF} = 5 V ±5%	Limits C Suffix 0 to 70°C Min[b]	Typ[a]	Max[b]	Unit
$\overline{FAULT}$ Output						
Output High Voltage	V_{OH}	I_{OH} = −100 µA	V_{CC} −0.8	V_{CC} −0.33		V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.25	0.50	
Output High Sourcing Current	I_{OHS}	V_{OUT} = 0 V		400	1100	µA
RETRACT Current Control ($\overline{RETRACT}$ = Low, Output Current from A to B)						
I_{RET} Bias Voltage	$V(I_{RET})$	V_{DD} = 10 V, R_{RET} = 3.74 kΩ		0.66		V
Retract Output Pull-Up Voltage	$V_{OUT\,A}$	V_{DD} = 2 V to 14 V, I_{OUTA} = 30 mA	V_{DD} −1			
Retract Output Pull-Down Current	I_{OUTB}	V_{DD} = 10 V, V_{OUTB} = 5 V R_{RET} = 3.74 kΩ R_{SB} = 0.5 Ω, T_A = 25°C	22	30	38	mA
Maximum Emergency Retract Current	I_{OUTB} (Max)	V_{DD} = 2 V, V_{OUTB} = 0.7 V R_{RET} = < 10 Ω R_{SB} = 0.5 Ω	40			
Retract Current V_{DD} Supply Rejection Ratio		V_{DD} = 2 V to 14 V, R_{RET} = 3.74 kΩ		3.0		%/V
Retract Current Temperature Coefficient		V_{DD} = 10 V, R_{RET} = 3.74 kΩ		−0.3		%/°C

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

Pin Configurations

24-Pin SOIC



Top View

Order Number: Si9961ACY

Applications

Introduction

The Si9961 Voice Coil Motor (VCM) driver integrates the active feedback and drive components of a head-positioning servo loop for high-performance hard-disk applications. The Si9961 operates from a 12-V (±10%) power supply and delivers 1 A of steady-state output current. This device is made possible by a power IC process which combines bipolar, CMOS and complimentary DMOS technologies. CMOS logic and linear components minimize power consumption, bipolar front-ends on critical amplifiers provide necessary accuracy, and complimentary (p- and n-channel) DMOS devices allow the transconductance output amplifier to operate from ground to V_{DD}. Two user-programmable, current feedback/input voltage ratios may be digitally selected to optimize gain for both seek and track following modes, to maximize system accuracy for a given DAC resolution. An undervoltage lockout circuit monitors the V+ supply and generates a fault signal to trigger an orderly head-retract sequence at a voltage level sufficient to allow the spindle motor's back EMF-generated voltage to supply the necessary head parking energy. Head retract can also be commanded via a separate $\overline{\text{RETRACT}}$ input. VCM current during retract can be user programmed with a single external resistor. External components are limited to R/C filter components for loop compensation and the resistors that are required to program gain, retract current, and the load current sense.

User-Programmable Gains

During linear operation, the transconductance amplifiers' gains (input voltage at V_{IN} vs. VCM current, in Figure 1) are set by external resistors $R_3 \rightarrow R_5$, R_{SA}, and R_{SB} and selected by gain input. After selecting a value for R_{SA} and R_{SB} that will yield the desired VCM current level, the High and Low feedback gain ratios may be determined by the following:

$$\text{High Gain} = \left(\frac{R_5}{R_3}\right)\frac{1}{4\,R_S} \quad \text{(GAIN SELECT Input = High)}$$

$$\text{Low Gain} = \left(\frac{R_5}{R_4}\right)\frac{1}{4\,R_S} \quad \text{(GAIN SELECT Input = Low)}$$

Where $R_S = R_{SA} = R_{SB}$
Input offset current may then be calculated as:

$$I_{OS} = \frac{1}{4\,R_S}\left(\left(\frac{(R_S + R_{IN})}{R_{IN}}\right)V_{OSA2} + 5\,V_{IAS3}\right)$$

Where $R_{IN} = R_3$ or R_4

Head Retract

A low on the $\overline{\text{RETRACT}}$ input pin turns output devices Q1 and Q4 on, and output devices Q2 and Q3 off. Maximum VCM current can be set during head retract by adding an external resistor between the IRET pin and ground. Maximum retract current may be calculated as:

$$I_{OUT} = 175 \times I_{ret} = 175 \times \frac{0.66\ V}{R_{ret}}$$

Head retract can be initiated automatically by an undervoltage condition (either the 12-V or 5-V supplies on the Si9961) by connecting the $\overline{\text{FAULT}}$ output to the $\overline{\text{RETRACT}}$ input.

A high $\overline{\text{ENABLE}}$ input puts both driver outputs in a high-impedance state. The $\overline{\text{ENABLE}}$ function can be used to eliminate quiescent output current when power is applied but the head has been parked, such as a sleep mode. A sleep-mode power down sequence should be preceded by a retract signal since a power failure during this state may not provide adequate spindle-motor back EMF to permit head retraction.

SERVO Loop Characterization

As a test vehicle, the circuit in Figure 2 was constructed, compensated, and characterized. The VCM chosen to serve as the load was characterized using an HP4192A Impedance Analyzer as follows: 2.7 mH @ f = 1 kHz/ 1.5 mH @ f = 10 kHz (L_m), and 54.9 Ω f = 1 kHz/90.4 Ω @ f = 10 kHz (R_m).

To compensate the system for a closed-loop bandwidth of 10 kHz:

$$C_L = \frac{64}{2\pi\,R_5 BW}\left(\frac{R_{SA}}{R_m + R_{SA}}\right) = 540\ \text{pF (Used 560 pF)}$$

$$R_L = \frac{LM}{CL\,(R_m + R_{SA})} = 29.5\ \text{k}\Omega\ \text{(Used 28.7 k}\Omega\text{)}$$

The Bode plot of the Si9961 closed-loop ac response is shown in Figure 3. The test equipment used to generate the data were the HP3330B Automatic Synthesizer and the HP3570A Network Analyzer. The −3-dB breakpoint is slightly below 10 kHz. Maximum peaking is approximately 0.22 dB at 2 kHz. Over a typical servo-system mechanical bandwidth range of 100−500 Hz the maximum phase shift is 1.5 degrees. The 20 dB/decade roll off is smooth from 10 kHz to 100 kHz.

Applications (Cont'd)

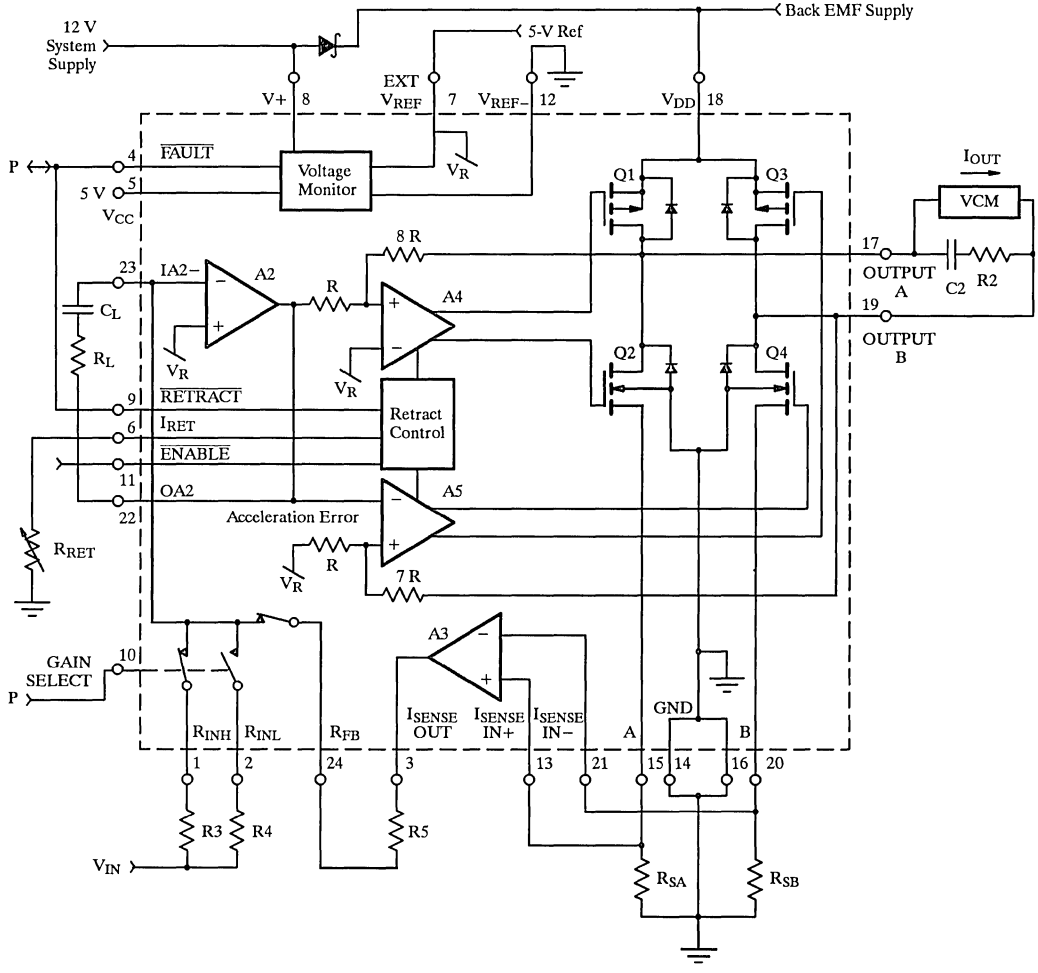


Figure 1. Si9961 Typical Application

The motor's transient response to a 500-mV (V_{REF} ±250 mV) input step is shown in Figure 4 (trace 1). Figure 4, trace 2 shows the output voltage of buffer amplifier A3, which represents the differential output current. Output current peaking is less than 12% of the total step amplitude and settling time is less than 250 µS.

The linearity of the transconductance amplifier (around a center value of 500 mA/volt) is shown in Figure 5. In this case, the output current sense resistors (R_{SA} and R_{SB}) were ±5% tolerance, 0.5 Ω. Any mismatch between R_{SA} and R_{SB} contribute directly to mismatch between the positive and negative "full-scale". Including the external resistor mismatch, the overall loop nonlinearity is approximately 1% maximum over a ±250-mV input voltage range.

Applications (Cont'd)

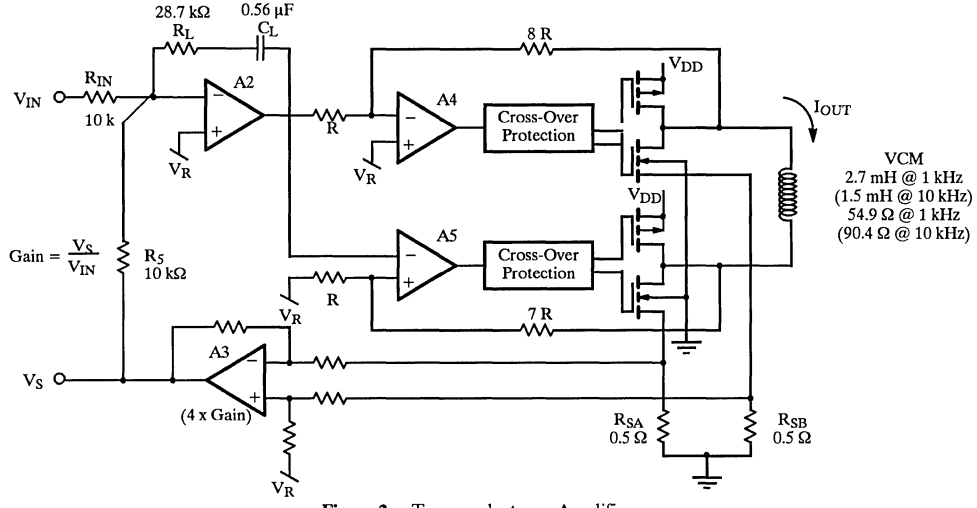


Figure 2. Transconductance Amplifier

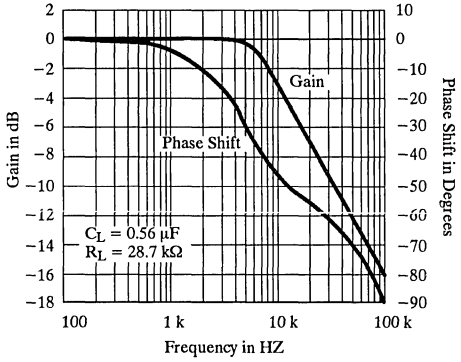


Figure 3. Bode Plot of Si9961 Current Gain

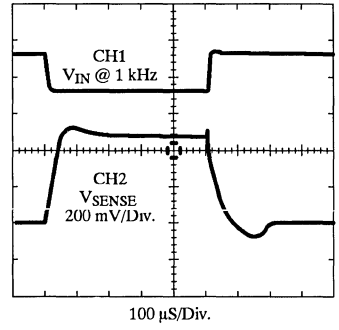


Figure 4. Motor Transient Response

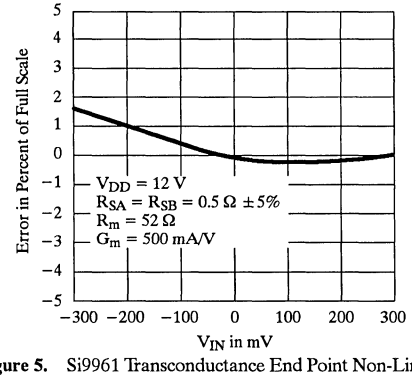


Figure 5. Si9961 Transconductance End Point Non-Linearity

Siliconix

Si9976DY

N-Channel Half-Bridge Driver

Features

- Single Input for High-Side and Low-Side MOSFETs
- 20- to 40-V Supply
- Static (dc) Operation
- Cross-Conduction Protected
- Undervoltage Lockout
- ESD and Short Circuit Protected
- Fault Feedback

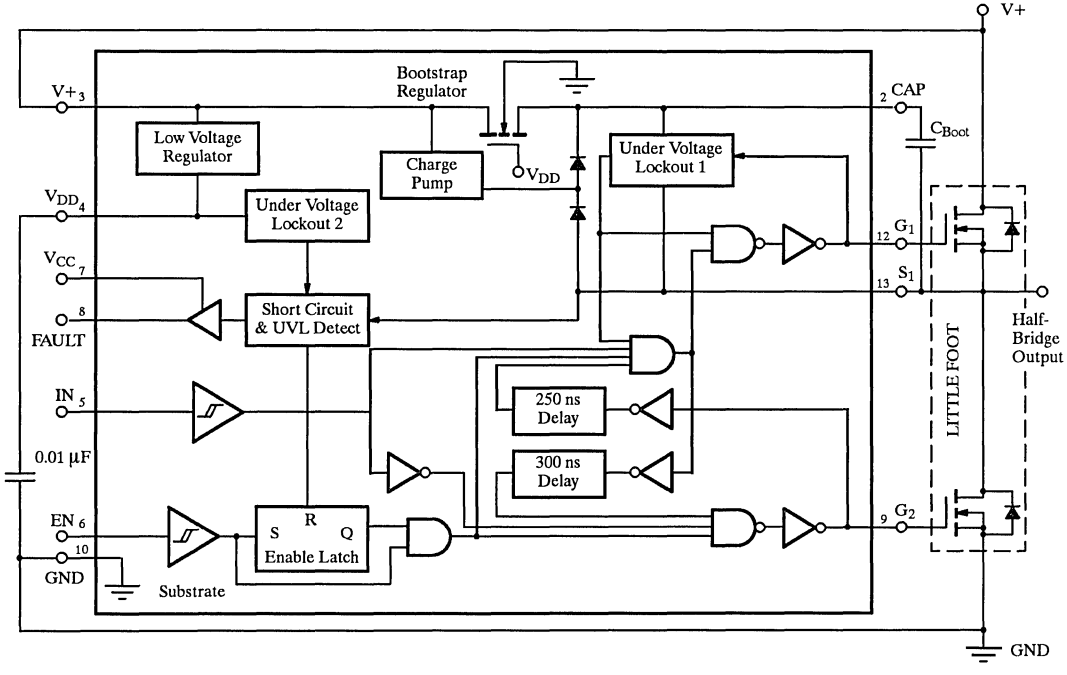
Applications

- Power Supplies
- Motor Drives
- Office Automation
- Computer Peripherals
- Industrial Controllers
- Robotics
- Medical Equipment

Description

The Si9976DY is an integrated driver for an n-channel MOSFET half-bridge. Schmitt trigger inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply of 20 to 40 volts. Both half-bridge n-channel gates are driven directly with low-impedance outputs. Addition of one external capacitor allows an internal circuit to level shift both the power supply and logic signal for the half-bridge high-side n-channel gate drive. An internal charge pump replaces leakage current lost in the high-side driver circuit to provide "static" (dc) operation in any output condition. Protection features include an undervoltage lockout, cross-conduction prevention logic, and a short circuit monitor. The Si9976DY is available in the 14-pin SOIC (surface mount) package, specified to operate over the industrial (−40 to 85°C) temperature range.

Functional Block Diagram



Absolute Maximum Ratings

Voltage on IN, EN (pins 5, 6) with respect to ground ..... −0.3 to V_{DD} +0.3 V
Voltage on V_{CC} (pin 7) ..... −0.3 to +18 V
Voltage on V+, S1 (pins 3, 13) ..... −0.3 to +50 V
Voltage on CAP, G1[a] (pins 2, 12) ..... −0.3 to +60 V
Peak Output Current ..... 0.5 A
Operating Temperature (T_A) ..... −40 to 85°C
Storage Temperature ..... −50 to 150°C

Maximum Junction Temperature (T_J) ..... 125°C
Power Dissipation[b] ..... 1 W
Θ_{JA} ..... 100°C/W[b]

Notes
a. Internally generated voltage for reference only.
b. Derate 10 mW/°C above 25°C.
c. PC board mounted with no forced air flow.

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified V+ = 20 to 40 V T_A = Operating Temperature Range	Limits D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Input						
Input Voltage High (EN and IN)	V_{INH}		4.0			V
Input Voltage Low (EN and IN)	V_{INL}				1.0	
Input Hysteresis Voltage	V_H			0.5		
Input Current—Input Voltage High	I_{INH}	(EN and IN) V_{IN} = 15 V			1	µA
Input Current—Input Voltage Low	I_{INL}	(EN and IN) V_{IN} = 0 V	−1			
Output						
Output Voltage High, G1[d]	V_{OUTH}	S1 = V+, I_{OUT} = −10 mA	10	12		V
Output Voltage High, G2[e]		S1 = GND, I_{OUT} = −10 mA	12	15		
Output Voltage Low, G1 and G2	V_{OUTL}	S1 = GND, I_{OUT} = 60 mA		1.2	3	
Fault Output Voltage High	V_{OH}	V_{CC} = 4.5 V, I_{OUT} = −0.2 mA	3.5	4		
Fault Output Voltage Low	V_{OL}	V_{CC} = 4.5 V, I_{OUT} = 0.6 mA		0.3	1.0	
Undervoltage Lockout 1	UVL1			11		
Undervoltage Lockout 2	UVL2			14		
Capacitor Current	I_{CAP}	S1 = GND, V_{CAP} = 0 V			−10	mA
		S1 = GND, V_{CAP} = 9 V			−2	
Supply						
V+ Supply Range			20		40	V
V+ Supply Current	I+ (H)	G2 High, No Load		1.7	3.5	mA
	I+ (L)	G2 Low, No Load, S1 = GND		2	4.5	
V_{CC} Supply Range			4.5		16.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 16.5 V			10	µA
V_{DD} Supply Voltage[f]	V_{DD}		15	16	17.5	V

Specifications[a]

Parameter	Symbol	Test Conditions UnlessOtherwise Specified V+ = 20 to 40 V T_A = Operating Temperature Range		Limits D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Dynamic							
Propogation Delay Time Low to High Level	t_{PLH}	50% IN to V_{OUT} = 5 V, C_L = 600 pF	G1		350		ns
			G2		400		
Propogation Delay Time High to Low Level	t_{PHL}		G1		150		
			G2		50		
Propogation Delay Time, Low to High Level, Enable-to-Fault Output		50% IN to FAULT = 2 V, S1 shorted to GND or V+			500		
Output Rise Time (G1, G2)	t_r	1 to 10 V, C_L = 600 pf			110		
Output Fall Time (G1, G2)	t_f	10 to 1 V, C_L = 600 pf			50		
Short Circuit Pulse Width	t_{SC}	50% to 50% of V_{OUT}			350		

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
d. To supply the output current of 10 mA on a dc basis, an external 13-V supply must be connected between the CAP pin and the S1 pin with the negative terminal of the supply connected to S1. This is not needed in an actual application because output currents are supplied by the C_{BOOT} capacitor. Voltage specified with respect to V+.
e. For testing purposes, the 10-mA load current must be supplied by an external current source to the V_{DD} pin to avoid pulling down the V_{DD} supply.
f. Internally generated voltage for reference only.

Truth Table

EN	IN	Condition	FAULT OUTPUT	G1 OUT	G2 OUT
1	0	Normal Operation	0	Low	High
1	1	Normal Operation	0	High	Low
0	X	Disabled	X[a]	Low	Low
1	0	Load Shorted to V+	1[b]	Low	Low
1	1	Load Shorted to Ground	1[b]	Low	Low
1	1	Undervoltage on C_{BOOT}	0	Low	Low
1	0	Undervoltage on C_{BOOT}	0	Low	High
X	X	Undervoltage on V_{DD}[c]	1	Low	Low

Notes
a. FAULT output retains previous state until ENABLE rising edge.
b. Latch FAULT condition, reset by ENABLE rising edge.
c. V_{DD} is an internally generated low-voltage supply.

Pin Description

Pin 1

No connection.

Pin 2: CAP

Connection for the positive terminal of the bootstrap capacitor C_{BOOT}. A 0.01-µF C_{BOOT} capacitor can be used for most applications.

Pin 3: V+

This is the only external power supply required for the Si9976DY, and must be the same supply used to power the half-bridge it is driving. The Si9976DY powers it's low-voltage logic, low-side gate driver, and bootstrap/charge pump circuits from self-contained voltage regulators which require only a bootstrap capacitor on the CAP pin and a bypass capacitor on the V_{DD} pin.

No voltage sensing circuitry monitors V+ directly; however, the low-voltage, internally generated V_{DD} supply and the bootstrap voltage (which are derived from V+) are directly protected by undervoltage monitors.

Pin 4: V_{DD}

Connection to the internally generated low-voltage supply which must be bypassed to ground with a 0.01-µF capacitor.

Pin 5: IN

Logic input. A low level input turns off the high-side half-bridge MOSFET and, after an internally set dead time, turns the low-side half-bridge MOSFET on. A high input level has the opposite effect. The input is compatible with 5-, 12- or 15-V logic outputs.

Pin 6: EN

Enable input. A low EN input level prevents turn on of either half-bridge MOSFET. If the Si9976DY is internally disabled as a result of an output short-circuit condition, a low-to-high transition on EN is required to clear the fault and resume operation. The input logic levels are the same as IN.

Pin 7: V_{CC}

If the FAULT output is used, the V_{CC} pin must be connected to the logic supply voltage in order to set the high level of the FAULT output. If the FAULT output is not used, this pin may be left open with no effect on internal fault sensing or protection circuitry.

Pin 8: FAULT

The Fault output is latched high when a short-circuit output condition is detected. FAULT will return low when the circuit is reset using the EN pin. The FAULT output also indicates the status of the undervoltage sense circuit on V_{DD}, however the fault condition is cleared automatically when the undervoltage condition clears.

Pin 9: G2

This pin drives the gate of the external low-side power transistor.

Pin 10: GND

The ground return for V+, logic reference, and connection for source of external low-side power transistor.

Pin 11

No connection.

Pin 12: G1

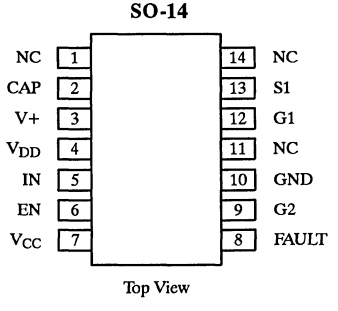
This pin drives the gate of the external high side power transistor.

Pin 13: S1

Connection for the source of the external high-side power transistor, the drain of the external low-side power transistor, the negative terminal of the bootstrap capacitor, and the system load. The voltage on this pin is sensed by the circuitry that monitors the load for shorts.

Pin 14

No connection.



Detailed Description

Power On Conditioning

Bootstrap-type floating supplies require that the bootstrap capacitor be charged at power on. In the case of the Si9976DY, this is accomplished by pulsing the IN line low with the EN line held high, thus turning on the low-side MOSFET and providing the charging path for the capacitor.

Operating Voltage: 20 to 40 V

The Si9976DY is intended to be powered by a single power supply within the range of 20 to 40 V and is designed to drive a totem pole pair of NMOS power transistors such as those within the Si9955. The power transistors must be powered by the same power supply as this driver. In addition to the high-voltage power supply (20 to 40 V), the Si9976DY must have a power supply connected to the V_{CC} terminal, if a fault output signal is desired. This power supply provides operating voltage for the fault output and allows the high output voltage level to be compatible with system logic that monitors the fault condition. The value of this power supply must be within the range of 4.5 to 16.5 V to ensure functionality of the output. Internal fault circuitry, which is used for shorted-load protection, is not affected by this power supply.

Cross-Conduction Protection

The high-side power transistor can only be turned on after a fixed time delay following the return to ground of the low-side power transistor's gate. The low-side transistor can only be turned on after a fixed time delay following the high-side transistor turn-off signal.

Undervoltage Lockout

During power up, both power transistors are held off until the internal regulated power supply, V_{DD}, is approximately one V_{be} from the final value, nominally 16 V. After power up, the undervoltage lockout circuitry continues to monitor V_{DD}. If an undervoltage condition occurs, both the high-side and low-side transistors will be turned off and the fault output will be set high. When the undervoltage condition no longer exists, normal function will resume automatically. Separate voltage sensing of the bootstrap capacitor voltage allows a turn-on signal to be sent to the high-side drive circuit if either the bootstrap capacitor has full voltage, or the load voltage is high (driven high by an inductive load or shorted high). The voltage sensing circuit will allow the high-side power transistor to turn on if an on signal is present and the voltage on the bootstrap capacitor rises from undervoltage to operating voltage.

Short Circuit Protection

This device is intended to be used only in a half-bridge which drives inductive loads. A shorted load is presumed if the load voltage does not make the intended transition within an allotted time. Separate timing is provided for the two transitions. A longer time is allowed for the high-side to turn on (300 ns vs. 200 ns) since the propagation delays are longer. Excessive capacitive loading can be interpreted as a short. The value of capacitance that is needed to produce the indication of a short depends on the load driving capability of the power transistors.

ESD Protection

Electrostatic discharge protection devices are between V_{DD} and GND, V_{CC} and GND, and from terminals IN, EN, G2, and FAULT to both V_{DD} and GND. V+, CAP, S1, and G1 are not ESD protected.

Fault Feedback

Detection of a shorted load sets a latch which turns off both the high-side and the low-side power transistors. If V_{CC} is present, a one level will be present on the FAULT output. To reset the system, the enable input, EN, must be lowered to a logic zero and then raised to a logic one. The logic level of the input, IN, will determine which power transistor will be turned on first after reset. An undervoltage condition on V_{DD} is not latched, but causes a one level on the FAULT output, if V_{CC} is present.

Static (dc) Operation

All components of a charge pump, except the holding (bootstrap) capacitor, are included in the circuit. This charge pump will provide current that is sufficient to overcome any leakage currents which would reduce the enhancement voltage of the high-side power transistor while it is on. This allows the high-side power transistor to be on continuously. When the low-side power transistor is turned on, additional charge is restored to the bootstrap capacitor, if needed. The maximum switching speed of the system at 50% duty cycle is limited by the on time of the low-side power transistor. During this time, the bootstrap capacitor charge must be restored. However, if the duty cycle is skewed so that the on time of the high-side power transistor is long enough for the charge pump to completely restore the charge lost during switching, then the on time of the low-side power transistor is not restricted.

Si9978DW

Siliconix

Configurable H-Bridge Driver

Features

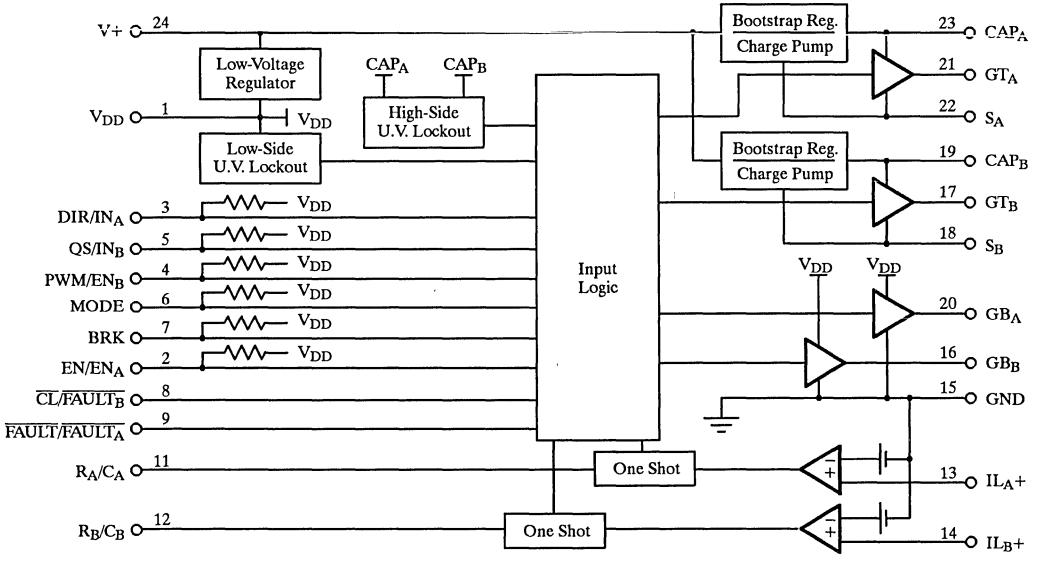
- H-Bridge or Dual Half-Bridge Operation
- 20- to 40-V Supply
- Static (dc) Operation
- Cross-Conduction Protected
- Current Limit
- Undervoltage Lockout
- ESD Protected
- Fault Output

Description

The Si9978DW is an integrated driver for an n-channel MOSFET H-bridge. The mode control allows operation as either a full H-bridge driver or as two independent half-bridges. The DIR/PWM input configuration allows easy implementation of either sign/magnitude or anti-phase PWM drive schemes for full H-bridges. Schmitt triggers on the inputs provide logic signal compatibility and hysteresis for increased noise immunity. An internal low-voltage regulator allows the device to be powered directly from a system supply of 20 to 40 volts. All n-channel gates are driven directly from low-impedance outputs. The addition of one external capacitor per half-bridge allows internal circuitry to level shift both the power supply and logic signal for the high-side n-channel gate drives. Internal charge pumps replace leakage current lost in the high-side driver circuits to provide "static" (dc) operation in any output condition. Protection features include an undervoltage lockout, cross-conduction prevention logic, and overcurrent monitors.

The Si9978DW is available in the 24-pin wide-body SOIC (surface mount) package, specified to operate over the industrial (−40 to +85°C) temperature range.

Functional Block Diagram



Advance Information

P-34668—Rev. A (03/23/94)

Absolute Maximum Ratings

Voltage on pins 2–7 with respect to ground ..... −0.3 to 16.5 V
Voltage on pin 24 ..... −0.3 to 50 V
Voltage on pins 17, 19, 21, 23 ..... −0.3 to +60 V
Voltage on pins 18, 22 ..... −2 to 50 V

Operating Temperature (T_A) ..... −40 to +85°C
Storage Temperature ..... −50 to 150°C
Maximum Junction Temperature (T_J) ..... 150°C
Power Dissipation ..... TBD

Recommended Operating Range

V+ ..... +20 to 40 V_{DC}
R_A, R_B ..... 100 kΩ

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V, T_A = −40 to +85°C	Limits Min[a]	Typ[b]	Max[a]	Unit
Power						
Supply Voltage Range	V+		20		40	V
Logic Voltage	V_{DD}		14.5	16	17.5	
Supply Current	I+	I_{DD} = 0 mA		4		mA
Inputs (DIR, PWM, EN, QS, MODE, BRK)						
High-State	V_{IH}		4.0			V
Low-State	V_{IL}				1.0	
High-State Input Current	I_{IH}	V_{IH} = V_{DD}			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V		−50		
Outputs						
Low-Side Gate Drive, High State	V_{GBH}		14	16	17.5	V
Low-Side Gate Drive, Low State	V_{GBL}				1	
High-Side Gate Drive, High State	V_{GTH}		14	16	18	
High-Side Gate Drive, Low State	V_{GTL}				1	
Low-Side Switching, Rise Time	t_{rL}	Rise Time = 1 to 10 V Fall Time = 10 to 1 V C_L = 600 pF		110		ns
Low-Side Switching, Fall Time	t_{fL}			50		
High-Side Switching, Rise Time	t_{rH}			110		
High-Side Switching, Fall Time	t_{fH}			50		
Break-Before-Make Time				250		
$\overline{FAULT}$, $\overline{CL}$	V_{OL}	I_{OL} = 1 mA			0.4	V
Protection						
Low-Side Undervoltage Lockout	UVLL			12.2		V
Low-Side Hysteresis	V_H			0.8		
High-Side Undervoltage Lockout	UVLH	$S_{A, B}$ = 0 V		V_{DD}−3.3 V		
Current Limit						
Comparator Input Bias Current	I_{IB}		−5			µA
Comparator Threshold Voltage	V_{TH}		90	100	110	mV
One Shot Pulse Width	t_p	R_A, R_B = 100 k, C_A, C_B = 100 pF	8	10	12	µs
		R_A, R_B = 100 k, C_A, C_B = 0.001 µF	80	100	120	
Propagation Delay	t_{pd}	C_L = 600 pF		600		ns

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Guaranteed by design, not subject to production test.

Truth Table

H-Bridge Mode

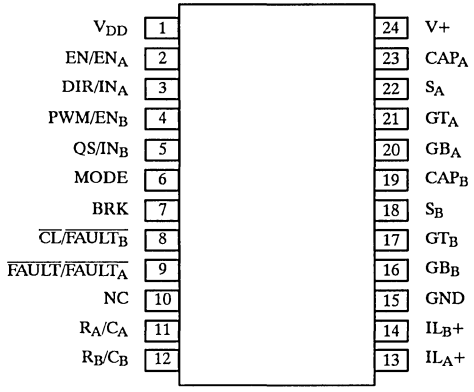
MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{CL}$/ $\overline{FAULT_B}$	$\overline{FAULT}$/ $\overline{FAULT_A}$	Condition
1	1	1	1	⎍	0	L	X	H	L	L	⎍	1	1	Normal Operation
1	1	1	0	⎍	0	L	X	⎍	L	L	⎍	1	1	
1	0	1	1	⎍	0	L	X	L	⎍	H	L	1	1	
1	0	1	0	⎍	0	L	X	L	⎍	⎍	L	1	1	
1	X	1	X	X	1	L	X	L	H	L	H	1	1	Brake
1	X	0	X	X	X	L	X	L	L	L	L	1	1	Disable
1	X	1	X	X	0	⎍	X	L	L	L	L	⎍	⎍	Overcurrent
1	X	X	X	X	X	X	X	L	L	L	L	1	0	Undervoltage on V_{DD}

Half-Bridge Mode

MODE	DIR/ IN_A	EN/ EN_A	QS/ IN_B	PWM/ EN_B	BRK	IL_A+	IL_B+	GT_A	GB_A	GT_B	GB_B	$\overline{CL}$/ $\overline{FAULT_B}$	$\overline{FAULT}$/ $\overline{FAULT_A}$	Condition
0	1	1	X	0	X	L	L	H	L	L	L	1	1	Normal Operation
0	0	1	X	0	X	L	L	L	H	L	L	1	1	
0	X	0	1	1	X	L	L	L	L	H	L	1	1	
0	X	0	0	1	X	L	L	L	L	L	H	1	1	
0	X	1	X	X	X	⎍	X	L	L	X	X	1	⎍	Overcurrent on A
0	X	X	X	1	X	X	⎍	X	X	L	L	⎍	1	Overcurrent on B
0	X	X	X	X	X	X	X	L	L	L	L	0	0	Undervoltage on V_{DD}

Pin Configuration

SO-24
(Wide Body)



Top View

Pin Description

Pin 1: V_{DD}

V_{DD} is an internally generated voltage. It is connected to this pin to allow connection of a decoupling capacitor.

Pin 2: EN/EN_A

The EN input allows normal operation when at logic "1", and turns all gate drive outputs off when at logic "0". When the mode pin is at logic "1", EN controls the entire H-bridge. When the mode pin is at logic "0", this pin becomes the ENABLE pin for half-bridge A.

Pin 3: DIR/IN_A

The function of this pin is determined by the MODE pin. When the MODE pin is at logic "1", it is the DIR pin, and when MODE is at logic "0", it is the IN_A pin.

As the DIR input, it is the direction control for the H-bridge, and determines which diagonal pair of power MOSFETs is active. A logic "1" turns on GT_A and enables GB_B, while a logic "0" turns on GT_B and enables GB_A. When implementing an anti-phase PWM control, the DIR input serves as the PWM input.

As the IN_A pin, it is the input that controls the "A" half-bridge. When at logic "1", the high-side MOSFET is turned on, and when at logic "0", the low-side MOSFET is turned on.

Pin 4: PWM/EN_B

With the mode pin at logic "1", this pin is the PWM input. It controls the switching of the active diagonal pair. A logic "1" turns the active MOSFETs on, while a logic "0" turns it off. The QS input determines whether the bottom or both bottom and top MOSFETs are switched. When implementing an anti-phase PWM control, the PWM input is connected to a logic "1". When the mode pin is at logic "0", this pin becomes the ENABLE pin for half-bridge B.

Pin 5: QS/IN_B

With the mode pin at logic "1", this input determines whether the bottom MOSFETs of the H-bridge or both bottom and top MOSFETs switch in response to the PWM signal. A logic "1" on this input enables only the bottom MOSFETs. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, both the bottom and top MOSFETs are enabled.

This input controls the B half-bridge when the MODE pin is at logic "0". When at logic "1", the high-side MOSFET is turned on, and when at logic "0", the low-side MOSFET is turned on.

Pin 6: MODE

This input determines whether the Si9978 functions as an H-bridge or as two independent half-bridges. When the MODE pin is at logic "1", the Si9978 functions as an H-bridge, and when MODE is at logic "0", it functions as two independent half-bridges.

Pin Description (Cont'd)

Pin 7: BRK

When this input is at logic "1", both bottom gate drives are switched high, turning on the bottom MOSFETs. When this input is at logic "0", the Si9978 operates normally.

Pin 8: $\overline{CL/FAULT_B}$

This is an open drain output which is active low. When the MODE pin is at logic "1", this pin functions as $\overline{CL}$ and indicates that the H-bridge is in current limit. It stays low for the duration of the current limit one-shot. With the MODE pin at logic "0", it serves as the $\overline{FAULT}$ output for half-bridge B to indicate when an undervoltage or overcurrent condition is detected. When indicating an overcurrent condition, the output stays low for the duration of the current limit one-shot. The $\overline{FAULT}$ output resets automatically when the condition clears.

Pin 9: $\overline{FAULT/FAULT_A}$

This is an open drain output which is switched low when an undervoltage or overcurrent condition is detected. When indicating an overcurrent condition, the output stays low for the duration of the current limit one-shot. When the MODE pin is at logic "1", this pin is the H-bridge $\overline{FAULT}$ output. With the MODE pin at logic "0", it serves as the $\overline{FAULT}$ output for half-bridge A. The $\overline{FAULT}$ output resets automatically when the condition clears.

Pin 10: NC

Pin 11: R_A/C_A

The timing resistor and capacitor for the current limit one-shot are connected to this pin. The values of the resistor and capacitor determine the off time set by the one-shot. The one-shot is triggered when the current limit comparator detects an overcurrent condition.

Pin 12: R_B/C_B

The timing resistor and capacitor for the current limit one-shot are connected to this pin. The values of the resistor and capacitor determine the off time set by the one-shot. The one-shot is triggered when the current limit comparator detects an overcurrent condition.

Pin 13: IL_A+ and Pin 14, IL_B+

These are the overcurrent sense inputs. Internally, they are connected to the noninverting inputs of the current limit comparators. Externally they are connected to the source(s) of the low-side MOSFET(s) and the current sense resistor.

Pin 15: GND

The GND pin is the ground return for V+ and the ground reference for the logic. Also, this is the ground reference input for the current limit comparators and is connected to the ground side of the internal 100-mV references. This pin should be connected directly to the ground side of the current sensing resistors.

Pin 16: GB_B and Pin 20, GB_A

These pins drive the gates of the low-side power MOSFETs.

Pin 17: GT_B and Pin 21, GT_A

These pins drive the gates of the high-side power MOSFETs.

Pin 18: S_B and Pin 22, S_A

These are the source connections of the high-side power MOSFETs, the drain of the external low-side power MOSFET, the negative terminal of the bootstrap capacitor, and the output for each half-bridge.

Pin 19: CAP_B and Pin 23, CAP_A

These are the connections for the positive terminals of the bootstrap capacitors C_{BA} and C_{BB}. A 0.01-µF capacitor can be used for most applications.

Pin 24: V+

This is the only external power supply required for the Si9978DW, and must be the same supply used to power the H-bridge it is driving. The Si9978DW powers it's low-voltage logic, low-side gate driver, and bootstrap/ charge pump circuits from self-contained voltage regulators which require only a bootstrap capacitor on the CAP pins.

No voltage sensing circuitry monitors V+ directly; however, the low-voltage, internally generated supply and the bootstrap voltage (which are derived from V+) are directly protected by undervoltage monitors.

Applications

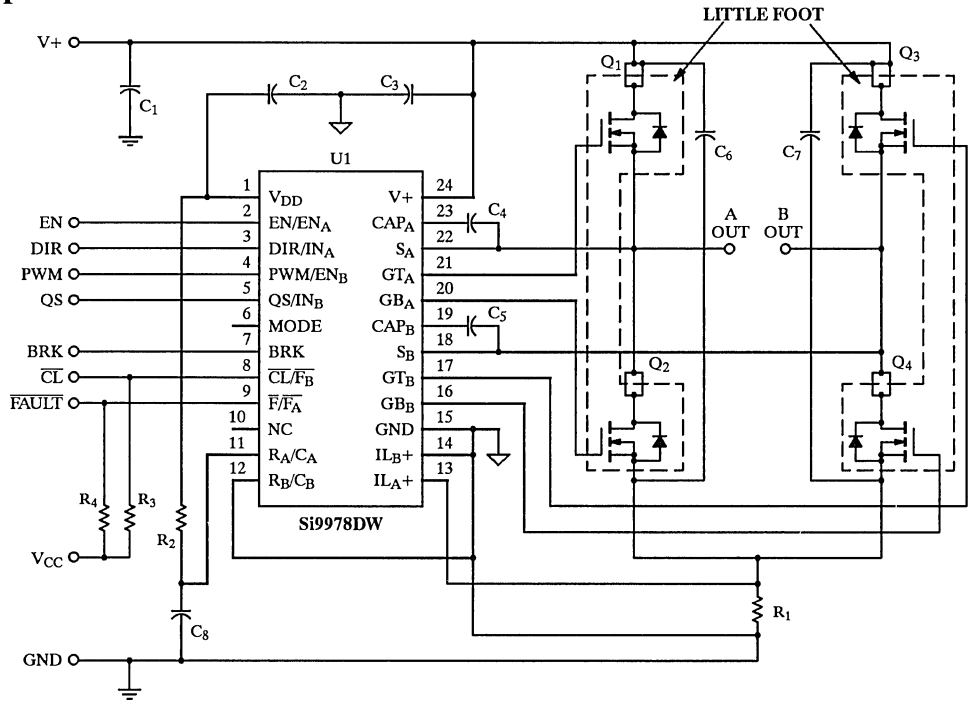


Figure 1. Basic H-Bridge Circuit

Si9979CS

Siliconix

3-Phase Brushless DC Motor Controller

Features

- Hall-Effect Commutation
- 60° or 120° Sensor Spacing
- Integral High-Side Drive for all N-Channel MOSFET Bridges
- PWM Input
- Quadrature Selection
- Tachometer Output
- Reversible
- Braking
- Output Enable Control
- Cross Conduction Protection
- Current Limiting
- Undervoltage Lockout
- Internal Pull-Up Resistors

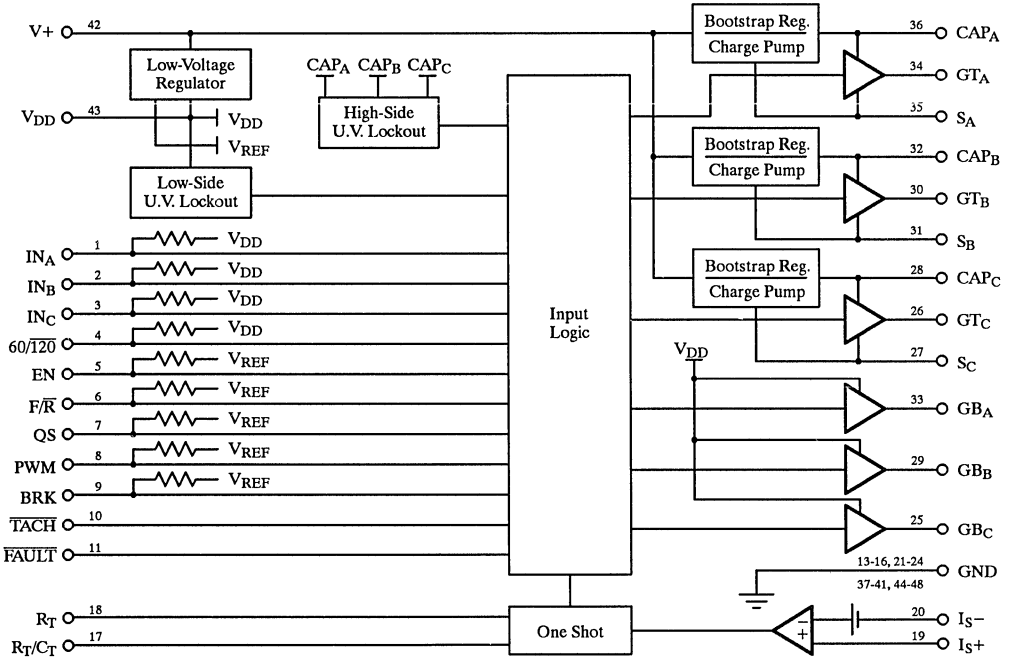
Description

The Si9979CS is a monolithic brushless dc motor controller with integral high-side drive circuitry. The Si9979 is configured to allow either 60°or 120° commutation sensor spacing. The internal low-voltage regulator allows operation over a wide input voltage range, 20- to 40-V dc.

The Si9979CS provides commutation from Hall-effect sensors. The integral high-side drive, which utilizes combination bootstrap/charge pump supplies, allows implementation of an all n-channel MOSFET 3-phase bridge. PWM, direction, quadrature select, and braking inputs are included for control along with a tachometer output. Protection features include cross conduction protection, current limiting, and undervoltage lockout. The $\overline{\text{FAULT}}$ output indicates when undervoltage, over current, disable, or invalid sensor shutdown has occurred.

The Si9979CS is specified to operate over the commercial (0°C to 70°C) temperature range.

Functional Block Diagram



Advance Information

Absolute Maximum Ratings

Voltage on Pin 42 ..... 50 V
Voltage on Pins 1–4, 10, 11 ..... −0.3 V to V_{DD} + 0.3 V
Voltage on Pins 5–9 ..... −0.3 V to 5.5 V
Voltage on Pins 26, 28, 30, 32, 34, 36 ..... 60 V
Voltage on Pins 27, 31, 35 ..... −2 to 50 V

Operating Temperature ..... 0 to 70°C
Storage Temperature ..... −65 to 150°C
Junction Temperature (T_J) ..... 150°C
Power Dissipation (P_D) ..... 0.7 W

Recommended Operating Range

V+ ..... +20 to 40 V_{DC}
R_T ..... 10 kΩ Min

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V	Limits C Suffix: 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Power						
Supply Voltage Range	V+		20		40	V
Logic Voltage	V_{DD}	−20 mA ≤ I_{DD} ≤ 0 mA	14.5	16	17.5	
Supply Current	I+	I_{DD} = 0 mA		4.5		mA
Logic Current	I_{DD}		−20			
Commutation Inputs (IN_A, IN_B, IN_C, 60/$\overline{120}$)						
High-State	V_{IH}		4.0			V
Low-State	V_{IL}				1.0	
High-State Input Current	I_{IH}	V_{IH} = V_{DD}			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V		−50		
Logic Inputs (F/$\overline{R}$, EN, QS, PWM, BRK)						
High-State	V_{IH}		2.0			V
Low-State	V_{IL}				0.8	
High-State Input Current	I_{IH}	V_{IH} = 5.5 V			10	µA
Low-State Input Current	I_{IL}	V_{IL} = 0 V		−125		
Outputs						
Low-Side Gate Drive, High State	V_{GBH}		14	16	17.5	V
Low-Side Gate Drive, Low State	V_{GBL}				0.1	
High-Side Gate Drive, High State	V_{GTH}			16	18	
High-Side Gate Drive, Low State	V_{GTL}				0.1	
Low-Side Switching, Rise Time	t_{rL}	Risetime = 1 to 10 V Falltime = 10 to 1 V C_L = 600 pF		70		ns
Low-Side Switching, Fall Time	t_{fL}			25		
High-Side Switching, Rise Time	t_{rH}			100		
High-Side Switching, Fall Time	t_{fH}			40		
Break-Before-Make Time	t_{BLH}			100		
	t_{BHL}			300		
$\overline{TACH}$ Output/$\overline{FAULT}$ Output	V_{OL}	I_{OL} = 1.0 mA		0.15	0.4	V
$\overline{TACH}$ Output Pulsewidth	t_T		300	600		ns

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 20 to 40 V	Limits C Suffix: 0 to 70°C Min[a]	Typ[b]	Max[a]	Unit
Protection						
Low-Side Undervoltage Lockout	UVLL			12.2		V
Low-Side Hysteresis	V_H			0.8		
High-Side Undervoltage Lockout	UVLH	$S_{A, B, C}$ = 0 V		V_{DD} − 3.3		
Current Limit						
Comparator Input Bias Current	I_{IB}		−5			µA
Comparator Threshold Voltage	V_{TH}		90	100	110	mV
Common Mode Voltage	V_{CM}		0		1	V
One Shot Pulse Width	t_p	R_T = 10 k C_T = 0.001 µF	8	10	12	µs
		R_T = 10 k C_T = 0.01 µF	80	100	120	

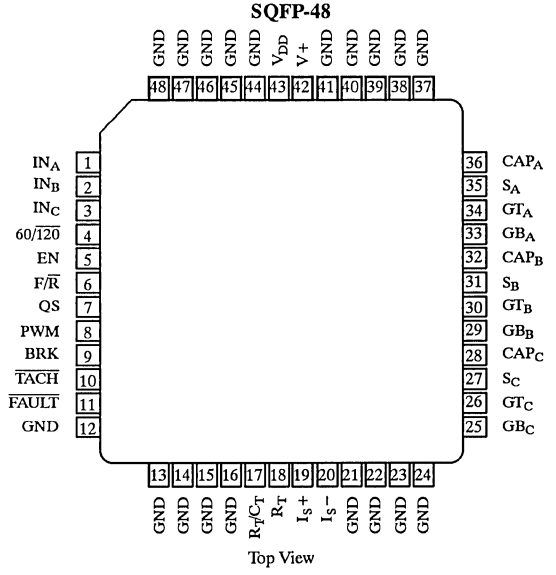
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Commutation Truth Table

Inputs										Outputs							Conditions
Sensors (60°Spacing)			Sensors (120°Spacing)							Top Drive			Bottom Drive				
IN_A	IN_B	IN_C	IN_A	IN_B	IN_C	EN	F/$\overline{R}$	BRK	I_S+	GT_A	GT_B	GT_C	GB_A	GB_B	GB_C	$\overline{FAULT}$	
0	0	0	1	0	1	1	1	0	0	1	0	0	0	1	0	1	
1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	1	
1	1	0	1	1	0	1	1	0	0	0	1	0	0	0	1	1	
1	1	1	0	1	0	1	1	0	0	0	1	0	1	0	0	1	
0	1	1	0	1	1	1	1	0	0	0	0	1	1	0	0	1	
0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	1	
0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	0	1	
1	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0	1	
1	1	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1	
1	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	
0	1	1	0	1	1	1	0	0	0	1	0	0	0	0	1	1	
0	0	1	0	0	1	1	0	0	0	0	1	0	0	0	1	1	
X	X	X	X	X	X	0	X	0	X	0	0	0	0	0	0	0	Disable
X	X	X	X	X	X	0	X	1	X	0	0	0	1	1	1	0	Power Down
L	L	L	L	L	L	1	X	1	0	0	0	0	1	1	1	1	Brake
L	L	L	L	L	L	1	X	1	1	0	0	0	1	1	1	0	Over I in BRK
L	L	L	L	L	L	1	X	0	1	0	0	0	0	0	0	0	Over I
1	0	1	1	1	1	1	X	0	X	0	0	0	0	0	0	0	
1	0	1	1	1	1	1	X	1	X	0	0	0	1	1	1	0	
0	1	0	0	0	0	1	X	0	X	0	0	0	0	0	0	0	
0	1	0	0	0	0	1	X	1	X	0	0	0	1	1	1	0	

Notes: L. Any valid sensor combination
X. Don't care

Pin Configuration



Top View

Pin Description

Pins 1–3: IN_A, IN_B, IN_C

IN_A, IN_B, and IN_C are the commutation sensor inputs, and are intended to be driven by open collector Hall effect switches. These inputs have internal pull up resistors tied to V_{DD}, which eliminates the need for external pull up resistors.

Pin 4: 60/$\overline{120}$

The 60/$\overline{120}$ input allows the use of the Si9979 with either a 60° or 120° commutation sensor spacing. An internal pull up resistor, which is tied to V_{DD}, sets the default condition to 60° spacing. 120° spacing is selected by pulling this input to ground.

Pin 5: EN (Enable)

A logic "1" on this input allows commutation of the motor. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, all gate drive outputs are turned off.

Pin 6: F/$\overline{R}$ (Forward/Reverse)

A logic "1" on this input selects commutation for motor rotation in the "forward" direction. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, the commutation sensor logic levels are inverted internally, causing reverse rotation.

Pin 7: QS (Quadrature Select)

This input determines whether the bottom MOSFETs or both bottom and top MOSFETs switch in response to the PWM signal. A logic "1" on this input enables only the bottom MOSFETs. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, both the bottom and top MOSFETs are enabled.

Pin 8: PWM

An open collector (drain) or TTL compatible signal is applied to this input to control the motor speed. The QS input determines which MOSFETs are switched in response to the PWM signal. If no PWM signal is being used, this input is left open. It is pulled up internally, which allows the MOSFETs to follow the commutation sequence.

Pin Description (Cont'd)

Pin 9: BRK

With this input at logic "1", the top MOSFETs are turned off and the bottom MOSFETs are turned on, shorting the motor windings together. This provides a braking torque which is dependent on the motor speed. This is the default condition as this pin is pulled up internally. When this pin is pulled to ground, the MOSFETs are allowed to follow the commutation sequence.

Pin 10: $\overline{\text{TACH}}$

This output provides a minimum 300 nanosecond output pulse for every commutation sensor transition, yielding a 6 pulse per electrical revolution tachometer signal. This output is open drain.

Pin 11: $\overline{\text{FAULT}}$

The $\overline{\text{FAULT}}$ output switches low to indicate that at least one of the following conditions exists, controller disable ($\overline{\text{EN}}$), undervoltage lockout, invalid commutation sensor code shutdown, or overcurrent shutdown. This output is open drain.

Pin 17: R_T/C_T

The junction of the current limit one shot timing resistor and capacitor is connected to this pin. This one-shot is triggered by the current limit comparator when an overcurrent condition exists. This action turns off all the gate drives for the period defined by R_T and C_T, thus stopping the flow of current.

Pin 18: R_T

One side of the current limit one shot timing resistor is connected to this pin.

Pin 19: I_S+

This is the sensing input of the current limit comparator and should be connected to the positive side of the current sense resistor. When the voltage across the current sense resistor exceeds 100 mV, the comparator switches and triggers the current limit one-shot. The one-shot turns off all the gate drives for the period defined by R_T and C_T, thus stopping the flow of current. If the overcurrent condition remains after the shutdown period, the gate drives will be held off until the overcurrent condition no longer exists.

Pin 20: I_S-

This pin is the ground reference for the current limit comparator. It should be connected directly to the ground side of the current sense resistor to enhance noise immunity.

Pins 12–16: 21–24, 37–41, 44–48, GND

These pins are the return path for both the logic and gate drive circuits. Also, they serve to conduct heat out of the package, into the circuit board.

Pin 25: GB_C

This is the gate drive output for the bottom MOSFET in Phase C.

Pin 26: GT_C

This is the gate drive output for the top MOSFET in Phase C.

Pin 27: S_C

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase C output.

Pin 28: CAP_C

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase C is connected between this pin and SC.

Pin 29: GB_B

This is the gate drive output for the bottom MOSFET in Phase B.

Pin 30: GT_B

This is the gate drive output for the top MOSFET in Phase B.

Pin 31: S_B

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase B output.

Pin Description (Cont'd)

Pin 32: CAP_B

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase B is connected between this pin and SB.

Pin 33: GB_A

This is the gate drive output for the bottom MOSFET in Phase A.

Pin 34: GT_A

This is the gate drive output for the top MOSFET in Phase A.

Pin 35: S_A

This pin is negative supply of the high-side drive circuitry. As such, it is the connection for the negative side of the bootstrap capacitor, the top MOSFET Source, the bottom MOSFET Drain, and the Phase A output.

Pin 36: CAP_A

This pin is the positive supply of the high-side circuitry. The bootstrap capacitor for Phase A is connected between this pin and SA.

Pin 42: V+

The supply voltage for the Si9979 is connected between this pin and ground. The internal logic and high-side supply voltages are derived from V+.

Pin 43: V_{DD}

V_{DD} is the internal logic and gate drive voltage. It is necessary to connect a capacitor between this pin and ground to insure that the current surges seen at the turn on of the bottom MOSFETs does not trip the undervoltage lockout circuitry.

Applications

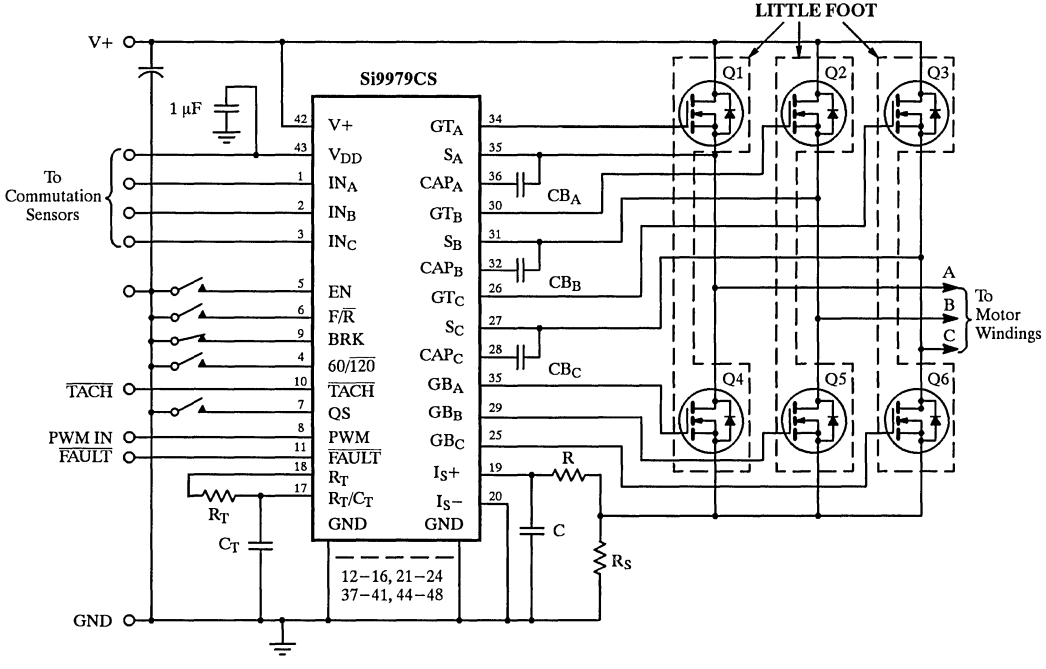


Figure 1. Three-Phase Brushless DC Motor Controller

Applications (Cont'd)

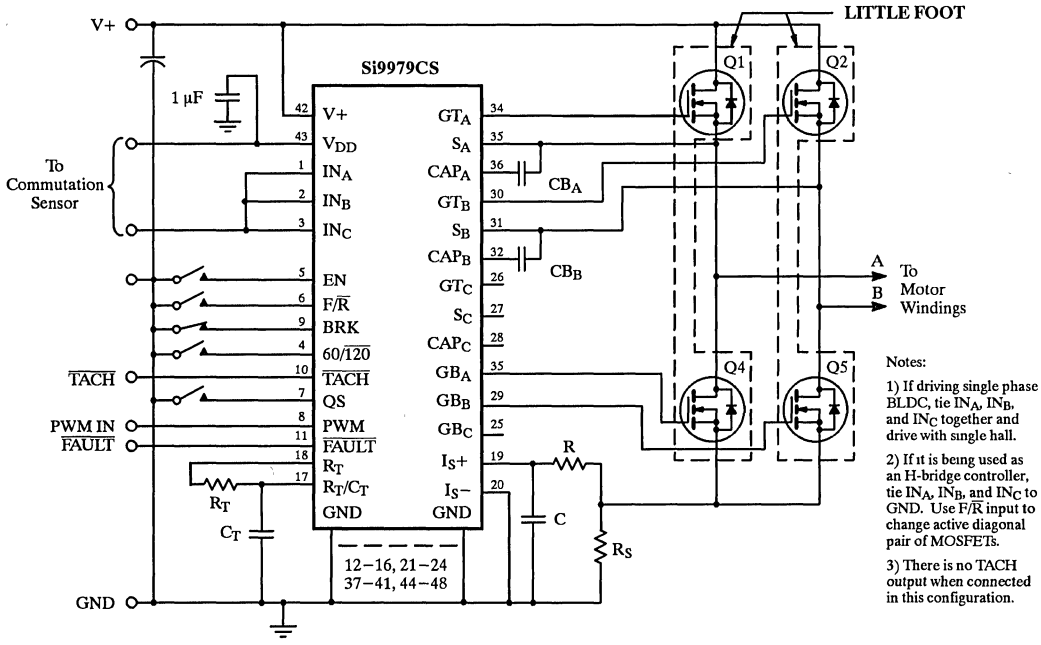


Figure 2. Single H-Bridge Controller

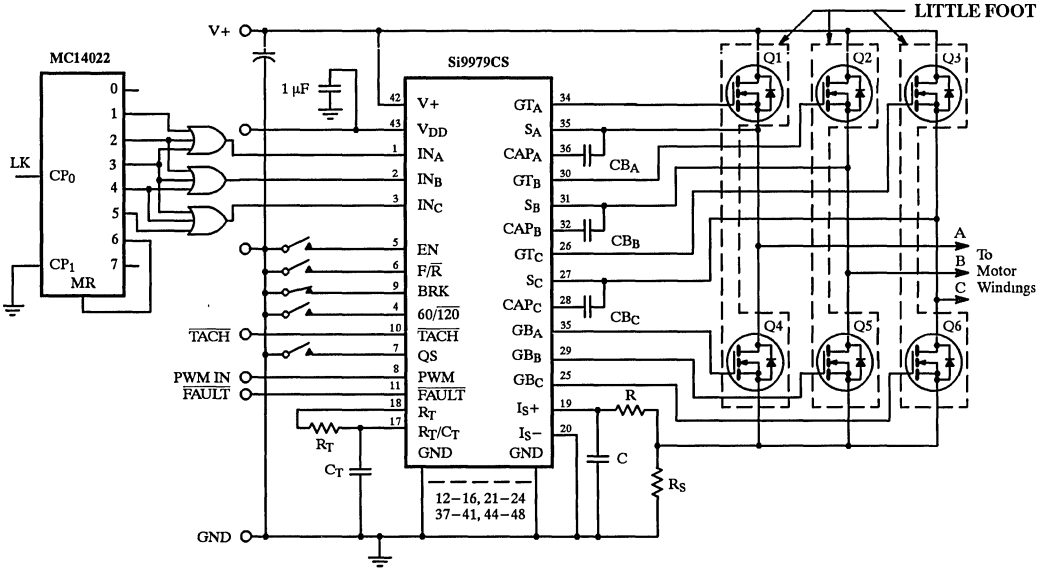
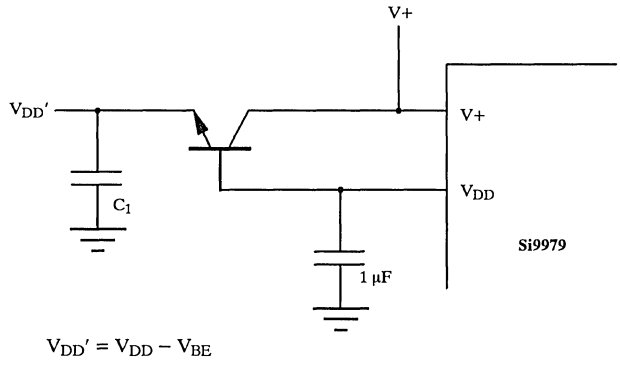


Figure 3. Three-Phase AC Motor Controller

Applications (Cont'd)



$V_{DD}' = V_{DD} - V_{BE}$

Figure 4. External V_{DD} Regulator

TEMIC

Bus Interface 5

Siliconix

Si9241

Single-Ended Bus Driver

Features

- Single-Ended Transceiver
- Survives Shorts and Transients on Automotive Bus
- Wide Power Supply Voltage Range
- Fault Detection
- ISO 9141 Compatible

Benefits

- Single-Wire Multiplexer Interface
- ISO Diagnosis Bus

Applications

- Automobiles
- Trucks
- Tractors

Description

The Si9241 is a monolithic bus driver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to GND or V_B. The transceiver pin is protected and can be driven beyond the V_B voltage.

A fault detector provides an active low in case of short circuit to V_B or an open load prevent proper data transmission. The open drain Fault output can be wire or-ed. The $\overline{CS}$ input can be tied high for receive only interfaces.

In the event of an over temperature condition, the output is immediately switched off and a fault indicated. This condition can only be reset once the over temperature condition is removed, and $\overline{CS}$ is toggled high.

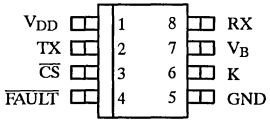
The Si9241 is built on the Siliconix BiC/DMOS process. This process supports bipolar transistors, CMOS and DMOS. An epitaxial layer prevents latchup.

The RX output is capable of driving CMOS or 1 × LSTTL load.

The Si9241 is available in a space efficient 8-pin SO package. It operates reliably over the automotive temperature range (−40 to 125°C).

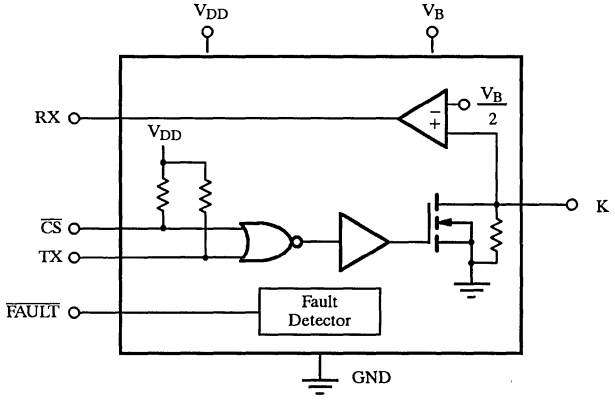
Pin Configurations and Functional Block Diagram

Narrow Body
SO Package

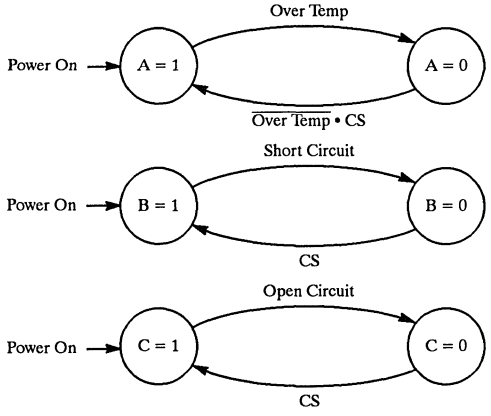


Top View

Order Number:
Si9241EY



Output Table and State Diagrams



Note: Over Temp is a condition and not meant to be a logic signal.

Inputs		State Variable			Output Table			
$\overline{CS}$	TX	A	B	C	RXK	K	$\overline{FAULT}$	Comments
0	0	1	1	1	0	0	1	
0	1	1	1	1	1	1	1	
x	x	0	1	1	K	HiZ	0	Over Temp
0	x	1	0	1	K	HiZ	0	Short Circuit
0	x	1	1	0	K	HiZ	0	Open Circuit
1	x	1	1	1	0	0	1	Receive Mode
1	x	1	1	1	1	1	1	

X = "1" or "0"
HiZ = High Impedance State

Absolute Maximum Ratings

Voltage Referenced to Ground
Voltage On V_{BAT} ..... 45 V
Voltage K ..... -3 to $V_{BAT} + 1$ V
Voltage or Max. Current On Any Pin
(Except V_{BAT}, K) ..... -0.3 to $V_{DD} + 0.3$ V or 10 mA

Voltage on V_{DD} ..... 7 V
Short Circuit Duration (to V_{BAT} or GND) ..... Continuous
Operating Temperature (T_A) ..... -40 to 125°C
Junction and Storage Temperature ..... -55 to 150°C
Thermal Resistance Θ_{JA} ..... TBD

Specifications[a]

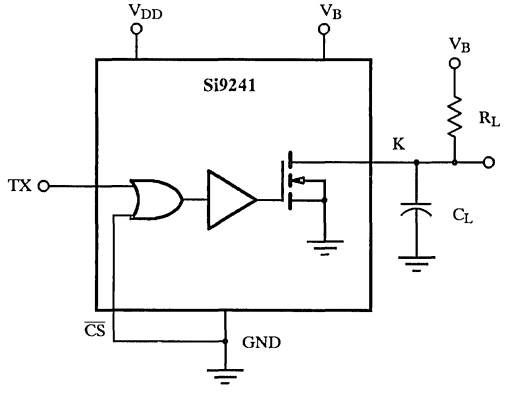
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_{BAT} = 8 to 35 V	Temp[b]	Limits E Suffix: -40 to 125°C Min[c]	Typ[d]	Max[c]	Unit
Transmitter and Logic Levels							
$\overline{CS}$, TX Input Low Voltage	V_{ILT}		Full			1.5	V
$\overline{CS}$, TX Input High Voltage	V_{IHT}		Full	3.5			
K Output Low Voltage	V_{OLK}	R_L = 510 Ω, C_L = 10 nF See Test Circuit	Full			0.2 V_{BAT}	
K Output High Voltage	V_{OHK}		Full	0.91 V_{BAT}			
K Rise, Fall Times	t_r, t_f		Full			9.6	µs
K Output Sink Resistance	Rsi	$\overline{CS}$ = 0 V, TX = 0 V	Full			110	Ω
K Output Capacitance[e]	C_O	$\overline{CS}$ = 0 V	Full			20	pF
TX Input Capacitance[e]	C_{INT}		Full			10	
$\overline{CS}$, TX Input Current	I_{INT}		Full	−60		−4	µA

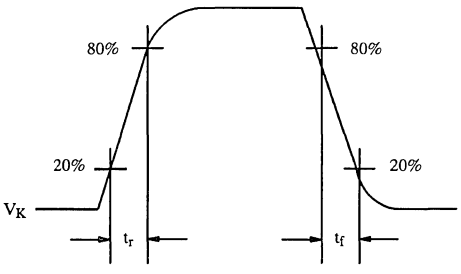
Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5 5 V, V_{BAT} = 8 to 35 V		Temp[b]	Limits E Suffix: −40 to 125°C Min[c]	Typ[d]	Max[c]	Unit
Receiver								
K Input Low Voltage[f]	V_{ILK}			Full		0.4 V_{BAT}	0.30 V_{BAT}	V
K Input High Voltage[f]	V_{IHK}			Full	0.70 V_{BAT}	0.6 V_{BAT}		V
RX Output Low Voltage	V_{OLR}	$\overline{CS}$ = 4 V	V_{ILK}, V_{ILL} = 0.30 V_{BAT} I_{OLR} = 1 mA	Full			0.4	V
RX High Voltage	V_{OHR}	$\overline{CS}$ = 4 V	V_{IHK}, V_{IHL} = 0.70 V_{BAT} I_{OHR} = −40 µA	Full	2.8			V
K Input Currents	I_{IHK}	$\overline{CS}$ = 4 V	V_{IHK} = V_{BAT}	Full	1 5		20	µA
Supplies								
Bat Supply Current	I_{BAT}	CS, TX = 1.5 V K Open		Full		2.7	5.0	mA
Logic Supply Current	I_{DD}	CS, TX = 1.5 V K Open		Full		1	3.0	mA
Miscellaneous								
Baud Rate	BR	R_L = 510 Ω, C_L = 10 nF		Full	10.4			k Baud
Fault Output Low Voltage	V_{OLF}	V_{ILT} = 0V, V_K = V_B, I_{OLF} = 1 mA		Full			0.4	V

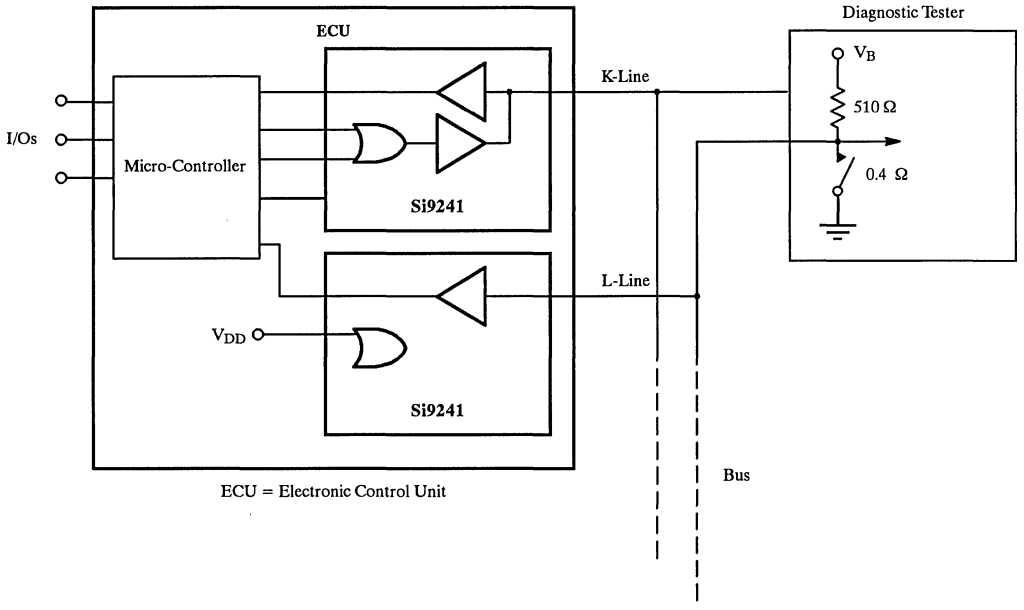
Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test
f. Hysterisis 0.2 V_{BAT} typical.

Test Circuit





Application



Single-Ended Bus Driver

Features

- Single-Ended Transceiver
- Survives Shorts and Transients on Automotive Bus
- Wide Power Supply Voltage Range
- Fault Detection
- ISO9141 Compatible

Description

The Si9243 is a monolithic bus driver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to GND or V_{BAT}. The transceiver pin is protected and can be driven beyond the V_{BAT} voltage.

The temperature and short circuit fault detection feature is still active as in the Si9242, but the $\overline{\text{FAULT}}$ signal is not brought out. In the transmit mode, load shorts and opens are generally detected by the processor monitoring RXK and TX. When the two mirror each other there is no fault, but the Si9243 will turn off the K output in the event of over temperature or short circuit to protect the IC. The fault will be reset when TX toggles "high".

TX is set "high" for receive only.

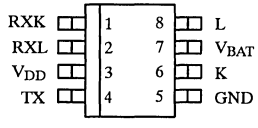
The RX output is capable of driving CMOS or 1 × LSTTL load.

The Si9243 is built on the Siliconix BiC/DMOS process. This process supports bipolar transistors, CMOS and DMOS. An epitaxial layer prevents latchup.

The Si9243 is available in a 8-pin SO package and operates over the automotive temperature range (−40 to 125°C).

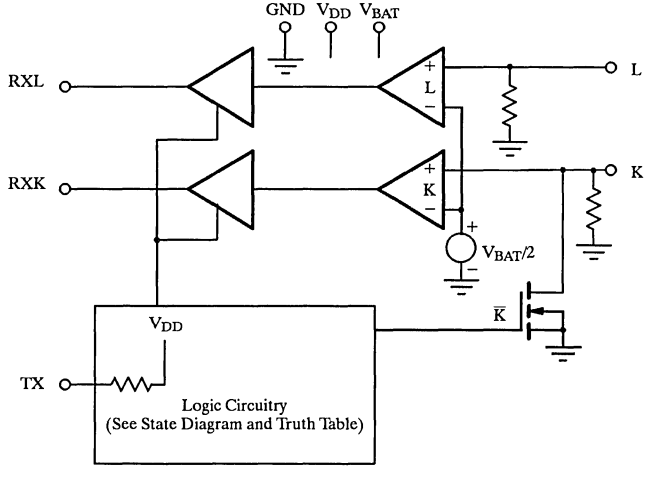
Pin Configurations and Functional Block Diagram

Narrow Body
SO Package

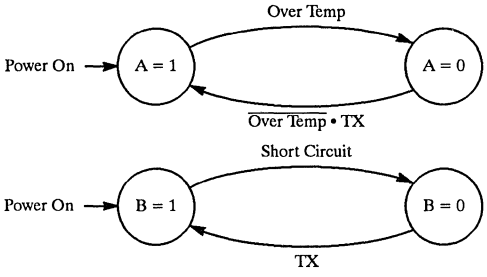


Top View

Order Number:
Si9243EY



Output Table and State Diagrams



Note: Over Temp is a condition and not meant to be a logic signal.

Inputs	State Variable		Output Table				
TX	A	B	K	RXK	L	RXL	Comments
0	1	1	0	0	0	0	
1	1	1	1	1	1	1	
0	1	1	0	0	1	1	
1	1	1	1	1	0	0	
x	0	1	HiZ	K	L	L	Over Temp
0	1	0	HiZ	1	L	L	Short Circuit
1	1	1	1	1	1	1	Receive Mode
1	1	1	0	0	0	0	

X = "1" or "0"
HiZ = High Impedance State

Absolute Maximum Ratings

Voltage Referenced to Ground
Voltage On V_{BAT} ..... 45 V
Voltage K, L ..... -3 to $V_{BAT} + 1$ V
Voltage On Any Pin (Except V_{BAT}, K)
or Max. Current ..... -0.3 to $V_{DD} + 0.3$ V or 10 mA

Voltage on V_{DD} ..... 7 V
Short Circuit Duration (to V_{BAT} or GND) ..... Continuous
Operating Temperature (T_A) ..... -40 to 125°C
Junction and Storage Temperature ..... -55 to 150°C
Thermal Resistance Θ_{JA} ..... TBD

Specifications[a]

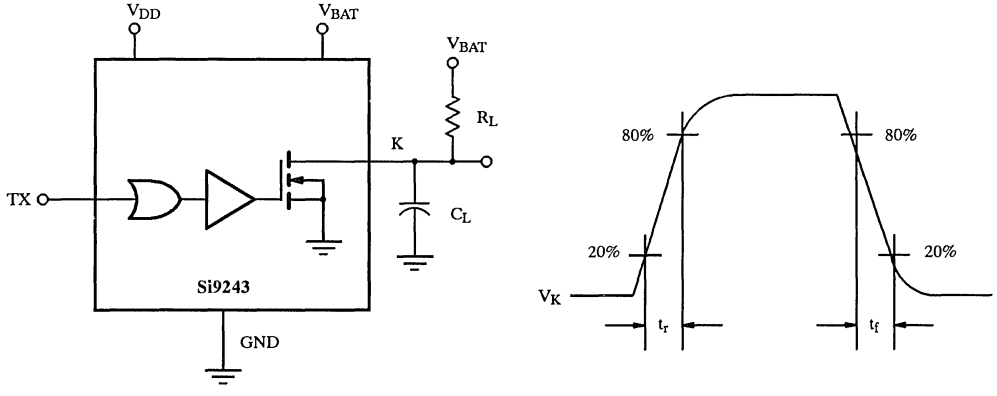
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_{BAT} = 8 to 35 V	Temp[b]	Limits E Suffix: -40 to 125°C Min[c]	Typ[d]	Max[c]	Unit
Transmitter and Logic Levels							
TX Input Low Voltage	V_{ILT}		Full			1.5	V
TX Input High Voltage	V_{IHT}		Full	3.5			
K Output Low Voltage	V_{OLK}	R_L = 510 Ω, C_L = 10 nF See Test Circuit	Full			0.2 V_{BAT}	
K Output High Voltage	V_{OHK}		Full	0.91 V_{BAT}			
K Rise, Fall Times	t_r, t_f		Full			9.6	µs
K Output Sink Resistance	Rsi	TX = 0 V	Full			110	Ω
K Output Capacitance[e]	C_O		Full			20	pF
TX Input Capacitance[e]	C_{INT}		Full			10	
TX Input Current	I_{INT}		Full	−60		−4	µA

Specifications[a]

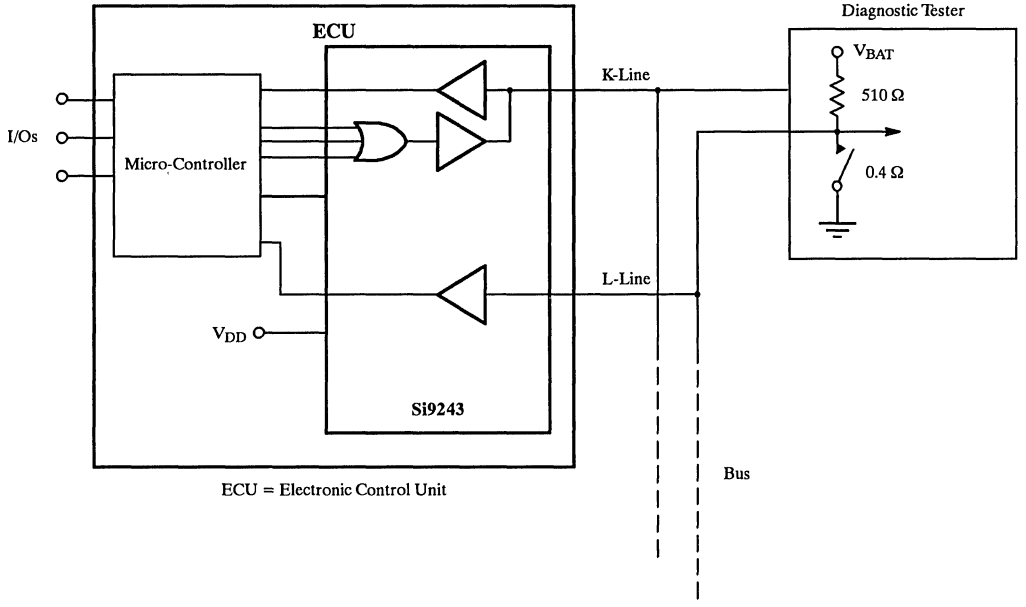
Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} = 4.5 to 5.5 V, V_{BAT} = 8 to 35 V		Temp[b]	Limits E Suffix: −40 to 125°C Min[c]	Typ[d]	Max[c]	Unit
Receiver								
L and K Input Low Voltage[f]	V_{ILK}			Full		0.4 V_{BAT}	0.3 V_{BAT}	V
L and K Input High Voltage[f]	V_{IHK}			Full	0.7 V_{BAT}	0.6 V_{BAT}		V
RXL and RXK Output Low Voltage	V_{OLR}	TX = 4 V	V_{ILK}, V_{ILL} = 0 30 V_{BAT} I_{OLR} = 1 mA	Full			0.4	V
RXL and RXK High Voltage	V_{OHR}	TX = 4 V	V_{IHK}, V_{IHL} = 0.70 V_{BAT} I_{OHR} = −40 µA	Full	2.8			V
L and K Input Currents	I_{IHK}	TX = 4 V	V_{IHK} = V_{BAT}	Full	1.5		20	µA
Supplies								
Bat Supply Current	I_{BAT}	TX = 1.5 V, K, L Open		Full		2.7	5.0	mA
Logic Supply Current	I_{DD}	TX = 1.5 V, K, L Open		Full		1	3.0	mA
Miscellaneous								
Baud Rate	BR	R_L = 510 Ω, C_L = 10 nF		Full	10.4			k Baud

Notes
a Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. Hysterisis 0.2 V_{BAT} typical.

Test Circuit



Application



N-/P-Channel MOSFETs

6

About N-/P-Channel MOSFETs

Siliconix is the industry leader for low on-resistance power MOSFETs, which are offered in a wide range of voltages and package types. Technologies packing as many as 8 million cells per square inch of silicon make possible 60-V devices with n-channel on-resistance of 8 mΩ and p-channel on-resistance of 20 mΩ—the lowest maximum rated values for any given package on the market. Products in this section include devices housed in the TO-220, DPAK, D^2PAK, and other packages rated for both the industrial and military temperature ranges.

Siliconix

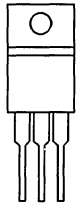
BUZ11

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.040	30

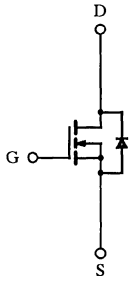
TO-220AB



G D S

Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		19	
Pulsed Drain Current		I_{DM}	120	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		75	°C/W
Junction-to-Case	R_{thJC}		1.67	
Case-to-Sink	R_{thCS}	1.0		

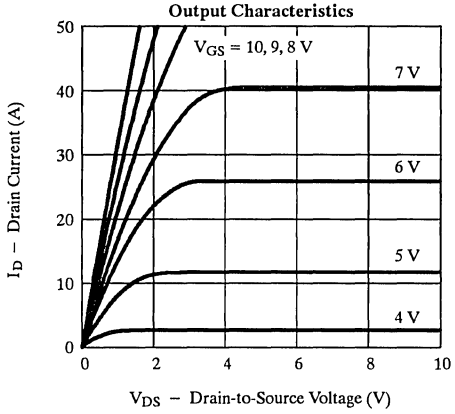
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA	2.1		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		V_{DS} = 50 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.030	0.040	Ω
		V_{GS} = 10 V, I_D = 15 A, T_J = 125°C		0.045	0.070	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 15 A	4.0	8.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1900	2000	pF
Output Capacitance	C_{oss}			1000	1100	
Reverse Transfer Capacitance	C_{rss}			260	400	
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 30 A		52	75	nC
Gate-Source Charge[c]	Q_{gs}			14		
Gate-Drain Charge[c]	Q_{gd}			22		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 10 Ω $I_D \simeq$ 3 A, V_{GEN} = 10 V, R_G = 25 Ω		30	45	ns
Rise Time[c]	t_r			50	110	
Turn-Off Delay Time[c]	$t_{d(off)}$			100	230	
Fall Time[c]	t_f			110	170	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				30	A
Pulsed Current	I_{SM}				120	
Forward Voltage[b]	V_{SD}	I_F = 30 A, V_{GS} = 0 V			2.6	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, dI_F/dt = 100 A/µs		65		ns
Reverse Recovery Charge	Q_{rr}			0.16		µC

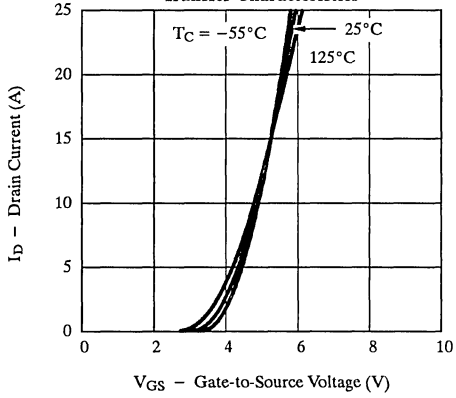
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

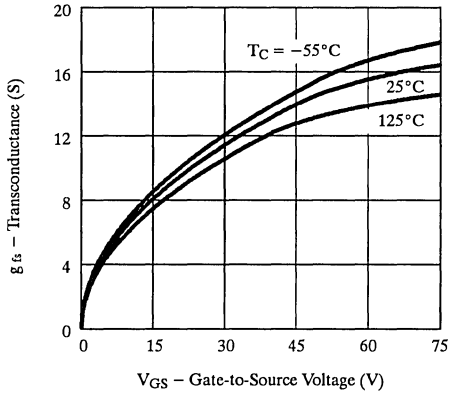
Output Characteristics



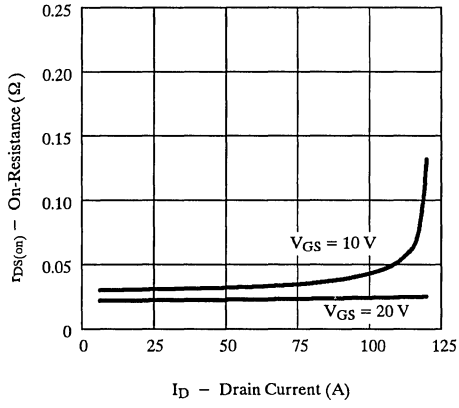
Transfer Characteristics



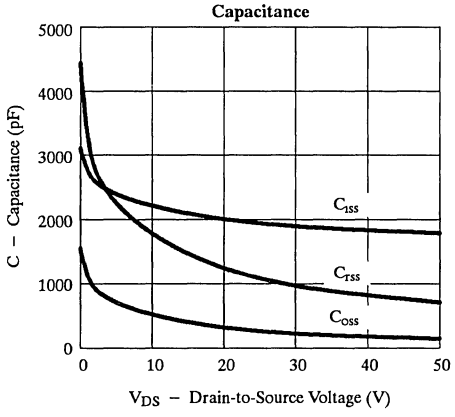
Transconductance



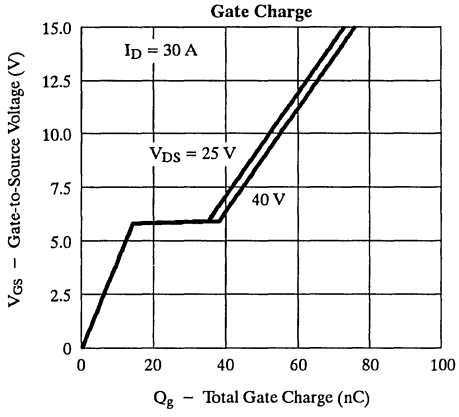
On-Resistance vs. Drain Current



Capacitance

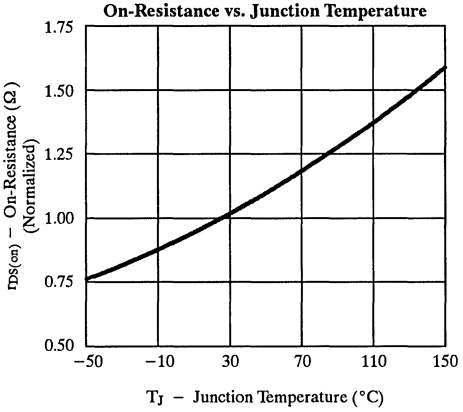


Gate Charge

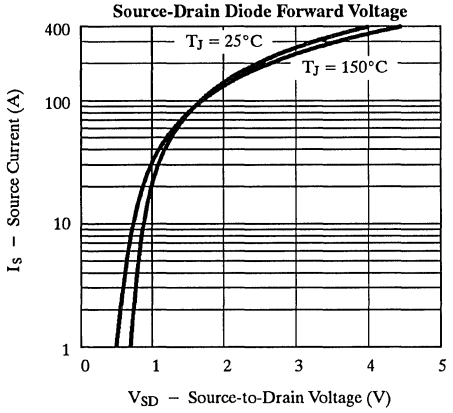


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

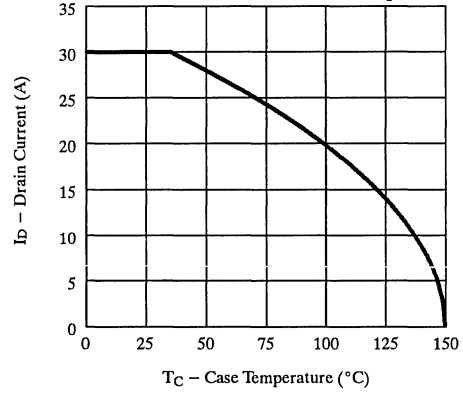


Source-Drain Diode Forward Voltage

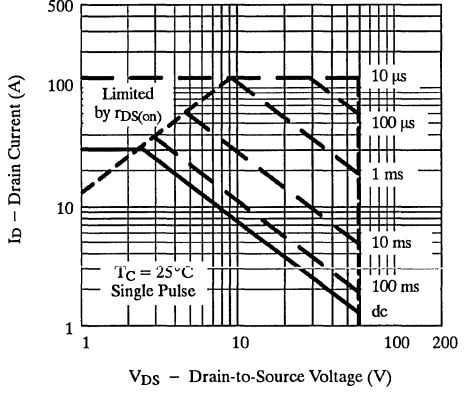


Thermal Ratings

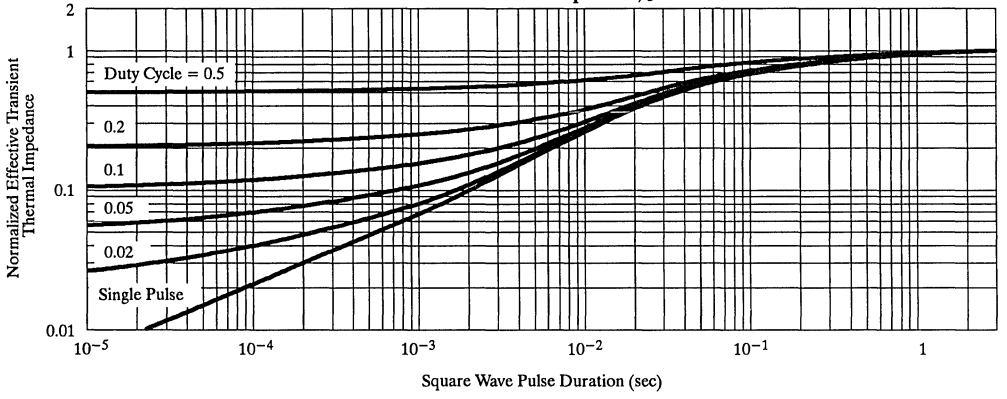
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

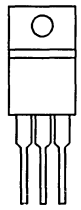


N-Channel Enhancement-Mode Transistors

Product Summary

Part Number	$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
BUZ71	50	0.10	14
BUZ71A	50	0.12	13

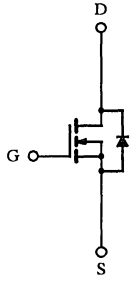
TO-220AB



G D S

Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	BUZ71	BUZ71A	Unit
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_C = 25°C	I_D	14	13	A
	T_C = 100°C		9	8.2	
Pulsed Drain Current		I_{DM}	56	48	
Power Dissipation	T_C = 25°C	P_D	40	40	W
	T_C = 100°C		16	16	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		75	°C/W
Junction-to-Case	R_{thJC}		3.1	
Case-to-Sink	R_{thCS}	1.0		

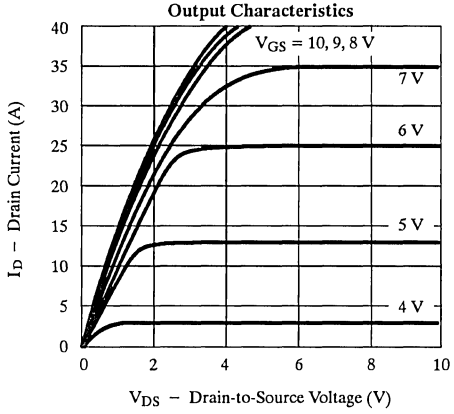
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.1		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V				250	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10 V	BUZ71	14			A
			BUZ71A	13			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 6 A	BUZ71		0.7	0.10	Ω
			BUZ71A		0.10	0.12	
		V_{GS} = 10 V, I_D = 6 A, T_J = 125°C	BUZ71		0.13	0.18	
			BUZ71A		0.17	0.20	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 6 A		3.0	8.0		S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			400	650	pF
Output Capacitance	C_{oss}				150	450	
Reverse Transfer Capacitance	C_{rss}				35	280	
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 13 A			14	30	nC
Gate-Source Charge[c]	Q_{gs}				3		
Gate-Drain Charge[c]	Q_{gd}				4		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 3 A, V_{GEN} = 10 V, R_G = 25 Ω			10	30	
Rise Time[c]	t_{rr}				20	85	
Turn-Off Delay Time[c]	$t_{d(off)}$				40	90	
Fall Time[c]	t_f				25	110	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)							
Continuous Current	I_S		BUZ71			14	A
			BUZ71A			13	
Pulsed Current	I_{SM}		BUZ71			56	
			BUZ71A			48	
Foward Voltage[b]	V_{SD}	I_F = I_S, V_{GS} = 0 V	BUZ71			1.8	V
			BUZ71A			2.2	
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs			120		ns
Reverse Recovery Charge	Q_{rr}				0.5		µC

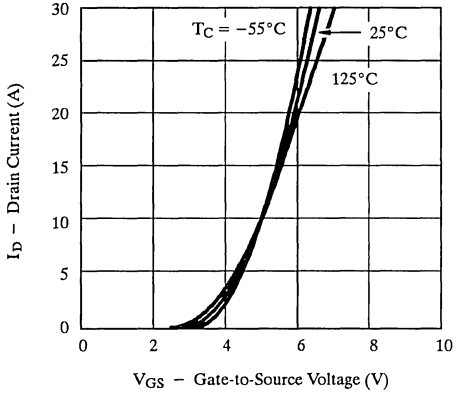
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

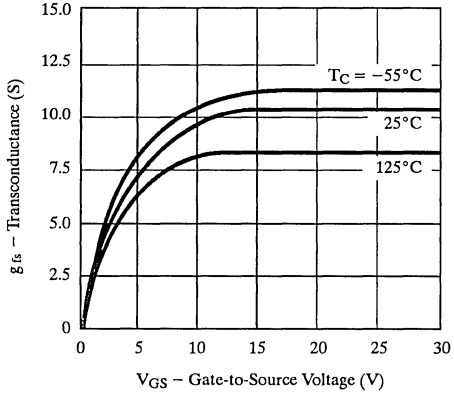
Output Characteristics



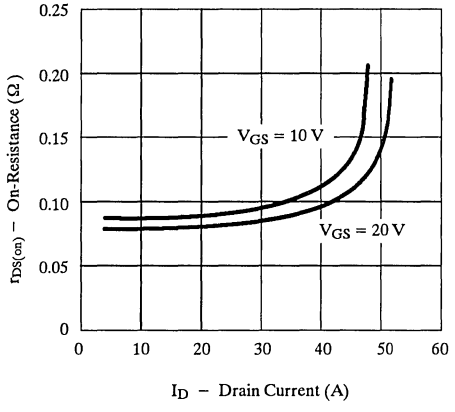
Transfer Characteristics



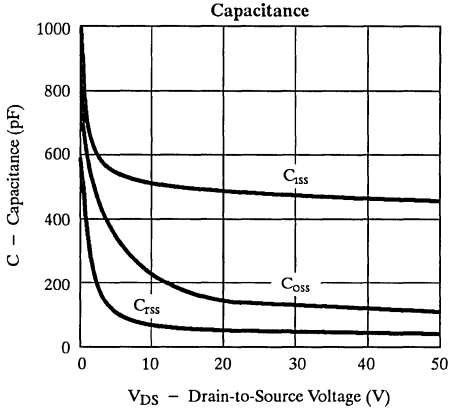
Transconductance



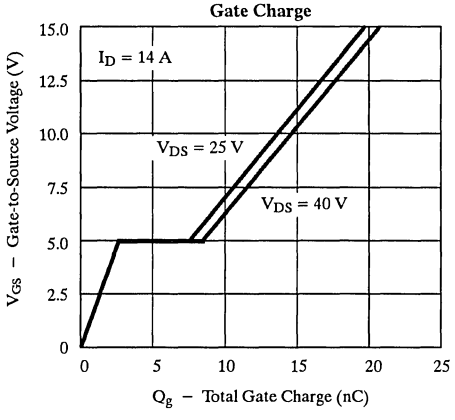
On-Resistance vs. Drain Current



Capacitance

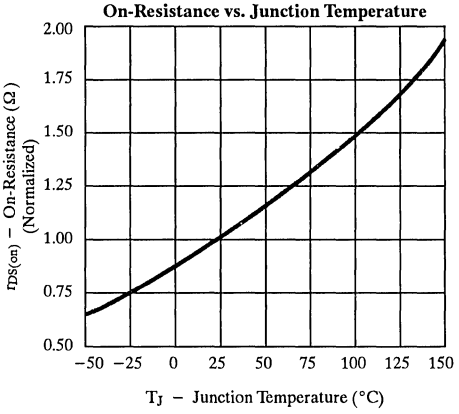


Gate Charge

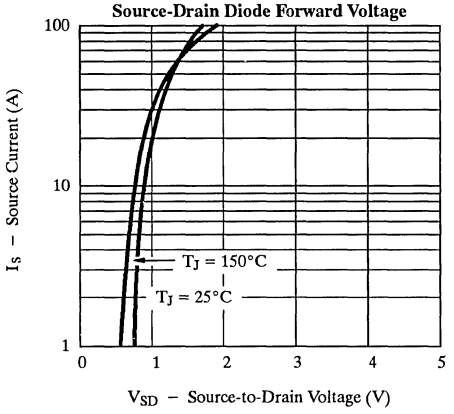


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

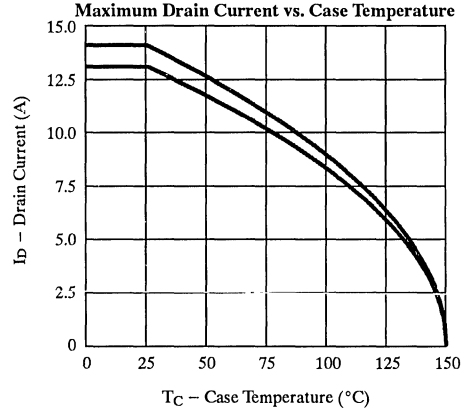


Source-Drain Diode Forward Voltage

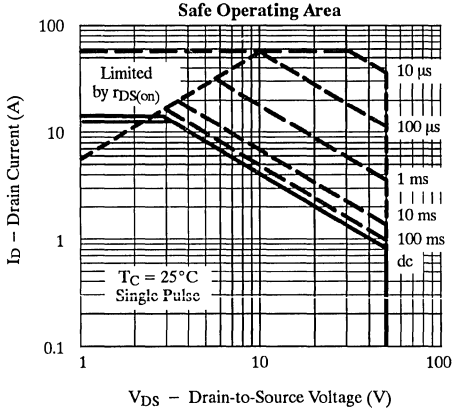


Thermal Ratings

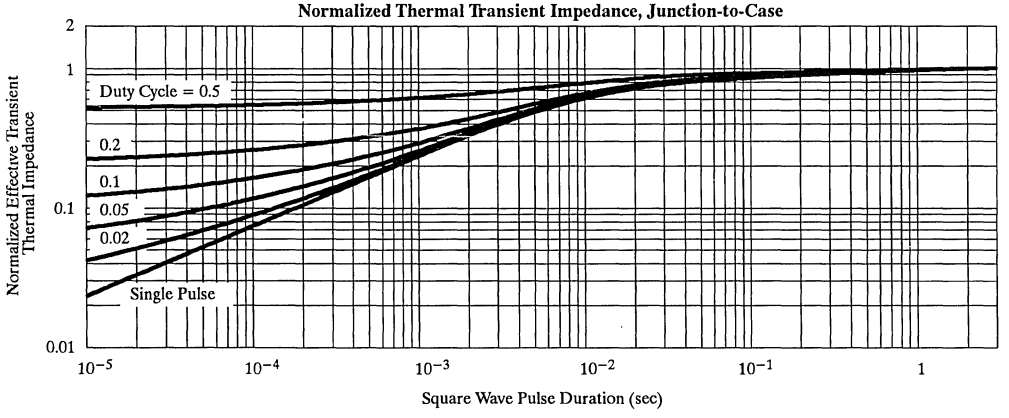
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

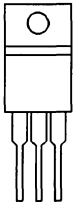
BUZ171

P-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−50	0.40	−7.0

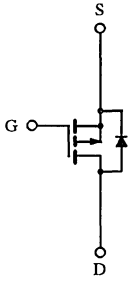
TO-220AB



DRAIN connected to TAB

G D S

Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	−7.0	A
	T_C = 100°C		−4.5	
Pulsed Drain Current[a]		I_{DM}	−28	
Power Dissipation	T_C = 25°C	P_D	40	W
	T_C = 100°C		16	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		75	°C/W
Junction-to-Case	R_{thJC}		3.1	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Pulse width limited by maximum junction temperature

Specifications (T_J = 25°C Unless Otherwise Noted)

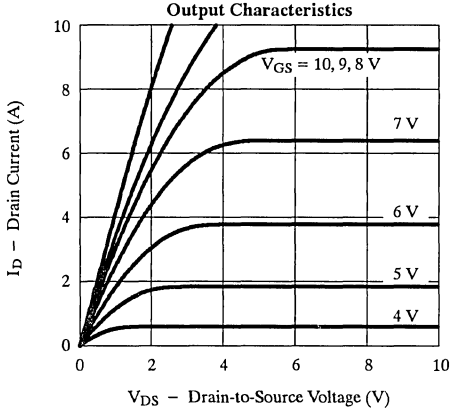
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−2.1		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −50, V_{GS} = 0 V			−250	µA
		V_{DS} = −50 V, V_{GS} = 0 V, T_J = 125°C			−1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−7.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −4.5 A		0.24	0.40	Ω
		V_{GS} = −10 V, I_D = −4.5 A, T_J = 125°C		0.40	0.72	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −4.5 A	1.5	2.8		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		600	1200	pF
Output Capacitance	C_{oss}			325	500	
Reverse Transfer Capacitance	C_{rss}			100	230	
Total Gate Charge[c]	Q_g	V_{DS} = −25 V, V_{GS} = −10 V, I_D = −7 A		16	20	nC
Gate-Source Charge[c]	Q_{gs}			3.8		
Gate-Drain Charge[c]	Q_{gd}			7.5		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 10 Ω $I_D \simeq$ −2.9 A, V_{GEN} = −10 V, R_G = 25 Ω		10	30	ns
Rise Time[c]	t_r			50	95	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	90	
Fall Time[c]	t_f			50	75	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				−7.0	A
Pulsed Current	I_{SM}				−28	
Forward Voltage[b]	V_{SD}	I_F = −7 A, V_{GS} = 0 V			−2.8	V
Reverse Recovery Time	t_{rr}	I_F = −7 A, dI_F/dt = 100 A/µs		70		ns
Reverse Recovery Charge	Q_{rr}			0.15		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independet of operating temperature.

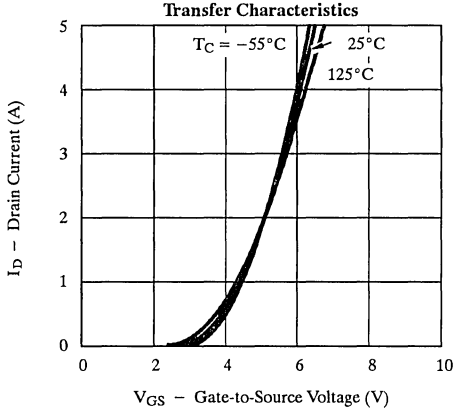
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

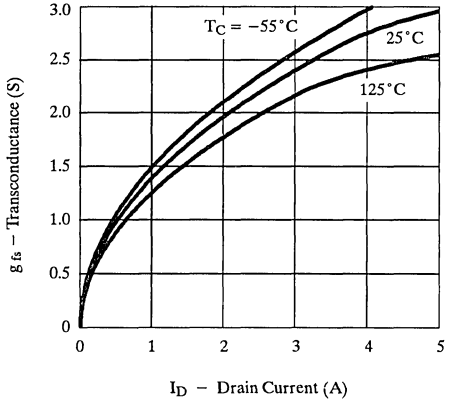
Output Characteristics



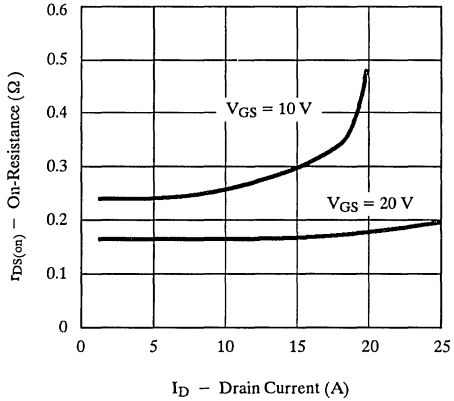
Transfer Characteristics



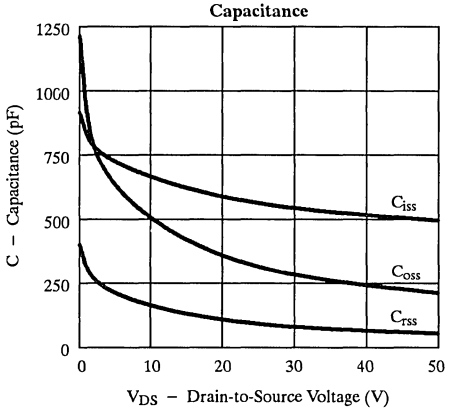
Transconductance



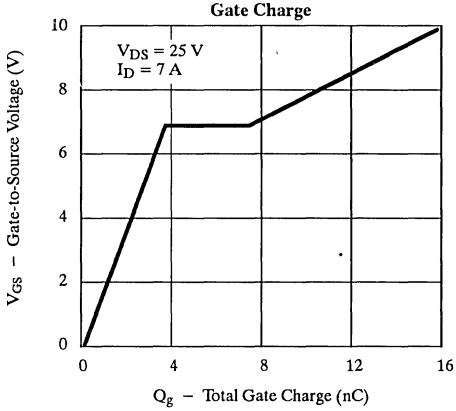
On-Resistance vs. Drain Current



Capacitance



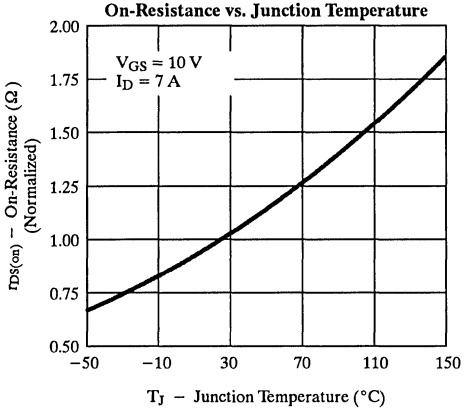
Gate Charge



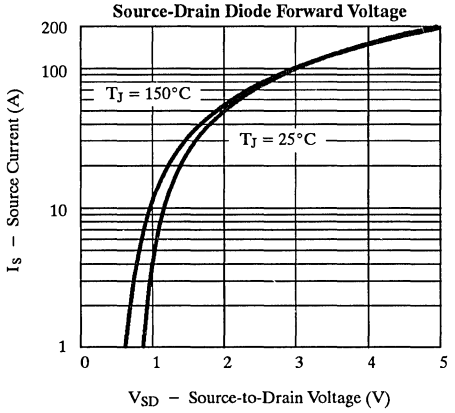
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

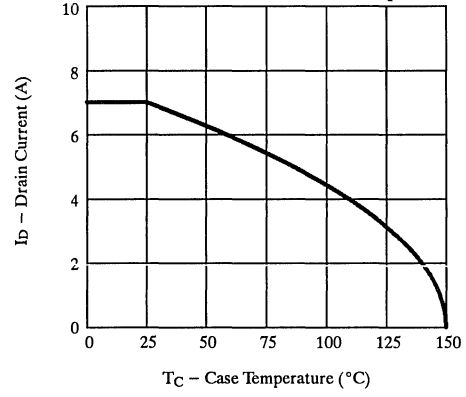


Source-Drain Diode Forward Voltage

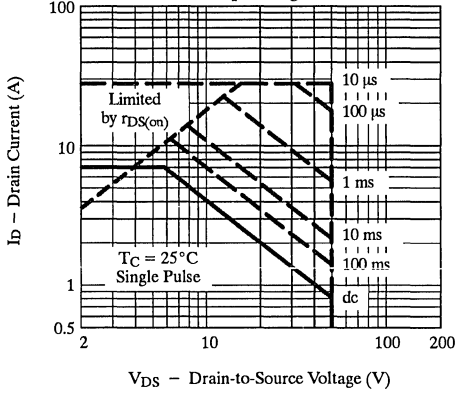


Thermal Ratings

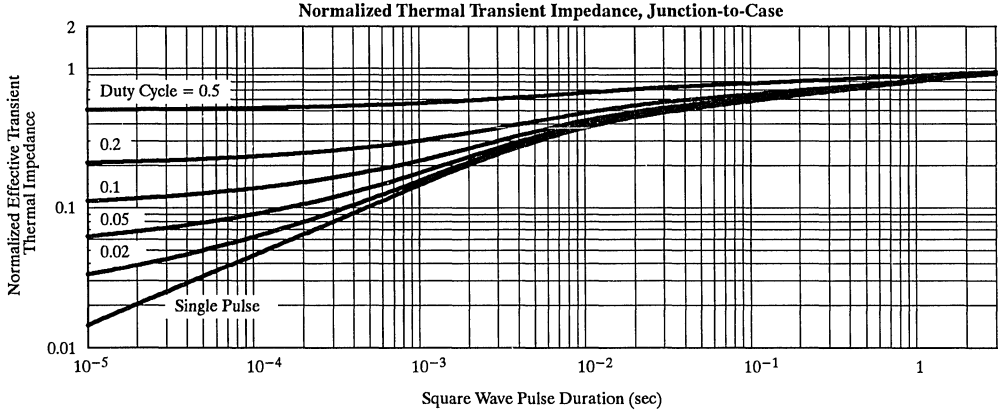
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

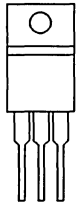
IRF510

N-Channel Enhancement-Mode Transistor

Product Summary

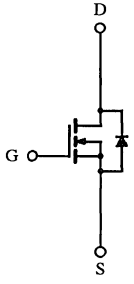
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.6	4.0

TO-220AB



Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.5	
Pulsed Drain Current		I_{DM}	16	
Avalanche Current		I_{AR}	4.0	
Repetitive Avalanche Energy[a]	L = 0.3 mH	E_{AR}	2.4	mJ
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		6.4	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

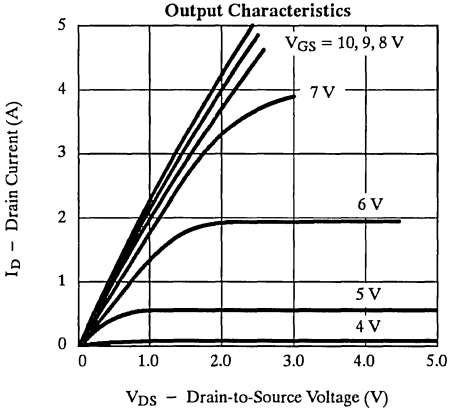
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	4.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.0 A		0.48	0.60	Ω
		V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C		0.8	1.1	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 2.0A	1.0	1.8		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		180	200	pF
Output Capacitance	C_{oss}			60	100	
Reverse Transfer Capacitance	C_{rss}			10	25	
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 4 A		7	7.5	nC
Gate-Source Charge[c]	Q_{gs}			1.9		
Gate-Drain Charge[c]	Q_{gd}			3.0		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 20Ω $I_D \simeq$ 2.0 A, V_{GEN} = 10 V, R_G = 25 Ω		7	20	ns
Rise Time[c]	t_r			14	25	
Turn-Off Delay Time[c]	$t_{d(off)}$			15	25	
Fall Time[c]	t_f			9	20	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				4.0	A
Pulsed Current	I_{SM}				16	
Forward Voltage[b]	V_{SD}	I_F = 4 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 4 A, dI_F/dt = 100 A/µs		65		ns
Reverse Recovery Charge	Q_{rr}			0.12		µC

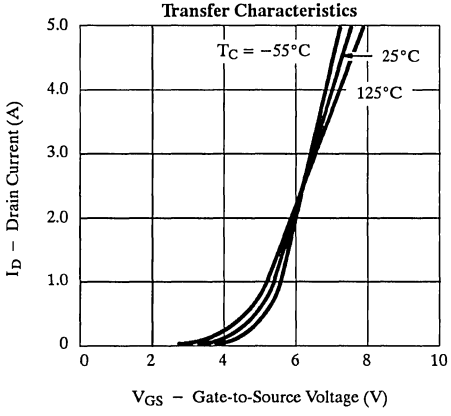
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

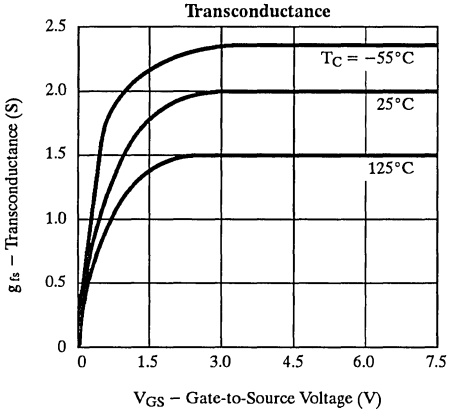
Output Characteristics



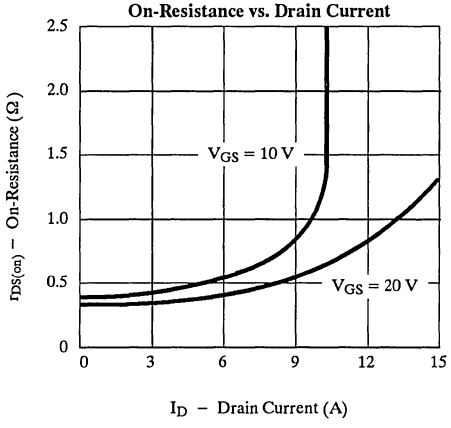
Transfer Characteristics



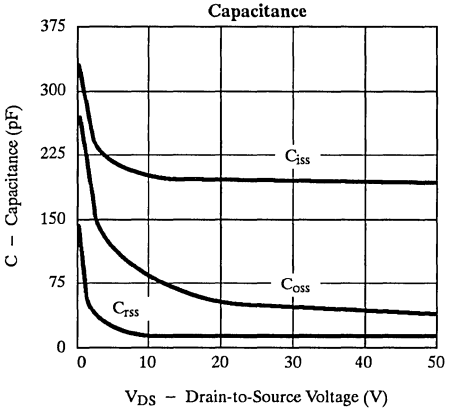
Transconductance



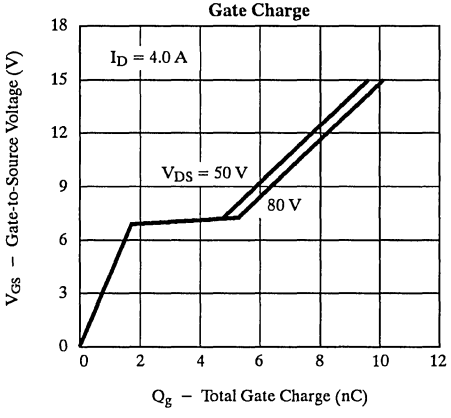
On-Resistance vs. Drain Current



Capacitance

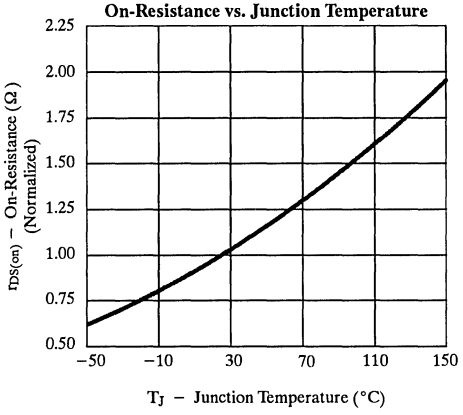


Gate Charge

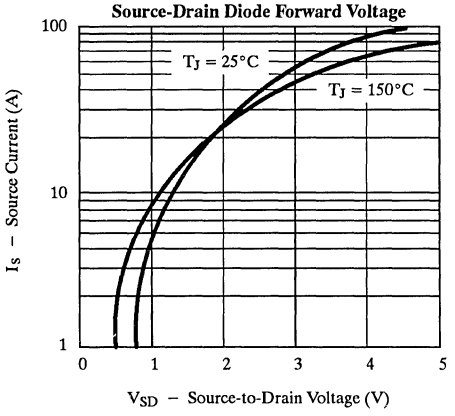


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

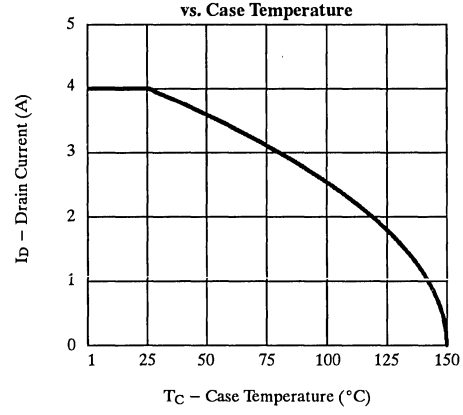


Source-Drain Diode Forward Voltage

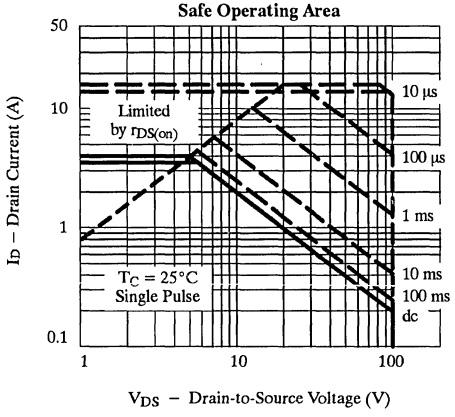


Thermal Ratings

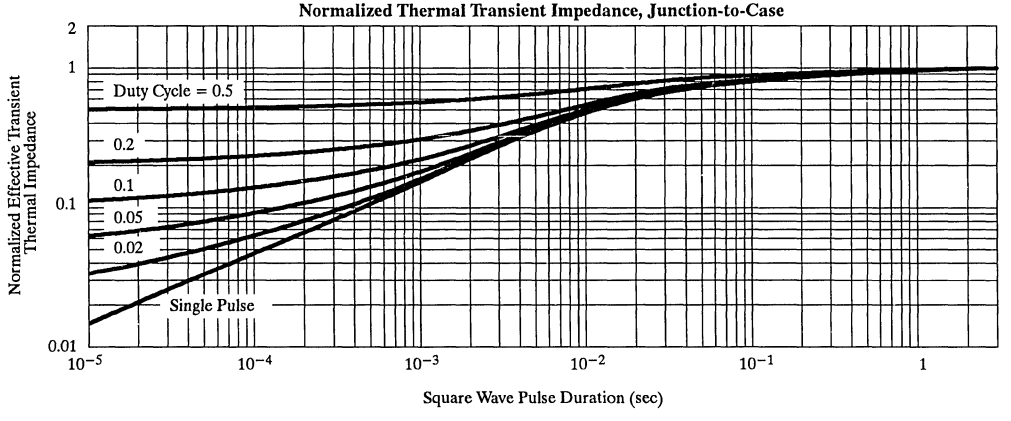
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

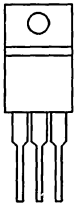
IRF520

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.3	8.0

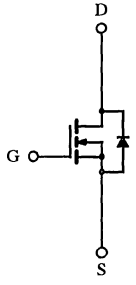
TO-220AB



G D S

Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.0	
Pulsed Drain Current		I_{DM}	32	
Avalanche Current		I_{AR}	8.0	
Repetitive Avalanche Energy[a]	L = 0 3 mH	E_{AR}	9.6	mJ
Power Dissipation	T_C = 25°C	P_D	40	W
	T_C = 100°C		16	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	C°/W
Junction-to-Case	R_{thJC}		3.12	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

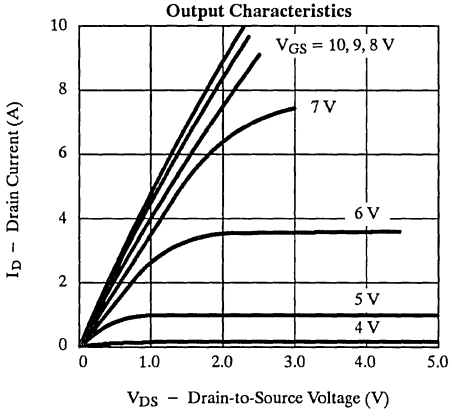
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	8.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.0 A		0.24	0.30	Ω
		V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C		0.44	0.54	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 4.0 A	1.5	2.9		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		360	600	pF
Output Capacitance	C_{oss}			120	400	
Reverse Transfer Capacitance	C_{rss}			15	100	
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 8 A		10	15	nC
Gate-Source Charge[c]	Q_{gs}			2.5		
Gate-Drain Charge[c]	Q_{gd}			5.2		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 10 Ω, I_D ≅ 4 A, V_{GEN} = 10 V, R_G = 25 Ω		7	40	ns
Rise Time[c]	t_r			30	70	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	100	
Fall Time[c]	t_f			17	70	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				8.0	A
Pulsed Current	I_{SM}				32	
Forward Voltage[b]	V_{SD}	I_F = 8 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 8 A, dI_F/dt = 100 A/µs		100		ns
Reverse Recovery Charge	Q_{rr}			0.15		µC

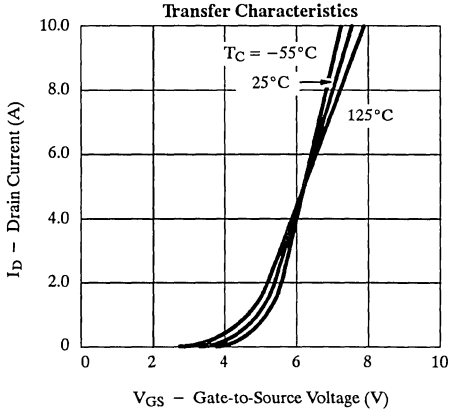
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

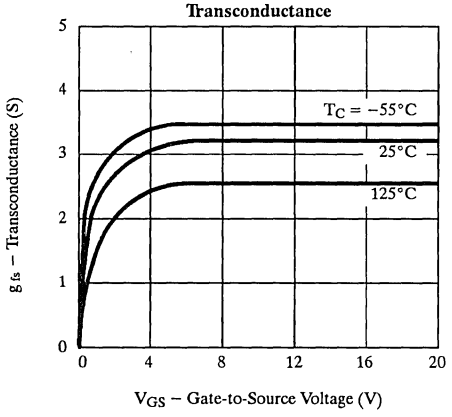
Output Characteristics



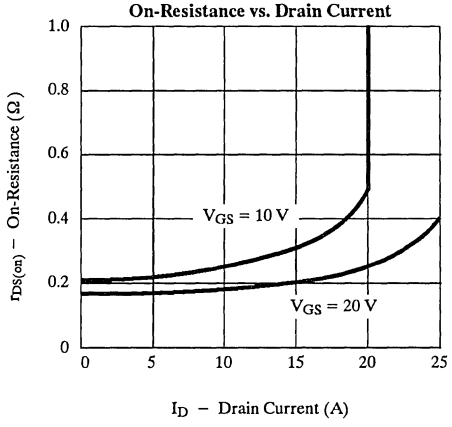
Transfer Characteristics



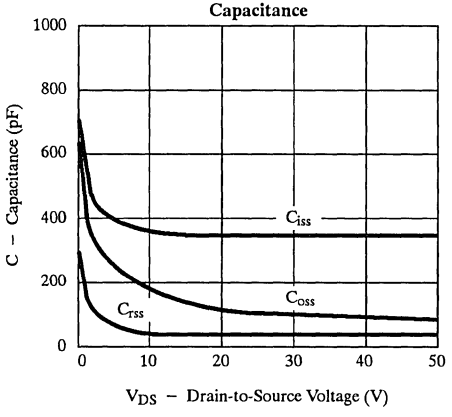
Transconductance



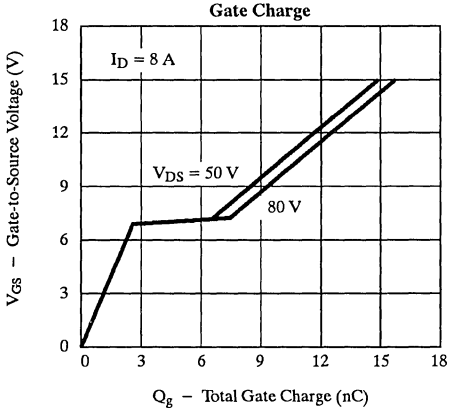
On-Resistance vs. Drain Current



Capacitance

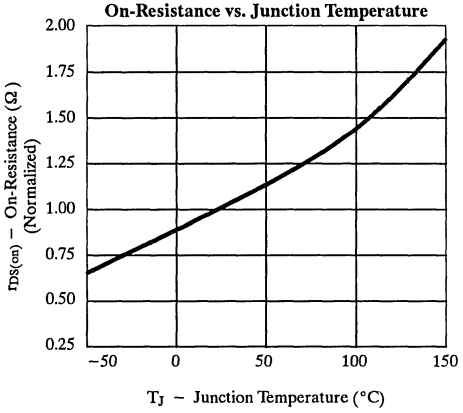


Gate Charge

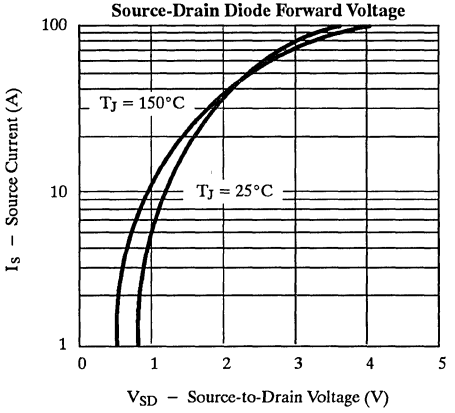


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

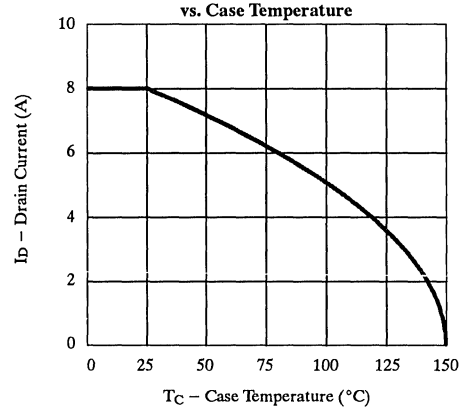


Source-Drain Diode Forward Voltage

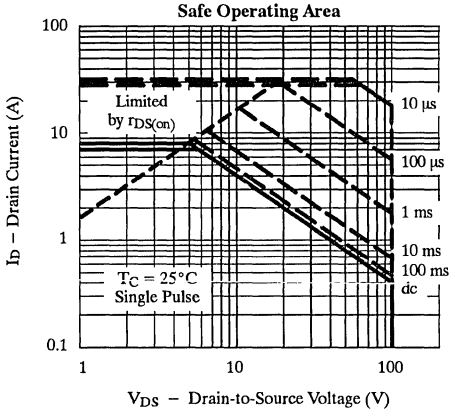


Thermal Ratings

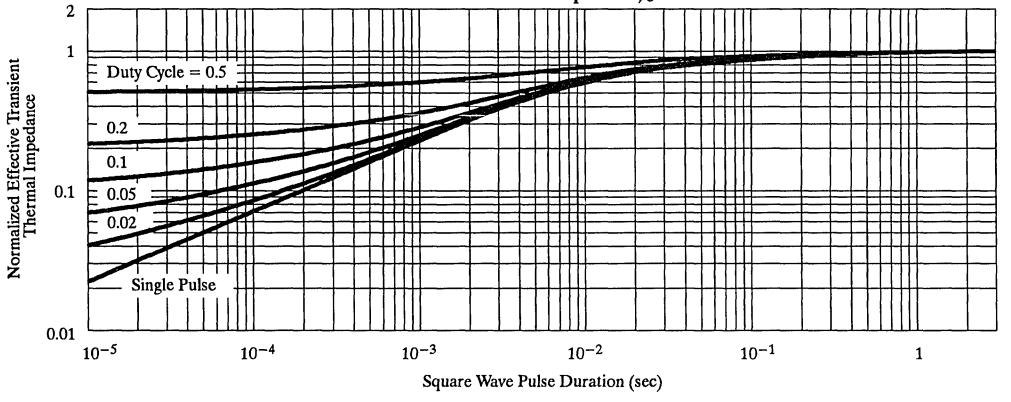
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

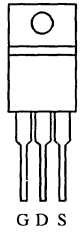
IRF530

N-Channel Enhancement-Mode Transistor

Product Summary

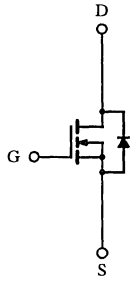
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.18	14

TO-220AB



Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		9.0	
Pulsed Drain Current		I_{DM}	56	
Avalanche Current		I_{AR}	14	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	10	mJ
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.67	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

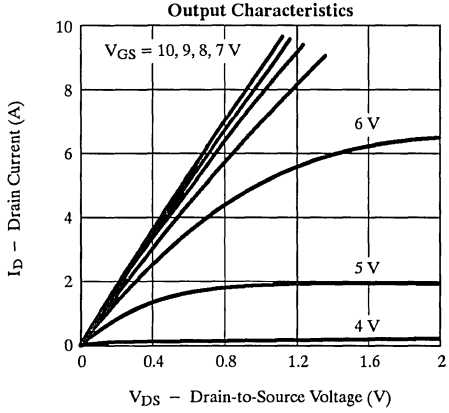
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	14			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A		0.13	0.18	Ω
		V_{GS} = 10 V, I_D = 8 A, T_J = 125°C		0.24	0.30	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 8 A	4.0			S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		700	800	pF
Output Capacitance	C_{oss}			200	500	
Reverse Transfer Capacitance	C_{rss}			40	150	
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 14 A		16	30	nC
Gate-Source Charge[c]	Q_{gs}			5		
Gate-Drain Charge[c]	Q_{gd}			7		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 25 Ω I_D ≅ 1.5 A, V_{GEN} = 10 V, R_G = 25 Ω		7	30	ns
Rise Time[c]	t_r			20	75	
Turn-Off Delay Time[c]	$t_{d(off)}$			20	40	
Fall Time[c]	t_f			10	45	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				14	A
Pulsed Current	I_{SM}				56	
Forward Voltage[b]	V_{SD}	I_F = 14 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 100 A/µs		100		ns
Reverse Recovery Charge	Q_{rr}			0.7		µC

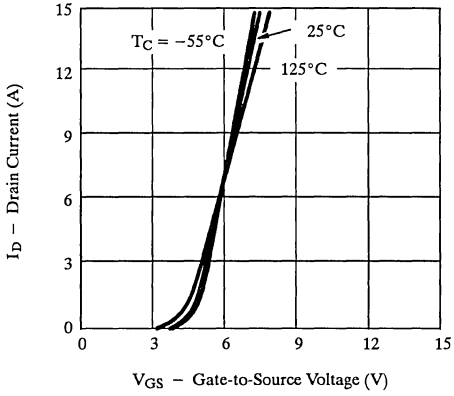
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

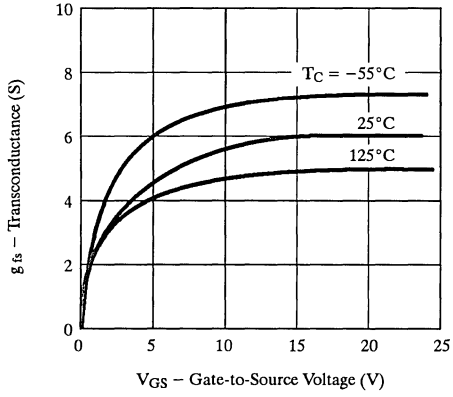
Output Characteristics



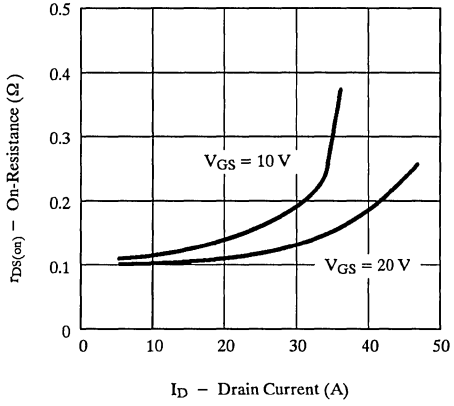
Transfer Characteristics



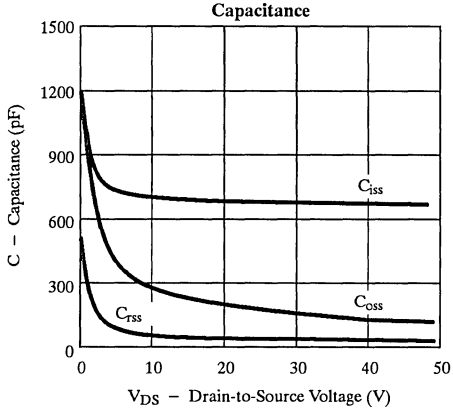
Transconductance



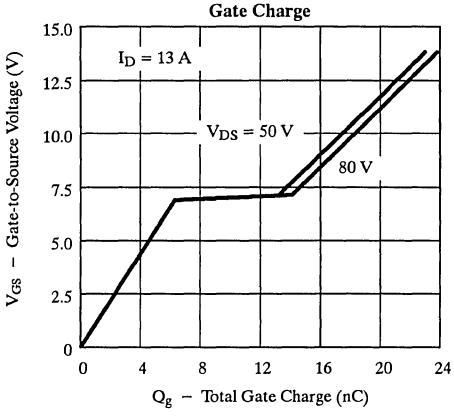
On-Resistance vs. Drain Current



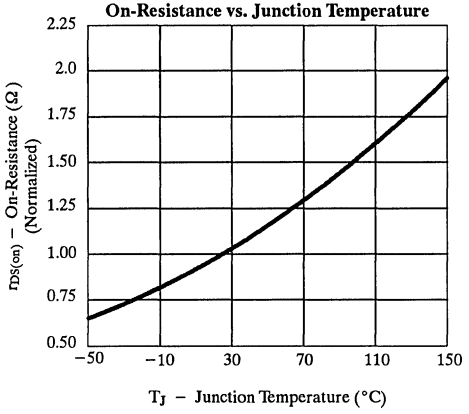
Capacitance

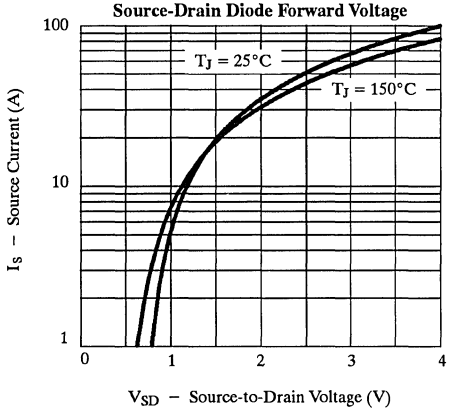


Gate Charge

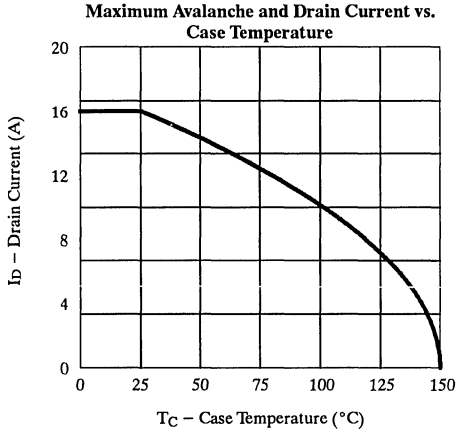


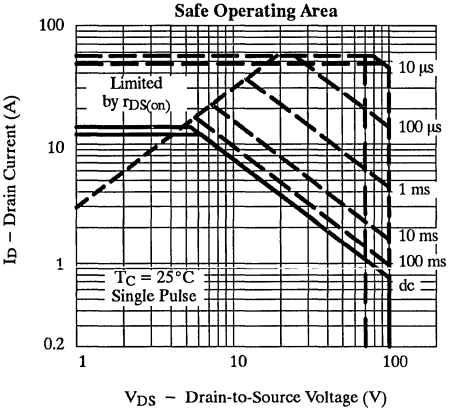
Typical Characteristics (25°C Unless Otherwise Noted)

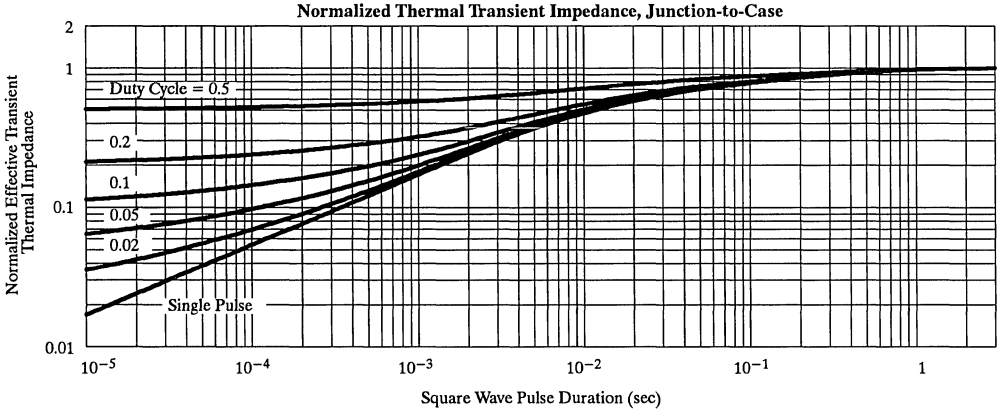




Thermal Ratings







Siliconix

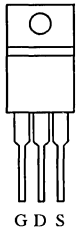
IRF540

N-Channel Enhancement Mode Transistor

Product Summary

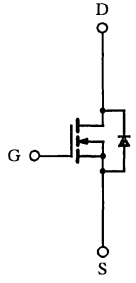
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.085	27

TO-220AB



Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	27	A
	T_C = 100°C		17	
Pulsed Drain Current		I_{DM}	108	
Avalanche Current		I_{AR}	27	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	36	mJ
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	1.0		

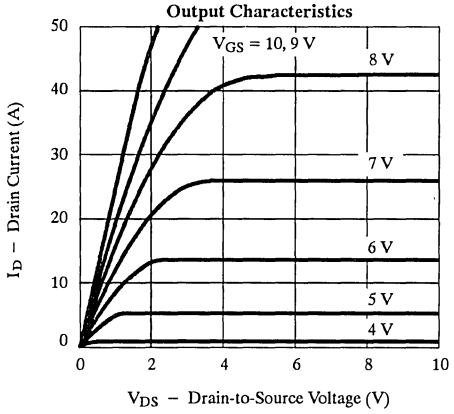
Notes:
a. Duty cycle ≤ 1%

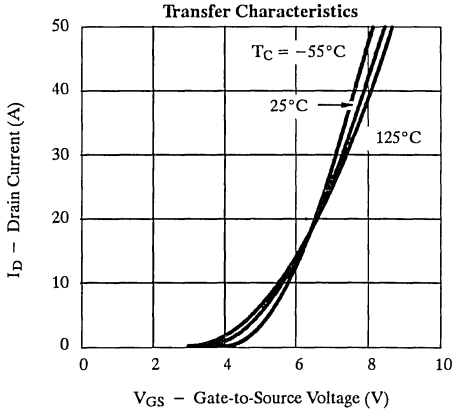
Specifications (T_J = 25°C Unless Otherwise Noted)

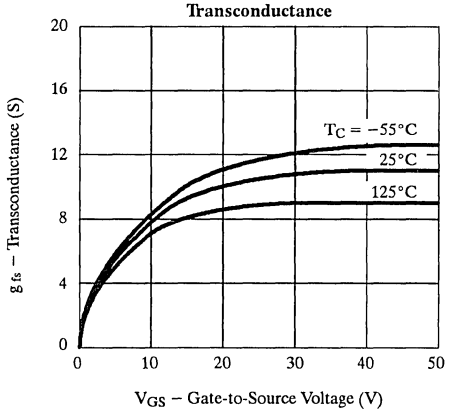
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	27			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.50	0.085	Ω
		V_{GS} = 10 V, I_D = 15 A, T_J = 125°C		0.10	0.15	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 15 A	6.0	8		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1500	1600	pF
Output Capacitance	C_{oss}			480	800	
Reverse Transfer Capacitance	C_{rss}			110	200	
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 27 A		38	60	nC
Gate-Source Charge[c]	Q_{gs}			10		
Gate-Drain Charge[c]	Q_{gd}			17		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 2 Ω, I_D ≅ 15 A, V_{GEN} = 10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			40	60	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	80	
Fall Time[c]	t_f			12	30	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				27	A
Pulsed Current	I_{SM}				108	
Forward Voltage[b]	V_{SD}	I_F = 27 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 27 A, dI_F/dt = 100 A/µs		150		ns
Reverse Recovery Charge	Q_{rr}			0.5		µC

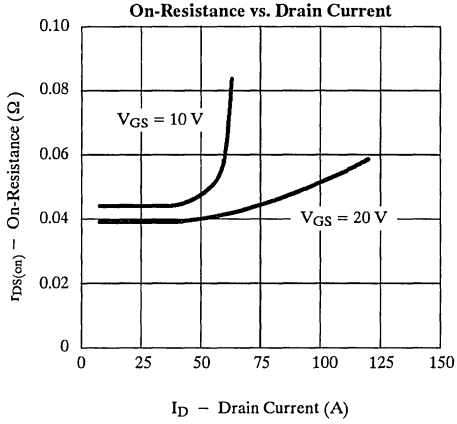
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

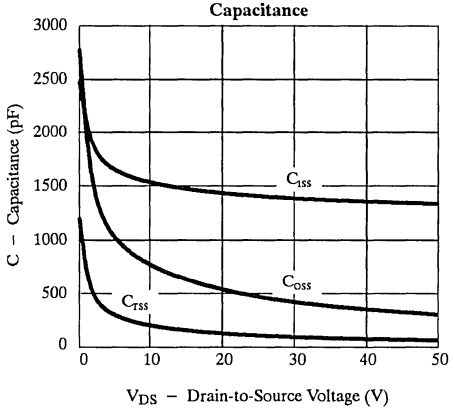
Typical Characteristics (25°C Unless Otherwise Noted)

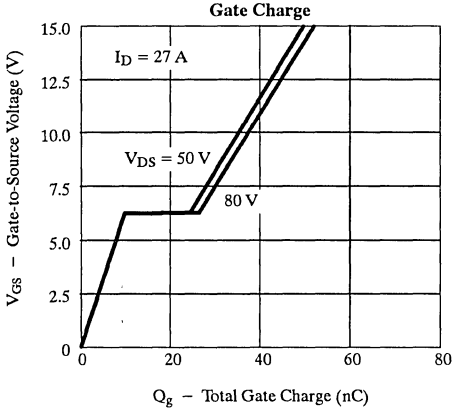






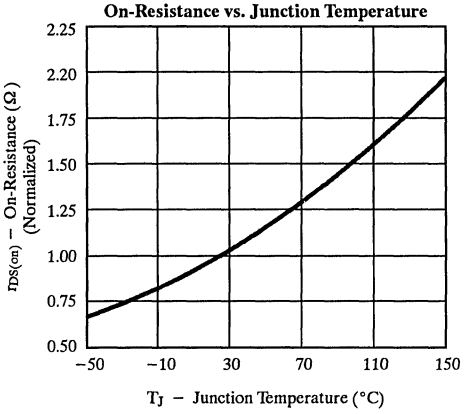




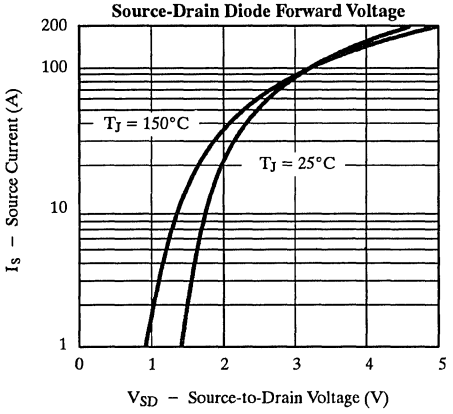


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

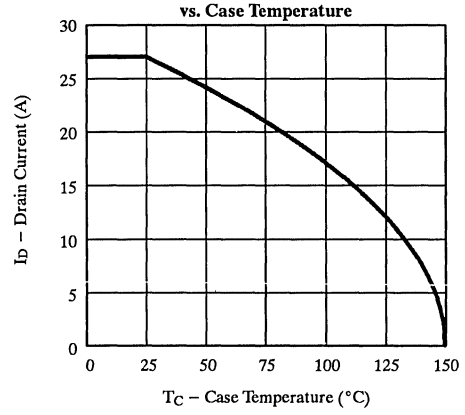


Source-Drain Diode Forward Voltage

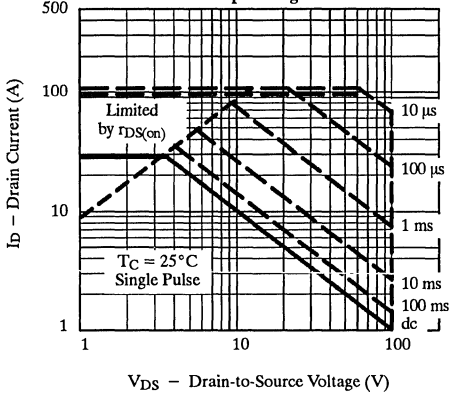


Thermal Ratings

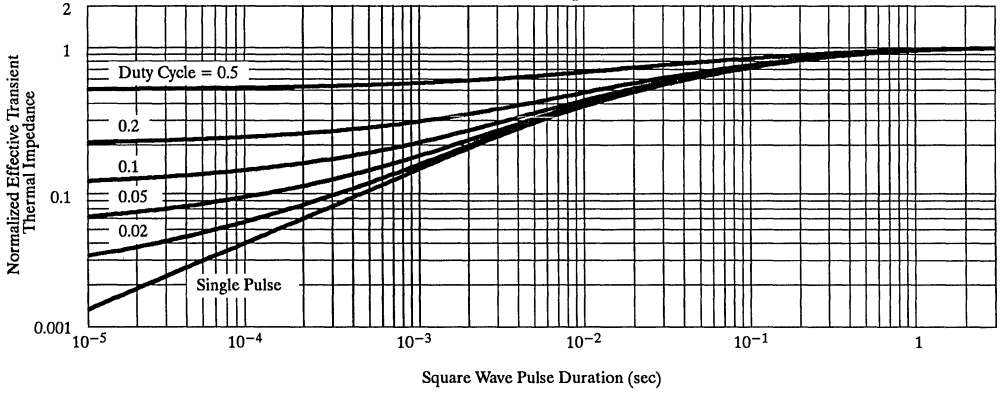
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

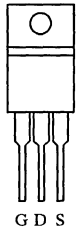
IRF9530

P-Channel Enhancement-Mode Transistor

Product Summary

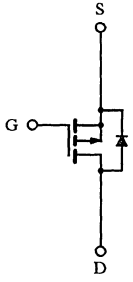
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.30	−12

TO-220AB



DRAIN connected to TAB

Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−12	A
	T_C = 100°C		−7.5	
Pulsed Drain Current		I_{DM}	−48	
Avalanche Current		I_{AR}	−12	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	7.2	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		1.67	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

Specifications (T_J = 25°C Unless Otherwise Noted)

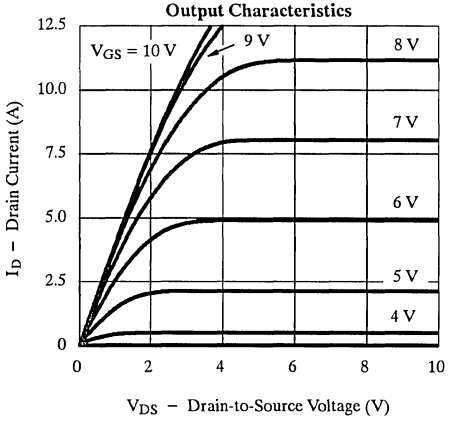
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −100 V, V_{GS} = 0 V			−250	µA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−12			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −7.5 A		0.25	0.30	Ω
		V_{GS} = −10 V, I_D = −7.5 A, T_J = 125°C		0.40	0.48	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −7.5 A	2.0	3.2		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		625	700	pF
Output Capacitance	C_{oss}			280	450	
Reverse Transfer Capacitance	C_{rss}			105	200	
Total Gate Charge[c]	Q_g	V_{DS} = −80 V, V_{GS} = −10 V, I_D = −12 A		26	45	nC
Gate-Source Charge[c]	Q_{gs}			3.4		
Gate-Drain Charge[c]	Q_{gd}			13.5		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −40 V, R_L = 3.3 Ω I_D ≅ −12 A, V_{GEN} = −10 V, R_G = 25 Ω		9	60	ns
Rise Time[c]	t_r			50	140	
Turn-Off Delay Time[c]	$t_{d(off)}$			60	140	
Fall Time[c]	t_f			40	140	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−12	A
Pulsed Current	I_{SM}				−48	
Diode Forward Voltage[b]	V_{SD}	I_F = −12 A, V_{GS} = 0 V			−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −12 A, di/dt = 100 A/µs		110		ns
Reverse Recovery Charge	Q_{rr}			0.4		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

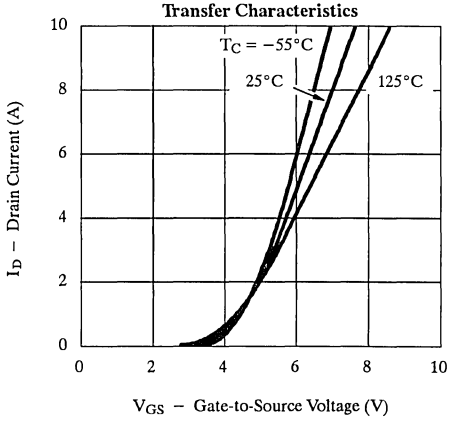
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

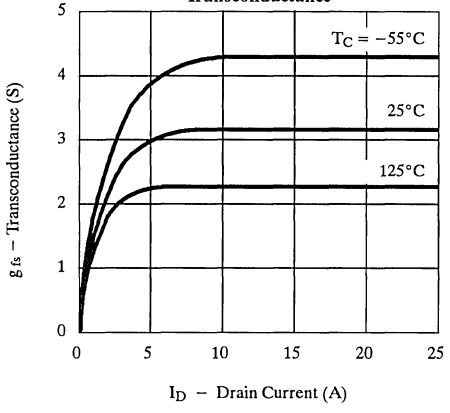
Output Characteristics



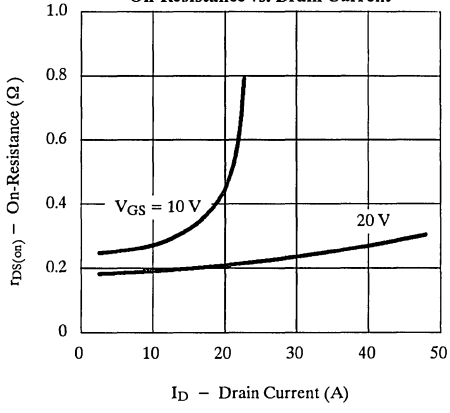
Transfer Characteristics



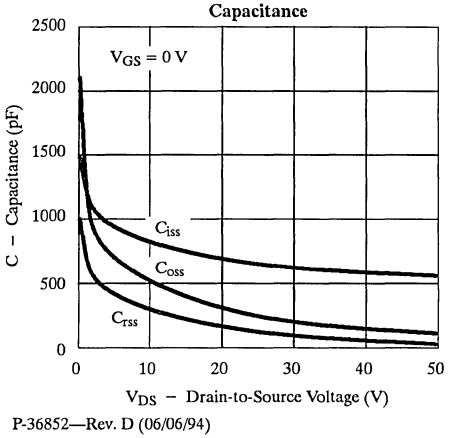
Transconductance



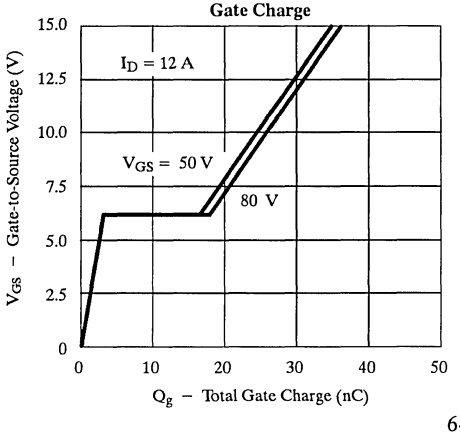
On-Resistance vs. Drain Current



Capacitance

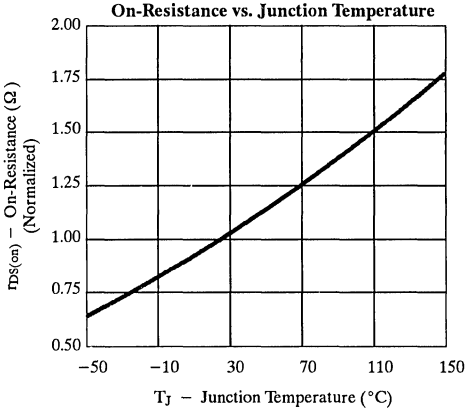


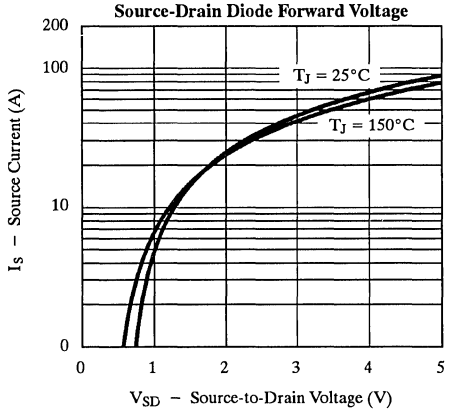
Gate Charge



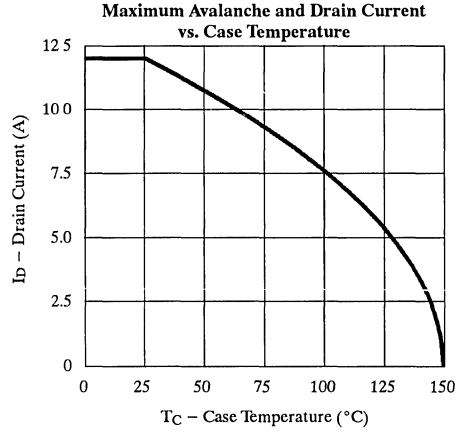
Typical Characteristics (25°C Unless Otherwise Noted)

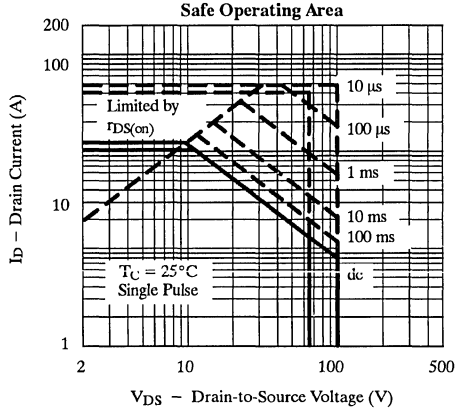
Negative signs omitted for clarity.

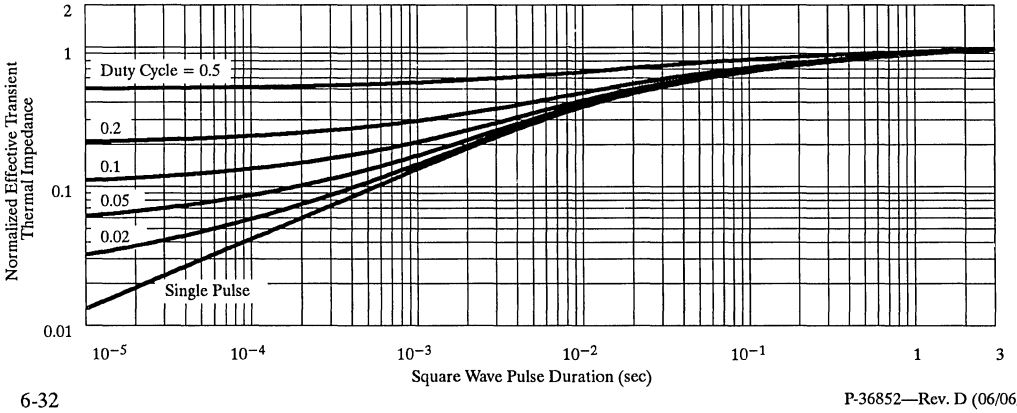




Thermal Ratings







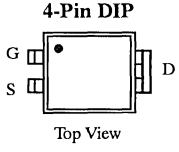
Siliconix

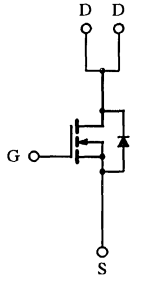
IRFD020

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.10	2.4





Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	2.4	A
	T_A = 100°C		1.5	
Pulsed Drain Current		I_{DM}	19	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.40	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	R_{thJA}	120	°C/W

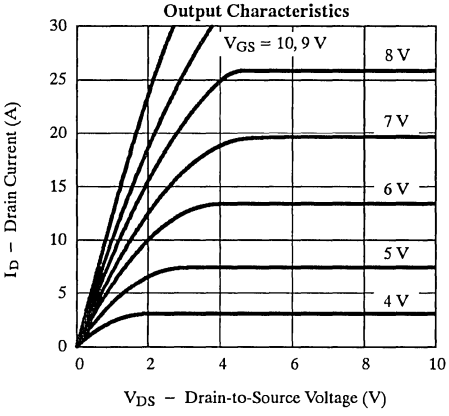
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			250	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10 V	2.4			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.4 A		0.08	0.10	Ω
		V_{GS} = 10 V, I_D = 1.4 A, T_J = 125°C		0.16	0.18	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A	4.9	5.5		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		550	850	pF
Output Capacitance	C_{oss}			300	350	
Reverse Transfer Capacitance	C_{rss}			80	100	
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 15 A		13	24	nC
Gate-Source Charge[c]	Q_{gs}			3.5		
Gate-Drain Charge[c]	Q_{gd}			5		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1.7 Ω $I_D \simeq$ 15 A, V_{GEN} = 10 V, R_G = 18 Ω		10	13	ns
Rise Time[c]	t_r			60	83	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	40	
Fall Time[c]	t_f			35	50	
Source-Drain Diode Ratings and Characteristics (T_A = 25°C)						
Continuous Current	I_S				2.4	A
Pulsed Current	I_{SM}				19	
Forward Voltage[b]	V_{SD}	I_F = 2.4 A, V_{GS} = 0 V			1.25	V
Reverse Recovery Time	t_{rr}	I_F = 2.4 A, dI_F/dt = 100 A/µs		65		ns
Reverse Recovery Charge	Q_{rr}			0.16	0.85	µC

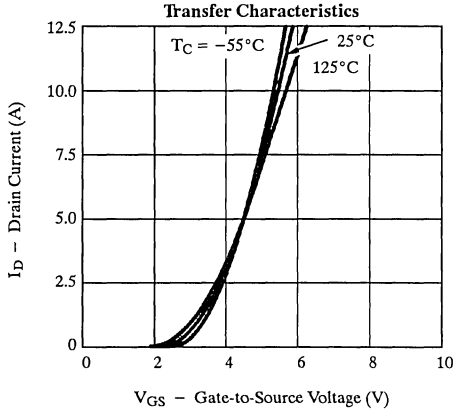
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

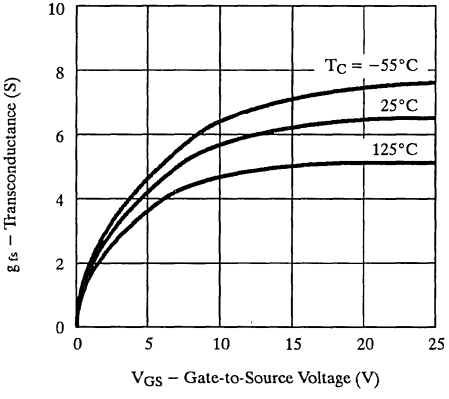
Output Characteristics



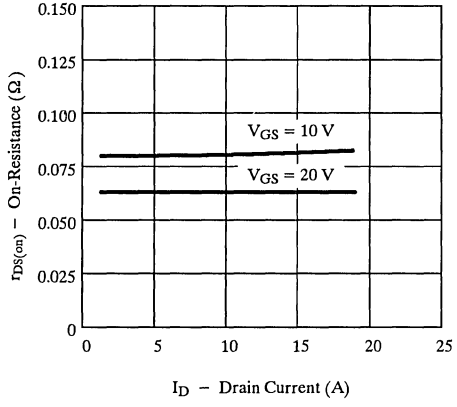
Transfer Characteristics



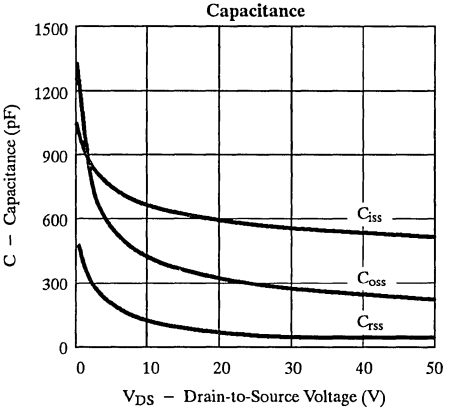
Transconductance



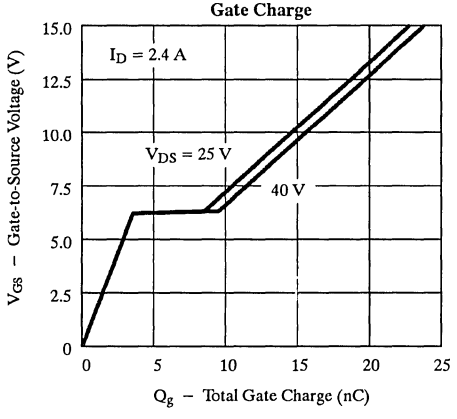
On-Resistance vs. Drain Current



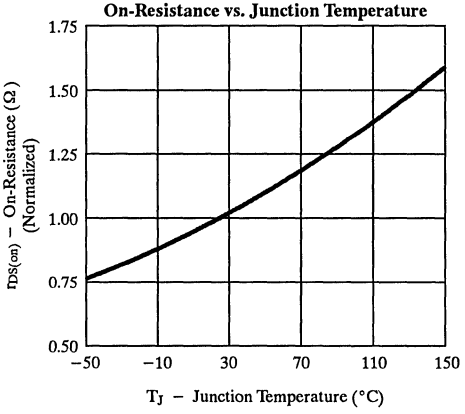
Capacitance

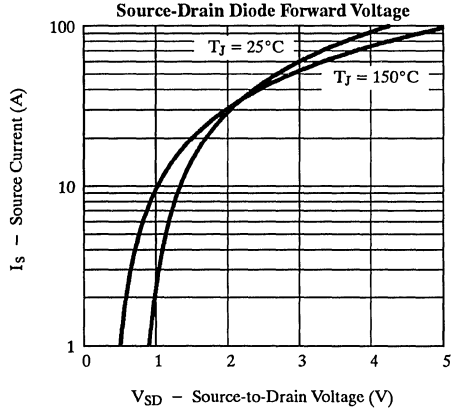


Gate Charge

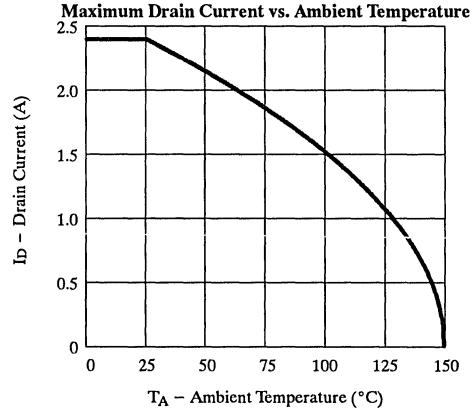


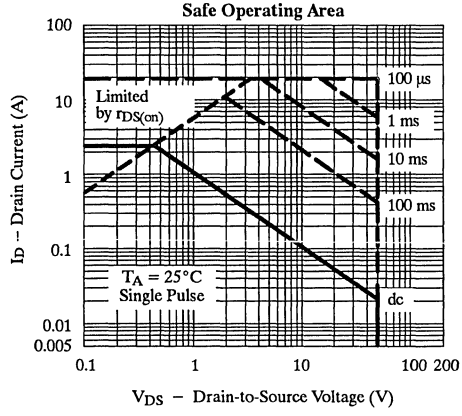
Typical Characteristics (25°C Unless Otherwise Noted)





Thermal Ratings





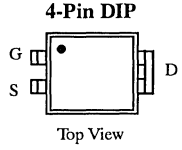
Siliconix

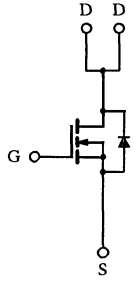
IRFD110

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.60	1.0





N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	1.0	A
	T_A = 100°C		0.6	
Pulsed Drain Current		I_{DM}	8.0	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

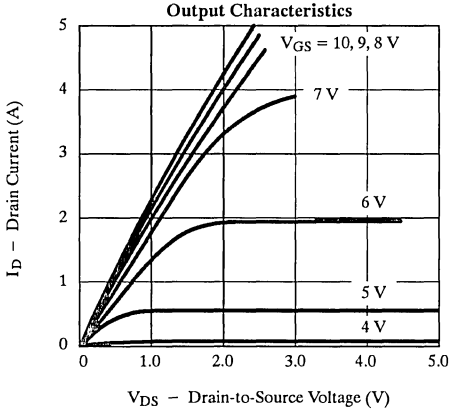
Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	R_{thJA}	120	°C/W

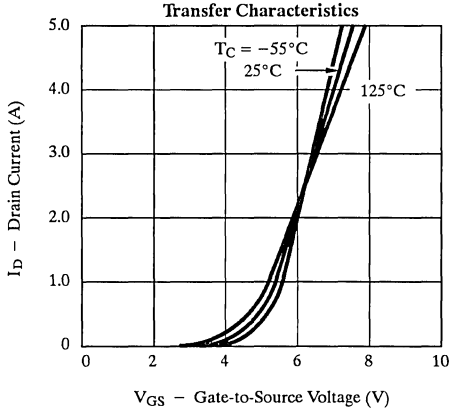
Specifications (T_J = 25°C Unless Otherwise Noted)

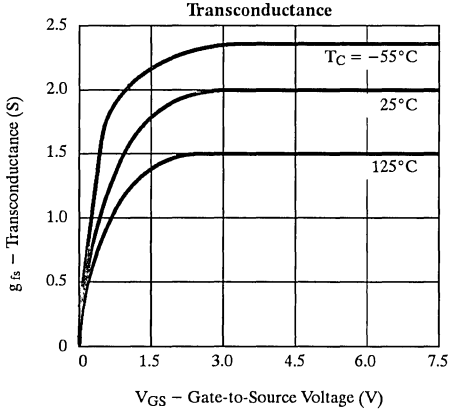
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.00			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.8 A		0.5	0.60	Ω
		V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C		0.8	1.0	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 0.8 A	0.8	1.5		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		180	200	pF
Output Capacitance	C_{oss}			60	100	
Reverse Transfer Capacitance	C_{rss}			10	25	
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 1 A		6	7.0	nC
Gate-Source Charge[c]	Q_{gs}			1.5		
Gate-Drain Charge[c]	Q_{gd}			3.0		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 40 V, R_L = 50 Ω $I_D \simeq$ 0.8 A, V_{GEN} = 10 V, R_G = 25 Ω		7	20	ns
Rise Time[c]	t_r			10	25	
Turn-Off Delay Time[c]	$t_{d(off)}$			13	25	
Fall Time[c]	t_f			9	20	
Source-Drain Diode Ratings and Characteristics (T_A = 25°C)						
Continuous Current	I_S				1.0	A
Pulsed Current	I_{SM}				8.0	
Forward Voltage[b]	V_{SD}	I_F = 1.0 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 1.0 A, dI_F/dt = 100 A/µs		45		ns
Reverse Recovery Charge	Q_{rr}			0.25		µC

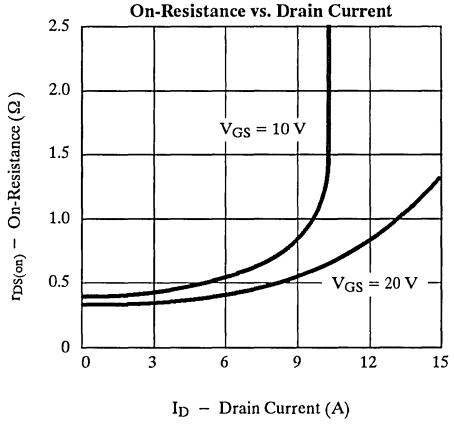
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

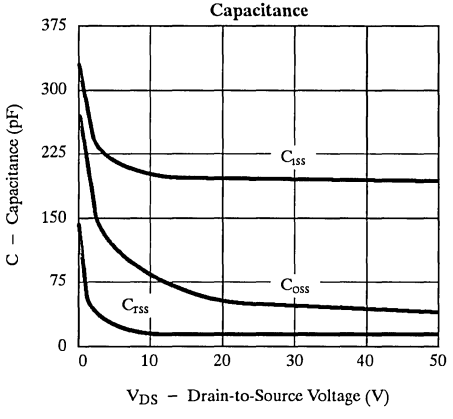
Typical Characteristics (25°C Unless Otherwise Noted)

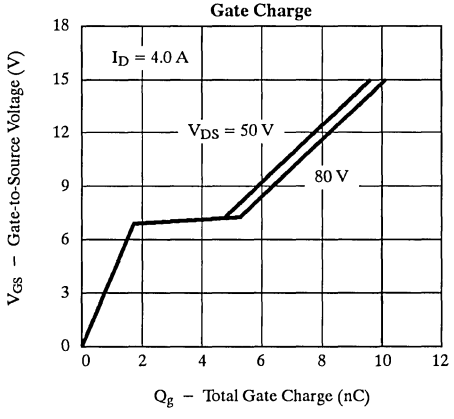




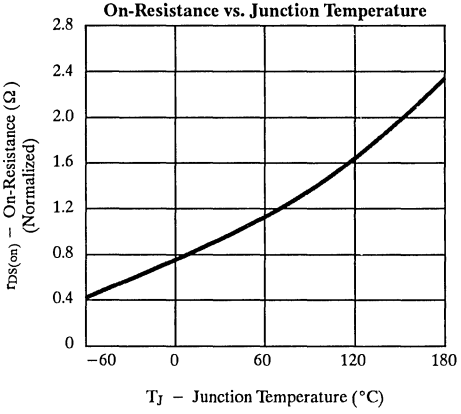


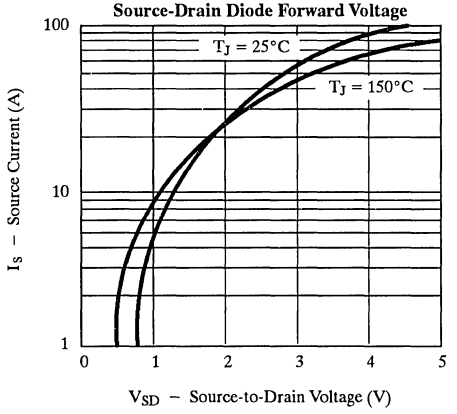




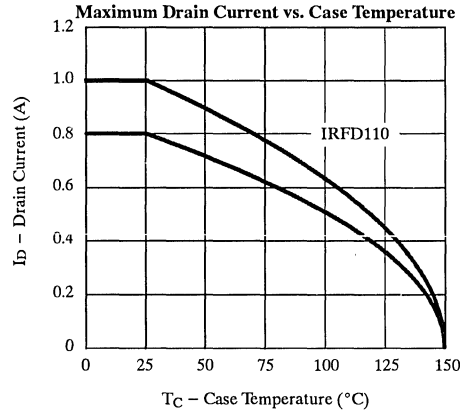


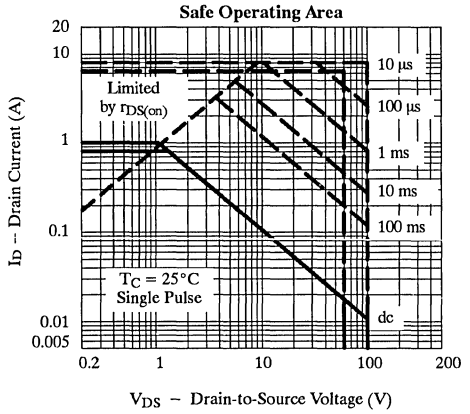
Typical Characteristics (25°C Unless Otherwise Noted)





Thermal Ratings





Siliconix

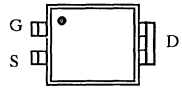
IRFD120/123

N-Channel Enhancement-Mode Transistors

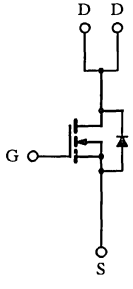
Product Summary

Part Number	$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
IRFD120	100	0.3	1.3
IRFD123	60	0.4	1.1

4-Pin DIP



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	IRFD120	IRFD123	Unit
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	1.3	1.1	A
	T_A = 100°C		0.8	0.7	
Pulsed Drain Current		I_{DM}	5.2	4.4	
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

Thermal Resistance Ratings

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	R_{thJA}	120	°C/W

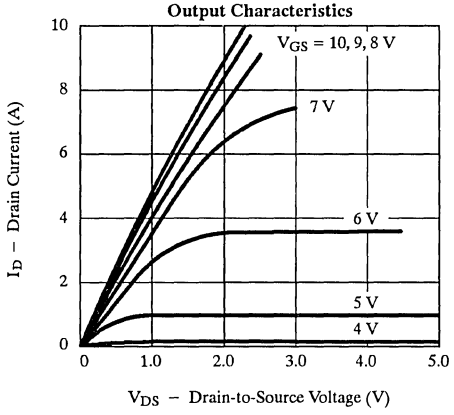
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	IRFD120	100			V
			IRFD123	60			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	IRFD120	1.3			A
			IRFD123	1.1			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.6 A	IRFD120		0.22	0.30	Ω
			IRFD123		0.30	0.40	
		V_{GS} = 10 V, I_D = 0.6 A, T_J = 125°C	IRFD120		0.4	0.60	
			IRFD123		0.6	0.80	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 0.6 A			1.6		S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz			360		pF
Output Capacitance	C_{oss}				120		
Reverse Transfer Capacitance	C_{rss}				15		
Total Gate Charge[c]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.3 A			10	15	nC
Gate-Source Charge[c]	Q_{gs}				2.4		
Gate-Drain Charge[c]	Q_{gd}				5.1		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 80 Ω I_D ≃ 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω			7	40	ns
Rise Time[c]	t_r				20	70	
Turn-Off Delay Time[c]	$t_{d(off)}$				20	100	
Fall Time[c]	t_f				10	70	
Source-Drain Diode Ratings and Characteristics (T_A = 25°C)							
Continuous Current	I_S		IRFD120			1.3	A
			IRFD123			1.1	
Pulsed Current	I_{SM}		IRFD120			5.2	
			IRFD123			4.4	
Forward Voltage[b]	V_{SD}	I_F = I_S, V_{GS} = 0 V	IRFD120			2.5	V
			IRFD123			2.3	
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs			100		ns
Reverse Recovery Charge	Q_{rr}				0.15		µC

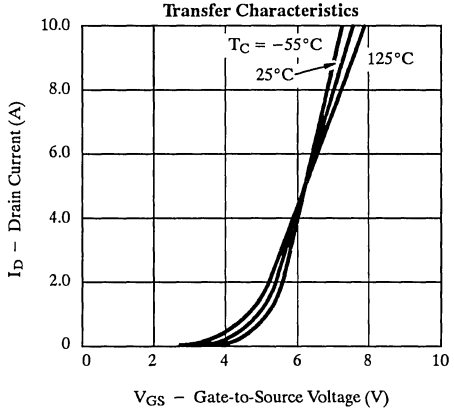
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

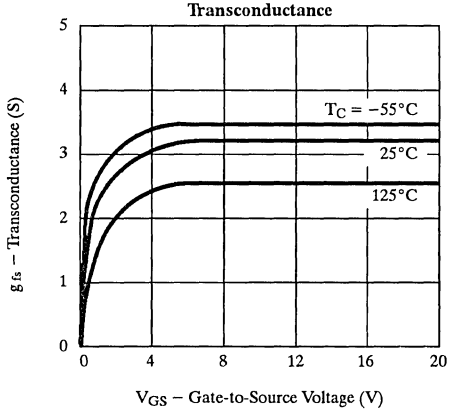
Output Characteristics



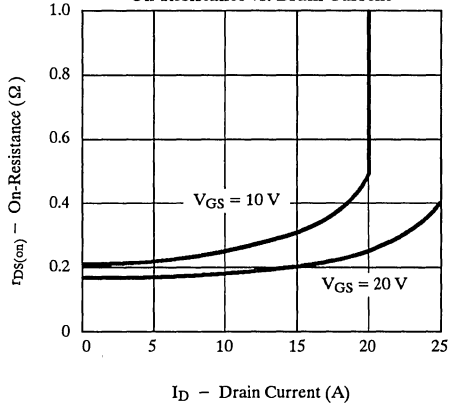
Transfer Characteristics



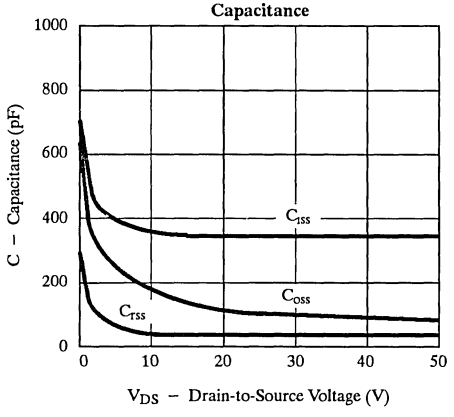
Transconductance



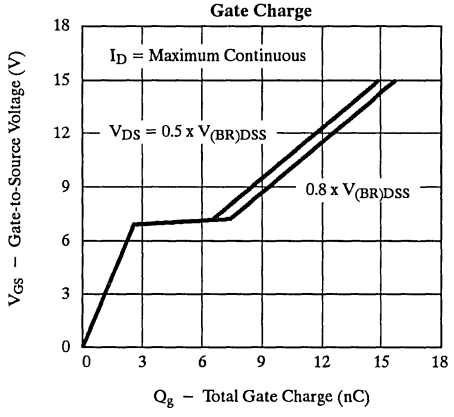
On-Resistance vs. Drain Current



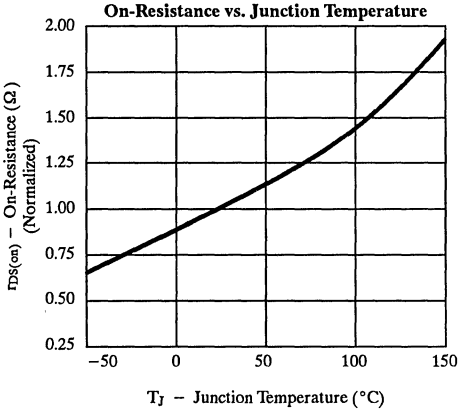
Capacitance

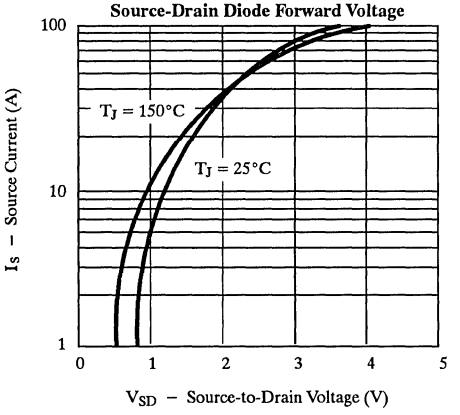


Gate Charge

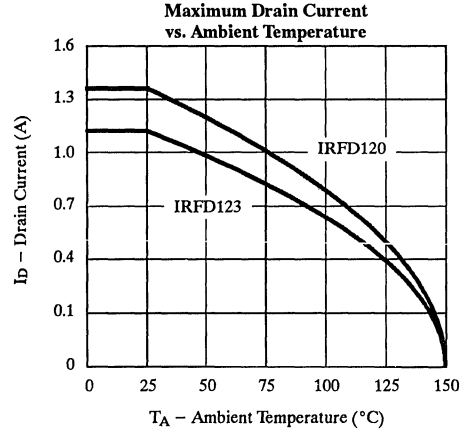


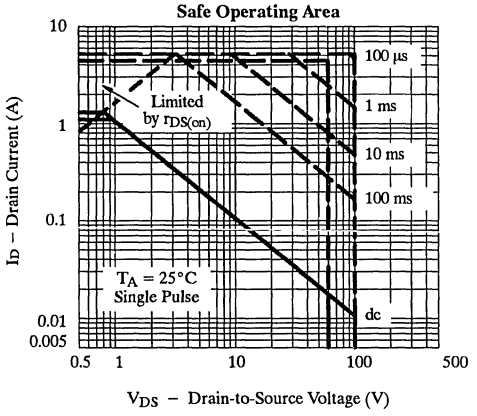
Typical Characteristics (25°C Unless Otherwise Noted)





Thermal Ratings





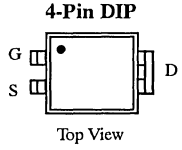
Siliconix

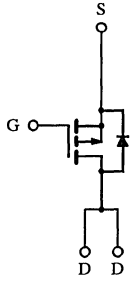
IRFD9020

P-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−50	0.28	−1.6





P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	−1.6	A
	T_A = 100°C		−1.0	
Pulsed Drain Current		I_{DM}	−13	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.40	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	R_{thJA}	120	°C/W

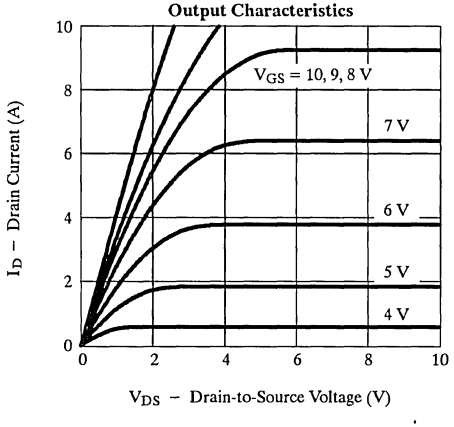
Specifications (T_J = 25°C Unless Otherwise Noted)

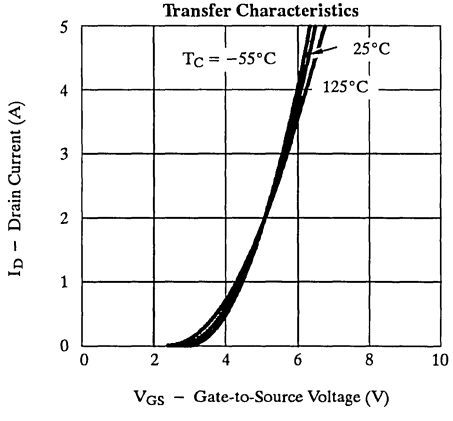
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −50 V, V_{GS} = 0 V			−250	µA
		V_{DS} = −40 V, V_{GS} = 0 V, T_J = 125°C			−1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −2 V, V_{GS} = −10 V	−1.6			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −1.1 A		0.24	0.28	Ω
		V_{GS} = −10 V, I_D = −1.1 A, T_J = 125°C		0.40	0.50	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −1.1 A	1.0	1.4		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		530	600	pF
Output Capacitance	C_{oss}			325	350	
Reverse Transfer Capacitance	C_{rss}			85	100	
Total Gate Charge[c]	Q_g	V_{DS} = −25 V, V_{GS} = −10 V, I_D = −1.6 A		16	26	nC
Gate-Source Charge[c]	Q_{gs}			2.8		
Gate-Drain Charge[c]	Q_{gd}			5.0		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −25 V, R_L = 15 Ω $I_D \simeq$ −1.6 A, V_{GEN} = −10 V, R_G = 18 Ω		10	12	ns
Rise Time[c]	t_r			80	86	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	35	
Fall Time[c]	t_f			50	60	
Source-Drain Diode Ratings And Characteristics (T_A = 25°C)						
Continuous Current	I_S				−1.6	A
Pulsed Current	I_{SM}				−13	
Forward Voltage[b]	V_{SD}	I_F = −1.6 A, V_{GS} = 0 V			−6.3	V
Reverse Recovery Time	t_{rr}	I_F = −1.6 A, dI_F/dt = 100 A/µs		70		ns
Reverse Recovery Charge	Q_{rr}			0.15		µC

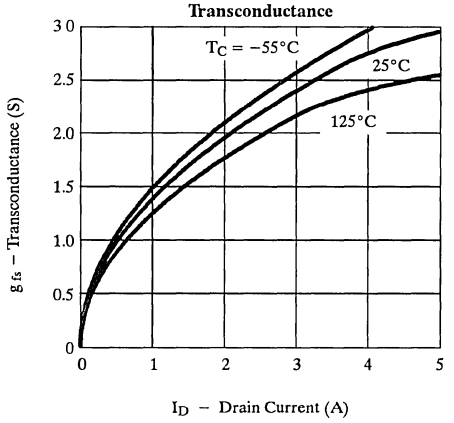
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

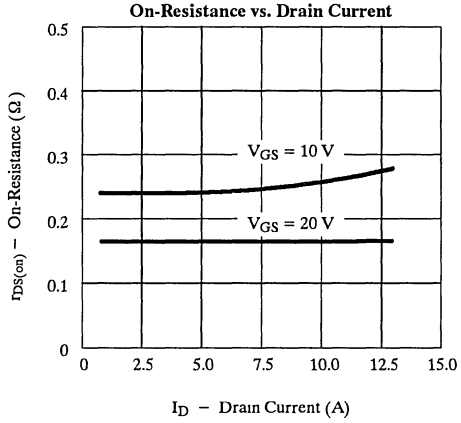
Typical Characteristics (25°C Unless Otherwise Noted)

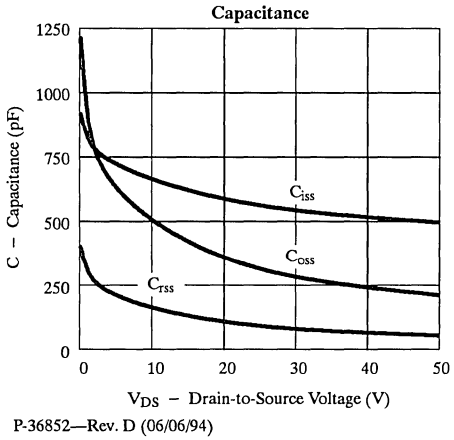
Negative signs omitted for clarity.

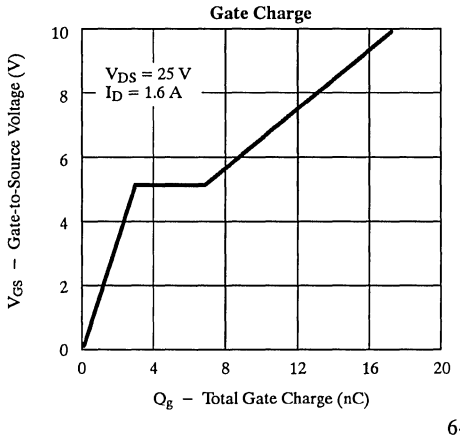






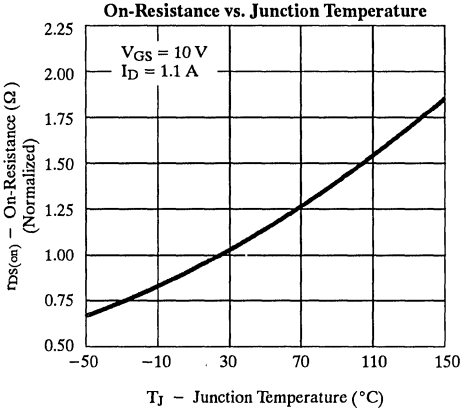


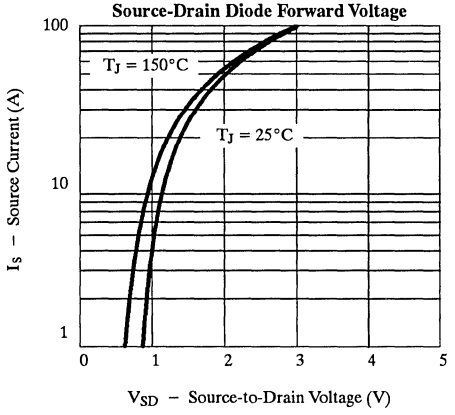




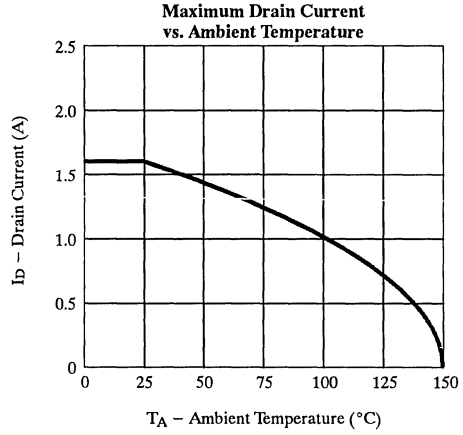
Typical Characteristics (25°C Unless Otherwise Noted)

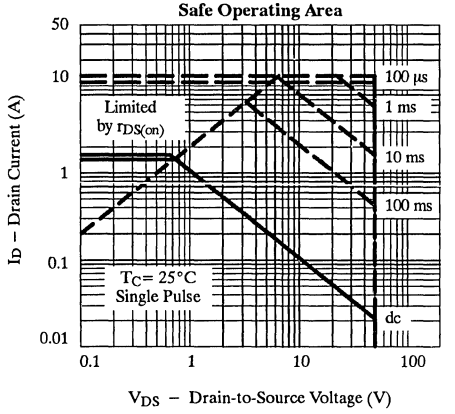
Negative signs omitted for clarity.





Thermal Ratings





Siliconix

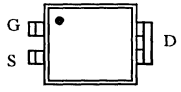
IRFD9120/9123

P-Channel Enhancement-Mode Transistors

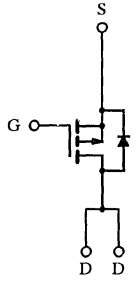
Product Summary

Part Number	$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
IRFD9120	−100	0.60	−1.0
IRFD9123	−60	0.80	−0.8

4-Pin DIP



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	IRFD9120	IRFD9123	Unit
Drain-Source Voltage		V_{DS}	−100	−60	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	−1.0	−0.8	A
	T_A = 100°C		−0.6	−0.5	
Pulsed Drain Current		I_{DM}	−8.0	−6.4	
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

Thermal Resistance Ratings

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	R_{thJA}	120	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

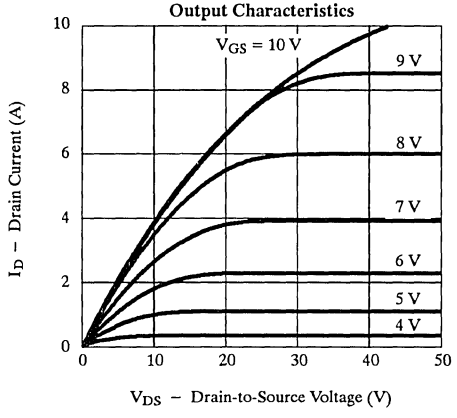
Parameter	Symbol	Test Condition		Min	Typ[a]	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	IRFD9120	−100			V
			IRFD9123	−60			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA		−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				−250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				−1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	IRFD9120	−1.0			A
			IRFD9123	−0.8			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −0.8 A	IRFD9120		0.50	0.60	Ω
			IRFD9123		0.60	0.80	
		V_{GS} = −10 V, I_D = −0.8 A, T_J = 125°C	IRFD9120		0.80	1.0	
			IRFD9123		1.00	1.4	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −0.8 A		0.8	1.0		S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz			350	450	pF
Output Capacitance	C_{oss}				205	350	
Reverse Transfer Capacitance	C_{rss}				80	100	
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = 10 V, I_D = −4 A			9	20	nC
Gate-Source Charge[c]	Q_{gs}				1.8		
Gate-Drain Charge[c]	Q_{gd}				5.6		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 62 Ω, $I_D \simeq$ −0.8 A, V_{GEN} = −10 V, R_G = 25 Ω			9	50	ns
Rise Time[c]	t_r				25	100	
Turn-Off Delay Time[c]	$t_{d(off)}$				30	100	
Fall Time[c]	t_f				30	100	
Source-Drain Diode Ratings and Characteristics (T_A = 25°C)							
Continuous Current	I_S		IRFD9120			−1.0	A
			IRFD9123			−0.8	
Pulsed Current	I_{SM}		IRFD9120			−8.0	
			IRFD9123			−6.4	
Forward Voltage[b]	V_{SD}	I_F = I_S, V_{GS} = 0 V	IRFD9120			−6.3	V
			IRFD9123			−6.0	
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs			80		ns
Reverse Recovery Charge	Q_{rr}				0.18		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

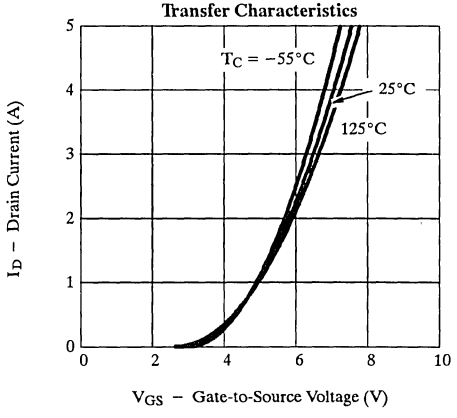
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

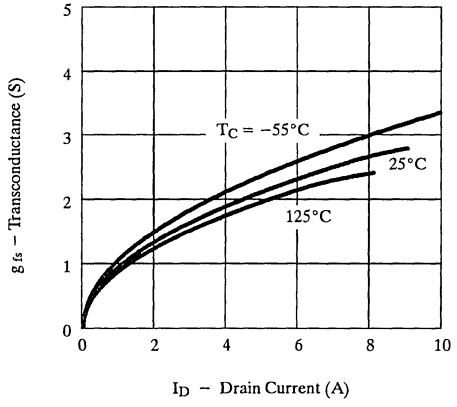
Output Characteristics



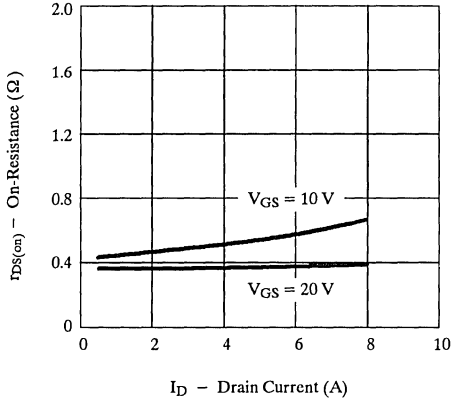
Transfer Characteristics



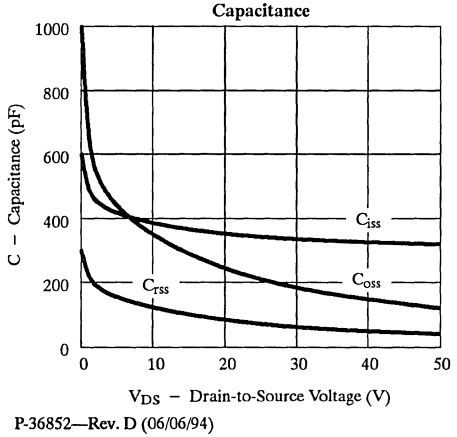
Transconductance



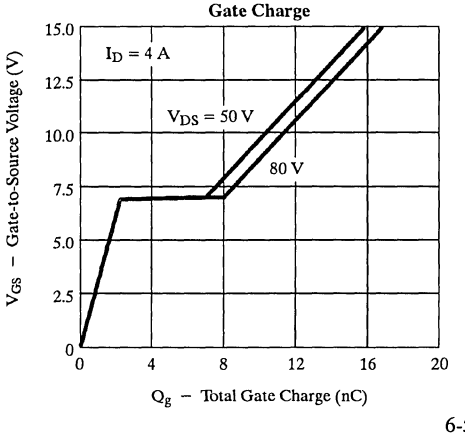
On-Resistance vs. Drain Current



Capacitance

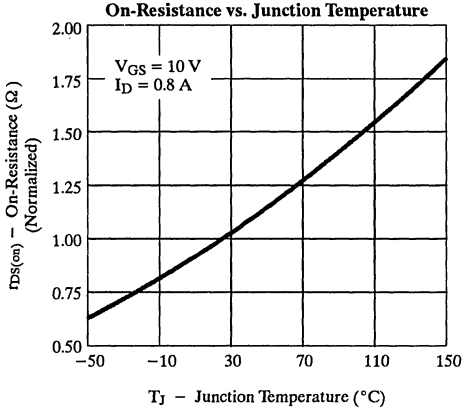


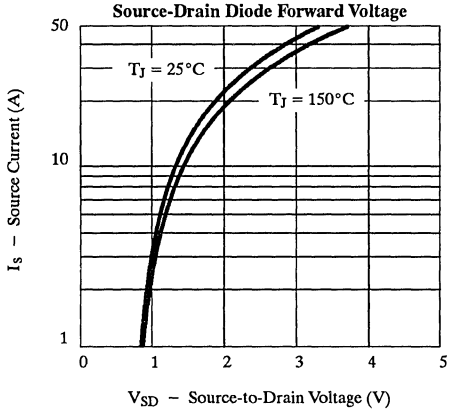
Gate Charge



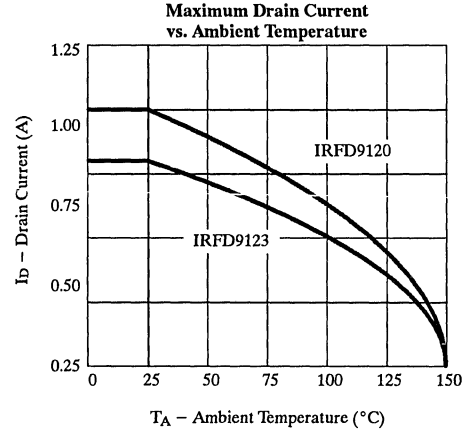
Typical Characteristics (25°C Unless Otherwise Noted)

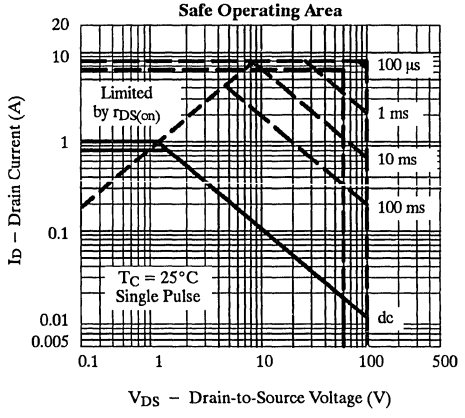
Negative signs omitted for clarity.





Thermal Ratings





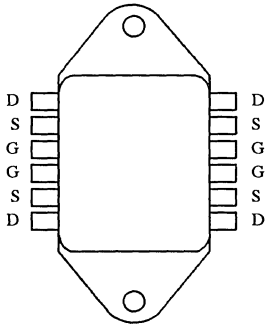
Siliconix

MOD100B/100C

Four N-Channel Enhancement-Mode Transistors

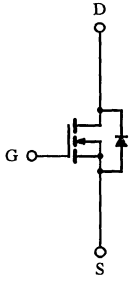
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.08	21



Leadform Options

MOD100B . . . Bent Down
MOD100C . . . Bent Up



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Single Die	All Die	Unit
Drain-Source Voltage		V_{DS}	100	100	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	21	84	A
	T_C = 100°C		21	70	
Pulsed Drain Current		I_{DM}	125	440	
Avalanche Current (See Thermal Ratings)		I_A	21		
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Isolation Voltage		V_{ISOL}	1000		V

Thermal Resistance Ratings

Parameter	Symbol	Typical	Single Die	All Die	Unit
Maximum Junction-to-Ambient	R_{thJA}		30	30	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	0.31	
Case-to-Sink	R_{thCS}	0.1			

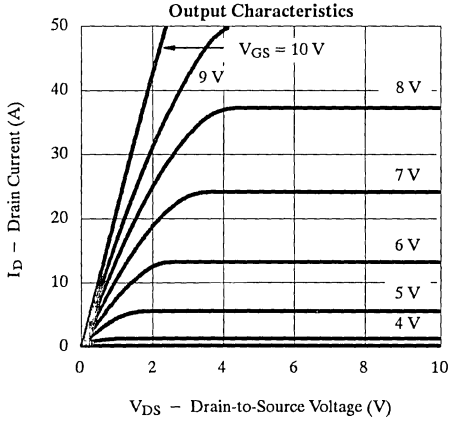
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 mA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			250	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	21			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.070	0.08	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125°C		0.100	0.120	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	9.0	11.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2800		pF
Output Capacitance	C_{oss}			1100		
Reverse Transfer Capacitance	C_{rss}			400		
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 21 A		90	125	nC
Gate-Source Charge	Q_{gs}			18	22	
Gate-Drain Charge	Q_{gd}			30	65	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 24 V, R_L = 1.2 Ω I_D ≅ 20 A, V_{GEN} = 10 V, R_G = 4.7 Ω		15	35	ns
Rise Time	t_r			30	100	
Turn-Off Delay Time	$t_{d(off)}$			50	125	
Fall Time	t_f			20	100	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				21	A
Pulsed Current	I_{SM}				125	
Diode Forward Voltage[a]	V_{SD}	I_F = 21 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F =21A, di/dt = 100 A/µs		150		ns
Reverse Recovery Charge	Q_{rr}			0.5		µC

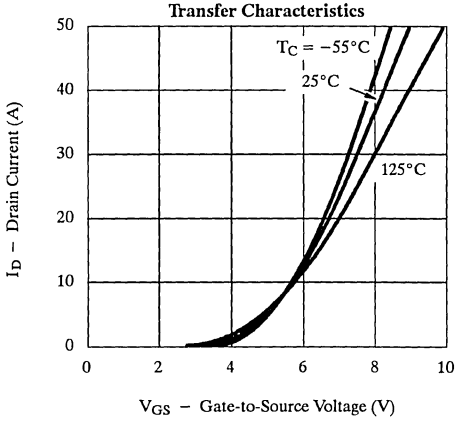
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

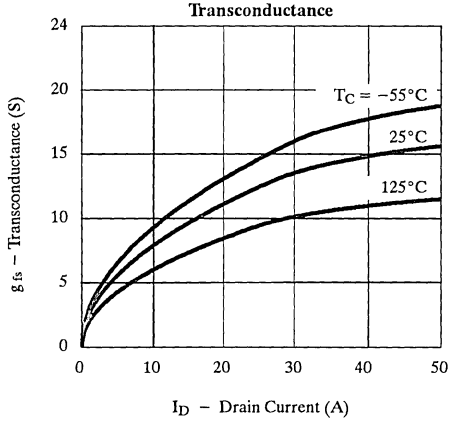
Output Characteristics



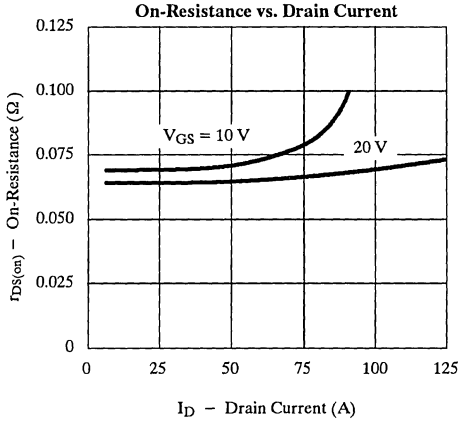
Transfer Characteristics



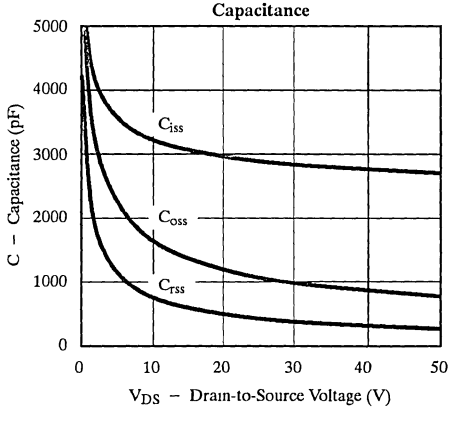
Transconductance



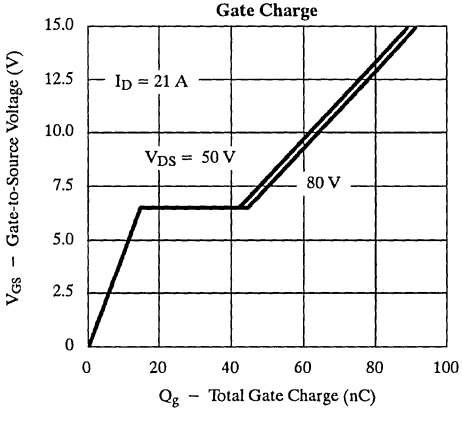
On-Resistance vs. Drain Current



Capacitance

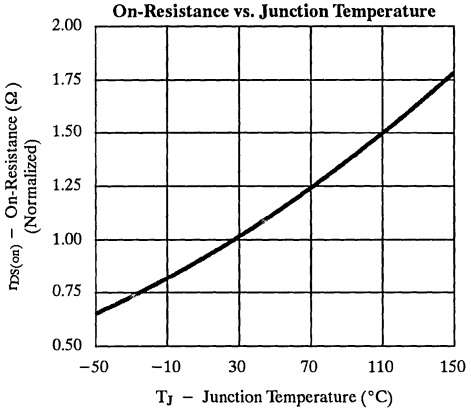


Gate Charge

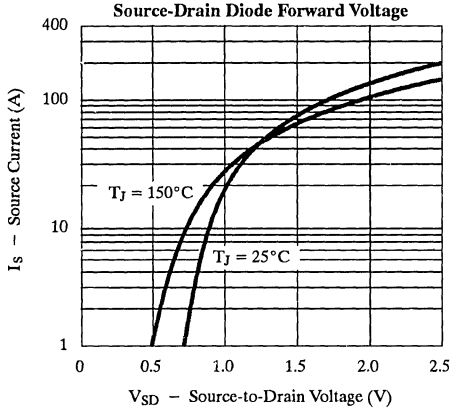


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

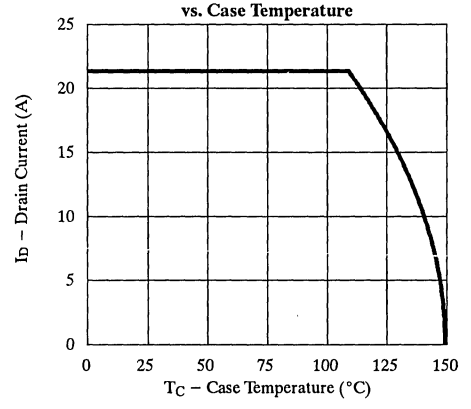


Source-Drain Diode Forward Voltage

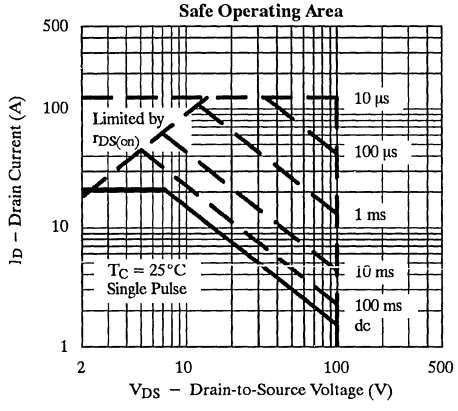


Thermal Ratings

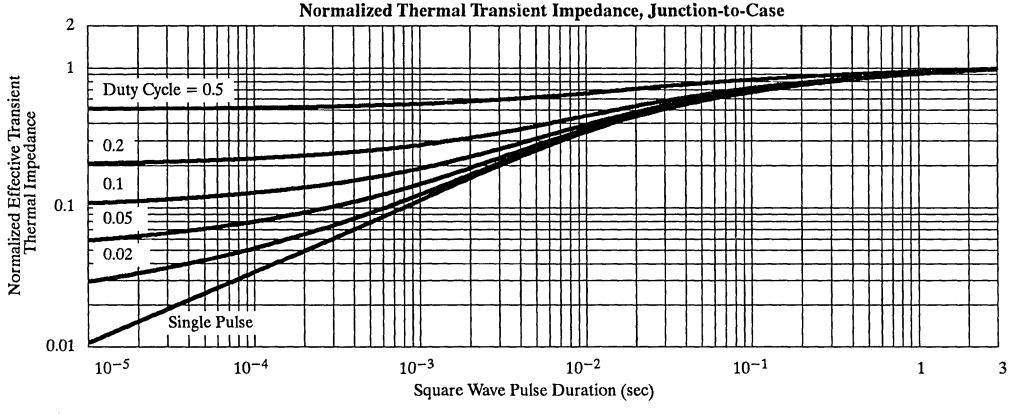
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



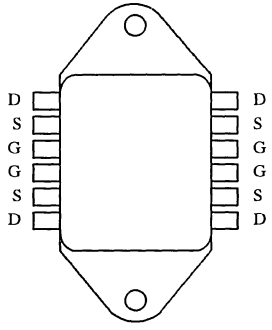
Siliconix

MOD200B/200C

Four N-Channel Enhancement-Mode Transistors

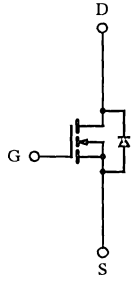
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.11	21



Leadform Options

MOD200B . . . Bent Down
MOD200C . . . Bent Up



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Single Die	All Die	Unit
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	21	84	A
	T_C = 100°C		17	56	
Pulsed Drain Current		I_{DM}	100	360	
Avalanche Current		I_A	21		
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Isolation Voltage		V_{ISOL}	1000		V

Thermal Resistance Ratings

Parameter	Symbol	Typical	Single Die	All Die	Unit
Maximum Junction-to-Ambient	R_{thJA}		30	30	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	0.31	
Case-to-Sink	R_{thCS}	0.1			

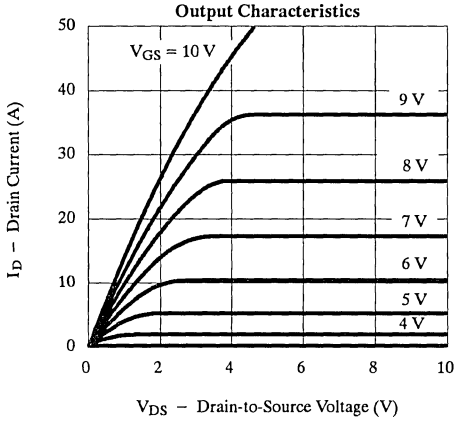
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 mA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			250	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	21			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 16 A		0.090	0.11	Ω
		V_{GS} = 10 V, I_D = 16 A, T_J = 125°C		0.150	0.175	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 16 A	8.0	13		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2700		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			300		
Total Gate Charge[b]	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 21 A		90	120	nC
Gate-Source Charge[b]	Q_{gs}			16	22	
Gate-Drain Charge[b]	Q_{gd}			37	60	
Turn-On Delay Time[b]	$t_{d(on)}$	V_{DD} = 95 V, R_L = 6.2 Ω I_D ≅ 16 A, V_{GEN} = 10 V, R_G = 4.7 Ω		15	35	ns
Rise Time[b]	t_r			30	100	
Turn-Off Delay Time[b]	$t_{d(off)}$			50	125	
Fall Time[b]	t_f			20	100	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				21	A
Pulsed Current	I_{SM}				100	
Diode Forward Voltage[a]	V_{SD}	I_F = 21 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 21 A, di/dt = 100 A/µs		150		ns
Reverse Recovery Charge	Q_{rr}			0.5		µC

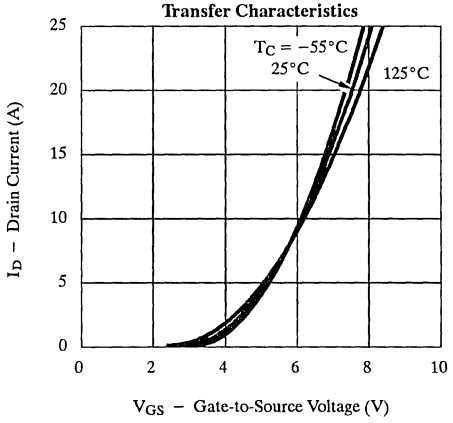
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

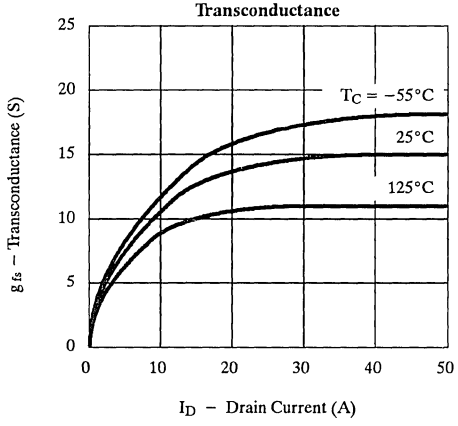
Output Characteristics



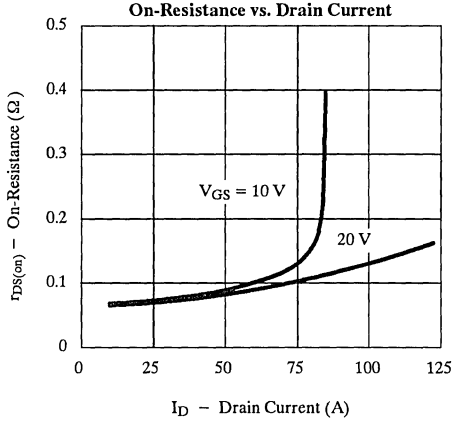
Transfer Characteristics



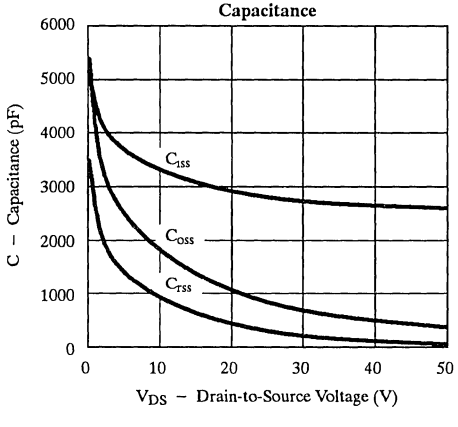
Transconductance



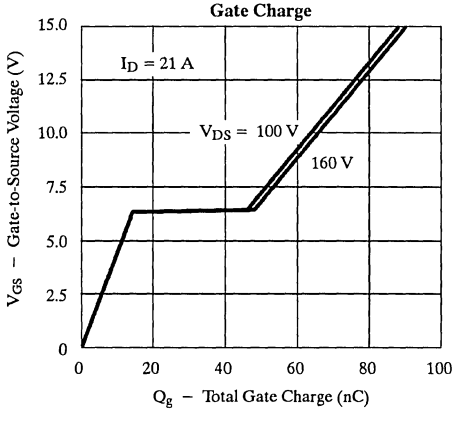
On-Resistance vs. Drain Current



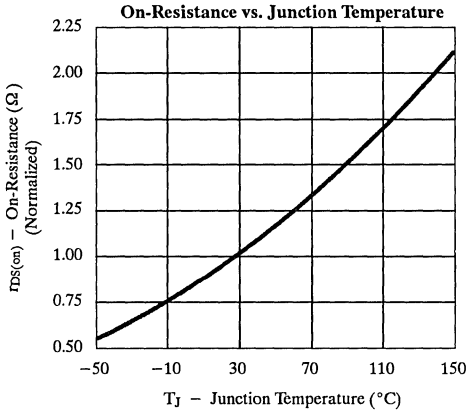
Capacitance

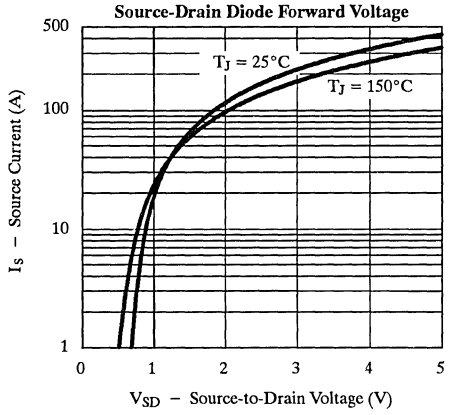


Gate Charge

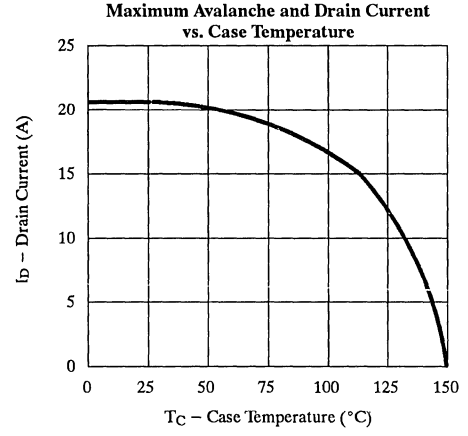


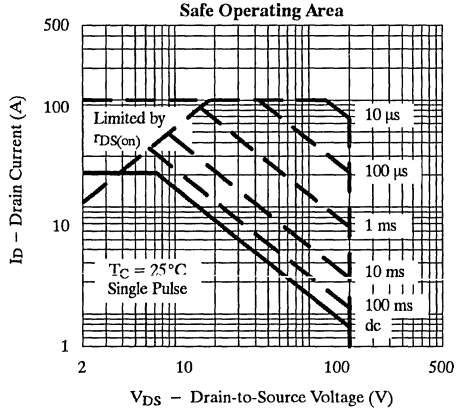
Typical Characteristics (25°C Unless Otherwise Noted)

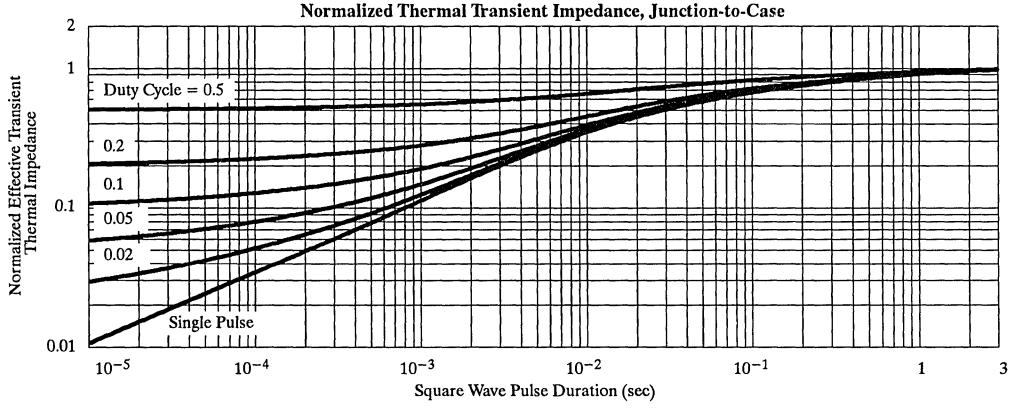




Thermal Ratings







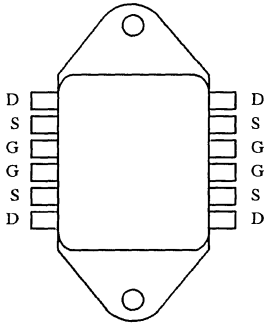
Siliconix

MOD400B/400C

Four N-Channel Enhancement-Mode Transistors

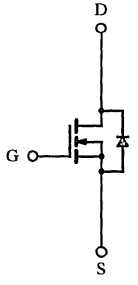
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
400	0.35	15



Leadform Options

MOD400B . . . Bent Down
MOD400C . . . Bent Up



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Single Die	All Die	Unit
Drain-Source Voltage		V_{DS}	400	400	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	15	47	A
	T_C = 100°C		9	30	
Pulsed Drain Current		I_{DM}	60	190	
Avalanche Current (see Thermal Ratings, page 6-64)		I_A	15		
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Isolation Voltage		V_{ISOL}	1000		V

Thermal Resistance Ratings

Parameter	Symbol	Typical	Single Die	All Die	Unit
Maximum Junction-to-Ambient	R_{thJA}		30	30	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	0.31	
Case-to-Sink	R_{thCS}	0.1			

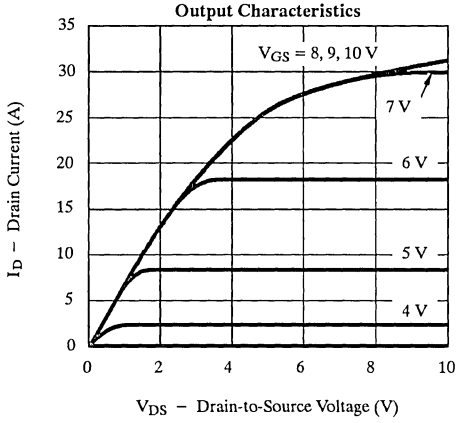
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	400			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 mA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 320 V, V_{GS} = 0 V			250	µA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	15			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 8 A		0.22	0.35	Ω
		V_{GS} = 10 V, I_D = 8 A, T_J = 125°C		0.40	0.62	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8 A	8.0	8.5		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2700		pF
Output Capacitance	C_{oss}			450		
Reverse Transfer Capacitance	C_{rss}			160		
Total Gate Charge[b]	Q_g	V_{DS} = 200 V, V_{GS} = 10 V, I_D = 15 A		105	120	nC
Gate-Source Charge[b]	Q_{gs}			13	18	
Gate-Drain Charge[b]	Q_{gd}			45	65	
Turn-On Delay Time[b]	$t_{d(on)}$	V_{DD} = 180 V, R_L = 25 Ω I_D ≅ 8 A, V_{GEN} = 10 V, R_G = 4.7 Ω		14	35	ns
Rise Time[b]	t_r			30	65	
Turn-Off Delay Time[b]	$t_{d(off)}$			54	150	
Fall Time[b]	t_f			15	75	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				15	A
Pulsed Current	I_{SM}				60	
Diode Forward Voltage[a]	V_{SD}	I_F = 15 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 15 A, di/dt = 100 A/µs		300		ns
Reverse Recovery Charge	Q_{rr}			2.0		µC

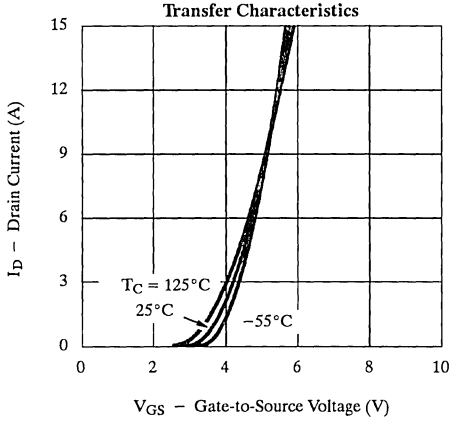
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

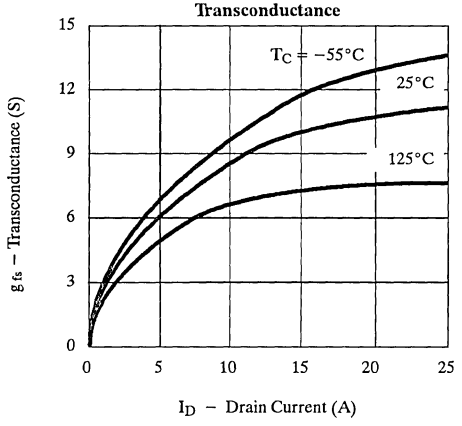
Output Characteristics



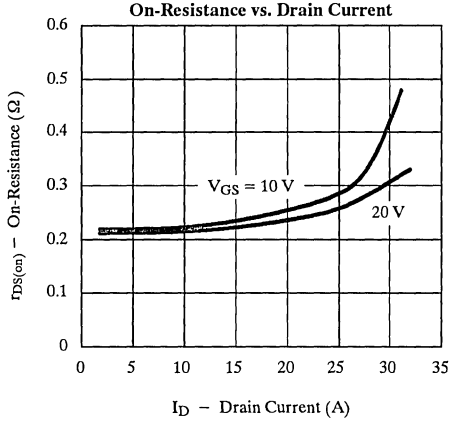
Transfer Characteristics



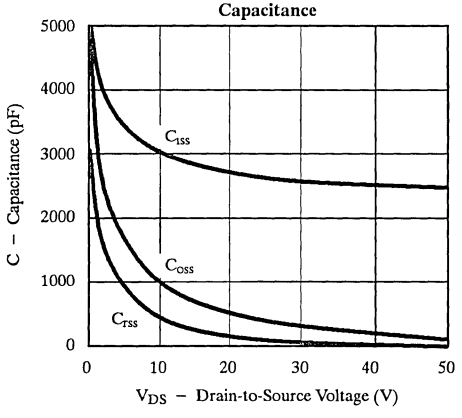
Transconductance



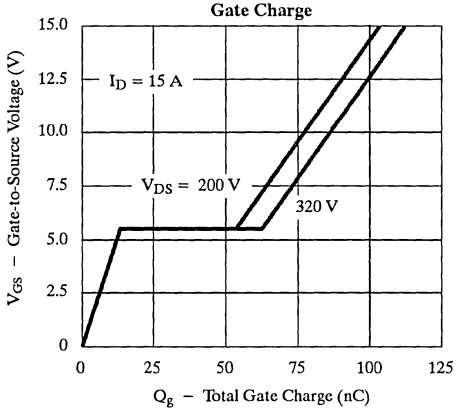
On-Resistance vs. Drain Current



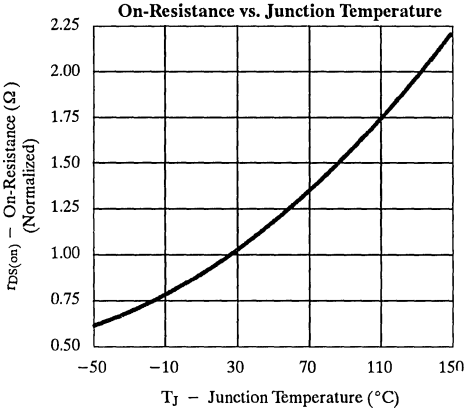
Capacitance

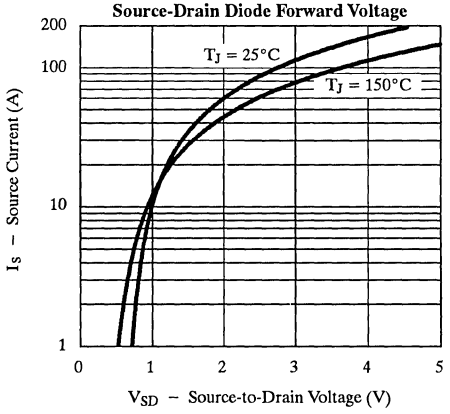


Gate Charge

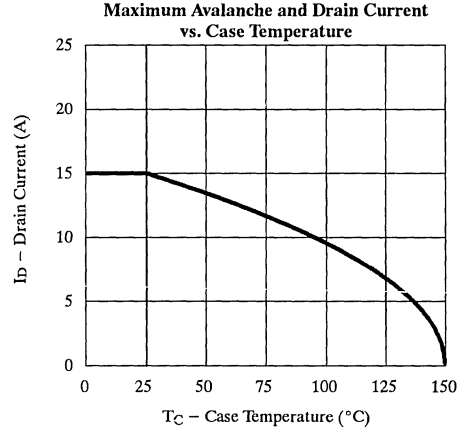


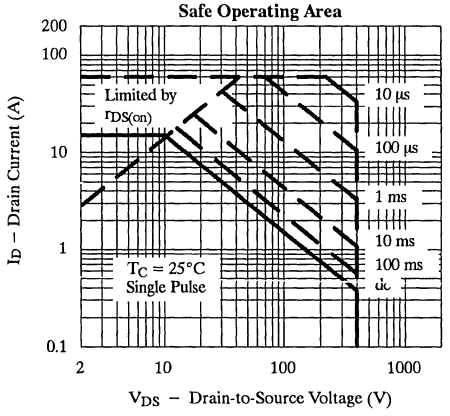
Typical Characteristics (25°C Unless Otherwise Noted)

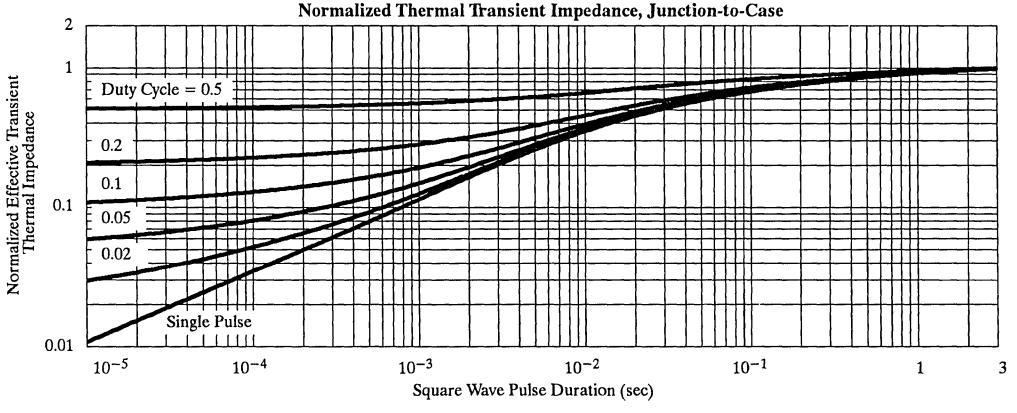




Thermal Ratings







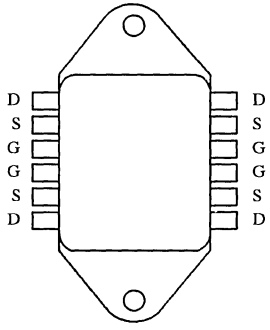
Siliconix

MOD500B/500C

Four N-Channel Enhancement-Mode Transistors

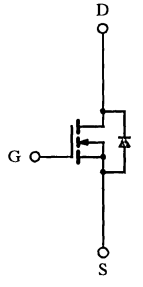
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
500	0.43	13



Leadform Options

MOD500B . . Bent Down
MOD500C . . . Bent Up



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Single Die	All Die	Unit
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	13	41	A
	T_C = 100°C		8	26	
Pulsed Drain Current		I_{DM}	52	164	
Avalanche Current		I_A	13		
Maximum Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	100	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Isolation Voltage		V_{ISOL}	1000		V

Thermal Resistance Ratings

Parameter	Symbol	Typical	Single Die	All Die	Unit
Maximum Junction-to-Ambient	R_{thJA}		30	30	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	0.31	
Case-to-Sink	R_{thCS}	0 1			

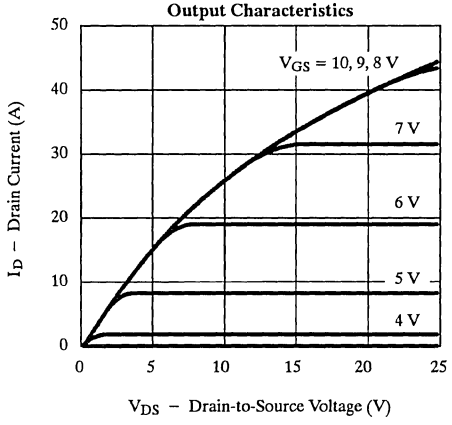
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	500			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 mA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			250	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	13			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 7 A		0.33	0.43	Ω
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C		0.66	0.88	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 7 A	6.0	9.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2700		pF
Output Capacitance	C_{oss}			410		
Reverse Transfer Capacitance	C_{rss}			140		
Total Gate Charge[b]	Q_g	V_{DS} = 250 V, V_{GS} = 10 V, I_D = 13 A		90	120	nC
Gate-Source Charge[b]	Q_{gs}			12	19	
Gate-Drain Charge[b]	Q_{gd}			47	70	
Turn-On Delay Time[b]	$t_{d(on)}$	V_{DD} = 210 V, R_L = 30 Ω I_D ≅ 7 A, V_{GEN} = 10 V, R_G = 4.7 Ω		13	35	ns
Rise Time[b]	t_r			26	50	
Turn-Off Delay Time[b]	$t_{d(off)}$			55	150	
Fall Time[b]	t_f			17	70	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				13	A
Pulsed Current	I_{SM}				52	
Diode Forward Voltage[a]	V_{SD}	I_F = 13 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 13 A, di/dt = 100 A/µs		300		ns
Reverse Recovery Charge	Q_{rr}			2.0		µC

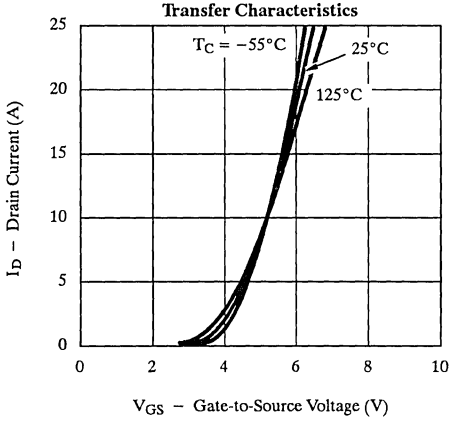
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

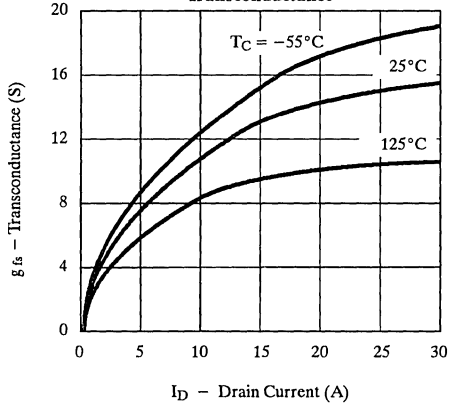
Output Characteristics



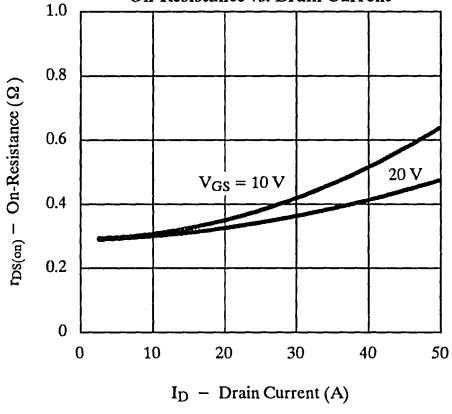
Transfer Characteristics



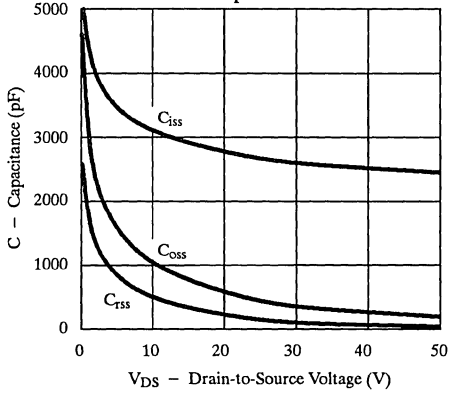
Transconductance



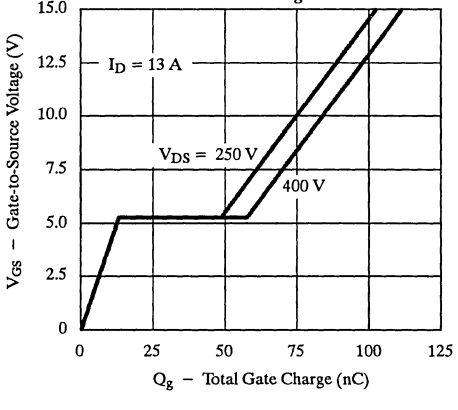
On-Resistance vs. Drain Current



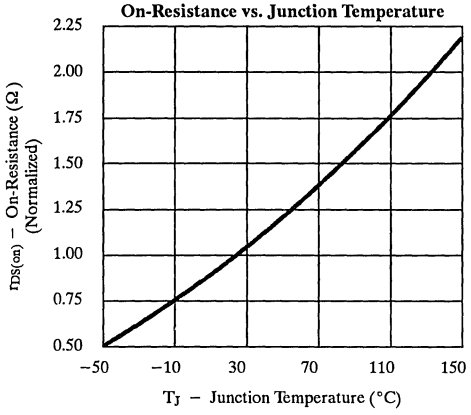
Capacitance

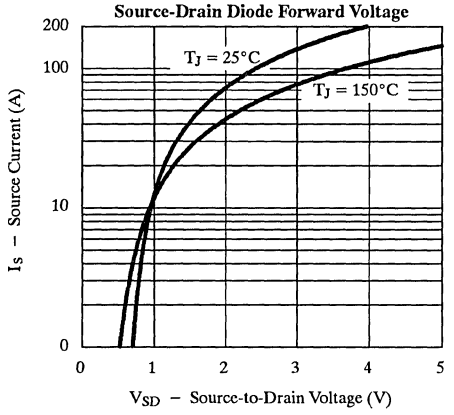


Gate Charge

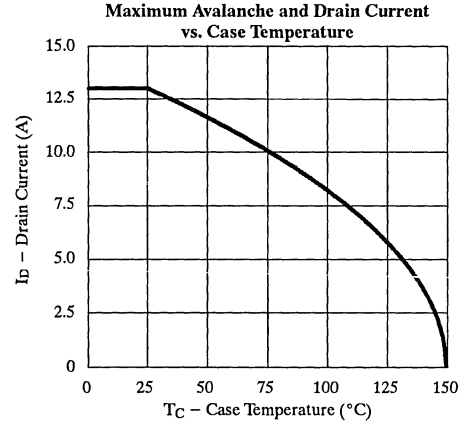


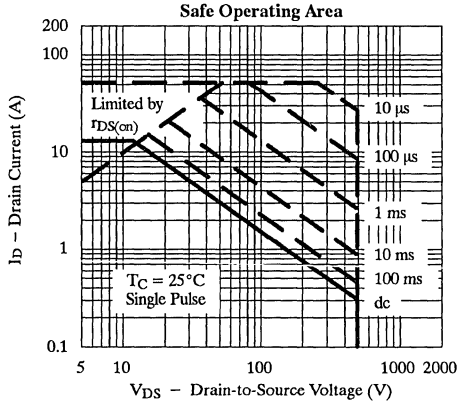
Typical Characteristics (25°C Unless Otherwise Noted)

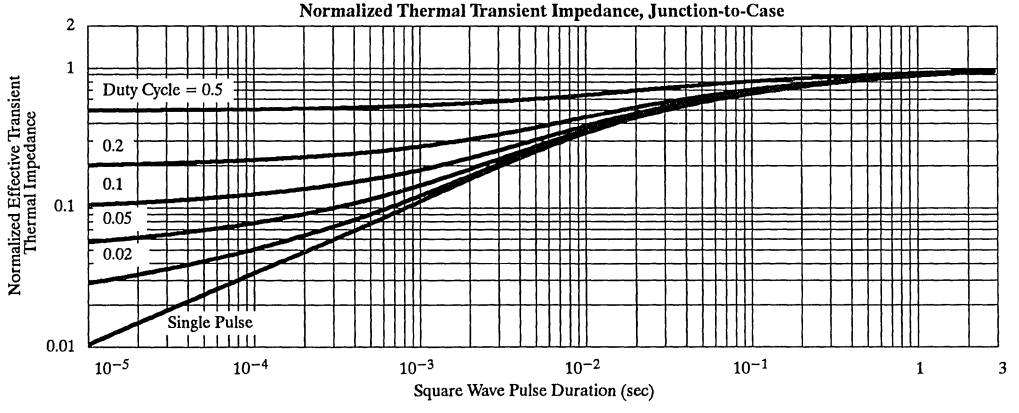




Thermal Ratings







Siliconix

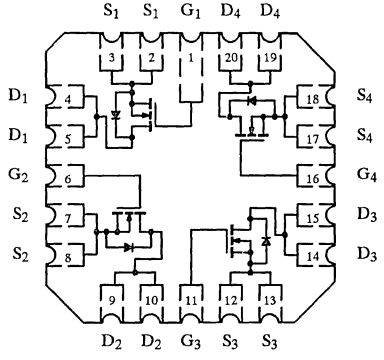
Si8956AZ/883

Quad N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.1 @ V_{GS} = 10 V	5
	0.2 @ V_{GS} = 4.5 V	1

LCC-20



Top View

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A = 25°C	I_D	5	A
	T_A = 100°C		3	
Pulsed Drain Current[a]		I_{DM}	14	
Continuous Source Current (Diode Conduction)		I_S	3	
Maximum Power Dissipation	T_A = 25°C	P_D	3	W
	T_A = 100°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	40	°C/W

Notes:
a. Drain current limited by package construction.

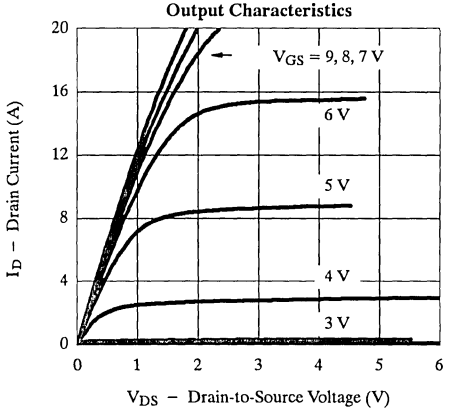
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Static					
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	20		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1	3.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V		10	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 125°C		25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	7		A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3 A		0.1	Ω
		V_{GS} = 4.5 V, I_D = 1 A		0.2	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 3 A	2		S
Dynamic					
Input Capacitance[a]	C_{iss}	V_{GS} = 0 V, V_{DS} = 16 V, f = 1 MHz		500	nC
Output Capacitance[a]	C_{oss}			300	
Reverse Transfer Capacitance[a]	C_{rss}			125	
Total Gate Charge[a, c]	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5 A		30	
Gate-Source Charge[a, c]	Q_{gs}			5	
Gate-Drain Charge[a, c]	Q_{gd}			8	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 10 V, R_L = 2 Ω I_D ≅ 3 A, V_{GEN} = 10 V, R_G = 6 Ω		30	ns
Rise Time[c]	t_r			35	
Turn-Off Delay Time[c]	$t_{d(off)}$			70	
Fall Time[c]	t_f			30	
Source-Drain Diode (T_C = 25°C)					
Pulsed Current	I_{SM}			3	A
Diode Forward Voltage[b]	V_{SD}	I_F = 3 A, V_{GS} = 0 V		1.6	V
Reverse Recovery Time	t_{rr}	I_F = 3 A, di/dt = 100 A/µs		100	ns

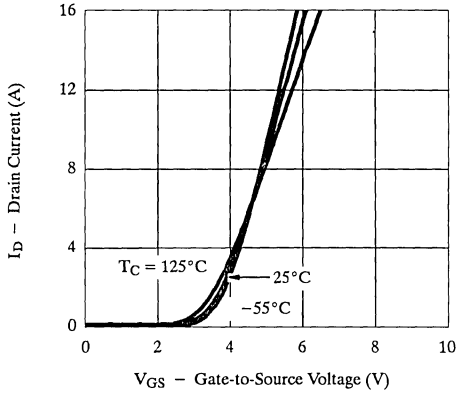
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

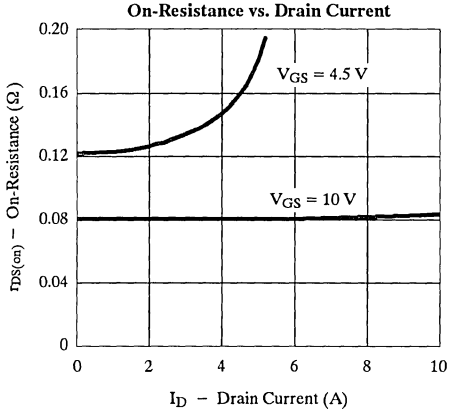
Output Characteristics



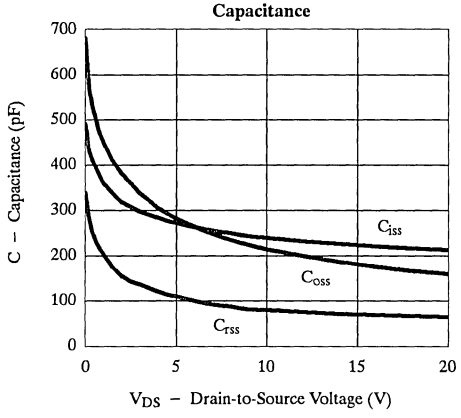
Transfer Characteristics



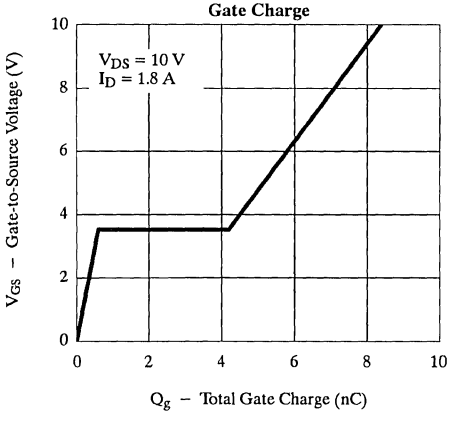
On-Resistance vs. Drain Current



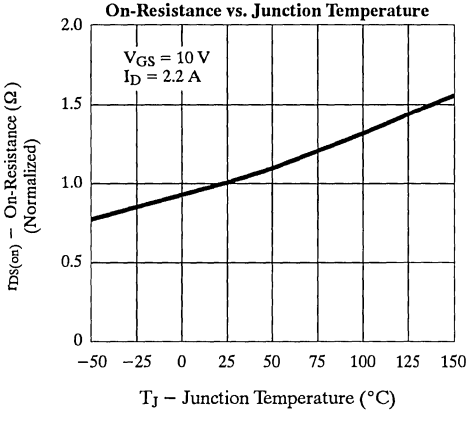
Capacitance



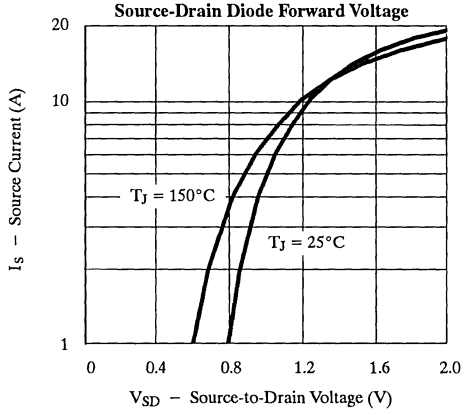
Gate Charge

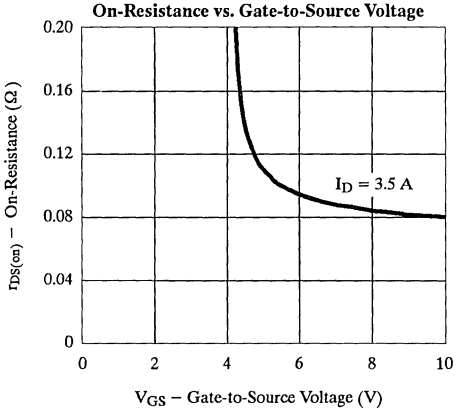


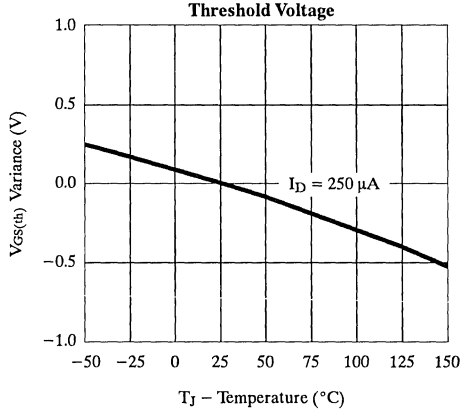
On-Resistance vs. Junction Temperature

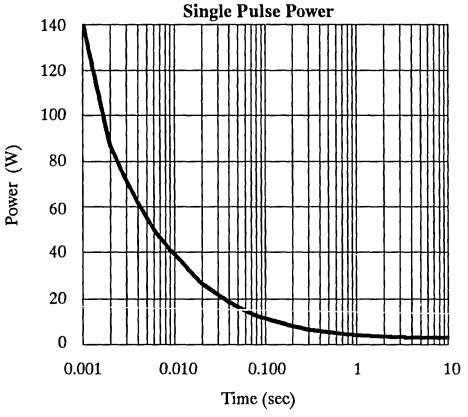


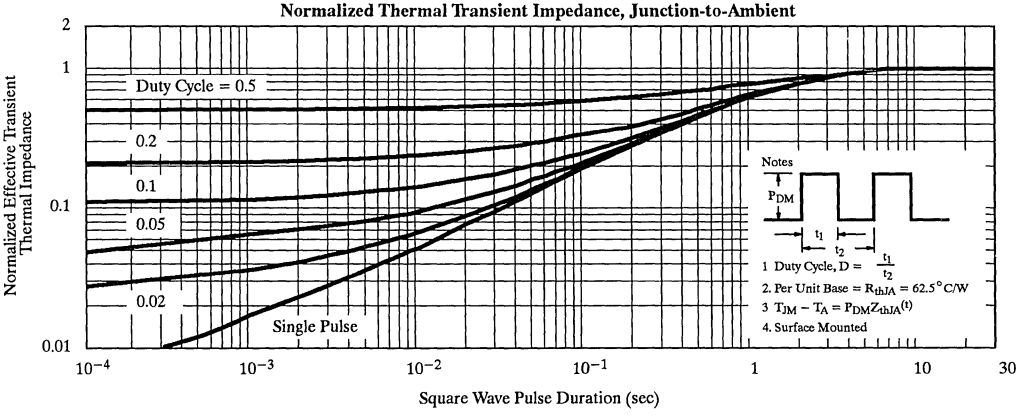
Typical Characteristics (25°C Unless Otherwise Noted)











Siliconix

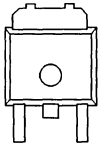
SMD/SMU10P05

P-Channel Enhancement-Mode Transistors

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
−50	0.28	−10

TO-252



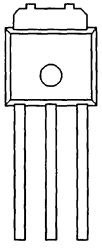
G D S

Top View

Drain Connected to Tab

Order Number: SMD10P05

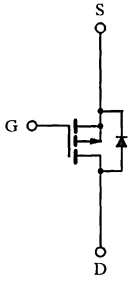
TO-251



G D S

Top View

Order Number: SMU10P05



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−50	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[b]	T_A = 25°C	I_D	−2.0	A
	T_A = 100°C		−1.3	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	−16	
Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Free Air, PC Board Mount[b]	R_{thJA}	50	60	°C/W
Junction-to-Ambient Free Air, Vertical Mount		50	60	
Junction-to-Case	R_{thJC}	2.3	3 0	

Notes:

a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).

b. Surface mounted on PC board or mounted vertically in free air.

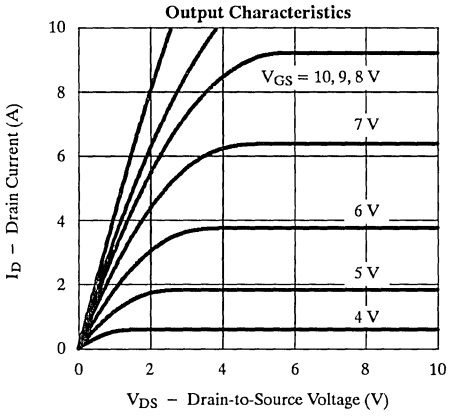
Specifications (T_J = 25°C Unless Otherwise Noted)

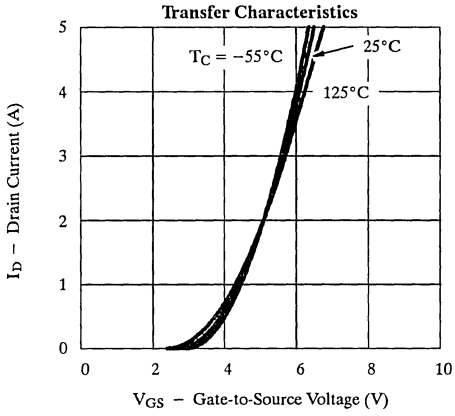
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −40 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −40 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −5 A		0.25	0.28	Ω
		V_{GS} = −10 V, I_D = −5 A, T_J = 125°C		0.4	0.50	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −5 A	1.0	3		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		530		pF
Output Capacitance	C_{oss}			325		
Reverse Transfer Capacitance	C_{rss}			85		
Total Gate Charge[c]	Q_g	V_{DS} = −25 V, V_{GS} = −10 V, I_D = − 10 A		13	20	nC
Gate-Source Charge[c]	Q_{gs}			3.6	5.0	
Gate-Drain Charge[c]	Q_{gd}			9	12.0	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 3 Ω I_D ≃ −10 A, V_{GEN} = −10 V, R_G = 25 Ω		10	30	ns
Rise Time[c]	t_r			50	95	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	90	
Fall Time[c]	t_f			50	75	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−2.0	A
Pulsed Current	I_{SM}				−24	
Forward Voltage[b]	V_{SD}	I_F = −2 A, V_{GS} = 0 V			−2.3	V
Reverse Recovery Time	t_{rr}	I_F = −2 A, dI_F/dt = 100 A/µs		70		ns
Reverse Recovery Charge	Q_{rr}			0.07		µC

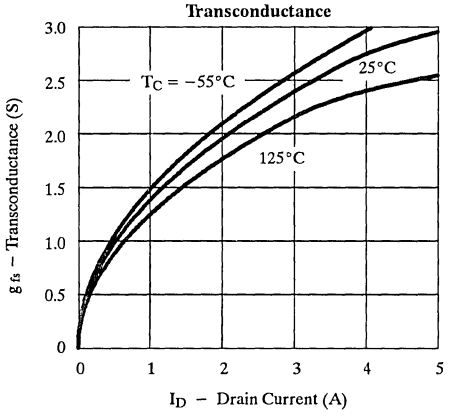
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

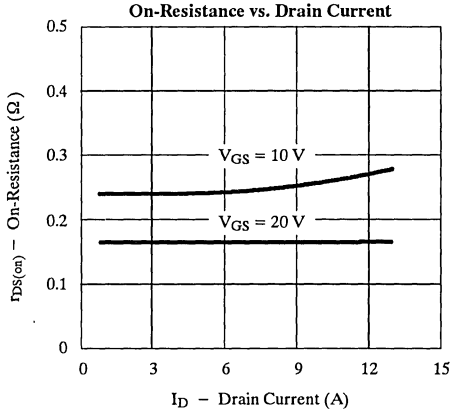
Typical Characteristics (25°C Unless Otherwise Noted)

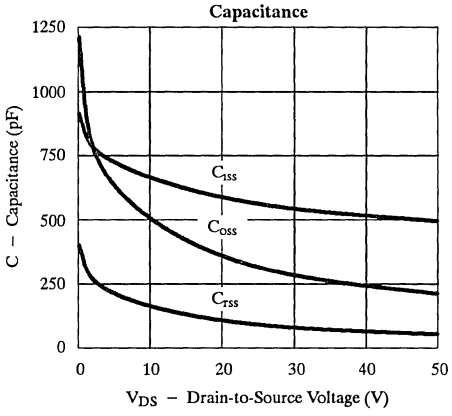
Negative signs omitted for clarity.

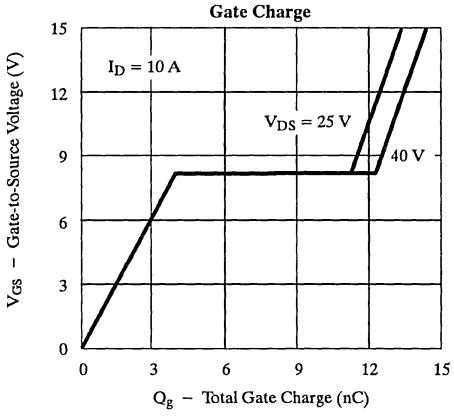








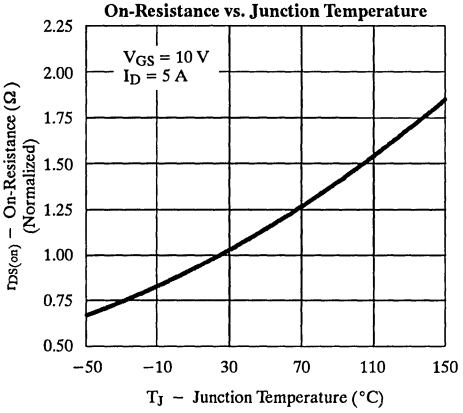




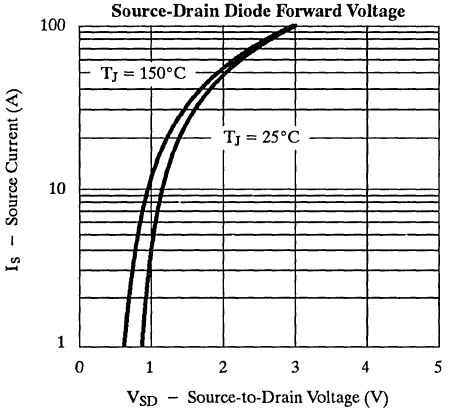
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

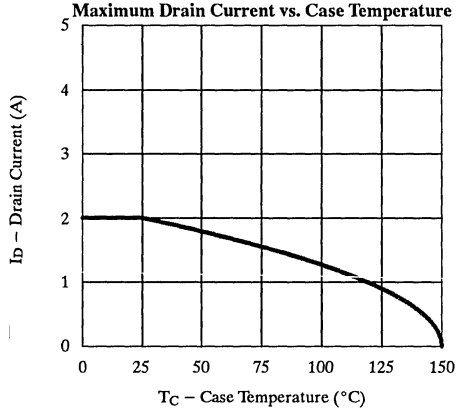


Source-Drain Diode Forward Voltage

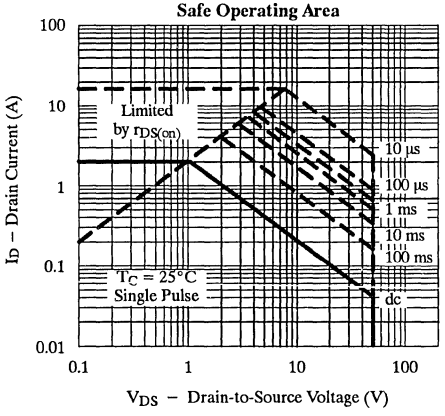


Thermal Ratings

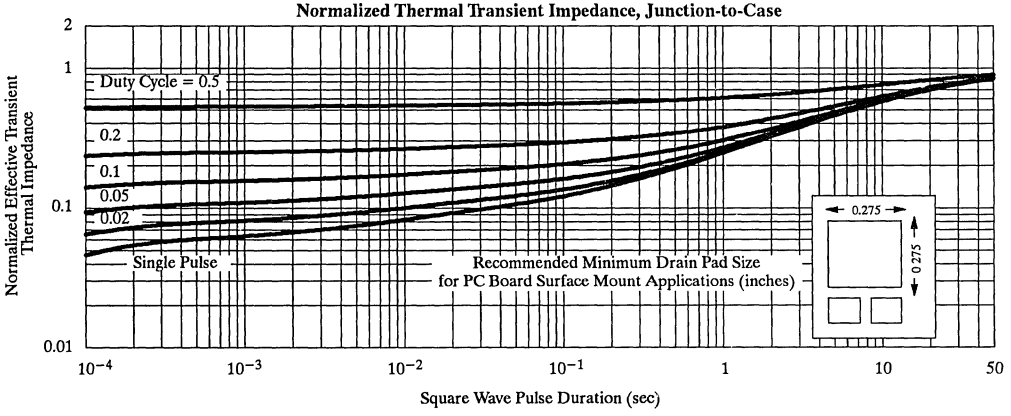
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SMD10P06

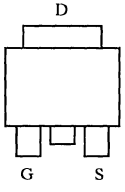
P-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

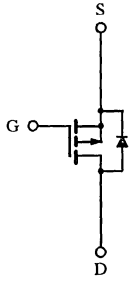
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
−60	0.28	−10

DPAK (TO-252)



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[b]	T_C = 25°C	I_D	−10	A
	T_C = 100°C		−5.7	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	−16	
Maximum Power Dissipation	T_C = 25°C	P_D	42	W
	T_A = 25°C		2.0[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air[b]	R_{thJA}	60	°C/W
Junction-to-Case	R_{thJC}	3.0	

Notes:
a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
b. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −48 V, V_{GS} = 0 V			−1	µA
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −3.0 A			0.28	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} = −10 V, I_D = −5.7 A	2.3			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz				pF
Output Capacitance	C_{oss}					
Reverse Transfer Capacitance	C_{rss}					
Total Gate Charge[c]	Q_g	V_{DS} = −48 V, V_{GS} = −10 V, I_D = −9.7 A			19	nC
Gate-Source Charge[c]	Q_{gs}					
Gate-Drain Charge[c]	Q_{gd}					
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 3 Ω I_D ≅ −10 A, V_{GEN} = −10 V, R_G = 25 Ω				ns
Rise Time[c]	t_r					
Turn-Off Delay Time[c]	$t_{d(off)}$					
Fall Time[c]	t_f					
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S	T_C= 25°C			−2.0	A
Pulsed Current	I_{SM}				−16	
Forward Voltage[b]	V_{SD}	I_F = 2.0 A, V_{GS} = 0 V			−1.2	V
Reverse Recovery Time	t_{rr}	I_F = 2.0 A, di/dt = 100 A/µs				ns
Reverse Recovery Charge	Q_{rr}					µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

SMD10P06L

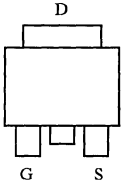
P-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

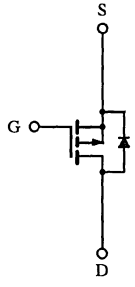
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
−60	0.28 @ V_{GS} = −10 V	−10
	0.35 @ V_{GS} = −4.5 V	−7.5

DPAK (TO-252)



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[b]	T_A = 25°C	I_D	−2.0	A
	T_A = 100°C		−1.2	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	−16	
Maximum Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Free Air[b]	R_{thJA}		60	°C/W
Junction-to-Case	R_{thJC}	2.3	3.0	

Notes:
a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
b. Surface mounted on PC board or mounted vertically in free air.

Specifications (T_J = 25°C Unless Otherwise Noted)

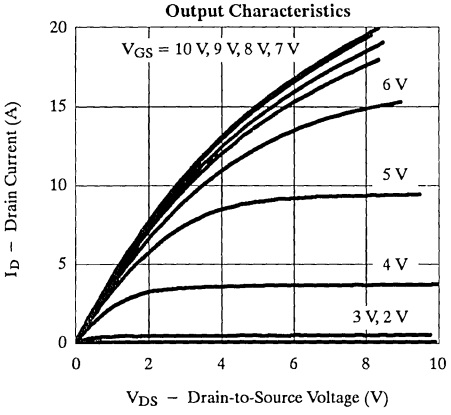
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−1.0		−3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −48 V, V_{GS} = 0 V			−2	µA
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 125°C			−100	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −2.3 A			0.28	Ω
		V_{GS} = −4.5 V, I_D = −1.6 A			0.35	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −5 A	1.0			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		440		pF
Output Capacitance	C_{oss}			140		
Reverse Transfer Capacitance	C_{rss}			25		
Total Gate Charge[c]	Q_g	V_{DS} = −30 V, V_{GS} = −10 V, I_D = −10 A		13	24	nC
Gate-Source Charge[c]	Q_{gs}			2.0	4.0	
Gate-Drain Charge[c]	Q_{gd}			4	8.0	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 3 Ω I_D ≅ −10 A, V_{GEN} = −10 V, R_G = 25 Ω		15		ns
Rise Time[c]	t_r			50		
Turn-Off Delay Time[c]	$t_{d(off)}$			80		
Fall Time[c]	t_f			80		
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−2 0	A
Pulsed Current	I_{SM}				−24	
Forward Voltage[b]	V_{SD}	I_F = −2.0 A, V_{GS} = 0 V			−1.2	V
Reverse Recovery Time	t_{rr}	I_F = −2.0 A, di/dt = 100 A/µs		60		ns
Reverse Recovery Charge	Q_{rr}			0.07		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

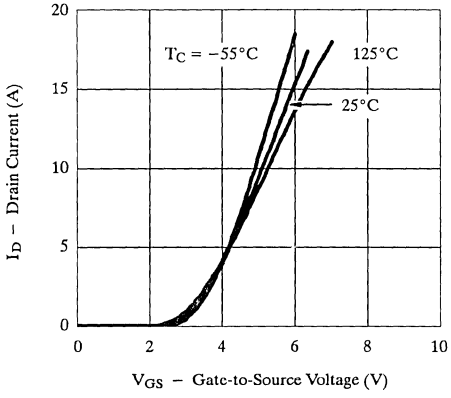
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

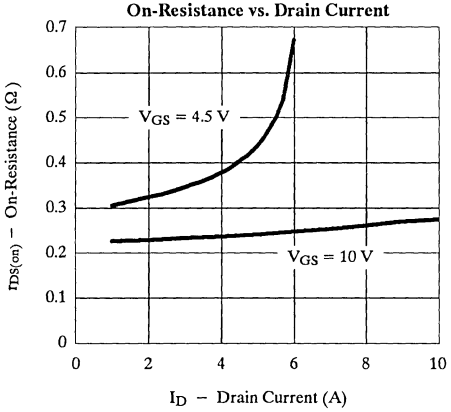
Output Characteristics



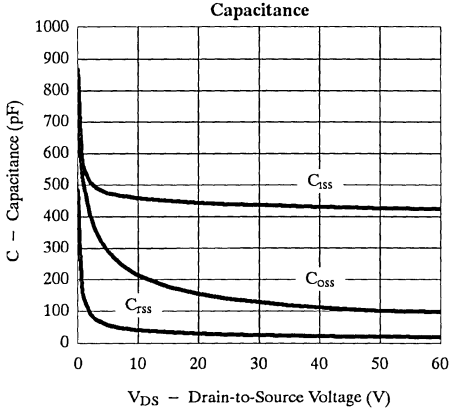
Transfer Characteristics



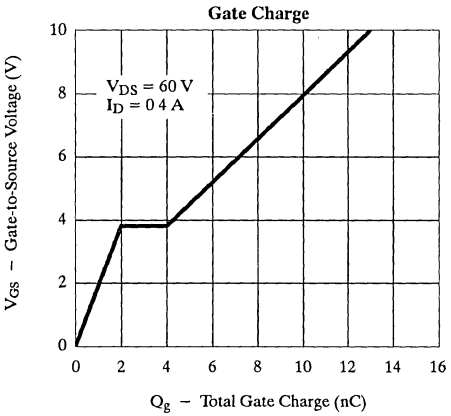
On-Resistance vs. Drain Current



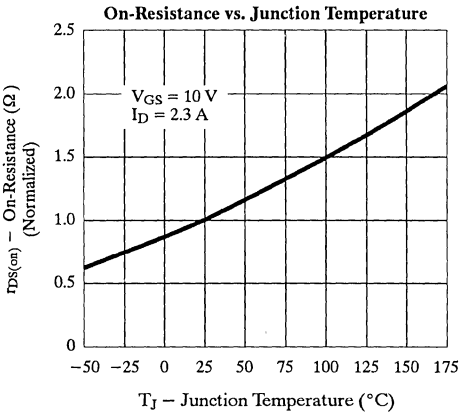
Capacitance



Gate Charge



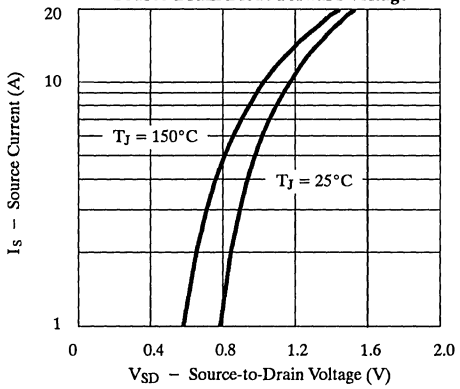
On-Resistance vs. Junction Temperature



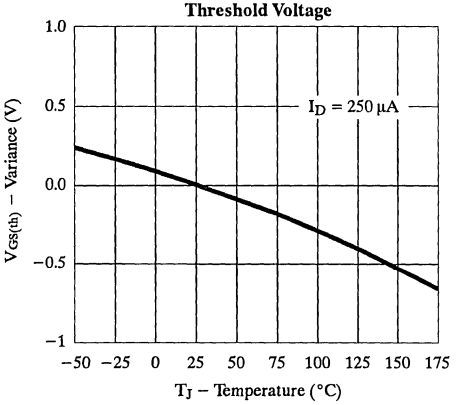
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

Source-Drain Diode Forward Voltage

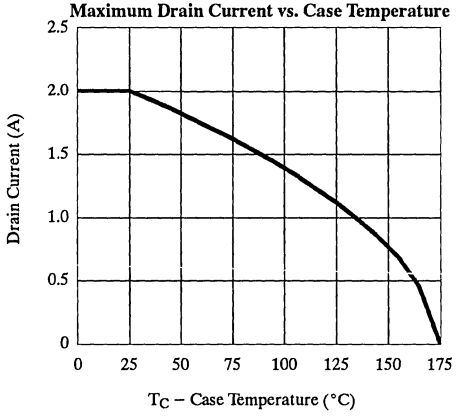


Threshold Voltage

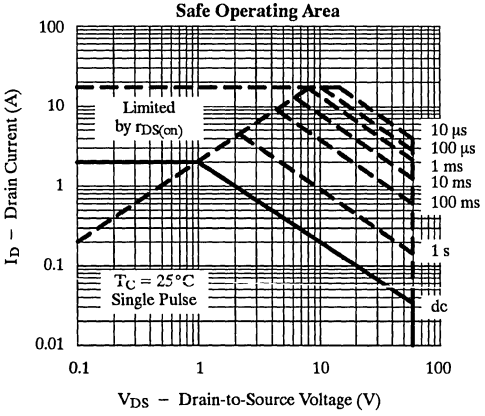


Thermal Ratings

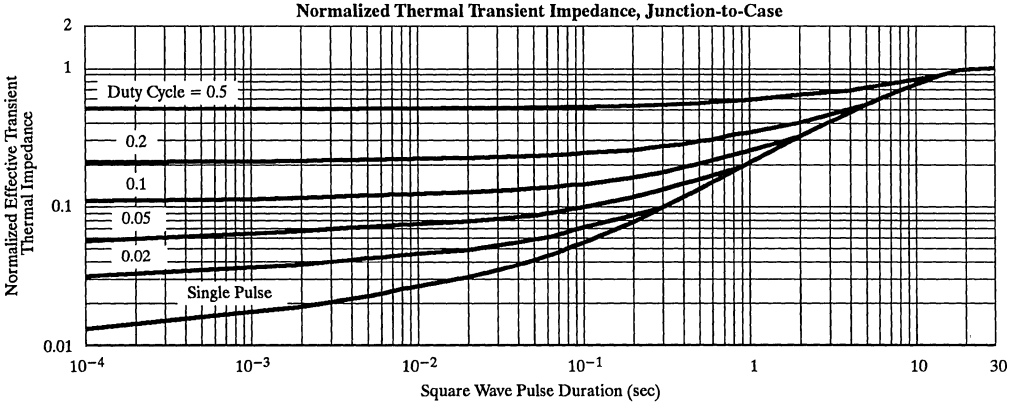
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SMD/SMU15N05

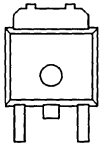
N-Channel Enhancement-Mode Transistors

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
50	0.10	15

TO-252



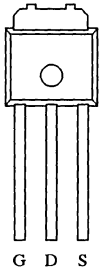
Drain connected to Tab

G D S

Top View

Order Number: SMD15N05

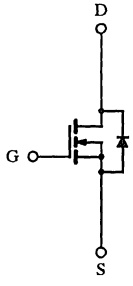
TO-251



G D S

Top View

Order Number: SMU15N05



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	SMD15N05	SMU15N05	Unit
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current[b]	T_A = 25°C	I_D	3.3[b]	2.3[c]	A
	T_A = 100°C		1.9[b]	1.3[c]	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	24	24	
Power Dissipation	T_C = 25°C	P_D	40	40	W
	T_A = 25°C		2.0[b]	1.0[c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Free Air, PC Board Mount	R_{thJA}	50	60	°C/W
Junction-to-Ambient Free Air, Vertical Mount			125	
Junction-to-Case	R_{thJC}		3.0	

Notes:

a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
b. Surface mounted on PC board.
c. Free air, vertical mount.

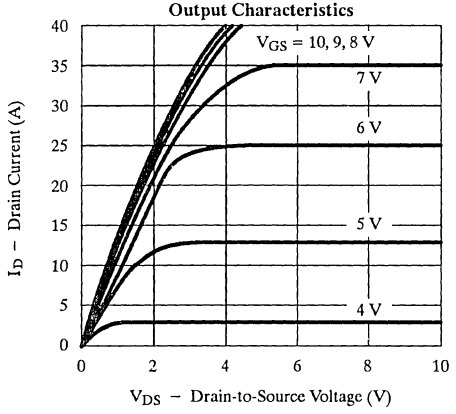
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			25	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	15			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 7.5 A		0.07	0.10	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C		0.13	0.18	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A	3.0	4.8		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		550		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			100		
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 15 A		15	30	nC
Gate-Source Charge[c]	Q_{gs}			3.5		
Gate-Drain Charge[c]	Q_{gd}			5		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1.67 Ω I_D ≃ 15 A, V_{GEN} = 10 V, R_G = 25 Ω		15	30	ns
Rise Time[c]	t_r			50	85	
Turn-Off Delay Time[c]	$t_{d(off)}$			80	90	
Fall Time[c]	t_f			80	110	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S	SMD15N05			3.3	A
		SMU15N05			1.0	
Pulsed Current	I_{SM}				24	
Forward Voltage[b]	V_{SD}	I_F = 3.3 A, V_{GS} = 0 V		1.8	2.3	V
Reverse Recovery Time	t_{rr}	I_F = 3.3 A, dI_F/dt = 100 A/µs		65		ns
Reverse Recovery Charge	Q_{rr}			0.16		µC

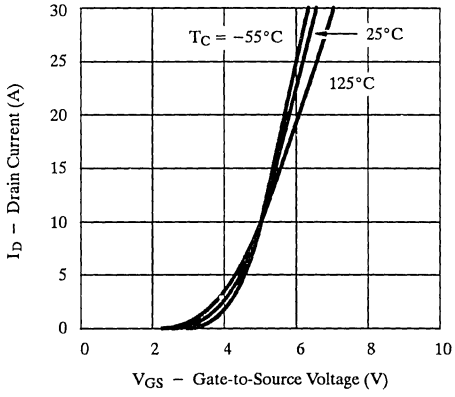
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

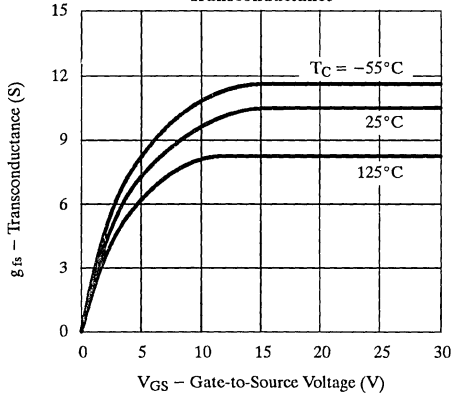
Output Characteristics



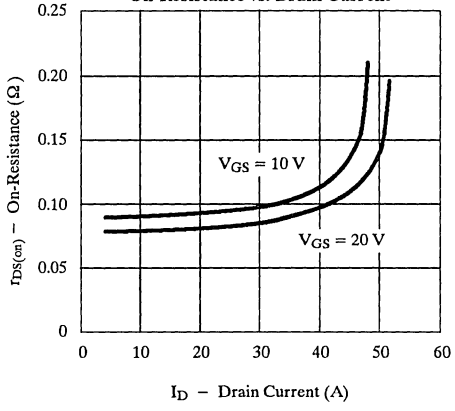
Transfer Characteristics



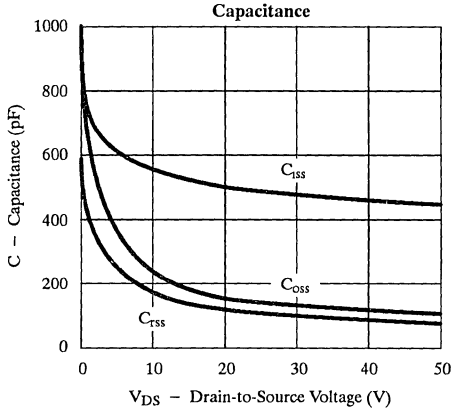
Transconductance



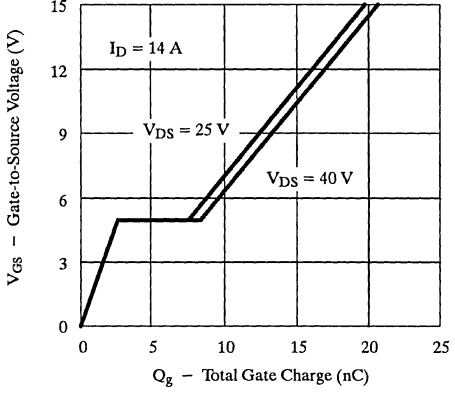
On-Resistance vs. Drain Current



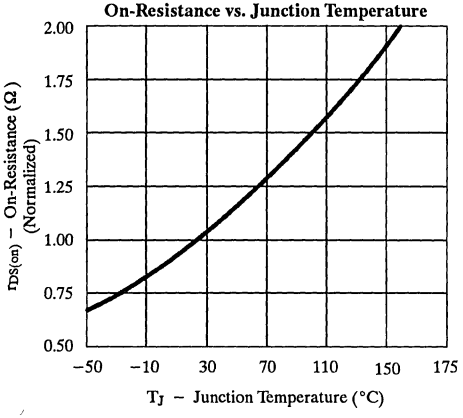
Capacitance

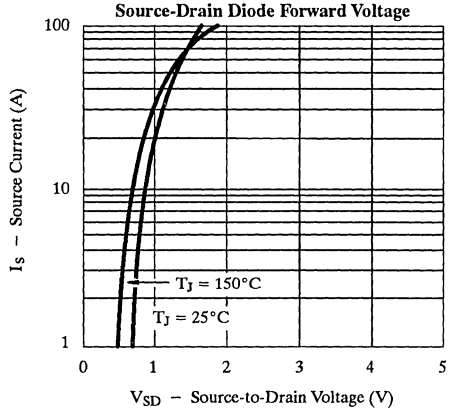


Gate Charge

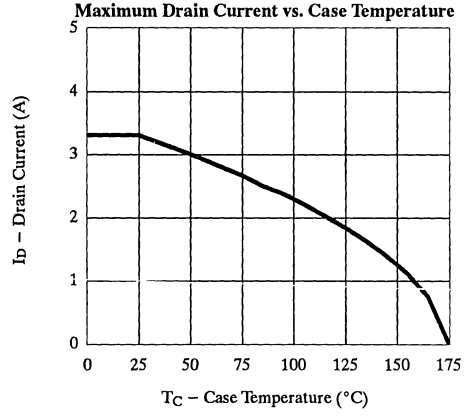


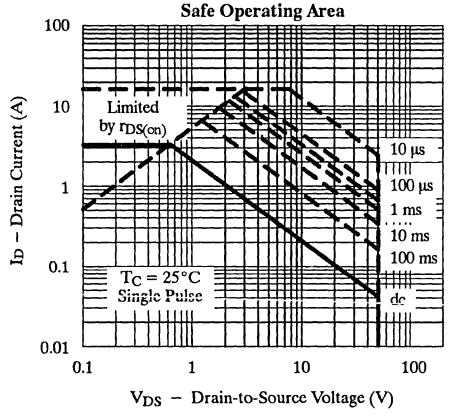
Typical Characteristics (25°C Unless Otherwise Noted)

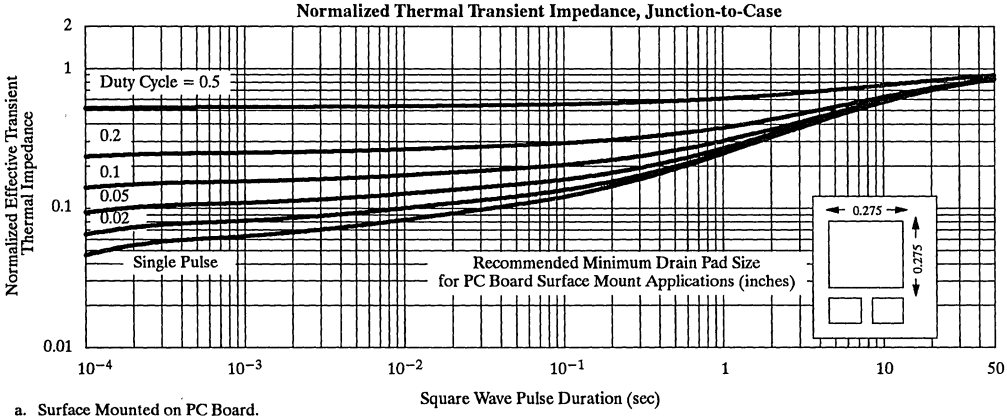




Thermal Ratings[a]







a. Surface Mounted on PC Board.

Siliconix

SMD15N06

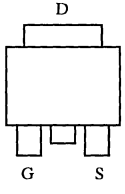
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

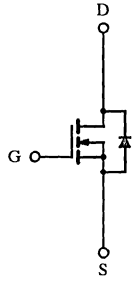
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
60	0.10	15

DPAK (TO-252)



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[b]	T_C = 25°C	I_D	15	A
	T_C = 100°C		7.5	
Pulsed Drain Current (maximum current limited by package)		I_{DM}	16	
Maximum Power Dissipation	T_C = 25°C	P_D	40	W
	T_A = 25°C		2.0[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air[b]	R_{thJA}	60	°C/W
Junction-to-Case	R_{thJC}	3.0	

Notes:
a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
b. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	15			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 7.5 A			0.10	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C			0.18	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 7.5 A	5.0			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		TBD		pF
Output Capacitance	C_{oss}			TBD		
Reverse Transfer Capacitance	C_{rss}			TBD		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 15 A		TBD	24	nC
Gate-Source Charge[c]	Q_{gs}			TBD	4.0	
Gate-Drain Charge[c]	Q_{gd}			TBD	8.0	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1.67 Ω I_D ≅ 15 A, V_{GEN} = 10 V, R_G = 25 Ω		TBD	30	ns
Rise Time[c]	t_r			TBD	85	
Turn-Off Delay Time[c]	$t_{d(off)}$			TBD	90	
Fall Time[c]	t_f			TBD	110	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S	T_C= 25°C			15	A
Pulsed Current	I_{SM}				16	
Forward Voltage[b]	V_{SD}	I_F = 3.3 A, V_{GS} = 0 V			2.2	V
Reverse Recovery Time	t_{rr}	I_F = 3.3 A, di/dt = 100 A/µs		TBD		ns
Reverse Recovery Charge	Q_{rr}			TBD		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

SMD/SMU25N05-45L

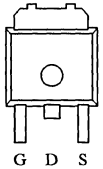
N-Channel Enhancement-Mode Transistors, Logic Level

175°C Maximum Junction Temperature

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
50	0.045	25

TO-252



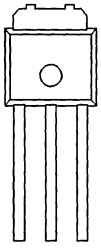
G D S

Top View

Order Number:
SMD25N05-45L

Drain Connected to Tab

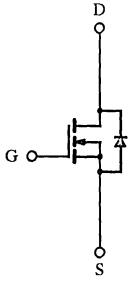
TO-251



G D S

Top View

Order Number:
SMU25N05-45L



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±16	V
Continuous Drain Current (T_J = 150°C)[b]	T_A = 25°C	I_D	5.0	A
	T_A = 100°C		3.1	
Pulsed Drain Current		I_{DM}	100	
Continuous Source Current (Diode Conduction)		I_S	5	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)	L = 0.1 mH	E_{AR}	31	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	50	W
	T_A = 25°C		2[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b]	R_{thJA}		60	°C/W
Maximum Junction-to-Case	R_{thJC}		2.5	
Case-to-Sink	R_{thCS}	1.0		

Notes:

a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).

b. Surface mounted on PC board or mounted vertically in free air.

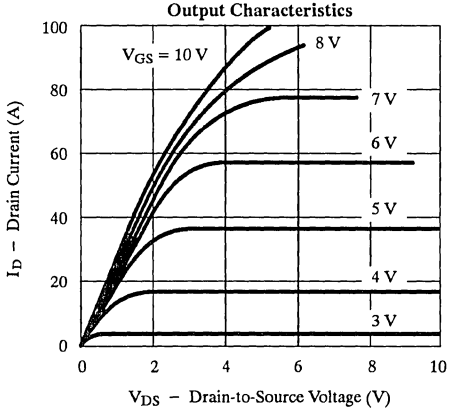
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.0	1.8	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C			100	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10V	25			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 12.5 A		0.035	0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C		0.060	0.080	
		V_{GS} = 5 V, I_D = 12.5 A		0.045	0.070	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A		19		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		950		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			110		
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 25 A		22	36	nC
Gate-Source Charge[c]	Q_{gs}			5	10	
Gate-Drain Charge[c]	Q_{gd}			10	16	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω I_D ≅ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω		10	20	ns
Rise Time[c]	t_r			21	40	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	60	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Pulsed Current	I_{SM}				100	A
Diode Forward Voltage	V_{SD}	I_F = 25 A, V_{GS} = 0 V		1.0	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, di/dt = 100 A/µs		120		ns

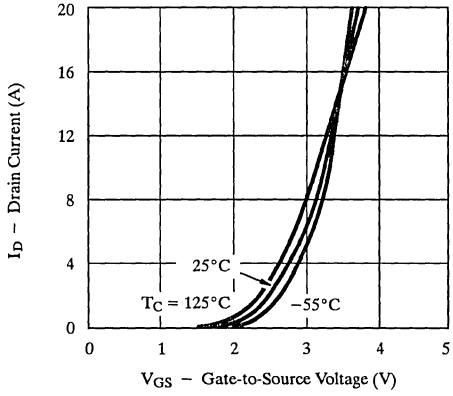
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

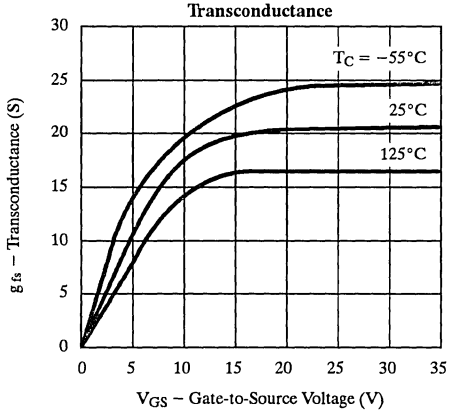
Output Characteristics



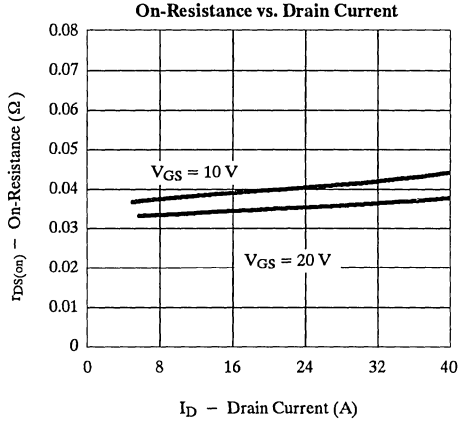
Transfer Characteristics



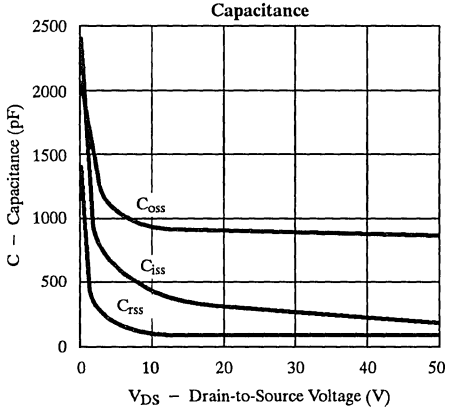
Transconductance



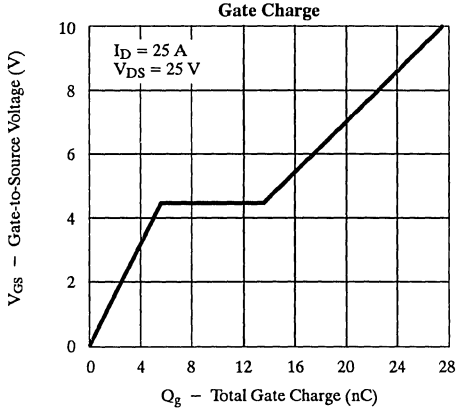
On-Resistance vs. Drain Current



Capacitance

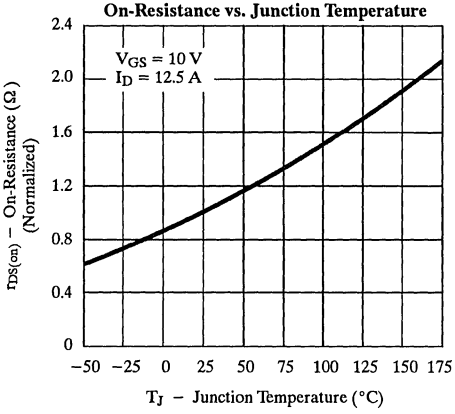


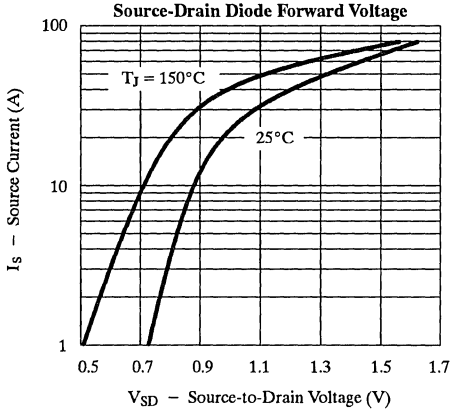
Gate Charge



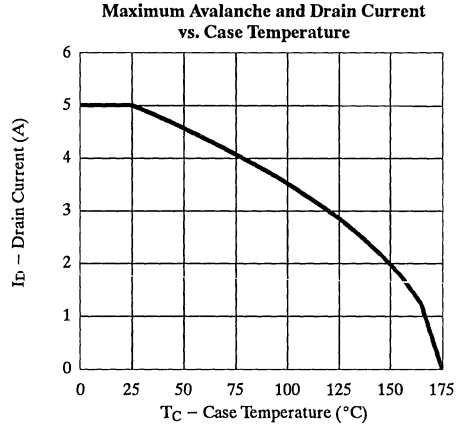
SMD/SMU25N05-45L

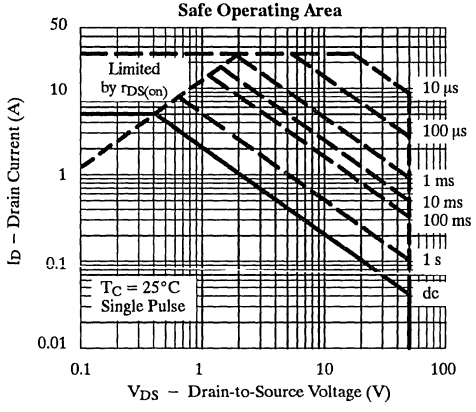
Typical Characteristics (25°C Unless Otherwise Noted)

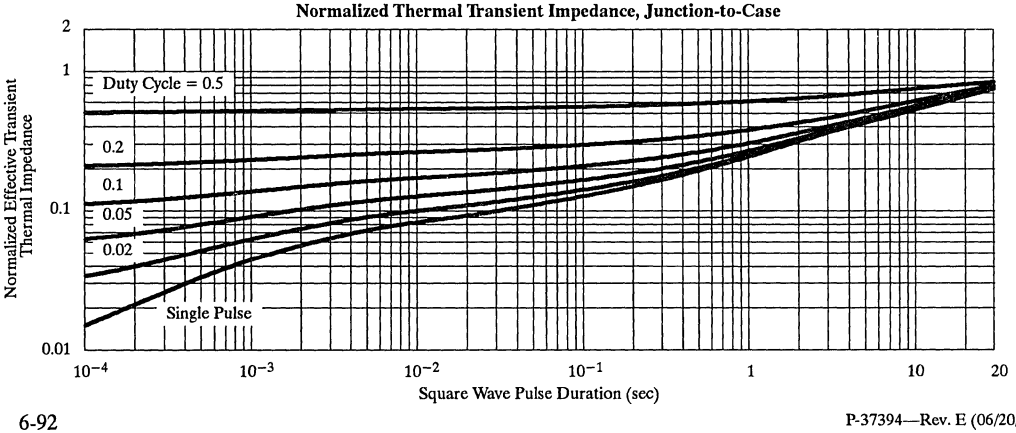




Thermal Ratings







Siliconix

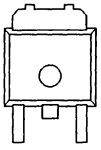
SMD/SMU30N03-30L

N-Channel Enhancement-Mode Transistors, Logic Level

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D[a] (A)
30	0.030	30

TO-252



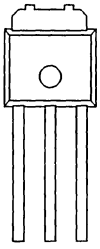
G D S

Top View

Order Number:
SMD30N03-30L

Drain Connected to Tab

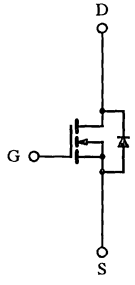
TO-251



G D S

Top View

Order Number:
SMU30N03-30L



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[b]	T_A = 25°C	I_D	60	A
	T_A = 100°C		3.8	
Pulsed Drain Current		I_{DM}	30	
Continuous Source Current (Diode Conduction)		I_S	6	
Avalanche Current		I_{AR}	30	
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)	L = 0.1 mH	E_{AR}	45	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	50	W
	T_A = 25°C		2[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b]	R_{thJA}		60	°C/W
Maximum Junction-to-Case	R_{thJC}		2.5	
Case-to-Sink	R_{thCS}	1.0		

Notes:

a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).

b. Surface mounted on PC board or mounted vertically in free air.

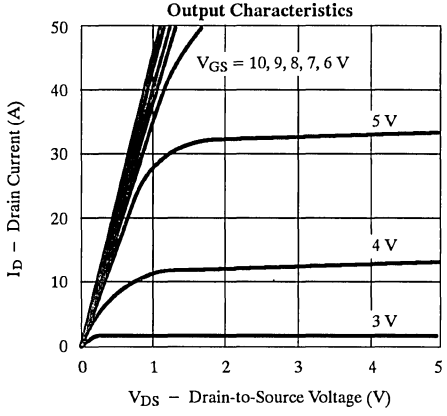
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.0	2.1	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			25	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.023	0.030	Ω
		V_{GS} = 10 V, I_D = 15 A, T_J = 125°C		0.031	0.050	
		V_{GS} = 5 V, I_D = 15 A		0.035	0.045	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		15		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		850		pF
Output Capacitance	C_{oss}			500		
Reverse Transfer Capacitance	C_{rss}			220		
Total Gate Charge[c]	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 30 A		30	35	nC
Gate-Source Charge[c]	Q_{gs}			5	8	
Gate-Drain Charge[c]	Q_{gd}			15	20	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.6 Ω I_D ≅ 30 A, V_{GEN} = 10 V, R_G = 7.5 Ω		9	15	ns
Rise Time[c]	t_r			25	40	
Turn-Off Delay Time[c]	$t_{d(off)}$			27	40	
Fall Time[c]	t_f			25	35	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[b]						
Pulsed Current	I_{SM}				100	A
Diode Forward Voltage	V_{SD}	I_F =6 A, V_{GS} = 0 V		1.1	1.8	V

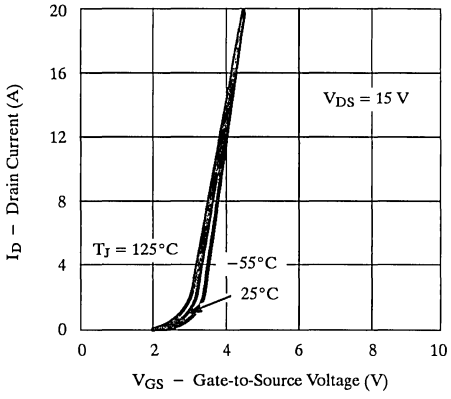
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

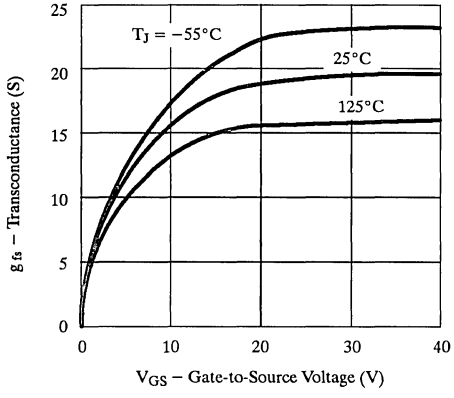
Output Characteristics



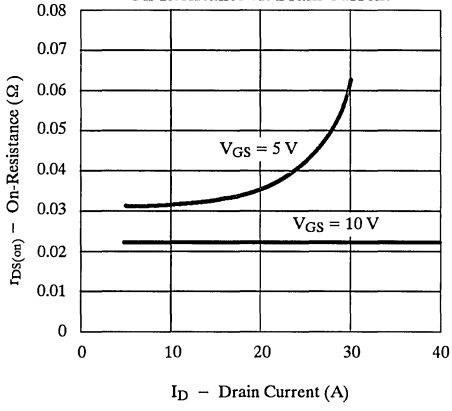
Transfer Characteristics



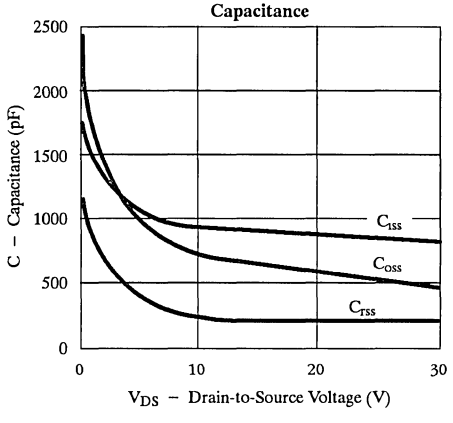
Transconductance



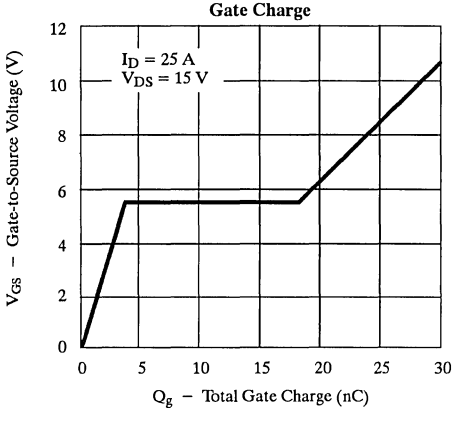
On-Resistance vs. Drain Current



Capacitance

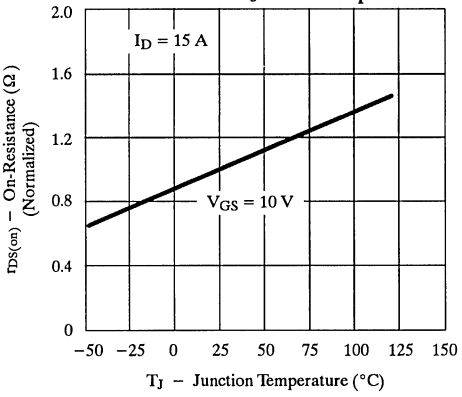


Gate Charge

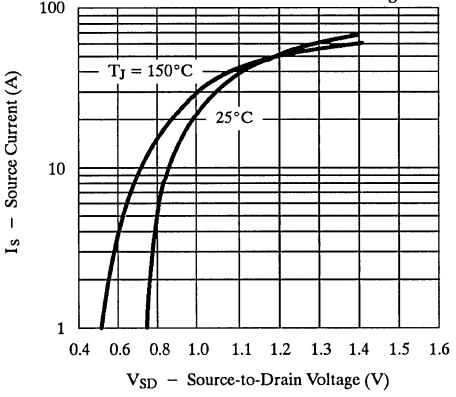


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

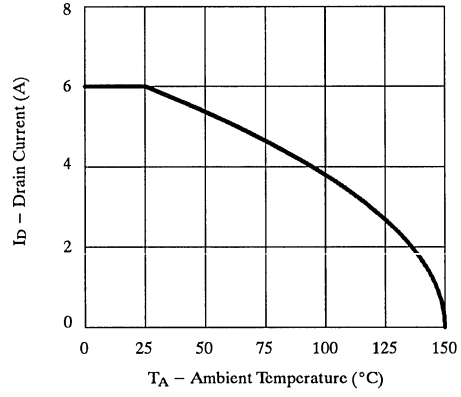


Source-Drain Diode Forward Voltage

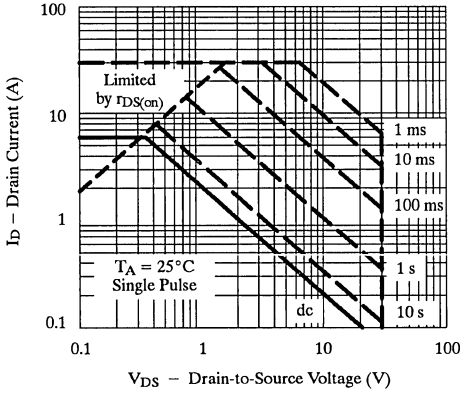


Thermal Ratings

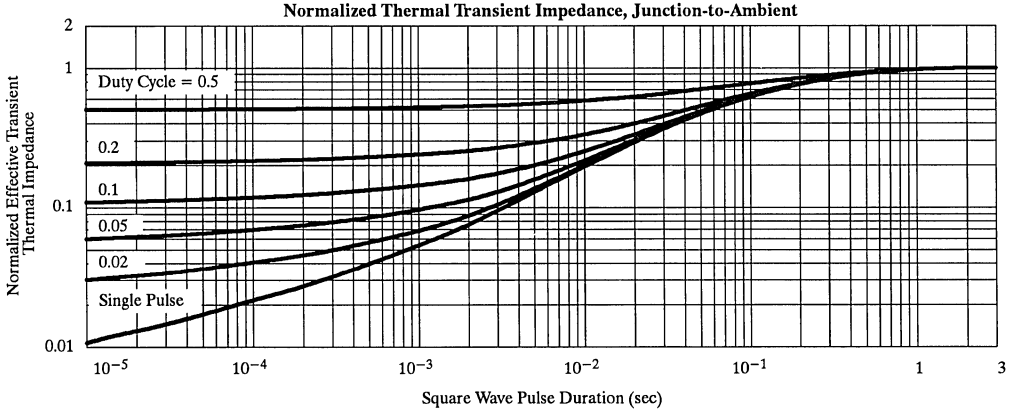
Maximum Avalanche and Drain Current vs. Ambient Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



Siliconix

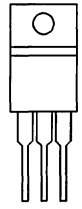
SMP20P10

P-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.20	−20

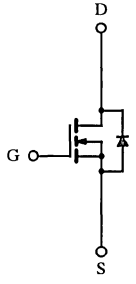
TO-220AB



Drain Connected to Tab

G D S

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−20	A
	T_C = 100°C		−12	
Pulsed Drain Current		I_{DM}	−80	
Avalanche Current		I_{AR}	−20	
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	20	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

Specifications (T_J = 25°C Unless Otherwise Noted)

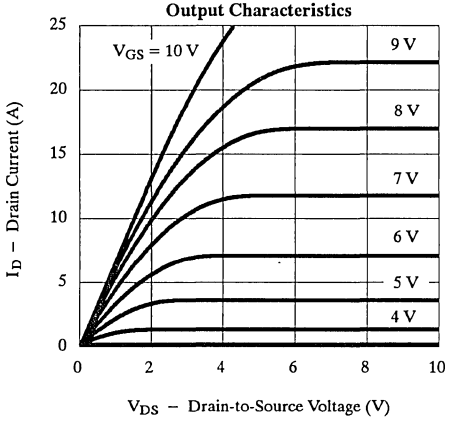
Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−250	µA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−1000	µA
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −12 A		0.15	0.20	Ω
		V_{GS} = −10 V, I_D = −12 A, T_J = 125°C		0.24	0.30	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −12 A	4.8	6.7		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			700		pF
Reverse Transfer Capacitance	C_{rss}			250		pF
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = −10 V, I_D = −20 A		47	60	nC
Gate-Source Charge[c]	Q_{gs}			10	18	nC
Gate-Drain Charge[c]	Q_{gd}			27	36	nC
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −40 V, R_L = 2.1 Ω, I_D ≅ −19 A, V_{GEN} = −10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			50	80	ns
Turn-Off Delay Time[c]	$t_{d(off)}$			25	80	ns
Fall Time[c]	t_f			15	60	ns
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−20	A
Pulsed Current	I_{SM}				−80	A
Diode Forward Voltage[b]	V_{SD}	I_F = −20 A, V_{GS} = 0 V			−1.7	V
Reverse Recovery Time	t_{rr}	I_F = −20 A, di/dt = 100 A/µs		150		ns
Reverse Recovery Charge	Q_{rr}			0.3		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

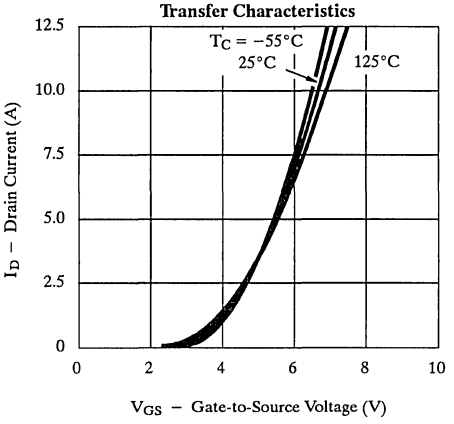
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

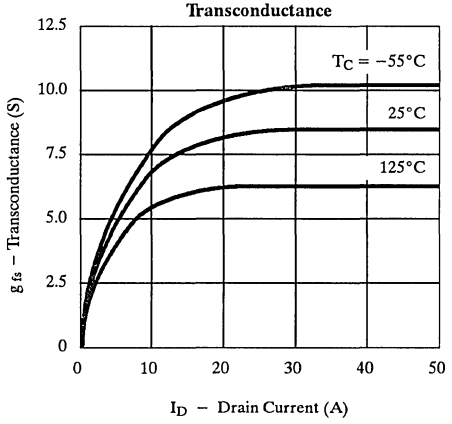
Output Characteristics



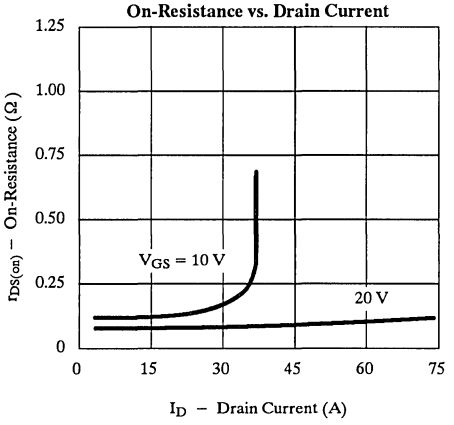
Transfer Characteristics



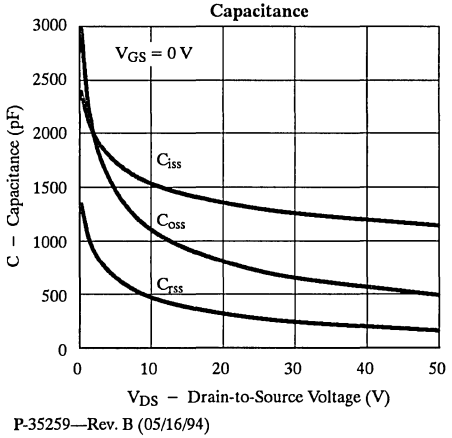
Transconductance



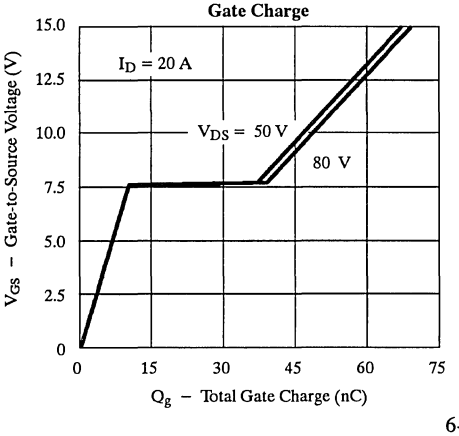
On-Resistance vs. Drain Current



Capacitance



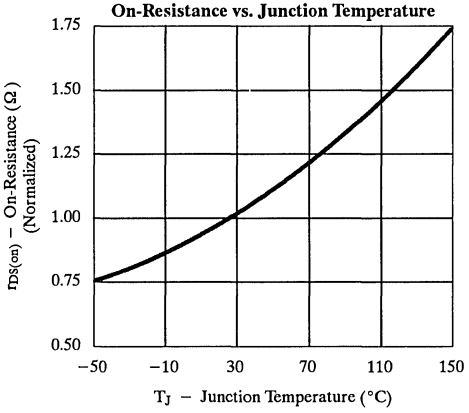
Gate Charge



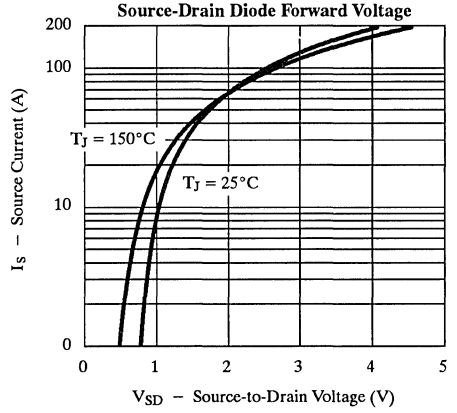
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

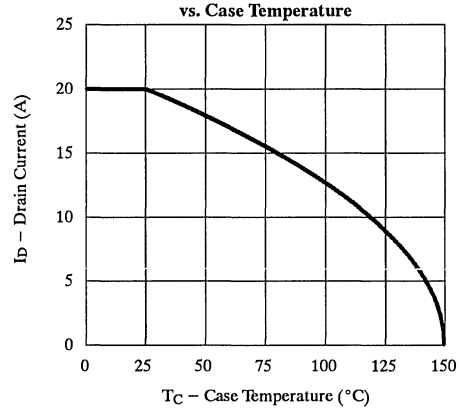


Source-Drain Diode Forward Voltage

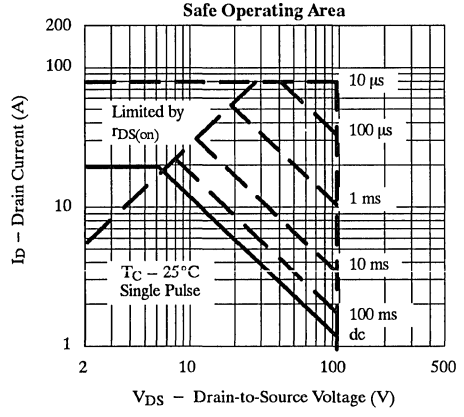


Thermal Ratings

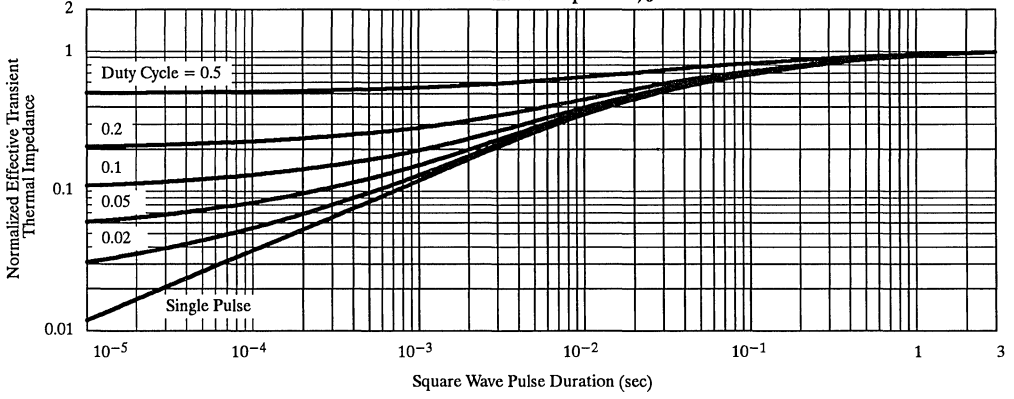
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SMP25N05-45L

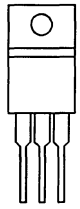
N-Channel Enhancement-Mode Transistor, Logic Level

175°C Maximum Junction Temperature

Product Summary

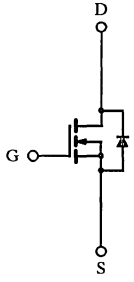
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
50	0.045 @ V_{GS} = 10 V	25
	0.060 @ V_{GS} = 4.25 V	25

TO-220AB



Drain Connected to Tab

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	16	V
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	25	A
	T_C = 100°C		±16	
Pulsed Drain Current		I_{DM}	100	
Avalanche Current (see Thermal Ratings, page 6-104)		I_{AR}	25	
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	31	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		36	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.08	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

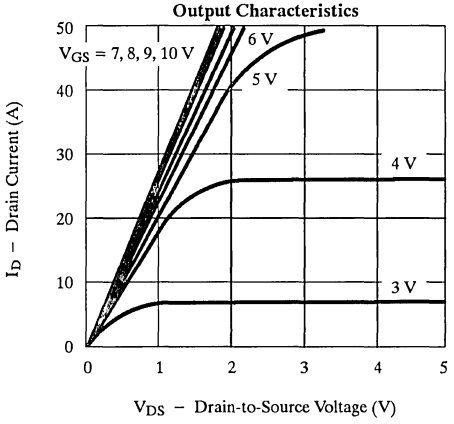
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.0	1.5	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C			100	
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 2 V, V_{GS} = 10 V	25			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 12.5 A		0.035	0.045	Ω
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C		0.060	0.080	
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 175°C		0.062	0.085	
		V_{GS} = 4.25 V, I_D = 12.5 A		0.045	0.060	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 12.5 A		19		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		950		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			110		
Total Gate Charge[c]	Q_g	V_{DS} = 25 V, V_{GS} = 10 V, I_D = 25 A		22		nC
Gate-Source Charge[c]	Q_{gs}			5		
Gate-Drain Charge[c]	Q_{gd}			10		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 25 V, R_L = 1 Ω I_D ≅ 25 A, V_{GEN} = 10 V, R_G = 7.5 Ω		10	20	ns
Rise Time[c]	t_r			25	40	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	60	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				25	A
Pulsed Current	I_{SM}				100	
Diode Forward Voltage[b]	V_{SD}	I_F = 25 A, V_{GS} = 0 V		1.0	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 25 A, di/dt = 100 A/µs		120		ns
Peak Reverse Recovery Current	$I_{RM(rec)}$					A
Reverse Recovery Charge	Q_{rr}			0.42		µC

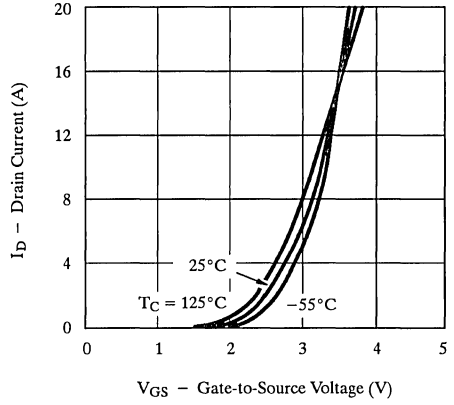
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

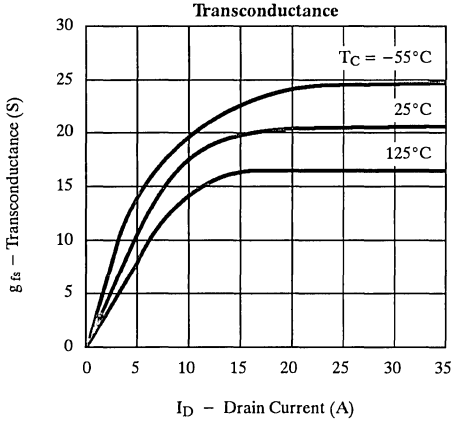
Output Characteristics



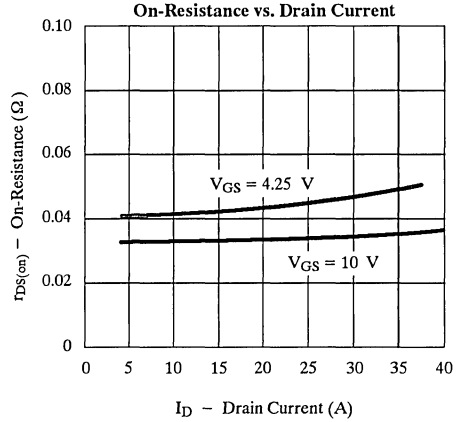
Transfer Characteristics



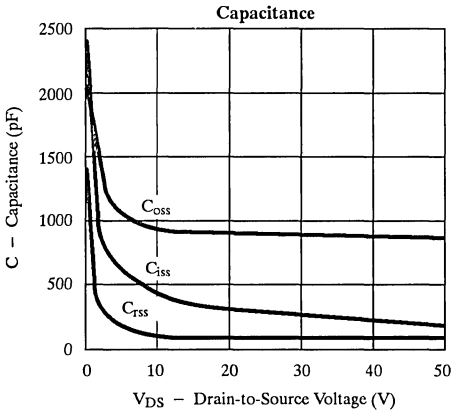
Transconductance



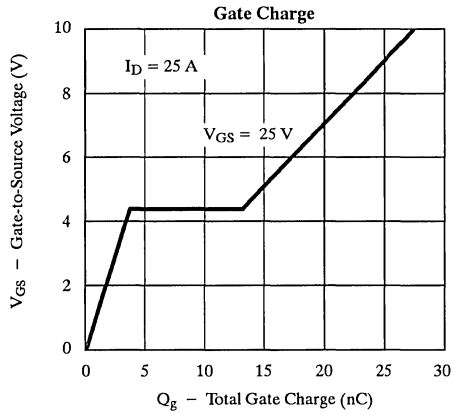
On-Resistance vs. Drain Current



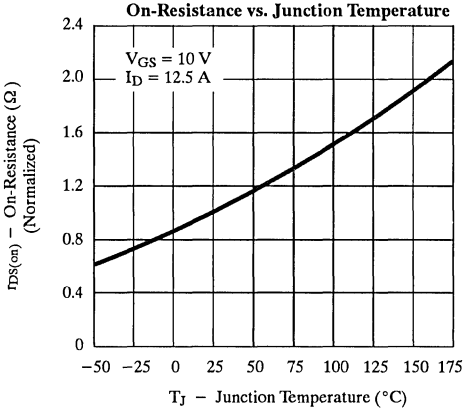
Capacitance

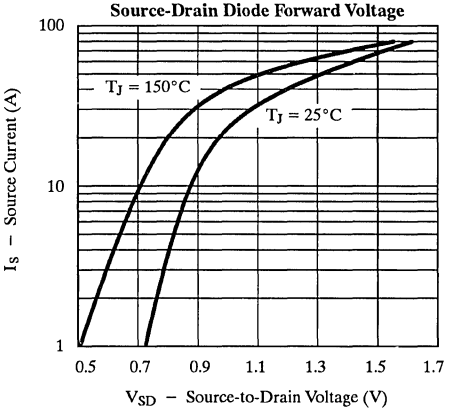


Gate Charge

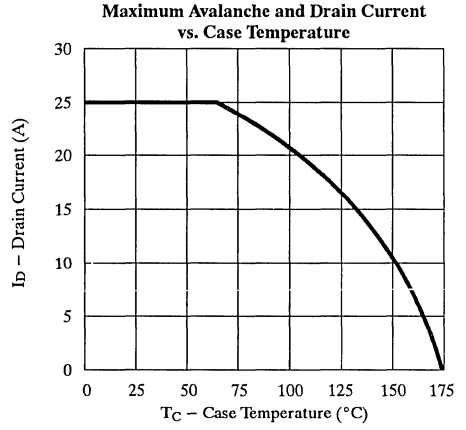


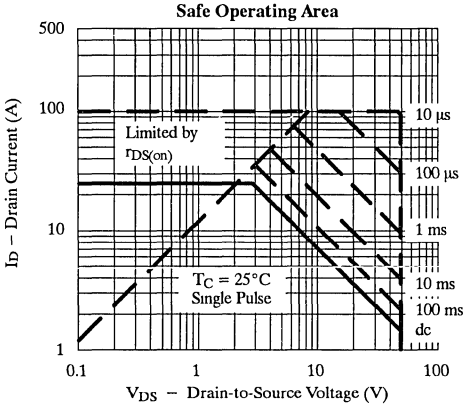
Typical Characteristics (25°C Unless Otherwise Noted)

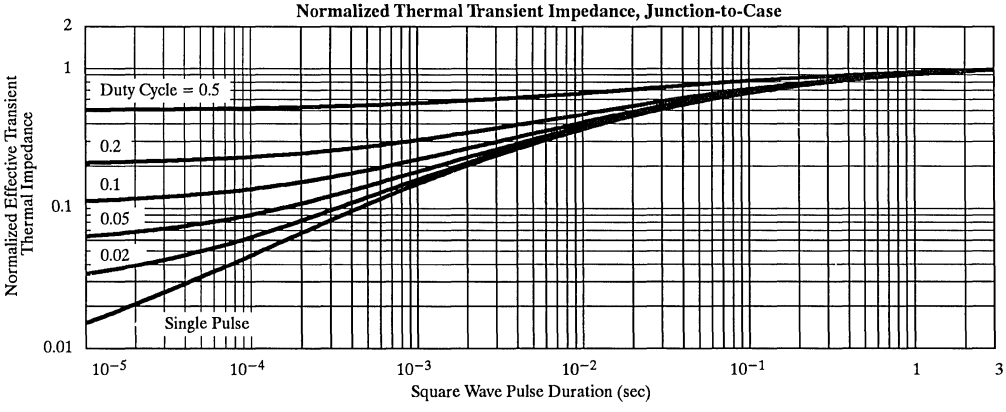




Thermal Ratings







Siliconix

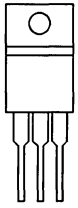
SMP30N10

N-Channel Enhancement-Mode Transistor

Product Summary

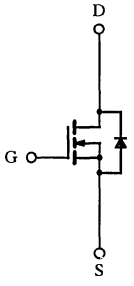
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.060	30

TO-220AB



DRAIN connected to TAB

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		18	
Pulsed Drain Current		I_{DM}	120	
Avalanche Current		I_{AR}	30	
Avalanche Energy	L = 0.3 mH	E_A	135	mJ
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	45	
Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.25	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

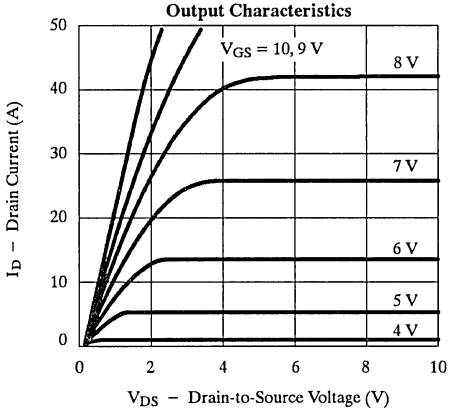
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100	110		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A		0.045	0.060	Ω
		V_{GS} = 10 V, I_D = 18 A, T_J = 125°C		0.085	0.100	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 18 A	7.0	10.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1400		pF
Output Capacitance	C_{oss}			480		
Reverse Transfer Capacitance	C_{rss}			110		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 30 A		35	50	nC
Gate-Source Charge[c]	Q_{gs}			10	19	
Gate-Drain Charge[c]	Q_{gd}			15	25	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.67 Ω I_D ≅ 30 A, V_{GEN} = 10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			80	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	60	
Fall Time[c]	t_f			15	30	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				30	A
Pulsed Current	I_{SM}				120	
Forward Voltage[b]	V_{SD}	I_F = 30 A, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}			130		ns
Reverse Recovery Charge	Q_{rr}			0.45		µC

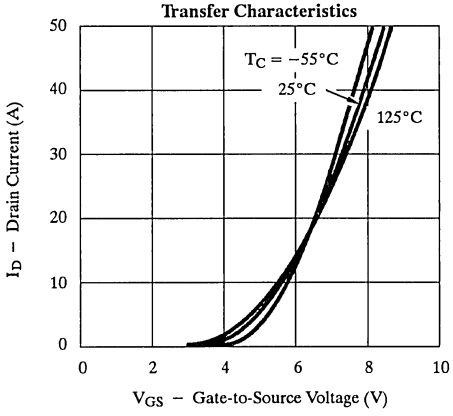
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

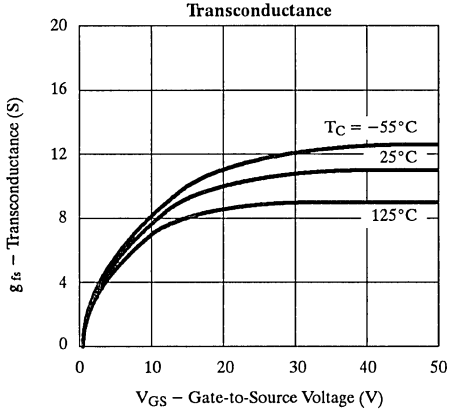
Output Characteristics



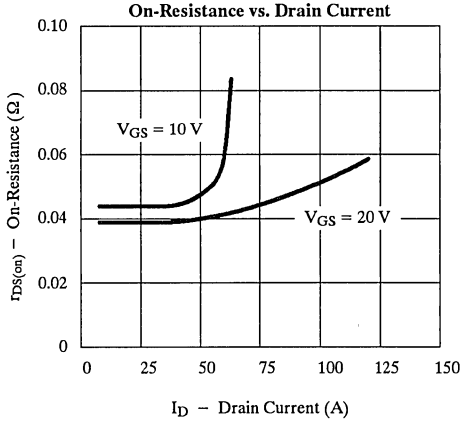
Transfer Characteristics



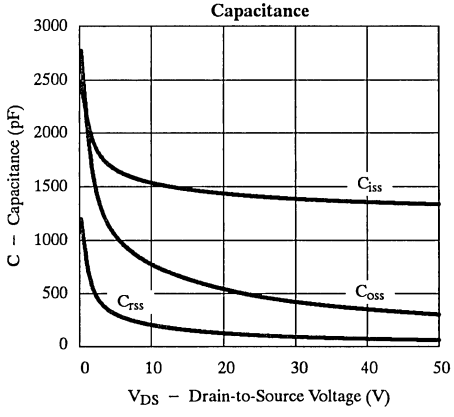
Transconductance



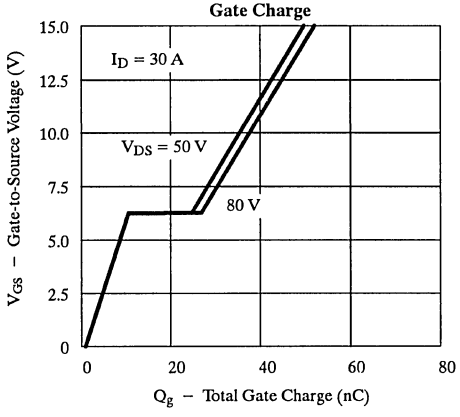
On-Resistance vs. Drain Current



Capacitance

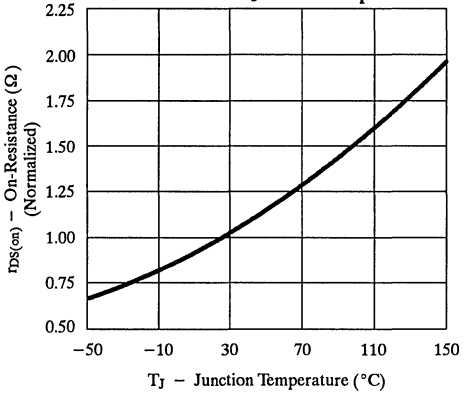


Gate Charge

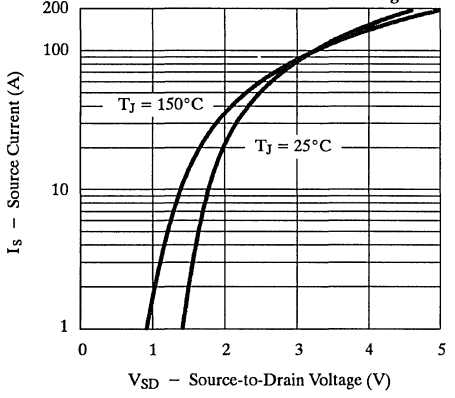


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

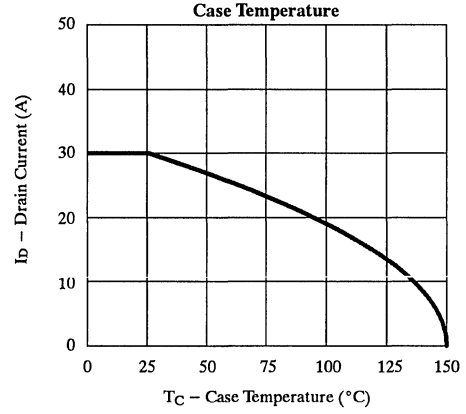


Source-Drain Diode Forward Voltage

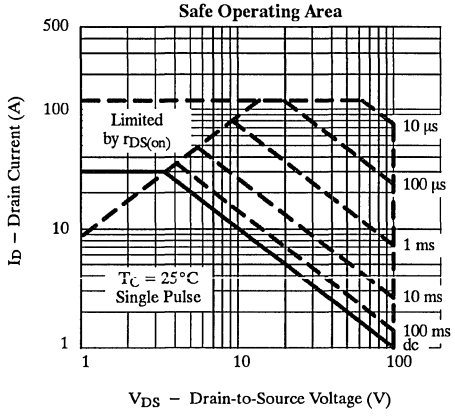


Thermal Ratings

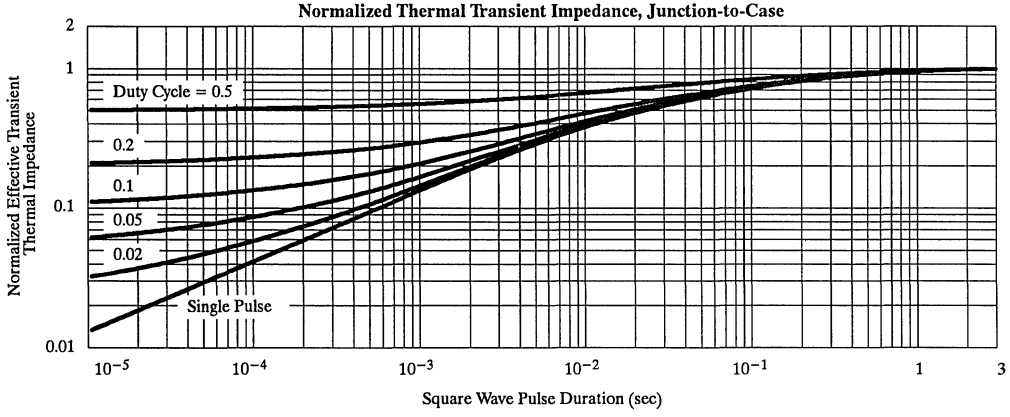
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

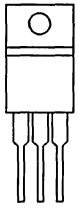
SMP40N10

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.040	40

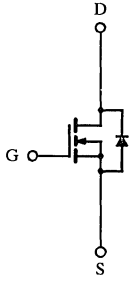
TO-220AB



DRAIN connected to TAB

G D S

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	40	A
	T_C = 100°C		25	
Pulsed Drain Current		I_{DM}	160	
Avalanche Current		I_{AR}	40	
Avalanche Energy	L = 0.3 mH	E_A	240	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	40	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤1%

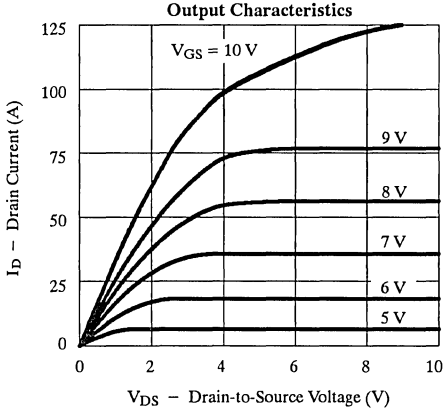
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		0.030	0.040	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		0.055	0.072	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 25 A	15	20		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3000		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 40 A		62	80	nC
Gate-Source Charge[c]	Q_{gs}			20	30	
Gate-Drain Charge[c]	Q_{gd}			26	35	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.25 Ω I_D ≅ 40 A, V_{GEN} = 10 V, R_G = 5 Ω		17	30	ns
Rise Time[c]	t_r			80	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			40	60	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				40	A
Pulsed Current	I_{SM}				180	
Forward Voltage[b]	V_{SD}	I_F = 40 A, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}			120	250	ns
Reverse Recovery Charge	Q_{rr}			0.3		µC

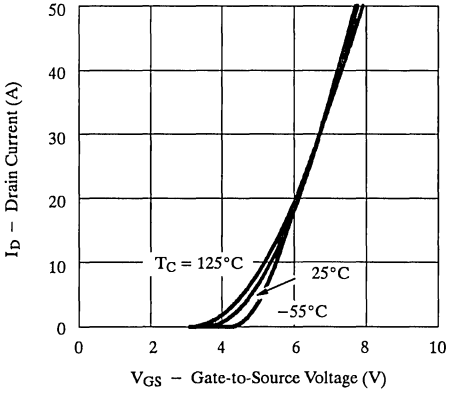
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

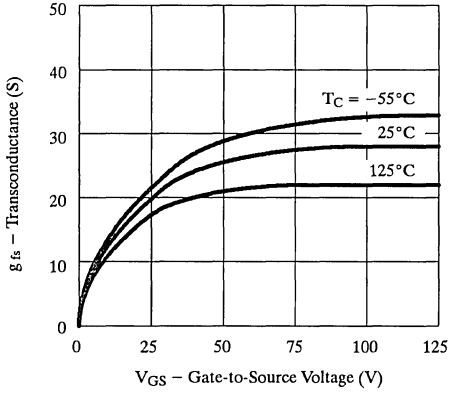
Output Characteristics



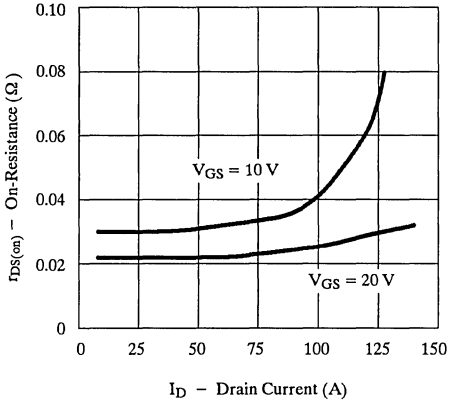
Transfer Characteristics



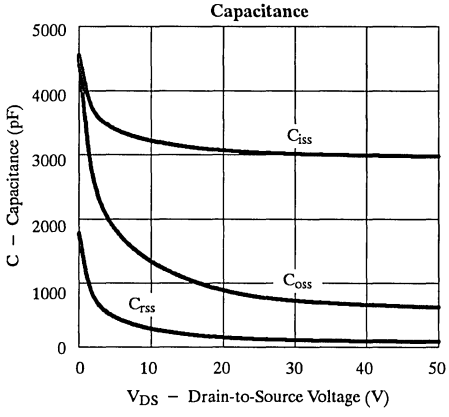
Transconductance



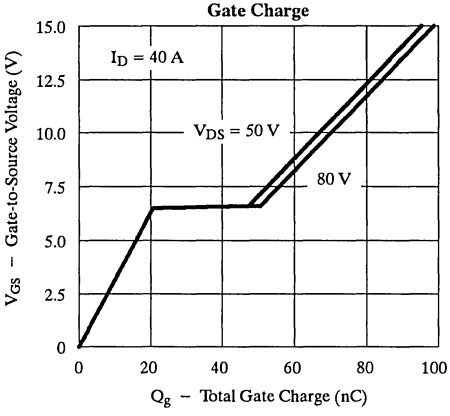
On-Resistance vs. Drain Current



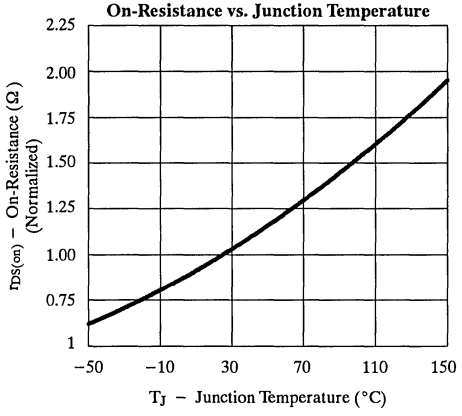
Capacitance

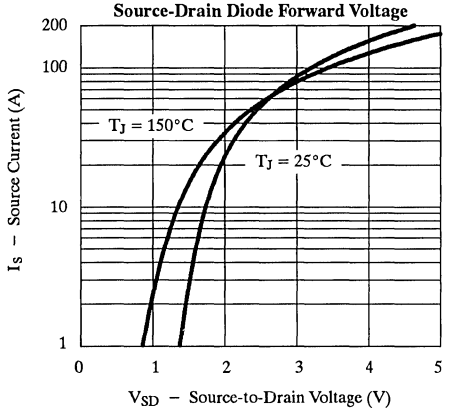


Gate Charge

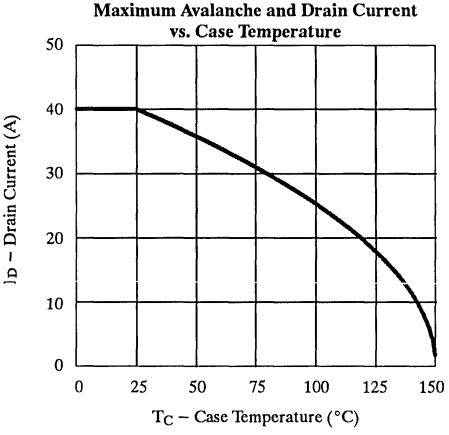


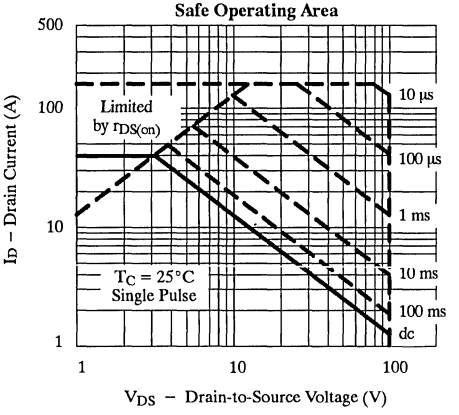
Typical Characteristics (25°C Unless Otherwise Noted)

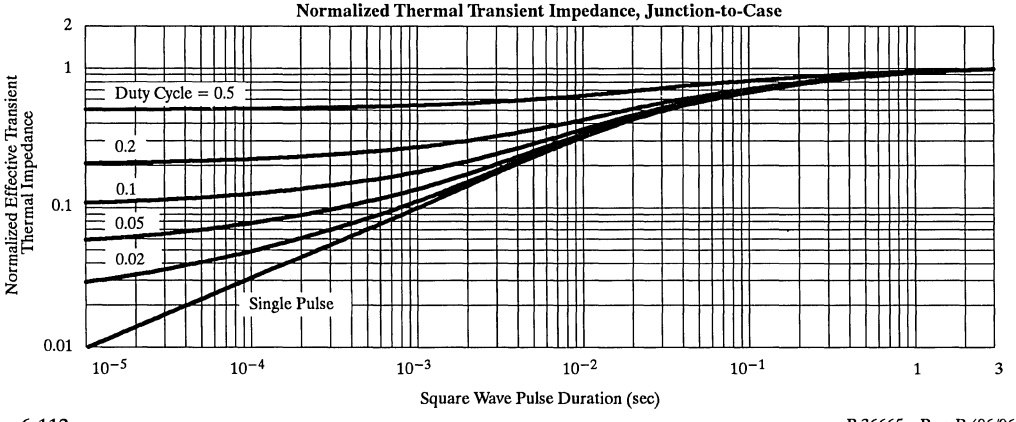




Thermal Ratings







Siliconix

SMP40P06

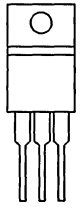
P-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−60	0.045	−40

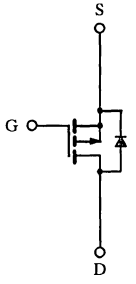
TO-220AB



DRAIN connected to TAB

G D S

Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	−40	A
	T_C = 100°C		−30	
Pulsed Drain Current		I_{DM}	−100	
Avalanche Current		I_{AR}	−40	
Avalanche Energy	L = 0.1 mH	E_{AS}	90	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	45	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		62	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.2	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%.

Specifications (T_J = 25°C Unless Otherwise Noted)

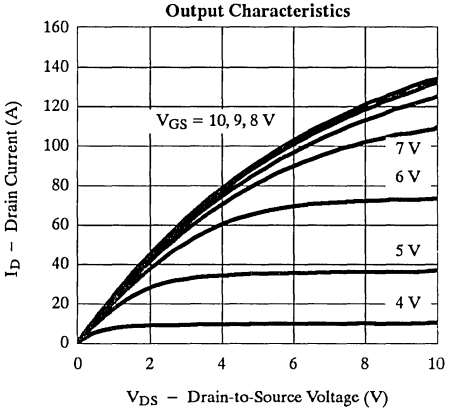
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−1		−3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −48 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 125°C			−250	
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 175°C			−500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} −10 V, I_D = −20 A		0.038	0.045	Ω
		V_{GS} = −10 V, I_D = −20 A, T_J = 125°C			0.080	
		V_{GS} = −10 V, I_D = −20 A, T_J = 175°C			0.090	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −20 A		28		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		2600		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge[c]	Q_g	V_{DS} = −30 V, V_{GS} = −10 V, I_D = −40 A		60	100	nC
Gate-Source Charge[c]	Q_{gs}			15	20	
Gate-Drain Charge[c]	Q_{gd}			17	50	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 1.5 Ω I_D ≅ −20 A, V_{GEN} = −10 V, R_G = 2.5 Ω		11	30	ns
Rise Time[c]	t_r			12	35	
Turn-Off Delay Time[c]	$t_{d(off)}$			70	140	
Fall Time[c]	t_f			75	150	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				−40	A
Pulsed Current	I_{SM}				−100	
Forward Voltage[b]	V_{SD}	I_F = −40 A, V_{GS} = 0 V		−1.2	−1 6	V
Reverse Recovery Time	t_{rr}	I_F = −40 A, dI_F/dt = 100 A/µs		81		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			7		A
Reverse Recovery Charge	Q_{rr}			0.3		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

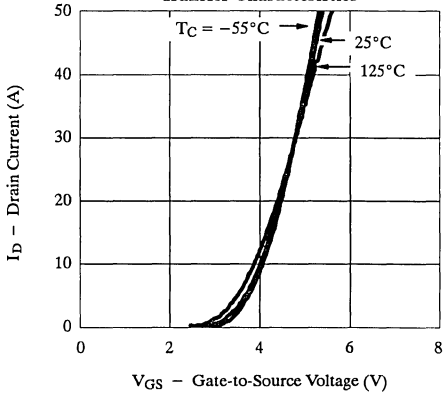
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

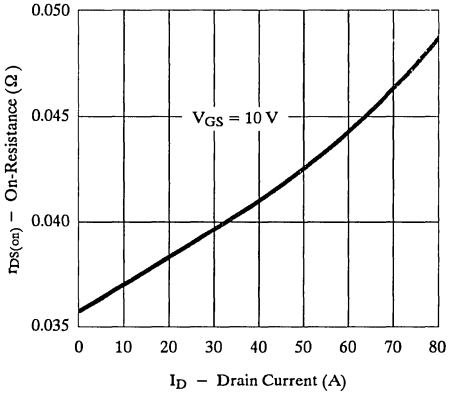
Output Characteristics



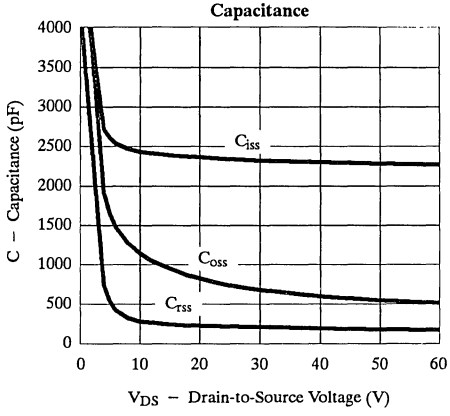
Transfer Characteristics



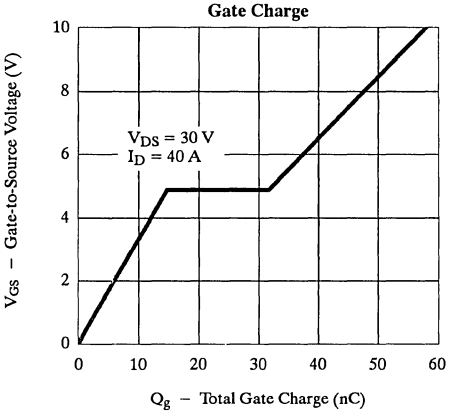
On-Resistance vs. Drain Current



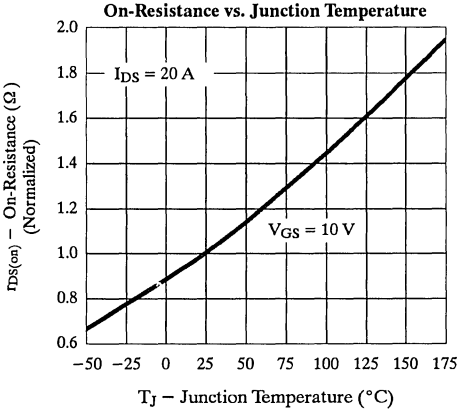
Capacitance



Gate Charge



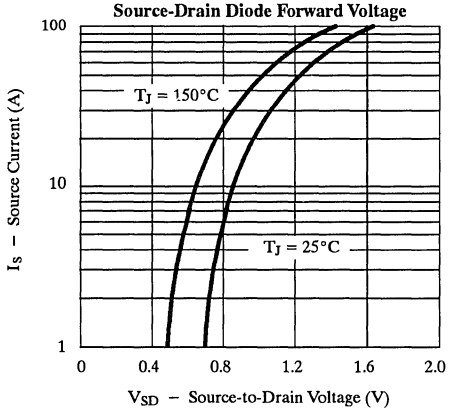
On-Resistance vs. Junction Temperature



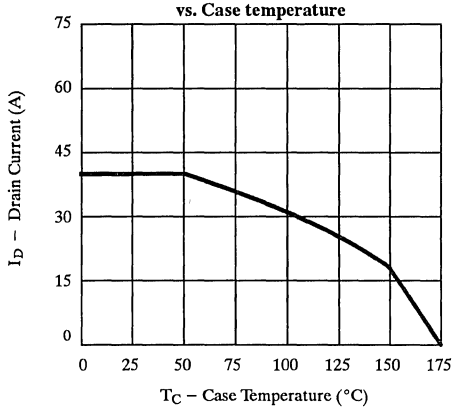
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

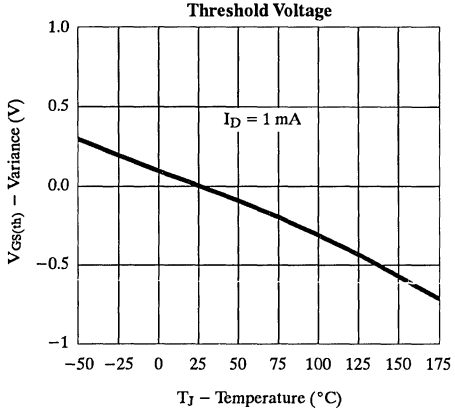
Source-Drain Diode Forward Voltage



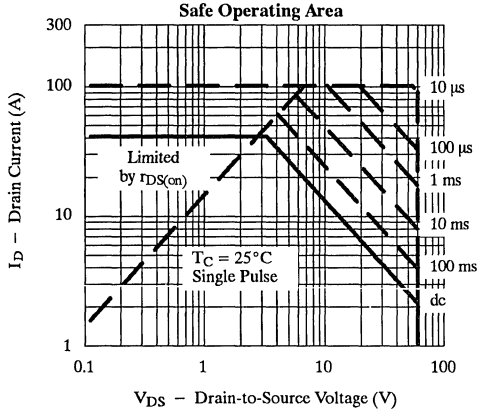
Maximum Avalanche and Drain Current vs. Case temperature



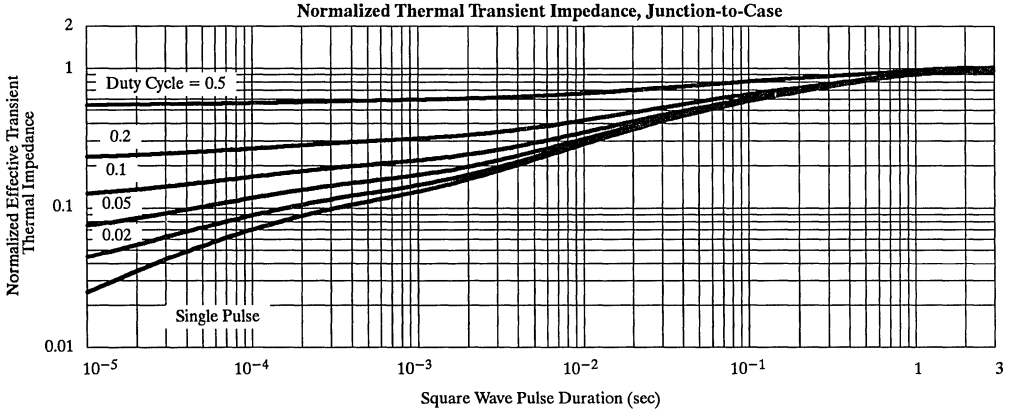
Threshold Voltage



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SMP50N06-25

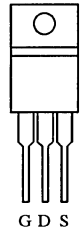
N-Channel Enhancement-Mode MOSFET, 25-mΩ $r_{DS(on)}$

175°C Maximum Junction Temperature

Product Summary

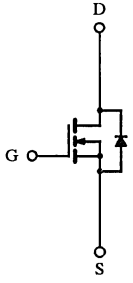
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.025	46

TO-220AB



DRAIN connected to TAB

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	46	A
	T_C = 100°C		32	
Pulsed Drain Current		I_{DM}	200	
Continuous Source Current (Diode Conduction)		I_S	46	
Avalanche Current		I_{AR}	46	
Avalanche Energy	L = 0.1 mH	E_{AS}	125	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	62.5	
Maximum Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		53	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		1.4	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

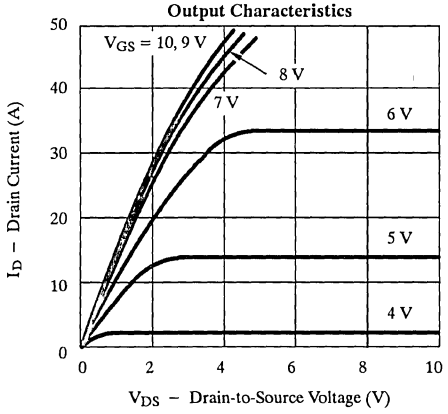
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2		4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	46			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		0.020	0.025	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		0.033	0.042	
		V_{GS} = 10 V, I_D = 25 A, T_J = 175°C		0.043	0.0525	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 25 A		20		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2000		nC
Output Capacitance	C_{oss}			570		
Reverse Transfer Capacitance	C_{rss}			120		
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 50 A		55	80	
Gate-Source Charge	Q_{gs}			9	15	
Gate-Drain Charge	Q_{gd}			24	40	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.6 Ω I_D ≅ 50 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	30	ns
Rise Time	t_r			20	35	
Turn-Off Delay Time	$t_{d(off)}$			40	65	
Fall Time	t_f			15	30	
Source-Drain Diode Ratings and Characteristics						
Diode Forward Voltage[b]	V_{SD}	I_F = 46 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 46 A, di/dt = 100 A/µs		130		ns
Peak Reverse Recovery Current	$I_{RM(rec)}$			10		A
Reverse Recovery Charge	Q_{rr}			0.7		µC

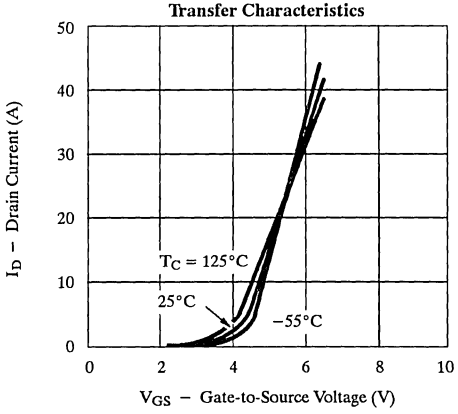
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

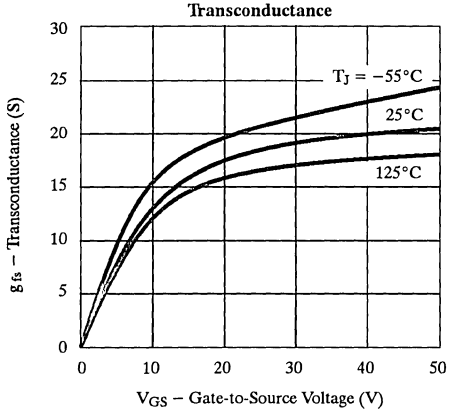
Output Characteristics



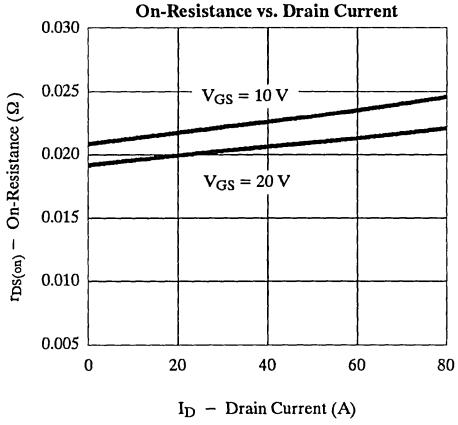
Transfer Characteristics



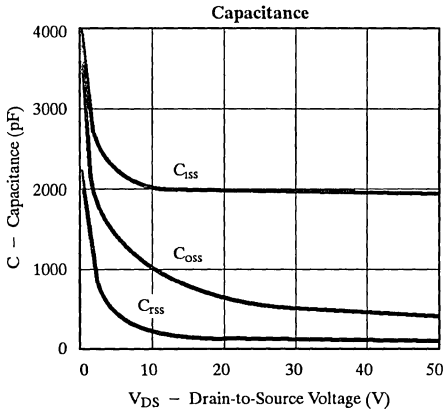
Transconductance



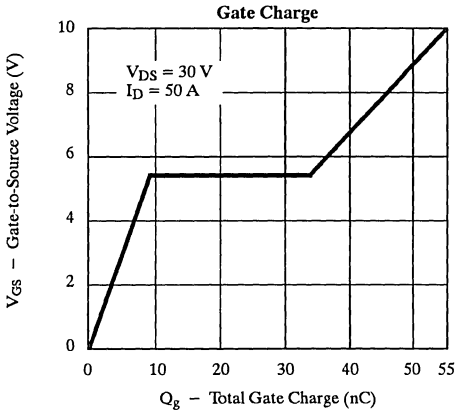
On-Resistance vs. Drain Current



Capacitance

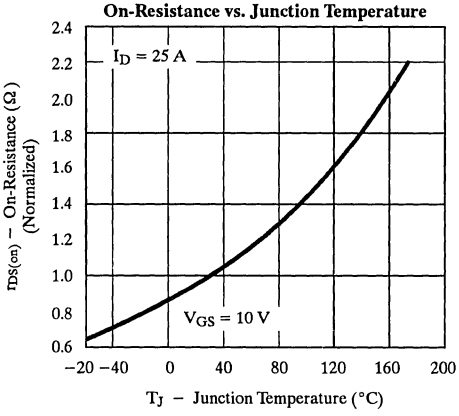


Gate Charge

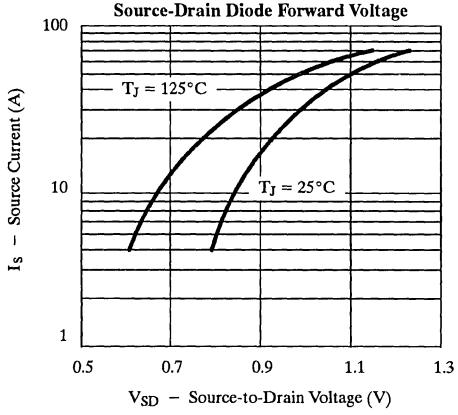


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

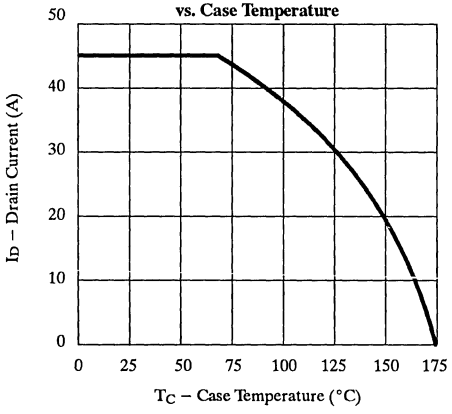


Source-Drain Diode Forward Voltage

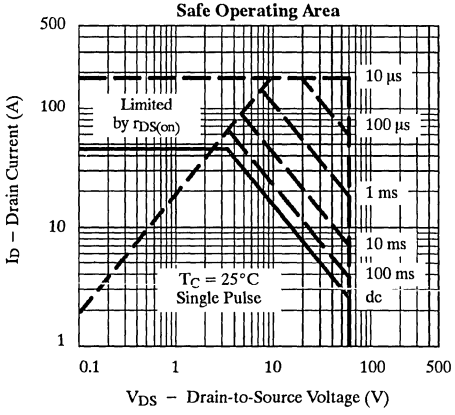


Thermal Ratings

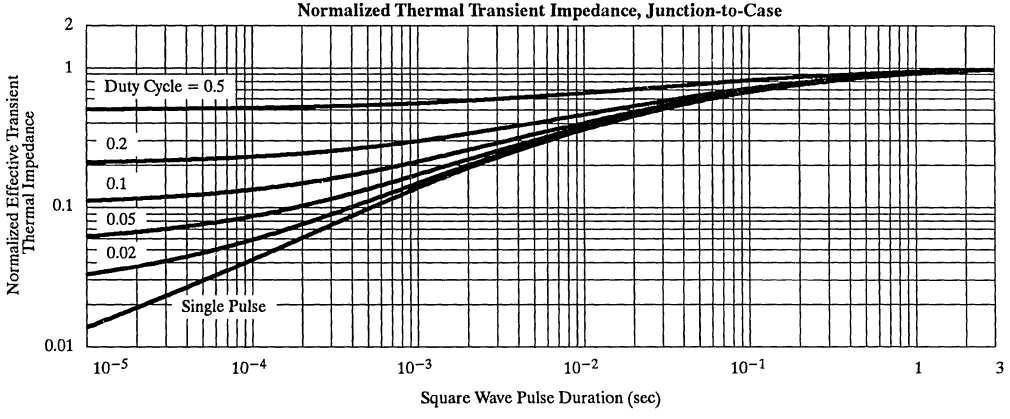
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

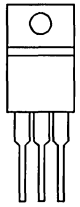
SMP60N03-10L

N-Channel Enhancement-Mode Transistor, Logic Level

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.01	60

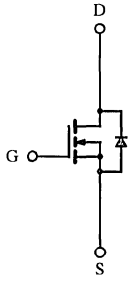
TO-220AB



DRAIN connected to TAB

G D S

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		51	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.2	
Case-to-Sink	R_{thCS}	1 0		

Notes:
a. Duty cycle ≤ 1%

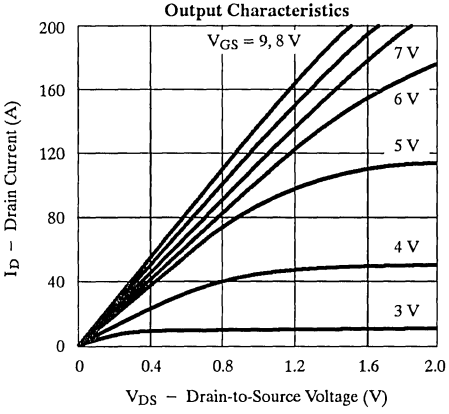
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	0.8		3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			25	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.007	0.010	Ω
		V_{GS} = 5 V, I_D = 30 A		0.010	0.015	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		0.009	0.014	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		45		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2600		pF
Output Capacitance	C_{oss}			1500		
Reverse Transfer Capacitance	C_{rss}			750		
Total Gate Charge[c]	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 60 A		100	120	nC
Gate-Source Charge[c]	Q_{gs}			10	15	
Gate-Drain Charge[c]	Q_{gd}			45	75	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≅ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω		14	30	ns
Rise Time[c]	t_r			25	50	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	100	
Fall Time[c]	t_f			45	80	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, dI_F/dt = 100 A/µs		160		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			13		A
Reverse Recovery Charge	Q_{rr}			1.0		µC

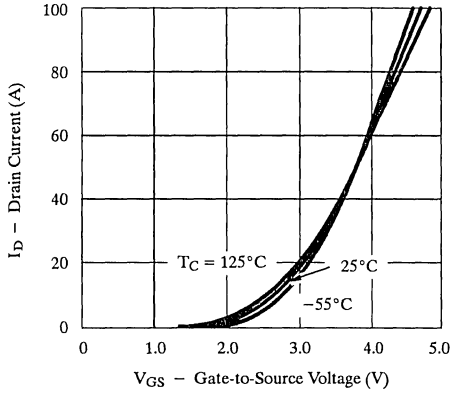
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

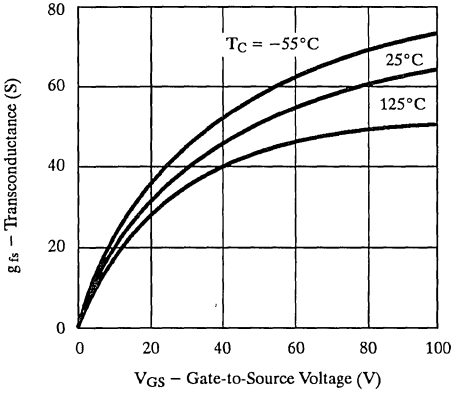
Output Characteristics



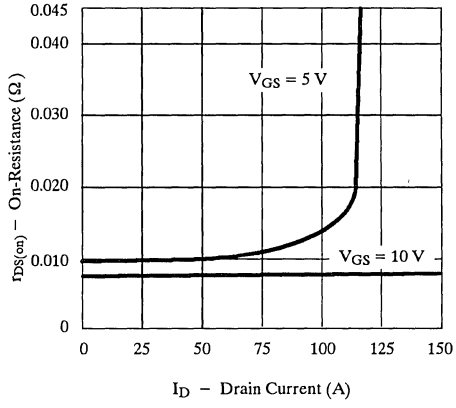
Transfer Characteristics



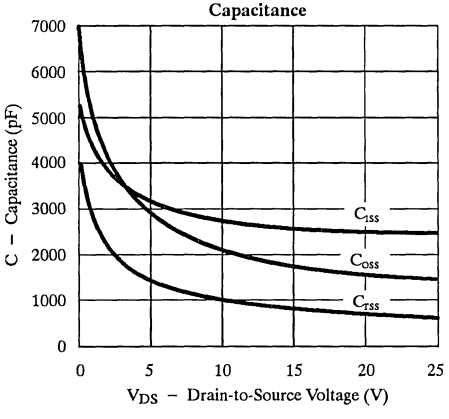
Transconductance



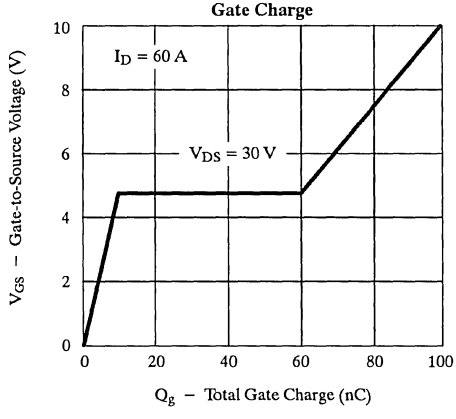
On-Resistance vs. Drain Current



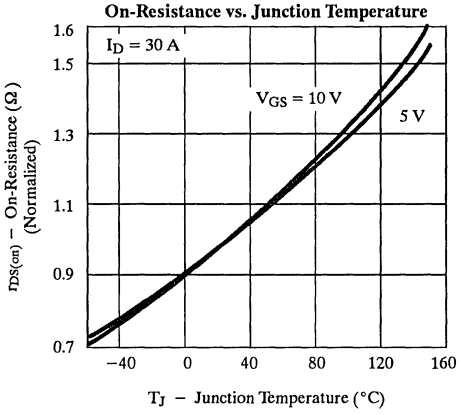
Capacitance

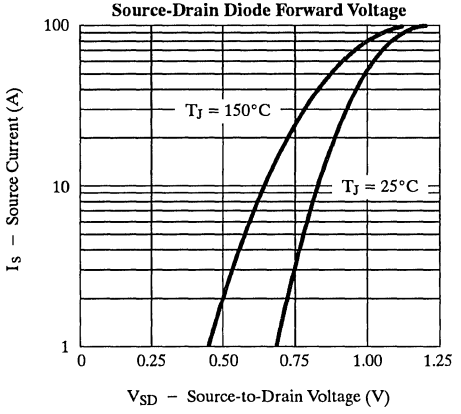


Gate Charge

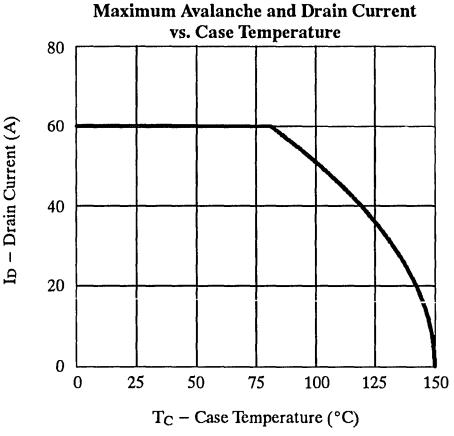


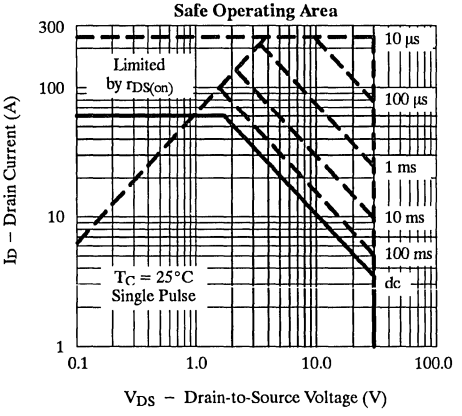
Typical Characteristics (25°C Unless Otherwise Noted)

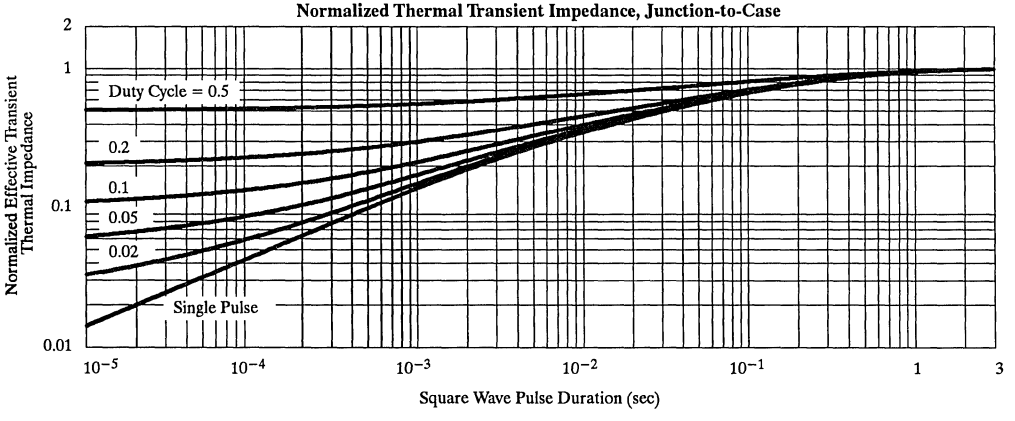




Thermal Ratings







Siliconix

SMP60N06-14

N-Channel Enhancement-Mode Transistor

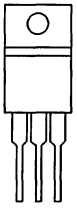
175°C Maximum Junction Temperature

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.014	60

See lower-cost version: SUP60N06-14

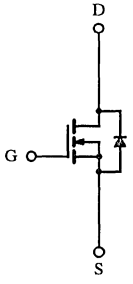
TO-220AB



DRAIN connected to TAB

G D S

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	60	A
	T_C = 100°C		50	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current[a]		I_{AR}	60	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature (1/16" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤1%

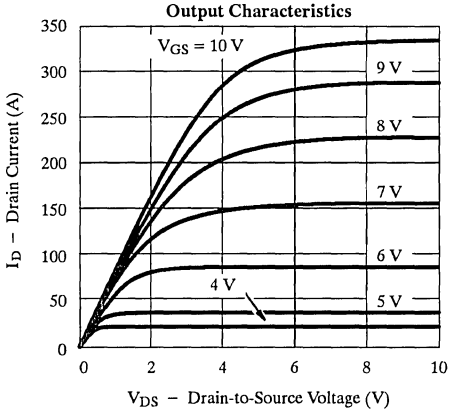
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 1 mA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.012	0.014	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		0.020	0.023	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C		0.025	0.028	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	30	48		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3450		pF
Output Capacitance	C_{oss}			1000		
Reversen Transfer Capacitance	C_{rss}			230		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		95	130	nC
Gate-Source Charge[c]	Q_{gs}			20		
Gate-Drain Charge[c]	Q_{gd}			45		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≃ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	30	ns
Rise Time[c]	t_r			130	180	
Turn-Off Delay Time[c]	$t_{d(off)}$			50	100	
Fall Time[c]	t_f			20	50	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_s				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V		1.0	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, dI_F/dt = 100 A/µs		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			9		A
Reverse Recovery Charge	Q_{rr}			0.6		µC

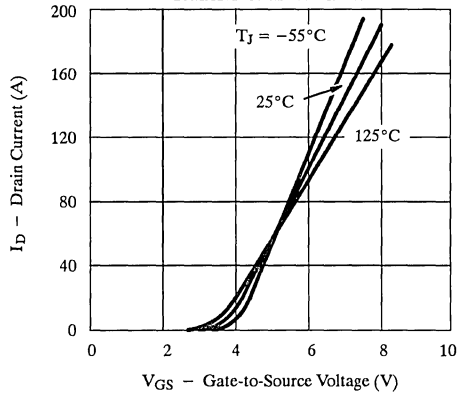
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

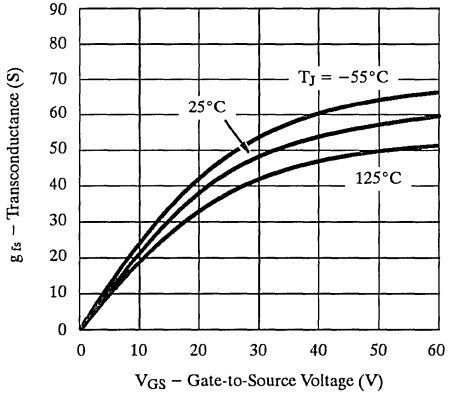
Output Characteristics



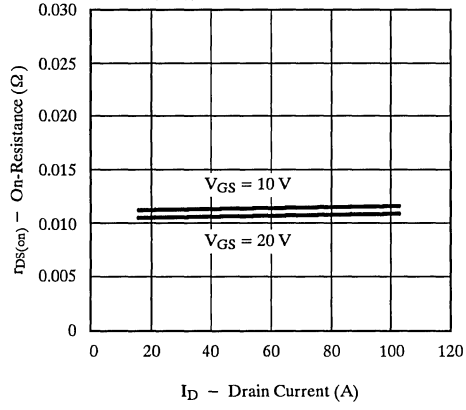
Transfer Characteristics



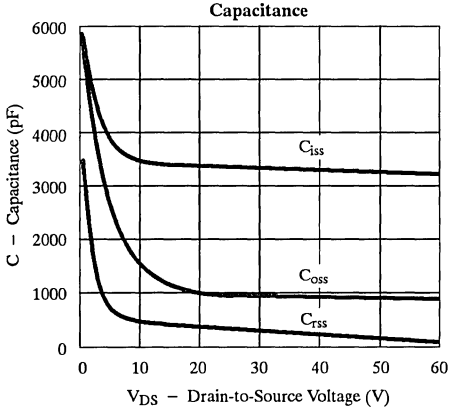
Transconductance



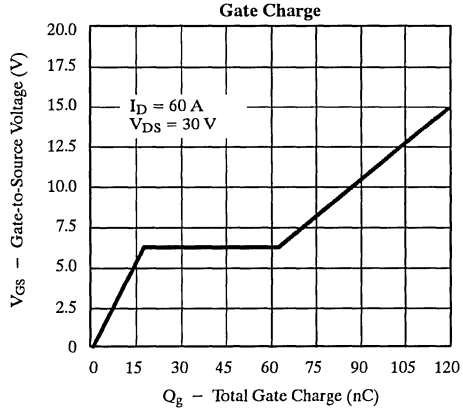
On-Resistance vs. Drain Current



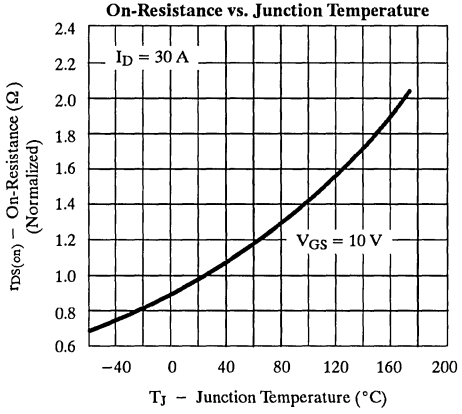
Capacitance

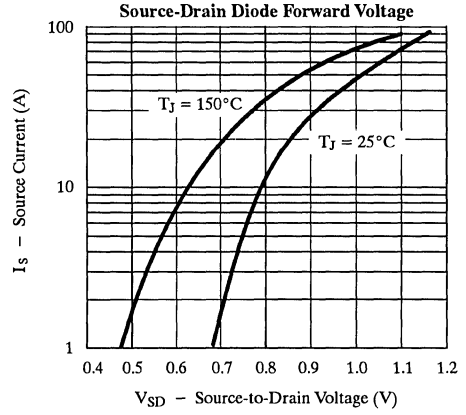


Gate Charge

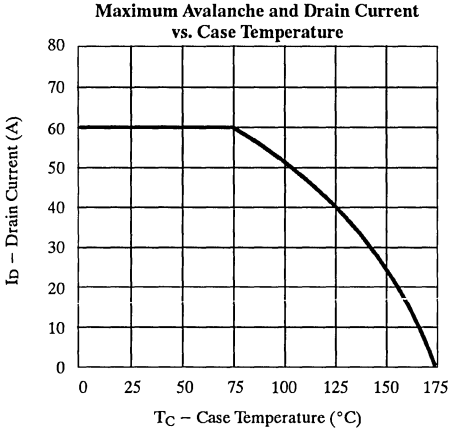


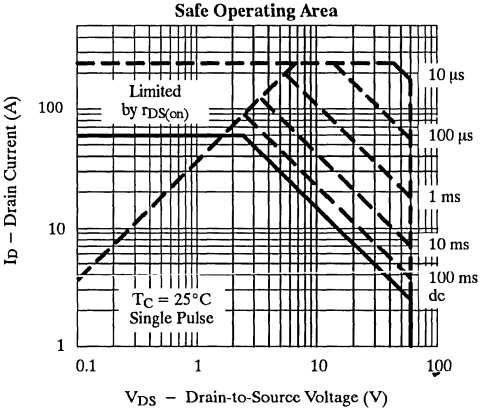
Typical Characteristics (25°C Unless Otherwise Noted)

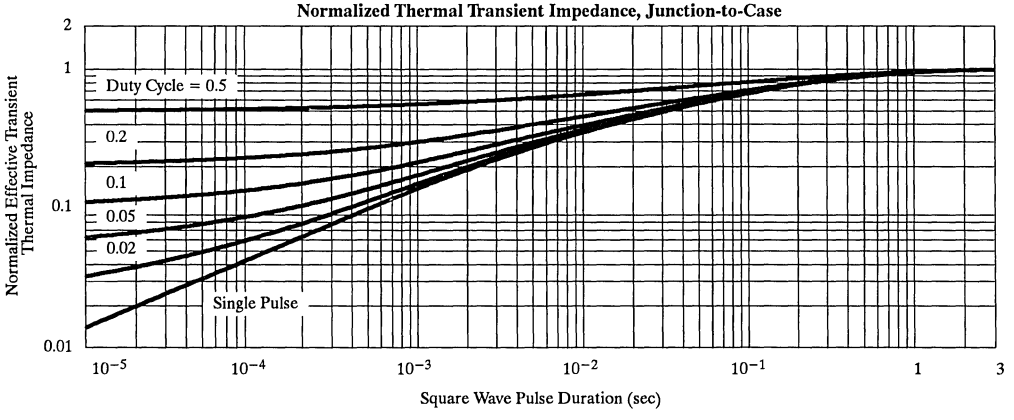




Thermal Ratings







Siliconix

SMP60N06-18

N-Channel Enhancement-Mode Transistor, 18-mΩ $r_{DS(on)}$

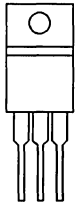
175°C Maximum Junction Temperature[a]

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.018	60

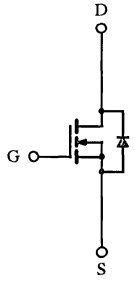
See lower-cost version: SUP50N06-18

TO-220AB



DRAIN connected to TAB

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		41	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	I_{AR}	180	mJ
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		62	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C
Lead Temperature (1/16" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.2	
Case-to-Sink	R_{thCS}	1.0		

Notes.
a. Duty cycle ≤ 1%

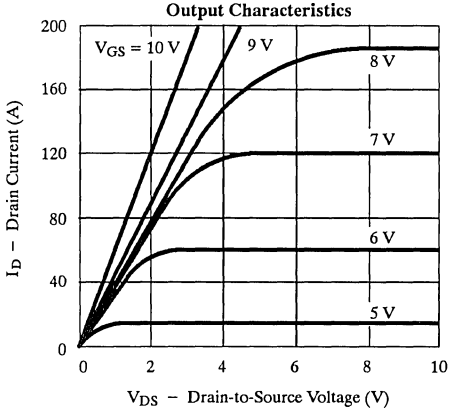
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 1 mA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.013	0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		0.023	0.030	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C		0.026	0.036	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		45		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2600		pF
Output Capacitance	C_{oss}			800		
Reversen Transfer Capacitance	C_{rss}			200		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		85	100	nC
Gate-Source Charge[c]	Q_{gs}			15	20	
Gate-Drain Charge[c]	Q_{gd}			35	50	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≅ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	30	ns
Rise Time[c]	t_r			20	35	
Turn-Off Delay Time[c]	$t_{d(off)}$			50	65	
Fall Time[c]	t_f			20	30	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_s				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, dI_F/dt = 100 A/µs		160		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			13		A
Reverse Recovery Charge	Q_{rr}			1.0		µC

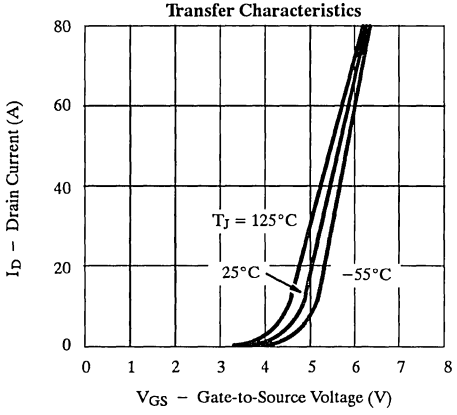
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

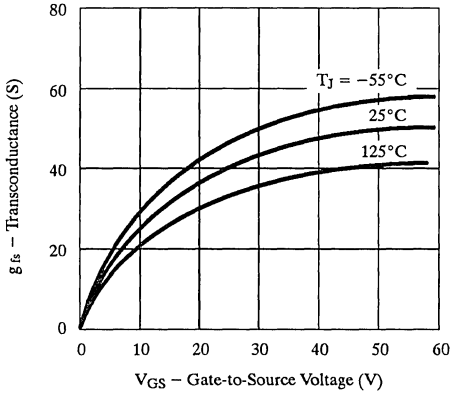
Output Characteristics



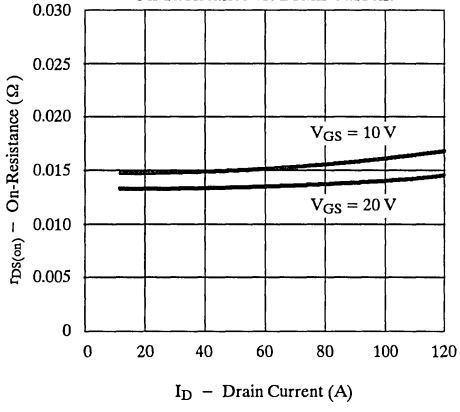
Transfer Characteristics



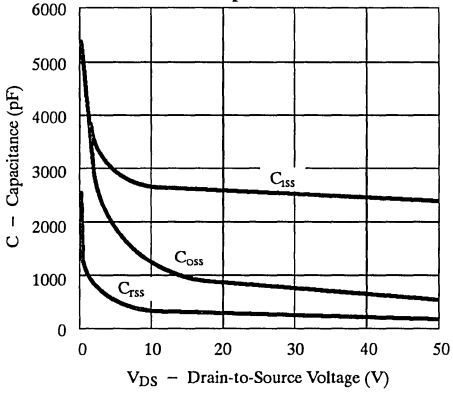
Transconductance



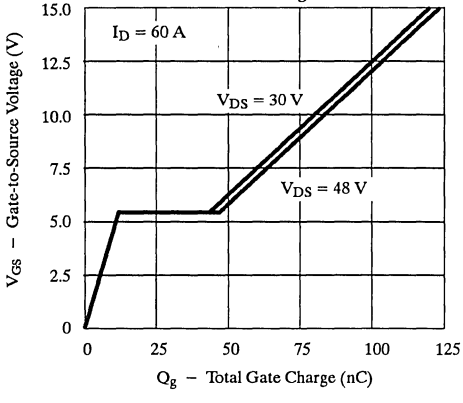
On-Resistance vs. Drain Current



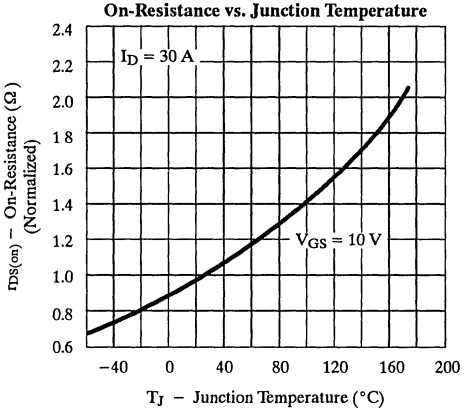
Capacitance

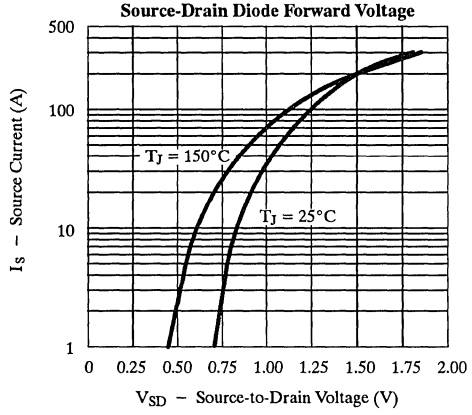


Gate Charge

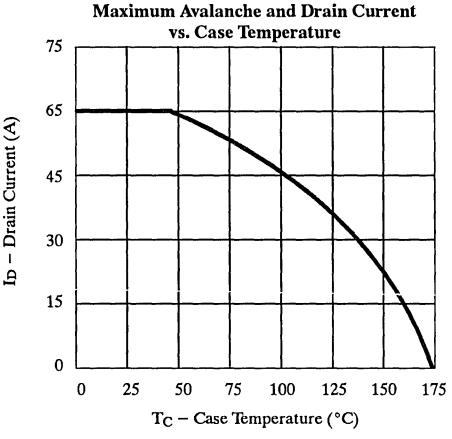


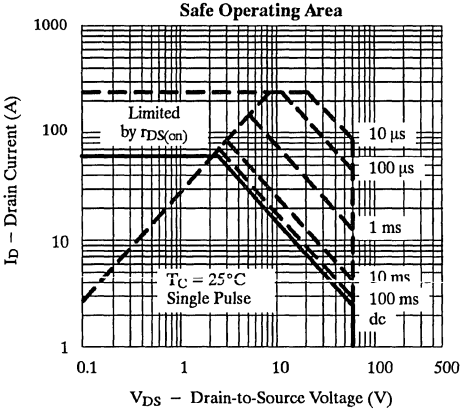
Typical Characteristics (25°C Unless Otherwise Noted)

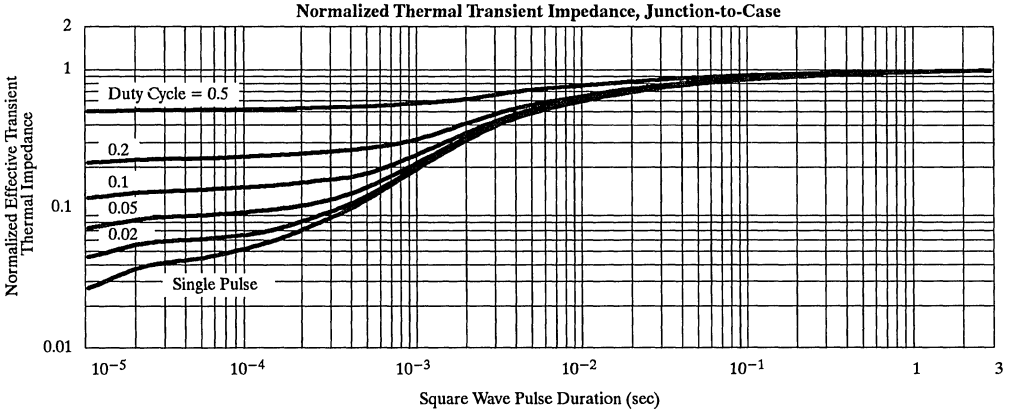




Thermal Ratings







Siliconix

SMW20P10

P-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.20	−20

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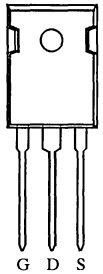
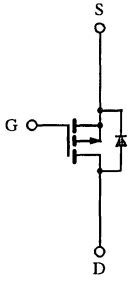


G D S
Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−20	A
	T_C = 100°C		−13	
Pulsed Drain Current		I_{DM}	−80	
Avalanche Current		I_{AR}	−20	
Repetitive Avalanche Energy[a]	L = 0 05 mH	E_{AR}	20	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		40	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.35		

Notes:
a. Duty cycle ≤ 1%

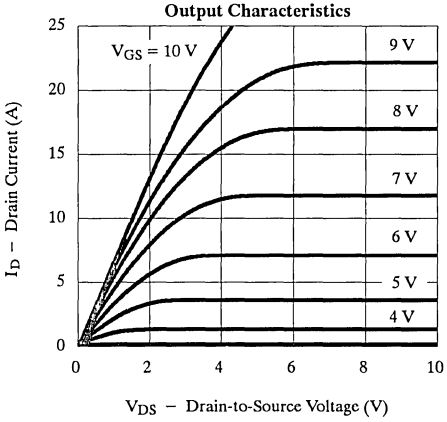
Specifications (T_J = 25°C Unless Otherwise Noted)

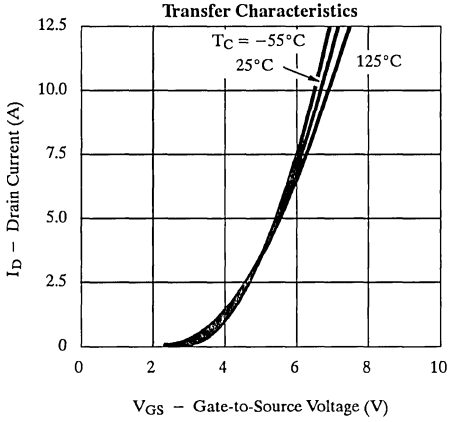
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −13 A		0.14	0.20	Ω
		V_{GS} = −10 V, I_D = −13 A, T_J = 125°C		0.22	0.32	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −13 A	5.0	6		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			700		
Reverse Transfer Capacitance	C_{rss}			250		
Total Gate Charge[c]	Q_g	V_{DS} = − 50 V, V_{GS} = −10 V, I_D = −20 A		47	62	nC
Gate-Source Charge[c]	Q_{gs}			10	15	
Gate-Drain Charge[c]	Q_{gd}			27	35	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 2.5 Ω I_D ≅ −20 A, V_{GEN} = −10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			50	80	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	80	
Fall Time[c]	t_f			15	60	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−20	A
Pulsed Current	I_{SM}				−80	
Diode Forward Voltage[b]	V_{SD}	I_F = −20 A, V_{GS} = 0 V			−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −20 A, di/dt = 100 A/µs		150		ns
Reverse Recovery Charge	Q_{rr}			0.3		µC

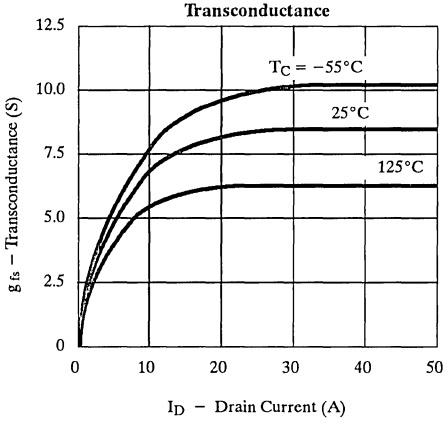
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

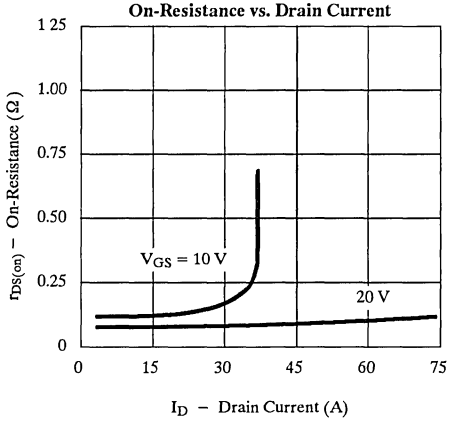
Typical Characteristics (25°C Unless Otherwise Noted)

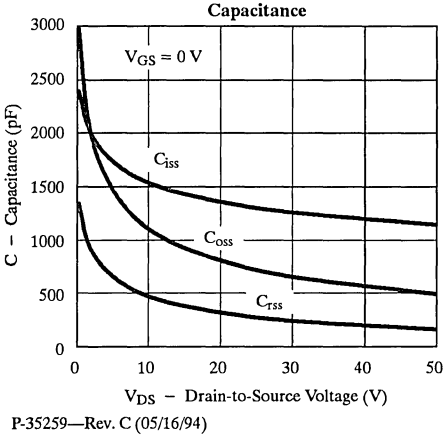
Negative signs omitted for clarity.

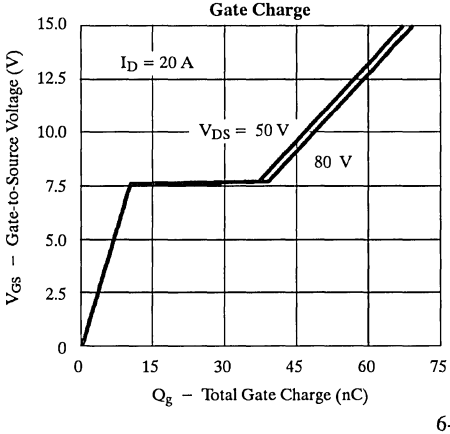






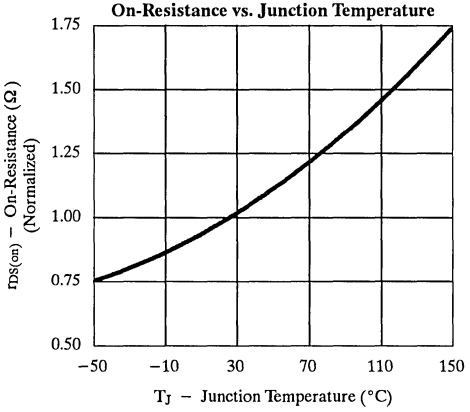


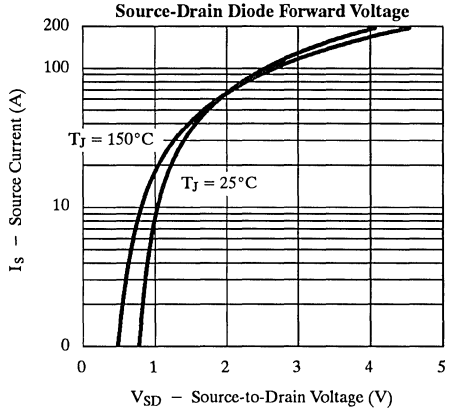




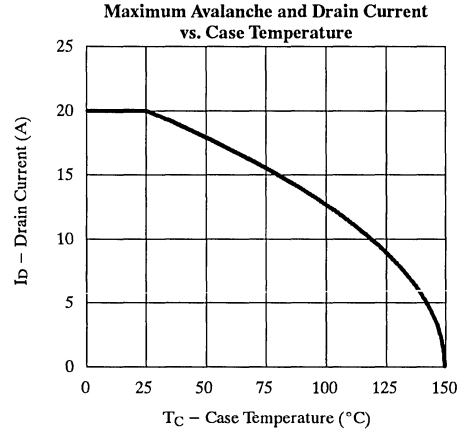
Typical Characteristics (25°C Unless Otherwise Noted)

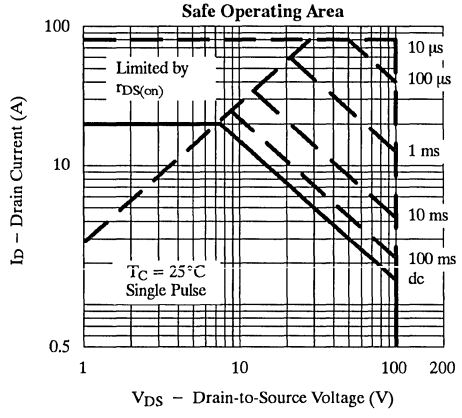
Negative signs omitted for clarity.

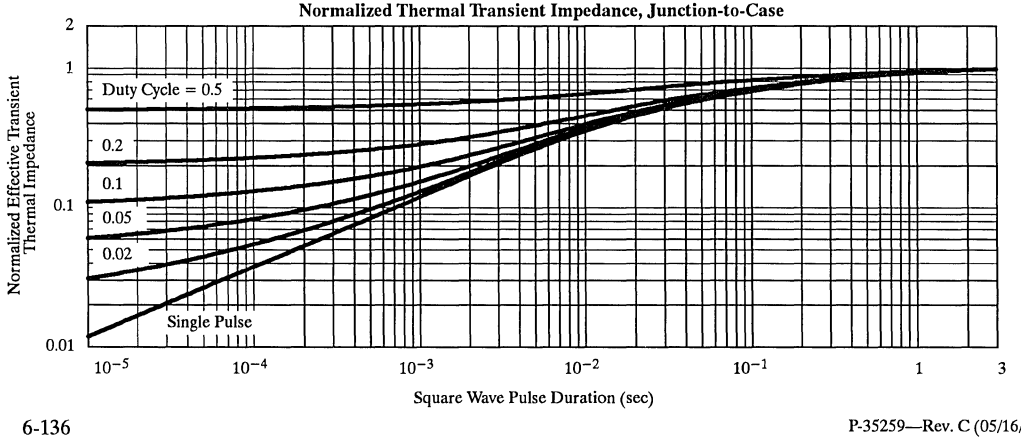




Thermal Ratings







Siliconix

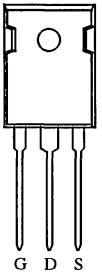
SMW45N10

N-Channel Enhancement-Mode Transistor

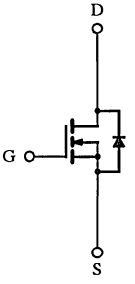
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.040	45

TO-247AD



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	45	A
	T_C = 100°C		27	
Pulsed Drain Current		I_{DM}	180	
Avalanche Current		I_{AR}	45	
Avalanche Energy	L = 0.3 mH	E_A	300	mJ
Repetitive Avalanche Energy[a]	L = 0.02 mH	E_{AR}	20	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		40	°C/W
Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.35		

Notes:
a. Duty cycle ≤ 1%

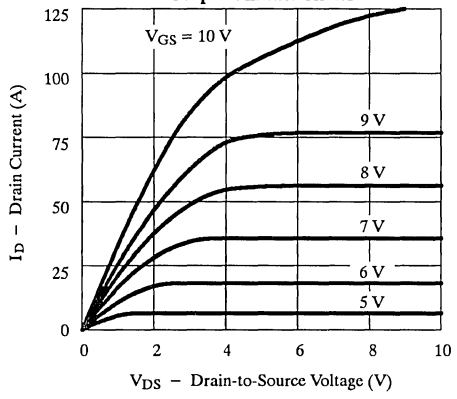
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	45			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 27 A		0.030	0.040	Ω
		V_{GS} = 10 V, I_D = 27 A, T_J = 125°C		0.058	0.072	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 27 A	15			S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3000		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 45 A		72	100	nC
Gate-Source Charge[c]	Q_{gs}			26	35	
Gate-Drain Charge[c]	Q_{gd}			31	40	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.1 Ω I_D ≅ 45 A, V_{GEN} = 10 V, R_G = 2.5 Ω		17	30	ns
Rise Time[c]	t_r			80	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			40	60	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				45	A
Pulsed Current	I_{SM}				180	
Forward Voltage[b]	V_{SD}	I_F = 45 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 45 A, dI_F/dt = 100 A/µs		130		ns
Reverse Recovery Charge	Q_{rr}			0.31		µC

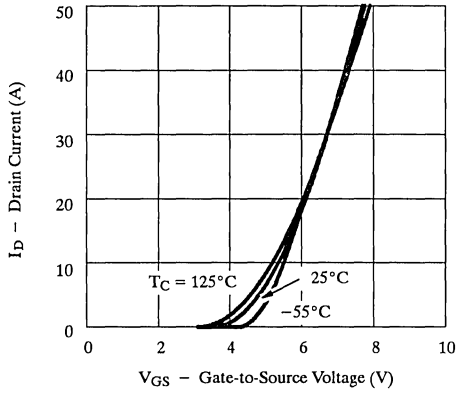
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

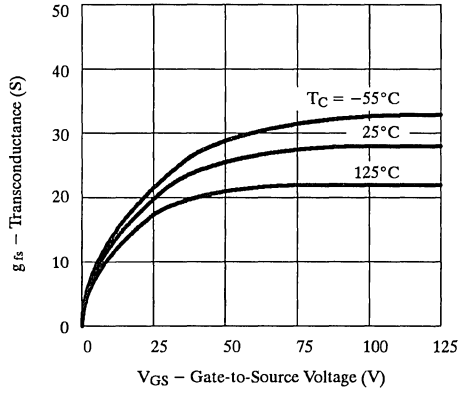
Output Characteristics



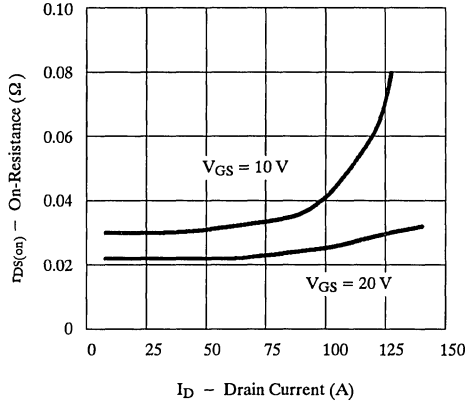
Transfer Characteristics



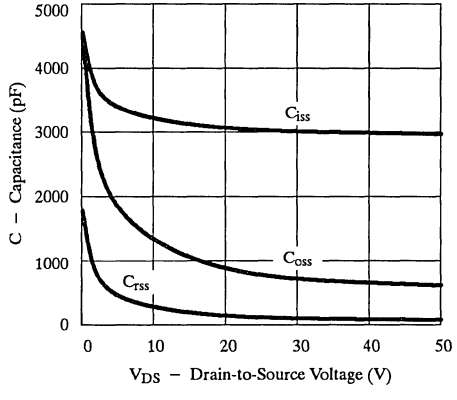
Transconductance



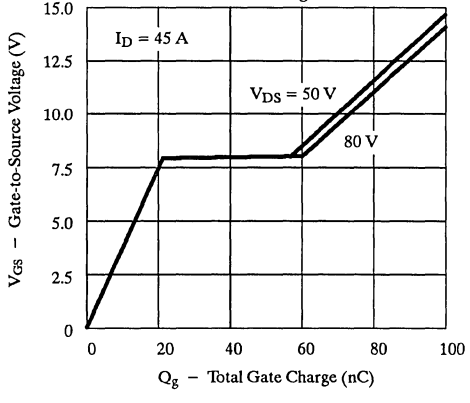
On-Resistance vs. Drain Current



Capacitance

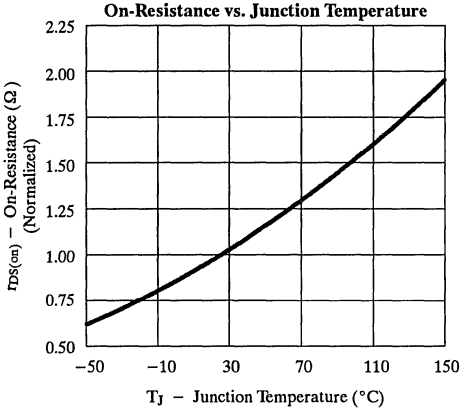


Gate Charge

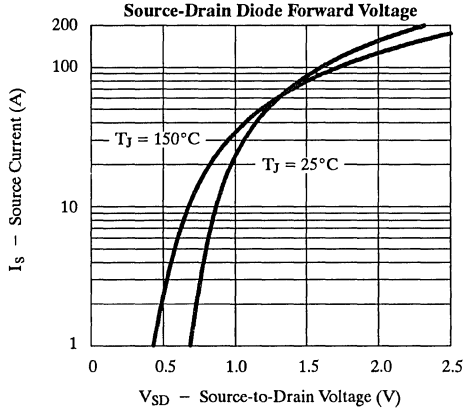


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

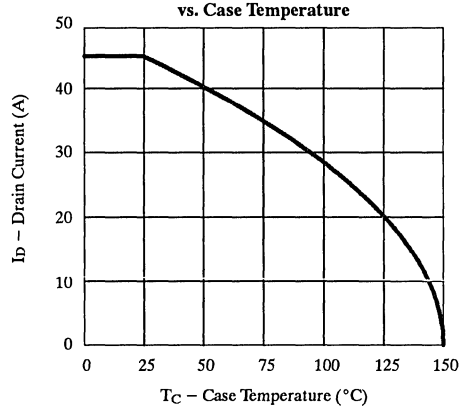


Source-Drain Diode Forward Voltage

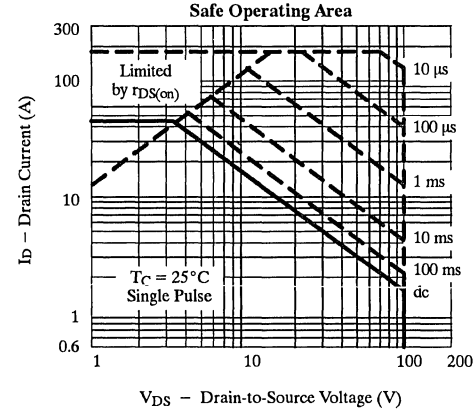


Thermal Ratings

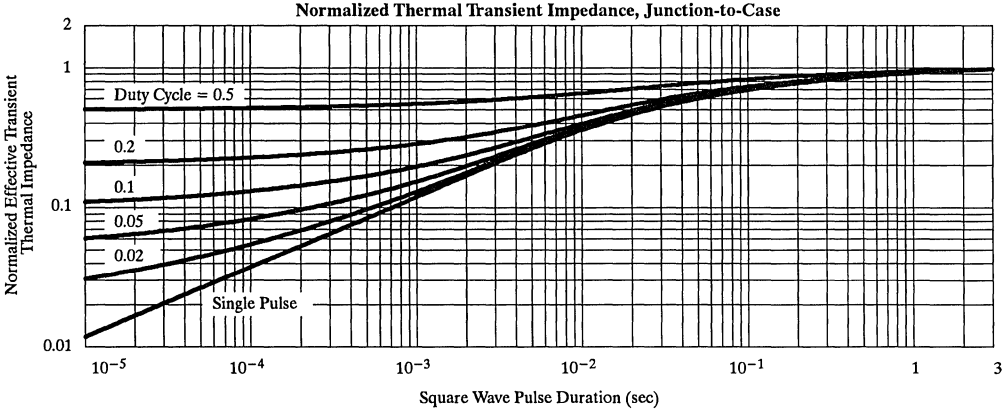
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SMW60N06-18

N-Channel Enhancement-Mode Transistor, 18-mΩ $r_{DS(on)}$

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.018	60

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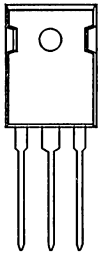
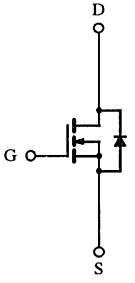


Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		40	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		40	°C/W
Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	0.35		

Notes:
a Duty cycle ≤ 1%

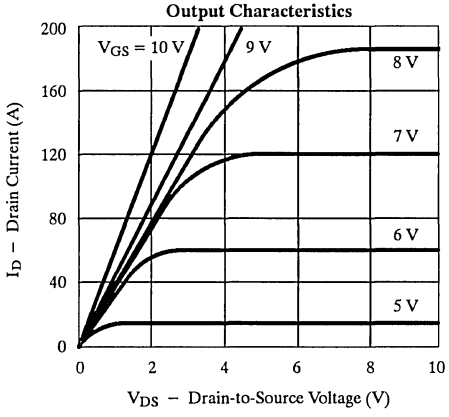
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.013	0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		0.023	0.030	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		45		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2600		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		85	100	nC
Gate-Source Charge[c]	Q_{gs}			15	20	
Gate-Drain Charge[c]	Q_{gd}			35	50	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	30	ns
Rise Time[c]	t_r			20	35	
Turn-Off Delay Time[c]	$t_{d(off)}$			50	65	
Fall Time[c]	t_f			15	30	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, dI_F/dt = 100 A/µs		160		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			13		A
Reverse Recovery Charge	Q_{rr}			1.0		µC

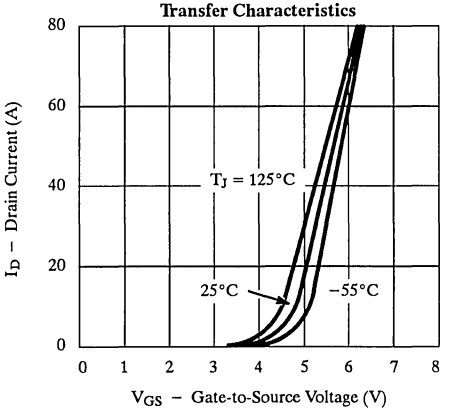
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

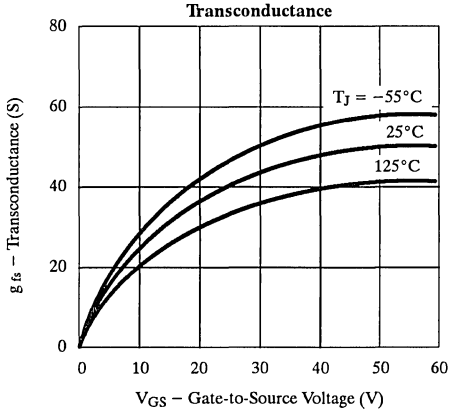
Output Characteristics



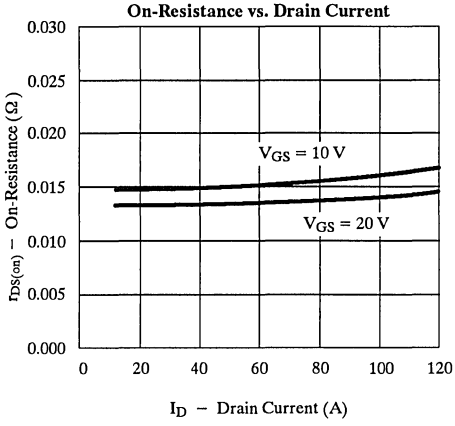
Transfer Characteristics



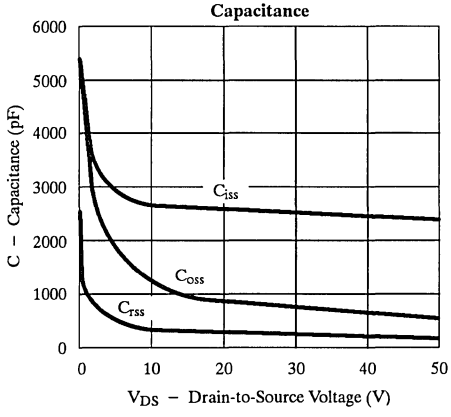
Transconductance



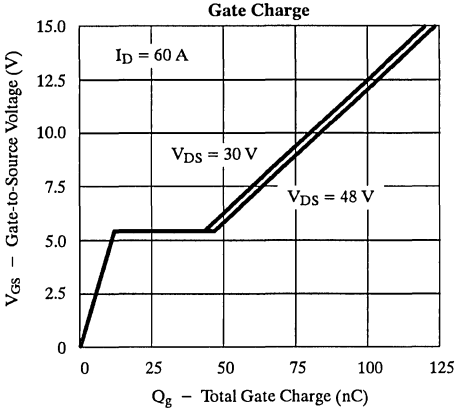
On-Resistance vs. Drain Current



Capacitance

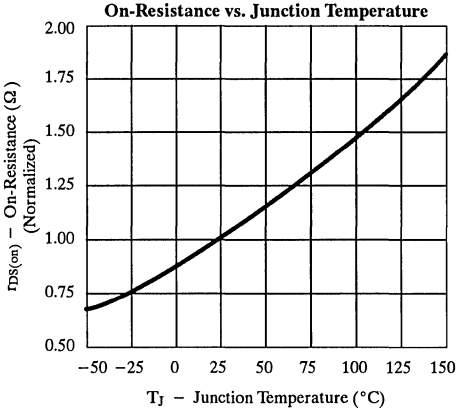


Gate Charge

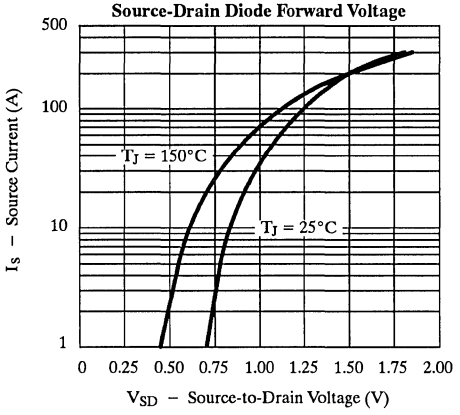


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

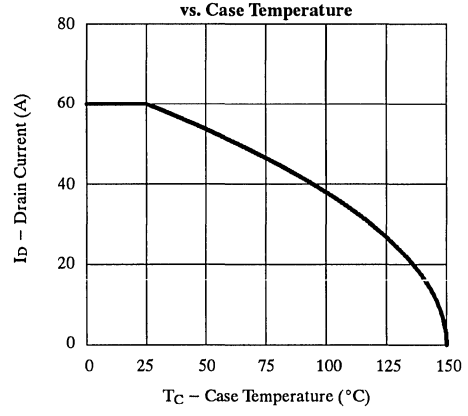


Source-Drain Diode Forward Voltage

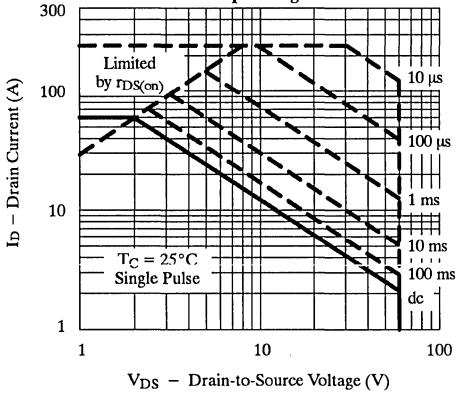


Thermal Ratings

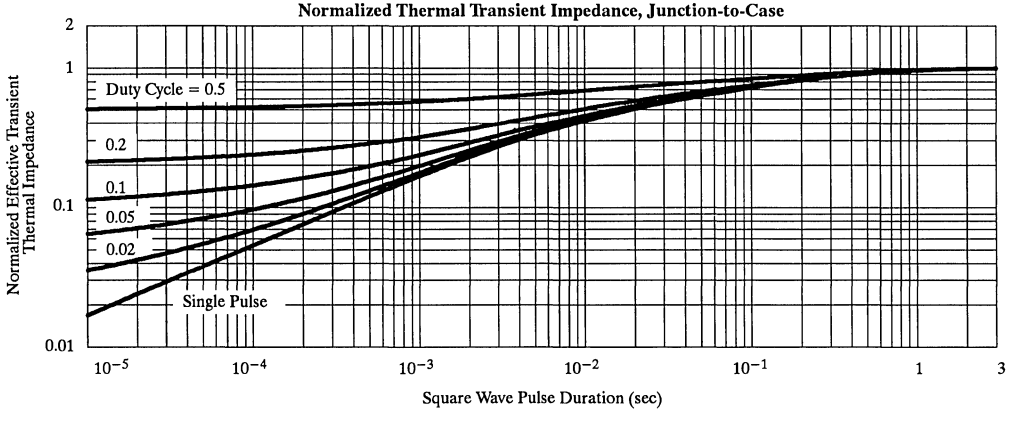
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SMW60N10

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.025	60

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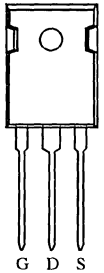
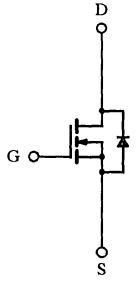


Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		37	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.3 mH	E_A	540	mJ
Repetitive Avalanche Energy[a]	L = 0.02 mH	E_{AR}	36	
Power Dissipation	T_C = 25°C	P_D	180	W
	T_C = 100°C		70	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		40	°C/W
Junction-to-Case	R_{thJC}		0.7	
Case-to-Sink	R_{thCS}	0.35		

Notes:
a. Duty cycle ≤ 1%

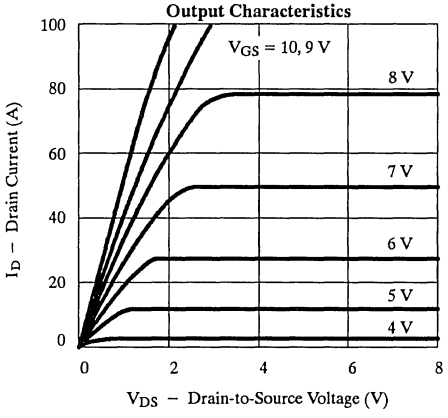
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 37 A		0.020	0.025	Ω
		V_{GS} = 10 V, I_D = 37 A, T_J = 125°C		0.034	0.045	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 37 A	20			S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4100		pF
Output Capacitance	C_{oss}			1200		
Reverse Transfer Capacitance	C_{rss}			310		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 60 A		110	140	nC
Gate-Source Charge[c]	Q_{gs}			30	40	
Gate-Drain Charge[c]	Q_{gd}			52	80	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 0.83 Ω I_D ≃ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		20	40	ns
Rise Time[c]	t_r			130	180	
Turn-Off Delay Time[c]	$t_{d(off)}$			40	80	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, dI_F/dt = 100 A/µs		125		ns
Reverse Recovery Charge	Q_{rr}			0.3		µC

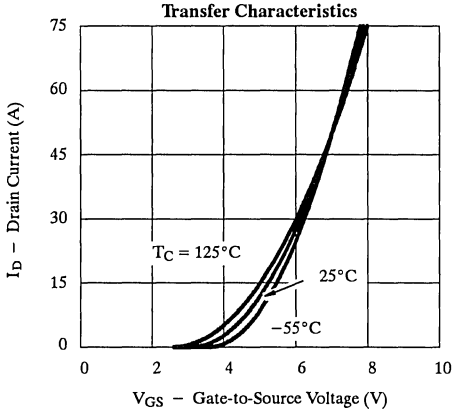
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

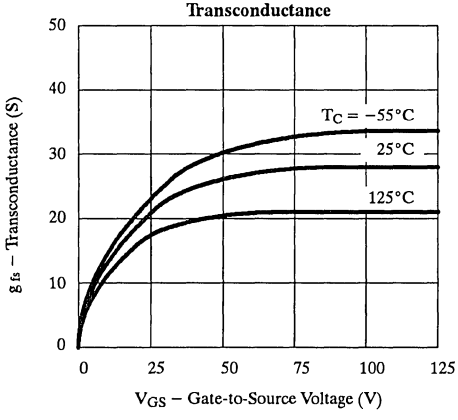
Output Characteristics



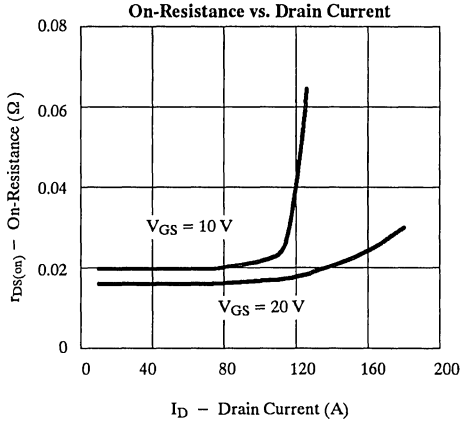
Transfer Characteristics



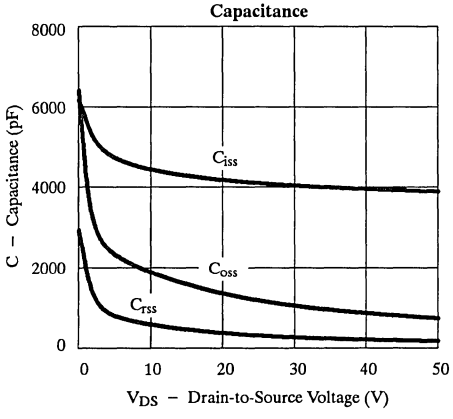
Transconductance



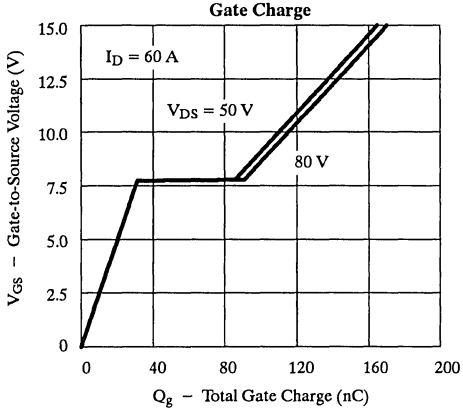
On-Resistance vs. Drain Current



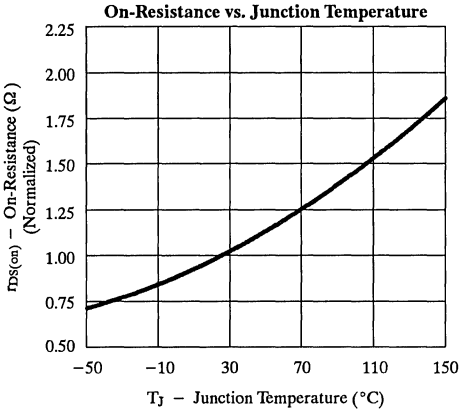
Capacitance

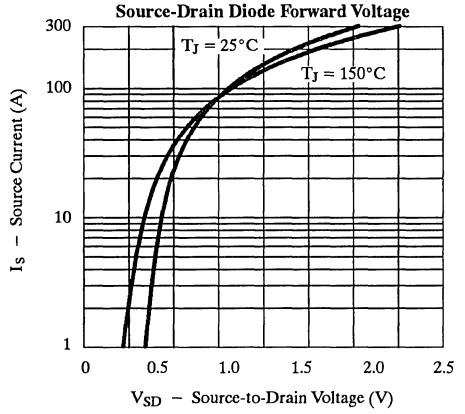


Gate Charge

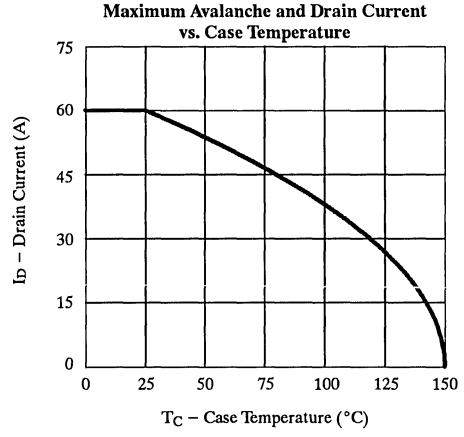


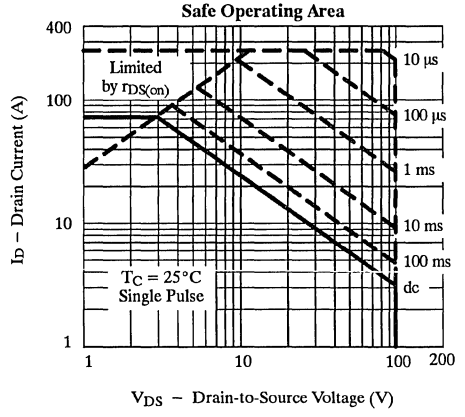
Typical Characteristics (25°C Unless Otherwise Noted)

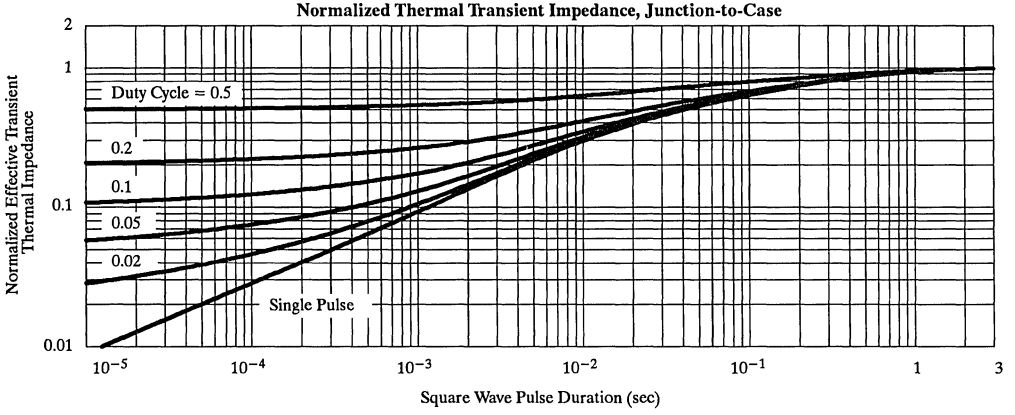




Thermal Ratings







Siliconix

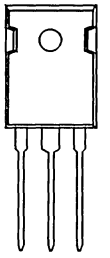
SMW70N06-14

N-Channel Enhancement-Mode Transistor

Product Summary

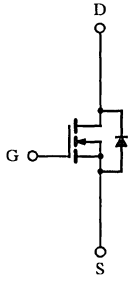
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.014	70

TO-247AD



Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	70	A
	T_C = 100°C		48	
Pulsed Drain Current		I_{DM}	280	
Avalanche Current[a]		I_{AR}	70	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	245	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		40	°C/W
Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.35		

Notes:
a. Duty cycle ≤ 1%

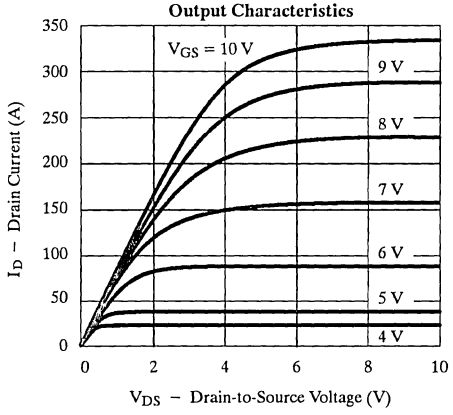
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	70			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 35 A		0.012	0.014	Ω
		V_{GS} = 10 V, I_D = 35 A, T_J = 125°C		0.020	0.023	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 35 A	30	50		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3450		pF
Output Capacitance	C_{oss}			1000		
Reverse Transfer Capacitance	C_{rss}			230		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 70 A		95	130	nC
Gate-Source Charge[c]	Q_{gs}			22		
Gate-Drain Charge[c]	Q_{gd}			44		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.39 Ω I_D ≃ 70 A, V_{GEN} = 10 V, R_G = 2.5 Ω		15	30	ns
Rise Time[c]	t_r			130	180	
Turn-Off Delay Time[c]	$t_{d(off)}$			50	100	
Fall Time[c]	t_f			20	50	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				70	A
Pulsed Current	I_{SM}				280	
Forward Voltage[b]	V_{SD}	I_F = 70 A, V_{GS} = 0 V		1.0	1.8	V
Reverse Recovery Time	t_{rr}	I_F = 70 A, dI_F/dt = 100 A/µs		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			9		A
Reverse Recovery Charge	Q_{rr}			0.6		µC

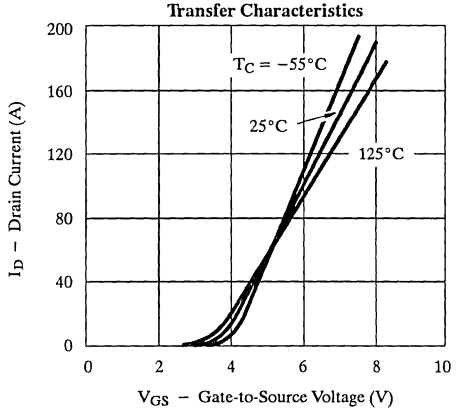
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

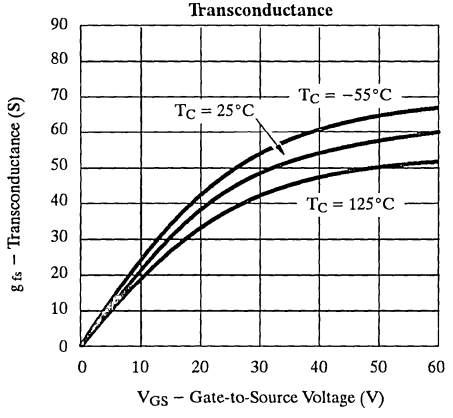
Output Characteristics



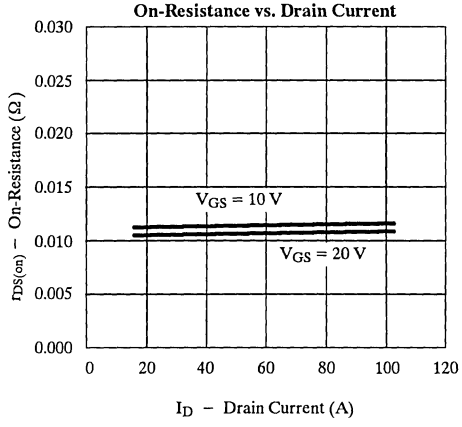
Transfer Characteristics



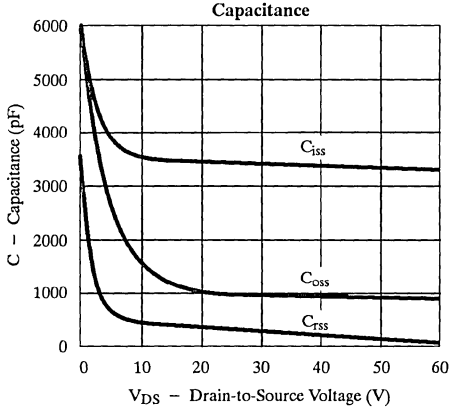
Transconductance



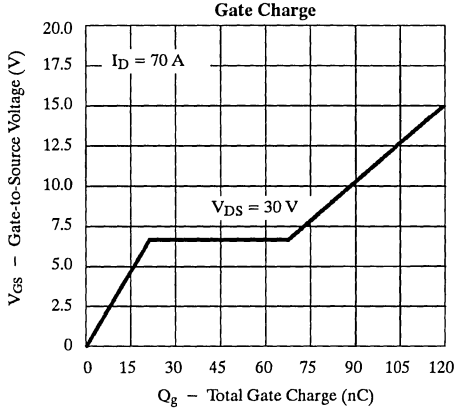
On-Resistance vs. Drain Current



Capacitance

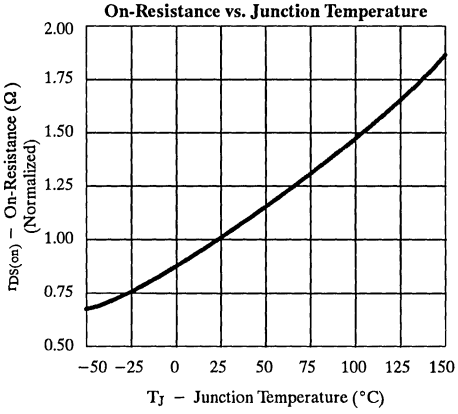


Gate Charge

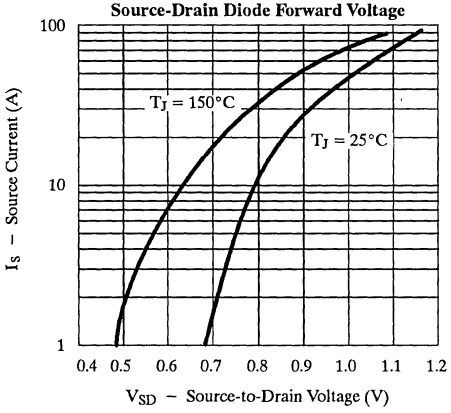


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

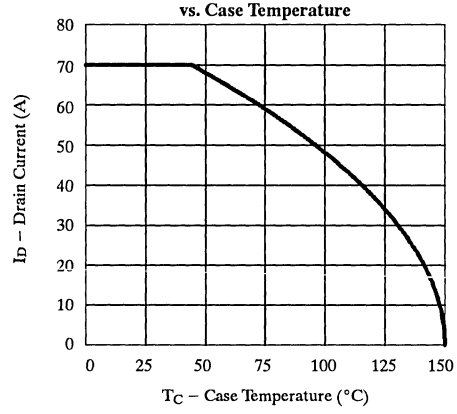


Source-Drain Diode Forward Voltage

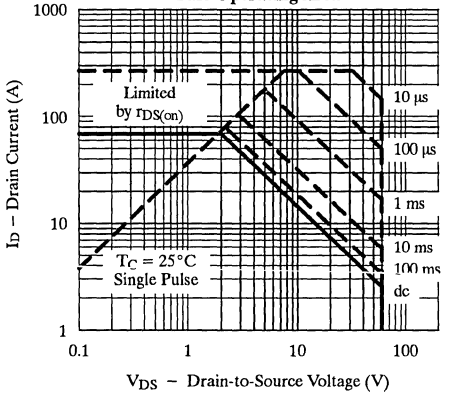


Thermal Ratings

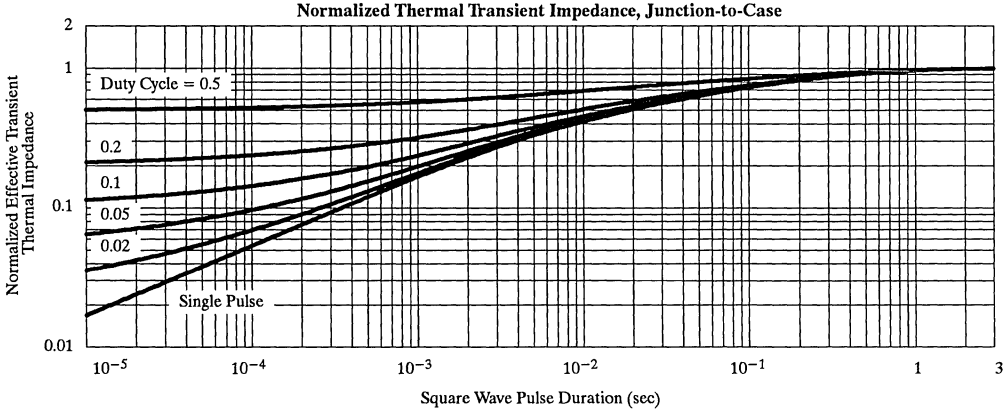
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SUB60N06-08

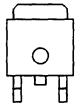
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

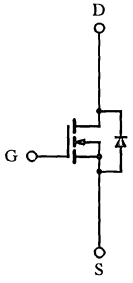
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.008	60[a]

TO-263



G D S
Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	60[a]	A
	T_C = 125°C		55	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_A = 25°C[c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient, PCB Mount[c]	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	1.0	

Notes
a. Package limited.
b. Duty cycle ≤ 1%.
c. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			0.008	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.012	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.016	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	30			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4300		pF
Output Capacitance	C_{oss}			1000		
Reverse Transfer Capacitance	C_{rss}			400		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		110	150	nC
Gate-Source Charge[c]	Q_{gs}			25		
Gate-Drain Charge[c]	Q_{gd}			50		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≅ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		20	40	ns
Rise Time[c]	t_r			120	200	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	120	
Fall Time[c]	t_f			30	60	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V		1.0	1.3	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, di/dt = 100 A/µs		67	120	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			4.7	8	A
Reverse Recovery Charge	Q_{rr}			0.16	0.48	µC

Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test: pulse width ≤ 300 µsec, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

SUP/SUB50N06-18

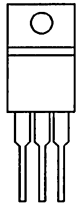
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.018	48

TO-220AB

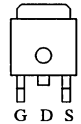


Top View

SUP50N06-18

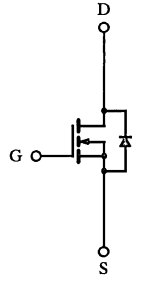
DRAIN connected to TAB

TO-263



Top View

SUB50N06-18



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	48	A
	T_C = 100°C		34	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	90	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	83	W
	T_A = 25°C (TO-263)[b]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[b]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)		80	
Junction-to-Case		R_{thJC}	1.8	

Notes:
a. Duty cycle ≤ 1%.
b. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 1 mA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	48			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			0.018	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.030	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.036	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A				S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz				pF
Output Capacitance	C_{oss}					
Reversen Transfer Capacitance	C_{rss}					
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 48 A			100	nC
Gate-Source Charge[c]	Q_{gs}				20	
Gate-Drain Charge[c]	Q_{gd}				50	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≃ 48 A, V_{GEN} = 10 V, R_G = 2.5 Ω			30	ns
Rise Time[c]	t_r				35	
Turn-Off Delay Time[c]	$t_{d(off)}$				65	
Fall Time[c]	t_f				30	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_s				48	A
Pulsed Current	I_{SM}				200	
Forward Voltage[b]	V_{SD}	I_F = 48 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 48 A, di/dt = 100 A/µs				ns
Peak Reverse Recovery Current	$I_{RM(REC)}$					A
Reverse Recovery Charge	Q_{rr}					µC

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

SUP60N06-08

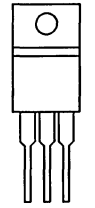
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

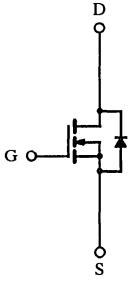
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.008	60

TO-220AB



DRAIN connected to TAB

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	60[a]	A
	T_C = 125°C		55	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy[a]	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient, Free Air	R_{thJA}	80	°C/W
Junction-to-Case	R_{thJC}	1.0	

Notes
a. Duty cycle ≤ 1%.

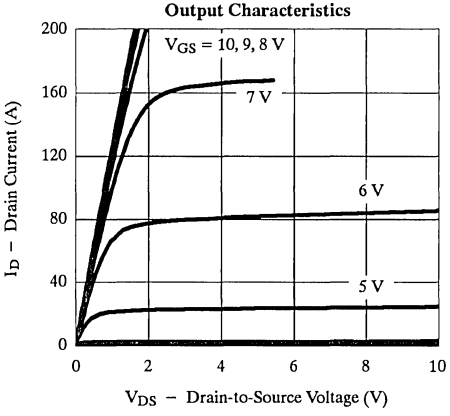
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	120			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			0.008	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.012	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.016	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A	30			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4300		pF
Output Capacitance	C_{oss}			1000		
Reverse Transfer Capacitance	C_{rss}			400		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		110	150	nC
Gate-Source Charge[c]	Q_{gs}			25		
Gate-Drain Charge[c]	Q_{gd}			50		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≅ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		20	40	ns
Rise Time[c]	t_r			120	200	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	120	
Fall Time[c]	t_f			30	60	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V		1.0	1.3	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, di/dt = 100 A/µs		67	120	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			4.7	8	A
Reverse Recovery Charge	Q_{rr}			0.16	0.48	µC

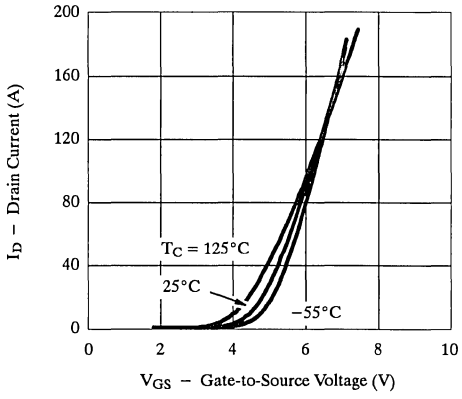
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test: pulse width ≤ 300 µsec, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

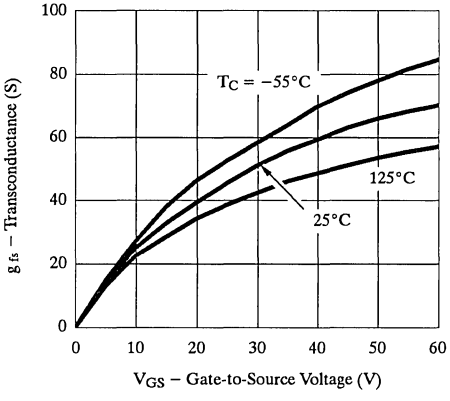
Output Characteristics



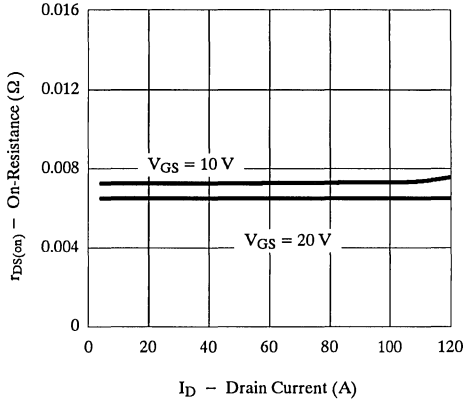
Transfer Characteristics



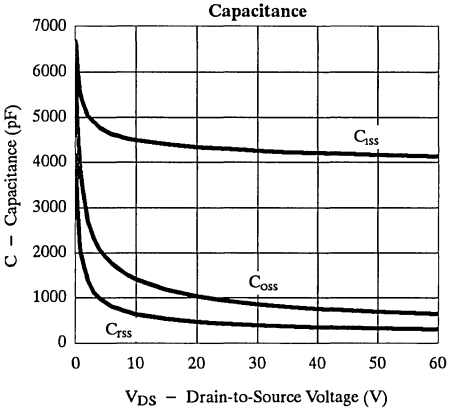
Transconductance



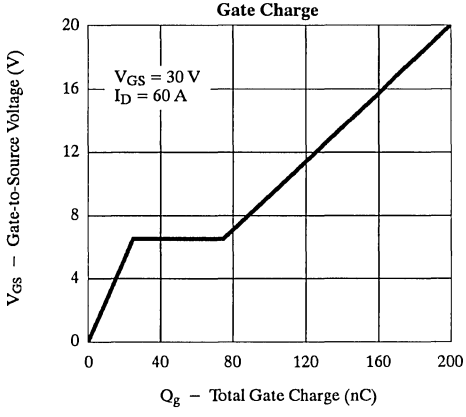
On-Resistance vs. Drain Current



Capacitance

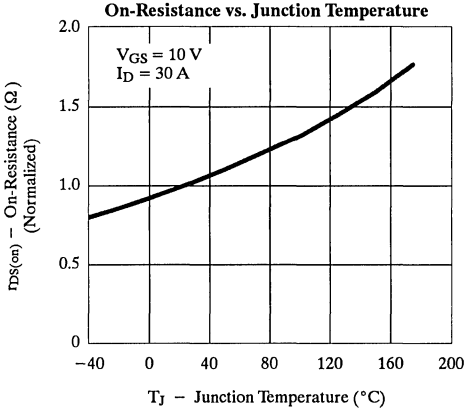


Gate Charge

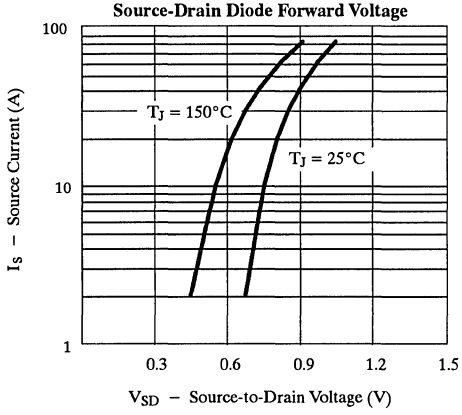


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

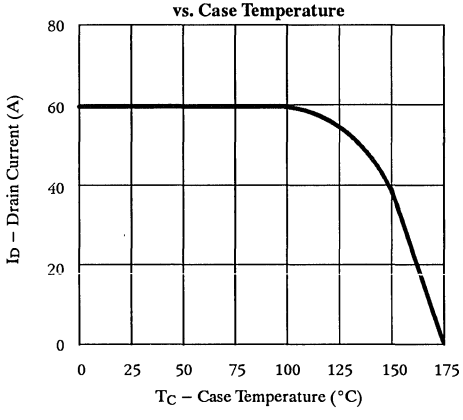


Source-Drain Diode Forward Voltage

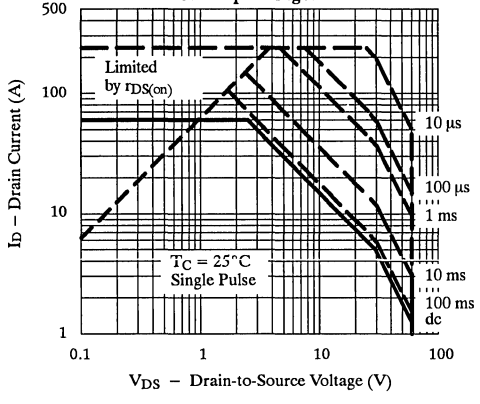


Thermal Ratings

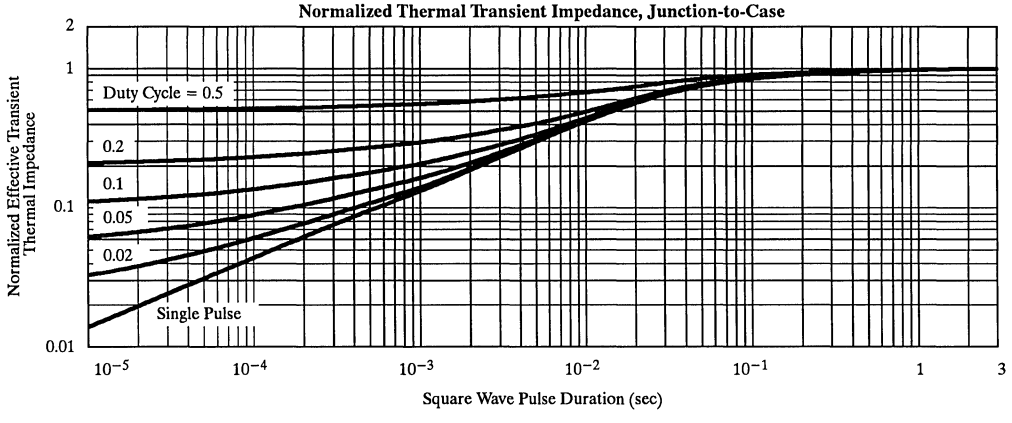
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

SUP/SUB60N06-14

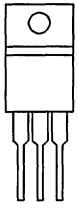
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.014	60[a]

TO-220AB

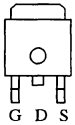


Top View

SUP60N06-14

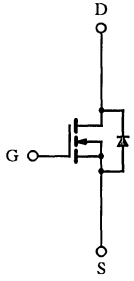
DRAIN connected to TAB

TO-263



Top View

SUB60N06-14



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	60[a]	A
	T_C = 100°C		42	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	100	W
	T_A = 25°C (TO-263)[c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)		80	
Junction-to-Case		R_{thJC}	1.5	

Notes:
a. Package limited.
b. Duty cycle ≤ 1%.
c. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 1 mA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 175°C			500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A			0.014	Ω
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C			0.023	
		V_{GS} = 10 V, I_D = 30 A, T_J = 175°C			0.028	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		TBD		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		TBD		pF
Output Capacitance	C_{oss}			TBD		
Reversen Transfer Capacitance	C_{rss}			TBD		
Total Gate Charge[c]	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 60 A		TBD	130	nC
Gate-Source Charge[c]	Q_{gs}			TBD		
Gate-Drain Charge[c]	Q_{gd}			TBD		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 0.47 Ω I_D ≅ 60 A, V_{GEN} = 10 V, R_G = 2.5 Ω		TBD	30	ns
Rise Time[c]	t_r			TBD	180	
Turn-Off Delay Time[c]	$t_{d(off)}$			TBD	100	
Fall Time[c]	t_f			TBD	50	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_s				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, di/dt = 100 A/µs		TBD		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			TBD		A
Reverse Recovery Charge	Q_{rr}			TBD		µC

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

SUP/SUB60P06-20

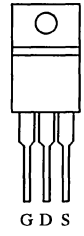
P-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−60	0.020	−60[a]

TO-220AB

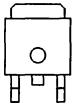


Top View

SUP60P06-20

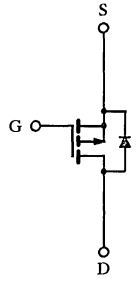
DRAIN connected to TAB

TO-263



Top View

SUB60P06-20



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (T_J = 175°C)	T_C = 25°C	I_D	−60[a]	A
	T_C = 125°C		−55	
Pulsed Drain Current		I_{DM}	−240	
Avalanche Current		I_{AR}	−60	
Repetitive Avalanche Energy[b]	L = 0.1 mH	E_{AR}	180	mJ
Power Dissipation	T_C = 25°C (TO-220AB and TO-263)	P_D	150	W
	T_A = 125°C (TO-263)[c]		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 175	°C

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263)[c]	R_{thJA}	40	°C/W
	Free Air (TO-220AB)	R_{thJA}	80	
Junction-to-Case		R_{thJC}	1.0	

Notes:
a. Package limited.
b. Duty cycle ≤ 1%.
c. When mounted on 1" square PCB (FR-4 material).

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −48 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 125°C			−250	
		V_{DS} = −48 V, V_{GS} = 0 V, T_J = 175°C			−500	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −10 V	−120			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −30 A			0.020	Ω
		V_{GS} = −10 V, I_D = −30 A, T_J = 125°C			0.030	
		V_{GS} = −10 V, I_D = −30 A, T_J = 175°C			0.040	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −30 A				S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		TBD		pF
Output Capacitance	C_{oss}			TBD		
Reversen Transfer Capacitance	C_{rss}			TBD		
Total Gate Charge[c]	Q_g	V_{DS} = −30 V, V_{GS} = −10 V, I_D = −60 A		TBD	150	nC
Gate-Source Charge[c]	Q_{gs}			TBD		
Gate-Drain Charge[c]	Q_{gd}			TBD		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −30 V, R_L = 0.47 Ω I_D ≃ −60 A, V_{GEN} = −10 V, R_G = 2.5 Ω		TBD	40	ns
Rise Time[c]	t_r			TBD	200	
Turn-Off Delay Time[c]	$t_{d(off)}$			TBD	120	
Fall Time[c]	t_f			TBD	60	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)[a]						
Continuous Current	I_s				−60	A
Pulsed Current	I_{SM}				−240	
Forward Voltage[b]	V_{SD}	I_F = −60 A, V_{GS} = 0 V		TBD	TBD	V
Reverse Recovery Time	t_{rr}	I_F = −60 A, di/dt = 100 A/µs		TBD	TBD	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			TBD	TBD	A
Reverse Recovery Charge	Q_{rr}			TBD	TBD	µC

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

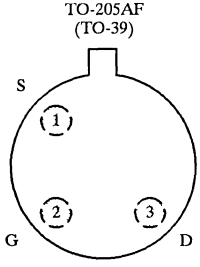
2N6849

P-Channel Enhancement-Mode Transistor

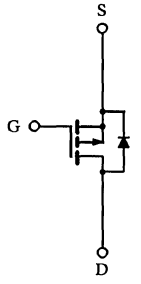
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.30	−6.5

Parametric limits in accordance with MIL-S-19500/564 where applicable.



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−6.5	A
	T_C = 100°C		−3.1	
Pulsed Drain Current		I_{DM}	−25	
Avalanche Current		I_{AR}	−3.1	
Maximum Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient	R_{thJA}	175	°C/W
Maximum Junction-to-Case	R_{thJC}	5.0	

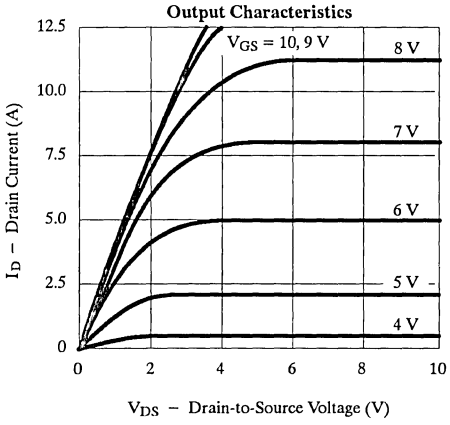
Specifications (T_J = 25°C Unless Otherwise Noted)

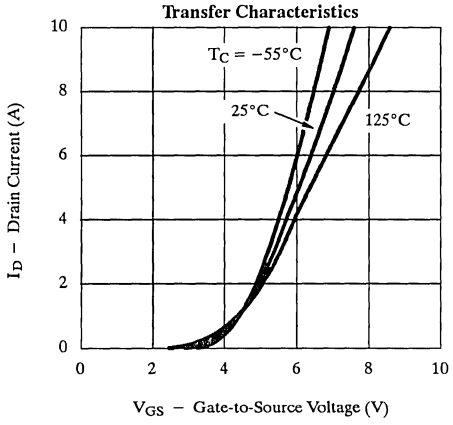
Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −1000 μA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−25	μA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −2.1 V, V_{GS} = −10 V	−6.5			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −4.1 A		0.25	0.30	Ω
		V_{GS} = −10 V, I_D = −4.1 A, T_J = 125°C		0.40	0.54	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −4.1 A	2.5	2.8	7.5	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		625		pF
Output Capacitance	C_{oss}			280		
Reverse Transfer Capacitance	C_{rss}			105		
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = −10 V, I_D = −6.5 A	14.7	24	34.8	nC
Gate-Source Charge[c]	Q_{gs}		0.8	3.4	6.8	
Gate-Drain Charge[c]	Q_{gd}		2.0	13.5	23.1	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 10 Ω I_D ≅ −4.1 A, V_{GEN} = −10 V, R_G = 7.5 Ω		9	60	ns
Rise Time[c]	t_r			50	140	
Turn-Off Delay Time[c]	$t_{d(off)}$			32	140	
Fall Time[c]	t_f			38	140	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−6.5	A
Pulsed Current	I_{SM}				−25	
Diode Forward Voltage[b]	V_{SD}	I_F = −6.5 A, V_{GS} = 0 V	−0.8		−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −6.5 A, di/dt = 100 A/μs		110	250	ns
Reverse Recovery Charge	Q_{rr}			0.4		μC

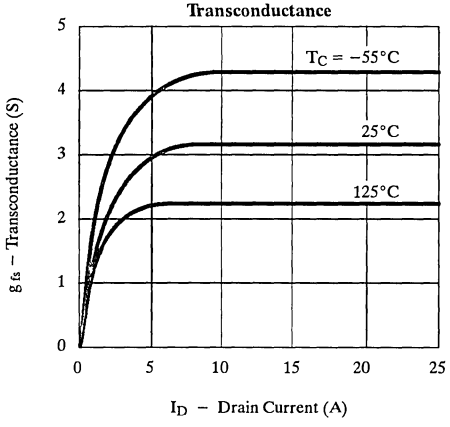
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
c. Independent of operating temperature.

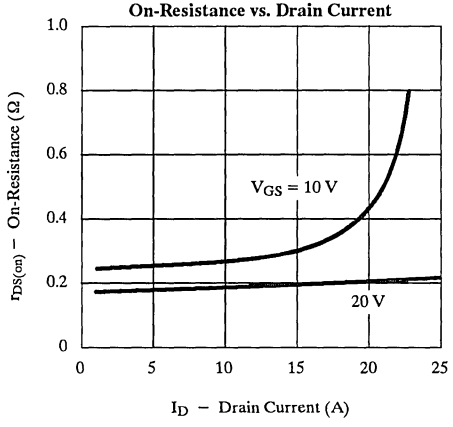
Typical Characteristics (25°C Unless Otherwise Noted)

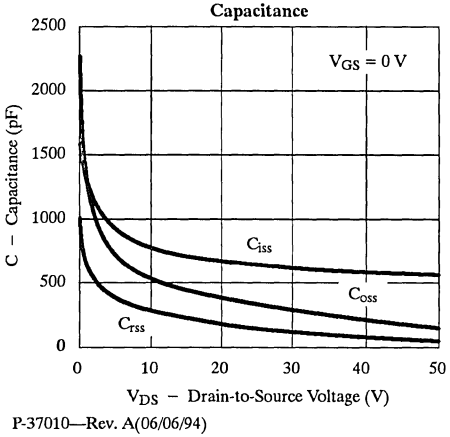
Negative signs omitted for clarity.

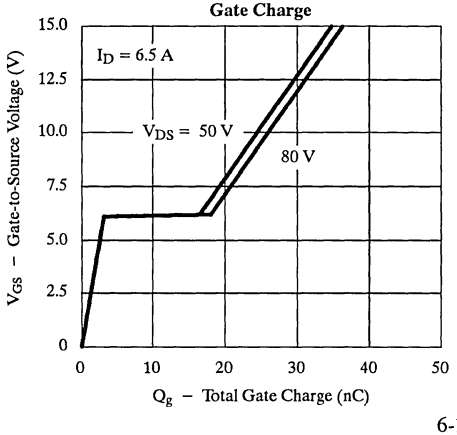








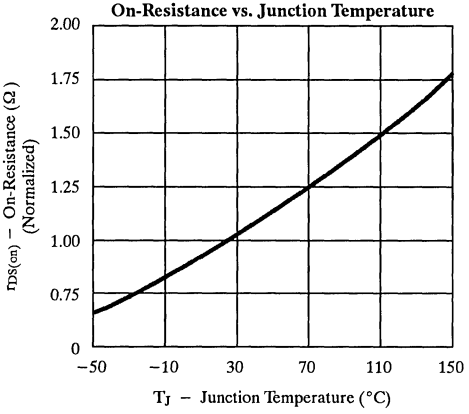




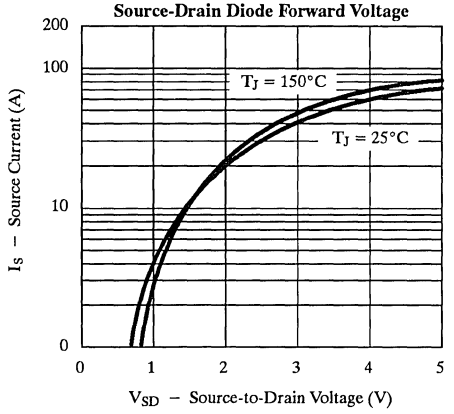
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

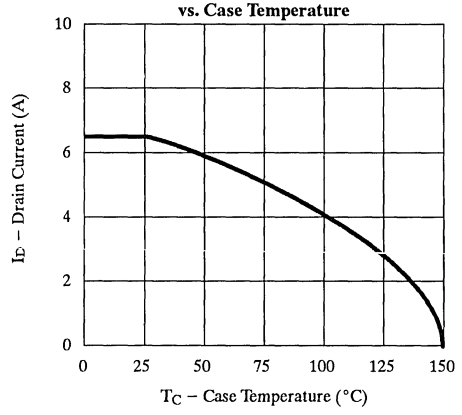


Source-Drain Diode Forward Voltage

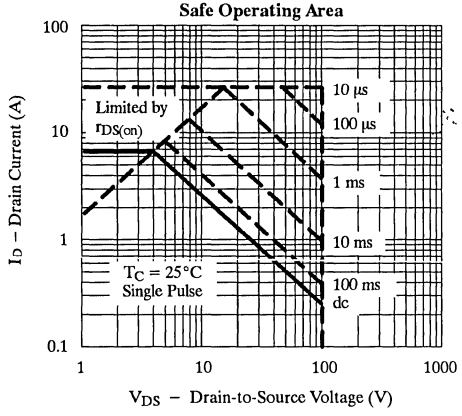


Thermal Ratings

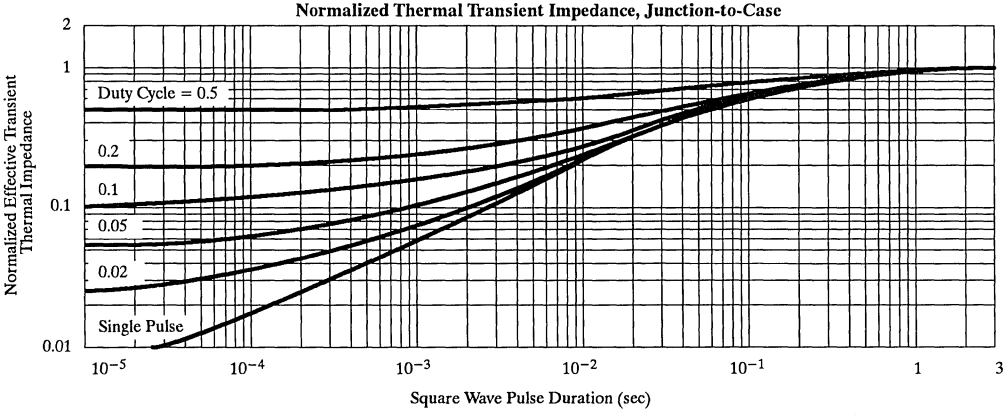
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

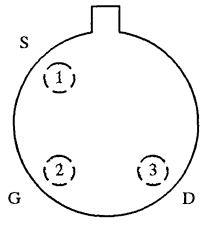
2N6851

P-Channel Enhancement-Mode Transistor

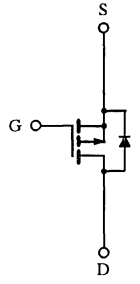
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−200	0.80	−4.0

Parametric limits in accordance with MIL-S-19500/564 where applicable.



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−4.0	A
	T_C = 100°C		−2.4	
Pulsed Drain Current		I_{DM}	−20	
Avalanche Current		I_{AR}	−3.1	
Maximum Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient	R_{thJA}	175	°C/W
Maximum Junction-to-Case	R_{thJC}	5.0	

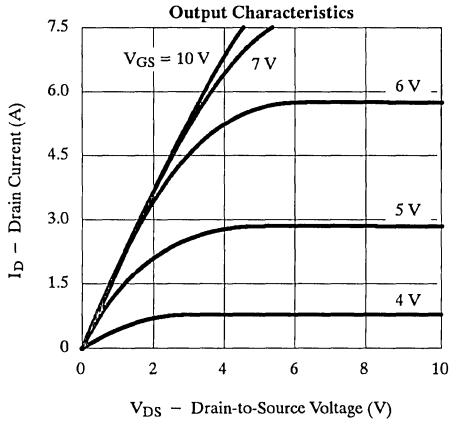
Specifications (T_J = 25°C Unless Otherwise Noted)

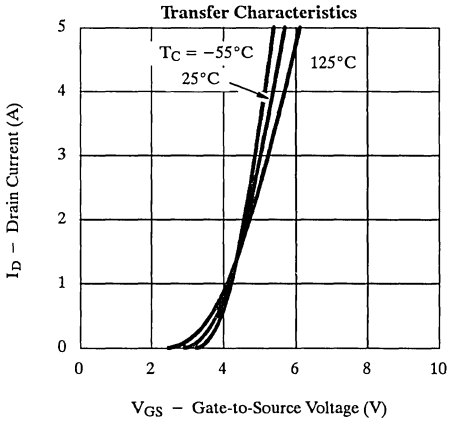
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −1000 µA	−200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −160 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −160 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −3.3 V, V_{GS} = −10 V	−4.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −2.4 A		0.50	0.80	Ω
		V_{GS} = −10 V, I_D = −2.4 A, T_J = 125°C		1.0	1.6	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −2.4 A	2.2	2.	6.6	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		625		pF
Output Capacitance	C_{oss}			280		
Reverse Transfer Capacitance	C_{rss}			105		
Total Gate Charge[c]	Q_g	V_{DS} = −100 V, V_{GS} = −10 V, I_D = −4.0 A	14.7	24	34.8	nC
Gate-Source Charge[c]	Q_{gs}		0.5	3.4	6.1	
Gate-Drain Charge[c]	Q_{gd}		3.3	13.5	20.1	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −100 V, R_L = 39 Ω I_D ≅ −2.4 A, V_{GEN} = −10 V, R_G = 7.5 Ω		9	50	ns
Rise Time[c]	t_r			50	100	
Turn-Off Delay Time[c]	$t_{d(off)}$			32	80	
Fall Time[c]	t_f			38	80	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−4.0	A
Pulsed Current	I_{SM}				−20	
Diode Forward Voltage[b]	V_{SD}	I_F = −4.0 A, V_{GS} = 0 V	−0.8		−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −4.0 A, di/dt = 100 A/µs		160	400	ns
Reverse Recovery Charge	Q_{rr}			1.6		µC

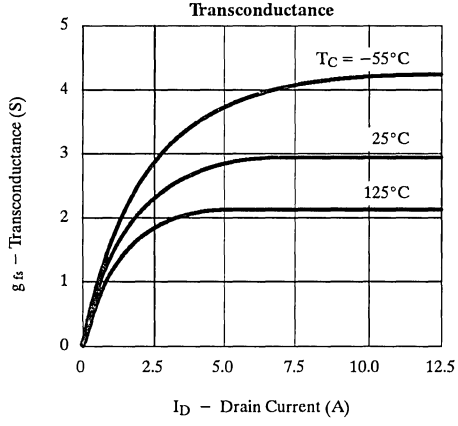
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

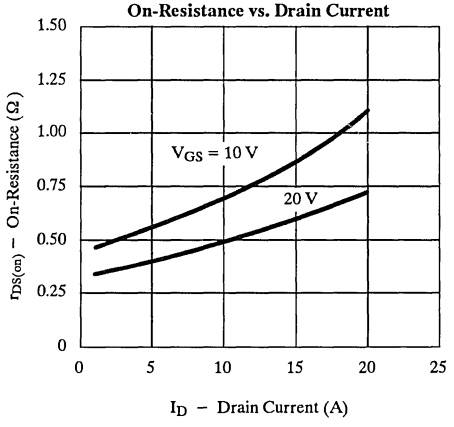
Typical Characteristics (25°C Unless Otherwise Noted)

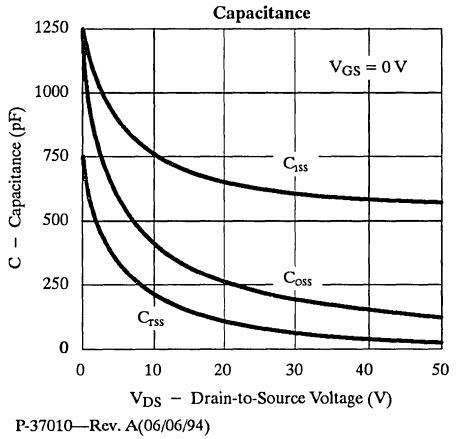
Negative signs omitted for clarity

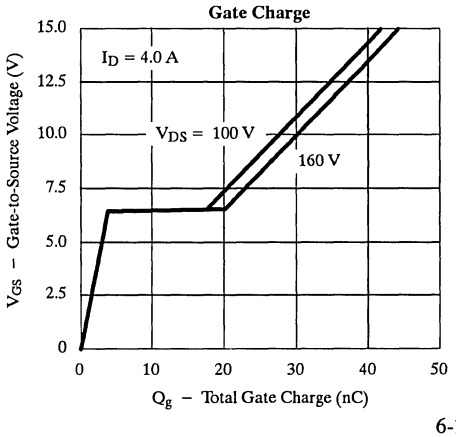






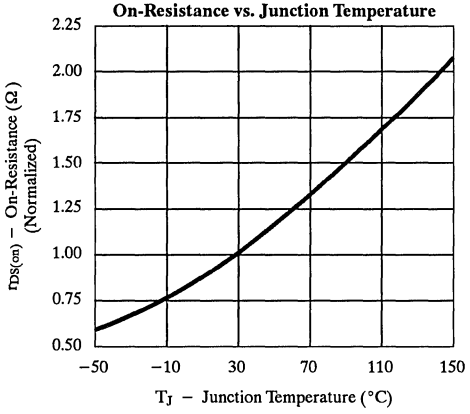


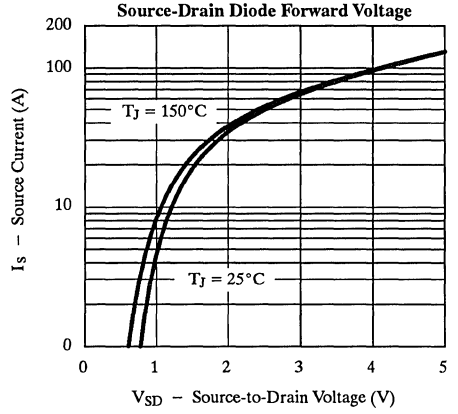




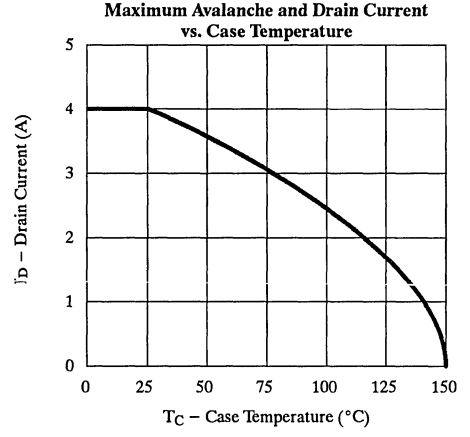
Typical Characteristics (25°C Unless Otherwise Noted)

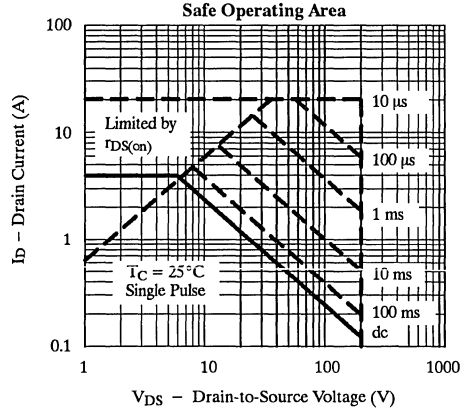
Negative signs omitted for clarity.

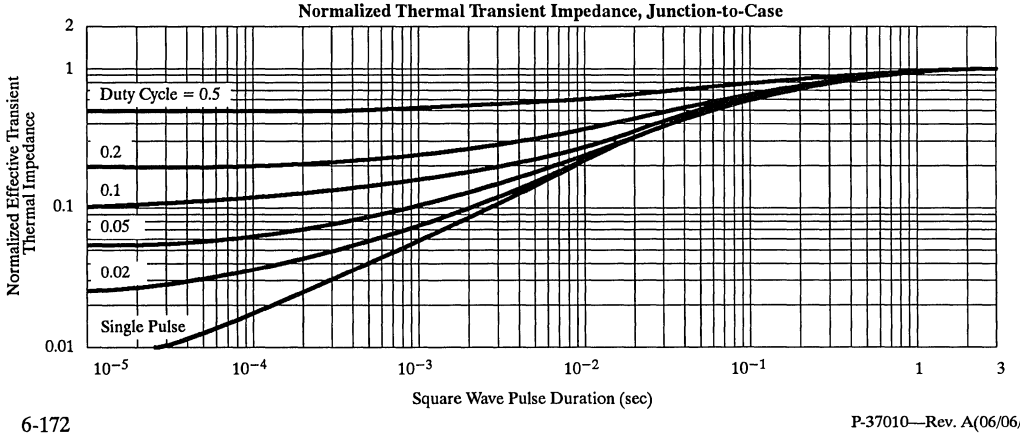




Thermal Ratings







Siliconix

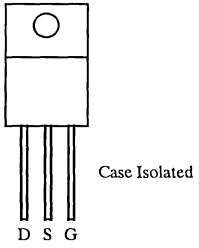
2N7075

N-Channel Enhancement-Mode Transistor

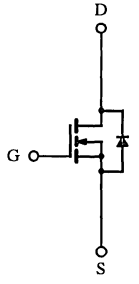
Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.065	30

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	30	A
	T_C = 100°C		24	
Pulsed Drain Current		I_{DM}	120	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		50	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.2		

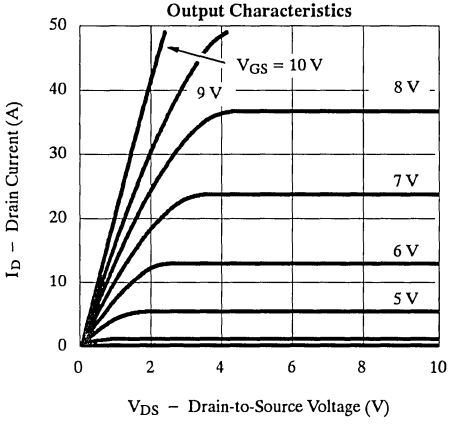
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 24 A		0.053	0.065	Ω
		V_{GS} = 10 V, I_D = 24 A, T_J = 125°C		0.08	0.10	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 24 A	9	11	27	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2800		pF
Output Capacitance	C_{oss}			1100		
Reverse Transfer Capacitance	C_{rss}			400		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 30 A		62	125	nC
Gate-Source Charge[c]	Q_{gs}			17	22	
Gate-Drain Charge[c]	Q_{gd}			35	65	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.67 Ω I_D ≅ 30 A, V_{GEN} = 10 V, R_G = 2.4 Ω		15	35	ns
Rise Time[c]	t_r			80	150	
Turn-Off Delay Time[c]	$t_{d(off)}$			60	125	
Fall Time[c]	t_f			50	100	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				30	A
Pulsed Current	I_{SM}				120	
Diode Forward Voltage[b]	V_{SD}	I_F = 30 A, V_{GS} = 0 V	0.6		1.9	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, di/dt = 100 A/µs		180	400	ns
Reverse Recovery Charge	Q_{rr}			0.6		µC

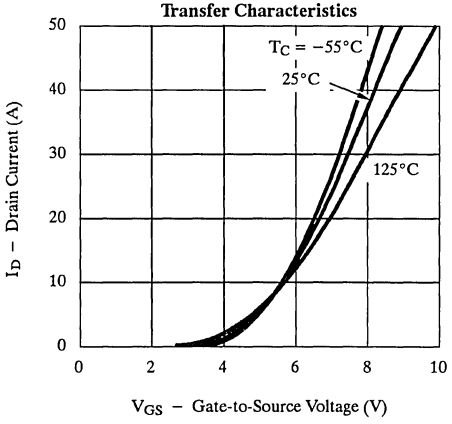
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

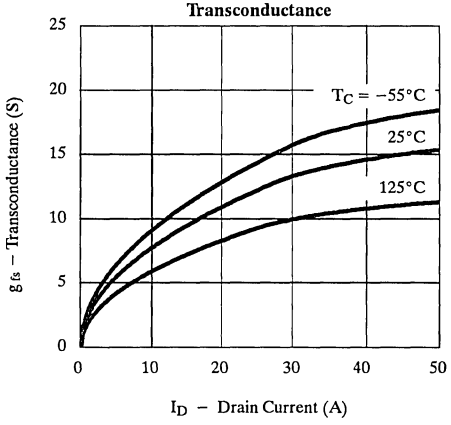
Output Characteristics



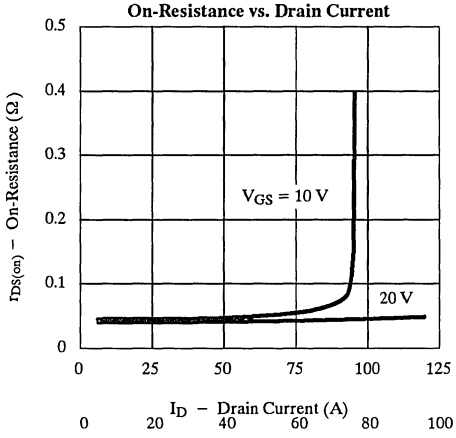
Transfer Characteristics



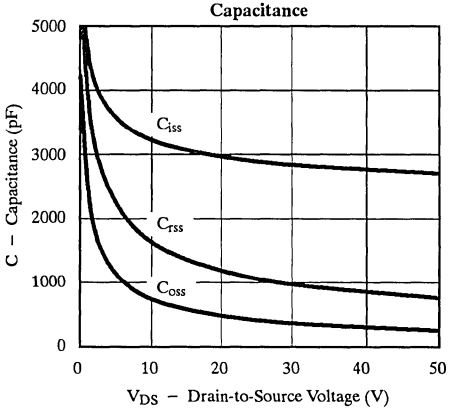
Transconductance



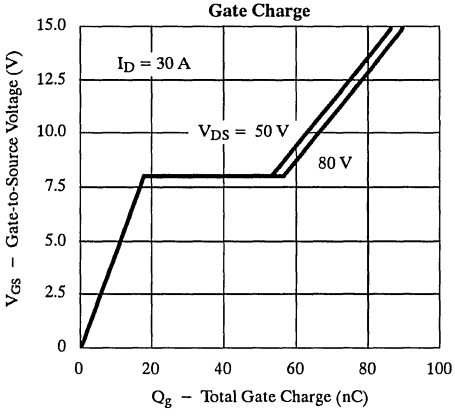
On-Resistance vs. Drain Current



Capacitance

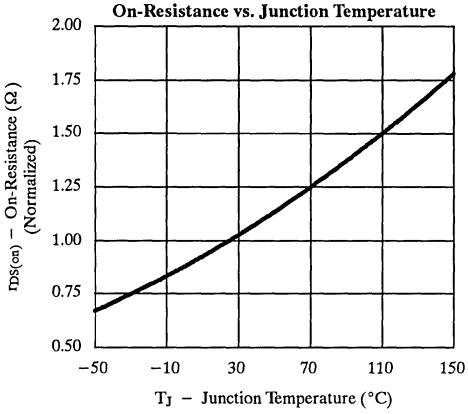


Gate Charge

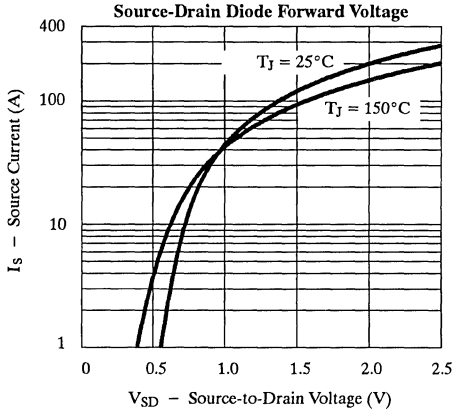


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

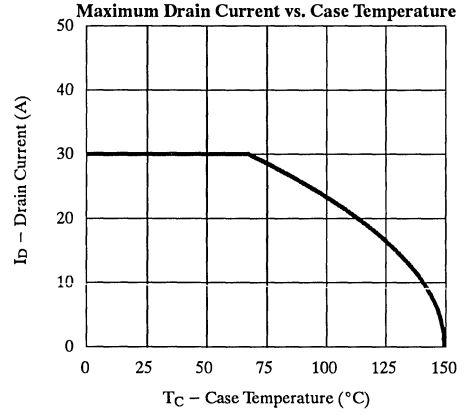


Source-Drain Diode Forward Voltage

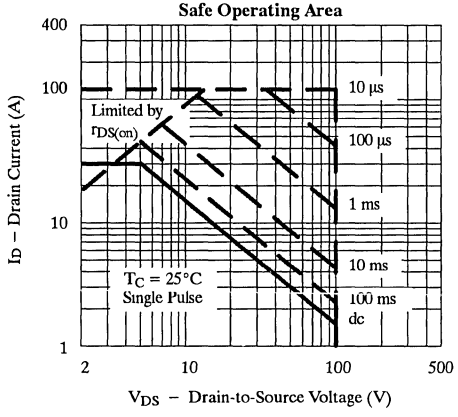


Thermal Ratings

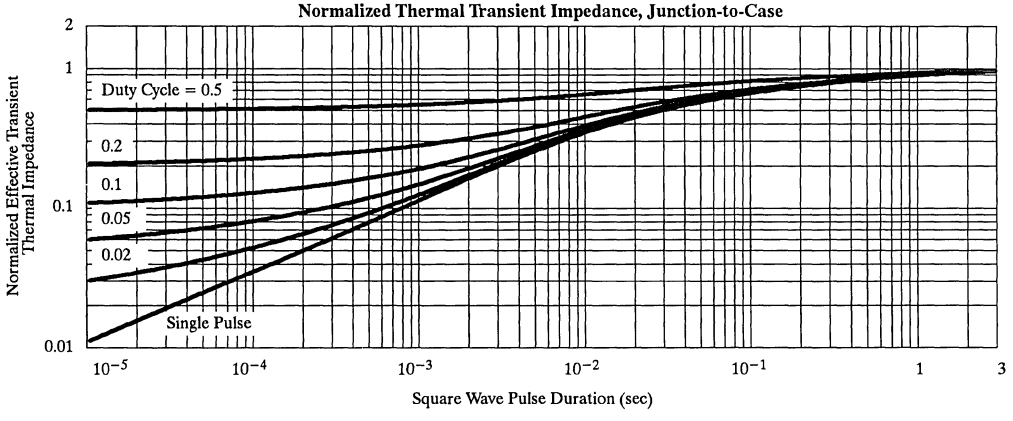
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

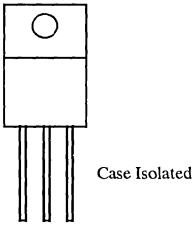
2N7076

N-Channel Enhancement-Mode Transistor

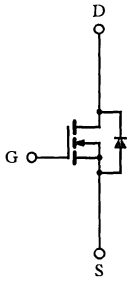
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.10	28

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	28	A
	T_C = 100°C		18	
Pulsed Drain Current		I_{DM}	112	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

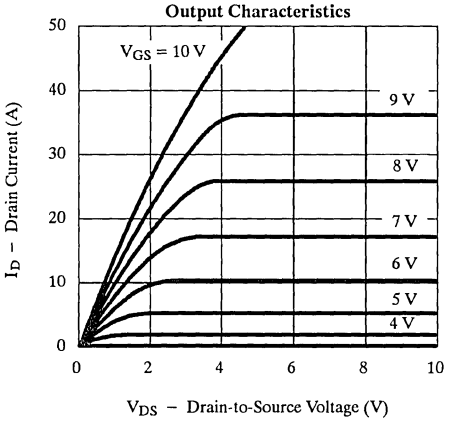
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		50	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.2		

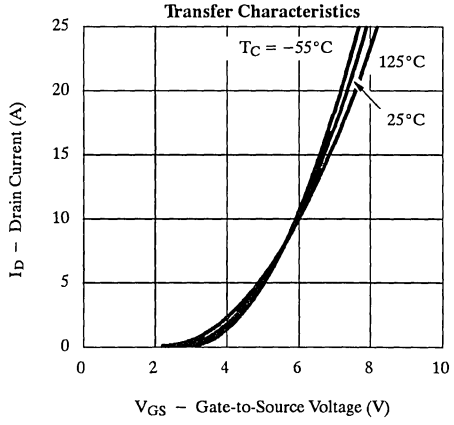
Specifications (T_J = 25°C Unless Otherwise Noted)

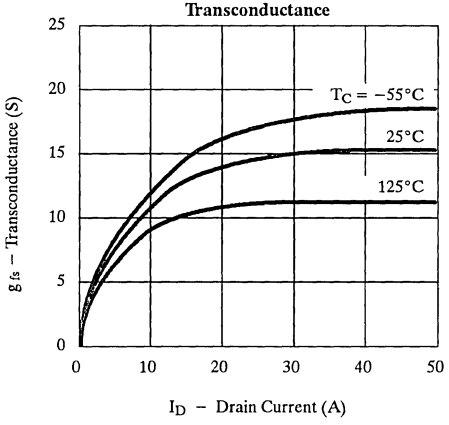
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	28			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A		0.080	0.10	Ω
		V_{GS} = 10 V, I_D = 18 A, T_J = 125°C		0.15	0.17	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 18 A	9.0	12	27	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2700		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			300		
Total Gate Charge[c]	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 28 A		63	115	nC
Gate-Source Charge[c]	Q_{gs}			14	21	
Gate-Drain Charge[c]	Q_{gd}			32	60	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 3.6 Ω I_D ≅ 28 A, V_{GEN} = 10 V, R_G = 2.4 Ω		15	35	ns
Rise Time[c]	t_r			100	150	
Turn-Off Delay Time[c]	$t_{d(off)}$			70	125	
Fall Time[c]	t_f			50	100	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				28	A
Pulsed Current	I_{SM}				112	
Diode Forward Voltage[b]	V_{SD}	I_F = 28 A, V_{GS} = 0 V	0.6		1.8	V
Reverse Recovery Time	t_{rr}	I_F = 28 A, di/dt = 100 A/µs		175	650	ns
Reverse Recovery Charge	Q_{rr}			0.6		µC

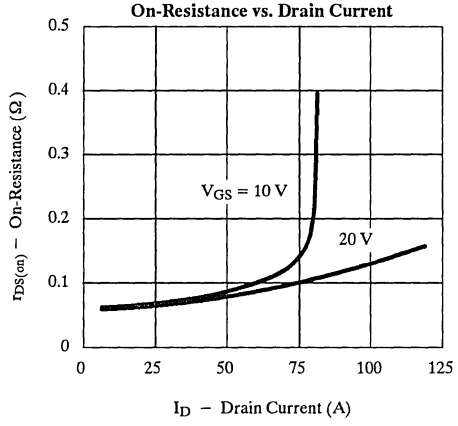
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

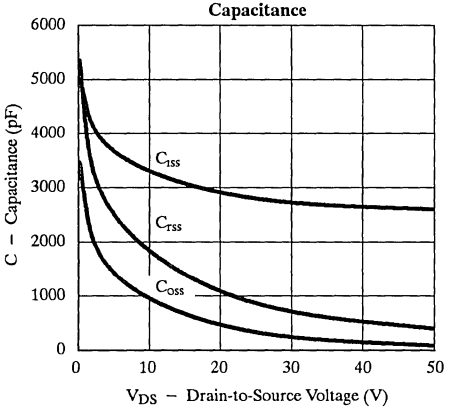
Typical Characteristics (25°C Unless Otherwise Noted)

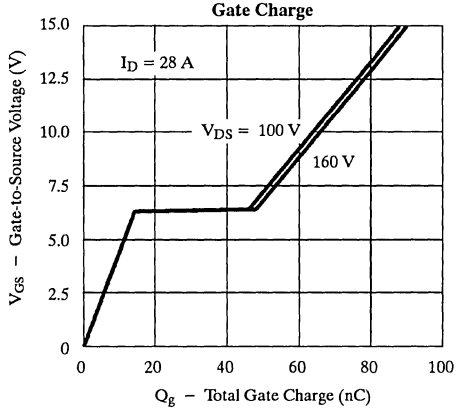




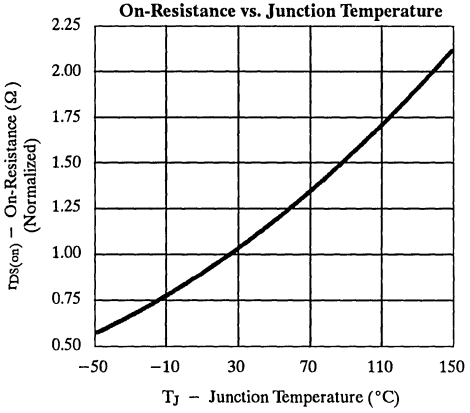


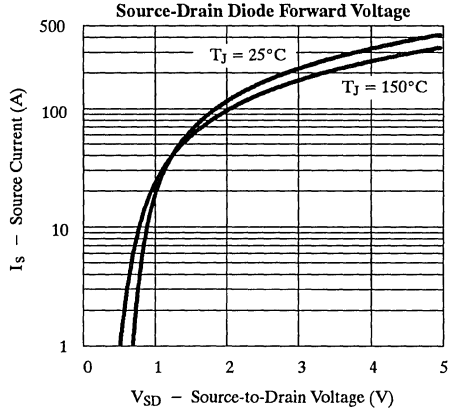




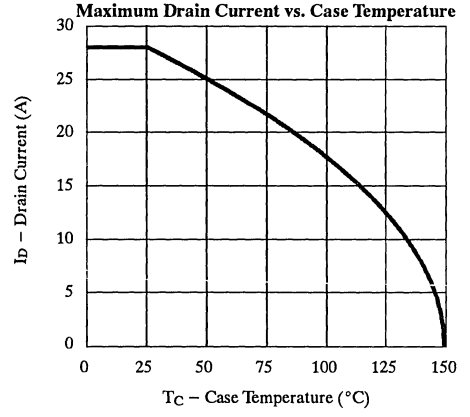


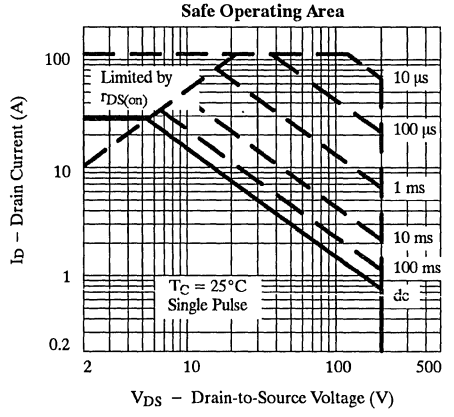
Typical Characteristics (25°C Unless Otherwise Noted)

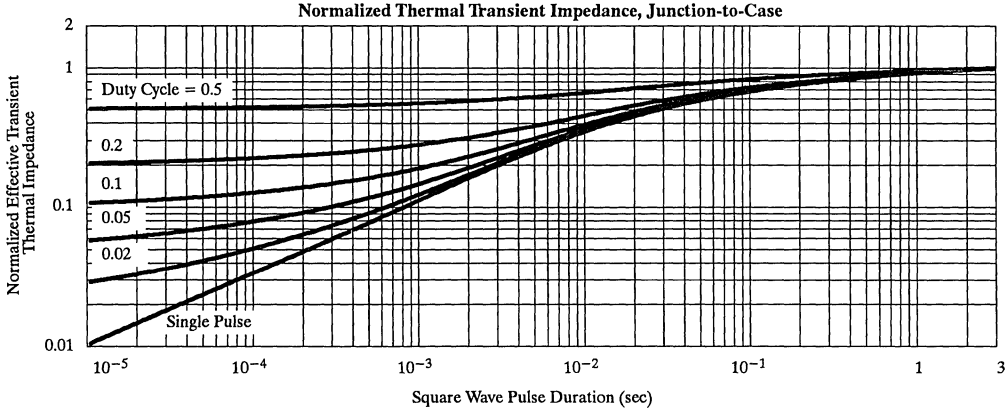




Thermal Ratings







Siliconix

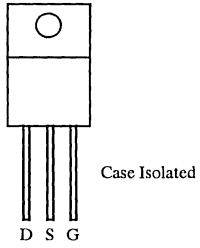
2N7077

N-Channel Enhancement-Mode Transistor

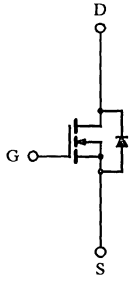
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
400	0.30	15

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	15	A
	T_C = 100°C		9.5	
Pulsed Drain Current		I_{DM}	60	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		50	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.2		

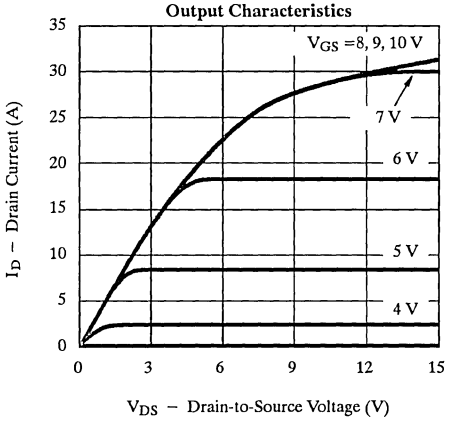
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	400			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 320 V, V_{GS} = 0 V			25	µA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	15.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 9.5 A		0.023	0.30	Ω
		V_{GS} = 10 V, I_D = 9.5 A, T_J = 125°C		0.4	0.66	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 9.5 A		8.5	24	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2700		pF
Output Capacitance	C_{oss}			450		
Reverse Transfer Capacitance	C_{rss}			160		
Total Gate Charge[c]	Q_g	V_{DS} = 200 V, V_{GS} = 10 V, I_D = 15 A		77	110	nC
Gate-Source Charge[c]	Q_{gs}			14	18	
Gate-Drain Charge[c]	Q_{gd}			39	65	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 200 V, R_L = 13 Ω I_D ≅ 15 A, V_{GEN} = 10 V, R_G = 2.4 Ω		14	35	ns
Rise Time[c]	t_r			30	60	
Turn-Off Delay Time[c]	$t_{d(off)}$			54	150	
Fall Time[c]	t_f			15	75	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				15	A
Pulsed Current	I_{SM}				60	
Diode Forward Voltage[b]	V_{SD}	I_F = 15 A, V_{GS} = 0 V	0 85		1.7	V
Reverse Recovery Time	t_{rr}	I_F = 15 A, di/dt = 100 A/µs		350	800	ns
Reverse Recovery Charge	Q_{rr}			2.0		µC

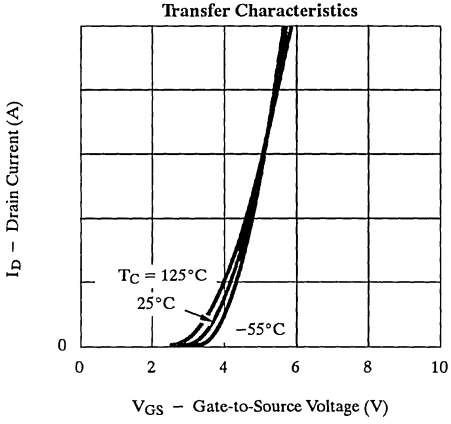
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

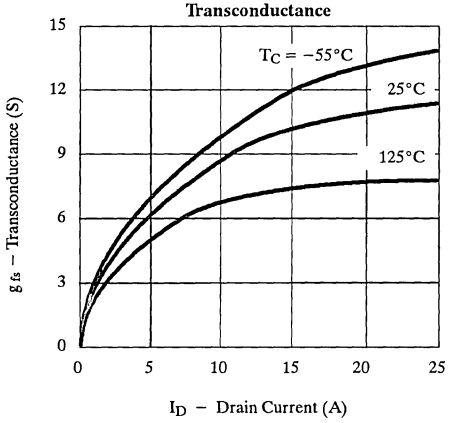
Output Characteristics



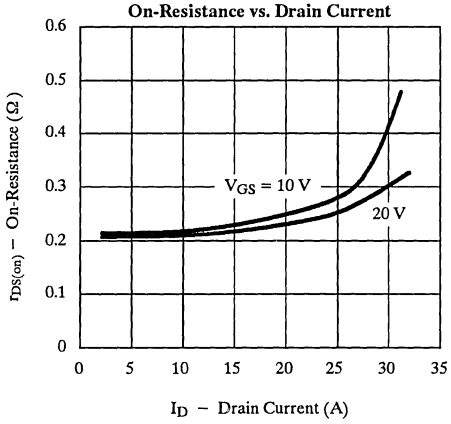
Transfer Characteristics



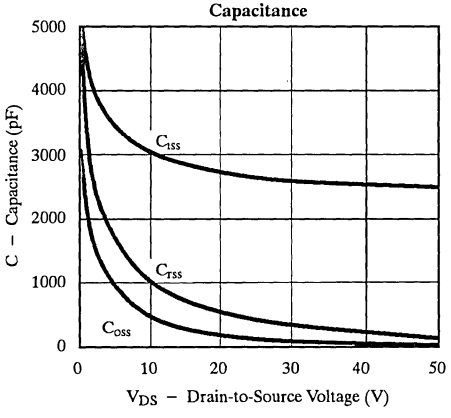
Transconductance



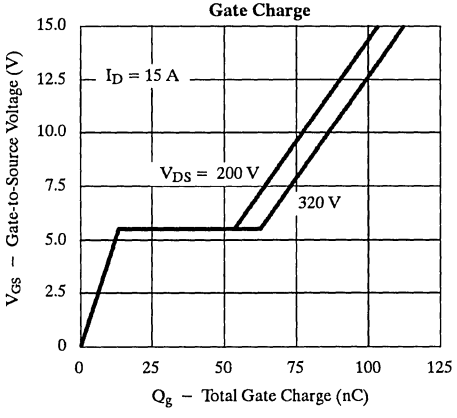
On-Resistance vs. Drain Current



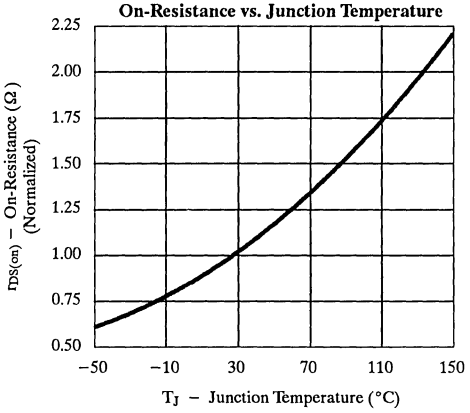
Capacitance

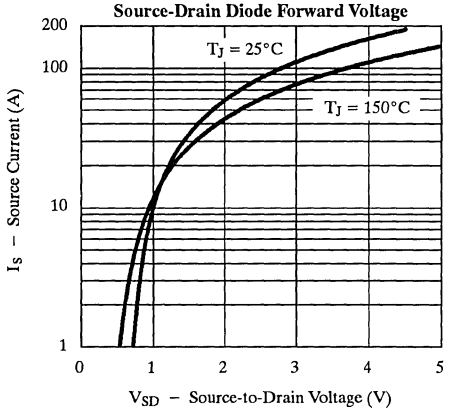


Gate Charge

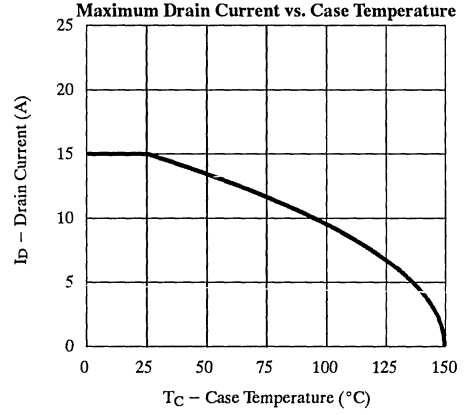


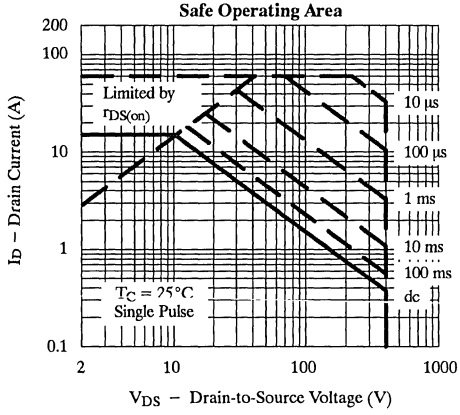
Typical Characteristics (25°C Unless Otherwise Noted)

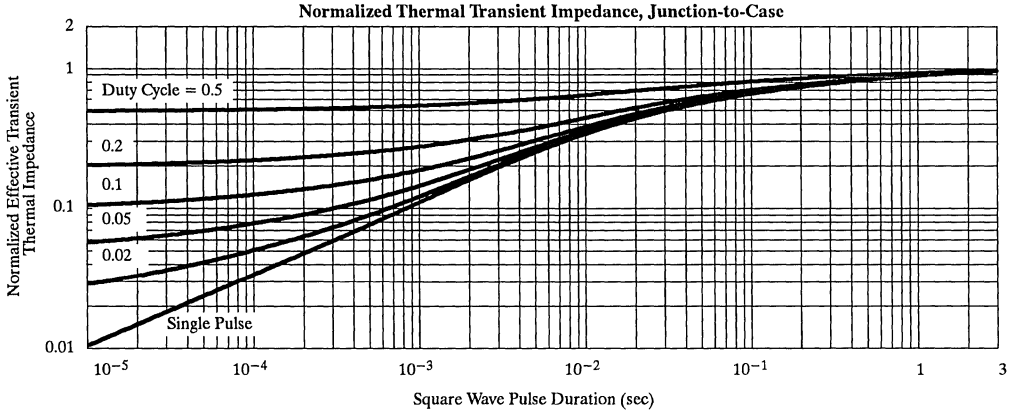




Thermal Ratings







Siliconix

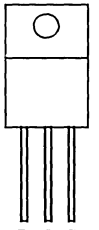
2N7078

N-Channel Enhancement-Mode Transistor

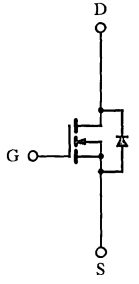
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
500	0.40	13

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	13	A
	T_C = 100°C		8.0	
Pulsed Drain Current		I_{DM}	50	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		50	°C/W
Maximum Junction-to-Case	R_{thJC}		0.83	
Case-to-Sink	R_{thCS}	0.2		

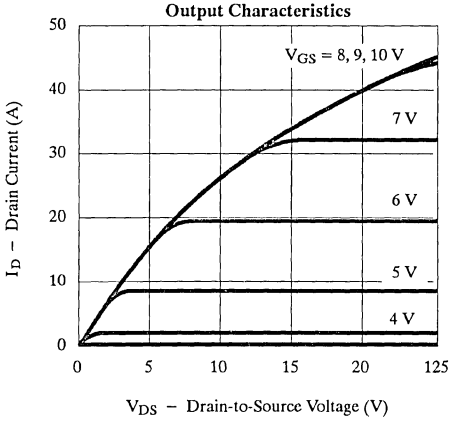
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	500			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V			25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	13.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 8.0 A		0.31	0.40	Ω
		V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C		0.67	0.90	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 8.0 A	8.0	10	24	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2700		pF
Output Capacitance	C_{oss}			500		
Reverse Transfer Capacitance	C_{rss}			140		
Total Gate Charge[c]	Q_g	V_{DS} = 250 V, V_{GS} = 10 V, I_D = 13 A		75	120	nC
Gate-Source Charge[c]	Q_{gs}			12	19	
Gate-Drain Charge[c]	Q_{gd}			35	70	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 13 Ω I_D ≅ 13 A, V_{GEN} = 10 V, R_G = 2.4 Ω		13	35	ns
Rise Time[c]	t_r			26	50	
Turn-Off Delay Time[c]	$t_{d(off)}$			55	150	
Fall Time[c]	t_f			17	70	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				13	A
Pulsed Current	I_{SM}				50	
Diode Forward Voltage[b]	V_{SD}	I_F = 13 A, V_{GS} = 0 V	0.80		1.6	V
Reverse Recovery Time	t_{rr}	I_F = 13 A, di/dt = 100 A/µs		400	1000	ns
Reverse Recovery Charge	Q_{rr}			2.0		µC

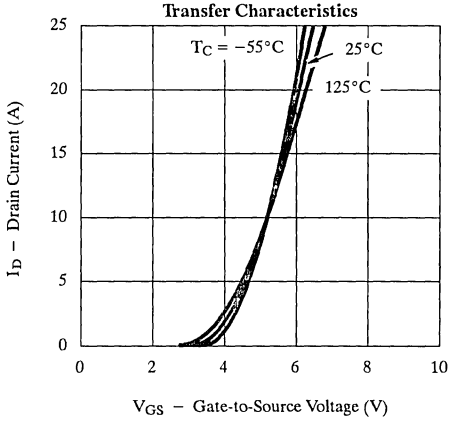
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

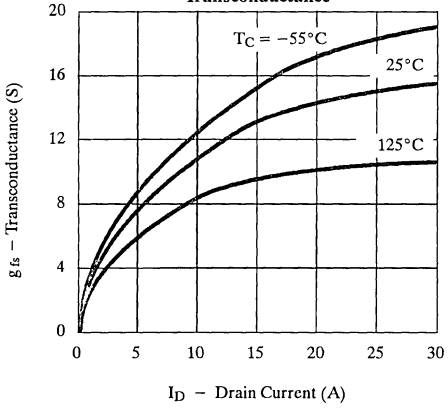
Output Characteristics



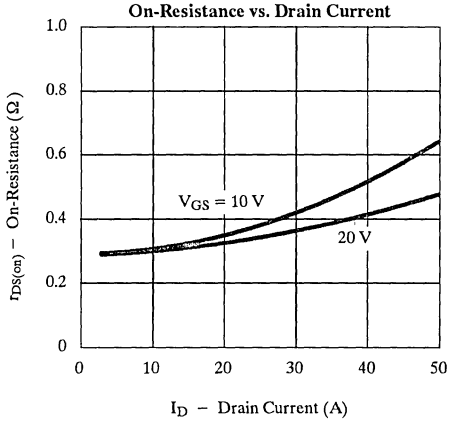
Transfer Characteristics



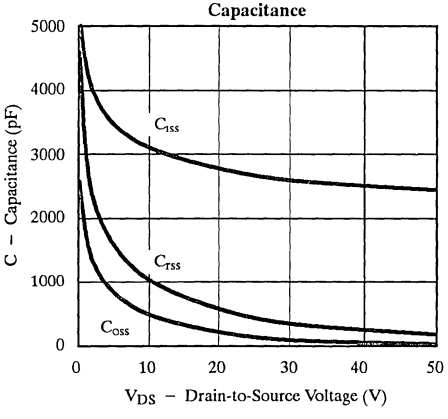
Transconductance



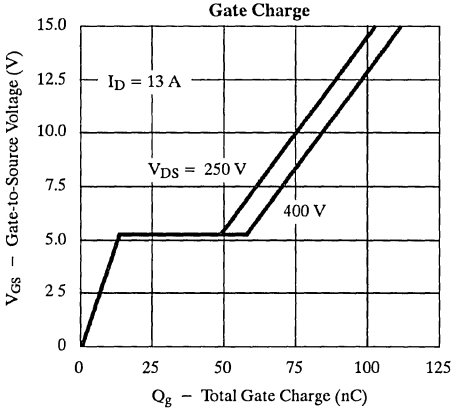
On-Resistance vs. Drain Current



Capacitance

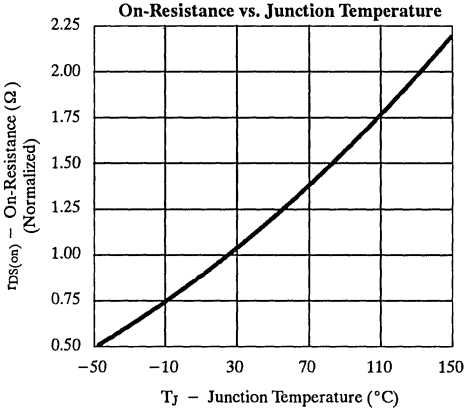


Gate Charge

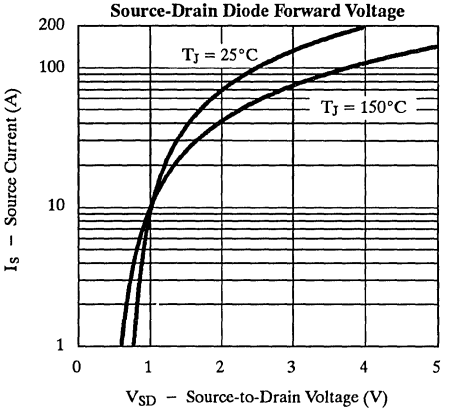


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

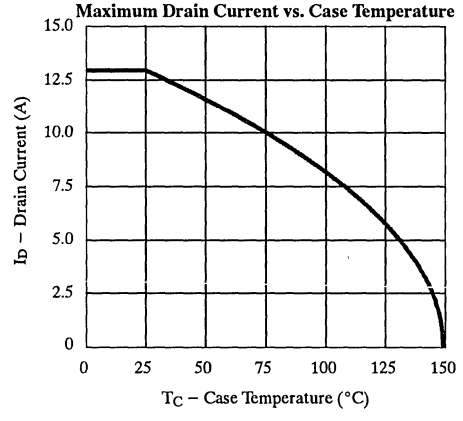


Source-Drain Diode Forward Voltage

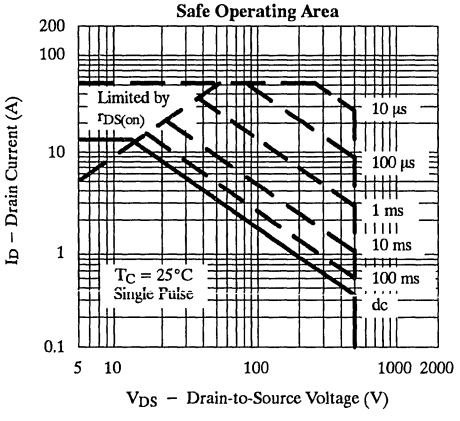


Thermal Ratings

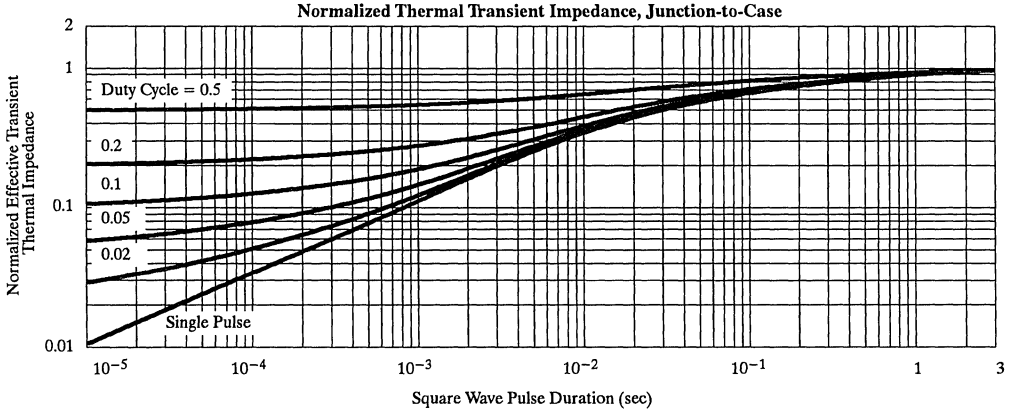
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

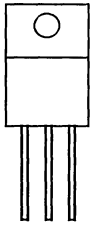
2N7079

P-Channel Enhancement-Mode Transistor

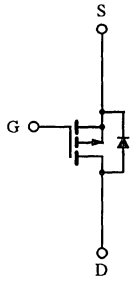
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.210	−17

TO-254AA
Hermetic Package



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−17	A
	T_C = 100°C		−10.8	
Pulsed Drain Current		I_{DM}	−68	
Maximum Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		50	°C/W
Maximum Junction-to-Case	R_{thJC}		1.25	
Case-to-Sink	R_{thCS}	0.2		

Specifications (T_J = 25°C Unless Otherwise Noted)

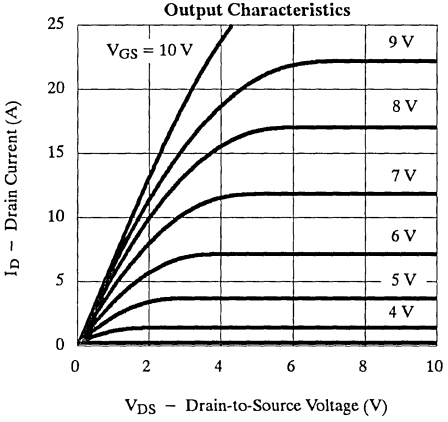
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−25	μA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−17			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −10.8 A		0.14	0.210	Ω
		V_{GS} = −10 V, I_D = −10.8 A, T_J = 125°C		0.22	0.32	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −10.8 A	5.0	5.5		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			300		
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = −10 V, I_D = −17 A		47	60	nC
Gate-Source Charge[c]	Q_{gs}			10	18	
Gate-Drain Charge[c]	Q_{gd}			27	36	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 2.7 Ω I_D ≅ −17 A, V_{GEN} = −10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			50	80	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	80	
Fall Time[c]	t_f			15	60	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−17	A
Pulsed Current	I_{SM}				−68	
Diode Forward Voltage[b]	V_{SD}	I_F = −17 A, V_{GS} = 0 V			−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −17 A, di/dt = 100 A/μs		150		ns
Reverse Recovery Charge	Q_{rr}			0.3		μC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
c. Independent of operating temperature.

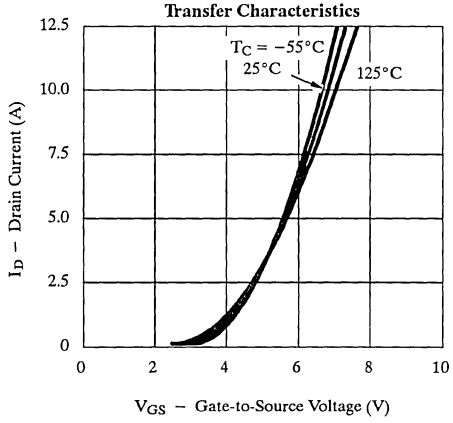
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

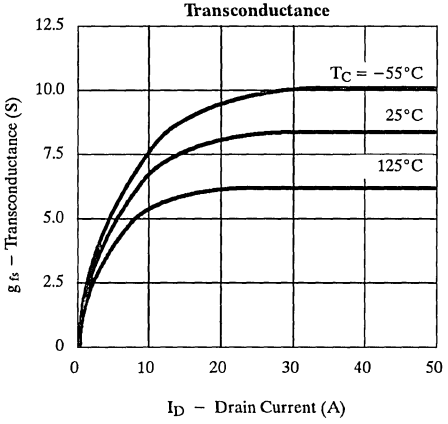
Output Characteristics



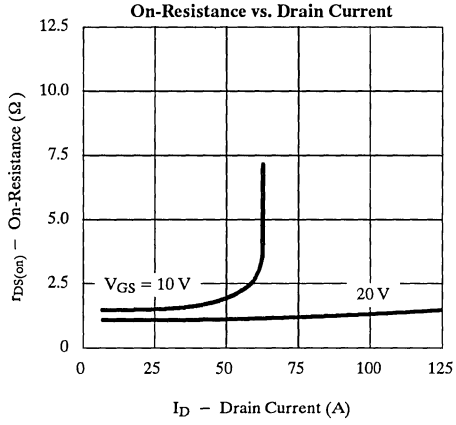
Transfer Characteristics



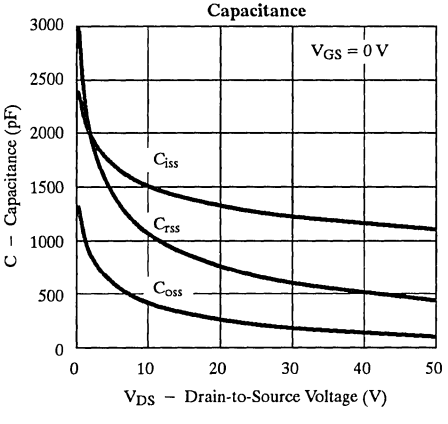
Transconductance



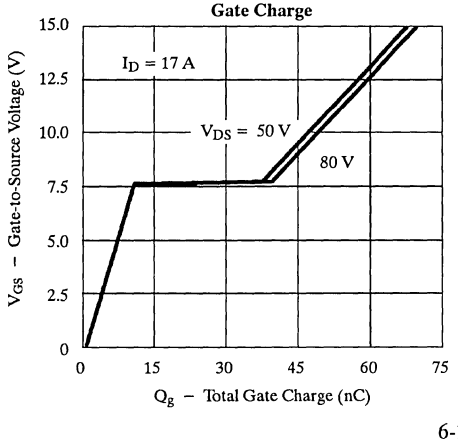
On-Resistance vs. Drain Current



Capacitance



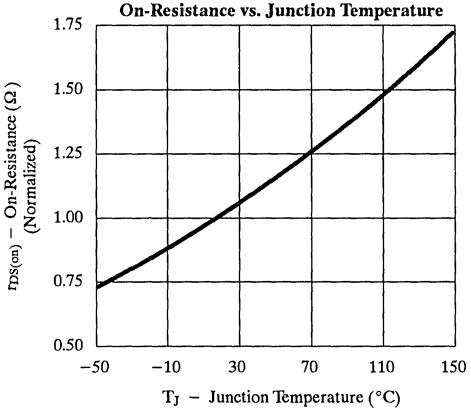
Gate Charge



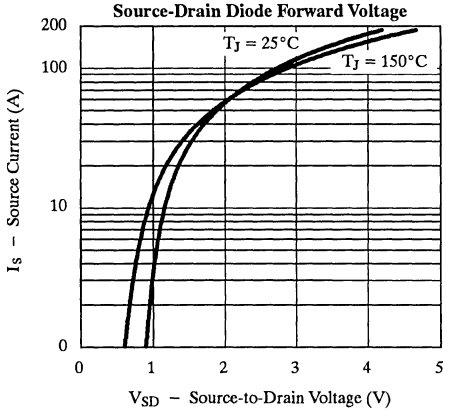
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

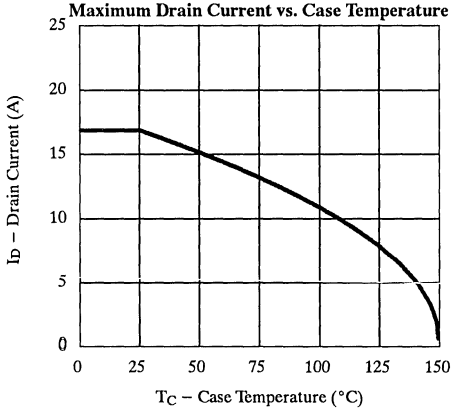


Source-Drain Diode Forward Voltage

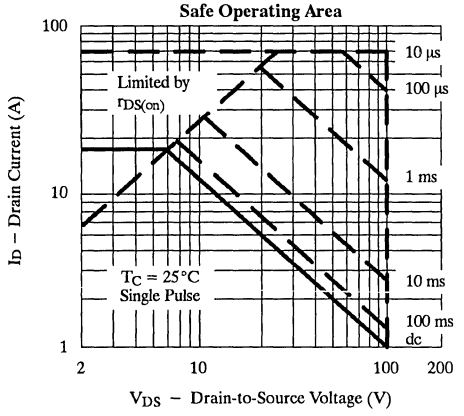


Thermal Ratings

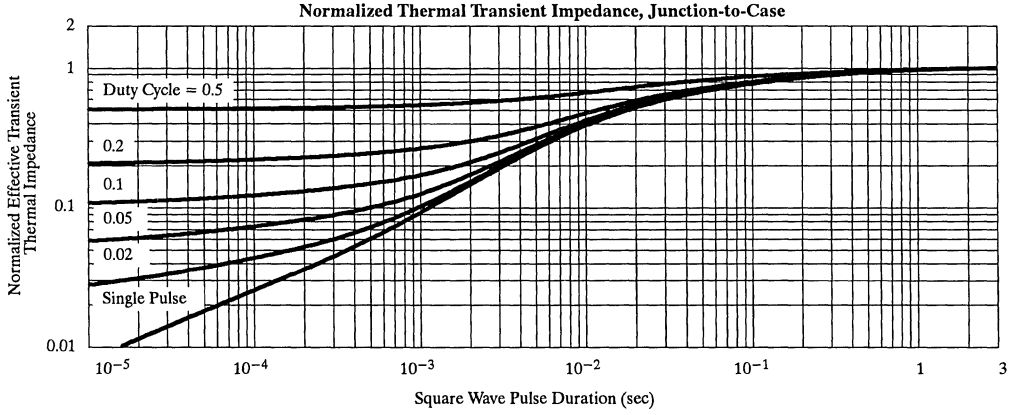
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

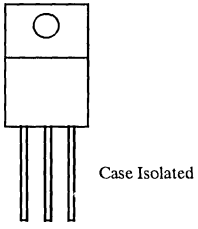
2N7080

P-Channel Enhancement-Mode Transistor

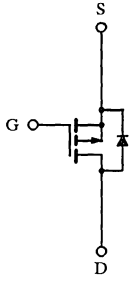
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−200	0.500	−9.5

TO-254AA
Hermetic Package



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−9.5	A
	T_C = 100°C		−6.1	
Pulsed Drain Current		I_{DM}	−38	
Maximum Power Dissipation	T_C = 25°C	P_D	100	W
	T_C = 100°C		40	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		50	°C/W
Maximum Junction-to-Case	R_{thJC}		1.25	
Case-to-Sink	R_{thCS}	0.2		

Specifications (T_J = 25°C Unless Otherwise Noted)

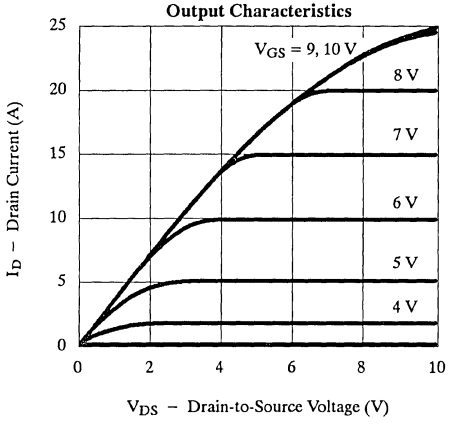
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −160 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −160 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−9.5			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −6.1 A		0.28	0.500	Ω
		V_{GS} = −10 V, I_D = −6.1 A, T_J = 125°C		0.5	1.0	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −6.1 A	4.0	4.8		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			450		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge[c]	Q_g	V_{DS} = −100 V, V_{GS} = −10 V, I_D = −9.5 A		55	75	nC
Gate-Source Charge[c]	Q_{gs}			9.0	15	
Gate-Drain Charge[c]	Q_{gd}			30	45	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −100 V, R_L = 10.2 Ω I_D = −9.5 A, V_{GEN} = −10 V, R_G = 4.7 Ω		10	25	ns
Rise Time[c]	t_r			30	50	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	80	
Fall Time[c]	t_f			16	40	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−9.5	A
Pulsed Current	I_{SM}				−38	
Diode Forward Voltage[b]	V_{SD}	I_F = −9.5 A, V_{GS} = 0 V			−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −9.5 A, di/dt = 100 A/µs		200		ns
Reverse Recovery Charge	Q_{rr}			1.0		µC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

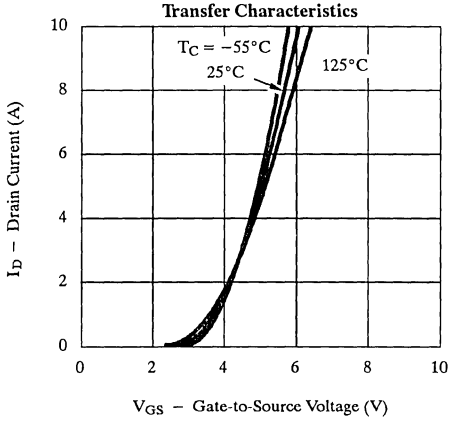
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

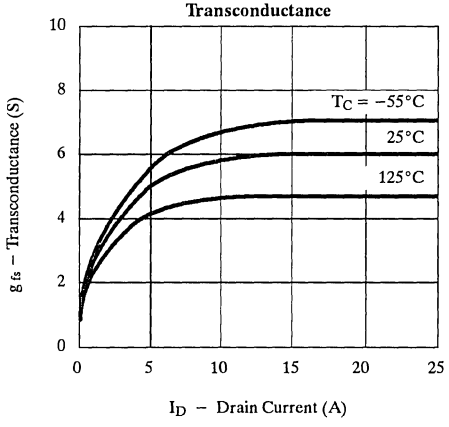
Output Characteristics



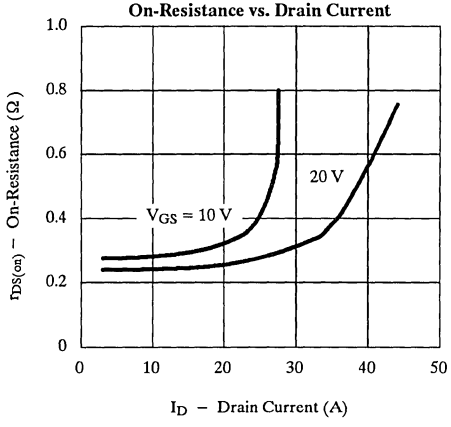
Transfer Characteristics



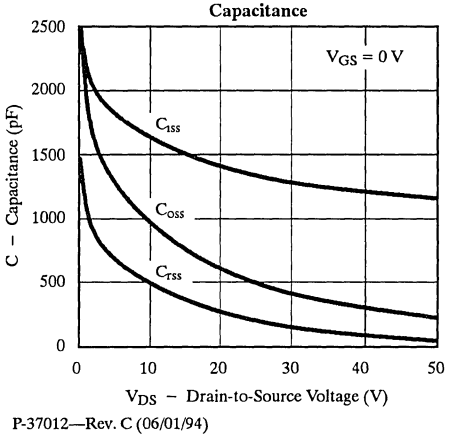
Transconductance



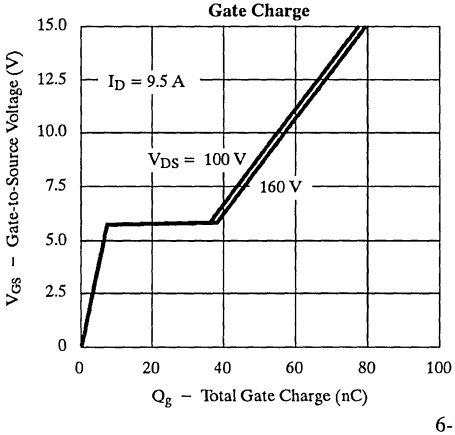
On-Resistance vs. Drain Current



Capacitance

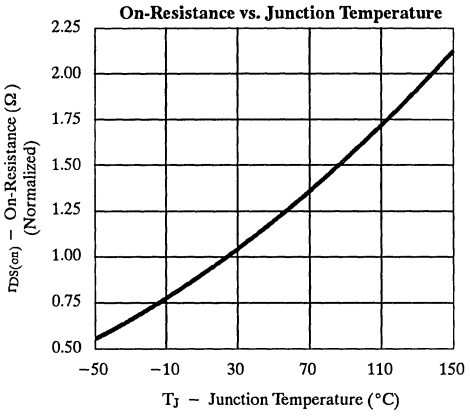


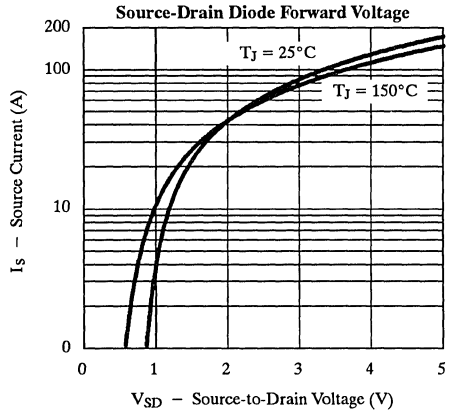
Gate Charge



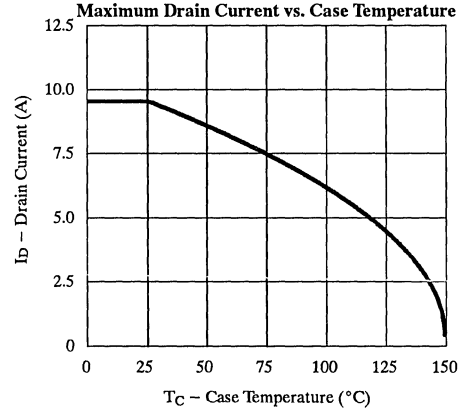
Typical Characteristics (25°C Unless Otherwise Noted)

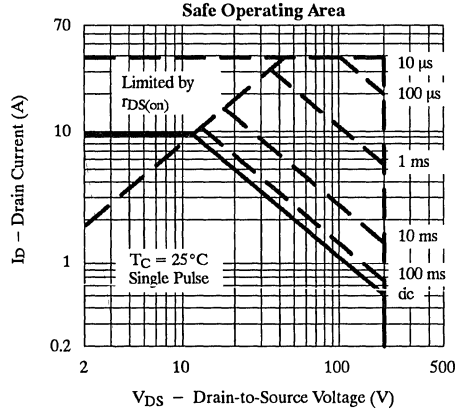
Negative signs omitted for clarity.

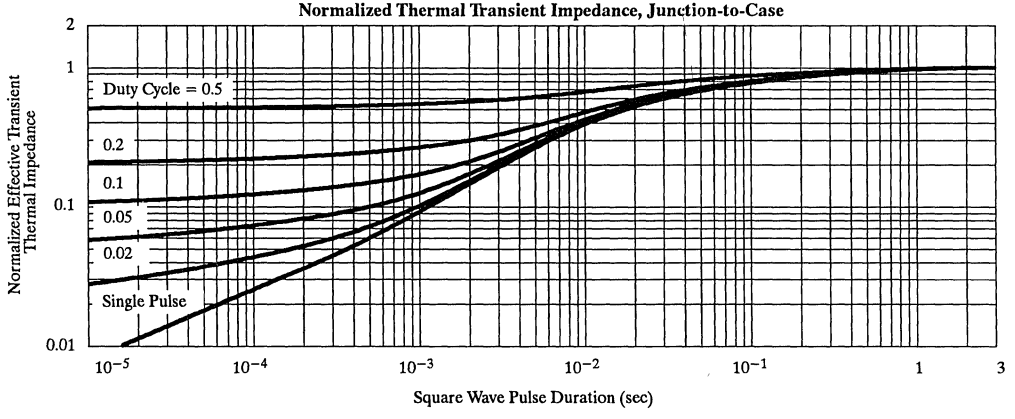




Thermal Ratings







Siliconix

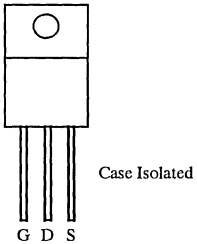
2N7081

N-Channel Enhancement-Mode Transistor

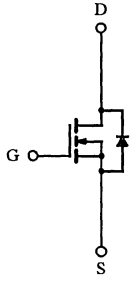
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.15	13

TO-257AB
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	13	A
	T_C = 100°C		8.0	
Pulsed Drain Current		I_{DM}	48	
Maximum Power Dissipation	T_C = 25°C	P_D	50	W
	T_C = 100°C		20	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.5	
Case-to-Sink	R_{thCS}	1.0		

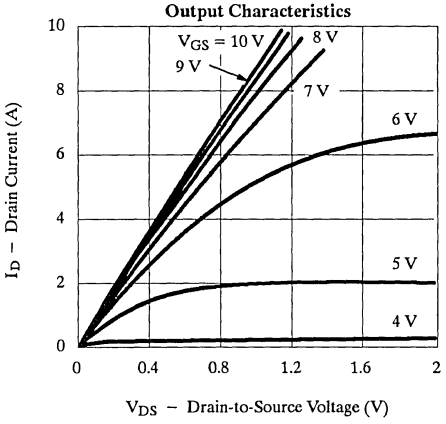
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	13.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 8.0 A		0.12	0.15	Ω
		V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C		0.22	0.27	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 8.0 A	4.0	5.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		600		pF
Output Capacitance	C_{oss}			190		
Reverse Transfer Capacitance	C_{rss}			35		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 13 A		17	30	nC
Gate-Source Charge[c]	Q_{gs}			6	9.0	
Gate-Drain Charge[c]	Q_{gd}			9	20	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 3.8 Ω, I_D ≅ 13 A, V_{GEN} = 10 V, R_G = 7.5 Ω		7	30	ns
Rise Time[c]	t_r			45	80	
Turn-Off Delay Time[c]	$t_{d(off)}$			30	60	
Fall Time[c]	t_f			10	40	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				13	A
Pulsed Current	I_{SM}				48	
Diode Forward Voltage[b]	V_{SD}	I_F = 13 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 13 A, di/dt = 100 A/µs		100	300	ns
Reverse Recovery Charge	Q_{rr}			0.7		µC

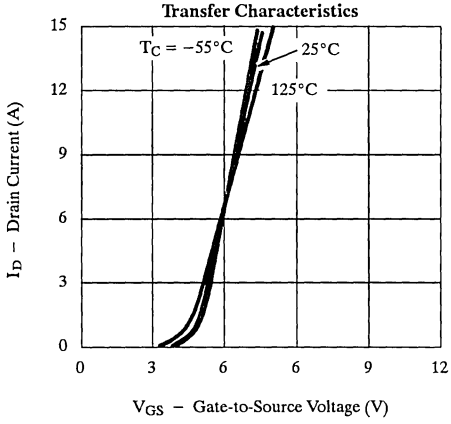
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

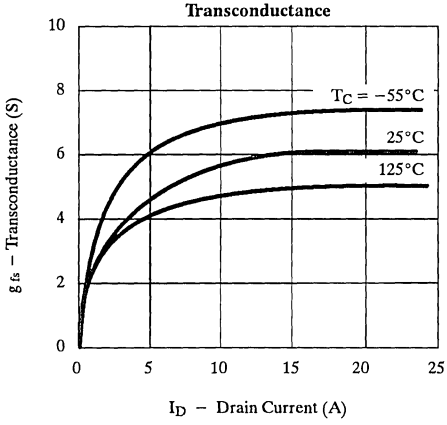
Output Characteristics



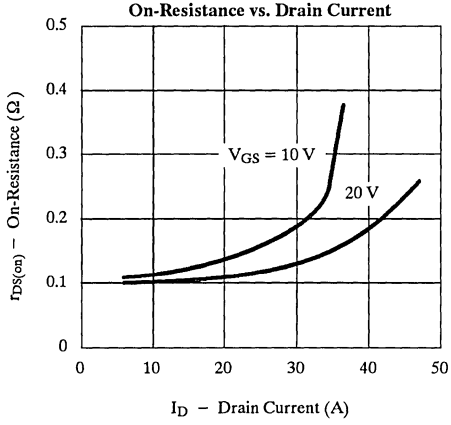
Transfer Characteristics



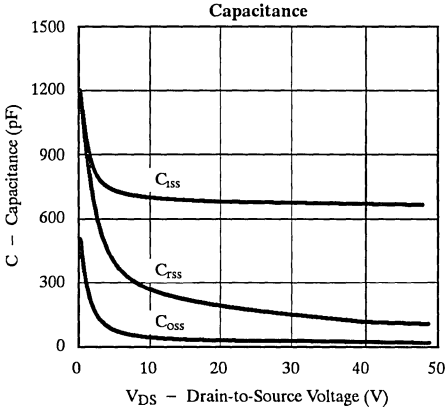
Transconductance



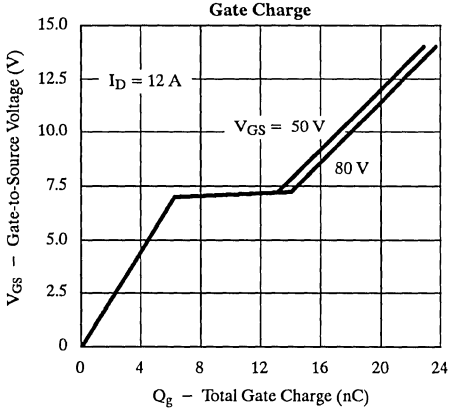
On-Resistance vs. Drain Current



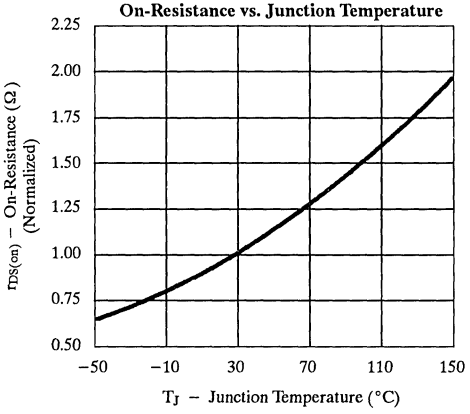
Capacitance

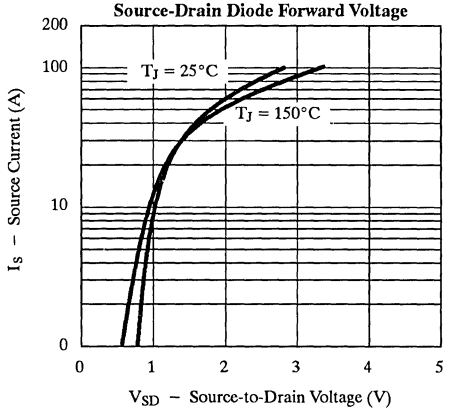


Gate Charge

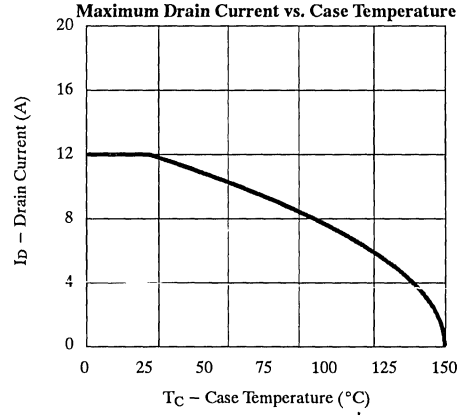


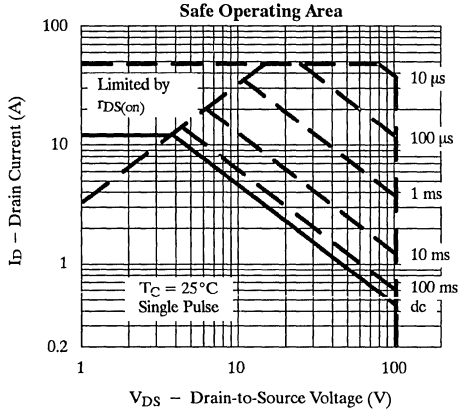
Typical Characteristics (25°C Unless Otherwise Noted)

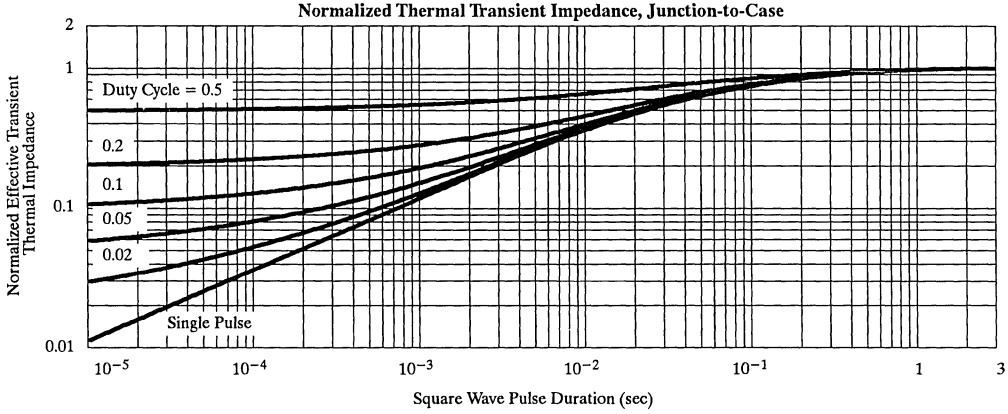




Thermal Ratings







Siliconix

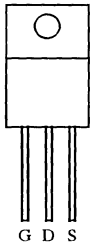
2N7085

N-Channel Enhancement-Mode Transistor

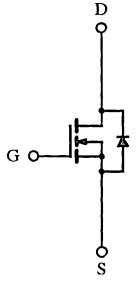
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.075	20

TO-257AB
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	20	A
	T_C = 100°C		12	
Pulsed Drain Current		I_{DM}	80	
Maximum Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		20	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

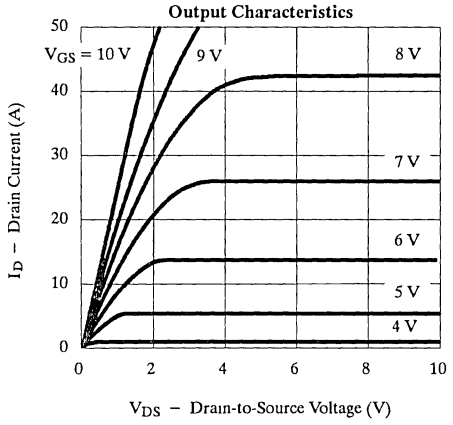
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.1	
Case-to-Sink	R_{thCS}	1.0		

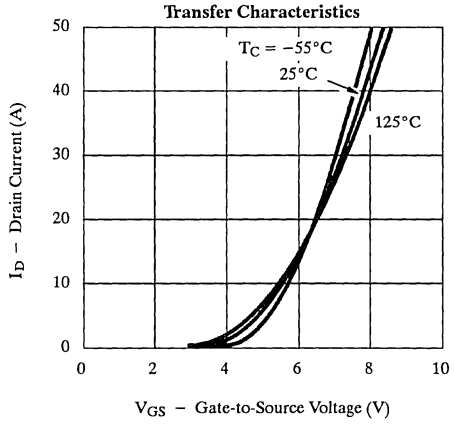
Specifications (T_J = 25°C Unless Otherwise Noted)

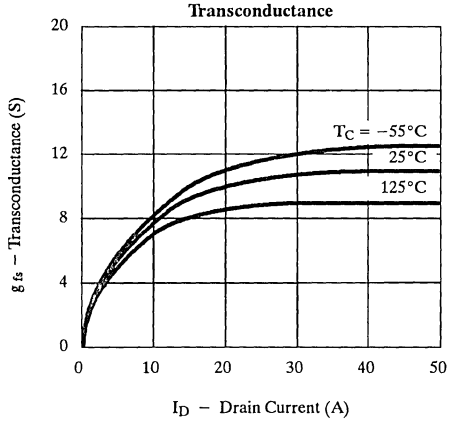
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 12 A		0.06	0.075	Ω
		V_{GS} = 10 V, I_D = 12 A, T_J = 125°C		0.11	0.14	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 12 A	5.0	8.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1400		pF
Output Capacitance	C_{oss}			480		
Reverse Transfer Capacitance	C_{rss}			110		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 20 A		35	50	nC
Gate-Source Charge[c]	Q_{gs}			10	20	
Gate-Drain Charge[c]	Q_{gd}			18	25	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 2.5 Ω I_D ≅ 20 A, V_{GEN} = 10 V, R_G = 4.7 Ω		13	30	ns
Rise Time[c]	t_r			85	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	80	
Fall Time[c]	t_f			75	95	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				20	A
Pulsed Current	I_{SM}				80	
Diode Forward Voltage[b]	V_{SD}	I_F = 20 A, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = 20 A, di/dt = 100 A/µs		150	400	ns
Reverse Recovery Charge	Q_{rr}			0.5		µC

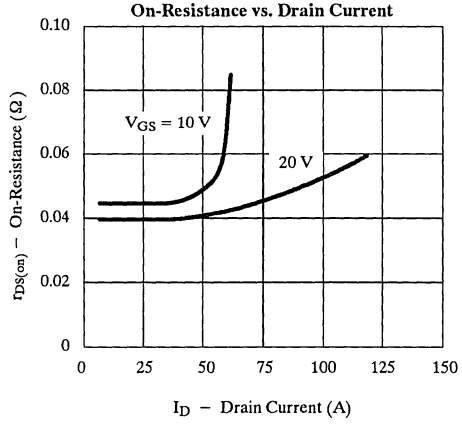
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

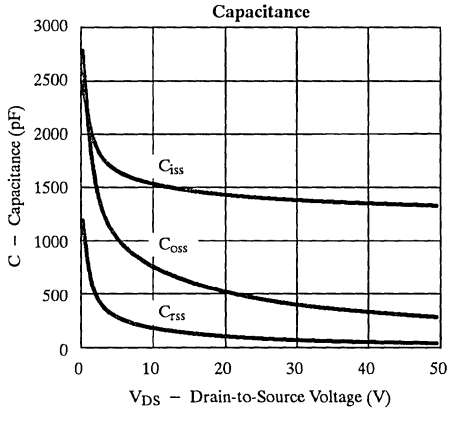
Typical Characteristics (25°C Unless Otherwise Noted)

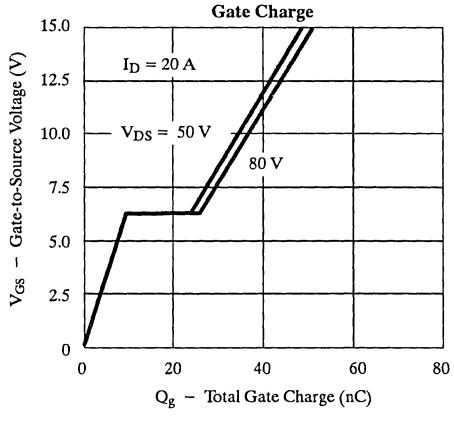






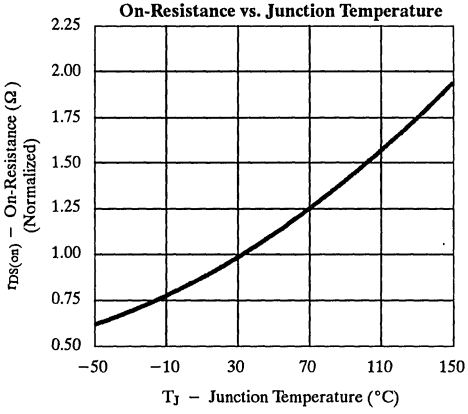




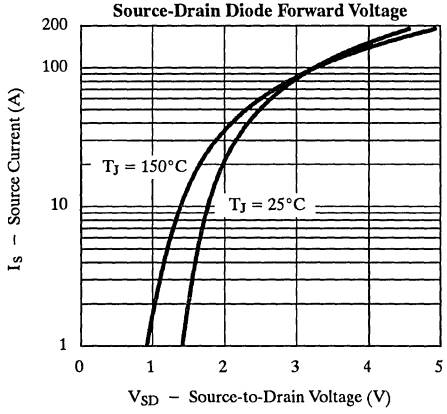


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

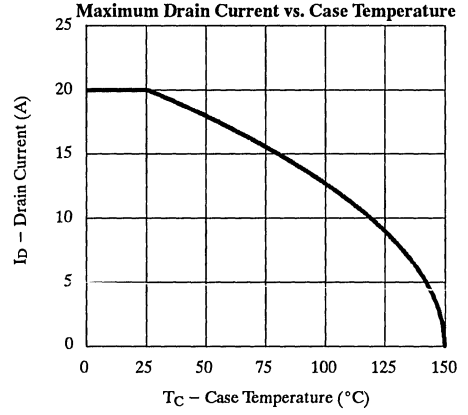


Source-Drain Diode Forward Voltage

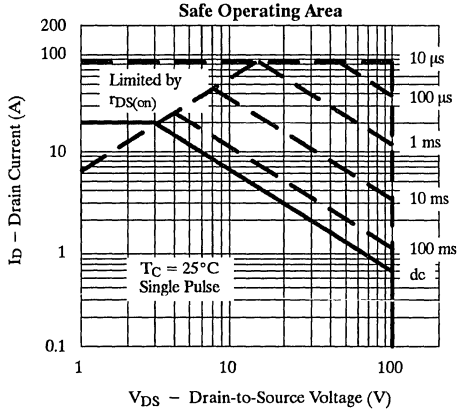


Thermal Ratings

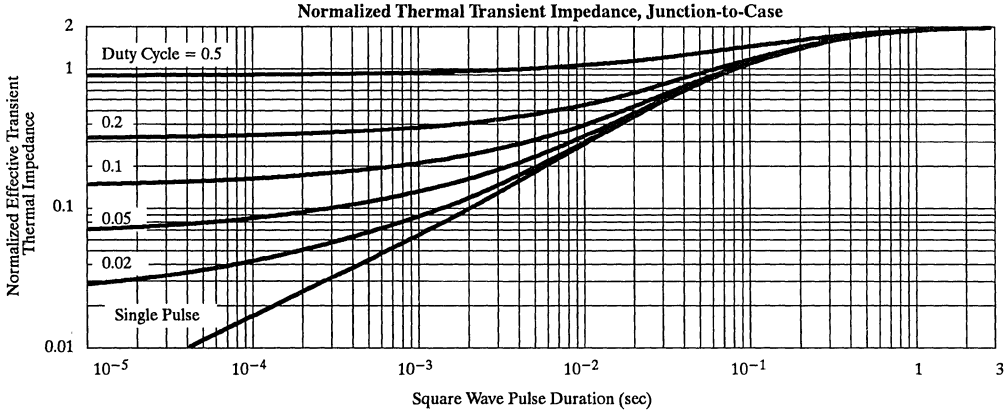
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

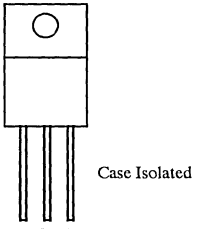
2N7086

N-Channel Enhancement-Mode Transistor

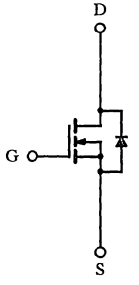
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.16	14

TO-257AB
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	14	A
	T_C = 100°C		8.5	
Pulsed Drain Current		I_{DM}	56	
Maximum Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		23	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

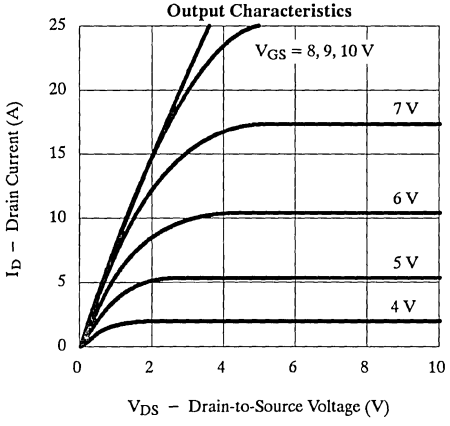
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.1	
Case-to-Sink	R_{thCS}	1.0		

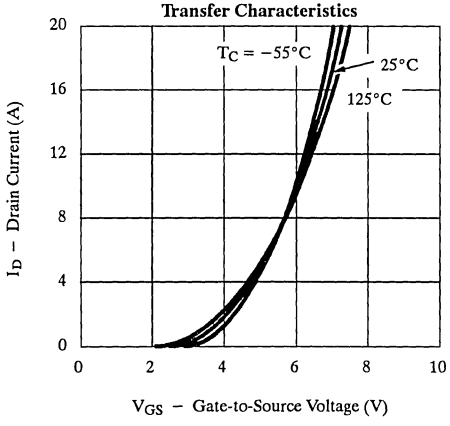
Specifications (T_J = 25°C Unless Otherwise Noted)

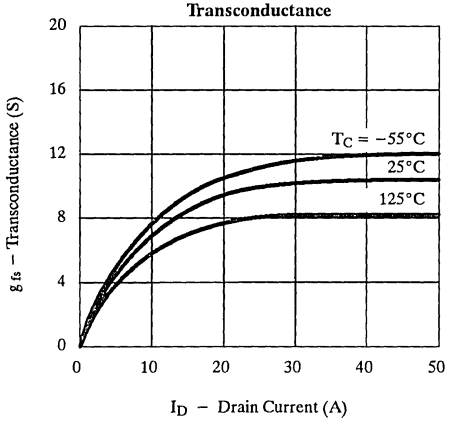
Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4 0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	µA
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	14			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 8.5 A		0.14	0.16	Ω
		V_{GS} = 10 V, I_D = 8.5 A, T_J = 125°C		0.25	0.30	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 8.5 A	5.0			S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1550		pF
Output Capacitance	C_{oss}			500		pF
Reverse Transfer Capacitance	C_{rss}			220		pF
Total Gate Charge[c]	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 14 A		44	77	nC
Gate-Source Charge[c]	Q_{gs}			10	15	nC
Gate-Drain Charge[c]	Q_{gd}			26	35	nC
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 7.1 Ω I_D ≃ 14 A, V_{GEN} = 10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			60	100	ns
Turn-Off Delay Time[c]	$t_{d(off)}$			30	80	ns
Fall Time[c]	t_f			40	95	ns
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				14	A
Pulsed Current	I_{SM}				56	A
Diode Forward Voltage[b]	V_{SD}	I_F = 14 A, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, di/dt = 100 A/µs		150	650	ns
Reverse Recovery Charge	Q_{rr}			0.5		µC

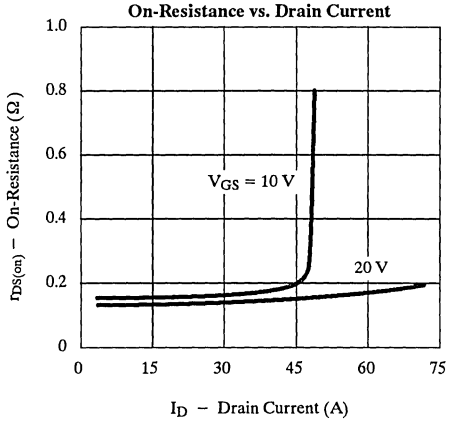
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

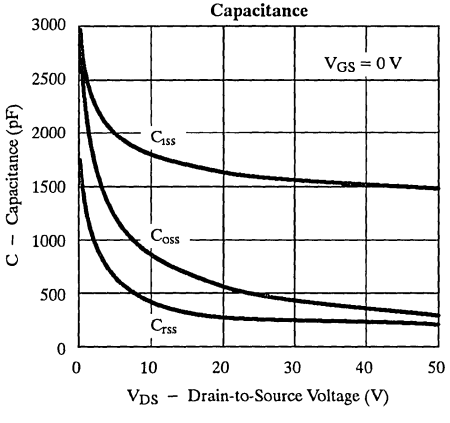
Typical Characteristics (25°C Unless Otherwise Noted)

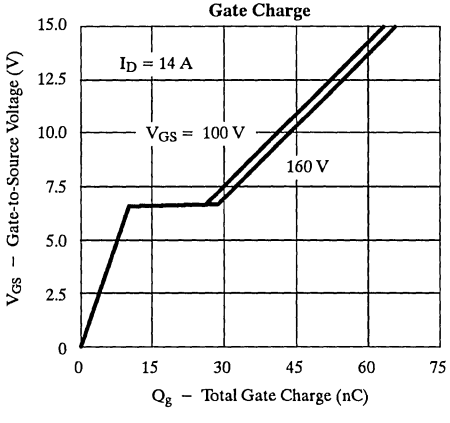




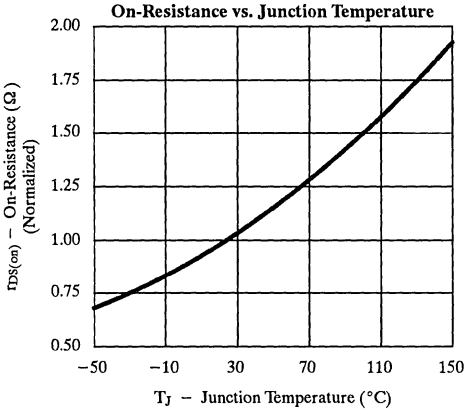


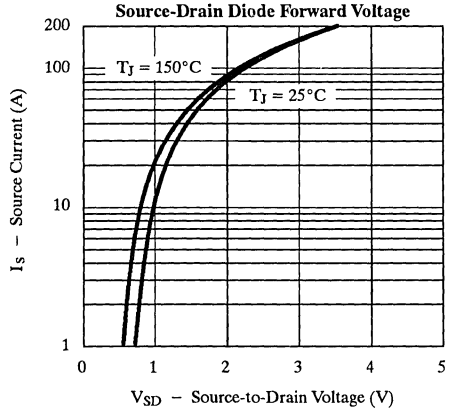




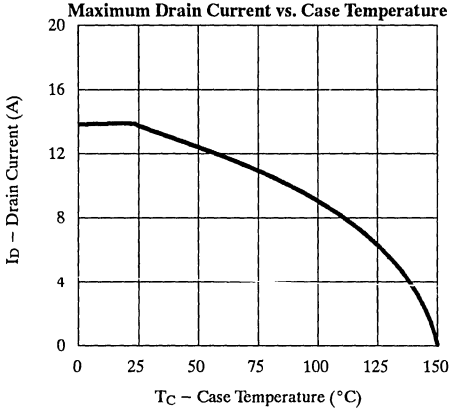


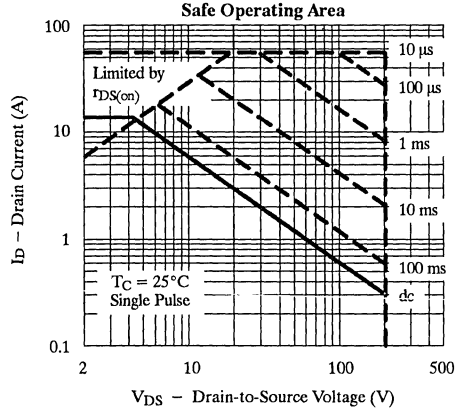
Typical Characteristics (25°C Unless Otherwise Noted)

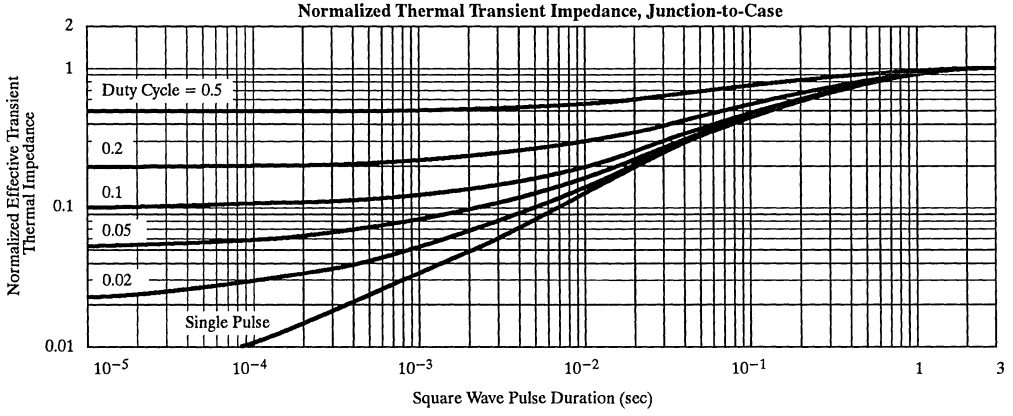




Thermal Ratings







Siliconix

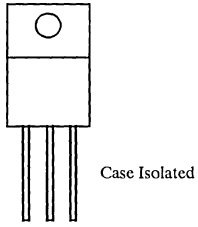
2N7089

P-Channel Enhancement-Mode Transistor

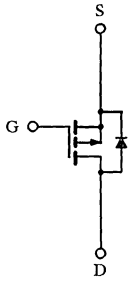
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.30	−10

TO-257AB
Hermetic Package



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−10	A
	T_C = 100°C		−6.7	
Pulsed Drain Current		I_{DM}	−40	
Maximum Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		24	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($1/16$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.0	
Case-to-Sink	R_{thCS}	1.0		

Specifications (T_J = 25°C Unless Otherwise Noted)

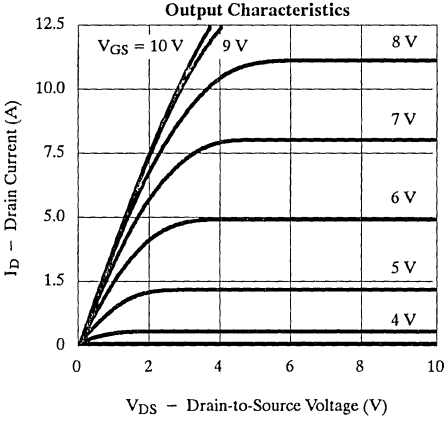
Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−2.0		−4.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−25	μA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−250	μA
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −6.7 A		0.25	0.30	Ω
		V_{GS} = −10 V, I_D = −6.7 A, T_J = 125°C		0.4	0.53	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −6.7 A	2.0	3.0		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		625		pF
Output Capacitance	C_{oss}			280		pF
Reverse Transfer Capacitance	C_{rss}			105		pF
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = −10 V, I_D = −10 A		24	40	nC
Gate-Source Charge[c]	Q_{gs}			3.4	6.0	nC
Gate-Drain Charge[c]	Q_{gd}			13.5	20	nC
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 5 Ω I_D ≅ −10 A, V_{GEN} = 10 V, R_G = 7.5 Ω		9	60	ns
Rise Time[c]	t_r			50	140	ns
Turn-Off Delay Time[c]	$t_{d(off)}$			60	140	ns
Fall Time[c]	t_f			38	140	ns
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−10	A
Pulsed Current	I_{SM}				−40	A
Diode Forward Voltage[b]	V_{SD}	I_F = 10 A, V_{GS} = 0 V			−2.0	V
Reverse Recovery Time	t_{rr}	I_F = 10 A, di/dt = 100 A/μs		110	250	ns
Reverse Recovery Charge	Q_{rr}			0.4		μC

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
c. Independent of operating temperature.

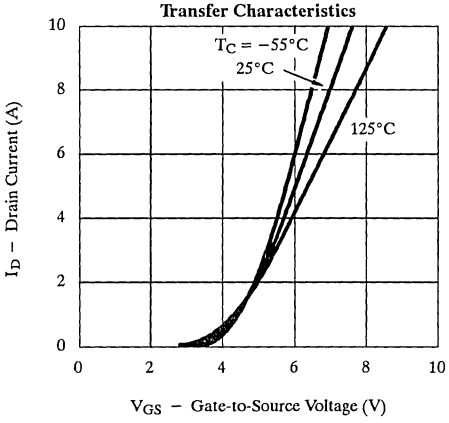
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

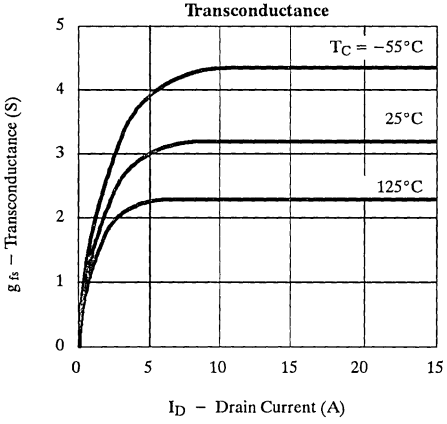
Output Characteristics



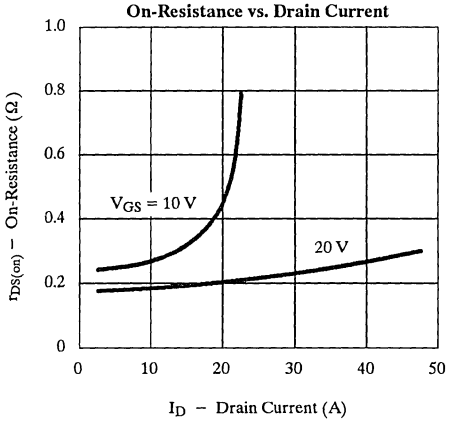
Transfer Characteristics



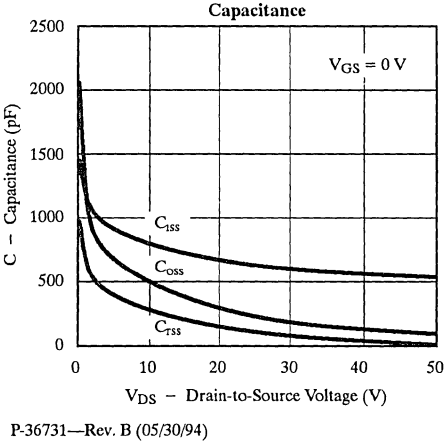
Transconductance



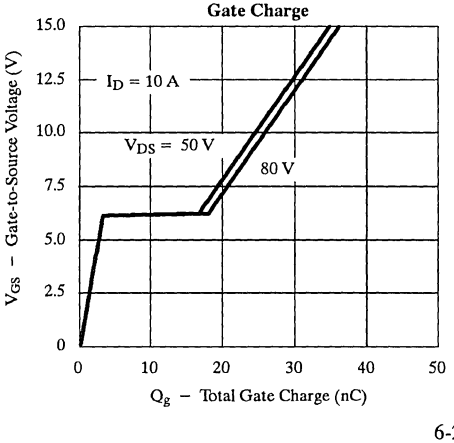
On-Resistance vs. Drain Current



Capacitance



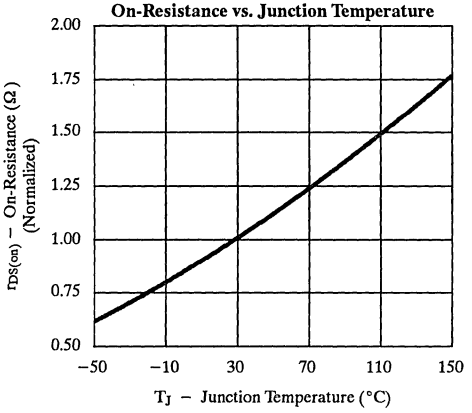
Gate Charge



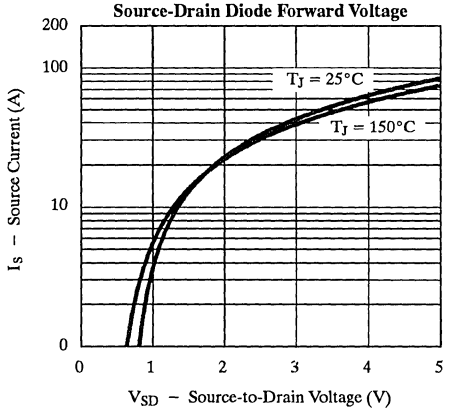
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

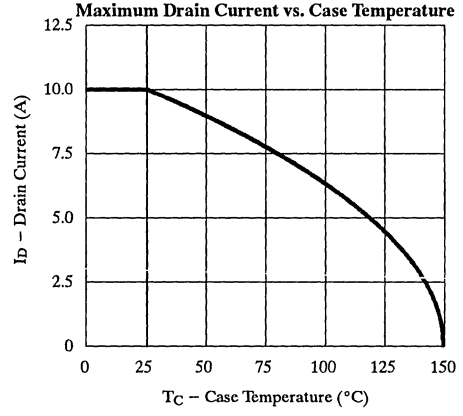


Source-Drain Diode Forward Voltage

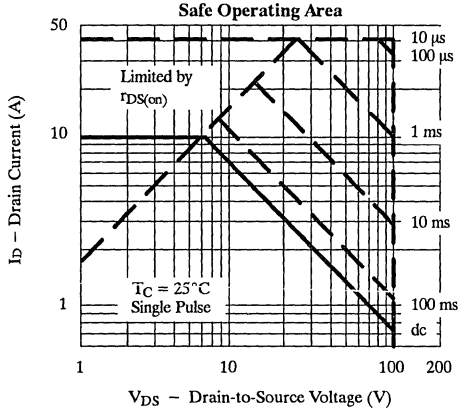


Thermal Ratings

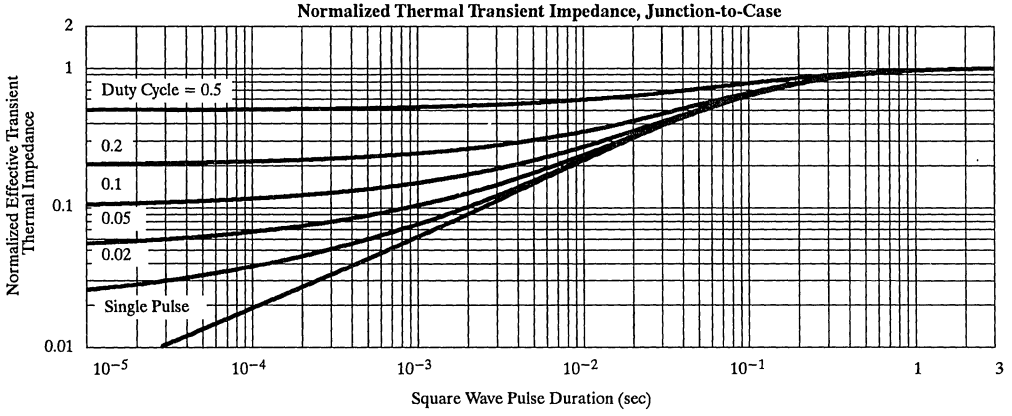
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

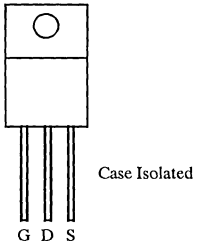
2N7090

P-Channel Enhancement-Mode Transistor

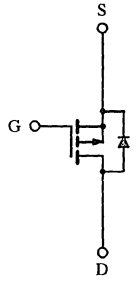
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−200	0.80	−5.7

TO-257AB
Hermetic Package



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−5.7	A
	T_C = 100°C		−3.6	
Pulsed Drain Current		I_{DM}	−23	
Maximum Power Dissipation	T_C = 25°C	P_D	60	W
	T_C = 100°C		25	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		2.0	
Case-to-Sink	R_{thCS}	1.0		

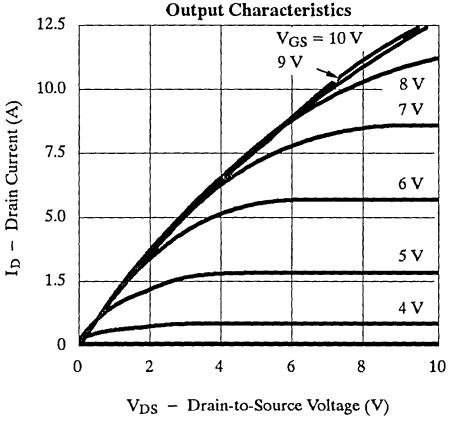
Specifications (T_J = 25°C Unless Otherwise Noted)

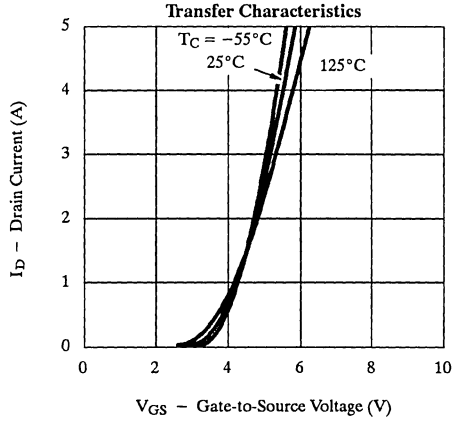
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −160 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −160 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−5.7			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −3.6 A		0.5	0 80	Ω
		V_{GS} = −10 V, I_D = −3.6 A, T_J = 125°C		1.0	1.6	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −3.6 A	2.2	2.7		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		510		pF
Output Capacitance	C_{oss}			180		
Reverse Transfer Capacitance	C_{rss}			75		
Total Gate Charge[c]	Q_g	V_{DS} = −100 V, V_{GS} = −10 V, I_D = −5.7 A		27	35	nC
Gate-Source Charge[c]	Q_{gs}			3.4	6.0	
Gate-Drain Charge[c]	Q_{gd}			15	25	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −100 V, R_L = 17 Ω I_D ≃ −5.7 A, V_{GEN} = −10 V, R_G = 7.5 Ω		9.0	50	ns
Rise Time[c]	t_r			33	100	
Turn-Off Delay Time[c]	$t_{d(off)}$			80	100	
Fall Time[c]	t_f			50	80	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−5.7	A
Pulsed Current	I_{SM}				−23	
Diode Forward Voltage[b]	V_{SD}	I_F = −5.7 A, V_{GS} = 0 V			−2.5	V
Reverse Recovery Time	t_{rr}	I_F = −5.7 A, di/dt = 100 A/µs		160	400	ns
Reverse Recovery Charge	Q_{rr}			1.6		µC

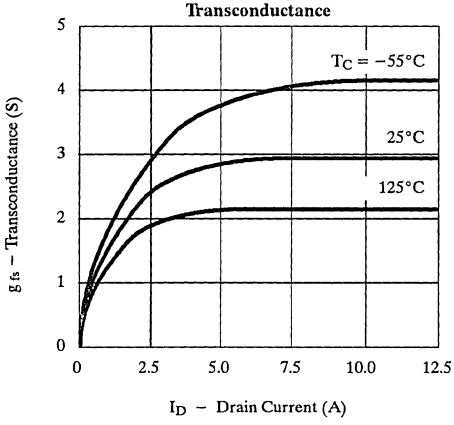
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

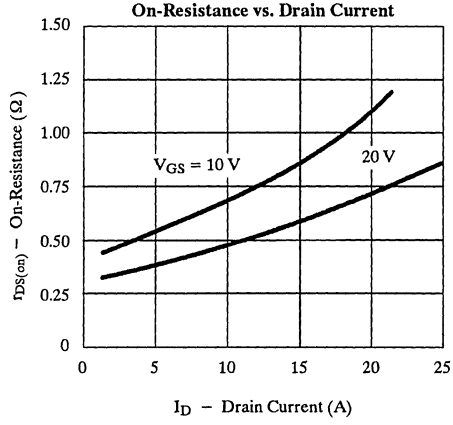
Typical Characteristics (25°C Unless Otherwise Noted)

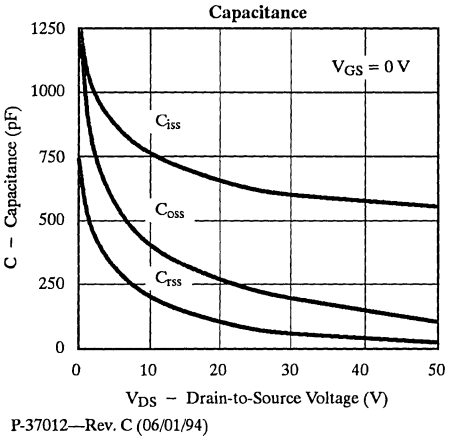
Negative signs omitted for clarity.

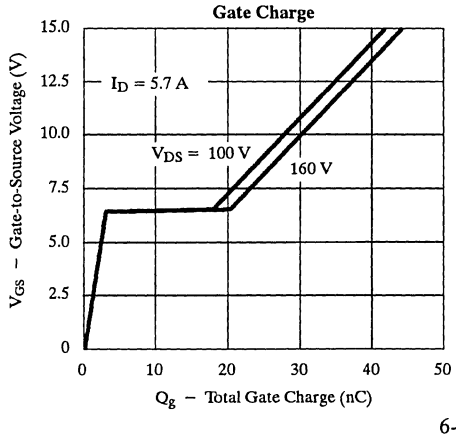






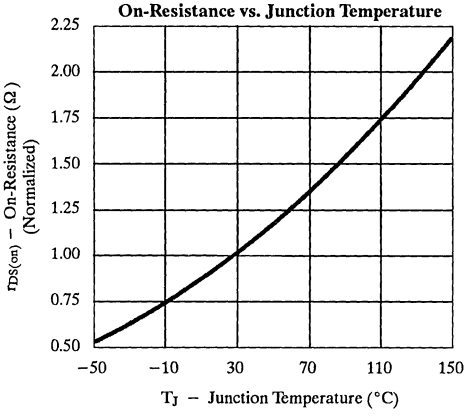


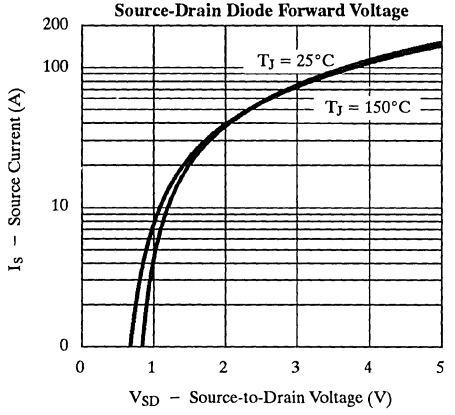




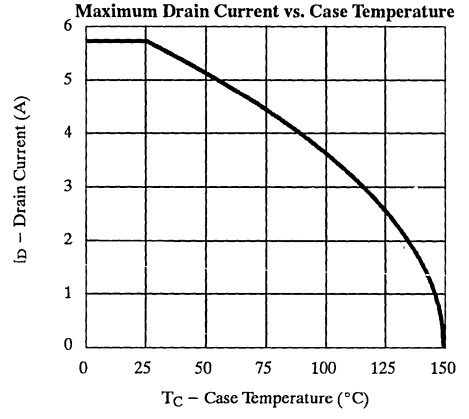
Typical Characteristics (25°C Unless Otherwise Noted)

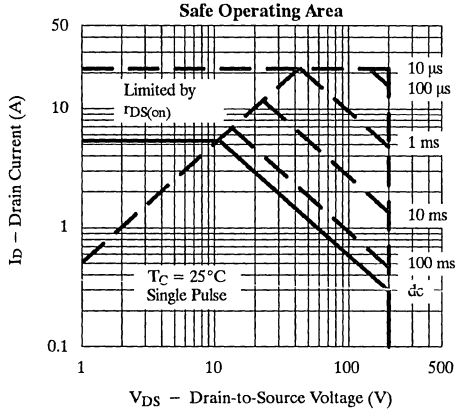
Negative signs omitted for clarity.

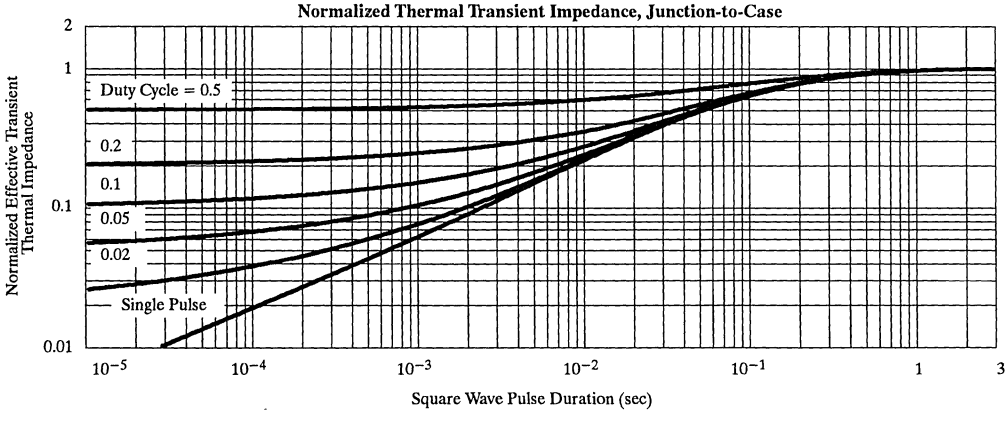




Thermal Ratings







Siliconix

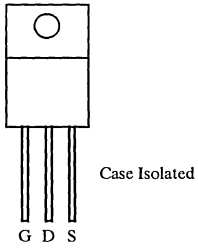
2N7091

P-Channel Enhancement-Mode Transistor

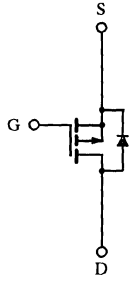
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−100	0.20	−14

TO-257AB
Hermetic Package



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	−100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	−14	A
	T_C = 100°C		−8.7	
Pulsed Drain Current		I_{DM}	−56	
Maximum Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		27	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient	R_{thJA}		80	°C/W
Maximum Junction-to-Case	R_{thJC}		1.8	
Case-to-Sink	R_{thCS}	1.0		

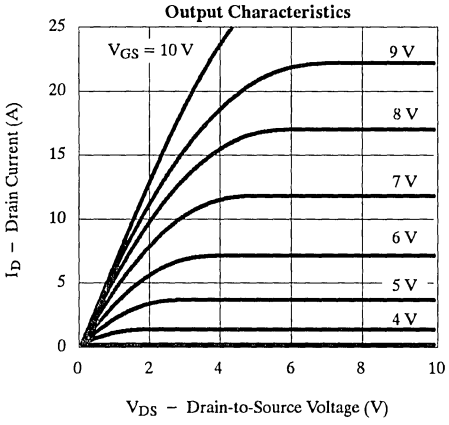
Specifications (T_J = 25°C Unless Otherwise Noted)

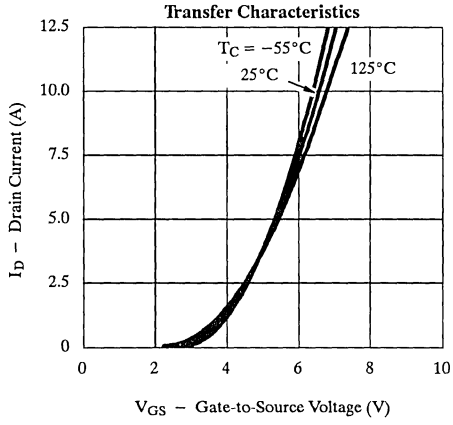
Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 µA	−100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 µA	−2.0		−4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V			−25	µA
		V_{DS} = −80 V, V_{GS} = 0 V, T_J = 125°C			−250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = −10 V, V_{GS} = −10 V	−14			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = −10 V, I_D = −8.7 A		0.15	0.20	Ω
		V_{GS} = −10 V, I_D = −8.7 A, T_J = 125°C		2.3	0.32	
Forward Transconductance[b]	g_{fs}	V_{DS} = −15 V, I_D = −8.7 A	5.0			S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			310		
Total Gate Charge[c]	Q_g	V_{DS} = −50 V, V_{GS} = −10 V, I_D = −14 A		50	62	nC
Gate-Source Charge[c]	Q_{gs}			10	15	
Gate-Drain Charge[c]	Q_{gd}			27	35	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = −50 V, R_L = 3.5 Ω I_D ≅ −14 A, V_{GEN} = −10 V, R_G = 4.7 Ω		10	30	ns
Rise Time[c]	t_r			50	80	
Turn-Off Delay Time[c]	$t_{d(off)}$			40	80	
Fall Time[c]	t_f			40	60	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				−14	A
Pulsed Current	I_{SM}				−56	
Diode Forward Voltage[b]	V_{SD}	I_F = −14 A, V_{GS} = 0 V			−2.0	V
Reverse Recovery Time	t_{rr}	I_F = −14 A, di/dt = 100 A/µs		150	300	ns
Reverse Recovery Charge	Q_{rr}			0.3		µC

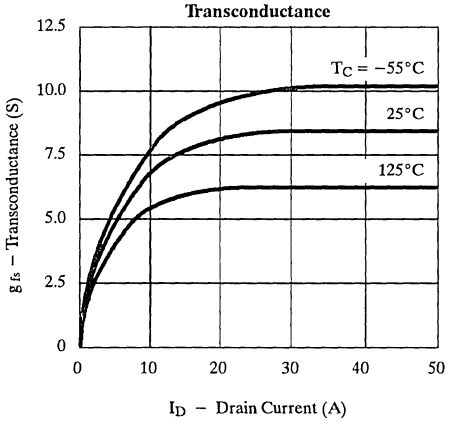
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

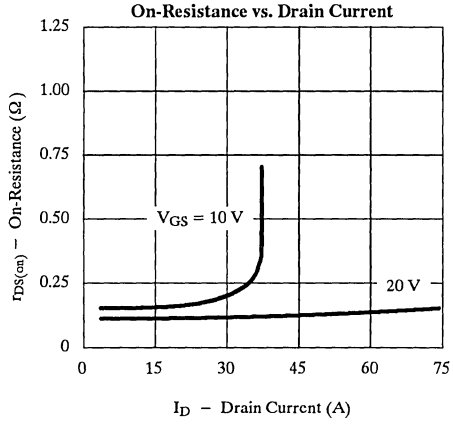
Typical Characteristics (25°C Unless Otherwise Noted)

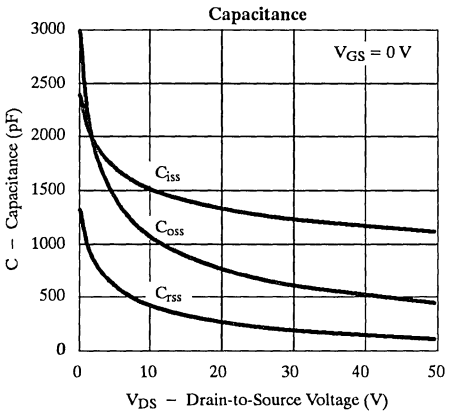
Negative signs omitted for clarity.

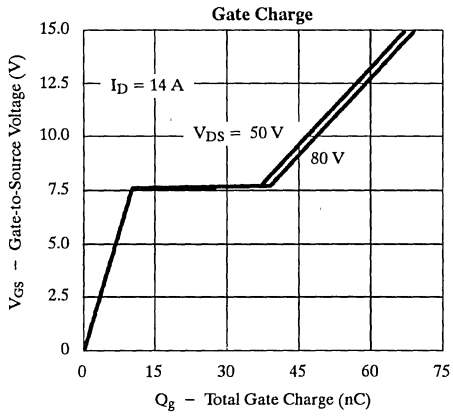








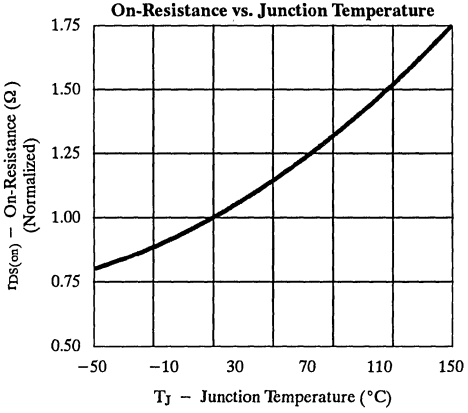




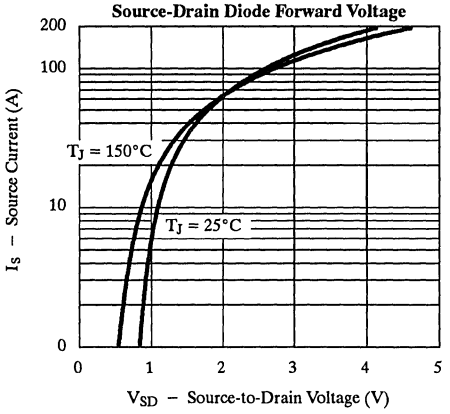
Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.

On-Resistance vs. Junction Temperature

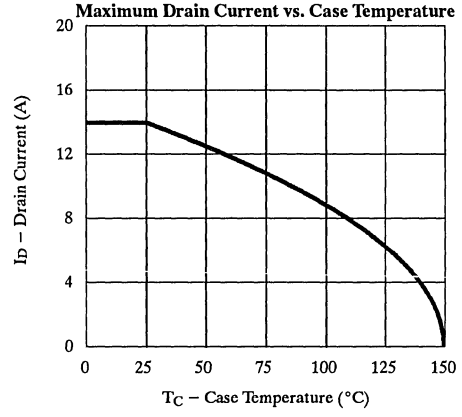


Source-Drain Diode Forward Voltage

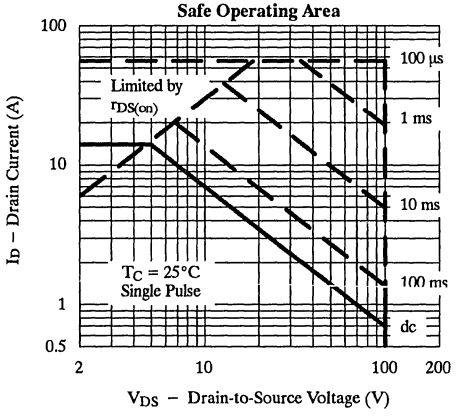


Thermal Ratings

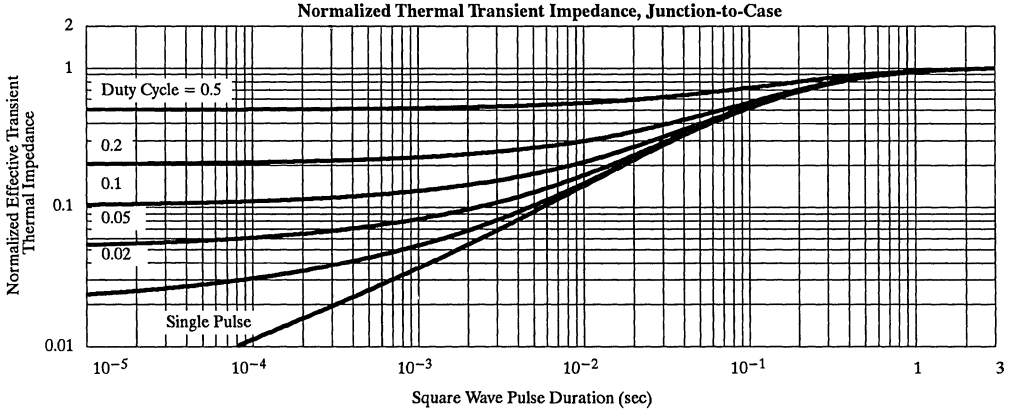
Maximum Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Siliconix

2N7224JANTX/JANTXV

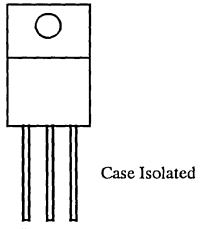
N-Channel Enhancement-Mode Transistors

Product Summary

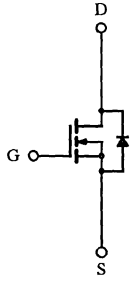
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.081	34

Parametric limits in accordance with MIL-S-19500/592 where applicable.

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	34	A
	T_C = 100°C		21	
Pulsed Drain Current		I_{DM}	136	
Avalanche Current		I_{AR}	34	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	0.83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1000 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA, T_J = −55°C			5.0	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = 25°C	2.0		4.0	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = 125°C	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C			±200	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125°C			1000	µA
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 34 A			0.081	Ω
		V_{GS} = 10 V, I_D = 21 A, T_J = 125°C			0.11	Ω
Dynamic						
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 34 A	50		125	nC
Gate-Source Charge[c]	Q_{gs}		8		22	nC
Gate-Drain Charge[c]	Q_{gd}		15		65	nC
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.47 Ω, I_D ≅ 34 A, V_{GEN} = 10 V, R_G = 2.35 Ω			35	ns
Rise Time[c]	t_r				190	ns
Turn-Off Delay Time[c]	$t_{d(off)}$				170	ns
Fall Time[c]	t_f				130	ns
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				34	A
Pulsed Current	I_{SM}				136	A
Diode Forward Voltage[b]	V_{SD}	I_F = 34 A, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}	I_F = 34 A, di/dt = 100 A/µs			500	ns

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

2N7225JANTX/JANTXV

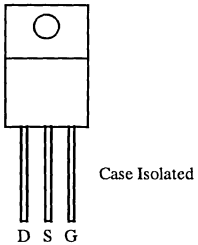
N-Channel Enhancement-Mode Transistors

Product Summary

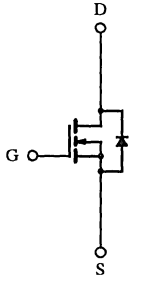
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.105	27.4

Parametric limits in accordance with MIL-S-19500/592 where applicable.

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	27.4	A
	T_C = 100°C		17	
Pulsed Drain Current		I_{DM}	110	
Avalanche Current		I_{AR}	27.4	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	0.83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1000 µA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA, T_J = −55°C			5.0	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = 25°C	2.0		4.0	
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = 125°C	1.0			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C			±200	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			25	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C			250	
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 125°C			1000	
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 27.4 A			0.105	Ω
		V_{GS} = 10 V, I_D = 17 A, T_J = 125°C			0.17	
Dynamic						
Total Gate Charge[c]	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 27.5 A	55		115	nC
Gate-Source Charge[c]	Q_{gs}		8		22	
Gate-Drain Charge[c]	Q_{gd}		30		60	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 3.6 Ω I_D ≅ 27.4 A, V_{GEN} = 10 V, R_G = 2.35 Ω			35	ns
Rise Time[c]	t_r				190	
Turn-Off Delay Time[c]	$t_{d(off)}$				170	
Fall Time[c]	t_f				130	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				27.4	A
Pulsed Current	I_{SM}				110	
Diode Forward Voltage[b]	V_{SD}	I_F = 27.4 A, V_{GS} = 0 V	0.8		1.9	V
Reverse Recovery Time	t_{rr}	I_F = 27.4 A, di/dt = 100 A/µs			950	ns

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

2N7227JANTX/JANTXV

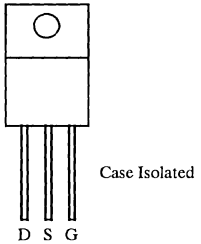
N-Channel Enhancement-Mode Transistors

Product Summary

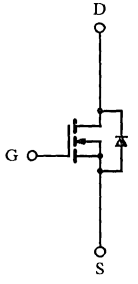
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
400	0.415	14

Parametric limits in accordance with MIL-S-19500/592 where applicable.

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	14	A
	T_C = 100°C		9	
Pulsed Drain Current		I_{DM}	56	
Avalanche Current		I_{AR}	14	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	0.83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1000 μA	400			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA, T_J = −55°C			5.0	V
		V_{DS} = V_{GS}, I_D = 250 μA, T_J = 25°C	2.0		4.0	V
		V_{DS} = V_{GS}, I_D = 250 μA, T_J = 125°C	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C			±200	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V, V_{GS} = 0 V			25	μA
		V_{DS} = 360 V, V_{GS} = 0 V, T_J = 125°C			250	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			1000	μA
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 14 A			0.415	Ω
		V_{GS} = 10 V, I_D = 9 A, T_J = 125°C			0.68	Ω
Dynamic						
Total Gate Charge[c]	Q_g	V_{DS} = 200 V, V_{GS} = 10 V, I_D = 14 A	52		110	nC
Gate-Source Charge[c]	Q_{gs}		5		18	nC
Gate-Drain Charge[c]	Q_{gd}		25		65	nC
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 200 V, R_L = 14.2 Ω I_D ≅ 14 A, V_{GEN} = 10 V, R_G = 2.35 Ω			35	ns
Rise Time[c]	t_r				190	ns
Turn-Off Delay Time[c]	$t_{d(off)}$				170	ns
Fall Time[c]	t_f				130	ns
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				14	A
Pulsed Current	I_{SM}				56	A
Diode Forward Voltage[b]	V_{SD}	I_F = 14 A, V_{GS} = 0 V			1.7	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, di/dt = 100 A/μs			1200	ns

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Siliconix

2N7228JANTX/JANTXV

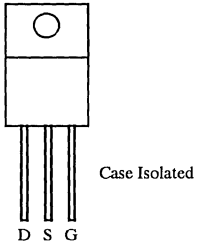
N-Channel Enhancement-Mode Transistors

Product Summary

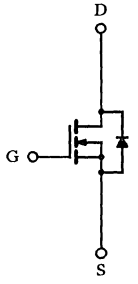
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
500	0.515	12

Parametric limits in accordance with MIL-S-19500/592 where applicable.

TO-254AA
Hermetic Package



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	12	A
	T_C = 100°C		8	
Pulsed Drain Current		I_{DM}	48	
Avalanche Current		I_{AR}	12	
Maximum Power Dissipation	T_C = 25°C	P_D	150	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	0.83	°C/W

Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit Min	Limit Typ[a]	Limit Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1000 µA	500			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA, T_J = −55°C			5.0	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = 25°C	2.0		4.0	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = 125°C	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C			±200	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V			25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			250	µA
		V_{DS} = 500 V, V_{GS} = 0 V, T_J = 125°C			1000	µA
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 12 A			0.515	Ω
		V_{GS} = 10 V, I_D = 8 A, T_J = 125°C			0.9	Ω
Dynamic						
Total Gate Charge[c]	Q_g	V_{DS} = 250 V, V_{GS} = 10 V, I_D = 12 A	55		120	nC
Gate-Source Charge[c]	Q_{gs}		5		19	nC
Gate-Drain Charge[c]	Q_{gd}		27		70	nC
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 20.8 Ω I_D ≅ 12 A, V_{GEN} = 10 V, R_G = 2.35 Ω			35	ns
Rise Time[c]	t_r				190	ns
Turn-Off Delay Time[c]	$t_{d(off)}$				170	ns
Fall Time[c]	t_f				130	ns
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				12	A
Pulsed Current	I_{SM}				48	A
Diode Forward Voltage[b]	V_{SD}	I_F = 12 A, V_{GS} = 0 V			1.7	V
Reverse Recovery Time	t_{rr}	I_F = 12 A, di/dt = 100 A/µs			1600	ns

Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Appendix 7

FREE INFO 24 HOURS A DAY 365 DAYS A YEAR

Siliconix Faxback 408-970-5600

With Siliconix Faxback, all it takes is a touch-tone phone plus a few simple commands. Data sheets and application notes on our power ICs, LITTLE FOOT® power transistors, analog switches, analog multiplexers, and low-power transistors will be sent to your fax machine – instantly!

How It Works

If you're calling for the first time, please follow these easy steps.

From a Touch-Tone Phone, Just Dial 408-970-5600

Siliconix Faxback will answer and lead you through a series of easy-to-understand automated voice prompts.

Order A Directory

Soon after calling, you will be asked whether you want to order a directory. Please order any or all of the directories listed below. A directory describes the available documents and gives you the Faxback order numbers for those documents.

- **Power Products Data Sheet Directory**

  Includes power transistors and integrated circuits for use in computers, automobiles, telecom systems, and a host of other applications. Data sheets and SPICE models are available for all LITTLE FOOT products, the industry's largest family of small-outline, surface-mount power MOSFETs for motion control and load management.

- **Analog ICs Data Sheet Directory**

  Includes analog switches and multiplexers used to route signals in video, multimedia, instrumentation, and test equipment in both the industrial and hi-rel environments.

- **Low-Power Discretes Data Sheet Directory**

  Includes JFETs, DMOS switches, low-power MOS transistors, low-leakage pico-amp diodes, voltage controlled resistors, and current regulator diodes, packaged for both the industrial and hi-rel environments.

- **Application Note Directory**

  Includes application notes for power products, analog ICs, and small-signal transistors.

Faxback Information

DEF 3

Enter Your Fax Number

When you're through ordering, Siliconix Faxback will ask you for the fax number of the machine you want your directories sent to. Just type in the area code and phone number on your touch-tone phone. If you are sending the information to a fax machine outside of North America, make sure you dial "011" first.

GHI 4

Identify Your Fax

Faxback lets you choose how your documents will be addressed. You can enter your name or your voice phone number. When the fax arrives at your selected destination, it will have your name or voice number on the cover sheet to identify it.

JKL 5

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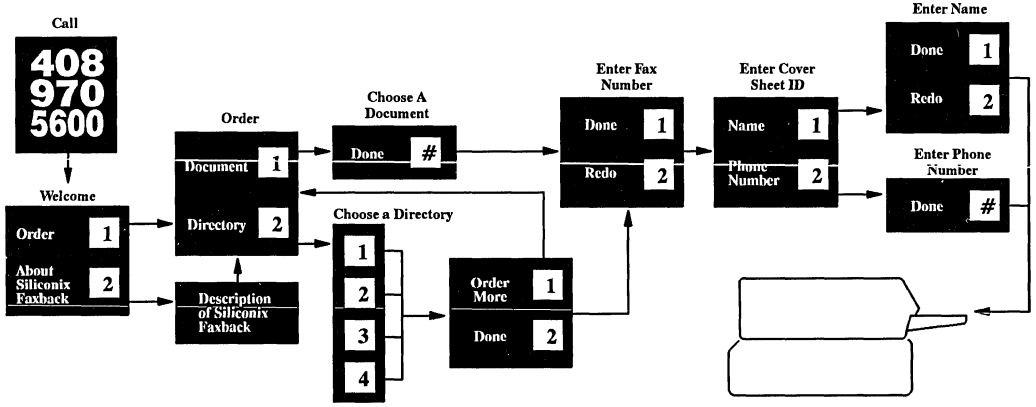
The information you ordered will be sent immediately. It's as easy as 1 + 2 = 3!

Once you have received and reviewed your directories, just call back and enter the Siliconix Faxback numbers of the data sheets and application notes you want.

In most cases, you will receive your documents within 5-10 minutes. If for some reason your fax machine is in use when Faxback is ready to send your documents, Faxback will automatically call back – up to three times (at two minute intervals) – until it reaches your fax machine. If after the third call your machine is still in use, you will have to call back and order your documents again.



Entering Your Name

In addition, you can use your touch-tone phone to spell out your name. Just follow this simple system. The documents you request will be sent with a cover sheet bearing your name. Or you can choose simply to have documents addressed to your direct phone number.

To enter a letter, press its key 1, 2, or 3 times: 2 enters **A**; 2 2 enters **B**; 2 2 2 enters **C**.

Special characters: 1 1 – **Q**; 1 1 1 – **Z**; # # – **SPACE**.

To back up and correct a letter, press: * . To end, press: # . For complete instructions, press: 0 .

Applications Information

The following literature is designed to help you use Siliconix products in your applications. Call our FaxBack system (408-970-5600) to have the document sent to you immediately via facsimile, or to order a copy to be sent by mail, call 800-554-5565.

Application Notes for Siliconix Power Products Products

Application Note Number	FaxBack Code Number	Description
LITTLE FOOT® MOSFETs		
AN801	8801	**Designing with Complementary Power MOSFETs in Surface-Mount (SO-8) Packages** The LITTLE FOOT complementary n- and p-channel Si9942DY can be used to drive inductive loads such as motors, solenoids, and relays directly, or it may be used as a low-impedance buffer to drive larger power MOSFETs or capacitive loads. In 12-V battery-powered applications, the Si9942DY allows a substantial increase in motor size without the need for additional heatsinking.
AN802	8802	**Low-Voltage Motor Drive Designs Using N-Channel Dual MOSFETS in Surface-Mount Packages** Dual n-channel LITTLE FOOT devices offer on-resistance advantages which extend the power range of surface-mount power devices. With the selection of a high-side gate drive circuit that complements an application's needs, an n-channel half-bridge can provide a surface-mount option that is economical and reliable.
AN803	8803	**Thermal Characteristics of Siliconix's LITTLE FOOT Family of Surface-Mount MOSFETs** Siliconix' LITTLE FOOT family of surface-mount power MOSFETs provides improved thermal transfer characteristics, high current handling capability, and lower on-resistance compared with DPAK and SOT packages. The copper lead frames designed for the LITTLE FOOT family maximize heat transfer to the PC board Combined with Siliconix' high-density transistor technologies, the result is a significantly extended range for surface-mount devices in power applications.
LITE FOOT™ MOSFETs		
AN1001	8501	**LITE FOOT, The Next Step in Surface-Mount Power MOSFETs** LITE FOOT is the first family of power MOSFETs combining high-density n- and p-channel technologies with TSSOP packaging. With a 1.1 mm profile, LITE FOOT devices are small enough to fit into any standard PCMCIA card. They provide an equally compact solution for load switching in small form-factor disk drives, cellular telephones, notebook computers, PDAs, and other applications where space and battery life is at a premium.
Power MOSFETs		
AN601	8601	**Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments** This application note reviews the history of unclamped inductive switching (UIS) and examines various theories pertaining to failure. It further identifies what appears to be two releated mechanisms -- thermal and bipolar -- believed to be responsible for failure during UIS and concludes by recommending how a power MOSFET should be qualified for ruggedness in the data sheet.
Power ICs		
AN701	8701	**Designing High-Frequency DC-to-DC Converters with the Si9114 Switchmode Controller** The Si9114 controller enables high-frequency power conversion by reducing delay times and adding additional features over previous generation products. As a result, dc-to-dc converters can be designed for frequencies up to 1 MHz with simple PWM topologies instead of the complex resonant ones. High-frequency designs with the Si9114 will enable designers to reduce the size of energy storage components, increase reliability by using ceramic capacitors, and simplify the implementation of a distributed power architecture.
AN702	8702	**Efficient ISDN Power Converters Using the Si9100** The Si9100 power IC facilitates compliance with ISDN design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested with measured efficiency greater than 80% for a wide range of loads.

Application Notes for Siliconix Power Products Products (Cont'd)

Application Note Number	FaxBack Code Number	Description
Power ICs (Cont'd)		
AN703	8703	**Designing DC/DC Converters with the Si9110 Switchmode Controller** Si9110 is the first BiC/DMOS switchmode controller IC to provide switching frequencies in the 100- to 500-kHz range while keeping current limit delay time under approximately 100 ns. To illustrate the Si9110's capabilities, a 15-W forward converter is presented, providing 5-V and 12-V outputs from a 9- to 36-V input range.
AN704	8704	**Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals** This application note specifically addresses design issues relating to emergency-designated ISDN terminals and presents design details for a dc-to-dc converter which conforms to the international standard.
AN705	8705	**The Si9910 Adaptive Power MOSFET Driver Improves Performance in High-Voltage Half-Bridge Applications** The Si9910DY introduces a new generation of "adaptive" power MOSFET gate drivers that use active feedback to protect the power MOSFET, while allowing logic-level control of high-voltage signals. When all of its protective options are enabled, the Si9910DY is capable of controlling the power MOSFET dv/dt, maximum peak current, minimum gate-drive voltage, and maximum source-drain voltage drop.
AN706	8706	**Motor Drive Circuits Using the D469A** The D469A contains four independent drive channels, and each channel can be configured as a logically inverting or non-inverting driver. Since the D469A is a CMOS device, it is compatible with low-power CMOS logic and microprocessors and draws minimal quiescent current. In motor drive applications, the D469A provides optimized gate drive signals and simplifies interface to the logic level control circuitry.
AN707	8707	**Designing Low-Power Off-Line Flyback Converters Using the Si9120 Switchmode Controller IC** The Si9120 was designed to get high efficiency from low-power off-line power supplies. This current-mode control PWM IC reduces typical quiescent power requirements to 0.85 mA while driving a 500-pF load at 50 kHz. The chip contains MOS capacitors for the clock circuit, so the only external timing component required is a resistor to set the operating frequency.
AN708	8708	**Low-Power Universal-Input Power Supply Achieves High Efficiency** A flyback circuit using the Si9120 PWM controller demonstrates that designing universal-input supplies can be a simple task. Good regulation is achieved while maintaining the 3750-V ac input-to-output isolation mandated by VDE. The Si9120 eliminates the need for external start-up circuitry, and its foldback current limiting requires no feedback across the isolation boundary.
AN709	8709	**Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs** The combination of the Si9976DY and a LITTLE FOOT MOSFET rated between 2 and 5 A creates a powerful and flexible solution for power switching in dc motor drives in 20- to 40-V systems.
AN710	8710	**High-Efficiency Buck Converter for Notebook Computers** This application note presents a dc-to-dc converter consisting of the Si9150CY BiCMOS controller IC and LITTLE FOOT low-voltage MOSFETs. In notebook computers and other portable products, the converter achieves a maximum efficiency of 94% while producing 400 mA at 3.3 V with input voltage of 6 V. The low losses of this efficient buck converter eliminate the need for heavy heat sinks and device packaging, and makes energy that is normally consumed by the power converter available for the application.
AN712	8712	**A High-Voltage Half-Bridge Using the Si9901 with the Si9911 or Si9914** The Si9901 can be used with the Si9911 or Si9914 MOSFET drivers as a two-package approach to half-bridges for applications in systems with operating voltages up to 500 V_{DC}. The resulting chip set provides the best available electrical isolation between the low and high sides, enhances noise immunity in level shifting circuitry, and allows the use of cost-effective manufacturing processes.
AN713	8713	**A 1-Watt Flyback Converter Using the Si9100** Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduction in parts count decreases system cost, improves reliability, and simplifies circuit design in feature phones and ISDN terminals.
AN714	8714	**A Compact Controller for Brushless DC Motors** The Si9979 is a monolithic controller with integral high-side drive circuitry, allowing easy implementation of an all-n-channel three-phase bridge. An internal voltage regulator allows the Si9979 to operate over a wide input voltage range, 20 to 40 V DC, and to power commutation sensors over this same range. Housed in a 7 mm SQFP package, the Si9979 reduces assembly cost and simplifies both motor and electronics packaging.

Introduction

Reliability at Siliconix is ensured with two primary programs: the Reliability Qualification Program and the Reliability Monitoring Program. Siliconix publishes this data by product family and it can be obtained by request through your local sales office.

Qualification Program

Qualification programs of accelerated stress testing are developed for the introduction of new devices (die qualifications), packages, major process changes, new materials or suppliers, new manufacturing equipment, and new manufacturing locations.

A qualification starts after a qualification test plan is developed. This plan specifies the following:

- Purpose and scope
- Device or geometry types and packages being qualified
- Process and assembly specs involved
- Test vehicles and location
- Tests and stresses
- Duration of each stress
- Sample sizes
- Acceptance criteria
- Number of lots required

Monitoring Program

The Reliability Monitoring Program, which includes accelerated life tests, is designed to continuously monitor product reliability. The program furnishes up-to-date failure-rate and failure-mechanism data which can be used to predict and improve long-term reliability performance. The Monitoring Program covers a wide range of technologies and product lines manufactured by Siliconix. In order to accomplish this, products are grouped by similar technologies. For example, components built in the same wafer fab, using the same manufacturing processes, having similar complexity, functionality, and package types are grouped into a technology family. One component or more representing each technology group is monitored according to a quarterly schedule.

The short-term and long-term monitor tests are outlined in Tables 1 and 2. Also, the Reliability Monitor Program is summarized in general outline form as a flow chart in Figure 1 and with operating life data in Table 3.

Accelerated Reliability

Accelerated tests were developed to shorten the time required for reliability testing. The life cycle of a component is accelerated by applying stress that is more severe than that encountered under normal operating conditions. This acceleration is produced by elevating temperatures, increasing humidity or pressure, alternating hot and cold temperature, switching power on and off, or some combination of these conditions. The test results are used to predict normal operating performance. In the sections below we present a brief description of each stress.

Summary of Tests

High-Temperature Reverse-Bias (HTRB) Test

The HTRB accelerated test is performed under reverse biasing at an elevated temperature of 150°C or 175°C with the drain-to-source junction reversed biased to 80% of BV_{DSS}. According to the reliability monitor specification, devices are to be tested at 168 hours (providing a fast reaction and infant mortality indication) and at the end point of 1000 hours. Reliability failure rates (expressed in FITs—*Failures In Time*) are then calculated from the long-term results. The reverse-biased test condition checks the integrity of the field termination and the quality of the body-drain junction. This test also detects surface states, especially in the termination area.

High-Temperature Gate-Bias (HTGB) Test

The HTGB accelerated test is performed with the gate biased to 80% of the gate-to-source voltage rating and at an elevated temperature of 150°C or 175°C. Test points are the same as for the HTRB stress. Biasing of the gate accelerates failures due to oxide defects or the presence of mobile ions. The long-term results are used in the prediction of reliability failures.

Temperature Cycling Test

Temperature cycling exploits the differences in thermal coefficients of expansion between silicon and the other materials used in die fabrication and packaging. Each cycle consists of 10-minute exposures (−60°C for MOSPOWER Discretes, −65°C for Power ICs) and 150°C with a 1-minute transfer at room temperature between the temperature extremes. This test reveals potential weaknesses in die and package materials and construction and in the integration of the die and package.

Thermal Shock Test

The purpose of the thermal shock test is similar to that of temperature cycling. This stress is more extreme, however, due to the fact that the ambient medium is liquid and not air, and the transition time is much shorter than for temperature cycling.

Each cycle consists of a 5-minute exposure at −60°C or −65° and 150°C with a maximum 10-second transfer time between the temperature extremes.

Bias Humidity Test

The bias humidity test is used to test plastic packaged devices for the effects of moisture penetration while electrical potentials are applied. The components are placed in a biased condition and then are subjected for 1000 hours to a temperature of 85°C and a relative humidity 85%. This test confirms package integrity.

Pressure Pot Test

In the pressure pot test, water vapor is forced into non-hermetic packages via micro gaps in the package-lead seal. Water is then carried to the die surface via capillary action of the bond wires. Electrical leakage may result. External contamination of the package or lead finish may be transported to the die or may directly cause corrosion of the leads.

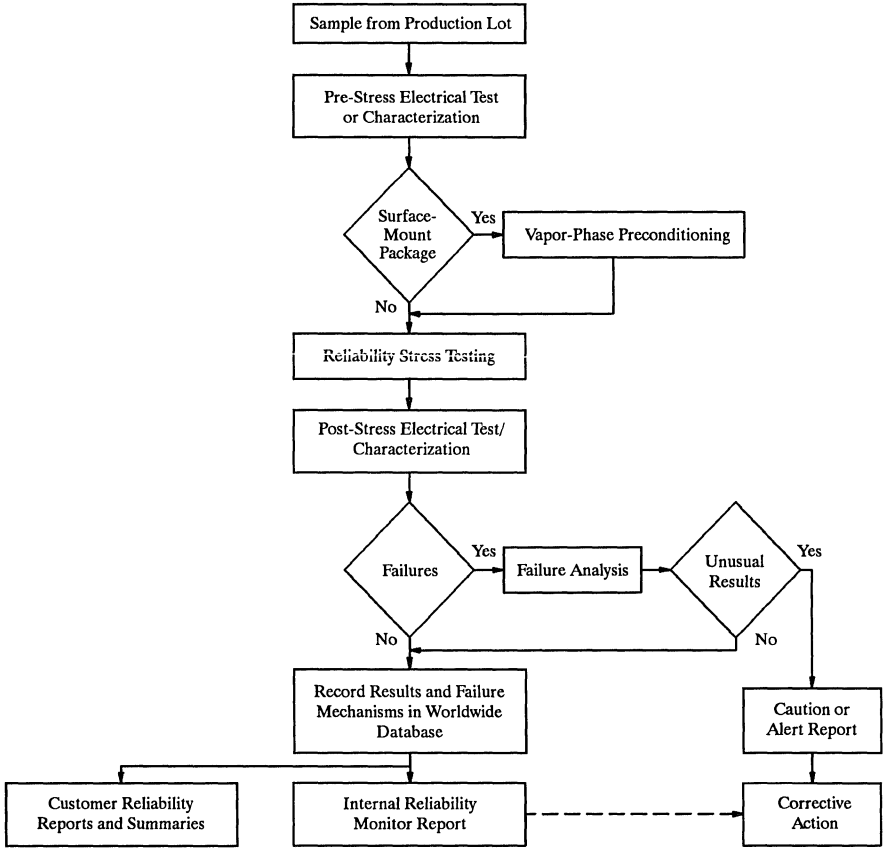


Figure 1. Reliability Monitor Flow (Short- and Long-Term Monitors)

MOSPOWER Discretes

Table 1. Short-Term Reliability Monitor for MOSPOWER Discretes

Test	Condition	Sample Size	Test Points
HTGB	150°C or 175°C	50	168 hours
HTRB			
Pressure Pot	121°C, 15 PSIG		96 hours (Plastic)
Thermal Shock	Liquid to liquid. −65°C to 150°C		100 cycles
Solderability	MIL-STD-883D, M2003	15 leads	(245°C ±5°C)
Lead Integrity	MIL-STD-883D, M2004		
Marking Permanency	MIL-STD-883D, M2015	16	
Salt Atmosphere	MIL-STD-883D, M1009	15	24 hours (Hermetic)

Table 2. Long-Term Reliability Monitor

Test	Condition	Sample Size	Test Points
HTGB	150°C or 175°C	50	0, 168, 1000 hours
HTRB			
Biased Humidity (Plastic)	85°C, 85% relative humidity		0, 500, 1000 hours
Temperature Cycling	Air-to-air −65°C to 150°C		0, 250, 1000 cycles
Power Cycling	$\Delta T_J = 100°C$	30	0, 2000, 6000 cycles

Table 3. Operating Life Data

High Temperature Operating Life Technology	Number of Units	Equivalent Device Hours at 55°C and 0.6 eV	FITs[a]	
			0.6 eV	1.0 eV
Power MOS	24,786	2,649,447,243	0.3	0.01

Note:
a. 1 failure per billion device hours

Power IC's

Table 1. Short-Term Reliability Monitor for Power IC's

Test	Condition	Sample Size	Test Points
Static Operating Life	150°C	50	168 hours
Dynamic Operating Life			
Pressure Pot	121°C, 15 PSIG		96 hours (Plastic)
Thermal Shock	Liquid to liquid. −60°C to 150°C		100 cycles
Solderability	MIL-STD-883D, M2003	15 leads	(245°C ±5°C)
Lead Integrity	MIL-STD-883D, M2004		
Lid Torque	MIL-STD-883D, M2024		(Hermetic)
Marking Permanency	MIL-STD-883D, M2015	16	
Salt Atmosphere	MIL-STD-883D, M1009	15	24 hours (Hermetic)

Table 2. Long-Term Reliability Monitor

Test	Condition	Sample Size	Test Points
Static Operating Life	150°C	50	0, 168, 1000 hours
Dynamic Operating Life			
Biased Humidity (Plastic)	85°C, 85% relative humidity		0, 500, 1000 hours
Temperature Cycling	Air-to-air −60°C to 150°C		0, 250, 1000 cycles

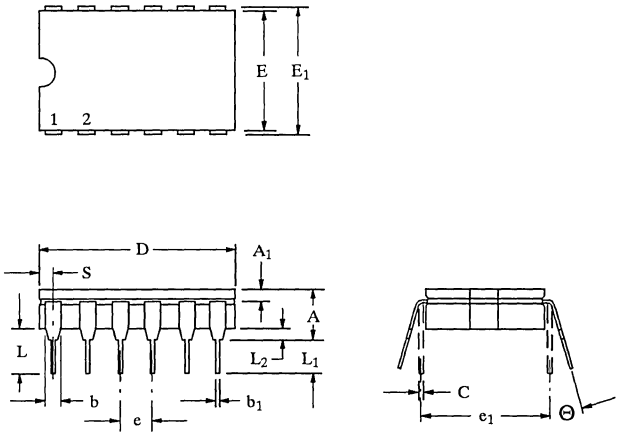
Table 3. Operating Life Data

High Temperature Operating Life Technology	Number of Units	Equivalent Device Hours at 55°C and 0.6 eV	FITs[a]	
			0.6 eV	1.0 eV
Power IC	2,097	4,618,752,555	7.2	0.35

Note:
a. 1 failure per billion device hours

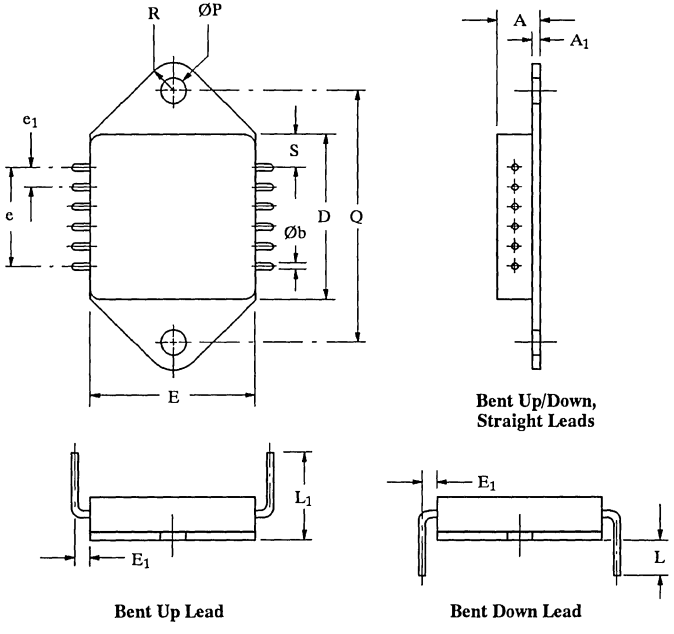
Package Information

Ceramic DIP, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	1.27	2.16	0.050	0.085
b	1.14	1.65	0.045	0.065
b_1	0.38	0.51	0.015	0.020
C	0.20	0.30	0.008	0.012
D–8	9.40	10.16	0.370	0.400
D–14	19.05	19.56	0.750	0.770
D–16	19.05	19.56	0.750	0.770
E	6.60	7.62	0.260	0.300
E_1	7.62	8.26	0.300	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3 81	5.08	0.150	0.200
L_1	3.18	3.81	0.125	0.150
L_2	0.51	1.14	0.020	0.045
S–8	0.64	1.52	0.025	0.060
S–14	1.65	2.41	0.065	0.095
S–16	0.38	1.14	0.015	0.045
Θ	0°	15°	0°	15°

Hermetic Power Module



Bent Up/Down, Straight Leads

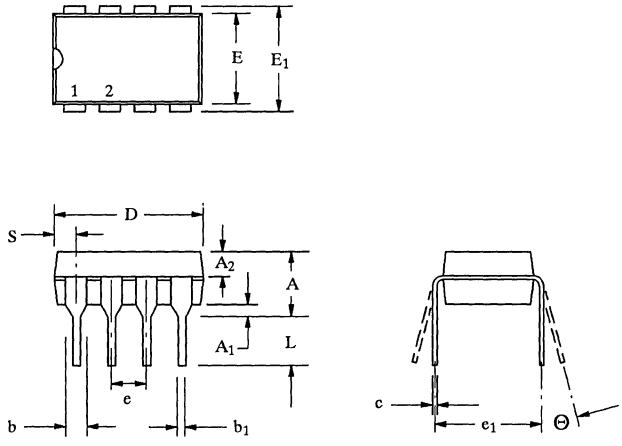
Bent Up Lead

Bent Down Lead

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	6.10	7.11	0.240	0.280
A_1	1.14	1.40	0.045	0.055
Øb	0.89	1.14	0.035	0.045
D	24.89	25.91	0.980	1.020
E	24.89	25.91	0.980	1.020
E_1	2.79	3.30	0.110	0.130
e	15.62	16.13	0.615	0.635
e_1	2.92	3.43	0.115	0.135
L	4.44	6.35	0.175	0.250
L_1	12.32	–	0.485	–
ØP	3.84	4.09	0.151	0.161
Q	38.35	38.86	1.510	0.161
R	4.19	4.44	0.165	0.175
S	4.57	4.95	0.180	0.195

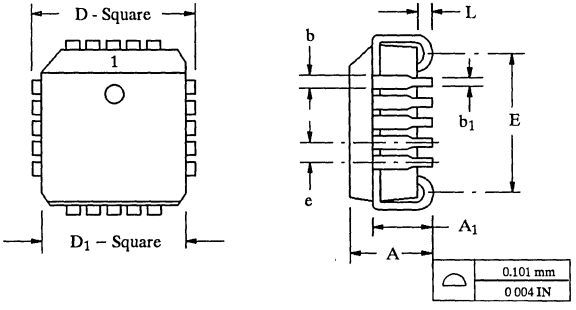
Package Information

■ Plastic DIP, 8- to 20-Pin



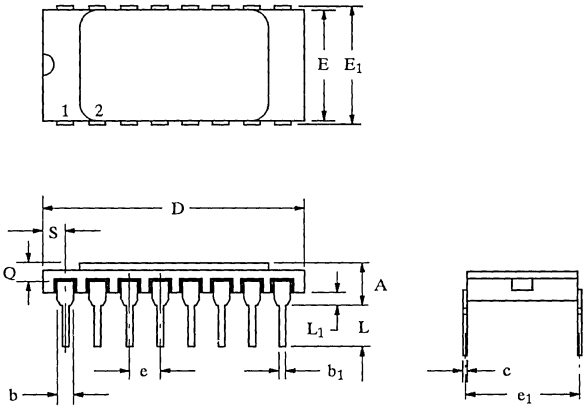
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D–8	9.65	11.68	0.380	0.460
D–14	17.27	19.30	0.680	0.760
D–16	18.93	21.33	0.745	0.840
D–20	24.89	26.92	0.980	1.060
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S–8	1.02	2.03	0.040	0.080
S–14	1.02	2.03	0.040	0.080
S–16	0.38	1.52	0.015	0.060
S–20	1.02	2.03	0.040	0.080
Θ	0°	15°	0°	15°

■ PLCC Package, 20-Pin



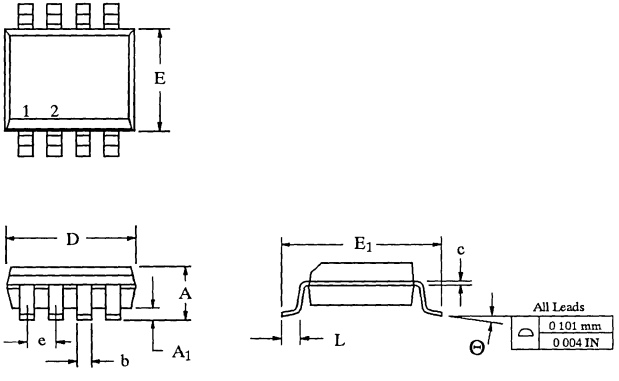
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.33	0.55	0.013	0.021
D	9.78	10.03	0.385	0.395
D_1	8.89	9.04	0.350	0.356
E	7.37	8.38	0.290	0.330
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

Sidebraze DIP, 14- to 24-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.44	0.105	0.175
b	0.97	1.52	0.038	0.060
b_1	0.38	0.53	0.015	0.021
c	0.20	0.30	0.008	0.012
D–14	17.53	19.55	0.690	0.770
D–16	19.56	21.08	0.770	0.830
D–20	24.89	26.16	0.890	1.030
D–24	29.97	31.24	1.180	1.230
E	7.12	7.87	0.280	0.310
E_1	7.37	8.25	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
L_1	0.64	1.39	0.025	0.055
Q	0.25	–	0.010	–
S–14	0.77	2.41	0.030	0.095
S–16	0.51	1.65	0.020	0.065
S–20	0.77	1.65	0.030	0.065
S–24	0.77	2.41	0.030	0.095

SO Package, 8- to 16-Pin

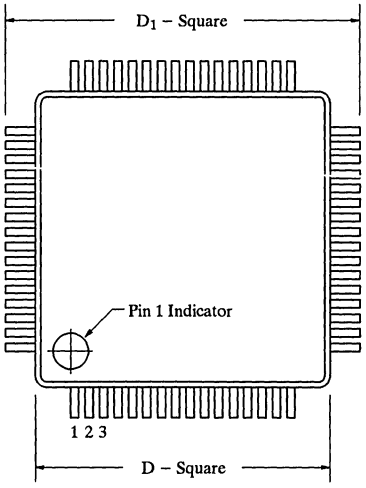


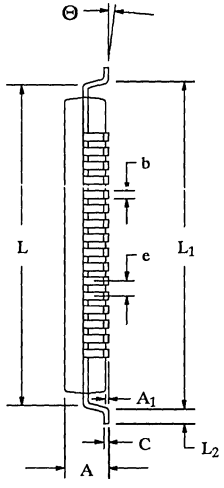
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
E_1	5.70	6.30	0.224	0.248
e	1.27 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

L	0.13	0.25	0.005	0.010
S	0.44	0.55	0.017	0.022
Θ	0°	8°	0°	8°

Package Information

■ SQFP, 48- to 64-Pin

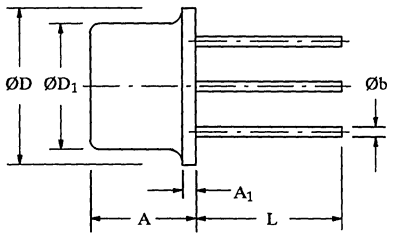


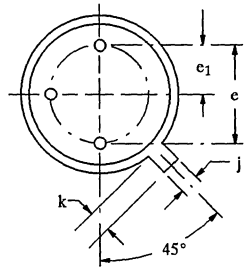


Dim	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.60	0.053	0.063
A_1	0.04	0.16	0.002	0.006
b	0.14	0.26	0.006	0.010
C	0.117	0.177	0.005	0 007
D-48	6.90	7.10	0.272	0.280
D-64	9.90	10.10	0.390	0.398
D_1-48	8.70	9.30	0.343	0.366
D_1-64	11.7	12.3	0.461	0.484
e	0.40	0.60	0.016	0.024
L-48	–	7.80	–	0.307
L-64	–	10.80	–	0.425
L_1-48	7.80	8.20	0.307	0.323
L_1-64	10.80	11.20	0.425	0.441
L_2	0.30	0.70	0.012	0.028
Θ	0°	7°	0°	7°

*For Reference Only

■TO-205AD/AF (TO-39)

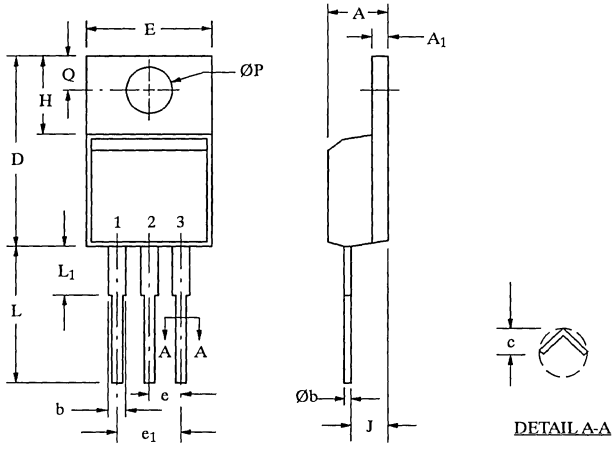




Dim	Millimeters		Inches	
	Min	Max	Min	Max
A-AD	6.10	6.60	0.240	0.260
A-AF	4.07	4.57	0.160	0.180
A_1	0.23	1.04	0.009	0.041
Øb	0.41	0.53	0.016	0.021
ØD-AD	8.51	9.39	0.335	0.370
ØD-AF	8.64	9.39	0.340	0.370
$ØD_1$-AD	7.75	8.51	0.305	0.335
$ØD_1$-AF	8.01	8.64	0.315	0.340
e	5.08 BSC		0.200 BSC	
e_1	2.54 BSC		0.100 BSC	
j	0.72	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	19.05	0.500	0.750

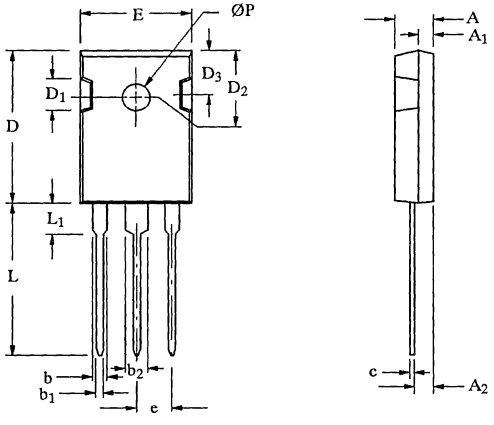
Package Information

TO-220AB



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.32	4.70	0.170	0.185
A_1	1.14	1.40	0.045	0.055
b	1.27	1.65	0.050	0.065
Øb	0.76	1.02	0.030	0.040
c	0.38	0.76	0.015	0.030
D	14.60	15.49	0.575	0.610
E	10.03	10.41	0.395	0.410
e	2.41	2.67	0.095	0.105
e_1	4.95	5.33	0.195	0.210
H	5.97	6.73	0.235	0.265
J	2.41	2.79	0.095	0.110
L	13.08	14.22	0.515	0.560
L_1	–	3.81	–	0.150
ØP	3.68	3.94	0.145	0.155
Q	2.54	3.05	0.100	0.120

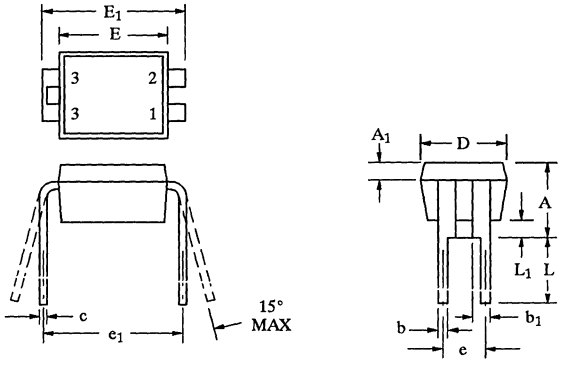
TO-247AD



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.70	5.30	0.185	0.209
A_1	1.50	2.50	0.059	0.098
A_2	2.20	2.59	0.087	0.102
b	1.65	2.13	0.065	0.084
b_1	1.02	1.40	0.040	0.055
b_2	2.87	3.13	0.113	0.123
c	0.40	0.79	0.016	0.031
D	20.80	21.46	0.819	0.845
D_1	4.32	5.49	0.140	0.216
D_2	5.84	6.48	0.230	0.255
D_3	5.38	6.20	0.212	0.244
E	15.49	16.26	0.610	0.640
e	5.46 BSC		0.215 BSC	
L	19.81	20.32	0.780	0.800
L_1	–	4.50	–	0.177
ØP	3.56	3.66	0.140	0.144

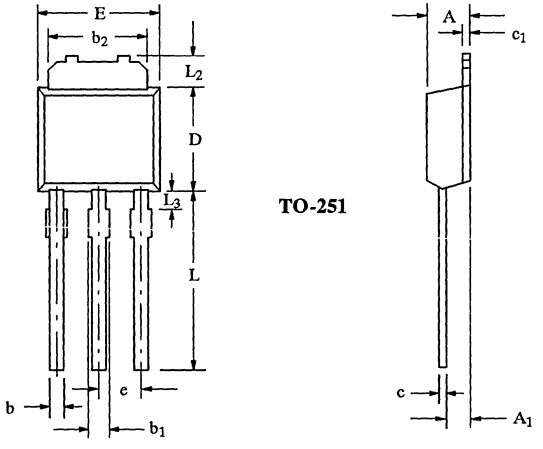
Package Information

■ TO-250 (4-Pin FETDIP)

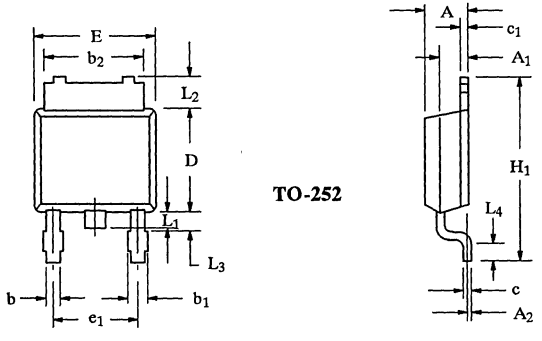


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A_1	0.86	1.12	0.034	0.044
b	0.51	0.61	0.020	0.024
b_1	0.89	1.14	0.035	0.045
c	0.33	0.43	0.013	0.017
D	4.93	5.03	0.194	0.198
E	5.97	6.48	0.235	0.255
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.62	7.87	0.300	0.310
L	3.18	4.06	0.125	0.160
L_1	0.89	1.40	0.035	0.055

■ TO-251 and TO-252

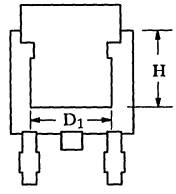


TO-251



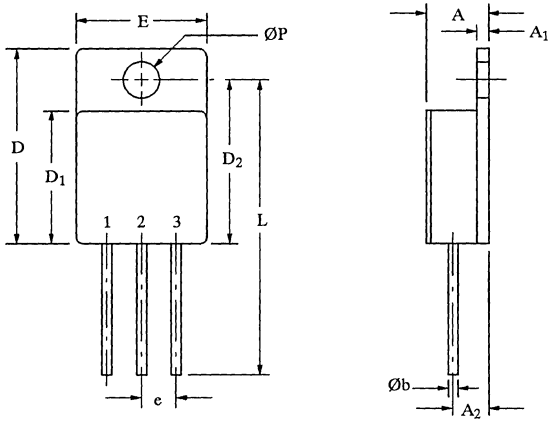
TO-252

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.21	2.39	0.087	0.094
A_1	0.89	1.14	0.035	0.045
A_2	0.03	0.23	0.001	0.09
b	0.71	0.89	0.028	0.035
b_1	0.76	1.14	0.030	0.045
b_2	5.23	5.44	0.206	0.215
c	0.46	0.58	0.018	0.023
c_1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D_1	4.49	5.00	0.177	0.197
E	6.48	6.73	0.255	0.265
e	2.29 BSC		0.090 BSC	
e_1	4.57 BSC		0.180 BSC	
H	4.32	–	0.170	–
H_1	9.65	10.41	0.380	0.410
L	8.89	9.53	0.355	0.375
L_1	0.64	1.02	0.025	0.040
L_2	0.89	1.27	0.035	0.050
L_3	1.02	1.52	0.040	0.060
L_4	0.51	–	0.020	–



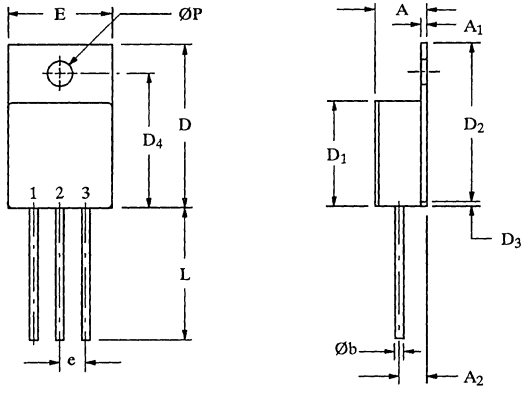
Package Information

TO-254AA



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	6.32	6.60	0.249	0.260
A_1	1.02	1.27	0.040	0.050
A_2	3.81 BSC		0.150 BSC	
Øb	0.89	1.14	0.035	0.045
D	20.07	20.32	0.790	0.800
D_1	13.59	13.84	0.535	0.545
D_2	16.89	17.40	0.665	0.685
E	13.59	13.84	0.535	0.545
e	3.81 BSC		0.150 BSC	
L	30.35	31.40	1.195	1.235
ØP	3.53	3.78	0.139	0.149

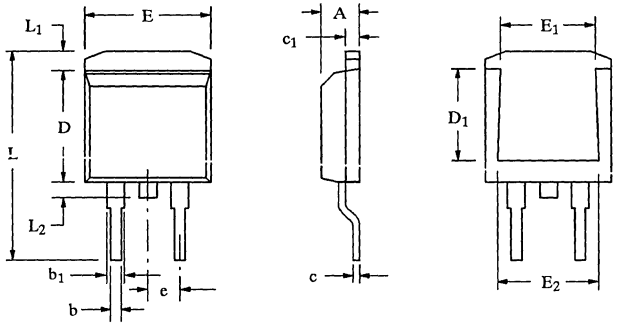
TO-257AB



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	–	5.33	–	0.210
A_1	0.64	0.89	0.025	0.035
A_2	2.79 BSC		0.110 BSC	
Øb	0.89	1.14	0.035	0.045
D	16.26	17.02	0.645	0.665
D_1	10.41	10.92	0.410	0.430
D_2	16.26	17.02	0.645	0.665
D_3	–	0.51	–	0.020
D_4	13.20	13.72	0.520	0.540
E	10.41	10.92	0.410	0.430
e	2.54 BSC		0.100 BSC	
L	12.70	14.73	0.500	0.580
ØP	3.56	3.81	0.140	0.150

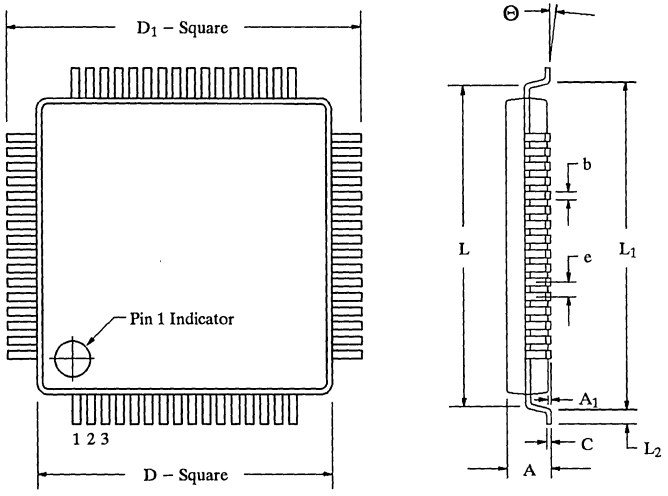
Package Information

■ TO-263 (D^2PAK)



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.32	4.70	0.170	0.185
b	0.71	1.02	0.028	0.040
b_1	1.27	1.65	0.050	0.065
c	0.33	0.51	0.013	0.020
c_1	1.14	1.40	0.045	0.055
D	8.64	9.65	0.340	0.380
D_1	–	5.72	–	0.225
E	10.03	10.41	0.395	0.410
E_1	7.87	8.64	0.310	0.340
E_2	9.02	9.53	0.355	0.375
e	2.54 BSC		0.100 BSC	
L	14.61	15.88	0.575	0.625
L_1	–	1.40	–	0.055
L_2	1.27	1.78	0.050	0.070

■ TQFP, 64-Pin

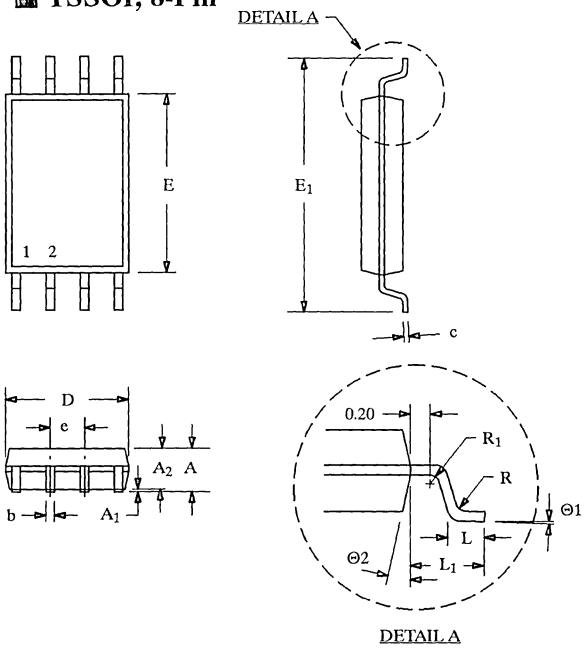


Dim	Millimeters		Inches*	
	Min	Max	Min	Max
A	0.977	1.177	0.039	0.046
A_1	0.04	0.16	0.002	0.006
b	0.14	0.26	0.006	0.010
C	0.117	0.177	0.005	0.007
D	9.90	10.10	0.390	0.398
D_1	11.7	12.3	0.461	0.484
e	0.40	0.60	0.016	0.024
L	–	10.80	–	0.425
L_1	10.80	11.20	0.425	0.441
L_2	0.30	0.70	0.012	0.028
Θ	0°	4°	0°	4°

*For Reference Only

Package Information

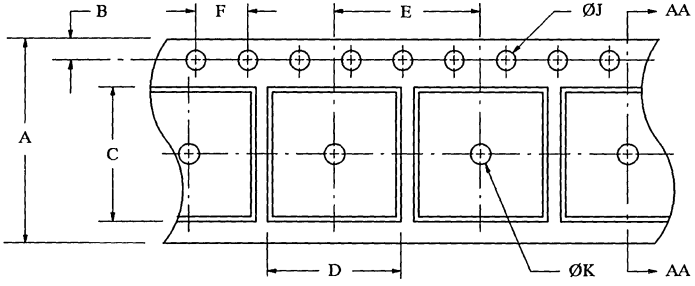
TSSOP, 8-Pin

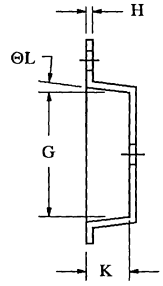


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.05	1.20	0.041	0.047
A_1	0.05	0.15	0.002	0.006
A_2	–	1.05	–	0.041
b	0.25	0.30	0.010	0.012
c	0.127		0.005	
D	2.90	3.10	0.114	0.122
E	4.30	4.50	0 170	0.177
E_1	6.20	6.60	0.244	0.260
e	0.65 BSC		0.025 BSC	
L	0.50	0.70	0.020	0.028
L_1	1.0		0.039	
R	0.09	–	0.004	–
R_1	0.09	–	0.004	–
Θ1	0°	8°	0°	8°
Θ2	12°			

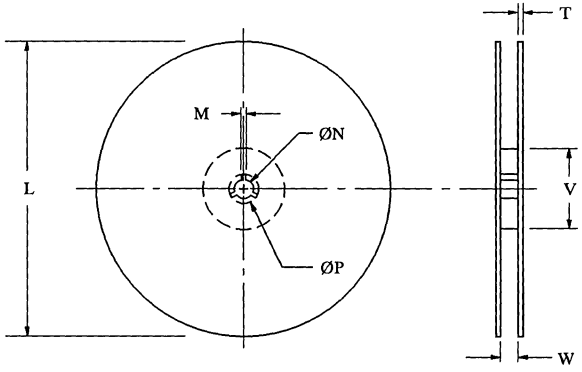
7 Appendix

■ Tape and Reel Options





SECTION A-A



Quantity Per Reel	
DPAK	2000
D^2PAK	800
SO-8	2500
SO-14	2500
SO-16	2500
SO-24 (WB)	1500

	SO-8				SO-14				SO-16			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	11.9	12.1	0.469	0.476	15.9	16.1	0 626	0.634	15.9	16.1	0.626	0.634
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	5.10	5.30	0.201	0.209	9.05	9.25	0.356	0.364	10.35	10.55	0.407	0.415
D	6.30	6.50	0.248	0.256	6.55	6.75	0.258	0.266	6.55	6.75	0.258	0.266
E	7.90	8.60	0.311	0.339	7.90	8.10	0.311	0.319	7.90	8.10	0.311	0.319
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	5.10	5.30	0.200	0.209	9.05	9.25	0.356	0.364	10.35	10.55	0.407	0.415
H	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.060	0.063	1.50	1.60	0.060	0.063
K	1.90	2.30	0.075	0.091	1.90	2.30	0.075	0.091	1.90	2.30	0.075	0.091
ØK	1.50	1.70	0.059	0.067	1.40	1.60	0.055	0.063	1.40	1.60	0.055	0.063
L	328	332	12.91	13.07	328	332	12.91	13.07	328	332	12.91	13.07
ΘL	–	3°	–	3°	–	3°	–	3°	–	3°	–	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098	1.50	2 50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.054	0.520	12.8	13.2	0.054	0.520
ØP	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	12.4	14.4	0.488	2.667	16.4	18.4	0.646	0.724	16.4	18.4	0.646	0.724

Tape and Reel Options (Cont'd)

	SO-24 (Widebody)				DPAK				D^2PAK			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	10.3	11.2	0.406	0.441	15.9	16.1	0 626	0.634	29.7	24.3	1.169	0.957
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	15.9	16.1	0.626	0.634	6.80	7.00	0.268	0.276	15.7	15.9	0.618	0.626
D	10.8	11.0	0.425	0.433	10.4	10.6	0.409	0.417	10.5	10.7	0.413	0.422
E	11.9	12.1	0.469	0.476	11.9	12.1	0.469	0.476	15.9	16.1	0.626	0.634
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	15.9	16.1	0.626	0.634	6.80	7.00	0.268	0.276	15.7	15.9	0.618	0 626
H	0.25	0 35	0.010	0.014	0.25	0.35	0.010	0.014	0.25	0.35	0.010	0.014
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063
K	2.8	3.2	0.110	0.126	2.50	2.70	0.098	0.1063	4.80	5 00	0.189	0.197
ØK	1.50	1.70	0.059	0.067	1.50	1.70	0.059	0.067	1.50	2.00	0.059	0.067
L	328	332	12.91	13.07	328	332	12.91	13 07	328	332	12.91	13.07
ΘL	–	3°	–	3°	–	3°	–	3°	–	3°	–	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12 8	13.2	0.504	0.520	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	24.4	26.4	0.961	1.039	16.4	18.4	0.646	0.724	24.4	26.4	0.961	1.039

Process Opiton Flows for Discrete Devices

Test and Condition			JANTXV Build and Test in Qualified 19500 Facility	JANTX Build Offshore Test in Qualified 19500 Facility	
Description	Methods Per MIL-S-19500 Power MOS	U.S. Build Only if Specified[a] Extended Hi-Rel	-1[b] Build and Test in Qualified 19500 Facility	-2[b] Offshore Build and Test	Industrial Standard
Traceability to W/L	With Exception	X	N/A	N/A	N/A
SEM	2077	X	N/A	N/A	N/A
Internal Visual	2069	Inhouse Spec Condition A	Inhouse Spec Condition B	Inhouse Spec Condition B	Inhouse Spec IND
Die Shear[c]	N/A	X	N/A	N/A	N/A
Bond Strength Cert/Data[c]	2037	X	N/A	N/A	N/A
Stab Bake	1032	X	X	X	N/A
Temp Cycle	1051	X	X	X	N/A
Centrifuge (if reg.)	2006	X	X	X	N/A
PIND	2052-A	X	N/A	N/A	N/A
Fine Leak[d]	1071	Condition G or H	Condition G or H	Condition G or H	AQL = 1% Hermetic
Gross Leak[d]	1071	Condition C or K	Condition C or K	Condition C or K	AQL = 1% Hermetic
Thermal Response	3161	X	X	X	AQL = 0.25%
Inductive Load	3470	X	X	X	N/A
Interim Electrical	per spec	Read/Record	Go/No-Go MOS	Go/No-Go MOS	N/A
Burn-In HTGB	1042-B	48 hrs. per dwg.	48 hrs. per dwg.	48 hrs. per dwg.	N/A
Interim Electrical	per spec	Read/Record per spec	Go/No-Go Read/Record per spec	Go/No-Go Read/Record per spec	N/A
Burn-In HTRB	1042-A	160 hrs. MOS 240 hrs. JFET/DMOS	160 hrs.	160 hrs.	N/A
Power Burn-In (MOS/LOPMOS)	1042-C	240 hrs. (Optional)	N/A	N/A	N/A
Interim Electrical	Static per spec MOS[e]	Read/Record 25°C PDA = 10%	Go/No-Go 25°C PDA = 10% Read/Record per spec	Go/No-Go 25°C PDA = 10% Read/Record per spec	N/A
Final Electrical	per spec	Subgroup 2-3	N/A	N/A	N/A
X-Ray	2076	X	N/A	N/A	N/A
External Visual	2071	X	LTPD-2	LTPD-2	AQL = 0.65%
QCI A MIL-S-19500 Sampling Plan for Group A Insp.	per spec	X	X	X	AQL = 0.065% Static Only
QCI B MIL-S-19500	per spec	X	per spec[f]	per spec[f]	N/A
QCI C MIL-S-19500	per spec	X	per spec[f]	per spec[f]	N/A
Read/Record Option	per spec	N/A	per spec[g]	per spec[g]	N/A
Deltas Option	per spec	Option	per spec	per spec	N/A
Solder Dip Option	per spec	Option	per spec	per spec	Option

Notes:
a. May be assembled offshore unless otherwise specified by MIL-S-19500 or drawing.
b. Per spec is a reference to Siliconix data sheet on -1 and -2 product or customer SCD whichever applies.
c. Test performed on line during assembly procedure (monitor).
d. Fine/gross leak test may be done at either steps after centrifuge or after final electrical.
e. PDA applies to second burn-ins.
f. For -1 and -2 level product, QCI B and C are performed by customer SCD only.
g. Read/record option by customer SCD only. (High-power MOS -1 & -2 include datalog & deltas. Low power—Go/No-Go

Process Option Flows for Discrete Chip/Wafer

Standard Die/Chip, and Chip Samples with Element Evaluation		
Die ship element evaluation Method 5008 Class B Subgroup 1 & 3 performed in-line screen.	Die ship. No canned samples.	Die Wafer Form
Wafer probe static 25°C (min) per device spec visual Method 2069 Cond B, MIL-STD-750.	Wafer probe static 25°C (min) per device spec visual Method 2069 Cond B, MIL-STD-750.	Wafer probe static 25°C (min) per device spec.
Canned samples: Per MIL-STD-883, Class B device. Subgroup 1 (ss−10/0) internal visual Method 2069 Cond B inhouse spec. Subgroup 2 (ss−10/1) final electrical static @ 25°C, elevated temperature per device spec. Subgroup 3 (5 die min) (s/s = 10/0 or 20/1 wires) NDT Method 2023 wire bond eval (bond pull). Method 2011 (cert & data). *SEM available	Die Prep Process	

Process Option Flows for Power ICs

Test and Condition		U.S. Build Only if Specified[a]	U.S. Build or QML Offshore Build	Parts Marked /883 or SMD, as Applicable[c]	
Description	Method Per MIL-STD-883	Space Rated Extended Hi-Rel[b]	Class B S/S JAN Devices	SMD and /883 Compliant Non-JAN Method 5004/5005	Ruggedized Plastic -4 Flow
Traceability to W/L		X	X	X	N/A
SEM		X	N/A	N/A	N/A
Internal Visual	2010	Condition A	Condition B	Condition B	Condition B
Die Shear	2019	X	N/A	N/A	N/A
Bond Strength Cert/Data	2011	X	N/A	N/A	N/A
Stab Bake	1008-C	X	X	X	X
Temp Cycle	1010-C	X	X	X	X
Centrifuge	2001-E	X	X	X	N/A
PIND	2020-A	X	N/A	N/A	N/A
Fine Leak	1014-A or -B	X	X	X	N/A
Gross Leak	1014-C	X	X	X	N/A
1st Electrical	per spec	X	X	X	X
Burn-In	1015-A or -C	72 hrs -A	160 hrs per S/S	160 hrs -A or -C	160 hrs. -A or -C
Interim Electrical Post Burn-In		per spec[d]	Static 25°C PDA per S/S	Static 25°C PDA = 5%	Static 25°C PDA = 5%
Burn-In	1015-A or -C	240 hrs Dyn. (Min.)	per S/S	N/A	N/A
Interim Electrical Post Burn-In	Static[e]	Static 25°C PDA = 5%	N/A	N/A	N/A
	Functional[e]	Functional 25°C PDA = 3% (datalog)	per S/S	N/A	N/A
Final Electrical	Min. Temp.	X	X	X	X
	Max. Temp.	X	X	X	X
Fine Leak	1014-A or -B	X	N/A	N/A	N/A
Gross Leak	1014-C	X	N/A	N/A	N/A
X-Ray	2012	X	N/A	N/A	N/A
QCI A	5005	per spec[d]	X	X	−55, 25, 125°C
QCI B	5005	X	X	X	N/A
QCI C	5005	N/A	X	X	N/A
QCI D	5005	X	X	X	N/A
External Visual	2009	X	X	X	X
Deltas Option		Option	X	N/A	N/A
Solder Dip Option		Option	Option	Option	N/A

Notes:
a. On U. S. builds, unless otherwise specified by 38510 or drawing, parts may be assembled offshore.
b. Space Rated Extended Hi-Rel process option available under customer SCD only.
c. Parts not qualified for /883 or SMD must not be marked as such. A special flow for non-compliant, non-JAN product can be generated as custom. Contact marketing for details.
d. Per spec is a reference to customer SCD.
e. PDA applies to both burn-ins.

Siliconix Direct Replacement

Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

Industry Part Number	Siliconix Part Number	Page
2N7012	IRFD123	6-41
2N7054	SMW45N10	6-137
HV9100	Si9100DY	3-1
HV9102	Si9102DY	3-9
HV9105	Si9105DY	3-24
HV9110	Si9110DY	3-31
HV9111	Si9111DY	3-31
HV9112	Si9112DY	3-38
HV9114	Si9114DY	3-44
HV9120	Si9120DY	3-49
IRF7101	Si9956DY	1-113
IRF7102	Si9959DY	1-123
IRF7103	Si9955DY	1-109
IRF7104	Si9953DY	1-105
IRF7105	Si9952DY	1-99
IRF7106	Si9942DY	1-65
IRF7201	Si9410DY	1-13
IRF7202	Si9400DY	1-1
IRF7204	Si9430DY	1-21
IRF7205	Si9435DY	1-33
IRF9540	SMP20P10	6-97
IRF9540	SMW20P10	6-133
IRFP048	SMW60N06-18	6-141
IRFP054	SMW70N06-14	6-149
IRFP150	SMW45N10	6-137
IRFP150	SMW60N10	6-145
IRFP9140	SMP20P10	6-97
IRFP9140	SMW20P10	6-133
IRFZ20	BUZ71	6-5
IRFZ22	BUZ71A	6-5
IRFZ30	BUZ11	6-1
IRFZ44	SMP50N06-25	6-117
IRFZ48	SMP60N06-14	6-125
MIC4469N, J	D469ADJ	4-1
MIC9400IBLM	Si9400DY	1-1

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MMDF1N05E	Si9955DY	1-109
MMDF2C02E	Si9942DY	1-65
MMDF2C05E	Si9950DY	1-93
MMDF2C02H	Si9958DY	1-117
MMDF2N02E	Si9956DY	1-113
MMDF2P01H	Si9933DY	1-47
MMDF2P02E	Si9953DY	1-105
MMDF2P02H	Si9947DY	1-85
MMDF3N03H	Si9936DY	1-51
MMDF4N02E	Si9956DY	1-113
MMSF3P02H	Si9430DY	1-21
MMSF3P03H	Si9435DY	1-33
MMSF4P01H	Si9433DY	1-25
MMSF5N03H	Si9410DY	1-13
MTB54N06HD	SUB60N06-14	6-161
MTD10N05E	SMD15N05	6-83
MTD10N05E-1	SMU15N05	6-83
MTD2955E	SMD10P05	6-73
MTD2955E-1	SMU10P05	6-73
MTD3055E	SMD15N05	6-83
MTD3055E-1	SMU15N05	6-83
MTH20P10	SMW20P10	6-133
MTH35N06E	SMW60N06-18	6-141
MTH40N06	SMW60N06-18	6-141
MTH40N08	SMW45N10	6-137
MTH40N10	SMW45N10	6-137
MTH50N05	SMW60N06-18	6-141
MTP10N05	BUZ71A	6-5
MTP12P10	IRF9530	6-29
MTP25N10	SMP30N10	6-105
MTP50N05E	SMP50N06-25	6-117
MTP50N06E	SMP50N06-25	6-117
MTP50N06E	SMP60N06-18	6-129
MTP54N06HD	SMP60N06-14	6-125
MTPP33N10E	SMP30N10	6-105

Cross Reference

Industry Part Number	Siliconix Part Number	Page
MTW20P10E	SMW20P10	6-133
MTW45N10E	SMW45N10	6-137
MTW45N10E	SMW60N10	6-145
NDB706A	SUB60N06-14	6-161
NDP505AEL	SMP25N05-45L	6-101
NDP606A	SMP50N06-25	6-117
NDP706A	SMP60N06-14	6-125
NDP706B	SMP60N06-18	6-129
NDP710B	SMP40N10	6-109
NDS9400	Si9400DY	1-1
NDS9405	Si9405DY	1-5
NDS9407	Si9407DY	1-9
NDS9410	Si9410DY	1-13
NDS9430	Si9430DY	1-21
NDS9435	Si9435DY	1-33
NDS9942	Si9942DY	1-65
NDS9943	Si9943DY	1-71
NDS9945	Si9945DY	1-81
NDS9947	Si9947DY	1-85
NDS9948	Si9948DY	1-89
NDS9952	Si9952DY	1-99
NDS9953	Si9953DY	1-105
NDS9955	Si9955DY	1-109
NDS9956	Si9956DY	1-113
NDS9958	Si9958DY	1-117
NTP12N05	BUZ71A	6-5
PWR-SMP400	Si9105DY	3-24
PWR-SMP520	Si9120DY	3-49
RFD10N05	SMU15N05	6-83
RFD10N05SM	SMD15N05	6-83
RFD14N05SM	SMD15N05	6-83
RFD16N05L	SMU25N05-45L	6-89
RFD16N05LSM	SMD25N05-45L	6-89
RFD805SM	SMD10P05	6-73
RFG40N10	SMW45N10	6-137

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RFG40N10	SMW60N10	6-145
RFG50N05	SMW60N06-18	6-141
RFG70N06	SMW70N06-14	6-149
RFP12P10	IRF9530	6-29
RFP25N05L	SMP25N05-45L	6-101
RFP30P06	SMP40P06	6-113
RFP40N10	SMP40N10	6-109
RFP50N05	SMP60N06-18	6-129
RFP70N06	SMP60N06-14	6-125
RRF520	IRF520	6-17
SSD2002	Si9952DY	1-99
SSD2003	Si9956DY	1-113
SSD2005	Si9953DY	1-105
SSD2007	Si9959DY	1-123
SSD2009	Si9955DY	1-109
STP40N10	SMP40N10	6-109
STP50N06	SMP50N06-25	6-117
STP60N03-10L	SMP60N03-10L	6-121
STP60N06	SMP60N06-18	6-129
STP60N06-16	SMP60N06-14	6-125
STVHD90	SMP60N06-18	6-129
STW60N10	SMW60N10	6-145
STW75N06	SMW70N06-14	6-149
TS9721	Si9433DY	1-25
TS9725	Si9435DY	1-33
TS9726	Si9410DY	1-13
TS9733	Si9933DY	1-47
TS9738	Si9936DY	1-51
TS9742	Si9925DY	1-37
TSC4469EOD	D469ADJ	4-1
TSC4469EPD	D469ADJ	4-1
TSC9100	Si9100DY	3-1
TSC9110	Si9110DY	3-31
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TSC9116	Si9120DY	3-49

Worldwide Sales Offices and Distributors

TEMIC

Siliconix

U.S. TEMIC Sales Offices

Eastern

Huntsville, AL (35824)
125 Electronics Boulevard, Ste. C-1
TEL: (205) 461-7894/7895
FAX: (205) 461-7928

Hoffman Estates, IL (60195)
1030 W. Higgins Road, Ste. 101
TEL: (708) 490-0374
FAX: (708) 490-1499

Troy, MI (48084)
Continental Plaza
2701 Troy Center Drive, Ste. 100
TEL: (810) 244-0610
FAX: (810) 244-0848

Annapolis, MD (21403)
1419 Forest Drive, Ste. 103
TEL: (410) 269-1898
FAX; (410) 974-8170

Asheville, NC (28801)
46 Haywood Street, Ste. 337
TEL: (704) 252-9827
FAX: (704) 252-5083

Nashua, NH (03062)
20 Heather Court
TEL: (603) 886-9603
FAX: (603) 886-9603

Annandale, NJ (08801)
1322 Route 31 North
TEL: (908) 735-6100
FAX: (908) 735-2258

Ossining, NY (10562)
74 Revolutionary Road
TEL: (914) 845-0618
FAX: (914) 945-0769

White Plains, NY (10605)
12 Roland Drive
TEL: (914) 997-1265
FAX: (914) 997-1277

Western

Santa Clara, CA (95056)
TEMIC c/o Siliconix Inc.
2201 Laurelwood Road
P.O. Box 54951
TEL: (408) 970-5700
FAX: (408) 970-3979

Irving, TX (75038)
TEMIC Technical Support Center
5605 North MacArthur Blvd.
TEL: (214) 756-0302
FAX: (214) 756-0702

Houston, TX (77027)
2100 West Loop South, Ste. 800
TEL: (713) 297-8871
FAX: (713) 297-8872

U.S. Sales Representatives

Alabama

Huntsville (35803)
Rep, Inc.
11535 Gilleland Road
TEL: (205) 881-9270
FAX: (205) 882-6692

Alaska

See Washington

Arizona

Tempe (85283)
QuadRep Southern
40 W. Baseline Road, Ste. 112
TEL: (602) 839-2102
FAX: (602) 839-2126

Arkansas

See Texas (Arlington)

California (Southern)

San Diego (92130)
QuadRep Southern, Inc.
11995 El Camino Real, Ste. 305
TEL: (619) 755-1188
FAX: (619) 793-9269

Irvine (92718)
QuadRep Southern, Inc.
15215 Alton Parkway, Ste. 200
TEL: (714) 727-4222
FAX: (714) 727-4033

California (Northern)

San Jose (95134)
QuadRep Crown, Inc.
2635 N. First Street, Ste. 116
TEL: (408) 432-3300
FAX: (408) 432-3428

Colorado

Englewood (80111)
QuadRep/RMS
6500 S. Quebec Street, Ste. 210
TEL: (303) 771-6886
FAX: (303) 771-6887

Connecticut

See New York (Metro/L.I.)

Delaware

See New Jersey (Southern)

District of Columbia

See Maryland

Florida

Lighthouse Point (33064)
Rep South, Inc.
3170 N. Federal Highway, Ste. 105
TEL: (305) 783-2501
FAX: (305) 783-2503

Maitland (32751)
Rep South, Inc.
235 S. Maitland, Ste. 211
TEL: (407) 628-4837
FAX: (407) 645-0356

Georgia

Tucker (30084)
Rep, Inc.
1944 Northlake Parkway
TEL: (404) 938-4358
FAX: (404) 938-0194

Hawaii

See California (Northern)

Idaho

Boise (83702)
QuadRep Crown, Inc.
1524 W. Hays
TEL: (208) 344-9588
FAX: (208) 344-9550

Illinois

Hoffman Estates (60195)
Victory Sales
1030 W. Higgins Road, Ste. 101
TEL: (708) 490-0300
FAX: (708) 490-1499

Indiana

Indianapolis (46250)
Victory Sales
8041 Knue Road
TEL: (317) 577-4786
FAX: (317) 577-4789

Iowa

Cedar Rapids (52402)
Stan Clothier Company
1930 Saint Andrews NE
TEL: (319) 393-1576
FAX: (319) 393-7317

Kansas

Lenexa (66215)
Stan Clothier Co.
13000 W. 87th St. Parkway, Ste. 105
TEL: (913) 492-2124
FAX: (913) 492-1855

Kentucky

See Indiana

Louisiana

See Arlington, Texas

Maine

See Massachusetts

Maryland

Towson (21204)
Arbotek Associates, Inc.
102 W. Joppa Road
TEL: (410) 825-0775
FAX: (410) 337-2781

Massachusetts

Waltham (02154)
Technology Sales, Inc.
332 Second Avenue
TEL: (617) 890-5700
FAX: (617) 890-3913

Michigan

See TEMIC Sales Offices, Troy, MI

Minnesota

Eden Prairie (55344)
Stan Clothier
9600 W. 76th Street, Ste. A
TEL: (612) 944-3456
FAX: (612) 944-6904

Mississippi

See Alabama

Missouri

Saint Charles (63303)
Stan Clothier Company
3910 Old Highway 94, South, Ste. 116
TEL: (314) 928-8078
FAX: (314) 447-5214

Montana

See Washington

Nebraska

See Missouri

Nevada (Except Clark County)

See Califronia (Northern)

Nevada (Clark County)

See Arizona

New Hampshire

See Massachusetts

New Jersey (Northern)

See New York (Metro/L.I.)

New Jersey (Southern)

Marlton (08053)
Astrorep
Evesham Commons
525 Route 73, Ste. 100
TEL: (609) 983-1020
FAX: (609) 983-1879

New Mexico

See Arizona

New York (Upstate)

Fairport (14450)
Technology Sales, Inc
920 Perinton Hills Office Park
TEL: (716) 223-7500
FAX: (716) 223-5526

New York (Metro/L.I.)

Babylon (11702)
Astrorep Incorporated
103 Cooper Street
TEL: (516) 422-2500
FAX: (516) 422-2504

North Carolina

Morrisville (27560)
Rep. Inc.
2500 Gateway Centre Blvd., Ste. 400
TEL: (919) 469-9997
FAX: (919) 481-3879

North Dakota

See Minnesota

Ohio

Beachwood (44122)
Victory Sales
25825 Science Park Drive, Ste. 100
TEL: (216)766-5785
FAX: (216) 766-5796

Centerville (45459)
Victory Sales
77 Elmwood Drive, Ste. 206
TEL: (513) 436-1222
FAX: (513) 436-1224

Oklahoma

See Texas (Arlington)

U.S. Sales Representatives (Cont'd)

Oregon

Portland (97224)
QuadRep Crown, Inc.
17020 SW. Upper Boones Ferry Rd., Ste. 202
TEL: (503) 620-8320
FAX: (503) 639-4023

Pennsylvania (Western)

See Indiana

Pennsylvania (Eastern)

See New Jersey (Southern)

Puerto Rico

San German (00683-0121)
Technology Sales, Inc.
PO Box 122, Edificio Rali, Ste. 216
TEL: (809) 892-4745
FAX: (809) 892-1128

Rhode Island

See Massachusetts

South Carolina

See Tennessee

South Dakota

See Minnesota

Tennessee

Jefferson City (37760)
Rep. Inc.
P. O. Box 490
1908 Branner Avenue
TEL: (615) 475-9012/9013
FAX: (615) 475-6340

Texas

Arlington (76006)
Ion Associates, Inc.
2221 E. Lamar, Ste. 250
TEL: (817) 695–8000
FAX: (817) 695-8010

Austin (78759)
Ion Associates, Inc.
4412 Spicewood Springs Rd., Ste. 202
TEL: (512) 794-9006
FAX: (512) 794-9008

Houston (77014)
Ion Associates, Inc.
14347-A Torrey Chase Blvd.
TEL: (713) 537-7717
FAX: (713) 537-5612

Utah

See Colorado

Vermont

See Massachusetts

Virginia

See Maryland

Washington

Bellevue (98005)
QuadRep Crown, Inc.
375 118th Ave., S.E., Ste. 110
TEL: (206) 453-5100
FAX: (206) 646-8775

West Virginia

See Maryland

Wisconsin

Brookfield (53005)
Victory Sales
405 N. Calhoun Road, Ste. 208
TEL: (414) 789-5770
FAX: (414) 789-5760

Wyoming

See Colorado

Brampton, Ontario (L6T 1K2)
Electronics Sales Professionals (ESP) Inc.
27 Anne Court
TEL: (905) 458-1103
FAX: (905) 458-4469

Montreal, Quebec (H2B 1Z2)
Electronics Sales Professionals (ESP) Inc.
2102 Place Etienne-Brule
TEL: (514) 388-6596
FAX: (514) 388-8402

North Gower, Ontario (K0A 2T0)
Electronics Sales Professionals (ESP) Inc.
5936 Third Line Road North RR #3
TEL: (613) 489-3379
FAX: (613) 489-2778

Scarborough, Ontario (M1V 3P6)
Electronics Sales Professionals (ESP) Inc.
60 Wilderness Drive
TEL: (416) 321-9693
FAX: (416) 321-9794

British Columbia

See Washington

Chip Distributor

Florida

Orlando (32810)
Chip Supply, Inc.
7725 N. Orange Blossom Trail
TEL: (407) 298-7100
TWX: (810) 850-0103
FAX: (407) 290-0164

U. S. Distributors

Alabama

Huntsville (35816)
Future Electronics Corp.
4825 University Square, Ste. 12
TEL: (205) 830-2322
FAX: (205) 830-6664

Huntsville (35801)
Marshall Industries
3313 Memorial Parkway South, Ste. 150
TEL: (205) 881-9235
FAX: (205) 881-1490

Huntsville (35816)
Pioneer Tech.
4835 University Square, Ste. 5
TEL: (205) 837-9300
FAX: (205) 837-9358

Arizona

Phoenix (85034)
Future Electronics Corp.
4636 E. University Drive, Ste. 245
TEL: (602) 968-7140
FAX: (602) 968-0334

Phoenix (85044)
Marshall Industries
9831 S. 51st Street, Ste. C108
TEL: (602) 496-0290
FAX: (602) 893-9029

Tempe (85281)
Bell Industries
140 S. Lindon Lane #102
TEL: (602) 966-3600
(800) 525-6666
FAX: (602) 967-6584

Tempe (85281)
Hamilton Hallmark
1626 S. Edward Drive
TEL: (800) 332-8638
FAX: (800) 257-0568

California

Agoura Hills (91301)
Bell Industries
30101 Agoura Court, Ste. 118
TEL: (818) 865-7900
(800) 525-6666
FAX: (818) 991-7695

Agoura Hills (91301)
Future Electronics
27489 West Agoura Road, Ste. 300
TEL: (818) 865-0040
TEL: (800) 876-6008
FAX: (818) 865-1340

Agoura Hills (91301)
Pioneer Std.
5126 Clareton Drive, Ste. 160
TEL: (818) 865-5800
FAX: (818) 865-5814

Calabasas (91302-1959)
Marshall Industries
26637 Agoura Road
TEL: (818) 878-7000
FAX: (818) 880-6846

Costa Mesa (92626)
Hamilton Hallmark – #29
3170 Pullman Street
TEL: (714) 641-4100
FAX: (714) 641-4122

Culver City (90230)
Hamilton Corporate
10950 W. Washington Blvd.
TEL: (310) 558-2000
FAX: (310) 558-2076 - Commercial
FAX: (310) 558-2809 - Military

El Monte (91731)
Marshall Corporate
9320 Telstar Avenue
TEL: (818) 307-6000
FAX: (818) 307-6297

Irvine (92718)
Bell Industries
220 Technology Drive, Ste. 100
TEL: (714) 727-4500
(800) 525-6666
FAX: (714) 453-4610

Irvine (92714)
Future Electronics Corp.
1692 Browning Ave.
TEL: (714) 250-4141
FAX: (714) 250-4185

Irvine (92718)
Marshall Industries
1 Morgan
TEL: (714) 859-5050
FAX: (714) 581-5255

Irvine (92718)
Pioneer Std.
217 Technology Drive, Ste. 110
TEL: (714) 753-5090
FAX: (714) 753-5074

Irvine (92718
Zeus Electronics
6 Cromwell, Ste. 100
TEL: (714) 581-4622
TEL: (800) 52-HI-REL
FAX: (714) 454-4355

Los Angeles (90049)
Bell Industries
11812 San Vincente Blvd., Ste. 300
TEL: (310) 826-2355
(800) 525-6666
FAX: (310) 826-1534

Milpitas (95035)
Marshall Industries
336 Los Coches Street
TEL: (408) 942-4600
FAX: (408) 262-1224

Rancho Cordova (95670)
Marshall Industries
3039 Kilgore Ave. Ste. 140
TEL: (916) 635-9700
FAX: (916) 635-6044

Reseda (91335)
JAN Devices
6925 Canby, Bldg. 109
TEL: (818) 757-2000
FAX: (818) 708-7436

Rocklin (95677)
Bell Industries
4311 Anthony Ct., Ste. 100
TEL: (916) 652-0418
(800) 525-6666
FAX: (916) 652-0403

Rocklin (95765)
Hamilton Hallmark – #35
580 Menlo Drive, Ste. 2
TEL: (916) 624-9781
FAX: (916) 961-0922

San Diego (92123)
Bell Industries
5520 Ruffin Road, Ste. 209
TEL: (619) 576-3924
(800) 525-6666
FAX: (619) 492-9826

U. S. Distributors (Cont'd)

California (Cont'd)

San Diego (92122)
Future Electronics Corp.
5151 Shoreham Place, Ste. 220
TEL: (619) 625-2800
FAX: (619) 625-2810

San Diego (92123)
Hamilton Hallmark – #02
4545 Viewridge Avenue
TEL: (619) 571-7540
FAX: (619) 277-6136

San Diego (92123)
Marshall Industries
5961 Kearny Villa Road
TEL: (619) 627-4140
FAX: (619) 627-4163

San Jose (95131)
Hamilton Hallmark – #03
2105 Lundy Avenue
TEL: (408) 435-3500
FAX: (408) 435-3720

San Jose (95131-1326)
Future Electronics Corp.
2220 O'Toole Avenue
TEL: (408) 434-1122
FAX: (408) 433-0822

San Jose (95134)
Pioneer Tech.
134 Rio Robles
TEL: (408) 954-9100
FAX: (408) 954-9113

San Jose (95119)
Zeus Electronics
6276 San Ignacio Ave., Ste. E
TEL: (408) 629-4789
TEL: (800) 52-HI-REL
FAX: (408) 629-4792

Sunnyvale (94089)
Bell Industries
1161 No. Fairoaks Avenue
TEL: (408) 734-8570
(800) 525-6666
FAX: (408) 734-8875

Woodland Hills (91367)
Hamilton /Avnet – #48
21150 Califa Street
TEL: (818) 594-0404
FAX: (818) 594-8234

Yorba Linda (92686)
Zeus Electronics
22700 Savi Ranch Pkwy.
TEL: (714) 921-9000
FAX: (714) 921-2715

Colorado

Lakewood (80215)
Future Electronics Corp.
12600 W. Colfax Avenue, Ste. B110
TEL: (303) 232-2008
(800) 950-3532
FAX: (303) 232-2009

Denver (80222)
Bell Industries
1873 S. Bellaire Street, Ste. 100
TEL: (303) 691-9270
(800) 525-6666
FAX: (303) 691-9036

Englewood (80111)
Hamilton Hallmark – #06
12503 E. Euclid Drive, Ste. 20
TEL: (303) 799-7800
FAX: (303) 790-4991

Thornton (80241)
Marshall Industries
12351 N. Grant Street, Ste A
TEL: (303) 451-8444
FAX: (303) 457-2899

Connecticut

Cheshire (06410)
Future Electronics Corp.
Westgate Office Center
700 West Johnson Ave.
TEL: (203) 250-0083
FAX: (203) 250-0081

Cheshire (06410)
Hamilton Hallmark – #21
125 Commerce Court, Unit 6
TEL: (203) 797-2800
FAX: (203) 272-1704

Shelton (06484)
Pioneer Std.
2 Trap Falls Road
TEL: (203) 929-5600
FAX: (203) 929-9791

Meriden (06413)
Bell Industries
1064 E. Main Street
TEL: (203) 639-6000
(800) 525-6666
FAX: (203) 639-6005

Wallingford (06492)
Marshall Industries
20 Sterling Drive
Barnes Industrial Park
TEL: (203) 265-3822
FAX: (203) 284-9285

Florida

Altamonte Springs (32701)
Bell Industries
650 S. North Lake Blvd., Ste. 400
TEL: (407) 339-0078
(800) 525-6666
FAX: (407) 339-0139

Altamonte Springs (32701)
Future Electronics Corp.
650 S. Northlake Blvd.
TEL: (407) 767-8414
FAX: (407) 834-9318

Altamonte Springs (32701)
Marshall Industries
380 S. Northlake Blvd., Ste. 1024
TEL: (407) 767-8585
FAX: (407) 767-8676

Altamonte Springs (32701)
Pioneer Tech.
337 South Northlake Blvd. #1000
TEL: (407) 834-9090
FAX: (407) 834-0865

Deerfield Beach (33442)
Pioneer Tech.
674 S. Military Trail
TEL: (305) 428-8877
FAX: (305) 481-2950

Fort Lauderdale (33309)
Hamilton Hallmark, – #17
3350 N.W. 53rd Street, Ste. 105
TEL: (305) 484-5482
FAX: (305) 484-4740

Fort Lauderdale (33309)
Marshall Industries
2700 W. Cypress Creek Road, Ste. D114
TEL: (305) 977-4880
FAX: (305) 977-4887

Lake Mary (32746)
Zeus Electronics
37 Skyline Drive, Bldg. D, Ste. 3101
TEL: (407) 333-3055
TEL: (800) 52-HI-REL
FAX: (407) 333-9681

Largo (34641)
Future Electronics
2200 Tall Pines Drive, Ste. 108
TEL: (813) 530-1222
FAX: (813) 538-9598

Georgia

Duluth (30136)
Hamilton Hallmark
3425 Corporate Way, Ste. A
TEL: (404) 623-4400
FAX: (404) 476-8806
FAX: (404) 476-3043

Duluth (30136)
Pioneer Tech.
4250C Rivergreen Parkway
TEL: (404) 623-1003
FAX: (404) 623-0665

Norcross (30071)
Bell Industries
3000 Business Park Drive #D
TEL: (404) 446-7167
(800) 525-6666
FAX: (404) 446-7264

Norcross (30071)
Future Electronics Corp.
3150 Holcomb Bridge Road, Ste. 130
TEL: (404) 441-7676
FAX: (404) 441-7580

Norcross (30093)
Marshall Industries
5300 Oakbrook Pkwy., Ste. 140
TEL: (404) 923-5750
FAX: (404) 923-2743

Illinois

Addison (60101)
Pioneer Std.
2171 Executive Drive, Ste. 200
TEL: (708) 495-9680
FAX: (708) 495-9831

Bensenville (60106)
Hamilton Hallmark – #10
1130 Thorndale Avenue
TEL: (708) 860-7780
FAX: (708) 773-7969

Elk Grove Village (60007)
Bell Industries
870 Cambridge Drive
TEL: (708) 640-1910
(800) 525-6666
FAX: (708) 640-1928

Hoffman Estates (60195)
Future Electronics Corp.
3150 W. Higgins Road, Ste. 160
TEL: (708) 882-1255
(800) 933-9841
FAX: (708) 490-9290

Itasca (60143)
Zeus Electronics
1140 W. Thorndale Ave.
TEL: (708) 595-9730
TEL: (800) 52-HI-REL
FAX: (708) 595-9896

Schaumburg (60173)
Marshall Industries
50 E. Commerce Drive, Unit I
TEL: (708) 490-0155
FAX: (708) 490-0569

Indiana

Fort Wayne (46803)
Bell Industries
3433 E. Washington Blvd.
TEL: (219) 422-4300
(800) 525-6666
FAX: (219) 423-3420

Indianapolis (46268)
Bell Industries
P.O. Box 6885
5230 W. 79th Street
TEL: (317) 875-8200
(800) 525-6666
FAX: (317) 875-8219

Indianapolis (46240)
Future Electronics Corp.
8425 Wood Field Crossing
TEL: (317) 469-0447
FAX: (317) 469-0448

Indianapolis (46268)
Hamilton Hallmark – #28
4275 W. 96th Street
TEL: (317) 872-8875
FAX: (317) 876-7165

Indianapolis (46240)
Pioneer Std.
9350 N. Priority Way West Drive
TEL: (317) 573-0880
(800) 332-5503 (IN)
(800) 428-9128 (IL, KY)
FAX: (317) 573-0979

Iowa

Cedar Rapids (52402)
Hamilton Hallmark – #44
2335-A Blairsferry N.E.
TEL: (319) 393-0033
FAX: (319) 393-7050

Kansas

Lenexa (66219)
Hamilton Hallmark – #58
10809 Lakeview Ave.
TEL: (913) 888-4747
FAX: (913) 888-0523

Lenexa (66214)
Marshall Industries
10413 W. 84th Terrace
TEL: (913) 492-3121
FAX: (913) 492-6205

Overland Park (66212)
Future Electronics Corp.
8826 Santa Fe Drive, Ste. 150
TEL: (913) 649-1531
(800) 950-1531
FAX: (913) 649-1786

Kentucky

Lexington (40511-1001)
Hamilton Hallmark
1847 Mercer Road, Ste. G
TEL: (606) 259-1475
FAX: (606) 288-4936

Maryland

Columbia (21046)
Bell Industries
8945 Guilford Road, Ste. 130
TEL: (410) 290-5100
(800) 525-6666
FAX: (410) 290-8006

Columbia (21046)
Future Electronics Corp.
6716 Alexander Bell Dr., Ste. 101
TEL: (41) 290-0600
FAX: (410) 290-0328

Columbia (21046-2101)
Hamilton Hallmark – #12
10240 Old Columbia Road
TEL: (410) 988-9800
FAX: (410) 381-2036

U. S. Distributors (Cont'd)

Maryland (Cont'd)

Columbia (21046)
Marshall Industries
9130 Guilford Road, Ste. B
TEL: (410) 880-3030
FAX: (410) 880-3202

Gaithersburg (20877)
Pioneer Tech.
9100 Gaither Road
TEL: (301) 921-0660
FAX: (301) 921-4255

Silver Springs (20904)
Marshall Industries
2221 Broad Birch Drive, Ste. G
TEL: (301) 622-1118
FAX: (301) 622-0451

Massachusetts

Andover (01810)
Bell Industries
100 Burtt Road, Suite 106
TEL: (508) 474-8880
(800) 525-6666
FAX: (508) 474-8902

Bolton (01740)
Future Electronics Corp.
41 Main Street
TEL: (508) 779-3000
FAX: (508) 779-5143

Lexington (02173)
Pioneer Std.
44 Hartwell Ave.
TEL: (617) 861-9200
FAX: (617) 863-1547

Peabody (01960)
Hamilton Hallmark – #18
10 M Centennial Drive
TEL: (508) 532-3701
FAX: (508) 532-9802

Wilmington (01877)
Zeus Electronics
25 Upton Drive
TEL: (508) 658-4776
FAX: (508) 694-2199

Wilmington (01887)
Marshall Industries
33 Upton Drive
TEL: (508) 658-0810
FAX: (508) 657-5931

Michigan

Grand Rapids (49512)
Future Electronics Corp.
4505 Broadmoor SE
TEL: (616) 698-6800
(800) 334-6808
FAX: (616) 698-6821

Grand Rapids (49512)
Pioneer Std.
4594 Broadmoor Ave. SE, Ste. 235
TEL: (616) 698-1802
FAX: (616) 698-1831

Livonia (48150)
Future Electronics Corp.
35200 Schoolcraft Road, Ste. 106
TEL: (313) 261-5270
FAX: (313) 261-8175

Livonia (48150)
Marshall Industries
31067 Schoolcraft Road
TEL: (313) 525-5850
FAX: (313) 525-5855

Plymouth (48270)
Pioneer Std.
44190 Plymouth Oaks Drive
TEL: (313) 416-2157
FAX: (313) 416-2415

Novi (40375)
Hamilton Hallmark – #66
41650 Gardenbrook, Ste. 100
TEL: (313) 347-4271
FAX: (313) 347-4021

Minnesota

Bloomington (55341)
Hamilton Hallmark – #63
9401 James Avenue South, Ste. 140
TEL: (612) 881-2600
FAX: (612) 881-9461

Eden Prairie (55344)
Future Electronics Corp.
10025 Valley View Road, Ste. 196
TEL: (612) 944-2200
FAX: (612) 944-2520

Eden Prairie (55344)
Pioneer Std.
7625 Golden Triangle Drive
TEL: (612) 944-3355
FAX: (612) 944-3794

Plymouth (55447)
Marshall Industries
14800 28th Ave. North, Ste. 175
TEL: (612) 559-2211
FAX: (612) 559-8321

Missouri

Earth City (63045)
Hamilton Hallmark – #05
3783 Rider Trail South
TEL: (314) 291-5350
FAX: (314) 291-0362

Saint Louis (63141)
Future Electronics Corp.
12125 Woodcrest Executive Drive, Ste. 220
TEL: (314) 469-6805
(800) 727-6805
FAX: (314) 469-7226

New Hampshire

See Massachusetts

New Jersey

Fairfield (07004)
Bell Industries
271 Route 46 West, Ste. F202-203
TEL: (201) 227-6060
(800) 525-6666
FAX: (201) 227-2626

Fairfield (07006)
Marshall Industries
101 Fairfield Road
TEL: (201) 882-0320
FAX: (201) 882-0095

Fairfield (07006)
Pioneer Std.
14 "A" Madison Road
TEL: (201) 575-3510
FAX: (201) 575-3454

Marlton (08053)
Future Electronics Corp.
12 E. Stow Road, Ste. 200, Bldg. 12
TEL: (609) 596-4080
FAX: (609) 596-4266

Mt. Laurel (08054)
Marshall Industries
158 Gaither Drive, Unit 100
TEL: (609) 234-9100 (NJ)
TEL: (215) 627-1920 (PA)
FAX: (609) 778-1819

New Mexico

Albuquerque (87123)
Bell Industries
11728 Linn N.E.
TEL: (505) 292-2700
(800) 525-6666
FAX: (505) 275-2819

Albuquerque (87109-3147)
Hamilton Hallmark – #22
7801 Academy Rd. NE-Bldg. 2, Ste. 102
TEL: (505) 345-0001
TWX: (910) 989-0614
FAX: (505) 828-0360

New York

Binghamton (13901)
Pioneer Std.
1249 Upper Front Street, #201
TEL: (607) 722-9300
FAX: (607) 722-9562

Endicott (13760)
Marshall Industries
100 Marshall Drive
TEL: (607) 798-1611
FAX: (607) 797-7031

Fairport (14450)
Pioneer Std.
840 Fairport Park
TEL: (716) 381-7070
FAX: (716) 381-5955

Hauppauge (11788)
Future Electronics Corp.
801 Motor Parkway
TEL: (516) 234-4000
FAX: (516) 234-6183

Hauppauge (11788)
Hamilton Hallmark – #20
933 Motor Parkway
TEL: (516) 434-7470
FAX: (516) 434-7491

Port Chester (10573)
Zeus Electronics
100 Midland Avenue
TEL: (914) 937-7400
(800) 52-HI-REL
FAX: (914) 937-2553

Rochester (14625)
Future Electronics Corp.
300 Linden Oaks
TEL: (716) 387-9550
(800) 950-5539
FAX: (716) 387-9563

Rochester (14623)
Hamilton Hallmark – #61
1057 E. Henrietta Road
TEL: (716) 475-9130
FAX: (716) 475-9119

Rochester (14624)
Marshall Industries
1250 Scottsville Road
TEL: (716) 235-7620
TWX: (510) 253-5526
FAX: (716) 235-0052

Syracuse (13212-4513)
Future Electronics Corp.
200 Salina Meadows Pkwy., Ste. 130
TEL: (315) 451-2371
FAX: (315) 451-7258

Woodbury (11797)
Pioneer Std.
60 Crossways Park W.
TEL: (516) 921-8700
FAX: (516) 921-2143

North Carolina

Concord (28026)
Future Electronics
Smith Tower, Ste. 314
Charlotte Motor Speedway
P.O. Box 600
TEL: (704) 455-9030
TEL: (800) 424-1019
FAX: (704) 455-9173

Morrisville (27560)
Pioneer Tech.
2200 Gateway Center Blvd., Ste. 215
TEL: (919) 460-1530
FAX: (919) 460-1540

Raleigh (27604)
Future Electronics Corp.
5225 Capitol
1 North Commerce Center
TEL: (919) 790-7111
FAX: (919) 790-9022

Raleigh (27604)
Hamilton Hallmark
5234 Greens Dairy Rd.
TEL: (919) 872-0712
FAX: (919) 878-8729

Raleigh (27604)
Marshall Industries
5224 Greens Dairy Road
TEL: (919) 878-9882
FAX: (919) 872-2431

Ohio

Cleveland (44105)
Pioneer Std.
4800 E. 131st Street
TEL: (216) 587-3600
FAX: (216) 587-3906

Dayton (45459)
Bell Industries
446 Windsor Park Drive
TEL: (513) 434-8231
(800) 525-6666
FAX: (513) 434-8103

Dayton (45459)
Hamilton Hallmark – #64
7760 Washington Village Drive
TEL: (513) 439-6721
FAX: (513) 439-6705

Dayton (45414)
Marshall Industries
3520 Park Center Drive
TEL: (513) 898-4480
FAX: (513) 898-9835

Dayton (45424)
Pioneer Std.
4433 Interpoint Blvd.
TEL: (513) 236-9900
FAX: (513) 236-8133

Mayfield Heights (44124)
Future Electronics Corp.
6009 E Lander Haven Drive
TEL: (216) 449-6996
FAX: (216) 449-8987

Solon (44139)
Marshall Industries
30700 Bainbridge Road Unit A
TEL: (216) 248-1788
FAX: (216) 248-2312

Worthington (43085)
Hamilton Hallmark – #64
777 Dearborn Lane, Ste. L
TEL: (614) 888-3313
(800) 767-0392
FAX: (614) 888-0767

U. S. Distributors (Cont'd)

Oklahoma

Tulsa (74146)
Hamilton Hallmark – #46
5411 S. 125th East Avenue, Ste. 305
TEL: (918) 252-7297
FAX: (918) 254-6207

Tulsa (74146)
Pioneer
9717 E. 42nd Street, Ste. 105
TEL: (918) 665-7840
FAX: (918) 665-1891

Oregon

Beaverton (97005)
Bell Industries
9275 S.W. Nimbus
TEL: (503) 644-3444
(800) 444-7853
FAX: (503) 520-1948

Beaverton (97006)
Future Electronics Corp
Cornell Oaks Corp Center
15236 N.W. Greenbrier
TEL: (503) 645-9454
FAX: (503) 645-1559

Beaverton (97005)
Hamilton Hallmark – #27
9750 SW Nimbus Ave.
TEL: (503) 526-6200
(800) 962-8648
FAX: (503) 641-5939

Beaverton (97005)
Marshall Industries
9705 S.W. Gemini
TEL: (503) 644-5050
FAX: (503) 646-8256

Pennsylvania

Horsham (19044)
Pioneer Tech.
500 Enterprise Road
Keith Valley Business Center
TEL: (215) 674-4000
TWX: (510) 665-6778
FAX: (215) 674-3107

Pittsburgh (15238)
Pioneer Std.
259 Kappa Drive
TEL: (412) 782-2300
FAX: (412) 963-8255

Trevose (19053)
Bell Industries
2556 Metropolitan Drive
TEL: (215) 953-2800
(800) 525-6666
FAX: (215) 364-4927

Texas

Austin (78759)
Future Electronics Corp.
9020 II Capital of Texas Hwy. N.
TEL: (512) 502-0991
(800) 678-0991
FAX: (512) 502-0740

Austin (78727)
Hamilton Hallmark – #26
12211 Technology Blvd.
TEL: (512) 258-8848
FAX: (512) 258-3777

Austin (78758)
Pioneer Std.
1826 D Kramer Lane
TEL: (512) 835-4000
FAX: (512) 835-9829

Carrollton (75006)
Zeus Electronics
3220 Commander Drive
TEL: (214) 380-4330
(800) 52-HI-REL
FAX: (214) 447-2222

Dallas (75244)
Pioneer Std.
13765 Beta Road
TEL: (214) 386-7300
FAX: (214) 490-6419

Houston (77042)
Future Electronics Corp.
10333 Richmond Ave., Ste. 970
TEL: (800) 785-1156
FAX: (713) 785-4558

Houston (77063)
Hamilton Hallmark – #11
8000 West Glen
TEL: (713) 781-6100
FAX: (713) 953-8420

Houston (77043)
Marshall Industries
10681 Haddington, Ste. 160
TEL: (713) 467-1666
FAX. (713) 467-9805

Houston (77099)
Pioneer Std.
10530 Rockley Road, Ste. 100
TEL: (713) 495-4700
FAX: (713) 495-5642

Richardson (75081)
Bell Industries
1701 Greenville Avenue, Ste. 306
TEL: (214) 690-0486
(800) 525-6666
FAX: (214) 690-0467

Richardson (75081)
Future Electronics Corp.
800 E. Campbell
TEL: (214) 437-2437
FAX: (214) 669-2347

Richardson (75081)
Marshall Industries
1551 N. Glenville Drive
TEL: (214) 705-0604
FAX: (214) 705-0675

Carrollton (75006)
Zeus Electronics
3220 Commander Drive
TEL: (214) 380-4330
FAX: (214) 447-2222

Utah

Midvale (84047)
Bell Industries
6912 South 185 West, Ste. B
TEL: (801) 561-9691
(800) 525-6666
FAX: (801) 255-2477

Salt Lake City (84106)
Future Electronics Corp.
3450 South Highland Drive, Ste. 301
TEL: (801) 467-4448
FAX: (801) 467-3604

Salt Lake City (84121)
Hamilton Hallmark – #09
1100 E. 6600 S., Ste. 120
TEL: (801) 266-2022
FAX: (801) 263-0104

Salt Lake City (84119-1552)
Marshall Industries
2355 S. 1070 W #D
TEL: (801) 485-1551
FAX: (801) 487-0936

Washington

Bellevue (98004)
Bell Industries
1715 114th Ave., S.E., Ste. 208
TEL: (206) 646-8750
(800) 723-1335
FAX: (206) 646-8559

Bellevue (98007)
Pioneer Tech., Ste. 100
2800 156th Avenue, S.E.
TEL: (206) 644-7500
FAX: (206) 644-7300

Bothell (98011)
Future Electronics Corp.
19102 N. Creek Pkwy., Ste. 118
TEL: (206) 489-3400
FAX: (206) 489-3411

Redmond (98052)
Hamilton Hallmark – #07
8630 154th Avenue, N.E.
TEL: (206) 881-6697
FAX: (206) 867-0159

Wisconsin

Brookfield (53045)
Future Electronics
250 N. Patrick Blvd., Ste. 170
TEL: (414) 879-0244
FAX: (414) 829-8250

Brookfield (53005)
Pioneer Standard
120 Bishops Way, Ste. 163
TEL: (414) 784-3480
FAX: (414) 784-8207

Milwaukee (53214)
Marsh Electronics, Inc.
1563 South 101st Street
TEL: (414) 475-6000
FAX: (414) 771-2847

New Berlin (53146)
Hamilton Hallmark
2440 S. 179th Street
TEL: (414) 780-7200
FAX: (414) 780-7201

Waukesha (53186)
Bell Industries
W. 226 N. 900 Eastmound Drive
TEL: (414) 547-8879
(800) 525-6666
FAX: (414) 547-6547

Waukesha (53186)
Future Electronics Corp.
20875 Crossroads Cir., Ste. 200
TEL: (414) 786-1884
FAX: (414) 786-0744

Waukesha (53186)
Marshall Industries
20900 Swenson Drive, Ste. 150
TEL: (414) 797-8400
FAX: (414) 797-8270

Canadian Distributors

Alberta

Calgary (T1Y 6B5)
Future Electronics Corp.
3833-29th Street N.E.
TEL: (403) 250-5550
FAX: (403) 291-7054

Edmonton (T6E 5N9)
Future Electronics Corp.
4606 97th Street
TEL: (403) 438-2858
FAX: (403) 434-0812

British Columbia

Burnaby (V5A 4N6)
Hamilton Hallmark – #45
8610 Commerce Ct.
TEL: (604) 437-6667
FAX: (604) 294-1206

Vancouver (V5K 4X7)
Future Electronics
1695 Boundary Road
TEL: (604) 294-1166
FAX: (604) 294-1206

Manitoba

Winnipeg (R3H 0N8)
Future Electronics Corp.
106 King Edward Court
TEL: (204) 786-7711
FAX: (204) 783-8133

Ontario

Brampton (L6O 5G3)
Marshall Industries
4 Paget – Unit 10–11
TEL: (416) 458-8046
FAX: (416) 458-1613

Mississauga (L4V 1W5)
Future Electronics Corp.
5935 Airport Road, Ste.200
TEL: (416) 612-9200
FAX: (416) 612-9185

Mississauga (L5T 2L1)
Hamilton Hallmark – #59
151 Superior Blvd.
TEL: (416) 564-6060
FAX: (416) 564-6033

Canadian Distributors

Ontario (Cont'd)

Mississauga (L4V 1X5)
Marshall Industries
6285 Northam Drive, Ste. 112
TEL: (905) 612-1771
FAX: (905) 612-1988

Ottawa (K2C 3P2)
Future Electronics
Baxter Centre
1050 Baxter Road
TEL: (613) 820-8313
FAX: (613) 820-3271

Quebec

Pointe Claire (H9R 5C7)
Future Electronics
237 Hymus Boulevard
TEL: (514) 694-7710
TLX: 05-823599
FAX: (514) 695-3707

Pointe Claire (H9R 5P7)
Marshall Industries
148 Brunswick Blvd.
TEL: (514) 694-8142
FAX: (514) 694-6989

Quebec (G2E 5G5)
Future Electronics Corp.
1000 Avenue St. Jean-Baptiste,
Ste. 100
TEL: (418) 877-6666
FAX: (418) 877-6671

Saint Laurent (H4S 1P8)
Hamilton Hallmark – #65
2795 Rue Halpern
TEL: (514) 335-1000
TLX: (610) 421-3731
FAX: (514) 335-2381

Ville St. Laurent (H4T 1V6)
Hamilton/Hallmark
7575 Transcanada Highway, Ste. 600
TEL: (514) 335-1000
FAX: (514) 335-2481

European Sales/Representatives/Distributors

Austria

Bacher Electronics
Eitnergasse 6
1223 Wien
TEL: (43) 0222 81602215
TLX: 131532
FAX: (43) 0222 863211201

EBV Elektronik
Diefenbachgasse35/6
1150 Wien
TEL: (43) 0222 8941774
FAX: (43) 0222 8941775

Belgium

Diode
Keiberg II
Minervastraat, 14/B2
1930 Zaventem
TEL: (32) 2 7254660
FAX: (32) 2 7254511

EBV Elektronik
Excelsiorlaan 35
1930 Zaventem
TEL: (32) 02 7209936
FAX: (32) 02 7208152

Sonetech CY
Limburg Styrun, 243
B–1810 Wemmel
TEL: (32) 2 4600707
FAX: (32) 2 4601200

Denmark

Farnell Electronic Services
Naverland 29
DK-2600 Glostrup
TEL: (45) 42 456645
FAX: (45) 42 457624

TEMIC
AEG Dansk Aktieselskab
Roskildevej 8–10
DK–2620 Albertslund
TEL: (45) 42 648522
FAX: (45) 43 626228

Finland

Tahinik OY
P.O. Box 125
Magistratsportti 4A
FIN-00241 Helsinki
TEL: (358) 0 1482177
FAX: (358) 0 1482189

Farnell Electronic Services
P.O. Box 25 TyÖpajakatu 5
FIN-00581 Helsinki
TEL: (358) 0-739100
FAX: (358) 0-7015683

France

Arrow Electronique
73–79 Rue des Solets
Silic 585
94663 Rungis
TEL: (33) 1 49-78-49-78
FAX: (33) 1 49-78-05-96

EBV Elektronik
16, rue de Galilee
77436 CHAMPS SUR MARNE
TEL: (33) 1 64-68-86-00
FAX: (33) 1 64-68-27-67

Farnell Electronic Services
16 Avenue des Andes
BP 16
91941 Les Ulis Cedex A
TEL: (33) 1 64-46-02-00
TLX: 603351
FAX: (33) 1 64-46-95-95

SCAIB
80 Rue d'Arcueil
94523 Rungis Cedex
TEL: (33) 1 46-87-23-13
TLX: 20467F
FAX: (33) 1 45-60-55-49

TEMIC
3, Avenue du Centre
B.P. 309
78054 Saint-Quentin-en-Yvelines
TEL: (33) 1 30-60-70-00
FAX: (33) 1 30-64-06-93

Germany

Eurodis Enatechnik Electronics
Sickingenstrasse 1 – 10553 Berlin
TEL: (49) 30 3441043
FAX: (49) 30 3449544

Eurodis Enatechnik Electronics
Rheinstrasse 24 – 64283 Darmstadt
TEL: (49) 6151 17410
FAX: (49) 6151 174111

Eurodis Enatechnik Electronics
St. Petersburger Str. 15 – 01069
Dresden
TEL: (49) 351 4962400
FAX: (49) 351 4962401

Eurodis Enatechnik Electronics
Hildesheimer Str. 31 – 30169
Hannover
TEL: (49) 511 816038
FAX: (49) 511 816048

Eurodis Enatechnik Electronics
Henschelring 5 – 85551 Kirchheim
TEL: (49) 89 9049820
FAX: (49) 89 90498240

Eurodis Enatechnik Electronics
Max-Stromeier Str. 1 – 78467
Konstanz
TEL: (49) 7531 61048
FAX: (49) 7531 67260

Eurodis Enatechnik Electronics
Bucher Str. 100 – 90408 Nürnberg
TEL: (49) 911 34750
FAX: (49) 911 347530

Eurodis Enatechnik Electronics
Schillerstrasse 14 – 25451 Quickborn
TEL: (49) 4106 612277
FAX: (49) 4106 612281

Eurodis Enatechnik Electronics
Breitwiesenstrasse 25
70565 Stuttgart
TEL: (49) 711 7889770
FAX: (49) 711 7889744

CED Ditronic
Bernbacherstrasse 9
90768 Fürth
TEL: (49) 911 752216
FAX: (49) 911 7520064

CED Ditronic
Laatzener Str. 19
TEL: (49) 0511 87640
FAX: (49) 0511 8764160

CED Ditronic
Benzstrasse 1 B
85551 Kirchheim
TEL: (49) 089 9038551
FAX: (49) 089 9030944

CED Ditronic
Julius-Hölder Str. 42
70597 Stuttgart
TEL: (49) 0711 720010
FAX: (49) 0711 7289780

EBV
Behaimst. 3 D-10585 Berlin
TEL: (49) 030 3421041
FAX: (49) 030 3419003

EBV Elektronik
In der Meineworth 21 – 30938
Burgwedel
TEL: (49) 5139 80870
FAX: (49) 5139 5199

EBV Elektronik
Schenckstrasse 99 – 60489 Frankfurt
99
TEL: (49) 069 785037
FAX: (49) 069 7894458

EBV Elektronik
Hans Pinsel Str. 4 – 88540 Haar
D–8013 Haar
TEL: (49) 089 460960
FAX: (49) 089 464488

EBV Elektronik
Matthias-Claudius Str. 2a
41564 Kaarst
TEL: (49) 02131 96770
FAX: (49) 02131 967730

EBV Elektronik
Böblinger Str. 13 – 71229 Leonberg
TEL: (49) 7152 300090
FAX: (49) 7152 75958

Farnell Electronic Services
Bahnhofstrasse 44 – 71696
Möglingen
TEL: (49) 07141 4870
FAX: (49) 07141 487210

Ing. Büro Rainer König
Königsberger Str. 16A – 12207
Berlin
TEL: (49) 30 7689090
FAX: (49) 30 7738363

Spoerle Electronic
Kackertstrasse 10
52072 Aachen
TEL: (49) 241 889690
FAX: (49) 241 8896923

Spoerle Electronic
Rudower Str. 27-29 – 12351 Berlin
TEL: (49) 30 606011
TLX: 186029
FAX: (49) 30 6014057

Spoerle Electronic
Höpfigheimer Strasse 5 – 74321
Bietigheim-Bissingen
TEL: (49) 7142 70030
FAX: (40) 7142 700360

Spoerle Electronic
Hildebrandstrasse 11 – 44319
Dortmund
TEL: (49) 231 218010
TLX: 822555
FAX: (49) 231 2180167

Spoerle Electronic
Im Gefierth 11a – 63303 Dreieich
TEL: (49) 6103 3040
TLX: 417983
FAX: (49) 6103 304201

Spoerle Electronic
Hans-Bunte Str. 2 – 79108 Freiburg
TEL: (49) 761 510450
TLX: 7721994
FAX: (49) 761 502233

Spoerle Electronic
Rodeweg 18 – 37081 Göttingen
TEL: (49) 551 9040
TLX: 96733
FAX: (49) 551 90446/48

Spoerle Electronic
Bereich Hamburg
Winsbergring 42
22525 Hamburg
TEL: (49) 40 85313450
TLX: 2164536
FAX: (49) 40 85313491

European Sales/Representatives/Distributors (Cont'd)

Germany (Cont'd)

Spoerle Electronic
Roscherstrasse 31 – 04105 Leipzig
TEL: (49) 341 5647201
FAX: (49) 341 5852087

Spoerle Electronic
Rathsbergstrasse 17
90411 Nurnberg
TEL: (49) 911 521560
FAX: (40) 911 5215635

Spoerle Electronic
Föhringer Allee 17 – 85774
Unterfohring
TEL: (49) 89 959990
FAX: (49) 89 9509999/97

TEMIC TELEFUNKEN
microelectronic
Theresienstrasse 2
D-74072 Heilbronn
Postfach 35 35
D-74025 Heilbronn
TEL: (49) 07131 67-0
FAX: (49) 07131 67-2100

Israel

Tritech Ltd.
4 Hayetzira St.
POB 2436
Ra'Anana 43100
TEL: (972) 9 917277
FAX: (972) 9 982616

Ireland

MEMEC Ireland Ltd.
Block H – Lock Quay
Clare Street – Limerick
Rep of Ireland
TEL: (353) 61 411 842
FAX: (353) 61 411 888

Italy

Avnet De Mico
Div. Della Avnet Adelsy Srl
V. Le Vittorio Veneto 8
20060 Cinisello B. Milano
TEL: (39) 2 953 43600
FAX: (39) 2 952 2227

Camel Electronica Srl
Via Degli Artigianelli 6
20159 Milan
TEL: (39) 2 668 02 788
FAX: (39) 2 668 02 919

EBV Elektronik Srl
Via C. Frova 34
20092 Cinisello B. Milano
TEL: (39) 2 660 17111
FAX: (39) 2 660 17020

Farnell Spa
V. Le Milanofiori E5
20094 Assago Milano
TEL: (39) 2 824 701
FAX: (39) 2 824 70278

Lasi Elettronica
Div. Della Silvestar Ltd. Spa
V. Le Fulvio Testi 280
20126 Milano
TEL: (39) 2 661 431
FAX: (39) 2 661 01385

TEMIC
Via Stephenson 94
20157 Milano
TEL: (39) 2 33 2121
FAX: (39) 2 33 212201

Netherlands

EBV
Planetenbaan 2
3606 AK Maarssenbroek
TEL: (31) 03465-62353
FAX: (31) 03465-64277

Diode Components BV
Postbus 7139
5605 JC Eindhoven
De Run 1120
5503 LA Veldhoven
TEL: (31) 040-545430
FAX: (31) 040-535540

Diode Composants BV
Coltbaan 17
3439 NG Nieuwege
TEL: (31) 3402 91234
FAX: (31) 3402 35924

Norway

Farnell Electronic Services
Nedre Kalbakkvei 88
N-1081 Oslo 10
TEL: (47) 22 321270
FAX: (47) 22 325120

Tahonic A/S
P.O. Box 140 – Kalbakken
Kakkelovnskroken 1
N-0902 Oslo 9
TEL: (47) 22 16 16 10
FAX: (47) 22 25 73 17

Portugal

Redis Logar
Rua Bernardo Lima
Nr. 27-1çIzda
1200 Lisbon
TEL: (351) 11-520101
FAX: (351) 11-520004

Spain

ADM Electronica S A.
28009 Madrid
TEL: (34) 1 5304121
FAX: (34) 1 5300164

EBV Elektronik Vertriebs
28049 Madrid
TEL: (34) 1 358 8608
FAX: (34) 1 358 8560

Redis Logar, S A.
28002 Madrid
TEL: (34) 1 413 9111
FAX: (34) 1 416 1971

TEMIC
Principe de Vergara, 112
Apartado 235
28002 Madrid
TEL: (34) 1 562 76 00
FAX: (34) 1 562 75 14

Sweden

Farnell Electronic Services
Ankdammsgatan 32
S-171 26 Solna
TEL: (46) 8 835150
FAX: (46) 8 271807

TEMIC Nordic A/S
Kavallerivägen 24, Rissne
P.O. Box 2042
17202 Sundbyberg, Sweden
TEL: (46) 8 733-0090
FAX: (46) 8 733-0558

TH's Elektronik AB
Arrendevagen 36
P.O. Box 3027
16303 Spanga
TEL: (46) 8 36 2970
FAX: (46) 8 761 3065

Switzerland

Abalec A.G.
Grabenstrasse 9
8952 Schlieren
TEL: 1-730-0455
FAX: 1-730-9801

EBV Elektronik
Vorstadstr. 37
8953 Dietikon
TEL: 1-7401090
FAX: 1-7415110

Fabrimex Distribution AG
Ein Unternehmen der Spoerle
Electronic
Cherstrasse 4
8152 Opfikon-Glattbrugg
TEL: (41) 1-874 6262
FAX: (41) 1-874 6200

Fabrimex Distribution AG
Ein Untrtnehmen der
Spoerle Electronic
8, rue des Pecheurs
1400 Yverdon-les-Bains
TEL: (41) 24-219222
FAX: (41) 24-218141

Turkey

ERDA Elektronik A.S.
San Ve Tic A.S.
Keskin Kalem Sokak 15
80300 Esentepi
Istanbul
TEL: (90) 1 144-21-68
FAX: (90) 127 50540

United Kingdom

Abacus Electronics Ltd.
Abacus House
Bone Lane
Newbury, Berks RG14 5SF
TEL: (44) 0 635-36 222
TLX: 847589
FAX: (44) 0 635-38670

Abacus Electronics Limited
Abacus House
Bone Lane
Newbury, Berks RG14 5SF
TEL: (44) 0 635-36222
FAX: (44) 0 635-38670

Abercorn Electronics Ltd.
Pardovan
Philip, Linlithgow EH49 6QZ
TEL: (44) 506 834 222
TLX: 77994
FAX: (44) 506 834 554

BCD Microelectronics Ltd
3 Station Road
Swaffham Bulbeck,
Cambridge CB5 0NB
TEL: (44) 0223 812598
FAX: (44) 0223 812686

Future Electronics
Poyle Road – Colnbrook
Berkshire SL3 0E2
TEL: (44) 0753 687 000
FAX: (44) 0753 689 100

HB Electronics Ltd.
Lever Street – Bolton
Lancs BL3 6BJ
TEL: (44) 204 255 44
TLX: 63478
FAX: (44) 204 384911

Macro-Marketing Ltd.
Burnham Lane
Slough, Berkshire SL1 6LN
TEL: (44) 0628 604422
TLX: 847945
FAX: (44) 0628 666873

Micromark
159 Boyn Valley Road
Maidenhead
Berkshire SL6 4DT
TEL: (44) 0628 76176
FAX: (44) 0628 783799

TEMIC UK Ltd.
Easthampstead Road
Bracknell
Berkshire RG12 1LX
TEL: (44) 344 485757
FAX: (44) 344 427371

Asia Pacific and Rest of the World

Argentina

YEL S.R.L.
Virrey Cevallos 143
1077 Buenos Aires
TEL: (54) 1 40-1025, (54) 1 45-7140,
(54) 1 45-7163
FAX: (54) 1 440-1533, (54) 1 45-2551

Australia

IRH Components
1-5 Carter Street
Lidcombe NWS 2141
Australia
TEL: (61) 2-364-1766
FAX: (61) 2-647-1545 (no charge)

Brazil

Intectra
2629 Terminal Blvd.
Mt. View, CA 94043
TEL: (415) 967-8818
TLX: 345545
FAX: (415) 967-8836

UNIÃO Digital
R. Georgia, 69
CEP 04559-010
Sao Paulo SP Brazil
TEL: (55) 11 533-0967
TEL: (55) 11 241-8052
FAX: (55) 11 533-6780

Asia Pacific and Rest of the World (Cont'd)

Hong Kong

TEMIC Hong Kong Limited
Suite 1701, World Finance Centre
South Tower, Harbour City
17 Canton Road, Tsimshatsui
Kowloon
TEL: (852) 3789 789
FAX: (852) 3755 733

India

Amspec (S) Pte Ltd
213 Henderson Road
#01-07 Henderson Industrial Park
Singapore 0315
TEL: (65) 2710016
FAX: (65) 2714112

Blue Star Ltd.
Sahas 414/2 Veer
Savarkar Marg
Prabhadevi, Bombay 400025
TEL: (91) 224 306155
FAX: (91) 224 307078

Israel

Tritech
4, Hayetzira Street
Ind. Zone – POB 2436
RA'ANANA 43100
TEL: (972) 9 917 277
FAX: (972) 9 982 616

Japan

Ryoden Trading Co., Ltd.
3-15-15 Higashi-Ikebukuro
Toshima-ku, Tokyo 170
TEL: (81) 3-5396-6233
FAX: (81) 3-5396-6443

TEMIC Japan K.K.
Roppongi First Bldg. 17F
1-9-9 Roppongi
Minato-Ku, Tokyo 106
TEL: (81) 3-5562-3321
FAX: (81) 3-5562-3316

Toko, Inc.
1-17 Higashi-Yukigaya 2-Chome
Ohta-ku, Tokyo 145
TEL: (81) 3-3727-1166
FAX: (81) 3-3727-1179

TOMEN Electronics Corp.
1-1 Uchisaiwaicho 2 Chome
Chiyoda-Ku, Tokyo 100
TEL Tokyo: (81) 3-3506-3690
FAX Tokyo: (81) 3-3506-3497

Korea

Changnam Electronics Ltd.
Rm. 903, Hosung Bldg.
#44-22, Yoido-Dong
Youngdeungpo-Ku
Seoul
TEL: (82) 2-7820412
FAX: (82) 2-7853643

Malaysia

Scan Components (M) Sdn. Bhd.
761-B, Jalan Sultan Azlan Shah
11900 Sungai Nibong
Penang
TEL: (60) 4-835136
FAX: (60) 4-836320

Mexico

TEMIC Mexicana
c/o AEG Mexicana S.A. de C.V.
Paseo De La Reforma
35-20
Col Jabacalera
06030 DF.
TEL: (52) 5-546-92-76
FAX: (52) 5-566-08-400

Arlington (76006)
Ion Associates Inc.
2221 E. Lamar, Ste. 250
TEL: (817) 695-8000
FAX: (817) 695-8010

Puerto Rico

MEC/Caribe
P.O. Box 5038
Caguas 00726
TEL: (809) 746-9897
FAX: (809) 746-9441

Singapore

TEMIC
AEG Building
25 Tampines Street 92, #02-00
1852
TEL: (65) 788-6668
FAX: (65) 788-3383
Sales FAX: (65) 788-0031

QuadRep Marketing (S) Pte. Ltd
1 Marine Parade Central
#12-05 Parkway Builders' Centre
1544
TEL: (65) 3461933
FAX: (65) 3461911

Scan Technology (S) Pte Ltd
50 Kallang Bahru #04-01/03
Kallang Basin Industrial Estate
1233
TEL: (65) 2942112
FAX: (65) 2961685

South Africa

Electrolink (PTY) Ltd.
P.O. Box 1020
Capetown
8000
Republic of South Africa
TEL: (27) 215350
FAX: (27) 4196256

Taiwan

TEMIC
6/F Room B, No. 297, Sec 2
Ho-Pin East Road
Taipei City, R.O.C.
TEL: (886) 2 755-6108
FAX: (886) 2 755-4777

Dynamar Taiwan Co. Ltd.
13F No. 186, Sec. 4
Nanking East Road
Taipei 10570, R.O.C.
TEL: (886) 2 5775670
FAX: (886) 2 5775867

Thailand

See Scan Technology, Singapore

Siliconix

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