Siliconix incorporated

Siliconix Data Book

FET

FET

DATA BOOK

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Small-Signal FET Data Book

Siliconix

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Introduction 1

Small Signal FET

Present Position:

Siliconix specializes in offering a broad product line of N and P Channel JFETs, N-Channel DMOS and N & P-Channel MOS products. Our packaging capabilities range from hermetically sealed metal cans, plastic TO-92 and surface mount packages to side braze type packages for switch arrays. These proucts are geared to offer design alternatives to our customers. We specialize in ultra low leakage, low noise, high gain/slew rate, low $R_{DS(on)}$, and high speed switching.

Future Product Plans:

Expanding the already broad FET product line will focus on the following new product areas:

- High current, high voltage current regulator
  I_F 10-100 mA
  $B_V \geq 100V$
- Series of depletion mode lateral DMOS devices for use in high gain amplification.
- Surface mount additions will include SOT143 (4 leaded SO package) and SO8 (8 leads).

Glossary of Terms and Abbreviations

Siliconix

1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e., V_G = Gate Voltage; or simply help define the symbol, i.e., t_f = Fall Time, t_r = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example: BV_{GSS} = Breakdown Voltage from gate to source with the drain shorted to the source.

b_{fg} = Common-Gate Forward Susceptance

b_{fs} = Common-Source Forward Susceptance

b_{igs} = Common-Gate Input Susceptance

b_{iss} = Common-Source Input Susceptance

b_{ogs} = Common-Gate Output Susceptance

b_{oss} = Common-Source Output Susceptance

b_{rg} = Common-Gate Reverse Susceptance

b_{rs} = Common-Source Reverse Susceptance

BV_{DG0} = Drain-Gate Breakdown Voltage with Source Open

BV_{DSS} = Drain-Source Breakdown Voltage with Gate Shorted

BV_{SDX} = Drain-Source Breakdown Voltage Tied to Reference Voltage

BV_{G1SS} = Gate 1-to-Source Breakdown Voltage with Gate Shorted

BV_{G2SS} = Gate 2-to-Source Breakdown Voltage with Gate Shorted

BV_{GSS} = Gate-Source Breakdown Voltage with Gate Shorted

BV_{SDS} = Source-Drain Breakdown Voltage with Gate Shorted

BV_{SGO} = Source-Gate Breakdown Voltage with Source Open

C_{db} = Drain-Body Capacitance

C_{dgo} = Drain-Gate Capacitance

C_{gb} = Gate-Body Capacitance

C_{gd} = Gate-Drain Capacitance

C_{gs} = Gate- Source Capacitance

C_{iss} = Common-Source Input Capacitance

C_{oss} = Common-Source Output Capacitance

C_{rss} = Common-Source Reverse Transfer Capacitance

C_{sb} = Source-Body Capacitance

C_{sd} = Source-Drain Capacitance

C_{sgo} = Source-Gate Capacitance

D = Drain

$\bar{e}_N$ = Equivalent Short-Circuit Input Noise Voltage

f_m = Figure of Merit

G = Gate

g_{fg} = Common-Gate Forward Transconductance

g_{fs} = Common-Source Forward Transconductance

g_{fso} = Common-Source Forward Transconductance @ $V_{GS} = 0$

g_{fs1}/g_{fs2} = Common-Source Forward Transconductance Ratio

g_{ig} = Common-Gate Input Conductance

g_{is} = Common-Source Input Conductance

g_{og} = Common- Gate Output Conductance

g_{os} = Common-Source Output Conductance

g_{oss} = Common-Source Output Conductance @ $V_{GS} = 0$

$g_{os1}-g_{os2}$ = Differential Output Conductance

Glossary of Terms and Abbreviations (Cont'd)

G_{pg} = Common-Gate Power Gain

G_{ps} = Common-Source Power Gain

$I_{D(off)}$ = Drain Cutoff Current

$I_{D(on)}$ = Drain ON Current

I_{DGO} = Drain-Gate Leakage

I_{DSS} = Saturation Drain Current with Gate Shorted

I_{DSS1}/I_{DSS2} = Saturation Drain Current Ratio

I_F = Forward Current

I_G = Gate Operating Current

I_{G1G2} = Gate-to-Gate Leakage Current

$|I_{G1}-I_{G2}|$ = Differential Gate Operating Currents

I_{GBS} = Gate-to-Body Leakage Current with Gate Shorted

$I_{G(f)}$ = Gate Forward Current

I_{GSS} = Gate Reverse Current with Gate Shorted

I_{G1SS} = Gate 1-to-Source Leakage Current with Gate Shorted

I_{G2SS} = Gate 2-to-Source Leakage Current with Gate Shorted

I_{G1SSR} = Gate 1-to-Source Reverse Leakage Current

I_{G2SSR} = Gate 2-to-Source Reverse Leakage Current

$\bar{i}_n$ = Equivalent Open-Circuit Noise Current

I_P = Pinch-Off Current

NF = Noise Figure

P_D = Continuous Power Dissipation

P_{OV} = Peak Operating Voltage

$r_{ds(on)}$ = Drain-Source ON Resistance

$r_{DS(on)}$ = Static Drain-Source ON Resistance

$Re\ (Y_{fg})$ = Common-Gate Forward Transconductance

$Re\ (Y_{fs})$ = Common-Source Forward Transconductance

$Re\ (Y_{ig})$ = Common-Gate Input Conductance

$Re\ (Y_{is})$ = Common-Gate Output Conductance

$Re\ (Y_{os})$ = Common-Source Output Conductance

$Re\ (Y_{rg})$ = Common-Gate Reverse Transconductance

$Re\ (Y_{rs})$ = Common-Source Reverse Transconductance

r_{GS} = Common-Source Input Resistance

S = Source

t_d = Delay Time

$t_{d(off)}$ = Turn-Off Delay Time

$t_{d(on)}$ = Turn-On Delay Time

t_f = Fall Time

T_j = Junction Temperature

t_{off} = Turn-Off Time

t_{on} = Turn-On Time

T_l = Lead Temperature

t_r = Rise Time

T_{stg} = Storage Temperature

V_B = Body Voltage

V_{BB} = Body Supply Voltage

V_D = Drain Voltage

V_{DD} = Drain Supply Voltage

$V_{DS(on)}$ = Drain-Source ON Voltage

V_G = Gate Voltage

V_{GG} = Gate Supply Voltage

V_{GS} = Gate-Source Voltage

$|V_{GS1}-V_{GS2}|$ = Differential Gate-Source Voltage

ΔV_{GS} = Differential Gate-Source Voltage

$\frac{\Delta|V_{gs1}-V_{gs2}|}{\Delta T}$ = Differential Gate-Source Voltage Change with Temperature

$V_{GS(f)}$ = Gate-Source Forward Voltage

$V_{GS(th)}$ = Gate Threshold Voltage

$V_{GS(off)}$ = Gate Source Cutoff Voltage

Glossary of Terms and Abbreviations (Cont'd)

$V_{G1S(off)}$ = Gate 1 to Source Cutoff Voltage

$V_{G2S(off)}$ = Gate 2 to Source Cutoff Voltage

V_S = Source Voltage

V_{SS} = Source Supply Voltage

Z_d = Dynamic Impedance

Z_k = Knee AC Impedance

θ_I = Current Temperature Coefficient

θ_{J-A} = Junction to Ambient Thermal Resistance

θ_{J-C} = Junction to Case Thermal Resistance

How to Use the Small-Signal FET Cross Reference

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N4391	N JFET	2N4391

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison.

Type and classification abbreviations are described as follows:

BF (JFET Plastic)
CR (Current Limited)
CRR (Current Limiter)
D (Dual)
DM N-Channel DMOS
DN (Dual N-Channel Metal Can)
DPAD (Dual Pico Ampere Diode)
FN (N-Channel Metal Can)
ENH (Enhancement-Mode Normally-Off)
JPAD (Plastic Pico Ampere Diode)
JR (Plastic High Voltage Diode)
N (N-Channel)
P (P-Channel)
PAD (Pico Ampere Diode)
SD (N-Channel DMOS)
SI (N-Channel FETs)
SST (JFET in SOT-23 Plastic Package
SOT-143
SOIC-8 Pin)

Small-Signal FET Cross Reference

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
1N5283	CL N JFET	CR022		
1N5284	CL N JFET	CR024		
1N5285	CL N JFET	CR027		
1N5286	CL N JFET	CR030		
1N5287	CL N JFET	CR033		
1N5288	CL N JFET	CR039		
1N5289	CL N JFET	CR043		
1N5290	CL N JFET	CR047		
1N5291	CL N JFET	CR056		
1N5292	CL N JFET	CR062		
1N5293	CL N JFET	CR068		
1N5294	CL N JFET	CR075		
1N5295	CL N JFET	CR082		
1N5296	CL N JFET	CR091		
1N5297	CL N JFET	CR100		
1N5298	CL N JFET	CR110		
1N5299	CL N JFET	CR120		
1N5300	CL N JFET	CR130		
1N5301	CL N JFET	CR140		
1N5302	CL N JFET	CR150		
1N5303	CL N JFET	CR160		
1N5304	CL N JFET	CR180		
1N5305	CL N JFET	CR200		
1N5306	CL N JFET	CR220		
1N5307	CL N JFET	CR240		
1N5308	CL N JFET	CR270		
1N5309	CL N JFET	CR300		
1N5310	CL N JFET	CR330		
1N5311	CL N JFET	CR360		
1N5312	CL N JFET	CR390		
1N5313	CL N JFET	CR430		
1N5314	CL N JFET	CR470		
2N3066	N JFET	2N4340		
2N3067	N JFET	2N4338		
2N3068	N JFET	2N4338		
2N3069	N JFET	2N4341		
2N3070	N JFET	2N4339		
2N3071	N JFET	2N4338		
2N3084	N JFET	2N4341		
2N3085	N JFET	2N4341		
2N3086	N JFET	2N4341		
2N3087	N JFET	2N4341		
2N3088	N JFET	2N4339		
2N3088A	N JFET	2N4339		
2N3089	N JFET	2N4339		
2N3089A	N JFET	2N4339		
2N3365	N JFET	2N4340		
2N3366	N JFET	2N4338		
2N3367	N JFET	2N4338		
2N3368	N JFET	2N4341		
2N3369	N JFET	2N4340		
2N3370	N JFET	2N4339		
2N3436	N JFET	2N4341		
2N3437	N JFET	2N4341		
2N3438	N JFET	2N4341		
2N3452	N JFET	2N4340		
2N3453	N JFET	2N4338		
2N3454	N JFET	2N4338		
2N3455	N JFET	2N4340		
2N3456	N JFET	2N4338		
2N3457	N JFET	2N4338		
2N3458	N JFET	2N4341		
2N3459	N JFET	2N4341		
2N3460	N JFET	2N4340		
2N3608	P MOS ENH	3N163		
2N3684	N JFET	2N4339		
2N3685	N JFET	2N4339		
2N3686	N JFET	2N4340		
2N3687	N JFET	2N4341		
2N3819	N JFET	2N3819		
2N3820	P JFET	J270		
2N3821	N JFET	2N3821		
2N3822	N JFET	2N3822		
2N3823	N JFET	2N3823		
2N3824	N JFET	2N3824		
2N3921	D N JFET	2N3921		
2N3922	D N JFET	2N3922		
2N3954	D N JFET	2N3954		
2N3954A	D N JFET	2N3954A		
2N3955	D N JFET	2N3955		
2N3955A	D N JFET	2N3955A		
2N3956	D N JFET	2N3956		
2N3957	D N JFET	2N3957		
2N3958	D N JFET	2N3958		
2N3967	N JFET	2N4221		
2N3967A	N JFET	2N4221		
2N3968	N JFET	2N4339		
2N3968A	N JFET	2N4339		
2N3969	N JFET	2N4339		
2N3970	N JFET	2N3970		
2N3971	N JFET	2N3971		
2N3972	N JFET	2N3972		
2N4084	D N JFET	2N4084		
2N4085	D N JFET	2N4085		
2N4091	N JFET	2N4091		
2N4091A	N JFET	2N4091		
2N4092	N JFET	2N4092		
2N4092A	N JFET	2N4092		
2N4093	N JFET	2N4093		
2N4093A	N JFET	2N4093		
2N4117	N JFET	2N4117		
2N4117A	N JFET	2N4117A		
2N4118	N JFET	2N4118		
2N4118A	N JFET	2N4118A		
2N4119	N JFET	2N4119		
2N4119A	N JFET	2N4119A		
2N4120	P MOS ENH	3N163		
2N4139	N JFET	2N3822		
2N4220	N JFET	2N4220		
2N4220A	N JFET	2N4220A		
2N4221	N JFET	2N4221		
2N4221A	N JFET	2N4221A		
2N4222	N JFET	2N4222		
2N4222A	N JFET	2N4222A		
2N4223	N JFET	2N4223		
2N4224	N JFET	2N4224		
2N4267	P MOS ENH	3N163		
2N4302	N JFET	PN4302-18		
2N4303	N JFET	PN4303-18		
2N4304	N JFET	PN4304-18		

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Small-Signal FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N4338	N JFET	2N4338		
2N4339	N JFET	2N4339		
2N4340	N JFET	2N4340		
2N4341	N JFET	2N4341		
2N4352	P MOS ENH	3N163		
2N4382	P JFET	2N5115		
2N4391	N JFET	2N4391		
2N4392	N JFET	2N4392		
2N4393	N JFET	2N4393		
2N4416	N JFET	2N4416		
2N4416A	N JFET	2N4416A		
2N4445	N JFET	2N5432		
2N4446	N JFET	2N5433		
2N4447	N JFET	2N5432		
2N4448	N JFET	2N5433		
2N4856	N JFET	2N4856		
2N4856A	NJFET	2N4856A		
2N4856JAN	N JFET	2N4856JAN		
2N4856JANTX	N JFET	2N4856JANTX		
2N4856JANTXV	N JFET	2N4856JANTXV		
2N4857	N JFET	2N4857		
2N4857A	N JFET	2N4857A		
2N4857JAN	N JFET	2N4857JAN		
2N4857JANTX	N JFET	2N4857JANTX		
2N4857JANTXV	N JFET	2N4857TANTXV		
2N4858	N JFET	2N4858		
2N4858A	N JFT	2N4858A		
2N4858JAN	N JFET	2N4858JAN		
2N4858JANTX	N JFET	2N4858JANTX		
2N4858JANTXV	N JFET	2N4858JANTXV		
2N4859	N JFET	2N4859		
2N4859A	N JFET	2N4859A		
2N4859JAN	N JFET	2N4859JAN		
2N4859JANTX	N JFET	2N4859JANTX		
2N4859JANTXV	N JFET	2N4859JANTXV		
2N4860	N JFET	2N4860		
2N4860A	N JFET	2N4860A		
2N4860JAN	N JFET	2N4860JAN		
2N4860JANTX	N JFET	2N4860JANTX		
2N4860JANTXV	N JFET	2N4860JANTXV		
2N4861	N JFET	2N4861		
2N4861A	N JFET	2N4861A		
2N4861JAN	N JFET	2N4861JAN		
2N4861JANTX	N JFET	2N4861JANTX		
2N4861JANTXV	N JFET	2N4861JANTXV		
2N4867	N JFET	2N4867		
2N4867A	N JFET	2N4867A		
2N4868	N JFET	2N4868		
2N4868A	N JFET	2N4868A		
2N4869	N JFET	2N4869		
2N4869A	N JFET	2N4869A		
2N4977	N JFET	2N5432		
2N4978	N JFET	2N5433		
2N4979	N JFET	2N5434		
2N5018	P JFET	2N5018		
2N5019	P JFET	2N5019		
2N5020	P JFET	2N3329		
2N5045	D N JFET	2N5045		
2N5046	D N JFET	2N5046		
2N5047	D N JFET	2N5047		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5103	N JFET	2N4416		
2N5104	N JFET	2N4416		
2N5105	N JFET	2N4416		
2N5114	P JFET	2N5114		
2N5115	P JFET	2N5115		
2N5116	P JFET	2N5116		
2N5158	N JFET	2N5434		
2N5159	N JFET	2N5433		
2N5196	D N JFET	2N5196		
2N5197	D N JFET	2N5197		
2N5198	DN JFET	2N5198		
2N5199	D N JFET	2N5199		
2N5245	N JFET	PN4416		
2N5246	N JFET	J305-18		
2N5247	N JFE	J304-18		
2N5248	N JFET	2N5486		
2N5257	N JFET	2N5457		
2N5258	N JFET	2N5458		
2N5259	N JFET	2N5459		
2N5358	N JFET	2N4340		
2N5359	N JFET	2N4340		
2N5360	N JFET	2N4339		
2N5361	N JFET	2N4339		
2N5362	N JFET	2N4339		
2N5363	N JFET	2N4222A		
2N5364	N JFET	2N4224		
2N5391	N JFET	2N4867A		
2N5392	N JFET	2N4868A		
2N5393	N JFET	2N4869A		
2N5394	N JFET	2N4869A		
2N5395	N JFET	2N4869A		
2N5396	N JFET	2N4869A		
2N5397	N JFET	J210		
2N5398	N JFET	U312		
2N5432	N JFET	2N5432		
2N5433	N JFET	2N5433		
2N5434	N JFET	2N5434		
2N5452	D N JFET	2N5452		
2N5453	D N JFET	2N5453		
2N5454	D N JFET	2N5454		
2N5457	N JFET	2N5457		
2N5458	N JFET	2N5458		
2N5459	N JFET	2N5459		
2N5460	P JFET	2N5460		
2N5461	P JFET	2N5461		
2N5462	P JFET	2N5462		
2N5463	P JFET	2N5463		
2N5464	P JFET	2N5464		
2N5465	P JFET	2N5465		
2N5484	N JFET	2N5484		
2N5485	N JFET	2N5485		
2N5486	N JFET	2N5486		
2N5515	D N JFET	2N5515		
2N5516	D N JFET	2N5516		
2N5517	D N JFET	2N5517		
2N5518	D N JFET	2N5518		
2N5519	D N JFET	2N5519		
2N5520	D N JFET	2N5520		
2N5521	D N JFET	2N5521		
2N5522	D N JFET	2N5522		

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Small-Signal FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5523	D N JFET	2N5523		
2N5524	D N JFET	2N5524		
2N5545	D N JFET	2N5545		
2N5546	D N JFET	2N5546		
2N5547	D N JFET	2N5547		
2N5549	N JFET	2N4392		
2N5561	D N JFET	U401		
2N5562	D N JFET	U402		
2N5563	D N JFET	U404		
2N5564	D N JFET	2N5564		
2N5565	D N JFET	2N5565		
2N5566	D N JFET	2N5566		
2N5592	N JFET	2N3822		
2N5593	N JFET	2N3822		
2N5594	N JFET	2N3822		
2N5638	N JFET	2N5638		
2N5639	N JFET	2N5639		
2N5640	N JFET	2N5640		
2N5647	N JFET	2N4117A		
2N5648	N JFET	2N4117A		
2N5649	N JFET	2N4117A		
2N5801	N JFET	2N4393		
2N5802	N JFET	2N4393		
2N5803	N JFET	2N4392		
2N5902	D N JFET	U421		
2N5903	D N JFET	U422		
2N5904	D N JFET	U423		
2N5905	D N JFET	U421		
2N5906	D N JFET	U422		
2N5907	D N JFET	U423		
2N5908	D N JFET	U423		
2N5909	D N JFET	U423		
2N5911	D N JFET	2N5911		
2N5912	D N JFET	2N5912		
2N5949	N JFET	PN4416		
2N5950	N JFET	PN4416		
2N5951	N JFET	PN4416		
2N5952	N JFET	J305		
2N5953	N JFET	J305		
2N6451	N JFET	2N4393		
2N6452	N JFET	2N4393		
2N6453	N JFET	2N4393		
2N6454	N JFET	2N4393		
2N6483	D N JFET	U401		
2N6484	D N JFET	U402		
2N6585	D N JFET	U404		
2N6568	N JFET	U290		
2N6656	V MOS N ENH	2N6656		
2N6657	V MOS N ENH	2N6657		
2N6658	V MOS N ENH	2N6658		
2N6659	V MOS N ENH	2N6659		
2N6660	V MOS N ENH	2N6660		
2N6661	V MOS N ENH	2N6661		
2N6905	D N JFET	2N6905		
2N6906	D N JFET	2N6906		
2N6907	D N JFET	2N6907		
2N6908	N JFET	2N6908		
2N6909	N JFET	2N6909		
2N6910	N JFET	2N6910		
2N6911	N JFET	2N6911		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
3N145	P MOS ENH	3N163		
3N146	P MOS ENH	3N163		
3N155	P MOS ENH	3N163		
3N155A	P MOS ENH	3N163		
3N156	P MOS ENH	3N163		
3N156A	P MOS ENH	3N163		
3N157	P MOS ENH	3N163		
3N157A	P MOS ENH	3N163		
3N158	P MOS ENH	3N163		
3N158A	P MOS ENH	3N163		
3N163	P MOS ENH	3N163		
3N164	P MOS ENH	3N164		
3N174	P MOS ENH	3N163		
14T	N JFET	2N3819		
142T	N JFET	PN4392		
158T	N JFET	PN4302		
159T	N JFET	PN4416		
100S	N JFET	PN4304		
102M	N JFET	2N5486		
102S	N JFET	PN4302		
103M	N JFET	2N5457		
103S	N JFET	2N5459		
104M	N JFET	2N5458		
105M	N JFET	2N5459		
105U	N JFET	2N4222		
106M	N JFET	2N5485		
107M	N JFET	2N5486		
110U	N JFET	2N4339		
115U	N JFET			
120U	N JFET	2N4340		
125U	N JFET	2N4339		
130U	N JFET	2N4341		
135U	N JFET	2N4339		
155U	N JFET	2N4416		
182S	N JFET	2N4391		
183S	N JFET	2N3823		
197S	N JFET	2N4338		
198S	N JFET	2N4340		
199S	N JFET	2N4341		
200S	N JFET	2N4392		
200U	N JFET	2N3824		
201S	N JFET	2N4391		
202S	N JFET	2N4392		
203S	N JFET	2N3821		
204S	N JFET	2N3821		
210U	N JFET	2N4416		
231S	D N JFET	2N3954		
232S	D N JFET	2N3955		
233S	D N JFET	2N3956		
234S	D N JFET	2N3957		
235S	D N JFET	2N3958		
241U	N JFET	2N4869		
250U	N JFET	2N4091		
251U	N JFET	2N4392		
703U	N JFET	2N4220		
704U	N JFET	2N4220		
705U	N JFET	2N4224		
707U	N JFET	2N4860		
714U	N JFET	2N3822		
734U	N JFET	2N4416		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
734EU	N JFET	PN4416		
751U	N JFET	2N4340		
752U	N JFET	2N4340		
753U	N JFET	2N4341		
754U	N JFET	2N4340		
755U	N JFET	2N4341		
756U	N JFET	2N4340		
1227A	N JFET	2N3822		
1278A	N JFET	2N3821		
1279A	N JFET	2N3821		
1280A	N JFET	2N4224		
1281A	N JFET	2N3822		
1282A	N JFET	2N4341		
1283A	N JFET	2N4340		
1284A	N JFET	2N4222		
1285A	N JFET	2N3821		
1286A	N JFET	2N4220		
1325A	N JFET	2N4222		
1714A	N JFET	2N4340		
2000M	N JFET	2N3823		
2001M	N JFET	2N3823		
2078A	D N JFET	2N3955		
2079A	D N JFET	2N3955		
2080A	D N JFET	2N5546		
2081A	D N JFET	2N5546		
2098A	D N JFET	2N5545		
2099A	D N JFET	2N5546		
2130U	D N JFET	2N5452		
2132U	D N JFET	2N3955		
2134U	D N JFET	2N3956		
2136U	D N JFET	2N3957		
2138U	D N JFET	2N3958		
2139U	D N JFET	2N3958		
2147U	D N JFET	2N3958		
2148U	D N JFET	2N3958		
2149U	D N JFET	2N3958		
A5T3821	N JFET	J305		
A5T3822	N JFET	J305		
A5T3823	N JFET	PN4416		
A5T3824	N JFET	J302-18		
A192	N JFET	2N4416		
AD830	D N JFET	U421		
AD831	D N JFET	U421		
AD832	D N JFET	U422		
AD833	D N JFET	U426		
AD833A	D N JFET	U423		
AD835	D N JFET	2N3921		
AD836	D N JFET	2N3921		
AD837	D N JFET	2N3922		
AD838	D N JFET	2N4085		
AD839	D N JFET	2N4085		
AD840	D N JFET	2N5196		
AD841	D N JFET	2N5197		
AD842	D N JFET	2N5199		
AD3954	D N JFET	2N3954		
AD3954A	D N JFET	2N3954A		
AD3955	D N JFET	2N3955		
AD3956	D N JFET	2N3956		
AD3957	D N JFET	2N3957		
AD3958	D N JFET	2N3958		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
BC264	N JFET	PN4304		
BC264A	N JFET	PN4302		
BC264B	N JFET	PN4304		
BC264C	N JFET	PN4304		
BC264D	N JFET	PN4416		
BF244A/B/C	N JFET	BF244A/B/C		
BF245A/B/C	D N JFET	BF245A/B/C		
BF410A	N JFET	J201		
BF410B	N JFET	J202		
BF410C	N JFET	J203		
BF410D	N JFET	J204		
BFQ10	N JFET	U401		
BFQ11	N JFET	U401		
BFQ12	N JFET	U402		
BFQ13	N JFET	U402		
BFQ14	N JFET	U403		
BFQ15	N JFET	U405		
BFQ16	N JFET	U405		
BFR30	N JFET	SST202		
BFR31	N JFET	SST202		
BFR45	N JFET	2N4416		
BFS21	N JFET	2N5199		
BFS21A	D N JFET	2N5199		
BFS67	N JFET	2N3821		
BFS68	N JFET	2N3823		
BFS68P	N JFET	PN4416		
BFS70	N JFET	2N3821		
BFS71	N JFET	2N3822		
BFS72	N JFET	2N3823		
BFS73	N JFET	2N3821		
BFS74	N JFET	2N4856		
BFS75	N JFET	2N4857		
BFS76	N JFET	2N4858		
BFS77	N JFET	2N4859		
BFS78	N JFET	2N4860		
BFS79	N JFET	2N4861		
BFS80	N JFET	2N4416A		
BFT46	N JFET	SST201		
BFW10	N JFET	2N3823		
BFW11	N JFET	2N3822		
BFW12	N JFET	2N4220		
BFW13	N JFET	2N4867		
BFW54	N JFET	2N3822		
BFW55	N JFET	2N3822		
BFW56	N JFET	2N4869		
BFW61	N JFET	2N4224		
BSD10	N MOS FETS	Si3000		
BSD12	N MOS FETS	Si3000		
BSD212	D N FET	SD212		
BSD213	D N FET	SD213		
BSD214	D N FET	SD214		
BSD215	D N FET	SD215		
BSR56	N JFET	SST4856		
BSR57	N JFET	SST4857		
BSR58	N JFET	SST4858		
BSS83	D N FET	SST213		
BSV22	N JFET	2N4416		
BSV78	N JFET	2N4856A		
BSV79	N JFET	2N4857A		
BSV80	N JFET	2N4858A		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
C413N	N JFET	2N5434		
C673	N JFET	2N4341		
C674	N JFET	2N4341		
C680	N JFET	2N4338		
C680A	N JFET	2N4338		
C681	N JFET	2N4338		
C681A	N JFET	2N4338		
C682	N JFET	2N4339		
C682A	N JFET	2N4339		
C683	N JFET	2N4339		
C683A	N JFET	2N4339		
C684	N JFET	2N4220		
C684A	N JFET	2N4220		
C685	N JFET	2N4220		
C685A	N JFET	2N4220		
C6690	N JFET	2N4341		
C6691	N JFET	2N4341		
C6692	N JFET	2N4340		
CM600	N JFET	2N4092		
CM601	N JFET	2N4091		
CM602	N JFET	2N4091		
CM603	N JFET	2N4091		
CM640	N JFET	2N4093		
CM641	N JFET	2N4093		
CM642	N JFET	2N4093		
CM643	N JFET	2N4092		
CM644	N JFET	2N4092		
CM645	N JFET	2N4092		
CM646	N JFET	2N4092		
CM647	N JFET	2N4091		
CM650	N JFET	2N5432		
CM651	N JFET	2N5433		
CM652	N JFET	2N5432		
CM653	N JFET	2N5433		
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP643	N JFET	2N5434		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP640	N JFET	U296		
CP643	N JFET	2N5434		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP640	N JFET	U296		
CP643	N JFET	2N5434		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
CR022 Thru CR530 Referenced Under 1N Series				
CRR0240-4300	CL N FET	CRR0240-4300		
DN5564-66	D N JFET	DN5564-66		
DN5567	D N JFET	DN5567		
DPAD1	D PAD N JFET	DPAD1		
DPAD2	D PAD N JFET	DPAD2		
DPAD5	D PAD N JFET	DPAD5		
DPAD10	D PAD N JFET	DPAD10		
DPAD20	D PAD N JFET	DPAD20		
DPAD50	D PAD N JFET	DPAD50		
DPAD100	D PAD N JFET	DPAD100		
DU4339	D N JFET	U235		
DU4340	D N JFET	U235		
E100	N JFET	J203-18		
E101	N JFET	J201-18		
E102	N JFET	J202-18		
E103	N JFET	J105-18		
E105	N JFET	J105-18		
E106	N JFET	J106-18		
E107	N JFET	J107-18		
E108	N JFET	J108-18		
E109	N JFET	J109-18		
E110	N JFET	J110-18		
E111	N JFET	J111-18		
E112	N JFET	J112-18		
E113	N JFET	J113-18		
E174	P JFET	J174-18		
E175	P JFET	J175-18		
E176	P JFET	J176-18		
E177	P JFET	J177-18		
E201	N JFET	J201-18		
E202	N JFET	J202-18		
E203	N JFET	J203-18		
E204	N JFET	J204-18		
E210	N JFET	J210		
E211	N JFET	J211		
E212	N JFET	J212		
E230	N JFET	J230-18		
E231	N JFET	J231-18		
E232	N JFET	J232-18		
E270	P JFET	J270-18		
E271	P JFET	J271-18		
E300	N JFET	J300		
E304	N JFET	J304		
E305	N JFET	J305		
E308	N JFET	J308		
E309	N JFET	J309		
E310	N JFET	J310		
E400	D N JFET	U410		
E401	D N JFET	U411		
E402	D N JFET	U410		
E410	D N JFET	U410		
E411	D N JFET	U411		
E412	D N JFET	U412		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
E413	D N JFET	U410		
E414	D N JFET	U411		
E415	D N JFET	U412		
E420	D N JFET	U440		
E421	D N JFET	U441		
E430	D N JFET	U430		
E431	D N JFET	U431		
E500	CL N JFET	J500		
E501	CL N JFET	J501		
E502	CL N JFET	J502		
E503	CL N JFET	J503		
E504	CL N JFET	J504		
E505	CL N JFET	J505		
E506	CL N JFET	J506		
E507	CL N JFET	J507		
E508	CL N JFET	J508		
E509	CL N JFET	J509		
E510	CL N JFET	J510		
E511	CL N JFET	J511		
EPAD50	DD N JFET	JPAD50		
EPAD100	DD N JFET	JPAD100		
EPAD200	DD N JFET	JPAD200		
EPAD500	DD N JFET	JPAD500		
ESM4091	N JFET	PN4091		
ESM4092	N JFET	PN4092		
ESM4093	N JFET	PN4093		
ESM4302	N JFET	PN4302		
ESM4303	N JFET	PN4303		
ESM4304	N JFET	PN4304		
FE100	N JFET	2N3821		
FE100A	N JFET	2N3821		
FE102	N JFET	2N4119		
FE102A	N JFET	2N4119		
FE104	N JFET	2N4118		
FE104A	N JFET	2N4118		
FE200	N JFET	2N3821		
FE202	N JFET	2N3821		
FE204	N JFET	2N3821		
FE300	N JFET	2N3822		
FE302	N JFET	2N3821		
FE304	N JFET	2N3821		
FE0654A	N JFET	2N5486		
FE0654B	N JFET	2N5485		
FE3819	N JFET	2N3819		
FE5457	N JFET	2N5457		
FE5458	N JFET	2N5458		
FE5459	N JFET	2N5459		
FE5484	N JFET	2N5484		
FE5485QN	N JFET	2N5485		
FE5486	N JFET	2N5486		
FM3954	D N JFET	2N3954		
FM3954A	D N JFET	2N3954A		
FM3955	D N JFET	2N3955		
FM3955A	D N JFET	2N3955A		
FM3956	D N JFET	2N3956		
FM3957	D N JFET	2N3957		
FM3958	D N JFET	2N3958		
FM4117	N JFET	FN4117		
FN4117A	N JFET	FN4117A		
FN4118	N JFET	FN4118		
FN4118A	N JFET	FN4118A		
FN4119	N JFET	FN4119		
FN4119A	N JFET	FN4119A		
FN4392	N JFET	FN4392		
FN4393	N JFET	FN4393		
FT0654A	N JFET	2N5486		
FT0654B	N JFET	2N5486		
FT0654C	N JFET	2N4221		
FT0654D	N JFET	2N4221		
FT704	P MOS ENH	3N163		
GET5457	N JFET	2N5457		
GET5458	N JFET	2N5458		
GET5459	N JFET	2N5459		
HDIG1030	P MOS ENH	3N163		
ID100	D PAD N JFET	DPAD1		
ID101	D PAD N JFET	DPAD10		
IMF3954	D N JFET	2N3954		
IMF3954A	D N JFET	2N3954A		
IMF3955	D N JFET	2N3955		
IMF3955A	D N JFET	2N3955A		
IMF3956	D N JFET	2N3956		
IMF3957	D N JFET	2N3957		
IMF3958	D N JFET	2N3958		
IMF6485	D N JFET	U405		
IT100	P JFET	2N5116		
IT101	P JFET	2N5114		
IT108	N JFET	2N5486		
IT109	N JFET	U310		
IT1700	P MOS ENH	3N163		
IT1702	P MOSENH	3N16		
ITE500	CL N JFET	J500		
ITE501	CL N JFET	J501		
ITE502	CL N JFET	J502		
ITE503	CL N JFET	J503		
ITE504	CL N JFET	J504		
ITE505	CL N JFET	J505		
ITE506	CL N JFET	J506		
ITE507	CL N JFET	J507		
ITE3066	N JFET	J202-18		
ITE3067	N JFET	J201-18		
ITE3068	N JFET	J201-18		
ITE4117	N JFET	2N4117		
ITE4118	N JFET	2N4118		
ITE4119	N JFET	2N4119		
ITE4338	N JFET	J201-18		
ITE4339	N JFET	J201-18		
ITE4340	N JFET	J202-18		
ITE4341	N JFET	J203-18		
ITE4391	N JFET	PN4391-18		
ITE4392	N JFET	PN4392-18		
ITE4393	N JFET	PN4393-18		
ITE4416	N JFET	PN4416		
ITE4867	N JFET	J230-18		
ITE4868	N JFET	J231-18		
ITE4869	N JFET	J232-18		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
J105	N JFET	J105		
J105-18	N JFET	J105-18		
J106	N JFET	J106		
J106-19	N JFET	J106-18		
J107	N JFET	J107		
J107-18	N JFET	J107-18		
J108	N JFET	J108		
J108-18	N JFET	J108-18		
J109	N JFET	J109		
J109-18	N JFET	J109-18		
J110	N JFET	J110		
J110-18	N JFET	J110-18		
J111	N JFET	J111		
J111-18	N JFET	J111-18		
J112	N JFET	J112		
J112-18	N JFET	J112-18		
J113	N JFET	J113		
J113-18	N JFET	J113-18		
J174	P JFET	J174		
J174-18	P JFET	J174-18		
J175	P JFET	J175		
J175-18	P JFET	J175-18		
J176	P JFET	J176		
J176-18	P JFET	J176-18		
J177	P JFET	J177		
J177-18	P JFET	J177-18		
J201	N JFET			
J201-18	N JFET			
J202	N JFET			
J202-18	N JFET			
J203	N JFET			
J203-18	N JFET			
J204	N JFET	J204		
J204-18	N JFET	J204-18		
J210	N JFET	J210		
J211	N JFET	J211		
J212	N JFET	J212		
J230	N JFET	J230		
J230-18	N JFET	J230-18		
J231	N JFET	J231		
J231-18	N JFET	J231-18		
J232	N JFET	J232		
J232-18	N JFET	J232-18		
J270	P JFET	J270		
J270-18	P JFET	J270-18		
J271	P JFET	J271		
J271-18	P JFET	J271-18		
J300	N JFET	J300		
J300A/B/C/D	N JFET	J300A/B/C/D		
J304	N JFET	J304		
J305	N JFET	J305		
J308	N JFET	J308		
J309	N JFET	J309		
J310	N JFET	J310		
J401	D N JFET	U401		
J402	D N JFET	U402		
J403	D N JFET	U403		
J9100	C L N FET	J552		
J1404	D N JFET	U404		
J1405	D N JFET	U405		
J1406	D N JFET	U406		
K210-18	N JFET	J210		
K211-18	N JFET	J211		
K212-18	N JFET	J212		
K300-18	N JFET	J210		
K304-18	N JFET	J304		
K305-18	N JFET	J305		
K308-18	N JFET	J308		
K309-18	N JFET	J309		
K310-18	N JFET	J310		
KE3684	N JFET	2N4341		
KE3685	N JFET	2N4340		
KE3686	N JFET	2N4339		
KE3687	N JFET	2N4338		
KE3823	N JFET	J304-18		
KE3970	N JFET	PN4391-18		
KE3971	N JFET	PN4392-18		
KE3972	N JFET	PN4393-18		
KE4091	N JFET	PN4391-18		
KE4092	N JFET	PN4392-18		
KE4093	N JFET	PN4393-18		
KE4220	N JFET	2N5457		
KE4221	N JFET	2N5457		
KE4222	N JFET	2N5459		
KE4223	N JFET	J304-18		
KE4224	N JFET	J304-18		
KE4391	N JFET	PN4391-18		
KE4392	N JFET	PN4392-18		
KE4393	N JFET	PN4393-18		
KE4416	N JFET	PN4416		
KE4856	N JFET	PN4391-18		
KE4857	N JFET	PN4392-18		
KE4858	N JFET	PN4393-18		
KE4859	N JFET	PN4391-18		
KE4860	N JFET	PN4392-18		
KE4861	N JFET	PN4393-18		
KE5103	N JFET	J305		
KE5104	N JFET	J304		
KE5105	N JFET	J306		
KK4416-18	N JFET	PN4416		
LDF603	N JFET	2N4221A		
LDF604	N JFET	2N4221A		
LDF605	N JFET	2N4221A		
M163	P MOS ENH	3N163		
M164	P MOS ENH	3N164		
MEM520	P MOS ENH	3N164		
MEM520C	P MOS ENH	3N164		
MEM561	P MOS ENH	3N163		
MEM561C	P MOS ENH	3N163		
MEM806	P MOS ENH	3N163		
MEM806A	P MOS ENH	3N163		
MFE823	P MOS ENH	MFE823		
MFE2000	N JFET	2N4416		
MFE2001	N JFET	2N4416		
MFE2004	N JFET	2N4093		
MFE2005	N JFET	2N4092		
MFE2006	N JFET	2N4091		
MFE2007	N JFET	2N4860		
MFE2008	N JFET	2N4859		
MFE2009	N JFET	2N4859		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
MFE2010	N JFET	2N5434		
MFE2011	N JFET	2N5433		
MFE2012	N JFET	2N5432		
MFE2093	N JFET	2N4338		
MFE2094	N JFET	2N4339		
MFE2095	N JFET	2N4540		
MK10	N JFET	2N4416		
MMBF310	N JFET	SST310		
MMBF4391	N JFET	SST113		
MMBF4392	N JFET	SST112		
MMBF4393	N JFET	SST111		
MMBF4416	N JFET	SST4416		
MMBF4860	N JFET	SST111/112		
MMBF5310	N JFET	SST310		
MMBF5457	N JFET	SST202		
MMBF5460	N JFET	SST5460		
MMBF5484	N JFET	SST202		
MMBF5484	N JFET	SST5484		
MMBF5486	N JFET	SST5486		
MMBFU310	N JFET	SST310		
MMF1	D N JFET	2N3921		
MMF2	D N JFET	2N3921		
MMF3	D N JFET	2N3921		
MMF4	D N JFET	2N3921		
MMF5	D N JFET	2N3921		
MMF6	D N JFET	2N3921		
MMT3823	N JFET	2N3823		
MPF102	N JFET	MPF102		
MPF103	N JFET	2N5457		
MPF104	N JFET	2N5458		
MPF105	N JFET	2N5459		
MPF106	N JFET	2N5485		
MPF107	N JFET	2N5486		
MPF108	N JFET	MPF108		
MPF109	N JFET	MPF109		
MPF111	N JFET	MPF111		
MPF112	N JFET	MPF112		
MPF256	N JFET	J309		
MPF820	N JFET	U310		
MPF970	P JFET	J174		
MPF971	P JFET	J176		
MPF4391	N JFET	PN4391-18		
MPF4392	N JFET	PN4392-18		
MPF4393	N JFET	PN4393-18		
NF500	N JFET	2N4416		
NF501	N JFET	2N4416		
NF506	N JFET	2N4416		
NF510	N JFET	2N4393		
NF511	N JFET	2N4393		
NF520	N JFET	2N4339		
NF521	N JFET	2N4339		
NF522	N JFET	2N4339		
NF523	N JFET	2N4340		
NF530	N JFET	2N4341		
NF531	N JFET	2N4339		
NF532	N JFET	2N4341		
NF533	N JFET	2N4339		
NF580	N JFET	2N5432		
NF581	N JFET	2N5432		
NF582	N JFET	2N5433		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
NF583	N JFET	2N5434		
NF584	N JFET	2N5433		
NF585	N JFET	2N4859		
NF4302	N JFET	2N4302		
NF4303	N JFET	2N4303		
NF4304	N JFET	2N4304		
NF4445	N JFET	2N5432		
NF4446	N JFET	2N5433		
NF4447	N JFET	2N5432		
NF4448	N JFET	2N5433		
NF5163	N JFET	2N5163		
NF5457	N JFET	2N5457		
FN5458	N JFET	2N5458		
NF5459	N JFET	2N5459		
NF5484	N JFET	2N5484		
NF5485	N JFET	2N5485		
NF5486	N JFET	2N5486		
NF5555	N JFET	2N5555		
NF5638	N JFET	2N5638		
NF5639	N JFET	2N5639		
NF5640	N JFET	2N5640		
NF5653	N JFET	2N5653		
NF5654	N JFET	2N5654		
PAD1	PAD N JFET	PAD1		
PAD2	PAD N JFET	PAD2		
PAD5	PAD N JFET	PAD5		
PAD10	PAD N JFET	PAD10		
PAD20	PAD N JFET	PAD20		
PAD50	PAD N JFET	PAD50		
PAD100	PAD N JFET	PAD100		
P1086	P JFET	P1086		
P1086-18	P JFET	P1086-18		
P1087	P JFET	P1087		
P1087-18	P JFET	P1087-18		
PN4091	N JFET	PN4091		
PN4092	N JFET	PN4092		
PN4093	N JFET	PN4093		
PN4117	N JFET	PN4117		
PN4117A	N JFET	PN4117A		
PN4118	N JFET	PN4118		
PN4118A	N JFET	PN4118A		
PN4119	N JFET	PN4119		
PN4119A	N JFET	PN4119A		
PN4120	N JFET	PN4120		
PN4120A	N JFET	PN4120A		
PN4302	N JFET	PN4302		
PN4302-18	N JFET	PN4302-18		
PN4303	N JFET	PN4303		
PN4303-18	N JFET	PN4303-18		
PN4304	N JFET	PN4304		
PN4304-18	N JFET	PN4304-18		
PN4391	N JFET	PN4391		
PN4391-18	N JFET	PN4391-18		
PN4392	N JFET	PN4392		
PN4392-18	N JFET	PN4392-18		
PN4393	N JFET	PN4393		
PN4393-18	N JFET	PN4393-18		
PN4416	N JFET	PN4416		
PN5163	N JFET	PN5163		
PF510	P JFET	2N5018		

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Small-Signal FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
PF511	P JFET	2N5014		
SD210DE	D N JFET	SD210DE		
SD211DE	D N JFET	SD211DE		
SD212DE	D N JFET	SD212DE		
SD213DE	D N JFET	SD213DE		
SD214DE	D N JFET	SD214DE		
SD215DE	D N JFET	SD215DE		
Si1000	N JFET	2N6908		
Si1010	N JFET	2N6909		
Si1020	N JFET	2N6910		
Si1100	N JFET	2N6911		
Si1800	JFET Array	Si1800		
Si2000	N JFET	Si2000		
SO4091	N JFET	SST4091		
SO4391	N JFET	SST4391		
SO4416	N JFET	SST4416		
SST111	N JFET	SST111		
SST112	N JFET	SST112		
SST113	N JFET	SST113		
SST174	P JFET	SST174		
SST175	P JFET	SST175		
SST176	P JFET	SST176		
SST177	P JFET	SST177		
SST201	N JFET	SST201		
SST202	N JFET	SST202		
SST203	N JFET	SST203		
SST204	N JFET	SST204		
SST211	N DMOS	SST211		
SST213	N DMOS	SST213		
SST215	N DMOS	SST215		
SST308	N JFET	SST308		
SST309	N JFET	SST309		
SST310	N JFET	SST310		
SST405	D N JFET	SST405		
SST406	D N JFET	SST406		
SST410	D N JFET	SST410		
SST411	D N JFET	SST411		
SST412	D N JFET	SST412		
SST4302	N JFET	SST4302		
SST4303	N JFET	SST4303		
SST4304	N JFET	SST4304		
SST4391	N JFET	SST4391		
SST4392	N JFET	SST4392		
SST4393	N JFET	SST4393		
SST4416	N JFET	SST4416		
SST4856	N JFET	SST4856		
SST4857	N JFET	SST4857		
SST4858	N JFET	SST4858		
SST4859	N JFET	SST4859		
SST4860	N JFET	SST4860		
SST5114	P JFET	SST5114		
SST5115	P JFET	SST5115		
SST5116	P JFET	SST5116		
SST5484	N JFET	SST5484		
SST5485	N JFET	SST5485		
SST5486	N JFET	SST5486		
SST5638	N JFET	SST5638		
SST5639	N JFET	SST5639		
SST5640	N JFET	SST5640		
SST6908	N JFET	SST6908		
SST6909	N JFET	SST6909		
SST6910	N JFET	SST6910		
SU2078	D N JFET	U425		
SU2079	D N JFET	U425		
SU2098	D N JFET	2N5197		
SU2098A	D N JFET	2N5197		
SU2098B	D N JFET	2N5196		
SU2099	D N JFET	2N5197		
SU2099A	D N JFET	2N5197		
SU2365	D N JFET	U401		
SU2365A	D N JFET	U401		
SU2366	D N JFET	U402		
SU2366A	D N JFET	U402		
SU2367	D N JFET	U403		
SU2367A	D N JFET	U403		
SU2368	D N JFET	U404		
SU2368A	D N JFET	U404		
SU2369	D N JFET	U405		
SU2369A	D N JFET	U405		
SU2410	D N JFET	U424		
SU2411	D N JFET	U425		
SU2412	D N JFET	U426		
TD5911	D N JFET	2N5911		
TD5911A	D N JFET	2N5911		
TD5912	D N JFET	2N5912		
TD5912A	D N JFET	2N5912		
TIS14	N JFET	2N4340		
TIS25	D N JFET	U401		
TIS26	D N JFET	U402		
TIS27	D N JFET	U404		
TIS41	N JFET	2N4859		
TIS58	N JFET	J305-18		
TIS59	N JFET	U1837		
TIS73	N JFET	PN4391-18		
TIS74	N JFET	PN4392-18		
TIS75	N JFET	PN4393-18		
TIS88	N JFET	2N5486		
TIXS41	N JFET	2N4859		
TIXS42	N JFET	PN4393-18		
TN4117	N JFET	2N4117		
TN4117A	N JFET	2N4117A		
TN4118	N JFET	2N4118		
TN4118A	N JFET	2N4118A		
TN4119	N JFET	2N4119		
TN4119A	N JFET	2N4119A		
TN4338	N JFET	2N4338		
TN4339	N JFET	2N4339		
TN4340	N JFET	2N4340		
TN4341	N JFET	2N4341		
TP5114	P JFET	2N5114		
TP5115	P JFET	2N5115		
TP5116	P JFET	2N5116		
U182	N JFET	2N4857		
U183	N JFET	2N3824		
U197	N JFET	2N4339		
U198	N JFET	2N4340		
U199	N JFET	2N4341		
U200	N JFET	U200		
U201	N JFET	U201		
U202	N JFET	U202		

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Small-Signal FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U221	N JFET	2N4391		
U222	N JFET	2N4391		
U231	D N JFET	U231		
U232	D N JFET	U232		
U233	D N JFET	U233		
U234	D N JFET	U234		
U235	D N JFET	U235		
U240	N JFET	2N5432		
U241	N JFET	2N5433		
U242	N JFET	2N5432		
U243	N JFET	2N5433		
U254	N JFET	2N4859		
U255	N JFET	2N4860		
U256	N JFET	2N4861		
U257	D N JFET	U257		
U273	N JFET	2N4118A		
U273A	N JFET	2N4118A		
U274	N JFET	2N4119A		
U274A	N JFET	2N4119A		
U275	N JFET	2N4119A		
U275A	N JFET	2N4119A		
U280	D N JFET	U231		
U281	D N JFET	U231		
U282	D N JFET	U232		
U283	D N JFET	U232		
U284	D N JFET	U233		
U285	D N JFET	U234		
U290	N JFET	U290		
U291	N JFET	U291		
U295	N JFET	U295		
U296	N JFET	U296		
U300	P JFET	2N5114		
U301	P JFET	2N5115		
U304	P JFET	U304		
U305	P JFET	U305		
U306	P JFET	U306		
U308	N JFET	U308		
U309	N JFET	U309		
U310	N JFET	U310		
U311	N JFET	U311		
U320	N JFET	U290		
U321	N JFET	U291		
U322	N JFET	U290		
U350	QUAD JFET	U350		
U401	D N JFET	U401		
U402	D N JFET	U402		
U403	D N JFET	U403		
U404	D N JFET	U404		
U405	D N JFET	U405		
U406	D N JFET	U406		
U410	D N JFET	U410		
U411	D N JFET	U411		
U412	D N JFET	U412		
U421	D N JFET	U421		
U422	D N JFET	U422		
U423	D N JFET	U423		
U424	D N JFET	U424		
U425	D N JFET	U425		
U426	D N JFET	U426		
U427	D N JFET	U427		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U428	D N JFET	U428		
U430	D N JFET	U430		
U431	D N JFET	U431		
U440	D N JFET	U440		
U441	D N JFET	U441		
U443	D N JFET	U443		
U444	D N JFET	U444		
U508	N JFET	CR030		
U1177	N JFET	2N4220A		
U1178	N JFET	2N3821		
U1179	N JFET	2N3821		
U1180	N JFET	2N4221A		
U1181	N JFET	2N4220A		
U1182	N JFET	2N3821		
U1277	N JFET	2N4339		
U1278	N JFET	2N4339		
U1279	N JFET	2N4340		
U1280	N JFET	2N4339		
U1281	N JFET	2N3822		
U1282	N JFET	2N4341		
U1283	N JFET	2N4340		
U1284	N JFET	2N4341		
U1285	N JFET	2N4220		
U1288	N JFET	2N4341		
U1287	N JFET	2N4092		
U1322	N JFET	2N4221A		
U1323	N JFET	2N4221A		
U1324	N JFET	2N4220A		
U1325	N JFET	2N4222		
U1420	N JFET	2N3821		
U1421	N JFET	2N3822		
U1422	N JFET	2N3822		
U1714	N JFET	2N4340		
U1637E	N JFET	U1837		
U1897	N JFET	U1897		
U1897-18	N JFET	U1897-18		
U1897E	N JFET	U1897-18		
U1898	N JFET	U1898		
U1898-18	N JFET	U1898-18		
U1898E	N JFET	U1898-18		
U1899	N JFET	U1899		
U1899-18	N JFET	U1899-18		
U1899E	N JFET	U1899-18		
U1994E	N JFET	U1994		
U2047E	N JFET	PN4416		
U3000	N JFET	2N4341		
U3001	N JFET	2N4339		
U3002	N JFET	2N1338		
U3011	N JFET	2N4340		
U3012	N JFET	2N4338		
UC20	N JFET	2N4341		
UC100	N JFET	2N4339		
UC110	N JFET	2N4339		
UC115	N JFET	2N4340		
UC120	N JFET	2N3686		
UC130	N JFET	2N4341		
UC155	N JFET	2N4416		
UC200	N JFET	2N3824		
UC201	N JFET	2N3824		
UC210	N JFET	2N4416		

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Small-Signal FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
UC220	N JFET	2N3822		
UC240	N JFET	2N4869		
UC241	N JFET	2N4869		
UC250	N JFET	2N4091		
UC251	N JFET	2N4392		
UC401	P JFET	2N5116		
UC450	P JFET	2N5114		
UC451	P JFET	2N5116		
UC588	N JFET	2N4417		
UC703	N JFET	2N4220		
UC704	N JFET	2N4220		
UC705	N JFET	2N4224		
UC707	N JFET	2N4860		
UC714	N JFET	2N3822		
UC714E	N JFET	J203-18		
UC734	N JFET	2N4416		
UC734E	N JFET	PN4416		
UC751	N JFET	2N4340		
UC752	N JFET	2N4340		
UC753	N JFET	2N4341		
UC754	N JFET	2N4340		
UC755	N JFET	2N4341		
UC756	N JFET	2N4340		
UC807	N JFET	2N4860		
UC1700	P MOS ENH	3N163		
UC1764	P MOS ENH	3N163		
UC2130	D N JFET	2N5452		
UC2132	D N JFET	2N3955		
UC2134	D N JFET	2N3966		
UC2136	D N JFET	2N3957		
UC2138	D N JFET	2N3958		
UC2139	D N JFET	2N3958		
UC2147	D N JFET	2N3958		
UC2148	D N JFET	2N3958		
UC2149	D N JFET	2N3958		
VCR2N	N JFET	VCR2N		
VCR3P	P JFET	VCR3P		
VCR4N	N JFET	VCR4N		
VCR5P	P JFET	VCR5P		
VCR6P	P JFET	2N5116		
VCR7N	N JFET	VCR7N		
VCR11N	N JFET	VCR11N		
WK5457	N JFET	2N5457		
WK5458	N JFET	2N5458		
WK5459	N JFET	2N5459		

Refer to the Small Signal FET Data Book

Refer to the Small Signal FET Data Book

FET Product Information

Siliconix FET products are divided into three basic categories:

- **Standard Products** — All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.

- **Examples of Modified Standard Products are:**

  Electrical Specials — Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

  Mechanical Specials — Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

  High Reliability Specials — Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

  In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** — Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 988-8000.

FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
BF	European Transistor Standard	
CR	Si Standard N-Channel Current Regulator	
CRR	Si Standard N-Channel Current Regulator	
DM		Si Special DMOS FET
DN		Si Dual N-Channel JFET
FN		Si N-Channel JFET
DPAD	Si Standard Dual JFET Diode	
J	Si Standard TO-92 Cased FET	Special TO-92 Cased FET
JR	Si Standard Current Limiter Diode TO-92 Cased FET	
JPAD	Si Standard JFET Diode	
PAD	Si Standard JFET Diode	
PF		Si P-Channel Special
PN		Si Standard TO-92 Cased FET
SD		Si Standard DMOS FET
SI		N-Channel JFET Circuit
SST		JFET in SOT-23 Plastic Package
U	Si Standard FET	
VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
2N		JEDEC-Registered Device
3N	JEDEC—Registered Device	

Suffix	
-05	Std TO-92 Pkg. Lead Formed to TO-5 Pin Circle
-18	Std TO-92 Pkg. with Center Lead Formed Toward Flat in TO-18 Pin Circle
-TR	Tape and Reel available on TO-92 FETs See Section #6 for tape & reel.

PROCESS OPTION MIL-STD 750 Method = –2 Contact Factory

Siliconix
Hi-Rel Capabilities

Hi-Rel Specials for Ultra-Reliability Requirements

Siliconix is poised to fulfill the most demanding needs for high-reliability small-signal FETs. The Company's dedicated Program Management can efficiently coordinate requirements for multiple customer locations/divisions. From scheduling and clearing orders to coordinating shipments, Siliconix has you covered.

When you place your hi-rel order with Siliconix, you can count on screening to military standards on all hermetically sealed parts—per customer specifications—at all manufacturing facilities.

Siliconix also offers Lockheed Monitored Line parts. This means on-line process monitoring by a resident team of reliability/quality engineers. With approval from the U.S. Air Force, this service can be used by any aerospace company and government agency.

Process Option Flow for Standard Devices

The process option flow chart shows the standard screening option provided by Siliconix for discrete FET transistors.

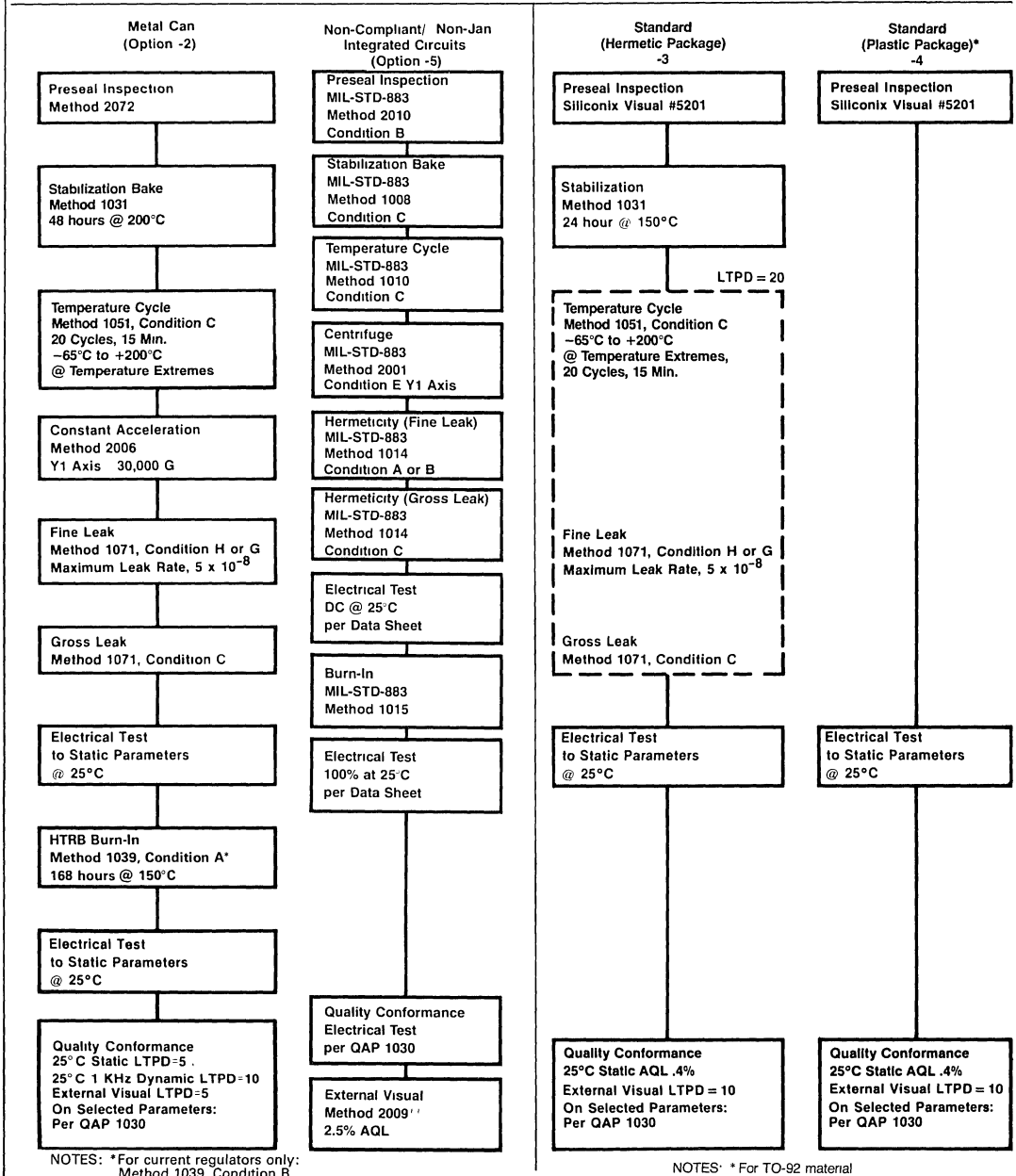
-2 and -5—Denotes the screening process for military temperature range parts including Group A sample at high, low and room temperatures.

-3—Is the screening for standard hermetic packages.

-4—Is the screening for standard plastic packages.

Siliconix offers the option, to our customers, of performing Group B & C as part of the purchase order. Requirements or submission of generic data in accordance with the reliability and quality manual generic family description.

FET Process Option Flow Chart



NOTES: *For current regulators only: Method 1039, Condition B 168 hours @ 125°C ±10% of rated power @ temp. with max V_F of 20% POV.

NOTES: * For TO-92 material burn-in is available. Contact sales or factory

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Small-Signal FETs Additional Product Options for European Customers

CECC 50 000

CECC 50 000 is a European system of continuous product assessment intended to produce electronic components of assessed quality to specifications and procedures which conform to internationally recognized standards. Components produced under the system are accepted by all participating countries without further testing being necessary.

At this time, member countries of the CECC are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Under this assessment scheme, devices are manufactured on an approved line to nationally approved specifications written in accordance with CECC rules. The manufacturer must comply with defined standards relating to organization, facilities and quality control procedures.

Specific device types are individually qualified against a fixed detail specification which has been approved by the British Standards Institute acting as the national supervising agency on behalf of CECC.

The CECC 50 000 scheme is administered in the UK by the BSI, and UK generated specifications are prefixed with the letters BS.

A number of popular standard device types are now qualified and the following detail specifications are available:

Type Number	BS Specification
2N3970/1/2	BS CECC 50012-001
2N4091/2/3	BS CECC 50012-002
2N4391/2/3	BS CECC 50012-004
2N4856/7/8	BS CECC 50012-005
2N4859/60/61	BS CECC 50012-005
2N4856A/7A/8A	BS CECC 50012-006
2N4859A/60A/61A	BS CECC 50012-006
2N3821/2	BS CECC 50012-007
2N3824	BS CECC 50012-008
2N4220/1/2	BS CECC 50012-009
2N4220/1A/2A	BS CECC 50012-009

Each of the approved types is now available with additional screening options, including high temperature reverse bias burn-in, of either 48, 72 or 168 hours duration. Screening details are appended to the detail specification and conform to appendix VI of the European Standard CECC 50 0000 ISSUE 3.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A sample inspection (lot by lot)
   quality assessment tests, assuring product conforms to electrical specification.
2. Group B sample inspection (lot by lot)
   reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.
3. Group C sample inspection (periodic—3 monthly)
   long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTRs (certified test records).

Manufacturing of BS CECC product is carried out at the Siliconix UK facility located in Morriston, Swansea SA6 6NE, South Wales

In addition to BS CECC approved product, the Siliconix UK facility can provide internationally recognized high-reliability screening options on standard products. These include Mil-750 and custom screening options.

JAN, JANTX or JANTXV processing for certain JEDEC-registered FETs can also be supplied.

For additional information and details of new/pending approvals inquiries may be directed to the nearest sales office.

Die Process Information

Siliconix is a large volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

Physical Data

- Physical layout and dimensions are presented in the die topography section.
- Each die is passivated with approximately 8,000 angstroms of non-crystalline glass.
- All die are gold backed. Gold backing is approximately 1,500 angstroms thick.
- Die metallization is deposited aluminum approximately 12,000 angstroms thick.
- Standard thickness 0.008 ± 0.002 in inches.

Die Screening Criteria

- **Probe Test Capability** — Siliconix performs three classes of electrical tests. The first category is a group of tests that may be performed on a 100 percent basis in wafer form. Examples are pinch-off voltage $V_{GS(off)}$ and breakdown voltage BV_{GSS}.

  A second group consists of tests such as very low leakage I_{GSS} where 100 percent testing is impractical, but sample testing may be performed. Generally, test time is the factor that renders these tests impractical on a 100 percent basis

  Finally, there are those tests that cannot be performed unless a sample group of units are assembled for evaluation. Capacitance and differential voltage drift are two examples (On request only).

  The adjacent table summarizes our wafer probe test capability and serves as a guide line to your design needs. Actual testing condition and procedure may vary. For specific parameters and test conditions, refer to the appropriate data sheet.

TEST PARAMETER	Condition Range			100% Wafer Sort Capability		Sample Wafer Sort Capability		Sample Test in Package Form	
				Limit Range		Limit Range		Limit Range	
	Cond.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
IGSS, IGSO, IOGD	VGS	0 01V	200V	100pA	10μA		0 5pA		0 5pA
IDSX, ISDX, IDSS, ISDS	VGS VDS	0 01V 0 01V	100V	100pA	100mA				
IG	ID VDG	10μA 0 01V	100mA 100V	100pA	10μA				
VGS(th), Vp, VGS	ID VDS	100pA 0 01V	100mA 100V	0 01V	100V				
BVGSS, BVGDD, BVGSO	IG	100pA	10μA	0 01V	200V				
BVDSX, BVSOX	ID	100pA	100mA	0 1V	100V				
VDS (on)	ID	10μA	100mA	1mV	10V				
rDS (on)	ID	10μA	100mA	1 ohm	10M ohm				
gfs (constant VGS)	VGS VDS	0 01V 0 01V	100V	10 μmho	100 mmho				
gfs (constant ID)	ID VDS	10μA 0 01V	100mA 100V	10 μmho	100 mmho				
$\overline{en}$ (constant VGS)	VGS VDS Freq	0 0 10 Hz	30V 100V 100 KHz					$\frac{3nv}{\sqrt{Hz}}$	$\frac{300\ nv}{\sqrt{Hz}}$
$\overline{en}$ (constant ID)	ID VDS Freq	1μA 0V 10 Hz	30 mA 100V 100 KHz					$\frac{3nv}{\sqrt{Hz}}$	$\frac{300\ nv}{\sqrt{Hz}}$
|VGS1 - VGS2|	VDG ID	0 01V 1μA	100V 10mA	0 1mV	100mV			20mV	
Capacitance high Frequency	VDS VGS ID	0V 0V 0A	100V 100V 100mA					0 1pF	1000pF
gfs1/gfs2 IDSS1/IDSS2 goss1-goss2 CMRR, Δ|Vgs1-VGS2|/ΔT	TESTS PERFORMED AFTER SAMPLE IS ASSEMBLED FOR EVALUATION								
QC Inspection				*0 65 AQL			1 5 AQL		1 5 AQL

* all in die form not after Customer Assembly

- **Visual Criteria** — Die are supplied with 100% visual sort to the criteria of MIL-STD-750 method 2072.

Die Process Information (Cont'd)

Assembly

- Chips supplied in waffle packs normally do not require cleaning. Wafers should be cleaned after sawing or scribing, and fracturing.
- Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides.
- When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases, handling precautions may be necessary for junction FET chips.
- Chips can be die attached either eutectically or by conductive epoxy when lower temperatures are necessary. Gold silicon eutectic occurs at temperatures between 385°C and 425°C.
- Bonding of wires from chip pads to posts can be achieved by thermocompression gold wire or ultrasonic aluminum wire bonded.

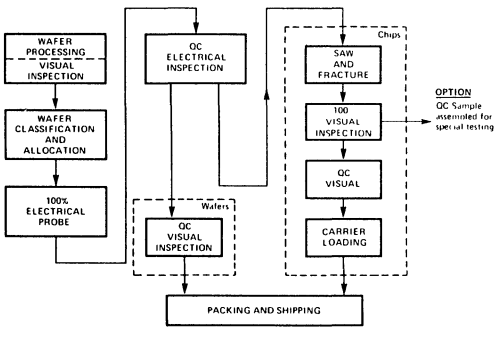
Options

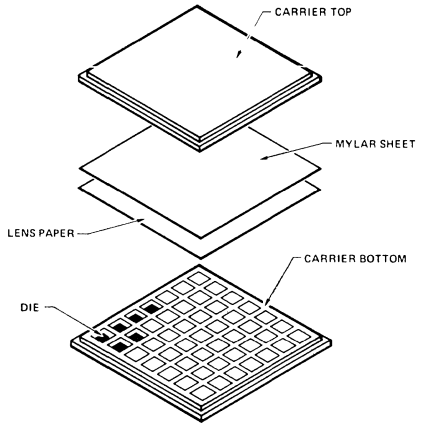
- **SEM** – Scanning electron microscope examination and control in accordance with MIL-STD-883 Method 2018 can be ordered on chips and wafers.
- **Wafer qualification to unprobed parameters** – sample testing of purchased chips to demonstrate capability to perform at data sheet temperature extremes by use of LTPD techniques can be provided.
- **Hot probe** – Siliconix has a chip processor/distributor with hot probe capability available.

Chip Packaging

- Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1 The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity
- Standard carrier 20 × 20 (400 die)—U.S.
  10 × 10 (100 die)—Europe only

Chip and Wafer Processing





NOTE CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

Ordering Information

- Identify standard part number and add CHP as suffix, i.e., 2N4416CHP for correct chip P/N.
- Special electrical selections available—contact local sales office.

Design Alternatives 2

Siliconix— The Source for FETs

This guide identifies the major tradeoffs of using a discrete approach vs. an IC. Most designers are familiar with biFET op amps, analog switches, diodes and current regulators. Siliconix offers performance alternatives that can enhance your overall circuit in achieving higher performance standards without compromises.

If you need subnano-second switching; very low noise at >> megohm input impedance; subpicoamp leakage; simple, two-leaded current sources and limiters; differential amplifiers with >> 100 volt/microsecond slewing while achieving picoamp input current; and protection diodes—Siliconix is the source.

Siliconix offers a wide variety of packages: the hermetically sealed metal can; plastic TO-92; surface-mount SOT-23, SOT-143, and SOIC; and also die/chip products. Our products include n- and p-channel JFETs, enhancement-mode MOSFETs, and n-channel enhancement-mode DMOS FETs – the broadest FET line in the world.

Siliconix has specialized in offering high-performance products for high-performance designs. Our specialty has been to fill the gap which exists between the best ICs available in the industry and discrete devices.

Siliconix began manufacturing small-signal Field Effects Transistors 20 years ago. Our emphasis has been, and will continue to be, ultrahigh-performance devices. Our product line is the broadest FET line in the world, and our commitment to this technology has never waivered. Our manufacturing capacity ensures timely delivery on even the large volume run-rates.

FETS
by Siliconix

2

Using JFETs as front end devices for Op Amps

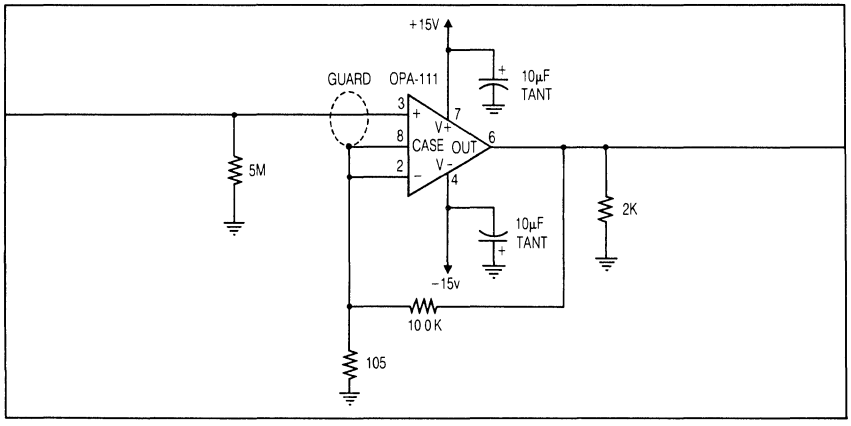
By using a low-leakage, low-noise and high-gain dual JFET with a relatively inexpensive, general-purpose biFET op amp, overall circuit performance is far superior than by using the best biFET op amp available. With present technology, the biFET-op amp approach has certain compromises – either on low-leakage, low noise or high gain (slew rates). One or two of these performance characteristics will be compromised with the biFET. By using a FET as a "front-end" device, all three can be achieved.

Check out the circuit performance:

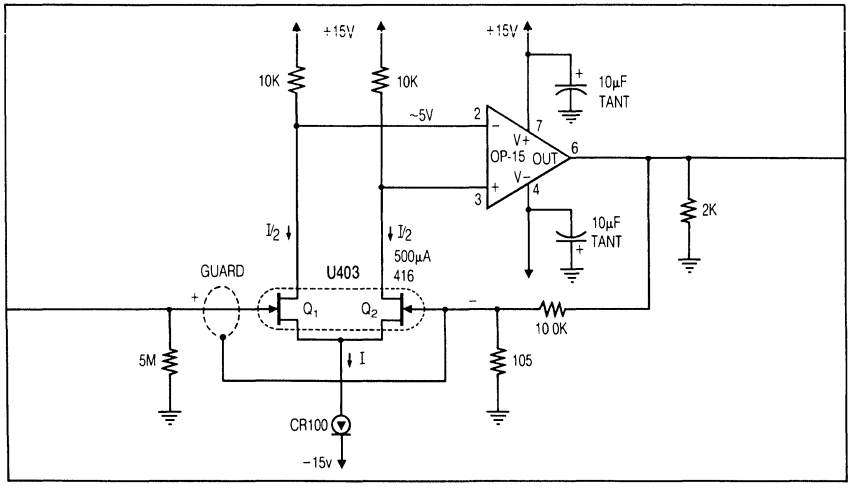
Overall Circuit Performance	Using OPA-111 Circuit	Using U403 with OP-15 Circuit
Noise (10 Hz)	33 nV/$\sqrt{Hz}$	20 nV/$\sqrt{Hz}$
Leakage	1 pA	1 pA
Slew Rate	2.9 V/μS	12 V/μS
Specific Device Performance Characteristics		
Low Noise (e_n)	< 10 nV/$\sqrt{Hz}$	U401-6, 2N6905-8, 2N5564-6
Low Leakage (I_G)	< 1 pA	U421-6
High Gain / (gfs)	> 7500 μmhos thru 450 MHz	2N5911-12
High Slew Rates	> 50 V/μS	2N5564-6

Compare Using JFETs as Front-End Devices

BiFET Op Amp



JFETs as Front-end Devices with a BiFET Op Amp



Using FETs as Analog Switches

JFETs and DMOS FETs offer flat ON-resistance, plus low ON-resistance in addition to ultrahigh-speed switching. Siliconix DMOS devices operate as high as 500 MHz.

Compare the discrete approach to the IC approach where performance makes the difference:

Device Technology	Switching time	$r_{DS(on)}$
Siliconix – DMOS		
SD210-15	1ns	45 ohms
SD5000-2		
CMOS		
CD4016	50 ns	50 ohms

FETs as Analog Switches Selector Guide

Device	Technology	Switching t (on)	$r_{DS(on)}$
SD210-15	DMOS	1 ns	45 ohms
SD5000	DMOS	1 ns	45 ohms
J111	JFET	7 ns	30 ohms
J112	JFET	7 ns	50 ohms
J113	JFET	7 ns	100 ohms
2N4391	JFET	15 ns	30 ohms
2N4392	JFET	15 ns	60 ohms
2N4393	JFET	15 ns	100 ohms
J105	JFET	15 ns	3 ohms
J106	JFET	15 ns	6 ohms
J107	JFET	15 ns	8 ohms
J108	JFET	4 ns	8 ohms
J109	JFET	4 ns	12 ohms
J110	JFET	4 ns	18 ohms

Using JFETs as Diodes

JFETs make ultralow-leakage diodes by using the gate and the drain of the device.

Compare traditional diodes to the Siliconix line of PAD – Pico Amp Diodes:

Device/ Technology	Switching Time (recovery time)	Capacitance	Breakdown Voltage	Leakage
1N914 (gold doped) 1N4148	2 ns	1.5 pF	75 V	7-10 nA
1N457 1N484	300 ns	1.5 pF	70 V	100 pA
JFETS PAD-1	250 ns	2 0 pF	45 V	1 pA
Bipolars as diodes (lowest leakage)	200 ns	3 0 pF	30-60 V	4-5 pA

If speed is critical, then the gold-doped diodes are the first choice If leakage is important – choose the Siliconix PAD-1 series

JFETs as low leakage Diode Selector Guide

Leakage I_R	Breakdown B_{VR} Reverse Breakdown Voltage	Capacitance c_R	Device Number	Type Package
1 pA	−45 V	0.8 pF	DPAD1*	Modified TO-78
2 pA	−45 V	0.8 pF	DPAD2*	Modified TO-71
5 pA	−45 V	0.8 pF	DPAD5*	Modified TO-71
10 pA	−35 V	2.0 pF	DPAD10*	Modified TO-71
20 pA	−35 V	2.0 pF	DPAD20*	Modified TO-71
50 pA	−35 V	2.0 pF	DPAD50*	Modified TO-71
100 pA	−35 V	2.0 pF	DPAD100*	Modified TO-71
5 pA	−35 V	2.0 pF	JPAD5	2-Leaded TO-92
10 pA	−35 V	2.0 pF	JPAD10	2-Leaded TO-92
20 pA	−35 V	2.0 pF	JPAD20	2-Leaded TO-92
50 pA	−35 V	2.0 pF	JPAD50	2-Leaded TO-92
100 pA	−35 V	2.0 pF	JPAD100	2-Leaded TO-92
200 pA	−35 V	2.0 pF	JPAD200	2-Leaded TO-92
500 pA	−35 V	2 0 pF	JPAD500	2-Leaded TO-92
1 pA	−45 V	0 8 pF	PAD1	3-Leaded TO-18
2 pA	−45 V	0 8 pF	PAD2	3-Leaded TO-18
5 pA	−45 V	0 8 pF	PAD5	3-Leaded TO-18
10 pA	−35 V	2.0 pF	PAD10	3-Leaded TO-18
20 pA	−35 V	2.0 pF	PAD20	3-Leaded TO-18
50 pA	−35 V	2 0 pF	PAD50	3-Leaded TO-18
100 pA	−35 V	2 0 pF	PAD100	3-Leaded TO-18

*D = Dual Diode

FETs as Current Regulators

Siliconix offers simple, two-leaded temperature-compensated current regulators. The inherent design of the JFET produces devices where the current is insensitive to temperature changes and with a temperature coefficient better than 30.00ppm per degree c. The breakdown voltage of the devices are rated at 100 V, and they provide excellent constant current down to 1-2 V. The devices are selected in the 10% ranges from 100 µA to 5.6 mA for use in precise instrumentation.

Current Regulator Selector Guide

Part Number	I_F(min)	TOLERANCE %	B_V	Package (all 2-leaded devices)
CR022	198 µA	10%	100 V	TO-18
CR024	216 µA	10%	100 V	TO-18
CR027	243 µA	10%	100 V	TO-18
CR030	270 µA	10%	100 V	TO-18
CR033	297 µA	10%	100 V	TO-18
CR039	351 µA	10%	100 V	TO-18
CR043	387 µA	10%	100 V	TO-18
CR047	423 µA	10%	100 V	TO-18
CR056	504 µA	10%	100 V	TO-18
CR062	558 µA	10%	100 V	TO-18
CR068	612 µA	10%	100 V	TO-18
CR075	675 µA	10%	100 V	TO-18
CR082	738 µA	10%	100 V	TO-18
CR091	819 µA	10%	100 V	TO-18
CR100	900 µA	10%	100 V	TO-18
CR110	990 µA	10%	100 V	TO-18
CR120	1.09 mA	10%	100 V	TO-18
CR130	1.17 mA	10%	100 V	TO-18
CR140	1.26 mA	10%	100 V	TO-18
CR150	1.35 mA	10%	100 V	TO-18
CR160	1.44 mA	10%	100 V	TO-18
CR180	1.62 mA	10%	100 V	TO-18
CR200	1 80 mA	10%	100 V	TO-18
CR220	1.98 mA	10%	100 V	TO-18
CR240	2.16 mA	10%	100 V	TO-18
CR270	2.43 mA	10%	100 V	TO-18
CR300	2.70 mA	10%	100 V	TO-18
CR330	2.97 mA	10%	100 V	TO-18
CR360	3.24 mA	10%	100 V	TO-18
CR390	3.51 mA	10%	100 V	TO-18
CR430	3.87 mA	10%	100 V	TO-18
CR470	4.23 mA	10%	100 V	TO-18
CR530	4.77 mA	10%	100 V	TO-18

Data Sheets 3

n-channel JFET
designed for . . .

- **General Purpose Amplifiers**
- **Analog Switching**

Siliconix

Performance Curves NH NRL
See Section 4

BENEFITS

- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

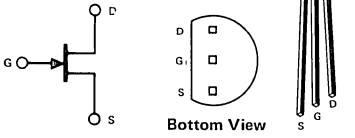
NOT RECOMMENDED FOR NEW DESIGNS.

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage ..... 25 V
Drain-Source Voltage ..... 25 V
Reverse Gate-Source Voltage ..... -25 V
Gate Current ..... 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) .....200 mW
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature
(1/16" from Case for 10 seconds) .....260°C

TO-92
See Section 6

Plastic



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		-2	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3					-2	μA		$T_A = 100°C$
4		I_{DSS}	Saturation Drain Current	2	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	
5		V_{GS}	Gate-Source Voltage	-0.5	-7.5	V	$V_{DS} = 15$ V, $I_D = 200\ \mu A$	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-8	V	$V_{DS} = 15$ V, $I_D = 2$ nA	
7	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transfer Admittance	2000	6500	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	f = 1 kHz
8		$\lvert y_{os} \rvert$	Common Source Output Admittance		50	μmho		
9		C_{iss}	Common Source Input Capacitance		8	pF	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 MHz
10		C_{rss}	Common Source Reverse Transfer Capacitance		4	pF		
11		$\lvert y_{fs} \rvert$	Common Source Forward Transfer Admittance	1600		μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 100 MHz

*JEDEC registered data

NH
NRL

NOTES:

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

n-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **Oscillators**

Siliconix

Performance Curves NRL
See Section 4

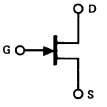
BENEFITS

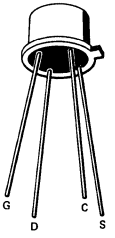
- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . –50 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3821 Min	2N3821 Max	2N3822 Min	2N3822 Max	2N3823 Min	2N3823 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.5	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1		-0.5	μA		150°C
3		BV_{GSS}	Gate Source Breakdown Voltage	-50		-50		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate Source Voltage	-0.5	-2						V_{DS} = 15 V, I_D = 50 μA	
						-1	-4				V_{DS} = 15 V, I_D = 200 μA	
								-1.0	-7.5		V_{DS} = 15 V, I_D = 400 μA	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	2.5	2	10	4	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 3)	1500	4500	3000	6500	3,500	6,500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common Source Forward Transadmittance	1500		3000		3,200				f = 100 MHz
9		g_{os}	Common Source Output Conductance (Note 3)		10		20		35			f = 1 kHz
10		C_{iss}	Common Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure		5		5		6	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
13		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		200		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

*JEDEC Registered Data. **NRL**

NOTES:
1 Due to symmetrical geometry, these units may be operated with source and drain leads interchanged
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3 These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFET *designed for . . .*

Siliconix

Performance Curves NRL
See Section 4

- **High Speed Commutators**
- **Choppers**

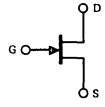
BENEFITS

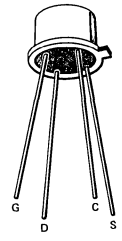
- Low Insertion Loss
  $r_{ds(on)} < 250\ \Omega$
- High Off-Isolation
  $I_{D(off)} < 0.1$ nA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . −50 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
2					−0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	I_G = −1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15 V, V_{GS} = −8 V	
					0.1	μA		150°C
5	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
6		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
7		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF	V_{GS} = −8 V, V_{DS} = 0	

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C

monolithic dual n-channel JFETs *designed for . . .*

■ Differential Amplifiers

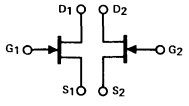
Siliconix

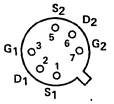
Performance Curves NNR
See Section 4

BENEFITS

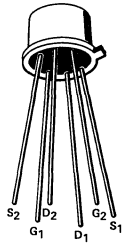
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 6





Bottom View



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C to 200°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1	μA		100°C
3		BV_{DGO}	Drain-Gate Breakdown Voltage	50			I_D = 1 μA, I_S = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3	V	V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-2.7		V_{DS} = 10 V, I_D = 100 μA	
6		I_G	Gate Operating Current		-250	pA	V_{DG} = 10 V, I_D = 700 μA	
7					-25	nA		100°C
8		I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35			
11		C_{iss}	Common-Source Input Capacitance		18	pF		
12		C_{rss}	Common-Source Reverse Transfer Capacitance		6			
13		g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10 V, I_D = 700 μA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		20			
15		NF	Spot Noise Figure		2	dB	V_{DS} = 10 V, V_{GS} 0	f = 1 kHz, R_G = 1 meg

		Characteristic		2N3921		2N3922		2N4084		2N4085		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCH	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		15		15	mV	V_{DG} = 10 V, I_D = 700 μA	T_A = 0°C, T_B = 100°C
17		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		10		25		10		25	μV/°C		
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data.

NNR

NOTES:
1. Pulse test duration = 2 ms.
2. Measured at end points, T_A and T_B.
3. Assumes smaller value in numerator.

monolithic dual n-channel JFETs *designed for . . .*

- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

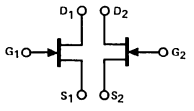
Siliconix

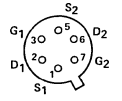
Performance Curves NQP
See Section 4

BENEFITS

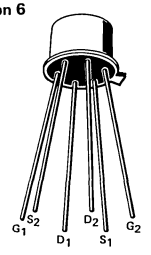
- High Accuracy & Stability
  Offset Less Than 5 mV (2N3954, 54A)
  Drift Less Than 5 μV/°C (2N3954A)
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Any Case-To-Lead Voltage . . . . . ±100 V
Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation at (Each Side) . . . . . .250 mW
85°C Case Temperature (Both Sides) . . . . . .500 mW
Power Derating (Each Side) . . . . . 2.86 mW/°C
(Both Sides) . . . . . 4.3 mW/°C
Storage Temperature Range . . . . . -65 to+200°C
Lead Temperature (1/16" from case for 10 seconds) . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3954		2N3954A		2N3955		2N3955A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100		-100	pA	V_{GS} = -30 V,	
2					-500		-500		-500		-500	nA	V_{DS} = 0	T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1 0	-4.5	-1.0	-4.5	-1.0	-4 5	-1.0	-4 5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2 0		2 0		2 0		V_{DS} = 0, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4 2		-4.2		-4 2		-4.2		V_{DS} = 20 V	I_D = 50 μA
7				-0 5	-4.0	-0 5	-4 0	-0.5	-4 0	-0.5	-4 0			I_D = 200 μA
8		I_G	Gate Operating Current		-50		-50		-50		-50	pA	V_{DS} = 20 V,	
9					-250		-250		-250		-250	nA	I_D = 200 μA	T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0 5	5 0	0 5	5 0	0 5	5 0	0 5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4 0		4 0		4.0		4 0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1 2		1 2		1 2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common Source Spot Noise Figure		0 5		0.5		0 5		0 5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA,	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0 95	1.0	0.95	1.0	0 95	1.0	–	V_{DS} = 20 V V_{GS} = 0	
20		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5 0		5.0		10.0		5.0	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		0 8		0.4		2.0		1.2			T = 25°C to -55°C
22					1.0		0.5		2.5		1.5			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0 97	1 0	0 97	1 0	0 97	1.0	0.95	1 0	–		f = 1 kHz

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NQP

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

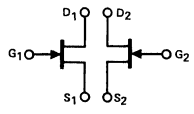
Performance Curves NQP
See Section 4

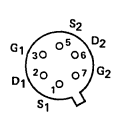
- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

BENEFITS

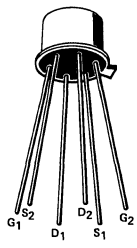
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

TO-71
See Section 6





Bottom View



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3956		2N3957		2N3958		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500		-500		-500	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1 0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		V_{DS} = 0 V, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		V_{DS} = 20 V, I_D = 50 μA	
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0		V_{DS} = 20 V, I_D = 200 μA	
8		I_G	Gate Operating Current		-50		-50		-50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					-250		-250		-250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4 0		4 0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Reverse Current		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	–	V_{DS} = 20 V, V_{GS} = 0	
20		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\lvert V_{GS1} - V_{GS2} \rvert$	Gate-Source Voltage Differential Change With Temperature		4.0		6.0		8.0			T = 25°C to -55°C
22					5.0		7.5		10.0			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.95	1 0	0.90	1.0	0.85	1.0	–		f = 1 kHz

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NQP

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Amplifiers**

Performance Curves NCB
See Section 4

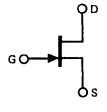
BENEFITS

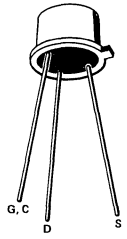
- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (2N3970)
- Good Off-Isolation
  $I_{D(off)} < 250$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
Derate Linearly at the Rate of 10 mW/°C . . . . . 1.8 W
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . .300°C

TO-18
See Section 6



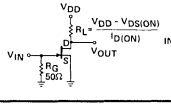


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	2N3970 Min	2N3970 Max	2N3971 Min	2N3971 Max	2N3972 Min	2N3972 Max	Unit	Test Conditions	
1		BV_{GSS} Gate Reverse Breakdown Voltage	–40		–40		–40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{DGO} Drain Reverse Current		250		250		250	pA	$V_{DG} = 20$ V, $I_S = 0$	
3				500		500		500	nA		150°C
4		$I_{D(off)}$ Drain Cutoff Current		250		250		250	pA	$V_{DS} = 20$ V, $V_{GS} = -12$ V	
5	STATIC			500		500		500	nA		150°C
6		$V_{GS(off)}$ Gate-Source Cutoff Voltage	–4	–10	–2	–5	–0.5	–3	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
7		I_{DSS} Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$ Drain-Source ON Voltage						2	V	$V_{GS} = 0$	$I_D = 5$ mA
9						1.5					$I_D = 10$ mA
10				1							$I_D = 20$ mA
11		$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
12		$r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13	DYN	C_{iss} Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance		6		6		6		$V_{DS} = 0$, $V_{GS} = -12$ V	
15		$t_{d(on)}$ Turn-On Delay Time		10		15		40		$V_{DD} = 10$ V, $V_{GS(on)} = 0$	
16	SW	t_r Rise Time		10		15		40	ns		
17		t_{off} Turn-Off Time		30		60		100			

	$I_{D(on)}$	R_L	$V_{GS(off)}$
2N3970	20 mA	450 Ω	–10 V
2N3971	10 mA	850 Ω	– 5 V
2N3972	5 mA	1.6KΩ	– 3 V

*JEDEC registered data.



NCB

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

3

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

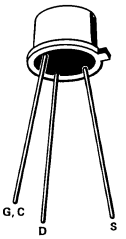
Siliconix

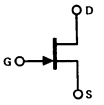
Performance Curves NCB
See Section 4

BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  $r_{DS(on)} < 30\ \Omega$ (2N4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (2N4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

TO-18
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-55 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

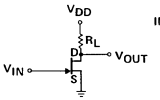
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4091		2N4092		2N4093		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$	
3					400		400		400	nA		150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V
5									400	nA		150°C
6							200			pA		$V_{GS} = -8$ V
7							400			nA		150°C
8					200					pA		$V_{GS} = -12$ V
9					400					nA		150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
12		$V_{DS(on)}$	Drain-Source ON Voltage						0 2	V	$V_{GS} = 0$	$I_D = 2\ 5$ mA
13							0.2					$I_D = 4$ mA
14					0.2							$I_D = 6.6$ mA
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V	
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$	
20		t_r	Rise Time		10		20		40			
21		t_{off}	Turn-OFF Time		40		60		80			

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4091	6.6 mA	-12 V	425 Ω
2N4092	4	-8	700
2N4093	2.5	-6	1120

*JEDEC registered data

NOTE:
1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE ≤ 10%
PULSE GENERATOR IMPEDANCE 50Ω

NCB
SAMPLING SCOPE
RISE TIME 0 4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1 7 pF

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NT
See Section 4

■ Ultra-High Input Impedance Amplifiers

Electrometers
pH Meters
Smoke Detectors
Intrusion Alarms

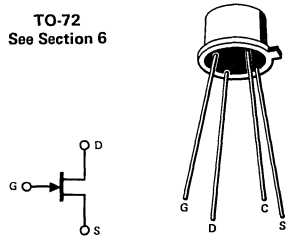
BENEFITS

- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (2N4117A Series)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate-Current ..... 50 mA
Total Device Dissipation
(Derate 2 mW/°C to 175°C) ..... 300 mW
Storage Temperature Range..... -65 to +175°C
Lead Temperature
(1/16" from case for 10 seconds)..... 255°C

TO-72
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4117/A FN4117/A Min	2N4117/A FN4117/A Max	2N4118 2N4118A Min	2N4118 2N4118A Max	2N4119 2N4119A Min	2N4119 2N4119A Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current 2N4117 Series Only		-10		-10		-10	pA	V_{GS} = -20 V, V_{DS} = 0	
2			FN4117		-25		-25		-25	nA		150°C
3		I_{GSS}	Gate Reverse Current 2N4117A Series Only		-1		-1		-1	pA	V_{GS} = -20 V, V_{DS} = 0	
4			FN4117A		-2.5		-2.5		-2 5	nA		150°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 10 V, I_D = 1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2) FN4117/A	0.03 0.015	0.09	0 08	0.24	0.20	0 60	mA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	210	80	250	100	330	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		3		5		10			
10		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

NT

*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

n-channel JFETs designed for . . .

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Siliconix

Performance Curves NRL/NPA See Section 4

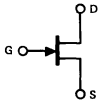
BENEFITS

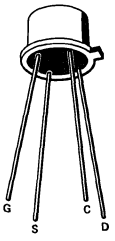
- High Gain
- Low Receiver Noise Figure

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -30 V
Gate Current ..... 10 mA
Drain Current ..... 15 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature ..... 300 mW
Derate Linearly to 175°C Free-Air Temperature at Rate of 2 mW/°C
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4220, 2N4220A		2N4221, 2N4221A		2N4222, 2N4222A		Units	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-0.1		-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8	V	V_{DS} = 15 V, I_D = 0.1 nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V	V_{DS} = 15 V, I_D = ( )	
				(50)	(50)	(200)	(200)	(500)	(500)	(μA)		
6		I_{DSS}	Saturation Drain Current (Note 2)	0 5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	2000	5000	2500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 2)		10		20		40			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg	f = 100 Hz

*JEDEC registered data.

NRL/NPA

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NRL/NH See Section 4

- **VHF Amplifiers**
- **Mixers**

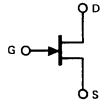
BENEFITS

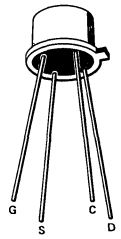
- Low Noise
  NF = 3 dB Typical @ 200 MHz
- Easy Tuning
  $C_{rss} < 2$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -30 V
Gate Current ..... 10 mA
Drain Current ..... 20 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N4223 Min	2N4223 Max	2N4224 Min	2N4224 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.25		-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15 V, I_D = ( )	
				(0.25)	(0 25)	(0.5)	(0.5)	(nA)		
5		V_{GS}	Gate-Source Voltage	-1 0	-7 0	-1.0	-7.5	V		
				(0 3)	(0.3)	(0.2)	(0 2)	(mA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYN	g_{fs}	Common-Source Forward Transconductance (Note 3)	3000	7000	2000	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
10	HIGH FREQ	$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	2700		1700		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
11		g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
12		g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
13		G_{ps}	Small Signal Power Gain	10				dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	
14		NF	Noise Figure		5					

*JEDEC registered data.

NRL/NH

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs *designed for . . .*

- **Small-Signal Amplifiers**
- **Choppers**
- **Voltage-Controlled Resistors**

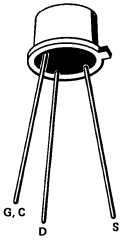
Siliconix

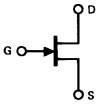
Performance Curves NPA
See Section 4

BENEFITS

- Low Noise
  NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages
  $V_{GS(off)}$ < 1 V (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances
  3:1 I_{DSS}, V_P, g_{fs} Ranges
- High Off-Isolation as a Switch
  $I_{D(off)}$ < 50 pA

TO-18
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Maximum Operating Temperature . . . . . 175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		2N4338		2N4339		2N4340		2N4341		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0 1		-0.1		-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0 3	-1	-0.6	-1 8	-1	-3	-2	-6		V_{DS} = 15 V, I_D = 0.1 μA	
5		$I_{D(off)}$	Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	V_{DS} = 15 V V_{GS} = ( )	
6		I_{DSS}	Saturation Drain Current (Note 3)	0 2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		5		15		30		60			
9		$r_{ds(on)}$	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
10		C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
12		NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

*JEDEC registered data

NPA

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C
3. These parameters are measured during a 2 msec interval 125 msec (I_{DSS}) and 625 msec (g_{fs}) after d-c power is applied. (Not a JEDEC condition.)

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves NCB
See Section 4

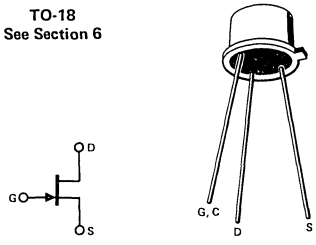
BENEFITS

- Low Insertion Loss, High Accuracy in Test Systems $r_{DS(on)} < 30\ \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . .300°C

TO-18
See Section 6



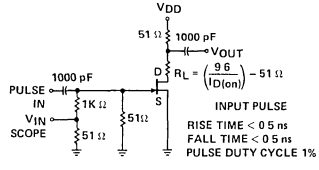
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4391 Min	2N4391 Max	2N4392 Min	2N4392 Max	2N4393 Min	2N4393 Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0		
2					-200		-200		-200	nA			150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$I_{D(off)}$	Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = -5 V	
5									200	nA			150°C
6							100			pA		V_{GS} = -7 V	
7							200			nA			150°C
8					100					pA		V_{GS} = -12 V	
9					200					nA			150°C
10		$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
11		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA		
12		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
13		$V_{DS(on)}$	Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
14							0.4					I_D = 6 mA	
15					0.4							I_D = 12 mA	
16		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
17		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
18	DYN	C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		
19		C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = - 5 V	f = 1 MHz
20							3.5					V_{GS} = - 7 V	
21					3.5							V_{GS} = -12 V	
22	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
23		t_r	Rise Time		5		5		5				
24		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50				
25		t_f	Fall Time		15		20		30				

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4391	12 mA	-12 V	
2N4392	6	-7	
2N4393	3	-5	

*JEDEC registered data

NOTE.
1 Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.



NCB

2N4416 2N4416A
PLASTIC EQUIVALENT PN4416

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NH
See Section 4

- **VHF Amplifiers**
- **Mixers**

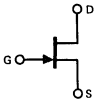
BENEFITS

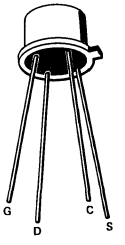
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage, 2N4416 . . . . . -30 V
Gate-Drain or Gate-Source Voltage, 2N4416A . . . . . -35 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -20 V, V_{DS} = 0 V	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0 V	2N4416
				-35				2N4416A
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
				-2.5	-6			2N4416A
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50	μmho		
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4	pF		
10		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
13		g_{oss}	Common-Source Output Conductance		75		100	μmho	
14		b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
15		g_{fs}	Common-Source Forward Transconductance			4000		μmho	
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

*JEDEC Registered data

NH

NOTES:
1. Pulse test duration = 300 μs

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves NCB
See Section 4

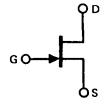
BENEFITS

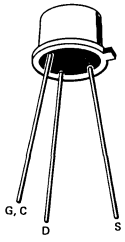
- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856, 59)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- High Speed
  $t_{ON} < 9$ ns

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate Source Voltage, 2N4856-58 ..... −40V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859-61 ..... −30V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C) 1.8W
Storage Temperature Range ..... −65 to +200°C
Lead Temperature (1″ from case for 10 seconds) ..... 300°C

TO-18
See Section 6



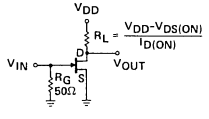


***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N4856 2N4859 Min	2N4856 2N4859 Max	2N4857 2N4860 Min	2N4857 2N4860 Max	2N4858 2N4861 Min	2N4858 2N4861 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	2N4856-58	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2			2N4859-61	−30		−30		−30				
3		I_{GSS} Gate Reverse Current	2N4856-58		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4					−500		−500		−500	nA		150°C
5			2N4859-61		−250		−250		−250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6					−500		−500		−500	nA		150°C
7		$I_{D(off)}$ Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8					500		500		500	nA		150°C
9		$V_{GS(off)}$ Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0 8	−4	V	$V_{DS} = 15$ V, $I_D = 0$ 5 nA	
10		I_{DSS} Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$ Drain-Source ON Voltage			0 75 (20)		0 50 (10)		0 50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss} Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance			8		8		8			
15	SWITCHING	$t_{d(on)}$ Turn-ON Delay Time			6 (20) [−10]		6 (10) [−6]		10 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ )$, $V_{GS(off)} = [\ ]$, $R_L =$ { 464 Ω, 2N4856, 59; 953 Ω, 2N4857, 60; 1910 Ω, 2N4858, 61 }	
16		t_r Rise Time			3 (20) [−10]		4 (10) [−6]		10 (5) [−4]	ns (mA) [V]		
17		t_{off} Turn-OFF Time			25 (20) [−10]		50 (10) [−6]		100 (5) [−4]	ns (mA) [V]		

*JEDEC registered data

NOTE:
1 Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%



NCB

INPUT PULSE
RISE TIME 0 25 ns
FALL TIME 0 75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0 75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2 5 pF

2N4856 2N4857 2N4858 2N4859 2N4860 2N4861 JAN TX
SURFACE MOUNT EQUIVALENTS: SST4856, 4857, 4858, 4860, 4861

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

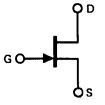
Siliconix

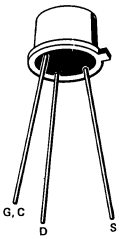
Performance Curves NCB
See Section 4

BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856A, 59A)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF
- High Speed
  $t_{ON} < 8$ ns

TO-18
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage,
2N4856A-58A . . . . . −40 V
Reverse Gate-Drain or Gate-Source Voltage,
2N4859A-61A . . . . . −30 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

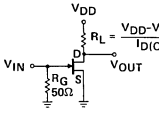
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4856A 2N4859A Min	2N4856A 2N4859A Max	2N4857A 2N4860A Min	2N4857A 2N4860A Max	2N4858A 2N4861A Min	2N4858A 2N4861A Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	2N4856A-58A	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2			2N4859A-61A	−30		−30		−30				
3		I_{GSS} Gate Reverse Current	2N4856A-58A		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4					−500		−500		−500	nA		150°C
5			2N4859A-61A		−250		−250		−250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6					−500		−500		−500	nA		150°C
7		$I_{D(off)}$ Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8					500		500		500	nA		150°C
9		$V_{GS(off)}$ Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS} Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$ Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D =$ ( )	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss} Common-Source Input Capacitance			10		10		10	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance			4		3.5		3.5			
15	SWITCHING	$t_{d(on)}$ Turn-ON Delay Time			5 (20) [−10]		6 (10) [−6]		8 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} =$ ( ), $V_{GS(off)} =$ [ ], $R_L =$ 464 Ω, 2N4856A, 59A; 953 Ω, 2N4857A, 60A; 1910 Ω, 2N4858A, 61A	
16		t_r Rise Time			3 (20) [−10]		4 (10) [−6]		8 (5) [−4]	ns (mA) [V]		
17		t_{off} Turn-OFF Time			20 (20) [−10]		40 (10) [−6]		80 (5) [−4]	ns (mA) [V]		

NCB

*JEDEC registered data

NOTE:
1 Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NPA
See Section 4

■ Audio and Sub-Audio Amplifiers

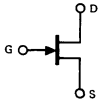
BENEFITS

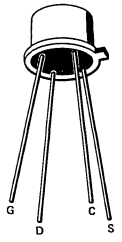
- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Souce Voltage (Note 1) ... -40 V
Gate Current or Drain Current ..... 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C) .....300 mW
Storage Temperature Range ..... -65°C to +200°C
Lead Temperature
(1/16" from case for 60 seconds) .....300°C

TO-72
See Section 6





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4867 2N4867A Min	2N4867 2N4867A Max	2N4868 2N4868A Min	2N4868 2N4868A Max	2N4869 2N4869A Min	2N4869 2N4869A Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0		
2					-0.25		-0 25		-0 25	μA			150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1 8	-5		V_{DS} = 20 V, I_D = 1 μA		
5		I_{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7 5	mA	V_{DS} = 20 V, V_{GS} = 0		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5		4		10				
8		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF			f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		25		25		25				
10		$\overline{e_n}$	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/$\sqrt{Hz}$	V_{DS} = 10 V, V_{GS} = 0	2N4867 Series	f = 10 Hz
11					10		10		10			2N4867A Series	
12					10		10		10			2N4867 Series	f = 1 kHz
13					5		5		5			2N4867A Series	
14		NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0 R_{gen} = 20 K, 2N4867 Series 5 K, 2N4867A Series		f = 1 kHz

*JEDEC registered data.

NPA

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.

p-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PSA/PSB See Section 4

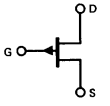
BENEFITS

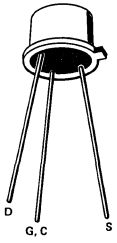
- Low Insertion Loss
  $r_{DS(on)} < 75\ \Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . .50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature (1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 6





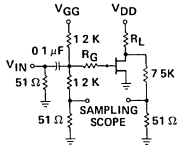
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5018 Min	2N5018 Max	2N5019 Min	2N5019 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15$ V, $V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		–10		–10	nA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5018)	
4					–10		–10	µA	$V_{GS} = 7$ V (2N5019)	150°C
5		I_{DGO}	Drain Reverse Current		–2		–2	nA	$V_{DG} = -15$ V, $I_S = 0$	
6					–3		–3	µA		150°C
7		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
8		I_{DSS}	Saturation Drain Current	–10		–5		mA	$V_{DS} = -20$ V, $V_{GS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		–0.5		–0.5	V	$V_{GS} = 0$, $I_D = -6$ mA (2N5018), $I_D = -3$ mA (2N5019)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1$ mA, $V_{GS} = 0$	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
12	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5018), $V_{GS} = 7$ V (2N5019)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6$ V, $V_{GS(on)} = 0$	
15		t_r	Rise Time		20		75			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
17		t_f	Fall Time		50		100			

	$V_{GS(off)}$	$I_{D(on)}$	R_L
2N5018	12 V	–6 mA	910 Ω
2N5019	7 V	–3 mA	1.8K Ω

*JEDEC registered data

NOTE:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged



PSA/PSB

INPUT PULSE	SAMPLING SCOPE
RISE TIME < 1 ns	RISE TIME 0 4 ns
FALL TIME < 1 ns	INPUT RESISTANCE 10 MΩ
PULSE WIDTH 100 ns	INPUT CAPACITANCE 1 5 pF
REPETITION RATE 1 MHz	

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

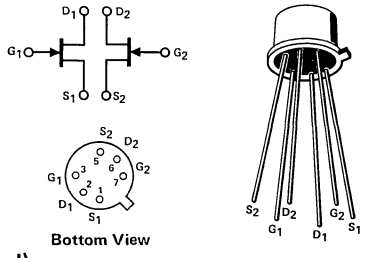
Performance Curves NQP
See Section 4

■ High Gain Differential Amplifiers

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5045)
- Low Drift
  5 mV Drift Maximum (2N5045)

TO-71
See Section 6



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Forward Gate Current . . . . . 30 mA
Total Dissipation (25°C Free Air Temp.) . . . . . 400 mW
Power Derating (to 175°C) . . . . . 2.67 mW/°C
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic (Note 1)		2N5045		2N5046		2N5047		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	μA	V_{GS} = -50 V, V_{DS} = 0 V	
2					-0.25		-0 25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0 V	
3					-250		-250		-250			T = 150°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5	-0.5	-4.5	-0 5	-4.5	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		I_{DSS}	Drain Saturation Current	0.5	8.0	0.5	8 0	0.5	8.0	mA	V_{DS} = 15V, VGS = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1.5	6 0	1.5	6.0	1.5	6 0	mmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		$\lvert y_{fs} \rvert$	Common-Source Forward Admittance	1 5		1 5		1.5				f = 100 MHz
8		g_{os}	Common-Source Output Conductance		25		25		25	μmho		f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		8 0		8 0		8.0	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		4 0		4.0		4 0			
11		NF	Spot Noise Figure		5 0		5.0			dB		f = 10 Hz, R_G = 1 MΩ
12		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200			$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
13	MATCHING	$\lvert I_{GSS1} - I_{GSS2} \rvert$	Differential Gate Current		10		10		10	nA	V_{GS} = -15 V, V_{DS} = 0 V	T_A = 100°C
14		I_{DSS1}/I_{DSS2}	Drain Current Ratio (Note 2)	0.95	1 0	0 9	1.0	0 8	1 0	—	V_{GS} = 0 V, V_{DS} = 15 V	
15		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DS} = 15 V	I_D = 50 μA
16					5		10		15			I_D = 200 μA
17		$\Delta\lvert V_{GS1} - V_{GS2} \rvert$	Gate-Source Voltage Differential Drift (Note 3)		5		10		15		V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C	T_B = -25°C
18					5		10		15			T_B = 100°C
19		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{DS} = 15 V, I_D = 200 μA	f = 1 kHz
20		$\lvert g_{os1} - g_{os2} \rvert$	Diff. Output Conductance		1.0		2 0		3.0	μmho		

*JEDEC registered data

NOTES:
1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements..
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B

NQP

3

SURFACE MOUNT EQUIVALENT: SST174 SERIES

2N5114 2N5115 2N5116 JAN TX

p-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves PSB
See Section 4

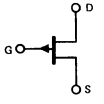
BENEFITS

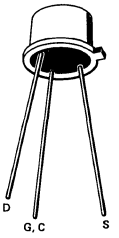
- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems $r_{DS(on)} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . .50 mA
Total Device Dissipation, Free-Air (Derate 3mW/°C for $T_A > 25°C$) . . . . . 500 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature (1/16" from case for 10 seconds) . . . . . 300°C

TO-18
See Section 6





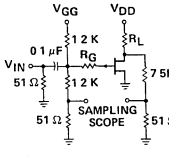
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5114 Min	2N5114 Max	2N5115 Min	2N5115 Max	2N5116 Min	2N5116 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	
3					1 0		1.0		1.0	μA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5114) $V_{GS} = 7$ V (2N5115), $V_{GS} = 5$ V (2N5116)	
5					-1 0		-1 0		-1.0	μA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	$V_{DS} = -15$ V, $I_D = -1$ nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{GS} = 0$, $V_{DS} = -18$ V (2N5114) $V_{DS} = -15$ V (2N5115, 2N5116)	
8		$V_{GS(f)}$	Forward Gate-Source Voltage		-1		-1		-1	V	$I_G = -1$ mA, $V_{DS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		-1 3		-0.8		-0.6		$V_{GS} = 0$, $I_D = -15$ mA (2N5114) $I_D = -7$ mA (2N5115), $I_D = -3$ mA (2N5116)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = -1$ mA	
11	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		25		25		27	pF	$V_{DS} = -15$, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5114) $V_{GS} = 7$ V (2N5115), $V_{GS} = 5$ V (2N5116)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		6		10		25	ns		
15		t_r	Rise Time		10		20		35			
16		$t_{d(off)}$	Turn-OFF Delay Time		6		8		20			
17		t_f	Fall Time		15		30		60			

	2N5114	2N5115	2N5116
V_{DD}	–10 V	–6 V	–6 V
V_{GG}	20 V	12 V	8 V
R_L	130 Ω	910 Ω	2000 Ω
R_G	100 Ω	220 Ω	390 Ω
$I_{D(on)}$	–15 mA	–7 mA	–3 mA

*JEDEC registered data

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse Test PW 300 μs, duty cycle ≈ 2



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 100 ns
REPETITION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0 4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1 5 pF

PSB

monolithic dual n-channel JFETs *designed for . . .*

- **Differential Amplifiers**
- **FET Input Op Amps**

Siliconix

Performance Curves NQP
See Section 4

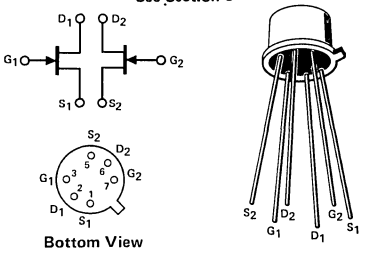
BENEFITS

- Minimum System Error and Calibration
  5 mV Maximum Offset (2N5196, 97)
- Low Drift
  5 μV/°C Maximum (2N5196)
- Simplifies Amplifier Design
  Low Output Conductance

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.56 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 4.3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +200°C

TO-71
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-50	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0 2	-3.8			
6		I_G	Gate Operating Current		-15	pA	V_{DG} = 20 V, I_D = 200 μA	
					-15	nA		125°C
7		I_{DSS}	Saturation Drain Current	0 7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	700	1600		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
15		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

		Characteristic		2N5196		2N5197		2N5198		2N5199		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0 95	1	0.95	1	0.95	1	0 95	1	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0 95	1	–	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
19		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
20		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	μV/°C		T_A = 25°C T_B = 125°C
21					5		10		20		40			T_A = -55°C T_B = 25°C
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

*JEDEC registered data. NQP

NOTES:
1 Assumes smaller value in numerator
2 Measured at end points, T_A and T_B

n-channel JFETs *designed for . . .*

Siliconix

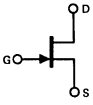
- **Low ON Resistance Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Capacitors**
- **Low Noise Audio Amplifiers**

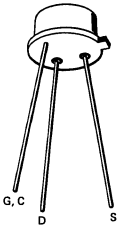
Performance Curves NIP See Section 4

BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 5\ \Omega$ (2N5432)
- Small Error in Measurement Systems
  $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{d(on)} < 4$ ns
- Low Noise Audio-Frequency Amplification
  $\overline{e_n} < 2\ nV/\sqrt{Hz}$ at 1 kHz Typical

TO-52
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 100 mA
Drain Current . . . . . 400 mA
Total Device Dissipation at 25°C
Free-Air Temperature (Note 1) . . . . . 300 mW
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

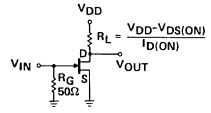
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N5432 Min	2N5432 Max	2N5433 Min	2N5433 Max	2N5434 Min	2N5434 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-200		-200		-200	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-200		-200		-200	nA		150°C
3		BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = -10 V	
5					200		200		200	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V_{DS} = 5 V, I_D = 3 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
9		$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
13	SW	$t_{d(on)}$	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -12 V, $I_{D(on)}$ = 10 mA, R_L = 145 Ω (2N5432), 143 Ω (2N5433), 140 Ω (2N5434)	
14		t_r	Rise Time		1		1		1			
15		$t_{d(off)}$	Turn-OFF Delay Time		6		6		6			
16		t_f	Fall Time		30		30		30			

*JEDEC registered data.

NIP

NOTES:
1. Derate linearly at the rate of 2.3 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NQP
See Section 4

■ Low and Medium Frequency Differential Amplifiers

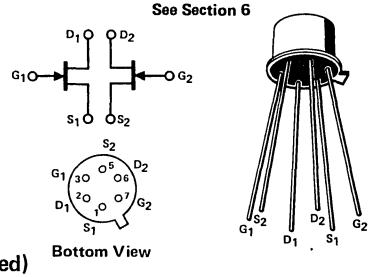
BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design
  Output Conductance Less that 1 μmho

*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage . . . . . ±100 V
Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation at (Each Side) . . . . . 250 mW
85°C Case Temperature (Both Sides) . . . . . 500 mW
Power Derating (Each Side) . . . . . 2.86 mW/°C
(Both Sides) . . . . . 4.3 mW/°C
Storage Temperature Range . . . . . -65 to +250°C
Lead Temperature (1/16" from case for 10 seconds) . . . 300°C

TO-71
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5452		2N5453		2N5454		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0 V	
2					-200		-200		-200	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	V	V_{DS} = 20 V, I_D = 50 μA	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2	V	V_{DS} = 0 V, I_G = 1 mA	
7		I_{DSS}	Drain Saturation Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
9				1000		1000		1000				f = 100 MHz
10		g_{os}	Common-Source Output Conductance		3.0		3.0		3.0	μmho		f = 1 kHz
11					1.0		1.0		1.0		V_{DS} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2	pF		
14		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5	pF	V_{DG} = 10 V, I_S = 0 V	
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
16		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
17	MATCHING	I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
19		$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0	mV		T = 25°C to -55°C
20					0.5		1.0		2.5	mV		T = 25°C to +125°C
21		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NQP

3

n-channel JFETs *designed for . . .*

Siliconix

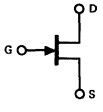
Performance Curves NRL, NPA, NH See Section 4

- **General Purpose Amplifiers**
- **Switches**

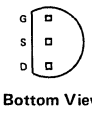
BENEFITS
- Low Cost
- Automated Insertion Package

Plastic

TO-92
See Section 6



Bottom View



*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature	135°C
Storage Temperature Range	-65 to +150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5457			2N5458			2N5459			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.01	-1.0		-0.01	-1.0		-0.01	-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
2						-200			-200			-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		-25	-60		-25	-60		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-6.0	-1.0		-7.0	-2.0		-8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0		5.0	2.0		9.0	4.0		16	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		5,000	1,500		5,500	2,000		6,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		10	50		15	50		20	50			
8		C_{iss}	Common-Source Input Capacitance		4.5	7.0		4.5	7.0		4.5	7.0	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0		1.0	3.0		1.0	3.0			
10		NF	Noise Figure		0.04	3.0		0.04	3.0		0.04	3.0	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 MΩ, NBW = 1 Hz	f = 1 kHz

*JEDEC registered data

NOTE:
1. Pulse test pulsewidth = 2 ms.

NRL, NPA, NH

p-channel JFET

Siliconix

designed for . . .

- **Amplifiers**
- **Analog Switches**

BENEFITS

- **Low Cost**
- **Automated Insertion Package**
- **Low Capacitance**

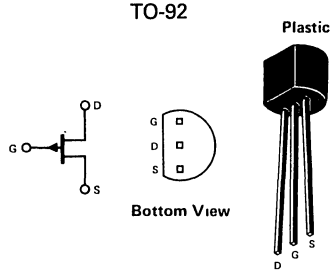
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted

Drain-Gate or Source-Gate Voltage
- 2N5460 - 2N5462 ..... 40V
- 2N5463 - 2N5465 ..... 60V

Gate Current .....10 mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range..... −55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Power Dissipation ..... 310 mW
- Derate Above 25°C ..... 2.8 mW/°C

PIN CONFIGURATION
TO-92



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Parameter				Min	Typ	Max	Units	Test Conditions	
BV_{GSS}	Gate-Source Breakdown Voltage		2N5460, 2N5461, 2N5462	40			V	I_G = 10 μAdc, V_{DS} = 0	
			2N5463, 2N5464, 2N5465	60					
$V_{GS(off)}$	Gate-Source Cutoff Voltage		2N5460, 2N5463	0.75		6.0	V	V_{DS} = 15 Vdc, I_D = 1.0 μAdc	
			2N5461, 2N5464	1.0		7.5			
			2N5462, 2N5465	1.8		9.0			
I_{GSSR}	Gate-Reverse Current		2N5460, 2N5461, 2N5462			5.0	nA	V_{DS} = 0	V_{GS} = 20V
			2N5463, 2N5464, 2N5465			5 0			V_{GS} = 30V
		T_A = 100°C	2N5460, 2N5461, 2N5462			1 0	μA		V_{GS} = 20V
			2N5463, 2N5464, 2N5465			1.0			V_{GS} = 30V
I_{DSS}	Zero-Gate Voltage Drain Current		2N5460, 2N5463	−1 0		−5.0	mA	V_{DS} = −15V	V_{GS} = 0
			2N5461, 2N5464	−2.0		−9 0			
			2N5462, 2N5465	−4.0		−16			
V_{GS}	Gate-Source Voltage		2N5460, 2N5463	0 5		4 0	V		I_D = 0 1 mA
			2N5461, 2N5464	0 8		4.5			I_D = −0.2 mA
			2N5462, 2N5465	1 5		6.0			I_D = −0 4 mA
g_{fs}	Forward Transadmittance		2N5460, 2N5463	1000		4000	μmho	V_{DS} = −15V V_{GS} = 0V	f = 1 0 kHz
			2N5461, 2N5464	1500		5000			
			2N5462, 2N5465	2000		6000			
g_{os}	Output Admittance					75	μmho		
C_{iss}	Input Capacitance				5.0	7	pF		
C_{oss}	Reverse Transfer Capacitance				1.0	2.0	pF		
NF	Common-Source Noise Figure				1.0	2.5	dB		f = 100 Hz BW = 1 0 Hz R_G = 1 0 MΩ ($\bar{e}_n$ only)
$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage				60	115	$\frac{nV}{\sqrt{Hz}}$		

3

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**
- **Analog Switches**

Siliconix

Performance Curves NH See Section 4

BENEFITS

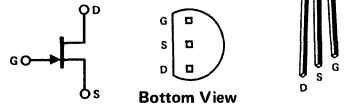
- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch
  Very Little Charge Coupling
  $C_{rss} < 1.0$ pF

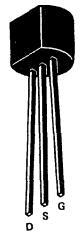
***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Gate Voltage . . . . . 25 V
Source Gate Voltage . . . . . 25 V
Drain Current . . . . . 30 mA
Forward Gate Current . . . . . 10 mA
Total Device Dissipation @ 25°C . . . . . 360 mW
Derate above 25°C . . . . . 3.27 mW/°C
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 240°C

Plastic

TO-92
See Section 6





***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N5484 Min	2N5484 Max	2N5485 Min	2N5485 Max	2N5486 Min	2N5486 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-200		-200		-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0 5	-4.0	-2.0	-6.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1 0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,000	6,000	3,500	7,000	4,000	8,000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		60		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	2,500								f = 100 MHz
9						3,000		3,500				f = 400 MHz
10		$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
11							100		100			f =400 MHz
12		$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
13							1,000		1,000			f = 400 MHz
14		C_{iss}	Common-Source Input Capacitance		5 0		5.0		5.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1 0		1.0		1.0			
16		C_{oss}	Common-Source Output Capacitance		2.0		2.0		2 0			
17		NF	Noise Figure		2 5		2 5		2 5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
18					3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz
19							2 0		2 0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	
20							4.0		4.0			f = 400 MHz
21		G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f = 100 MHz
22						18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	
23						10	20	10	20			f = 400 MHz

* JEDEC registered data

NH

NOTE:
1 Pulse Test PW 300 μs, duty cycle ≤ 3%

monolithic dual n-channels JFETs *designed for . . .*

Siliconix

Performance Curves NQP
See Section 4

BENEFITS

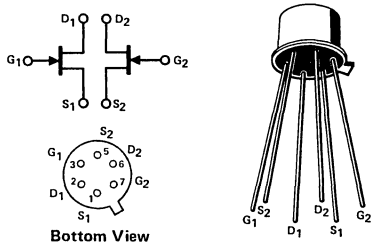
- Ultra-Low Noise
  $\overline{e_n}$ = 8 nV/√Hz at 10 Hz (Typical)
  $\overline{e_n}$ = 2 nV/√Hz at 1 kHz (Typical)
- Minimum System Error and Calibration
  5 mV Offset Maximum
  CMRR > 100 dB

■ Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Souce Voltage ..... -40 V
Gate Current ..... 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.0 mW/°C ..... 250 mW
Total Device Dissipation T_A = 85°C
(Derate 3.0 mW/°C) ..... 375 mW
Storage Temperature Range ..... -65°C to +200°C
Lead Temperature
(1/16" from case for 30 seconds) ..... 300°C

TO-71
*See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-250	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40			I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0 7	-4	V	V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage	-0 2	-3 8			
6		I_G	Gate Operating Current		-100	pA	V_{DG} = 20 V, I_D = 200 μA	
					-100	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0 5	7 5	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	500	1000		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		10		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		1		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		5			
14		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage	2N5515-19	30	nV/√Hz	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
				2N5520-24	15			
				2N5515-24	10			f = 1 kHz

		Characteristic		2N5515,20 Min	2N5515,20 Max	2N5516,21 Min	2N5516,21 Max	2N5517,22 Min	2N5517,22 Max	2N5518,23 Min	2N5518,23 Max	2N5519,24 Min	2N5519,24 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0 95	1	0 95	1	0 95	1	0 95	1	0 90	1	–	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV		
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
					5		10		20		40		80			T_A = -55°C, T_B = 25°C
19		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0 1		0 1		0 1		0 1		0 1	μmho		f = 1 kHz
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0 97	1	0 97	1	0 95	1	0 95	1	0.90	1	–		
21		CMRR	Common Mode Rejection Ratio (Note 4)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA	

*JEDEC registered data

NOTES.
1 Pulse test required, pulsewidth = 300 μs, duty cycle ⩽ 3%.
2 Assumes smaller value in numerator
3 Measured at end points, T_A and T_B
4 $CMRR = 20\log_{10}\left(\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right)$, ΔV_{DD} = 10 V

NQP

monolithic dual n-channel JFETs *designed for . . .*

■ General Purpose Differential Amplifiers

Siliconix

Performance Curves NCB/NZB See Section 4

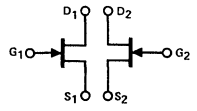
BENEFITS

- High Input Impedance
  $I_G < 50$ pA
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5545)

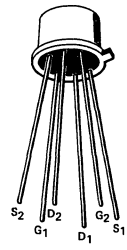
*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –50 V
Gate Current . . . . . 30 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 1.67 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 25°C
(Derate 2.67 mW/°C) . . . . . 400 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 30 seconds) . . . . . .300°C

TO-71
See Section 6



Bottom View



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0		
2					-150	nA			T_A = 150°
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 15 V, I_D = 0.5 nA		
5		I_G	Gate Operating Current		-50	pA	V_{DG} = 15 V, I_D = 200 μA		
6		I_{DSS}	Saturation Drain Current	0.5	8	mA	V_{DS} = 15 V, V_{GS} = 0		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0		f = 1 kHz
8		g_{os}	Common-Source Output Conductance		25				
9		C_{iss}	Common-Source Input Capacitance		6	pF			f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		2				
11		NF	Spot Noise Figure		3.5	dB	V_{DG} = 15 V, I_D = 200 μA	2N5545	f = 10 Hz, R_G = 1 MΩ
					5			2N5546	
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		180	$\frac{nV}{\sqrt{Hz}}$		2N5545	f = 10 Hz
					200			2N5546	

		Characteristic		2N5545		2N5546		2N5547		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
13	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5	nA	V_{DG} = 15 V, I_D = 200 μA	T_A = 125°C
14		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.90	1	0.90	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 15 V	I_D = 50 μA
					5		10		15			I_D = 200 μA
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		10		20		40	μV/°C	V_{DG} = 15 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
					10		20		40			T_A = -55°C, T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.95	1	0.90	1	–		f = 1 kHz
18		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		2		3	μmho		

*JEDEC registered data.

NCB/NZB

NOTES:
1 Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

matched dual n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NCB See Section 4

■ Wideband Differential Amplifiers

■ Commutators

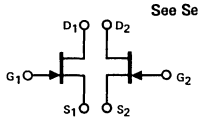
BENEFITS

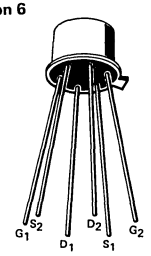
- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

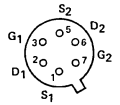
*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage ..... ±80 V
Gate-Drain or Gate-Source Voltage ..... -40 V
Gate Current ..... 50 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 2.2 mW/°C) ..... 325 mW
Total Device Dissipation, T_A = 25°C
(Derate 3.3 mW/°C) ..... 650 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) .....300°C

TO-71
See Section 6







Bottom View

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0 5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		1.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	30	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
				7000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance		45			f = 1 kHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		12			
12		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		2N5564		2N5565		2N5566		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0 95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C T_B = 125°C
					10		25		50			T_A = -55°C T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0 95	1	0.90	1	0.90	1	–		f = 1 kHz

*JEDEC registered data.

NCB

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ⩽ 3%.
2. Assumes smaller value in numerator
3. Measured at ends points, T_A and T_B.

3

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

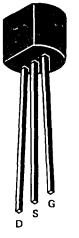
Performance Curves NCB/NZB See Section 4

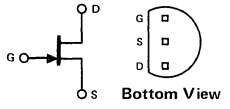
BENEFITS

- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching
  $t_{rise} < 5$ ns (2N5638)
- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (2N5638)
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF

Plastic

TO-92
See Section 6





*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at T_{LEAD} = 25°C	625 mW
Derate above 25°C	5.68 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

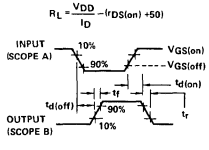
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5638		2N5639		2N5640		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
3					-1.0		-1.0		-1.0	μA		T_A = +100°C
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = -12 V (2N5638)	
5					1.0		1.0		1.0	μA	V_{GS} = -8 V (2N5639), V_{GS} = -6 V (2N5640)	T_A = +100°C
6		I_{DSS}	Saturation Drain Current	50		25		5.0		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	V_{GS} = 0, I_D = 12 mA (2N5638), I_D = 6 mA (2N5639), I_D = 3 mA (2N5640)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	I_D = 1 mA, V_{GS} = 0	
9		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0	f = 1 kHz
10	DYN	C_{iss}	Common-Source Input Capacitance		10		10		10	pF	V_{GS} = -12 V, V_{DS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
12	SW	$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	nsec	V_{DD} = 10 V $I_{D(on)}$ = 12 mA (2N5638) R_L = 800 Ω (2N5638)	
13		t_r	Rise Time		5.0		8.0		10		$V_{GS(on)}$ = 0 $I_{D(on)}$ = 6 mA (2N5639) R_L = 1.6k Ω (2N5639)	
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		15		$V_{GS(off)}$ = -10 V $I_{D(on)}$ = 3 mA (2N5640) R_L = 3.2k Ω (2N5640)	
15		t_f	Fall Time		10		20		30			

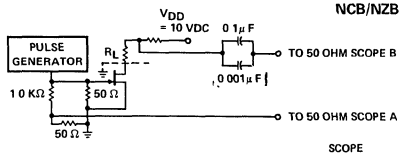
* JEDEC registered data

NOTE:

1 Pulse test PW ≤ 300 μsec, duty cycle ≤ 3.0%



NCB/NZB



matched dual n-channel JFETs *designed for . . .*

- **Differential Amplifiers**
- **High Input Impedance Amplifiers**

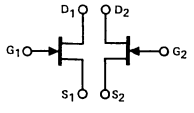
Siliconix

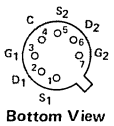
Performance Curves NT
See Section 4

BENEFITS

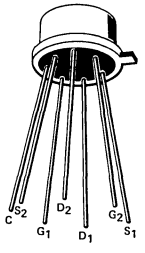
- Matching Characteristics Specified
- High Input Impedance
  I_G = 1 pA Max (2N5906–9)

TO-78
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage ..... ±80 V
Gate-Drain or Gate-Source Voltage ..... -40 V
Gate Current ..... 10 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3 mW/°C) ..... 367 mW
Total Device Dissipation, T_A = 25°C
(Derate 4 mW/°C) ..... 500 mW
Storage Temperature Range ..... -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5902-5 Min	2N5902-5 Max	2N5906-9 Min	2N5906-9 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-2	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-10		-5	nA		125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage		-4		-4			
6		I_G	Gate Operating Current		-3		-1	pA	V_{DG} = 10 V, I_D = 30 μA	
7					-3		-1	nA		125°C
8	DYNAMIC	I_{DSS}	Saturation Drain Current	30	500	30	500	μA		
9		g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		5		5			
11		C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
12		C_{rss}	Common Source Reverse Transfer Capacitance		1.5		1.5			
13		g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	V_{DG} = 10 V, I_D = 30 μA	
14		g_{os}	Common-Source Output Conductance		1		1			f = 1 kHz
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
16		NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 M

		Characteristic		2N5902, 6 Min	2N5902, 6 Max	2N5903, 7 Min	2N5903, 7 Max	2N5904, 8 Min	2N5904, 8 Max	2N5905, 9 Min	2N5905, 9 Max	Unit	Test Conditions	
17	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20		20		20	nA	V_{DG} = 10 V, I_D = 30 μA, T_A = 125°C	2N5902-5
18					0.2		0.2		0.2		0.2			2N5906-9
19		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
21		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
22		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
23					5		10		20		40			T_A = -55°C, T_B = 25°C
24		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

*JEDEC registered data

NOTES:

1. Assumes smaller value in numerator
2. Measured at end points, T_A and T_B

3

matched dual n-channel JFETs *designed for . . .*

■ Wideband Differential Amplifiers

Siliconix

Performance Curves NZF-D
See Section 4

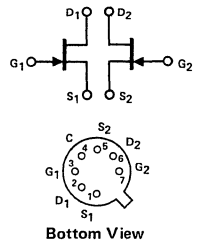
BENEFITS

- High Gain through 100 MHz
  $g_{fs} > 5000$ μmho
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage ..... ±80 V
Gate-Drain or Gate-Source Voltage ..... -25 V
Gate Current ..... 50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C).. 367 mW
Total Device Dissipation, (Derate 4 mW/°C) ..... 500 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) .....300°C

TO-78
See Section 6



*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4		V_{DG} = 10 V, I_D = 5 mA	
6		I_G	Gate Operating Current		-100	pA		
					-100	nA		T_A = 125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K

		Characteristic		2N5911 Min	2N5911 Max	2N5912 Min	2N5912 Max	Unit	Test Conditions	
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	T_A = 125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
19		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		20		40	μV/°C		T_A = 25°C T_B = 125°C
20					20		40			T_A = -55°C T_B = 25°C
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.95	1	0.95	1	–		f = 1 kHz

*JEDEC registered data

NZF-D

NOTES:
1. Pulsewidth ≤ 300 μs, duty cycle ≤ 3%
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

monolithic dual n-channel JFETs *designed for . . .*

- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Siliconix

Performance Curves NNR See Section 4

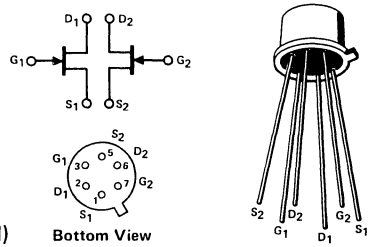
BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N6905)
  95 dB Minimum CMRR (2N6905-07)
- Low Drift with Temperature
  10 μV/°C Maximum (2N6905)
- Operates from Low Power Supply Voltages
  $V_{GS(off)}$ <2.5 V
- Simplified Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  e_n = 10 nV/$\sqrt{Hz}$ at 10 Hz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... 35 V
Forward Gate Current ..... 10 mA
Device Dissipation (each side)
@ T_A = 85°C derate 2.6 mW%°C ..... 300 mW
Total Device Dissipation
@ T_A = 85°C) ..... 500 mW
Storage Temperature Range ..... −65 to 200°C

TO-71



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		Characteristic		2N6905/5A Min	2N6905/5A Max	2N6906/6A Min	2N6906/6A Max	2N6907/7A Min	2N6907/7A Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage (A Version)	−35 −50		−35 −50		−35 −50		V	V_{DS} = 0, I_G = −1μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		−15		−15		−15	pA	V_{DS} = 0, V_{GS} = −15 V	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.2	−3.0	−0.2	−3.0	−0.2	−3.0	V	V_{DS} = 15 V, I_D = 1 nA	
4		$V_{GS(on)}$	Gate-Source Voltage (on)		−2.3		−2.3		−2.3		V_{DG} = 15 V, I_D = 200μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G	Gate Current (Note 1)		−5		−5		−5	pA	V_{DG} = 15 V, I_D = 200μA	
7					−5		−5		−5	nA		T_A = 125°C
8	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		20		20		20			
10		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF	V_{DG} = 15 V, I_D = 200μA	f = 1 MHz
11		C_{rss}	Common Source Reverse Transfer Capacitance		3.0		3.0		3.0			
12		$\overline{e}_N$	Equivalent Short-Circuit Input Noise Voltage		15		15		15	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
13	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		dB	V_{DG} = 10 to 20 V, I_D = 200μA	
14		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		25	mV	V_{DG} = 10 V, I_D = 200μA	
15		$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		25		50	μV/°C	V_{DG} = 10 V, I_D = 200μA	T_A = −55°C, T_B = +25°C, T_C = +125°C

NOTES

1 Approximately doubles for every 10°C increase in T_A 2 Pulse test duration = 300μs duty cycle ≤ 3% 3 CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2} \rvert}\right]$ ΔV_{DD} = 10V

4 Measured at end points, T_A, T_B and T_C

3

n-channel JFET *designed for . . .*

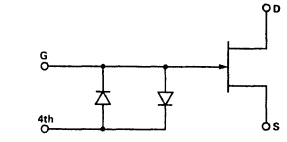
- **Infra-red Detector**
- **Micropower Pre-amplifier**
- **Transducer Impedance Converter**
- **Hearing Aid Pre-amplifier**

Siliconix

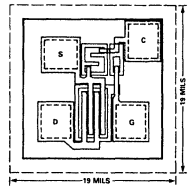
Performance Curves NBB See Section 4

BENEFITS

- **Reduced Component Count, Lower Circuitry Cost**
- **Input Over Voltage Clamp by Two Built-in Diodes**
- **Low Noise**
- **Low Leakage**



TO-72



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... −30 V
Gate-Current ..... 10 mA
Total Device Dissipation (25°C) ..... 300 mW
Storage Temperature Range ..... −55 to 200°C
Operating Temperature Range ..... −55 to 150°C
Power Derating ..... 2.4 mW/°C
Lead Temperature (10 seconds @ 1/16") ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristics	2N6908		2N6909		2N6910		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
BV_{GSS}	Gate-Source Breakdown Voltage (Note 1)	−30		−30		−30		V	I_G = −1 μA, V_G4 = 0 V, V_{DS} = 0 V
I_{GSS}	Gate Reverse Current (Note 1)	Typ −1	−25	Typ −1	−25	Typ −1	−25	pA	V_{GS} = −15 V, V_{DS} = 0 V, V_G4 = 0 V
$V_{GS(off)}$	Gate Source Cutoff Voltage (Note 1)	−0.3	−1.8	−0.6	−2.3	−0.9	−3.5	V	V_{DS} = 10 V, I_D = 1 nA, V_G4 = 0 V
I_{DSS}	Saturation Drain Current (Note 1)	0.05	2.0	0.20	3.5	0.6	5.0	mA	V_{DS} = 10 V, V_{GS} = 0 V, V_G4 = 0 V
g_{fs}	Common-Source Forward Transconductance (Note 1)	100	3000	400	3500	1200	4000	μmho	V_{DS} = 10 V, V_{GS} = 0 V, V_G4 = 0 V
g_{os}	Common-Source Output Conductance (Note 1)		50		75		100		
C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF	V_{DS} = 10V, V_{GS} = 0 V, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 1)		2.0		2.0		2.0	pF	V_{DS} = 10 V, V_{GS} = 0 V, V_G4 = 0 V, FREQ = 1 MHz
e_n	Equivalent Short Circuit Input Noise Voltage	Typ 10	25	Typ 10	25	Typ 10	25	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz
$V_{GS(f)}$	Gate-Source Forward Voltage (Note 1)		± 1.2		± 1.2		± 1.2	V	I_G = ±0.5 mA, V_{DS} = 0 V, V_D4 = 0 V
I_{G4}	Forward Gate Diodes Current (Note 2)	Typ ±1	±10	Typ ±1	±10	Typ ±1	±10	pA	V_G4 = ±100 mV
NF	Noise Figure		1.0		1.0		1.0	dB	V_{DS} = 15 V, V_{GS} = 0 V, R_{GEN} = 1 MEG, F = 1 kHz

NOTES: NBB

1. Measured when the gate lead is shorted to the 4th lead, i.e., characteristic of the FET only (V_G4 = 0 V).
2. Forward diodes' current when a voltage is applied between the gate and the 4th lead.

Device Available in Surface Mount (SOT-143)—Order Number = SST6908, SST6909, SST6910

n-channel JFET Amplifier *designed for . . .*

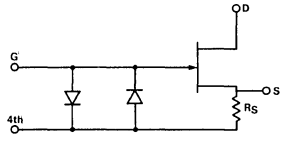
- **Infra-red Detector**
- **Micropower Pre-amplifier**
- **Transducer Impedance Converter**
- **Hearing Aid Pre-amplifier**

Siliconix

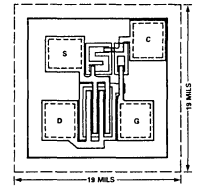
Performance Curves NBB See Section 4

BENEFITS

- **Reduces Component Count, Lower Circuitry Cost**
- **Input Over Voltage Clamp by Two Built-in Diodes**
- **Monolithic Source Resistor**
- **Low Noise**
- **Low Leakage**



TO-72



ABSOLUTE MAXIMUM RATINGS (25°C)

Maximum Supply Voltage (V_{DD}) ..... −30 V
Gate Current ..... 100 mA
Total Device Dissipation (25°C) ..... 300 mW
Storage Temperature Range ..... −55 to 200°C
Operating Temperature Range ..... −55 to 150°C
Power Derating ..... 2.4 mW/°C
Lead Temperature (10 seconds @ 1/16") ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic	Min	Typ	Max	Unit	Test Conditions
V_{GS}(oper)	Gate-Source Voltage	0.15		2.8	V	V_{DG} = 20 V, V_G4 = 0 V (Note 1)
I_D(oper)	Drain Current	5.0		85	μA	
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		10	25	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0 V FREQ = 100 Hz
I_{G4}	Forward Signal Current		±1	±10	pA	V_{GS} = ±100 mV
Av	Source Follower Gain (AV)	0.75	0.85		V/V	V_{DD} = 10 V, FREQ = 1 kHz
Z(in)	Input Impedance		100		GΩ	V_{GS} ≤ ±100 mV
Z(out)	Output Impedance	30	45	70	KΩ	V_{DD} = 10 V, FREQ = 1 kHz, V_G4 = 0 V (Note 1)
V_f	Forward Voltage			±1.0	V	I_G = ±0.5 mA, V_{DS} = 0 V, V_D4 = 0 V
I_G	Gate Leakage Current		1	25	pA	V_{DD} = 15 V, V_G4 = 0 V (Note 1)
NF	Noise Figure			1	dB	V_{DD} = 15 V, V_G4 = 0 V, R_{GEN} = 1 MΩ, F = 1 kHz

NOTE:
1. V_G4 = 0 V, Test Condition implies the gate and 4th lead are shorted.

NBB

Device Available in Surface Mount (SOT 143)—Order Number—SST6911

3

enhancement-type p-channel MOSFETs *designed for . . .*

Siliconix

Performance Curves MRA See Section 4

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke Detectors**
  - **pH Meters**
- **Digital Switching Interfaces**
- **Analog Switching**

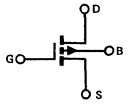
BENEFITS

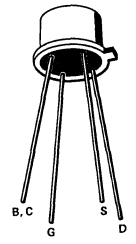
- Rugged MOS Gate Minimizes Handling Problems
  ±125 V Transient Capability
- Low Gate-Leakage
  Typically 0.02 pA
- High Off-Isolation as a Switch
  $I_{DSS} < 200$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source or Gate-Source Voltage 3N163 . . . . . -40 V
Drain-Source or Gate-Source Voltage 3N164 . . . . . -30 V
Transient Gate-Source Voltage (Note 1) . . . . . ±125 V
Drain Current . . . . . -50 mA
Storage Temperature . . . . . -65 to +200°C
Operating Junction Temperature . . . . . -55 to +150°C
Total Device Dissipation
(Derate 3.0 mW/°C to 150°C) . . . . . 375 mW
Lead Temperature 1/16" From Case For 10 Seconds . .265°C

TO-72
See Section 6





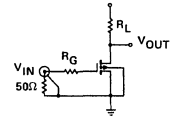
*ELECTRICAL CHARACTERISTICS (25°C and V_{BS} = 0 unless otherwise noted)

		Characteristic		3N163 Min	3N163 Max	3N164 Min	3N164 Max	Unit	Test Conditions	
1		I_{GSS}	Gate-Body Leakage Current		-10			pA	V_{GS} = -40 V, V_{DS} = 0	T_A = 125°C
2					-25					
3							-10		V_{GS} = -30 V, V_{DS} = 0	
4							-25			T_A = 125°C
5	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	I_D = -10 μA, V_{GS} = 0	
6		BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			I_S = -10 μA, V_{GD} = V_{BD} = 0	
7		V_{GS}	Gate Source Voltage	-3	-6.5	-2.5	-6.5		V_{DS} = -15 V, I_D = -0.5 mA	
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2	-5	-2	-5		V_{DS} = V_{GS}, I_D = -10 μA	
9		I_{DSS}	Drain Cutoff Current		-200		-400	pA	V_{DS} = -15 V, V_{GS} = 0	
10		I_{SDS}	Source Cutoff Current		-400		-800		V_{SD} = -20 V, V_{GD} = 0, V_{DB} = 0	
11		$I_{D(on)}$	ON Drain Current	-5	-30	-3	-30	mA	V_{DS} = -15 V, V_{GS} = -10 V	
12		$r_{DS(on)}$	Drain-Source ON Resistance		250		300	Ω	V_{GS} = -20 V, I_D = -100 μA	
13	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000	4,000	1,000	4,000	μmho	V_{DS} = -15 V, I_D = -10 mA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		250		250			
15		C_{iss}	Common-Source Input Capacitance		2.5		2.5	pF	V_{DS} = -15 V, I_D = -10 mA	f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		0.7		0.7			
17		C_{oss}	Common-Source Output Capacitance		3		3			
18	SW	$t_{d(on)}$	Turn-ON Delay Time		12		12	ns	V_{DD} = -15 V	
19		t_r	Rise Time		24		24		$I_{D(on)}$ = -10 mA	
20		t_{off}	Turn-OFF Time		50		50		R_G = R_L = 1.5 kΩ	

*JEDEC registered data

MRA

NOTE:
1. Transient gate-source voltage JEDEC registered as ±125 V.



INPUT PULSE	SAMPLING SCOPE
RISE TIME ≤ 2 ns	t_r ≤ 0.2 ns
PULSE WIDTH ≥ 200 ns	C_{IN} ≤ 2 pF
	R_{IN} ≥ 10 MΩ

n-channel JFETs *designed for . . .*

Siliconix

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NH
See Section 4

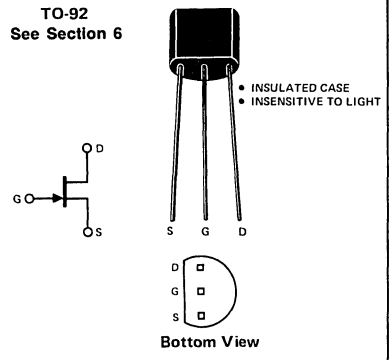
BENEFITS

- Wide Band
  High y_{fs}/C_{iss} Ratio
- Low Feedback Capacitance
  C_{rss} = 0.85 pF Typical
- Selected I_{DSS} and V_{GS} Ranges

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 30 V
Drain-Source Voltage . . . . . 30 V
Reverse Gate-Source Voltage . . . . . 30 V
Forward Gate Current . . . . . 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) . . . . . 200 mW
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage		−30			V	I_G = −1 μA, V_{DS} = 0
2		I_{GSS} Gate Reverse Current				−5	nA	V_{GS} = −20 V, V_{DS} = 0
3		I_{DSS} Saturation Drain Current		2		25	mA	V_{DS} = 15 V, V_{GS} = 0
4		I_{DSS} Selected into Following Groups (Note 2)	BF244A	2.0		6.5	mA	V_{DS} = 15 V, V_{GS} = 0
5			BF244B	6.0		15	mA	
6			BF244C	12		25	mA	
7		V_{GS} Corresponding to I_{DSS} groups	BF244A	−0.4		−2.2	V	V_{DS} = 15 V, I_D = 200 μA
8			BF244B	−1.6		−3.8	V	
9			BF244C	−3.2		−7.5	V	
10		$V_{GS(off)}$ Gate-Source Cutoff Voltage		−0.5		−8	V	V_{DS} = 15 V, I_D = 10 μA
11	DYNAMIC	g_{fs} Small-Signal Common-Source Forward Transconductance		3	5.5	6.5	mmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz
12		C_{rss} Common-Source Reverse Transfer Capacitance			0.85		pF	V_{DS} = 20 V, V_{GS} = −1 V
13		$\frac{1}{g_{is}}$ Input Resistance			25		kΩ	V_{DS} = 20 V, V_{GS} = −1 V, f = 100 MHz
14					10		kΩ	f = 200 MHz
15		C_{iss} Common-Source Input Capacitance			4		pF	V_{DS} = 20 V, V_{GS} = −1 V
16		C_{oss} Common-Source Output Capacitance			1.6		pF	V_{DS} = 20 V, V_{GS} = −1 V

NOTE:
1. Derate linearly to 125°C free-air temperature at the rate of 2.5 mW/°C.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NH

3

BF245A BF245B BF245C
PREFERRED PARTS 2N5484-6

n-channel JFETs designed for . . .

- VHF/UHF Amplifiers
- Oscillators
- Mixers

Siliconix

Performance Curves NH
See Section 4

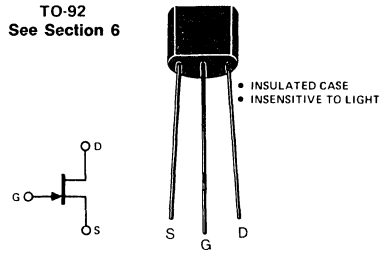
BENEFITS

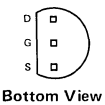
- Wide Band
  High y_{fs}/C_{iss} Ratio
- Low Feedback Capacitance
  C_{rss} = 0.85 pF Typical
- Selected I_{DSS} and V_{GS} Ranges

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 30 V
Drain-Source Voltage . . . . . 30 V
Reverse Gate-Source Voltage. . . . . 30 V
Forward Gate Current. . . . . 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) . . . . . 200 mW
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage		−30			V	I_G = −1 μA, V_{DS} = 0
2		I_{GSS} Gate Reverse Current				−5	nA	V_{GS} = −20 V, V_{DS} = 0
3		I_{DSS} Saturation Drain Current		2		25	mA	V_{DS} = 15 V, V_{GS} = 0
4		I_{DSS} Selected into Following Groups (Note 2)	BF245A	2 0		6 5	mA	V_{DS} = 15 V, V_{GS} = 0
5			BF245B	6.0		15	mA	
6			BF245C	12		25	mA	
7		V_{GS} Corresponding to I_{DSS} groups	BF245A	-0.4		-2.2	V	V_{DS} = 15 V, I_D = 200 μA
8			BF245B	1 6		−3.8	V	
9			BF245C	−3.2		-7 5	V	
10		$V_{GS(off)}$ Gate-Source Cutoff Voltage		−0 5		−8	V	V_{DS} = 15 V, I_D = 10 μA
11	DYNAMIC	g_{fs} Small-Signal Common-Source Forward Transconductance		3	5 5	6 5	mmho	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz
12		C_{rss} Common-Source Reverse Transfer Capacitance			0 85		pF	V_{DS} = 20 V, V_{GS} = 1 V
13		$\frac{1}{g_{is}}$ Input Resistance			25		kΩ	V_{DS} = 20 V, V_{GS} = −1 V, f = 100 MHz
14					10		kΩ	f = 200 MHz
15		C_{iss} Common-Source Input Capacitance			4		pF	V_{DS} = 20 V, V_{GS} = −1 V
16		C_{oss} Common-Source Output Capacitance			1 6		pF	V_{DS} = 20 V, V_{GS} = −1 V

NOTE: NH

1. Derate linearly to 125°C free-air temperature at the rate of 2 5 mW/°C
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%

n-channel JFETs *designed for . . .*

Siliconix

- **UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH See Section 4

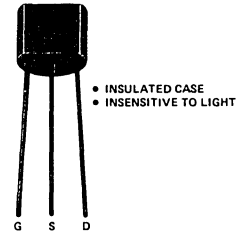
BENEFITS

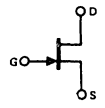
- High Gain
  G_{pg} = 14 dB Typical at 800 MHz
- Selected I_{DSS} Ranges

ABSOLUTE MAXIMUM RATINGS

Drain-Gate Voltage . . . . . 30 V
Drain-Source Voltage . . . . . 30 V
Reverse Gate-Source Voltage. . . . . 30 V
Forward Gate Current. . . . . 50 mA
Total Device Dissipation @ 25°C. . . . . 350 mW
Derate above 25°C . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 260°C

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DGO}	Drain-Gate Breakdown Voltage	−30			V	I_G = −1 μA, V_{DS} = 0	
2		I_{GSS}	Gate-Reverse Current			−5	nA	V_{GS} = −20 V, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5		−7.5	V	V_{DS} = 15 V, I_D = 10 nA	
4		I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	3	12	18	mA	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
5		I_{DSS}	Selected into Following Groups (Note 1) BF256LA	3		7	mA		
6			BF256LB	6		13	mA		
7			BF256LC	11		18	mA		
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4.5	5.5		mmho		
9		g_{os}	Common-Source Output Conductance		50		μmho		
10		C_{iss}	Common-Source Input Capacitance			4.5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.2	pF		
12		$f(y_{fs})$	Cutoff Frequency (Note 2)		1000		MHz		
13		G_{pg}	Common-Gate Neutralized Insertion Power Gain		14		dB	V_{DS} = 10 V, R_S = 47 Ω, f = 800 MHz	
14		NF	Noise Figure		7.5		dB	V_{DS} = 15 V, R_S = 47 Ω, f = 800 MHz	

NH

NOTES:
1. Pulse test PW ⩽ 300 μs, duty cycle ⩽ 2%.
2. Frequency at which the real part of the forward transconductance falls 3 dB relative to the value at 1 kHz.

current regulator diodes

designed for . . .

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

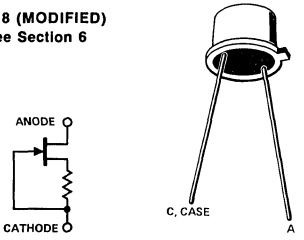
Siliconix

Performance Curves
NKL NKM NKO See Section 4

BENEFITS

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  Temperature Coefficient Better Than 3000 ppm/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  No Power Supplies Required
- 1V Operation

TO-18 (MODIFIED)
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at T_C = 25°C	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55° to +200°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	I_{F1}			Z_d		Z_k		V_L		POV	θ_1			GEOM
Parameter	Regulator Current			Dynamic Impedance		Knee Impedance		Limiting Voltage		Peak Operating Voltage	Temperature Coefficient (Typicals)			
Test Conditions	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)		V_F = 6 V		I_F = 0.8 $I_{F1(Min)}$ (Note 3)		I_F = 1.1 $I_{F1(Max)}$ (Note 4)	V_F = 25 V −55°C ≤ T_A ≤ 25°C	V_F = 25 V 0°C ≤ T_A ≤ 50°C	V_F = 25 V 25°C ≤ T_A ≤ 125°C	
Units	(mA)			MΩ		MΩ		Volts		Min Volts	Typ ppm/°C	Typ ppm/°C	Typ ppm/°C	
	Nom	Min	Max	Min	Typ	Min	Typ	Max	Typ					
CR022	0.22	0.198	0.242	9.0	11.5	2.75	3.6	1.0	0.38	100	+2600	+1900	+1220	NKL
CR024	0.24	0.216	0.264	8.0	10.4	2.35	3.3	1.0	0.41	100	+2400	+1650	+1050	
CR027	0.27	0.243	0.297	7.0	9.4	1.95	2.9	1.0	0.46	100	+2100	+1400	+800	
CR030	0.30	0.270	0.330	6.0	8.5	1.60	2.6	1.0	0.51	100	+1800	+1150	+600	
CR033	0.33	0.297	0.363	5.0	7.8	1.35	2.1	1.0	0.55	100	+1500	+950	+450	
CR039	0.39	0.351	0.429	4.10	6.9	1.00	2.0	1.05	0.65	100	+1050	+800	+150	
CR043	0.43	0.387	0.473	3.30	6.1	0.87	1.8	1.05	0.71	100	+800	+350	0	
CR047	0.47	0.423	0.517	2.70	5.6	0.75	1.6	1.10	0.77	100	+550	+150	−200	
CR056	0.56	0.504	0.616	1.90	5.0	0.56	1.3	1.20	0.91	100	+50	−250	−500	
CR062	0.62	0.558	0.682	1.55	4.4	0.47	1.15	1.30	1.00	100	−200	−450	−700	
CR068	0.68	0.612	0.748	1.35	8.5	0.400	1.70	1.15	0.70	100	250	−50	−375	NKM
CR075	0.75	0.675	0.825	1.15	7.2	0.335	1.50	1.20	0.75	100	200	−150	−475	
CR082	0.82	0.738	0.902	1.00	6.0	0.290	1.30	1.25	0.80	100	−25	−400	−550	
CR091	0.91	0.819	1.001	0.88	5.2	0.240	1.10	1.29	0.85	100	−200	−550	−675	
CR100	1.00	0.900	1.100	0.80	4.4	0.205	0.95	1.35	0.95	100	−425	−925	−825	
CR110	1.10	0.990	1.210	0.70	3.8	0.180	0.80	1.40	1.05	100	−450	−1000	−950	
CR120	1.20	1.08	1.32	0.64	3.3	0.155	0.71	1.45	1.15	100	−675	−1200	−1050	
CR130	1.30	1.17	1.43	0.58	3.2	0.135	0.60	1.50	1.25	100	−1050	−1300	−1150	
CR140	1.40	1.26	1.54	0.54	2.5	0.115	0.52	1.55	1.30	100	−1125	−1250	−1225	
CR150	1.50	1.35	1.65	0.51	2.2	0.105	0.46	1.60	1.35	100	−1150	−1225	−1275	
CR160	1.60	1.44	1.76	0.475	1.00	0.092	0.35	1.65	0.50	100	1300	875	400	NKO
CR180	1.80	1.62	1.98	0.420	0.95	0.074	0.30	1.75	0.55	100	1000	550	225	
CR200	2.00	1.80	2.20	0.395	0.88	0.061	0.25	1.85	0.60	100	725	250	0	
CR220	2.20	1.98	2.42	0.370	0.80	0.052	0.22	1.95	0.65	100	425	0	−225	
CR240	2.40	2.16	2.64	0.345	0.75	0.044	0.20	2.00	0.70	100	125	−225	−400	
CR270	2.70	2.43	2.97	0.320	0.68	0.035	0.18	2.15	0.75	100	−150	−425	−600	
CR300	3.00	2.70	3.30	0.300	0.60	0.029	0.14	2.25	0.85	100	−375	−550	−700	
CR330	3.30	2.97	3.63	0.280	0.56	0.024	0.13	2.35	0.90	100	−650	−750	−875	
CR360	3.60	3.24	3.96	0.265	0.52	0.020	0.11	2.50	0.95	100	−825	−850	−1000	
CR390	3.90	3.51	4.29	0.255	0.48	0.017	0.10	2.60	1.00	100	−925	−900	−1100	
CR430	4.30	3.87	4.73	0.245	0.45	0.014	0.09	2.75	1.10	100	−1025	−1000	−1200	
CR470	4.70	4.23	5.17	0.235	0.40	0.012	0.08	2.90	1.40	100	−1100	−1100	−1300	
CR530	5.30	4.77	5.83	0.220	0.35	0.010	0.05	3.10	1.70	100	−1200	−1200	−1400	

NOTES:
1 Pulse test—steady state currents may vary
2 Pulse test—steady state impedances may vary
3 Main V_F required to insure I_F > 0.8 $I_{F1(min)}$
4 Max V_F where I_F < 1.1 $I_{F1(max)}$ is guaranteed

current regulator diodes designed for . . .

Siliconix

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

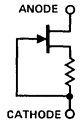
BENEFITS

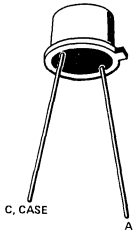
- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at T_C = 25°C	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55 to +200°C

TO-18 (MODIFIED)
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	POV	I_{F1}			Z_d		V_L	
Parameter	Peak Operating Voltage	Regulator Current			Dynamic Impedance		Limiting Voltage	
Test Conditions	$I_F = 1.1 I_{F1}$(Max) (Note 1)	V_F = 25 V (Note 2)			V_F = 25 V (Note 3)		$I_F = 0.8 I_{F1}$(Min) (Note 4)	
Units	Maximum Volts	(mA)			(mΩ)		(V)	
		Nom	Min	Max	Min	Typ	Max	Typ
CRR0240	100	0.240	0.180	0.300	5	13	1.0	0.5
CRR0360	100	0.360	0.270	0.450	2.5	9.5	1.05	0.7
CRR0560	100	0 560	0.420	0.700	1 2	6	1.30	1.1
CRR0800	100	0.800	0.600	1.000	0.8	5.2	1.35	0.85
CRR1250	100	1.250	0.937	1.560	0.5	2.5	1.60	1.3
CRR1950	100	1.950	1.460	2.440	0.37	0.8	1.95	0.65
CRR2900	100	2.900	2.160	3.600	0.28	0.56	2.35	0.9
CRR4300	100	4.300	3.240	5.400	0.22	0.35	3.00	1.45

NOTES:
1. Max V_F where $I_F < 1.1\ I_{F1}$ (max) is guaranteed.
2. Pulse test – steady state current may vary.
3. Pulse test – steady state impedances may vary.
4. Min V_F required to insure $I_F > 0.8\ I_{F1}$ (min).

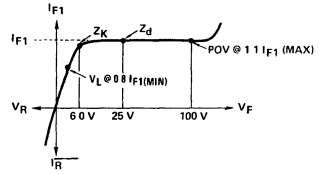
CRR0240-560 — NKL
CRR0800-1250 — NKM
CRR1950-4300 — NKO

3

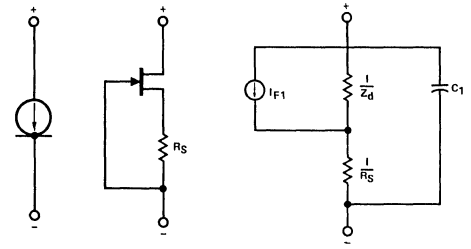
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

Current-Limiter Diode V-I Characteristic

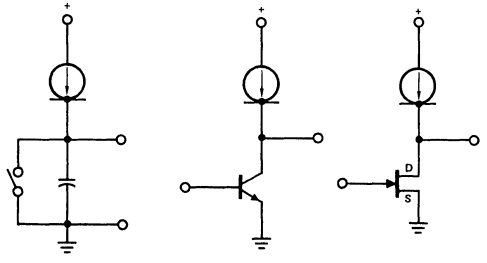


EQUIVALENT CIRCUIT

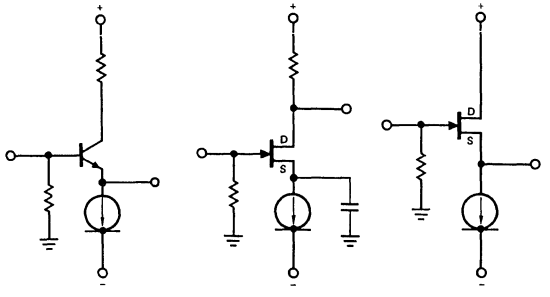


Constant-Current Timing Circuits

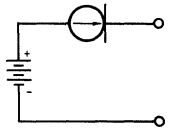
Collector or Drain Hi-Z Load Resistors



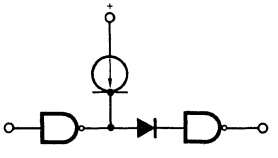
Emitter or Source Biasing



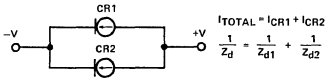
Constant-Current Supply or Current-Limiting Element



Logic Circuit Pull-Up Current Source

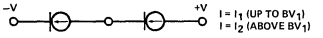


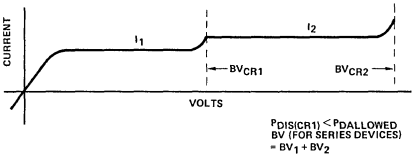
Parallel Operation



Series Operation

(When $I_1 < I_2$, that is $I_2 - I_1 < 0.2\ I_1$)





SYMBOLS AND DEFINITIONS

A	Anode (Drain)
C	Cathode (Source and Gate Shorted)
I_F	Forward Current (Anode Positive)
I_{F1}	Current at a specified Test Voltage, V_F
POV	Peak Operating Voltage
θ_I	Current Temperature Coefficient
θ_{JC}	Thermal Resistance Junction to Case
θ_{JA}	Thermal Resistance Junction to Ambient
Z_K	Knee AC Impedance at specified V_F. Z_K should be as high as possible and is specified as a minimum.
Z_d	Dynamic Impedance at specified V_F. Z_d is specified as a minimum.

matched dual n-channel JFETs *designed for . . .*

Siliconix

■ Wideband Differential Amplifiers

■ Commutators

Performance Curves NCB-D
See Section 4

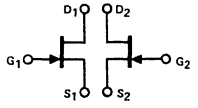
BENEFITS

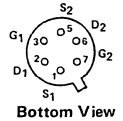
- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

ABSOLUTE MAXIMUM RATINGS (25°C)

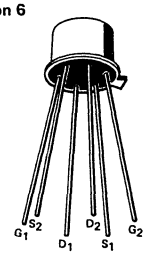
Gate–Gate Voltage ..... ±80 V
Gate-Drain or Gate-Source Voltage ..... -40 V
Gate Current ..... 50 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 2.2 mW/°C) ..... 325 mW
Total Device Dissipation, T_A = 25°C
(Derate 3.3 mW/°C) ..... 650 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

TO-71
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		2		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	50	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
				7000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance		65			f = 1 kHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		12			
12		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		DN5564 Min	DN5564 Max	DN5565 Min	DN5565 Max	DN5566 Min	DN5566 Max	Unit	Test Conditions	
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C, T_B = 125°C
					10		25		50			T_A = -55°C, T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

NCB-D

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B

3

matched dual n-channel JFETs *designed for...*

Siliconix

Performance Curves
NCB-D
See Section 4

■ Dual FET

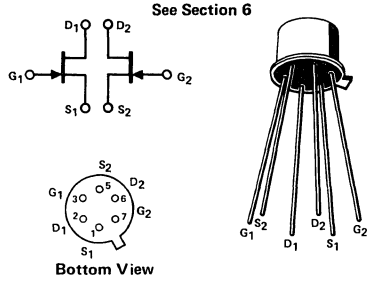
BENEFITS

- High Density
- Matched Switch Resistance
- Constant $r_{DS(on)}$ with Signal

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage . . . . . ±80 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 2.2 mW/°C) . . . . . 325 mW
Total Device Dissipation, T_A = 25°C
(Derate 3.3 mW/°C) . . . . . 650 mW
Storage Temperature Range . . . . . −65°C to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		−100	pA	V_{GS} = −20 V, V_{DS} = 0	
2					−200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40		V	I_G = 1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		2.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	60	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYN	C_{gd}	Drain-Gate Capacitance		7	pF	V_{GS} = −10 V	f = 1 MHz
9		C_{gs}	Gate-Source Capacitance		7		V_{DS} = 10 V	
10	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.9	1	–	V_{DS} = 15 V, V_{GS} = 0	
11		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		20	mV		
12		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.9	1	–		f = 1 kHz

NOTES: NCB-D

1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

dual pico ampere diodes *designed for . . .*

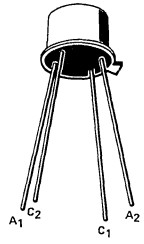
Siliconix

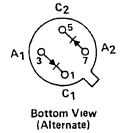
- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

- Very High Off-Isolation
  1 pA Max (DPAD1)
- High Isolation Between Diodes
  20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

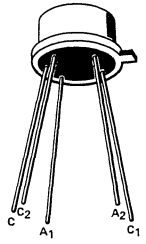
TO-71 (MODIFIED)
(Pins 2 and 6 Removed)
See Section 6

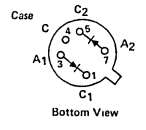




Bottom View
(Alternate)

TO-78 (MODIFIED)
(DPAD1 Only)
See Section 6





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

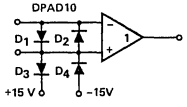
Forward Gate Current, Each Side. . . . . 50 mA
Total Device Dissipation @ T_A = 25°C
Derate 4.0 mW/°C to 125°C. . . . . 400 mW
Storage Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

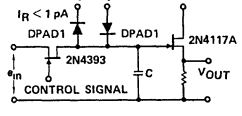
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION	
1	STATIC	I_R	Reverse Current			−1	pA	V_R = −20 V	DPAD1
2						−2			DPAD2
3						−5			DPAD5
4						−10			DPAD10
5						−20			DPAD20
6						−50			DPAD50
7						−100			DPAD100
8		B_{VR}	Reverse Breakdown Voltage	−45		−120	V	I_R = −1 μA	DPAD1, 2, 5
9				−35					DPAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		I_F = 1 mA	DPAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	V_R = −5 V, f = 1 MHz	DPAD1, 2, 5
12						2.0			DPAD10, 20, 50, 100
13	MAT	$\lvert C_{R1}-C_{R2}\rvert$	Differential Capacitance		0.1	0.2	pF	$V_{R1} = V_{R2}$ = −5 V, f = 1 MHz	DPAD1, 2, 5, 10, 20, 50, 100

APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS D_1 and D_2 Common mode input voltage limited by DPADS D_3 and D_4 to ±15 V.



Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



3

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NT
See Section 4

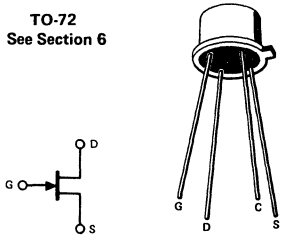
■ Ultra-High Input Impedance Amplifiers

Electrometers
pH Meters
Smoke Detectors

BENEFITS

- Low Current
  I_{DSS} < 0.15 mA (FN4117A)
- Minimum Circuit Loading
  I_{GSS} < 1 pA

TO-72
See Section 6



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -40 V
Gate-Current . . . . . 50 mA
Total Device Dissipation
(Derate 2 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 255°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		FN4117A		FN4118A		FN4119A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-2.5		-2.5		-2.5	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0 03	0.15	0.08	0.4	0.20	1.2	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	250	80	250	100	330	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		3		5		10			
8		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

NT

*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves NCB
See Section 4

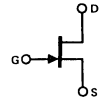
BENEFITS

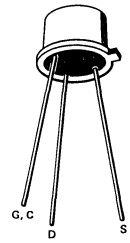
- Low Insertion Loss, High Accuracy in Test Systems r_{ON}
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . .300°C

TO-18
See Section 6



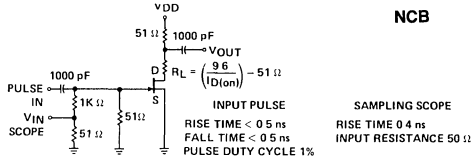


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		FN4392 Min	FN4392 Max	FN4393 Min	FN4393 Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0		
2					-200		-200	nA			150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$I_{D(off)}$	Drain Cutoff Current				100	pA	V_{DS} = 20 V	V_{GS} = -5 V	
5							200	nA			
6					100			pA			150°C
7					200			nA			
8		$V_{GS(f)}$	Gate-Source Forward Voltage		1		1	V	I_G = 1 mA, V_{DS} = 0		
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA		
10		I_{DSS}	Saturation Drain Current (Note 1)	25	100	5	60	mA	V_{DS} = 20 V, V_{GS} = 0		
11		$V_{DS(on)}$	Drain Source ON Voltage				0.4	V	V_{GS} = 0	I_D = 3 mA	
12					0.4					I_D = 6 mA	
13										I_D = 12 mA	
14		$r_{DS(on)}$	Static Drain-Source ON Resistance		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
15		$r_{ds(on)}$	Drain-Source ON Resistance		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
16	DYN	C_{iss}	Common-Source Input Capacitance		16		16	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
17		C_{rss}	Common-Source Reverse Transfer Capacitance				5		V_{DS} = 0	V_{GS} = - 5 V	
18					5					V_{GS} = - 7 V	
19										V_{GS} = -12 V	
20	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
21		t_r	Rise Time		5		5			$I_{D(on)}$	$V_{GS(off)}$	R_L
22		$t_{d(off)}$	Turn-OFF Delay Time		35		50		FN4392	6	-7	1.6KΩ
23		t_f	Fall Time		20		30		FN4393	3	-5	3.2KΩ

NOTE:
1 Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%

NCB



3

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

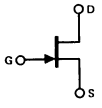
Performance Curves NVA See Section 4

BENEFITS

- Very Low Insertion Loss
  $r_{DS(on)} < 3\ \Omega$ (J105)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver

TO-92
See Section 6

Plastic



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J105			J106			J107			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0 V, V_{GS} = -15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	V_{DS} = 5 V, I_D = 1 μA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25				V_{DS} = 0 V, I_G = -1 μA	
4		I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	V_{DS} = 15 V, V_{GS} = 0 V	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6		$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	$V_{DS} \leq$ 0 1 V, V_{GS} = 0 V	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0 V, V_{GS} = -10 V	f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35			
9		$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		V_{DS} = V_{GS} = 0 V	
10		$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions	
11		t_r	Rise Time		20			20			20				
12		$t_{d(off)}$	Turn Off Delay Time		15			15			15				
13		t_f	Fall Time		20			20			20				

Switching Time Test Conditions	J105	J106	J107
V_{DD}	1.5 V	1 5 V	1 5 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	50 Ω	50 Ω	50 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NVA

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NIP See Section 4

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

BENEFITS

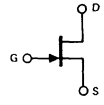
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $r_{DS(on)} < 8\ \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 5$ ns Typical
- Low Noise
  $\overline{e_n} = 6\ nV/\sqrt{Hz}$ at 10 Hz, Typ (J110)

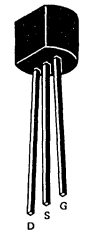
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25° C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . .300°C

Plastic

TO-92
See Section 6





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J108 Min	J108 Typ	J108 Max	J109 Min	J109 Typ	J109 Max	J110 Min	J110 Typ	J110 Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–3'			–3			–3	nA	$V_{DS} = 0$ V, $V_{GS} = -15$ V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–3		–10	–2		–6	–0 5		–4	V	$V_{DS} = 5$ V, $I_D = 1\ \mu$A
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	$V_{DS} = 0$ V, $I_G = -1\ \mu$A
4	STATIC	I_{DSS}	Drain Saturation Current (Note 2)	80			40			10			mA	$V_{DS} = 15$ V, $V_{GS} = 0$ V
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance J110A			8			12			18 25	Ω	$V_{DS} \leq 0\ 1$ V, $V_{GS} = 0$ V
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85	pF	$V_{DS} = V_{GS} = 0$; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		1			1			1		ns	J108 / J109 / J110
12	DYNAMIC	$t_{d(off)}$	Turn OFF Delay Time		6			6			6		ns	V_{DD} 1 5 V / 1.5 V / 1.5 V
13	DYNAMIC	t_f	Fall Time		30			30			30		ns	$V_{GS(off)}$ –12 V / –7 V / –5 V
														R_L 150 Ω / 150 Ω / 150 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs, duty cycle ≤ 3%

NIP

3

n-channel FETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NCB
See Section 4

BENEFITS

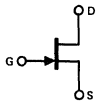
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –35V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

Plastic

TO-92
See Section 6



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111 Min	J111 Typ	J111 Max	J112 Min	J112 Typ	J112 Max	J113 Min	J113 Typ	J113 Max	UNIT	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–1			–1			–1	nA	V_{DS} = 0 V, V_{GS} = –15 V
2	STATIC	$V_{GS(off)}$	Gate Source Cutoff Voltage	–3		–10	–1		–5			–3	V	V_{DS} = 5 V, I_D = 1 μA
3	STATIC	BV_{GSS}	Gate Source Breakdown Voltage	35			35			–35			V	V_{DS} = 0 V, I_G = –1 μA
4	STATIC	I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	V_{DS} = 15 V, V_{GS} = 0 V
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			–1			–1			–1	nA	V_{DS} = 5 V, V_{GS} = –10 V
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	V_{DS} = 0 1 V, V_{GS} = 0 V
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0 V, V_{GS} = –10 V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0 V, V_{GS} = –10 V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28	pF	V_{DS} = V_{GS} = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		6			6			6		ns	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		20			20			20		ns	
13	DYNAMIC	t_f	Fall Time		15			15			15		ns	

Switching Time Test Conditions	J111	J112	J113
V_{DD}	10 V	10 V	10 V
$V_{GS(off)}$	–12 V	–7 V	–5 V
R_L	800 Ω	1,600 Ω	3,200 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

NCB

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NCB See Section 4

- **Analog Switches**
- **Choppers**
- **Commutators**

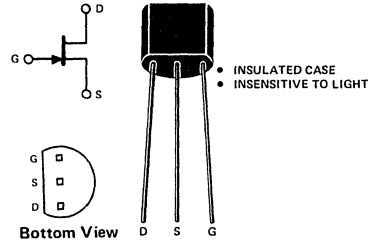
BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (J111A)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- No Error or Offset Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Drain Current . . . . . 400 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 350 mW
Power Derating . . . . . 3.27 mW/°C
Storage Temperature Range . . . . . −55 to +150°C
Operating Temperature . . . . . −55 to +135°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111A Min	J111A Max	J112A Min	J112A Max	J113A Min	J113A Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)		−200		−200		−200	pA	V_{DS} = 0, V_{GS} = −15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5	−10	−2	−7	−1	−5	V	V_{DS} = 5 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	V_{DS} = 0, I_G = −1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	30		15		8		mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)		200		200		200	pA	V_{DS} = 5 V, V_{GS} = −10 V	
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance		30		50		80	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYN	$C_{dg(off)}$	Drain Gate OFF Capacitance		5		5		5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
8	DYN	$C_{sg(off)}$	Source-Gate OFF Capacitance		5		5		5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
9	DYN	$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance		28		28		28	pF	$V_{DS} = V_{GS}$ = 0	f = 1 MHz

NOTES: NCB
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

J174 J175 J176 J177
(SURFACE MOUNT EQUIV. = SST 174, 175, 176, 177)

p-channel JFETs designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves PSA/PSB/PSC See Section 4

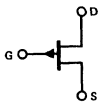
BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when Combined with J113, its N-Channel Complement
- Low Insertion Loss
  $r_{DS(on)} < 85\ \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)} < 5.5$ pF
  $C_{dg(off)} < 5.5$ pF
- Fast Switching
  $t_{d(on)} + t_r = 7$ ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6



Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristics	J174 Min	J174 Typ	J174 Max	J175 Min	J175 Typ	J175 Max	J176 Min	J176 Typ	J176 Max	J177 Min	J177 Typ	J177 Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20 V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15 V, I_D = -10 nA
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1 μA
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-20		-135	-7		-70	-2		-35	-1.5		-20	mA	V_{DS} = -15 V, V_{GS} = 0
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15 V, V_{GS} = 10 V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1 V
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance		32			32			32			32		pF	$V_{DS} = V_{GS}$ = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		5			10			20			25		ns	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		5			10			15			20		ns	
13	DYNAMIC	t_f	Fall Time		10			20			20			25		ns	

Switching Time Test Conditions	J174	J175	J176	J177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.

PSA/PSB/PSC

n-channel JFETs *designed for . . .*

Siliconix

■ General Purpose Amplifiers

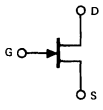
Performance Curves NPA
See Section 4

BENEFITS

- **High Input Impedance**
  I_G = 10 pA Typical
- **Good for Low Power Supply Operation**
  $V_{GS(off)}$ < 1.5V (J201)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate Current ..... 50 mA
Total Device Dissipation at 25° C Ambient
(Derate 3.27 mW/°C)..... 360 mW
Operating Temperature Range.....–55 to 135°C
Storage Temperature Range.....–55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) .....300°C



Plastic

Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J201			J202			J203			J204			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-100			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2	STATIC	$V_{GS(off)}$	Gate Source Cutoff Voltage	-0 3		-1 5	-0 8		-4 0	-2 0		-10 0	–0 3		-2 0	V	V_{DS} = 20 V, I_D = 10 nA	
3	STATIC	BV_{GSS}	Gate Source Breakdown Voltage	-40			-40			-40			-25				V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	0 2		1 0	0 9		4 5	4 0		20	0 2	1 2	3	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		–10			–10			–10			–10		pA	V_{DG} = 20 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 3)	500			1,000			1,500			500	1500		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common Source Output Conductance		1			3 5			10			2 5				
8	DYNAMIC	C_{iss}	Common Source Input Capacitance		4			4			4			4		pF		f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1			1				
10	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		5			5			5			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES: **NPA**

1 Geometry is symmetrical. Units may be operated with source and drain leads interchanged
2 Approximately doubles for every 10°C increase in T_A
3 Pulse test duration = 2 ms

n-channel JFETs *designed for . . .*

Siliconix

■ General Purpose Amplifiers

Performance Curves NZF
See Section 4

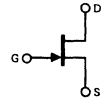
BENEFITS

- High Gain
  g_{fs} = 7000 μmho Minimum
  (J211, J212)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

TO-92
See Section 6

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C



Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J210			J211			J212			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2.5		-4.5	-4		-6	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	V_{DS} = 15 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 1 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	6,000		12,000	7,000		12,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			150			200			200			
8		C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
10		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NZF

n-channel JFETs *designed for . . .*

Siliconix

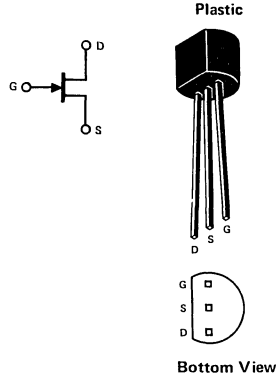
Performance Curves NPA See Section 4

■ Audio and Sub-Audio Amplifiers

BENEFITS

- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

TO-92
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . –40V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J230			J231			J232			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-250			-250			-250	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0 5		-3	-1 5		-5	-3		-6	V	V_{DS} = 20 V, I_D = 1 μA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40				V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	0.7		3	2		6	5		10	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		–2			–2			–2		pA	V_{DG} = 10 V, I_D = 0.5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1,000		3,500	1,500		4,000	2,500		5,000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance		1.5			3			5				
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
10	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		8	30		8	30		8	30	nV/$\sqrt{Hz}$	V_{DS} = 10 V, V_{GS} = 0	f = 10 Hz
11	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		2			2			2		nV/$\sqrt{Hz}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES:
1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

NPA

p-channel JFETs *designed for . . .*

■ General Purpose Amplifiers

Siliconix

Performance Curves
PSA/PSB/PSC
See Section 4

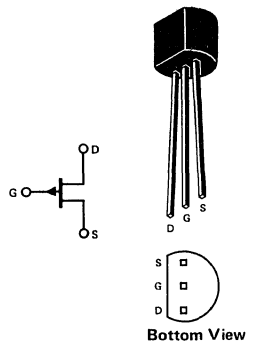
BENEFITS

- **Low Cost**
- **Automatic Insertion Package**
- **High Gain Amplifiers**
  g_{fs} = 14,000 μmho Typical (J271)
- **Low Noise**
  $\overline{e_n}$ = 6 nV/$\sqrt{Hz}$ at 1 kHz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . –50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6
Plastic



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J270 Min	J270 Typ	J270 Max	J271 Min	J271 Typ	J271 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2 0	1.5		4.5	V	V_{DS} = -15 V, I_D = -1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			V	V_{DS} = 0, I_G = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-2		-15	-6		-50	mA	V_{DS} = -15 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = -15 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	μmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			200			500	μmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		32			32		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		4			4		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	e_n	Equivalent Short-Circuit Input Noise Voltage		6			6		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = -10 V, I_D = $I_{DSS(min)}$	f = 1 kHz

NOTES: PSA/PSB/PSC

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs *designed for . . .*

Siliconix

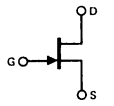
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

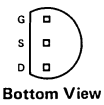
Performance Curves NZF
See Section 4

BENEFITS

- High Power Gain
  20–23 dB Typical at 100 MHz, Common-Source
  17.5–20.5 dB Typical at 100 MHz, Common-Gate
- Low Noise Figure
  1.3 dB Typical at 100 MHz
- High Dynamic Range
  Greater than 100 dB

TO-92
See Section 6





Bottom View

Plastic

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.5	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.1	μA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 1)	–1.5	–7.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1, 2)	4	45	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	9000	μmho	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	
7		g_{os}	Common-Source Output Conductance		200			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.7	pF	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	
9		C_{iss}	Common-Source Input Capacitance		5.5			

Characteristic		J300A		J300B		J300C		J300D		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{DSS} (Note 2)	Saturation Drain Current	4	9	7	15	12	25	21	45	mA	V_{DS} = 10V V_{GS} = 0V
$V_{GS(off)}$	Gate Source Cutoff Voltage	–1.5	–3.0	–2.0	–4.0	–2.5	–5.0	–3.5	–7.0	V	V_{DS} = 10V I_D = 1nA

NOTES:
1. I_{DSS} and $V_{GS(off)}$ are selected into 5 ranges and labeled according to above table.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NZF

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

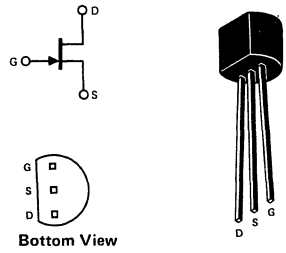
Siliconix

Performance Curves NH See Section 4

BENEFITS

- Characterized for Operation at 100 and 400 MHz
- Low Noise
  NF = 1.7 dB Typical at 100 MHz

TO-92
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J304			J305			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2	STATIC	$V_{GS(off)}$	Gate Source Cutoff Voltage	-2		-6	-0 5		-3	V	V_{DS} = 15 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate Source Breakdown Voltage	-30			-30				V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6	DYNAMIC	g_{os}	Common-Source Output Transconductance			50			50			
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
8	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		0.85			0.85				
9	DYNAMIC	C_{oss}	Common-Source Output Capacitance		1 0			1.0				
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
11	HIGH FREQUENCY				4,200							f = 400 MHz
12	HIGH FREQUENCY	g_{oss}	Common-Source Output Conductance		60			60				f = 100 MHz
13	HIGH FREQUENCY				80							f = 400 MHz
14	HIGH FREQUENCY	b_{oss}	Common-Source Output Susceptance		800			800				f = 100 MHz
15	HIGH FREQUENCY				3,600							f = 400 MHz
16	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		80			80				f = 100 MHz
17	HIGH FREQUENCY				800							f = 400 MHz
18	HIGH FREQUENCY	b_{iss}	Common-Source Input Susceptance		2,000			2,000				f = 100 MHz
19	HIGH FREQUENCY				7,500							f = 400 MHz
20	HIGH FREQUENCY	G_{ps}	Common-Source Power Gain		20					dB	V_{DS} = 15 V, I_D = 5 mA	f = 100 MHz
21	HIGH FREQUENCY				11							f = 400 MHz
22	HIGH FREQUENCY	NF	Noise Figure (Single Sideband)		1.7						V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ	f = 100 MHz
23	HIGH FREQUENCY				3.8							f = 400 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

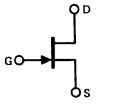
Siliconix

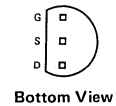
Performance Curves NZB
See Section 4

BENEFITS

- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

TO-92
See Section 6





Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J308			J309			J310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25			V	I_G = −1 μA, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current			−1 0			−1 0			−1 0	nA	V_{GS} = −15 V, V_{DS} = 0	
3	STATIC	I_{GSS}	Gate Reverse Current			−1 0			−1 0			−1 0	μA	V_{GS} = −15 V, V_{DS} = 0	T = +125°C
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1 0		−6 5	−1 0		−4 0	−2 0		−6 5	V	V_{DS} = 10 V, I_D = 1 nA	
5	STATIC	I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6	STATIC	$V_{GS(f)}$	Gate-Source Forward Voltage			1 0			1 0			1 0	V	V_{DS} = 0, I_G = 1 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000	17,000		10,000	17,000		8,000	17,000		μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8	DYNAMIC	g_{os}	Common-Source Output Conductance			250			250			250	μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
9	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000		μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
10	DYNAMIC	g_{og}	Common-Gate Output Conductance		150			100			150		μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
11	DYNAMIC	C_{gd}	Gate-Drain Capacitance		1 8	2 5		1 8	2 5		1 8	2 5	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
12	DYNAMIC	C_{gs}	Gate-Source Capacitance		4 3	5 0		4 3	5 0		4 3	5 0	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
15	HI FREQ	$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
16	HI FREQ	$Re(y_{is})$	Common-Source Input Conductance		0 4			0 4			0 4		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
17	HI FREQ	$Re(y_{os})$	Common-Source Output Conductance		0 15			0 15			0 15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
18	HI FREQ	G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
19	HI FREQ	NF	Noise Figure		1 5			1 5			1 5		dB	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
20	HI FREQ	G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11		dB	V_{DS} = 10 V, I_D = 10 mA	f = 450 MHz
21	HI FREQ	NF	Noise Figure		2 7			2 7			2 7		dB	V_{DS} = 10 V, I_D = 10 mA	f = 450 MHz

NOTE.
1 Pulse test PW 300 μs, duty cycle ≤ 3%

NZB

n-channel JFETs current regulator diodes

Siliconix

designed for . . .

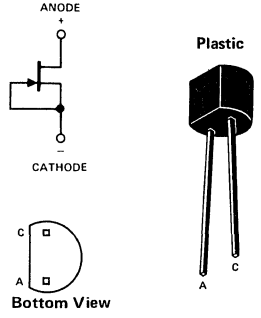
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

Performance Curves NCL See Section 4

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

TO-92 (MODIFIED)
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . . 50 V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

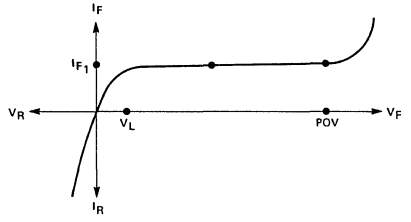
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			J500	J501	J502	J503	J504	J505	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	0.192	0.264	0.344	0.448	0.600	0.800	mA	V_F = 25 V
2				Nominal	0.240	0.330	0.430	0.560	0.750	1.000		
3				Max	0.288	0.396	0.516	0.672	0.900	1.200		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	I_F = 1.1 I_{FI} (Max)
5		V_L	Limiting Voltage (Note 3)	Max	1.2	1 3	1 5	1.7	1.9	2.1		I_F = 0.9 I_{FI} (Min)
6				Typ	0 8	0.9	1.1	1.2	1.4	1.5		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	4.0	2 2	1 5	1 2	0.8	0 5	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	8.0	6.0	4.4	3.4	2.5	1.9		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NOTES:
1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

NCL

Current-Limiter Diode
V-I Characteristic



n-channel JFETs current regulator diodes *designed for . . .*

Siliconix

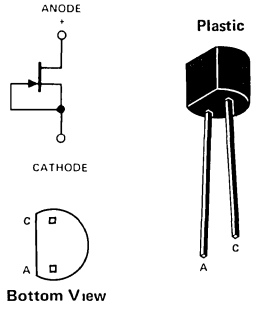
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

Performance Curves NCL See Section 4

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

TO-92 (MODIFIED) See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . . 50 V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

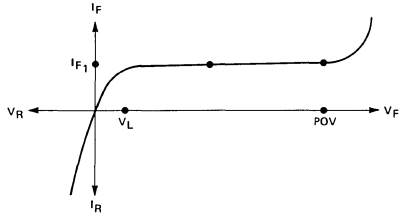
			Characteristic		J506	J507	J508	J509	J510	J511	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	1 120	1.440	1.9	2 4	2 9	3.8	mA	V_F = 25 V
2				Nominal	1.400	1.800	2 4	3.0	3.6	4.7		
3				Max	1.680	2.160	2 9	3.6	4 3	5.6		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	I_F = 1 1 I_{FI} (Max)
5		V_L	Limiting Voltage (Note 3)	Max	2.5	2.8	3 1	3.5	3 9	4.2		I_F = 0 9 I_{FI} (Min)
6				Typ	1.8	2 0	2.2	2.5	2 8	3.0		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	0 33	0 2	0 2	0.15	0 15	0 12	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	1.4	1.0	0.70	0 60	0.50	0.30		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NOTES

1 Pulse test duration = 2 ms
2 Maximum V_F where $I_F < 1\ 1\ I_{FI(Max)}$ is guaranteed
3. Minimum V_F required to insure $I_F > 0\ 9\ I_{FI(Min)}$

NCL

Current-Limiter Diode
V-I Characteristic



n-channel JFETs current regulator diodes

Siliconix

designed for . . .

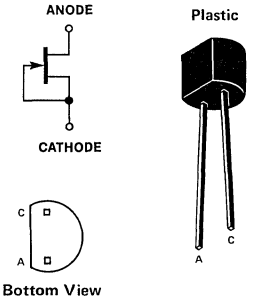
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

Performance Curves NKL, VRMA
See Section 4

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources
  No Power Supplies Required

TO-92 (MODIFIED)
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage 100V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.27 mW/°C
Storage Temperature Range . . . . . –55 to 135°C
Operating Temperature Range . . . . . –55 to 135°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	Min	Typical	Max	Unit	Test Conditions
1	STATIC	I_{F1}	Forward Current (Note 1)			770	μA	V_F = 100 V
2				250		700		V_F = 25 V
3				200		—		V_F = 1.0 V
4		POV	Peak Operating Voltage (Notes 1 and 2)	100			V	I_F = 1•d I_{FI} (Max)
5		V_L	Limiting Voltage (Note 3)		1.1	1 5		I_F = 0 9 I_{FI} (Min)
6								
7	DYN	Z_{F1}	Small-Signal Dynamic Impedance (Note 1)	1.0	4 4		MΩ	V_F = 25 V, f = 1 kHz
8								
9		C_F	Anode-Cathode Capacitance		2		pF	V_F = 25 V, f = 1 MHz

NOTES:
1 Pulse test duration = 2 ms
2. Maximum V_F where $I_F < 1\ 1\ I_{F1(Max)}$ is guaranteed
3. Minimum V_F required to insure $I_F > 0\ 9\ I_{F1(Min)}$

NKL, VRMA

current regulator diodes designed for . . .

Siliconix

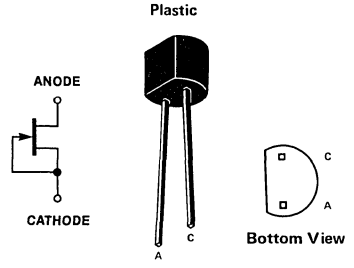
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

Performance Curves NCL
See Section 4

BENEFITS

- Simple Two Lead Current Source
- In Low Cost Plastic Package
- Simplifies Floating Current Sources No Power Supplies Required

TO-92 (MODIFIED)
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . . 50 V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Regulator Current			Limiting Voltage		Peak op Volt	Dynamic Impedance	Knee Impedance
	V_F=25V			I_F=0.8 $I_{FI(min)}$ I_{FF} 1.1				
PART NUMBER	I_F NOM	I_F MIN	I_F MAX	V_L	V_L	V_{OP}	'ZD	'ZK
	Nominal mA	Min mA	Max mA	Max Volts	Typical	I_{FI} (Max) Min Volts	Typical Megohms	Typical Megohms
J553	0 5	0 18	0.75	1 3	0 75	50	10	2
J554	1 0	0.6	1 6	1.75	0 55	50	1	1
J555	2.0	1 4	2.6	2.15	0 75	50	88	0 25
J556	3 0	2.4	3 8	2.6	0 75	50	6	0 14
J557	4 5	3 6	5 3	3 0	1 5	50	48	0 09

NOTES:
1 Pulse test—steady state currents may vary.
2. Pulse test—steady state impedance may vary.
3 Min V_F required to insure I_F>0 8 I_{F1} (min).
4 Max V_F where I_F < 1 1 $I_{F1(max)}$ is guaranteed.

NCL

3

low-leakage pico-amp diodes *designed for . . .*

Siliconix

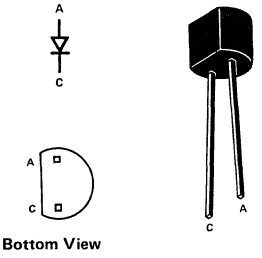
- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

BENEFITS

- Low Cost

TO-92 (MODIFIED)
See Section 6

Plastic



ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . . 10 mA
Total Device Dissipation . . . . . 360 mW
Storage Temperature Range . . . . . –65°C to +135°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic			Min	Typ	Max	Unit	Test Conditions
1	STATIC	I_R	Reverse Current (Note 1)	JPAD5			–5	pA	V_R = –20 V
				JPAD10			–10		
				JPAD20			–20		
				JPAD50			–50		
				JPAD100			–100		
				JPAD200			–200		
				JPAD500			–500		
2		BV_R	Breakdown Voltage (Reverse)		–35	–80		V	I_R = –1 μA
3		V_F	Forward Voltage Drop			0.8	1.5	V	I_F = 5 mA
4	DYN	C_R	Capacitance			1.5	2.0	pF	V_R = –5 V, f = 1 MHz

NOTE:
1. The JPAD type number denotes its maximum reverse current value in pico amps. Devices with I_R values intermediate to those shown are also available on request.

high voltage protection diode

designed for. . .

- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

Siliconix

Performance Curves VRMA
See Section 4

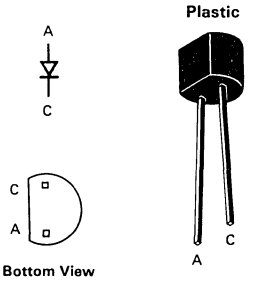
BENEFITS

- Offers High Voltage Protection
- Broad Current Range

ABSOLUTE MAXIMUM RATINGS (25°C)

Anode to Cathode Voltage
JR135V 135V
JR170V 170V
JR200V 200V
JR220V 220V
JR240V 240V
Forward Diode Current I_F 20mA
Reverse Diode Current I_F 50mA
Power Dissipation P_D 360mW
(Derate 3.27mW/°C)
Storage Temperature T_{STG} . . . . . −55°C to 150°C
Operating Temperature T_{OP} . . . . . −55°C to 135°C

TO-92 (MODIFIED)
See Section 6



ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	P_{OV}	Peak Operating Voltage[1]	JR135V	135			V	$I_F = 1mA$
			JR170V	170				
			JR200V	200				
			JR220V	220				
			JR240V	240				
2	I_F[1]	Forward Current		200			μA	$V_F = 2V$
	I_F[2]			200		770		$V_F = 100V$
3	V_L	Limiting Current				0.9	V	$I = 0.8\ I_F$[1] (min)
4	Z_D	Dynamic Impedance			2		MΩ	$V_F = 25V$
5	$\Delta I_F/\Delta T$	I_F Temp Coefficient			+0.6		%/°C	$V_F = 2\text{-}100V$
								$T_A = -20$ to $+85°C$

NOTE:
1. Pulse test duration 2 ms.

VRMA

3

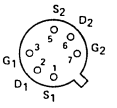
monolithic dual n-channel JFET *designed for . . .*

Siliconix

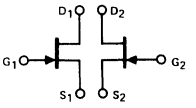
Performance Curves NNZ
See Section 4

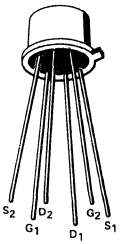
- **Hybrid Circuits**
- **Wideband Differential Amplifiers**
- **VHF/UHF Amplifiers**

TO-71
See Section 6



Bottom View





TO-71 = M440, M441

BENEFITS

- High Gain through 100 MHz
  $g_{fs} > 4500$ μmho
- Low Insertion Loss
- Tight Tracking

ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-Drain or Gate Source Voltage ..... –25 V
Gate Current ..... 50 mA

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		M440			M441			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500			-500	pA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	-1		-6	V	V_{DS} = 10 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)			-500			-500	pA	V_{DG} = 10 V, I_D = 5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			200			200	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		50			50		pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		12			12		pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
10	MAT	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20	mV	V_{DG} = 10 V, I_D = 5 mA	

NNZ

NOTES:
1. Approximately doubles for every 10°C increase in T_A
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.

monolithic dual n-channel JFETs

designed for . . .

- **Hybrid Circuits**
- **Wideband Differential Amplifiers**
- **VHF/UHF Amplifiers**

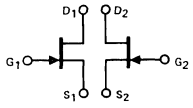
Siliconix

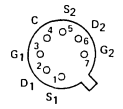
Performance Curves NNZ
See Section 4

BENEFITS

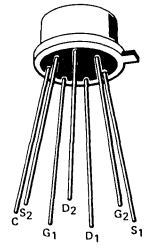
- High Gain through 100 MHz
  $g_{fs} > 5000\ \mu mho$
- Low Insertion Loss
- Tight Tracking

TO-78
See Section 6





Bottom View



TO-78 = M5911, M5912

ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-Drain or Gate Source Voltage ..... −25 V
Gate Current ..... 50 mA

*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0 3	-4			
6		I_G	Gate Operating Current		-100	pA	V_{DG} = 10 V, I_D = 5 mA	
					-100	nA		T_A = 125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1 2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K

		Characteristic		M5911 Min	M5911 Max	M5912 Min	M5912 Max	Unit	Test Conditions	
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	T_A = 125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0 95	1	0 95	1	–	V_{DS} = 10 V, V_{GS} = 0	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
19		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3) (Guarantee-no test)		20		40	μV/°C		T_A = 25°C T_B = 125°C
20					20		40			T_A = -55°C T_B = 25°C
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0 95	1	0 95	1	–		f = 1 kHz

*JEDEC registered data

NNZ

NOTES:
1 Pulsewidth ≤ 300 μs, duty cycle ≤ 3%
2 Assumes smaller value in numerator
3 Measured at end points, T_A and T_B

enhancement-type p-channel MOSFET *designed for . . .*

Siliconix

Performance Curves MRA See Section 4

- **High-Input Impedance Amplifiers**
  - **Smoke Detectors**
  - **Electrometers**
  - **pH Meters**

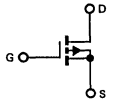
BENEFITS

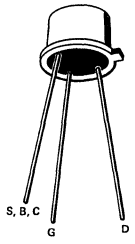
- High Input Impedance
  I_{GSS} = 30 Femto Amp Typical
- High Gain
  g_{fs} = 1000 μmho Minimum

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage . . . . . 25 V
Gate-Source Voltage . . . . . ±10 V
Drain Current . . . . . 30 mA
Total Device Dissipation at (Or Below) T_A = 25°C
(Derate 3 mW/°C to +150°C) . . . . . 375 mW
Operating Junction Temperature. . . . . −55 to +150°C
Storage Temperature. . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 265°C

TO-18
See Section 6





ELECTRICAL CHARACTERISTICS (25°C)

			Characteristic	Min	Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate-Source Leakage Current		−1.0	pA	V_{GS} = −10 V, V_{DS} = 0
2		BV_{DSS}	Drain-Source Breakdown Voltage	−25		V	I_D = −10 μA, V_{GS} = 0
3		V_{GS}	Gate-Source Voltage	−2.0	−6.0	V	V_{DS} = −10 V, I_D = −10 μA
4		I_{DSS}	Drain Cutoff Current		−20	nA	V_{DS} = −10 V, V_{GS} = 0
5		$I_{D(on)}$	ON Drain Current	−3.0		mA	V_{DS} = −10 V, V_{GS} = −10 V
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		μmhos	V_{DS} = −10 V, I_D = −2 mA, f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		6.0	pF	V_{DS} = −10 V, V_{GS} = −10 V, f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		

MRA

n-channel JFET
designed for . . .

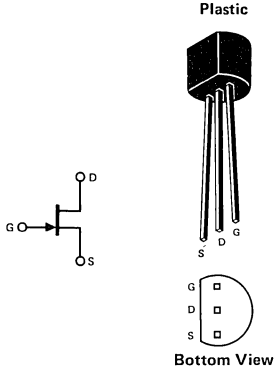
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Siliconix

Performance Curves NH/NRL
See Section 4

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–2.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–2.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–8.0		V_{DS} = 15 V, I_D = 2 nA	
5		I_{DSS}	Saturation Drain Current	2.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6		V_{GS}	Gate-Source Voltage	–0.5	–7.5	V	V_{DS} = 15 V, I_D = 200 μA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0			

NOTE:
1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH/NRL

3

n-channel JFET
designed for . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

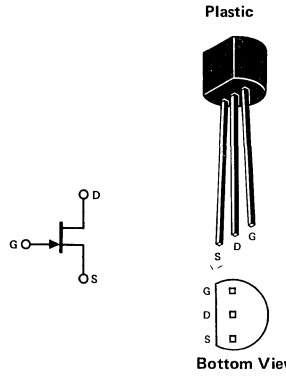
Siliconix

Performance Curves NH/NRL See Section 4

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 6

Plastic



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–1.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	i_G = –10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5	–8.0		V_{DS} = 15 V, I_D = 10 μA	
5		I_{DSS}	Saturation Drain Current	1.5	24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.5	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.5			
13		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
14					3.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 100 MHz

NOTE: NH/NRL
1. Pulse test, pulse width = 300 μs, duty cycle ≤ 3%.

n-channel JFET
designed for . . .

Siliconix

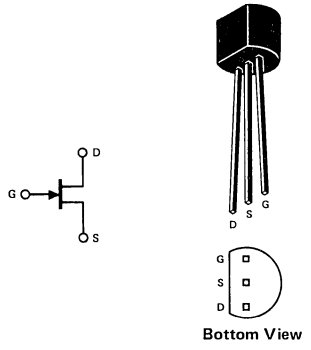
Performance Curves NRL/ NPA/NH See Section 4

- **General Purpose Amplifiers**
- **Analog Switches**

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 6

Plastic



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.01	–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25	–60		V	I_G = –10 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.2		–8.0	V	V_{DS} = 15 V, I_D = 10 μA	
4	STATIC	I_{DSS}	Saturation Drain Current	0.5		24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	800		6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6	DYNAMIC	g_{os}	Common-Source Output Conductance		10	75	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5	7.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
8	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
9		NF	Noise Figure		0.04	2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

NOTE:
1. Pulse test PW ≤ 630 ms, duty cycle ≤ 10%.

NRL/NPA/NH

3

n-channel JFET *designed for . . .*

- **General Purpose Amplifiers**
- **Analog Switches**

Siliconix

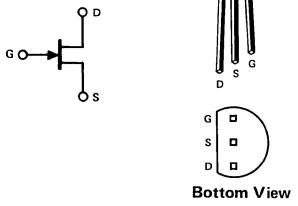
Performance Curves NRL/ NPA/NH See Section 4

BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 6

Plastic



Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage 20V
Source-Gate Voltage 20V
Drain-Source Voltage. 20V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		–.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–20			V	I_G = –10 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0		V_{DS} = 10 V, I_D = 1 μA	
4		I_{DSS}	Saturation Drain Current	0.5		20	mA	V_{DS} = 10 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	500			μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Conductance		10				
7		C_{iss}	Common-Source Input Capacitance		4.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0				

NRL/NPA/NH

NOTE:
1. Pulse test PW ≤ 630 msec, duty cycle ≤ 10%.

n-channel JFET
designed for . . .

Siliconix

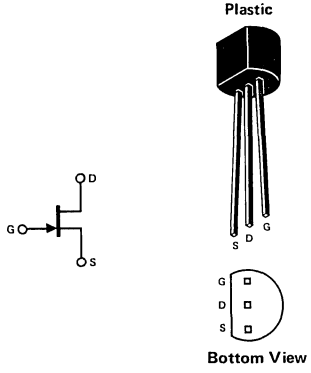
Performance Curves NRL
See Section 4

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current		–0.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			V	I_G = –10 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0	V	V_{DS} = 10 V, I_D = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current	1		25	mA	V_{DS} = 10 V, V_{GS} = 0, (Note 1)	
5	STATIC	g_{fs}	Common-Source Forward Transconductance	1000		7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6	DYN	$Re_{(y_{fs})}$	Common-Source Forward Transconductance	800			μmho	V_{DS} = 10 V, V_{GS} = 0	f = 100 MHz
7	DYN	C_{iss}	Common-Source Input Capacitance		3.5		pF	V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz
8	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		0.85		pF	V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz

NOTE:
1. Pulse test PW = 300 μs, duty cycle ≤ 3%.

NRL

3

p-channel JFETs designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves
PSA/PSB/PSC
See Section 4

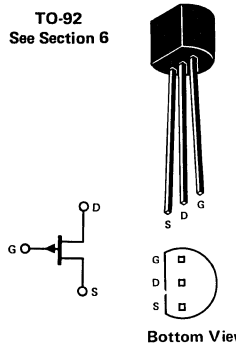
BENEFITS

- Low Insertion Loss
  $r_{DS(on)}$ = 75 Ω Maximum (P1086)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		P1086 Min	P1086 Max	P1087 Min	P1087 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		2		2	nA	V_{GS} = 15 V, V_{DS} = 0	
3	STATIC	$I_{D(off)}$	Drain Cutoff Current		–10		–10	nA	V_{DS} = –15 V, V_{GS} = 12 V (P1086) V_{GS} = 7 V (P1087)	
4					–0.5		–0.5	μA		T_A = 85°C
5		I_{DGO}	Drain Reverse Current		2		2	nA	V_{DG} = –15 V, I_S = 0	
					0.1		0.1	μA		T_A = 85°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	V_{DS} = –15 V, I_D = –1 μA	
7		I_{DSS}	Saturation Drain Current	–10		–5		mA	V_{DS} = –20 V, V_{GS} = 0	
8		$V_{DS(on)}$	Drain-Source ON Voltage		–0.5		–0.5	V	V_{GS} = 0, I_D = –6 mA (P1086), I_D = –3 mA (P1087)	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	I_D = –1 mA, V_{GS} = 0	
10		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	V_{DS} = –15 V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		V_{DS} = 0, V_{GS} = 12 V (P1086) V_{GS} = 7 V (P1087)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = –6 V, $V_{GS(on)}$ = 0	
14		t_r	Rise Time		20		75			
15		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
16		t_f	Fall Time		50		100			

	$V_{GS(off)}$	$I_{D(on)}$	R_L
P1086	12 V	–6 mA	910 Ω
P1087	7 V	–3 mA	1.8K Ω

PSA/PSB/PSC

NOTE:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

low-leakage pico-amp diodes *designed for . . .*

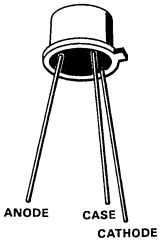
- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

Siliconix

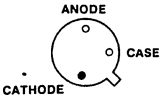
BENEFITS

- Very High Off-Isolation 1 pA Max (PAD1)

TO-18 (MODIFIED)
See Section 6



(Case lead for PAD1, 2, & 5 only)



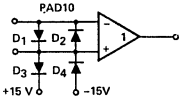
Bottom View

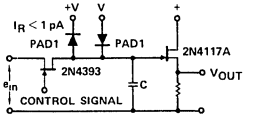
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . . 50 mA
Total Device Dissipation . . . . . 300 mW
Storage Temperature Range . . . . . -55°C to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_R Reverse Current			-1	pA	V_R = -20 V	PAD1
2					-2			2
3					-5			5
4					-10			PAD10
5					-20			20
6					-50			50
7					-100			PAD100
8		BV_R Breakdown Voltage (Reverse)	-45		-120	V	I_R = -1 μA	PAD1, 2, 5
9			-35					PAD10, 20, 50, 100
10		V_F Forward Voltage Drop		0.8	1.5		I_F = 5 mA	PAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R Capacitance			0.8	pF	V_R = -5 V, f = 1 MHz	PAD1, 2, 5
12					2			PAD10, 20, 50, 100





APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D_1 and D_2 Common mode input voltage limited by PADS D_3 and D_4 to ±15 V.

Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

PN4091 PN4092 PN4093
PN4091 = SST 4091, 4092, 4093
SURFACE MOUNT EQUIVALENT

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NCB See Section 4

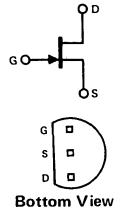
BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  $r_{DS(on)} < 30\ \Omega$ (PN4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (PN4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6



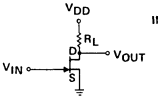
Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4091		PN4092		PN4093		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V	
5									400	nA			150°C
6							200			pA		$V_{GS} = -8$ V	
7							400			nA			150°C
8					200					pA		$V_{GS} = -12$ V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA	
13							0.2					$I_D = 4$ mA	
14					0.2							$I_D = 6.6$ mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V		
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$		
20		t_r	Rise Time		10		20		40			$I_{D(on)}$	$V_{GS(off)}$ R_L
21		t_{off}	Turn-OFF Time		40		60		80		PN4091	6.6 mA	-12 V 425 Ω
											PN4092	4	-8 700
											PN4093	2.5	-6 1120

NOTE:
1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE ≤ 10%
PULSE GENERATOR IMPEDANCE 50Ω

NCB
SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NT
See Section 4

■ Ultra-High Input Impedance Amplifiers

Electrometers
pH Meters
Smoke Detectors

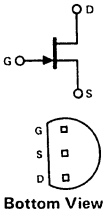
BENEFITS

- Low Power
  $I_{DSS} < 90\ \mu A$ (PN4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (PN4117A Series)

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6



Bottom View

Plastic

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4117 PN4117A Min	Typ	Max	PN4118 PN4118A Min	Typ	Max	PN4119 PN4119A Min	Typ	Max	PN4120 PN4120A Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current PN4117 Series Only			-10			-10			-10			-20	pA	V_{GS} = -20 V, V_{DS} = 0	
2						-25			-25			-25			-50	nA		100°C
3		I_{GSS}	Gate Reverse Current PN4117A Series Only		-1			-1			-1			-5		pA	V_{GS} = -20 V, V_{DS} = 0	
4						-2 5			-2 5			-2 5			-10	nA		100°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40					-40	V	I_G = -1 μA, V_{DS} = 0	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0 6		-1 8	-1		-3	-2		-6	-0 6		3		V_{DS} = 10 V, I_D = 1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0 03		0 09	0.08		0.24	0 20		0 60	0 03		0 3	mA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70		210	80		250	100		330	70		300	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3			5			10			20			
10		C_{iss}	Common-Source Input Capacitance			3			3			3			3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1 5			1 5			1 5			1 5			

NT

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied.

3

n-channel JFETs *designed for . . .*

Siliconix

■ General Purpose Amplifiers

Performance Curves NPA, NH
See Section 4

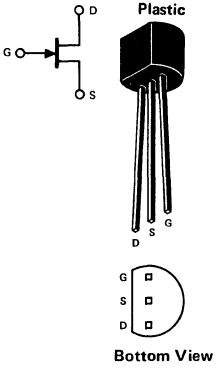
BENEFITS

- Low Cost
- High Input Impedance
  I_G = 35 pA Typically
- Low Noise
  $\overline{e_n}$ = 5 nV/$\sqrt{Hz}$ Typically @ 1 kHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . –30V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient.
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6



Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4302 Min	PN4302 Max	PN4303 Min	PN4303 Max	PN4304 Min	PN4304 Max	Unit	Test Conditons	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		1		–1		–1	nA	V_{GS} = –10 V, V_{DS} = 0	
2					0 1		–0.1		–0.1	µA		T_A = 85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		–30		–30		V	I_G = –1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–4 0		–6 0		–10		V_{DS} = 20 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current (Note 3)	0.5	5.0	4.0	10	0.5	15	mA	V_{DS} = 20 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000		2000		1000		µmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		50		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		C_{DG}	Drain-Gate Capacitance		2		2		2		V_{DG} = 10 V, I_S = 0	f = 140 kHz
11		NF	Noise Figure		2.0		2 0		3.0	dB	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz, R_{gen} = 1 0M Ω
12		$\|y_{fs}\|$	Common-Source Short Circuit Forward Transadmittance (Note 3)	700		1400		700		µmho	V_{DS} = 20 V, V_{GS} = 0	f = 10 MHz

NPA, NH

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms

n-channel JFETs *designed for . . .*

Siliconix

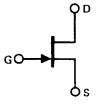
Performance Curves NCB See Section 4

- **Analog Switches**
- **Commutators**
- **Choppers**

BENEFITS

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Low Cost

TO-92
See Section 6



Plastic

Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Forward Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	PN4391 Min	PN4391 Max	PN4392 Min	PN4392 Max	PN4393 Min	PN4393 Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		–1 0		–1 0		–1 0	nA	V_{GS} = –20 V, V_{DS} = 0	
2					–200		–200		–200			100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current						1 0	nA	V_{DS} = 20 V	V_{GS} = –5 V
5									200			100°C
6							1 0					V_{GS} = –7 V
7							200					100°C
8					1 0							V_{GS} = –12 V
9					200							100°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–4	–10	–2	–5	–0 5	–3	V	V_{DS} = 20 V, I_D = 1 nA	
11		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	100	5	60	mA	V_{DS} = 20 V, V_{GS} = 0	
12		$V_{DS(on)}$	Drain-Source ON Voltage						0 4	V	V_{GS} = 0	I_D = 3 mA
13							0 4					I_D = 6 mA
14					0 4							I_D = 12 mA
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA	
16		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, V_{DS} = 0	f = 1 kHz
17	DYN	C_{iss}	Common-Source Input Capacitance		16		16		16	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance						5		V_{DS} = 0	V_{GS} = –5 V
19							5					V_{GS} = –7V
20					5							V_{GS} = –12 V
21	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0	
22		t_r	Rise Time		5		5		5		$I_{D(on)}$ / $V_{GS(off)}$ / R_L: PN4391 12 mA / –12 V / 800 Ω; PN4392 6 / –7 / 1 6K; PN4393 3 / –5 / 3 2K	
23		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50			
24		t_f	Fall Time		15		20		30			

NCB

NOTE
1 Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%

PN4416 (SURFACE MOUNT EQUIV. = SST 4416)

n-channel JFETs *designed for . . .*

- **VHF Amplifiers**
- **Mixers**

Siliconix

Performance Curves NH
See Section 4

BENEFITS

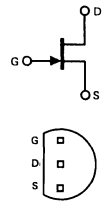
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

ABSOLUTE MAXIMUM RATINGS (25°C)

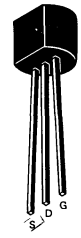
Gate-Drain or Gate-Source Voltage . . . . . –30V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

Plastic

TO-92
See Section 6



Bottom View



		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		10	nA	V_{GS} = –15 V, V_{DS} = 0 V	
2								
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	I_G = –1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–6		V_{DS} = 15 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4			
10		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz		400 MHz		Unit	Test Conditions
				Min	Max	Min	Max		
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000		
13		g_{oss}	Common-Source Output Conductance		75		100		
14		b_{oss}	Common-Source Output Susceptance		1000		4000		
15		g_{fs}	Common-Source Forward Transconductance			4000			
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4		V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

NH

NOTES:
1. Pulse test duration = 300 μs

n-channel JFET
designed for . . .

Siliconix

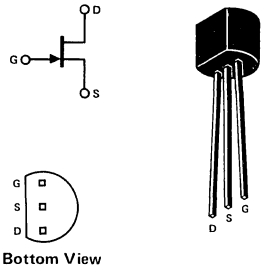
■ Low and Medium Frequency Amplifiers

BENEFITS
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current (FWD) . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 6
Plastic



Bottom View

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS} Gate Reverse Current		–10	nA	V_{GS} = –15 V, V_{DS} = 0		
2				–0.6	μA			T_A = 85°C
3		BV_{GSS} Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0		
4		$V_{GS(off)}$ Gate-Source Cutoff Voltage	–0.4	–8.0		V_{DS} = 15 V, I_D = 1 μA		
5		V_{GS} Gate-Source Voltage		–7.5		V_{DS} = 15 V, I_D = 100 μA		
6		I_{DSS} Saturation Drain Current	1.0	40	mA	V_{DS} = 15 V, V_{GS} = 0		
7		$r_{ds(on)}$ Drain-Source ON Resistance		500	Ω	V_{GS} = 0, I_D = 0		
8	DYNAMIC	g_{fs} Common-Source Forward Transconductance	2000	9000	μmho	V_{DS} = 15 V, V_{GS} = 0		f = 1 kHz
9		g_{os} Common-Source Output Conductance		200				
10		g_{fs} Common-Source Forward Transconductance	1800					f = 1 MHz
11		C_{iss} Common-Source Input Capacitance		20	pF			
12		C_{rss} Common-Source Reverse Transfer Capacitance		5.0				
13		NF Common-Source Spot Noise Figure		3.0	dB	V_{DS} = 15 V, I_D = 1 mA	R_G = 150k Ω	f = 1 kHz NBW = 150 Hz
14		$\bar{e}_N$ Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$			

*JEDEC registered data

3

n-channel DMOS FETs

Designed for Military and Industrial Applications . . .

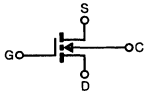
- **High-Speed Switching**
- **Analog Switch**
- **Multiplexer**
- **Digital Switch**
- **A to D Converters**
- **D to A Converters**
- **Choppers**
- **Sample and Hold**

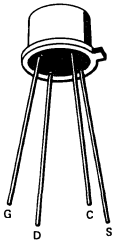
Performance Curves DMCB
See Section 4

BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1ns)
- Gate can accept ±40V

TO-72
See Section 6





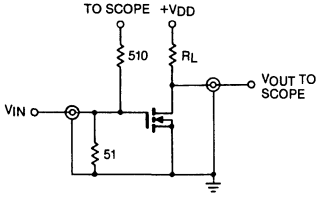
ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current.....50mA
Total Device Dissipation at 25°C
Case Temperature.....1.2W
Storage Temperature Range..... −65° to +200°C
Lead Temperature (1/16″ from case for 10 sec.)..... 300°C
Operating Temperature Range ..... −55° to +150°C

PARAMETER		SD210	SD212	SD214	UNIT
V_{DS}	Drain-to-source	+30	+10	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+15	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+25	Vdc
V_{GS}	Gate-to-source	±40	±40	±40	Vdc
V_{GB}	Gate-to-substrate	±40	±40	±40	Vdc
V_{GD}	Gate-to-drain	±40	±40	±40	Vdc

TEST CONDITIONS

Switching

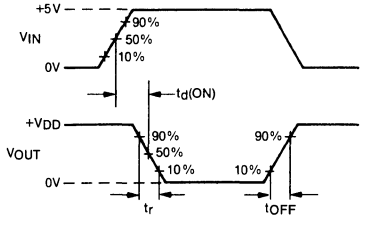


Input pulse t_d, t_r < 1ns
Pulse width = 100ns
Rep rate = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

		$t_{d(ON)}$ (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified.)

		PARAMETER		TEST CONDITIONS	SD210 Min	SD210 Typ	SD210 Max	SD212 Min	SD212 Typ	SD212 Max	SD214 Min	SD214 Typ	SD214 Max	UNIT
1	STATIC	**Breakdown voltage** BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$ $V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	30 10	35 25		 10	 25		 20	 25		V
2	STATIC	BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			20			V
3	STATIC	BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			25			V
4	STATIC	BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			25			V
5	STATIC	**Leakage current** I_{DS} (OFF)	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$ $V_{DS} = +20V$		1	10		1	10		 1	 10	nA
6	STATIC	I_{SD} (OFF)	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$ $V_{SD} = +20V$		1	10		1	10		 1	 10	nA
7	STATIC	I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = \pm 40V$			0.1			0.1			0.1	nA
8	STATIC	V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
9	STATIC	r_{DS} (ON)	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$ $V_{GS} = +25V$		 50 30 23 19 17	 70 45		 50 30 23 19 17	 70 45		 50 30 23 19 17	 70 45	Ω

AC ELECTRICAL CHARACTERISTICS

		PARAMETER		TEST CONDITIONS	SD210 Min	SD210 Typ	SD210 Max	SD212 Min	SD212 Typ	SD212 Max	SD214 Min	SD214 Typ	SD214 Max	UNIT
10	DYNAMIC	gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
11	DYNAMIC	**Small Signal Capacitances** (See capacitance model) $C_{(GS+GD+GB)}$	Gate node	$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$		2.4	3.5		2.4	3.5		2.4	3.5	pF
12	DYNAMIC	$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
13	DYNAMIC	$C_{(GS+SB)}$	Source node			3.5	5.5		3.5	5.5		3.5	5.5	pF
14	DYNAMIC	C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

DMCB

n-channel DMOS FETs

Designed for Military and Industrial Applications . . .

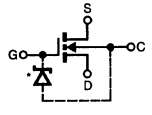
- **High-Speed Switching**
- **Analog Switch**
- **Multiplexer**
- **Digital Switch**
- **A to D Converters**
- **D to A Converters**
- **Choppers**
- **Sample and Hold**

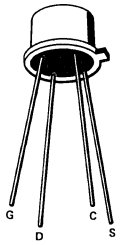
Performance Curves DMCB
See Section 4

BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1ns)
- Diode protected gate

TO-72
See Section 6





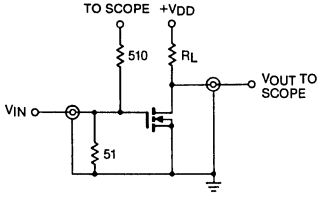
ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current.....50mA
Total Device Dissipation at 25°C
Case Temperature.....1.2W
Storage Temperature Range.....–65° to +200°C
Lead Temperature (1/16″ from case for 10 sec.).....300°C
Operating Temperature Range.....–55° to +150°C

PARAMETER		SD211	SD213	SD215	UNIT
V_{DS}	Drain-to-source	+30	+10	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+15	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+25	Vdc
V_{GS}	Gate-to-source	−15 +25	−15 +25	−25 +30	Vdc
V_{GB}	Gate-to-substrate	−0.3 +25	−0.3 +25	−0.3 +30	Vdc
V_{GD}	Gate-to-drain	−30 +25	−15 +25	−25 +30	Vdc

TEST CONDITIONS

Switching

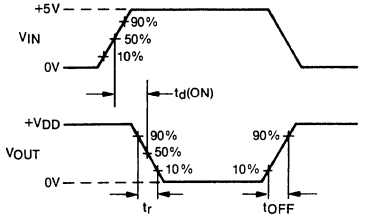


Input pulse. t_d, t_r < 1ns
Pulse width = 100ns
Rep rate = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

		$t_{d(ON)}$ (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified.)

		PARAMETER		TEST CONDITIONS	SD211 Min	SD211 Typ	SD211 Max	SD213 Min	SD213 Typ	SD213 Max	SD215 Min	SD215 Typ	SD215 Max	UNIT
1	STATIC	**Breakdown voltage** BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$ $V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	30 10	35 25		 10	 25		 20	 25		V
2		BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			20			
3		BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			25			
4		BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			25			
5		**Leakage current** I_{DS} (OFF)	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$ $V_{DS} = +20V$		1	10		1	10		1	10	nA
6		I_{SD} (OFF)	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$ $V_{SD} = +20V$		1	10		1	10		1	10	
7		I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = +25V$ $V_{GB} = +30V$			10			10			10	μA
8		V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
9		r_{DS} (ON)	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$ $V_{GS} = +25V$		50 30 23 19	70 45		50 30 23 19	70 45		50 30 23 19 17	70 45	Ω

AC ELECTRICAL CHARACTERISTICS

		PARAMETER		TEST CONDITIONS	SD211 Min	SD211 Typ	SD211 Max	SD213 Min	SD213 Typ	SD213 Max	SD215 Min	SD215 Typ	SD215 Max	UNIT
10	DYNAMIC	gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
11		**Small Signal Capacitances** (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										pF
		$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	
12		$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	
13		$C_{(GS+SB)}$	Source node			3.5	5.5		3.5	5.5		3.5	5.5	
14		C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	

DMCB

n-channel D-MOS FETs

Siliconix

designed for Military and Industrial Applications . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**
- **High-Speed Switching**
- **Normally "On" Switch**
- **Analog/Digital Switch**
- **Multiplexer**
- **Low-Voltage Switch**

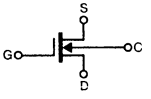
FEATURES
- **High Figure-of-Merit gfs/C**
- **High Speed Switch (< 1 /ns)**
- **High Gain**
- **Wide Dynamic Range-Input**
- **Low Voltage Requirements = Battery Operation**

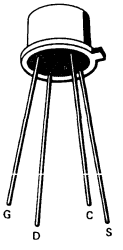
BENEFITS
- **High Frequency Gain**
- **High Speed Switching**
- **Low Distortion**

ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current ..... 50 mA
Total Device Dissipation at 25°C
Case Temperature 1.2W
Storage Temperature Range ..... −65° to +200°C
Lead Temperature
(1/16 from case for 10 sec.) ..... 300°C
Operating Temperature Range ..... −55° to +150°C

TO-72
See Section 6





DC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

	Parameter		Test Conditions		Min	Typ	Max	Unit
1	BV_{DS}	Drain-Source Breakdown Voltage	I_D = 1 μA V_{GS} = V_{BS} = 0		25			V
2	I_{GSS}	Gate Reverse Current	V_{GS} = ±25V V_{BS} = 0			±0.01	±1.0	nA
3	$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS} = 10V, V_{BS} = 0 I_D = 1 μA			−1.0	−2.0	V
4	V_{GS}	Gate-Source Voltage	V_{DG} = 10V	I_D = 5 mA	0	+0.5	+1.0	V
5			V_{BS} = 0	I_D = 20 mA		+1.7	+2.5	V
6	I_{DSS}	Saturation Drain Current	V_{DS} = 10V V_{GS} = V_{BS} = 0		1.0		5.0	mA
7	r_{DS}	Drain-Source ON Resistance	V_{DS} = 100 mV V_{BS} = 0	V_{GS} = 0		150	200	Ω
8				V_{GS} = +5V		35	50	Ω

AC ELECTRICAL CHARACTERISTICS

	Parameter		Test Conditions		Min	Typ	Max	Unit
9	g_{fs}	Forward Transconductance	V_{DG} = 10V, V_{BS} = 0, f = 1 KHz	I_D = 20 mA	10	14	20	mmho
10				I_D = 5 mA	8	10		mmho
11	g_{os}	Common-Source Output Conductance	V_{DG} = 10V, V_{BS} = 0, I_D = 20 mA, f = 1 MHz			80	200	μmho
12	C_{iss}	Common-Source Input Capacitance	V_{DG} = 10V, V_{BS} = 0, I_D = 5 mA, f = 1 MHz			4.0	.0	pF
13	C_{rss}	Reverse Transfer Capacitance				1.5	2.5	pF

SWITCHING CHARACTERISTIC

		$t_{d(ON)}$ – ns		t_r – ns		t_{OFF} – ns	
V_{DD}	R_L	V_{IN} – 2 to + 0V	V_{IN} – 2 to +4V	–2 to +0V	–2 to +4V	–2 to +0V	–2 to +4V
		Typ	Typ	Typ	Typ	Typ	Typ
5	670	1.2	0.8	0.7	0.4	4.0	6.0
10	670	1.3	0.8	2.3	0.4	4.4	5.3
15	670	1.5	0.8	4.3	0.5	4.4	4.8

n-channel dual enhancement mode lateral D-MOS FETs

Siliconix

designed for . . .

- **Wideband Differential Amplifiers**
- **Cascode High Slew Rate Amplifiers**
- **Single Ended High-Speed Amps**
- **High-Speed Analog Comparators**
- **Sample & Hold Ckts**
- **High-Speed Matched Analog Switches**

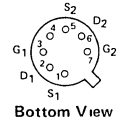
FEATURES
- High Figure-of-Merit gfs/C
- Ultra Low Feedback Capacitance 0.3 pF
- Low Output Capacitance
- Low Input (Gate) Leakage
- Non-Critical Operating Current/Voltage
- Matched Characteristics

BENEFITS
- High Frequency Performance
- High Slew Rate
- High Speed Switching
- Tight Temperature Tracking

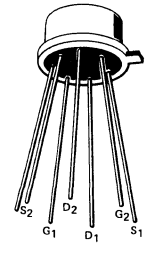
ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Drain Voltage	±25V
Drain-Source Voltage	+25V
Drain Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-78
See Section 6



Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Typ	Max	Unit	Test Conditions
I_{GSS}	Gate Reverse Current		0.05	1	nA	V_{GS} = +15V, V_{DS} = 0
BV_{DS}	Drain-Source Breakdown Voltage	25			V	I_D = 1 μA, V_{GS} = 0
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.1	0.8	2.0	V	V_{DS} = V_{GS} = 10V, I_D = 1 μA
V_{GS}	Gate-Source Voltage		1.9	3.0	V	V_{DG} = 10V, I_D = 5 mA
I_G	Gate Operating Current		0.05	1	nA	V_{DG} = 10V, I_D = 5 mA
gfs	Common-Source Forward Transconductance	7,000	9,000	15,000	μmhos	V_{DS} = 10V, V_{GS} = 0, f = 1 KHz
gos	Common-Source Output Conductance		20	100	μmhos	
$R_{DS(ON)}$	Drain-Source Resistance			60	Ω	I_D = 1 mA, V_{GS} = 10V
C_{iss}	Common-Source Input Capacitance		3.2	5	pF	V_{DS} = 10V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		0 5	1.2	pF	

Characteristic			SD2110		SD2120		Unit	Test Condition	
			Min	Max	Min	Max			
MATCHING	$\lvert V_{GS1} = V_{GS2} \rvert$	Differential Gate-Source Voltage		10		20	mV	V_{DG} = 10V, I_D = 5 mA	T_A = 25°C T_B = 125°C
	$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Drift[3]		25 25		50 50	μV/°C μV/°C		T_A = −55°C T_B = 25°C
	$\frac{gfs_1}{gfs_2}$	Transconductance Ratio[2]	0.95	1	0.95	1			f = 1 KHz

NOTES:
1. Pulsewidth ≤ 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

DMOS FET Quad Analog Switch Arrays

designed for Military and Industrial Applications . . .

Siliconix

FEATURES	BENEFITS	APPLICATIONS
• Low "ON" Resistance	• "OFF Isolation of −107 dB	• Audio Switching
• Low Input Capacitance	• Low Insertion Loss	• Video Switching
• Low Output Capacitance	• Glitch Free Signals	• Sample/Hold
• Low Feedback Capacitance	• Fast Switching	• Choppers
• High Channel-to-Channel Isolation		• Crosspoint Switches

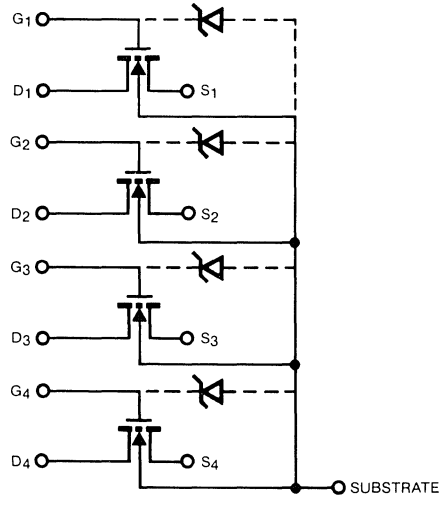
DESCRIPTION

The Siliconix SD5000 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video, and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5000 is rated for analog signals of ±10 V, while the SD5001 and SD5002 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and ON resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

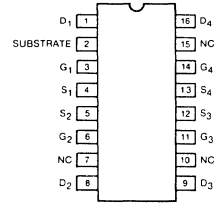
The SD5000 family is available in 16-pin plastic and side braze dual-in-line packages, and is rated for operation over the -55° to 125°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

Order Part Numbers:
SD5000I, SD5001I, SD5002I
Plastic
SD5000N, SD5001N, SD5002N
Ceramic
See Section 6

ABSOLUTE MAXIMUM RATINGS

	SD5000	SD5001	SD5002
V_{DS}	20 V	10 V	15 V
V_{SD}[1]	20 V	10 V	15 V
V_{DB}	25 V	15 V	22.5 V
V_{SB}	25 V	15 V	22.5 V
V_{GS}	30/−25 V	25/−15 V	30/−22.5 V
V_{GB}	30/−0.3 V	25/−0.3 V	30/−0.3 V
V_{GD}	30/−25 V	25/−15 V	30/−22.5 V

I_D ..... 50 mA
Operating Temperature ..... −55° to +125°C
Storage Temperature ..... −55 to 150°C
Power Dissipation (Package)[2] ..... 640 mW
(Each Device) ..... 300 mW

ELECTRICAL CHARACTERISTICS[3]

T_A = 25°C

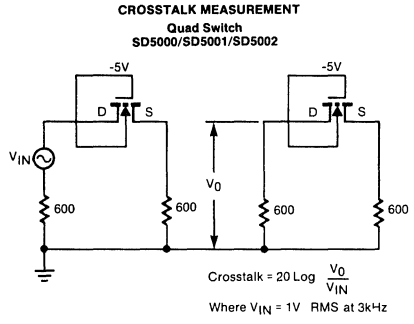
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:		LIMITS SD5000 MIN[4]	SD5000 TYP[5]	SD5000 MAX	SD5001 MIN[4]	SD5001 TYP[5]	SD5001 MAX	SD5002 MIN[4]	SD5002 TYP[5]	SD5002 MAX	UNIT
Analog Signal Range	V_{ANALOG}			−10		10	−5		5	−7.5		7.5	V
Drain-Source Breakdown Voltage	BV_{DS}	$V_{GS} = V_{BS}$ = −5 V, I_D = 10 nA		20	25		10	25		15	25		V
Source-Drain Breakdown Voltage	BV_{SD}	$V_{GD} = V_{BD}$ = −5 V, I_S = 10 nA		20			10			15			V
Drain-Substrate Breakdown Voltage	BV_{DB}	V_{GB} = 0 V, I_D = 10 nA, Source Open		25			15			22.5			V
Source-Substrate Breakdown Voltage	BV_{SB}	V_{GB} = 0 V, I_S = 10 µA, Drain Open		25			15			22.5			V
Drain-Source Leakage Current	$I_{DS(off)}$	$V_{GS} = V_{BS}$ = −5 V	V_{DS} = 20 V		1	10							nA
			V_{DS} = 10 V					1	10				nA
			V_{DS} = 15 V								1	10	nA
Source-Drain Leakage Current	$I_{SD(off)}$	$V_{GD} = V_{BD}$ = −5 V	V_{SD} = 20 V		1	10							nA
			V_{SD} = 10 V					1	10				nA
			V_{SD} = 15 V								1	10	nA
Gate Leakage Current	I_{GBS}	$V_{DB} = V_{SB}$ = 0 V	V_{GB} = 30 V			1							µA
			V_{GB} = 25 V						1				µA
			V_{GB} = 30 V									1	µA
Threshold Voltage	V_T	$V_{DS} = V_{GS} = V_T$, I_D = 1 µA, V_{SB} = 0 V		0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
Drain-Source ON Resistance	$r_{DS(on)}$	I_D = 1 mA, V_{SB} = 0 V	V_{GS} = 5 V		50	70		50	70		50	70	Ω
			V_{GS} = 10 V		30			30			30		Ω
			V_{GS} = 15 V		23			23			23		Ω
			V_{GS} = 20 V		19			19			19		Ω
Resistance Match[6]	$r_{DS(on)}$	I_D = 1 mA, V_{SB} = 0 V, V_{GS} = 5 V			1	5		1	5		1	5	Ω
Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 20 mA, V_{SB} = 0 V, f = 1 kHz		10	15		10	15		10	15		mS[7]
Gate Node Capacitance	C_G	V_{DS} = 10 V, $V_{GS} = V_{BS}$ = −15 V, f = 1 MHz See Capacitance Model Figure 1			2.4	3.5		2.4	3.5		2.4	3.5	pF
Drain Node Capacitance	C_D				1.3	1.6		1.3	1.6		1.3	1.6	pF
Source Node Capacitance	C_S				3.5	5		3.5	5		3.5	5	pF
Reverse Transfer Capacitance	C_{DG}				0.3	5		0.3	5		0.3	5	pF
Crosstalk		See Test Circuits 1 and 2 f = 3 kHz			−107			−107			−107		dB

DMCAI

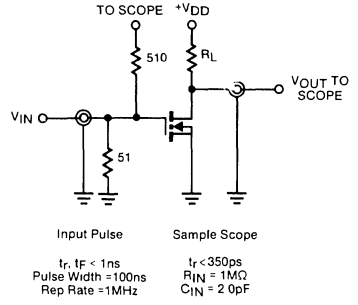
NOTES:

1 Refer to test conditions specified in Electrical Characteristics Tables
2 Derate 5 mW/°C above 25°C
3 Refer to PROCESS OPTION FLOWCHART for additional information
4 The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet
5 Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
6 This untested parameter is guaranteed by design
7 1 mS = 1 m-mho (℧)

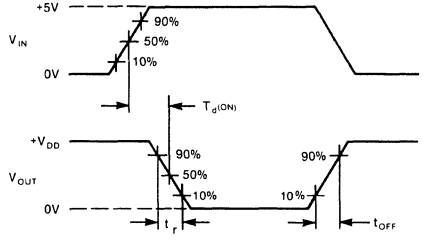
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS

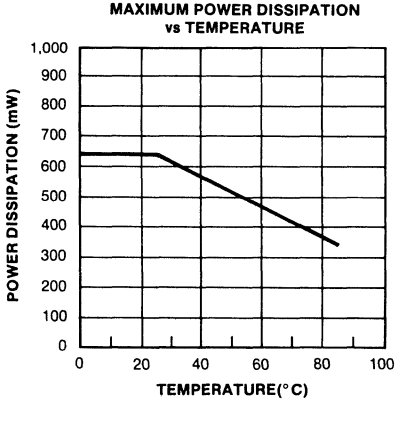


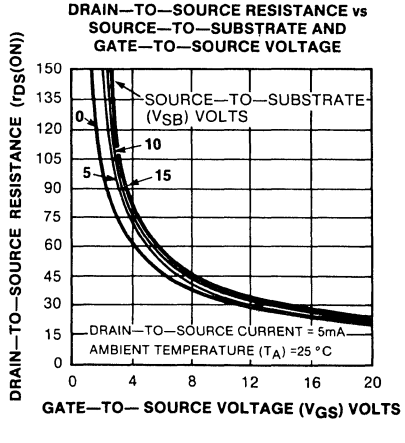
SWITCHING CHARACTERISTICS

		$t_{d(ON)}$(ns)		t_r(ns)		* t_{OFF}(ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

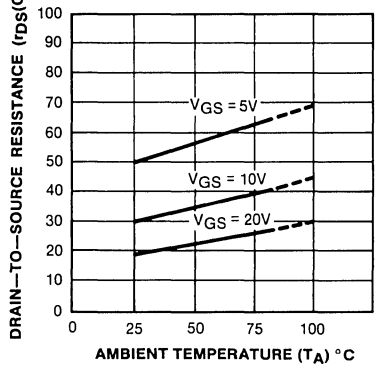
TYPICAL CHARACTERISTICS



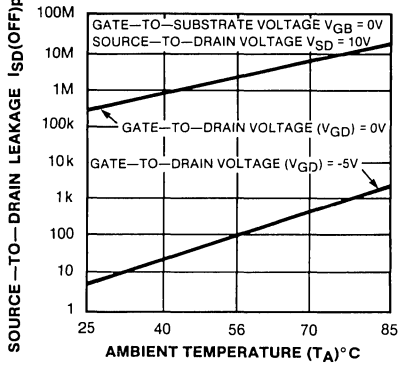


TYPICAL CHARACTERISTICS (Cont.)

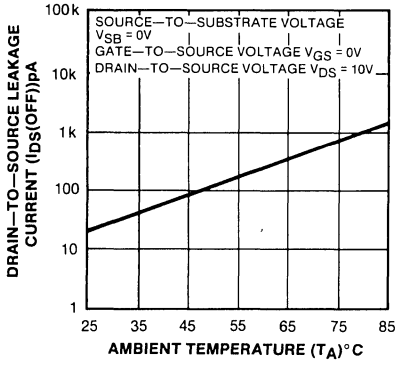
DRAIN—TO—SOURCE RESISTANCE vs TEMPERATURE



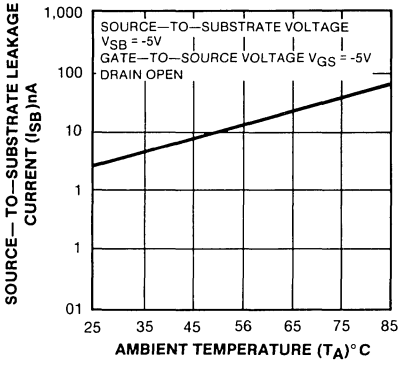
SOURCE—TO—DRAIN LEAKAGE CURRENT vs TEMPERATURE



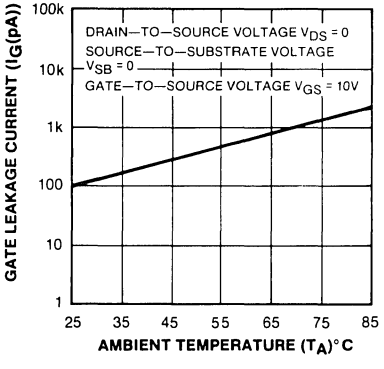
DRAIN—TO—SOURCE LEAKAGE CURRENT vs TEMPERATURE



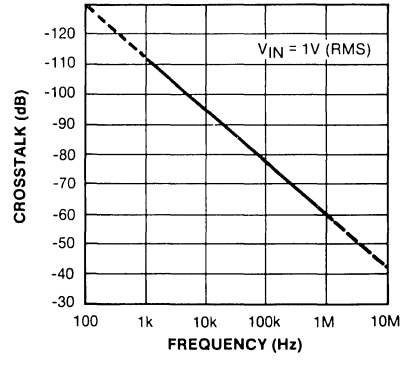
SOURCE—TO—SUBSTRATE LEAKAGE CURRENT vs TEMPERATURE



GATE LEAKAGE CURRENT vs TEMPERATURE



CROSSTALK vs FREQUENCY



THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of ±10 volts for the SD5000, ±5 volts for the SD5001 and ±7.5 volts for the SD5002. Each switch of the array is a DMOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T, the FET switch starts to turn ON with V_{GS} in excess of +10 volts, a low resistance path (typically 30 Ω) exists between input and ouput of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5000 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically 30 Ω and OFF resistance is typically 10^{10} Ω, which results in an OFF to ON resistance ratio in excess of 10^9. Isolation from output to input from 3 kHz analog signals is typically −107 dB.

Feedback and feedthrough transients are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss depends upon the source and load impedances involved. As an example, for 600 Ω source impedance the insertion loss for voice signals (1 V RMS at 3 kHz) is less than 0.3 dB. Thus the SD5000 series makes good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5000 switches turn ON at subnanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30 dB at 1 GHz).

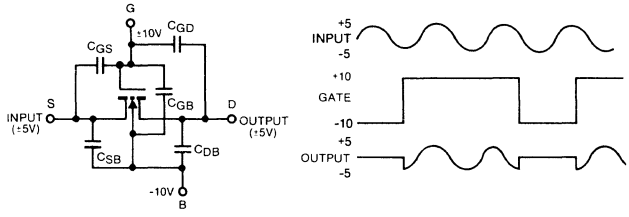
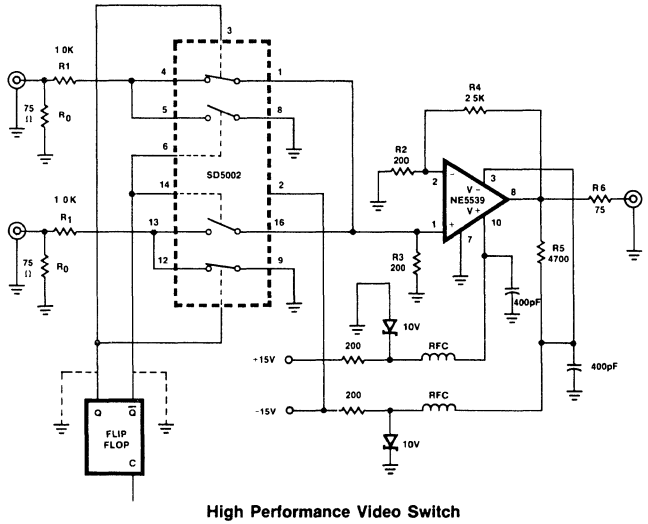


Figure 1

TYPICAL APPLICATION

Figure 2 shows an SD5002 configured for operation as a one of two channel video switch. The "L" switches of the two channels are terminated at the input by the two R_O resistors, allowing impedance matching to various transmission line impedances. The switches can be directly controlled by standard CMOS or TTL logic gates. For more detailed information on this application, see AN83-15.



High Performance Video Switch
Figure 2

D-MOS FET quad analog switch arrays and driver

Siliconix

designed for Military and Industrial Applications . . .

SD5200 APPLICATIONS

- **Switch Drivers**

DESCRIPTION

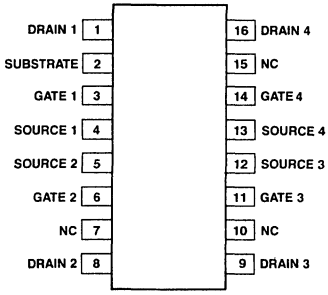
The SILICONIX D-MOS SD5200 monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enchancement mode technology.

This device is designed to handle a wide variety of driver applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

FEATURES

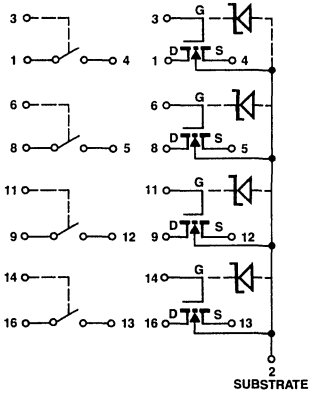
- **Low Input Capacitance—2.4 pF**
- **Low Feedback Capacitance—0.3 pF**
- **Low Output Capacitance—1.3 pF**
- **±10V Analog Signal Range**
- **Low Propagation Delay Time—600 ps**
- **Low on Resistance—30Ω**
- **Low Feedthrough and Feedback Transients**
- **Ion Implanted for Greater Reliability**
- **High Channel-to-Channel Isolation—107 dB**
- **Transient Protection for Gates**

I, N PACKAGE
(TOP VIEW)



ORDER PART NO.
SD5200N (PLASTIC)
SD52001 (SIDE BRAZE)

SD5200



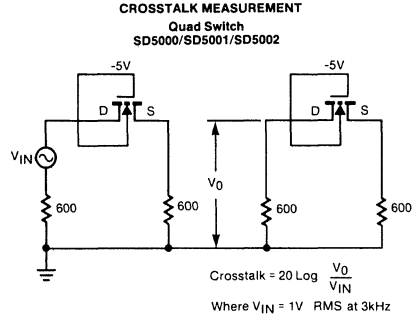
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Parameters		SD5200	Unit
V_{DS} Drain-to-Source		+30	V_{dc}
V_{SD} Source-to-Drain[1]		+0.5	
V_{DB} Drain-to-Substrate		+30	
V_{SB} Source-to-Substrate		+0.5	
V_{GS} Gate-to-Source		+20	
V_{GB} Gate-to-Substrate		+20	
		−0.3	
V_{GD} Gate-to-Drain		+20	
I_D Drain Current		50	mA
Ambient Temperature Range	Storage	−55 to +150	°C
	Operating	−55 to +125	
Power Dissipation	Total Package Dissipation[2]	640	mW
	Individual Transistor Dissipation	300	

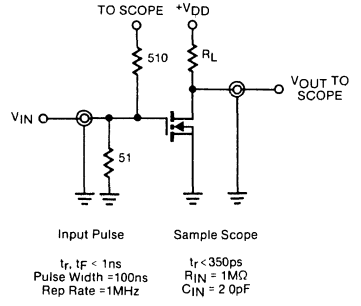
NOTES

1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5 mW per degree centigrade.

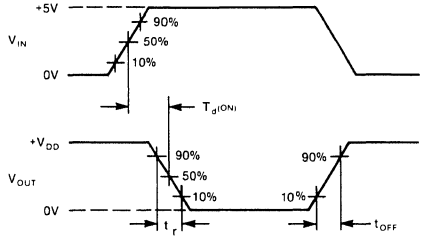
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS

		$t_{d(ON)}$(ns)		t_{r}(ns)		* t_{OFF}(ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0 7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

Parameter		Test Conditions	SD5200			Unit
			Min	Typ	Max	
BREAKDOWN VOLTAGE BV_{DS}	Drain-to-Source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\ \mu A$	30	35		V
		$V_{GS} = V_{BS} = -5V$, $I_S = 10$ nA				
BV_{SD}	Source-to-Drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10$ nA				V
BV_{DB}	Drain-to-Substrate	$V_{GB} = 0V$, Source Open $I_D = 10$ nA				V
BV_{SB}	Source-to-Substrate	$V_{GB} = 0V$, Drain Open $I_S = 10\ \mu A$				V
LEAKAGE CURRENT $I_{DS(OFF)}$	Drain-to-Source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +15V$ $V_{DS} = +10V$				nA
$I_{SD(OFF)}$	Source-to-Drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +15V$ $V_{SD} = +10V$				nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = 30V$				μA
V_T	Threshold Voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\ \mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-Source Resistance	$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +5V$		50	80	Ω
		$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +10V$		30		
		$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +15V$		23		
		$I_D = 1.0$ mA, $V_{SB} = 0$, $V_{GS} = +20V$		19		
$r_{DS(ON)}$	Resistance Match[1]	$I_D = 1.0$ mA, $V_{SB} = 0$ $V_{GS} = +5V$				Ω

NOTE:
1. This untested parameter is guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	SD5200			Unit
			Min	Typ	Max	
gfs	Forward Transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20$ mA, f = 1 kHz	10	15		mmho
$C_{(GS+GD+GB)}$	Gate Node Capacitances	$V_{DS} = 10V$, f = 1 MHz $V_{GS} = V_{BS} = -15V$ See Capacitance Model in Figure 1		2.4	3.5	pF
$C_{(GD+DB)}$	Drain Node Capacitances			1.3	1.5	
$C_{(GS+SB)}$	Source Node Capacitances					
C_{DG}	Reverse Transfer Capacitances			0.3	0.5	
C_T	Cross Talk	See Test Circuits No. 1 and 2, f = 3 kHz		−107		dB

DMOS FET Quad Analog Switch Arrays

Siliconix

FEATURES

- Low "ON" Resistance (<30 Ω)
- Low Input Capacitance (6 pF)
- Low Output Capacitance (2 pF)
- Low Feedback Capacitance (0.5 pF)
- High Channel-to-Channel Isolation (−107 dB)
- Small Outline Package

BENEFITS

- Low Crosstalk
- Low Insertion Loss
- Glitch Free Signals
- Fast Switching
- Reduced Board Space Requirements

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- Choppers
- Crosspoint Switches

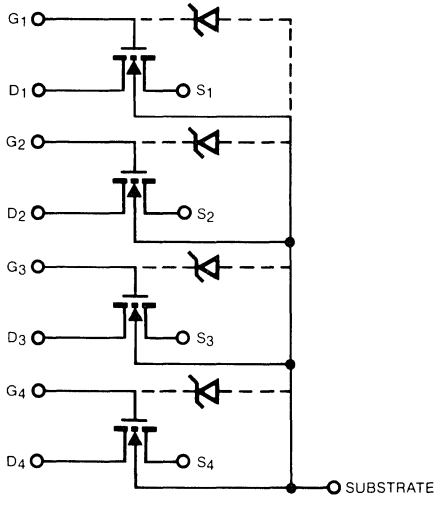
DESCRIPTION

The Siliconix SD5400 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video, and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5400 is rated for analog signals of ±10 V, while the SD5401 and SD5402 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and ON resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

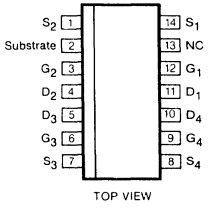
The SD5400 family is available in a 14-pin plastic Small Outline (SO) package, and is rated for operation over the 0 to 70°C commercial temperature range.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

SO Package



TOP VIEW

Order Numbers:
SD5400CY, SD5401CY,
or SD5402CY
See Section 6

ABSOLUTE MAXIMUM RATINGS

	SD5400	SD5401	SD5402
V_{DS}	20 V	10 V	15 V
V_{SD}[1]	20 V	10 V	15 V
V_{DB}	25 V	15 V	22.5 V
V_{SB}	25 V	15 V	22.5 V
V_{GS}	30/−25 V	25/−15 V	30/−22.5 V
V_{GB}	30/−0.3 V	25/−0.3 V	30/−0.3 V
V_{GD}	30/−25 V	25/−15 V	30/−22.5 V

I_D ..... 50 mA
Operating Temperature ..... 0 to 70°C
Storage Temperature ..... −55 to 125°C
Power Dissipation (Package)[2] ..... 850 mW
(Each Device) ..... 300 mW

ELECTRICAL CHARACTERISTICS[3]

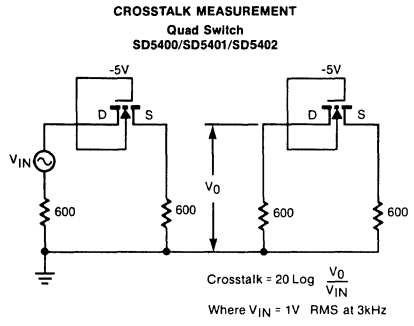
T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:		LIMITS SD5400 MIN[4]	SD5400 TYP[5]	SD5400 MAX	SD5401 MIN[4]	SD5401 TYP[5]	SD5401 MAX	SD5402 MIN[4]	SD5402 TYP[5]	SD5402 MAX	UNIT
Analog Signal Range	V_{ANALOG}			−10		10	−5		5	−7.5		7.5	V
Drain-Source Breakdown Voltage	BV_{DS}	V_{GS} = V_{BS} = −5 V, I_D = 10 nA		20	25		10	25		15	25		V
Source-Drain Breakdown Voltage	BV_{SD}	V_{GD} = V_{BD} = −5 V, I_S = 10 nA		20			10			15			V
Drain-Substrate Breakdown Voltage	BV_{DB}	V_{GB} = 0 V, I_D = 10 nA, Source Open		25			15			22.5			V
Source-Substrate Breakdown Voltage	BV_{SB}	V_{GB} = 0 V, I_S = 10 µA, Drain Open		25			15			22.5			V
Drain-Source Leakage Current	$I_{DS(off)}$	V_{GS} = V_{BS} = −5 V	V_{DS} = 20 V		1	10							nA
			V_{DS} = 10 V					1	10				nA
			V_{DS} = 15 V								1	10	nA
Source-Drain Leakage Current	$I_{SD(off)}$	V_{GD} = V_{BD} = −5 V	V_{SD} = 20 V		1	10							nA
			V_{SD} = 10 V					1	10				nA
			V_{SD} = 15 V								1	10	nA
Gate Leakage Current	I_{GBS}	V_{DB} = V_{SB} = 0 V	V_{GB} = 30 V			1							µA
			V_{GB} = 25 V						1				µA
			V_{GB} = 30 V									1	µA
Threshold Voltage	V_T	V_{DS} = V_{GS} = V_T, I_D = 1 µA, V_{SB} = 0 V		0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
Drain-Source ON Resistance	$r_{DS(on)}$	I_D = 1 mA, V_{SB} = 0 V	V_{GS} = 5 V		50	70		50	70		50	70	Ω
			V_{GS} = 10 V		30			30			30		Ω
			V_{GS} = 15 V		23			23			23		Ω
			V_{GS} = 20 V		19			19			19		Ω
Resistance Match[6]	$r_{DS(on)}$	I_D = 1 mA, V_{SB} = 0 V, V_{GS} = 5 V			1	5		1	5		1	5	Ω
Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 20 mA, V_{SB} = 0 V, f = 1 kHz		10	15		10	15		10	15		mS[7]
Gate Node Capacitance	C_G	V_{DS} = 10 V, V_{GS} = V_{BS} = −15 V, f = 1 MHz, See Capacitance Model Figure 1			24	35		24	35		24	35	pF
Drain Node Capacitance	C_D				13	2		13	2		13	2	pF
Source Node Capacitance	C_S				35	6		35	6		35	6	pF
Reverse Transfer Capacitance	C_{DG}				0.3	5		0.3	5		0.3	5	pF
Crosstalk		See Test Circuits 1 and 2, f = 3 kHz			107			107			-107		dB

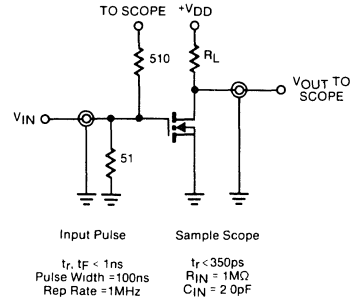
NOTES: DMCAI

1 Refer to test conditions specified in Electrical Characteristics Tables
2 Derate 6.9 mW/°C above 25°C
3 Refer to PROCESS OPTION FLOWCHART for additional information
4 The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet
5 Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
6 This untested parameter is guaranteed by design
7 1 mS = 1 m-mho (℧)

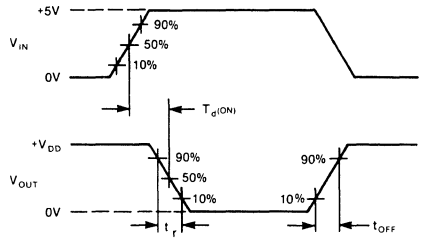
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS

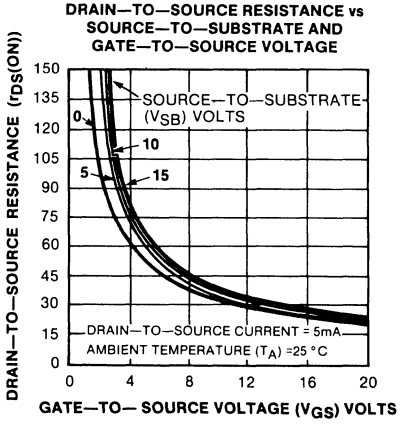


SWITCHING CHARACTERISTICS

		$t_{d(ON)}$(ns)		t_{r}(ns)		* t_{OFF}(ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0 7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

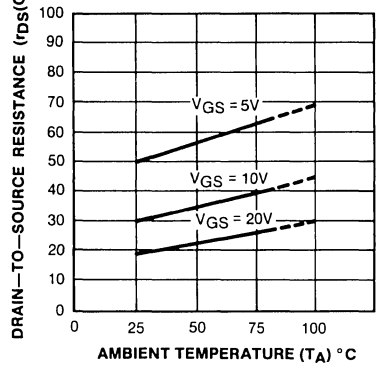
*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

TYPICAL CHARACTERISTICS

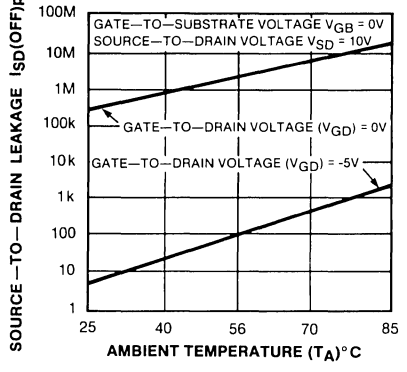


TYPICAL CHARACTERISTICS (Cont.)

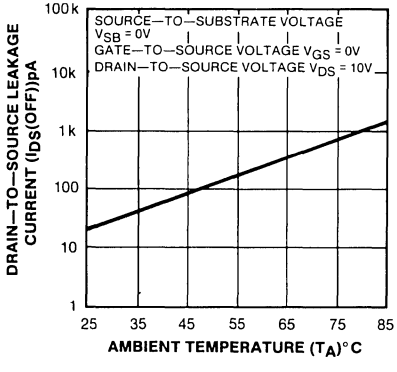
DRAIN—TO—SOURCE RESISTANCE vs TEMPERATURE



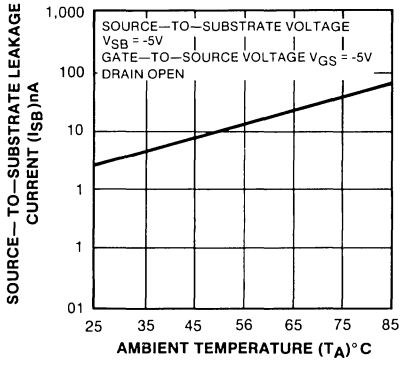
SOURCE—TO—DRAIN LEAKAGE CURRENT vs TEMPERATURE



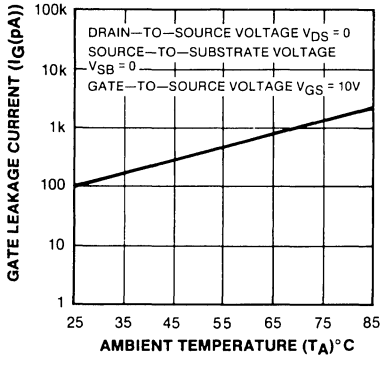
DRAIN—TO—SOURCE LEAKAGE CURRENT vs TEMPERATURE



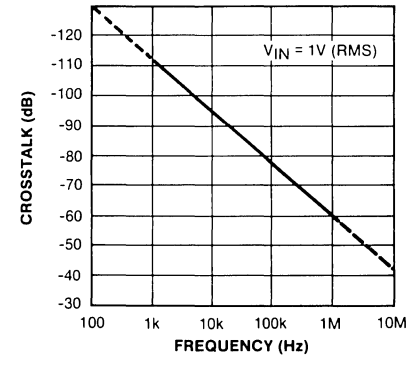
SOURCE—TO—SUBSTRATE LEAKAGE CURRENT vs TEMPERATURE



GATE LEAKAGE CURRENT vs TEMPERATURE



CROSSTALK vs FREQUENCY



3

THEORY OF OPERATION

The SD5400 series consists of four SPST switches with analog signal capability of ±10 volts for the SD5400, ±5 volts for the SD5401 and ±7.5 volts for the SD5402. Each switch of the array is a DMOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T, the FET switch starts to turn ON with V_{GS} in excess of +10 volts, a low resistance path (typically 30 Ω) exists between input and ouput of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5400 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically 30 Ω and OFF resistance is typically 10^{10} Ω, which results in an OFF to ON resistance ratio in excess of 10^9. Isolation from output to input from 3 kHz analog signals is typically −107 dB.

Feedback and feedthrough transients are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss depends upon the source and load impedances involved. As an example, for 600 Ω source impedance the insertion loss for voice signals (1 V RMS at 3 kHz) is less than 0.3 dB. Thus the SD5400 series makes good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5400 switches turn ON at subnanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30 dB at 1 GHz).

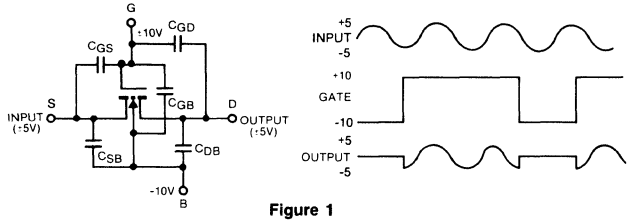
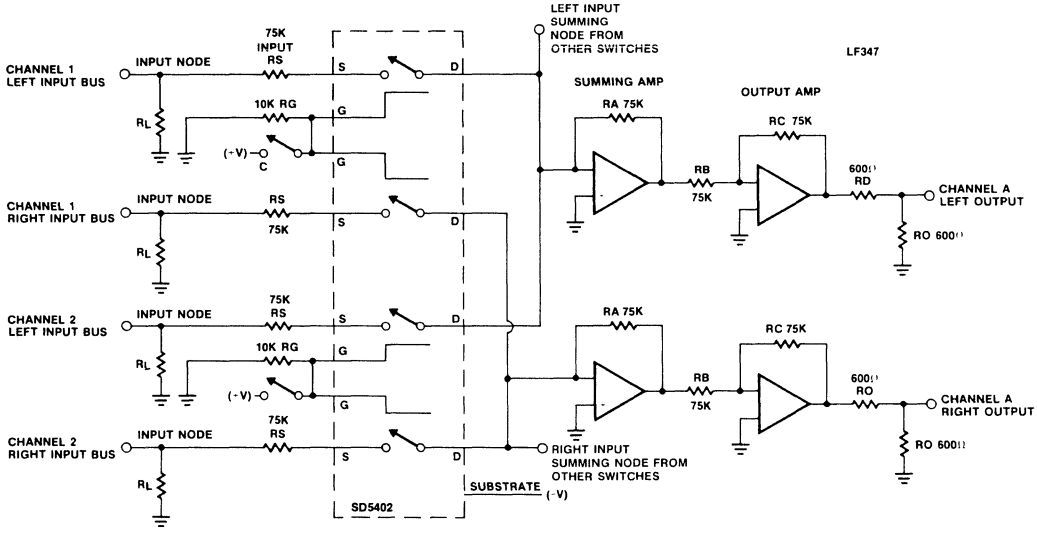


Figure 1

TYPICAL APPLICATION

Figure 2 shows the SD5402 used as an audio crosspoint switch. Each SD5402 provides switching for 2 stereo channels. Additional channels can be added by connecting each output to its respective summing node. For additional information on this application refer to AN83-7



Audio Crosspoint Switch
Figure 2

n-channel JFET 8 switch array

Designed for Military and Industrial Applications . . .

■ High Speed Sense/Drive Switch Array

ABSOLUTE MAXIMUM RATINGS (25°C)

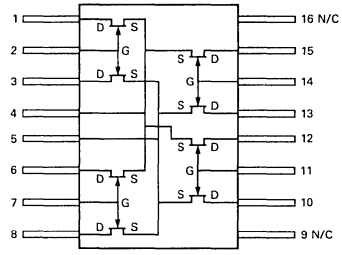
For Each Individual Chip:

Gate-Source Voltage ..... −25V
Gate-Drain Voltage ..... −25V
Gate Current ..... 100 mA
Drain Current ..... 400 mA
Storage Temp Range ..... −65°C to +200°C
Oper Temp Range ..... −55°C to +150°C
Lead Temp (Soldering, 10 sec) ..... +300°C
Power Dissipation ..... 300 mW
Derate above 25°C ..... 2.3 mW/°C

BENEFITS

- Low $R_{DS(ON)}$ < 7 OHMS
- High Speed
- T_R = 1 ns; $T_{(OFF)}$ = 5 ns
- High Radiation Resistance

PACKAGE: 16 PIN FLAT PACKAGE



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		Min	Typical	Max	Unit	Test Condition
1	STATIC	I_{GSSR}			2.0	nA	V_{GS} = −15V, V_{DS} = 0
2		I_{GSSR}			5	μA	V_{GS} = −15V, V_{DS} = 0, TA = 125°C
3		B_{VGSS}	−25			V	I_G = 8μA, V_{DS} = 0
4		$V_{GS(off)}$	−5		−10	V	V_{DS} = 5V, I_D = 100 nA
5		$I_{D(off)}$			1	nA	V_{DS} = 5V, V_{GS} = −10V
6		$I_{D(off)}$			5	μA	V_{DS} = 5V, V_{GS} = −10V, TA = 125°C
7		$R_{DS(on)}$			7	ohm	V_{GS} = 0, I_D = 10 mA
8	DYNAMIC	C_{iss}			30	pf	V_{DS} = 0, V_{GS} = −10V, f = 1 mHz
9		C_{rss}			15	pf	V_{DS} = 0, V_{GS} = −10V, f = 1 mHz
10		t_d		3		ns	V_{DD} = 1.5V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = 12V
11		$t_{(off)}$		5		ns	
12		t_f		5		ns	
13		t_r		1		ns	

n-channel enhancement—mode lateral D-MOS FETs

Siliconix

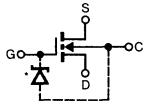
designed for Military and Industrial Applications . . .

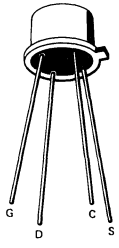
- **High Speed Switching**
- **Analog Switch**
- **Multiplexer**
- **Digital Switch**
- **A to D Converters**
- **D to A Converters**
- **Choppers**
- **Sample and Hold**

BENEFITS

- **High Speed Switching**
- **Ultra Low Feedback Capacitance**
- **Low $R_{DS(ON)}$**
- **Diode Protected Gate**

TO-72
See Section 6





ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current ..... 50 mA
Total Device Dissipation at 25°C
Case Temperature 1.2W
Storage Temperature Range ..... −65° to +150°C
Lead Temperature
(1/16" from case for 10 sec)..... 300°C
Operating Temperature Range ..... −55° to +150°C

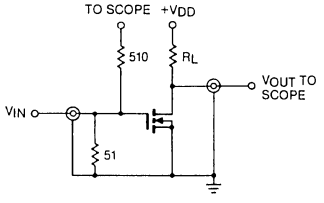
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic—DC		Min	Typ	Max	Unit	Test Conditions
I_{GSS}	Gate Reverse Current		0.1	1	μA	V_{GS} = 20V, V_{DS} = V_{GS} = V_{BS} = 0
B_{VSD}	Breakdown Voltage Source to Drain	10			V	V_{GD} = V_{BD} = −5V, I_D = 1 μA
B_{VSB}	Breakdown Voltage Source to Body	10			V	I_S = 10 μA, V_{GB} = 0
B_{VDS}	Breakdown Voltage Drain to Source	15			V	V_{GS} = V_{BS} = 0V, I_D = 10 μA
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5		2 5	V	V_{DS} = V_{GS} = V_{th}, I_D = 10 μA
gfs	Common-Source Forward Transconductance	25	30		mmhos	V_{DS} = 15V, I_D = 20 mA, F = 1 KHz
$R_{DS(ON)}$	Drain to Source Resistance					I_D = 5 mA, V_{BS} = 0V
				18	Ω	V_{GS} = 5V
				12	Ω	V_{GS} = 10V
			8		Ω	V_{GS} = 15V
Characteristic—AC		**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Small Signal Capacitance						V_{DS} = 10V, V_{GS} = V_{BS} = −15V, f = 1 MHz
$C_{(GS+GD+GB)}$	Gate Mode			17	pF	
$C_{(GD+DS)}$	Drain Mode			7	pF	
C_{DG}	Reverse Transfer			2.5	pF	

SWITCHING CHARACTERISTICS

TEST CONDITIONS

Switching

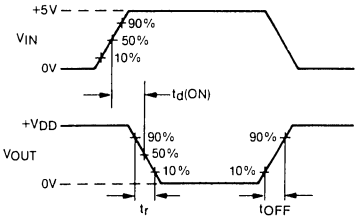


Input pulse t_d, t_r < 1ns
Pulse width = 100ns
Rep rate = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

		td(ON) (ns)		tr(ns)		tOFF(ns)	
VDD	RL	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

*tOFF is dependent on R_L and C_L and does not depend on the device characteristics

Si8901
Ring Demodulator/ Balanced Mixer

Siliconix

FEATURES

- High Third-Order Intercept Point
- <6% Device Matching Error

BENEFITS

- Low Harmonic Distortion
- Wide Dynamic Range
- Reduced System Component Count

APPLICATIONS

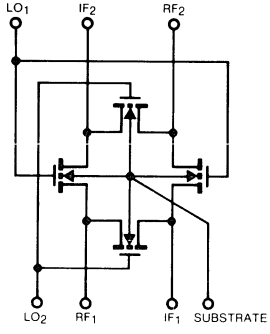
- HF Mixer/Demodulator
- HF Modulator/Up-converter

Contact factory for Application Note AN 85-2.

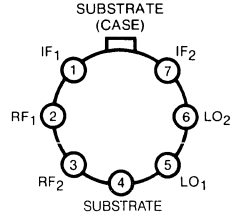
DESCRIPTION

The Si8901 Ring Demodulator/Balanced Mixer offers significant improvement for HF mixer applications where the third-order harmonic distortion has been a problem. When used as a commutation HF double-balanced mixer, the Si8901 provides a high-fidelity IF output with typical conversion loss of 8 dB. Signal frequencies may be as high as 150 MHz. Available in an 8-pin TO-99 package, this device is specified over -55 to 125°C operating temperature range.

FUNCTIONAL BLOCK DIAGRAM



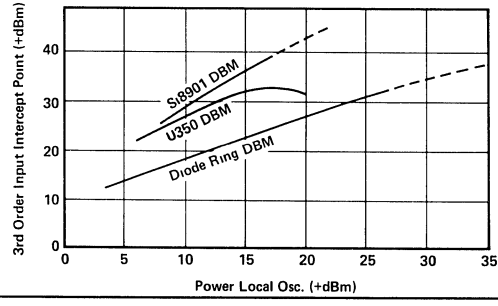
PIN CONFIGURATION



TOP VIEW

Order Numbers:
Si8901A (TO-78)
Si8901Y (SO 14)
See Section 6

PERFORMANCE COMPARISON



ABSOLUTE MAXIMUM RATINGS

V_{DS} Drain to Source ..... 15 V
V_{DB} Drain to Substrate ..... 22.5 V
V_{SB} Source to Substrate ..... 22.5 V
V_{GS} Gate to Source ..... -22.5 V to 30 V
V_{GB} Gate to Substrate ..... -0.3 V to 30 V
V_{GD} Gate to Drain ..... -22.5 V to 30 V

I_D Drain Current ..... 50 mA
Operating Temperature ..... -55 to 125°C
Storage Temperature ..... -65 to 150°C
Power Dissipation (Package) ..... 640 mW*

* Derate 5 mW/C above 25°C

ELECTRICAL CHARACTERISTICS[1]

$T_A = 25°C$

	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED:	LIMITS MIN[2]	LIMITS TYP[3]	LIMITS MAX	UNIT
STATIC	Drain-Source Breakdown Voltage	BVDS	$V_{GS} = V_{SB} = -5$ V, $I_S = 10$ nA	15	25		V
	Source-Drain Breakdown Voltage	BVSD	$V_{GD} = V_{DB} = -5$ V, $I_D = 10$ nA	15			
	Drain-Substrate Breakdown Voltage	BVDB	Source Open, $V_{GB} = 0$V, $I_D = 10$ nA	22 5			
	Source-Substrate Breakdown Voltage	BVSB	Drain Open, $V_{GB} = 0$V, $I_D = 10$ uA	22 5			
	Threshold Voltage	V_{TH}	$V_{DS} = V_{GS} = V_{TH}$, $I_S = 1$ uA, $V_{SB} = 0$ V	0 1	1	2 0	
	Gate Leakage Current	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V			2	uA
	Drain-Source "ON" Resistance	r_{DS} (on)	$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		50	75	Ω
			$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 10$ V		30		
			$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 15$ V		23		
			$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 20$ V		19		
	Resistance Matching	r_{DS} (on)	$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V		3_1	7	
DYNAMIC	LO_1-LO_2 Capacitance	C_{gg}	$V_{DS} = 0$ V, $V_{BS} = -5$ 5 V, $V_{GS} = 4$ V		4 4		pF
	Conversion Loss	L_C	See Figure 1, $P_{LO} = +17$ dBm		8		dB
	Third Order Intercept	IMD_3			+35		
	Maximum Operating Frequency	f_{max}			200		MHz

NOTES:
1 Refer to PROCESS OPTION FLOWCHART for additional information
2 The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet
3 Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing

APPLICATION HINTS

Schematic of the basic commutation-type HF double-balanced mixer using resonant-gate excitation Recommended reading is AN85-2 "A Commutation Double-Balanced MOSFET Mixer of High Dynamic Range."

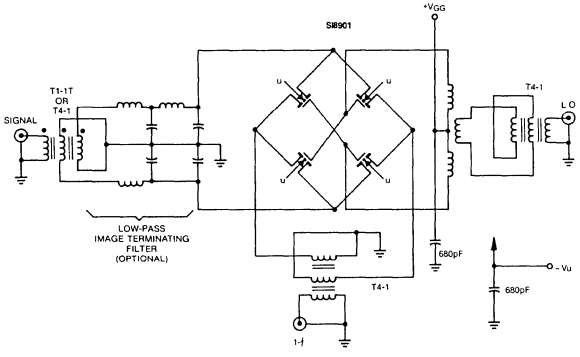
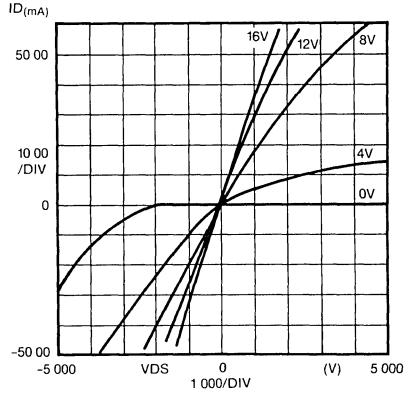


Figure 1



First and Third Quadrant I-E Characteristics Showing Effect of Gate Voltage Leading to Large-Signal Overload Distortion.

Figure 2

Small Signal JFETs

designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curve NCB
See Section 4

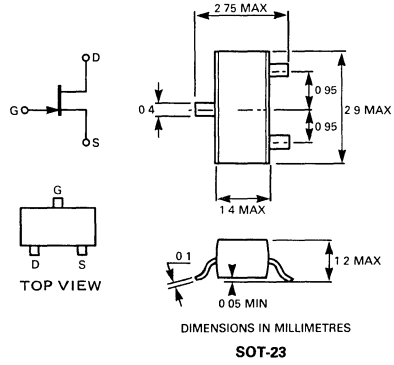
Siliconix

BENEFITS

- **Low Cost**
- **Automated Insertion Package**
- **Low Insertion Loss**
  $r_{DS(on)}$ <30 Ω (SST111)
- **No Offset or Error Voltages Generated by Closed Switch**
  Purely Resistive
  High Isolation Resistance from Driver
- **Fast Switching**
  $t_{d(on)} + t_r$ = 13 ns Typical
- **Short Sample and Hold Aperture Time**
  $C_{gd(off)}$ <5 pF
  $C_{gs(off)}$ <5 pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage ..... −35 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) ..... 360 mW
Operating Temperature Range ..... −55 to 135°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds ..... 300°C



SOT-23

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		SST111		SST112		SST113		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
I_{GSS}	Gate-Reverse Current		1		1		1	nA	V_{DS} = 0 V, V_{GS} = −15 V
$V_{GS(off)}$	Gate-Source (n+off) Voltage	−3	−10	−1	−5		−3	V	V_{DS} = 5 V, I_D = 1 μA
BV_{GSS}	Gate-Source Breakdown Voltage	−35		−35		−35		V	V_{DS} = 0, I_G = 1 μA
I_{DSS}	Saturation Drain Current (Note 1)	20		5		2		mA	V_{DS} = 15 V, V_{GS} = 0
$r_{DS(on)}$	Drain-Source on Resistance		30		50		100	ohm	V_{DS} = 0.1 V, V_{GS} = 0
$C_{dg(off)}$/ $C_{sg(off)}$	Drain-Gate off/ Source-Gate off Capacitance		5		5		5	pf	V_{DS} = 0, V_{GS} = −10 V, f = 1 MHz
$C_{dg(on)}$/+ $C_{sg(on)}$	Drain-Gate on/ Source-Gate on Capacitance		28		28		28	pf	V_{DS} = V_{GS} = 0, f = 1 MHz

NOTE: NCB
1. Pulse test duration 300 μs; duty cycle ≤3%

ORDERING INFORMATION

Device	Marking
SST111	C11
SST112	C12
SST113	C13

Small Signal JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curve PSA/ PSB/PSC See Section 4

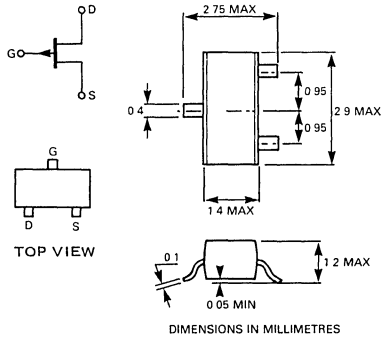
Siliconix

BENEFITS

- **Low Cost**
- **Simplifies Series-Shunt Switching when Combined with SST113, its N-Channel Complement**
- **Low Insertion Loss**
  $r_{DS(on)}$ <85 Ω (SST174)
- **No Offset or Error Voltages Generated by Closed Switch**
  Purely Resistive
  High Isolation Resistance from Driver
- **Short Sample and Hold Aperture Time**
  $C_{sg(off)}$ 6.0 pF Typical
  $C_{dg(off)}$ 6.0 pF Typical
- **Fast Switching**
  $t_{d(on)} + t_r$ = 7 ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... 30 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) ..... 360 mW
Operating Temperature Range ..... −55 to 135°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) ..... 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		SST174 Min	SST174 Max	SST175 Min	SST175 Max	SST176 Min	SST176 Max	SST177 Min	SST177 Max	Unit	Test Conditions
I_{GSS}	Gate-Reverse Current (Note 2)		1		1		1		1	nA	V_{DS} = 0, V_{GS} = 20 V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	0.8	2.25	V	V_{DS} = −15 V, I_D = −10 nA
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		30		V	V_{DS} = 0, I_G = 1 μA
I_{DSS}	Saturation Drain Current (Note 3)	−20	−135	−7	−70	−2	−35	−1.5	−20	mA	V_{DS} = −15 V, V_{GS} = 0
$r_{DS(on)}$	Static Drain-Source ON Resistance		85		125		250		300	ohm	V_{GS} = 0, V_{DS} = −0.1 V
$C_{dg(off)}$ / $C_{sg(off)}$	Drain-Gate off/ Source-Gate off Capacitance		TYP 6		TYP 6		TYP 6		TYP 6	pf	V_{DS} = 0, V_{GS} = 10 V, f = 1 MHz
$C_{dg(on)}$ / $C_{sg(on)}$	Drain-Gate on/ Source-Gate on Capacitance		TYP 32		TYP 32		TYP 32		TYP 32	pf	V_{DS} = V_{GS} = 0, f = 1 MHz

NOTES: **PSA/PSB/PSC**

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ≤3%

ORDERING INFORMATION

Device	Marking
SST174	S74
SST175	S75
SST176	S76
SST177	S77

Small Signal JFETs *designed for . . .*

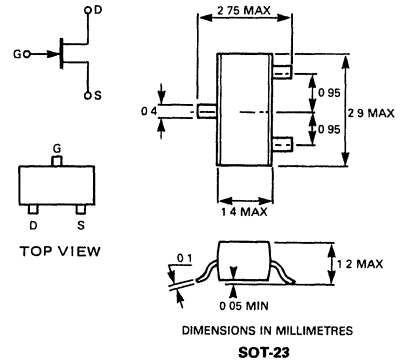
■ General Purpose Amplifiers

Performance Curve NP
See Section 4

Siliconix

BENEFITS

- **High Input Impedance**
  I_G = 5 pA Typical
- **Good for Low Power Supply Operation**
  $V_{GS(off)} < 1.5$ V (SST201)



DIMENSIONS IN MILLIMETRES
SOT-23

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ... −40 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C
(Derate 3.27 mW/°C) ..... 360 mW
Operating Temperature Range ..... −55 to 135°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		SST201		SST202		SST203		SST204		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{GSS}	Gate Reverse Current (Note 2)		0.1		0.1		0.1		0.1	nA	V_{DS} = 0, V_{GS} = −20 V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.3	−1.5	−0.8	−4	−2.0	−10.0	−0.3	−2.0	V	V_{DS} = 20 V, I_D = 10nA
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		−40		V	V_{DS} = 0, I_G = 1μA
I_{DSS}	Saturation Drain Current (Note 3)	0.2	1.0	0.9	4.5	4.0	20	0.2	3	mA	V_{DS} = 20 V, V_{GS} = 0
I_G	Gate Current		TYP 5		TYP 5		TYP 5		TYP 5	pA	V_{DG} = 20 V, I_D = 200 μA
g_{fs}	Common-Source Forward Transconductance (Note 3)	500		1000		1500		500		μmhos	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
g_{os}	Common-Source Output Conductance		TYP 1.0		TYP 3.5		TYP 10.0		TYP 2.0	μmhos	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		TYP 4		TYP 4		TYP 4		TYP 4	pf	V_{DS} = 20 V, V_{GS} = 0
e_n	Noise Voltage		TYP 5		TYP 5		TYP 5		TYP 10	nV/√Hz, f = 1 kHz	V_{DS} = 10 V, V_{GS} = 0, f = 1 kHz

NPA

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

ORDERING INFORMATION

Device	Marking
SST201	P01
SST202	P02
SST203	P03
SST204	P04

n-channel DMOS FETs

Designed for Military and Industrial Applications . . .

- **High-Speed Switching**
- **Analog Switch**
- **Multiplexer**
- **Digital Switch**
- **A to D Converters**
- **D to A Converters**
- **Choppers**
- **Sample and Hold**

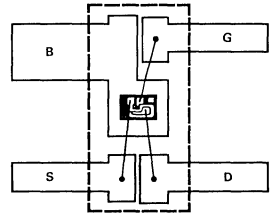
Performance Curve DMCB
See Section 4

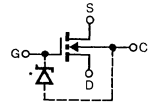
BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1 ns)
- Diode protected gate

SOT-143

TOP VIEW





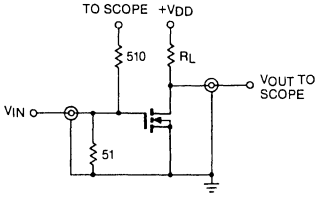
ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current 50mA
Total Device Dissipation at 25°C
Case Temperature 360mW
Storage Temperature Range . . . . . −55° to +150°C
Lead Temperature (1/16″ from case for 10 sec.) . . . . . 300°C
Operating Temperature Range . . . . . --55° to +150°C

PARAMETER		SD211	SD213	SD215	UNIT
V_{DS}	Drain-to-source	+30	+10	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+15	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+25	Vdc
V_{GS}	Gate-to-source	−15 +25	−15 +25	−25 +30	Vdc
V_{GB}	Gate-to-substrate	−0.3 +25	−0.3 +25	−0.3 +30	Vdc
V_{GD}	Gate-to-drain	−30 +25	−15 +25	−25 +30	Vdc

TEST CONDITIONS

Switching

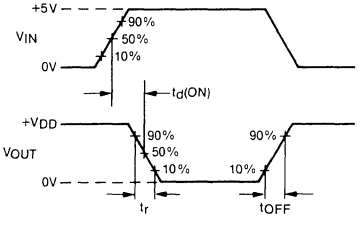


Input pulse t_d, t_r < 1 ns
Pulse width = 100 ns
Rep rate = 1 MHz

SAMPLING SCOPE

t_r < 360 ps
R_{IN} = 1 MΩ
C_{IN} = 2 0pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

		$t_{d(ON)}$ (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0 6	1 0	0 7	1 0	9 0	*
10	680	0 7		0 8		9 0	*
15	1k	0 9		1 0		14 0	*

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified.)

		PARAMETER		TEST CONDITIONS	SST211 Min	SST211 Typ	SST211 Max	SST213 Min	SST213 Typ	SST213 Max	SST215 Min	SST215 Typ	SST215 Max	UNIT
1		**Breakdown voltage** BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$ $V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	30 10	35 25		 10	 25		 20	 25		V
2		BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			20			
3		BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			25			
4		BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			25			
5	STATIC	**Leakage current** I_{DS} (OFF)	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$ $V_{DS} = +20V$		1	10		1	10		 1	 10	nA
6	STATIC	I_{SD} (OFF)	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$ $V_{SD} = +20V$		1	10		1	10		 1	 10	
7		I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = +25V$ $V_{GB} = +30V$			10			10			 10	μA
8		V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
9		r_{DS} (ON)	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$ $V_{GS} = +25V$		 50 30 23 19	 75 50		 50 30 23 19	 75 50		 50 30 23 19 17	 75 50	Ω

AC ELECTRICAL CHARACTERISTICS

		PARAMETER		TEST CONDITIONS	SST211 Min	SST211 Typ	SST211 Max	SST213 Min	SST213 Typ	SST213 Max	SST215 Min	SST215 Typ	SST215 Max	UNIT
10	DYNAMIC	gfs	Forward trans-conductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	9.0	15		9.0	15		9.0	15		mmhos
		Small Signal Capacitances (See capacitance model)		$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										pF
11		$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	
12		$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	
13		$C_{(GS+SB)}$	Source node			3.5	6.0		3.5	6.0		3.5	6.0	
14		C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	

DMCB

ORDERING INFORMATION

Device	Marking
SST211	D11
SST213	D13
SST215	D15

Small Signal JFETs

designed for . . .

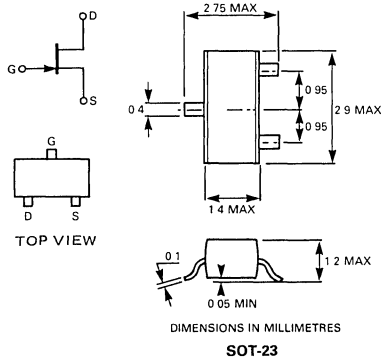
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curve NZB
See Section 4

Siliconix

BENEFITS

- **Industry Standard Part In Low Cost Plastic Package**
- **High Power Gain 11 dB Typical at 450 MHz Common-Gate**
- **Low Noise 2.7 dB Typical at 450 MHz**
- **Wide Dynamic Range Greater than 100 dB**
- **Easily Matches to 75 Ω Input**



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage ..... 25 V
Source-Gate Voltage ..... 25 V
Forward Gate Current ..... 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) ..... 360 mW
Operating Temperature Range ..... −55 to 135°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		SST308		SST309		SST310		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
I_{GSS}	Gate-Reverse Current		−1		−1		−1	nA	V_{GS} = −15 V, V_{DS} = 0
BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		−25		V	V_{DS} = 0, I_G = 1 μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−6.5	−1	−4	−2	−6.5	V	V_{DS} = 10 V, I_D = 1 nA
I_{DSS}	Saturation Drain Current (Note 1)	12	60	12	30	24	60	mA	V_{DS} = 10 V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance	8000		10000		8000		μmhos	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz
NF	Noise Figure		TYP 2.7		TYP 2.7		TYP 2.7	dB	V_{DS} = 10 V, I_D = 10 mA, f = 450 MHz

NOTE: **NZB**
1. Pulse test PW 300 μs; duty cycle ≤3%

ORDERING INFORMATION

Device	Marking
SST308	Z08
SST309	Z09
SST310	Z10

3

monolithic dual n-channel JFETs *designed for . . .*

- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Siliconix

Performance Curves NNR See Section 4

BENEFITS

- **Minimum System Error and Calibration**
- **15 mV Offset Maximum (SST404)**
  95 dB Minimum CMRR (SST404)
- **Low Drift with Temperature**
  25 μV/° C Maximum (SST404)
- **Operates from Low Power Supply Voltages**
  $V_{GS(off)} < 2.5V$
- **Simplifies Amplifier Design**
  Output Conductance < 2 μmho
- **Low Noise**
  e_n = 6 nV$\sqrt{Hz}$ at 10 Hz Typical

ABSOLUTE MAXIMUM RATINGS (25° C)

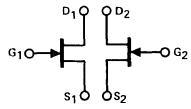
Gate-Drain or Gate-Source Voltage . . . . . 50 V
Forward Gate Current . . . . . 10 mA
Device Dissipation (each side)
@ T_A = 85° C derate 2.6 mW/° C . . . . . 300 mW
Total Device Dissipation
@ T_A = 85° C (derate 5 mW/° C) . . . . . 500 mW
Storage Temperature Range . . . . . −65 to 200° C

ORDERING INFORMATION

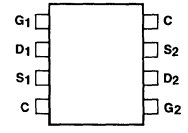
Device	Marking
SST404	404
SST405	405
SST406	406

ELECTRICAL CHARACTERISTICS (@ 25° C unless otherwise noted)

		Characteristic		404 Min	404 Max	405 Min	405 Max	406 Min	406 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate Source Breakdown Voltage	−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		−25		−25		−25	pA	V_{DS} = 0, V_{GS} = −30 V	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4		$V_{GS(on)}$	Gate Source Voltage (on)		−2.3		−2.3		−2.3		V_{DG} = 15 V, I_D = 200 μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G	Gate Current (Note 1)		−15		−15		−15	pA	V_{DG} = 15 V,	
7					−10		−10		−10	nA	I_D = 200 μA	T_A = 125° C
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0 I_G = ±1 μA	
9		g_{fs}	Common Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common Source Output Conductance		20		20		20			
11	DYNAMIC	g_{fs}	Common Source Forward Transconductance	1000	2000	1000	2000	1000	2000		V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common Source Reverse Transfer Capacitance		3.0		3.0		3.0			
15		$\bar{e}_N$	Equivalent Short Circuit Input Noise Voltage		20		20		20	nV $\sqrt{Hz}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common Mode Rejection Ratio (Note 3)	95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18		$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate Source Voltage Differential Drift (Note 4)		25		40		80	μV/° C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55° C, T_B = +25° C T_C = +125° C



SOIC—8 PIN



NOTES
1 Approximately doubles for every 10° C increase in T_A 2 Pulse test duration = 300 μs, duty cycle ≤ 3% 3 CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS1}-V_{GS2} \rvert}\right]$, ΔV_{DD} = 10 V
4 Measured at end points, T_A, T_B and T_C

NNR

Small Signal JFETs *designed for . . .*

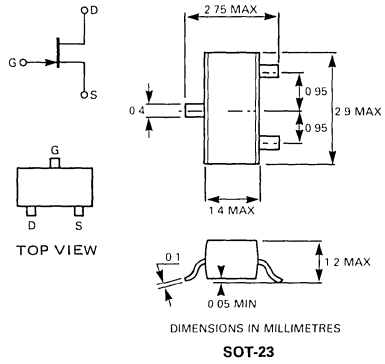
- **VHF Amplifiers**
- **Mixers**

Siliconix

Performance Curve NH
See Section 4

BENEFITS

- **Low Noise**
  NF=3dB Typical at 400/MHz
- **Wide Band**
  High g_{fs}/C_{iss} Ratio



SOT-23

ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-Drain or Gate-Source Voltage ..... −30 V
Gate Current ..... 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW°C) ..... 360 mW
Operating Temperature Range ..... −55 to 135°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic	Min	Max	Unit	Test Conditions	
I_{GSS}	Gate Reverse Current		1.0	nA	V_{GS} = 15 V, V_{DS} = 0 V	
BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = 1 μA, V_{DS} = 0 V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−6		V_{DS} = 15 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
g_{os}	Common-Source Output Conductance		50			
C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		4			
C_{oss}	Common-Source Output Capacitance		2			

	Characteristic	100 MHz TYP	400 MHz TYP	Unit	Test Conditions
g_{iss}	Common-Source Input Conductance	50	700	μmho	V_{DS} = 15 V, V_{GS} = 0 V
b_{iss}	Common-Source Input Susceptance	2000	8000		
g_{oss}	Common-Source Output Conductance	45	60		
b_{oss}	Common-Source Output Susceptance	700	3000		
g_{fs}	Common-Source Forward Transconductance		5500		
G_{ps}	Common-Source Power Gain	20	13	dB	V_{DS} = 15 V, I_D = 5 mA
NF	Noise Figure	1	2.5		V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ

NOTE: **NH**

1. Pulse test duration = 300 μs.

ORDERING INFORMATION

Device	Marking
SST4416	H16

3

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves NCB
See Section 4

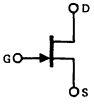
BENEFITS

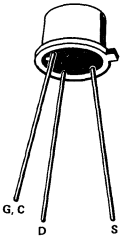
- Low Insertion Loss
  $r_{DS(on)} < 50\ \Omega$ (U202)
- Good Off-Isolation
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-18
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U200 Min	U200 Max	U201 Min	U201 Max	U202 Min	U202 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-1		-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		V_{DS} = 20 V, I_D = 10 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	V_{DS} = 10 V, V_{GS} = -12 V	
					1		1		1	μA		150°C
6		I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		8		8		8		V_{DS} = 0 V_{GS} = -12 V	

NOTE:
1. Pulse test required, pulsewidth = 300 μsec, duty cycle ≤ 3%.

NCB

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

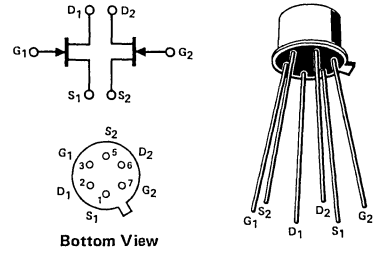
Performance Curves NQP
See Section 4

■ Differential Amplifiers

BENEFITS

- Good Matching Characteristics

TO-71
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C
(Derate 1.7 mW/°C to 200°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4.0			
6		I_G	Gate Operating Current		-50	pA	V_{DG} = 20 V, I_D = 200 μA	
					-250	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	5000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
				1000				f = 100 MHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		10		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	10	10	10	10	10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV	V_{DG} = 20 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	μV/°C		T_A = 25°C, T_B = 125°C
19				10	25	50	75	100			T_A = -55°C, T_B = 25°C
20		$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance	5	5	5	5	5	μmho		

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

NQP

3

matched dual n-channel JFET *designed for . . .*

Siliconix

■ Wideband Differential Amplifiers

Performance Curves NZF-D, NNZ See Section 4

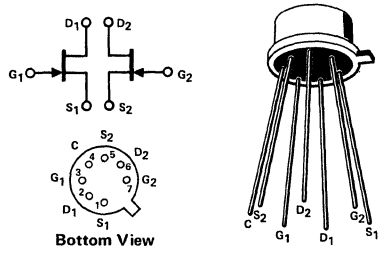
BENEFITS

- **High Gain through 100 MHz**
  g_{fs} = 4500 μmho Minimum
- **Matching Characteristics Specified**

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 3.85 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 7.7 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to + 200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-78
See Section 6



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{fs}	Common-Source Forward Transconductance	4500	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
8		g_{os}	Common-Source Output Conductance		200		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		200		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
10		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
13	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
14		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
15		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.85	1			f = 1 kHz
16		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTES:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 30%.
2. Assumes smaller value in numerator.

NZF-D, NNZ

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NVA
See Section 4

- **Analog Switches**
- **Commutators**
- **Choppers**

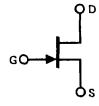
BENEFITS

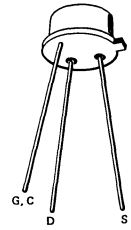
- **Ultra-Low Insertion Loss**
  $r_{DS(on)}$ <3.0Ω **(U290)**
- **High Off-Isolation**
  $I_{D(off)}$ <1 nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 100 mA
Drain Current . . . . . 1.5 A
Total Device Dissipation at 25°C
Free-Air Temperature (Note 1) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-52
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U290 Min	U290 Max	U291 Min	U291 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-1.5	-4.5		V_{DS} = 15 V, I_D = 3 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6					1		1	μA		150°C
7		$V_{DS(on)}$	Drain-Source ON Voltage		30		70	mV	V_{GS} = 0, I_D = 10 mA	
8		I_{DSS}	Saturation Drain Current (Note 2)	500		200		mA	V_{DS} = 10 V, V_{GS} = 0	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance	10	3.0	2	7	Ω	V_{GS} = 0 V, I_D = 10 mA	
10	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance	1.0	3.0	2	7	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{SGO}	Source-Gate OFF Capacitance		30		30	pF	V_{SG} = 15 V, I_D = 0	f = 1 MHz
12		C_{DGO}	Drain-Gate OFF Capacitance		30		30		V_{DG} = 15 V, I_S = 0	
13		$C_{SG}+C_{DG}$	Source Gate Plus Drain Gate On Capacitance		160		160		V_{DS} = 0, V_{GS} = 0	
14	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = 1.5 V, $I_{D(on)}$ = 30 mA, R_L = 50 Ω, $V_{GS(on)}$ = 0 V, $V_{GS(off)}$ = -12 V (U290) $V_{GS(off)}$ = - 7 V (U291)	
15		t_r	Rise Time		20		20			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		15			
17		t_f	Fall Time		20		20			

NOTES: **NVA**

1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PSA/PSB/PSC See Section 4

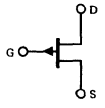
BENEFITS

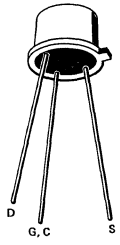
- Low Insertion Loss
  $r_{DS(on)} < 85\ \Omega$ (U304)
- High Off-Isolation
  $I_{D(off)} < 500$ pA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation, Free-Air
(Derate 2.8 mW/°C) . . . . . 350 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0	
2					1.0		1.0		1.0	µA		125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		V_{DS} = -15 V, I_D = -1 µA	
5		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		V_{GS} = 0, I_D = -15 mA (U304), I_D = -7 mA (U305), I_D = -3 mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	V_{DS} = -15 V, V_{GS} = 0	
7		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15 V, V_{GS} = 12 V (U304), V_{GS} = 7 V (U305), V_{GS} = 5 V (U306)	
8					-1.0		-1.0		-1.0	µA		125°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0 V, I_D = -1 mA	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		27		27		27	pF	V_{DS} = -15 V, V_{GS} = 0	
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		V_{DS} = 0, V_{GS} = 12 V (U304) V_{GS} = 7 V (U305), V_{GS} = 5 V (U306)	f = 1 MHz
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns		
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn-OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 µs, duty cycle ≤ 3%.

PSA/PSB/PSC

n-channel JFETs *designed for . . .*

Siliconix

- **VHF Amplifiers**
- **Front End High Sensitivity Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZB
See Section 4

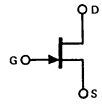
BENEFITS

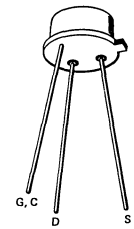
- Industry Standard
- High Power Gain
  16 dB at 105 MHz, Common-Gate
  11 dB at 450 MHz, Common-Gate
- Low Noise
  2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- 75 Ω Input Match Common Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 20 mA
Total Power Dissipation at T_A = 25°C . . . . . 500 mW
Power Derating to 150°C . . . . . 4.0 mW/°C
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-52
See Section 6





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U308 Min	U308 Typ	U308 Max	U309 Min	U309 Typ	U309 Max	U310 Min	U310 Typ	U310 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150			-150	pA	V_{GS} = -15 V, V_{DS} = 0	
2						-150			-150			-150	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
7	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10	17		10	17		10	17		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance			250			250			250	μmho		
9		C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = -10 V, V_{DS} = 10 V	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
11		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
13					14			14			14				f = 450 MHz
14		g_{og}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 105 MHz
15					0.32			0.32			0.32				f = 450 MHz
16		G_{pg}	Common-Gate Power Gain (Note 2)	14	16		14	16		14	16		dB		f = 105 MHz
17				10	11		10	11		10	11				f = 450 MHz
18		NF	Noise Figure		1.5	2.0		1.5	2.0		1.5	2.0			f = 105 MHz
19					2.7	3.5		2.7	3.5		2.7	3.5			f = 450 MHz

NOTES:
1. Pulse test duration = 2 ms
2. Gain (G_{pg}) measured at optimum input noise match.

NZB

U311

PREFERRED PART U310

n-channel JFET
designed for . . .

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

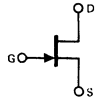
Siliconix

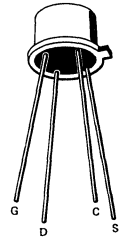
Performance Curves NZB
See Section 4

BENEFITS

- High Power Gain
  16 dB Typ @ 105 MHz, Common-Gate
  11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure
  1.5 dB Typ @ 105 MHz
  2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

TO-72
See Section 6





ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Typ	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-150		pA	V_{GS} = -15 V, V_{DS} = 0	
2					-150		nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6			V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	20	60		mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		1		V	I_G = 1 mA, V_{DS} = 0	
7	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000		17,000	μmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance		250				
9		C_{gd}	Gate-Drain Capacitance		2.5		pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance		5.0				

NOTE:
1. Pulse test duration = 2 ms.

NZB

n-channel JFETs *designed for . . .*

Siliconix

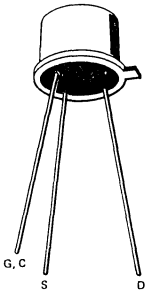
- **VHF Buffer Amplifiers**
- **IF Amplifiers**

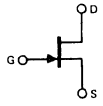
Performance Curves NIP See Section 4

BENEFITS

- High Gain
  g_{fs} = 120,000 μmho Typical
- Wide Dynamic Range
- Low Intermodulation Distortion

TO-39
See Section 6





ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . −25 V
Gate Current . . . . . 100 mA
Total Device Dissipation (25°C Case Temperature) . . . . . .3 W
Power Derating (to 150°C) . . . . . 24 mW/°C
Storage Temperature Range . . . . . −55 to +150°C
Operating Temperature Range . . . . . −55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U320			U321			U322			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-0 5			-0 5			-0.5	μA		T = 100°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2		-10	-1		-4	-3		-10	V	V_{DS} = 5 V, I_D = 1 mA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				I_G = -1 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	100		500	80		250	200		700	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1			1			1	V	I_G = 1 mA, V_{DS} = 0 V	
7		$r_{DS(on)}$	Drain-Source ON Resistance			10			11			8	Ω	V_{GS} = 0 V, I_D = 10 mA	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	75	120	200	75	120	200	75	130	200	mmhos	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance			30			30			30	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance			15			15			15			
11		C_{gs}	Gate-Source Capacitance		12			12			12			V_{GS} = -10 V, I_D = 0	
12		C_{gd}	Gate-Drain Capacitance		12			12			12			V_{GD} = -10 V, I_S = 0	
13		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		2			2			2		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 5 V, I_D = 10 mA	f = 1 kHz
14	HIGH FREQ	g_{fg}	Common Gate Forward Transconductance		55			55			55		mmho	V_{DG} = 20 V, I_D = 25 mA	f = 50 MHz
15		g_{ig}	Common-Gate Input Conductance		56			56			56				
16		g_{og}	Common-Gate Output Conductance		0 5			0.5			0 5				
17		G_{PS}	Power Gain (Note 3)		9			9			9		dB		
18		F_t	Gain-Bandwidth (Note 4)		400			400			400		MHz	V_{DS} = 15 V, V_{GS} = 0 V	
19		NF	Noise Figure (Note 3)		2.5			2 5			2 5		dB	V_{DG} = 20 V, I_D = 25 mA	f = 30 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A
2. Pulse test duration = 2 ms.
3. Noise figure (SSB) and power gain measured in circuit shown in Figure 1
4. Computed as g_{fs}/C_{rss}.

NIP

3

quad-ring demodulator designed for . . .

Siliconix

- **VHF Double-Balanced Mixers**
- **Analog Multipliers**

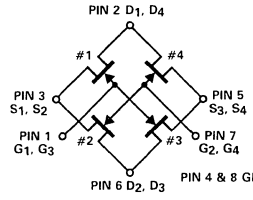
Performance Curves NZB See Section 4

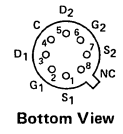
BENEFITS

- High IMD Intercept Point
- Conversion Gain
- High 1 dB Compression
- Suitable for PC Board Construction

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... −25V
Gate Current ..... 25 mA
Total Continuous Power Dissipation
at (or Below) 25°C Free Air Temperature
(Derate 8.0 mW/°C to 150°C 1W
Storage Temperature Range ..... −65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C



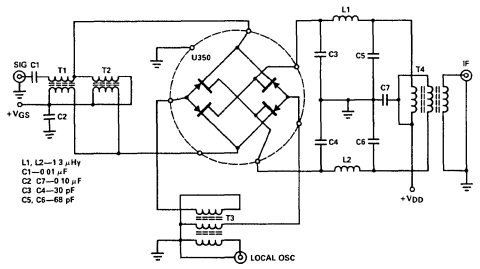


Bottom View

FEATURES

- 4 Matched U310 JFETS
- Low Turn-on Resistance
- High Transductance
  Reference Application Note AN72-1

Contact factory for Application Note AN 73-4.



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U350 Min	U350 Typ	U350 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			−1	nA	V_{GS} = −15 V, V_{DS} = 0 (Note 1)	
2						−1	μA		T_A = +125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25			V	I_G = −1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−2		−6	V	I_D = 1 nA, V_{DS} = 10 V (Note 1)	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1	V	I_G = 1 mA, V_{DS} = 0 (Note 1)	
6		I_{DSS}	Drain Saturation Current	24		60	mA	V_{DS} = 15 V, V_{GS} = 0 (Notes 1 and 2)	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10		18	mΩ	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz (Note 1)
8		g_{os}	Common-Source Output Conductance			150	μΩ		
9		C_{gs}	Gate-Source Capacitance			5	pF	V_{GS} = −10 V, I_D = 0	f = 1 MHz (Note 1)
10		C_{gd}	Drain Gate Capacitance			2.5		V_{GD} = −10 V, I_S = 0	
11		$R_{ds(on)}$	Drain-Source ON Resistance		50	90	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
12	HF	G_c	(Conversion Gain)		4		dB	V_{DS} = 20 V, V_{GS} = ½$V_{GS(off)}$, R_D = 1,700 Ω	f = 100 MHz (Note 3)
13		NF	Noise Figure		7				
14	MATCH	I_{DSS}/I_{DSS}	Saturation Drain Current Ratio	0.9		1.0		V_{DS} = 15 V, V_{GS} = 0 (Note 2)	
15		$V_{GS(off)}/V_{GS(off)}$	Gate-Source Cutoff Voltage Ratio	0.9		1.0		V_{DS} = 15 V, I_D = 1 nA	
16		g_{fs}/g_{fs}	Common-Source Forward Transconductance	0.9		1.0		V_{DS} = 15 V, I_D = 10 mA	f = 1 kHz
17		g_{os}/g_{os}	Differential Output Conductance	0.9		1.0			

NOTES NZB
1 Other gate terminal clamped to −8 V 2 Pulse test PW 300 μsec DC ≤ 3% 3 See Figure 1

monolithic dual n-channel JFETs *designed for . . .*

- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

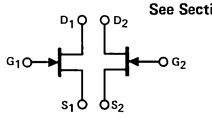
Siliconix

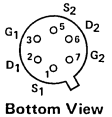
Performance Curves NNR See Section 4

BENEFITS

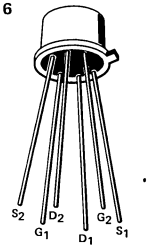
- Minimum System Error and Calibration
  5 mV Offset Maximum (U401)
  95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
  10 μV/°C Maximum (U401, 02)
- Operates from Low Power Supply Voltages
  $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\overline{e}_n = 6\ nV/\sqrt{Hz}$ at 10 Hz Typical

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side) @ T_A = 85°C derate 2.6 mW/°C	300 mW
Total Device Dissipation @ T_A = 85°C (derate 5 mW/°C)	500 mW
Storage Temperature Range	−65 to 200°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		Characteristic		U401		U402		U403		U404		U405		U406		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		−25		−25		−25		−25		−25		−25	pA	V_{DS} = 0, V_{GS} = −30 V	
3		$V_{GS(off)}$	Gate Source Cutoff Voltage	−5	−2 5	−5	−2 5	−5	−2.5	−5	−2 5	−5	−2 5	−5	−2 5	V	V_{DS} = 15 V, I_D = 1 nA	
4		$V_{GS(on)}$	Gate-Source Voltage (on)		−2 3		−2 3		−2 3		−2 3		−2 3		−2 3		V_{DG} = 15 V, I_D = 200 μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0 5	10 0	0 5	10 0	0 5	10 0	0 5	10 0	0 5	10 0	0 5	10 0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G	Gate Current (Note 1)		−15		−15		−15		−15		−15		−15	pA	V_{DG} = 15 V,	
7					−10		−10		−10		−10		−10		−10	nA	I_D = 200 μA	T_A = 125°C
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA	
9	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common Source Output Conductance		20		20		20		20		20		20			
11		g_{fs}	Common Source Forward Transconductance	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000		V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
12		g_{os}	Common Source Output Conductance		2 0		2 0		2 0		2 0		2 0		2 0			
13		C_{iss}	Common-Source Input Capacitance		8 0		8 0		8 0		8 0		8 0		8 0	pF		f = 1 MHz
14		C_{rss}	Common Source Reverse Transfer Capacitance		3 0		3 0		3 0		3 0		3 0		3 0			
15		$\overline{e}_N$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	nV/√Hz	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17		$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55°C, T_B = +25°C, T_C = +125°C

NOTES
1 Approximately doubles for every 10°C increase in T_A 2 Pulse test duration = 300 μs, duty cycle ≤ 3% 3 CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V
4 Measured at end points, T_A, T_B and T_C

NNR

3

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NQP
See Section 4

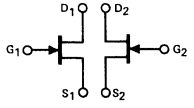
BENEFITS

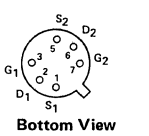
- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (U410)
  70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  10 μV/°C Maximum (U410)
- Simplifies Amplifier Design
  Low Output Conductance

ABSOLUTE MAXIMUM RATINGS (25°C)

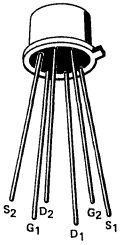
Gate-To-Gate Voltage ..... ±40 V
Gate-Drain or Gate-Source Voltage ..... −40 V
Gate Current ..... 50 mA
Total Package Dissipation (25°C Free-Air) ..... 375 mW
Power Derating ..... 3.0 mW/°C
Storage Temperature Range ..... −65 to +150°C
Lead Temperature (1/16" from case for 10 seconds) . .300°C

TO-71
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U410			U411			U412			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-200			-200			-200	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-3 5	-0.5		-3 5	-0.5		-3 5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0 V, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0 5		5 0	0.5		5.0	0.5		5 0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
5	STATIC	I_G	Gate Current (Note 1)			-200			-200			-200	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	-0 2		-3.0	-0.2		-3 0	-0 2		-3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	600		1,200	600		1,200	600		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4 5			4 5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1 2			1.2			1.2		pF		
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A
2. Pulse test duration = 300 μsec, duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP

monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Siliconix

Performance Curves NNT
See Section 4

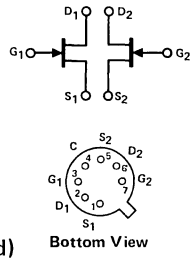
BENEFITS

- **High Input Impedance**
  I_G = 0.25 pA Maximum (U421-3)
- **High Gain g_{fs} = 120 μmho Minimum @ I_D = 30 μA (U421-6)**
- **Low Power Supply Operation**
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- **Minimum System Error and Calibration**
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage ..... ±40 V
Gate-Drain or Gate-Source Voltage ..... -40 V
Gate Current ..... 10 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3.2 mW/°C to 150°C) ..... 400 mW
Total Device Dissipation, T_A = 25°C
(Derate 6.0 mW/°C to 150°C) ..... 750 mW
Storage Temperature Range ..... -65°C to +150°C

TO-78
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	U421-3 Min	U421-3 Typ	U421-3 Max	U424-6 Min	U424-6 Typ	U424-6 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	-40	-60		-40	-60		V	I_G = -1 μA, V_{DS} = 0	
2		BV_{G1G2} Gate-Gate Breakdown Voltage	±40			±40			V	I_G = -1 μA, I_D = 0, I_S = 0	
3		I_{GSS} Gate Reverse Current (Note 1)			10			30	pA	T = +25°C	V_{GS} = -20 V, V_{DS} = 0
					10			30	nA	T = +125°C	
4		I_G Gate Operating Current (Note 1)			25			0.5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 μA
					250			500		T = +125°C	
5		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.4		-2.0	-0.4		-3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS} Gate-Source Voltage			-1.8			-2.9	V	V_{DG} = 10 V, I_D = 30 μA	
7		I_{DSS} Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs} Common-Source Forward Transconductance	300		1500	300		1500	μ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os} Common-Source Output Conductance			10			10	μ℧		
10		C_{iss} Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss} Common-Source Reverse Transfer Capacitance			1.5			1.5	pF		
12		g_{fs} Common-Source Forward Transconductance	120		350	120		350	μ℧	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
13		g_{os} Common-Source Output Conductance			3.0			3.0	μ℧		
14		$\bar{e}_n$ Equivalent Short Circuit Input Noise Voltage		20	70		20	70	nV/√Hz		f = 10 Hz
				10			10				f = 1 kHz
15		NF Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10MΩ

		Characteristic	U421, 4 Min	U421, 4 Typ	U421, 4 Max	U422, 5 Min	U422, 5 Typ	U422, 5 Max	U423,6 Min	U423,6 Typ	U423,6 Max	Unit	Test Conditions
16	MATCH	$\lvert V_{GS1} - V_{GS2}\rvert$ Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10 V, I_D = 30 μA
17		$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$ Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = -55°C, T_B = 25°C, T_C = 125°C
18		CMRR Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V

NOTES.
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V
4. Case lead not connected.

NNT

monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Siliconix

Performance Curves NNT
See Section 4

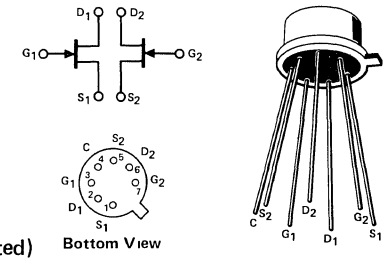
BENEFITS

- **High Input Impedance**
  I_G = 5 pA (U427)
- **High Gain g_{fs} = 120 μmho Minimum @**
  I_D = 30 μA
- **Low Power Supply Operation**
  $V_{GS(off)}$ = 2 V Maximum (U427)
- **Minimum System Error and Calibration**
  25 mV Maximum Offset

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150°C

TO-78
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U427 Min	U427 Typ	U427 Max	U428 Min	U428 Typ	U428 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1 μA, V_{DS} = 0	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40			V	I_G = −1 μA, I_D = 0, I_S = 0	
3		I_{GSS}	Gate Reverse Current (Note 1)			5			10	pA	T = +25°C	V_{GS} = −20 V, V_{DS} = 0
						5			10	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			3			5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 μA
						3			5	nA	T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2 0	−0.4		−3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS}	Gate-Source Voltage			−1.8			−2.9	V	V_{DG} = 10 V, I_D = 30 μA	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1500	μ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3 0			5.0	μ℧		
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5	pF		
12		g_{fs}	Common-Source Forward Transconductance	120		350	120		350	μ℧	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			0 5			1 0	μ℧		
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	nV/√Hz		f = 10 Hz
					10			10		nV/√Hz		f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω
16	MATCH	$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage			25			40	mV	V_{DG} = 10 V, I_D = 30 μA	
17		$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			40			80	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = −55°C, T_B = 25°C, T_C = 125°C	
18		CMRR	Common Mode Rejection Ratio (Note 3)		90			90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V	

NOTES
1 Approximately doubles for every 10°C increase in T_A
2 Measured at end points T_A, T_B and T_C
3 $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V
4 Case lead not connected

NNT

matched dual n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NZB-D
See Section 4

- **Balanced Mixers**
- **Differential Amplifiers**

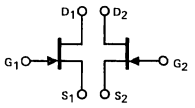
BENEFITS

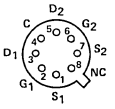
- Low Noise Figure
- Low IMD
  30 dBm Intercept Point

ABSOLUTE MAXIMUM RATINGS (25°C)

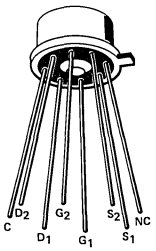
Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Continuous Power Dissipation at
(or Below) 25°C Free Air Temperature
Derate 4 mW/°C to 150°C. . . . . 500 mW
Continuous Device Dissipation (Each Side) at
(or Below) 25°C Free Air Temperature
Derate 2.4 mW/°C to 150°C . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-99/TO-78
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		U430 Min	U430 Typ	U430 Max	U431 Min	U431 Typ	U431 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150	pA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-150			-150	nA		T = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	I_G = -1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-4.0	-2.0		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0		V_{DS} = 0 V, I_G = 10 mA	
6		I_{DSS}	Saturation Drain Current (Note 4)	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0 V	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10	17		10	17		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			250			250	μmho		
9		C_{gs}	Gate-Source Capacitance			5 0			5.0	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{gd}	Drain Gate Capacitance			2 5			2 5			
11		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fs}	Common-Source Forward Transconductance		12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
13		g_{os}	Common-Source Output Conductance		0.15			0.15				
14		g_{ig}	Power-Match Source Admittance		12			12				
15		G_c	Conversion Gain (See Note 1)		3 0			3.0		dB	V_{DS} = 20 V, V_{GS} = 1/2 $V_{GS(off)}$	
16		IMD	Intercept Point (See Notes 1 and 2)		+30			+30		dBm		
17	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 3)	0.9		1 0	0 9		1.0		V_{DS} = 10 V	V_G = 0 V
18		$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	Gate-Source Cutoff Voltage Ratio (Note 3)	0.9		1.0	0.9		1 0			I_D = 1 nA
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 10 mA

NOTES:
1. VHF single-balanced mixer drain load impedance 2k Ω
2. 2-tone 3rd-order IMD.
3. Assumes smaller value in numerator.
4. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

NZB-D

3

matched dual n-channel JFETs *designed for . . .*

Siliconix

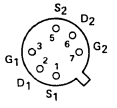
■ VHF/UHF Amplifiers

Performance Curves NZF-D
See Section 4

BENEFITS

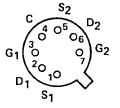
- High Gain
  g_{fs} = 4500 μmho Minimum
- Dual Version of J300 with Matched Gate-to-Source Voltage

TO-71
See Section 6

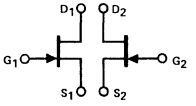


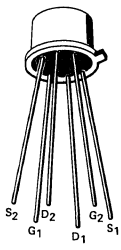
Bottom View

TO-78
See Section 6

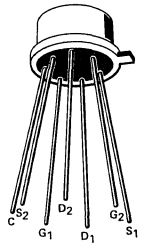


Bottom View





TO-71 = U440, U441



TO-78 = U443, U444

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage ..... ±50 V
Gate-Drain or Gate-Source Voltage ..... -25 V
Gate Current ..... 50 mA
Total Package Dissipation
(25°C Free-Air Temperature) ..... 350 mW
Power Derating ..... 2.8 mW/°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U440/U443			U441/U444			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500			-500	pA	V_{DS} = 0, V_{G} = -15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	-1		-6	V	V_{DS} = 10 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)			-500			-500	pA	V_{DG} = 10 V, I_D = 5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			200			
8		C_{iss}	Common-Source Input Capacitance		35			3.5		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8				
10	MAT	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20	mV	V_{DG} = 10 V, I_D = 5 mA	

NZF-D

NOTES:
1. Approximately doubles for every 10°C increase in T_A
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NCB See Section 4

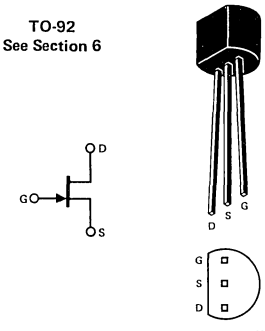
- **Analog Switches**
- **Choppers**
- **Commutators**

BENEFITS

- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (U1897)
- No Error or Offset Voltage Generated by Closed Switch
  Purely Resistive

Plastic

TO-92
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –40V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25° C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	U1897 Min	U1897 Max	U1898 Min	U1898 Max	U1899 Min	U1899 Max	Unit	Test Conditions
1		BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
2		BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40		V	$I_G = -1\ \mu A$, $I_S = 0$
3		BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40		V	$I_G = -1\ \mu A$, $I_D = 0$
4		I_{GSS}	Gate Reverse Current		–400		–400		–400	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
5		I_{DGO}	Drain-Gate Leakage Current		200		200		200	pA	$V_{DG} = 20$ V, $I_S = 0$
6	STATIC	I_{SGO}	Source-Gate Leakage Current		200		200		200	pA	$V_{SG} = 20$ V, $I_D = 0$
7		$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	$V_{DS} = 20$ V, $V_{GS} = -12$ V (U1897)
8					10		10		10	nA	$V_{GS} = -8$ V (U1898), $V_{GS} = -6$ V (U1899), $T_A = 85°C$
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–5.0	–10	–2.0	–7.0	–1.0	–5.0	V	$V_{DS} = 20$ V, $I_D = 1$ nA
10		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	$V_{DS} = 20$ V, $V_{GS} = 0$
11		$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0$, $I_D = 6.6$ mA (U1897), $I_D = 4.0$ mA (U1898), $I_D = 2.5$ mA (U1899)
12		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1$ mA, $V_{GS} = 0$
13		C_{DG}	Drain-Gate Capacitance		5		5		5	pF	$V_{DG} = 20$ V, $I_S = 0$, f = 1 MHz
14		C_{SG}	Source-Gate Capacitance		5		5		5	pF	$V_{SG} = 20$ V, $I_D = 0$, f = 1 MHz
15	DYNAMIC	C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5	pF	$V_{DS} = 20$ V, $V_{GS} = 0$, f = 1 MHz
17		$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions
18		t_r	Rise Time		10		20		40	ns	
19		t_{off}	Turn OFF Time		40		60		80	ns	

Switching Time Test Conditions

	U1897	U1898	U1899
V_{DD}	3 V	3 V	3 V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	–12 V	–8 V	–6 V
R_L	430 Ω	700 Ω	1100 Ω
$I_{D(on)}$	6.6 mA	4 mA	2.5 mA

NOTE:
1. Pulse test pulsewidth = 300 μs; duty cycle ≤ 3%.

NCB

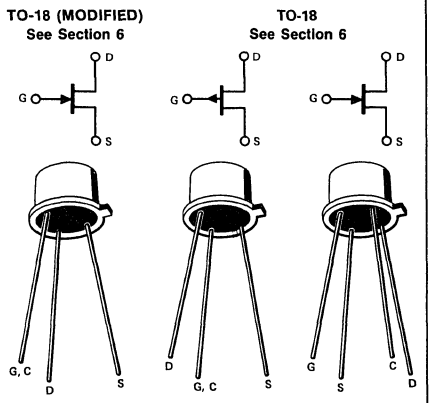
3

voltage-controlled resistor FETs *designed for . . .*

Siliconix

Performance Curves
NCB, NPA, NT, PSB
See Section 4

- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 15 V
Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

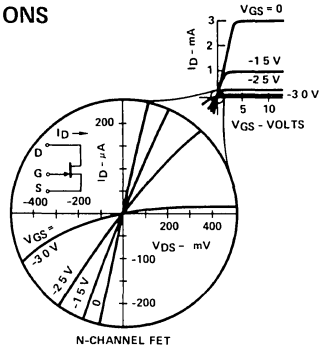
N-Channel VCR FETs

		Characteristic		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	1.0	3.5	-3.5	-7	-2.5	-5		I_D = 1 μA, V_{DS} = 10 V	
4		$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		7.5		3		1.5		V_{GS} = -10 V, I_D = 0	
				NCB		NPA		NT				

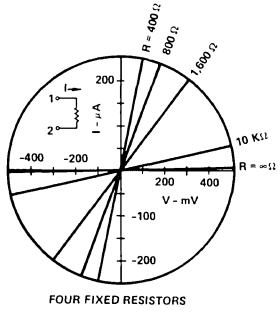
P-Channel VCR FETs

				VCR3P				
1	STATIC	I_{GSS}	Gate Reverse Current		20	nA	V_{GS} = 15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	15		V	I_G = 1 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	1.0	5		I_D = -1 μA, V_{DS} = -10 V	
4		$r_{ds(on)}$	Drain-Source ON Resistance	70	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		25	pF	V_{GD} = 10 V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		15		V_{GS} = 10 V, I_D = 0	
				PSA/PSB				

APPLICATIONS



N-Channel JFET Output Characteristic Enlarged Around V_{DS} = 0
Figure 1



V-I Characteristic of Four Fixed Resistors
Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around V_{DS} = 0, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when V_{GS} = 0 and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around V_{DS} = 0. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at I_D/I_{DSS} = 0.001. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at V_{DS} = V_{GS} = 0) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

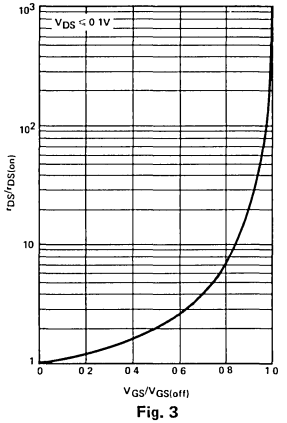


Fig. 3

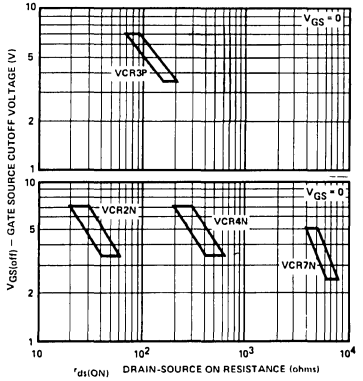


Fig. 4

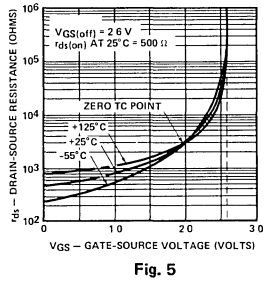


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

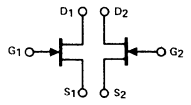
* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

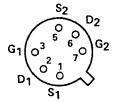
voltage-controlled resistor FETs *designed for . . .*

Siliconix

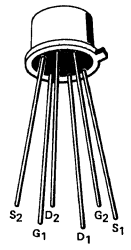
- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic		VCR11N Min	VCR11N Max	Unit	Test Conditions	
1	I_{GSS}	Gate Reverse Current		-0 2	nA	V_{GS} = -15 V, V_{DS} = 0	
2	BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
3	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-8	-12		I_D = 1 μA, V_{DS} = 10 V	
4	$r_{ds(on)}$	Drain Source ON Resistance	100	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	C_{dgo}	Drain-Gate Capacitance		8	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6	C_{sgo}	Source-Gate Capacitance		8		V_{GS} = -10 V, I_D = 0	
7	r_{DSmin}/r_{DSmax}		95	1		V_{DS} = 100 mV	r_{DS1} = 200Ω
			95	1		$V_{GS1} = V_{GS2}$	r_{DS1} = 2kΩ

Note
1 V_{GS1} + Control Voltage necessary to force r_{DS} to 200Ω or 2KΩ

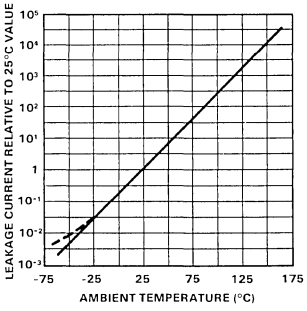
NSH*
*Contact factory for geometry information.

Geometry

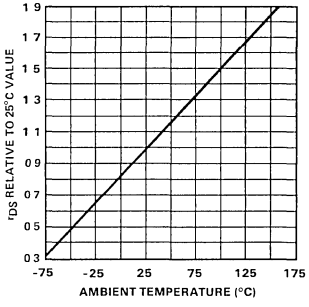
4

Useful JFET Parameter Relationships (Approximate)

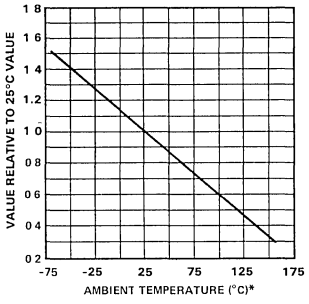
Bulk & Junction Leakage Current vs Ambient Temperature



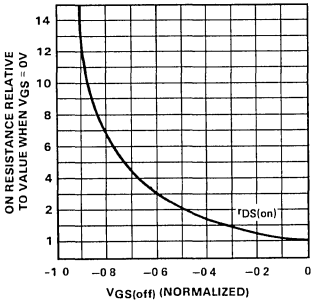
On Resistance vs Ambient Temperature

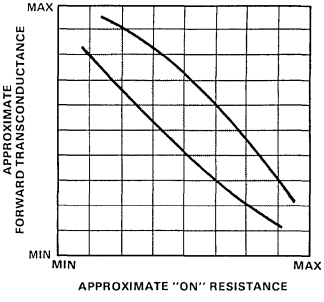


Drain Current and Transconductance vs Ambient Temperature

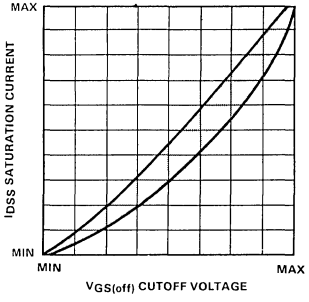


Typical $r_{DS(on)}$ vs Normalized Gate Source Cutoff Voltage

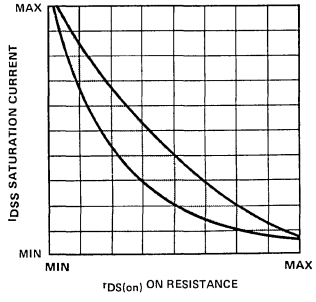




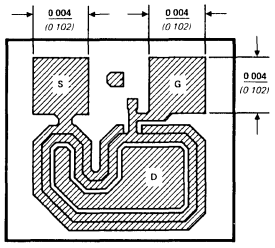
Saturation Current vs Cutoff Voltage



Saturation Current vs ON Resistance

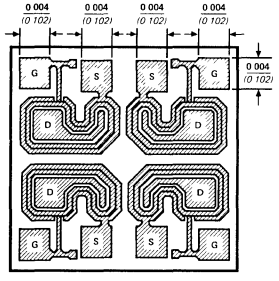


*When $I_D > 5 \times I_{D2}$



DIE SIZE = 19.0 X 19.0 MILS
BACKSIDE = SUBSTRATE

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



DIE SIZE = 35.0 X 35.0 MILS
BACKSIDE = SUBSTRATE

n-channel DMOS FET
designed for . . .

- **Ultra high speed switching**
- **High gain amplification**

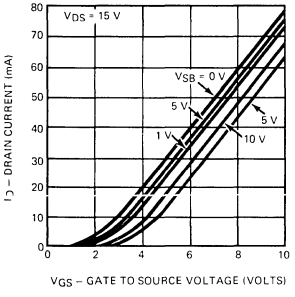
BENEFITS:

- **Switching speed < 1 ns**
- **Gain g_{fs} > 10,000 μmhos**

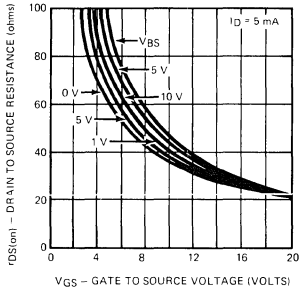
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	SD210DE, SD211DE SD212DE, SD213DE SD214DE, SD215DE
Quad	Dual in Line 16 Pin Side Braze	SD5000I, SD5001I SD5002I
	Dual in Line 16 Pin Plastic	SD5000N, SD5001N SD5002N
	Surface Mount SO-14	SD5400CY, SD5401CY SD5402CY
	Chip/Wafer	Available as above specifications

PERFORMANCE CURVES (25°C unless otherwise noted)

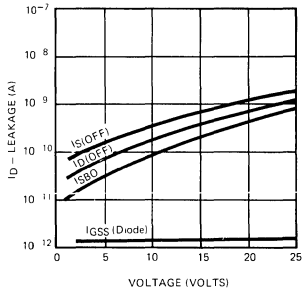
Drain Current
vs Drain to Source Voltage



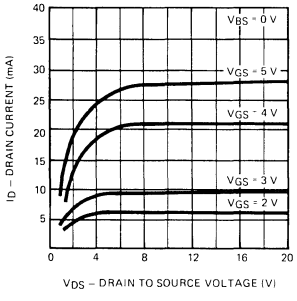
Drain to Source Resistance
vs Gate to Source Voltage



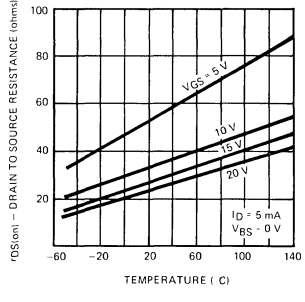
Leakage vs Voltage



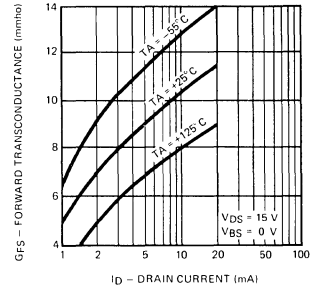
Drain Current
vs Gate to Source Voltage



Drain to Source Resistance
vs Temperature

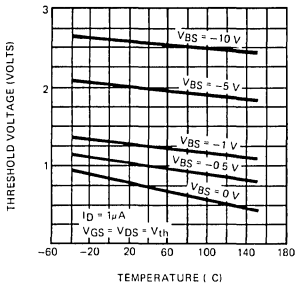


Forward Transconductance
vs Drain Current

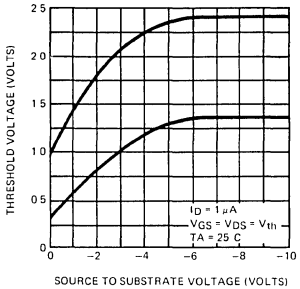


PERFORMANCE CURVES (Cont'd) (25° C unless otherwise noted)

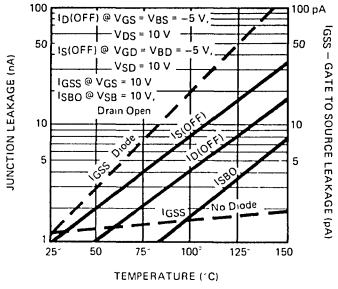
Threshold Voltage vs Temperature



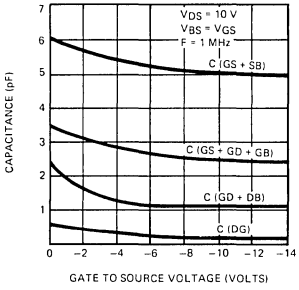
Threshold Voltage vs Source to Substrate Voltage



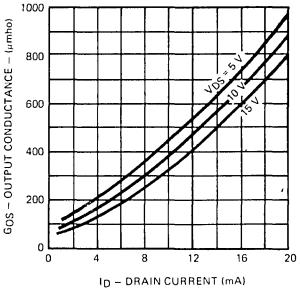
Leakage vs Temperature

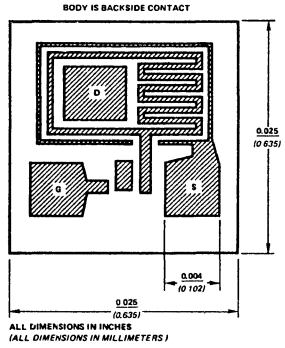


Capacitance vs Gate to Source Voltage



Common-Source Output Conductance vs Drain Current





enhancement-type n-channel MOSFET

designed for . . .

- Audio Amplifiers
- Analog Circuits
- Digital Switching Circuits
- Commutating Circuits

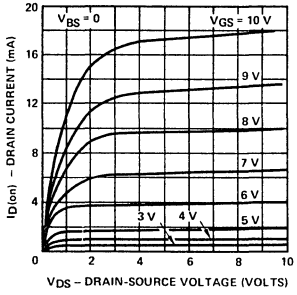
BENEFITS:

- Integrated Zener Clamp Protects the Gate
- Normally OFF

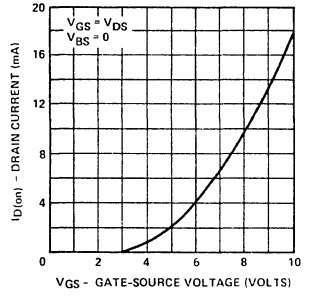
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	M116
Single	Chip	M116CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

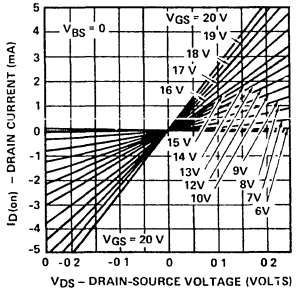
Output Characteristics



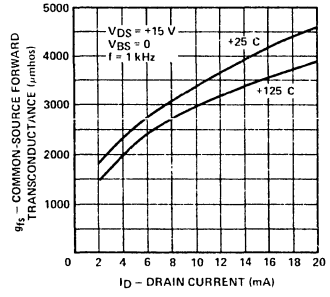
Transfer Characteristic



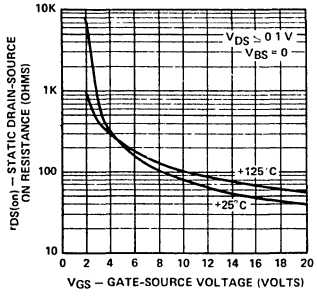
Low Voltage Output Characteristics



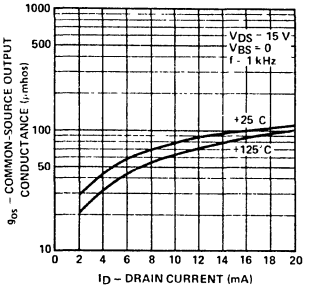
Forward Transconductance vs Drain Current



Drain-Source ON State Resistance vs Gate-Source Bias

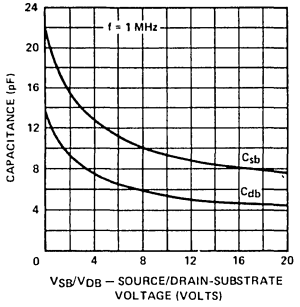


Output Conductance vs Drain Current

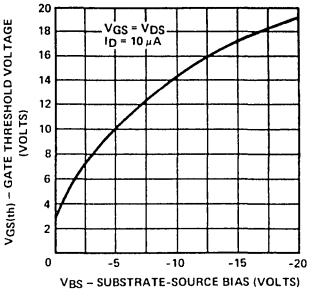


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

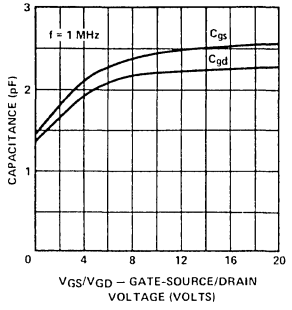
Substrate Capacitance vs Voltage



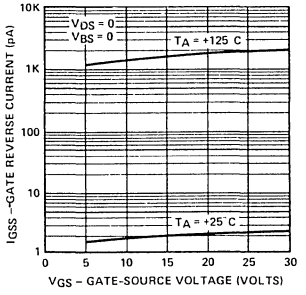
Gate Threshold Voltage vs Substrate Bias



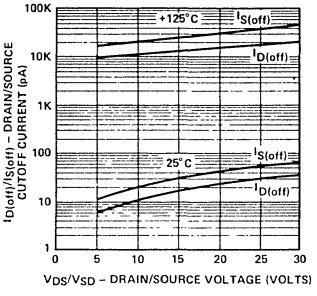
Gate Capacitance vs Voltage

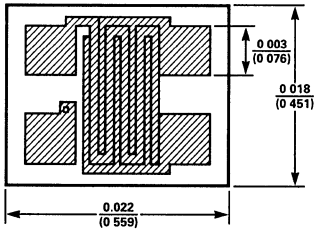


Gate Leakage Current vs Gate-Source Bias



Source-Drain Leakage Currents vs Voltage





all dimensions in inches
(all dimensions in millimeters)

enhancement-type p-channel MOSFET *designed for . . .*

Siliconix

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

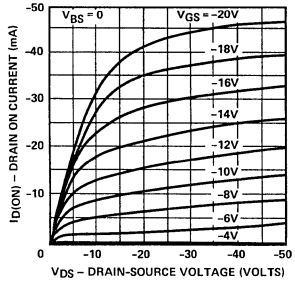
BENEFITS:

- **High Gate Transient Voltage Breakdown Eliminates Need for Gate Protective Diode**
- **Ultra-High Input Impedance**
- **Low Leakage**
- **Normally OFF**

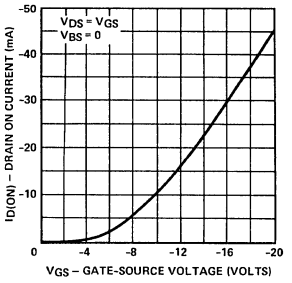
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	MFE823
Single	TO-72	3N163-64
Single	Chip	3N163-64CHP, MFE823CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

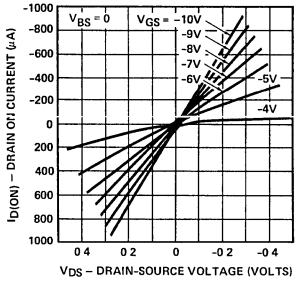
Output Characteristics



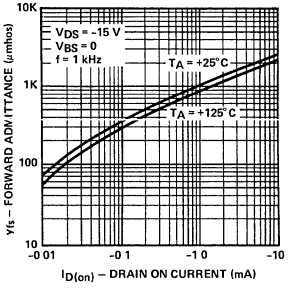
Transfer Characteristic



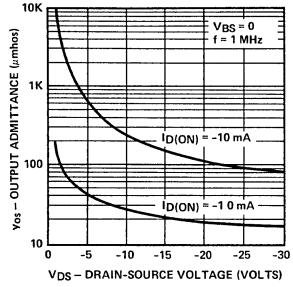
Low-Level Output Characteristics



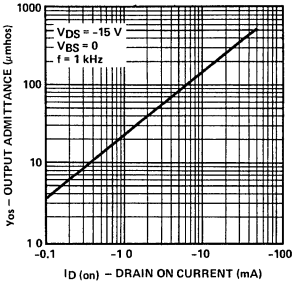
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

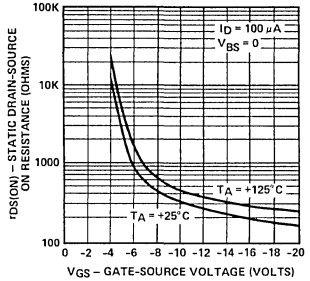


Common-Source, Short-Circuit, Output Admittance vs Drain Current

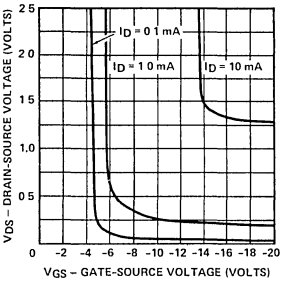


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

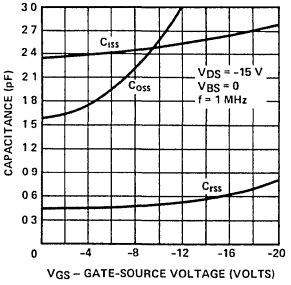
Drain-Source ON Resistance vs Gate-Source Voltage



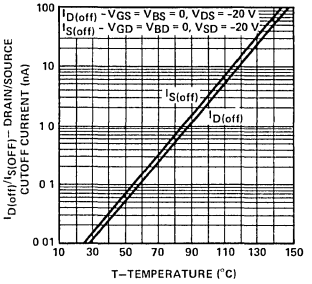
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage

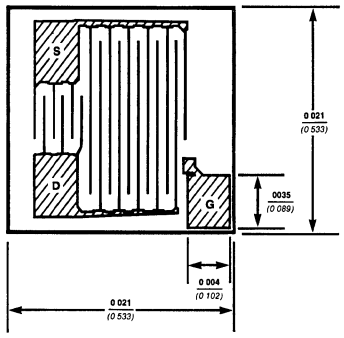


Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFETs
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

Siliconix

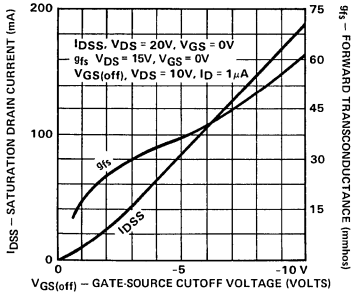
BENEFITS:

- **No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance From Driver**
- **High Off-Isolation $I_{D(off)}$ < 100 pA**
- **High Speed t_{ON} < 20 ns**

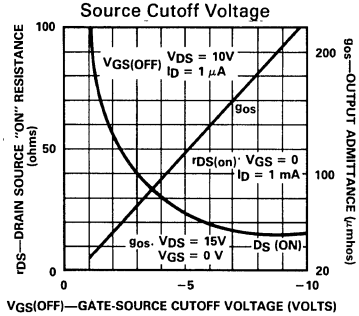
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3970-72, 2N4091-93, 2N4391-93 2N4856-61, 2N4856A-61A, FN4392,93 U200-01, VCR2N
Single	TO-92	2N5638-40, 2N5653-54, J111-13 PN4091,93 PN4391-93 U1897-99
Dual	TO-71	2N5564-66, DN5564-66, DN5567
Single	Chip	All of above single devices available in chip form
Dual	Chip	2N5566 Chip Set, DN5566 Chip Set

PERFORMANCE CURVES (25°C unless otherwise noted)

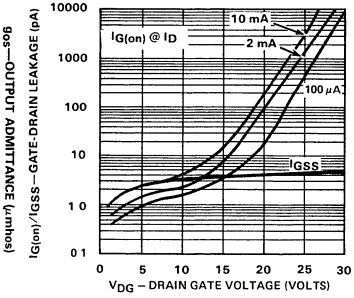
Drain Current & Transconductance vs Gate Source Voltage



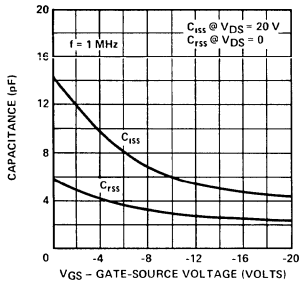
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



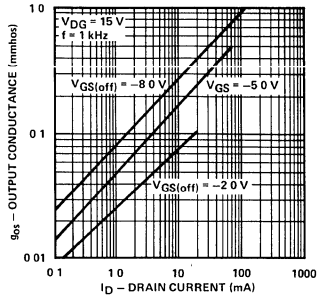
Gate Operating Current vs Drain Gate Voltage



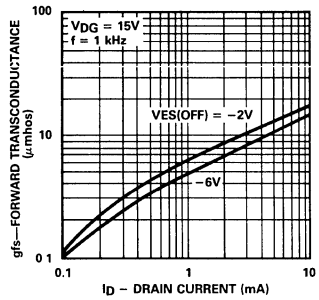
Common-Source Capacitances vs Gate-Source Voltage



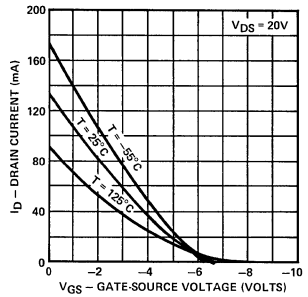
Common-Source Output Conductance vs Drain Current



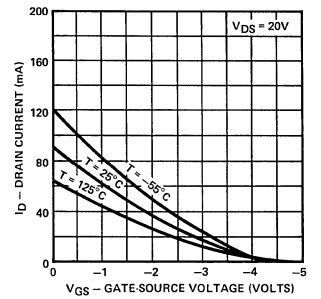
Transconductance vs Drain Current



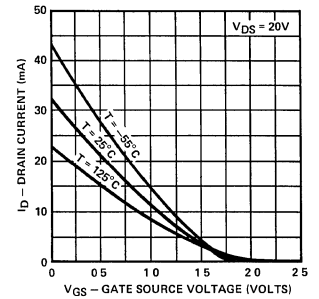
Transfer Characteristics



Transfer Characteristics

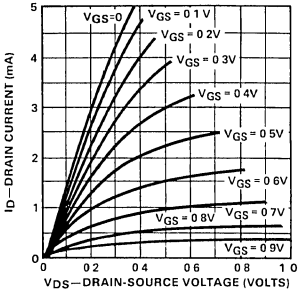


Transfer Characteristics

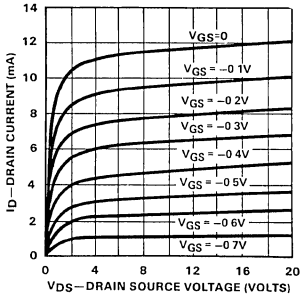


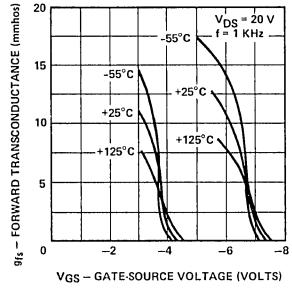
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

Output Characteristic
($V_{GS(off)}$ = −1.5V)

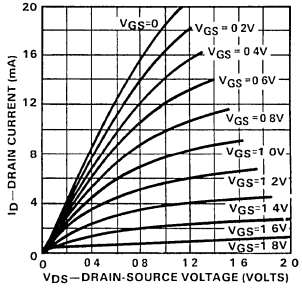


Output Characteristic
($V_{GS(off)}$ = −1.5V)

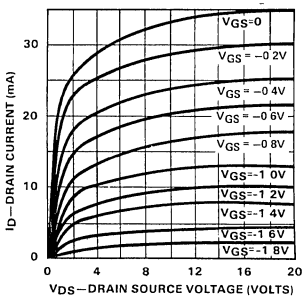




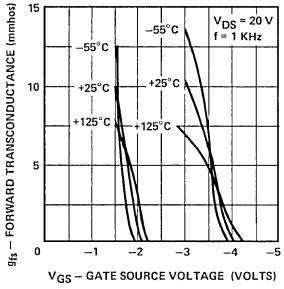
Output Characteristic
($V_{GS(off)}$ = −3.0V)



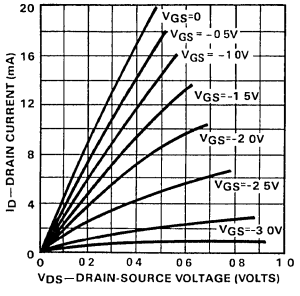
Output Characteristic
($V_{GS(off)}$ = −3.0V)



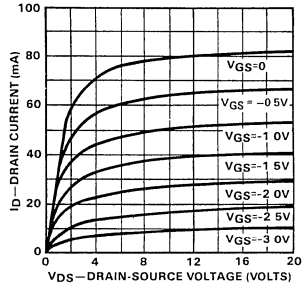
Transconductance Characteristics



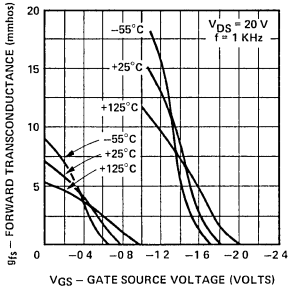
Output Characteristic
($V_{GS(off)}$ = −5.0V)



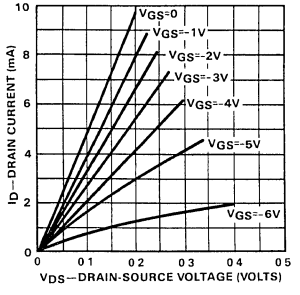
Output Characteristic
($V_{GS(off)}$ = −5.0V)



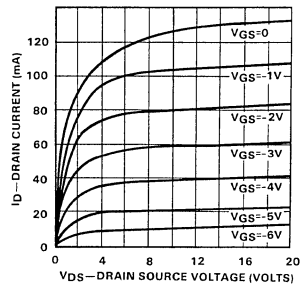
Transconductance Characteristics



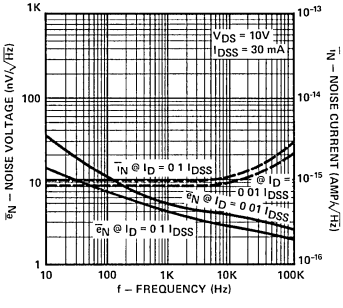
Output Characteristic
($V_{GS(off)}$ = −8.0V)



Output Characteristic
($V_{GS(off)}$ = −8.0V)

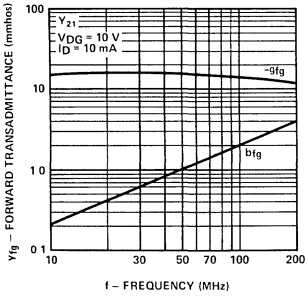


Equivalent Input Noise Voltage and Noise Current vs Frequency

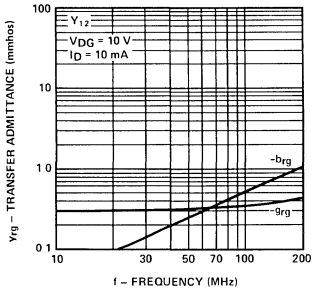


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

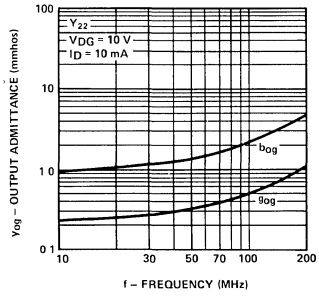
Common-Gate Forward Transadmittance vs Frequency



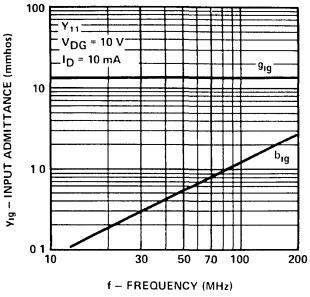
Common-Gate Reverse Transfer Admittance vs Frequency



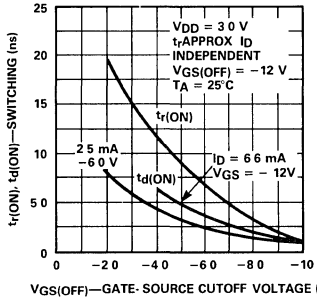
Common-Gate Output Admittance vs Frequency



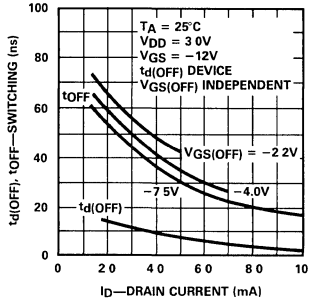
Common-Gate Input Admittance vs Frequency

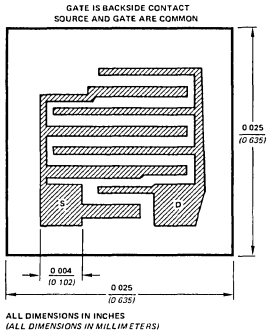


Turn-On Switching



Turn-Off Switching





n-channel JFET current regulator diode *designed for . . .*

Siliconix

- Current Regulation
- Current Limiting
- Biasing

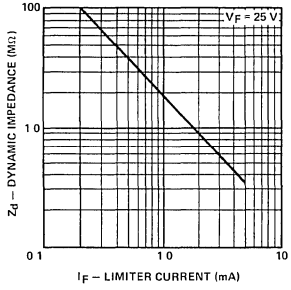
BENEFITS:

- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Low Cost

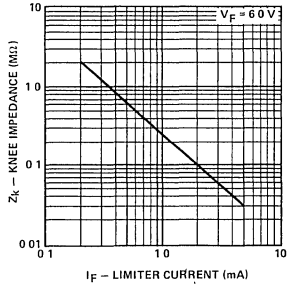
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-92	J500-505, J506-511, J553-7
Single	Chip	J500CHP-505CHP, J506CHP-511 CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

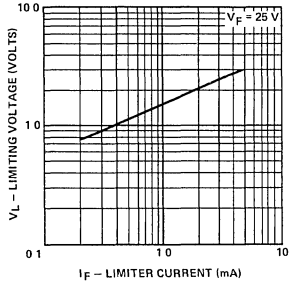
Dynamic Impedance vs Limiter Current



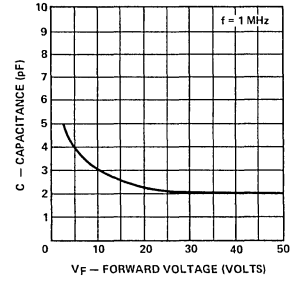
Knee Impedance vs Limiter Current



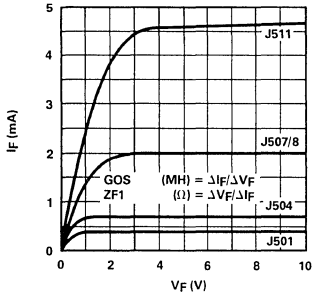
Limiting Voltage at 0.9 I_D vs Limiter Current



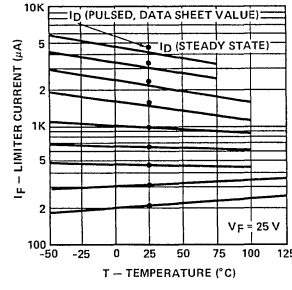
Capacitance vs Forward Voltage

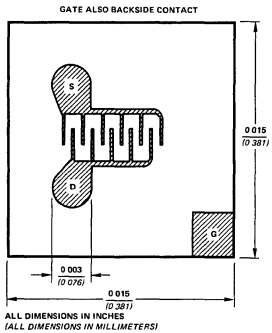


Family Curves



Typical Variation of I_D with Temperature Steady State and Pulsed Value





n-channel JFET
designed for . . .

Siliconix

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

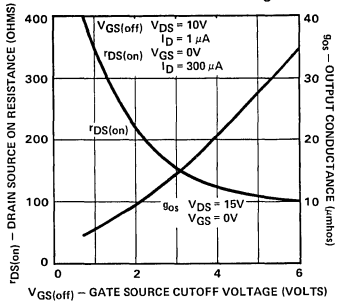
BENEFITS:

- Low Noise
  NF = 3 dB Typical @ 400 MHz
- Wideband
  High g_{fs}/C_{iss} Ratio

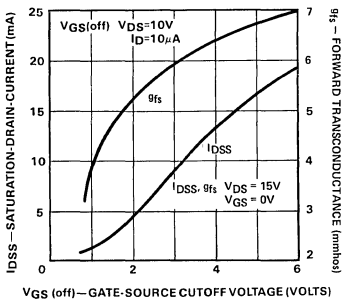
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3966, 2N4416-16A, 2N3819, 2N4223-4, 2N5484-6,
Single	TO-92	2N5555, 2N5668-70, MPF102, MPF108, MPF112, PN4416, J304-5, MPF109, MPF111
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

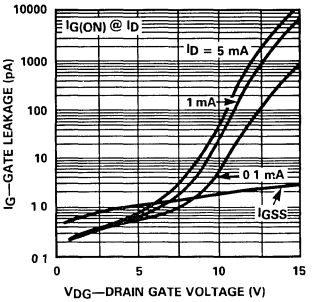
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



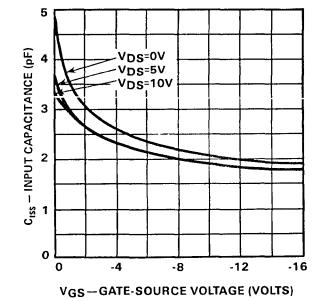
Drain Current & Transconductance vs Gate Source Cutoff Voltage



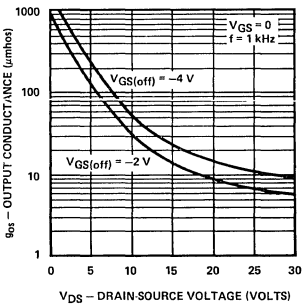
Gate Operating Current vs Drain-Gate Voltage



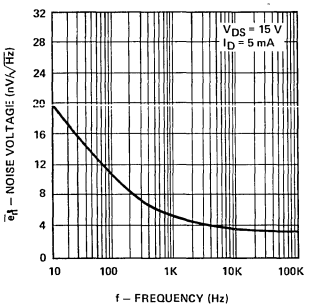
Common Source Input Capacitance vs Gate-Source Voltage



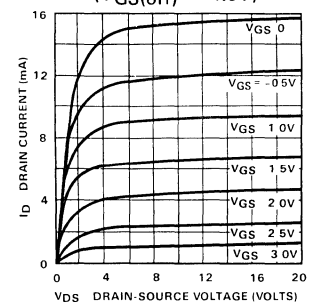
Common-Source Output Conductance vs Drain-Source Voltage



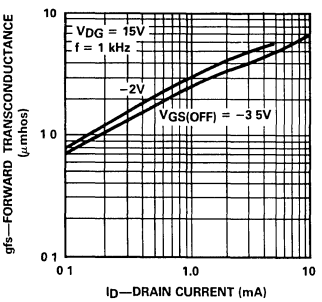
Equivalent Input Noise Voltage vs Frequency



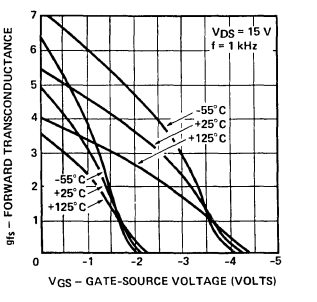
Output Characteristic ($V_{GS(off)}$ = –4.0V)



Transconductance vs Drain Current

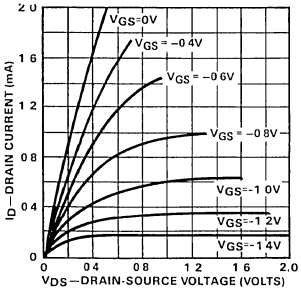


Transconductance Characteristics

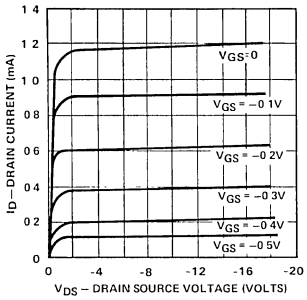


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

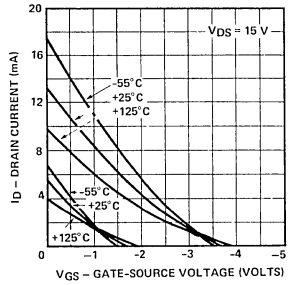
Output Characteristic
($V_{GS(off)}$ = −2V)



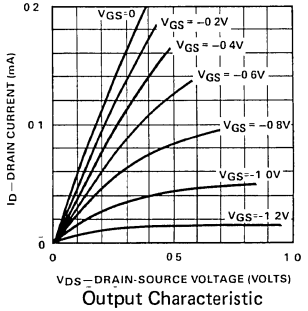
Output Characteristic
($V_{GS(off)}$ = −1.0V)



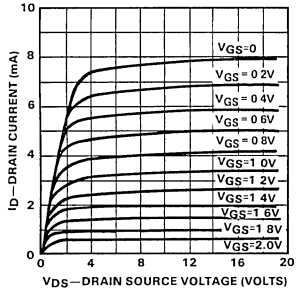
Transfer Characteristics



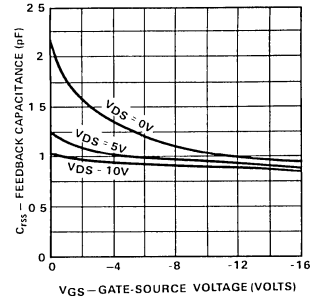
Output Characteristic
($V_{GS(off)}$ = −1.5V)



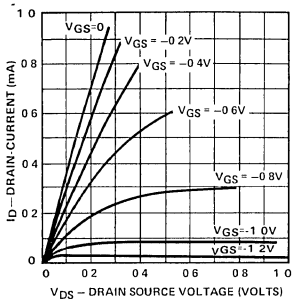
Output Characteristic
($V_{GS(off)}$ = −3.0V)



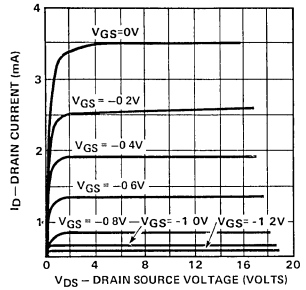
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



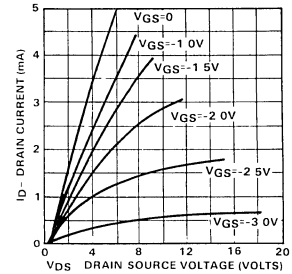
Output Characteristic
($V_{GS(off)}$ = −1.5V)



Output Characteristic
($V_{GS(off)}$ = −1.5V)

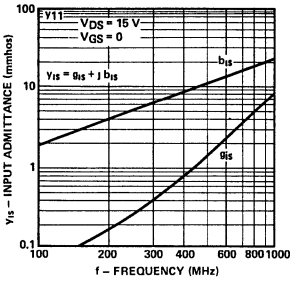


Output Characteristic
($V_{GS(off)}$ = −4.0V)

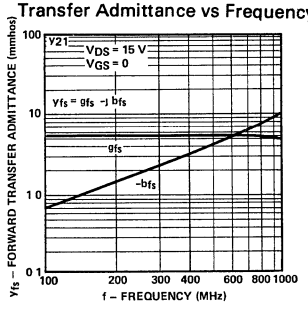


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

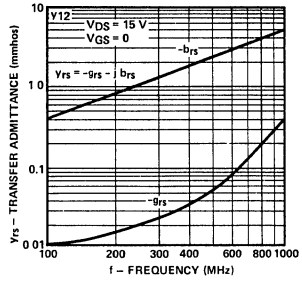
Common-Source Input Admittance vs Frequency



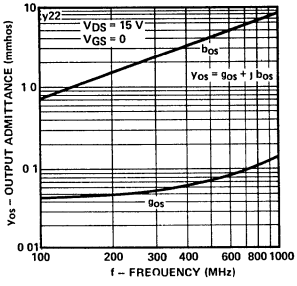
Common-Source Forward Transfer Admittance vs Frequency



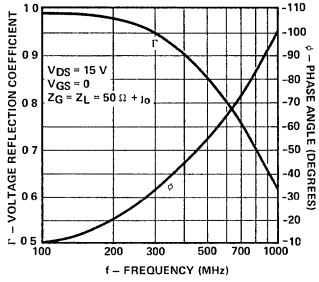
Common-Source Reverse Transfer Admittance vs Frequency



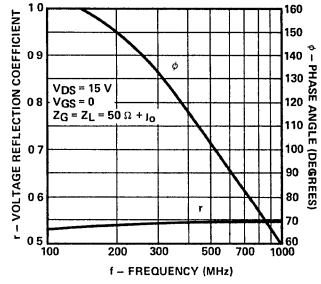
Common-Source Output Admittance vs Frequency



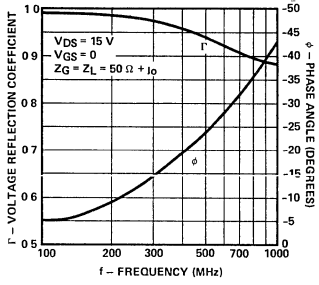
S Parameters S_{11} Common-Source vs Frequency

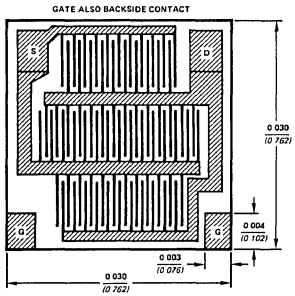


S Parameters S_{21} Common-Source vs Frequency



S Parameters S_{22} Common-Source vs Frequency





n-channel JFET

designed for . . .

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

Siliconix

BENEFITS:

- Low Insertion Loss
- Small Error in Measurement Systems
  $V_{DS(on)}$ < 50 mV (2N5432)
- High Off-Isolation $I_{D(off)}$ < 200 pA
- High Speed $t_{d(on)}$ < 4 ns
- Low Noise Audio-Freq Amplification
  $\overline{e_N}$ < 2 nV/$\sqrt{Hz}$ at 1 kHz

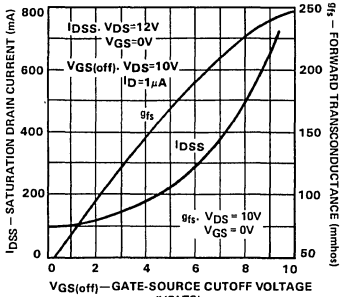
TYPE	PACKAGE
Single	TO-52
Single	TO-92
Single	Chip

PRINCIPAL DEVICES

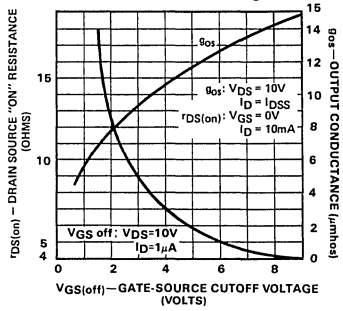
2N5432-34
J108-10
All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

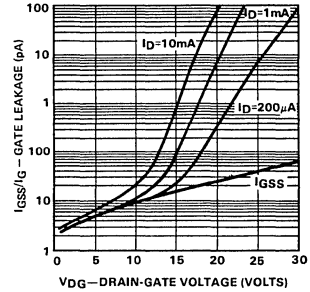
Drain Current & Forward Transconductance vs Gate Source Cutoff Voltage



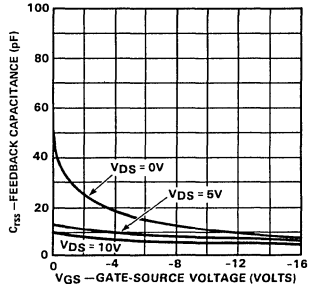
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



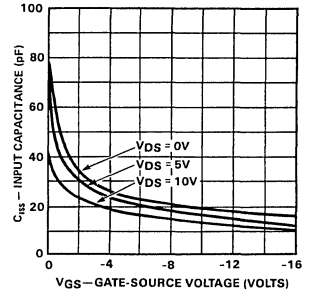
Gate Operating Current vs Drain-Gate Voltage



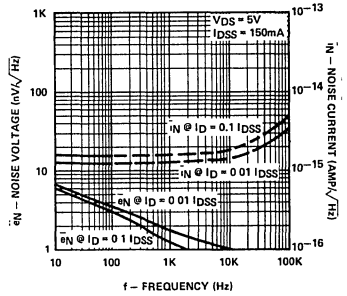
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



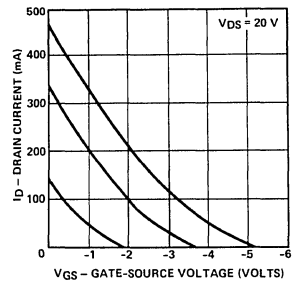
Common Source Input Capacitance vs Gate-Source Voltage



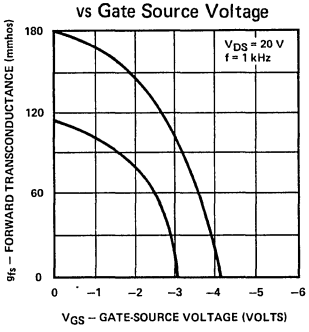
Equivalent Input Noise Voltage and Noise Current vs Frequency



Transfer Characteristics



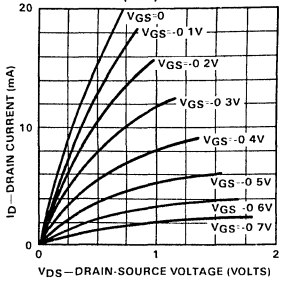
Forward Transconductance vs Gate Source Voltage



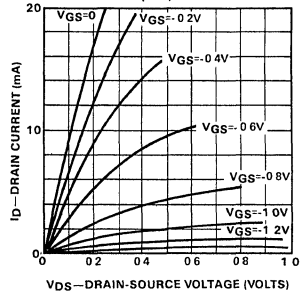
4

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

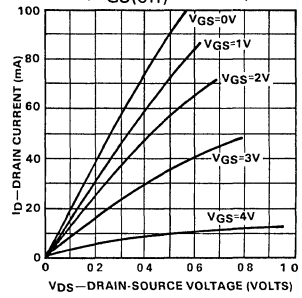
Output Characteristic
($V_{GS(off)}$ = −1.5V)



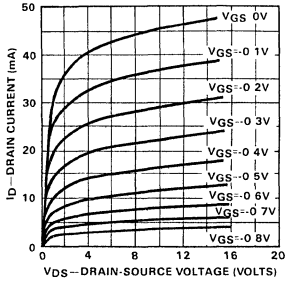
Output Characteristic
($V_{GS(off)}$ = −2.0V)



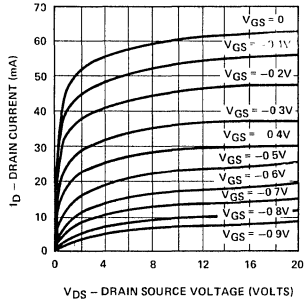
Output Characteristic
($V_{GS(off)}$ = −6.5V)



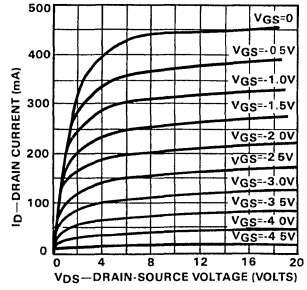
Output Characteristic
($V_{GS(off)}$ = −1.5V)



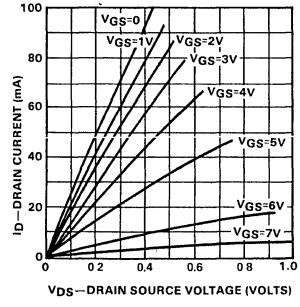
Output Characteristic
($V_{GS(off)}$ = −2V)



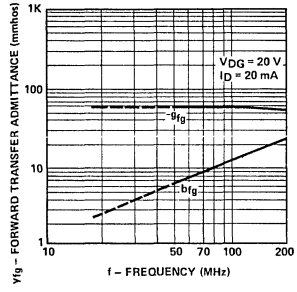
Output Characteristic
($V_{GS(off)}$ = −6.5V)



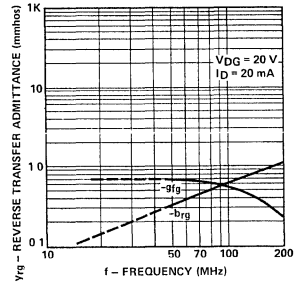
Output Characteristic
($V_{GS(off)}$ = −9.0V)



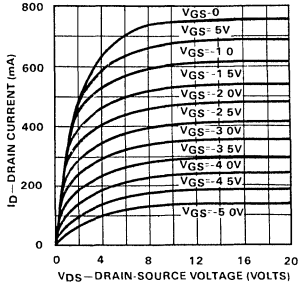
Forward Transfer Admittance Common Gate vs Frequency



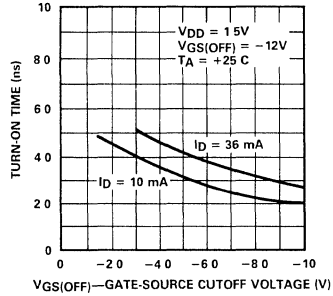
Reverse Transfer Admittance Common Gate vs Frequency



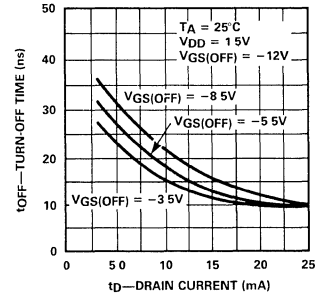
Output Characteristic
($V_{GS(off)}$ = −9.0V)

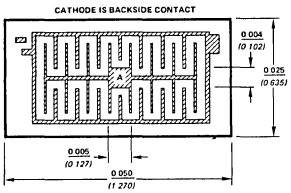


Switching Turn-On vs Gate-Source Voltage



Switching Turn-On Time vs Drain Current





n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

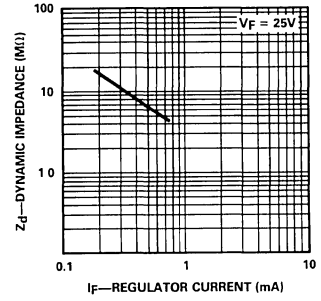
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

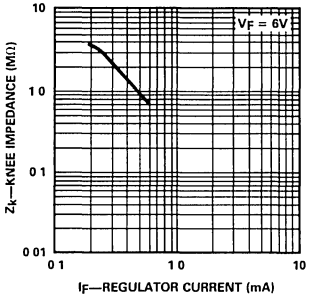
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR022 Thru CR062 CRR0240 Thru CRR0560
Single	Chip	All of above

PERFORMANCE CURVES (25°C unless otherwise noted)

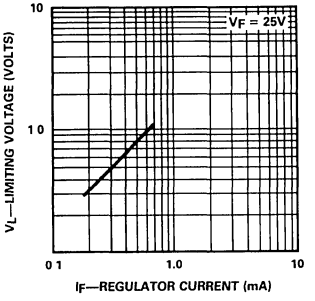
Dynamic Impedance vs Regulator Current



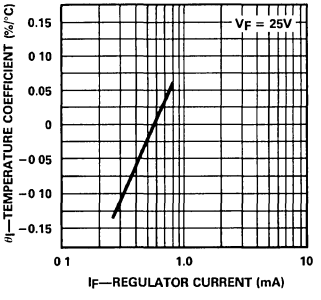
Knee Impedance vs Regulator Current



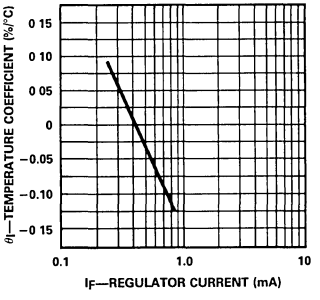
Limiting Voltage @ 0.8 I_F vs Regulator Current



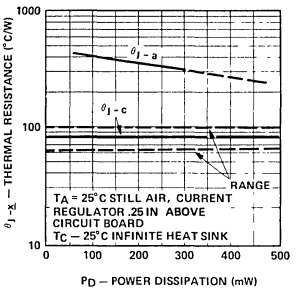
Temperature Coefficient $-55°C \leq T_j \leq 25°C$ vs Regulator Current



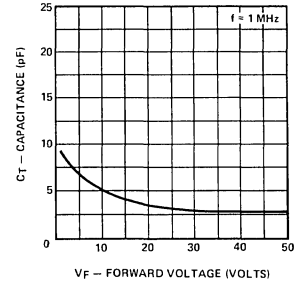
Temperature Coefficient $25°C \leq T_j \leq 125°C$ vs Regulator Current



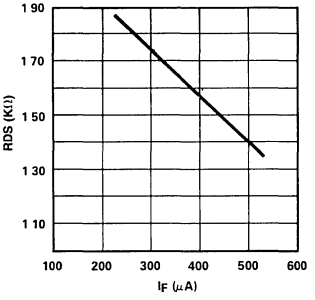
Thermal Resistance vs Power Dissipation



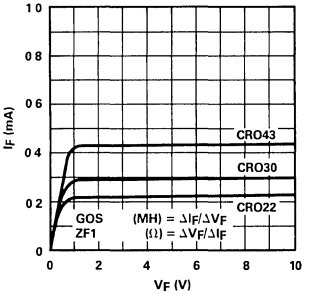
Capacitance vs Forward Voltage



RDS vs I_F Geometry: NKL

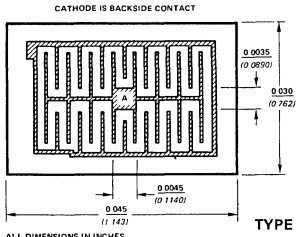


Family Curves



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}PD$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-a}}$ or $\frac{1}{\theta_{j-c}}$ is the derating factor for all devices.



n-channel JFET current regulator diode

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- Low Voltage References

Siliconix

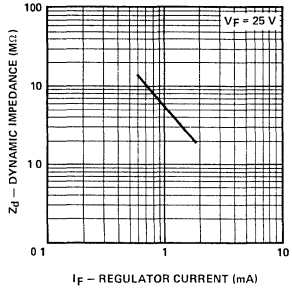
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

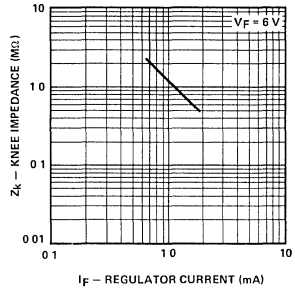
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR068 Thru CR150 CRR0800 Thru CRR1250
Single	Chip	All of above

PERFORMANCE CURVES (25°C unless otherwise noted)

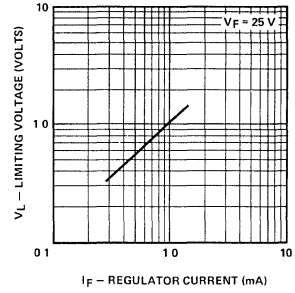
Dynamic Impedance vs Regulator Current



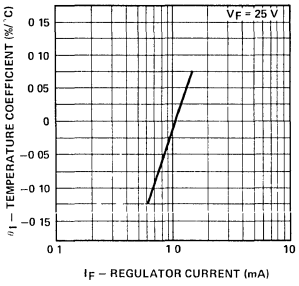
Knee Impedance vs Regulator Current



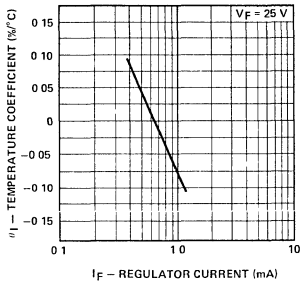
Limiting Voltage @ 0.8 I_F vs Regulator Current



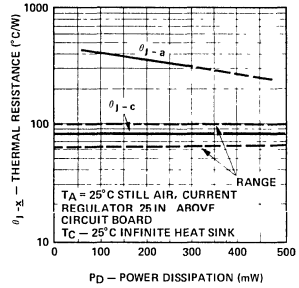
Temperature Coefficient $-55°C \leqslant T_j \leqslant 25°C$ vs Regulator Current



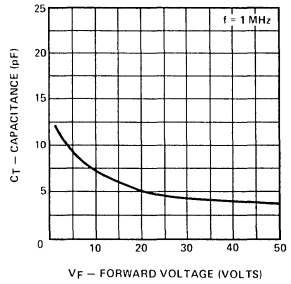
Temperature Coefficient $25°C \leqslant T_j \leqslant 125°C$ vs Regulator Current



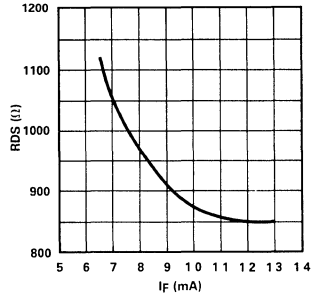
Thermal Resistance vs Power Dissipation



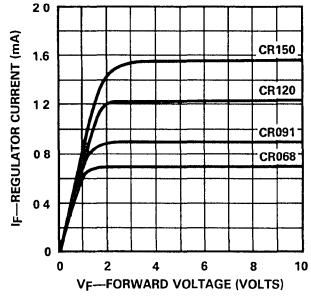
Capacitance vs Forward Voltage



RDS vs I_F

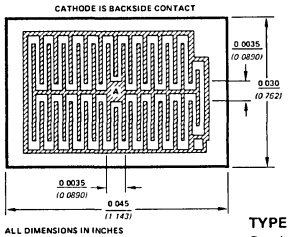


Family Output Characteristics



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_J = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}PD$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-a}}$ or $\frac{1}{\theta_{j-c}}$ is the derating factor for all devices.



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

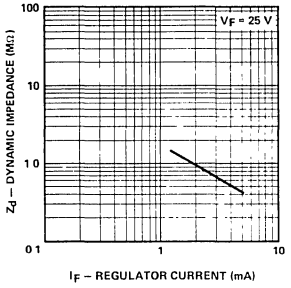
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

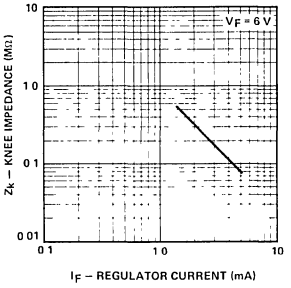
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR160 Thru CR530 CRR1950 Thru CRR4300 All of above
Single	Chip	

PERFORMANCE CURVES (25°C unless otherwise noted)

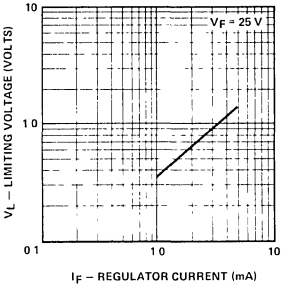
Dynamic Impedance vs Regulator Current



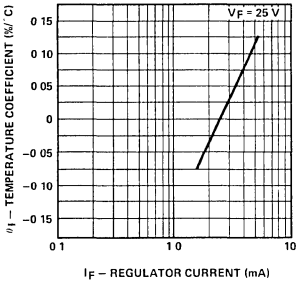
Knee Impedance vs Regulator Current



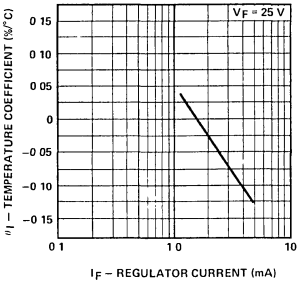
Limiting Voltage @ 0.8 I_F vs Regulator Current



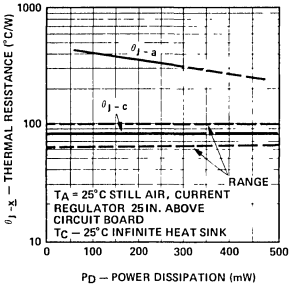
Temperature Coefficient -55°C ≤ T_j ≤ 25°C vs Regulator Current



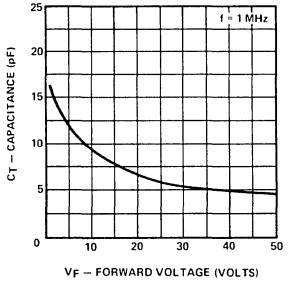
Temperature Coefficient 25°C ≤ T_j ≤ 125°C vs Regulator Current



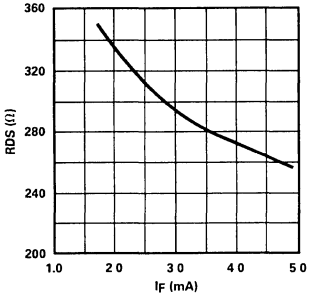
Thermal Resistance vs Power Dissipation



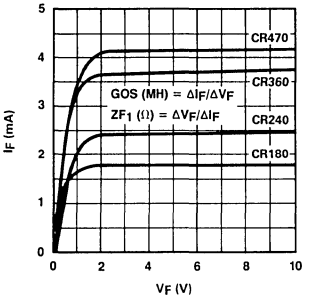
Capacitance vs Forward Voltage



RDS vs I_F

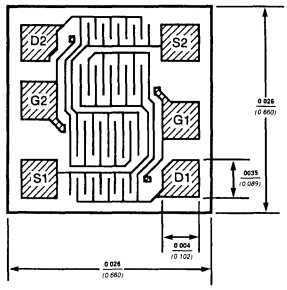


Family Curves



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}PD$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-a}}$ or $\frac{1}{\theta_{j-c}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET

designed for . . .

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Compartors

Siliconix

BENEFITS

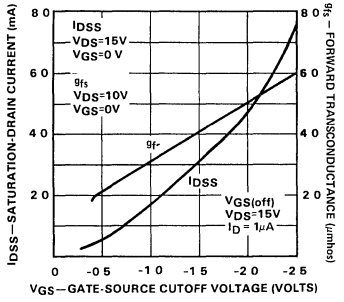
- **Minimum System Error and Calibration**
  5 mV Offset Maximum (J401)
  95 dB Minimum CMRR
- **Low Drift With Temperature**
  10 μV/°C (J401)
- **Simplifies Amplifier Design**
  Output Conductance < 2 μmho
- **Low Noise**
  $\overline{e_n}$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

TYPE	PACKAGE
Dual	TO-71
Dual	Chip

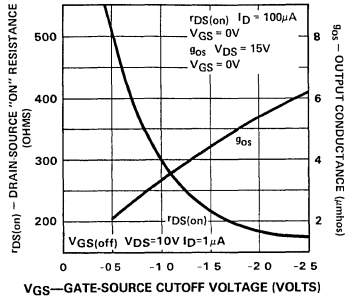
PRINCIPAL DEVICES

2N3921-2, 2N4084-5, 2N5045-7,
2N6905-7, U401-6, 2N5046CHP-47CHP,
U403CHP-06CHP, 2N4085CHP, 2N6905-7CHP

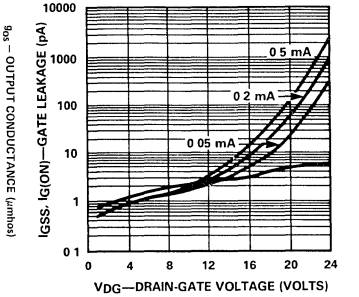
Drain Current & Transconductance vs Gate Source Voltage



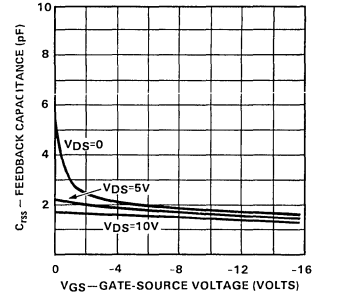
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



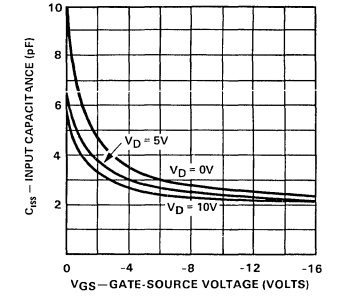
Gate Operating Current vs Drain Gate Voltage



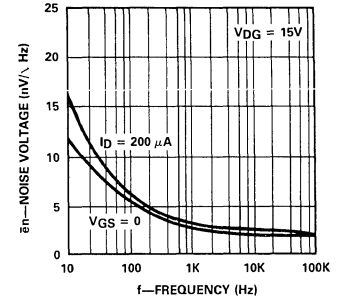
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



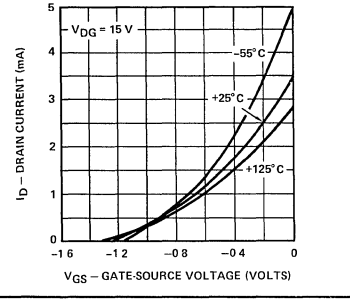
Common-Source Input Capacitance vs Gate-Source Voltage



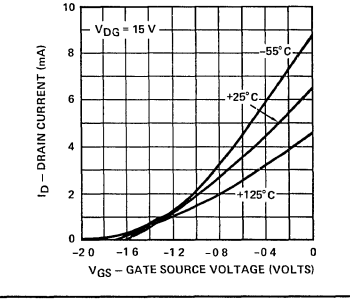
Equivalent Input Noise Voltage vs Frequency



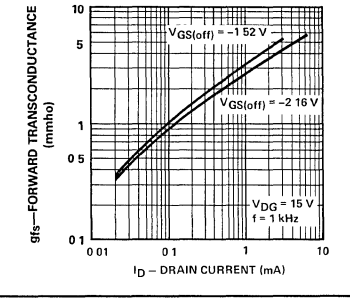
Transfer Characteristics Low $V_{GS(off)}$ Unit (−1.5 V)



Transfer Characteristics Medium $V_{GS(off)}$ Unit (−2.2 V)

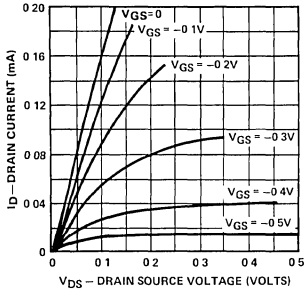


Forward Transconductance vs Drain Current

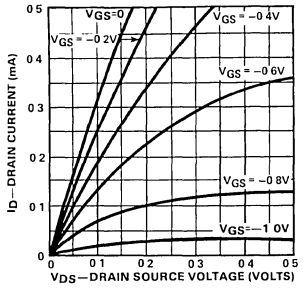


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

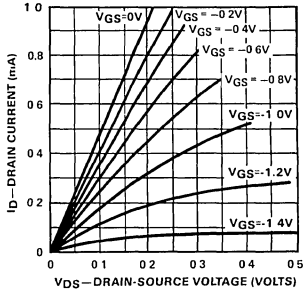
Output Characteristic
($V_{GS(off)}$ = −0.6V)



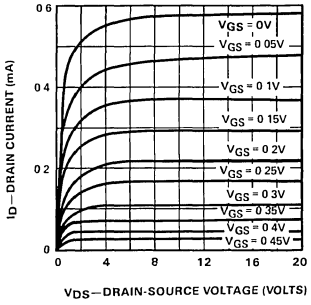
Output Characteristic
($V_{GS(off)}$ = −1.2V)



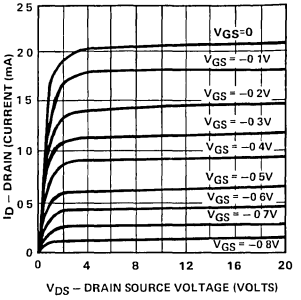
Output Characteristic
($V_{GS(off)}$ = −1.7V)



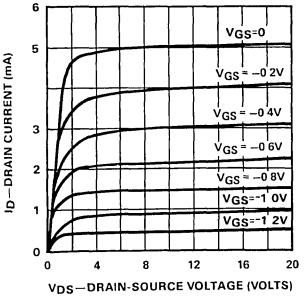
Output Characteristic
($V_{GS(off)}$ = −0.6V)



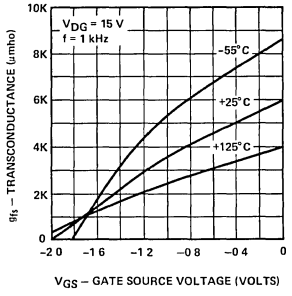
Output Characteristic
($V_{GS(off)}$ = −1.2V)



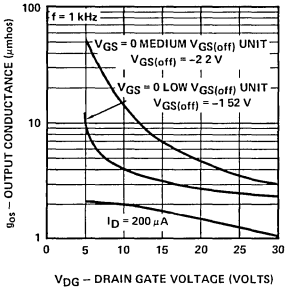
Output Characteristic
($V_{GS(off)}$ = −1.7V)



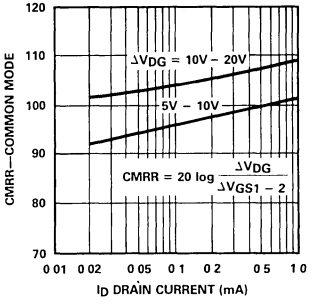
Transconductance vs Gate Source Voltage
Medium $V_{GS(off)}$ Unit (−2.0V)

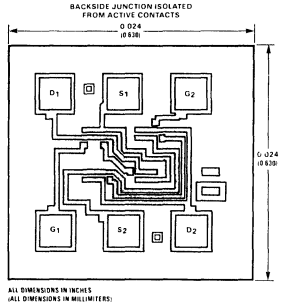


Output Conductance
vs Drain Gate Voltage



CMRR vs Drain Current





monolithic dual n-channel JFETs

designed for . . .

- Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

BENEFITS:

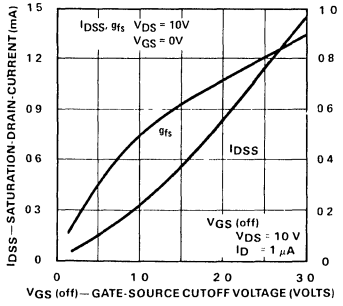
- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-78	U421-28
Dual	Chip	U423CHP-428CHP

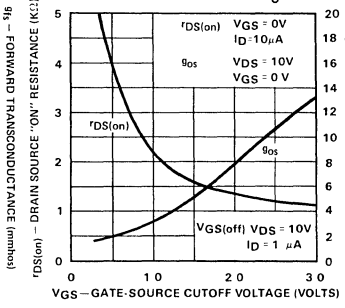
Improved Replacement for 2N5902-9 Series

PERFORMANCE CURVES (25° C unless otherwise noted)

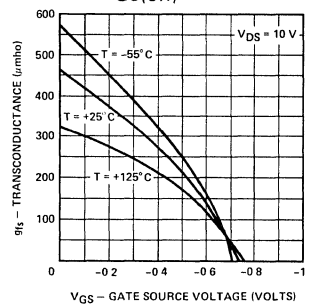
Drain Current & Transconductance vs Gate Source Cutoff Voltage



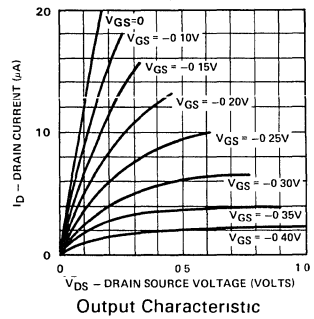
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



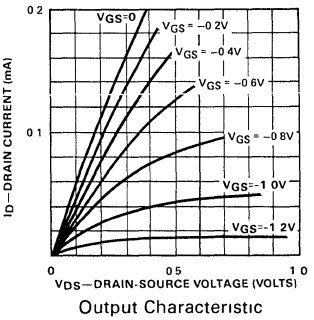
Transconductance vs Gate Source Voltage Low $V_{GS(off)}$ Unit (1.0 V)



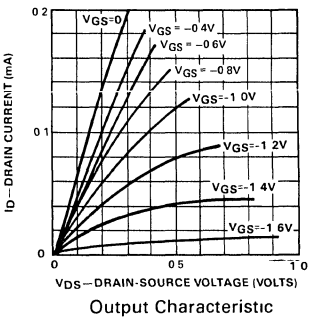
Output Characteristic ($V_{GS(off)}$ = -0.5V)



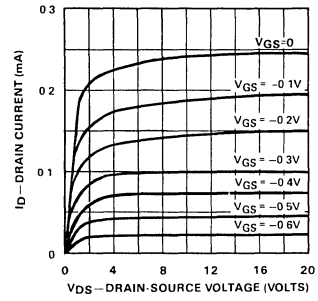
Output Characteristic ($V_{GS(off)}$ = -1.5V)



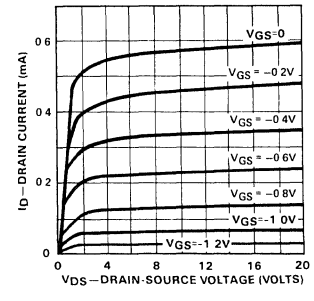
Output Characteristic ($V_{GS(off)}$ = -2.0V)



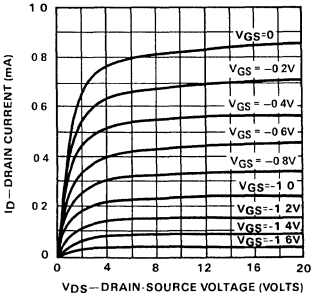
Output Characteristic ($V_{GS(off)}$ = -0.5V)



Output Characteristic ($V_{GS(off)}$ = -1 5V)

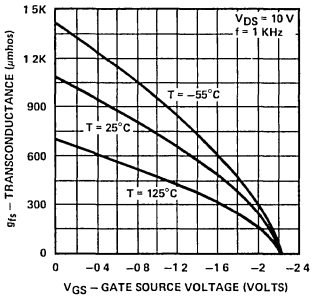


Output Characteristic ($V_{GS(off)}$ = -2 0V)

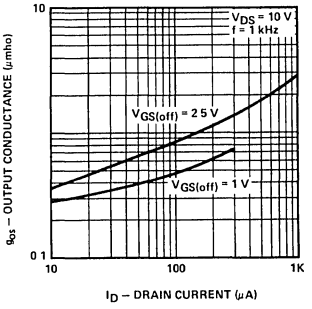


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

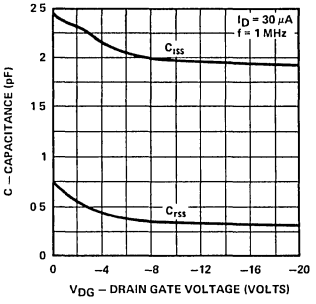
Transconductance vs Gate Source Voltage
High $V_{GS(off)}$ Unit (2.5 V)



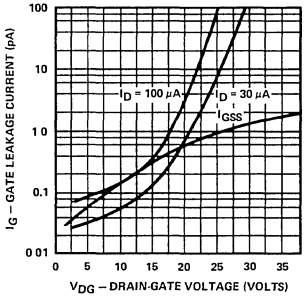
Common-Source Output Conductance vs Drain Current



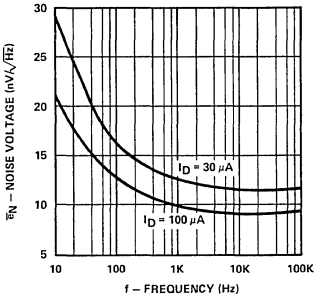
Capacitance vs Drain Gate Voltage



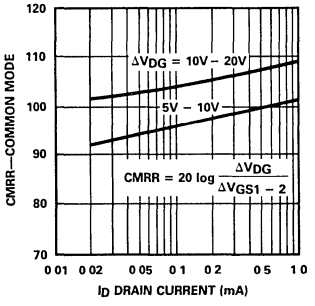
Gate Operating Current vs Drain-Gate Voltage

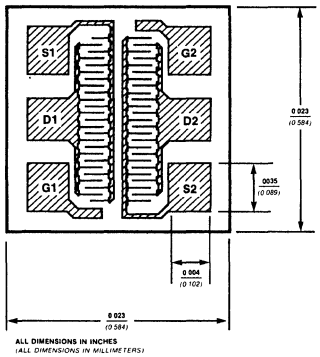


Equivalent Input Noise Voltage vs Frequency



CMRR vs Drain Current





n-channel JFET
designed for . . .

Siliconix

- High Frequency Amplifiers
- Mixers
- Oscillators

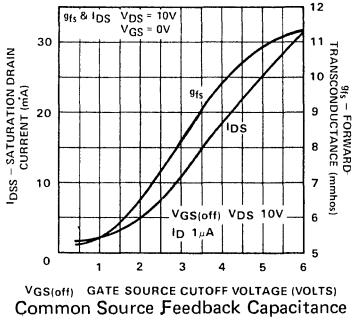
BENEFITS:

- High Power Gain
- Low Input Capacitance

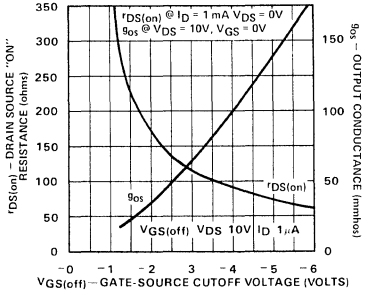
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-78	2N5911-12, U257 U443-U444
Dual	TO-71	U440-41
Dual	Chip	M5911CHP, M5912CHP, M440CHP, M441CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

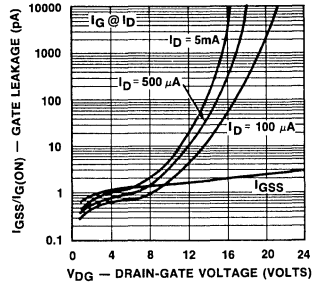
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



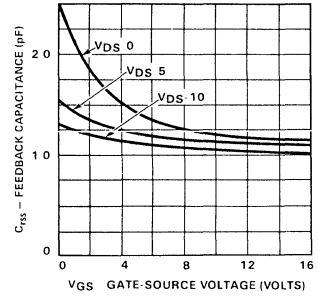
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



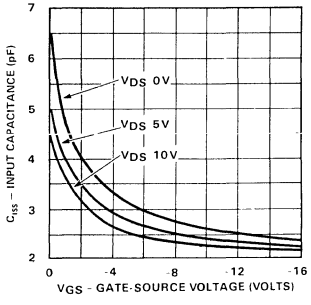
Gate Operating Current vs Drain-Gate Voltage



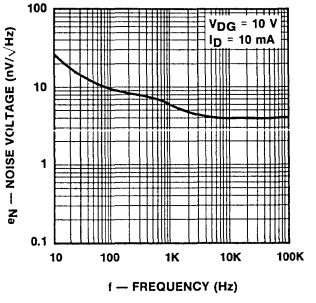
Common Source Feedback Capacitance vs Gate-Source Voltage



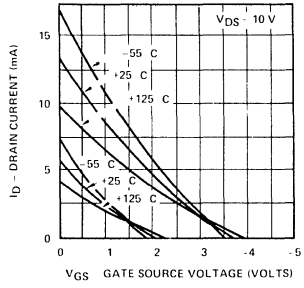
Common Source Input Capacitance vs Gate-Source Voltage



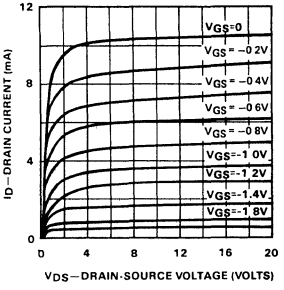
Equivalent Input Noise Voltage vs Frequency



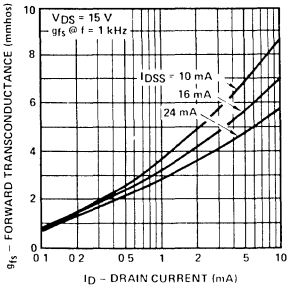
Transfer Characteristics

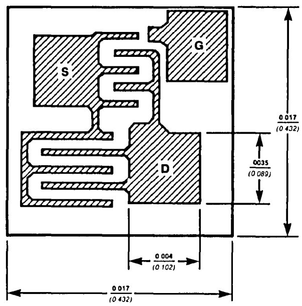


Output Characteristic ($V_{GS(off)} = -2.8V$)



Forward Transconductance vs Drain Current





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

BENEFITS:

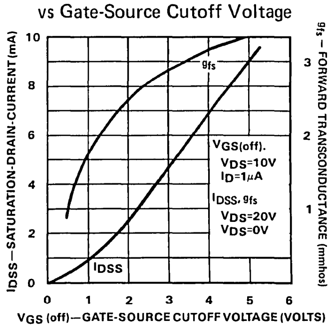
- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages, $V_{GS(off)}$ < 1 V (2N4338)
- High Off-Isolation As a Switch $I_{D(off)}$ < 50 pA
- High Input Impedance

TYPE	PACKAGE
Single	TO-18
Single	TO-72
Single	TO-92
Dual	Chip
Single	Chip

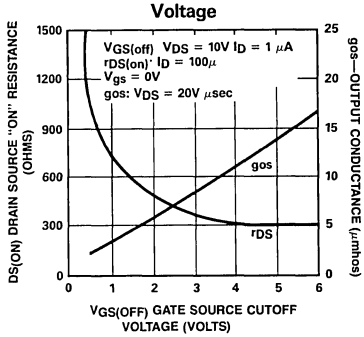
PRINCIPAL DEVICES
2N4338-41, VCR4N
2N4867-9, 2N4869A-9A
2N4220-2 2N4220A-2A,
J201-204, PN4302-04, J230-2
All single Part No's above

PERFORMANCE CURVES (25°C unless otherwise noted)

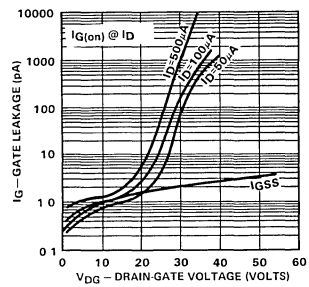
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



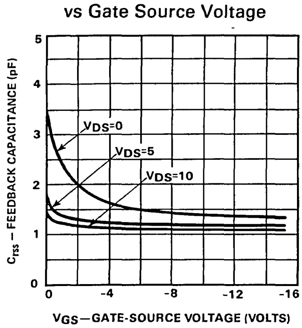
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



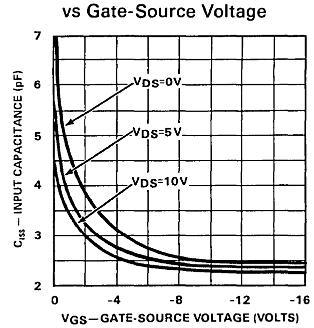
Gate Operating Current vs Drain-Gate Voltage



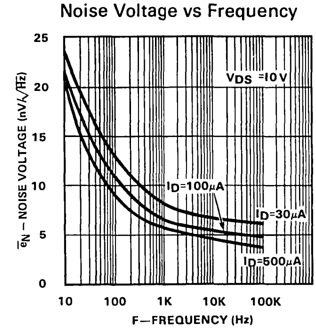
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



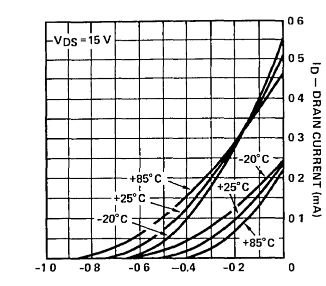
Common Source Input Capacitance vs Gate-Source Voltage



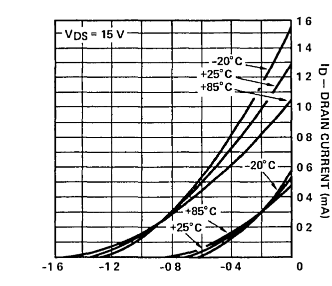
Noise Voltage vs Frequency



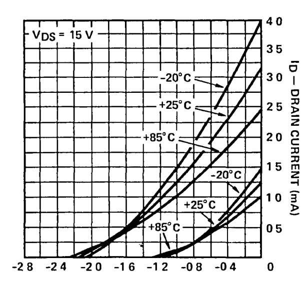
Transfer Characteristics



Transfer Characteristics

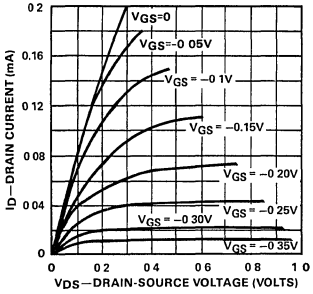


Transfer Characteristics

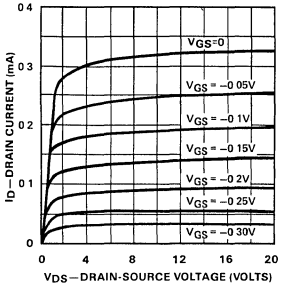


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

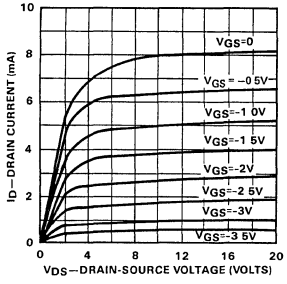
Output Characteristic
($V_{GS(off)}$ = −0.5V)



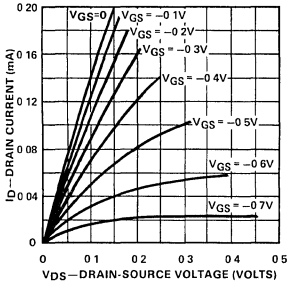
Output Characteristic
($V_{GS(off)}$ = −0.5V)



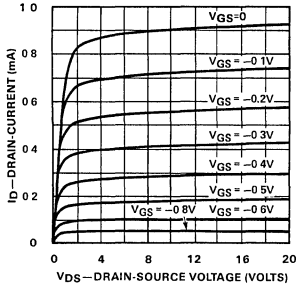
Output Characteristic
($V_{GS(off)}$ = −4.2V)



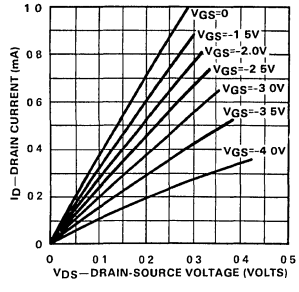
Output Characteristic
($V_{GS(off)}$ = −1.0V)



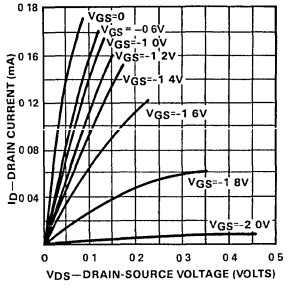
Output Characteristic
($V_{GS(off)}$ = −1.0V)



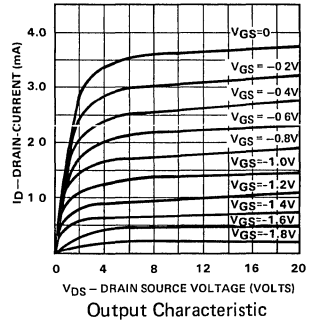
Output Characteristic
($V_{GS(off)}$ = −4.2V)



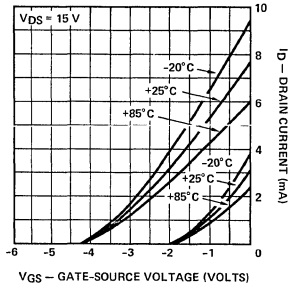
Output Characteristic
($V_{GS(off)}$ = −2.3V)



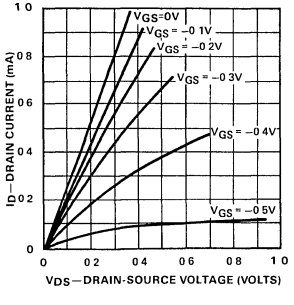
Output Characteristic
($V_{GS(off)}$ = −2.3V)



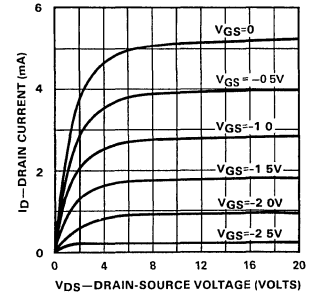
Transfer Characteristics



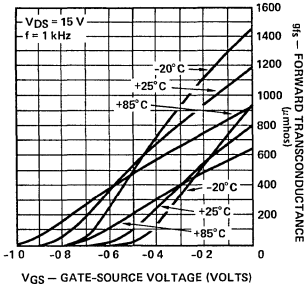
Output Characteristic
($V_{GS(off)}$ = −3.0V)



Output Characteristic
($V_{GS(off)}$ = −3.0V)

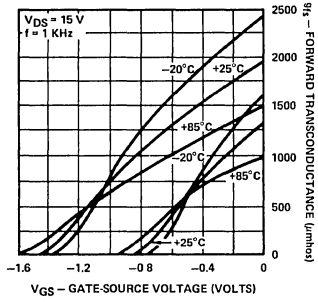


Transconductance Characteristics

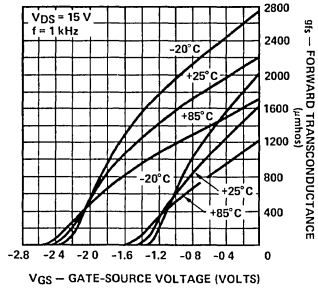


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

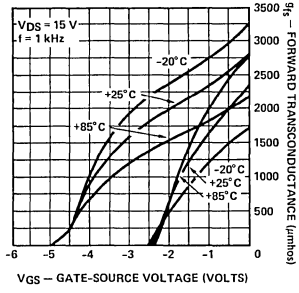
Transconductance Characteristics

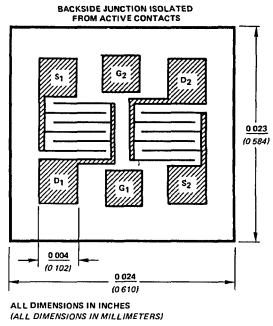


Transconductance Characteristics



Transconductance Characteristics





monolithic dual n-channel JFET

designed for . . .

- General Purpose Differential Amplifiers

TYPE	PACKAGE
Dual	TO-71
Dual	Chip

BENEFITS:

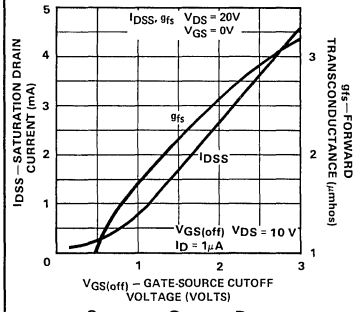
- Low Cost
- High Input Impedance

PRINCIPAL DEVICES

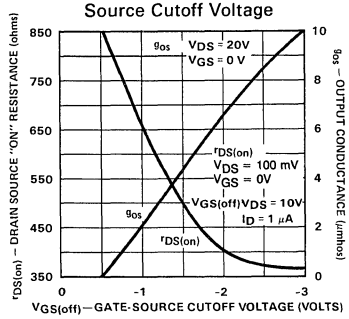
2N3954-55, 2N3954A-55A,
2N3956-58, 2N5045-47,
2N5196-99, 2N5515-24, 2N5452-54
U231-35, U410-12
2N3955, 2N3956-58
2N5047, 2N5199
2N5454, U233-35
U411, 12

PERFORMANCE CURVES (25°C unless otherwise noted)

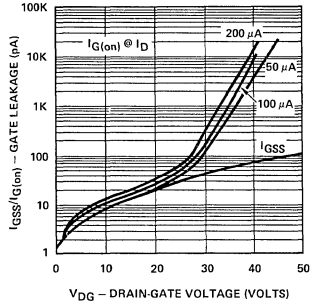
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



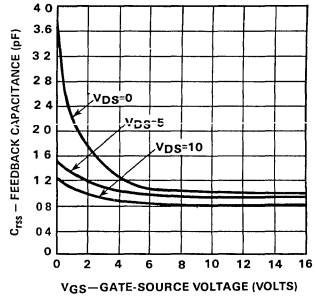
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



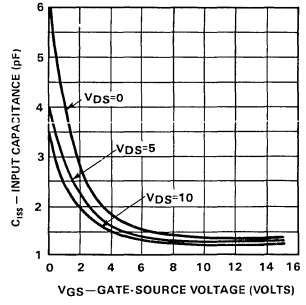
Gate Operating Current vs Drain Current



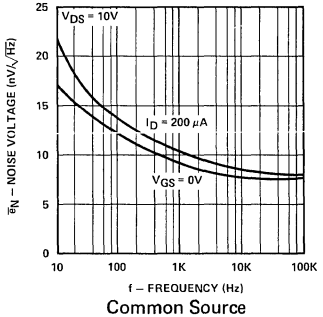
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



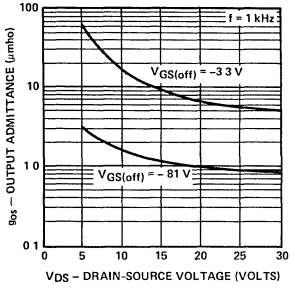
Common Source Input Capacitance vs Gate-Source Voltage



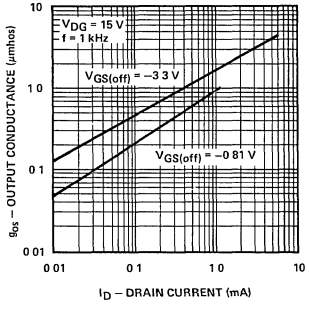
Equivalent Input Noise Voltage vs Frequency



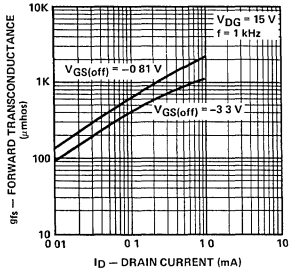
Common Source Output Admittance vs Drain-Source Voltage



Common-Source Output Conductance vs Drain Current

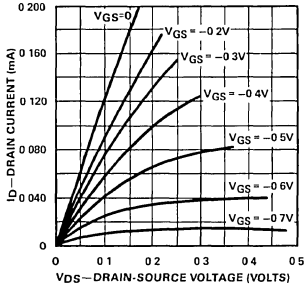


Common Source Forward Transconductance vs Drain Current

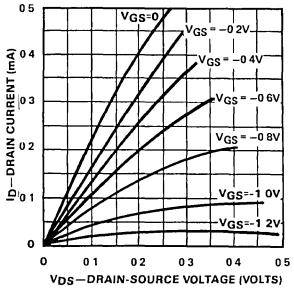


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

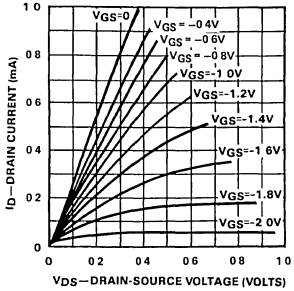
Output Characteristic
($V_{GS(off)}$ = −1.0V)



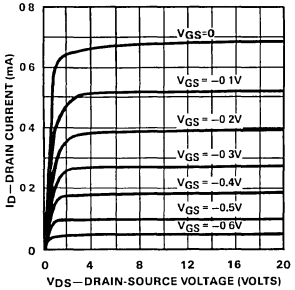
Output Characteristic
($V_{GS(off)}$ = −1.5V)



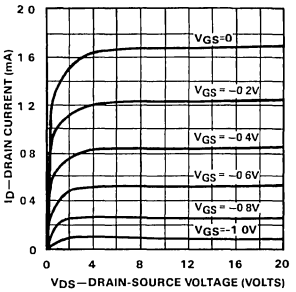
Output Characteristic
($V_{GS(off)}$ = −2.3V)



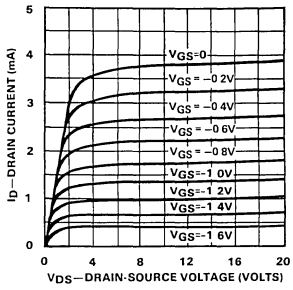
Output Characteristic
($V_{GS(off)}$ = −1.0V)



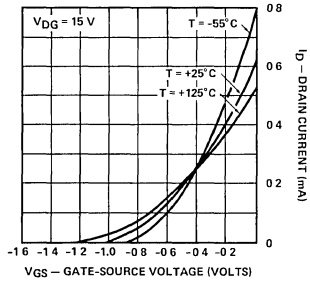
Output Characteristic
($V_{GS(off)}$ = −1.5V)



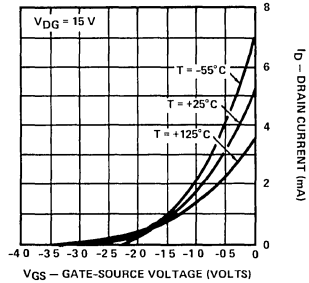
Output Characteristic
($V_{GS(off)}$ = −2.3V)



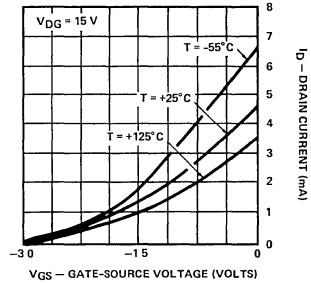
Transfer Characteristics
Low $V_{GS(off)}$



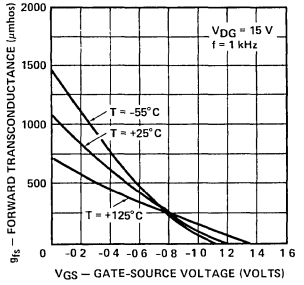
Transfer Characteristics
Medium $V_{GS(off)}$



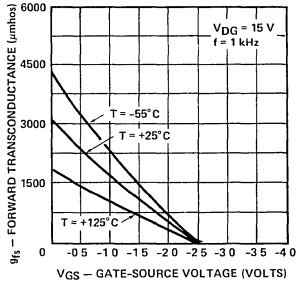
Transfer Characteristics
High $V_{GS(off)}$



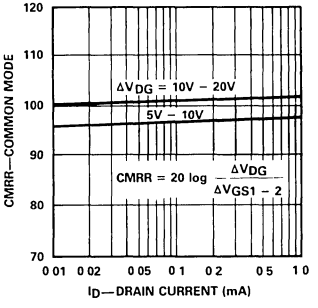
Transconductance Characteristics
Low $V_{GS(off)}$

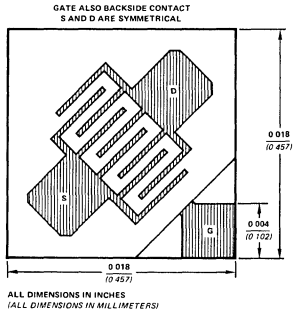


Transconductance Characteristics
Medium $V_{GS(off)}$



CMRR vs Drain Current





n-channel JFET
designed for . . .

- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

Siliconix

BENEFITS:

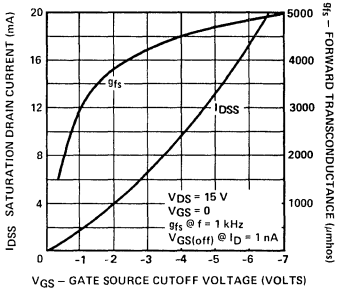
- Wide Input Dynamic Range
  High I_G Breakpoint Voltage
- High Gain
- Low Insertion Loss Switches

TYPE	PACKAGE
Single	TO-72
Single	TO-92
Single	Chip

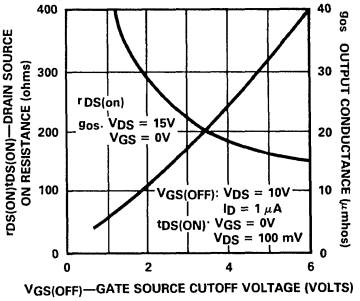
PRINCIPAL DEVICES
2N3821-4, 2N3921-22, 2N4220-2
2N4220A-2A, 2N4223-24
2N3819, 2N5457-9
MPF109, MPF111, MPF102, MPF108, MPF112
All of the above

PERFORMANCE CURVES (25°C unless otherwise noted)

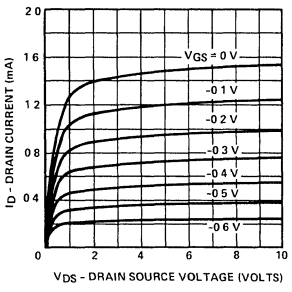
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



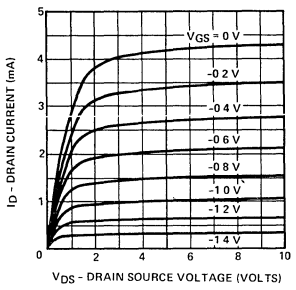
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



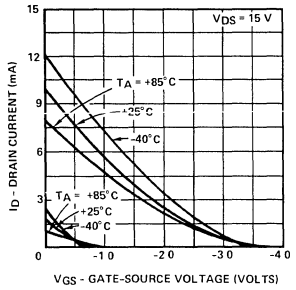
Output Characteristic ($V_{GS(off)}$ = −0.8V)



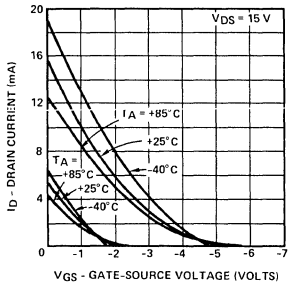
Output Characteristic ($V_{GS(off)}$ = −2.0V)



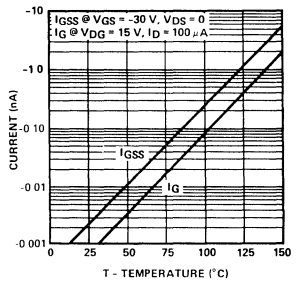
Transfer Characteristic



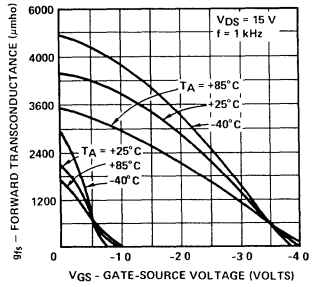
Transfer Characteristics



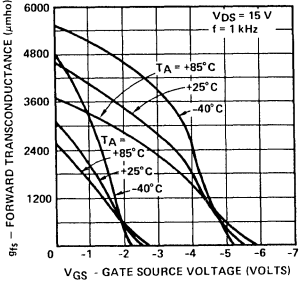
Leakage Currents vs Ambient Temperature



Transconductance Characteristics

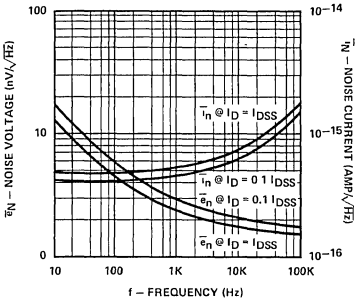


Transconductance Characteristics

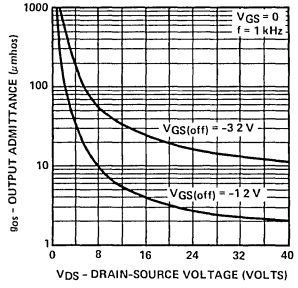


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

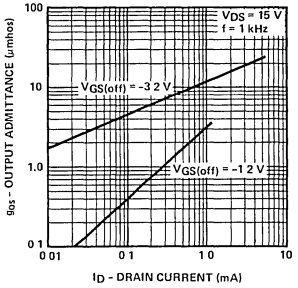
Equivalent Input Noise Voltage and Noise Current vs Frequency



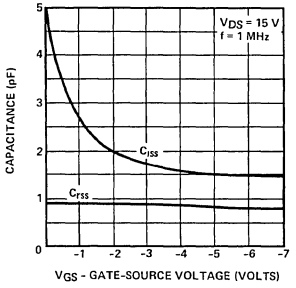
Common-Source Output Admittance vs Drain-Source Voltage



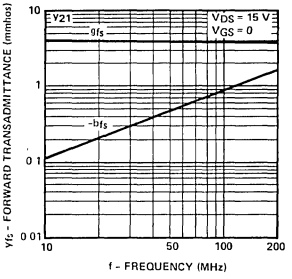
Common-Source Output Admittance vs Drain Current



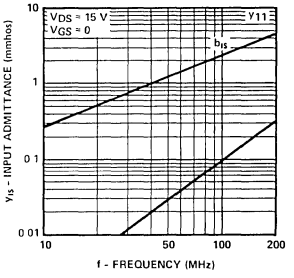
Common-Source Capacitances vs Gate-Source Voltage



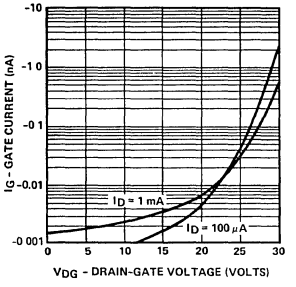
Common-Source Forward Transadmittance vs Frequency



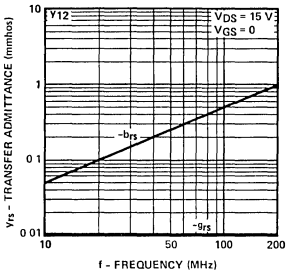
Common-Source Input Admittance vs Frequency



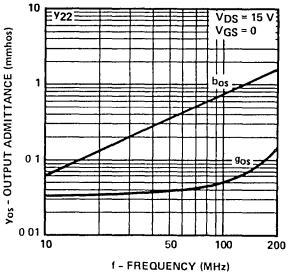
Gate Operating Current vs Drain-Gate Voltage



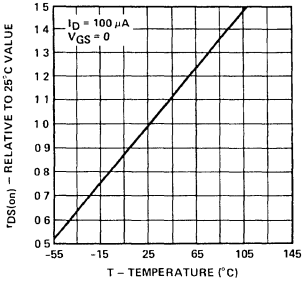
Common-Source Reverse Transfer Admittance vs Frequency



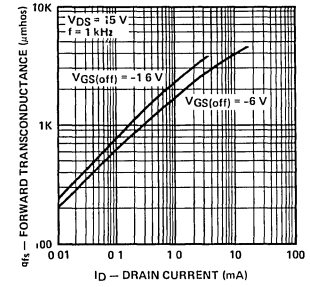
Common-Source Output Admittance vs Frequency



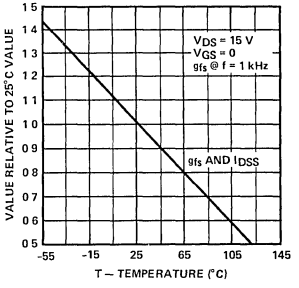
'ON' Resistance vs Ambient Temperature

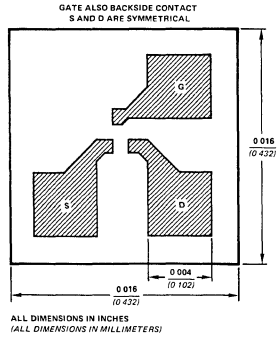


Common-Source Forward Transconductance vs Drain Current



Drain Current and Transconductance vs Ambient Temperature





n-channel JFET
designed for . . .

Siliconix

- **Ultra-High Input Impedance Amplifiers**
  - Electrometers
  - pH Meters
  - Smoke Detectors

TYPE	PACKAGE
Single	TO-72
Single	TO-92
Dual	TO-78
Single	Chip

BENEFITS:

- **Low Power**
  $I_{DSS} < 90\ \mu A$ (2N4117)
- **High Input Impedance**
  $I_G < 1$ pA (2N5906-09)

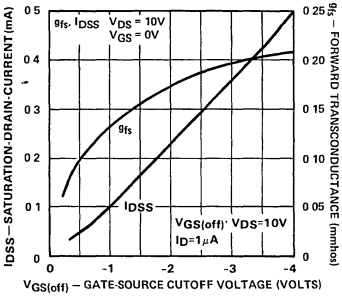
PRINCIPAL DEVICES

2N4117-9, 2N4117A-9A,
FN4117-18, FN4117A-18A, VCR7N
PN4117 Thru PN4120
PN4117A Thru 4120A

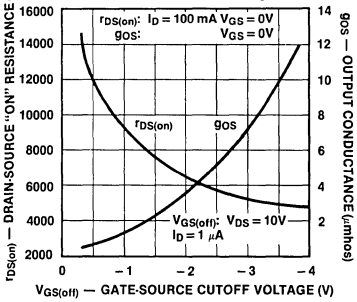
All singles above,

PERFORMANCE CURVES (25°C unless otherwise noted)

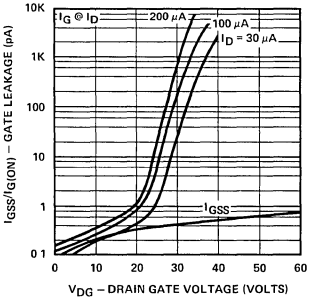
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



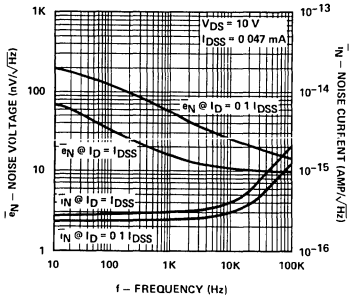
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



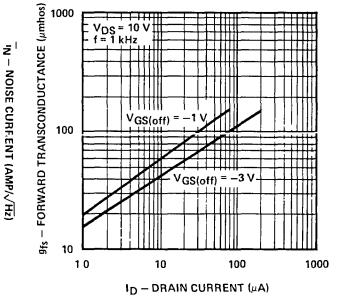
Gate Operating Current vs Drain-Gate Voltage



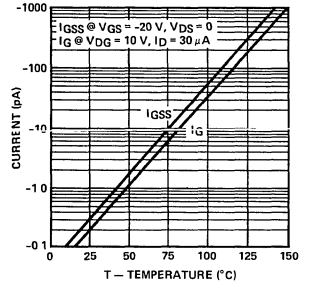
Equivalent Input Noise Voltage and Noise Current vs Frequency



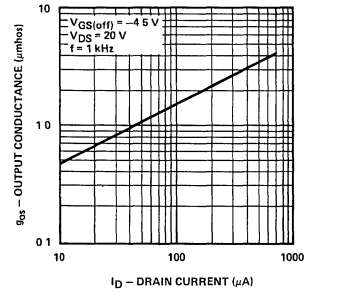
Common-Source Forward Transconductance vs Drain Current



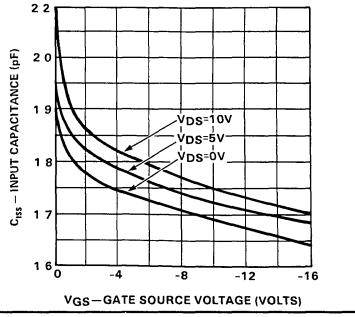
Leakage Currents vs Ambient Temperature



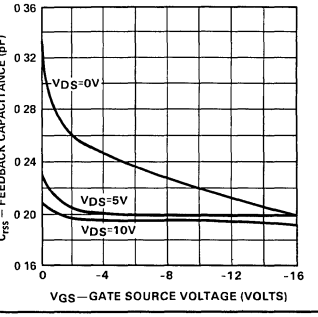
Common-Source Output Conductance vs Drain Current



Input Capacitance vs Gate-Source Voltage

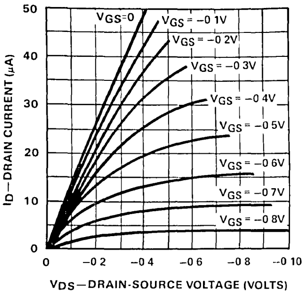


Reverse Feedback Capacitance vs Gate Source Voltage

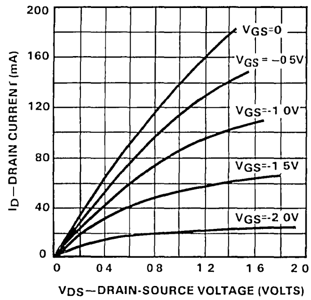


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

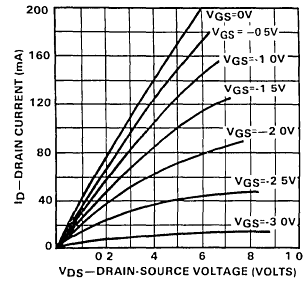
Output Characteristic
($V_{GS(off)}$ = −1.0V)



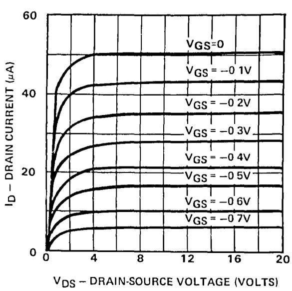
Output Characteristic
($V_{GS(off)}$ = −2.5V)



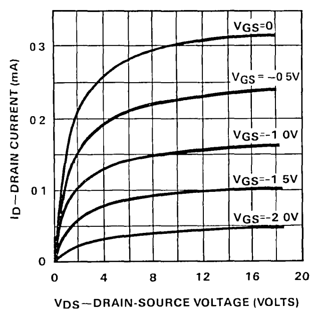
Output Characteristic
($V_{GS(off)}$ = −3.5V)



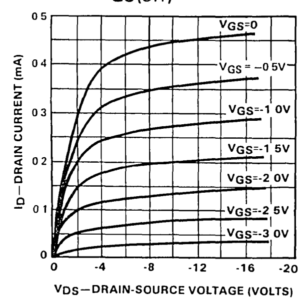
Output Characteristic
($V_{GS(off)}$ = −1.0V)



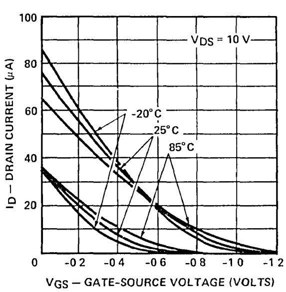
Output Characteristic
($V_{GS(off)}$ = −2.5V)



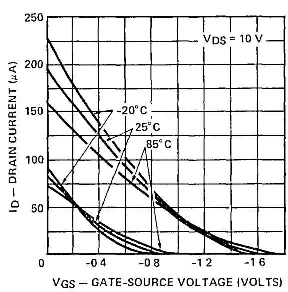
Output Characteristic
($V_{GS(off)}$ = −3.5V)



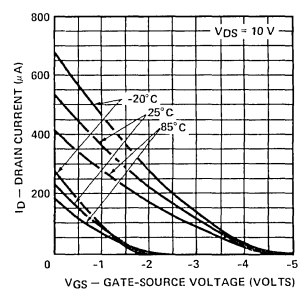
Transfer Characteristics



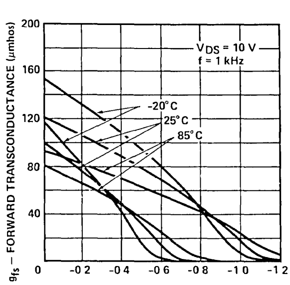
Transfer Characteristics



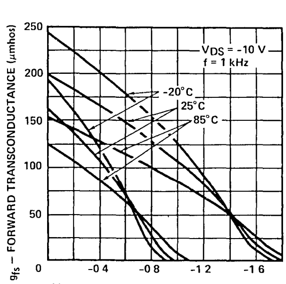
Transfer Characteristics



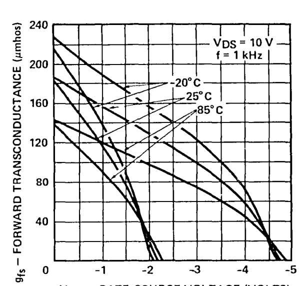
Transconductance Characteristics

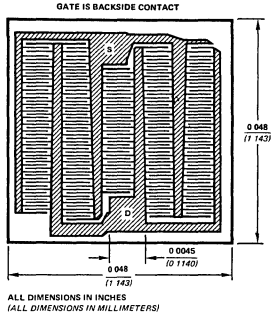


Transconductance Characteristics



Transconductance Characteristics





n-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers

Siliconix

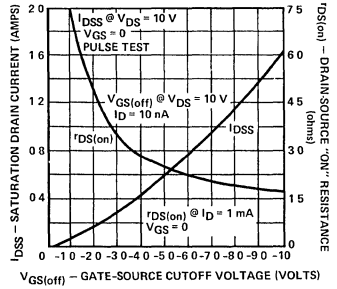
BENEFITS:

- Very Low Insertion Loss
  $r_{DS(on)}$ < 2.5 Ohms (U290)
- High Off-Isolation

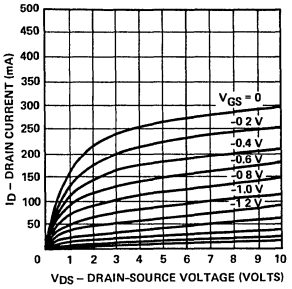
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U290-1
Single	TO-92	J105-7
Single	Chip	U290CHP-1CHP, J105CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

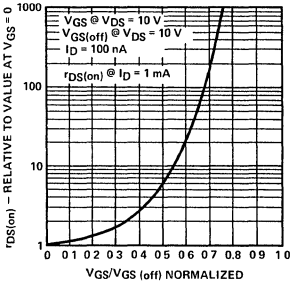
Saturation Drain Current and Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



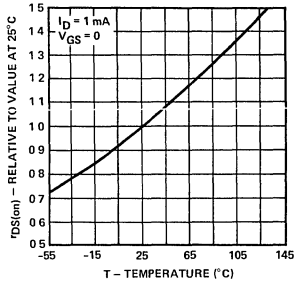
Output Characteristic



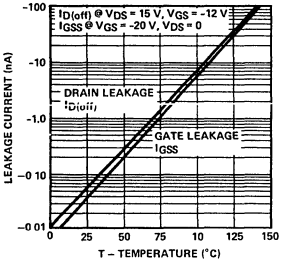
Drain-Source Resistance vs Normalized Gate-Source Voltage



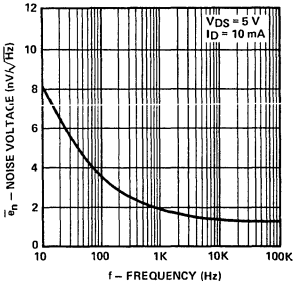
Drain-Source 'ON' Resistance vs Ambient Temperature



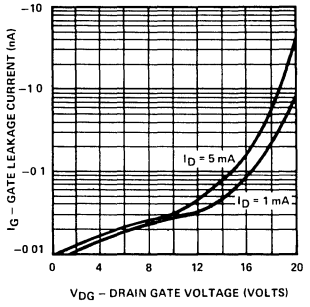
Leakage Currents vs Ambient Temperature



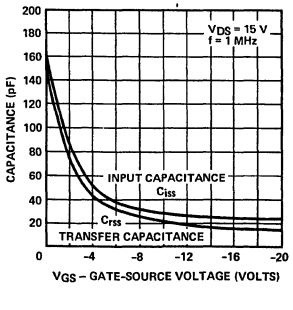
Equivalent Input Noise Voltage vs vs Frequency



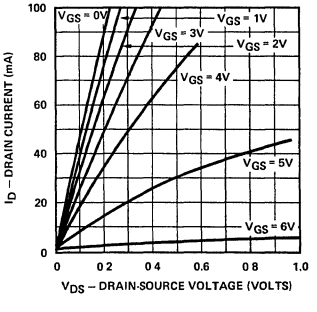
Leakage Current vs Drain-Gate Voltage

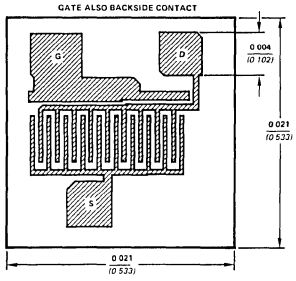


Common-Source Capacitance vs Gate-Source Voltage



Output Characteristic ($V_{GS(off)}$ = −7.5V)





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U308-10
Single	TO-72	U311
Single	TO-92	J308-10, 2N5638-40
Dual	TO-78	U4301, 4350
Single	Chip	J308CHP-10CHP, U308CHP-10CHP, U311CHP
Dual	Chip	U430CHP-1CHP

n-channel JFET
designed for . . .

- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

BENEFITS

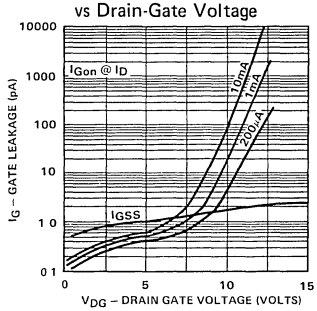
- Industry Standard
- High Power Gain
  16 dB at 100 MHz, Common Gate
  11 dB at 450 MHz, Common Gate

Siliconix

BENEFITS

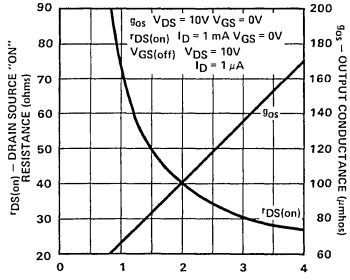
- Low Noise
  3 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater Than 100 dB
- 75 Ohm Input Match Common Gate

Gate Operating Current vs Drain-Gate Voltage

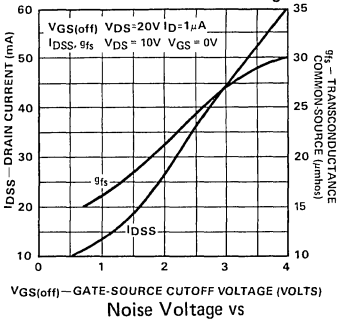


PERFORMANCE CURVES (25°C unless otherwise noted)

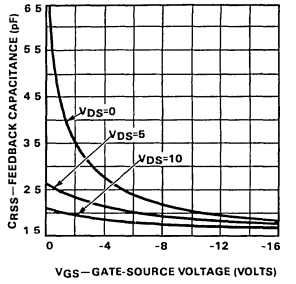
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



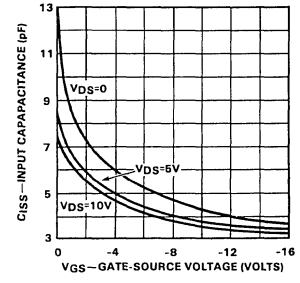
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



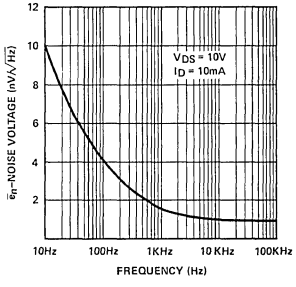
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



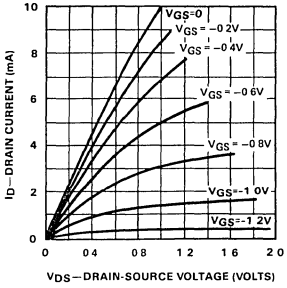
Common Source Input Capacitance vs Gate-Source Voltage



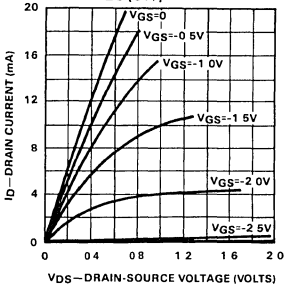
Noise Voltage vs Frequency



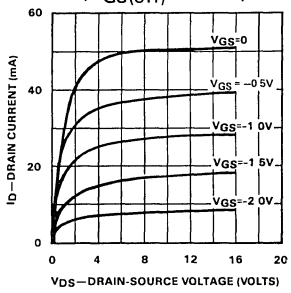
Output Characteristic (VGS(off) = −1.7V)



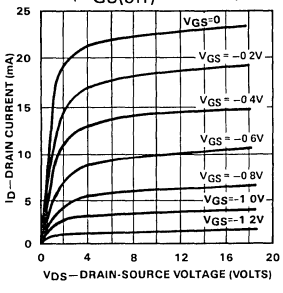
Output Characteristic (VGS(off) = −3.0V)



Output Characteristic (VGS(off) = −3.0V)



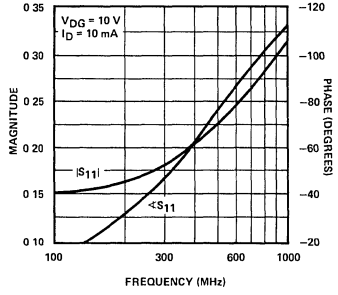
Output Characteristic (VGS(off) = −1.7V)



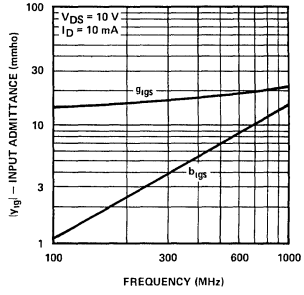
4

PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

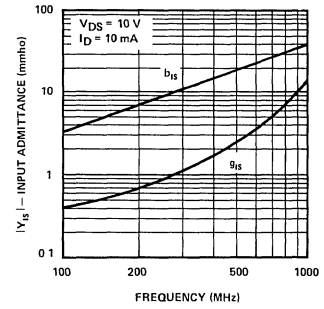
Forward Reflection Coefficient Common Gate



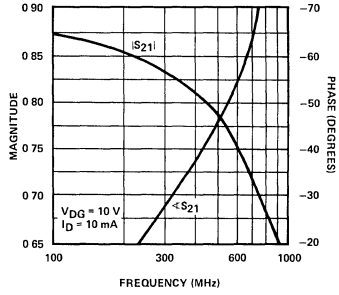
Input Admittance Common Gate



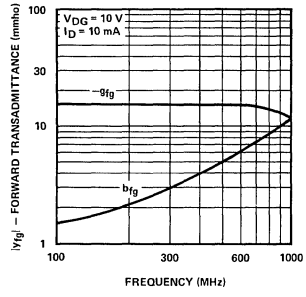
Input Admittance Common Source



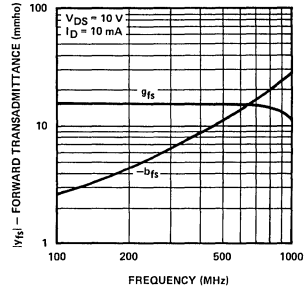
Forward Transmission Coefficient Common Gate



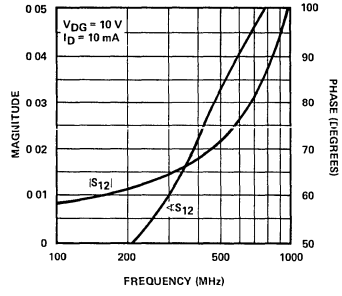
Forward Transfer Admittance Common Gate



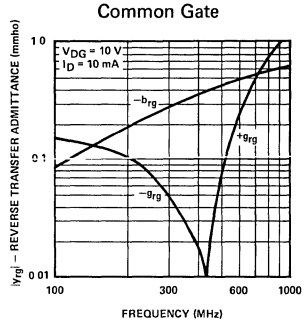
Forward Transfer Admittance Common Source



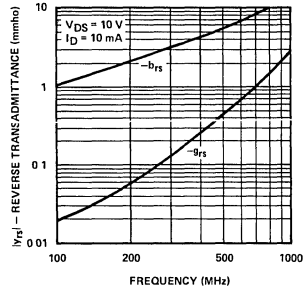
Reverse Transmission Coefficient Common Gate



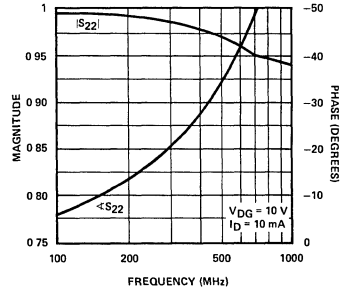
Reverse Transfer Admittance Common Gate



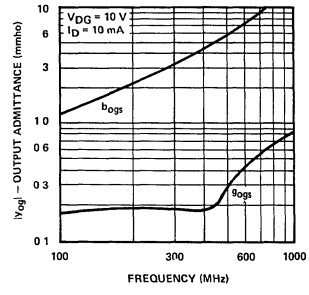
Reverse Transfer Admittance Common Source



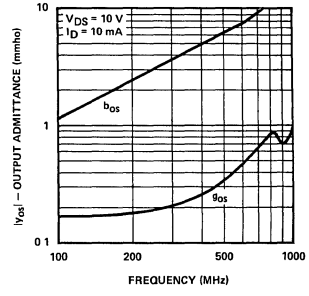
Reverse Reflection Coefficient Common Gate

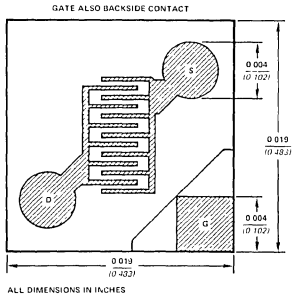


Output Admittance Common Gate



Output Admittance Common Source





n-channel JFET
designed for . . .

Siliconix

- High Frequency Amplifiers
- Mixers
- Oscillators

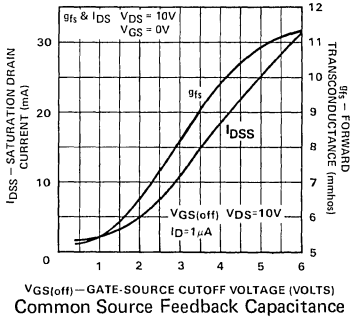
BENEFITS:

- High Power Gain
- Low Input Capacitance

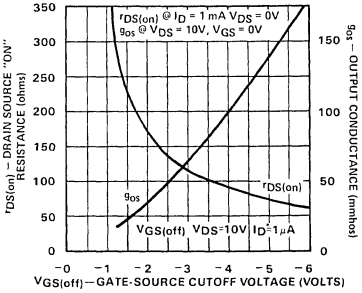
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-92	J300, J210-12
Dual	TO-78	2N5911-12, U257 U443-U444
Dual	TO-71	U440-41
Single	Chip	J300, J210-2CHP
Dual	Chip	2N5912CHP, U257CHP U441CHP, U444CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

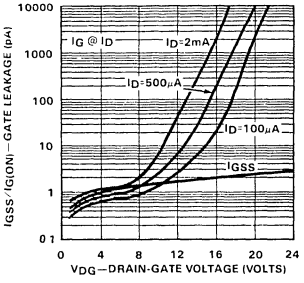
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



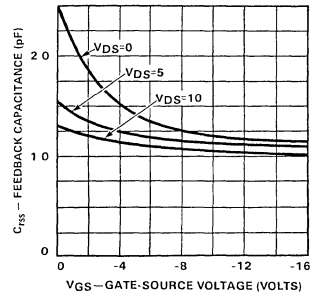
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



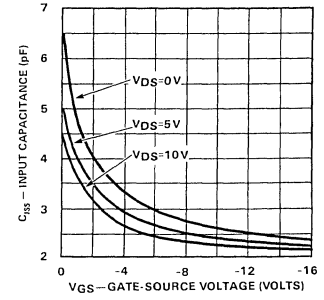
Gate Operating Current vs Drain-Gate Voltage



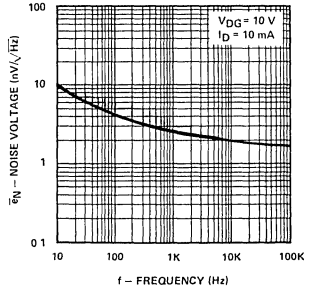
Common Source Feedback Capacitance vs Gate-Source Voltage



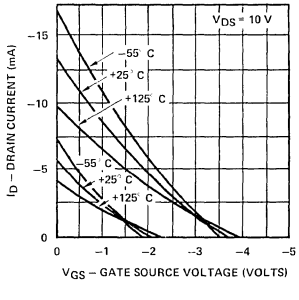
Common Source Input Capacitance vs Gate-Source Voltage



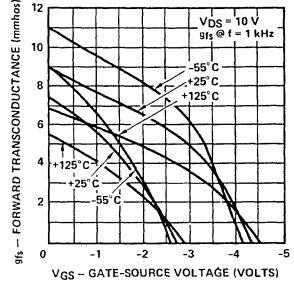
Equivalent Input Noise Voltage vs Frequency



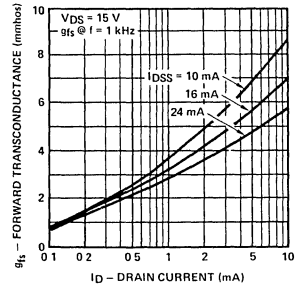
Transfer Characteristics



Transconductance Characteristics

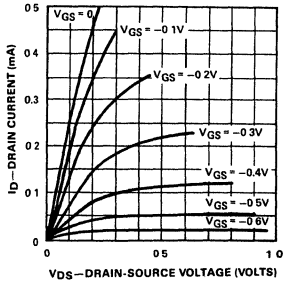


Forward Transconductance vs Drain Current

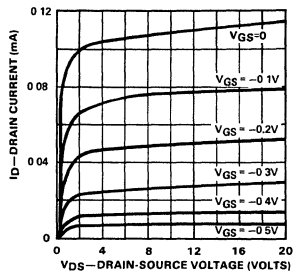


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

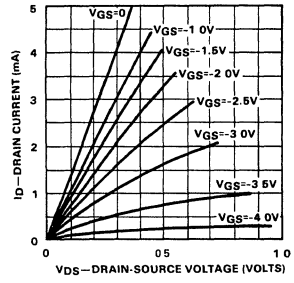
Output Characteristic
($V_{GS(off)}$ = −0.8V)



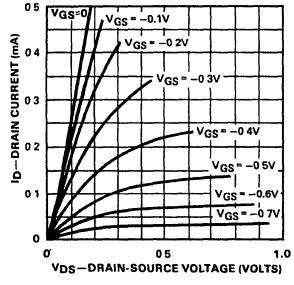
Output Characteristic
($V_{GS(off)}$ = −0.8V)



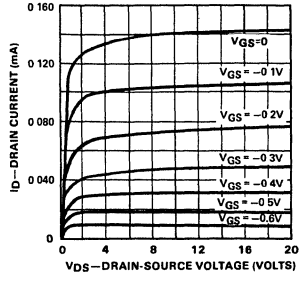
Output Characteristic
($V_{GS(off)}$ = −5.0V)



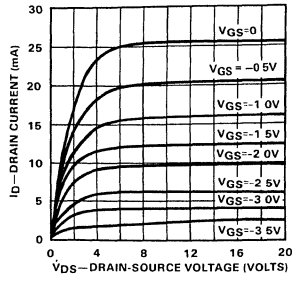
Output Characteristic
($V_{GS(off)}$ =-1.0V)



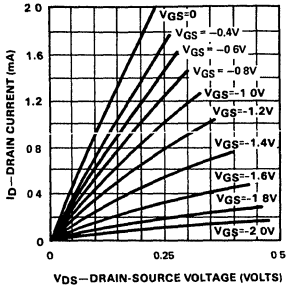
Output Characteristic
($V_{GS(off)}$ =-1.0V)



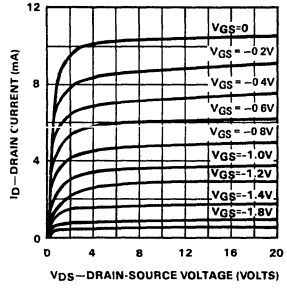
Output Characteristic
($V_{GS(off)}$ = −5.0V)



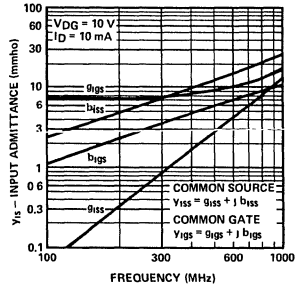
Output Characteristic
($V_{GS(off)}$ = −2.8V)



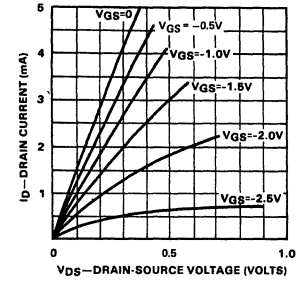
Output Characteristic
($V_{GS(off)}$ = −2.8V)



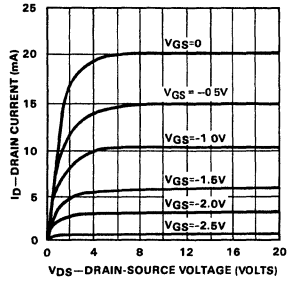
Input Admittance vs Frequency



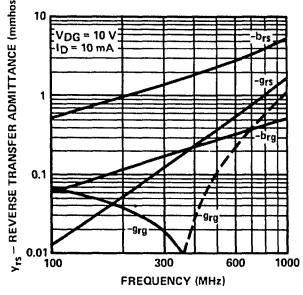
Output Characteristic
($V_{GS(off)}$ = −3.5V)



Output Characteristic
($V_{GS(off)}$ = −3.5V)

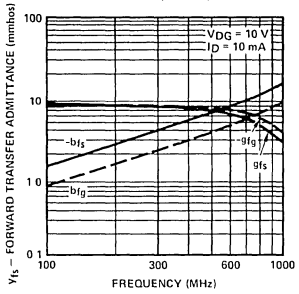


Reverse Transfer Admittance vs Frequency

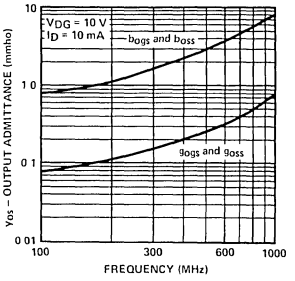


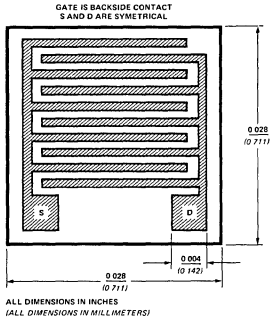
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

Forward Transfer Admittance vs Frequency



Output Admittance vs Frequency





p-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

Siliconix

BENEFITS:

- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

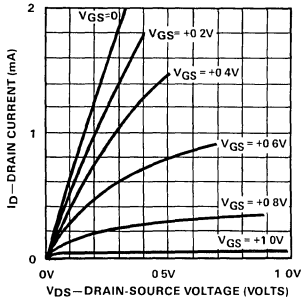
TYPE	PACKAGE
Single	TO-18
Single	TO-92
Single	Chip

PRINCIPAL DEVICES

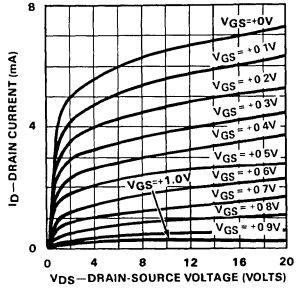
2N5018-19, 2N5114-16, U304-6, VCR3P
J174-7, J270-1, P1086-87
2N5018CHP-19CHP, 2N5114CHP-16CHP
U304CHP-6CHP, P1086CHP-87CHP
J270CHP-271CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

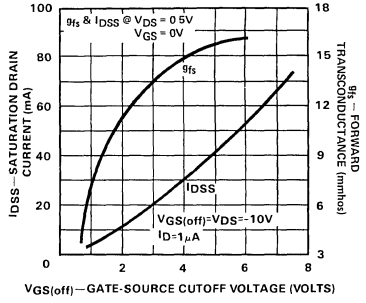
Output Characteristic
($V_{GS(off)}$ = +1.5V)



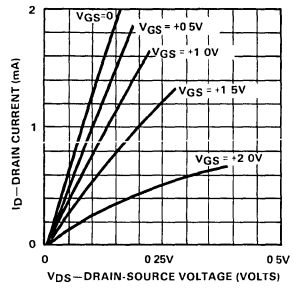
Output Characteristic
($V_{GS(off)}$ =+1.5V)



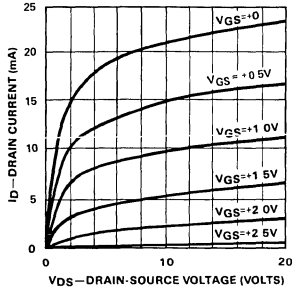
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



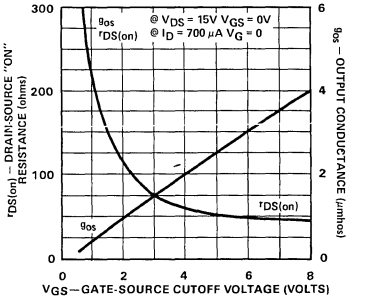
Output Characteristic
($V_{GS(off)}$ = +3.0V)



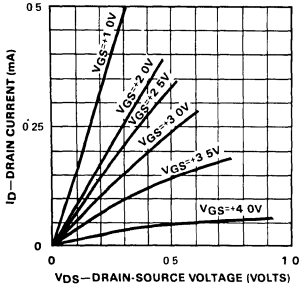
Output Characteristic
($V_{GS(off)}$ = +3.0V)



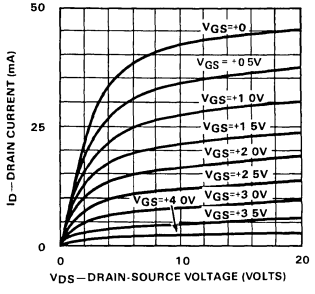
On Resistance and Output Conductance vs Gate-Source Voltage



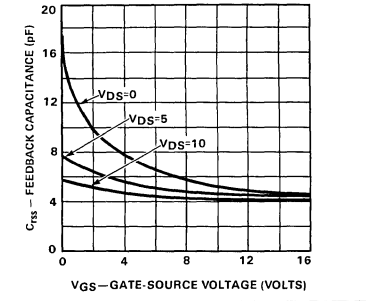
Output Characteristic
($V_{GS(off)}$ = +5.0V)



Output Characteristic
($V_{GS(off)}$ = +5.0V)

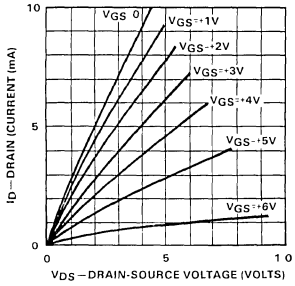


Common Source Reverse Feedback Capacitance vs Gate Source Voltage

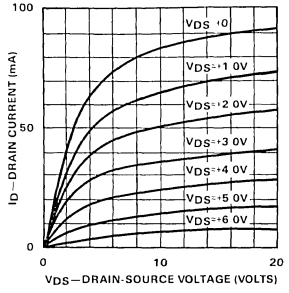


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

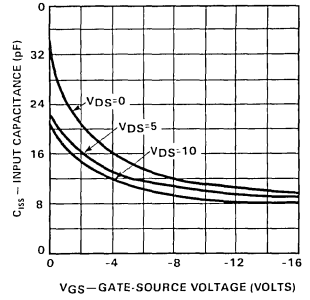
Output Characteristic
($V_{GS(off)}$ = +8.0V)



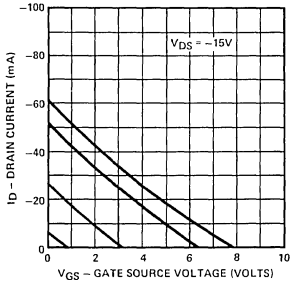
Output Characteristic
($V_{GS(off)}$ = +8.0V)



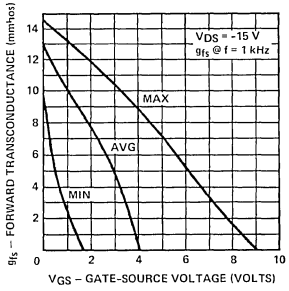
Common Source Input Capacitance vs Gate-Source Voltage



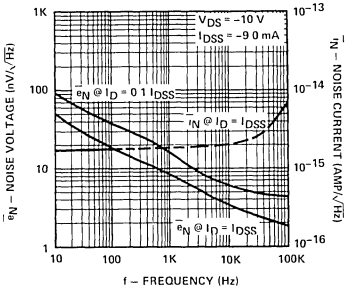
Transfer Characteristics

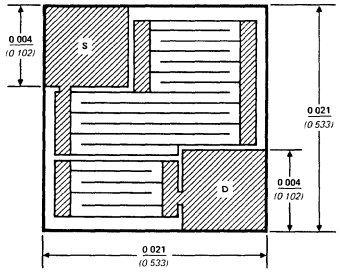


Transconductance Characteristics



Equivalent Input Noise Voltage and Noise Current vs Frequency





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

p-channel JFET
designed for . . .

- Amplifiers
- Sample and hold
- Choppers
- Analog Switches

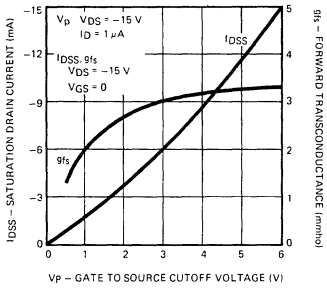
Siliconix

BENEFITS:

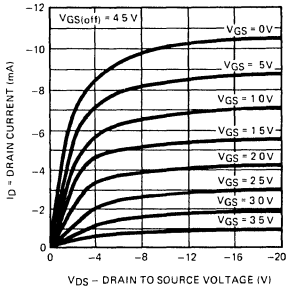
- **Low $\bar{e}_n < 15\ nV/\sqrt{Hz}$ at 10 kHz**
- **Low leakage < 10 pA at 30 V**

TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-92	2N5460 – 65
	Chip	All of the above
	TO-72	Available thru the factory
	TO-18	Contact local sales office

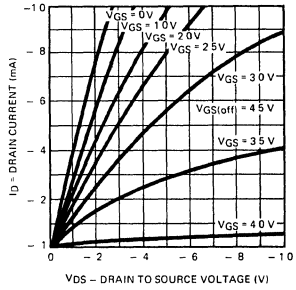
Drain Current & Transconductance vs Gate to Source Cutoff Voltage



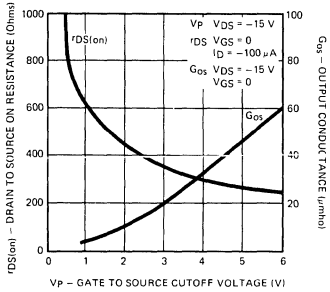
Output Characteristics



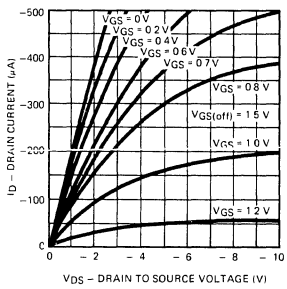
Output Characteristics



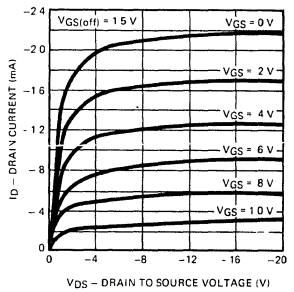
ON Resistance & Output Conductance vs Gate to Source Cutoff Voltage



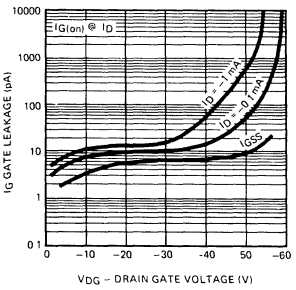
Output Characteristics



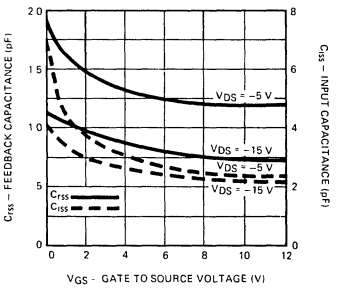
Output Characteristics



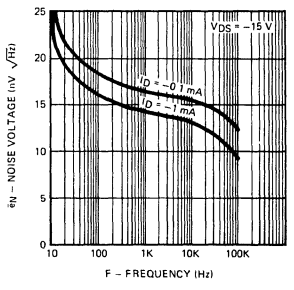
Gate Operating Current vs Drain-Gate Voltage

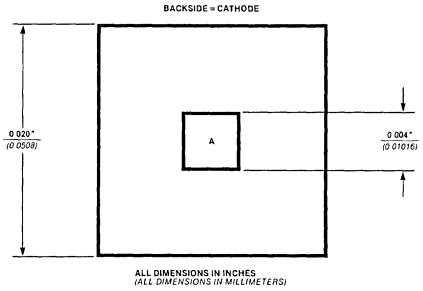


Capacitance vs Gate to Source Voltage



Noise Voltage vs Frequency





high voltage protection diode

designed for . . .

- **Limiting Current**
- **Voltage Protection**
- **Voltage Decoupling**

BENEFITS

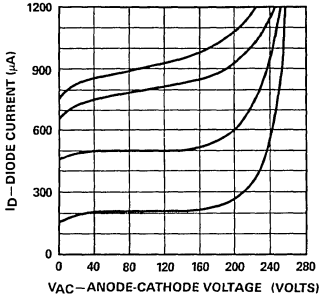
- Series element
- Two terminals
- Simple to use
- High breakdown voltage (JR240V—240 volts)
- Low Cost

TYPE	PACKAGE
Single	TO-92

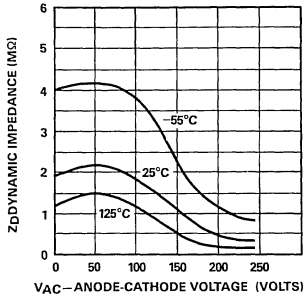
PRINCIPAL DEVICES
JR135V, JR170V, JR200V
JR220V, JR240V

PERFORMANCE CURVES (25°C unless otherwise specified)

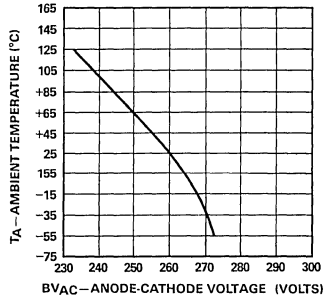
Output Characteristic



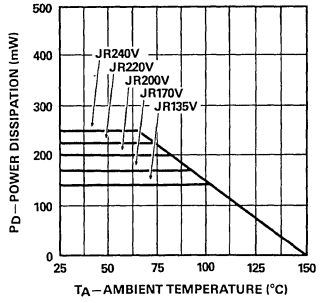
Dynamic Impedance Vs. Anode-Cathode Voltage at Temperature



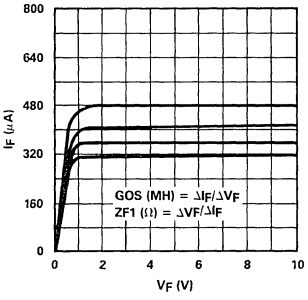
Breakdown Voltage Vs. Temperature



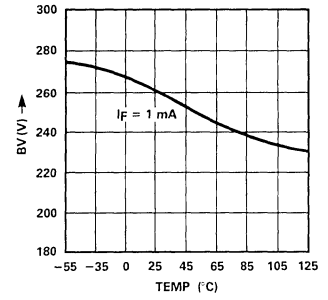
Free Air Temperature Dissipation Derating Curve



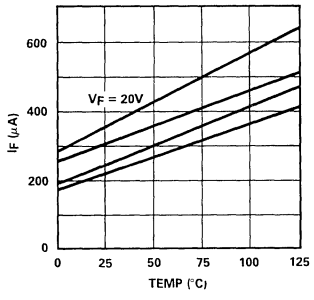
Family Curves



BV vs Temperature



IF vs Temperature



Selector Guides 5

Tips on Selecting the Right FET for Your Application

The "Product Specification," a short form version of technical data, will provide you direct reference to Siliconix part numbers and a condensed version of technical specifications

IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 5-4, "How to Choose the Correct FET for Your Application." Using this guide, determine the important FET parameters.
2. Next, turn to page 5-6, "JFET Geometry Selector Guide." Using this guide, choose the appropriate geometry.
3. Once you have chosen a geometry, turn to "Geometry Characteristics," section 4 of the catalog. Here you make the choice of a suitable part number.
4. Now that you have the part number, you will find complete electrical specifications of these products in the "Data Sheets," section 2 of the catalog.

IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Product Specifications," pages 5-9 through 5-18 to determine the proper part number(s).
2. Double-check your choices against the data sheets, and select the part most suited for your application.

Small-Signal FET Application Selection Preference

Additional Information

Popular Product Type	Si8901, U350	2N4117-9, PN4117-20, 2N4338-41, 2N4867-9A, J230-2	2N4416, PN4416, J304-5, 2N5484-6	2N3821-2, 2N5457-9, U3008-10, J300, J210-2	J105-7, U290-1	2N5432-4, J108-10	2N4856-61, 2N4391-3, J111-13, 2N4391-3	3N163, 4, MFE823	U421-U428	2N5196-9, 2N5515-24, 2N5555-7, 2N5906-8, U231-5	U401-6, 2N6905-7	2N5911-12, U440-1, U443-4	2N5564-6, DN5564-6	2N5018-21, 2N5114-6, J174-7, VCR 32	2N5460-5	J500-J511	CRR0240-CRR0560, J6100	CRR0800-CRR1250, CR1068-CR150	CR1450-CRR4300, CR1160-CR530	SD210-SD215DE	JR135V-JR240V	M5397CHP-12CHP, M440CHP, M441CHP	M116—CONTACT FACTORY	SI1600-20, SI100, 2N6908-10, 2N6911	SD5000, SD210
Process Designation	**NT**	**NPA**	**NH**	**NRL**	**NZB**	**NZF**	**NVA**	**NIP**	**NCB**	**MRA**	**NNT**	**NQP**	**NNR**	**NZFD**	**NCB-D**	**PSB**	**PSCB**	**NCL**	**NKL**	**NKM**	**NKO**	**DMCB**	**VRMA**	**NNZ**	**MBN**	**NBA**	**DMCA/B**
Low Current Amplifier	P	S		S						P	P	P	P				P								P	
Low Freq Amplifier < 100 Hz		S		S					S	P		P	P			S									P	
High Freq Amplifier > 100 MHz			P		P	P								P								P		P		S	P
HF > 400 MHz Prime					P	S																P					P
General Purpose Amplifier		P	P	P					P							P	P					S				P	
Low Noise Amp (10 Hz e_n)		P	S	S				S	P			P	P		P											P	
Low Noise Amp > 50 MHz			P	S	P	P								P	P									P		P	
High Frequency Mixer	P		P		P	P																					P
Dual Diff Pair									S		P	P	P	P	S									P			
AGC Amplifier			P	P		P																					
Electrometer Preamp	P	S									P	S	S														
Microvolt Amplifier	P	S									P	P	P													P	
Low Leakage Diode	P	S																								P	
Low Leakage Dual Diode											P	S														P	
Smoke Detector Input	P									P																	
Battery Operated Amp < 1.5V	P	P									P																
Diff/Single Ended Inp Stag									S		P	P	P	P	P									P		P	
High Slew Rate Diff Amp									S					P	P									P		P	P
Active Filter		S	P	P																							
Oscillator		S	P	P	P	P																S					
Voltage Controlled Resistor		S	P	P					P				P			P	S										
Hybrid Chips	P	P	P	P					P		P	P	P			P	P	P	P	P	P					P	P
Analog/Digital Switch			S				P	P	P	S			S		S	P						P			P		P
Multiplexing			P	S			S	S	P							P						P			P		P
Choppers							P	P	P						P	P						P			P		P
Reed Relay Replacement							P	P														P					P
Sub pA Dual Diff Pair											P																
Sample Hold			P	S					P		S	S	S			P	P								S		P
Buffer Interface to CMOS																P	P										
Matched Switch												S	P	S	P									S			
Current Limiter									P							P		P	P	P	P		S				
Current Source	S	S		LV							LV							P	P	P	P						
High Voltage Protection Diode																							P				

Military Application

As an option, Siliconix offers all hermetically packaged product processed to MIL-STD-750. For information, contact your local Siliconix Sales Office or Siliconix, Incorporated direct.

P = Prime Choice
S = Secondary (alternative) Choice
LV = Limited Value

Small-Signal FET Product Selector Guide

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters	Preferred Parts
AMPLIFIER	Audio	Low noise (e_n), g_{fs}/g_{os}	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times	2N4339-40 2N4867-69 J230-32 J202-4 J308-10 U308-10 2N5911-12 2N4117A-19A U401-6 U421-6 2N6905-7 2N6908-11 SI1000-20 SI1100 SST201-4 SST4416 SST308-10
	Buffer	Low I_G, high g_{fs}			
	Differential	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	High Input Impedance	Very low I_G (e.g., MOSFET)			
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters			
	FET Input Op Amp	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude			
	Low Supply Voltage	Low $V_{GS(off)}$			
	Low Noise	Low e_n, i_n, low 1/f noise, low NF			
	Preamplifier	Operate near I_{DZO}, high g_{fs}/I_D ratio			
	Video	High g_{fs}/C_{iss} ratio, NF			
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs. Capacitance	g_{fs} g_{os} I_{DSS} max	SD210-15DE SD5000 2N4091-3 2N4391-3 PN4391-3 J108-10 J105-7 U290-1 2N5432-4 2N4856-61 2N5114-16
	Choppers	$r_{DS}/I_{D(off)}$ switching efficiency			
	Commutators	Low C_{rss}			
	Digital	Fast switching time			
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}			
	Sample and Hold	Low C_{rss}			
CONSTANT CURRENT SOURCE	Current Limiting	Low g_{oss}, low $V_{GS(off)}$, high BV_{GSS}	I_{DSS} vs. BV_{GSS}	g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters, capacitance	CRR Series J501-11 J552 Any J-FET
	Reference Current Source				
	Biasing				
VOLTAGE CONTROLLED RESISTORS	Gain Control	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}	VCR Series Any J-FET
	Amplitude Stability				
	Attenuators				
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}		$r_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$	U350 U430-1 U440-1-3-4 2N5911-12 U308-10 J308-10 SD210-15DE Si8901
	UHF				
	Double Balanced	Matching characteristics			
OSCILLATORS	Class A	Good g_{fs} at operating frequency	g_{fs} vs. Capacitance		2N4416 PN4416 U308-10 J308-10
	Class C	Low C_{iss} for VHF operation			

5

Small Signal FET Application/ Parameter Importance Guide

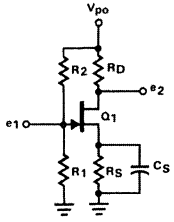
KEY PARAMETERS	BV_{GSS} (POV)	I_{GSS} (I_G)	I_D (off)	V_{GS1-2}/ V_{GS} (temp)	V_{GS} (off)	r_{DS}	I_{DSS}	g_{fso} (g_{fs} @ I_D)	g_{os}	High frequency Y parameters/PGain	e_n (NF)	C_{iss}/C_{rss}	t_{on}/t_{off}
LIMIT	**Min.**	**Max.**	**Max.**	**Max.**	**Min. Max.**	**Max.**	**Min. Max.**	**Min.**	**Max.**	**Min. Max.**	**Max.**	**Max.**	**Max.**
Low Current Amplifier	*	*			/*		*	*	D		?	?	
Low Freq Amplifier ≤ 100 Hz	*	*			/*		*	*	D		*		
High Freq Amplifier > 100 MHz	*	*		/*		*	*	D	G		*		
HF ≥ 400 MHz Prime	*	D			/*		*	*	?	G		*	
General Purpose Amplifier	*	*			/*		*	*	D		?		
Low Noise Amp (10 Hz e_n)	*	*			/*		*	*		G		*	
Low Noise Amp > 50 MHz	*	*			/*		*	*	?	G		*	
High Frequency Mixer	*	D			?/*		*	*	?	G		*	
Dual Diff Pair	*	(*)		*	/*		*/D	(*)	*		?	D	
AGC Amplifier	*	*			*/*		*	*	?			D	
Electrometer Preamp	*	(*)			/*		*	*	D		?	D	
Microvolt Amplifier	*	*			/*		*	*	*		*	D	
Low Leakage Diode	*	*										?	
Low Leakage Dual Diode	*	*										?	
Smoke Detector Input	*	*			*/*		*/	*	?				
Battery Operated Amp < 1.5V	*	*			/*		*	*	D			D	
Diff/Single Enced Inp. Stag.	*	(*)		*	/*		*	(*)	D			?	
High Slew Rate Diff Amp	*	(*)		*	/*		*/	(*)	*			*	
Active filter	*	*			/*		*	*	?			D	
Oscillator	*	*			/*		*	*	?			*	
Voltage Controled Resistor	?	D			*/*	*						D	
Hybrid Chips	Same as application area												
Analog/Digital Switch	*	*	*			*	*/					*	*
Multiplexing	*	*	*			*	*/					*	*
Choppers	*	*	*			*	*/					*	*
Reed Relay Replacement	*	*	*			*	*/					?	*
Sub pA Dual Diff Pair	*	(*)		*	/*		*/	(*)	*		?	D	
Sample Hold	*	*	*		/*	*	*/					*	
Buffer Interface to CMOS	*								?				
Matched Switch	*	*	*			*	*/					*	*
Current Limiter	*						*/*		*				
Current Source	*						*/*		*				
High Voltage Protection Diode	*						*/*		*				

* - Important FET Parameter - Required
? - Important for some applications
D - Desired "nominal" limit - rarely critical
G - Guaranteed by C_{iss}, C_{rss}, g_{fs}, and device design

*/ - Indicates "Min"
/* - Indicates "Max"
(*) - Indicates Parameter in Parenthesis

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters
AMPLIFIER	Audio Buffer Differential High Input Impedance High Frequency FET Input Op Amp Low Distortion Low Supply Voltage Low Noise Preamplifier Video	Low noise ($\overline{e}_n$), g_{fs}/g_{os} Low I_G, high g_{fs} Good matching V_{GS}, g_{fs}, I_{DSS}, I_G Very low I_G (eg., MOSFET) High g_{fs}/C_{iss} ratio, NF, RF parameters Good matching V_{GS}, g_{fs}, I_{DSS}, I_G High $V_{GS(off)}$ compared to signal amplitude Low $V_{GS(off)}$ Low $\overline{e}_n$, $\overline{i}_n$, low 1/f noise, low NF Operate near I_{DZO}, high g_{fs}/I_D ratio High g_{fs}/C_{iss} ratio, NF	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times
SWITCHES	Analog Gates Choppers Commutators Digital Integrator Reset Sample and Hold	Fast switching time $r_{DS}/I_{D(off)}$ switching efficiency Low C_{rss} Fast switching time Very low $R_{DS(on)}$, High I_{DSS} Low C_{rss}	$R_{DS(on)}$ vs Capacitance	g_{fs} g_{os} I_{DSS} max
CONSTANT CURRENT SOURCE	Current Limiting Reference Current Source Biasing	Low g_{oss}, low $V_{GS(off)}$, high BV_{GSS}	I_{DSS} vs BV_{GSS}	g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters capacitance
VOLTAGE CONTROLLED RESISTORS	Gain Control Amplitude Stability Attenuators	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}
MIXERS	VHF UHF Double Balanced	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss} Matching characteristics		$r_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$
OSCILLATORS	Class A Class C	Good g_{fs} at operating frequency Low C_{iss} for VHF operation	g_{fs} vs Capacitance	

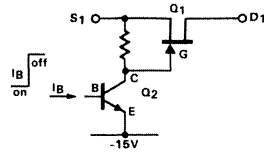
Basic Circuit*	Preferred Parts



V_{DD} (V)	R_S Ω	R_1 MΩ	R_2 MΩ	C_S NF	I_{DD} mA	R_D Ω	e_0 (V)	A_V
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97

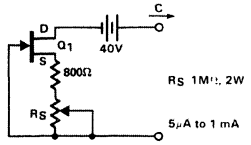
JFET Voltage Amplifier Stage Application Note: TA70-2

2N4339-40
2N4867-69
J230-32
J202-4
J308-10
U308-10
U401-6
U421-6



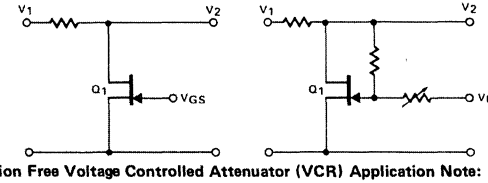
Shunt-Resistor Analog Switch Application Note: AN73-5

2N4091-3
2N4391-3
PN4091-3
PN4391-3
J108-10
J105-7
U290-1
2N5432-4
SD210DE-215DE



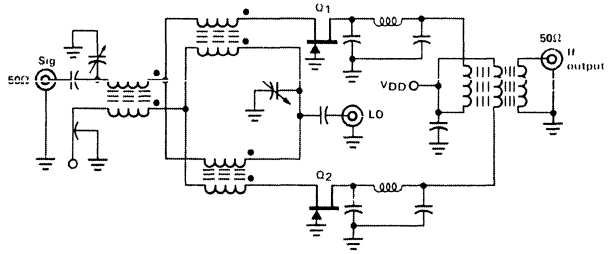
Equivalent Circuit of a JFET Current Limiter Application Note: DI71-1

CRR Series
J501-11
J552-7
Any J-FET
JR135V-240V



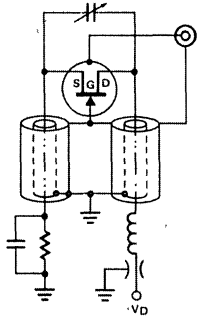
Distortion Free Voltage Controlled Attenuator (VCR) Application Note: AN73-1

VCR Series
Any J-FET



Single-Balanced VHF Balanced Mixer Application Note: AN72-1

U430-1
U440-1-3-4
2N5911-12
U308-10
J308-10
2N4416
U350
SD8901



UHF Transmission Line Oscillator Application Note: DI73-2

2N4416
PN4416
U308-10
J308-10

*for further details see Application Notes, Index 5

JFET Geometry Selector Guide

USEFUL JFET INFORMATION

	=	$C_{qs} + C_{gd}$	Input Capacitance
C_{OSS}	=	$C_{ds} + C_{gs} + C_{bd}$	Output Capacitance
C_{RSS}	=	C_{qd}	Reverse Feedback Capacitance
I_{DZ}	=	$I_{DSS} \left(\frac{0.63}{V_{GS(off)}}\right)^2$	Variation of $I_{(zero\ tc)}$ with Gate Source Cutoff Voltage
g_{fso}	=	$K \frac{I_{DSS}}{V_{GS(off)}}$	Forward transconductance as a function of I_{DSS} and $V_{GS(off)}$ at zero gate-source voltage (K = 1.5 to 2.5; typically = 2 for N-channel junction FET)
g_{fs}	=	$g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$	Variation of g_{fs} with gate bias
g_{fs}	=	$g_{fso}\sqrt{I_D/I_{DSS}}$	Variation of g_{fs} with drain current
$V_{GS(off)}$	=	$\frac{2\ I_{DSS}}{g_{fso}}$	Gate-Source cutoff voltage in terms of I_{DSS} and g_{fso}
V_{DS}	≈	$V_{GS(off)}\left(\frac{I_D}{I_{DSS}}\right)^{1/2}$	Drain voltage at which drain current saturates
r_{DS}	≃	$\frac{1}{g_{fs}}$	Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e. in the triode region
r_{DS}	≃	$\frac{[V_{GS(off)}]^2}{KI_{DSS}[V_{GS(off)} - V_{GS}]}$	K = 1.5 to 2.5 Variation of drain resistance in the triode region
I_D	=	$I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$	Variation of drain current with gate-source voltage. The square law transfer characteristic.

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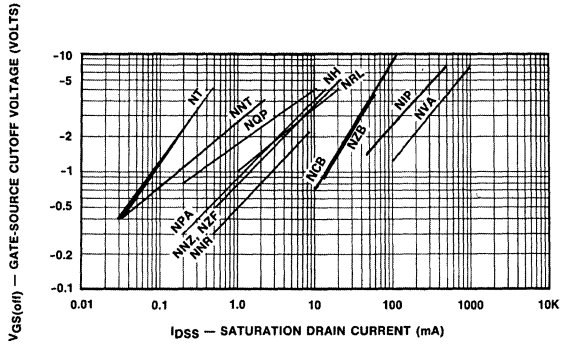
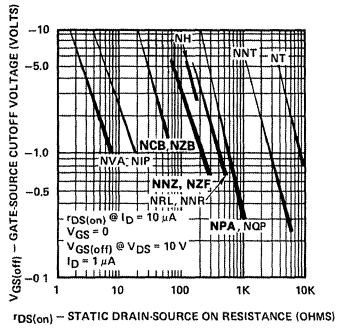
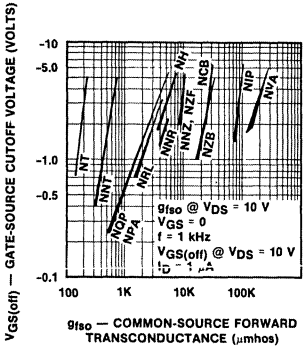
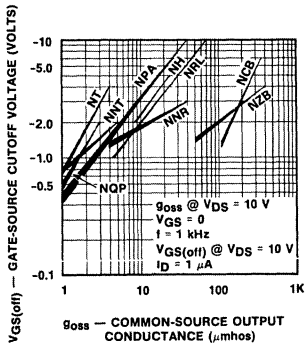
JFET Geometry Selector Guide (Cont'd)

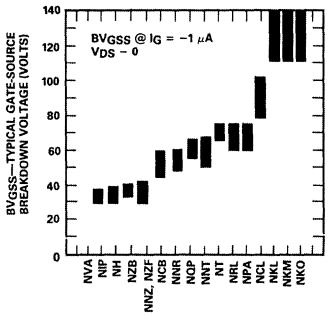
N-Channel JFETs

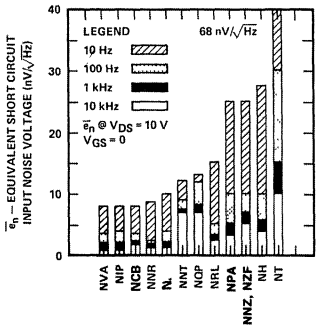


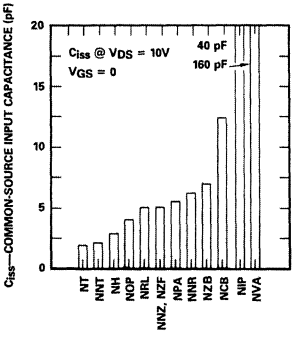


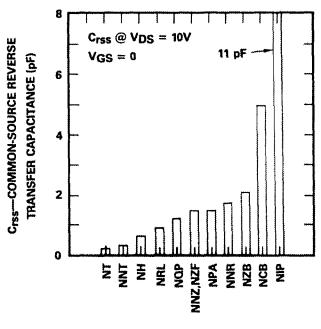






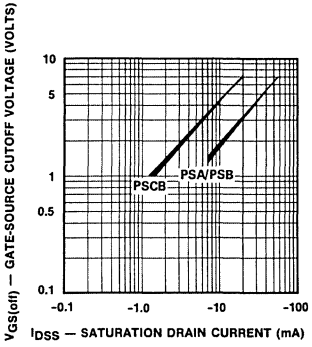


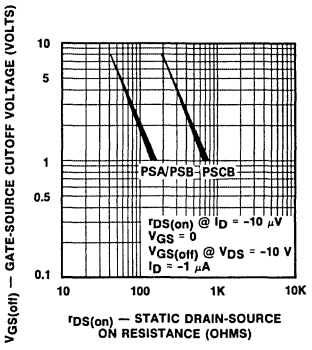


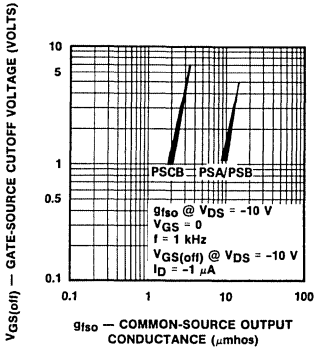


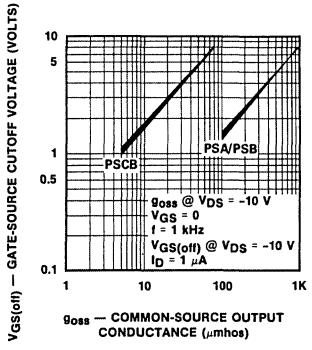
JFET Geometry Selector Guide (Cont'd)

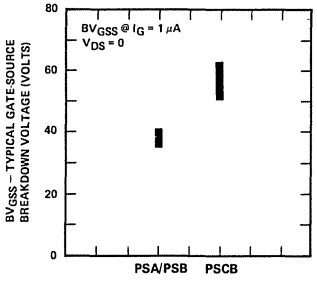
P-Channel JFETs

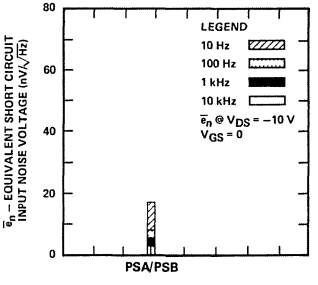


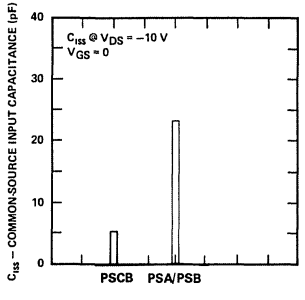


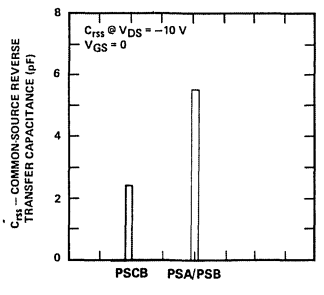












Small-Signal FET Product Specifications

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	LEAKAGE (nA, MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate Ω	RESISTANCE Chnl Ω, Max	GEOMETRY (Section 4)	DEVICE
2N4117	N	72	0 01	–	1.8	40	0 03	0 09	70	210	3	–	–	–	NT	LOW LEAKAGE
2N4117A	N	72	0.001	–	1 8	40	0 03	0 09	70	210	3	–	–	–	NT	
2N4118	N	72	0 01	–	3 0	40	0.08	0 24	80	250	3	–	–	–	NT	
2N4118A	N	72	0.001	–	3 0	40	0.08	0 24	90	250	3	–	–	–	NT	
2N4119	N	72	0 01	–	6.0	40	0 2	0 6	100	330	3	–	–	–	NT	
2N4119A	N	72	0 001	–	6.0	40	0 2	0 6	100	330	3	–	–	–	NT	
PN4117	N	92	0.01		– 40		0 03	0.09	70	210	–	–	–	3K	NT	
PN4117A	N	92	0 001		– 40		0.03	0 09	70	210	–	–	–	3K	NT	
PN4118	N	92	0.01		– 40		0 08	0 24	80	250	–	–	–	3K	NT	
PN4118A	N	92	0.001		– 40		0 08	0 24	80	250	–	–	–	3K	NT	
PN4119	N	92	0 01		– 40		0 2	0.6	100	330	–	–	–	3K	NT	
PN4119A	N	92	0 001		– 40		0.2	0 6	100	330	–	–	–	3K	NT	
PN4120	N	92	–		– 40		0.2	0.6	100	330	–	–	–	3K	NT	
FN4117	N	72	0 005		– 40		0 03	0.09	70	210	–	–	–	3K	NT	
FN4117A	N	72	0.001		2 0	40	0 03	0 2	70	210	3	–	–	–	NT	
FN4118	N	72	0 005		– 40		0.08	0.24	80	250	–	–	–	3K	NT	
FN4118A	N	72	0.001		2 0	40	0 08	0 4	80	250	3	–	–	–	NT	
FN4119	N	72	0.005		– 40		0.2	0.6	100	330	–	–	–	3K	NT	
FN4119A	N	72	0.001		6 0	40	0.2	1.2	100	330	3	–	–	–	NT	
FN4392	N	18	0 1	0.1	40		25	100	–		–	–	60	14	NCB	
FN4393	N	18	0 1	0.1	40		5.0	60	–		–	–	100	14	NCB	
2N4220A	N	72	0 1	–	4 0	30	0 5	3 0	1000	4000	6	2.5	1M		NRL	LOW NOISE
2N4221 A	N	72	0.1	–	6 0	30	2.0	6 0	2000	5000	6	2 5	1M		NRL	
2N4222	N	72	0 1	–	8 0	30	5 0	15	2500	6000	6	2 5	1M		NRL	
2N4338	N	18	0.1	–	1 0	50	0.2	0 6	600	1800	7	1 0	1M		NPA	
2N4339	N	18	0.1	–	1 8	50	0 5	1 5	800	2400	7	1 0	1M		NPA	
2N4340	N	18	0.1	–	3 0	50	1 2	3 6	1300	3000	7	1 0	1M		NPA	
2N4341	N	18	0 1	–	6 0	50	3 0	9 0	2000	4000	7	1 0	1M		NPA	
2N4867	N	72	0.25	–	2 0	40	0 4	1 2	700	2000	25	20	–		NPA	
2N4867A	N	72	0.25	–	2 0	40	0 4	1 2	700	2000	25	10		–	NPA	
2N4868	N	72	0 25	–	3.0	40	1 0	3 0	1000	3000	25	20	–		NPA	
2N4868A	N	72	0.25	–	3 0	40	1 0	3 0	1000	3000	25	10		–	NPA	
2N4869	N	72	0 25	–	5.0	40	2 5	7 5	1300	4000	25	20			NPA	
2N4869A	N	72	0.25	–	5 0	40	2 5	7 5	1300	4000	25	10	–		NPA	
SI1000-(2N6908)	N	72	0.025	–	1 8	30		2.0	100	3000	5	25	–	–	NBA-A	
SI1010-(2N6909)	N	72	0.025	–	2.3	30		3.5	400	3500	5	25	–	–	NBA-A	
SI1020-(2N6910)	N	72	0.025	–	3.5	30		5 0	1200	4000	5	25	–	–	NBA-A	
SI1100-(2N6911)	N	72	0 025	–	2.8	30		–	–	–	–	25	–	–	NBA-B	
J230	N	92	0 25	–	3 0	40	0.7	3 0	1000	2500	–	30	–		NPA	
J230-18	N	92	0 25	–	3 0	40	0 7	3 0	1000	2500	–	30	–		NPA	
J231	N	92	0 25	–	5 0	40	2.0	6 0	1500	3000	–	30			NPA	
J231-18	N	92	0 25	–	5.0	40	2 0	6 0	1500	3000	–	30	–		NPA	
J232	N	92	0 25	–	6 0	40	5.0	10	2500	4000	–	30	–	–	NPA	

Small-Signal FET Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
J232-18	N	92	0.25	–	6.0	40	5.0	10	2500	4000	–	30	–	–	NPA	RF AMPLIFIERS
J270-18	P	92	0.2	–	2.0	30	2.0	15	6000	15000	–	–	–	–	PS-A/B	
2N3819	N	92	2.0	–	8.0	25	2.0	20	2000	6500	8.0	–	–	–	NRL	
2N3823	N	72	0.5	–	8.0	30	4.0	20	3500	6500	6	2.5	1K	–	NRL	
2N4223	N	72	0.25	–	8.0	30	3.0	18	3000	7000	6	5.0	1K	–	NRL	
2N4224	N	72	0.5	–	8.0	30	2.0	20	2000	7500	6	–	–	–	NRL	
2N4416	N	72	0.1	–	6.0	30	5.0	15	4500	7500	4	2.0	1K	–	NH	
2N4416A	N	72	0.1	–	6.0	35	5 0	15	4500	7500	4	2.0	1K	–	NH	
2N5484	N	92	1.0	–	3.0	25	1 0	5.0	3000	6000	5	3.0	1K	–	NH	
2N5485	N	92	1.0	–	4.0	25	4 0	10	3500	7000	5	2.0	1K	–	NH	
2N5486	N	92	1 0	–	6 0	25	8.0	20	4000	8000	5	2 0	1K	–	NH	
2N5668	N	92	2.0	–	4 0	25	1.0	5.0	1500	6500	7	2 5	1K	–	NH	
2N5669	N	92	2.0	–	6 0	25	4.0	10	2000	6500	7	2.5	1K	–	NH	
2N5670	N	92	2.0	–	8.0	25	8 0	20	3000	7500	7 0	2 5	1K	–	NH	
J210	N	92	0.1	–	3 0	25	2.0	15	4000	12000	–	–	–	–	NZF	
J211	N	92	0 1	–	4.5	25	7.0	20	7000	12000	–	–	–	–	NZF	
J212	N	92	0.1	–	6.0	25	15	40	7000	12000	–	–	–	–	NZF	
J270	P	92	0.2	–	2.0	30	2 0	15	6000	15000	–	–	–	–	PS-A/B	
J271	P	92	0 2	–	4 5	30	6 0	50	8000	18000	–	–	–	–	PS-A/B	
J300	N	92	0.5	–	6.0	25	6.0	30	4500	9000	5.5	–	–	–	NZF	
J304	N	92	0.1	–	6.0	30	5.0	15	4500	7500	–	–	–	–	NH	
J305	N	92	0.1	–	3.0	30	1.0	8.0	3000	–	–	–	–	–	NH	
J308	N	92	1.0	–	6 5	25	12	60	8000	20000	7.5	–	–	–	NZB	
J309	N	92	1.0	–	4.0	25	12	30	10000	20000	7.5	–	–	–	NZB	
J310	N	92	1.0	–	6 5	25	24	60	8000	18000	7.5	–	–	–	NZB	
MPF102	N	92	2.0	–	7.5	25	2.0	20	2000	7500	7.0	–	–	–	NH	
MPF108	N	92	1.0	–	8.0	25	1.5	24	2000	7500	6 5	2.5	1M	–	NH	
MPF112	N	92	100	–	10	25	1.0	25	1000	7500	–	–	–	–	NH	
PN4416	N	92	1.0	–	6.0	30	5.0	15	4500	7500	4 0	2 0	1K	–	NH	
U308	N	52	0 15	–	6 0	25	12	60	10000	20000	7.5	–	–	–	NZB	
U309	N	52	0.15	–	4 0	25	12	30	10000	20000	7 5	–	–	–	NZB	
U310	N	52	0.15	–	6.0	25	24	60	10000	18000	7 5	–	–	–	NZB	
U311	N	72	0 15	–	6.0	25	20	60	10000	20000	7 5	–	–	–	NZB	
U312	N	52	0.1	–	6 0	25	10	30	6000	10000	5 0	–	–	–	NZF	

Small-Signal FET Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	LEAKAGE (nA, MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate Ω	RESISTANCE Chnl Ω, Max.	GEOMETRY (Section 4)	DEVICE
2N3824	N	72	0.1	0.1	8.0	50	–	–	–	–	6 0	–	–	250	NRL	SWITCHES & CHOPPERS
2N3970	N	18	0 25	0 25	10	40	50	150	–	–	25	–	–	30	NCB	
2N3971	N	18	0.25	0.25	5.0	40	25	75	–	–	25	–	–	60	NCB	
2N3972	N	18	0 25	0.25	3 0	40	5.0	30	–	–	25	–	–	100	NCB	
2N4091	N	18	0.2	0.2	10	40	30	–	–	–	16	–	–	30	NCB	
2N4092	N	18	0.2	0.2	7.0	40	15	–	–	–	16	–	–	50	NCB	
2N4093	N	18	0 2	0.2	5.0	40	8.0	–	–	–	16	–	–	80	NCB	
2N4391	N	18	0 1	0.1	10	40	50	150	–	–	14	–	–	30	NCB	
2N4392*	N	18	0.1	0.1	5.0	40	25	75	–	–	14	–	–	60	NCB	
2N4393*	N	18	0.1	0.1	3.0	40	5.0	30	–	–	14	–	–	100	NCB	
2N4856	N	18	0.25	0.25	10	40	50	–	–	–	18	–	–	25	NCB	
2N4856A	N	18	0.25	0 25	10	40	50	–	–	–	10	–	–	25	NCB	
2N4857	N	18	0 25	0.25	6.0	40	20	100	–	–	18	–	–	40	NCB	
2N4857A	N	18	0.25	0 25	6.0	40	20	100	–	–	10	–	–	40	NCB	
2N4858	N	18	0.25	0.25	4 0	40	8.0	80	–	–	18	–	–	60	NCB	
2N4858A	N	18	0.25	0.25	4.0	40	8.0	80	–	–	10	–	–	60	NCB	
2N4859	N	18	0.25	0.25	10	30	50	–	–	–	18	–	–	25	NCB	
2N4859A	N	18	0.25	0.25	10	30	50	–	–	–	10	–	–	25	NCB	
2N4860	N	18	0.25	0.25	6.0	30	20	100	–	–	18	–	–	40	NCB	
2N4860A	N	18	0.25	0.25	6.0	30	20	100	–	–	10	–	–	40	NCB	
2N4861	N	18	0.25	0.25	4.0	30	8.0	80	–	–	18	–	–	60	NCB	
2N4861A	N	18	0.25	0.25	4.0	30	8.0	80	–	–	10	–	–	60	NCB	
2N5018	P	18	2.0	10.0	10	30	10	–	–	–	45	–	–	75	PS-A/B	
2N5019	P	18	2.0	10.0	5.0	30	5.0	–	–	–	45	–	–	150	PS-A/B	
2N5114	P	18	0.5	0.5	10	30	30	90	–	–	25	–	–	75	PS-A/B	
2N5115	P	18	0.5	0 5	6.0	30	15	60	–	–	25	–	–	100	PS-A/B	
2N5116	P	18	0.5	0.5	4.0	30	5.0	25	–	–	27	–	–	150	PS-A/B	
2N5432	N	52	0.2	0.2	10	25	150	–	–	–	30	–	–	5.0	NIP	
2N5433	N	52	0.2	0.2	9.0	25	100	–	–	–	30	–	–	7.0	NIP	
2N5434	N	52	0.2	0.2	4 0	25	30	–	–	–	30	–	–	10	NIP	
2N5638	N	92	1.0	1.0	12	30	50	–	–	–	10	–	–	30	NCB	
2N5639	N	92	1.0	1.0	8.0	30	25	–	–	–	10	–	–	60	NCB	

*FN4392 and FN4393 available

Small-Signal FET Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		DEVICE	GEOMETRY (Section 4)
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
2N5640	N	92	1.0	1.0	6.0	30	5.0	–	–	–	10	–	–	100	SWITCHES & CHOPPERS	NCB
J105	N	92	3.0	3.0	10.0	25	500	–	–	–	–	–	–	3 0		NVA
J105-18	N	92	3.0	3.0	10	25	500	–	–	–	–	–	–	3.0		NVA
J106	N	92	3 0	3.0	6.0	25	200	–	–	–	–	–	–	6 0		NVA
J106-18	N	92	3.0	3.0	6.0	25	200	–	–	–	–	–	–	6.0		NVA
J107	N	92	3.0	3.0	4.5	25	100	–	–	–	–	–	–	8.0		NVA
J107-18	N	92	3.0	3.0	4 5	25	100	–	–	–	–	–	–	8 0		NVA
J108	N	92	3.0	3.0	10	25	80	–	–	–	–	–	–	8 0		NIP
J108-18	N	92	3.0	3.0	10	25	80	–	–	–	–	–	–	8.0		NIP
J109	N	92	3.0	3.0	6.0	25	40	–	–	–	–	–	–	12		NIP
J109-18	N	92	3.0	3.0	6.0	25	40	–	–	–	–	–	–	12		NIP
J110	N	92	3.0	3.0	4.0	25	10	–	–	–	–	–	–	18		NIP
J110-18	N	92	3.0	3.0	4.0	25	10	–	–	–	–	–	–	18		NIP
J111	N	92	1.0	1.0	10	35	20	–	–	–	–	–	–	30		NCB
J111-18	N	92	1.0	1.0	10	35	20	–	–	–	–	–	–	30		NCB
J112	N	92	1.0	1.0	5.0	35	5.0	–	–	–	–	–	–	50		NCB
J112-18	N	92	1 0	1.0	5.0	35	5.0	–	–	–	–	–	–	50		NCB
J113	N	92	1 0	1.0	3.0	35	2 0	–	–	–	–	–	–	100		NCB
J113-18	N	92	1.0	1.0	3.0	35	2.0	–	–	–	–	–	–	100		NCB
J174	P	92	1.0	1.0	10	30	20	100	–	–	–	–	–	85		PS-A/B
J174-18	P	92	1.0	1.0	10	30	20	100	–	–	–	–	–	85		PS-A/B
J175	P	92	1.0	1.0	6.0	30	7.0	60	–	–	–	–	–	125		PS-A/B
J175-18	P	92	1.0	1.0	6.0	30	7.0	60	–	–	–	–	–	125		PS-A/B
J176	P	92	1.0	1.0	4.0	30	2.0	25	–	–	–	–	–	250		PS-A/B
J176-18	P	92	1.0	1.0	4.0	30	2.0	25	–	–	–	–	–	250		PS-A/B
J177	P	92	1.0	1.0	2.25	30	1.5	20	–	–	–	–	–	300		PS-A/B
J177-18	P	92	1.0	1.0	2.25	30	1.5	20	–	–	–	–	–	300		PS-A/B
P1086	P	92	2.0	10.0	10	30	10	–	–	–	45	–	–	75		PS-A/B
P1086-18	P	92	2.0	10.0	10	30	10	–	–	–	45	–	–	75		PS-A/B
P1087	P	92	2 0	10 0	5 0	30	5 0	–	–	–	45	–	–	150		PS-A/B
P1087-18	P	92	2 0	10 0	5 0	30	5 0	–	–	–	45	–	–	150		PS-A/B
PN4391	N	92	1.0	1.0	10	40	50	150	–	–	14	–	–	30		NCB
PN4391-18	N	92	1.0	1 0	10	40	50	150	–	–	14	–	–	30		NCB
PN4392	N	92	1.0	1.0	5 0	40	25	100	–	–	14	–	–	60		NCB
PN4392-18	N	92	1 0	1 0	5 0	40	25	100	–	–	14	–	–	60		NCB
PN4393	N	92	1.0	1.0	3 0	40	5 0	60	–	–	14	–	–	100		NCB
PN4393-18	N	92	1 0	1.0	3.0	40	5 0	60	–	–	14	–	–	100		NCB

Small-Signal FET Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
SD210	N	72	100	100	2.0	30	10	—	—	—	5.5	—	—	70	DMCB-B	SWITCHES & CHOPPERS
SD211	N	72	100	100	2.0	30	10	—	—	—	5.5	—	—	70	DMCB-A	
SD212	N	72	100	100	2.0	10	10	—	—	—	5.5	—	—	70	DMCB-B	
SD213	N	72	100	100	2.0	10	10	—	—	—	5.5	—	—	70	DMCB-A	
SD214	N	72	100	100	2.0	20	10	—	—	—	5.5	—	—	70	DMCB-B	
SD215	N	72	100	100	2.0	20	10	—	—	—	5.5	—	—	70	DMCB-A	
U200	N	18	1.0	1.0	3.0	30	3.0	25	—	—	30	—	—	150	NCB	
U201	N	18	1.0	1.0	5.0	30	15	75	—	—	30	—	—	75	NCB	
U202	N	18	1.0	1.0	10	30	30	150	—	—	30	—	—	50	NCB	
U290	N	52	1.0	1.0	10	30	500	—	—	—	60	—	—	2 5	NVA	
U291	N	52	1.0	1.0	4.5	30	200	—	—	—	60	—	—	7.0	NVA	
U304	P	18	0.5	0.5	10	30	30	90	—	—	27	—	—	85	PS-A/B	
U305	P	18	0.5	0.5	6.0	30	15	60	—	—	27	—	—	110	PS-A/B	
U306	P	18	0.5	0.5	4.0	30	5.0	25	—	—	27	—	—	175	PS-A/B	
U1897	N	92	0.4	0.2	10	40	30	—	—	—	16	—	—	30	NCB	
U1897-18	N	92	0.4	0.2	10	40	30	—	—	—	16	—	—	30	NCB	
U1898	N	92	0.4	0.2	7.0	40	15	—	—	—	16	—	—	50	NCB	
U1898-18	N	92	0.4	0.2	7.0	40	15	—	—	—	16	—	—	50	NCB	
U1899	N	92	0.4	0.2	5.0	40	8.0	—	—	—	16	—	—	80	NCB	
U1899-18	N	92	0.4	0.2	5.0	40	8.0	—	—	—	16	—	—	80	NCB	

Small-Signal FET Specifications (Cont'd)

N & P-Channel Single FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
2N3821	N	72	0.1	–	4 0	50	0.5	2 5	1500	4500	6	200	–	–	NRL	GENERAL PURPOSE
2N3822	N	72	0.1	–	6.0	50	2 0	10	3000	6500	6	200	–	–	NRL	
2N4220	N	72	0.1	–	4 0	30	0.5	3.0	1000	4000	6	–	–	–	NRL	
2N4221	N	72	0.1	–	6.0	30	2.0	6 0	2000	5000	6	–	–	–	NRL	
2N4222	N	72	0.1	–	8.0	30	5.0	15	2500	6000	6	–	–	–	NRL	
2N5457	N	92	1.0	–	6.0	25	1.0	5 0	1000	5000	7	3.0	1M	–	NRL	
2N5458	N	92	1 0	–	7 0	25	2 0	9 0	1500	5500	7	3.0	1M	–	NRL	
2N5459	N	92	1.0	–	8.0	25	4 0	16	2000	6000	7	3.0	100M	–	NRL	
J201	N	92	0 1	–	1 5	40	0 2	1.0	500	–	5 0	–	–	–	NPA	
J201-18	N	92	0.1	–	1 5	40	0 2	1 00	500	–	5 0	–	–	–	NPA	
J202	N	92	0 1	–	4 0	40	0 9	4.5	1000	–	5 0	–	–	–	NPA	
J202-18	N	92	0 1	–	4.0	40	0.9	4 5	1000	–	5.0	–	–	–	NPA	
J203	N	92	0 1	–	10	40	4 0	20	1500	–	5 0	–	–	–	NPA	
J203-18	N	92	0.1	–	10	40	4.0	20	1500	–	5 0	–	–	–	NPA	
J204	N	92	0.1	–	2 0	25	1.2	3.0	–	–	5 0	–	–	–	NPA	
J204-18	N	92	0.1	–	2.0	25	1.2	3.0	–	–	5 0	–	–	–	NPA	
J270	P	92	0 2	–	4 5	30	6.0	50	8000	18000	–	–	–	–	PS-A/B	
J271-18	P	92	0 2	–	4 5	30	6 0	50	8000	18000	–	–	–	–	PS-A/B	
MPF109	N	92	1.0	–	8.0	25	0 5	24	800	6000	7 0	2 5	1M	–	NRL	
MPF111	N	92	100	–	10	20	0.5	20	500	–	–	–	–	–	NRL	
PN4302	N	92	1 0	–	4.0	30	0.5	5.0	1000	–	6	2.0	1M	–	NPA	
PN4302-18	N	92	1.0	–	4.0	30	0 5	5 0	1000	–	6 0	2.0	1M	–	NPA	
PN4303	N	92	1 0	–	6.0	30	4.0	10	2000	–	6	2 0	1M	–	NPA	
PN4303-18	N	92	1.0	–	6 0	30	4 0	10	2000	–	6 0	2.0	1M	–	NPA	
PN4304	N	92	1.0	–	10.0	30	0 5	15	1000	–	6	3 0	1M	–	NPA	
PN4304-18	N	92	1.0	–	10	30	0 5	15	1000	–	6.0	2 0	1M	–	NPA	
PN5163	N	92	10	–	8.0	25	1 0	40.0	2000	9000	20	50.0	–	–	–	

Small-Signal FET Specifications (Cont'd)

N-Channel Dual FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking μV/ C	OUTPUT CONDUCTANCE gos (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
2N5196	N	71	0 025	4 0	50	0 7	7 0	1000	—	6 0	20	5 0	5 0	50	NQP	LOW LEAKAGE
2N5197	N	71	0 025	4 0	50	0 7	7 0	1000	—	6 0	20	5 0	10	50	NQP	
2N5198	N	71	0.025	4.0	50	0.7	7 0	1000	—	6 0	20	10	20	50	NQP	
2N5199	N	71	0.025	4.0	50	0.7	7.0	1000	—	6 0	20	15	40	50	NQP	
2N5545	N	71	0 1	4.5	50	0 5	8.0	1500	—	6.0	200	5 0	10	25	NQP	
2N5546	N	71	0 1	4.5	50	0 5	8.0	1500	—	6 0	200	10	20	25	NQP	
2N5547	N	71	0 1	4 5	50	0 5	8 0	1500	—	6 0	200	15	40	25	NQP	
2N6905	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	5	10	—	NNR	
2N6906	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	15	25	—	NNR	
2N6907	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	25	50	—	NNR	
U401	N	71	0 025	2 5	50	0 5	10	2000	—	8 0	20	5 0	10	2 0	NNR	
U402	N	71	0 025	2.5	50	0 5	10	2000	—	8 0	20	10	10	2.0	NNR	
U403	N	71	0 025	2.5	50	0 5	10	2000	—	8 0	20	10	25	2 0	NNR	
U404	N	71	0 025	2.5	50	0 5	10	2000	—	8 0	20	15	25	2 0	NNR	
U405	N	71	0 025	2.5	50	0 5	10	2000	—	8 0	20	20	40	2 0	NNR	
U406	N	71	0.025	2.5	50	0 5	10	2000	—	8 0	20	40	80	2 0	NNR	
U421	N	78	0 001	2.0	40	0 06	1 0	300	1500	3 0	10	10	10	0 5	NNT	
U422	N	78	0 001	2.0	40	0 06	1 0	300	1500	3 0	10	15	25	0 5	NNT	
U423	N	78	0 001	2.0	40	0 06	1 0	300	1500	3 0	10	25	40	0 5	NNT	
U424	N	78	0 003	3 0	40	0 06	1 8	300	1500	3 0	10	10	10	1 0	NNT	
U425	N	78	0 003	3 0	40	0 06	1 8	300	1500	3 0	10	15	25	1 0	NNT	
U426	N	78	0 003	3 0	40	0 06	1 8	300	1500	3 0	10	25	40	1 0	NNT	
U427	N	78	0.005	2 0	40	0 06	1 8	250	—	3.0	—	25	40	3 0	NNT	
U428	N	78	0.005	3 0	40	0 06	1.8	250	—	3 0	—	40	80	5 0	NNT	
2N5515	N	71	0 25	4 0	40	0 5	7 5	1000	—	25	30	5 0	5 0	1 0	NQP	LOW NOISE
2N5516	N	71	0.25	4 0	40	0 5	7 5	1000	—	25	30	5 0	10	1 0	NQP	
2N5517	N	71	0.25	4 0	40	0 5	7 5	1000	—	25	30	10	20	1 0	NQP	
2N5518	N	71	0.25	4 0	40	0 5	7 5	1000	—	25	30	15	40	1 0	NQP	
2N5519	N	71	0 25	4.0	40	0 5	7 5	1000	—	25	30	15	80	1 0	NQP	
2N5520	N	71	0 25	4 0	40	0 5	7 5	1000	—	25	15	5 0	5 0	1 0	NQP	
2N5521	N	71	0.25	4 0	40	0 5	7 5	1000	—	25	15	5 0	10	1 0	NQP	
2N5522	N	71	0.25	4 0	40	0 5	7 5	1000	—	25	15	10	20	1 0	NQP	
2N5523	N	71	0.25	4 0	40	0.5	7.5	1000	—	25	15	15	40	1 0	NQP	
2N5524	N	71	0 25	4.0	40	0.5	7 5	1000	—	25	15	15	80	1 0	NQP	
2N6905	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	5	10	—	NNR	
2N6906	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	10	25	—	NNR	
2N6907	N	71	0.015	2.5	35	0.5	10	2000	—	8.0	15	25	50	—	NNR	
U401	N	71	0.025	2 5	50	0 5	10	2000	—	8.0	20	5.0	10	2 0	NNR	
U402	N	71	0.025	2 5	50	0 5	10	2000	—	8.0	20	10	10	2 0	NNR	

Small-Signal FET Specifications (Cont'd)

N-Channel Dual FETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking μV/°C	OUTPUT CONDUCTANCE gos (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
U404	N	71	0.025	2.5	50	0.5	10	2000	–	8 0	20	15	25	2 0	NNR	LOW NOISE
U405	N N	71	0.025	2.5	50	0 5	10	2000	–	8.0	20	20	40	2 0	NNR	
U406	N	71	0.025	2.5	50	0 5	10	2000	–	8 0	20	40	80	2 0	NNR	
2N5564	N	71	0.1	3.0	40	5 0	30	7500	–	12	50	5 0	10	45	NCB	RF AMPLIFIER
2N5565	N	71	0.1	3.0	40	5 0	30	7500	–	12	50	10	25	45	NCB	
2N5566	N	71	0 1	3.0	40	5 0	30	7500	–	12	50	20	50	45	NCB	
2N5911	N	78	0.1	5 0	25	7 0	40	5000	–	3 0	20	10	20	100	NZF-D	
2N5912	N	78	0.1	5.0	25	7.0	40	5000	–	3 0	20	15	40	100	NZF-D	
U257	N	78	0.1	5 0	25	5 0	40	5000	–	5 0	30	100	–	150	NZF-D	
U430	N	99	0.15	4 0	25	12	30	10000	–	7 5	12	-	–	150	NZA-D	
U431	N	99	0.15	6.0	25	24	60	10000	–	7.5	10	–	–	150	NZA-D	
U440	N	71	0 50	6.0	25	6.0	30	4500	–	3 5	–	10	–	200	NZF-D	
U441	N	71	0.50	6 0	25	6 0	30	4500	–	3 5	–	20	–	200	NZF-D	
U443	N	78	5	6	25	6 0	30	4500	9000	3 5	–	10	–	200	NZF-D	
U444	N	78	.5	6	25	6 0	30	4500	9000	3.5	–	20	–	200	NZF-D	
2N3921	N	71	1.0	3.0	50	1 0	10	1500	–	18	2.0	5 0	10	35	NNR	GENERAL PURPOSE
2N3922	N	71	1.0	3 0	50	1.0	10	1500	–	18	2 0	5 0	25	35	NNR	
2N3954	N	71	0 1	4 5	50	0.5	5 0	1000	–	4.0	0.5	5 0	10	35	NQP	
2N3954A	N	71	0 1	4.5	50	0 5	5 0	1000	–	4.0	0.5	5 0	5 0	35	NQP	
2N3955	N	71	0.1	4 5	50	0 5	5.0	1000	–	4.0	0 5	10	25	35	NQP	
2N3955A	N	71	0 1	4 5	50	0 5	5 0	1000	–	4.0	0 5	10	15	35	NQP	
2N3956	N	71	0 1	4 5	50	0 5	5.0	1000	–	4 0	0 5	15	50	35	NQP	
2N3957	N	71	0 1	4 5	50	0.5	5.0	1000	–	4 0	0 5	20	75	35	NQP	
2N3958	N	71	0.1	4.5	50	0.5	5 0	1000	–	4 0	0 5	25	100	35	NQP	
2N5045	N	71	0.25	4 5	50	0.5	8 0	1500	–	8 0	200	5 0	67	25	NQP	
2N5046	N	71	0 25	4 5	50	0 5	8 0	1500	–	8.0	200	10	133	25	NQP	
2N5047	N	71	0.25	4.5	50	0 5	8.0	1500	–	8 0	200	15	200	25	NQP	
2N5452	N	71	0 1	4.5	50	0.5	5 0	1000	–	4.0	20	5 0	5 0	1.0	NQP	
2N5453	N	71	0.1	4 5	50	0 5	5.0	1000	–	4 0	20	10	10	1 0	NQP	
2N5454	N	71	0 1	4.5	50	0.5	5.0	1000	–	4.0	20	15	25	1.0	NQP	
DN5564	N	71	1	3 0	40	5	50	7500	12500	12	50	5	10	65	NCB-D	
DN5565	N	71	1	3 0	40	5	50	7500	12500	12	50	10	25	65	NCB-D	
DN5566	N	71	1	3 0	40	5	50	7500	12500	12	50	20	50	65	NCB-D	
U231	N	71	0 1	4 5	50	0 5	5.0	1000	–	6 0	80	5 0	:0	35	NQP	
U232	N	71	0 1	4 5	50	0 5	5.0	1000	–	6.0	80	10	25	35	NQP	
U233	N	71	0.1	4 5	50	0 5	5.0	1000	–	6 0	80	15	50	35	NQP	
U234	N	71	0 1	4 5	50	0.5	5 0	1000	–	6.0	80	20	75	35	NQP	
U235	N	71	0.1	4 5	50	0.5	5.0	1000	–	6 0	80	25	100	35	NQP	
U410	N	71	0.2	3 5	40	0.5	6 0	1000	–	–	13	10	10	20	NQP	
U411	N	71	0 2	3 5	40	0 5	6.0	1000	–	–	13	20	25	20	NQP	
U412	N	71	0 2	3 5	40	0.5	6 0	1000	–	–	13	40	80	20	NQP	
DN5567	N	71	0 1	3 0	–40	5	60	–	–	7.0	–	20	–	–	NCB-D	SWITCH

Product Specifications (Cont'd)

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts)		Forward Voltage Drop Volts (Max.)	Capacitance (pF, Max.)
				Min.	Max.		
DPAD1	78	Dual	1	45	120	1.5	0 8
DPAD2	71	Dual	2	45	120	1.5	0.8
DPAD5	71	Dual	5	45	120	1.5	0.8
DPAD10	71	Dual	10	35	–	1 5	2.0
DPAD20	71	Dual	20	35	–	1.5	2.0
DPAD50	71	Dual	50	35	–	1.5	2.0
DPAD100	71	Dual	100	35	–	1.5	2.0
JPAD5	92	Single	5	35	–	1.5	2.0
JPAD10	92	Single	10	35	–	1.5	2.0
JPAD20	92	Single	20	35	–	1.5	2 0
JPAD50	92	Single	20	35	–	1 5	2 0
JPAD100	92	Single	50	35	–	1 5	2.0
JPAD200	92	Single	100	35	–	1 5	2 0
JPAD500	92	Single	500	35	–	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1 5	0 8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	–	1 5	2.0
PAD20	18	Single	20	35	–	1 5	2 0
PAD50	18	Single	50	35	–	1.5	2.0
PAD100	18	Single	100	35	–	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts)		Resistance (Channel Ω)		Geometry
				Min.	Max.	Min.	Max.	
VCR2N	N	18	15	3.5	7 0	20	60	NCB
VCR3P	P	72	15	3.5	7.0	70	200	PS-A/B
VCR4N	N	18	15	3.5	7.0	200	600	NPA
VCR5P	P	72	15	3.5	7 0	300	900	PS-A/B
VCR7N	N	72	15	2.5	5 0	4000	8000	NT

P-Channel MOSFETs

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω, Max.)	Leakage Channel On (mA)		Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
					Min.	Max.					
3N163	72	ENH	5.0	250	5.0	30	–	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	–	30	2.5	0.7	MRA
MFE823	18	ENH	6.0	–	3 0	–	20	25	6.0	1.5	MRA

Product Specifications (Cont'd)

Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (MΩ, Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0 22	10	1 00	100	13	–	NKL
CR024	18	0 24	10	1 00	100	10	–	NKL
CR027	18	0 27	10	1 00	100	9 0	–	NKL
CR030	18	0 30	10	1 00	100	8 0	–	NKL
CR033	18	0 33	10	1 00	100	6.6	-	NKL
CR039	18	0 39	10	1 05	100	4 1	-	NKL
CR043	18	0 43	10	1 05	100	3.3	–	NKL
CR047	18	0 47	10	1 10	100	2 7	–	NKL
CR056	18	0 56	10	1 20	100	1 9	–	NKL
CR062	18	0 62	10	1.30	100	1 55	–	NKL
CR068	18	0 68	10	1 15	100	1 35	--	NKM
CR075	18	0 75	10	1 20	100	1 15	–	NKM
CR082	18	0 82	10	1 25	100	1 00	-	NKM
CR091	18	0 91	10	1 29	100	0 88	-	NKM
CR100	18	1 00	10	1 35	100	0 80	-	NKM
CR110	18	1 10	10	1 40	100	0 70	–	NKM
CR120	18	1 20	10	1 45	100	0 64	-	NKM
CR130	18	1 30	10	1.50	100	0 58		NKM
CR140	18	1 40	10	1 55	100	0 54	--	NKM
CR150	18	1 50	10	1 60	100	0 51	–	NKM
CR160	18	1 60	10	1 65	100	0 475	-	NKO
CR180	18	1 80	10	1 75	100	0 42	--	NKO
CR200	18	2 00	10	1 85	100	0 395		NKO
CR220	18	2 20	10	1 95	100	0 37		NKO
CR240	18	2 40	10	2 00	100	0.345	–	NKO
CR270	18	2 70	10	2 15	100	0 32	–	NKO
CR300	18	3 00	10	2 25	100	0 30	-	NKO
CR330	18	3 30	10	2 35	100	0.28	-	NKO
CR360	18	3 60	10	2 50	100	0 265	-	NKO
CR390	18	3.90	10	2 60	100	0 255	-	NKO
CR430	18	4 30	10	2 75	100	0 245	-	NKO
CR470	18	4 70	10	2 90	100	0 235	-	NKO
CR530	18	5.30	10	3.10	100	0.20	–	NKO
CRR0240	18	.24	25	1.0	100	.9	–	NKL
CRR0360	18	.36	25	1 05	100	4 1	–	NKL
CRR0560	18	.56	25	1 30	100	1.15	–	NKL
CRR0800	18	80	25	1 35	100	0 8	–	NKL
CRR1250	18	1 95	25	1 60	100	.54	–	NKM
CRR1950	18	1 95	25	1 95	100	.37	–	NKM
CRR2900	18	2 90	25	2 35	100	.28	–	NKO
CRR4300	18	4 30	25	3 00	100	0 5	--	NKO
J500	92	0 24	20	1 20	50	5.0	2	NCL
J501	92	0.33	20	1 30	50	3 0	2	NCL
J502	92	0 43	20	1 50	50	2 0	2	NCL
J503	92	0.56	20	1 70	50	1 4	2	NCL
J504	92	0 75	20	1 90	50	1.0	2	NCL
J505	92	1.00	20	2 10	50	0 6	2	NCL
J506	92	1 40	20	2 50	50	0 4	2	NCL
J507	92	1.80	20	2.80	50	0 25	2	NCL
J508	92	2 40	20	3 10	50	0 25	2	NCL
J509	92	3.00	20	3 50	50	0 20	2	NCL
J510	92	3 60	20	3 90	50	0 20	2	NCL
J511	92	4.70	20	4 20	50	0.15	2	NCL
J552	92	0.05	50	1 5	50	2 0	2	NKL
J553	92	(18 - 0 75)	–	75	50	10	–	NCL
J554	92	(06 -1.6)	–	75	50	1 0	–	NCL
J555	92	(1.4 - 2.6)	–	.75	50	88	–	NCL
J556	92	(2 4 - 3 8)	–	.75	50	.6	–	NCL
J557	92	(3 6 - 5.3)	–	1 5	50	.48	–	NCL
J9100	92	0.05	50	1.5	50	2 0	2	NCL
JR135V	92	0.200	–	0 9	135	2.0	–	VRMA
JR170V	92	0.200	–	0.9	170	2.0	–	VRMA
JR200V	92	0.200	–	0.9	200	2.0	–	VRMA
JR220V	92	0.200	–	0.9	220	2.0	–	VRMA
JR240V	92	0.200	–	0.9	240	2.0	–	VRMA

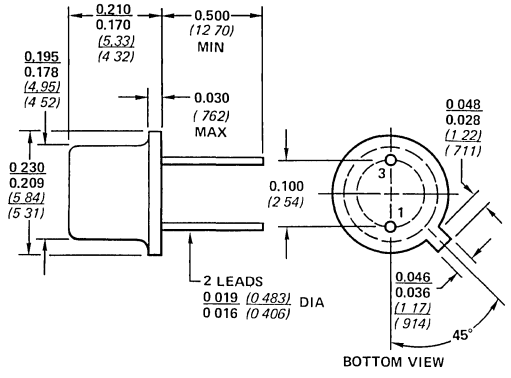
5

Package Data

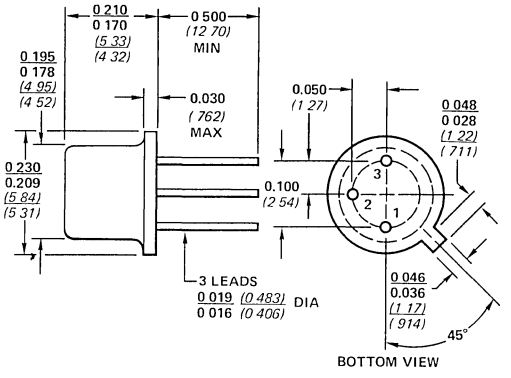
6

Package Data At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.

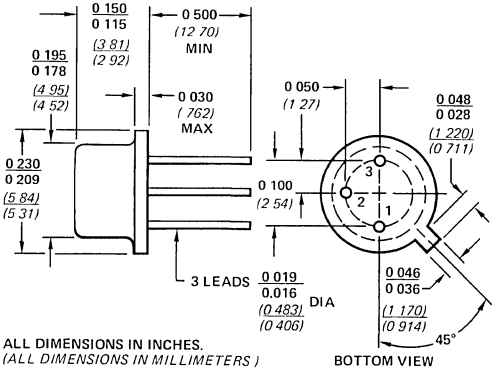
Siliconix



TO-18
(2 PIN)

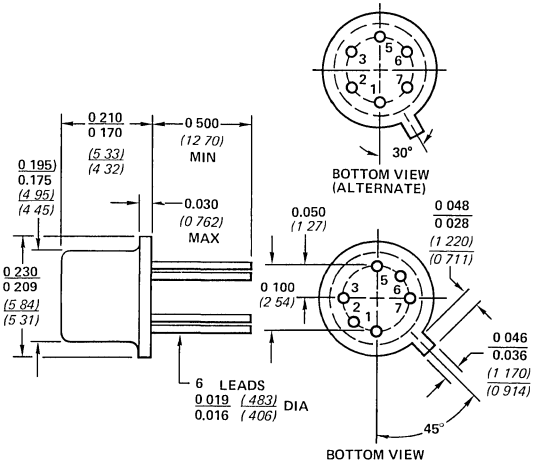


TO-18
(3 PIN)



ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS)

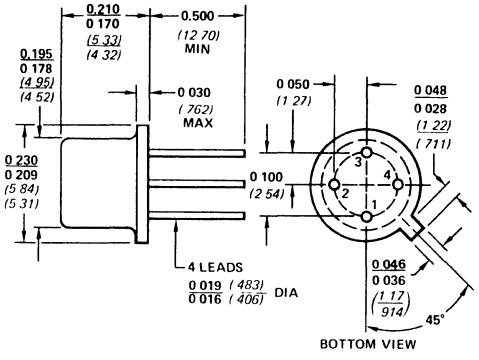
TO-52



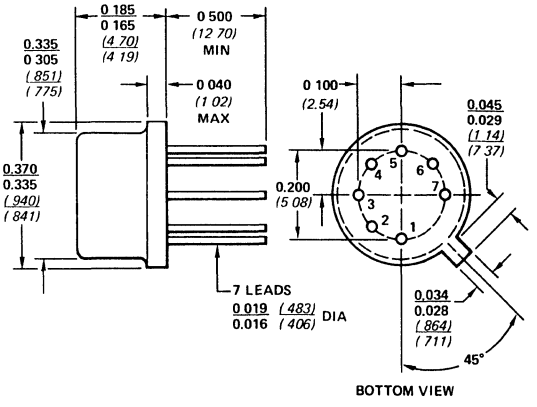
TO-71

Package Data (Cont'd)

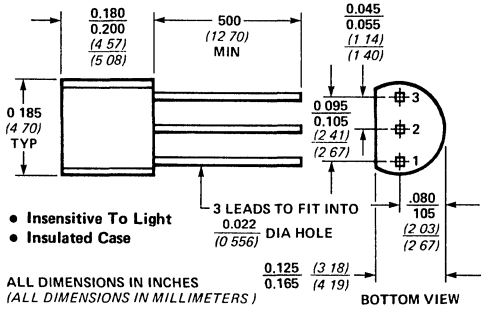
At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.



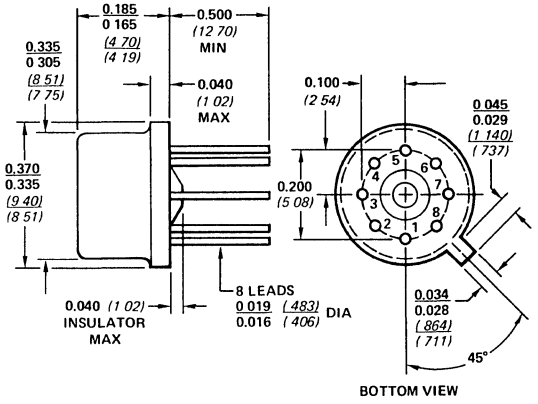
TO-72



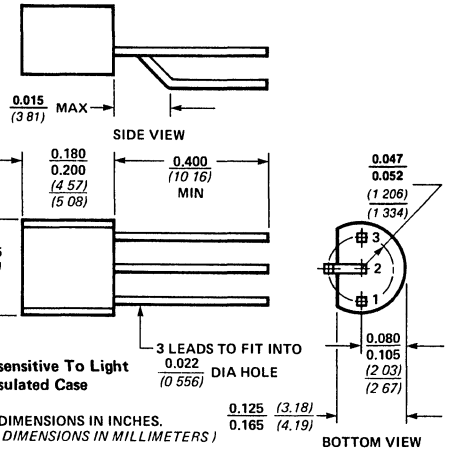
TO-78



TO-92

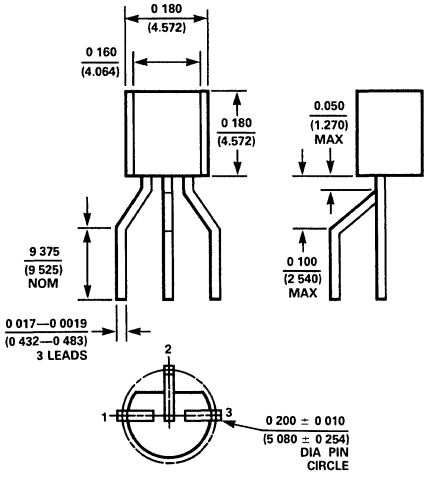


TO-99



TO-92 LEAD FORM (–18)

Order number (-18) suffix to standard part type

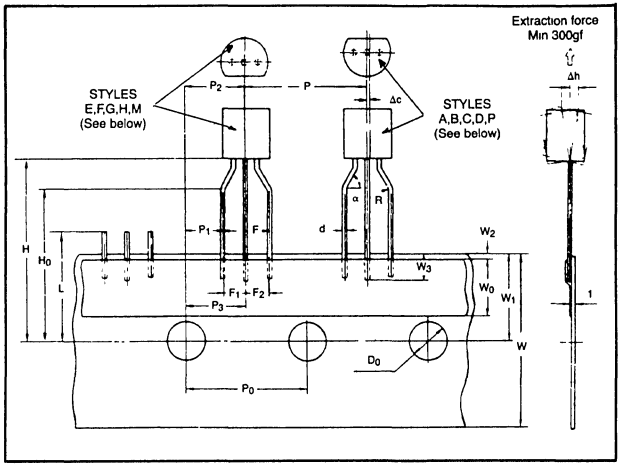


TO-92 Device to TO-5 Pin Circle

Order number (-05) suffix to standard part type

Package Data (Cont'd) At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.

TO-92 TAPING SPECIFICATIONS AND WINDING STYLES

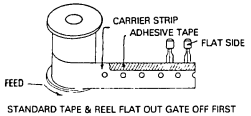


P	12.7±0.5	H_0	16±0.5
P_0	12.7±0.2	F	$5^{+0.8}_{-0.2}$
P_1	3.85±0.5	$F_1 - F_2$	±0.3
P_2	6.35±0.5	D_0	4±0.2
P_3	6.35	t	0.7±0.2
W	$18^{+1.0}_{-0.5}$	Δh	0±1
W_0	6±1	d	$0.50^{+0.06}_{-0.05}$ dia.
W_1	9±0.5	R	0.8
W_2	Max. 0.5	α	45°-60°
W_3	Min. 4.5	L	Max. 11
H	19.5±0.5	Δc	0±0.5

All dimensions in millimeters.

OPTION 1

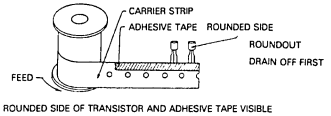
STYLE E IS A PREFERRED STYLE



STANDARD TAPE & REEL FLAT OUT GATE OFF FIRST

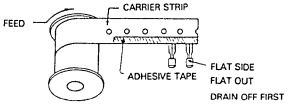
OPTION 3

STYLE A IS PREFERRED



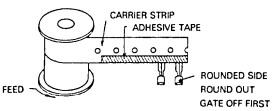
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

OPTION 2



FLAT SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

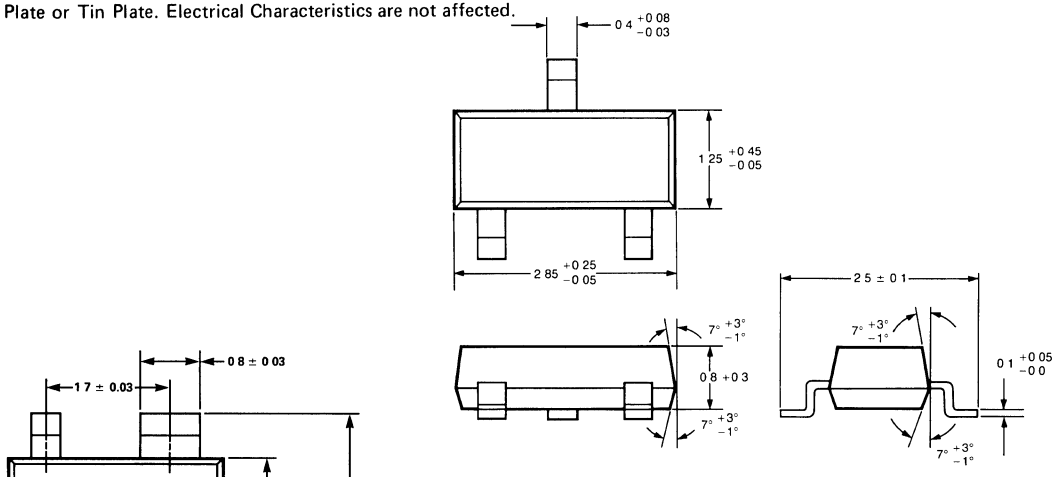
OPTION 4



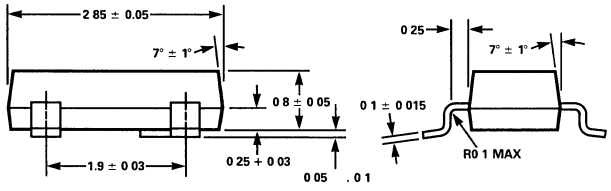
ROUNDED SIDE OF TRANSISTOR AND ADHESIVE TAPE VISIBLE

Note: Order information—TRX = option (Standard Si option = Option 1) If not designated option 1 will be chosen. Tape and ammopack available—contact factory.

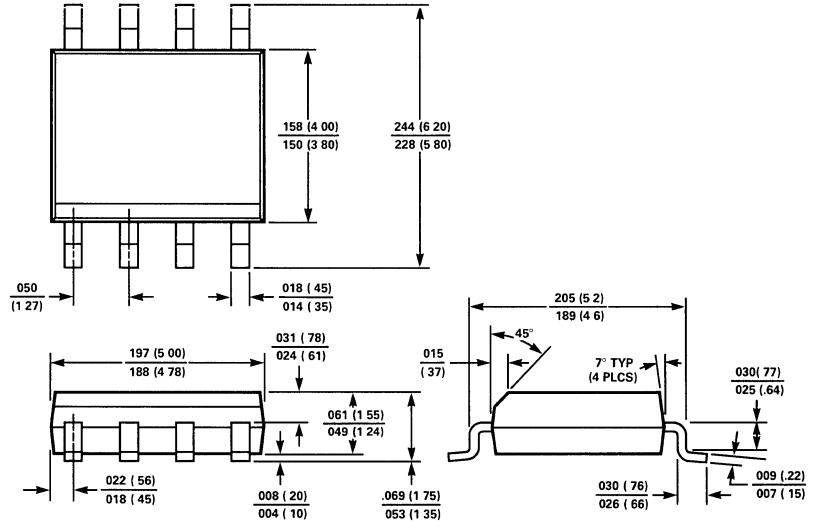
Package Data (Cont'd) At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.



SOT-23

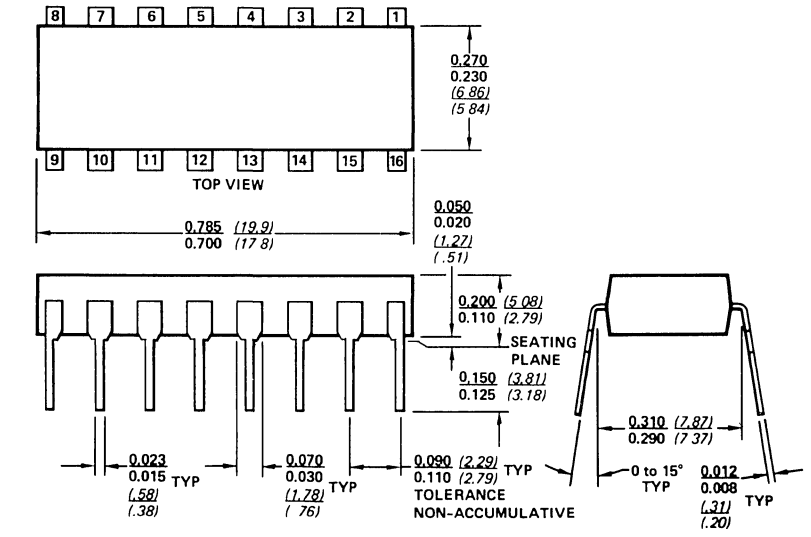


SOT-143

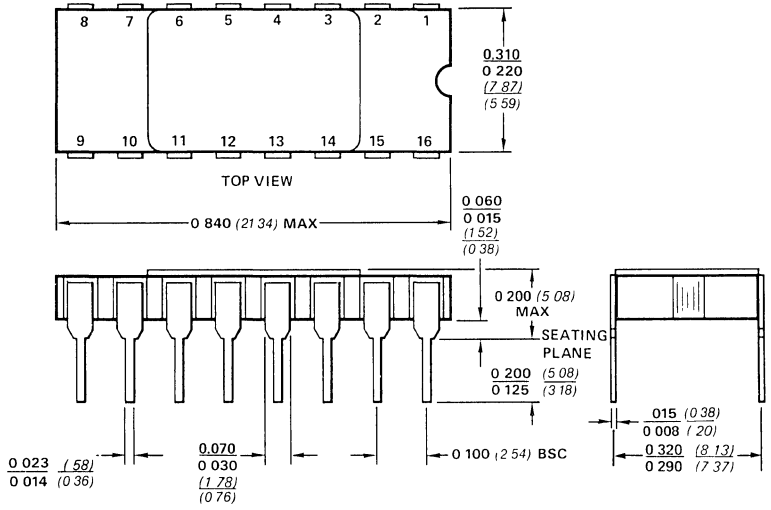


SOIC-8 PIN

Package Data (Cont'd) At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.

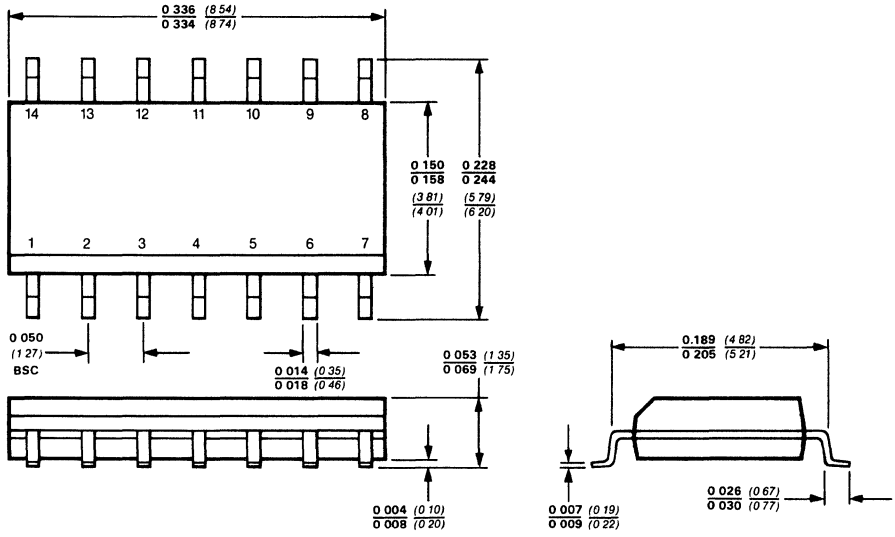


16 LEAD DUAL IN LINE PACKAGE
(PLASTIC)



16 LEAD DUAL IN LINE PACKAGE
(SIDE BRAZE)

Package Data (Cont'd) At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.



14 LEAD SO (Y)
(PLASTIC)

Application Notes

7

An Introduction to FETs

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilenfeld's patent of 1925. The theoretical description of a FET made by Schockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

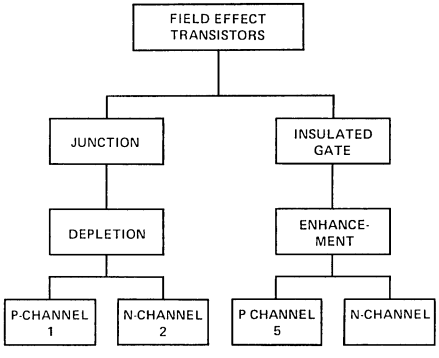
Amplifiers	*Switches*	*Current Limiters*
Small Signal	Chopper-type	*Voltage-Controlled*
Low Distortion	Analog Gate	*Resistors*
High Gain	Commutator	*Mixers*
Low Noise		*Oscillators*
Selective		
D.C.		
High-Frequency		

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics – which are very different from those of bipolar devices – can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits.

In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils; this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.



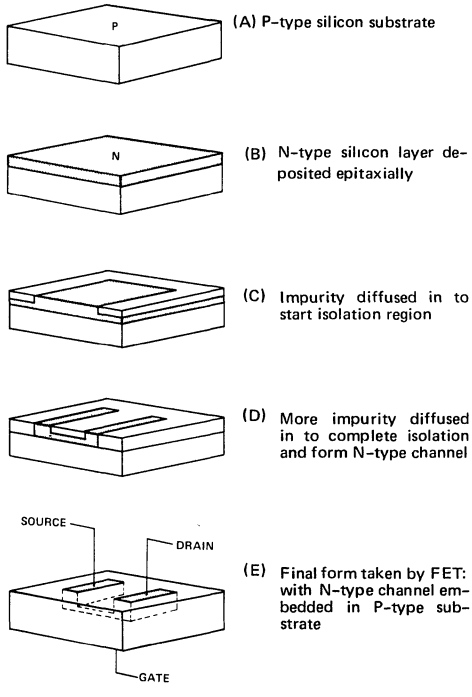
FET Family Tree
Figure 1

7

Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.



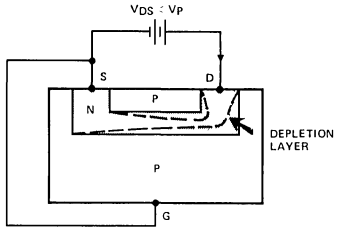
Idealized Manufacture of an N-Channel Junction FET
Figure 2

In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

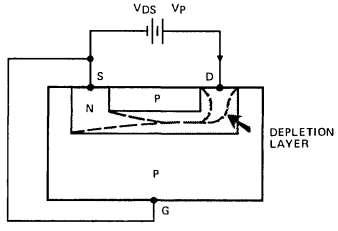
(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

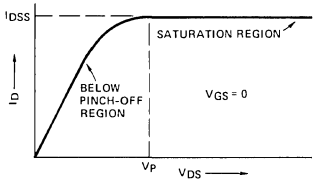
Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be *pinched off*. The physical meaning of this term leads to one definition of *pinch-off voltage*, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.



(A) N-channel FET working below saturation (V_{GS} = 0). (Depletion shown only in channel region).



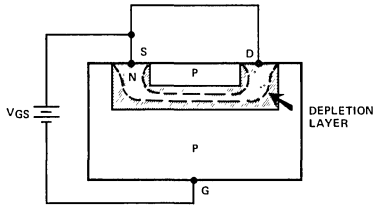
(B) N-channel FET working in saturation region (V_{GS} = 0)



(C) Idealized output characteristic for V_{GS} = 0.

Figure 3

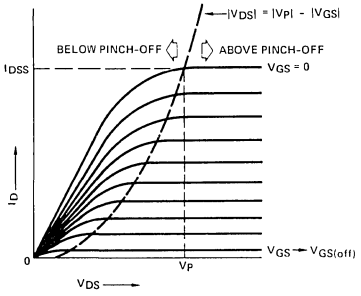
In Figure 4, consider the case where V_{DS} = 0, and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for V_{GS} = 0. In fact, at a value of $|V_{GS}| \geq |V_P|$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_P or by $V_{GS(off)}$. V_P has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_P, strictly speaking, are equal in magnitude but opposite in polarity.



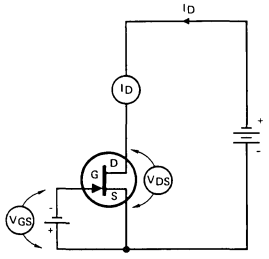
N-channel FET Showing Depletion Due To Gate-Source Voltage (V_{DS} = 0)
Figure 4

The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET



(B) Circuit arrangement for N-channel FET

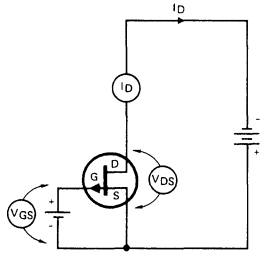
Figure 5

The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type chan-

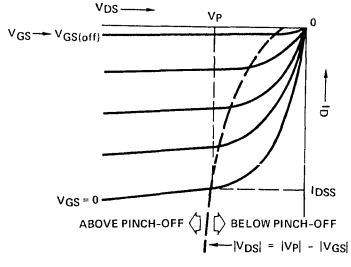
7

nel. In the P-Channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_P, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

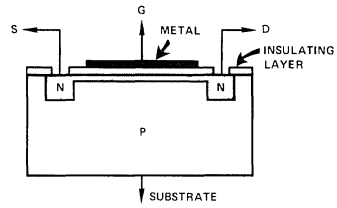


(B) Family of output characteristics for P-channel FET

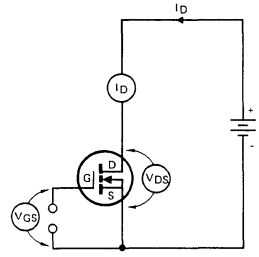
Figure 6

MOSFETs

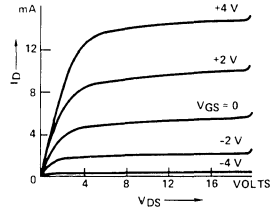
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the 2N3631 N-channel depletion MOSFET

Figure 7

in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.

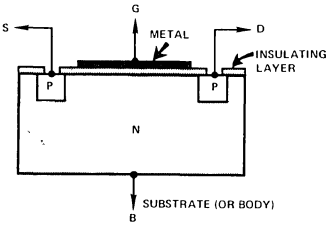
Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved, V_{GS} can be reversed without engendering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and I_D will become greater than I_{DSS}. This mode of operation is represented by the higher members of the family of ourput characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons – thus reducing I_D – the device just described is called a *depletion-mode* MOSFET.

The foregoing has established that the depletion-mode MOSFET is a "normally-ON" device: when $V_{GS} = 0$, a conducting path exists between source and drain. In many circuits a "normally-OFF" device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur, I_D being zero when $V_{GS} = 0$.

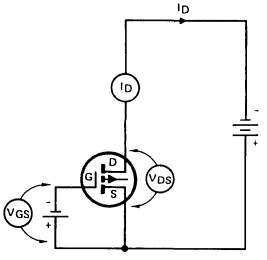
A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical MOSFET is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

If a constant (negative) gate voltage, ($V_{GS(K)}$) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is applied, then current, I_D, will flow through the drain. As $|V_{DS}|$ increases, I_D also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of I_D versus V_{DS} will eventually reach a limiting value when $V_{DS} = V_{GS}$, and the channel becomes pinched off. This condition is shown in Figure 9C.

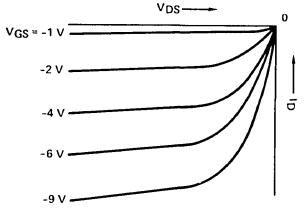
Different values of V_{GS} give rise to limiting values of I_D, so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for V_{GS} values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family in current use, and is in fact the basic element in many LSI integrated circuits.



(A) Idealized cross-section through a P-channel enhancement MOSFET

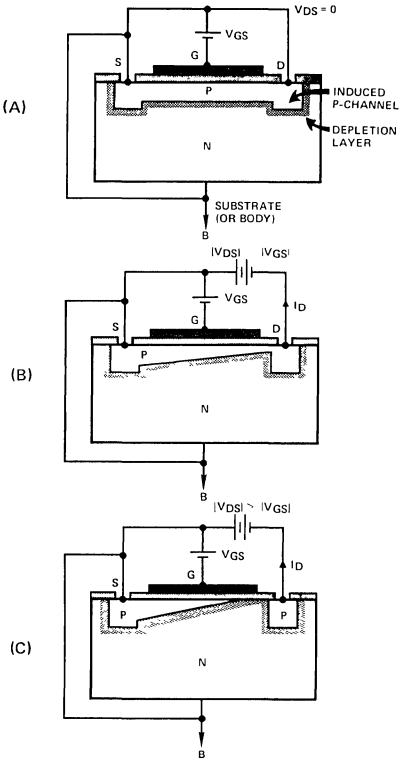


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off,
(A) $V_{DS} = 0$, (B) $|V_{DS}| < |V_{GS}|$, (C) $|V_{DS}| > |V_{GS}|$

Figure 9

7

FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (> 100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of g_m are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of 10^{10} to 10^{12} Ω. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be 22K Ω at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters – in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} – Drain current with the gate shorted to the source
- $V_{GS(off)}$ – Gate-source cutoff voltage
- I_{GSS} – Gate-to-source current with the drain shorted to the source
- BV_{GSS} – Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} – Common-source forward transconductance
- C_{gs} – Gate-source capacitance
- C_{gd} – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In FET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript does not refer to the FET source terminal. It is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11}\ V_{11} + Y_{21}\ V_{22} \qquad (1)$$

When Y_{11}, Y_{21}, Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$\begin{aligned} i_1 &= y_i\ v_{11} + y_r\ v_{22} \\ i_2 &= y_f\ v_{11} + y_o\ v_{22} \end{aligned} \qquad (2)$$

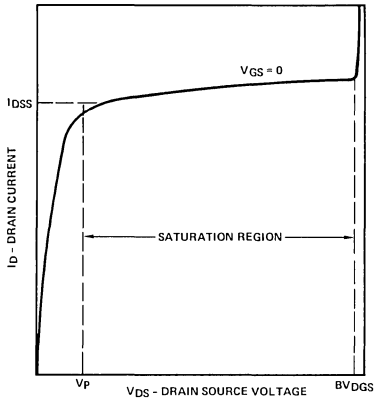
For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

$$\begin{aligned} i_i &= y_{is}\ v_{gs} + y_{rs}\ v_{ds} \\ i_o &= y_{fs}\ v_{gs} + y_{os}\ v_{ds} \end{aligned} \qquad (3)$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

I_{DSS} – Drain Current at Zero Gate Voltage (I_D at $V_{GS} = 0$)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_P (see Figure 10), I_{DSS} indicates the drain saturation current at zero gate voltage. Some FET data sheets label I_{DSS} for V_{DS} greater than V_P as $I_{D(on)}$.



FET Characteristic at $V_{GS} = 0$
Figure 10

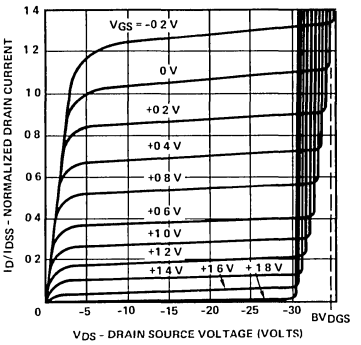
$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by $R = \rho L/A$, where

ρ = resistivity
L = length of the channel
A = W x T = cross-sectional area of channel

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance, r_{DS}, approaches infinity. As earlier noted, this condition is referred to as "pinch-off" or "cutoff" because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D. Accordingly, the pinch-off region is also referred to as the pentode or "constant-current" region.

In Figure 10, pinch-off occurs with $V_{GS} = 0$. In Figure 11, V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the "knee" of the curve. The current scale in Figure 11 has been normalized to a specific value of I_{DSS}.



FET I_D vs V_D Output Characteristics
Figure 11

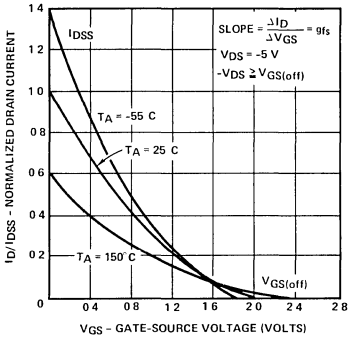
The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with $V_{GS} = 0$. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. The specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_P, defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as V_P. Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee, which approximates V_P. However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 12. The curve can be closely approximated by

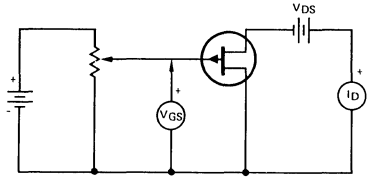
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4)$$



Typical I_D vs V_{GS} Transfer Characteristic
Figure 12

Equation 4 and Figure 12 indicate that at $V_{GS} = V_{GS(off)}$, $I_D = 0$. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS}, V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS}, the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, at room temperature, 1 percent of I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 13. At $V_{GS} = 0$, the value of I_{DSS} can be measured. Then, by increasing V_{GS} until I_D is 0.01 percent of I_{DSS}, the value of $V_{GS(off)}$ is obtained. From a production standpoint, it is more convenient to specify I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS}. Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring $V_{GS(OFF)}$
Figure 13

Table I
Typical Pinch-Off Voltage Specification

Characteristic		Min	Max	Units
$V_{GS(off)}$	Gate-source pinch-off voltage of $V_{DS} = -5$ V, $I_D = -1$ μA	1	4	Volts

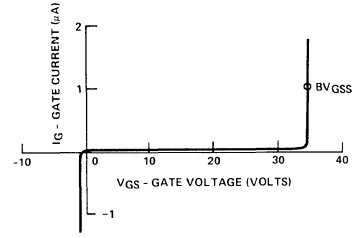
Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, whereas the parameter of interest is $V_{GS} = 8$ volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 volts, but no provision is made for stating a *minimum* $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off)\,(min)}$ is to be specified.

Table II
Indication of Maximum V_P

Characteristic		Test Conditions	Min	Max	Unit
$I_{D(off)}$	Pinch-off drain current	$V_{DS} = -12$ V, $V_{GS} = 8$ V		-10	μA

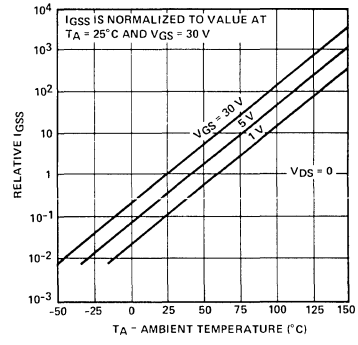
I_{GSS} – Gate-Source Cutoff Current

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic
Figure 14

In the normal operating mode, with V_{GS} positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a d-c gate-source resistance which is typically more than 100M Ω. The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for I_{GSS} versus temperature and V_{GS}.



I_{GSS} vs Temperature
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if V_{GS} exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current: I_{GDO}, I_{GSO}, and the combined measurement I_{GSS}. These measurement circuits are shown in Figure 16.

The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO} + I_{GDO} > I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if V_G is greater than $V_{GS(off)}$, the difference between $(I_{GSO} + I_{GDO})$ and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO}.

In a circuit, V_{GD} may be biased between zero and BV_{GDS}, while V_{GS} will be between zero and $V_{GS(off)}$: therefore, I_G is not necessarily the same as I_{GSS}.

BV_{GSS} – Gate-Source Breakdown Voltage

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

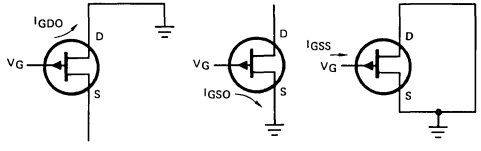
A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also possible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1. A better method is to use a BV_{GSS} rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n, in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The BV_{GSS} test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

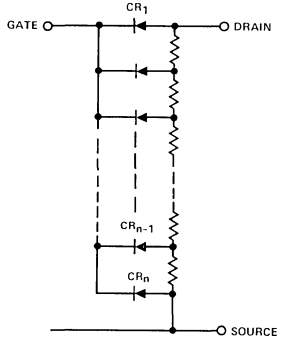
Admittedly, a BV_{GSS} test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

Test Procedures for BV_{GSS}

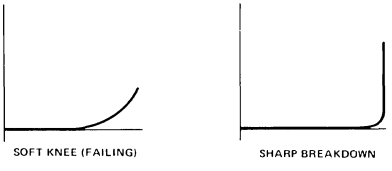
Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurement of Gate Current
Figure 16



A Useful FET Equivalent Circuit
Figure 17



Examples of Soft Knee and Sharp Knee Breakdown
Figure 18

g_{fs} – Transconductance

Transconductance, g_{fs}, is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, \quad V_{DS} = \text{constant} \tag{5}$$

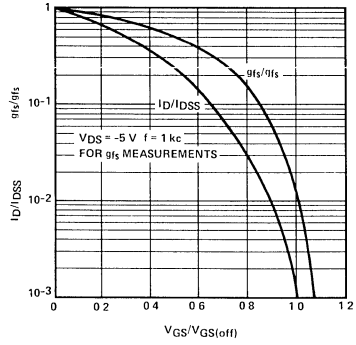
The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(OFF)}$ should be noted. Equations 4, 6 and 7 describe the value of I_D and g_{fs} in a FET for any value of V_{GS} between zero and $V_{GS(OFF)}$.

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \tag{6}$$

$$g_{fso} = -\frac{2I_{DSS}}{V_{GS(off)}} \tag{7}$$

where g_{fso} is the value of g_{fs} at $V_{GS} = 0$ and I_{DSS} is the value of I_D at $V_{GS} = 0$. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(off)}$ are known.

Figure 19 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2606. The curves agree very well with Equations 4 and 6 until $V_{GS(off)}$ is approached. For these curves, $V_{GS(off)}$ was assumed to be the value of V_{GS} where $I_D/I_{DSS} = 0.001$.



Normalized Curves for I_D and g_{fs} as Functions of V_{GS}
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_D/\text{triode} = I_{DSS}\left(\frac{V_{DS}}{V_{GS(off)}}\right)^{1/2} \tag{8}$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

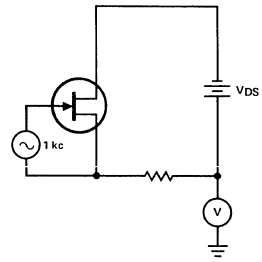
Table III (2N3823)

Characteristic		Test Conditions	Min	Max	Unit
g_{fs}	Small-signal common-source forward transconductance	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	3,500	6,500	μmho

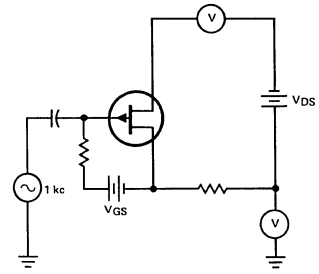
Table IV (2N3329)

Characteristic		Test Conditions	Min	Max	Unit
Y_{fs}	Common-source forward transfer admittance	V_{DS} = −10 V, I_D = −1 mA f = 1 kHz		20	μmho

The test conditions shown in Table IV specify a certain value for I_D (−1 mA for the 2N3329). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table III simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS}. Figures 20 and 21 show typical test setups for the two methods.



Test Circuit for g_{fs} with $V_{GS} = 0$
Figure 20



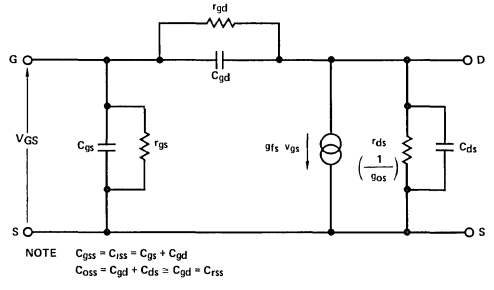
Test Circuit for g_{fs} with I_D Specified
Figure 21

Junction FET Capacitances

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS}. Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd}, exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds}, also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS}, V_{GS} and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the −2.2 mV/°C change in junction potential difference.

Assuming that the FET is properly biased – that is, that the d-c conditions are met by the external circuitry – it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



Incremental Equivalent Circuit for the Junction FET
Figure 22

The equivalent capacitance from the gate to the source, C_{gs}, is shunted by a very large input resistance, r_{gs}, with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd}. (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} – which stems from the header material – is shunted by the incremental channel resistance, r_{ds}. This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs}, multiplied by the incremental gate voltage. For the small signal, v_{gs}, this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET, in a "positive" direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} adn r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd}.

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss} \text{ (or } C_{iss}) = C_{gs} + C_{gd} \tag{9}$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss} \text{ (or } C_{oss}) \approx C_{gd} \tag{10}$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gd} is C_{rss}, which refers to the "reverse" capacitance.

In data sheets, it is customary to state (= C_{iss}) C_{gss} and C_{dss} (= C_{oss}). C_{rss} is often given in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usually the case, then $C_{rss} \cong C_{oss}$ Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd}, as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \tag{11}$$

and

$$C_{gd} = C_{rss} \tag{12}$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix J202 N-channel FET. They are given as

C_{iss} (at V_{DS} = 20 V and f = 1 MHz) = 5 pF max.

and

C_{rss} (at V_{DS} = 20 V and F = 1 MHz) = 2 pF max.

Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz, C_{gs} = 5 - 2 = 3 pF maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

Siliconix

FET Biasing

INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance in spite of wide device variations is to use a combination of constant-voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the V_{GS} = −0.4 V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD}, of 30 V and a drain resistance, R_D, of 39K Ω are being used.

The quiescent drain-to-source voltage, V_{DSQ}, is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ±0.2 V will produce output voltage swings of ±7.0 V – a voltage gain of 35.

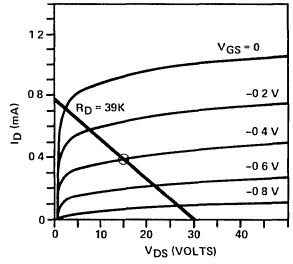


Figure 1. A large dynamic range is provided by the operating point at V_{DSQ} = 15 V, I_{DQ} = 0.39 mA and V_{GSQ} = −0.4 V. The output characteristics are for a typical 2N4339.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for V_{GG} = constant on the transfer characteristic of the FET.

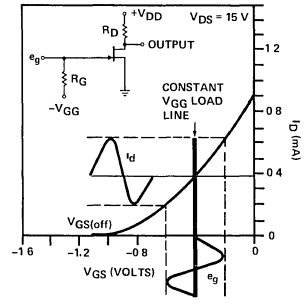


Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical 2N4339 transfer curve. Input signal e_g moves the load line horizontally.

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The transfer characteristic is a plot of I_D vs V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, it is quite useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

The heavy vertical line at V_{GS} = −0.4 V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g, combine in series with V_{GS} so that they add algebraically to the fixed value of −0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source-coupled differential amplifiers, and to ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

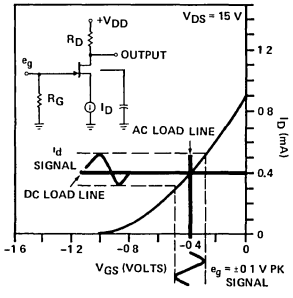


Figure 3. Constant-current bias fixes the output voltage for any R_D. Hence, input signals cannot affect the output unless the current source is bypassed.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

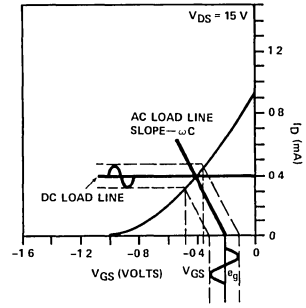


Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g.

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g, is reduced by the drop across the capacitor:

$$v_{gs} = e_g - v_S = e_g - i_S X_C \qquad (1)$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to V_{gs}, the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S, to the gate. Since no voltage is dropped across R_S when I_D = 0, the self-bias load line passes through the origin. Its slope is given by $-1/R_S$. Therefore, the desired Q-point is established by setting $-1/R_S = I_{DQ}/V_{GSQ}$.

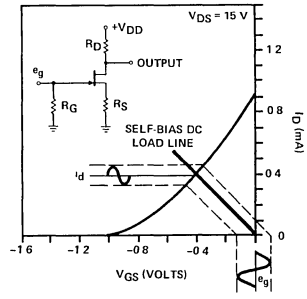


Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with X_C replaced by R_S. The ac gain of the circuit can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S) = -(\omega C + 1/R_S)$.

7

The circuit is biased automatically at the desired Q-point, requires no extra power supply and provides a degree of current stabilization not possible with constant-voltage biasing.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG}. (The bias line intercepts the V_{GS} axis at V_{GG}.) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

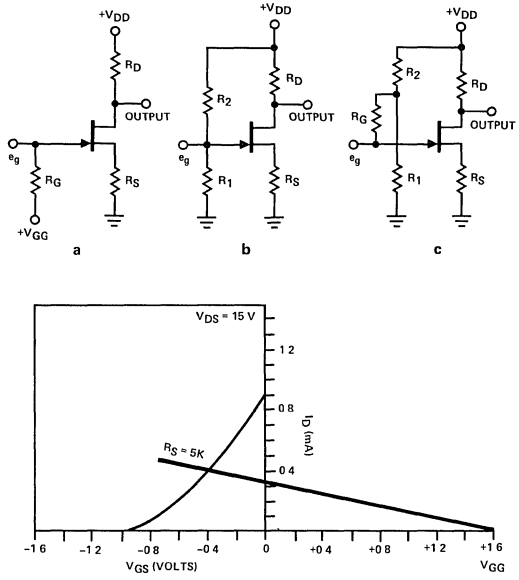


Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6(c) overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

One point of caution worth remembering is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore with low V_{DD}, there may be a significant decrease in the allowable output voltage swing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7

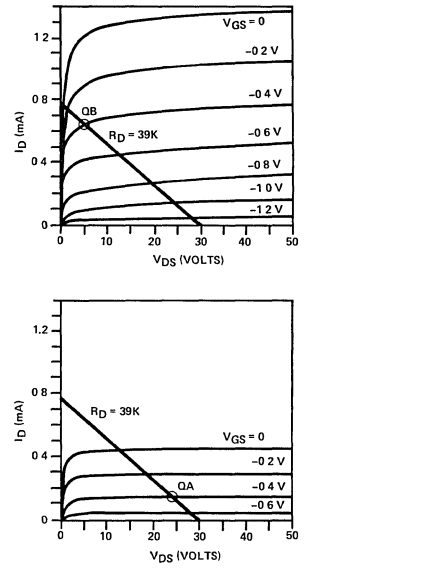


Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

where two limiting sets of output characteristics, representing the actual min-max spread of the Siliconix 2N4339, are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8. (See next page.)

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance – for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At V_{GS} = –0.4 V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{DSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with R_D = 39K Ω and V_{DD} = 30 V, V_{DSQ} varies from near saturation (5 V) to 25 V.

An apparently excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate I_{DQ} = constant for all devices. For the constant-current bias plot of Figure 8, with I_{DQ} = 0.39 mA, V_{GS} would range from –0.11 to –0.67 V.

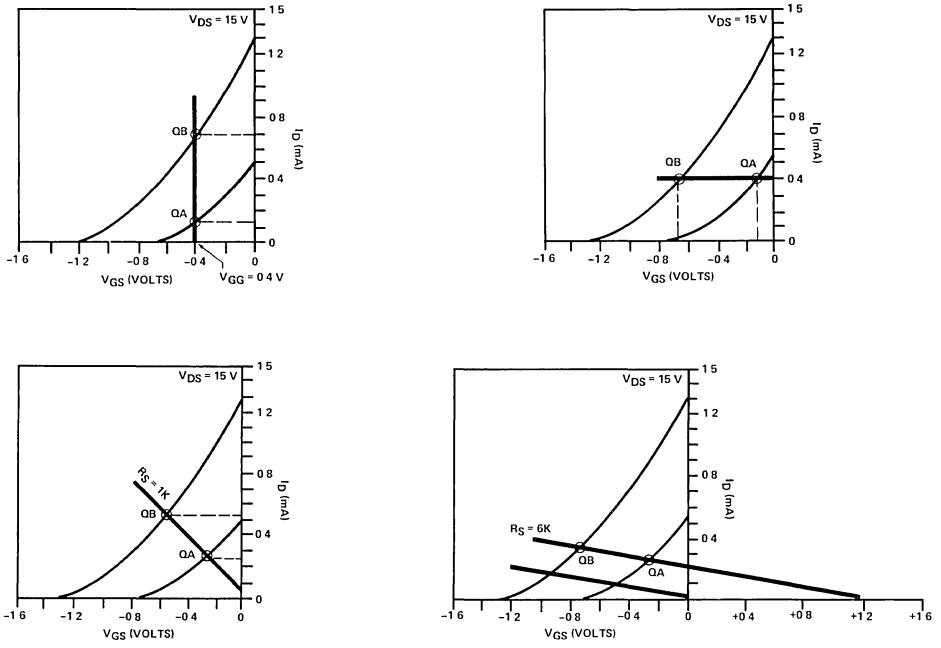


Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS}. With R_D = 39K Ω and V_{DD} = 30 V, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs}, of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S.

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for R_S = 1K Ω, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D. Clearly, for R_D = 39K Ω, the maximum-limit device (device B) would operate with V_{DSQ} = 9.8 V and the minimum-limit device (device A) would operate with V_{DSQ} = 20.6 V. This results in fairly satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with V_{GG} = 1.2 V. The range of I_{DQ} for this bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in I_{DQ} could be achieved with R_S = 6K Ω and V_{GG} = 0, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows v_{gs} = ±1.8 V (limited by I_{DSSA}), while the lower line allows a v_{gs} of only ±0.7 V (limited by $V_{GS(off)A}$). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with R_D = 62K Ω, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of (V_{DD} − $2V_{GS(off)typ}$) or 14 V, yields R_D = (14 V/0.285 mA) = 49K Ω.

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

Minimize the Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

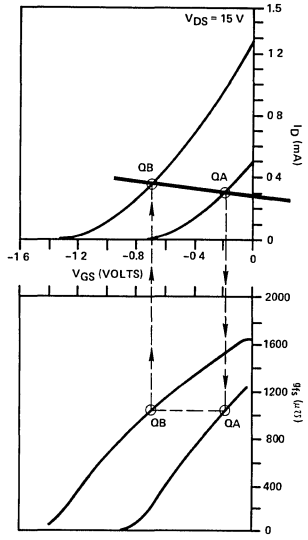


Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values so that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

Step 1. Select a desired I_{DQA} below I_{DSSA}. A good value, allowing for temperature variations, is 60% of I_{DSSA}. This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.

Step 2. Enter the transfer curves at $I_{DQA} \cong 0.6\ I_{DSSA}$ (0.3 mA) to find V_{GSQA}. This $V_{GSQA} \cong 0.2$ V for the 2N4339.

Step 3. Drop vertically at V_{GSQA} to the minimum limit transconductance curve to find g_{fsQA}. The value as read from the plot is approximately 1000 μmho.

Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs}. This is $V_{GSQB} \cong -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB}. This is $I_{DQB} \cong 0.36$ mA.

Step 6. Construct an R_S bias line through points Q_A and Q_B on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG}.

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB})/(I_{DQB} - I_{DQA}) \quad (2)$$

and the bias voltage is

$$V_{GG} = R_S\, I_{DQB} + V_{GSQB} \quad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})}/-V_{GS(\text{intercept})} \quad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point Q_A and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is Q_B.

Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ}. However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

Step 1. Establish R_S and limiting values of I_{DQ}, V_{GSQ} and g_{fsQ} from the transfer curve.

Step 2. Establish V_{DD} as available, but in no case greater than BV_{GSS} nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous v_{dg} be allowed to fall below 2 x $V_{GS(off)}$ if minimum distortion is to be achieved.

Step 3. Set V_{DSQ} approximately midway between V_{DD} and 2 x $V_{GS(off)}$; lower if large output signals will not be handled.

Step 4. Select R_D to give the appropriate V_{DSQ}. The formula is:

$$R_D = [(V_{DD} - V_{DSQ})/0.5\ I_{DQA} + I_{DQB}] - R_S \quad (5)$$

In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30\text{-}3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5\ (0.52 + 0.24)$ mA $- 1K\ \Omega = 42.5K\ \Omega$.

Step 5. Check to ensure that with this R_D, device B is not in a saturated condition $- V_{DQB} = V_{DD} - I_{DBQ} R_D > 2V_{GS(off)} + R_S I_{DBQ}$.

Decrease R_D if this condition is not met.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

Step 3. Determine required stage gain, A_V, and set $R_D = A_V/g_{fsQ}$.

Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S) I_{DQ} \qquad (6)$$

Step 5. If necessary, change I_{DQ}, V_{DD}, A_V and/or R_D to obtain an optimum compromise. ■■

FET SOURCE-FOLLOWER CIRCUITS

Too little knowledge of biasing methods for FET amplifiers sometimes keeps engineers from making maximum use of FETs in circuit designs. The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors.

By considering 10 circuits, which represent virutally every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d, Q_2 must have a lower cut-off voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.
- Circuits e, g, h and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

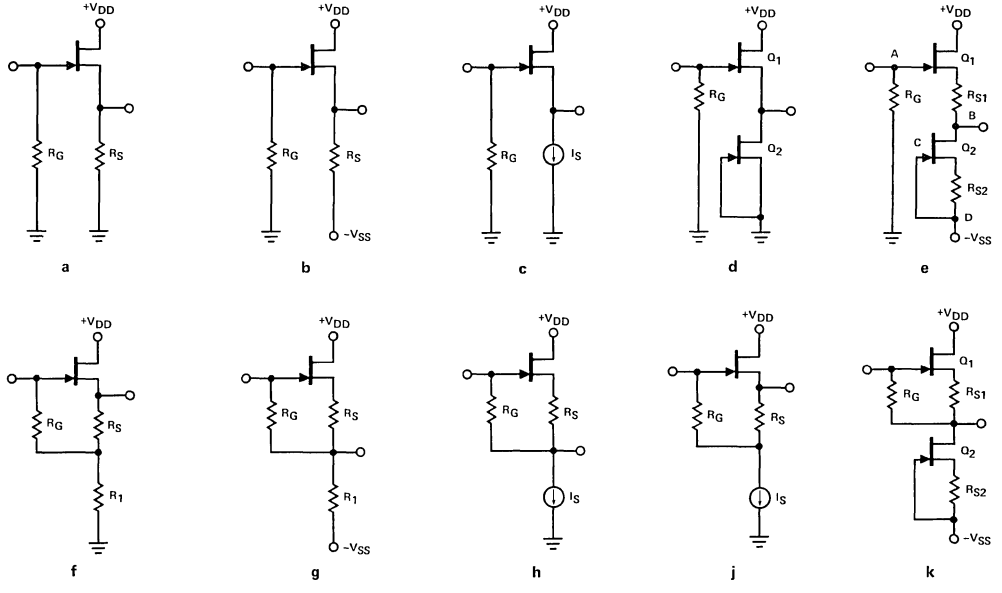


Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

Biasing Without Feedback is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this article, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1K Ω source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.

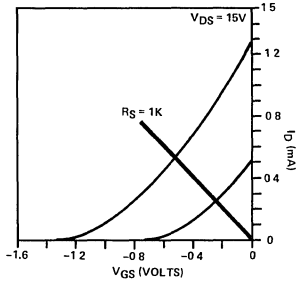


Figure 11. Self biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 10(b) is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for $V_{SS} = -15$ V and the other $V_{SS} = -1.6$ V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.

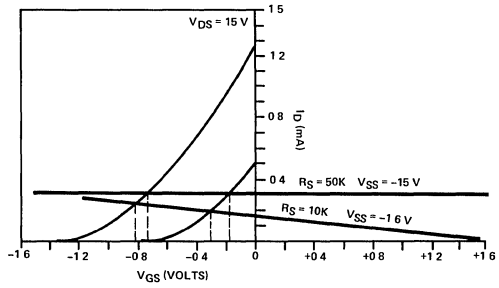


Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS}-axis is at $V_{GS} = -V_{SS}$. Bias lines are shown for $V_{SS} = -15$ V and $V_{SS} = -1.6$ V.

The bias load line for circuit 10(c) is just a horizontal line (I_D = constant). The quiescent output voltage is between +0.15 and 0.7 V for $I_D = 0.3$ mA.

Circuit 10(d) is similar to 10(c) except that the $V_{GS} = 0$ output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(off)}$ is significantly higher than the equivalent $V_{GS(off)}$ of the current-source FET diode.

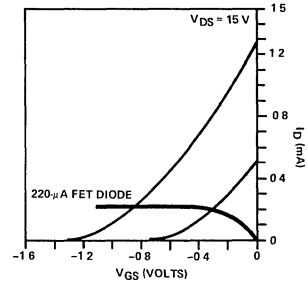


Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(off)}$ than Q_2 does.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Figure 14. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

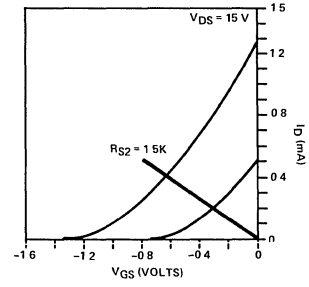


Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). If its components are properly matched, the circuit will have zero or near-zero offset.

Since $I_{D1} = I_{D2}$ and $V_{GS1} = V_{GS2}$, choosing $R_{S1} = R_{S2}$ will ensure that the voltage from point A to B equals the voltage point from point C to D (Figure 10(e)). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

Biasing With Feedback Increases Z_{in}

Each of the feedback-type source followers (Figure 10(f) through 10(k)) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero. R_1 is usually much larger than R_S.

Circuit 10(f) is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

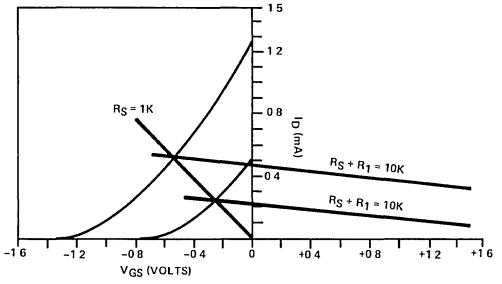


Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{fb} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

In the circuit of Figure 10(g), R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 ohms and 2.5K Ω. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

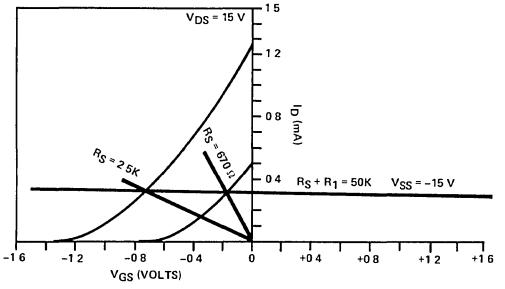


Figure 16. R_S can be trimmed to provide zero offset at some point between 670 ohms and 2.5K Ω (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of −1/50K, because the current source is not perfect; it has a finite impedance.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of circuit 1(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of −1/50k.

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work at all properly.

In Figure 17, the constant-current load line represents a 0.3-mA current source, and the effect of a 1K Ω source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For R_S = 1K Ω, V_{FB} will be between −0.1 V and +0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

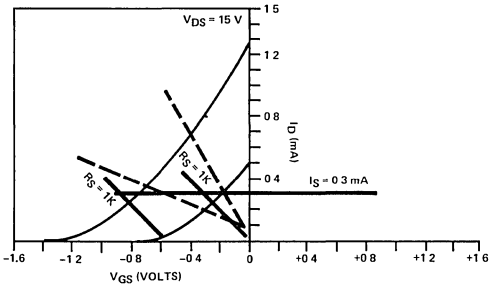


Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

This can be done by trimming R_S, as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raise the input impedance.■■

REFERENCES

(1) Sherwin, J.S., "How, Why and Where to Use FETs," *Electronic Design*, May 17, 1966, p. 94.

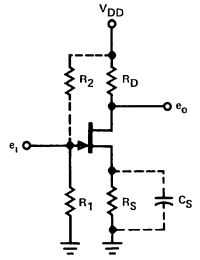
(2) Sherwin, J.S., "Knowing the Cause Helps to Cure Distortion in FET Amplifiers," *Electronics*, Dec. 12, 1966, pp. 99-105.

APPLICATIONS

Siliconix

Amplifier Charts

For convenience this chart offers the designer circuit values for a variety of commonly used J-FET amplifiers.

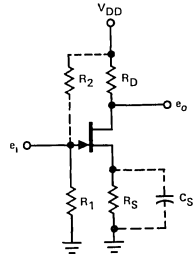


Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

V_{DD} (V)	R_S (Ω)	R_1 (MΩ)	R_2 (MΩ)	C_S (μF)	I_{DD} (mA)	R_D (Ω)	e_o Max (V)	A_V
J111								
30	560	1	∞	100	11	1K	3	9
	2 7K	3 3	10	100	6	1K	2 5	8
V_{DD} = 15 V_{SS} = -15	3K	1	Source Follower		7	0	8 5	0 96
	7 5K	1			6	0	8 5	0 96
V_{DD} = 15 V_{SS} = -15	7 5K	1	Source Follower		6	0	15	0 97
J112								
20	2K	4 7	11	100	5	1K	1 5	8-11
	330	1	∞	100	8	820	1 5	9
	330	1	∞	0	8	820	3	1 9
30	2K	4 7	11	100	6	2 7K	5	18-24
	330	1	∞	100	8	1 5K	2 5	15
	330	1	∞	0	8	1 5K	5 5	3 3
V_{DD} = 15 V_{SS} = -15	4 7K	1	Source Follower		5	0	11	0 97
J113								
10	220	1	∞	0	5	1 2K	1 5	3 5
20	220	1	∞	0	5	2 2K	3 5	7
30	1K	1	12	100	4	3 9K	5	38
	1K	1	12	100	4	5 6K	3 5	40-55
V_{DD} = 15 V_{SS} = -15	4 7K	1	Source Follower		2 5	0	13	0 98
	7 5K	1			1 5	0	13	0 98

V_{DD} (V)	R_S (kΩ)	R_1 (MΩ)	R_2 (MΩ)	C_S	I_{DD} (μA)	R_D (kΩ)	e_o Max (pK V)	A_V
2N4117								
10	10	1M	∞		45	120	1	5 7
20	10	1M	∞		45	270	1 5	12
						360	1	15
30	10	1M	∞		45	420	4	17
						620	1	22
V_{DD} = +15 V_{SS} = -15	510	1M	∞	Source Follower	35	0	8	0 97
2N4118								
10	8 2	1M	∞		120	36	0 6	2 2
						50	0 2	3 5
20	8 2	1M	∞		120	120	1	7 5
30	8 2	1M	∞		120	180	2	10
V_{DD} = +15 V_{SS} = -15	510	1M	∞	Source Follower	35	0	8	0 97
2N4119								
20	56	1	∞	5 μF* at 5 V	70	150	1	10
30	56	1	∞		70	240	3	17
						330	1	17-23
20	6 8	1	∞		300	27	1	1 8
30	6 8	1	∞		300	68	2	4 5
V_{DD} = +15 V_{SS} = -15	510	1	∞	Source Follower	40	0	10	0 97

*AC Amplifier



Amplifier Design Chart

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4338								
15	1500	1M	∞	0	0.25	36	2 5	9-12
				30		36	1 5	16-24
						47	2 0	20-30
	5100	1M	∞	0	0.12	82	3.0	10-10.5
				25		82	1.5	24-37
	36K	1M	2M	30	0.15	27	1.0	13-18.5
30	1500	1M	∞	0	0.25	82	4 0	21.5-27
				30		82	2.5	32-49
						100	3.0	43-64
	5100	1M	∞	0	0.12	150	4.5	14.5-16
				25		150	2.5	38-54
						200	1.5	40-50
	36K	1M	5M	30	0.15	82	5.0	37-52
45	1500	1M	∞	0	0.25	120	6.5	27-33
				30		120	4.0	45-68
	5100	1M	∞	0	0.12	270	10	28-31
				25		270	5 0	76-105
	36K	1M	8 2M	0	0.15	120	14	2 8
				30		120	7.0	54-76
V_{DD} = +15 V_{SS} = −15	100K	1M	∞	0	0 15	0	9.0	0 98
2N4339								
15	1800	1M	∞	0	0 42	20	3.0	7-7.5
				40		20	2.0	17-22
						27	2.0	23-27
	9100	1M	6.8M	35	0.32	18	2.0	17-19
						30	2 5	26-28
	27K	1M	3M	25	0 2	22	1.0	16-18
						43	2.0	28-30
30	1800	1M	∞	0	0 42	47	6.5	15-17
				40		47	4.0	38-47
						51	4.5	40-50
	9100	1M	13M	0	0 32	43	8.0	4.5
				35		43	5.0	40-43
						68	4.5	53-60
	27K	1M	7 5M	25	0.2	68	4 0	49-52
						100	7.0	66-70
45	1800	1M	∞	0	0 42	75	7 5	23-25
				40		75	5.0	58-70
						100	7 0	73-77
	9100	1M	22M	0	0.32	68	7 0	7.0
				25		68	6.5	59-64
						120	7 0	80-85
	27K	1M	12M	0	0.2	100	12	3 3
				25		100	5 0	65-68
						180	8 0	100-115
V_{DD} = +15 V_{SS} = −15	75K	1M	∞	0	0 22	0	10	0.98

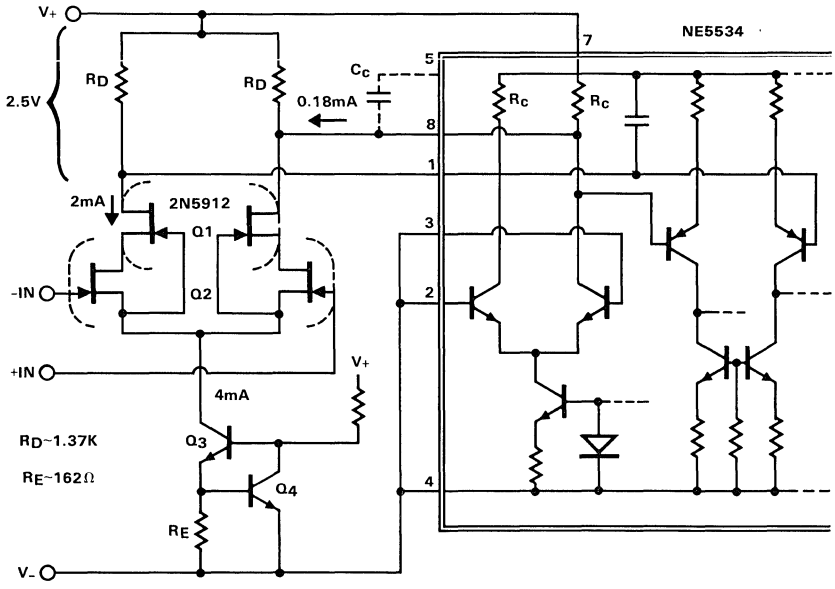
V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4340								
15	680	1M	∞	0	1 5	5 1	3 0	3 5-4
				65		5.1	1.5	7-8 5
						6.8	2.0	9-10.5
	1200	1M	∞	0	1 1	7 5	2 5	3 5-4
				60		7.5	2.0	9-11
						10	2 0	11-13
	3900	1M	∞	0	0 4	18	4 0	3 5-4
				40		18	1 5	15-18
						22	1 0	19-22
30	680	1M	∞	0	1 5	12	6 0	9.5-10
				65		12	3 0	17-22
						18	1 0	24-26
	1200	1M	∞	0	1 1	18	6 0	9-9 5
				60		18	4.0	21-26
						24	2.0	29
	3900	1M	∞	0	0 4	39	7.0	7.5-8
				40		39	7.0	30-36
						62	0.5	34-45
	20K	1M	6 8M	35	0 35	30	3 0	25-27
						56	6 5	40
45	680	1M	∞	0	1.5	20	10 5	14-15 5
				65		20	8 0	27-32
						27	4.0	35
	1200	1M	∞	0	1 1	27	12.5	16-18
				60		27	5 0	30-37
						39	2 0	39-42
	3900	1M	∞	0	0 4	68	12	12-13
				40		68	7 0	52-61
						91	3 0	56-63
	20K	2M	3M	55	1 0	10	5 0	15
						20	4 0	27-28
V_{DD} = +15 V_{SS} = −15	22K	1M	∞	0	0 75	0	12	0.96
2N4341								
15	1000	1M	∞	70	2.7	2	1 0	3-3.5
						2.7	2.0	4-4.5
	1200	1.2M	7.5M	80	3.5	1.2	2 0	2 5
						2.2	3 0	3-4 5
	2000	1M	∞	65	1 8	3	2 0	4-4.5
						4.7	1.5	6-6 5
30	1000	1M	∞	0	2.7	6.2	7 0	4 0
				70		6.2	3.5	10
						9.1	1 5	11-13
	1200	1.1M	15M	80	3.5	3.9	4 0	7.5-8
	2000	1M	∞	0	1.8	9 1	6.0	3.0
				65		9 1	4.0	12
						15	1.0	13-19
	15K	1M	3 3M	50	0.7	18	3 0	16-21
45	1000	1M	∞	0	2 7	10	8.5	6.3
				70		10	6 0	16
	1200	1M	22M	80	3 5	6.8	7 0	13
	2000	1M	∞	0	1 8	15	8.5	5.5
				65		15	5 0	20-21
	15K	1M	5.6M	50	0.7	30	9.0	28-35
V_{DD} = +15 V_{SS} = −15	10K	1M	∞	0	1.9	0	13 5	0 94

Composite Op Amp for High Performance

For op amp applications requiring the best possible performance, consider a composite op amp that takes advantage of differing process technologies. A JFET dual can be combined with a Signetics NE5534 bipolar op amp for outstanding performance. Input bias current can be reduced, yet slew rate can be very high (20V/μsec to 40V/μsec) and the circuit is unity-gain stable. Output swing is a minimum of ±12V into a 600 ohm load when operating from ±15V power supplies. This high output capability combined with a JFET input stage makes this an excellent amplifier for high-speed integrators, SAMPLE/HOLD circuits, peak detectors, and log amplifiers.

The input portion of the circuit is shown in Figure 1. The NPN input stage of the NE5534 IC op amp is biased into cut-off by connecting both inverting and non-inverting inputs to the negative rail. A JFET preamplifier input stage

High Performance Op Amp Using The Siliconix 2N5912



is then connected into the PNP second stage of the NE5534 and the currents that formerly flowed through the NE5534 NPN input pair are now diverted into the JFET input pair. Drain resistors R_D effectively parallel the collector resistors R_C from within the IC op amps and the JFET drain currents will then be the sum of the currents through R_D and R_C. The voltage across the parallel combination of R_D and R_C is nominally 2.5V due to the internal biasing of the NE5534. Going directly into the second stage of the IC op amp rather than into the NE5534 NPN input stage has two distinct advantages:

1. Frequency response is better in that the phase shift of the bipolar input stage is avoided. A high-current JFET input stage, such as the 2N5912 when operated in the 1mA to 8mA drain current range, has excellent frequency response in comparison to an NPN stage operating in the 150μA to 200μA range.

2. The operating level at the JFET drains is only 2.5V below the positive supply rail, therefore the common-mode input range for the JFET input stage can be relatively high. The combination of low input bias current with high frequency response is useful for SAMPLE/HOLD circuits, high-speed integrators, photo-multiplier tube amplifiers, and high-speed data conversion circuits.

Although more expensive than a single monolithic op amp, the combination of a JFET preamp with a bipolar IC second stage can provide substantially better performance than any monolithic alternatives.

A Siliconix 2N5912 JFET dual was chosen for the input stage in this example because of its high operating current range, high gain, and excellent frequency response. The saturation drain current I_{DSS} has a specified range of 7mA to 40mA, but is typically 10mA to 24mA. Gate source cutoff voltage $V_{GS(off)}$ is in the range of -1V to -5V with a typical value of approximately -2V to -4V. The 2N5912 characterization curves indicate that any drain current from 1mA to 8mA will provide good performance, and 2mA was chosen for this application.

The current diverted from the bipolar input stage to the JFET input stage is nominally 180μA on each side; therefore a drain current on each side of 1.82mA is needed from the drain resistors R_D to make up a total drain current of 2.0mA. The drain resistor R_D therefore needs to be approximately 2.5V/1.82mA, or 1370 ohms on each side.

Gain of the JFET input stage can now be calculated. From the 2N5912 characterization curves, forward transconductance g_{fs} will be in the range of 2.6mmhos to 5mmhos for units having I_{DSS} of 10mA to 24mA and when operated at a drain current of 2mA. The differential gain can be approximated by the product $g_{fs} R_D$. Using a center value of 4.3mmhos and 1230 ohms, (R_D and R_C in parallel), then the gain will be approximately 6.5, or 16dB. Total amplifier gain was found to closely approximate the gain curve for a 5534 being operated alone.

The cascode configuration using two input pairs as shown has several advantages. Most importantly, the input gate current is dramatically reduced due to the lower drain-to-gate voltage on the input pair. In the cascode configuration, the gate-to-source voltage on the upper pair will be the drain-to-source voltage of the input pair even with the common-mode input variations. All of the common-mode swing is taken up by variations in V_{DS} of the upper pair. Gate leakage of the input pair is primarily dependent on drain-to-gate voltage V_{DG}, which will be a constant $-2V_{GS}$ in this cascode configuration. Drain-to-gate voltage on the input pair will be low, typically in the 3V to 6V range, which is well below the "I_G breakpoint". From the characterization curves on the 2N5912, gate current leakage will be under 2pA for drain-to-gate voltages under 6V. The cascode configuration is very effective in reducing input bias current for JFET input stages. Another advantage of the cascode configuration is a reduction of input capacitance. The input pair drains are "bootstrapped" to the common source point and both must follow the gate voltage. The effective capacitance from gate-to-drain and from gate-to-source is reduced. In addition, output conductance is reduced by the cascode configuration which also helps CMR. Adding the second JFET pair significantly improves both input bias current and common-mode rejection without degrading other parameters.

The constant current source consisting of Q3 and Q4 primarily improves common-mode rejection and rejection of power supply variation. It also establishes the nominal operating voltage at the input (pins 1 and 8) of the 5534 op amp. The current will be a constant V_{BE}/R_E independent of fluctuations in power supply voltage or input voltage level. This current source has very high impedance, therefore common-mode inputs are heavily attenuated.

Common-mode-rejection-ratio (CMRR) is very high due to the use of a constant current source, but can be further improved by matching of drain resistance. The parallel combination of R_D and R_C is the effective drain resistance for this design. The transconductance ratio between the two sides of the input pair also directly affects CMRR. The drain resistors should be well-matched to minimize the CMRR adjustment range since it also affects offset and drift.

Each 1% mismatch in drain resistance will cause approximately 11μV/°C of input offset voltage drift. CMRR can be readily trimmed to over 100dB. CMRR vs. frequency is excellent due to the use of the 2N5912, a wide-bandwidth FET, in a cascode configuration.

A high performance op amp should also have good output characteristics, low noise, and high slew rate. The NE5534 op amp is rated for ±14V mimimum output swing into a 600 ohm load when operating from ±15V power supplies. Output resistance is typically 0.3 ohms. The Siliconix

2N5912 characterization curves show a typical equivalent input noise voltage of only $10nV/\sqrt{Hz}$ at 10Hz. There is also a component of noise from the second stage, but its effect is divided by the input stage gain and its contribution is small. Input current noise of this composite op amp is very low due to the typical operating level of 1pA input bias current. For slew rate, this circuit is capable of $50V/\mu sec$ when going negative. Positive slew rate is $50V/\mu sec$ without use of a compensation capacitor, but drops to $25V/\mu sec$ with a 20pF compensation capacitor. Compensation capacitance will generally be needed only when driving capacitive loads. Even the lower value of slew rate, $25V/\mu sec$, corresponds to a full-power (±10V) frequency of 400KHz.

While the vast majority of op amp applications can be satisfied through use of conventional IC op amps, there are applications in high-performance instrumentation systems that require superior performance. This composite op amp, which makes use of precision dual JFET input pairs and a high performance IC op amp, provides a unique combination of low input bias current, high CMR, low noise, excellent frequency response, and high output swing.

Siliconix

Applications for the Si1000 Series JFET Amplifier

Doyle L. Slack

INTRODUCTION

The Siliconix Si1000 series is much more than a JFET, it is a complete monolithic amplifier circuit featuring a low noise, low leakage JFET and two parallel diodes from the gate of the device to the substrate. An optional internal source resistor may be connected between source and substrate to provide a complete source follower amplifier in one small package. This application note will discuss the operation of the Si1000 series and its uses and advantages. Also, several example applications circuits are included to show the Si1000 series' versatility as an impedance matching circuit and/or small signal amplifier.

DEVICE OPERATION AND SPECIFICATIONS

The Si1000 series NBA geometry comes in two versions: the Si1000 family and the Si1100. The Si1000 family (Si1000, Si1010, Si1020) incorporates the features of two of our more popular JFET products, producing a unique combination of low noise *and* low leakage. Two parallel diodes are connected between the JFET gate and the substrate (which is tied to the fourth lead of the package). These diodes clip transient spikes and overvoltages, protecting the output of the circuit from sudden voltage fluctuations.

The Si1100 has the same features as the Si1000 but also includes an internal resistor from source to substrate. This resistor completes the source follower circuit and sets the output impedance of the amplifier.

Figure 1 shows the two circuits and their connections to the leads of a TO-72 can. It also gives the pad layout and dimensions of the Si1000 and Si1100 die for use in hybrid circuit applications. The internal source resistor in the Si1100 supplies a complete source follower amplifier circuit with a typical R_S range of 30 to 60 Kohms. However, if a source resistor outside of this range is desired or a different type of amplifier that still provides input overvoltage protection is needed, the Si1000 series without the source resistor should be used, since it allows more design flexibility. Table 1 shows some of the more important typical values for the Si1000 series and Si1100 device, and Table 2 gives the differences between the parts in each of the two families. A transfer characteristic graph is included in Figure 2 to give an idea of the operating range of the Si1000 series.

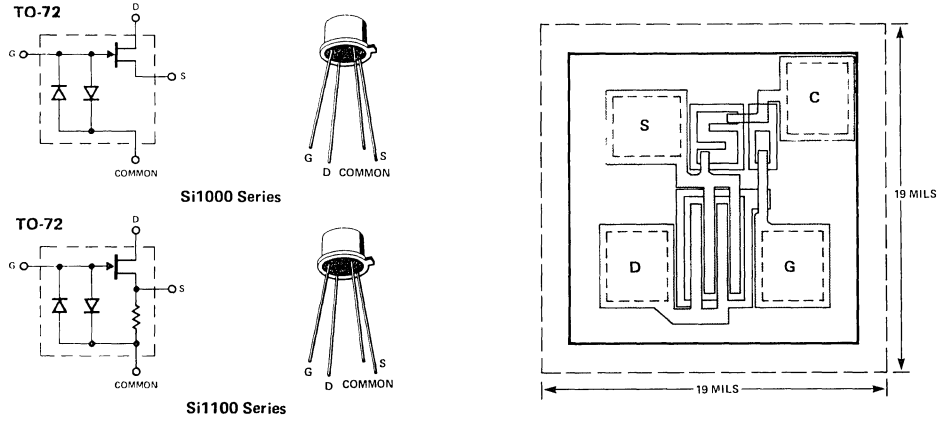


Figure 1. Schematic diagrams, lead connections, and die layout for the Si1000 series and Si1100 circuits.

7

Table 1. Typical values for discussed parameters of the Si1000 family and the Si1100.

PARAMETER	Si1000 Family	Si1100	Test Conditions
Diode Leakage	<2 pA	same	V_{G4}=+/-100mV
JFET Leakage	<1 pA	same	V_{GS}=OV, V_{DD}=10V V_{G4}=OV
Noise	10 nV/$\sqrt{Hz}$	same	V_{DS}=10V, V_{GS}=OV F=10 Hz
R_S	N/A	45 Kohms	V_{D4}=10V F=10 kHz

Table 2. Operating parameters of each of the parts in the Si1000 family.

PARAMETER	Si1000	Si1010	Si1020
V_P	-.3v/-1.8V	-.6V/-2.3V	-.9V/-3.5V
I_{DSS}	50uA/2mA	200uA/3.5mA	600uA/5mA
g_{fs}	100/3000 umho	400/3500 umho	1200/4000 umho

PARAMETER	Si1100	
V_G(operating)	.3V-2.7V	for
I_D(operating)	6uA-60uA	R_S=45 Kohms

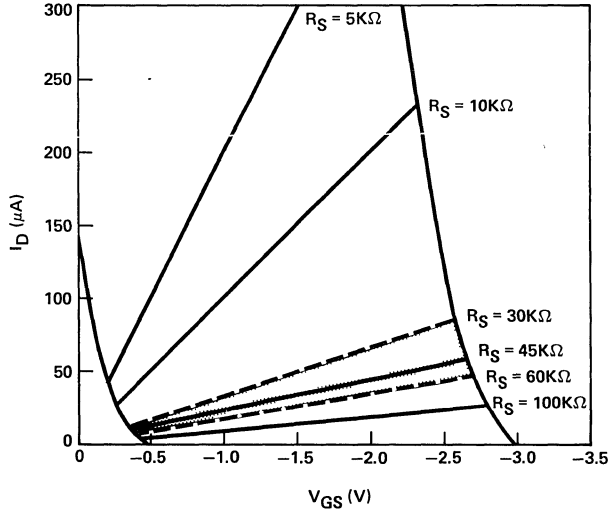


Figure 2. Graph of the transfer characteristics of the Si1000 family. Note that the shaded area is the area of operation for the internal R_S Si1100 with the typical 45K line in the center.

ADVANTAGES AND APPLICATIONS

Several advantages of the Si1000 series such as low noise, low leakage, and small size have already been mentioned. These and other advantages over discrete amplifiers including improvements in both circuit operation and ease of implementation make the Si1000 series very attractive:

1. A low noise and low leakage combination is effective in providing an extremely high input impedance and low loading. These characteristics allow connection to the outputs of high impedance transducers with minimal signal loss and signal noise injection.
2. The diodes provide overvoltage protection for later stages. If voltage sensitive circuits follow the Si1000 series part, the maximum output swing of the Si1000 source follower amplifier will be less than a diode forward voltage drop above or below ground potential if the fourth lead of the device is grounded.
3. Monolithic design reduces space requirements to a minimum, allowing circuit placement in locations that are often impossible for discrete amplifiers It also reduces the possibility of noise insertion from nearby sources because the case of the part is normally grounded to provide an effective RF shield. Also, the Si1000 series' small die size makes it very attractive for use in hybid circuits such as hearing aids where minimizing space is the greatest design factor.
4 Low current/low voltage capability makes the Si1000 series amplifier ideal for battery operation. This is important for low cost field operation and for portable equipment.

The most universal application of the Si1000 family is in impedance matching for high impedance sources (such as transducers) to low impedance loads (such as transmission lines). Figure 3 demonstrates how simply the Si1000 or Si1100 can solve the impedance problem. The input impedance of the JFETs are typically in the range of 500 Gigaohms (10^9) while the output impedance of the amplifier is set by the source resistor. In Figure 4, the Si1100 is shown in a more specific application—as a preamplifier for an electret microphone.

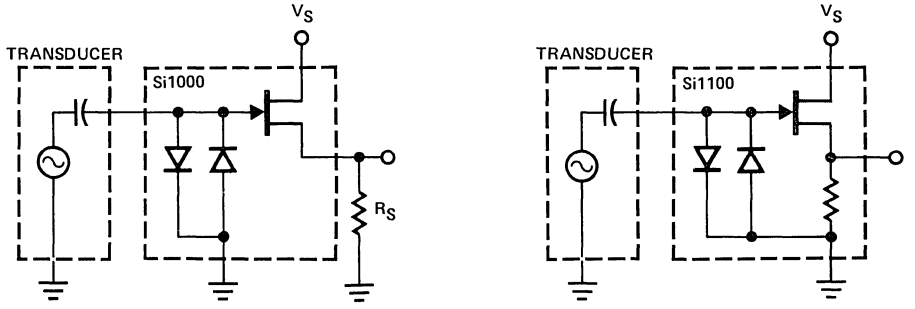


Figure 3. Si1000 and Si1100 devices connected as impedance transformers.

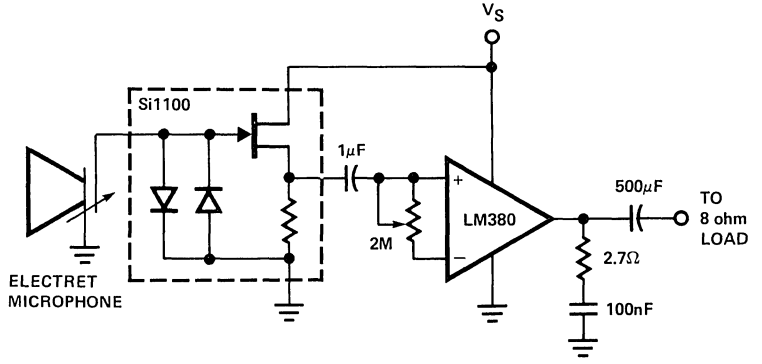


Figure 4. Schematic diagram of an audio amplifier utilizing the Si1100 as a microphone preamplifier.

But what if an even lower load impedance such as 50 ohms from a transmission line is to be used? Figure 5 shows how the output impedance of the source follower circuit can be lowered even more with the help of a bipolar transistor. The reflected resistance through the base of the bipolar is paralleled with the effective output resistance of the Si1000 circuit to produce an output resistance of less than 60 ohms and a voltage gain of better than .95 V/V. This allows both the source and load to be optimally matched with virtually no signal loss.

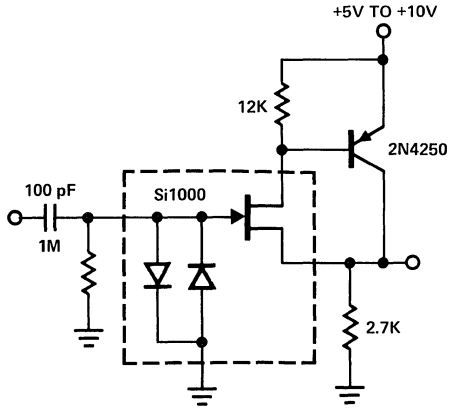


Figure 5. Schematic diagram of the bipolar assisted low output impedance source follower amplifier.

The bipolar assisted source follower gives great flexibility by allowing interface between any ultra high impedance source and a 50 ohm load with virtually no signal loss or noise insertion. Some examples of ultra high impedance transducers are electret microphones, input preamplifiers for hearing aids, accelerometers for military and industrial sensing, infrared sensors, and ion chambers such as those used for industrial radiation exposure monitors.

Another example of how the Si1100 family could be used is given in Figure 6. Here, the Si1100 series circuit input is connected to a capacitive field sensor (as simple as a piece of double sided circuit board). Any induced voltage change on the plates is fed to the input of the peak detector section of the op-amp circuit. The Schmitt trigger monitors the voltage across the capacitor and changes its output state when the capacitor voltage crossed the 2.5 Volt trigger point. The output from the Schmitt trigger switches between 0 and 5 Volts and is microprocessor compatible for sensor applications such as computer-controlled intruder alarms.

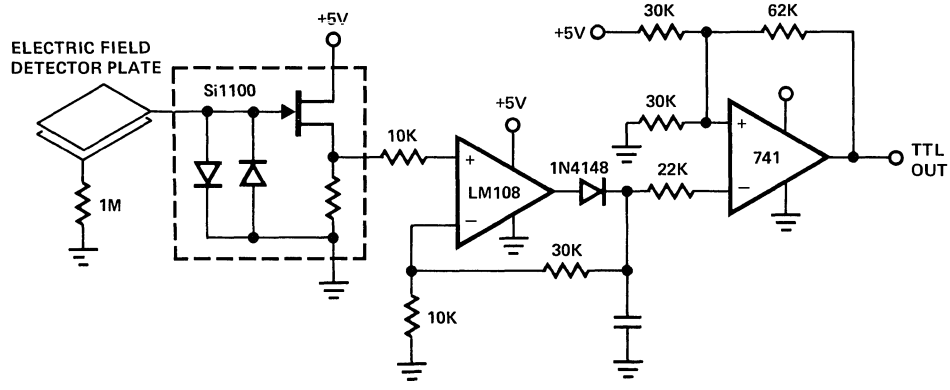


Figure 6. Schematic diagram of the Si1100 proximity sensor.

Another transducer interface problem occurs when high impedance measurement networks are connected to operational amplifiers for differential measurement. This can be solved by the circuit in Figure 7. Here a pair of Si1000 series parts has been used to monitor a high impedance bridge for an instrumentation amplifier. This circuit allows precision measurement at low input signal levels and easy zeroing of the amplifier output.

However, don't think that the Si1000 family has to be used just as a source follower. Another use of the Si1000 version is in the common source amplifier mode where low power or battery operation is important. Figure 8 gives a circuit that will operate in the 10 to 20 microamp range at a 12 Volt supply voltage. The diode protection is still available in this configuration, but the circuit voltage gain will be between 10 and 20, with extremely low power consumption (approximately 250uW). This is very desirable for remote or battery operation where minimum maintenance is important.

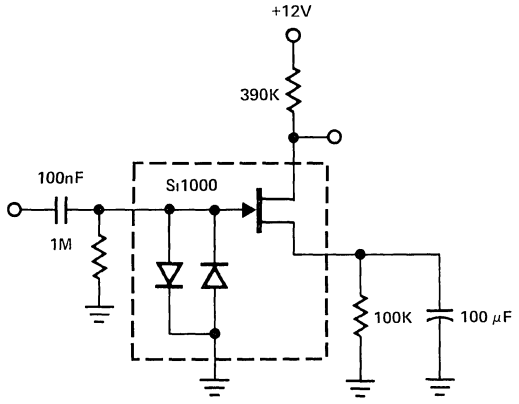


Figure 7. Schematic diagram of the low signal Si1000 high impedance instrumentation amplifier.

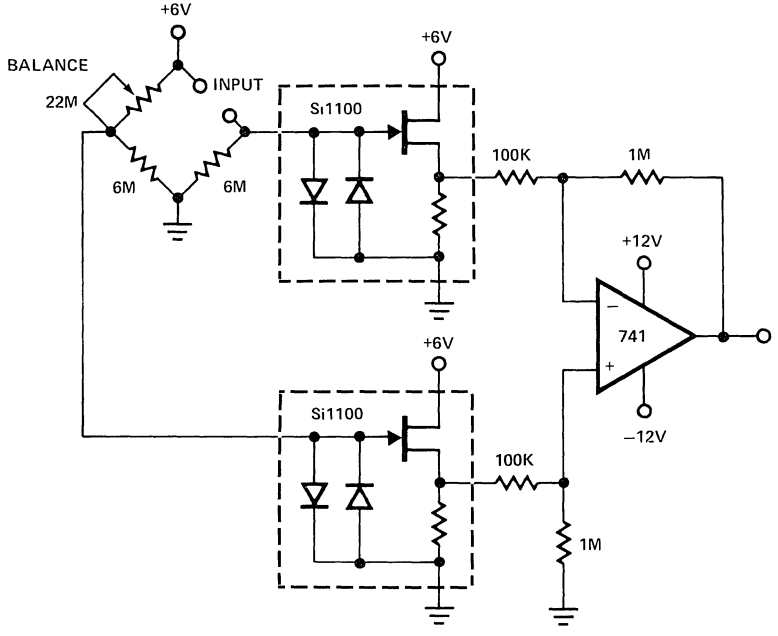


Figure 8. Schematic diagram of the Si1000 series low power common source amplifier.

CONCLUSION

With its low noise and low leakage combination, the Si1000 series amplifier is an ideal circuit for impedance matching. The Si1100 series circuits are dedicated for use as source follower amplifiers. Although the Si1000 series has also been designed for source follower applications, it is flexible enough that it may easily be converted to any suitable amplifier design and still provide diode protection. There are many good reasons to include these devices in your designs, such as small size, outstanding performance, and reasonable cost. These advantages make the Si1000 series preferable for numerous small signal applications.

FETs for Video Amplifiers

INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one or two transistor circuits. DC input resistances in the tens of megohms range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

Behavior of FET Input Resistance

A prime FET parameter, input impedance, has a large effect in determining the frequency response of a FET video amplifier. It is not a simple RC network but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance R_g and the FET input impedance Z_{in} form a frequency sensitive attenuation network. The larger the R_g, the worse will be the frequency response, and vice versa. Examining this in greater detail, consider the input equivalent circuit of a FET connected in the common source configuration,

where

R_{gs} and R_{gd} = bulk series gate resistance
C_{gs} and C_{gd} = bulk series gate capacitance
G_{oss} = output conductance

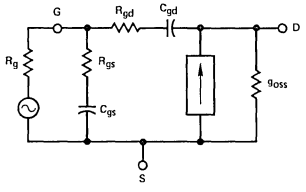


Figure 1

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel RC combination results in

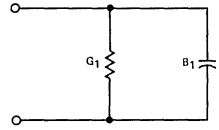


Figure 2

where

$$G_1 = \mathrm{Re}\,|Y_{in}| = \frac{\omega^2[T_1C_1(1+\omega^2T_2^2) + T_2C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2 + \omega^2(T_1^2+T_2^2)} \quad (1)$$

and

$$B_1 = \mathrm{Im}\,|Y_{in}| = \frac{\omega[C_1(1+\omega^2T_2^2) + C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2 + \omega^2(T_1^2+T_2^2)} \quad (2)$$

where

$$T_1 = C_{gd}R_{gd}$$
$$T_2 = C_{gs}R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

7

In common-source circuits, $1/G_1$ will typically fall to < 2K ohms at 100 MHz while C_1 remains substantially constant at least up to 1000 MHz. Figures 3 and 4 below exhibit these relationships.

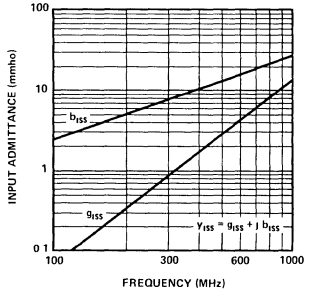


Figure 3

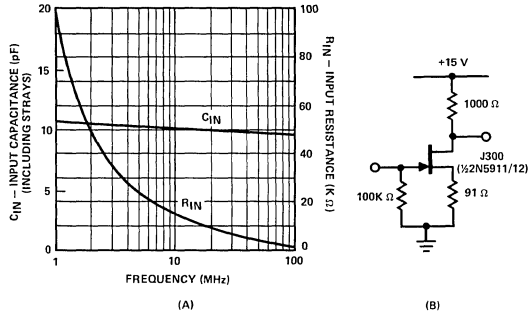


Figure 4

To maintain low input capacitance, and thus a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "FET and Bipolar Cascade" section (page 5). The effect of R_g on the frequency response is shown in Figures 6, 9, 11, 13 where various amplifier configurations are investigated.

Circuits to Consider

Five video amplifier circuits are considered. They are:

- Common-Source Configuration
- Shunt-Peaked Common-Source Configuration
- Source Follower
- Cascode Amplifier
- FET and Bipolar Cascade

Common-Source Circuit[1]

The circuit of Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 ohms to maintain good bandwidth which, with 50-ohm generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560\ \Omega \quad (4)$$

$$C_T = C_{gd} + C_D + C_S \quad (5)$$

C_{gd} = 2.0 pF, C_D the VTVM probe, 2.0 pF, and C_S is circuit stray capacitance of 3 pF.

$$C_T = 2 + 2 + 3 = 7\ \text{pF} \quad (6)$$

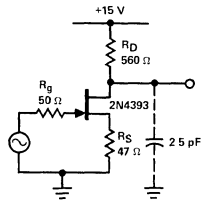


Figure 5

The 3-dB frequency ω_3 is given by:

$$\omega_3 = \frac{1}{C_T R_D} \quad (7)$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \quad (8)$$

$$\omega_3 = 255 \times 10^6 \quad (9)$$

$$f_3 = 39\ \text{MHz} \quad (10)$$

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs} R_D}{1 + g_{fs} R_S} \quad (11)$$

$$A_V = 4.9 \quad (12)$$

where

g_{fs} = 15 mmho when I_D = 12 mA, the quiescent current

$$R_D = 560\ \Omega \quad (13)$$

$$R_S = 47\ \Omega \quad (14)$$

Measured Performance

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

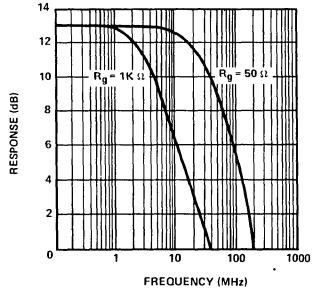


Figure 6

Effect of Increasing Generator Impedance

If the generator resistance R_g is increased to 1K ohm, the input time constant of the FET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance (R_g = 1K ohm) shunted by C_{in} (see Figure 7).

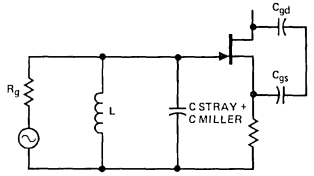


Figure 7

where

$$C_{in} = \left(1 + \frac{g_{fs}R_D}{1 + g_{fs}R_S}\right) C_{gd} + \left(1 - \frac{g_{fs}R_S}{1 + g_{fs}R_S}\right) C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \quad (15)$$

$$C_{in} = 30 \text{ pF} \quad (16)$$

where

$$C_{gd} = 3.5 \text{ pF} \quad (17)$$

$$C_{gs} = 10 \text{ pF} \quad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in}R_g} \quad (19)$$

$$= \frac{1}{30 \times 10^{-12} \times 10^3} = \frac{10^9}{30} \quad (20)$$

$$f_3 = 5.3 \text{ MHz} \quad (21)$$

which agrees closely with the measured bandwidth as shown in Figure 6.

Shunt-Peaked Common-Source Circuit

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. Consider first the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the FET input capacitance. The frequency of resonance is determined by:

$$f_o = \frac{1}{2\pi\sqrt{LC_{in}}} \quad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \quad (23)$$

The response of an input signal of frequency f_o will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q in turn is dependent on the unloaded Q of inductor L, R_g and the FET input resistance.

Next consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of C_{gd} plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

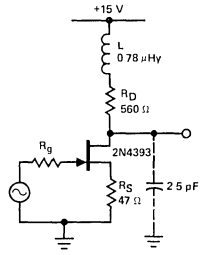


Figure 8

The required value of L is:

$$L = \frac{R_D{}^2C}{2}, \text{ and for the circuit in Figure 8.} \quad (24)$$

$$= 0.78\ \mu\text{H} \quad (25)$$

where

$$R_D = 560\ \Omega \quad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM\ PROBE} \quad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5 \text{ pF} \quad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz giving a gain bandwidth product of:

$$67 \times 4.2 = 281 \text{ MHz} \quad (29)$$

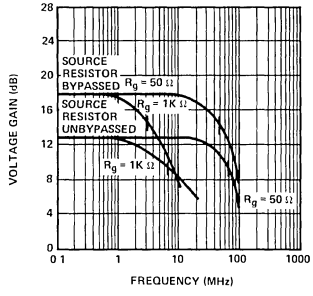


Figure 9

7

When R_S is bypassed by a 0.1 capacitor, the low frequency voltage gain is given simply by:

$$A_V = g_{fs}R_D \quad (30)$$

$$= 15 \times 10^{-3} \times 560 \quad (31)$$

$$= 8.4\ (18.5\ dB) \quad (32)$$

The gain bandwidth product tends to remain constant whether R_S is bypassed or not and this effect is shown in Figure 9.

Source-Follower Circuit[2]

A J300 is used in the FET source-follower circuit, Figure 10, because of its low input capacitance and high g_{fs} which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of g_{fs} which is independent of frequency up to about 600 MHz. The input capacitance is $C_{gd} + C_{gs}(1 - A_V)$ which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance R_o.

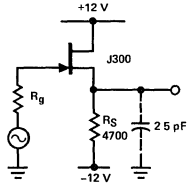


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when R_g is increased to 1K ohm the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to $1/f^2$ as explained in the section, "Behavior of Input Resistance," and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when R_S is 1000 ohms, the input resistance is real at this frequency.

The voltage gain of a source follower is given by:

$$A_V = \frac{g_{fs}R_S}{1 + g_{fs}R_S} \quad (33)$$

Thus A_V is almost independent of R_S when R_S is large. Using typical values for the J300 (or ½ 2N5912) in Figure 10, the drain current is 3 mA, g_{fs} is 5 mmho and R_S 4700 ohms,

$A_V = 0.96$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by:

$$R_o = \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200\ \Omega \quad (34)$$

and in this circuit, R_o was measured at 165 ohms. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

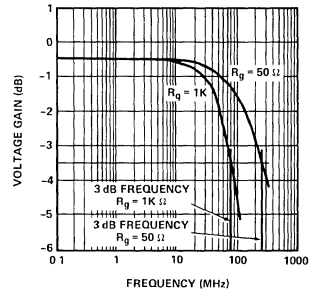


Figure 11

Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high stability oscillators or in low level power amplifiers[2] mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration, Figure 12, are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V)\,C_{dg} \quad (35)$$

$$C_{in} = C_{iss} + C_{gd} \quad (36)$$

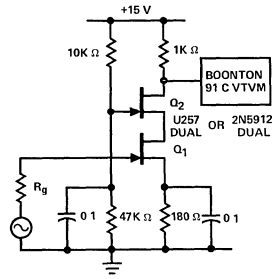


Figure 12

where A_V is the voltage gain from Q_1 gate to Q_1 drain which is essentially unity. C_{iss} for the U257 dual FET is 5 pF and C_{dg} is 1 pF, therefore

$C_{in} = 5 + 1 = 6$ pF, excluding strays of 4 pF

Thus Miller effect is minimized and a good gain bandwidth product is achieved.

Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB (x 5.6) and the bandwidth is 24.5 MHz with a generator impedance of 50 ohms. Gain bandwidth product is 137 MHz.

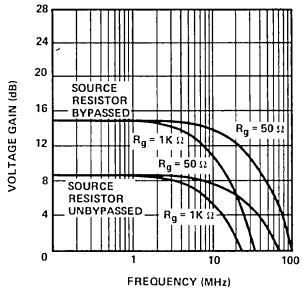


Figure 13

FET and Bipolar Cascade

The FET and bipolar transistor combination of Figure 14 makes a good video amplifier because the FET input provides the voltage gain thus obtaining a superior gain bandwidth product. The feedback capacitor a-c couples the emitter to the drain. The a-c voltage at the gate is nearly equal to that at the source. This source voltage is d-c coupled to the base.

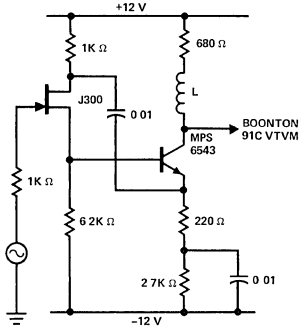


Figure 14

This produces an a-c voltage at the emitter whose amplitude is almost equal to that at the base. Thus at the FET, $v_g \cong v_s \cong v_d$ and all three signals are in phase. In this way Miller effect capacitance is largely eliminated.

The frequency response of this circuit is controlled by the output time constant if f_t of the transistor is much greater than the amplifier bandwidth. In the circuit shown the a-c load is 2.5 pF.

CONCLUSION

The input resistance of a FET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first: in the example, the low frequency gain is 4.5 and the 30-dB bandwidth 44 MHz (gain bandwidth 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with GBW almost 300 MHz and an output resistance of $1/g_{fs}$. The cascode circuit features a low input capacitance and GBW of 137 MHz. The circuit featuring the best gain bandwidth is the FET and bipolar combination. A gain of 11 dB and bandwidth of 90 MHz is achieved.

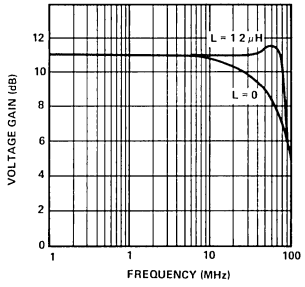
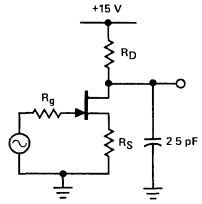


Figure 15

Selection of Video Amplifier Designs with Performance Summary

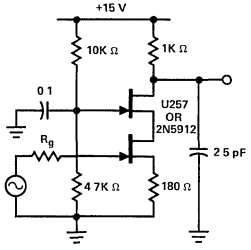
Note. All output voltages measured with Boonton 91C VTVM.

Common Source Stage



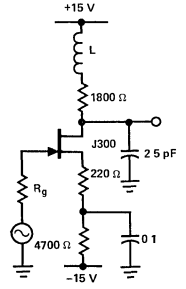
Device	R_g Ω	R_S Bypassed	R_S Ω	R_D Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
2N4393	50		47	560	4.5	13.0		44	197
	50	x	47	560	7.5	17.5		40	300
	1K		47	560	4.5	13.0		5.0	22
	1K	x	47	560	7.5	17.5		3.5	26
J300	50		91	1K	3.8	11.6	11.0	27.5	103
½	50	x	91	1K	6.3	16.0	14.5	30.0	189
2N5912	1K		91	1K	3.8	11.6	11.0	9.5	36
	1K	x	91	1K	6.3	16.0	14.5	6.5	41
2N4416	50		120	1.5K	3.9	11.8	11.5	25	98
	50	x	120	1.5K	6.2	15.8	13	19	118
	1K		120	1.5K	3.9	11.8	11.5	8	31
	1K	x	120	1.5K	6.2	15.8	13	7	44

Cascode



R_g Ω	R_S Bypassed	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		2.7	8.5	9	27	73
50	x	5.6	15	11.5	27	151
1K		2.7	8.5	9	9.5	73
1K	x	5.6	15	11.5	9.0	51

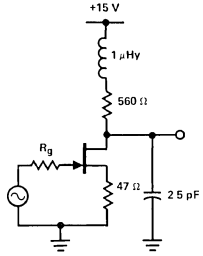
Common-Source Circuit



R_g Ω	L μH	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	0	3.5	11	2	20	70
1K	0	3.5	11	2	11	38.5
50	8	3.5	11	2	37	130
1K	15	3.5	11	2	17	60

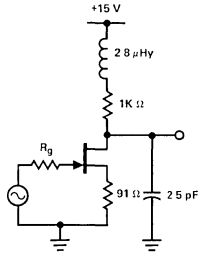
Shunt-Peaked Common-Source Stage

2N4393



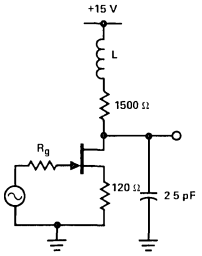
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		4.2	12.5	66	277
50	x	7.5	17.5	54	405
1K		4.2	12.5	6.0	25
1K	x	7.5	17.5	3.5	26

J300
(½2N5911/12)



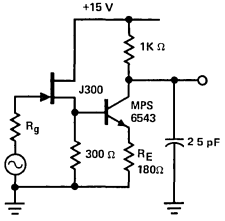
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		3.9	11.8	67	262
50	x	6.3	16.0	67	421

2N4416

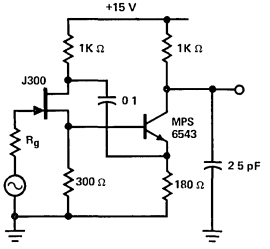


R_g Ω	L μH	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50	4		3.9	11.8	45	175
50	4	x	6.2	15.8	40	248
50	5	x	6.2	15.8	45	279

Common-Drain Common-Emitter Stage



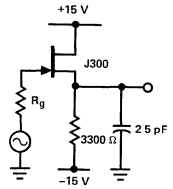
R_g Ω	R_E Bypassed (0.1 μF)	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		3	9.5	2.0	39	117
50	x	25	28	2.0	21	525
1K		3	9.5	2.0	13	39
1K	x	25	28	2.0	11	275



R_g Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	5.6	15	1.0	32	179
1K	5.6	15	1.0	15	84

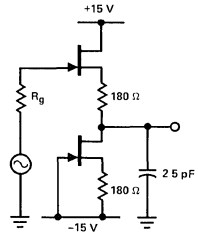
7

Source-Follower Circuit



R_g Ω	Gain	C_{in} Stray pF	C_{in} Total pF	R_o Ω	BW MHz	GBW MHz
50	0.92	2.2	2.7	165	350	326
1K	0.92	2.2	2.7	165	55	50

Note. R_o = output resistance of the source follower.



Dual FET	R_g Ω	Offset (Max) (Input to Output) mV	Gain	BW MHz	GBW MHz
U257	50	100	0.98	70	69
2N5912	1K	100	0.98	15	14.7
U232	50	10	0.98	85	83
	1K	10	0.98	13	12.7

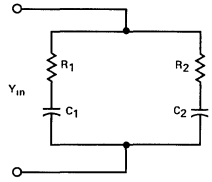
Derivation of Input Admittance Terms

where

$R_1 = R_{gs}$ $C_1 = C_{gs}$ (1)

$R_2 = R_{gd}$ $C_2 = C_{gd}$ (2)

$s = j\omega$



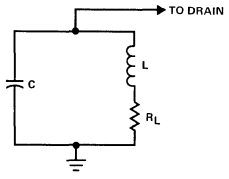
$$Y_{in} = \frac{sC_1}{R_1C_1\,s+1} + \frac{sC_2}{R_2C_2\,s+1} \quad (3)$$

$$= \frac{-\omega^2C_1C_2(R_1+R_2) + s(C_1+C_2)}{(1-\omega^2R_1R_2C_1C_2) + s(C_1R_1+C_2R_2)} \quad (4)$$

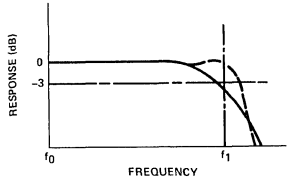
Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Figure below. The total impedance seen by the drain is given by:

$$Z = \left[\frac{R_L^2+\omega^2L^2}{(1-\omega^2LC)^2+\omega^2C^2R_L^2}\right]^{\frac{1}{2}} \quad (5)$$



The response below shows the "normal" 3-dB frequency without peaking – f_1. It is now required to raise the response at f_1 by 3 dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f_1 must equal the impedance seen by the drain at f_o. Also at f_1, $X_C = R_L$. Substituting for X_C in Equation 5:



$$R_L^2 = \frac{R_L^2+\omega^2L^2}{\left(1-\frac{\omega L}{R_L}^2+1\right)} \quad (6)$$

$$R_L^2 - 2\omega LR_L + \omega^2L^2 + R_L^2 = R_L^2 + \omega^2L^2 \quad (7)$$

$$R_L^2 = 2\omega LR_L \quad (8)$$

$$R_L = 2\omega L \quad (9)$$

$$L = \frac{R_L}{4\pi f_1} \quad (10)$$

and

$$f_1 = \frac{1}{2\pi R_LC}, \therefore L = \frac{R_L^2C}{2} \quad (11)$$

REFERENCES

1. Sherwin, J.S., "Liberate Your FET Amplifier," Electronic Design, May 1970.
2. Siliconix Application Tip, "FET Cascode Circuits Reduce Feedback Capacitance," August 1970.

Audio-Frequency Noise Characteristics of Junction FETs

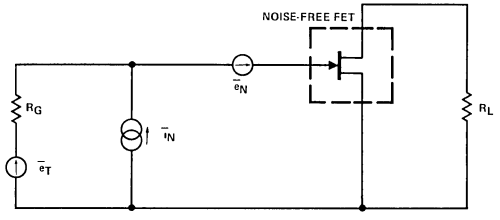
Bruce Watson

INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors. Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the FET, and how those characteristics may be specified by production-oriented test parameters.

Defining FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources, $\bar{e}_N$ and $\bar{i}_N$. These noise sources are chosen to have the same output as would an actual noisy FET. An equivalent circuit is shown in Figure 1.



Representing Noise in an Ideal FET
Figure 1

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise factor, a source resistor R_G, with a thermal noise voltage $\bar{e}_T$, is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across R_G is[1]

$$\bar{e}_T = \sqrt{4kTR_GB} \qquad (1)$$

where $k = 1.380 \times 10^{-23}$ Joules/°K (Boltzmann's Constant), T = temperature in °K, and B = bandwidth in Hz. Therefore noise power due to R_G is

$$\frac{\bar{e}_T^2}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \qquad (2)$$

7

The noise power of the FET referred to the input is

$$\frac{\bar{e}_N^2}{R_G} + i_N^2 \cdot R_G \tag{3}$$

When expressions for the noise power of both the FET and R_G are substituted, the noise factor becomes

$$F = 1 + \frac{\bar{e}_N^2 + \bar{i}_N^2 R_G^2}{4kTR_GB} \tag{4}$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance R_G:

$$NF = 10 \log_{10} [F] \tag{5}$$

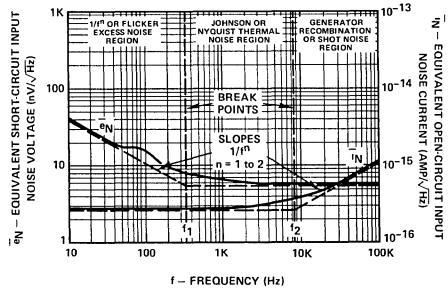
The noise figure of the FET is

$$NF = 10 \log_{10} \left[1 + \frac{\bar{e}_N^2 + \bar{i}_N^2 R_G^2}{4kTR_GB} \right] dB \tag{6}$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises in that the noise figure value is dependent upon the value of the generator resistance, R_G. Therefore, the $\bar{e}_N$, $\bar{i}_N$ method remains as the best way to quantitatively express the noise characteristics of the FET itself.

Describing Junction FET Noise Characteristics

Junction FET $\bar{e}_N$ and $\bar{i}_N$ characteristics are frequency-dependent within the audio noise spectrum, and take a form as shown in Figure 2.



Characteristics of Junction FET Noise
Figure 2

$\bar{e}_N$, the equivalent short circuit input noise voltage (with the exception of the $1/f^n$ region), is defined as[2]

$$\bar{e}_N = \sqrt{4kTR_NB} \tag{7}$$

where $R_N \cong 0.67/g_{fs}$, the equivalent resistance for noise. The $\bar{e}_N$, except in the $1/f^n$ region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called $1/f^n$ region, $\bar{e}_N$ is expressed as

$$\bar{e}_N = \sqrt{4KR_NB(1 + f_1/f^n)} \tag{8}$$

where n varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in $\bar{e}_N$ in the $1/f^n$ region has been observed to some extent in all junction FETs submitted to test. The breakpoint or corner frequency shown as f_1 in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8), $\bar{e}_N$ is inversely proportional to the square root of the transconductance of the FET ($\bar{e}_N \propto 1/\sqrt{g_{fs}}$). $\bar{e}_N$ can be lowered by a factor of $1/\sqrt{N}$ if N devices with matched electrical characteristics are connected parallel. For example, when

$$N = 2 \tag{9}$$

let

$$\bar{e}_{N1} = \bar{e}_{N2} \tag{10}$$

and let

$$g_{fs1} = g_{fs2} \tag{11}$$

Thus,

$$g_{fs}TOTAL = 2\, g_{fs1} \text{ or } 2\, g_{fs2} \tag{12}$$

From Equation (7)

$$\bar{e}_{N1} = \sqrt{4kT(0.67/g_{fs1})B} \tag{13}$$

and

$$\bar{e}_N TOTAL = \sqrt{4kT(0.67/2g_{fs1})B} \tag{14}$$

Thus,

$$\bar{e}_N TOTAL = \frac{1}{\sqrt{2}}\, \bar{e}_{N1} \tag{15}$$

A second way to achieve low $\bar{e}_N$ is to use a device with a large gate area. Empirically, $\bar{e}_N$ is inversely proportional to the square of the gate area ($\bar{e}_N \propto 1/A_G^2$), independent of g_{fs}. This large gate area philosophy has been followed in the

design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this Application Note. A major advantage of this type of design is that $\bar{e}_N$ is significantly lowered and $\bar{i}_N$ also remains at a low value.

The equivalent open-circuit input noise current, $\bar{i}_N$, with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\bar{i}_N = \sqrt{2qI_GB} \qquad (16)$$

where $q = 1.602 \times 10^{-19}$ coulomb (the magnitude of the electron charge), I_G is the measured DC operating gate current in amperes, and B is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2, $\bar{i}_N$ can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:(3)

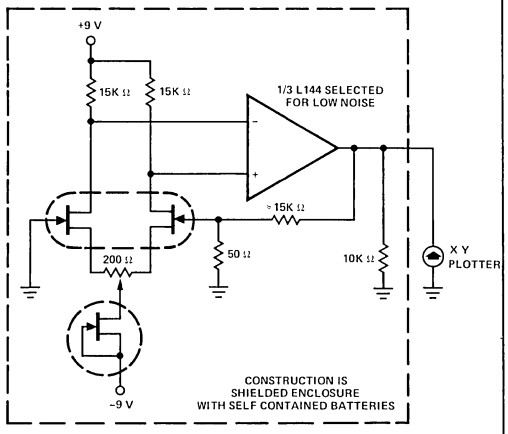
$$\bar{i}_N = \sqrt{\frac{4kTB}{R_p}} \qquad (17)$$

where R_p is the real part of the gate-to-source input impedance. The breakpoint or corner frequency f_2 in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

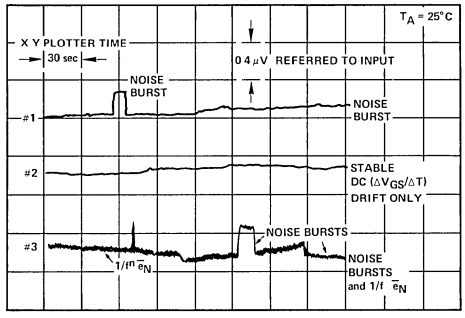
Popcorn noise is a form of random burst input noise current which remains at the same amplitude, and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidation processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, and not on a production-line basis. No correlation between $1/f^n$ noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then $1/f^n$ noise voltage ($\bar{e}_N$) is masked and difficult to evaluate at 10 Hz.



Test Circuit to Measure Popcorn Noise
Figure 3

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.



Popcorn Noise in Differential Amplifiers
Figure 4

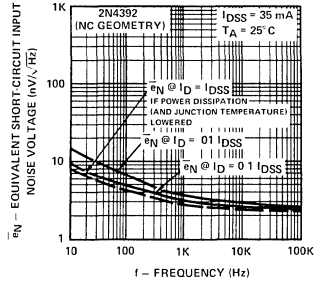
Operating Point Considerations

Unlike bipolar transistors, where $\bar{e}_N$ and $\bar{i}_N$ characteristics vary directly with change in collector current (I_C), similar characteristics in junction FETs will vary only slightly as drain current (I_D) is varied. This is true so long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ($V_{DS} > V_p$ or $V_{GS(off)}$).

The $\bar{e}_N$ in junction FETs will be lowest when the devices are operated at $V_{GS} = 0$ ($I_D = I_{DSS}$), where transconductance (g_{fs}) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

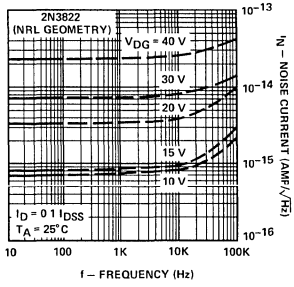
7

The curves in Figure 5 illustrate changes in $\bar{e}_N$ as the operating drain current (I_D) is varied. Note that the lowest $\bar{e}_N$ did not occur at V_{GS} = 0, because of high power dissipation and a resultant rise in junction temperature at the operating point.



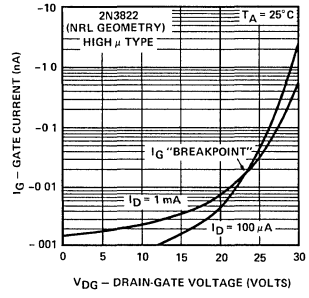
$\bar{e}_N$ Changes vs I_D Variations
Figure 5

The optimum (lowest) $\bar{i}_N$ in depletion-mode junction FETs should occur at V_{GS} = 0 (I_D = I_{DSS}). In practice, very little change will be seen in $\bar{i}_N$ when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current (I_G) breakpoint and power dissipation is kept at a low level. The curves in Figure 6 illustrate $\bar{i}_N$ characteristics as a function of drain-gate voltage at points below, on, and above the I_G breakpoint voltage.

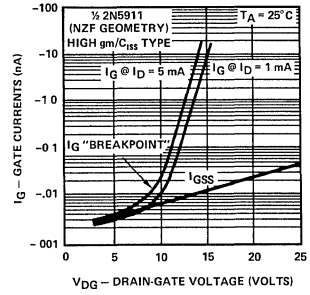


$\bar{i}_N$ Characteristics as Function of Drain-Gate Voltage
Figure 6

In circuit design, particular attention must be paid to drain-gate voltage (V_{DG}) to minimize gate current (I_G) under operating conditions. The critical drain-gate voltage (I_G breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design.[4] Gate operating current (I_G) should not be considered equal to gate reverse current (I_{GSS}) in linear amplifier applications. I_{GSS} is only an indication of reverse-biased junction leakage under non-operating conditions. The Curves in Figures 7 and 8 show how I_G breakpoint is related to basic device design. Device designs with a high g_{fs}/C_{iss} ratio have low breakpoint voltages, typically at V_{DG} = 10 V, whereas high μ devices ($\mu = r_{ds} \cdot g_{fs}$). have much higher I_G breakpoints, typically V_{DG} = 20 – 30 V.



Gate Operating Current vs Drain-Gate Voltage
Figure 7

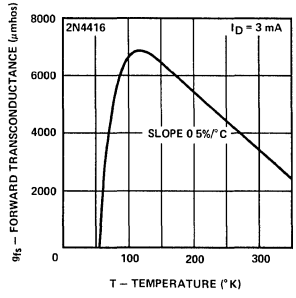


Gate Currents vs Drain-Gate Voltage
Figure 8

Characteristics of $\bar{e}_N$ and $\bar{i}_N$ at Low Temperature

Three equations presented earlier ((7), (16) and (17)) show that $\bar{e}_N$ and $\bar{i}_N$ are temperature dependent. $\bar{e}_N$ and $\bar{i}_N$ are proportional to $\sqrt{T}$, and both will be reduced if the temperature is lowered. In Equation (16), $\bar{i}_N$ is proportional to $\sqrt{I_G}$; I_G will halve for each temperature drop of 10 to 11°C. $\bar{e}_N$ is also proportional to $\sqrt{R_N}$, where $R_N \cong 0.67/g_{fs}$. Thus when g_{fs} is increased, which is typical of junction FETs operating at low temperature, $\bar{e}_N$ will also lower.

In Figure 9, g_{fs} has been plotted vs temperature for a silicon junction FET, and the low temperature limitation caused by a dropoff in g_{fs} is clearly shown.



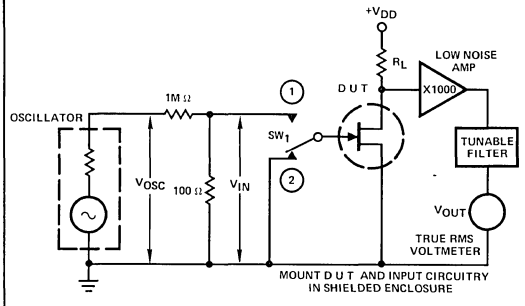
g_{fs} vs Temperature
Figure 9

In connection with the plot of g_{fs} vs temperature, note that the relationship can vary from approximately 0.2% to 1% per degree C. The g_{fs} slope depends upon the basic design of the FET, and upon the proximity of the drain current operating point to I_{DZ}, the zero temperature coefficient point.

The major application for junction FETs at low temperature is in charge-sensitive amplifiers.[5] For best performance in this type of application, a high g_{fs}/C_{iss} ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 (NH geometry) and the U311 (NZA geometry).

Test Measurements

By definition, $\bar{e}_N$ and $\bar{i}_N$ are referred to the input of the device under test. To measure $\bar{e}_N$, the test circuit shown in Figure 10 will prove useful.



Test Circuit to Measure $\bar{e}_N$
Figure 10

The following procedure should be used to make the $\bar{e}_N$ test:

1. Set tunable filter to required f_{low} and f_{high}. Adjust oscillator to mean center frequency ($f_{mean} = [f_{low} \cdot f_{high}]^{1/2}$).
2. Set V_{osc} to 100 mV with Switch 1 in position (1). Compute $V_{in1} = 10^{-1} \times \frac{10^2}{10^6} = 10^{-5}$ V = 10 μV.
3. Measure V_{out1}. Compute overall gain as $A_v = \frac{V_{out1}}{V_{in1}} = \frac{V_{out1}}{10\,\mu V}$.
4. Set Switch 1 to position (2) and measure V_{out2}. Compute V_{in2}, the equivalent short-circuit input noise voltage ($\bar{e}_N$), using A_v from Step 3. $V_{in2} = \frac{V_{out2}}{A_v} = \bar{e}_N$ in volts over bandwidth f_{low} to f_{high}.

An alternate method of performing the above test is to use a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring $\bar{e}_N$ and determining NF with various values of R_G in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure $\bar{e}_N$ at certain frequencies over certain bandwidths in the $1/f^n$ region. The rms noise over a bandwidth from f_{low} to f_{high}, where there is a $1/f^n$ characteristic over the entire range, can be computed as

$$\bar{e}_N = \left[\bar{e}_N \text{ known}\right] \cdot \left[f_{known} \cdot \ln\left(\frac{f_{high}}{f_{low}}\right)\right]^{1/2n} \qquad (18)$$

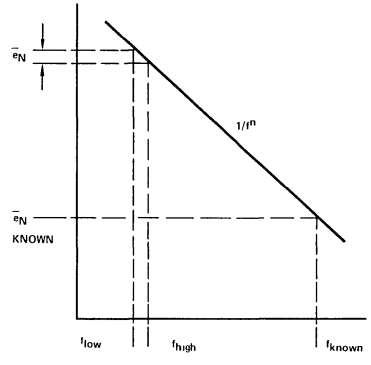
Figure 11 represents this equation graphically. For example, $\bar{e}_N$ known = 70 x 10^{-9} V/$\sqrt{\text{Hz}}$ at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a $1/f^1$ characteristic over the entire range. Thus

$$\bar{e}_N = \left[70 \times 10^{-9}\right] \cdot \left[10 \cdot \ln\left(\frac{5.5}{4.5}\right)\right]^{1/2} \text{ Volts} \qquad (19)$$

or

$$\bar{e}_N = 99.16 \times 10^{-9} \text{ V}/\sqrt{\text{Hz}} \text{ @ } 4.975 \text{ Hz}, \qquad (20)$$

4.975 Hz is the mean center frequency where $f_{mean} = (f_{low} \cdot f_{high})^{1/2}$.



Computing rms Noise Over a Bandwidth
Figure 11

$\bar{i}_N$ measurements are difficult to implement at best. At frequencies below f_2 in Figure 2, $\bar{i}_N$ is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current, I_G. From Equation (16) I_G is established as the measured bulk gate current. Because measured gate current (I_G) is the result of all conductances at the gate, the resultant gate current and the computed $\bar{i}_N$ due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by[6]

$$\bar{e}_{ni}^2 = \bar{e}_T^2 + \bar{e}_N^2 + \bar{i}_N^2 \cdot R_G^2 \quad (21)$$

where $\bar{e}_T^2$ is the thermal noise of the generator resistance R_G and $\bar{e}_{ni}^2$ is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that $\bar{i}_N^2$ can be calculated if $\bar{e}_N^2$, $\bar{e}_T^2$ and total noise $\bar{e}_{ni}^2$ are known. The difficulty here is that in MOS or junction FETs, the R_G must be very large to detect the anticipated small value of $\bar{i}_N$. However, when R_G is very large $\bar{e}_T^2$ is much greater than $\bar{i}_N^2 \cdot R_G^2$. For example, over a 1 Hz bandwidth at 25°C, if R_G is equal to 100 MΩ, then

$$\bar{e}_T^2 = 4kTR_G = 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8 = 1.63 \times 10^{-12}\ V/\sqrt{Hz}. \quad (22)$$

Anticipated $\bar{i}_N$ is

$$\bar{i}_N \approx 10^{-15}\ \text{Amperes}/\sqrt{Hz} \quad (23)$$

and

$$\bar{i}_N^2 = 10^{-30}\ \text{Amperes}/\sqrt{Hz}. \quad (24)$$

Thus

$$\bar{i}_N^2 \cdot R_G^2 = 10^{-30} \cdot 10^{16} = 10^{-14}\ V/\sqrt{Hz}. \quad (25)$$

Therefore, $\bar{i}_N^2 \cdot R_G^2$ is much less than $\bar{e}_T^2$, which renders this method of finding $\bar{i}_N$ impractical for most common MOS FETs or junction FETs.

An improved method of measuring $\bar{i}_N^2$ is to substitute a low-loss mica capacitor for resistor R_G. The mica capacitor by definition does not have equivalent thermal noise voltage, and thus Equation (21) becomes

$$\bar{e}_{ni}^2 = \bar{e}_N^2 + \bar{i}_N^2 \cdot X_C^2 \quad (26)$$

(where X_C = capacitive reactance)

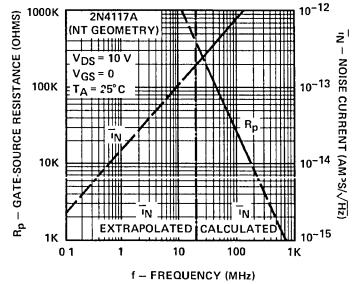
or

$$\bar{i}_N = \frac{(\bar{e}_{ni}^2 - \bar{e}_N^2)^{1/2}}{X_C} \quad (27)$$

When a 10 pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz) a correlation of from 80 to 90% was obtained when compared to $\bar{i}_N^2$ computed from measured gate current readings.

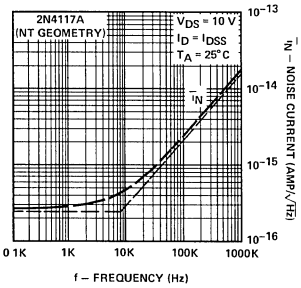
At frequencies above 100 Hz direct computation of $\bar{i}_N$ via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

In calculating $\bar{i}_N$ at higher frequencies, an alternate method is to measure (R_p) the real part of the gate-source impedance of the FET.[7] When R_p is measured at various frequencies, the equivalent short-circuit input noise current ($\bar{i}_N$) can be computed as a function of frequency (See Equation (17)). A convenient instrument to measure R_p is the Hewlett-Packard Type 250A Rx meter or equivalent. The Type 250A Rx meter can measure R_p accurately up to 200K ohms. As is shown in Figure 12, this establishes the low frequency limit of 20 MHz for $\bar{i}_N$ computed via direct measurement of R_p for the Siliconix FET Type 2N4117A. For frequencies between 100 Hz and 20 MHz, $\bar{i}_N$ must be extrapolated, as is shown in Figures 12 and 13. For FET types with lower R_p (such as the Siliconix 2N4393) $\bar{i}_N$ can be computed down to 2 MHz, and hence extrapolated $\bar{i}_N$ between 100 Hz and 100 kHz is more accurate.



Low Frequency Limit for Calculated $\bar{i}_N$

Figure 12

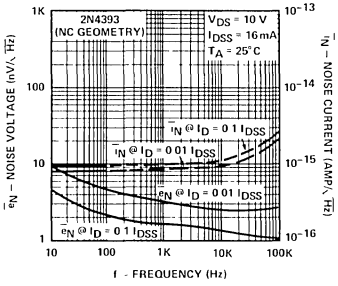


Extrapolated $\bar{i}_N$ vs Frequency

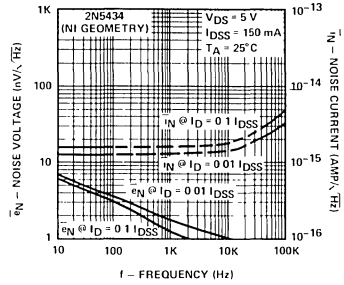
Figure 13

The following are representative $\overline{e_N}$, $\overline{i_N}$ curves for Siliconix J-FET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.

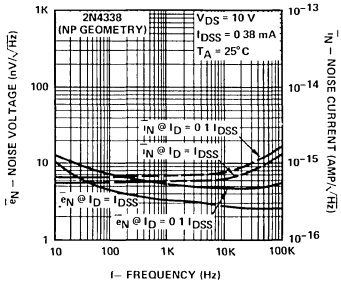
NCB



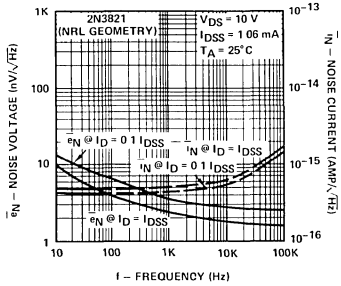
NIP



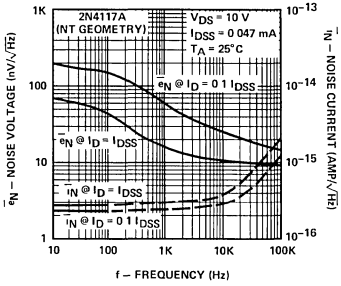
NPA



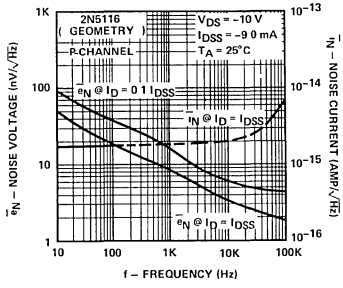
NRL



NT



PSA



FET Noise Characteristics by Geometry
Figure 14

CONCLUSION

Contemporary junction FETs have noise voltages ($\bar{e}_N$) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current ($\bar{i}_N$) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this Application Note, the excellent low-noise characteristics of high g_{fs} junction FETs can be realized.

The curves shown in Figure 14 are representative of $\bar{e}_N$ and $\bar{i}_N$ performance of Siliconix junction FETs. Of particular importance in these curves is the process geometry by which the basic design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data, and for specific part numbers stemming from the generic process geometries.

In the measurement section of this Application Note, it was shown that direct $\bar{e}_N$ measurements can readily be made. $\bar{i}_N$ can be guaranteed at frequencies below 100 Hz by measuring the DC operating gate current (I_G). When I_G is known, $\bar{i}_N$ can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

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Differential JFET Amplifier

Ted List

The discrete JFET differential amplifier has many performance advantages over its integrated circuit equivalent. In particular, the noise levels and input leakage currents can be significantly lower. Given adequate device characterization data, designing a discrete amplifier is a simple two-step procedure.

For example, the U401 is a monolithic dual JFET used in low-noise JFET-input amplifiers, low-to-medium frequency amplifiers, precision instrumentation amplifiers and comparators. The device has an excellent offset voltage rating (5mV) and normally does not need thermal and offset adjustments in the circuit because the two JFETs are closely matched. The characteristics are guaranteed at 15V and 200μA, Table 1, and the equivalent input noise is specified at $20nV/\sqrt{Hz}$ maximum at 10Hz.

Two steps are required to design a circuit with good gain and noise characteristics.

Step 1: Using the circuit shown in Figure 1, assume ±15V supplies are available ($\pm V_1$). The source voltage V_S is set equal to zero so that 15V appears across the current-limiting diode, CR_1. Since the JFETs are characterized and production tested at 200μA, choose a current-limiting diode with a forward-current rating close to 400μA (200μA quiescent current in each JFET).

The CR043, for instance, is rated at 430μA and operates well with a 15V drop across it. The remaining 15V is divided between the JFETs and the drain resistors. The 7.5V across the JFETs is more than sufficient for operation in the saturation region.

Step 2: Calculate the value of the drain resistors from their voltage drop (7.5V) and current (215μA):

$$R_{L1} = R_{L2} = {}^{7.5}/_{0.215} = 34.884k\Omega$$

The nearest standard 5% value to 34.88kΩ is 36kΩ; 33kΩ could also be used.

In summary.

$+V_1 = +15V$
$-V_1 = -15V$
Q_1 and Q_2 = ½ U401
$R_{L1} = R_{L2} = 36k\Omega$ (3kΩ optional)
CR_1 = CR043

The amplifier characteristics are shown in Table 2.

Table 1 – U401 Partial List of Parameters

Parameters	Condition	Limits
$V_{GS(off)}$	$V_{DS} = 15V\ I_D = 1nA$	−0.5 to −2.5V
I_G	$V_{DS} = 15V\ I_D = 200\mu A$	−15pA
g_{fs}	$V_{DS} = 15V\ I_D = 200\mu A$	2 to 7mmhos
g_{os}	$V_{DS} = 15V\ I_D = 200\mu A$	20μmhos
C_{RSS}	$V_{DS} = 15V\ I_D = 200\mu A$	3pF
$\bar{e}_n$	$V_{DS} = 15V\ V_{GS} = 0V$	$20nV/\sqrt{Hz}$
$V_{GS1} - V_{GS2}$	$V_{DS} = 10V\ I_{DS} = 200\mu A$	5mV
$\Delta(V_{GS1} - V_{GS2})\ \Delta T$	$V_{DS} = 10V\ I_n = 200\mu A$	10μV/°C

Table 2 – Amplifier Characteristics

A_O	≅33
Z_O	≅31kΩ
I_{bias}	<15pA
e_{offset}	≅5mV
P_D	≅13mW

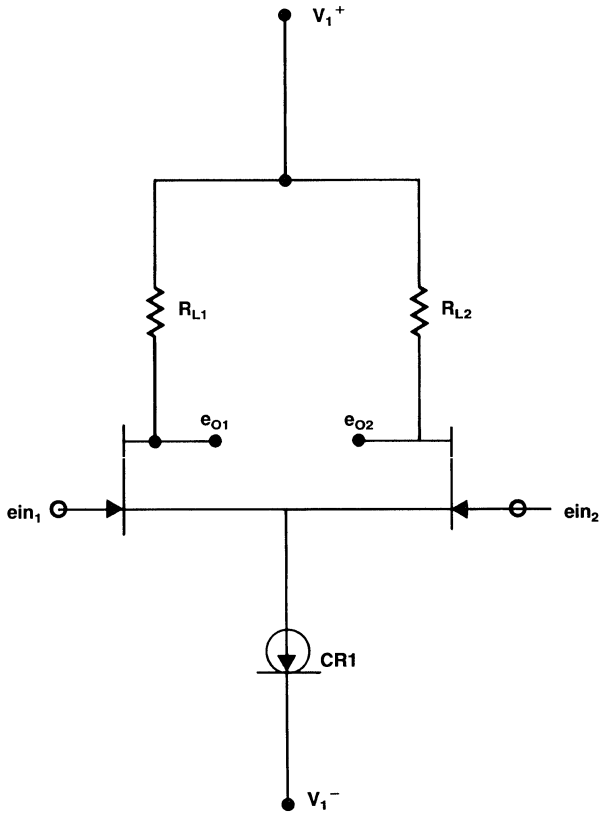


Figure 1

Wideband UHF Amplifier with High-Performance FETs

Ed Oxner

INTRODUCTION

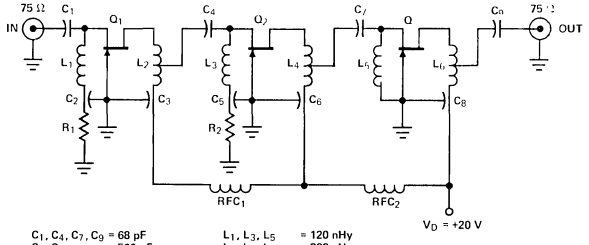
A new freedom in UHF amplifier design is possible with high-performance "Super FETs" such as the Siliconix U310 Junction FET. Typical advantages include a closely-matched 75 ohm input for extremely low return loss in cable systems, and high spurious response rejection with the 3rd order IM intercept measured at +29 dB.(1)

Additionally, the high common-gate forward transconductance of the U310 (20,000 μmho maximum) makes it possible to design an amplifier with wide bandwidth and good gain, since the figure of merit (g_m/C) of the FET is 2.35 x 10^9 typical – higher than any other known UHF Junction FET.

The amplifier circuit in Figure 1 is designed for 225 MHz center frequency, 1 dB bandwidth of 50 MHz, low input VSWR in a 75-ohm system, and 24 dB gain. Three stages of U310 FETs are used, in a straight forward design.

Typical parameters are taken from the U310 data sheet:

Forward Transconductance		14 mmhos
Input Admittance at 225 MHz	g_{igs}	13 mmhos
	b_{igs}	4 mmhos
Output Admittance at 225 MHz	g_{ogs}	0.27 mmhos
	b_{ogs}	2.6 mmhos



C1, C4, C7, C9 = 68 pF
C2, C5 = 500 pF
C3, C6, C8 = 1000 pF
Q1, Q2, Q3 = Siliconix U310
L1, L3, L5 = 120 nHy
L2, L4, L6 = 222 nHy
RFC1, RFC2 = 2.2 nHy
R1, R2 = 51 Ω

Figure 1

Input match is simplified because the FET input (real) impedance is nearly 77 ohms. A coupling capacitor is used in the amplifier, rather than a tuned circuit, and thus the values may be determined:

$$R_s\sqrt{\frac{R_{ig}}{R_s} - 1} = X_s = 75\sqrt{\frac{77}{75} - 1} = 11.85\ \Omega$$

$$C_s = \frac{1}{\omega X_s} \approx 68\ \text{pF}$$

$$X_P = \frac{R_s R_p}{X_s} = \frac{75 \times 77}{11.85} = 488\ \Omega$$

$$C_P = 1.47\ \text{pF}$$

$$C_T = 4.4\ \text{pF}\ (C_T = C_P + C_{igs})$$

$$L_s = \frac{1}{\omega^2 C_T} = 120\ \text{nHy}$$

Figure 2 shows that the measured input VSWR in the 75-ohm system indicated an available bandwidth considerably greater than that required for the amplifier design criteria.

Three cascaded synchronous single-tuned stages are used to achieve the desired gain, and thus stage bandwidth and Q are determined:[2]

$$\frac{B/W}{f} = \frac{1}{Q}\sqrt{\left(\frac{E_o}{E}\right)^2 - 1}$$

where:

$$\frac{\text{Bandwidth of 3 Stages}^{(3)}}{\text{Bandwidth of 1 Stage}} = \sqrt{2^{1/3} - 1}$$

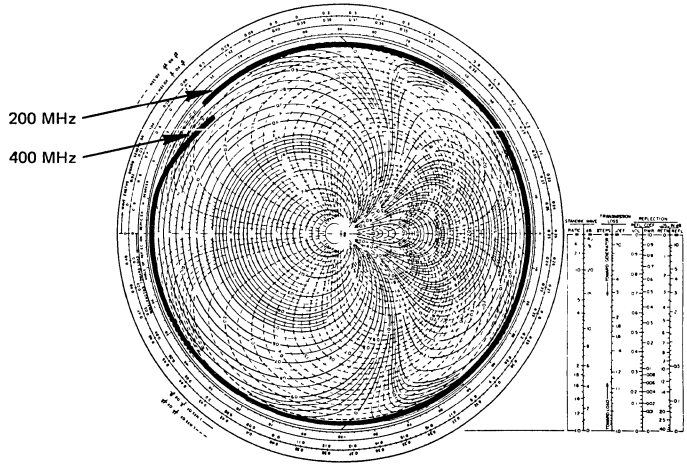
and

$$\left(\frac{E_o}{E}\right) = 1.122\ (1\ \text{dB})$$

giving

$$B/W\ (1\ \text{dB}) = 98\ \text{MHz}$$

$$Q = 1.15$$



Blanchard Chart (Inverted Circle Impedance Chart)
Figure 2

With a FET output impedance of 3700 ohms shunted by approximately 2.5 pF (with 0.5 pF allowed for stray capacitance), the total parallel resistance necessary to obtain the desired bandwidth is:

$$Q = \omega C R_t$$

$$R_t = \frac{1.15}{1.415 \times 10^9 \times 2.5 \times 10^{-12}} = 330\ \Omega$$

The tank circuit impedance appearing in shunt with the FET, is therefore calculated to be about 365 ohms. From this, the inductance is:

$$L = \frac{R}{\omega Q} = \frac{365}{\omega 1.15} = 222\ \text{nHy}$$

with a turns ratio of 2.3:1 to match to 75 ohms. Since each stage is designed for 75 ohm input and output, three cascaded stages complete the amplifier design.

The computed voltage gain per stage is approximately $g_{fs}\ R_{t/n}$ or 2.22 (7 dB). Measured gain for all three stages is 24 dB. The U310 FET in the final stage operates at I_{DSS}, and thus accounts for the higher measured gain. The gain/bandwidth response of the amplifier is shown in Figure 3.

The 3rd order spurious intercept point is plotted graphically in Figure 4.[4] The importance of a high intercept point becomes apparent in a crowded high-level area of the spectrum where signal purity is of utmost priority.

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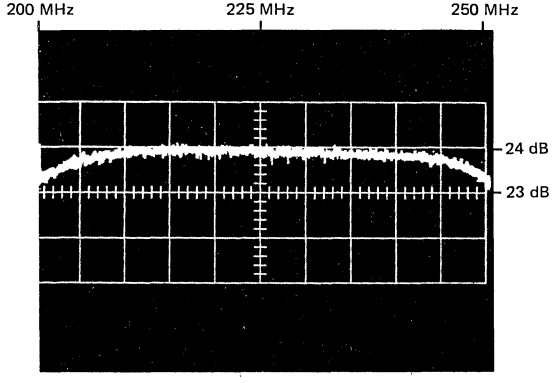


Figure 3

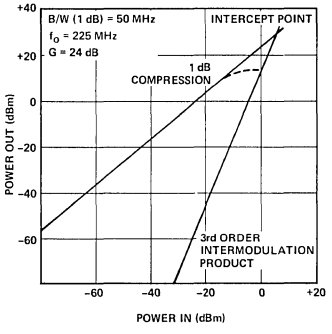


Figure 4

High-Performance FETs In Low-Noise VHF Oscillators

Ed Oxner

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. However, some receiver designs are available which overcome this limitation by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. There still remain certain limitations in dynamic range which cannot be remedied by parametric devices. In these cases, the problem lies in the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

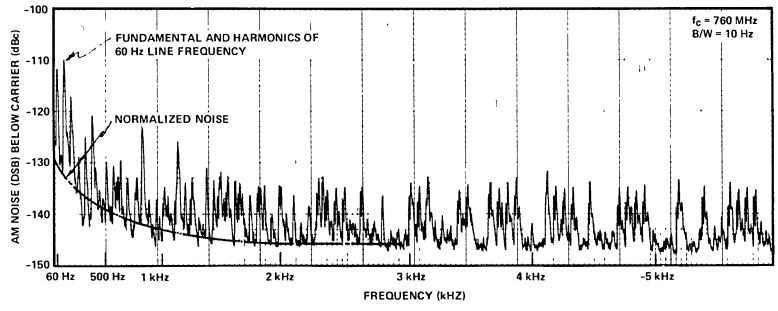
Common Types of Noise

Although noise is often difficult to characterize because of its random or nondeterministic nature, it is possible to differentiate various forms of noise through an understanding of the Gaussian distribution of noise about an RF carrier. Briefly stated, the three major forms of noise are (1) low-frequency noise (1/f); (2) thermal noise (4kTRB); and "shot" noise (i_n). Further, these types of noise can be identified from their relationship to the main RF carrier. For example, low-frequency noise predominates very close to the carrier, and falls to insignificant levels when it is displaced more than 250 Hz from the carrier. Low-frequency noise is associated with surface contamination and other irregularities, such as gate current leakage.

Thermal noise plays the predominant role in the region from the 1/f decay point to approximately 20 kHz from the carrier, and is commonly associated with equivalent resistance where the rms value of noise voltage of the Thevenin generator becomes the classic $(4kTBR)^{1/2}$. Noise appearing beyond the 20 kHz is known as Shot noise, and is directly attributable to noise current. Because of the typically uniform distribution of shot noise it is also referred to as "white noise."

Origins of Oscillator AM Noise

Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain close to the carrier is observed on a spectrum analyzer, noise appears as a modulation phenomenon. This observation would be greatly enhanced if the noise contribution was coherent and consisted of discrete sideband frequencies. Without a doubt, the major component of AM noise is the contribution of low-frequency noise (1/f). Both thermal and shot noise are relatively insignificant segments of AM noise when compared to 1/f. A graph of AM noise vs frequency removed is shown in Figure 1.

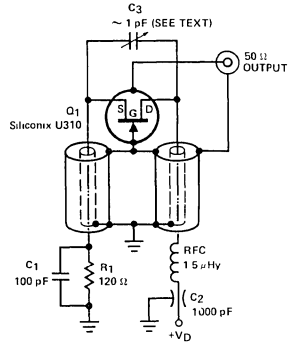


AM Noise vs Frequency Removed from the Carrier
Figure 1

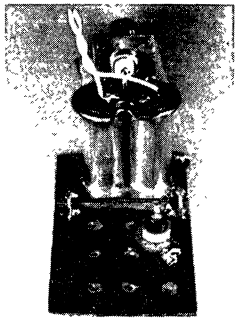
Design of a VHF Oscillator

The important design considerations for best oscillator performance include using a FET with high forward transconductance, maintaining the gate at ground potential, and keeping a high unloaded tank Q. The high transconductance is necessary to reduce the effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator design is somewhat extraordinary for a circuit employing a FET. The FET chosen was the Siliconix U310, which has a forward transconductance value higher than 18 mmho at zero bias ($V_{GS} = 0$). The oscillator basically consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is established by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Optimum resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 ohms. The oscillator circuit is shown in Figure 2, and construction details are shown in Figure 3.



Oscillator Circuit
Figure 2



Oscillator Construction Details
Figure 3

The technique to establish the proper resonator length for the desired frequency is somewhat tricky, and requires a first-order approximation of the anticipated capacitive fringing which derives from both the FET and the feedback network. A short circuited coaxial transmission line is theoretically resonant at a quarter-wave length of the resonating frequency, except for the effects of fringe field capacitance. At resonance

$$X_L = X_C \tag{1}$$

If the fringe capacitance is known, X_C can be calculated as

$$X_C = \frac{1}{\omega C} \tag{2}$$

From this, the resonator length can be determined as

$$X_C = \tan \beta \ell \tag{3}$$

In making these calculations, a Smith chart is invaluable, as is shown in the following illustration:

Frequency of oscillation	= 760 MHz	
FET b_{igs} (from data sheet)	= 16 mmho	
Capacitance from b_{igs}		C_{gs} = 3.4 pF
Allow for stray capacitance and the feedback network		C_S = 1.5 pF
		4.9 pF

Thus X_C = j 0.57 (normalized to 75 Ω)

Locate 0.57 on the Smith chart. The wavelength toward the load = 0.081 λ. Since a wavelength at 760 MHz is 39.5 cm., then the resonator cavity length is simply

$$39.5 \times 0.081 = 3.20 \text{ cm } (1.26 \text{ inches}) \tag{4}$$

In the completed FET coaxial oscillator circuit, the output coupling loop consists of a single turn made fast to the cavity by the BNC flange and the FET itself. Although the feedback network appears somewhat crude, it can be replaced by a small trimmer capacitor for similar operation.

Conclusions

Measured performance of the oscillator is shown in Table IA; AM noise measurements in a 10 Hz bandwidth are shown in Table IB.

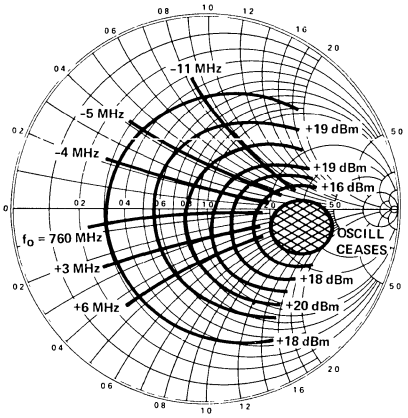
TABLE IA
Oscillator Measured Performance @ 25°C

V_{DD}(V)	+10	+15	+20	+25
I_D (mA)	15	16.2	18.2	21
P_{out} (dBm)	+6.6	+15.2	+18.3	+20
Frequency (MHz)	725	742.7	754.7	762.9

TABLE IB
AM Noise Measurement

Frequency Displaced From Carrier	dBc
50 Hz	-130
500 Hz	-139
1 kHz	-143.5
5 kHz	-146

The Reike diagram shown in Figure 4 makes possible the accurate prediction of expected power output and operating frequency with the oscillator feeding directly into a mismatched load. Expansion of the Reike diagram to show frequency vs transmission line length (in degrees) will allow prediction of the long-line effect on oscillator stability.



Reike Diagram
Figure 4

Siliconix

FETs in Balanced Mixers

Ed Oxner

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

Characteristic	MIXER TYPE		
	Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0 25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

Table II

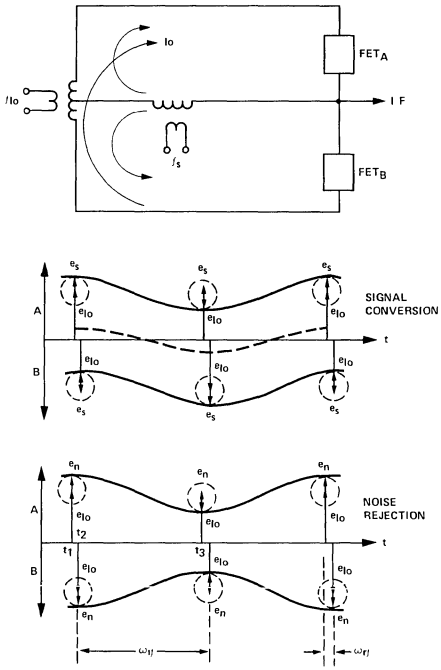
DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L.O Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain not possible at Optimum Square Law Response Level High L.O. Power
Dual-Gate MOS FET	Low IM Distortion AGC Square Law Characteristic	High Noise Figure Poor Burnout Level Unstable

those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors
Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{ift}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{lo}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° (ω_{ift}) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.(1)

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

(1) Intermodulation and Cross-Modulation
(2) Conversion Gain
(3) Noise Figure
(4) Selecting the Proper FET
(5) Local Oscillator Injection
(6) Designing the Input Transformer
(7) Designing the IF Network

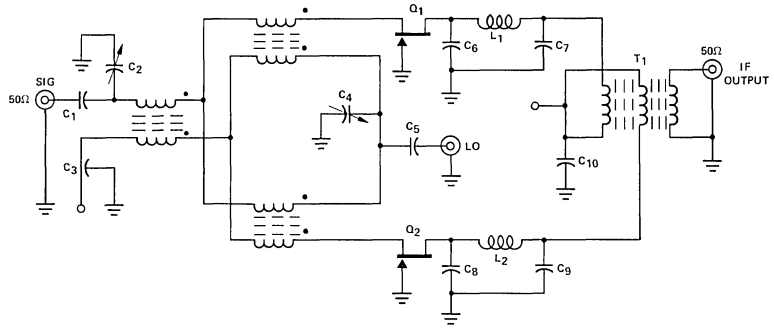
Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.(2)

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier.



C1, C5 – 01 μfd
C2, C4 – 1 - 10 pF
C3 – 1000 pF
C6, C8 – 30 pF
C7, C9 – 68 pF
C10 – 0 1 μF
L1, L2 – 1 3 μHy
Q1, Q2 – U310 (2) or U430
T1 – RELCOM BT-9

Prototype Active Balanced Mixer

Figure 2

Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_V, as:

$$A_V = g_c R_L \quad (1)$$

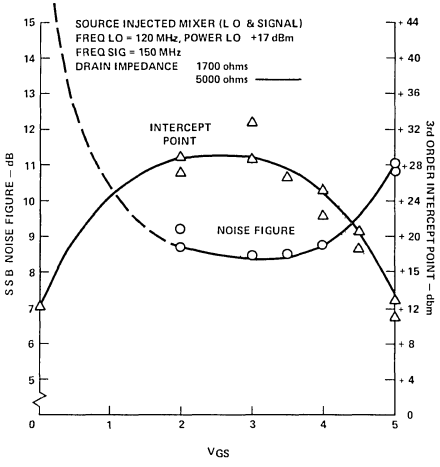
where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion – particularly intermodulation product distortion.

Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

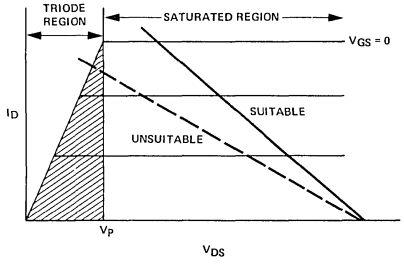
The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.(3) A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-sorce voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics.(4) A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



Comparison of Mixer IM Characteristics

Figure 3



Plotting Drain Load Lines

Figure 4

Conversion Gain

In a FET, forward transconductance is defined as[5]

$$g_{fs} = \frac{dI_D}{dV_{gs}} \tag{2}$$

and conversion transconductance is defined as[6]

$$g_c = \frac{dI_{D(\omega i)}}{dV_{gs(\omega r)}} \tag{3}$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \tag{4}$$

For square law operation[7]

$$V_2 + V_{GS} \leqslant V_{GS(off)} \tag{5}$$

Drain current is approximately defined by[8]

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \tag{6}$$

or[9]

$$I_D \approx \frac{g_{fso}\, V_{GS(off)}}{2}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \tag{7}$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}}\left[V_{GS(off)} - v_{gs}\right]^2 \tag{8}$$

then[10]

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \text{ (complex Taylor expansion)} \tag{9}$$

which can be reduced to

$$I_{D(IF)} \approx \frac{g_{fso}}{2V_{GS(off)}}\, V_1 V_2 \cos(\omega_1 - \omega_2)t \tag{10}$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}}\,|V_2| \tag{11}$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

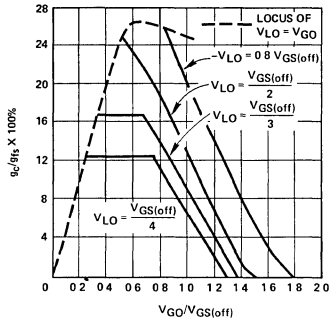
Thus

$$2\,V_{2\,peak} \leqslant V_{GS(off)} \tag{12}$$

or

$$V_{2\,peak} \leqslant \frac{V_{GS(off)}}{2} \tag{13}$$

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.



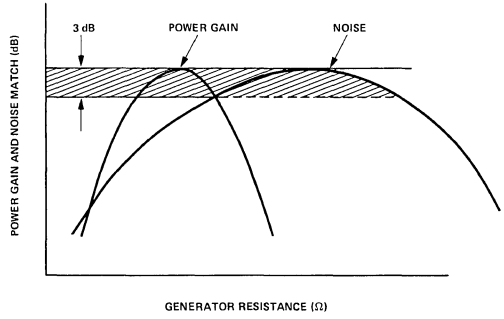
Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$ (from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.)

Figure 5

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g.[11] A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



Power Gain and Noise Matching

Figure 6

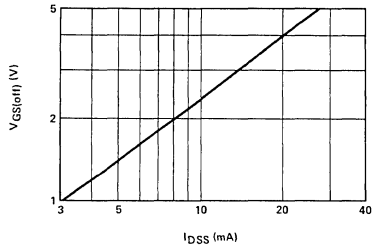
How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$:

$$g_c = \frac{I_{DSS}}{V_{GS(off)}^2} |V_2| \quad (14)$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \quad (15)$$

Equation 15 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7A and 7B show that devices from a family selected for high I_{DSS} do *not* provide high conversion transconductance, but actually produce a lower value of g_c.



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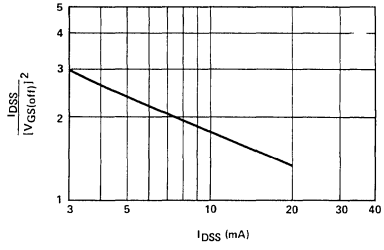


b.

Relationship of I_{DSS} and $V_{GS(off)}$
Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000 μmhos max at V_{DS} = 10 V, I_D = 10 mA, and f = 1 kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach – the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a numbei of possible alternatives to the U310.

Table III

Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

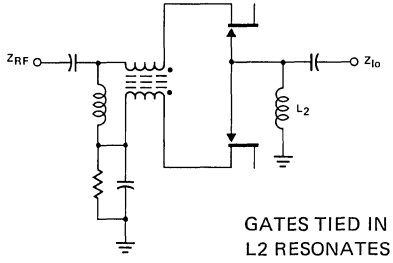
*Similar devices are also available in plastic packages:

U310 (J310)
2N4416 (2N5486, J304-18)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing, Two circuits to obtain direct gate coupling are suggested in Figure 8.



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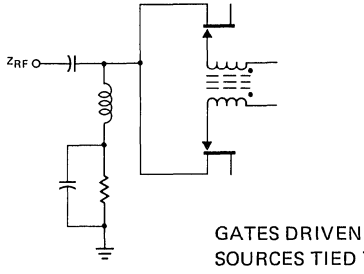


b.

Alternate Forms of L.O. Injection
Figure 8

The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer. best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

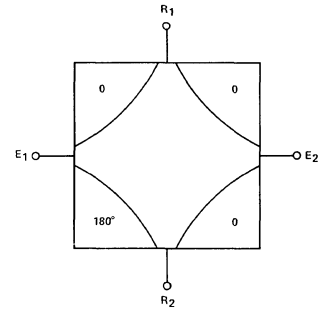
(1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B

(2) Offer a match between either input to a symmetrical balanced load

(3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)

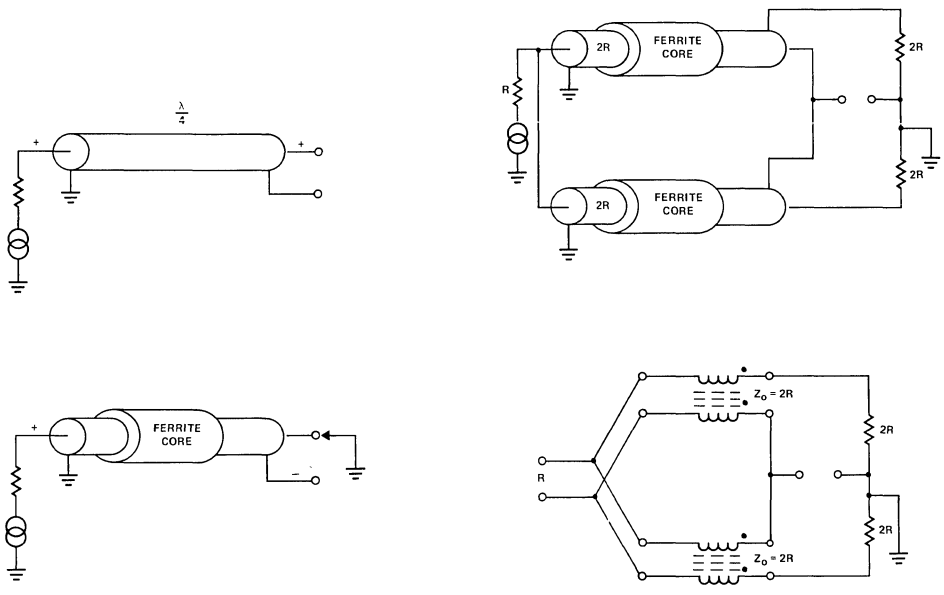
(4) Maintain a differential phase of 180° across the symmetrical balanced loads

(5) Introduce the least possible amount of loss



4-Port Hybrid with Phase and Isolation
Figure 9

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.[12] The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.[13]



Hybrid Input Coupling Transformer
Figure 10

Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.[14] The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \qquad (16)$$

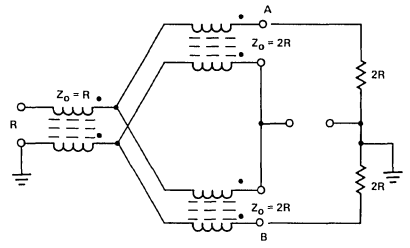
$$\text{min length} = \frac{20\,R_L}{(1 + \mu/\mu_o)\,f_{lower}} \text{ (inches)} \qquad (17)$$

where R_L = the load impedance, μ/μ_o = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.[15] A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line condcutors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_o, is to be preferred over a higher Z_o. Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_o = 100 ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2).[16] A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.



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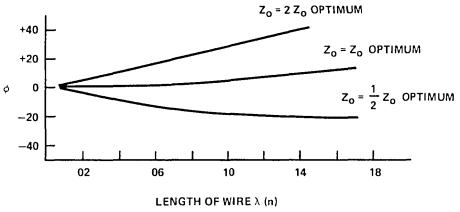


b.

Toroid Coil Winding Data
Figure 11

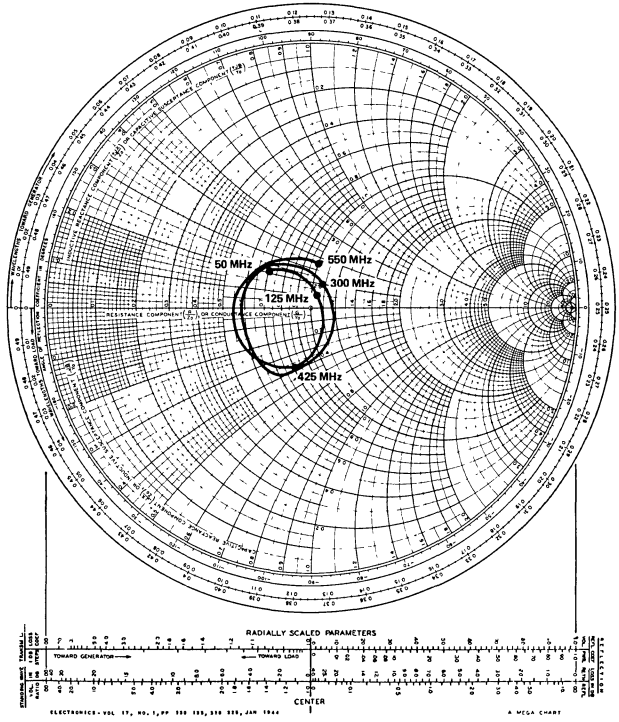
Designing the IF Network

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network.[17] This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o.[18, 19] This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be



50Ω – 200Ω Balun
Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors.(20) If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2\,V_{GS(off)}}{i_d} \qquad (18)$$

where

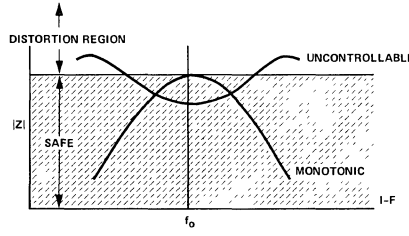
$$i_d = I_{DSS}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \qquad (19)$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \qquad (20)$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function
Figure 13

IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.[21] With two signals 300 kHz apart, the balanced mixer suppressed third-order products –89 dB with both signals at –10 dBm, representing an intercept point of +32 dBm.

Table IV

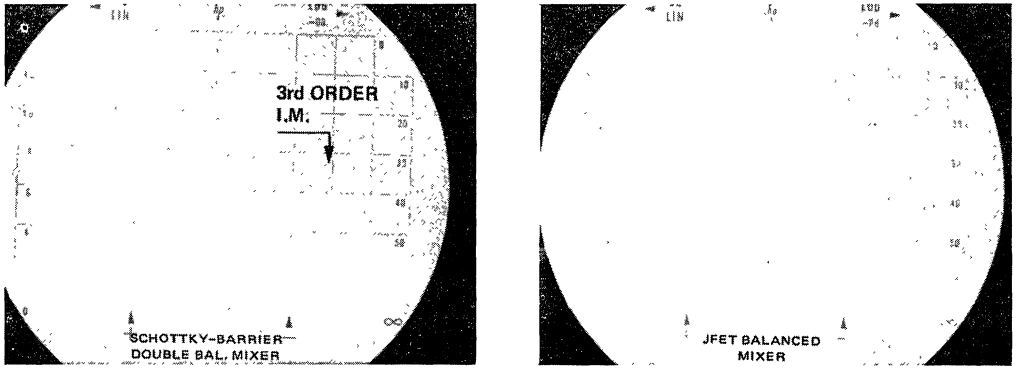
50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	–6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

†Estimated *Conservative minimum

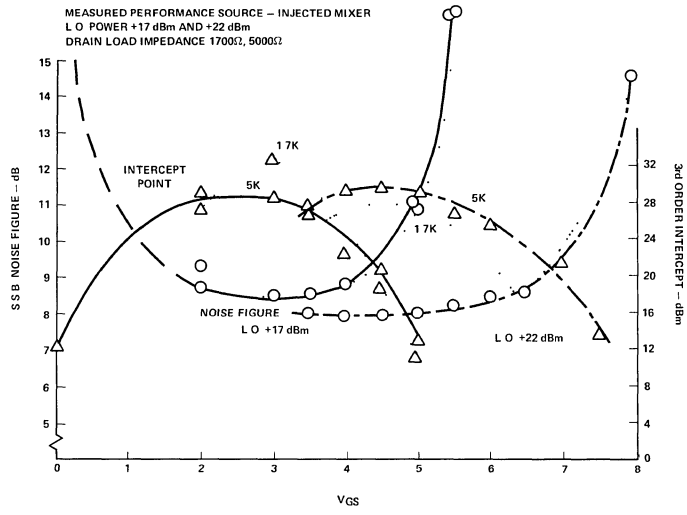
Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products

Figure 14



Noise Figure and Intercept Point Performance
Figure 15

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

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A New Current Limiter Extends Protection to 240V

Ted List

INTRODUCTION

Siliconix has developed a family of protective devices with ratings ranging from 135 volts to 240 volts. These are two terminal devices which provide active current control over a voltage range of 0.9V to 240V. Five parts are offered which provide protection for the following maximum voltages:

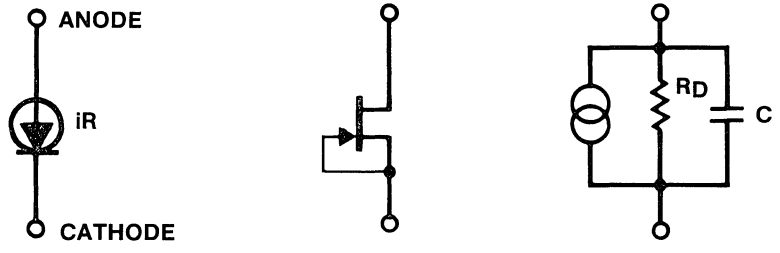
Part No.	Peak Operating Voltage
JR 135V	135 volts
JR 170V	170 volts
JR 200V	200 volts
JR 220V	220 volts
JR 240V	240 volts

The current is limited to a minimum of 160μA at 0.9 volts and a maximum of 1mA at the Peak Operating Voltage (POV). The series impedance is a resistive 5KΩ and at signal levels below 0.6 volts, no additional distortion is introduced. Power consumption is micro-watts, except in the protective mode where the dissipation is the applied voltage multiplied by the limiting current.

Because these are two-terminal devices, installation into a PC board is simple, cost effective, and no additional circuitry or power supplies are needed.

FUNCTIONAL DETAIL

The equivalent circuit (shown in Fig. 1c) is a current generator with a resistor and capacitor in parallel. This differs from the classic constant-current diode in that it contains no external source resistor. Voltage is developed across the channel-source resistance (V_P/I_{dss}).



a) Symbol b) Schematic c) Equivalent

FIGURE 1
High Voltage Protection Diode (current limiter)

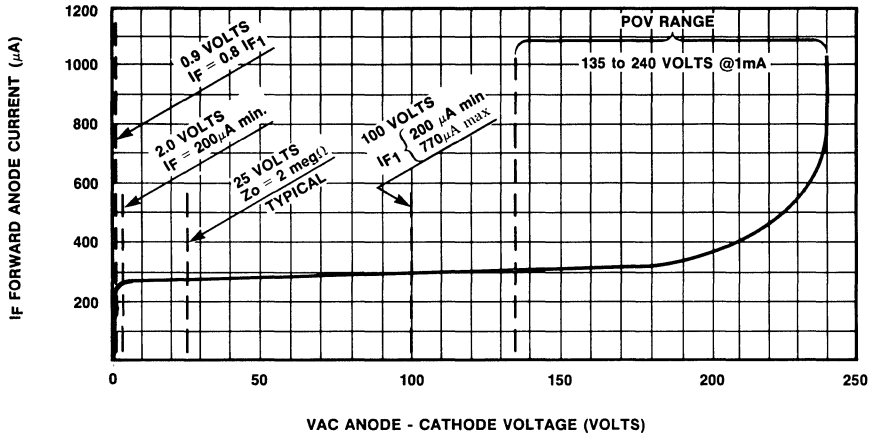


FIGURE 2
JR135 Output Characteristics

FIGURE 2 OUTPUT CHARACTERISTICS

There is a difference between a current limiter and a current regulator. The difference involves both the intended usage and the current tolerance. The current regulator is intended to be an accurate device providing a specific amount of current at a specific circuit location. Naturally, a nominal value and a tolerance are involved; typical maximum tolerances are 5%, 10%, 20% or 30%, and interchangibility and control of circuit parameters are the reasons for the tolerance.

In contrast, the current limiter is a protective device. Minimum and maximum limits of current are imposed, but the tolerance is much less important. The JR 135, for example, has no nominal value but does have a 770μA maximum value and a 200μA minimum value. This equates to a nominal 485μA ±58%.

The output characteristic is shown in Fig. 2 with the measured and typical parameters to show how device functions and how it is controlled.

The first point of note is V_L, the limiting voltage. This is 0.9 volts and is measured at 80% of I_{F1} minimum. The other information provided by this measurement is the maximum insertion resistance. Applying Ohm's law, 0.9 volts divided by 160μA (0.8 x 200Δ) gives series impedance (resistive) of 5625 ohms.

The device is measured for minimum current at 2.0 volts. The value is 200μA minimum. This value defines one point on the line representing dynamic impedance. The dynamic impedance is a measure of control of current as voltage changes. A typical value of dynamic impedance is specified at 25 volts. The value is 2 meg ohms minimum. The current will change 0.5μA per volt of voltage change.

The next point of interest is at 100 volts. At 100 volts, both minimum and maximum currents are measured. Interestingly enough, if we apply what we know about the parts, some trends then form:

1. Minimum value 200μA at 25V plus 75 volts-times-0.5μA shows a minmum 100-volt limit of 237μA.
2. Working backward from 770μA at 100V gives maximum value at 2 volts of 733μA and a band 533μA wide instead of 570μA.

The remaining point of interest is the POV. This is measured at 1mA because the maximum allowable open line current in a telephone system is 1mA, and this part was developed with the telephone market in mind. The breakdown characteristic of this device is softer than that of the J-Fet current regulator.

APPLICATIONS

The primary advantage of using this device is high POV. The JR series of devices offers applications for two types of needs:

1. Protection
2. Current Regulation

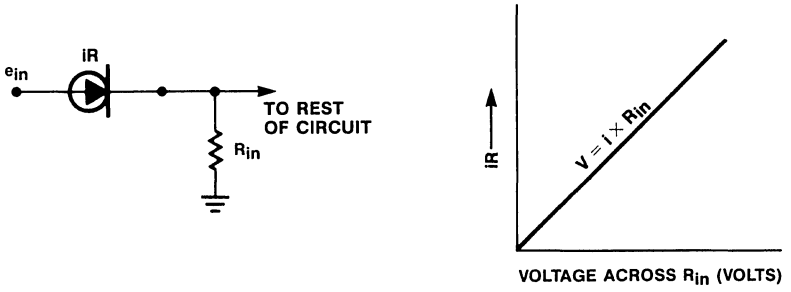


FIGURE 3a
Simple Series Protection

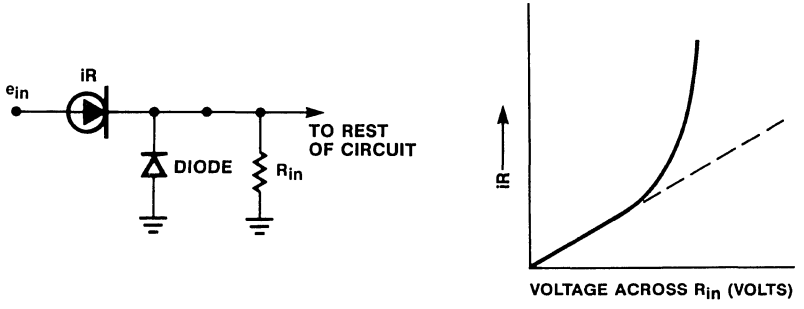


FIGURE 3b
Series Protection With Shunt Diode

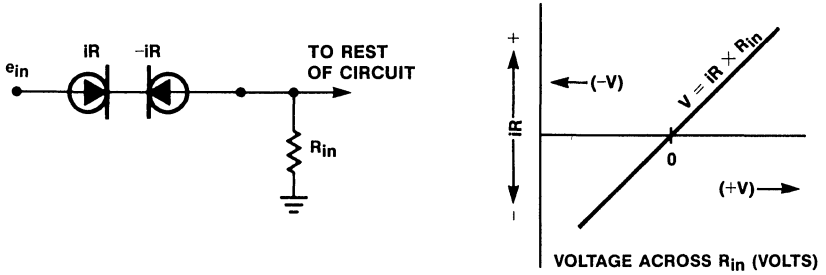


FIGURE 3c
Bipolar Series Protection

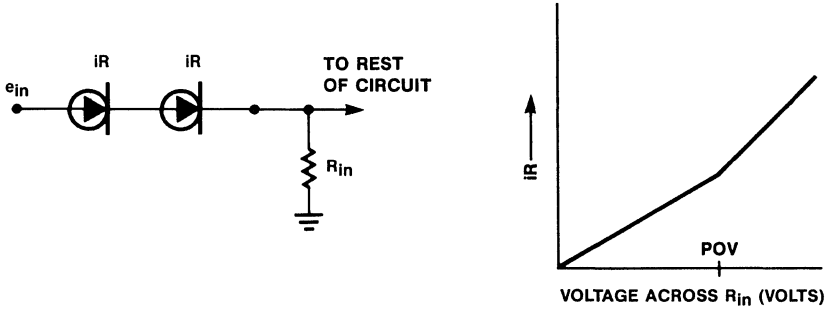


FIGURE 3d
Series Regulators Increase Voltage Protection

7

Protection

Fig. 3 illustrates four variations on the Protective Theme. A plot of the resultant voltage (V_{RL}) and I_{in} accompanies each variation. Combined variations are possible.

Fig. 3a depicts the simple series limiter. The voltage developed across R_{in} is a function of the resistance of R_{in}. If R_{in} is large, the voltage applied to R_{in} will be large. If the power dissipated in R_{in} and the remainder of the input circuit is too large, either the R_{in} must be reduced or the voltage must be limited. Zener diodes or forward-biased diodes will limit this voltage.

A diode can be used to limit the voltage across R_{in} (Fig. 3b). The diode starts to limit at 0.6 or 0.7 volts, the same as the current limiter.

Bipolar voltage protection can be provided by using back-to-back current limiters. (Fig. 3c). The same considerations apply as in Fig. 3a and 3b.

Increased protection can be accomplished by connecting the devices in series. (Fig. 3d). The ultimate circuit using 3 devices in series appears in Fig. 4

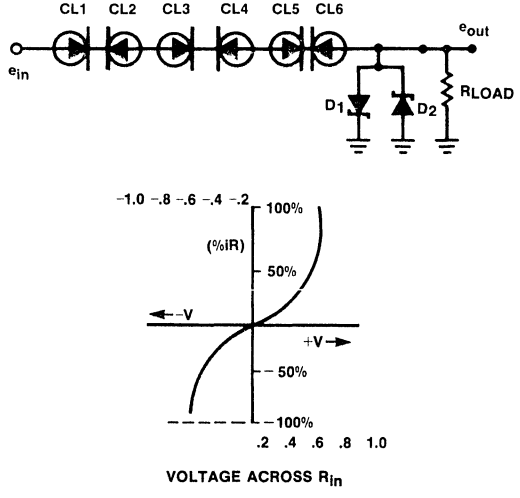


FIGURE 4
High Voltage Bipolar Clamped Protection Circuit

One last concept needs to be brought forward. A protective device must be transparent to information passed through it when it is inactive. The J-Fet current limiter is transparent to voltages of less the ±0.6 volts.

In this voltage span, the protective device functions as a resistor with a maximum value of 5625 ohms.

Current Regulation

Another use of the high-voltage current limiter is that of current regulator. This is a matter of current tolerance. The JR Series current limit is 200μA to 770μA measured at 100 volts. These parts are also measured at 2.0 volts with a single limit value of 200μA minimum. The maximum value is 360% of the minimum value. This does not make a good current regulator, but selection is possible.

By special order, parts can be selected to 100μA band. This would be a mid band percentage of ±10.3% varying from 7% at the high end to 20% at the low end. In addition, the current range can be extended to 2mA. So, between 200μA and 2mA, selections as tight as 100μA can be made.

APPLICATIONS

The following are applications of the JR Series of Devices. These applications would require the selected devices.

Differential Amplifier

The constant-current diode makes an excellent current source for a differential amplifier. Improved common-mode voltage rejection will result from the low-compliance voltage of the device.

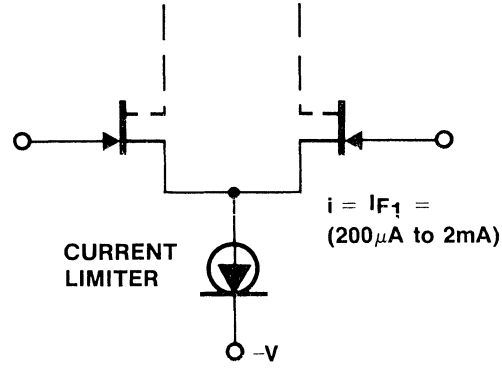


FIGURE 5
Differential Amplifier Current Source

Timing Circuits

Timing circuits often require ramp generators, and the obvious choice for a ramp generator is a current source in the series with a capacitor. Current flows through the constant current diode and charges the capacitor at a constant rate. (Fig. 6a). Additional circuitry to stop the charging and to discharge the capacitor completes this simple, accurate "heart" for timing circuits.

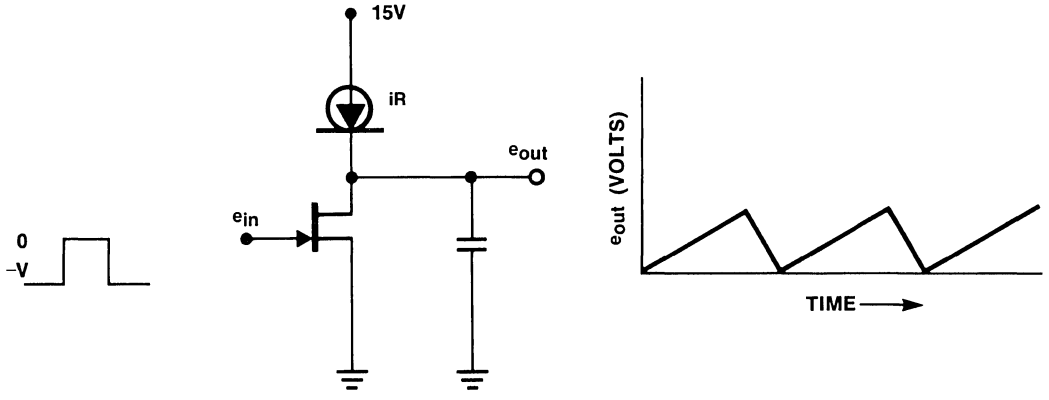


FIGURE 6a
Saw Tooth Generator

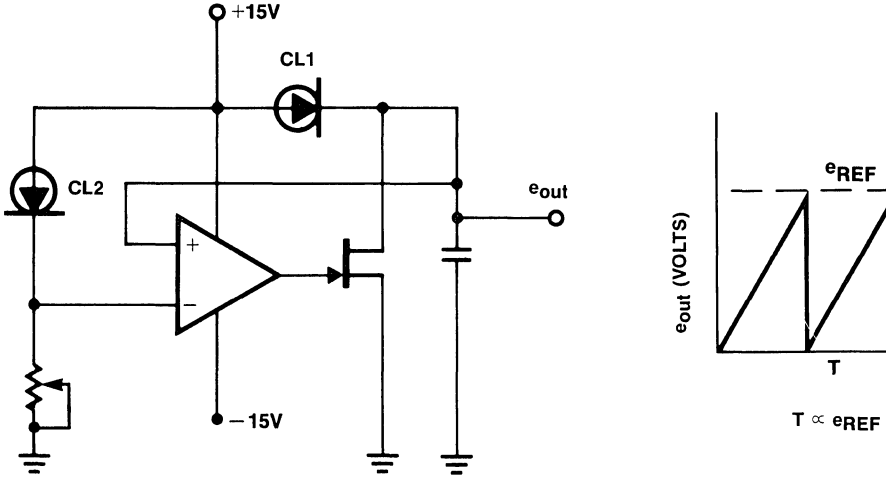


FIGURE 6b
Variable Frequently Saw Tooth Generator

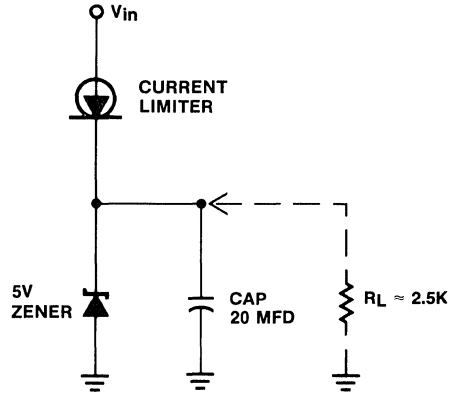


FIGURE 7A

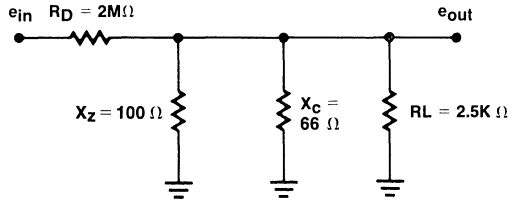


FIGURE 7B

FIGURE 7

Current Limiter as Filter Circuit Element and Equivalant Circuit

Timing circuit in Fig. 6b shows the complete circuit, including the capacitor discharge switch.

FILTERING

An interesting effect occurs if the diode in Fig. 3b is replaced by a zener. The current limiter assumes the functions of a constant current for the zener, and the combination becomes a lowpass filter. This leads into the final application. This application uses current limiter dynamic-impedance to replace frequently sensitive magnetics as ripple filters into low-power power supplies.

Ripple frequency would be 120Hz and maximum value could be as high as 30 volts. The combined impedance of X_Z and X_C would be 40 ohms. Forty ohms is series with 2 meg ohms attenuates the ripple by $4x10^{-5}$ (100db).

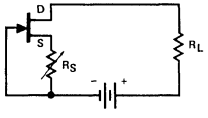
SUMMARY

The current limiter series of devices are primarily rated for high breakdown and low compliance voltage. They serve a complete range of constant current diode applications. Use of the normal strong features, high voltage, high dynamic impedance, low limiting voltage plus a willingness to select current values through practical current range, extends the usefulness of these current limiters throughout the entire range of possible constant current applications.

The FET Constant Current Source

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant current source. An adjustable current source may be built with a FET, a variable resistor and a small battery, Figure 1. For good thermal stability, the FET should be biased near the zero T.C. point.[1]



Field-Effect Transistor Current Source
Figure 1

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant current source at any current below its saturation current I_{DSS}.

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)} \left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \quad (1)$$

where k can vary from 1.7 to 2.0, depending upon device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in supply voltage, or change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = \Delta V_{DS} g_{oss} \quad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant current source. As g_{oss} may range from less than 1 μmho to more than 50 μmho according to the FET type, the dynamic impedance can be greater than 1 megohm to less than 20K. This corresponds to a current stability range of 1 μA to 50 μA per volt. The value of g_{oss} depends also on the operating point, being highest at I_{DSS} and at low V_{DS}. Output conductance g_{oss} decreases approximately linearly with I_D, becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \quad (4)$$

where

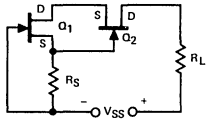
$$g_{oss} = g'_{oss} \quad (5)$$

when

$$V_{GS} = 0 \quad (6)$$

So as $V_{GS} \rightarrow V_{GS(off)}$, $g_{oss} \rightarrow$ zero. For best regulation, I_D must be considerably less than I_{DSS}.

It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs as shown in Figure 2.



Cascade FET Current Source
Figure 2

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The d-c value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition $V_{GS1} = 0$.

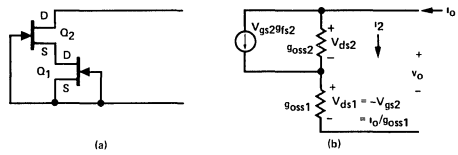


Figure 3

$$i_o = i_2 + v_{gs2}g_{fs2} = v_{ds2}g_{oss2} - i_o\frac{g_{fs2}}{g_{oss1}} \quad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \quad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \quad (9)$$

$$v_o = v_{ds2}\frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \quad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \quad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \quad (13)$$

When

$R_S \neq 0$ as in Figure 2 (14)

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2)} \quad (15)$$

$$\approx \frac{g_{oss}^2}{g_{fs}(1 + R_Sg_{fs})} \quad (16)$$

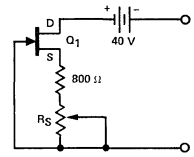
In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage V_{DG}. That is,

$V_{DG} > V_{GS(off)}$, preferably $V_{DG} > 2\,V_{GS(off)}$ (17)

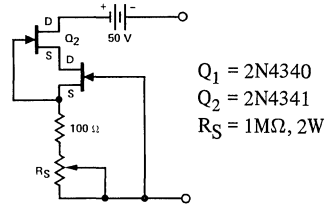
If $V_{DG} < 2\,V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A 2N4340 has typical $g_{oss} = 4$ μmho at $V_{DS} = -20$ V and $V_{GS} = 0$. At $V_{DS} \approx -V_{GS(off)} = 2$ V, $g_{oss} \approx 100$ μmho.

The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4869 exhibits typical $g_{oss} = 1$ μmho at $V_{DS} = 20$ V. A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from 5 μA to 1 mA with internal impedance greater than 2 megohms.



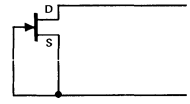
Adjustable Current Source
Figure 4

The cascade circuit of Figure 5 provides a current adjustable from 2 μA to 1 mA with internal resistance greater than 10 megohms.

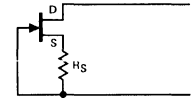


Cascade FET Current Source
Figure 5

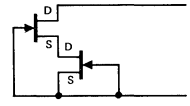
For each circuit discussed, g_{oss} is represented by the following equations:



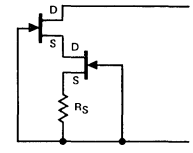
$g_o = g_{oss}$



$$g_o \approx \frac{g_{oss}}{1 + R_Sg_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}(1 + R_Sg_{fs})}$$

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(1) "Biasing FETs for Zero DC Drift," Evans, L., **Electrotechnology**, August 1964.

BUILD A PRECISION CONSTANT CURRENT SOURCE

By John Grabeklis

The junction field-effect transistor (J-FET) has been popular as a constant-current source (CCS) but was restricted in application because of its relatively low current and voltage ratings. Furthermore, the J-FET CCS generally involved a tradeoff between high current and low precision, or low current with somewhat improved precision; and temperature always played a critical role.

The MOSPOWER® FET, controlled by a low-cost op-amp resolves many of the former problems of the J-FET regulator. MOSPOWER FETs may be selected offering high standoff voltages capable of handling many amperes. Since precision control of current no longer depends solely upon the selection of the FET precision high-current regulation is possible.

An adjustable CCS using a MOSPOWER FET and an op-amp can have either a positive or negative compliance voltage. A CCS with negative compliance is shown in Figure 1. To establish a positive compliance voltage, the *n*-channel VN1206B is replaced by a *p*-channel VN1206B; ground is connected to point B instead of point A; and the current-sensing resistor is connected to point C instead of point D.

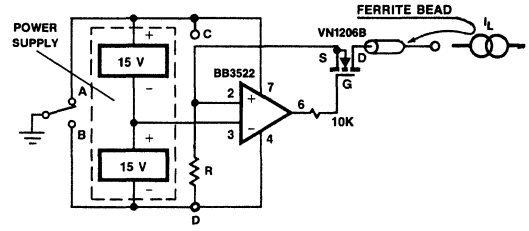
The output current range, using either the *p*-channel VN1008B or the *n*-channel VN1206B, extends from 10 μA to 100 mA. This current is provided by the dual 15 V power supply which must also accommodate the CCS reference current. The circuit shown in Figure 1 can work into loads ranging in voltage from −10 VDC to +50 V DC. Power dissipation is a limiting factor at high currents and care must be taken in mounting the MOSPOWER FET to a suitable heatsink.

Since it is impossible to design a CCS with an output current lower than the I_{DSS} of the MOSFET, care should be taken to use the lowest leakage MOSFET consistent with the desired goals. Furthermore, the overall precision of the regulator depends upon using the lowest gate leakage current, I_{GSS}, available.

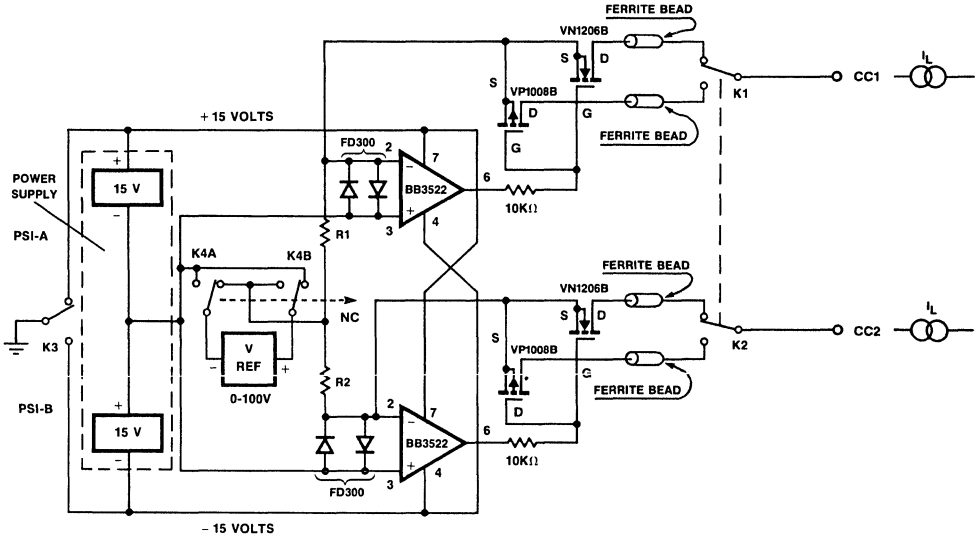
Combining the VN1206B and the VN1008B a dual bidirectional CCS regulator can be assembled, as shown in Figure 2. By ganging the switches, K1 - K4, this design can be used to supply either a positive or negative current. Current tracking between the two outputs, CC1 and CC2, depends upon the precision matching of R1 and R2. Accuracy depends upon the combined gate leakage current, I_{GSS}; the offset voltage and current of the op-amps; the tolerance and match of the resistors, R1 and R2; and the accuracy of the reference voltage, V_{REF}.

TABLE
VALUE OF R (Fig. 1 & Fig. 2)

I_{Load} (I_L)	Resistance (R)	Power Rating
10 μA	1.5 MΩ	¼W
100 μA	150 KΩ	¼W
1 mA	15 KΩ	¼W
10 mA	1.5 KΩ	½W
100 mA	150 KΩ	3W



Precision Current Source
Figure 1 (Note 1)



Dual Precision Current Source
Figure 2 (Note 1)

NOTE:
1. All switches are shown for negative compliance.

FETs As Voltage-Controlled Resistors

INTRODUCTION

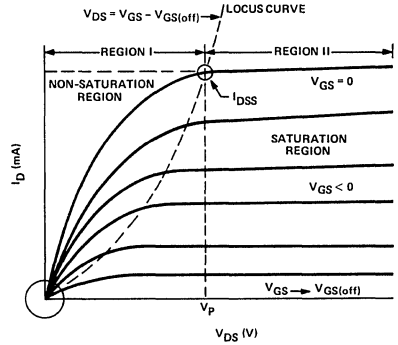
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS}, and the net drain-source voltage, V_{DS}.

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.(1) Maximum drain-source current, I_{DSS}, and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.(2) The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

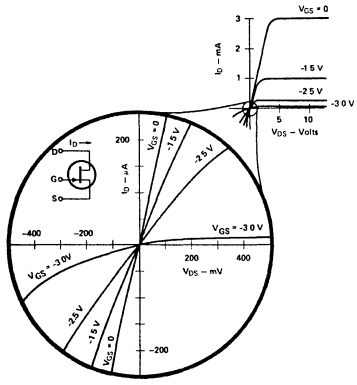


Typical N-Channel JFET Operating Characteristics
Figure 1

Resistance Properties of FETs

The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d.c. resistance, r_{DS}, and is a function of V_{GS}.(3)

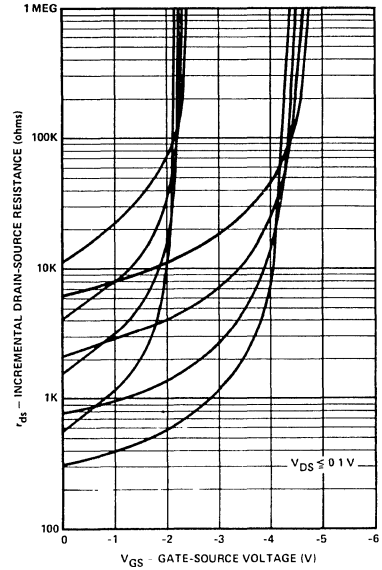
Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D/\Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 2

Figure 3 extends the r_{ds} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.

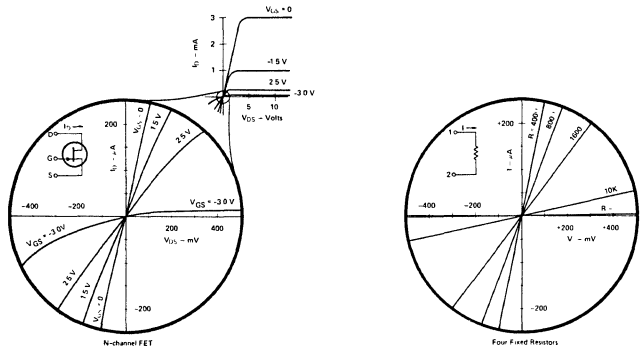
Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.(4) The graphs are useful in estimating r_{DS} values at any given value of V_{GS}. All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefor deisrable to convert Figure 4 to a normalized plot. This



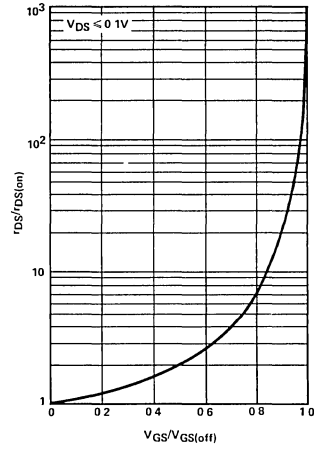
Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

has been done in Figure 5. The resistance is normalized to its specific value at $V_{GS} = 0$ V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.

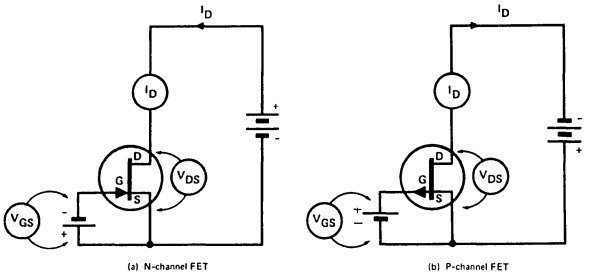
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).



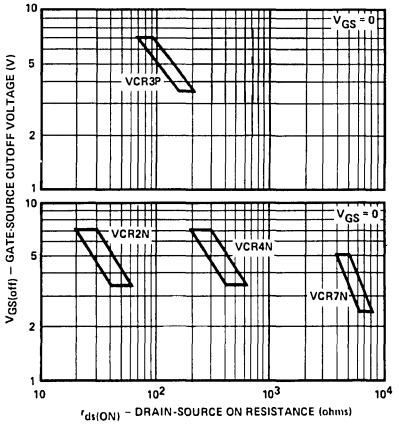
Comparison of FET and Resistor Characteristics
Figure 3



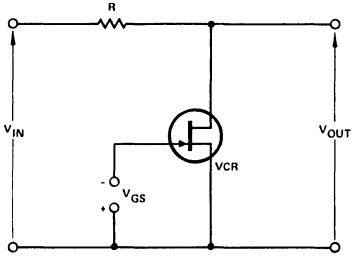
Normalized r_{ds} Data
Figure 5



Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.(5)

The output voltage is

$$v_{OUT} = \frac{V_{in}\, r_{DS}}{R + r_{DS}} \quad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is

$$v_{OUT(min)} = \frac{V_{in}\, r_{DS(on)}}{R + r_{DS(on)}} \quad (2)$$

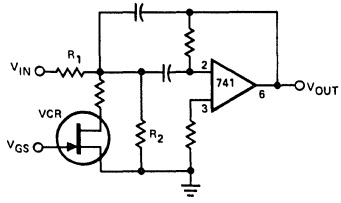
7

The highest value is

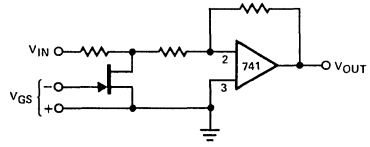
$$V_{OUT(max)} = V_{in} \qquad (3)$$

since r_{DS} can be extremeley large.

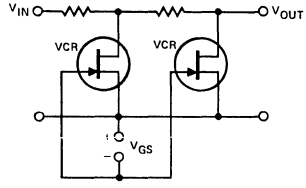
A number of other FET VCR applications are shown in Figures 9-16.



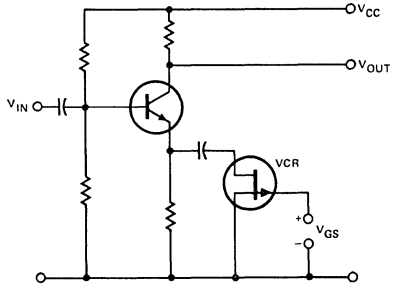
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1
Figure 9



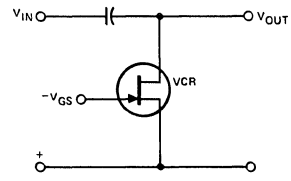
Electronic Gain Control
Figure 10



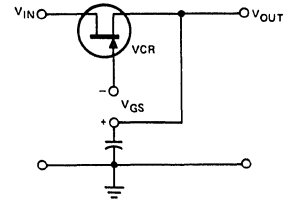
Cascaded VCR Attenuator
Figure 11



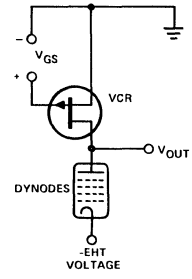
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



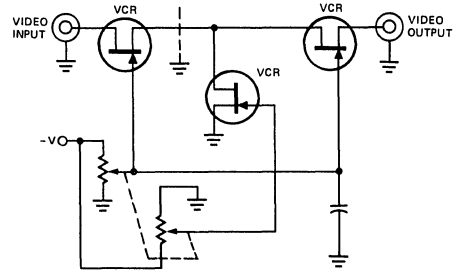
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



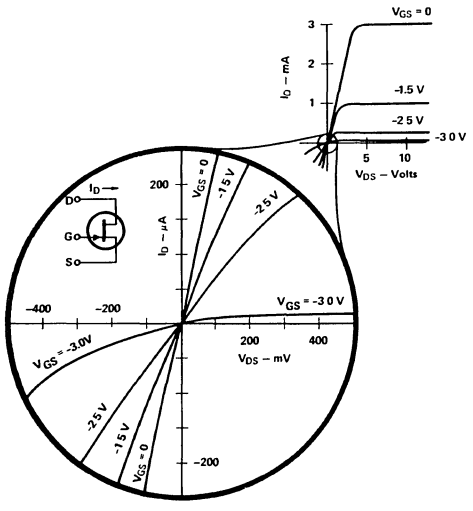
P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually $< 1\ \mu A$) Implies that VCR will Always Perform in Linear Region Near Origin
Figure 15



Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$

Figure 17A

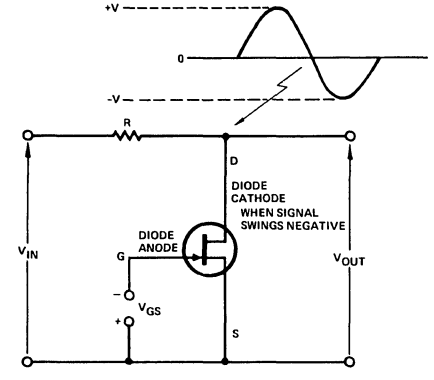


Figure 17B

in the third quadrant, rising negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

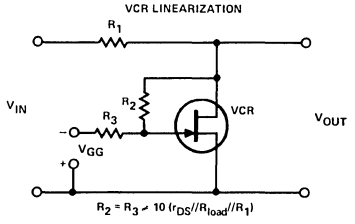


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geq 10\ [R_1 \,||r_{ds}\,(\max)\,||R_L] \qquad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)}\,||R_L$ to $[(r_{DS(on)}\,||R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \ \frac{r_{DS(on)}\,||R_L}{(r_{DS(on)}\,||R_L) + R_1} \qquad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

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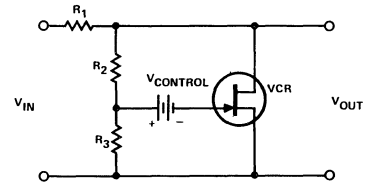


Figure 19

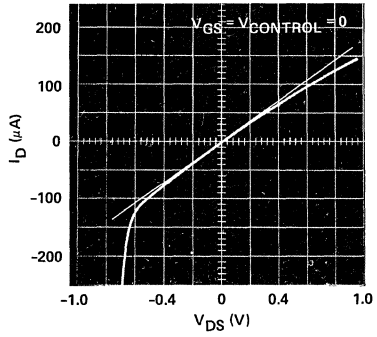
Experimental Results

Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the V_{GS} = 0 V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

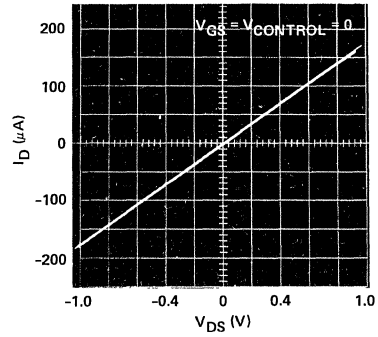
The forward-biased gate-drain PN junction may be seen at approximately –0.6 V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

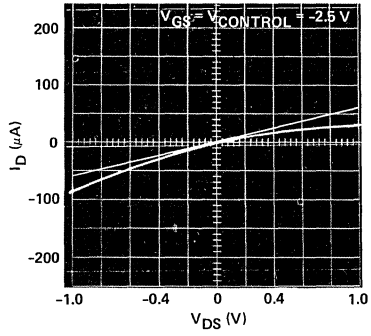
In Figures 22 and 23, the same VCR FET characteristics are shown, with V_{GS} adjusted for higher r_{DS}. No feedback network is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.



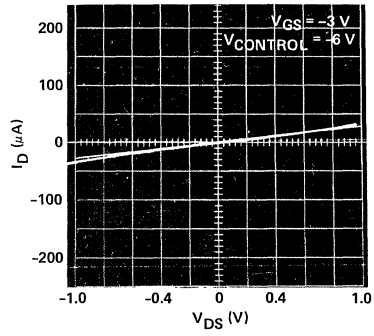
VCR7N with No Feedback
Figure 20



VCR7N with Feedback
Figure 21

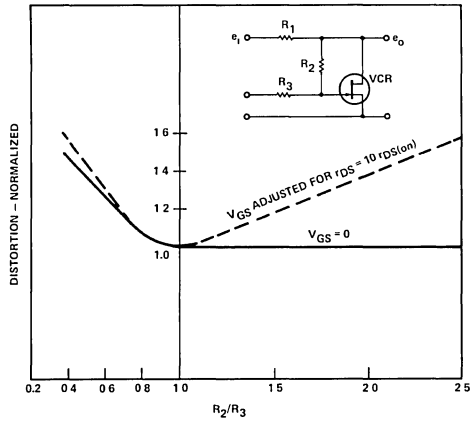


VCR7N with No Feedback
Figure 22



VCR7N with Feedback
Figure 23

Some degree of non-linearity will be experienced in both the first and third quadrants as V_{GS} approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs R_2/R_3, in both quadrants.



Distortion vs R_2/R_3
Figure 24

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique. r_{DS} will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

Table I

Temperature (°C)	Without Feedback		With Feedback	
	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\ r_{DS(on)}$	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\ r_{DS(on)}$
+125	>13%	>6%	<0.5%	<0.5%
+ 25	>10%	>5%	<0.5%	<0.5%
– 55	3.9%	3.2%	<0.5%	<0.5%

SUMMARY

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

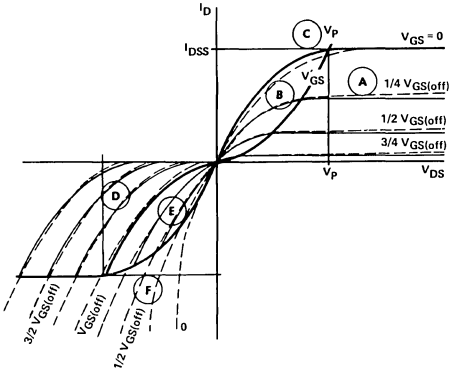
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ (compatible with the desired r_{DS} value) if large signal levels are to be encountered.

APPENDIX A — **From proceedings of the IEEE, October, 1968, pp. 1718-1719.**

Abstract — An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.[6,7] The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.



Comparison Between Mathematical Approximation of FET Characteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET
Figure 25

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off) I_D is independent of V_{DS}:[8]

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

Region B, where $V_{DS} < (V_{GS} - V_P)$, is the so-called triode region. (In the following discussion all the signs (+, –) will be valid for N-Channel FETs.) The characteristics can be

7

approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS}\left[\left(1-\frac{V_{GS}}{V_P}\right)^2-\left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2\right]$$

$$=\frac{2I_{DSS}}{(V_P)^2}\ V_{DS}\left(V_{GS}-V_P-\frac{V_{DS}}{2}\right) \quad (2)$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction (V_{GS}, V_{GD}) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If V_{GD} were the controlling voltage and $V_{DS} < 0$, $I_D < 0$, then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V^2_P}\ V_{DS}\left(V_{GD}-V_P+\frac{V_{DS}}{2}\right) \quad (3)$$

Since the controlling voltage for both regions (B and E) is V_{GS},

$$V_{GD} = V_{GS} - V_{DS} \quad (4)$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are $V_{GD} = 0$ and $V_{GD} = V_P$. The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS}\left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2 \quad (5)$$

The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

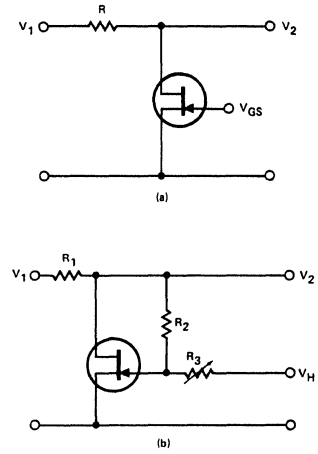
$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$

$$-\frac{I_{DSS}}{(V_P)^2}\ V_{DS} = g_{DS} + \frac{g_{DSS}V_{DS}}{2V_P} \quad (6)$$

where g_{DS} is the differential conductance at the origin; when $V_{GS} = 0$, then $g_{DS} = g_{DSS}$. The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1+Rg_{DS}}$$

$$=\left[1+Rg_{DS}+\frac{Rg_{DSS}\,V_1}{2V_P\left(1+Rg_{DS}+\frac{2Rg_{DS}\,V_1}{2V_P\,(1+Rg_{DS})}\right)}\right]^{-1} \quad (7)$$



(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical
Figure 26

To reduce (7) to a more tractable form, the following inequality is introduced:

$$\frac{V_1\,Rg_{DSS}}{2V_P\,[1+Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the expansion

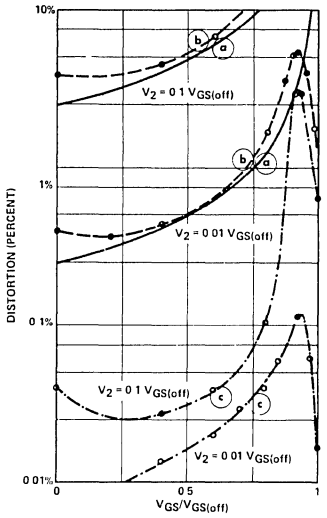
$$V_2 = \frac{V_1}{1+g_{DS}R}\left(1-\frac{Rg_{DS}\,V_1}{2V_P\,[1+Rg_{DS}]^2}+\ldots\right) \quad (8)$$

Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ($d \ll 1$ and $Rg_{DSS} \gg 1$),

$$d = \frac{V_1\,Rg_{DSS}}{4\,|V_P|\,[1+Rg_{DS}]^2} \quad (9)$$

If V_2 is held constant,

$$d = \frac{V_2\,Rg_{DS}}{4\,|V_P|\,[1+Rg_{DS}]} \approx \frac{V_2}{4\,|V_P - V_{GS}|} \quad (10)$$



Distortion as a Function of $V_{GS}/V_{GS(off)}$ for Two Different $V_2/V_{GS(off)}$. (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b)

Figure 27

Figure 27 shows a comparison of measured and calculated distortion. If V_{GS} approaches V_P, the above restrictions are violated; the expression for the distortion can no longer be applied. If $V_{DS} < 0$, $V_{GS} = 0$, then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of V_{GS}:

$$V_{2max} = 4d_{max} |V_P - V_{GS}| \tag{11}$$

For a given d_{max} and V_{2max} the ratio of minimum to maximum attenuation is

$$\frac{A_{min}}{A_{max}} = m = \frac{1 + Rg_{DSS}}{1 + Rg_{DSS} \dfrac{V_{2max}}{4d_{max}|V_P|}} \approx \frac{4d_{max}|V_P|}{V_{2max}} \tag{12}$$

valid only for $m > 1$. Note that the maximum distortion is reached only for minimum attenuation. Examples:

d_{max} = 10 percent $V_{2max} = 0.001\ V_P$ $m = 400$

d_{max} = 1 percent $V_{2max} = 0.01\ V_P$ $m = 4$

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to V_P. FETs with high V_P are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low V_P for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseries, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if V_{GD} were the control voltage in the third quadrant. By adding $0.5\ V_{DS}$ to the control voltage, the two voltage V_{GS} and V_{GD} interchange when V_{DS} changes sign:

$$\begin{aligned} V_{GS} &= V_H + 0.5\ V_{DS} \\ V_{GD} &= V_H - 0.5\ V_{DS} \end{aligned} \tag{13}$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V_P^2}\ V_{DS}\,(V_H - V_P) \tag{14}$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for $V_2 = 0.1\ V_P$ at $V_{GS} = 0.8\ V_P$ is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal V_H to keep the direct interference of V_H on V_2 small. R_3 is set for minimum distortion. If V_2 and V_H are in the same frequency range, a high impedance amplifier must be used. V_2 is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with V_2 occurs.

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(4) "FETs As Voltage-Controlled Resistors," Siliconix, inc., Santa Clara, Calif., 1966.

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FETs as Analog Switches

INTRODUCTION

The past has seen a pronounced growth of analog/digital systems which employ integrated circuits. One of the interface elements in such a system is the digitally-controlled analog switch. As more and more applications arise for the analog switch, especially in the areas of industrial processing and control, the question is often asked: "Which is the best switch for my application?"

The sheer variety of applications precludes any pat answer to this question; however, the user of analog switches can gain valuable insight on the subject through an understanding of the nature of solid-state switches. Areas which require exploration include:

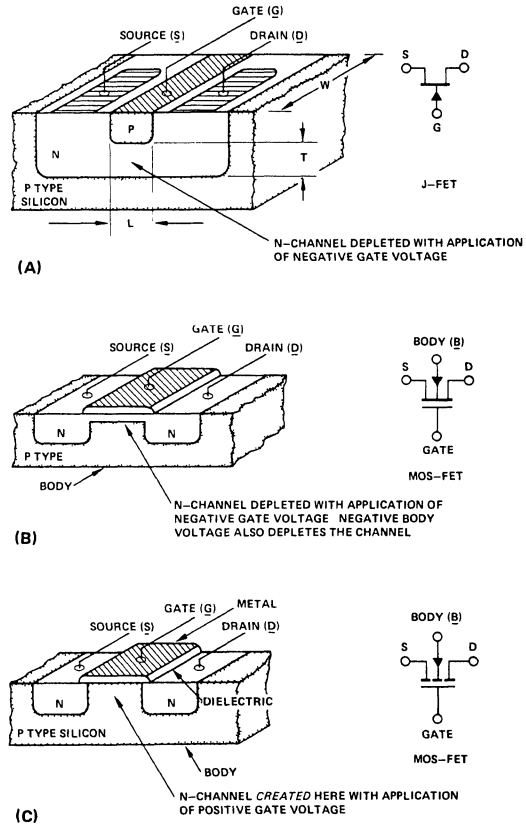
(1) Basic factors affecting switch performance.
(2) Details of switch-driver circuit design.
(3) Total switching characteristics of driver circuits and switches.
(4) Characterization of the analog switch at high frequencies.

The intent of this Application Note is to consider (1) above, in detail, with minor attention to the other areas.

Field-Effect Transistor Operation

The field-effect transistor (FET) is in effect a conductor whose cross-sectional area may be varied by the application of appropriate voltages. When the conducting area (the channel) is maximum, conductance is also maximum (minimum resistance). When the conducting area is minimum, conductance is minimum (maximum resistance). This phenomenon makes possible the use of FETs as analog switches. When conductance is maximum, the switch is in the ON state; when conductance is minimum, the switch is in the OFF state. In the ON state, an N-type channel contains N-type carriers; similarly, P-channel FETs contain P-type carriers.

Cross-sections for three types of N-channel FETs are shown in Figure 1.



N-Channel FET Cross-Sections
Figure 1

P-channel FET cross-sections are quite similar, except that the channel contains P-type carriers and the voltage polarities are reversed. Depletion-mode devices are shown in Figures 1A and 1B; these FET types have high channel conductance (are ON) with zero gate-channel voltage, and are characterized as "normally-ON" switches. An enhancement-mode FET is shown in Figure 1C. This device requires that voltage be applied to the control gate to create a conducting channel – the ON state. Enhancement-mode FETs are said to be normally-OFF.

For enhancement-mode devices, channel conductance (g_{DS}) is a function of length (L), width (W), thickness (T), carrier mobility (μ), and mobile carrier concentration (Nc):

$$g_{DS} = K_1 \frac{WT}{L} \mu Nc$$

Effective channel thickness and carrier concentration are functions of the electric field in the channel. Voltage on the control gate changes the field, and hence the channel conductance, g_{DS}.

The gate voltage is applied with respect to the channel (source or drain). In most devices, the function of the source and drain can be interchanged, because of symmetrical FET geometry. By convention, however, voltage is specified between gate and source, V_{GS}. Figure 2 shows the variation of g_{DS} with V_{GS} for both N- and P-channel devices. In all cases, $g_{DS} = 1/r_{DS}$.

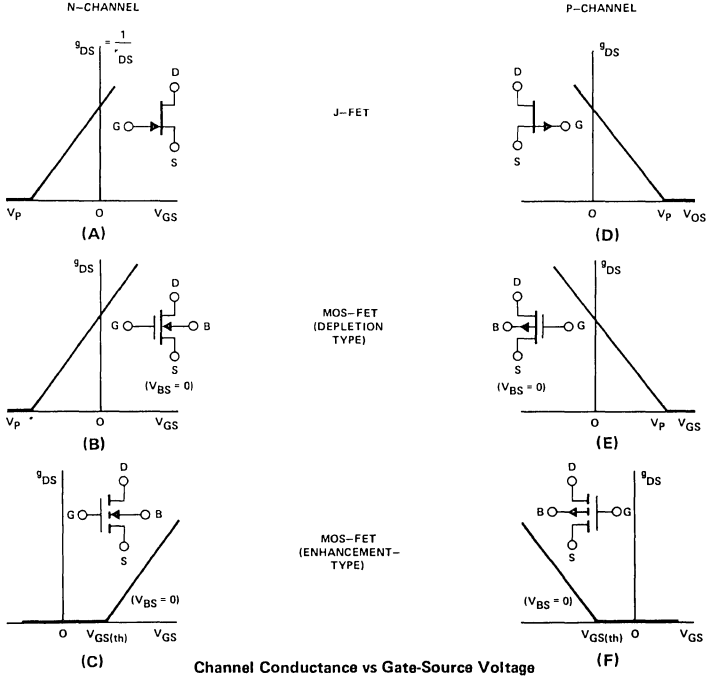
Note that the slopes ($\Delta g_{DS}/\Delta V_{GS}$) for all three types of N-channel FETs are constant and positive, while the slopes for the P-channel devices are constant and negative. N- and P-channel depletion-mode FETs are ON when $V_{GS} = 0$, while enhancement-mode devices of both types are OFF when $V_{GS} = 0$. Typically, the cut-off voltage, $V_{GS(off)}$, is designed to fall in the 1-to-10 volt range, while the gate-to-source threshold voltage, $V_{GS(th)}$ – that amount of voltage applied to the point where the device begins to conduct – falls in the 1-to-5 volt range. Figure 2 also demonstrates that g_{DS} is approximately a linear function of V_{GS}, with zero g_{DS} occuring at $V_{GS(off)}$ or $V_{GS(th)}$, as follows:

$$g_{DS} = K_2 |V_{GS} - V_{GS(off)}| \qquad \text{(depletion)}$$

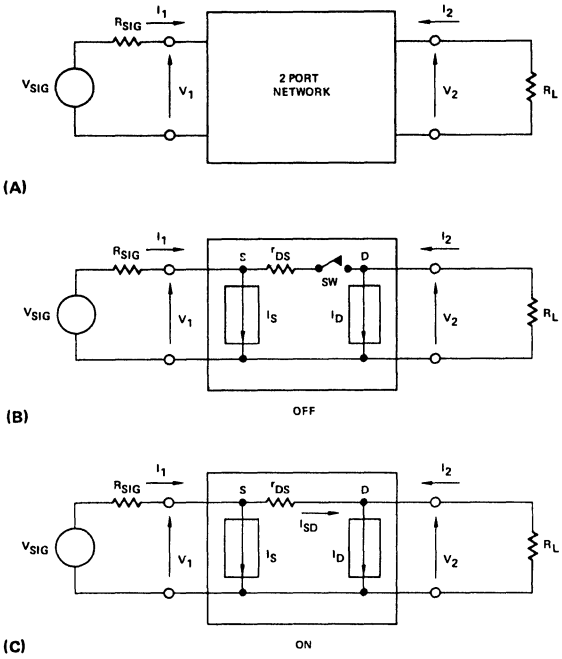
$$g_{DS} = K_2 |V_{GS} - V_{GS(th)}| \qquad \text{(enhancement)}$$

For a given active area, a junction FET (JFET) will have a higher conductance slope than a MOS FET. Additionally, N-channel carriers have higher mobility than P-type carriers. Thus, all things being equal, N-type FETs have higher g_{DS} ($= 1/r_{DS}$) than P-type devices. If the active area of the device is increased to raise the g_{DS} level, three other FET parameters will also be increased: leakage, capacitance, and cost. The design tradeoffs of these latter parameters are discussed in this Application Note.

When a FET is used as an analog switch, the drain-to-source voltage, V_{DS}, may be either positive or negative. In the OFF state, a typical switch may have $V_{DS} = \pm 20$ V. In the ON state, current flows equally well from drain to source or from source to drain (the channel is a resistor). For most applications, the voltage across the switch will be small.



Channel Conductance vs Gate-Source Voltage
Figure 2



D-C Equivalent Circuits
Figure 3

DC Equivalent Circuits

The perfect switch would have infinite resistance (zero conductance) when open and zero resistance (infinite conductance) when closed. While the FET is not a perfect switch, there are many applications where this deviation from perfection is unimportant. This statement can be justified by an analysis of the implications of the circuits shown in Figure 3.

The general two-port network in Figure 3A couples the signal source, V_{SIG}, to a resistive load, R_L. The network can be characterized by its terminal voltages and currents, V_1, V_2, I_1, and I_2. Figure 3B shows the equivalent circuit of a FET switch in the OFF state. In this condition, the "source" and "drain" are not connected to one another; however, two leakage current sources, I_S and I_D, are present. The same device is shown in the ON state in Figure 3C. The following typical values are assumed for the circuit:

V_{SIG} = 10 V (full scale)

$I_S = I_D$ = 1 nA

r_{DS} = 100 Ω

R_L = 200K Ω

R_{SIG} = 10 Ω

In the following calculations, leakage current (deviation from the state of a perfect switch) is expressed in terms of error percentage.

OFF Condition Calculation

(1) $I_1 = I_S$ = 1 nA

$V_{SIG} - V_1 = I_1 \cdot R_{SIG}$ = (1 nA) (10 Ω) = 10 nV

$$\% \text{ Error in } V_1 = \frac{(10^{-8}\text{ V})(10^2)}{10\text{ V}} = 1 \times 10^{-7}\%$$

(2) $I_2 = I_D$ = 1 nA

$V_2(\text{off}) = I_2 R_L$ = (1 nA) (200K Ω) = −200 μV

$$\% \text{ Error in } V_2(\text{off})^* = \frac{(2 \times 10^{-4})(10^2)}{10} = 0.002\%$$

ON Condition Calculation

$I_1 = I_S + I_D - I_2$

$$I_2 = \frac{V_2}{R_L} \cong \frac{V_{SIG}}{R_L + R_{SIG} + r_{DS}}$$

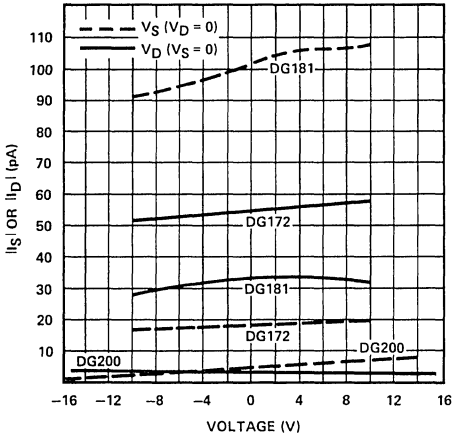
$V_{SIG} - V_2 \cong$ (50 μA) (110 Ω) = 5.5 mV

$$\% \text{ Error in } V_2^* = \frac{(5.5 \times 10^{-3})(10^2)}{10} = 5.5 \times 10^{-2} = 0.055\%$$

*Referred to V_{SIG} (full scale)

The foregoing calculations indicate that for all but the most critical applications the performance of the FET equivalent circuits in Figure 3 is a good approximation of the perfect switch. In particular, the OFF condition leakage currents contribute only a negligible portion of total error.

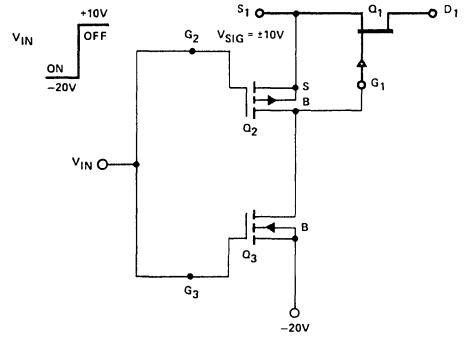
The actual error currents of three different types of FET switches are shown in Figure 4. The measured error is much lower than the 1 nA (1000 pA) obtained from the sample calculations. These data are taken from a MOS FET, an N-channel JFET, and a complementary MOS (CMOS) combination including a P-channel device and an N-channel device diffused onto the same substrate. The behavior of these FETs as elements of analog switching integrated circuits will be dealt with in detail elsewhere in this Application Note.



FET Switch Error Currents
Figure 4

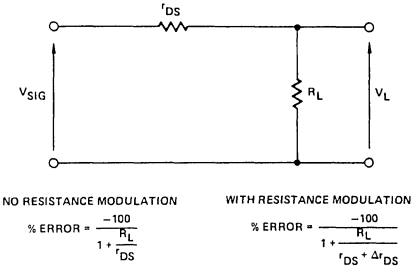
The JFET as a Switch

A suitable driving circuit must be considered when assessing the performance of the JFET as a switch. Such a circuit is shown in Figure 5.



JFET Switch Control Circuit
Figure 5

Note that Q_1 is an N-channel JFET, Q_2 is an enhancement-mode P-channel MOS FET, and Q_3 is an enhancement-mode N-channel MOS FET. From Figure 2, V_{IN} of −20 V will turn Q_2 ON and Q_3 OFF, so that S_1 and G_1 are connected (V_{GS} = 0 V) and Q_1 is ON. If V_{GS} is allowed to vary, g_{DS} (= $1/r_{DS}$) will also vary. This variation in resistance appears as a source of error when the switch is ON, and the error is defined as resistance modulation. In Figure 6, the error percentage in the case of resistance modulation is greater than that which occurs when Δr_{DS} = 0.

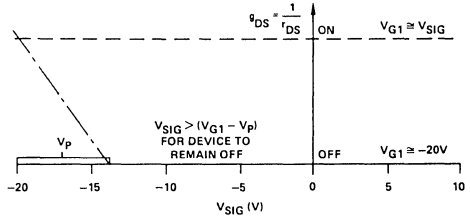


Error Due to Switch ON Resistance (r_{DS})
Figure 6

The suggested driving circuit of Figure 5 eliminates Δr_{DS} at low frequencies. The typical positive supply voltage is +10 V and the typical negative supply voltage is −20 V. In order for V_{GS} to change, current must flow through Q_2, which is ON. There are only two possible current paths through Q_2; (1), through Q_3, which is OFF and subject only to variations in leakage current, or (2), into the gate of Q_1, which is also subject to leakage current. Since both paths through Q_2 provide only negligible changes in V_{GS}, their effect in the circuit may be ignored. As the switching frequency is increased, capacitive reactance will provide lower impedance paths, so that some degree of Δr_{DS} is possible. Thus two conditions contribute to Δr_{DS} = 0 in the circuit. First, $V_{SIG} \cong V_{G1}$, due to the low impedance between these points. Second, the output impedance of Q_3 (driver output) is very large when compared to the R_{ON} of Q_2.

When V_{IN} is +10 volts, Q_2 is OFF and Q_3 is ON; G_1 is at −20 volts and Q_1 is OFF. In Figure 7, note that Q_1 will remain OFF only so long as $V_{SIG} > (V_{G1} - V_{GS(off)})$. $V_{GS(off)}$ is a *negative* voltage for an N-channel FET; thus the negative analog signal is limited by the $V_{GS(off)}$ of Q_1 and the negative supply ($V_{G1} \cong$ −20 V).

The ON condition is also shown in Figure 7. g_{DS} is constant because with $V_{G1} \cong V_{SIG}$ imposed by the switch control circuit, $V_{GS} \cong 0$.

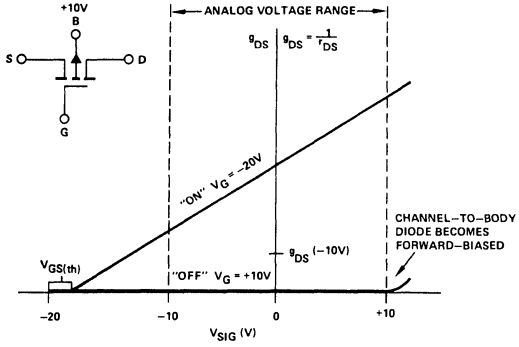


Switch ON Condition
Figure 7

The MOS FET as a Switch

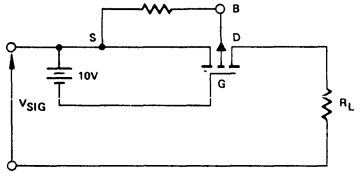
The P-channel enhancement-mode MOS FET is currently used in more applications than its N-channel counterpart. The consideration of MOS FET switch performance will thus center on P-channel devices.

The ON and OFF conditions of the MOS FET are analyzed in Figure 8. When the device is in the ON stage, note that the FET begins to turn ON when V_{SIG} (V_S or V_D) becomes $V_{GS(th)}$ volts more positive than V_G (= −20 V).



PMOS Channel Conductance (r_{DS}) vs Signal Voltage
Figure 8

Figure 8 also indicates that at any given point along the g_{DS} vs V_{SIG} curve, a unique value of g_{DS} will be obtained. Assume that a battery is inserted between the source and the gate, with the source clamped to the body as shown in Figure 9.



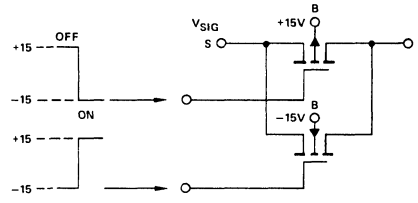
"Floating" Battery and Clamped Source
Figure 9

A constant voltage between source and gate will produce a constant value of g_{DS} vs V_{SIG}, provided that the body-to-source voltage is also constant. In a MOS FET, variation of the body-to-source voltage will also cause a modulation of g_{DS}. To further complicate the picture, several MOS FETs will have a common body when they are integrated on a single chip. Finally, the construction of a "floating battery" circuit is difficult. Thus MOS FET switch designers currently cope with the problem of Δr_{DS} by specifying r_{DS} for a given switch at several points over the entire analog voltage range.

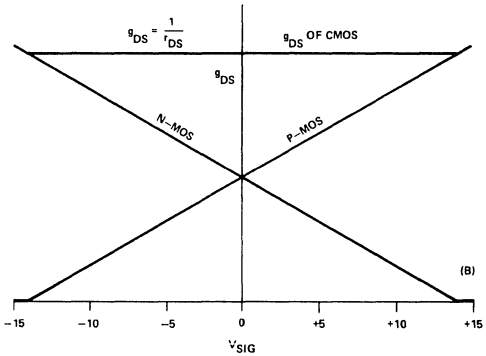
Referring to the switch in the OFF condition (V_G = +10 V), it is apparent that no problem will exist until the source-to-body or drain-body diode becomes forward-biased.

The CMOS Switch

As noted previously, the typical PMOS switch circuit will exhibit a variation in ON conductance as the analog voltage is varied. This undesirable characteristic can be overcome by paralleling P- and N-channel FETs, as shown in Figure 10A. For the ON state, the N-channel gate is forced positive and the P-channel gate is forced negative. Figure 10B shows the combined conductance of the two FET switches. The integrated combination of N-channel and P-channel devices on a common substrate is referred to as complementary MOS (CMOS).

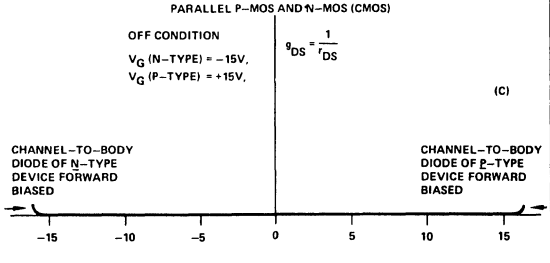


(A)



	P−MOS	N−MOS	
V_G	−15V	+15V	ON
V_G	+15V	−15V	OFF

(B)



(C)

Characteristics of CMOS Devices
Figure 10

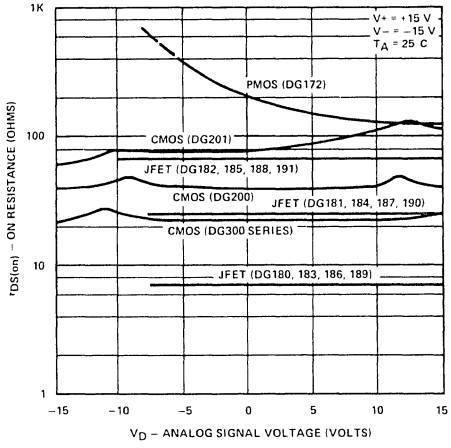
The OFF condition for the CMOS device will be maintained so long as the channel-to-body diodes do not become forward-biased, as shown in Figure 10C.

The major advantages the CMOS construction technique makes to analog switching are:

- Lower r_{DS} variation with analog signal characteristics, similar to the performance of a junction FET.
- Analog signal range extends to + and – supply voltages. For instance, using the same ±15 V supplies typical of operational amplifiers, the signal-handling capability of the system is limited by the op amp, *not by the switch.*

Summary of FET Switch Performance and Tradeoffs

Figure 11 compares the performance of three switch types with respect to $r_{DS(on)}$ vs V_{SIG}. If one examines the r_{DS} characteristics of the integrated switching circuits DG172 and DG181, there may be a tendency to dismiss the DG172 on the basis of its apparent inferior performance

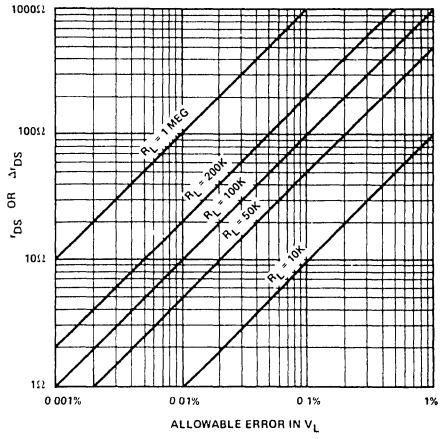


Performance of Three FET Switches
Figure 11

In reality, the comparison between the monolithic DG172 and the hybrid DG181 is not clear-cut. Initial circuit design considerations must determine what degree of error can be tolerated by the application in terms of Δr_{DS} and r_{DS}. Once this error factor has been determined, the designer should contact a switch manufacturer for applications assistance in selecting the best switch for his purpose, in terms of both r_{DS} *and* cost From this viewpoint, the single-chip DG172 will perform creditably in applications where Δr_{DS} and r_{DS} error are not critical, and the device costs considerably less than the DG181.

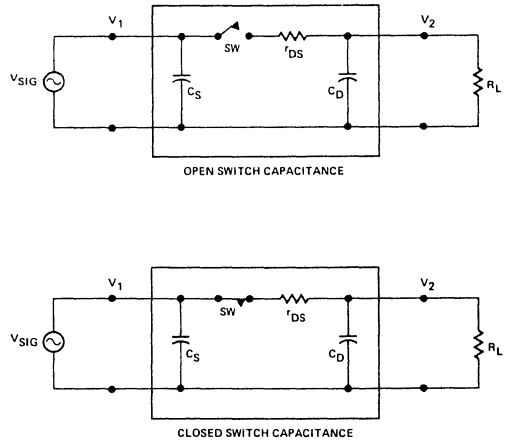
To amplify the preceding point, consider the definition of the tolerable level of Δr_{DS} and r_{DS}.

The curves in Figure 12 define the maximum r_{DS} (or Δr_{DS}) which can exist for a given allowable error percentage with a fixed value of R_L. Recall that in the circuit in Figure 3, a resistive load of 200K Ω was assumed. If it is also assumed that an error level of 0.1% is tolerable, then r_{DS} = 200 Ω is the maximum allowable switch resistance. On the other hand, if settling time is not critical, then an R_L of 1 megohm, yielding r_{DS} = 1K Ω is permissible.



Tolerable Level of Δr_{DS} and r_{DS}
Figure 12

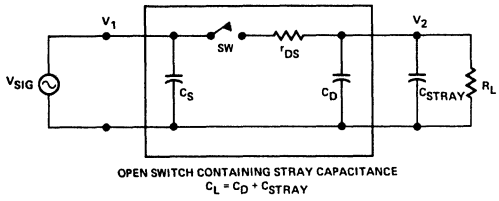
In situations where settling time is indeed a design consideration, the circuits in Figure 13 will provide an overview of the exact nature of settling time for V_2 (=V_L) at turn-OFF and turn-ON. For a turn-ON signal, C_L charges through r_{DS}. During turn-OFF, C_L discharges through R_L. For a system error level of 0.1%, R_L = 1000 r_{DS}; therefore, the maximum settling time for V_2 occurs during turn-OFF.



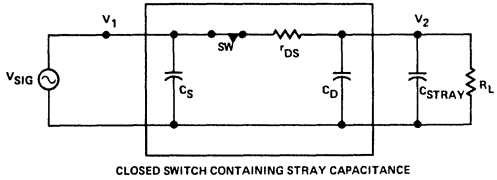
Switch Settling Time Equivalent Circuits
Figure 13

(Cont'd)

7



OPEN SWITCH CONTAINING STRAY CAPACITANCE
$C_L = C_D + C_{STRAY}$



CLOSED SWITCH CONTAINING STRAY CAPACITANCE

Switch Settling Time Equivalent Circuits
Figure 13

Consider a switch with $C_S = C_D = 3$ pF, for an application requiring 0.1% accuracy with 5 μsec settling time. A typical stray capacitance (C_{IN} for an op amp) may be 6 to 7 pF. Therefore, $C_L = 3$ pF + 7 pF = 10 pF. Resistance loads, R_L, of 100K Ω, 50K Ω, and 25K Ω are considered for the switch. The time required for an RC system to settle to within 0.1% of its final value is 6.9 time constants (6.9 RC). Table I shows the R_L and r_{DS} values necessary to satisfy a number of settling time specifications. From Table I, it is apparent that so long as $R_L \leqslant 72K\ \Omega$, the desired settling time of 5 μsec will be achieved.

TABLE I

R_L (Ω)	r_{DS} (Ω)	C_L (pF)	$t_{ON}(V_2)$** (0.1% settling time) (nsec)	$t_{OFF}(V_2)$** (0.1% settling time) (μsec)
25K	25	10	1.72	1.72
50K	50	10	3.45	3.45
*72K	72	10	5.00	5.00
100K	100	10	6.90	6.90

*Maximum R_L for t_{set} = 5 μsec

**Does not include delay times

If cost is a design constraint, it is wise to make a close analysis of actual system switch requirements. Too often, designers buy unnecessary performance capability. In Table I, the switch with $r_{DS} = 25\ \Omega$ costs nearly twice as much as does the switch with $r_{DS} = 50\ \Omega$, yet either switch will meet the 5 μsec settling time specification.

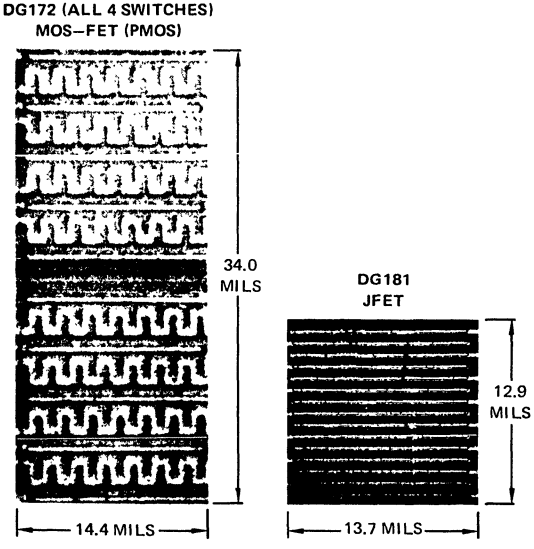
Switch Capacitance

In general, the lower the switch capacitance the better the switching time and high-frequency isolation performance. The subjects of switching time and high-frequency isolation are covered in other Application Notes in this series.

The simplified representation of switch capacitance shown in Figure 13 can be used to provide a very good estimate of what problems (if any) will be caused by switch capacitance in a given application.

In general, capacitance is proportional to the active area in a FET chip, prior to bonding onto a header. Additional stray capacitances are introduced when the leads are brought out through the device package. Thus, as lower r_{DS} (higher g_{DS}) is required, the active area is generally increased to obtain that parameter. The increase in area leads to an increase in capacitance.

The foregoing statements are true so long as one is dealing with a given device type. However, in transition from a JFET to a PMOS device, a significant difference will be observed in the active areas required for a given r_{DS}. Figure 14 compares the area of a JFET (from the hybrid DG181 circuit) and the monolithic PMOS circuit of all 4 switches of a DG172. Note that the r_{DS} for the JFET is approximately one-third that of the total PMOS device, while the active PMOS area is almost three times greater than that of the JFET. Yet the ratio of PMOS-to-JFET capacitance is almost 2:1. For the single DG172 switch the comparison to the JFET is a larger $r_{DS(on)}$ for the smaller area.



Active Area Comparison of PMOS and JFET Switches
Figure 14

Switch Comparison

A comparison between the characteristics of the three types of JFET switches is made in Table II.

This Application Note has surveyed the characteristics of FET switches and their associated drivers. In considering the FET as an analog switch, discussion has largely centered on the devices themselves, including specific load problems and applicable driver circuits. Total switch performance is a function of the switch *and* the switch driver. Typically, high-performance switch drivers require numerous switching transistors. When discrete devices are considered, the total parts count will be high and the cost will be prohibitive. From the standpoint of cost, improved performance, and smaller size, the integrated circuit FET switch and driver is often the superior choice.

TABLE II

Switch Type	Analog Signal Range	r_{DS}	Δr_{DS}	Leakage, I_D or I_S
PMOS	$(V_- - V_{GS(th)}) < V_{SIG}$*	High	High	Low
JFET	$(V_- - V_{GS(off)}) < V_{SIG}$*	Low	Low	Low
CMOS	$V_- \leqslant V_{SIG} \leqslant V_+$	Medium	Medium	Low

*Both $V_{GS(th)}$ (for PMOS) and $V_{GS(off)}$ (for N-channel JFET) are *negative* voltages.
V_+ is defined as positive supply voltage.
V_- is defined as negative supply voltage.

DMOS FET Analog Switches and Switch Arrays

Jack Armijos

INTRODUCTION

This Application Note describes in detail the principle of operation of the SD5000/210 series of high-speed analog switches, switch arrays, and drivers. It also contains an explanation of the most important switch characteristics. Application examples, test data, and other application hints are included.

DESCRIPTION

The Siliconix SD210 and SD5000 series are single and quad monolithic arrays, respectively, of single-pole single-throw analog switches. The switches are n-channel enhancement-mode silicon field-effect transistors that are built using double-diffusion silicon-gate technology.

This family of devices is designed to handle a wide variety of video, fast ATE and telecom, analog switching applications. They are capable of ultrafast switching speeds (t_r = 1 ns, t_{off} = 9 ns) and excellent transient response. Thanks to the reduced parasitic capacitances, DMOS can handle wideband signals with high OFF-isolation and minimum cross-talk.

The SD210 series of single-channel FETs is available non-zenered to minimize leakage and in Zener protected versions to eliminate electrostatic discharge hazards. The SD5000 series is presented in 16-lead dual in-line plastic or sidebraze ceramic packages, as well as in 14-lead SOT plastic packages. Analog signal voltage ranges up to ±10 V and frequencies up to 1 GHz can be controlled.

APPLICATIONS

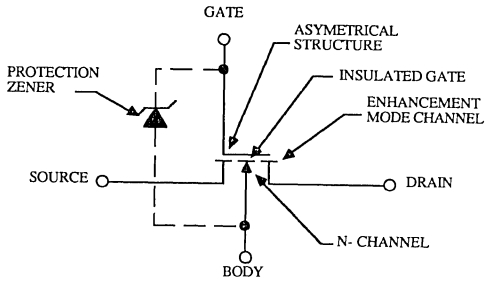
Thanks to the fast switching speeds, low ON-state resistance, high channel-to-channel isolation, low capacitance, and low charge injection, these DMOS devices are especially well suited for a variety of applications such as: high-speed video/audio switching, fast analog or digital signal multiplexing, sample and hold, choppers, etc.

A few of the many possible application areas for DMOS analog switches (and their improved characteristics) are listed below:

1. **Video and RF switching** (high speed, high off-isolation, low cross-talk):
   - Multiple video distribution networks
   - Sampling scanners for RF systems
2. **Audio routing** (glitch-and noise-free)
   - High-speed switching
   - Audio switching systems using digitized remote control
3. **Data acquisition** (high speed, low charge injection, low leakage):
   - High-speed sample and hold
   - Audio and communication analog-to-digital converters
4. **Other:**
   - Digital switching
   - PCM distribution networks
   - UHF Amplifiers
   - VHF Modulators and Double Balanced Mixers
   - High-speed inverters/drivers
   - Switched capacitor filters
   - Choppers

PRINCIPLE OF OPERATION

The electrical symbol shown in Figure 1 provides several important bits of information: It depicts an n-channel enhancement-mode device with an insulated gate and asymmetrical structure. The gate protection Zener is shown with broken lines to indicate that, although it is present on the chip, it is not a main constituent of the fundamental switch structure.



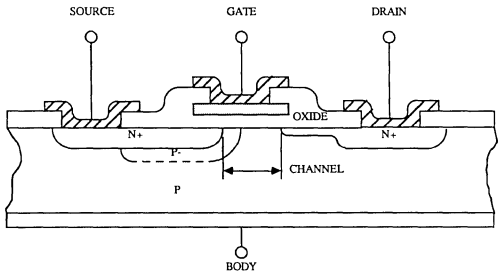
DMOS Electrical Symbol

Figure 1

Each switch is a DMOS n-channel field-effect transistor of the enhancement-mode type; that is, the device is normally OFF when gate-to-source voltage (V_{GS}) is 0 V. The lateral double-diffused MOS (DMOS) transistor, shown in cross-section in Figure 2, has three terminals (source, gate, and drain) on the top surface and one (the body or substrate) on the bottom of the chip. A Zener diode with a breakdown voltage of approximately 40 V is added to protect the gate against overvoltage and electrostatic discharges.

The double-diffusion process creates a thin self-aligning region of p-type material, isolating the source from the drain region. The very short channel length that results between the two junction depths permit achieving extremely low source-to-drain and gate-to-drain capacitances at the same time that provides good breakdown voltages.

The silicon-gate process allows for high manufacturing repeatability and very stable performance without the instabilities associated with the metal-gate technique.

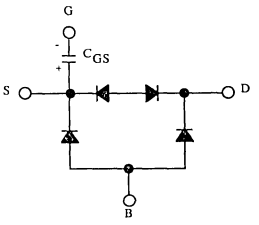


Cross-sectional View of the Idealized DMOS Structure

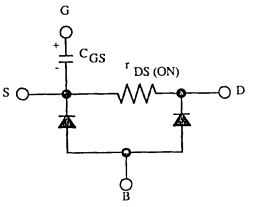
Figure 2

When the gate potential is equal to or negative with respect to the source, the switch is OFF. In this state, the p-type material in the channel forms two back-to-back diodes and prevents channel conduction (Figure 3a). If a voltage is applied between the S and D regions, only a small junction leakage current will flow.

Figure 3

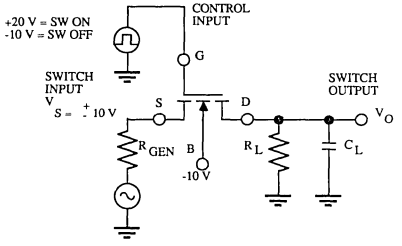


(a) Equivalent "OFF" Circuit



(b) Equivalent "ON" Circuit

The oxide insulator present between gate and source forms a small capacitor that accumulates charge. If the gate-to-source potential (V_{GS}) is made positive, the capacitive effect attracts electrons to the channel area immediately adjacent to the gate oxide. As V_{GS} increases, the electron density in the channel will exceed the hole density, and the channel becomes an n-type region. As the channel conductivity is enhanced, the n-n-n structure then becomes a simple silicon resistor through which current can easily flow in either direction. Figure 4 shows the normal mode of operation of a single switch for ±10 V analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when the drain is used as the output. In this case, the gate is driven by +20, −10 V for which an SD5200, SD210, or D211 could be used.



Normal Switch Configuration for ±10 V Analog Switch

Figure 4

As can be seen from Figures 3a and 3b, the body-source and body-drain pn junction should be kept reverse biased at all times; otherwise, signal clipping and even device damage may occur if unlimited currents are allowed to flow. Body biasing is conveniently set, in most cases, by connecting the substrate to V−.

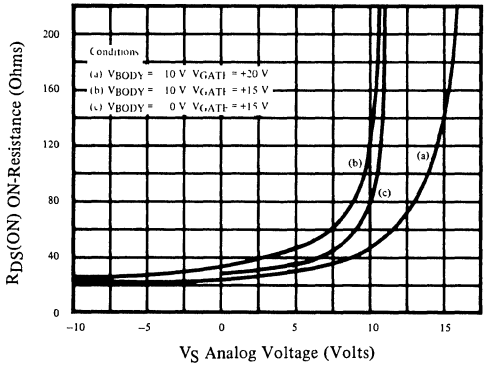
MAIN SWITCH CHARACTERISTICS

$r_{DS(ON)}$

ON-channel resistance is controlled by the electric field present across and along the channel. Channel resistance is mainly determined by the gate-to-source voltage difference. When V_{GS} exceeds the threshold voltage (V_T), the FET starts to turn on.

Numerous applications call for switching a point to ground. In these cases the source and substrate are connected to ground and a gate voltage of 3 to 4 V is sufficient to ensure switching action.

With a V_{GS} in excess of +5 V, a low resistance path exists between the source and the drain. The circuit shown in Figure 4 exhibits the $r_{DS(ON)}$ vs. analog signal voltage relationship shown in Figure 5.



ON-Resistance Characteristics

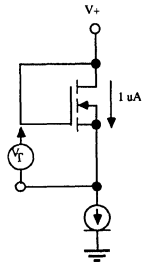
Figure 5

When the analog signal excursion is large (for example ±10 V) the ON-channel resistance changes as a function of signal level. To achieve minimum distortion, this ON-channel resistance modulation should be kept in mind, and the amount of resistance placed in series with the switch should be properly sized. For instance, if the switch resistance varies between 20Ω and 30Ω over the signal range and the switch is in series with a 200-load, the result will be a total ΔR = 4.5%. Whereas, if the load is 100 kΩ, ΔR will only be 0.01%.

THRESHOLD VOLTAGE

The threshold voltage (V_T) is a parameter used to describe how much voltage is needed to initiate channel conduction. Figure 6 shows the applicable test configuration. In this circuit, it is worth noting, for instance, that if the device has a V_T = 0.5 V, when V+ = 0.5 V, the channel resistance will be:

$$R_{channel} = \frac{0.5\ V}{1\ \mu A} = 500\ k\Omega$$

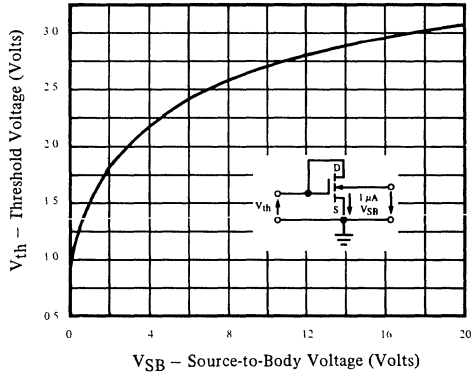


Threshold Voltage Test Configuration

Figure 6

BODY EFFECT

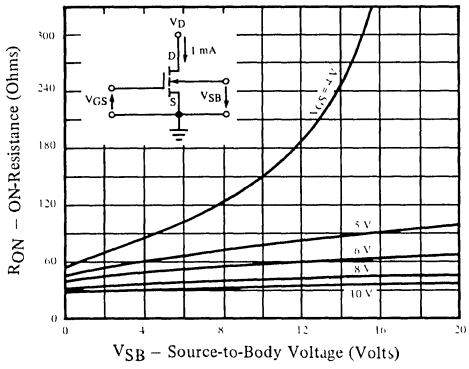
For a MOSFET with a uniformly doped substrate, the threshold voltage is proportional to the square root of the applied source-to-body voltage. The SD5000 family has a non-uniform substrate, and the V_{th} behaves somewhat differently. Figure 7 shows the typical V_{th} variation as a function of the source-to-body voltage V_{SB}.



Threshold vs. Source-to-Body Voltage

Figure 7

As the body voltage increases in the negative direction, the threshold goes up. In consequence, if V_{GS} is small, the ON-resistance of the channel can be very high. Figure 8 shows the effects of V_{SB} and V_{GS} on R_{ON}. Therefore, to maintain a low ON-resistance it is preferable to bias the body to a voltage close to the negative peaks of V_S and use a gate voltage as high as possible.



ON-Resistance vs. Source-to-Body and Gate-to-Source Voltages

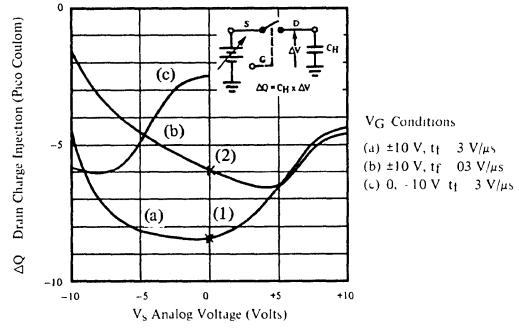
Figure 8

CHARGE INJECTION

Charge injection describes that phenomenon by which a voltage excursion of the gate produces an injection of electric charges via the gate-to-drain and the gate-to-source capacitances into the analog signal path. Another popular name for this phenomenon is "switching spikes."

Since these DMOS devices are asymmetrical[1], the charges injected into the S and D terminals are different. Typical parasitic capacitances are on the order of 0.2 pF for C_{DG} and 1.5 pF for C_{SG}.

Another factor that influences the amount of charge injected is the amplitude of the gate-voltage excursion. This is a directly proportional relationship: the larger the excursion, the larger the injected charge. This can be seen by comparing curves (a) and (c) in Figure 9. One other variable to consider is the rate of gate-voltage change: Large amounts of charge are injected when faster rise and fall times are present at the gate. This is shown by curves (a) and (b) in Figure 9.

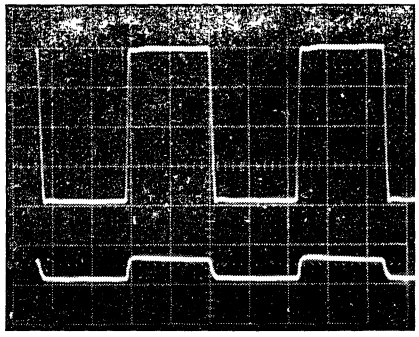


SD5000 Charge Injection

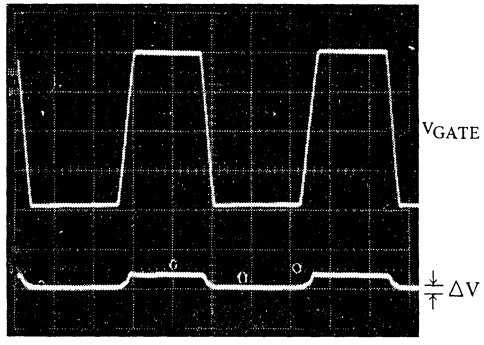
Figure 9

Switching spikes occur at switch turn-on as well as turn-off time. When the switch turns on, the charge injection effect is minimized by the usually low signal-source impedance. This low impedance tends to produce a rapid decay of the extra charge introduced in the channel. At turn-off, however, the injected charge might become stored in a sampling capacitor and create offsets and errors. These errors will have a magnitude that is inversely proportional to the magnitude of the holding capacitance.

Figure 9 illustrates several typical charge injection characteristics. Figure 10 shows some of the corresponding waveforms. The DMOS devices, thanks to their inherent low parasitic capacitances, produce very low charge injection when compared to other analog switches, either PMOS, CMOS, JFET, BIFET etc. Still, when the offsets created are unacceptable, charge injection compensation techniques exist that eliminate or minimize them. The solution basically consists of injecting another charge of equal amplitude but opposite polarity at the time when the switch turns off.



(a) Top: 5 V/div Hor: .5 μs/div
Bot: 50 mV/div Point (1)



(b) Top: 5 V/div Hor: 2 μs/div
Bot: 50 mV/div Point (2)

Waveforms for points (1) & (2) of Figure 7

Figure 10

[1] The chip geometry is such that non-identical behavior occurs when the source and drain terminals are reversed in a circuit.

OFF-ISOLATION AND CROSSTALK

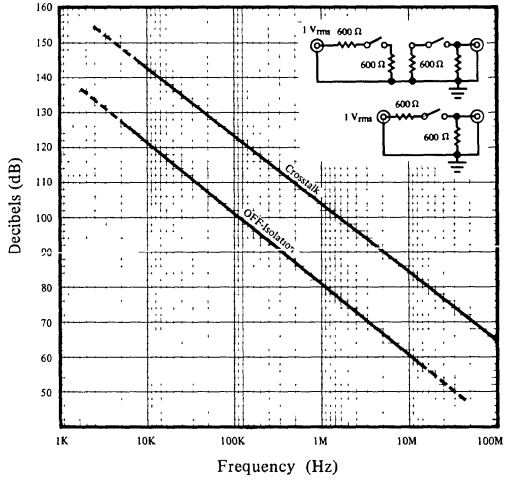
The dc ON-state resistance is typically 30 Ω and the OFF-state resistance is typically 10^{10} Ω, which results in an OFF-state to ON-state resistance ratio in excess of 10^8. However, for video and VHF switching applications, the upper usable frequency limit is determined by how much of the incoming signal is coupled through the parasitic capacitances and appears at the switch output when ideally no signal should appear there, in the OFF state.

Off-isolation is defined by the formula:

$$\text{Off-Isolation (dB)} = 20 \log \frac{V_{out}}{V_{in}},$$

(when the switch is OFF)

When several analog switches are simultaneously being used to control high frequency signals, crosstalk becomes a very important characteristic. For video applications, the stray signal coupled via parasitic capacitances to the signal of an adjacent channel can form ghosts and signal interference. To help obtain high degrees of isolation, it becomes necessary to exercise careful circuit layout, reducing parasitic capacitive and inductive couplings, and to use proper shielding and bypassing techniques. Figure 11 shows the excellent off-isolation and crosstalk performance typical of this family of DMOS analog switches.



SD5000 Crosstalk and OFF-Isolation vs. Frequency

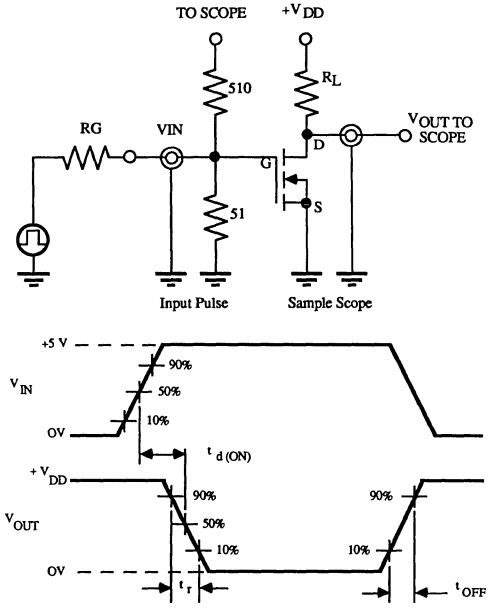
Figure 11

INSERTION LOSS

At low frequencies, the attenuation caused by the switch is a function of its ON-state resistance and the load impedance. They form a simple series voltage divider network. As an example, for a 600-Ω load impedance the insertion loss for voice signals (1 V_{rms} at 3 kHz) is less than 0.3 dB. Thus, the SD5000 series make good telephone crosspoint switches.

SPEED

Because the ON-state resistance and input capacitance are low, the DMOS switches are capable of subnanosecond switching speeds. At these speeds the external circuit rather than the FET itself is often responsible for the rise and fall times that can be obtained. Let's consider the switching test circuit of Figure 12. At turn-on, the fall time observed at the drain is a function of R_G and of the input pulse amplitude and rise time. The sooner C_{GS} reaches V_T, the sooner turn-on will occur, and the lower the $r_{DS(ON)}$ reached, the faster C_{DS} will be discharged.



Switching Test Circuit

Figure 12

The turn-off time (or the rise time of V_D) is not as much limited by the velocity at which C_{GS} can be discharged by the gate control pulse as it is, by the time it takes to charge up C_{DS} and C_{DG} via the load resistor R_L. Table 1 shows typical performance obtained. It is important to realize that stray capacitance and parasitic inductances as well as scope probe capacitance can seriously affect the rise and fall times (switching speed).

Table 1. Typical Switching Times

V_{DD} (V)	R_L (Ω)	$t_{d\ (ON)}$ (ns)	t_r (ns)	*t_{OFF} (ns)
5	680	0.6	0.7	9.0
10	680	0.7	0.8	9.0
15	1K	0.9	1.0	14.0

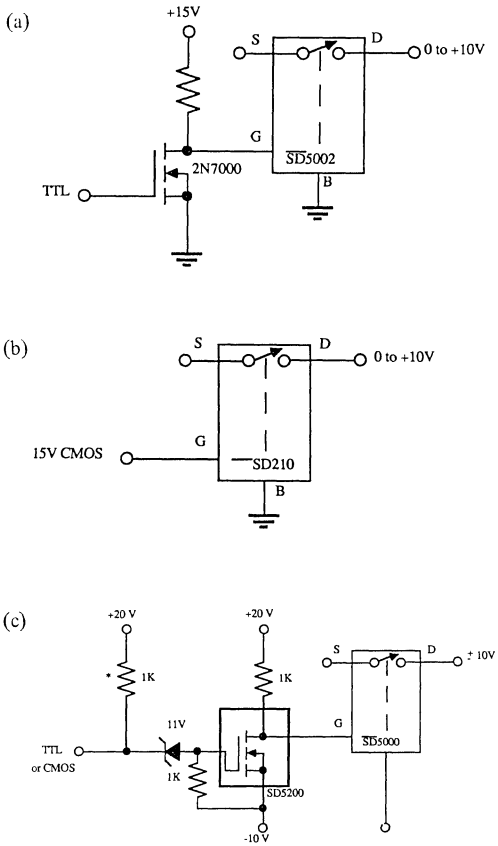
* t_{OFF} is dependent on R_L and does not depend on the device characteristics.

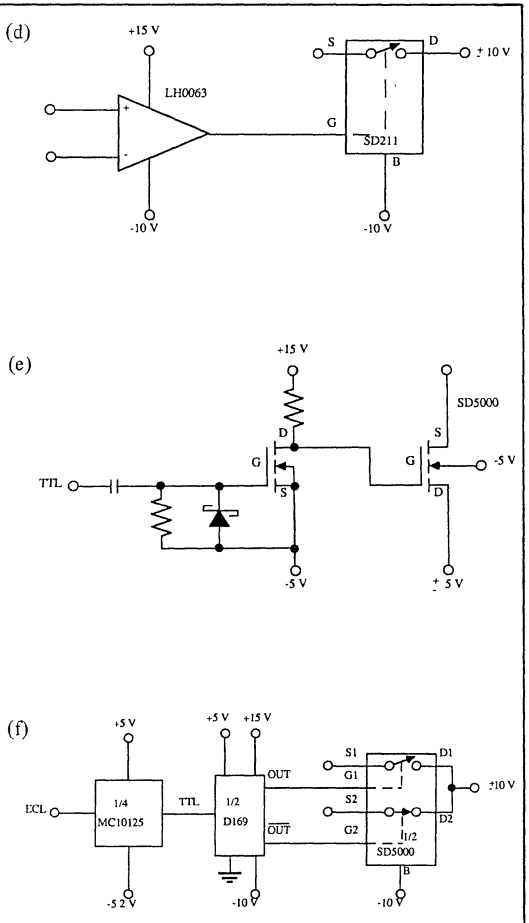
DRIVERS

The switch driver's function is to translate logic control levels, (either TTL, CMOS or ECL) into the appropriate voltages needed at the gate so that the switch can be turned ON or OFF.

The SD5200 operates as an inverter capable of driving up to 30 V. This high voltage rating, together with its high speed, make it an ideal driver for the other members of the SD5000 family. Figure 13 shows this and several other driving methods. The Siliconix D169 is a convenient TTL compatible driver.

Since switching times depend on the C_{GS} charge/discharge times, it is important to note that the driver's current source/sink capability plays a very important role in the process.





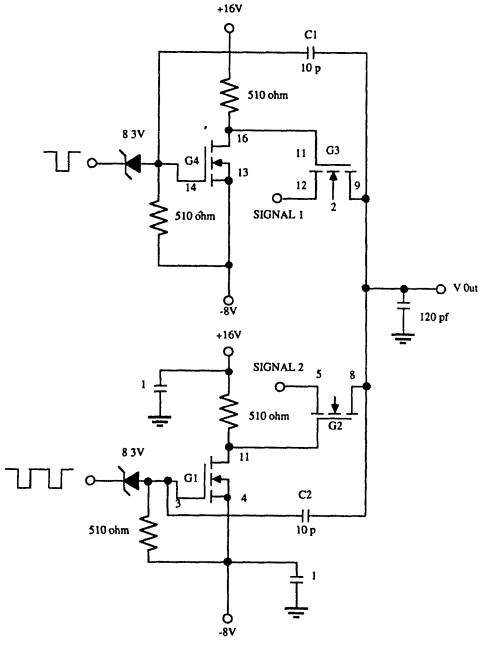
Various DMOS Drivers

Figure 13

7

DESIGN IDEA

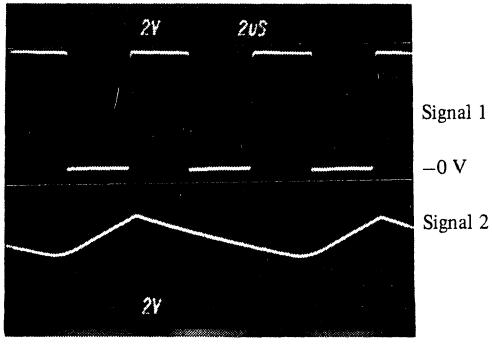
In a typical application, the circuit of Figure 14 is used to multiplex, sample, and hold two analog signals at a 5-MHz rate. Two of the switches in an SD5000 are used as level shifter/drivers to provide the gate drive of the single-pole-double-throw arrangement formed by switches 3 and 4. Capacitors C1 and C2 provide charge injection compensation.



5 MHz Multiplexer and Sample-and-Hold Circuit

Figure 14

Signal 1 is a 6-V, 156 kHz square wave. Signal 2 is a 2-V_{pp}, 78-kHz alternating waveform with a dc offset of –3.4 V (Figure 15).

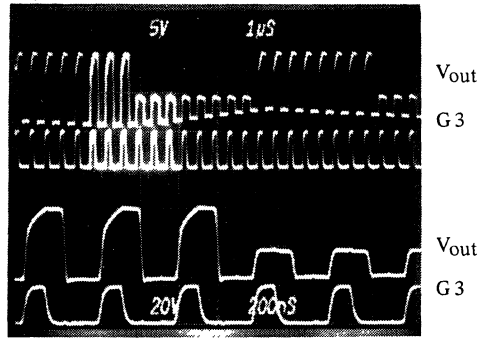


The Two Analog Signals to be Sampled

Figure 15

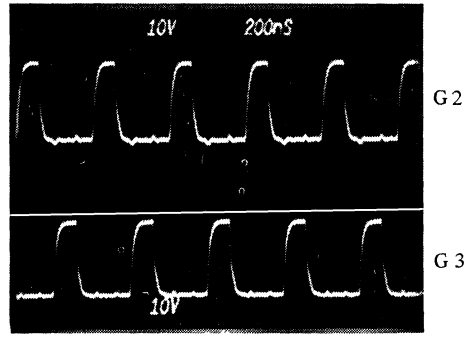
Figure 16 illustrates the resulting composite waveform present at the holding capacitor along with the gate 3 control signal.

As can be seen, the switching times are about 15 ns, the acquisition time is 80 ns, and the holding time is about 90 ns. The total sample-and-hold cycle has taken 200 ns. Even though not maximized, this speed is faster than what any other presently available (50 ns) analog switch products can achieve.



Composite Sample and Hold Output Along with Gate 3 Control Signal

Figure 16

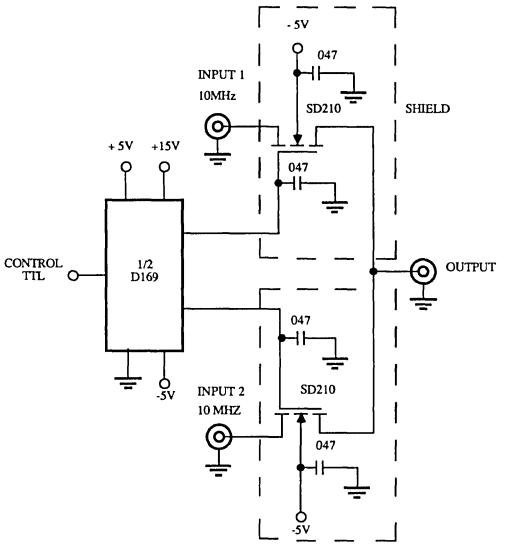


Gate Control Signals for the SPDT Switch Configuration

Figure 17

The timing and amplitude of gate 3 and gate 4 control-signals can be examined in Figure 17.

Figure 18 shows a single-pole-single-throw configuration used to select one of two AM modulated 10-MHz signals. Figure 19 illustrates the two waveforms available at the output. Table 2 contains typical values of crosstalk and off-isolation attainable with this configuration.

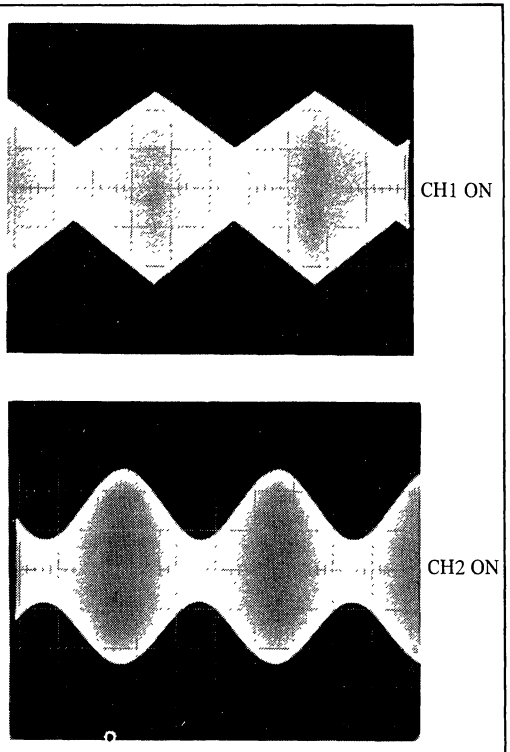


High Frequency SPDT Switch

Figure 18

Table 2. SPDT Switch Performance

FREQ	SIG LVL	INS LOSS	OFF ISOL	XTALK
100 kHz	0 dBm	1.8 dB	80 dB	113 dB
1 MHz	0 dBm	1.8 dB	70 dB	92 dB
5 MHz	0 dBm	1.9 dB	69 dB	69 dB
10 MHz	0 dBm	2.0 dB	61 dB	65 dB
10 MHz	6 dBm	2.0 dB	61 dB	66 dB
10 MHz	12 dBm	2.0 dB	61 dB	66 dB



Scales – Vert: 1 V/div
Horiz: 20 μs/div

Two 10 MHz AM Modulated Outputs for the SPDT Switch of Figure 14

Figure 19

REFERENCES

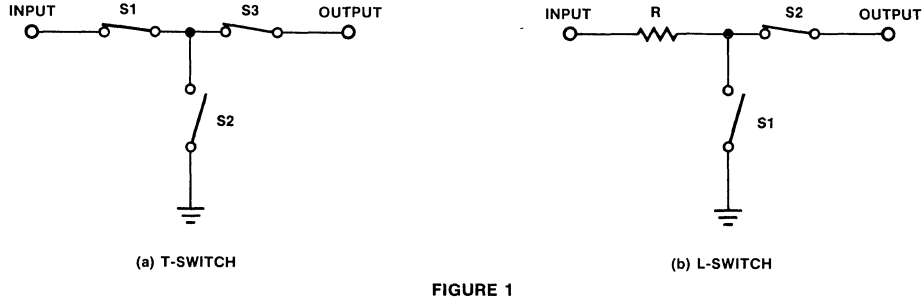
1. *"Signetics D-MOS Data,"* booklet (1982).
2. Bob Zavel,*"A High Quality Audio Crosspoint Switch,"* Siliconix Application Note AN83-7 (October 1983).
3. Bob Zavrel, *"A High Performance Video Switch Using the SD5002,"* Siliconix Application Note AN83-15 (December 1983).
4. R. R. Schellenbach, *"Switched Capacitor Filters – An Economical Approach to Critical Filtering,"* Integrated Circuits Magazine (October, 1984).

A High Performance Video Switch Using the SD5002

As the trend toward more advanced video systems accelerates, designers will need improved switching techniques. High resolution video and advanced computer graphics are only two areas demanding better switch performance. A high performance solution to this problem is presented here. The desirable characteristics of a high performance video switch include:

1. low cost
2. flat response from DC to VHF
3. minimal phase shift and group delay
4. constant input and output impedances
5. unity or variable switch gain
6. direct control by digital gates
7. minimum parts count
8. small size
9. very high switching speed (< 1 ns.)
10. low channel crosstalk
11. useof only DC coupling

The physical size of a video switch may be reduced and the design simplified by using integrated circuit analog switches. With this reduced size, however, increased crosstalk is introduced because of increased switch-to-switch capacitance. A fundamental goal of video switch design is to take advantage of the IC switch while minimizing crosstalk. The two popular schemes that have been developed to realize this goal are shown in Figure 1. In the "T" switch, S1 and S3 are used to route the signal to the load. S2 closes when the "T" configuration is "off" providing a near ground potential to the switch node and greatly reducing crosstalk. Unfortunately analog switches each have a channel capacitance which has an undesirable effect on frequency response and phase linearity. To minimize this capacitance, we can simply use fewer switches. The "L" configuration uses two switches but requires a loading resistor R (Fig. 1). R also serves as an isolation pad for the video source.



(a) T-SWITCH

(b) L-SWITCH

FIGURE 1
Equivalent circuits for a T-switch, a, and L-switch, b.

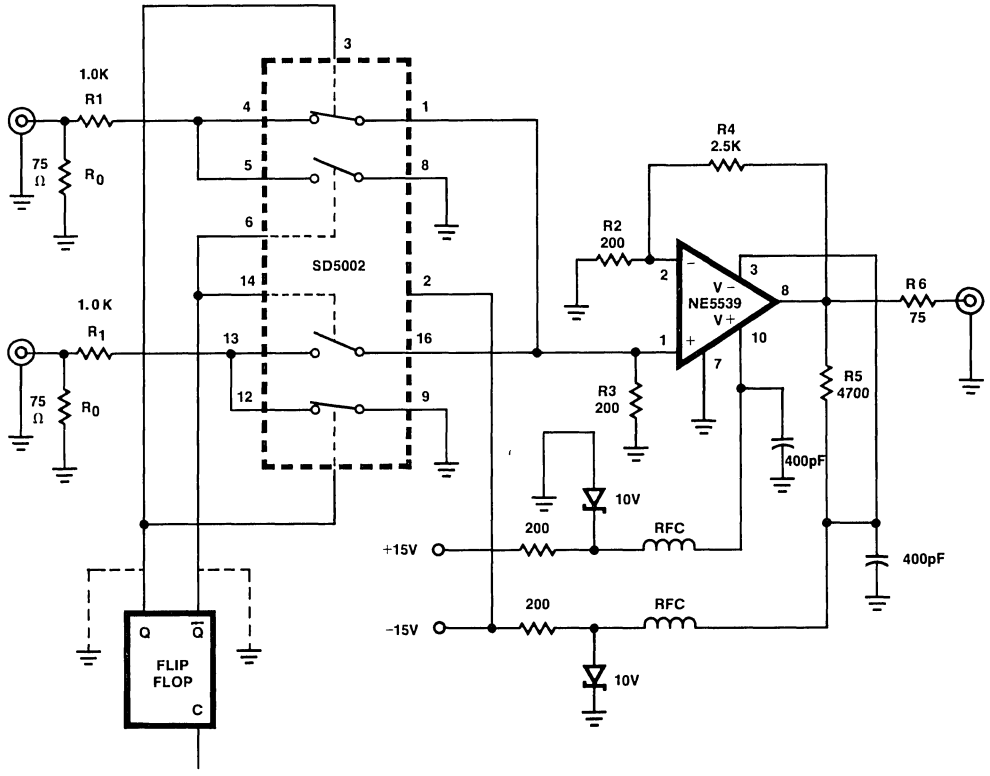


FIGURE 2
Actual circuit of a video switch with an L-configuration.

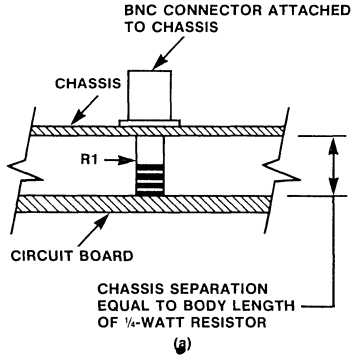
Figure 2. shows the completed circuit, a one-of-two switch with a summing amplifier. The video source's line can be terminated either externally or internally to the switch (R0). With this termination resistor, a load change of less than 1 ohm will be "seen" by the source when the switch changes state. For this reason input isolation amplifiers are not necessary.

Siliconix SD5002 analog switches were chosen because of low "on" resistance, very low switch capacitance, and high switching speed. Also, the SD5002 can be directly controlled by standard CMOS logic gates or from TTL gates through standard interface techniques. The Siliconix SD213 is the discrete equivalent to the SD5002 IC. Use of these discrete devices can reduce crosstalk at the expense of increased switch size and greater circuit complexity. The Signetics NE5539 was chosen as a summing amplifier because of its very high slew rate and gain bandwidth product. R4 (Fig. 2) can be varied to control circuit gain but should never be less than a value of 1400 ohms since the NE5539 is internally compensated for gain values greater than 7. A value of approximately 2500 ohms for 4R will set circuit gain to near unity. Additionally, the circuit output impedance is set by R6 while R5 sets the output DC offset to near-zero.

Use of high quality components alone will not guarantee top performance. Circuit board layout and shielding are critical for meeting the desired specifications. The switch should be considered a subassembly with its own chassis even if included in a larger system. The designer should be ever mindful of stray capacitances and inductances. 1 pf of lead capacitance represents about 5K ohms of reactance at 30 MHz, which can ruin the crosstalk performance. The input and output BNC connectors should be mounted directly above or below the appropriate points on the circuit board (Fig. 3). Double sided PC board should be used with signal route leads etched as short as possible. The pin configurations of the SD5002 and NE5539 plastic DIP packages are very helpful to this end, which is evident on inspection.

Gate voltage control can be implemented by a very wide range of techniques including mechanical switches or logic gates. Since the two switches for each channel input in effect form a SPDT switch, a flip-flop logic circuit is a good choice for circuit control. Figure 2 shows the special case of a one-of-two channel switching circuit. The gate of the grounding switch of channel 1 is tied to the gate of the series switch of channel 2 and vice-versa. Thus in this unique case, one flip-flop may be used to control all four switches.

Figure 4 shows the response of the circuit from input to output with the applicable channel turned "on." Very good response linearity has been realized from DC to VHF which should prove to be quite adequate for the most demanding applications. Figure 5 shows channel-to-channel crosstalk isolation with equal input level signals and with channel 1 "on" and channel 2 "off." It can be seen that crosstalk isolation is better than 60 db. at 10 MHz. The switch was tested with a staircase test signal for various video response parameters. The photographs (Figs. 6 to 10) show the results while Chart 1 shows the test set-up used during this test. The photographs indicate imperceptible switch influences on the test signal.



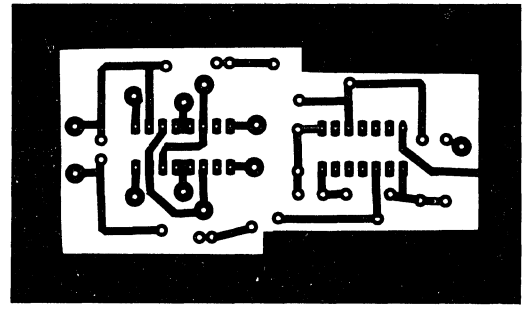


FIGURE 3
Suggested method for mounting BNC connectors, a; printed-circuit pattern of the prototype board, b.

The switch specifications exceeded the resolution of the test equipment used. Chart 2 shows the test set-up used for the crosstalk and response tests.

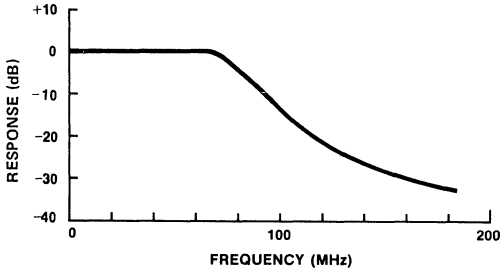


FIGURE 4
Frequency response for the circuit of Figure 2.

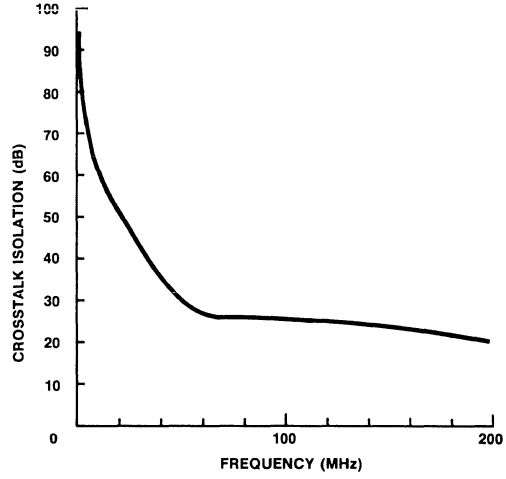


FIGURE 5
Channel-to-channel crosstalk isolation for the L-switch configuration.

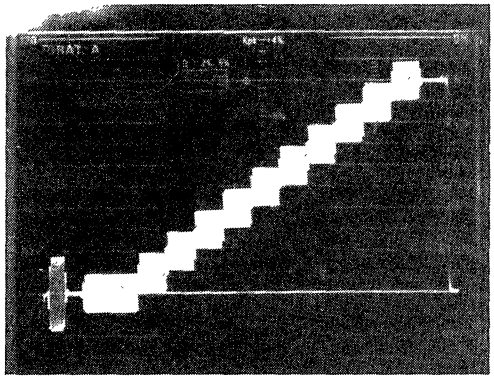


FIGURE 6
Staircase input test signal.

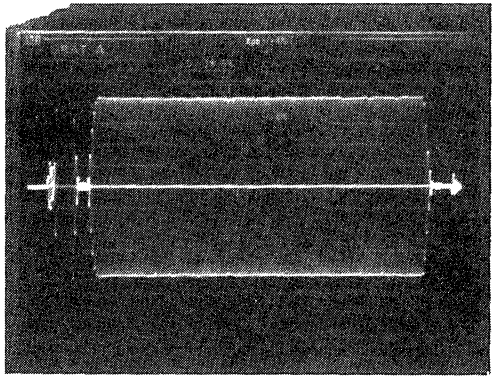


FIGURE 7
Small portion of the output video signal showing chroma.

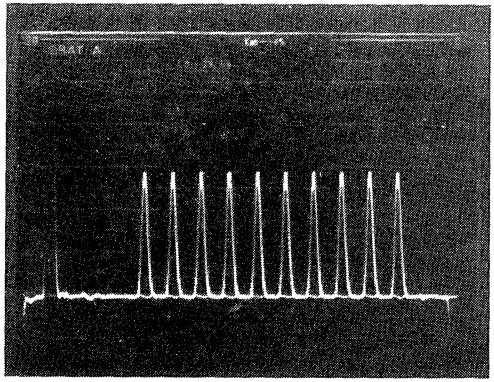


FIGURE 8
Risers (derivative) of the staircase input signal.

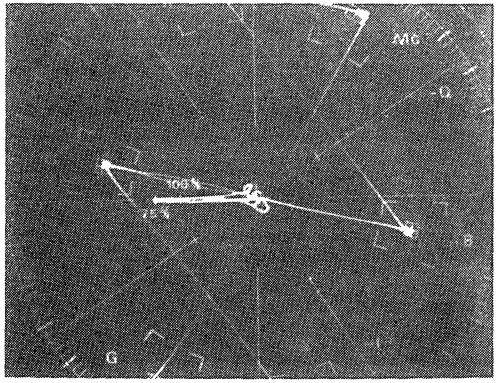


FIGURE 9
Vector scope of the color bars.

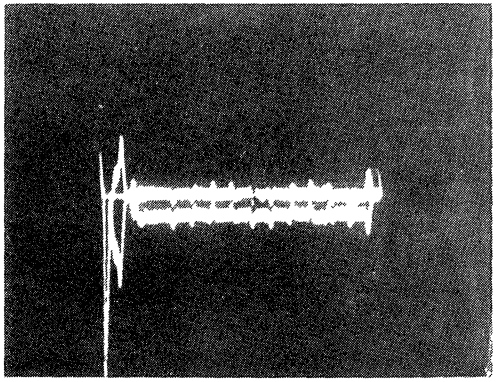
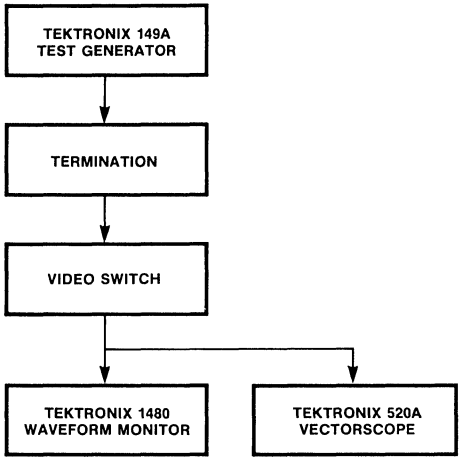


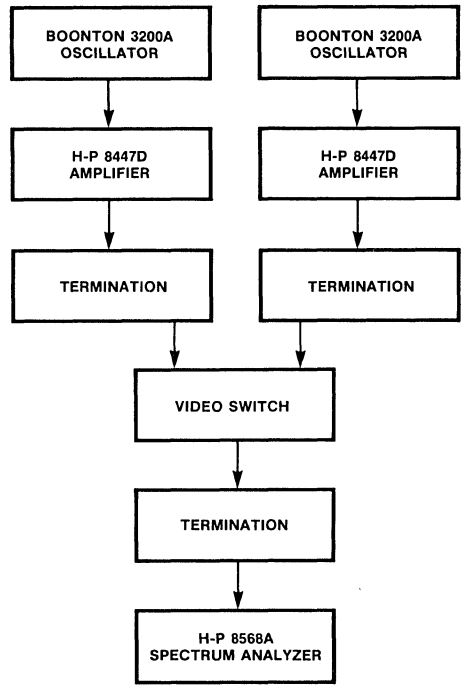
FIGURE 10
Phase shift test: parallel lines indicate no phase shift.

CHART 1



Instrumentation set-up for the video parameter tests.

CHART 2



Instrumentation set-up for the video crosstalk and frequency-response tests.

A High Quality Audio Crosspoint Switch

INTRODUCTION

Recent advances in analog switch integrated circuits have made superior audio switch specifications possible. A crosspoint switch for the most demanding audio applications is described here. Although this switch may be used in recording studio and radio broadcast mixers where little compromise is acceptable, the low cost and small size makes this switch ideal for a much more diverse range of applications. Such applications can include audio follow switches found in video systems, audio synthesizers, high quality multiplexers, and home entertainment systems.

A high quality audio frequency switch should have the following features:

1. Reasonable cost
2. Unity or variable gain
3. Very low harmonic distortion (<.01%)
4. Flat response (DC to > 1 MHz.)
5. Low crosstalk
6. High "Off" Isolation
7. Excellent phase linearity
8. High speed switching (< 1 ns.)
9. freedom from switch "popping"
10. Small size
11. Direct control by digital gates
12. Use of DC coupling only

The size of a complex audio switching array can be greatly reduced by using IC analog switches. The prototype array is an 8x2 stereo crosspoint switch mounted on a 4x7 inch board. Other switch configurations may be fabricated with little effect on the switch characteristics. This single board can replace a score of rotary switches and the bundles of audio cable often found in audio mixers. Furthermore, ground loop problems are reduced by eliminating the cable bundles.

Siliconix SD5002s were chosen because of low "on" resistance, low switch capacitance, and very fast switching times. The National Semiconductor LF347 quad op-amp was chosen for its excellent audio characteristics in a quad package. Two LF347s are used in this switch providing a summing and output amplifier for each of four channels. The SD5002s are held "normally open" by biasing the switch gates to ground potential through 10K ohm resistors. For any switch configuration, the appropriate switch(es) are closed by biasing the appropriate gate(s) to the positive voltage supply. In this circuit pairs of switches are controlled together to affect the left and right channels of a stereo input simultaneously. This is accomplished simply by tying the applicable switch gates together and using a common bias resistor. The ability to directly interface the SD5002 gates to digital integrated circuits opens up immense opportunities to the design engineer for switch control.

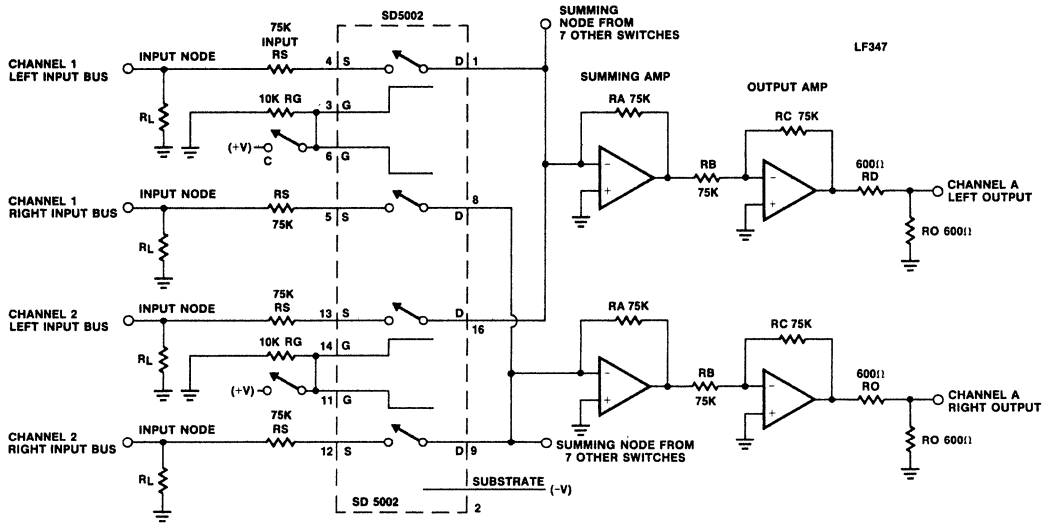


FIGURE 1

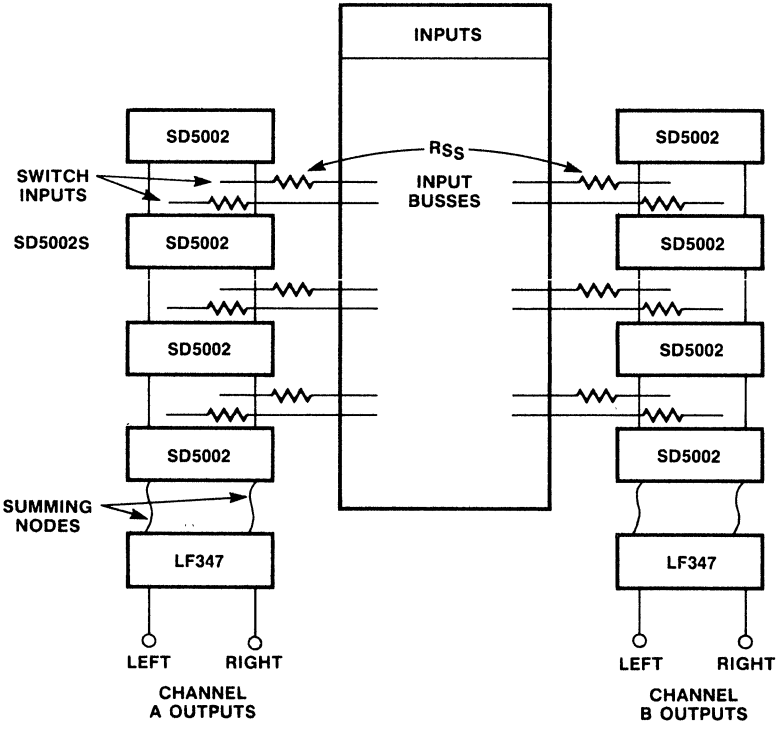


FIGURE 2

Figure 1 shows how a single SD5002 is configured as a 2x1 stereo switch. Figure 2 shows how the circuit can be expanded into a switch matrix. Eight SD5002s are required to construct the 8x2 stereo matrix array. One RL is required for each channel input for termination while separate RSs are employed to feed the signal from the inputs to the various switches. An input bus is consequently formed at the junction of these resistors.

The summing nodes are located at the inverting inputs of the summing amplifiers. The SD 5002 drains are connected to these summing nodes. A larger array will cause reduced system performance due to longer lead lengths and increased circuit capacitance. Nevertheless, large matricies can be configured with little performance compromise because of the low initial switch capacitance. RL's value should reflect the value of the source impedance. Deletion of RL will seriously degrade crosstalk and off isolation performance while lower values of RL will improve these specifications. RC may be adjusted for a wide range of system gain while a value of about 150K ohms will set the circuit to unity gain. RD sets the value of the output impedance and if the switch is to feed a high impedance load, RO should be included to maintain system performance.

Electrolytic and mica capacitors are used on the circuit board for bypassing the two power supply voltages. Supply voltage bypassing will reduce both high and low frequency noise and help stabilize the system. The entire circuit should be well shielded particularly if it will be exposed to strong RF or power line fields. Conductors carrying high currents should be kept away from the circuit. Double sided PC board should be used creating a ground plain on the component side as an additional precautionary measure.

Table 1 shows the switch performance of the 8x2 crosspoint configuration. RL was set to 10K ohms, reflecting the high impedance of the test oscillator's output. Regulated power supply voltages of plus and minus 9 to 15 volts may be used. The signal voltages should be kept under about 3.5 volts PTP to maintain switch performance.

TABLE 1

Frequency (Hz.)	Crosstalk	"Off" Isolation	%THD
50	−74db.	−75db.	.006
100	−74	−75	.005
200	−74	−75	.004
500	−74	−75	.003
1K	−74	−75	.003
2K	−73	−74	.003
5K	−70	−71	.003
10K	−67	−68	.004
20K	−62	−62	.006
50K	−55	−55	.020
100K	−50	−49	.045

Signal voltages: 3 volts P.T.P.
supply voltages: + and − 12 volts

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