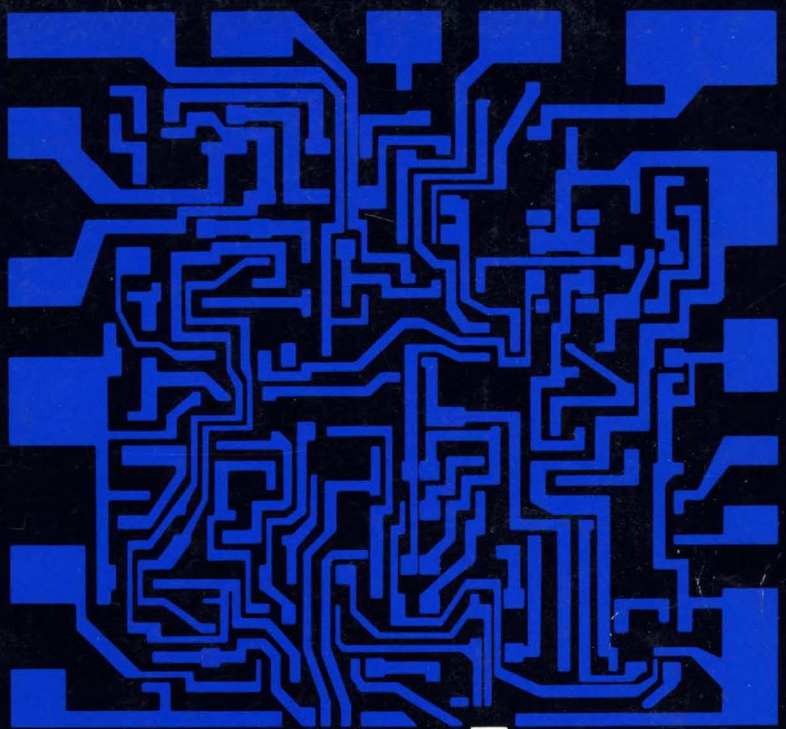


signetics

digital
linear
mos

Supplement No.1, 1974

Supplement No.1 1974
signetics
digital linear mos

SIGNETICS CORPORATION

Signetics Corporation reserves the right to make changes in the products contained in this book in order to improve design or performance and to supply the best possible product.

Signetics Corporation assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

Only the following product lines will be made available for military applications (i.e., applications requiring full military temperature range and/or specifications other than those on the device data sheets).

54 Series
54S Series
82 Series (except as noted on the data sheet)
82S Series (except as noted on the data sheet)
8T Series (except as noted on the data sheet)
Bipolar Memories: 82S06, 82S07

Linear devices will generally be available in military temperature range but such availability will be limited to ceramic DIP and T-05/T-03 can package configurations. Linear devices will not be available to environmental specifications other than Signetics standard production screening tests.

Your local Signetics representative will be happy to provide information on alternate devices and/or sources for discontinued military product types.

NUMERICAL INDEX AND TABLE OF CONTENTS

54/74

FUNCTIONAL INDEX AND TABLE OF CONTENTS

SALES OFFICES

NORTHEAST REGIONAL SALES OFFICES

Lexington, Massachusetts 02173
594 Marrett Road, Suite 7-11
Phone: (617) 861-0840
TWX: (710) 326-6711

Wappingers Falls, New York
P.O. Box 66
Phone: (914) 297-4074

ATLANTIC STATES REGIONAL SALES OFFICES

Atlanta, Georgia 30339
Executive Office Suite, #250
6666 Powers Ferry Rd.
Phone: (404) 252-2832

Pompano Beach, Florida 33062
950 Federal Highway
Phone: (305) 782-8225
TWX: (510) 956-9401

Piscataway, New Jersey 08854
255 Old New Brunswick Rd.
Phone: (201) 981-0123
TWX: (710) 997-9669

Medford, New Jersey 08055
Cedar Brook Building
Taunton Blvd.
Phone: (609) 665-5071
TWX: (510) 683-6291

Rockville, Maryland 20852
11400 Rockville Pike, Suite 304
Phone: (301) 881-5710
TWX: (710) 828-0532

Woodbury, Long Island, New York 11797
20 Crossway Park, North
Phone: (516) 364-9100
TWX: (510) 221-2158

CENTRAL REGIONAL SALES OFFICES

Birmingham, Michigan 48011
725 S. Adams Road
Phone: (313) 642-0420
TWX: (810) 232-1673

Dallas, Texas 75230
12830 Hillcrest, Suite 207
Phone: (214) 661-1296
TWX: (910) 860-5475

Indianapolis, Indiana 46205
4002 Meadows Drive, Suite L-6
Phone: (317) 545-3232
TWX: (810) 341-3248

Minneapolis, Minnesota 55431
8200 Humboldt Ave., S.
Phone: (612) 884-7451
TWX: (910) 576-2845

Rolling Meadows, Illinois 60008
5105 Tollview Drive
Phone: (312) 259-8300
TWX: (910) 687-0765

NORTHWEST REGIONAL SALES OFFICE

Sunnyvale, California 94086
465 Mathilda, Suite 301
Phone: (408) 736-7565

SOUTHWEST REGIONAL SALES OFFICES

Encino, California 91316
15910 Ventura Blvd., Suite 813
Phone: (213) 990-2610
TWX: (910) 495-1772

Irvine, California 92664
2061 Business Center Drive, Suite 214
Phone: (714) 833-8980 or
(213) 924-1668
TWX: (910) 595-1506

Phoenix, Arizona 85022
12601 N. Cave Creek Rd., Suite 105
Phone: (602) 971-2517
TWX: (910) 950-1299

San Diego, California 92111
6827 Convoy Court
Phone: (714) 560-0242
TWX: (910) 335-2086

CANADIAN REGIONAL SALES OFFICE

Rexdale, Ont., Canada M9W-1H5
282 Belfield Road
Phone: (416) 677-6303
TWX: (610) 492-9373
TELEX: 06-968-735

REPRESENTATIVES

COLORADO

- **Denver 80237:**
  Parker/Webster Company
  3615 South Tamarac
  Phone: (303) 770-1972

CONNECTICUT

- **Washington Depot 06794**
  Kanan Associates
  P.O. Box 127
  Phone: (203) 868-0513

FLORIDA

- **Altamonte Springs 32701:**
  WMM Associates, Inc.
  505 Tivoli Ct.
  Phone: (305) 831-4645
- **Clearwater 33515:**
  WMM Associates, Inc.
  1822 Drew Street
  Phone: (813) 447-2533
- **Pompano Beach 33060:**
  WMM Associates, Inc.
  1628 E. Atlantic Blvd.
  Phone: (305) 943-3091

KANSAS

- **Olathe 66061:**
  B. C. Electronic Sales, Inc.
  1015 W. Santa Fe
  Phone: (913) 782-6696

MASSACHUSETTS

- **Reading 01867:**
  Kanan Associates
  100 Main Street
  Phone: (617) 944-8484

MICHIGAN

- **Detroit 48224:**
  Rathsburg Associates, Inc.
  16621 East Warren Avenue
  Phone: (313) 882-1717

MISSOURI

- **Hazelwood 63042:**
  B. C. Electronic Sales, Inc.
  348 Brookes Drive
  Phone: (314) 731-1255

NEW MEXICO

- **Albuquerque 87110:**
  The Staley Company, Inc.
  2925 Charleston N.E.
  Phone: (505) 294-2660

UPSTATE NEW YORK

- **Dewitt 13214:**
  TriTech Electronics, Inc.
  P.O. Box C
  Phone: (315) 446-2881

OHIO

- **Centerville 45459:**
  Norm Case Associates
  P.O. Box 217
  Phone: (513) 435-1301
- **Fairview Park 44126:**
  Norm Case Associates
  P.O. Box 4791
  Phone: (216) 333-4120

OREGON

- **Portland 97221:**
  Western Technical Sales
  2035 S.W. 58th Avenue
  Phone: (503) 297-1711

WASHINGTON

- **Bellevue 98005:**
  Western Technical Sales
  P.O. Box 902
  Phone: (206) 641-3900

DISTRIBUTORS

ARIZONA

- **Phoenix 85034:**
  Hamilton/Avnet Electronics
  2615 S. 21st St.
  Phone: (602) 275-7851
- **Phoenix 85034:**
  Kierulff Electronics
  2633 East Buckeye Road
  Phone: (602) 273-7331

CALIFORNIA

- **Culver City 90230:**
  Hamilton Electro Sales
  10912 W. Washington
  Phone: (213) 870-7171
- **El Segundo 90245:**
  Liberty Electronics
  124 Maryland St.
  Phone: (213) 322-8100
- **Los Angeles 90040:**
  Kierulff Electronics
  2585 Commerce Way
  Phone: (213) 685-5511
- **Mountain View 94041:**
  Hamilton/Avnet Electronics
  575 East Middlefield Road
  Phone: (415) 961-7000
- **Palo Alto 94303:**
  Kierulff Electronics
  3969 East Bayshore Road
  Phone: (415) 968-6292
- **San Diego 92123:**
  Cramer Electronics
  8975 Complex Drive
  Phone: (714) 565-1881
- **San Diego 92123:**
  Hamilton/Avnet Electronics
  8917 Complex Dr.
  Phone: (714) 279-2421
- **San Diego 92123:**
  Kierulff Electronics
  8797 Balboa Avenue
  Phone: (714) 278-2112
- **Sunnyvale 94086:**
  Cramer Electronics
  720 Palomar
  Phone: (408) 739-3011

COLORADO

- **Denver 80222:**
  Cramer Electronics
  5465 E. Evans Place at Hudson
  Phone: (303) 758-2100
- **Denver 80216:**
  Hamilton/Avnet Electronics
  5921 N. Broadway
  Phone: (303) 534-1212

CONNECTICUT

- **Hamden 06514:**
  Arrow Electronics
  295 Treadwell Street
  Phone: (203) 248-3801
- **Georgetown 06829:**
  Hamilton/Avnet Electronics
  643 Danbury Road
  Phone: (203) 762-0361
- **North Haven 06473:**
  Cramer Electronics
  35 Dodge Avenue
  Phone: (203) 239-5641

FLORIDA

- **Hollywood 33021:**
  Hamilton/Avnet Electronics
  4020 No. 29th Ave.
  Phone: (305) 925-5401
- **Hollywood 33020:**
  Schweber Electronics
  2830 North 28th Terrace
  Phone: (305) 927-0511
- **Orlando 32805:**
  Hammond Electronics
  911 West Central Blvd.
  Phone: (305) 241-6601

GEORGIA

- **Atlanta 30340:**
  Schweber Electronics
  4126 Pleasantdale Road, Suite 14
  Phone: (404) 449-9170
- **Norcross 30071:**
  Hamilton/Avnet Electronics
  6700 Interstate 85 Access Rd.
  Suite 2B
  Phone: (404) 448-0800

ILLINOIS

- **Elk Grove 60007:**
  Schweber Electronics
  1380 Jarvis Avenue
  Phone: (312) 593-2740
- **Elmhurst 60126:**
  Semiconductor Specialists
  195 Spangler Avenue
  Elmhurst Industrial Park
  Phone: (312) 279-1000
- **Schiller Park 60176:**
  Hamilton/Avnet Electronics
  3901 No. 25th Avenue
  Phone: (312) 678-6310

INDIANA

- **Indianapolis 46241:**
  Semiconductor Specialists
  P.O. Box 41630, Weir Cook Airport
  Phone: (317) 243-8271

KANSAS

- **Lenexa 66215:**
  Hall-Mark Electronics
  9006 Rosehill Road
  Phone: (913) 888-4747
- **Lenexa 66215:**
  Hamilton/Avnet Electronics
  37 Lenexa Industrial Center
  9900 Pflumm Road
  Phone: (913) 888-8900

MARYLAND

- **Hanover 21076:**
  Hamilton/Avnet Electronics
  7255 Standard Drive
  Phone: (301) 796-5000
- **Rockville 20850:**
  Pioneer Washington Electronics
  1037 Taft Street
  Phone: (301) 424-3300
- **Rockville 20852:**
  Schweber Electronics
  5640 Fisher Lane
  Phone: (301) 881-2970

MASSACHUSETTS

- **Burlington 01803:**
  Hamilton/Avnet Electronics
  185 Cambridge Street
  Phone: (617) 273-2120
- **Newton 02159:**
  Cramer Electronics
  85 Wells Avenue
  Phone: (617) 969-7700
- **Waltham 02154:**
  Schweber Electronics
  213 Third Ave.
  Phone: (617) 890-8484

MICHIGAN

- **Detroit 48240:**
  Semiconductor Specialists, Inc.
  25127 W. Six Mile Road
  Phone: (313) 255-0300
- **Livonia 48150:**
  Hamilton/Avnet Electronics
  12870 Farmington Road
  Phone: (313) 522-4700
- **Troy 48084:**
  Schweber Electronics
  86 Executive Drive
  Phone: (313) 583-9242

MINNESOTA

- **Edina 55435:**
  Hamilton/Avnet Electronics
  7683 Washington Ave., S.
  Phone: (612) 941-3801
- **Minneapolis 55420:**
  Semiconductor Specialists
  8030 Cedar Avenue South
  Phone: (612) 854-8844

MISSOURI

- **Hazelwood 63042:**
  Hamilton/Avnet Electronics
  364 Brookes Lane
  Phone: (314) 731-1144
- **St. Louis 63134:**
  Hall-Mark Electronics
  6100 Madison Avenue
  Phone: (314) 521-3800

NEW MEXICO

- **Albuquerque 87108:**
  Cramer Electronics
  137 Vermont, N.E.
  Phone: (505) 265-5767
- **Albuquerque 87117:**
  Hamilton/Avnet Electronics
  2450 Baylor Dr., S.E.
  (P.O. Box 9081)
  Phone: (505) 765-1500

NEW YORK

- **Buffalo 14202:**
  Summit Distributors
  916 Main Street
  Phone: (716) 884-3450
- **Farmingdale, L. I. 11735:**
  Arrow Electronics
  900 Broad Hollow Rd.
  Phone: (516) 694-6800
- **Rochester 14623:**
  Schweber Electronics
  2 Townline Circle
  Phone: (716) 461-4000
- **Syracuse 13057:**
  Hamilton/Avnet Electronics
  6500 Joy Road
  Phone: (315) 437-2642
- **Westbury, L.I. 11590:**
  Hamilton/Avnet Electronics
  70 State Street
  Phone: (516) 333-5800
- **Westbury, L.I. 11590:**
  Schweber Electronics
  Jericho Turnpike
  Phone: (516) 334-7474

NORTHERN NEW JERSEY

- **Cedar Grove 07009:**
  Hamilton/Avnet Electronics
  218 Little Falls Road
  Phone: (201) 239-0800
- **Saddlebrook 07662:**
  Arrow Electronics
  285 Midland Avenue
  Phone: (201) 797-5800

SOUTHERN NEW JERSEY AND PENNSYLVANIA

- **Cherry Hill, N. J. 08034:**
  Milgray-Delaware Valley
  1165 Marlkress Road
  Phone: (609) 424-1300
- **Moorestown 08057:**
  Arrow/Angus Electronics
  Pleasant Valley Ave.
  Phone: (609) 235-1900
- **Mt. Laurel, N. J. 08057:**
  Hamilton/Avnet Electronics
  113 Gaither Dr.
  E. Gate Industrial Park
  Phone: (609) 234-2133

CENTRAL NEW JERSEY AND PENNSYLVANIA

- **Somerset, N. J. 08873:**
  Schweber Electronics
  43 Belmont Drive
  Phone: (201) 469-6008

NORTH CAROLINA

- **Greensboro 27406:**
  Hammond Electronics
  P.O. Box 21728
  Phone: (919) 275-6391

OHIO

- **Beechwood 44122:**
  Schweber Electronics
  23880 Commerce Park Road
  Phone: (216) 464-2970
- **Dayton 45459:**
  Hamilton/Avnet Electronics
  118 W. Park Road
  Phone: (513) 433-0610
- **Cleveland 44122:**
  Arrow Electronics
  23500 Mercantile Rd.
  Phone: (216) 464-2000
- **Cleveland 44105:**
  Pioneer Standard Electronics
  4800 East 131st Street
  Phone: (216) 587-3600
- **Kettering 45429:**
  Arrow Electronics
  3100 Plainfield Road
  Phone: (513) 253-9176

TEXAS

- **Dallas 75220:**
  Cramer Electronics
  2970 Blystone Ave.
  Phone: (214) 350-1355
- **Dallas 75207:**
  Hamilton/Avnet Electronics
  4445 Sigma Road
  Phone: (214) 661-8661
- **Houston 77036:**
  Component Specialties
  7313 Ashcroft, Suite 202
  Phone: (713) 771-7237
- **Houston 77019:**
  Hamilton/Avnet Electronics
  1216 West Clay Street
  Phone: (713) 526-4661

UTAH

- **Salt Lake City 84115:**
  Alta Electronics
  2280 S. Main St.
  Phone: (801) 486-7227
- **Salt Lake City 84119:**
  Hamilton/Avnet Electronics
  647 West Billinis Road
  Phone: (801) 262-8451

WASHINGTON

- **Bellevue 98005:**
  Hamilton/Avnet Electronics
  13407 Northrup Way
  Phone: (206) 746-8750
- **Seattle 98108:**
  Cramer Electronics
  5602 6th Avenue, South
  Phone: (206) 762-5725

INTERNATIONAL SALES

EUROPEAN HEADQUARTERS

Signetics International Corp.
Yeoman House, 63 Croydon Road
Penge, London, S.E. 20, England
Phone: (01) 659-2111

FRANCE

Signetics S.A.R.L.
36 Rue de Silly
F92100 Boulogne
Phone: 604-23-07

WEST GERMANY

Signetics GmbH
Dantestr. 29
D 8 München 19
Phone: (0811) 151029/151020

Signetics GmbH
Ernsthaldenstrasse 17
D 7 Stuttgart 80
Phone: (0711) 73-50-61

Signetics GmbH
Eulenkrugstr. 81 E
D 2 Hamburg 67
Phone: (0411) 60-35-242

STOCKING DISTRIBUTORS

AFRICA

Allied Electronic (PTY) Ltd.
P.O. Box 6090
Dunswart, Transvaal, South Africa
Phone: 52431

AUSTRALIA

Tecnico Electronics
Premier St.
Marrickville, N.S.W. 2204
Phone: 550 411

Tecnico Electronics
2 High St. Northcote
Melbourne, Vic. 3070
Phone: 489-9322

AUSTRIA

Ing. Ernst Steiner
Beckgasse 30
A-1130 Wien
Phone: (222) 82-10-605

BELGIUM

Klaasing Benelux S.A.
Avenue de L'Universite 93
1050 Bruxelles
Phone: (02) 49-85-32

BRAZIL

Teleimport Electronica Ltd.
Rua Sta. Ifigenia 402-8° A 10° and
01207 Sao Paulo
Phone: 221-3296

CANADA

- **Downsview M3G-2K9, Ontario:**
  Cesco Electronics
  24 Martin Ross Avenue
  Phone: (416) 661-0220
- **Downsview, Ontario:**
  Cramer Electronics
  920 Alness Ave.
  Unit 9
  Phone: (416) 661-9222
- **Mississauga, Ontario L4V1H2:**
  Hamilton/Avnet Electronics
  6291 Dorman Rd., Unit 16
- **Montreal, Quebec:**
  Cesco Electronics
  4050 Jean Talon West
  Phone: (514) 735-5511
- **Montreal H4T-1R2, Quebec:**
  Hamilton/Avnet Electronics
  935 Montee des Liesses
  Phone: (514) 331-6443
- **Ottawa K1Z-5L9, Ontario:**
  Cesco Electronics
  1300 Carling Avenue
  Phone: (613) 729-5118

- **Ottawa, Ontario:**
  Hamilton/Avnet Electronics
  880 Lady Ellen Place
  Phone: (613) 725-3071
- **Quebec City:**
  Cesco Electronics
  128 St. Vallier St.
  Phone: (418) 524-3518
- **Vancouver, B.C.:**
  Bowtek Electric Co. Ltd.
  993 West 8th Avenue
  Phone: (604) 736-7677

DENMARK

E. Friis-Mikkelsen A/S
Krogshojvej 51
DK-2880 Bagsvaerd
Phone: (01) 986333

FRANCE

Elic 38, Grenoble
8 Av. du Grand Sablon
38700 La Tronche
Phone: (76) 87-67-71

Elic 38, Lyon
156, Av. Gabriel Peri
69120 Vaube en Velin
Phone: (78) 84-38-01

REA-D
57 Rue Henry Litolff
92 Bois Colombes
Phone: 242-5397

R.T.F.
73 Avenue Charles de Gaulle
92-Neuilly
Phone: 722-70-40

HONG KONG

Astec Components Ltd.
2nd Floor, Keystone House
6 Hankow Road
Kowloon
Phone: 687-760

ISRAEL

RAPAC Electronics Ltd.
15, Karl Herbst St.
P.O. Box 18053
Tel-Baruch
Tel-Aviv
Phone: 477 115

ITALY

Metroelettronica S.A.S.
Viale Cirene 18
1-20135 Milano
Phone: 546-26-41

JAPAN

Asahi Glass Co., Ltd.
1-2 Marunouchi, 2 Chome
Chiyoda-ku, Tokyo
Phone: 218-5536

NORWAY

A. S. Kjell Bakke
Kjellergt 11
Lillestrom 2000
Phone 71 18 72/71 53 30

SINGAPORE/MALAYSIA

General Engineers Corp. Pte. Ltd.
37 Hill Street
Singapore 1
Phone: 71 042

SPAIN

Ataio Ingenieros, S.A.
Enrique Larreta, 10Y12
Madrid 16
Phone: 215/35/43

SWEDEN, FINLAND

A. B. Kuno Källman
Folkungagatan 16-18
411 02 Gothenburg, Sweden
Phone: 010 46 31 80 30 20

A. B. Kuno Källman
Sibyllegatan 28, 11443
Stockholm, Sweden
Phone: 08/671711-671595

SWITZERLAND

Omni Ray AG
Dufourstrasse 56
8008 Zurich
Phone: 01/478200

TAIWAN R.O.C.

Dynatek Corp.
92, 3rd Floor, Jen-Ai Rd.
Section 3, Taipei 106
Phone: 713-362

THAILAND/LAOS

Saeng Thong Radio L.P.
199/5 Phayathai Road
Pathumwan Circle
Bangkok 5, Thailand
Phone: 57395

THE NETHERLANDS

Mulder-Hardenberg
Westerhoutpark 1-A
P.O. Box 3059, Haarlem
Phone: (023) 3191 84

UNITED KINGDOM

Quarndon Electronics Ltd.
Slack Lane
Derby, Derbyshire
Phone: Derby 3 26 51

S.D.S. (Components) Ltd.
Hilsea Industrial Estate
Portsmouth, Hampshire
Phone: 6 53 11

Semicomps Ltd.
5 Northfield Industrial Estate
Beresford Ave.
Wembley, Middlesex
Phone: (01) 903-3161

A. M. Lock & Co. Ltd.
Neville Street, Middleton Road
Oldham, Lancashire
Phone: (061) 624-6832

Semicomps Northern Ltd.
42 The Square
Kelso, Roxburghshire
Phone: Kelso 2366

WEST GERMANY

EBV Elektronik GmbH.
Augustenstrasse 79
D 8 München 2
Phone: (0811) 52-43-40/48

EBV Elektronik GmbH.
Myliusstrasse 54
D 6 Frankfurt/Main 1
Phone: (0611) 72-04-16/18

EBV Elektronik GmbH.
Scheurenstrasse 1
D 4 Düesseldorf
Phone: (0211) 8-48-46/47

Mirotronic
2 Hamburg 54, Ahornllee 5
Phone: (0411) 560-40-54

EBV Elektronik GmbH
Abraham-Wolf Strasse 48
D 7 Stuttgart-Sonnenberg
Phone: (0711) 765072/3

"Mütron" Muller & Co. KG
Postfach 164, Bornstrasse 22
D 28 Bremen 1
Phone: (0421) 31-04-85

Omni-Ray GmbH
67 Ludwigshafen, Moltkestrasse
8 Postfach 211023
Phone: (0621) 51-30-55/56

Distron GmbH
D 1 Berlin 31, Wilhelmsaue 39-41
Phone: (0311) 82-13-064

REPRESENTATIVES

ARGENTINA

Electronica del Atlantico SRL
C. Pellegrini 143, Of. 37
Buenos Aires
Phone: 35-2624

AUSTRALIA

Tecnico Electronics
Premier St.
Marrickville, N.S.W. 2204
Phone: 550 411

Tecnico Electronics
2 High St., Northcote
Melbourne, Vic. 3070
Phone: 489-9322

BRAZIL

Teleimport Electronica Ltd.
Rua Sta. Ifigenia 402-8° A 10° and
01207 Sao Paulo
Phone: 221-3296

CANADA

- **Downsview (Toronto), Ontario:**
  Kaytronics Limited
  1001 Finch Ave.
  Phone: (416) 638-5511
- **Montreal, Quebec:**
  Kaytronics Limited
  7370 Cote St. Luc Road
  Phone: (514) 487-3434

HONG KONG

Astec Components Ltd.
2nd Floor, Keystone House
6 Hankow Road
Kowloon
Phone: 687 760

INDIA

Semiconductors Limited
5th Floor, Radia House
6 Rampart Row
Fort Bombay 1
Phone: 293 667

ISRAEL

RAPAC Electronics Ltd.
15, Karl Herbst Street
P.O. Box 18053
Tel Baruch
Tel-Aviv
Phone: 477 115

JAPAN

Asahi Glass Co. Ltd.
1-2, Marunouchi, 2 Chome
Chiyoda-ku, Tokyo
Phone: 218-5536

NORWAY

A. S. Kjell Bakke
Kjellergt 11
Lillestrom 2000
Phone: 71 18 72/71 53 30

TAIWAN R.O.C.

Dynatek Corporation
92, 3rd Floor, Jen-Ai Road
Section 3, Taipei 106
Phone: 713-362

SWEDEN, FINLAND

A. B. Kuno Källman
Folkungagatan 16-18
411 02 Gothenburg, Sweden
Phone: 031-803020

A. B. Kuno Källman
Sibyllegatan 28, 11443
Stockholm, Sweden
Phone: 08/671711-671595

SWITZERLAND

Omni Ray AG
Dufourstrasse 56, 8008 Zurich
Phone: 01/478200

SINGAPORE/MALAYSIA

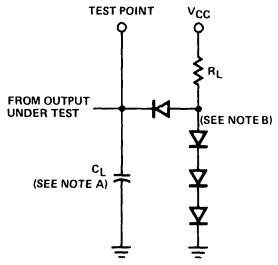
General Engineers Corp. Pte. Ltd.
37 Hill Street
Singapore 1
Phone: 71 042

THAILAND/LAOS

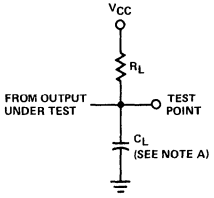
Saeng Thong Radio L.P.
1995 Phayathai Road
Pathumwan Circle
Bangkok 5, Thailand
Phone: 57395

TEST CIRCUITS

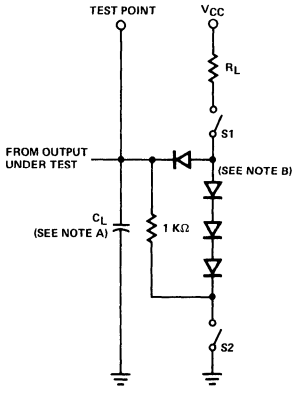
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



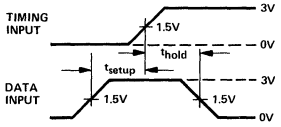
NOTES

A. C_L includes probe and jig capacitance.

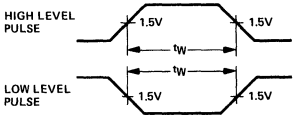
B. All diodes are 1N916 or 1N3064.

WAVEFORMS

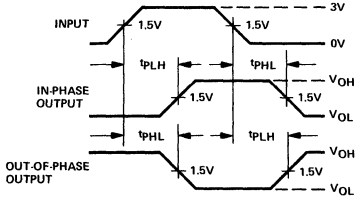
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



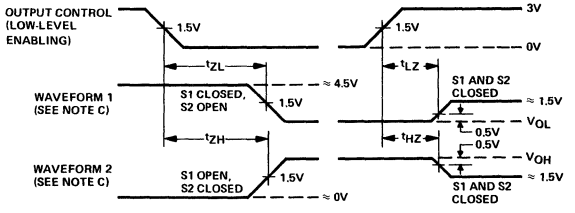
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\Omega$ and:

For Series 54/74, $t_r \leq 7$ ns, $t_f \leq 7$ ns;

For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

DESCRIPTION

These positive NOR buffers are functionally identical to the 5402 and 7402 but are designed to drive highly capacitive loads with significantly improved dynamic performance. The devices are directly applicable for use as clock drivers where the distributed capacitive load is relatively large. In systems where "clock skew" must be considered, these devices can simplify clock distribution.

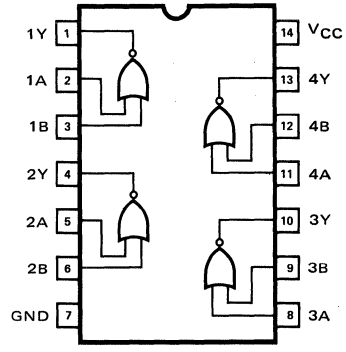
The 5428 and 7428 can drive up to 60 loads at high logic level or 30 loads at low logic level and still maintain a 7-nanosecond typical propagation delay. The 54128 will drive 75-ohm and 50-ohm lines, respectively, and in addition will simultaneously drive 60 loads at a high logic level or 30 loads at a low logic level.

These buffers are completely compatible with most TTL and DTL logic families. Typical average power dissipation is 112 milliwatts.

The 5428, 5433 and 54128 devices are characterized for operation over the full military temperature range of −55°C to 125°C; the 7428 and 74128 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATION (Top View)

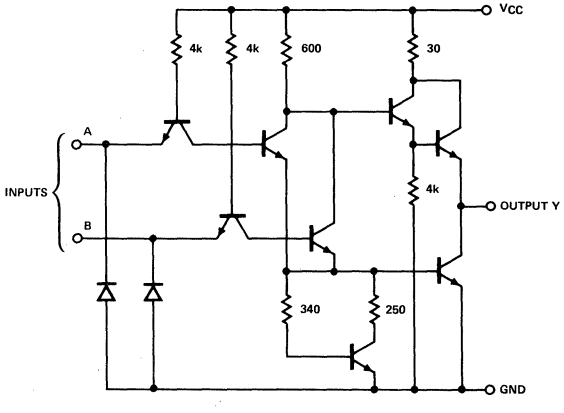
A,F,W PACKAGE



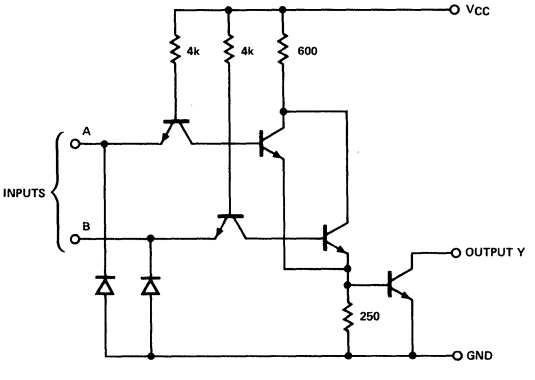
positive logic: $Y = \overline{A + B}$

SCHEMATIC (Each Buffer)

5428, 7428, 54128, 74128 (TOTEM POLE OUTPUT)



5433, 7533 (OPEN COLLECTOR OUTPUT)



Resistor values are nominal in ohms.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		5428			7428			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N Normalized fan-out from each output	High logic level			60			60	
	Low logic level			30			30	
T_A Operating free-air temperature		-55		125	0		70	°C

PARAMETER	5433			7433			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{OH} High-level output voltage			5.5			5.5	V
I_{OL} Low-level output current			48			48	mA
T_A Operating free-air temperature	-55		125	0		70	°C

PARAMETER	54128			74128			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
N Normalized fan-out from each output at low logic level			30			30	
I_{OH} High-level output current			-29			-42.4	mA
T_A Operating free-air temperature	-55		125	0		70	C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]	5428, 7428			5433, 7433			54128, 74128			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage		2			2			2			V
V_{IL}	Low-level input voltage				0.8			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -12mA			-1.5			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.8V, I_{OH} = -2.4mA	2.4	3.3								V
		V_{CC} = MIN, V_I = 0.4V, I_{OH} = -13.2mA							2.4			
		V_{CC} = MIN, V_I = 0.4V, I_{OH} = MAX							2			
I_{OH}	High-level output current	V_{CC} = MIN, V_I = 2V						250				μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2V, I_{OL} = 48mA		0.26	0.4			0.4		0.26	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6			-1.6			-1.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX	-70		-180				-70		-180	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, See Note 3		12	21		1.8	3.6		12	21	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 4		33	57		6.9	13.8		33	57	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[2] All typical values are at V_{CC} = 5V, T_A = 25°C.

[3] Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

NOTES: 3. I_{CCH} is measured with all inputs grounded and outputs open.
4. I_{CCL} is measured with one input of each gate at 5V, the remaining inputs grounded, and outputs open.

Load circuit and typical waveforms are shown at front of this section.

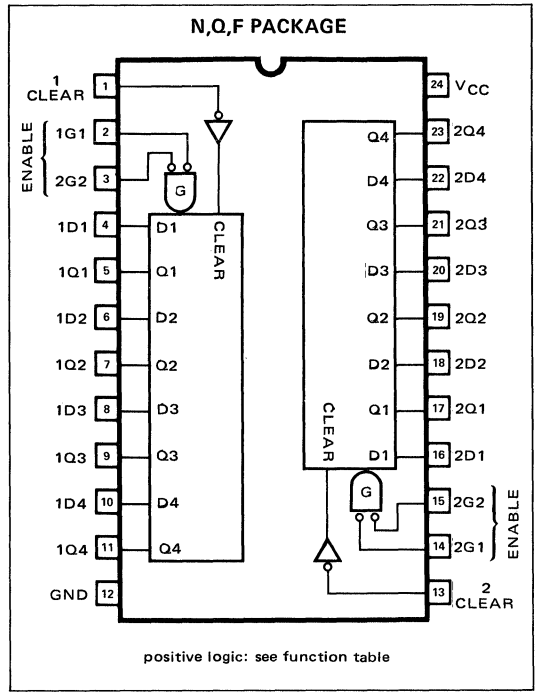
DESCRIPTION

These monolithic TTL circuits utilize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

The S54116 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74116 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION (Top View)



FEATURES

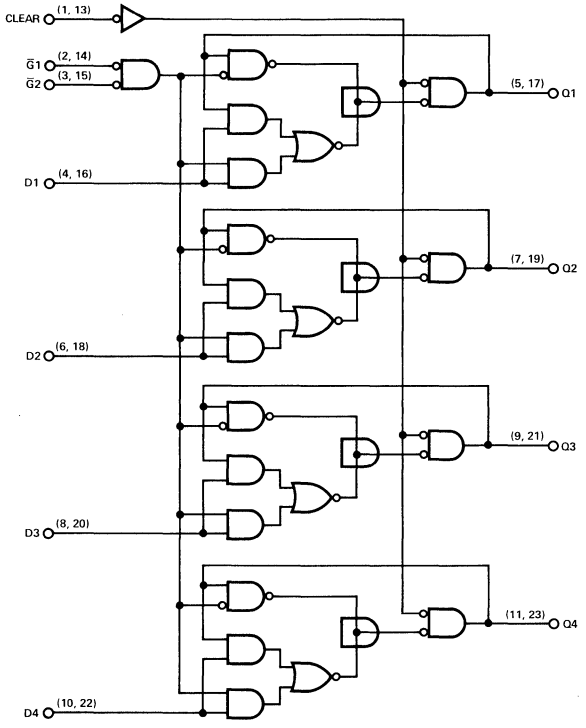
- TWO INDEPENDENT 4-BIT LATCHES IN A SINGLE PACKAGE
- SEPARATE CLEAR INPUTS PROVIDE ONE-STEP CLEARING OPERATION
- DUAL GATED ENABLE INPUTS SIMPLIFY CASCADING AND REGISTER IMPLEMENTATION
- COMPATIBLE FOR USE WITH TTL AND DTL CIRCUITS
- INPUT CLAMPING DIODES SIMPLIFY SYSTEM DESIGN

FUNCTION TABLE (Each Latch)

INPUTS				OUTPUT
CLEAR	ENABLE $\overline{G1}$	ENABLE $\overline{G2}$	DATA	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before these input conditions were established.

FUNCTIONAL BLOCK DIAGRAM (Each 4-bit Latch)



RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54116			N74116			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				-800			-800	μA
I_{OL}	Low-level output current				16			16	mA
t_w	Input pulse width	Enable	18			18			ns
		Clear	18			18			
t_{setup}	Data setup time	High logic level	8			8			ns
		Low logic level	14			14			
t_{setup}	Clear inactive-state setup time		8			8			ns
$t_{release}$	Data release time, high-level data				2			2	ns
t_{hold}	Data hold time, low-level data		8			8			
T_A	Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −800μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX,	V_I = 2.4V			40	μA
		Any D					60	
I_{IL}	Low-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX,	V_I = 0.4V			−1.6	mA
		Any D, initial peak					−2.4	
		Any D, steady-state					−1.6	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	S54116	−20		−57	mA
				N74116	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition A		60	100	mA
				Condition B		40	70	

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.
NOTE 2: With outputs open, I_{CC} is measured for the following conditions:
A. All inputs grounded.
B. All $\overline{G}$ inputs are grounded and all other inputs are at 4.5V.

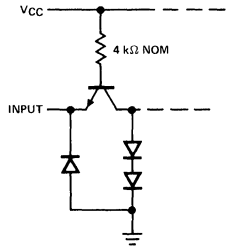
SWITCHING CHARACTERISTICS, (V_{CC} = 5V, T_A = 25°C)

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any Q	C_L = 15 pF, R_L = 400 Ω		19	30	ns
t_{PHL}					15	22	
t_{PLH}	Data	Q			10	15	ns
t_{PHL}					12	18	
t_{PHL}	Clear	Any Q			15	22	ns

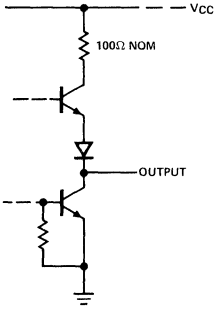
[1] t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

TEST CIRCUITS

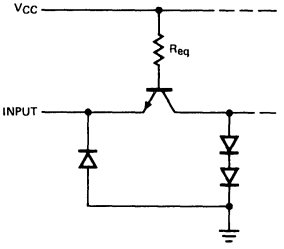
EQUIVALENT OF CLEAR, $\overline{G}1$, AND $\overline{G}2$ INPUTS



EQUIVALENT OF DATA INPUTS



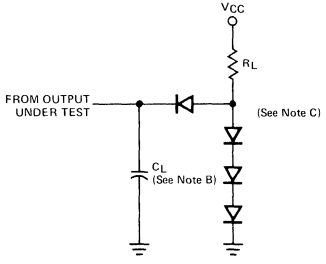
TYPICAL OF ALL OUTPUTS



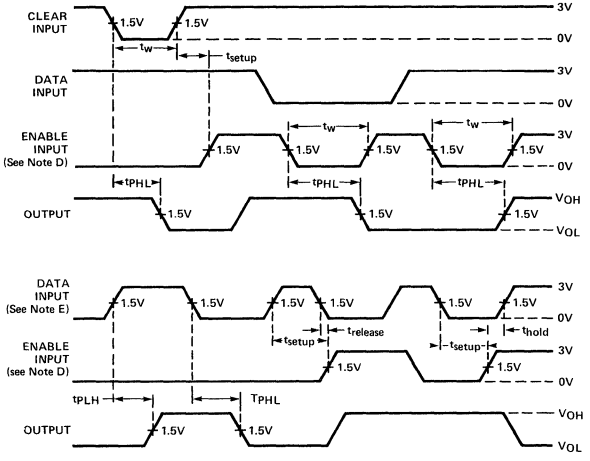
Initial R_{eq} = 3 kΩ NOM
Steady-state R_{eq} = 6 kΩ NOM

SWITCHING PARAMETER MEASUREMENT INFORMATION Figure 1

LOAD CIRCUIT



SWITCHING TIMES FROM DATA INPUTS



NOTES

A. Input pulses are supplied by generators having the following characteristics: $t_r \leq 10$ns, $t_f \leq 10$ns, PRR = 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. The other enable input is low.
E. Clear input is high.

signetics

10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

S54147/148-B,F,W • N74147/148-B,F

DIGITAL 54/74 TTL SERIES

S54147
N74147
S54148
N74148

DESCRIPTION

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 54147 and 74147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All inputs are buffered to represent one normalized Series 54/74 load. The 54148 and 74148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

FUNCTION TABLE (54147, 74147)

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

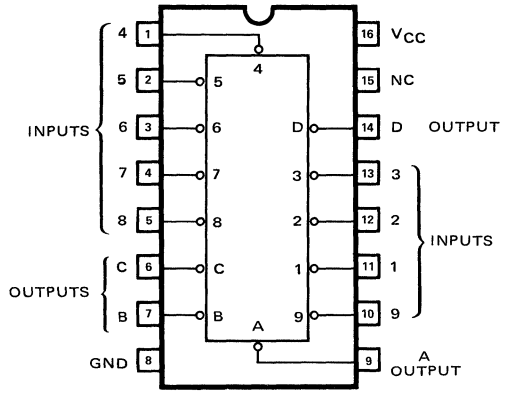
FUNCTION TABLE (54148, 74148)

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

PIN CONFIGURATION (Top View)

B,F,W PACKAGE

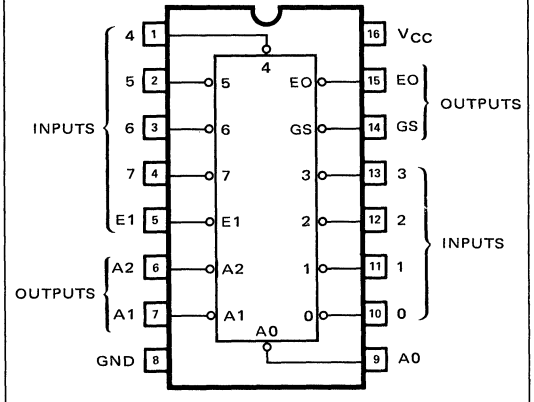
S54/N74147



positive logic: see functions table

NC—No internal connection

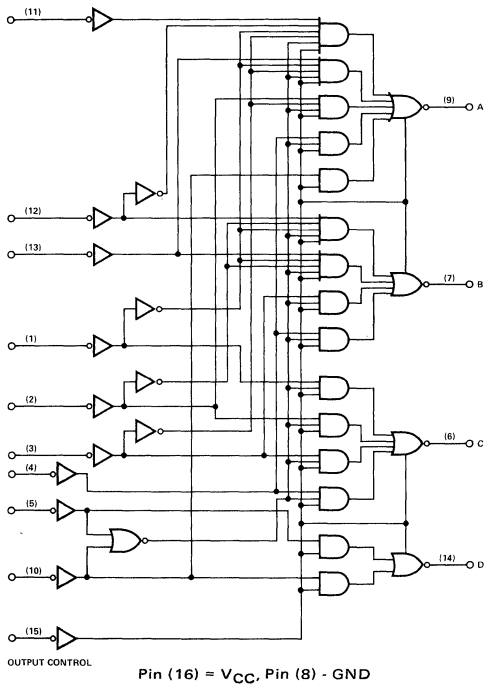
S54/N74148



positive logic: see function table

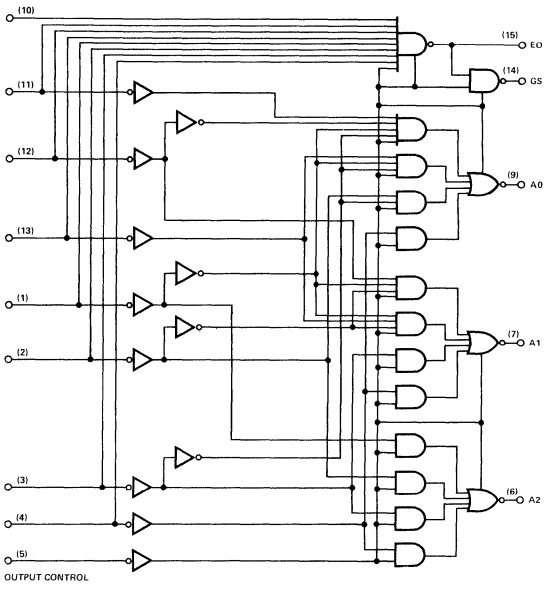
FUNCTIONAL BLOCK DIAGRAMS

54147, 74147



Pin (16) = V_{CC}, Pin (8) - GND
Pin (15) = No connection

54148, 74148



Pin (16) = V_{CC}, Pin (8) = GND

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		54147, 54148			74147, 74148			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from any output	High logic level			20			20	
		Low logic level			10			10	
T_A	Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE

(Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS[1]		54147 74147			54148 74148			UNIT
					MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = -12 mA			-1.5			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = -800 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	0 input	V_{CC} = MAX,	V_I = 2.4 V						40	μA
		Any input except 0					40			80	
I_{IL}	Low-level input current	0 input	V_{CC} = MAX,	V_I = 0.4 V						-1.6	mA
		Any input except 0					-1.6			-3.2	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-35		-85	-35		-85	mA
I_{CC}	Supply current		V_{CC} = MAX,	Condition 1		50	70		40	60	mA
			See Note 4	Condition 2		42	62		35	55	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. All typical values are at V_{CC} = 5 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. For 54147, 74147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For 54148, 74148, I_{CC} (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open, I_{CC} (condition 2) is measured with all inputs and outputs open.

S54147, N74147 SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase	C_L = 15 pF, P_L = 400 Ω		9	14	ns
t_{PHL}			output			7	11	
t_{PLH}	Any	Any	Out-of-phase			13	19	ns
t_{PHL}			output			10	15	

S54148, S74148 SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	0 thru 7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 400 Ω		10	15	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	A0, A1, or A2	Out-of-phase output			13	19	ns
t_{PHL}						10	15	
t_{PLH}	0 thru 7	EO	Out-of-phase output			6	10	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	GS	In-phase output			14	21	ns
t_{PHL}						12	18	
t_{PLH}	EI	A0, A1, or A2	In-phase output			10	15	ns
t_{PHL}						10	15	
t_{PLH}	EI	GS	In-phase output			8	12	ns
t_{PHL}						10	15	
t_{PLH}	EI	EO	In-phase output			8	13	ns
t_{PHL}						13	19	

t_{PLH} ≡ propagation delay time, low-to-high level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuits and waveforms are shown on page 143.

Load circuits and typical waveforms are shown at the front of this section.

DESCRIPTION

These high-speed monolithic counters consist of four DC coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter or a divide-by-two and a divide-by-eight counter. These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

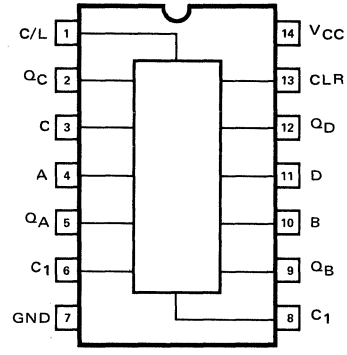
During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

FEATURES

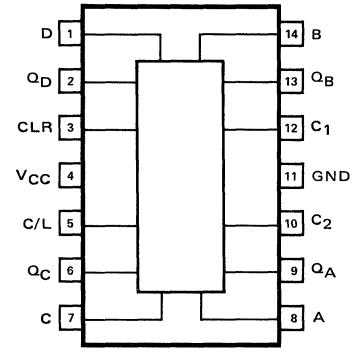
- DC COUPLED
- NEGATIVE EDGE-TRIGGERED CLOCKING
- PRE-SETTABLE

PIN CONFIGURATIONS (Top View)

A,F PACKAGES



W PACKAGE



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-Air Temperature Range Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SEE 8280, 8281, 8290, 8291 Data Sheet for Pin-for-Pin Replacement				

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

These shift registers utilize fully DC coupled storage elements and feature synchronous parallel inputs and parallel outputs. The S54179/N74179 has a direct clear line and complementary output from the D flip-flop, thereby differing from the S54178/N74178.

Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is inhibited.

Shift right is also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input.

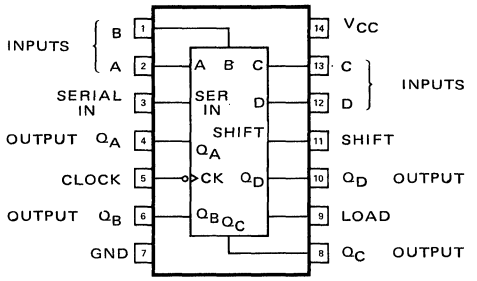
When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register.

FEATURES

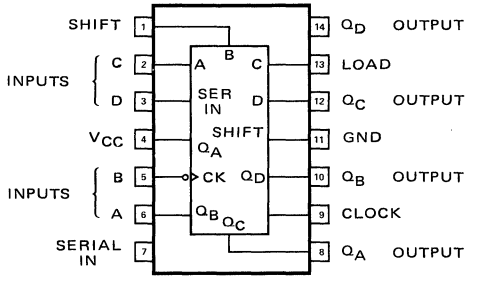
- THREE OPERATING MODES:
  - SYNCHRONOUS PARALLEL LOAD
  - RIGHT SHIFT
  - HOLD (DO NOTHING)
- NEGATIVE-EDGE-TRIGGERED CLOCKING
- DC COUPLING SIMPLIFIES SYSTEM DESIGNS

PIN CONFIGURATION (Top View)

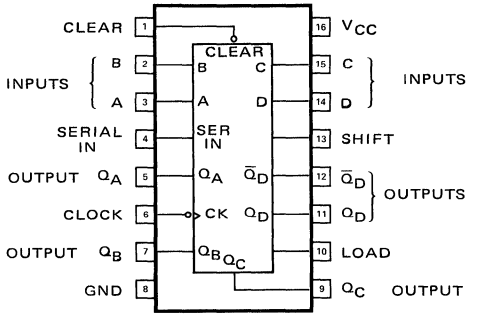
A,F PACKAGES (S54178, N74178)



W PACKAGE (S54178)



B,F,W PACKAGES (S54179, N74179)



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	See 8270, 8271 Data Sheet for Pin-for-Pin Replacement				

Load circuits and typical waveforms are shown at the front of this section.

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT TRIGGER INPUTS

S54221
N74221

S54221-B,F,W • N74221B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54221 and N74221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the S54121 and N74121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to 28 seconds by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, an output pulse of typically 30 nanoseconds is achieved which may be used as a DC triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

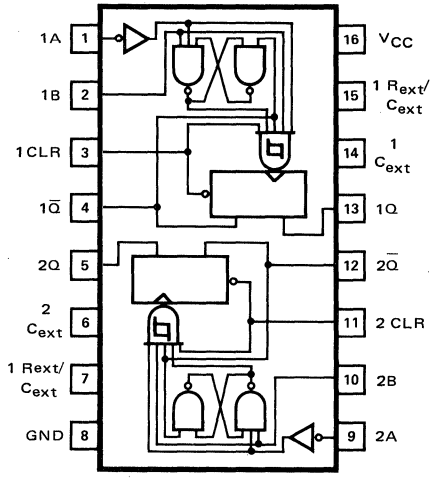
Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 30kΩ for the S54221 and 2kΩ to 40kΩ for the N74221). Throughout these ranges, pulse width is defined by the relationship: $t_{W(out)} = C_{ext}R_{ext} \ln 2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components. An example of this distribution is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature are shown in Figures 3 and 4, respectively.

Pin assignments for these devices are identical to those of the S54123 or N74123 so that the S54221 or N74221 can be substituted for the S54123 or N74123 in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

PIN CONFIGURATION (Top View)

B,F,W PACKAGE

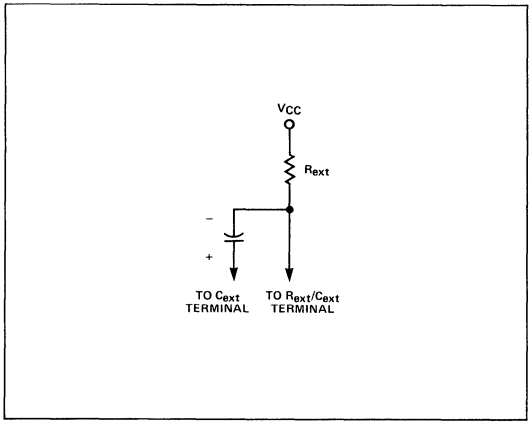


positive logic: Low input to clear reset Q low and Q high regardless of d-c levels at A or B input.

FEATURES

- DUAL VERSION OF HIGHLY STABLE S54121, N74121 ONE-SHOT ON A MONOLITHIC CHIP
- PULSE-WIDTH VARIANCE IS TYPICALLY LESS THAN ±0.5% FOR 98% OF THE UNITS
- DEMONSTRATES ELECTRICAL AND SWITCHING CHARACTERISTICS THAT ARE VIRTUALLY IDENTICAL TO THE S54121, N74121 ONE-SHOT
- PIN-OUT IS IDENTICAL TO THE S54123, N74123
- OVERRIDING CLEAR TERMINATES OUTPUT PULSE

TIMING COMPONENT CONNECTIONS



FUNCTION TABLE (Each Monostable)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

Also see description and switching characteristics

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high-level pulse
⎎ = one low level pulse
X = irrelevant

RECOMMENDED OPERATING CONDITIONS

PARAMETER		S54221			N74221			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current				-800			-800	μA
I_{OL} Low-level output current				16			16	mA
dv/dt Rate of rise or fall of input pulse	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			
t_{setup} Clear-inactive-state setup time		15			15			ns
R_{ext} External timing resistance		1.4		30	1.4		40	kΩ
C_{ext} External timing capacitance		0		1000	0		1000	μF
Output duty cycle	R_{ext} = 2kΩ			67			67	%
	R_{ext} = MAX R_{ext}			90			90	
T_A Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = MAX		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V	Input A			40	μA
			Input B, Clear			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V	Input A			−1.6	mA
			Input B, Clear			−3.2	
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	S54221	−20		−55	mA
			N74221	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15pF, R_L = 400Ω, See Figure 1	C_{ext} = 80pF, R_{ext} = 2kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	$\overline{Q}$					40	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80pF, R_{ext} = 2kΩ	70	110	150	ns
				C_{ext} = 0, R_{ext} = 2kΩ	20	30	50	
				C_{ext} = 100pF, R_{ext} = 10kΩ	650	700	750	
				C_{ext} = 1μF, R_{ext} = 10kΩ	6.5	7	7.5	ms

[1] t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

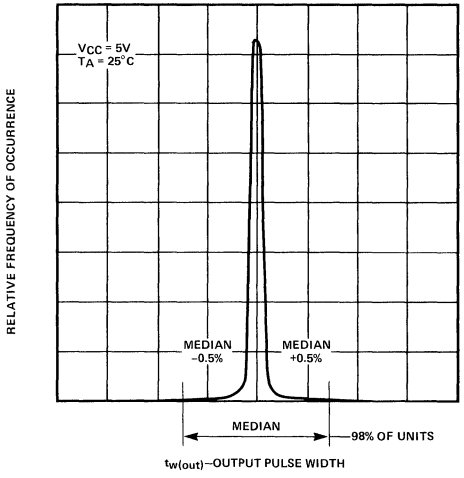


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH VS SUPPLY VOLTAGE

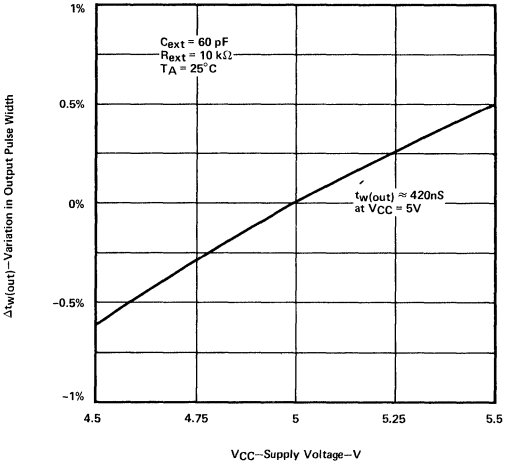


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH VS FREE-AIR TEMPERATURE

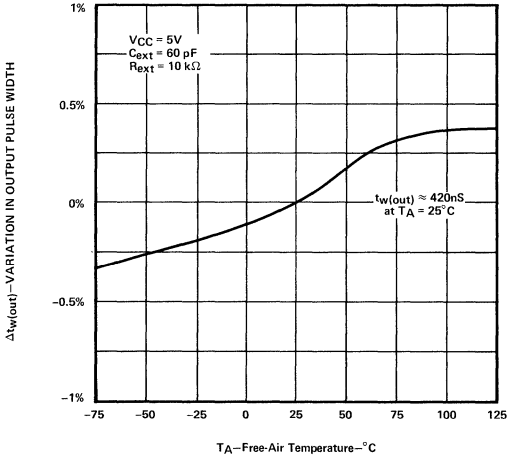


FIGURE 4

OUTPUT PULSE WIDTH VS TIMING RESISTOR VALUE

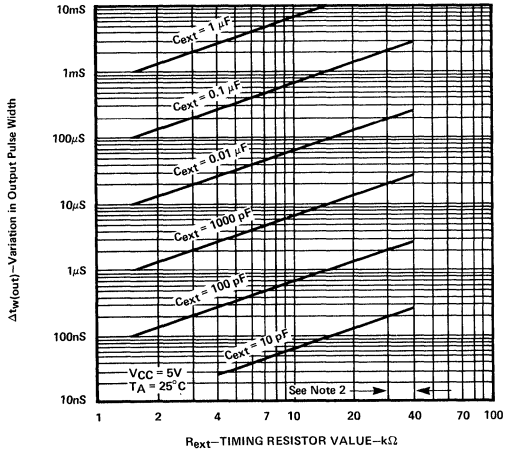
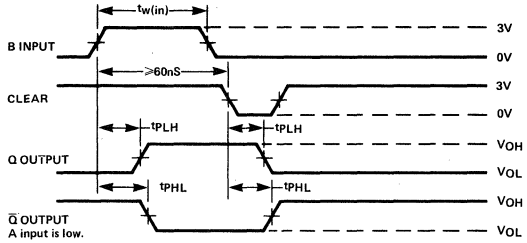


FIGURE 5

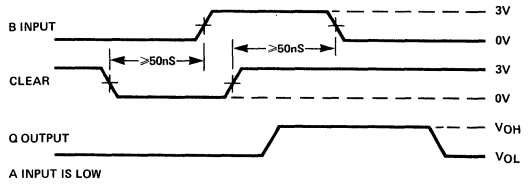
NOTE 2: These values of resistance exceed the maximum recommended for use over the full temperature range of the S54221.

† Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75V and above 5.25V are applicable for the S54221 only.

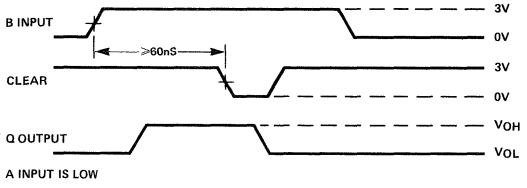
FIGURE 1—SWITCHING PARAMETER MEASUREMENT INFORMATION



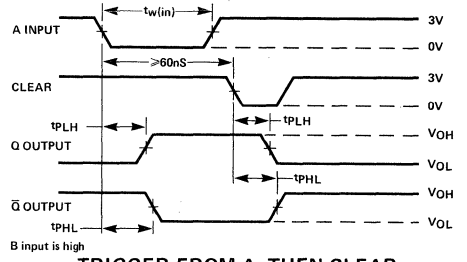
TRIGGER FROM B, THEN CLEAR—CONDITION 1



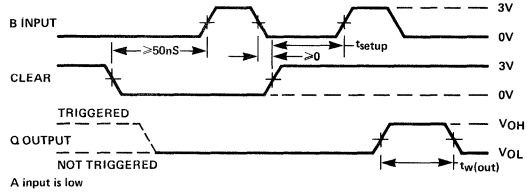
TRIGGERING FROM POSITIVE TRANSITION OF CLEAR



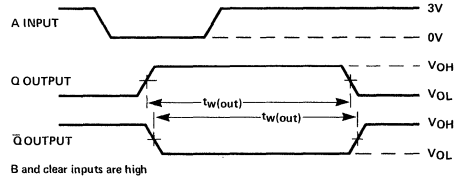
TRIGGER FROM B, THEN CLEAR—CONDITION 2



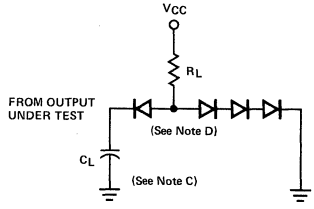
TRIGGER FROM A, THEN CLEAR



CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGER FROM A



LOAD CIRCUIT

NOTES

A. Input pulses are supplied by generators having the following characteristics: $t_r \leq 7$ nS, $t_f \leq 7$ nS, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.
B. All measurements are made between the 1.5V points of the indicated transitions.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

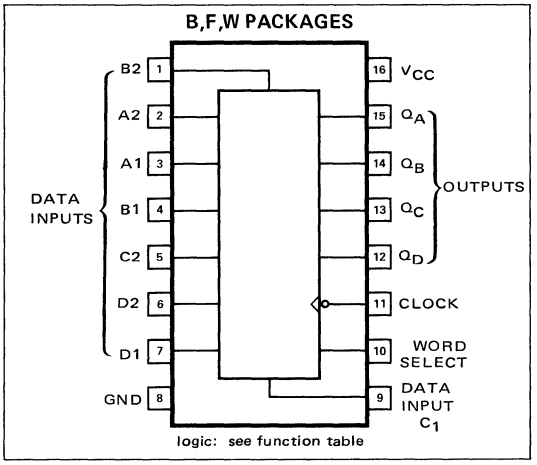
DESCRIPTION

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions 54157/74157 and 54175/74175 in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 195 milliwatts. The 54298 is characterized for operation over the full military temperature range of −55°C to 125°C; the 74298 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION (Top View)

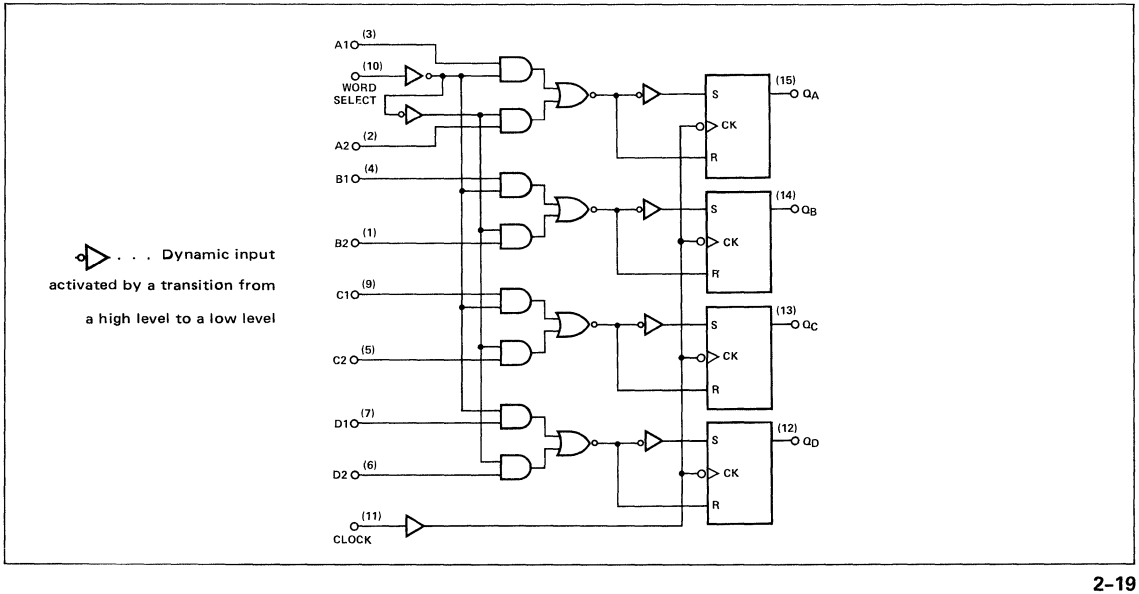


FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
A1, A2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the last ↓ transition of the clock input.

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER		54298			74298			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N Normalized fan-out from each output	High logic level			20			20	
	Low logic level			10			10	
t_w Width of clock pulse, high or low level		20			20			ns
t_{setup} Setup time	Data	15			15			ns
	Word select	25			25			
t_{hold} Hold time	Data	5			5			ns
	Word select	0			0			
T_A Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = -800 μA	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 16mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	54298	-20		-57	mA
			74298	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		39	65	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5V, followed by ground, to the clock input.

SWITCHING CHARACTERISTICS, (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			21	32	

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

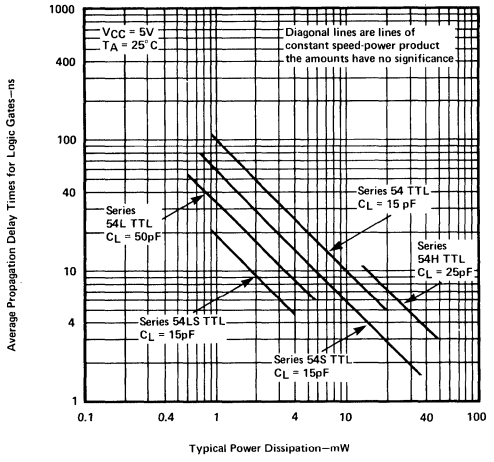
The Series 54LS/74LS Schottky TTL family features both Schottky-barrier-diode inputs and emitter inputs and utilizes full Schottky-barrier-diode clamping to achieve speeds comparable to Series 54/74 at one-fifth of the power. They retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54LS/74LS circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54S/74S TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the speed-power ranges offered (Series 54/74, 54H/74H, 54LS/74LS, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

Definitive specifications are provided for operating characteristics over the full military temperatures range of −55°C to 125°C for Series 54LS circuits and over the temperature range of 0°C to 70°C for Series 74LS circuits.

SPEED-POWER RELATIONSHIPS
OF DIGITAL IC FAMILIES‡



‡Typical saturated logic gate from the indicated families.

FEATURES

LOW-POWER, HIGH-SPEED OPERATION
- 9.5ns TYPICAL GATE PROPAGATION DELAY TIME
- 2mW PER-GATE POWER DISSIPATION AT 50% DUTY CYCLE – SPEED-POWER PRODUCT = 19pJ TYP.
- 45MHz TYPICAL J-K FLIP-FLOP MAXIMUM CLOCK FREQUENCY (DC COUPLED)

EASE OF SYSTEM DESIGN
- FULLY COMPATIBLE WITH SERIES 54/74, 54H/74H AND 54S/74S TTL (INCLUDING MSI/LSI), AND MOST DTL
- SCHOTTKY-DIODE CLAMPED INPUTS SIMPLIFY SYSTEM DESIGN
- TERMINATED, CONTROLLED-IMPEDANCE LINES NOT NORMALLY REQUIRED
- LOW OUTPUT IMPEDANCE: PROVIDES LOW AC NOISE SUSCEPTABILITY – DRIVES HIGHLY CAPACITIVE LOADS

IMPROVED CIRCUIT PERFORMANCE
- SWITCHING TIMES VIRTUALLY INSENSITIVE TO POWER SUPPLY AND/OR TEMPERATURE VARIATIONS
- POWER DISSIPATION REMAINS RELATIVELY LOW AT OPERATING FREQUENCIES UP TO 30MHz
- HIGH FAN-OUT:
  - 20 54LS/74LS LOADS (OR 10 54/74 LOADS) AT THE HIGH LOGIC LEVEL
  - 10 54LS/74LS LOADS (OR 2.5 54/74 LOADS) AT THE LOW LOGIC LEVEL
  - 20 54LS/74LS LOADS (OR 5 54/74 LOADS) AT THE LOW LOGIC LEVEL OVER THE 0°C TO 70°C TEMPERATURE RANGE

UNUSED INPUTS OF POSITIVE-AND/NAND GATES

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the

floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7V and 3.5V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

c. Connect unused inputs to V_{CC} through a 1kΩ resistor so that if a transient which exceeds the 5.5V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1kΩ resistor.

d. Connect unused inputs to the output of an inverter that has its input grounded.

INPUT-CURRENT REQUIREMENTS

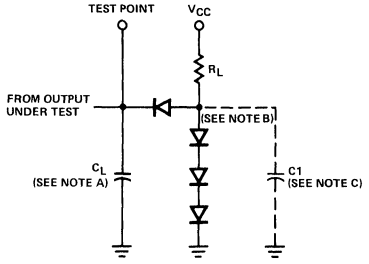
Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 0.36mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 20μA maximum for each emitter. Currents into the input terminals are specified as positive values.

FAN-OUT CAPABILITY

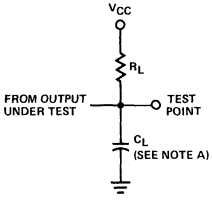
Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54LS or 74LS loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard Series 54LS output is capable of sinking current from 10 Series 54LS loads (N_L = 10) over the full operating free-air temperature range of −55°C to 125°C, and each standard Series 74LS output is capable of sinking current from 20 Series 74LS loads (N_L = 20) over the operating free-air temperature range of 0°C to 70°C.

TEST CIRCUITS

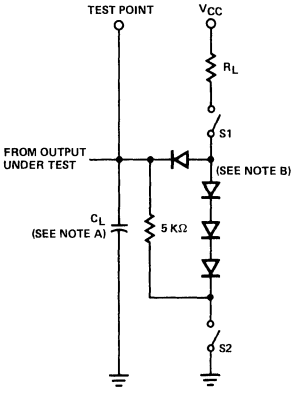
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



NOTES

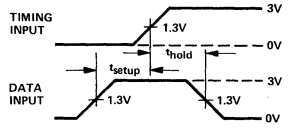
A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

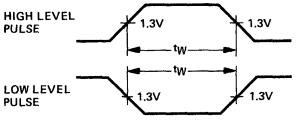
C. C1 (30 pF) is used for testing Series 54L/74L devices only.

WAVEFORMS

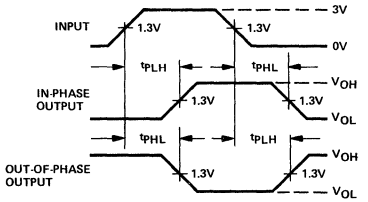
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



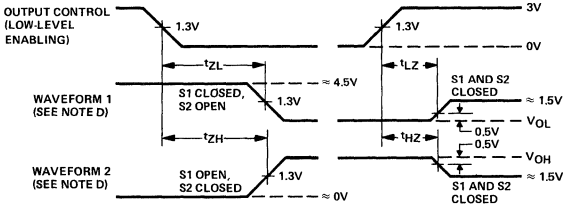
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phrase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\Omega$ and $t_r \leq 15$ ns, $t_f \leq 6$ ns.

signetics

LOW POWER SCHOTTKY POSITIVE NAND GATES HEX INVERTERS

S54LS-A,F,W • N74LS-A,F

DIGITAL 54/74 TTL SERIES

S54LS00 N74LS00
S54LS04 N74LS04
S54LS10 N74LS10
S54LS20 N74LS20
S54LS30 N74LS30

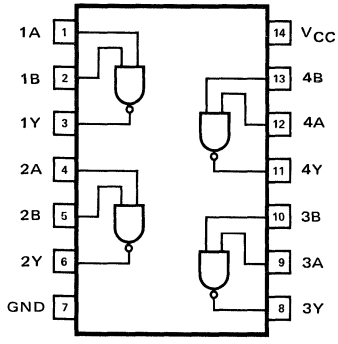
FEATURES

- TYPICAL PROPAGATION TIME – 25ns @ C_L = 15pF
- TYPICAL POWER DISSIPATION – 2mW PER GATE @ 50% DUTY CYCLE
- LOGICALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 EQUIVALENTS

PIN CONFIGURATION (Top View)

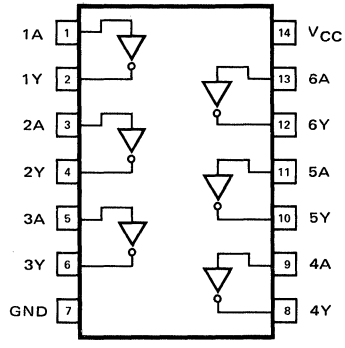
A,F,W PACKAGE

S54LS00, N74LS00
QUADRUPLE 2-INPUT NAND GATES



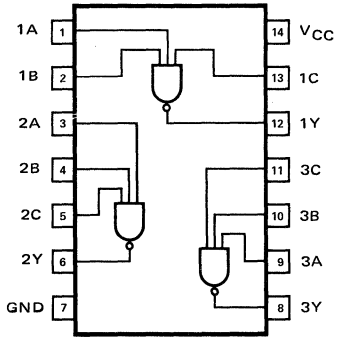
positive logic: $Y = \overline{AB}$

S54LS04, N74LS04
HEX INVERTERS



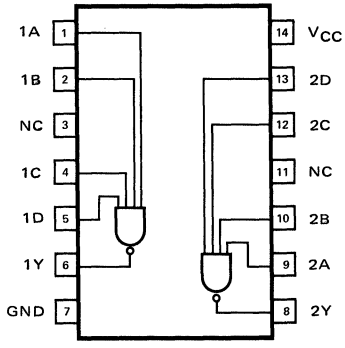
positive logic: $Y = \overline{A}$

S54LS10, N74LS10
TRIPLE 3-INPUT NAND GATES



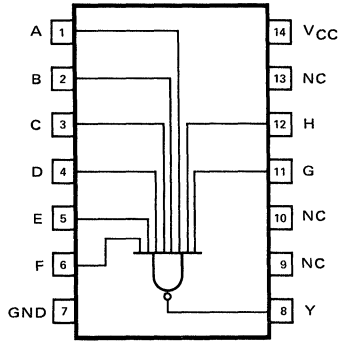
positive logic: $Y = \overline{ABC}$

S54LS20, N74LS20
DUAL 4-INPUT NAND GATES



positive logic: $Y = \overline{ABCD}$

S54LS30, N74LS30
8-INPUT NAND GATES



positive logic: $Y = \overline{ABCDEFGH}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS00 S54LS04, S54LS10 S54LS20, S54LS30			N74LS00 N74LS04, N74LS10 N74LS20, N74LS30			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
T_A	Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]		54LS00 54LS04, 54LS10 54LS20, 54LS30			74LS00 74LS04, 74LS10 74LS20, 74LS30			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2		0.8	2			V
V_{IL}	Low-level input voltage					-1.5			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA							-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -400μA	V_{IL} = 0.7V	2.5	3.4					V
			V_{IL} = 0.8V				2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V	I_{OL} = 4mA			0.4				V
			I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.36			-0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CCH}	Supply current, outputs high (average per gate)	V_{CC} = MAX, All inputs at 0V			0.2	0.4		0.2	0.4	mA
I_{CCL}	Supply current, outputs low (average per gate)	V_{CC} = MAX, All inputs at 5V			0.6	1.1		0.6	1.1	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

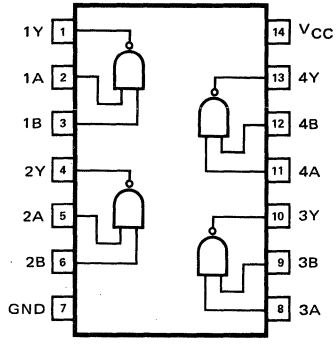
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 15 pF, R_L = 2 kΩ		9	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output	54/74LS00, 04, 10, 20			10	20	ns
		54LS30, 74LS30			25	35	

Load circuits and typical waveforms are shown at the front of this section.

PIN CONFIGURATION (TOP VIEW)

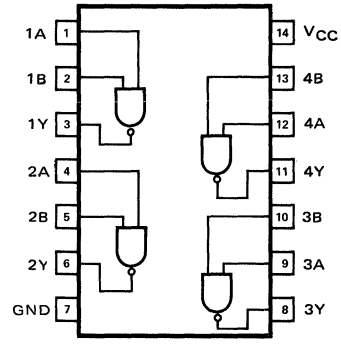
A,F,W PACKAGE

S54LS01, N74LS01
QUADRUPLE 2-INPUT NAND GATES



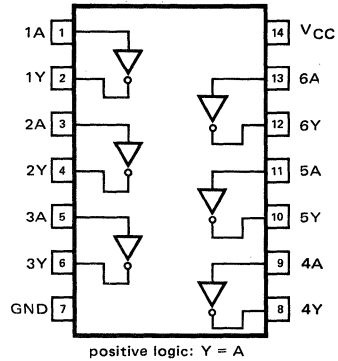
positive logic: Y = AB

S54LS03, N74LS03
QUADRUPLE 2-INPUT NAND GATES



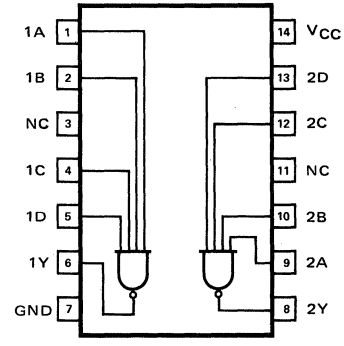
positive logic: $Y = \overline{AB}$

S54LS05, N74LS05
HEX INVERTERS



positive logic: Y = A

S54LS22, N74LS22
DUAL 4-INPUT NAND GATES



positive logic: Y = ABCD NC—No internal connection

FEATURES

- TYPICAL PROPAGATION TIME — 16ns @ C_L = 15pF
- TYPICAL POWER DISSIPATION — 2mW PER GATE @ 50% DUTY CYCLE
- LOGICALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 EQUIVALENTS

RECOMMENDED OPERATING CONDITIONS

PARAMETER		S54LS01, S54LS03 S54LS05, S54LS22			N74LS01, N74LS03 N74LS05, N74LS22			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output			10			20	
T_A	Operating free-air temperature	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		54LS01, 54LS03 54LS05, 54LS22			74LS01, 74LS03 74LS05, 74LS22			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = 18 mA				-1.5			-1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V	V_{IL} = 0.7 V			100				μA
			V_{IL} = 0.8 V						100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 4 mA			0.4				V
			I_{OL} = 8 mA						0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				-0.36			-0.36	mA
I_{CCH}	Supply current, outputs high (average per gate)	V_{CC} = MAX, All inputs at 0 V			0.2	0.4		0.2	0.4	mA
I_{CCL}	Supply current, outputs low (average per gate)	V_{CC} = MAX, All inputs at 5 V			0.6	1.1		0.6	1.1	mA

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5 V, T_A = 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 2 KΩ		17	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	28	ns

Load circuit and typical waveforms are shown at the front of this section.

signetics

LOW POWER SCHOTTKY QUADRUPLE 2-INPUT POSITIVE NOR GATES

S54LS02
N74LS02

S54LS-A,F,W • N74LS-A,F

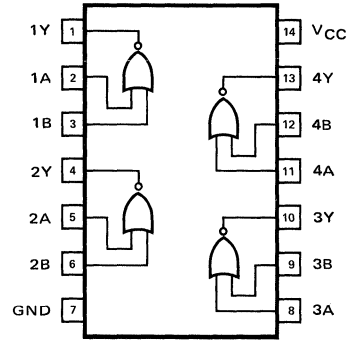
DIGITAL 54/74 TTL SERIES

FEATURES

- **TYPICAL PROPAGATION TIME — 10ns @ C_L = 15pF**
- **TYPICAL POWER DISSIPATION — 2.75mW PER GATE @ 50% DUTY CYCLE**
- **LOGICALLY AND MECHANICALLY IDENTICAL TO SERIES 54/74 EQUIVALENTS**

PIN CONFIGURATION (Top View)

A,F,W PACKAGE



positive logic: $Y = \overline{A+B}$

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		S54LS02			N74LS02			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18 mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -400μA	V_{IL} = 0.7 V	2.5	3.4					V
			V_{IL} = 0.8 V				2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 4 mA			0.4				V
			I_{OL} = 8 mA						0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				-0.36			-0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CCH}	Supply current, outputs high (average per gate)	V_{CC} = MAX, All inputs at 0 V			0.4	0.8		0.4	0.8	mA
I_{CCL}	Supply current, outputs low (average per gate)	V_{CC} = MAX, All inputs at 5 V			0.7	1.35		0.7	1.35	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[2] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS02			N74LS02			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
T_A	Operating free-air temperature		-55		125	0		70	°C

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 2 kΩ		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns

Load circuit and typical waveforms are shown at the front of this section.

PIN CONFIGURATIONS (Top View)

A,F,W PACKAGE

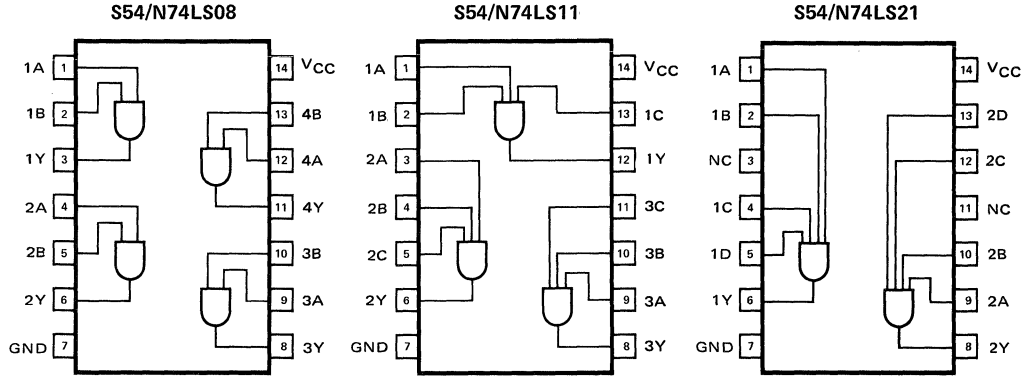


TABLE 1–SUPPLY CURRENT

PARAMETER		54/74LS08			54/74LS11			54/74LS21			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCH}	Total with outputs high		2.4	4.4		1.8	3.6		1.2	2.4	mA
I_{CCL}	Total with outputs low		6.8	8.8		3.3	6.6		2.2	4.4	mA
I_{CC}	Average per gate (50% duty cycle)		0.85			0.85			0.85		mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54LS08/11/21			74LS08/11/21			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−400			−400	μA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2		0.8	V
V_{IL}	Low-level input voltage		54 Family			0.8	V
			74 Family			0.8	
V_I	Input clamp voltage	V_{CC} = MIN, I_I = +18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, I_{OH} = MAX	54 Family	2.5	3.4		V
			74 Family	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} MAX., I_{OL} = MAX	54 Family		0.25	0.4	
			74 Family		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_{IH} = 2.4V			20	μA
			V_{IH} = 2.7V				
I_{IL}	Low-level input current	V_{CC} = MAX	V_{IL} = 0.4V			−0.36	mA
			V_{IL} = 0.5V				
I_{OS}	Short circuit output current[3]	V_{CC} = MAX	54 Family	−6		−40	mA
			74 Family	−5		−42	
I_{CC}	Supply current	V_{CC} = MAX			See Table 1		mA

[1]For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

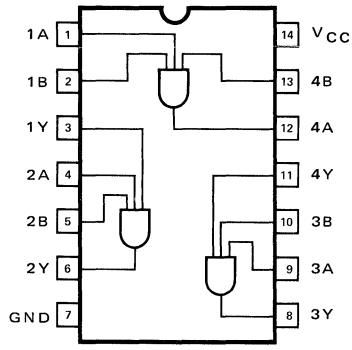
PARAMETER		TEST CONDITIONS	S54/N74LS08,11,21			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		12	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	24	ns

Load circuit and typical wave forms are shown at the front of this section.

PIN CONFIGURATION (Top View)

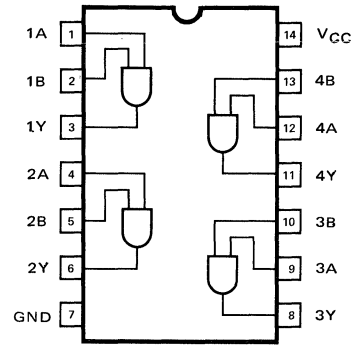
A,F,W PACKAGES

S54LS15
N74LS15



positive logic: Y = AB

S54LS09
N74LS09



positive logic: Y = AB

FEATURES

- TYPICAL PROPAGATION TIME – 20ns @ C_L = 15pF
- TYPICAL POWER DISSIPATION – 4.25mW PER GATE @ 50% DUTY CYCLE
- LOGICALLY AND MECHANICALLY IDENTICAL TO SERIES 54/74 EQUIVALENTS

RECOMMENDED OPERATING CONDITIONS

PARAMETER		S54LS09 S54LS15			N74LS09 N74LS15			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output			10			20	
T_A	Operating free-air temperature	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]	S54LS09 S54LS15			N74LS09 N74LS15			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA			-1.5			-1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V, V_{IH} = 2V			100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 4mA			0.4			0.5	V
		V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 8mA							
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-0.36			-0.36	mA
I_{CCH}	Supply current, outputs high (average per gate)	V_{CC} = MAX, All inputs at 5V		0.6	1.2		0.6	1.2	mA
I_{CCL}	Supply current, outputs low (average per gate)	V_{CC} = MAX, All inputs at 0V		1.1	2.2		1.1	2.2	mA

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.

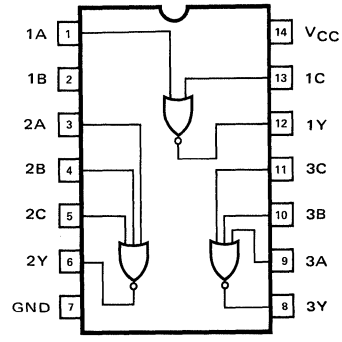
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		20	35	ns
t_{PHL} Propagation delay time, high-to-low-level output			20	35	ns

Load circuit and typical waveforms are shown at the front of this section.

PIN CONFIGURATION (Top View)

A,F,W PACKAGE



positive logic: $Y = \overline{A+B+C}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54LS27			74LS27			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High level output current			400			400	μA
I_{OL}	Low level input current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54 Family			0.8	V
				74 Family			0.8	
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.5	3.4		V
				74 Family	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, I_{OL} = MAX	54 Family		0.25	0.4	V
				74 Family		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current	Data inputs	V_{CC} = MAX	V_{IH} = 2.4V				μA
		Strobe of '25		V_{IH} = 2.7V			20	
		All inputs		V_{IL} = 0.3V				
I_{IL}	Low-level input current	Data inputs	V_{CC} = MAX	V_{IL} = 0.4V			−0.36	mA
		Strobe of '25						
		All inputs		V_{IL} = 0.5V				
I_{OS}	Short circuit output current		V_{CC} = MAX	54 Family	−6		−40	mA
				74 Family	−5		−42	
I_{CC}	Supply current		V_{CC} = MAX	See Table 1				mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

TABLE 1 – SUPPLY CURRENT[1]

I_{CCH} Total with outputs high		I_{CCL} Total with outputs low		I_{CC} Average per gate (50% duty cycle)		UNIT
TYP	MAX	TYP	MAX	TYP	MAX	
2.0	4	3.4	6.8	0.9		mA

NOTE

1. Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5V, T_A = 25°C.

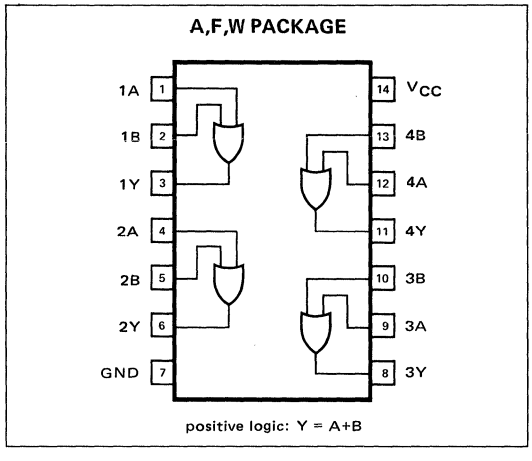
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITION	54/74LS27			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level input	C_L = 15pF, R_L = 2KΩ		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level input			10	20	ns

NOTE

1. All input pulses are supplied by generators having the following characteristics: $t_r \leq 15$ns, $t_f \leq 6$ns, PRR ≤ 1MHz, $Z_{out} \approx 50\Omega$ and t_w = 100ns. Load circuit and typical waveforms are shown at the front of this section.

PIN CONFIGURATION Top View



ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-Air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54 Family			0.8	V
				74 Family			0.8	
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, I_{OH} = MAX	54 Family	2.5	3.4		V
				74 Family	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OL} = MAX	54 Family		0.25	0.4	V
				74 Family		0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V				0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_{IH} = 2.4V			20	μA
				V_{IH} = 2.7V				
I_{IL}	Low-level input current		V_{CC} = MAX, V_{IL} = 0.4V				-0.36	mA
I_{OS}	Short-circuit input current		V_{CC} = MAX	54 Family	−6		−40	mA
				74 Family	−5		−42	
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX			8.1	6.2	mA
		Total, outputs low				4.9	9.8	
		Average per gate	V_{CC} = 5V, 50% duty cycle			1.00		

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

RECOMMENDED OPERATING CONDITIONS

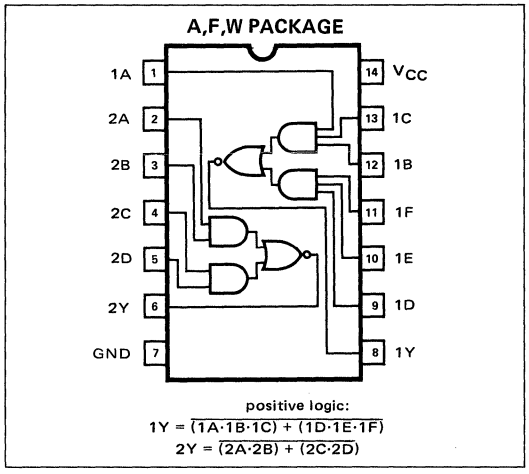
PARAMETER		54LS32			74LS32			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level input current			−400			−400	μA
I_{OL}	Low-level input current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER		TEST CONDITION	54/74LS32			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level input	C_L = 15pF		14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level input	R_L = 2KΩ		14	22	ns

Load circuit and typical waveforms are shown at front of this section.

PIN CONFIGURATION (Top View)



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		S54LS51			N74LS51			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -400μA	V_{IL} = 0.7V	2.5	3.4					V
			V_{IL} = 0.8V				2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V	I_{OL} = 4mA			0.4				V
			I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.36			-0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CCH}	Supply current, outputs high (average per AO1 gate)	V_{CC} = MAX, See Note 1			0.4	0.8		0.4	0.8	mA
I_{CCL}	Supply current, outputs low (average per AO1 gate)	V_{CC} = MAX, See Note 2			0.7	1.4		0.7	1.4	mA

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.

NOTES: 1. I_{CCH} is measured with all inputs grounded and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5V, the remaining inputs grounded, and the outputs open.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS51			N74LS51			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
T_A	Operating free-air temperature		-55		125	0		70	°C

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		12	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			12.5	20	ns

Load circuit and typical waveforms are shown at the front of this section.

signetics

LOW POWER SCHOTTKY 4-WIDE 2-3-3-2-INPUT AND-OR-INVERT GATES

S54LS54 N74LS54

S54LS-A,F,W • N74LS-A,F

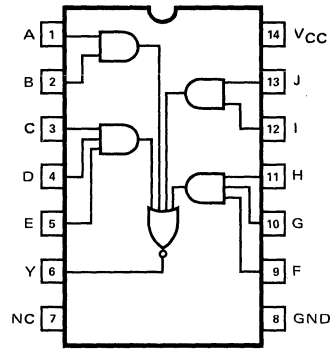
DIGITAL 54/74 TTL SERIES

FEATURES

- TYPICAL PROPAGATION TIME — 12.5ns @ C_L = 15pF
- TYPICAL POWER DISSIPATION — 4.5mW @ 50% DUTY CYCLE
- LOGICALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 EQUIVALENT

PIN CONFIGURATION (Top View)

A,F,W PACKAGE



positive logic:

$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

NC—No internal connection

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		S54LS54			N74LS54			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -400μA	V_{IL} = 0.7V	2.5	3.4					V
			V_{IL} = 0.8V				2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V	I_{OL} = 4mA			0.4				V
			I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.36			-0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CCH}	Supply current, output high	V_{CC} = MAX, See Note 1			0.8	1.6		0.8	1.6	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2			1.0	2		1.0	2	mA

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[2]All typical values are at V_{CC} = 5V, T_A = 25°C.

[3]Not more than one output should be shorted at a time.

NOTES: 1. I_{CCH} is measured with all inputs grounded, and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5V, the remaining inputs grounded, and the outputs open.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54LS55			74LS55			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			10	
T_A	Operating free-air temperature		-55		125	0		70	°C

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

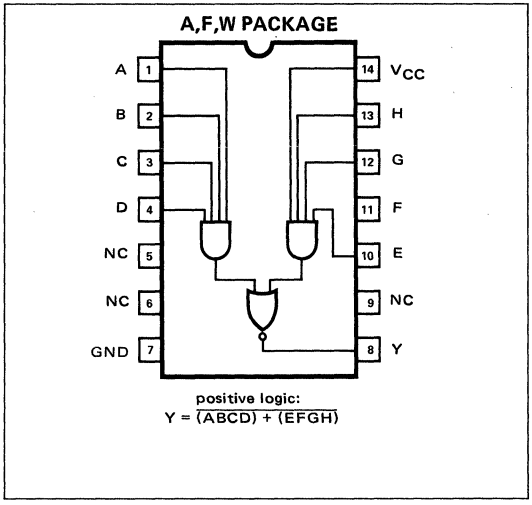
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 2kΩ		12	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			12.5	20	ns

Load circuit and typical waveforms are shown at front of this section.

FEATURES

- TYPICAL PROPAGATION TIME – 12.5ns @ C_L = 15pF
- TYPICAL POWER DISSIPATION – 2.75mW PER GATE @ 50% DUTY CYCLE
- LOGICALLY AND MECHANICALLY IDENTICAL TO THE SERIES 54/74 EQUIVALENT

PIN CONFIGURATION (Top View)



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]		54LS55			74LS55			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -400μA	V_{IL} = 0.7V	2.5	3.4					V
			V_{IL} = 0.8V				2.7	3.4		
V_{OL}	Low-level output voltage		I_{OL} = 4mA			0.4				V
			I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				-0.36			-0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CCH}	Supply current, output high	V_{CC} = MAX, See Note 1			0.4	0.8		0.4	0.8	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2			0.7	1.3		0.7	1.3	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC}= 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

NOTES: 1. I_{CCH} is measured with all inputs grounded, and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5V, the remaining inputs grounded, and the outputs open.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS54			N74LS54			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			10	
T_A	Operating free-air temperature		-55		125			70	C

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15pF		12	20	ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 2kΩ		12.5	20	ns

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

These monolithic edge-triggered dual J-K flip-flops feature individual J, K, clock, and clear inputs to each flip-flop. A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

FUNCTION TABLE (Each Flip-Flop)

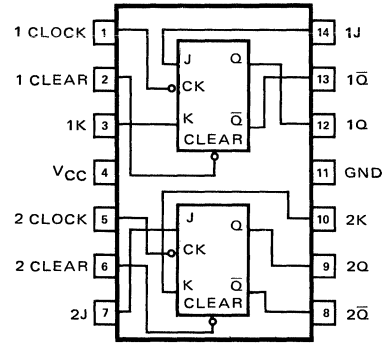
INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

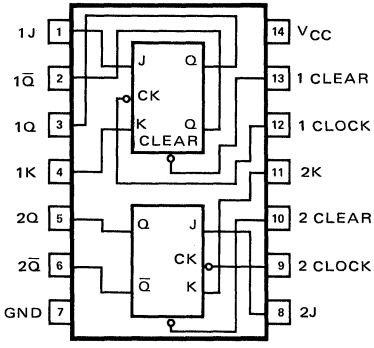
PIN CONFIGURATION (Top View)

A,F,W PACKAGE

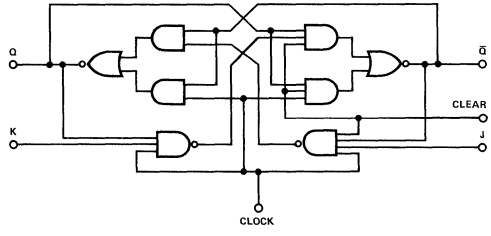
54/74LS73



54/74LS107



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER		S54LS73			N74LS73			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
N Normalized fan-out from each output	High logic level			20			20	
	Low logic level			10			20	
f_{clock} Clock Frequency		0		30	0		30	MHz
t_w Width of clock or clear pulse		25			25			ns
t_{setup} Input set up time		20			20			ns
t_{hold} Input hold time		0			0			ns
T_A Output free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS[1]			S54LS73/107			N74LS73/107			UNIT
						MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH} High-level input voltage						2			2			V
V_{IL} Low-level input voltage								0.8			0.8	V
V_I Input clamp voltage			V_{CC} = MIN,	I_I = -18mA				-1.5			-1.5	V
V_{OH} High-level output voltage			V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = -400μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage			V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V	I_{OL} = 4mA			0.4				V
					I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	J or K	V_{CC} = MAX,	V_I = 5.5V				0.1			0.1	mA
		Clear						0.3			0.3	
		Clock						0.4			0.4	
I_{IH}	High-level input current	J or K	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
		Clear						60			60	
		Clock						80			80	
I_{IL}	Low-level input current	J or K	V_{CC} = MAX,	V_I = 0.4V				-0.36			-0.36	mA
		Clear						-0.8			-0.8	
		Clock						-0.72			-0.72	
I_{OS} Short-circuit output current[3]			V_{CC} = MAX			-6		-40	-5		-42	mA
I_{CC} Supply current			V_{CC} = MAX,	See Note 1			4	8		4	8	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[2] All typical values are at V_{CC} = 5V, T_A = 25°C.

[3] Not more than one output should be shorted at a time.

NOTE 1: I_{CC} is measured with outputs open, first with all inputs grounded, and second with J and clear at 4.5V, K grounded, and clock at a momentary 4.5V, then grounded.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF R_L = 2kΩ	30	45		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			15	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			15	30	ns

NOTES

A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 15$ns, $t_f \leq 6$ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\Omega$, and t_w = 100ns.

Load circuit and typical waveforms are shown at the front of this section.

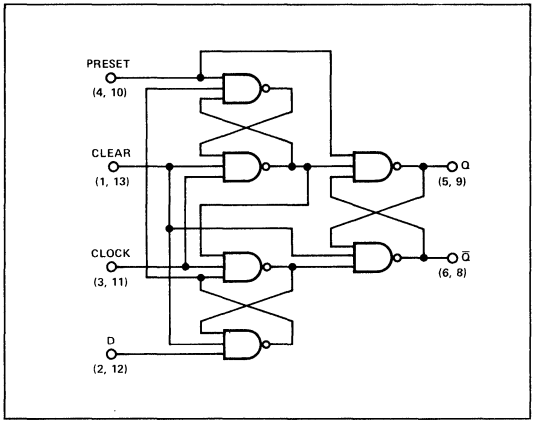
TO BE ANNOUNCED

DESCRIPTION

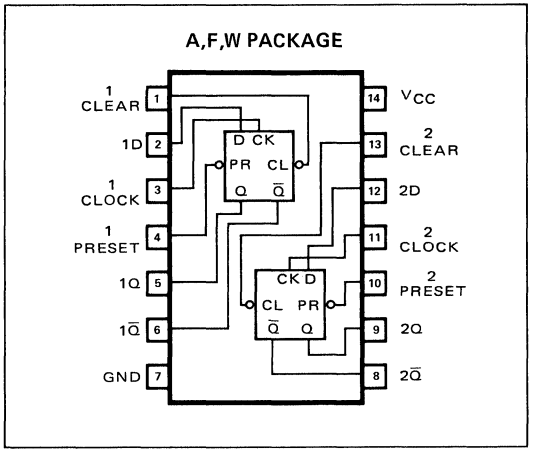
These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION (Top View)



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
H	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state) L = low level (steady state)

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS74			N74LS74			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
f_{clock}	Clock frequency		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock pulse		25			25			ns
$t_{w(preset)}$	Width of preset pulse		25			25			ns
$t_{w(clear)}$	Width of clear pulse		25			25			ns
t_{setup}	Input setup time	High-level data	25			25			ns
		Low-level data	20			20			
t_{hold}	Input hold time		0			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]	54LS74			74LS74			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = -18mA			-1.5			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V V_{IL} = V_{IL} max, I_{OH} = -400μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 4mA			0.4				V
			V_{IL} = V_{IL} max I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	D input	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
		Clock or preset				0.2			0.2	
		Clear				0.3			0.3	
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.7V			20			20	μA
		Clock or preset				40			40	
		Clear				60			60	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4V			-0.36			-0.36	mA
		Clock or preset				-0.8			-0.8	
		Clear				-1.15			-1.15	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	-6		-40	-5		-42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		4	8		4	8	mA

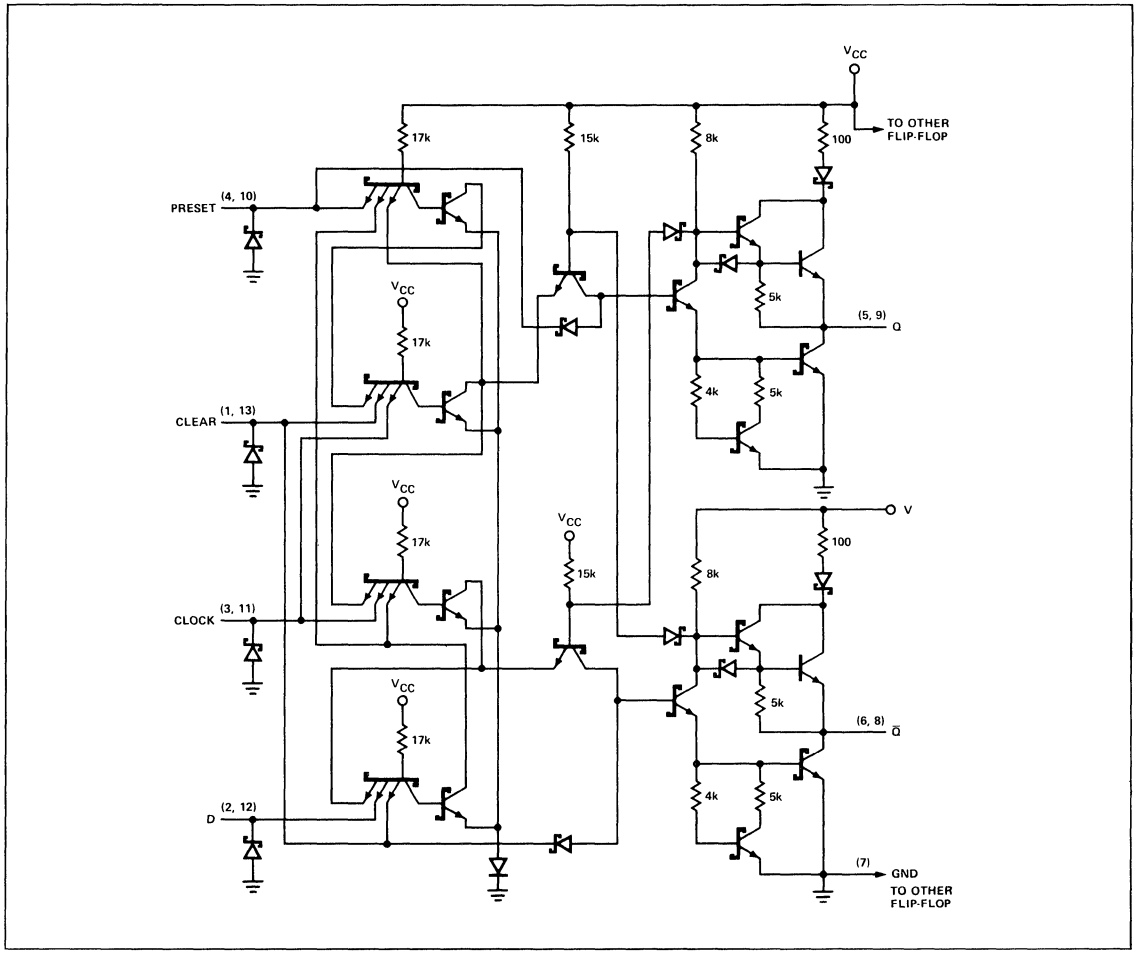
NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable device type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. I_{CC} is measured with outputs open with D, Clock and Preset grounded; then with D, Clock and Clear grounded.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF R_L = 2kΩ	25	33		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns

SCHEMATIC (Each Flip-Flop)



Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

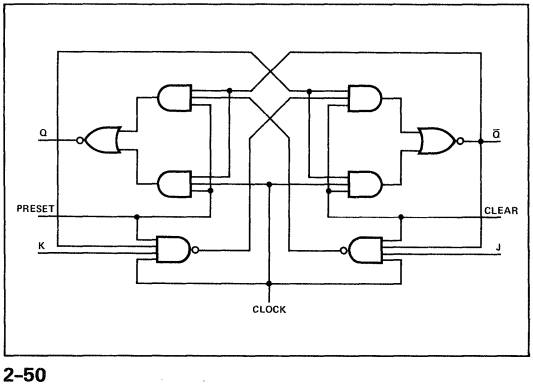
These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

FUNCTION TABLE (Each Flip Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

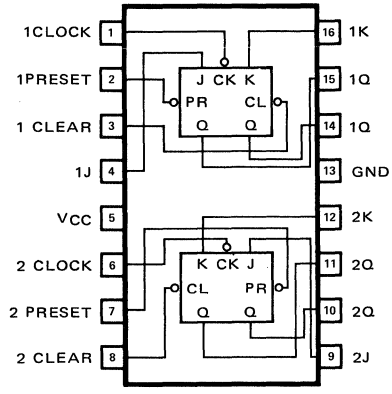
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

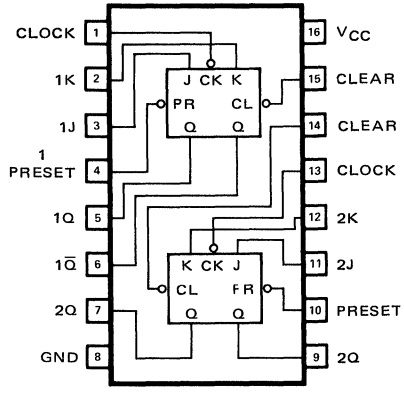
B,F,W PACKAGE

S54/N74LS76



positive logic: see function table

S54/N74LS112



positive logic: see function table

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS76 S54LS112			N74LS76 N74LS112			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
f_{clock}	Clock frequency		0		30	0		30	MHz
$t_{w(clock)}$	Width of clock pulse		20			20			ns
$t_{w(preset)}$	Width of preset pulse		25			25			ns
$t_{w(clear)}$	Width of clear pulse		25			25			ns
t_{setup}	Input setup time		20			20			ns
t_{hold}	Input hold time		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS[1]			S54LS76 S54LS112			N74LS76 N74LS112			UNIT
						MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN,	V_{IH} = 2V,	I_{OL} = 4mA			0.4				V
			V_{IL} = V_{IL} max		I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	J or K						0.1			0.1	mA
		Clock	V_{CC} = MAX,	V_I = 5.5V				0.4			0.4	
		Preset or Clear						0.3			0.3	
I_{IH}	High-level input current	J or K						20			20	μA
		Clock	V_{CC} = MAX,	V_I = 2.7V				80			80	
		Preset or Clear						60			60	
I_{IL}	Low-level input current	J or K						−0.36			−0.36	mA
		Clock	V_{CC} = MAX,	V_I = 0.4V				−0.72			−0.72	
		Preset or Clear						−0.8			−0.8	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−6		−40	−6		−42	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 1			4	8		4	8	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.
NOTE 1: I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5V; then with clock, J, K, and preset grounded and clear at 4.5V.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

These monolithic dual J-K edge-triggered flip-flops feature individual J, K, and preset inputs plus common clock and common clear inputs. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

FUNCTION TABLE Each Flip-Flop

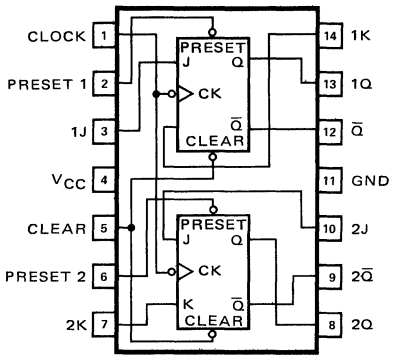
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN CONFIGURATION

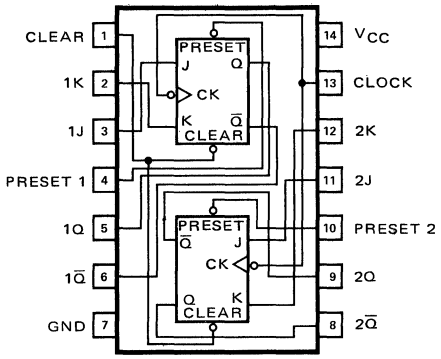
A,F,W PACKAGE

S54/N74LS78



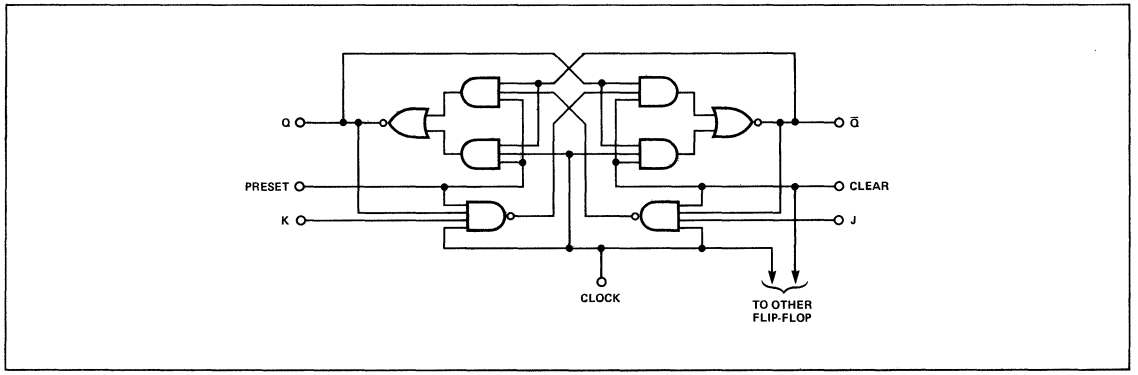
positive logic: see function table

S54/N74LS114



positive logic: see function table

FUNCTIONAL BLOCK DIAGRAM Each Flip-Flop



RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS78 S54LS114			N74LS78 N74LS114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
f_{clock}	Clock frequency		0		30	0		30	MHz
$t_{w(clock)}$	Width of clock frequency		20			20			ns
$t_{w(preset)}$	Width of preset pulse		25			25			ns
$t_{w(clear)}$	Width of clear pulse		25			25			ns
t_{setup}	Input setup time		20			20			ns
t_{hold}	Input hold time		0			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]		S54LS78 S54LS114			N74LS78 N74LS114			UNIT
					MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = -18mA			-1.5			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = -400μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V, I_{OL} = 4mA			0.4				V
				I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	J or K	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
		Preset					0.3			0.3	
		Clear					0.6			0.6	
		Clock					0.8			0.8	
I_{IH}	High-level input current	J or K	V_{CC} = MAX,	V_I = 2.7V			20			20	μA
		Preset					60			60	
		Clear					120			120	
		Clock					160			160	
I_{IL}	Low-level input current	J or K	V_{CC} = MAX,	V_I = 0.4V			-0.36			-0.36	mA
		Preset					-0.8			-0.8	
		Clear					-1.6			-1.6	
		Clock					-1.44			-1.44	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-5		-40	-5		-42	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 1		4	8		4	8	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

NOTE 1: I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5V, then with clock, J, K, and preset grounded and clear at 4.5V.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF R_L = 2kΩ	30	45		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns

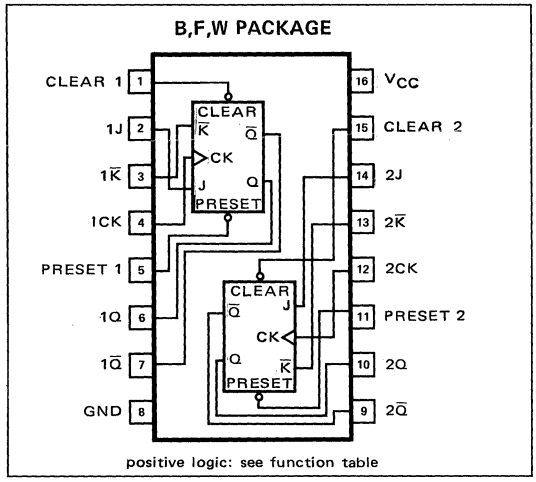
Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

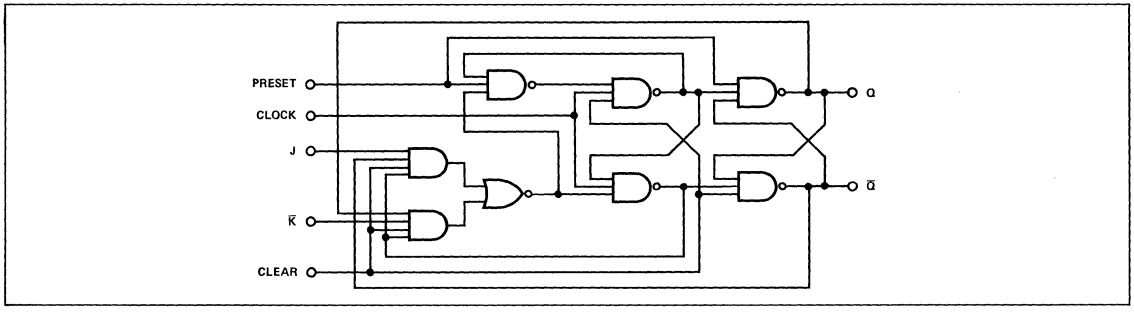
These monolithic dual J-$\overline{K}$ edge-triggered flip-flops feature individual J, $\overline{K}$, clock, preset, and clear inputs. A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs.

The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

PIN CONFIGURATION (Top View)



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS109			N74LS109			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.35	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
f_{clock}	Clock frequency		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock pulse		25			25			ns
$t_{w(preset)}$	Width of preset pulse		25			25			ns
$t_{w(clear)}$	Width of clear pulse		25			25			ns
t_{setup}	Input setup time		20			20			ns
t_{hold}	Input hold time		0			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level on each ↑ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS[1]			S54LS109			N74LS109			UNIT
						MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN,	V_{IH} = 2V,	I_{OL} = 4mA			0.4				V
			V_{IL} = V_{IL} max		I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	J or $\overline{K}$	V_{CC} = MAX,	V_I = 5.5V				0.1			0.1	mA
		Clock or preset						0.2			0.2	
		Clear						0.4			0.4	
I_{IH}	High-level input current	J or $\overline{K}$	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
		Clock or preset						40			40	
		Clear						80			80	
I_{IL}	Low-level input current	J or $\overline{K}$	V_{CC} = MAX,	V_I = 0.4V				−0.4			−0.4	mA
		Clock or preset						−0.8			−0.8	
		Clear						−1.6			−1.6	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 1			4	8		4	8	mA

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.
NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, $\overline{K}$, preset, and clear at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 2kΩ	25	33		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns

Load circuit and typical waveforms are shown at the front of this section.

LOW POWER SCHOTTKY DUAL J-K POSITIVE EDGE-TRIGGERED FLIP-FLOPS

S54LS113
N74LS113

S54LS113-A,F,W • N74LS113-A,F

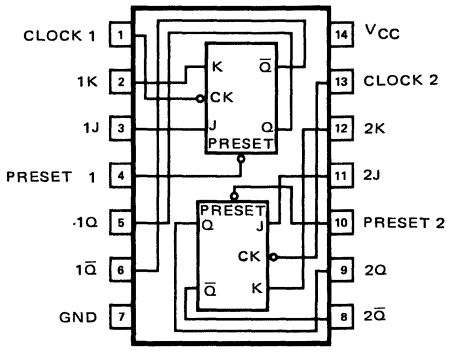
DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic dual J-K edge-triggered flip-flops feature individual J, K, clock, and preset inputs. A low level at the preset input sets the Q output high regardless of the levels at the other inputs. When preset is inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

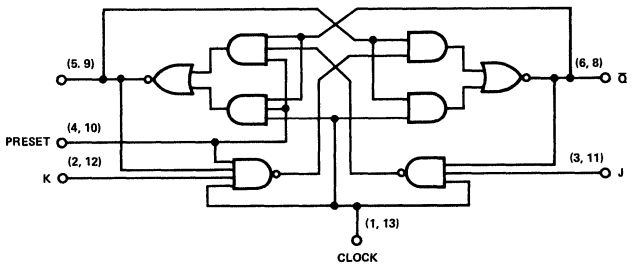
PIN CONFIGURATION (Top View)

A,F,W PACKAGE



positive logic: see function table

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS113 MIN	S54LS113 TYP	S54LS113 MAX	N74LS113 MIN	N74LS113 TYP	N74LS113 MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
f_{clock}	Clock frequency		0		30	0		30	MHz
$t_{w(clock)}$	Width of clock pulse		20			20			ns
$t_{w(preset)}$	Width of preset pulse		25			25			ns
t_{setup}	Input setup time		20			20			ns
t_{hold}	Input hold time		0			0			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

FUNCTION TABLE Each Flip-Flop

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level of each ↓ clock transition.

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]		S54LS113			N74LS113			UNIT
					MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = -18mA			-1.5			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = -400μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V, I_{OL} = 4mA			0.4				V
				I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	J or K	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
		Preset					0.3			0.3	
		Clock					0.4			0.4	
I_{IH}	High-level input current	J or K	V_{CC} = MAX,	V_I = 2.7V			20			20	μA
		Preset					60			60	
		Clock					80			80	
I_{IL}	Low-level input current	J or K	V_{CC} = MAX,	V_I = 0.4V			-0.36			-0.36	mA
		Preset					-0.8			-0.8	
		Clock					-0.72			-0.72	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 1		4	8		4	8	mA

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.
NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, and preset at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 2kΩ	30	45		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns

Load circuit and typical waveforms are shown at the front of this section.

TO BE ANNOUNCED

DESCRIPTION

The S54LS138 and N74LS138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications. Typical delay time through the three-level address circuitry is 22 nanoseconds. Typical power dissipation is 32 milliwatts.

The S54LS139 and N74LS139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. Typical total delay time is 22 nanoseconds through the three-gate-level address circuitry and power consumption is typically 34 milliwatts total.

FEATURES

- INDIVIDUAL STROBES SIMPLIFY CASCADING FOR DECODING OR DEMULTIPLEXING LARGER WORDS
- INPUT CLAMPING DIODES SIMPLIFY SYSTEMS DESIGN
- TYPICAL AVERAGE SELECT-TO-OUTPUT PROPAGATION DELAY OF 22 ns THROUGH 3 LEVELS OF LOGIC
- LOW POWER DISSIPATION
- SCHOTTKY-DIODE-CLAMPED TRANSISTORS

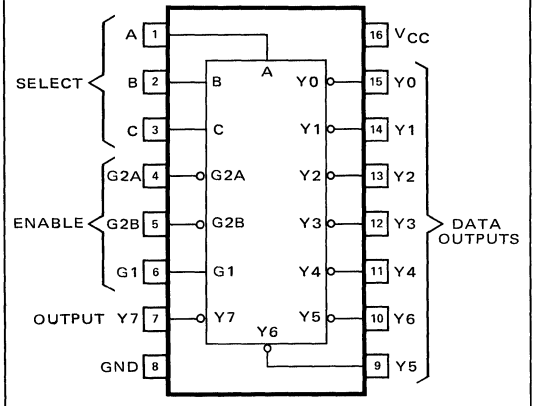
APPLICATIONS

54/74LS138: 3-TO-8-LINE DECODER
1-TO-8-LINE DEMULTIPLEXER
54/74LS139: DUAL 2-TO-4-LINE DECODER
DUAL 1-TO-4-LINE DEMULTIPLEXER

PIN CONFIGURATION (Top View)

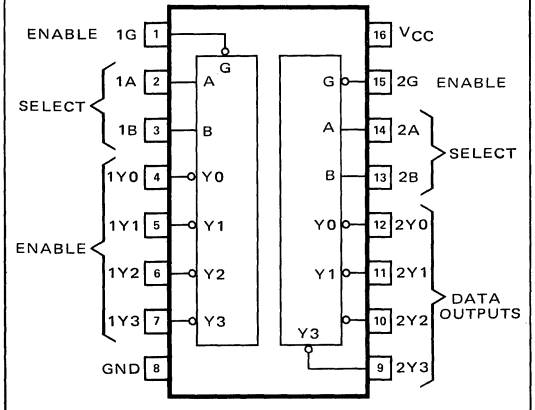
B,F,W PACKAGE

S54/N74LS138



positive logic: see function table

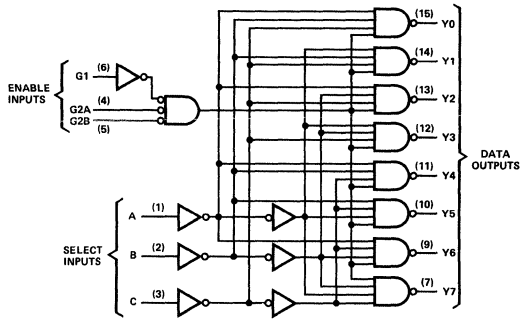
S54/N74LS139



positive logic: see function table

FUNCTIONAL BLOCK DIAGRAMS AND LOGIC

S54/N74LS138

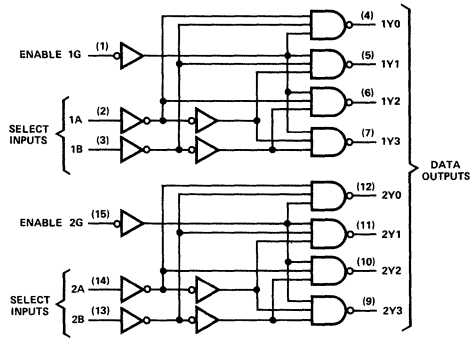


FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

S54/N74LS139



FUNCTION TABLE (Each Decoder/Demultiplexer)

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS138 S54LS139			N74LS138 N74LS139			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
N	Normalized fan-out from each output	High logic level			20			20	
		Low logic level			10			20	
T_A	Operating free-air temperature		55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]			S54LS138 S54LS139			N74LS138 N74LS139			UNIT
					MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2V,	I_{OL} = 4mA			0.4				V
		V_{IL} = V_{IL} max		I_{OL} = 8mA						0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				−0.36			−0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX,		54/74LS138		6.3	10		6.3	10	mA
		Outputs enabled and open		54/74LS139		6.8	11		6.8	11	

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	S54LS138 N74LS138			S54LS139 N74LS139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	C_L = 15pF, R_L = 2kΩ		13	20		13	20	ns
t_{PHL}						27	41		22	33	ns
t_{PLH}			3			18	27		18	29	ns
t_{PHL}						26	39		25	38	ns
t_{PLH}	Enable	Any	2			12	18		16	24	ns
t_{PHL}						21	32		21	32	ns
t_{PLH}			3			17	26				ns
t_{PHL}						25	28				ns

[1]t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

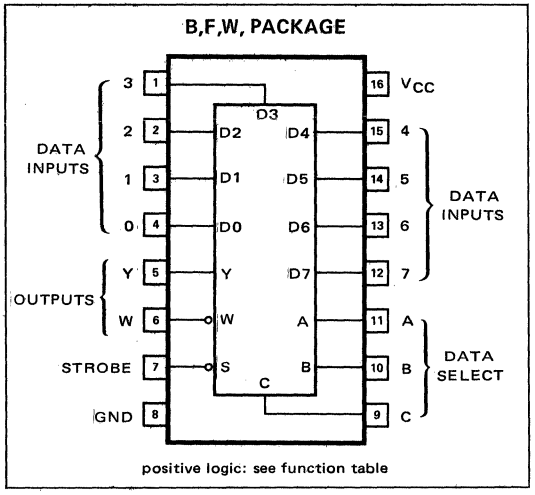
Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

The S54/N74LS151 is a monolithic data selector/multiplexer which contains full on-chip binary decoding to select the desired data source.

This device features complementary W and Y outputs. It also has a strobe input which must be at a low logic level to enable the device. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

PIN CONFIGURATION (Top View)



FEATURES

- SELECT ONE-OF-EIGHT DATA SOURCES
- PERFORMS PARALLEL-TO-SERIAL CONVERSION
- PERMITS MULTIPLEXING FROM N LINES TO ONE LINE
- ALSO FOR USE AS BOOLEAN FUNCTION GENERATOR
- INPUT-CLAMPING DIODES SIMPLIFY SYSTEM DESIGN

FUNCTION TABLE

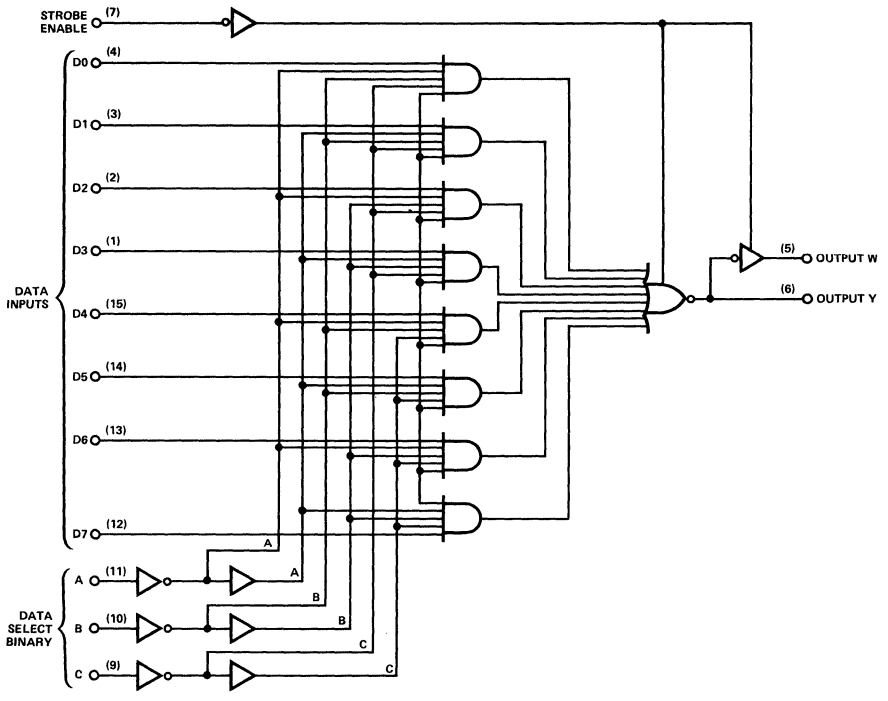
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

RECOMMENDED OPERATING CONDITIONS

PARAMETER		S54LS151			N74LS151			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-400			-400	μA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]	S54LS151			N74LS151			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max, I_{OH} = -400μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 4mA		0.25	0.4				V
		V_{IL} = V_{IL} max I_{OL} = 8mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-0.4			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	-6		-40	-5		-42	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open, All inputs at 4.5V		6.0	10		6.0	10	mA

[1]For conditions shown as MIN or MAX, use the appropriate value under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH} t_{PHL}	A, B, or C (4 levels)	Y	C_L = 15pF R_L = 2kΩ		27 31	43 50	ns
t_{PLH} t_{PHL}	A, B, or C (3 levels)	W			24 20	39 32	ns
t_{PLH} t_{PHL}	Strobe	Y			23 25	37 42	ns
t_{PLH} t_{PHL}	Strobe	W			19 16	31 26	ns
t_{PLH} t_{PHL}	Any D	Y			16 20	26 32	ns
t_{PLH} t_{PHL}	Any D	W			13 9	21 15	ns

[1] t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

Load circuit and typical waveforms are shown at front of this section.

TO BE ANNOUNCED

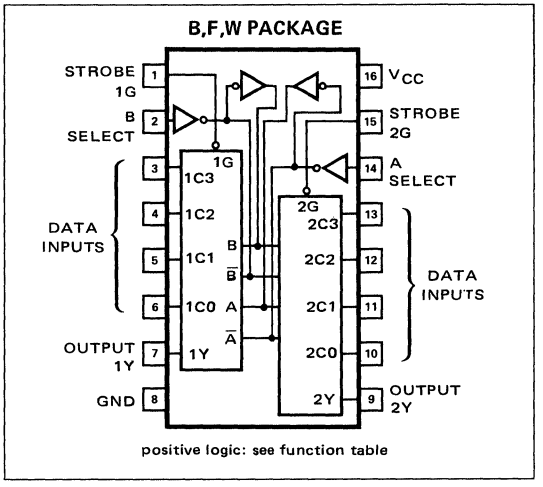
DESCRIPTION

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

FEATURES

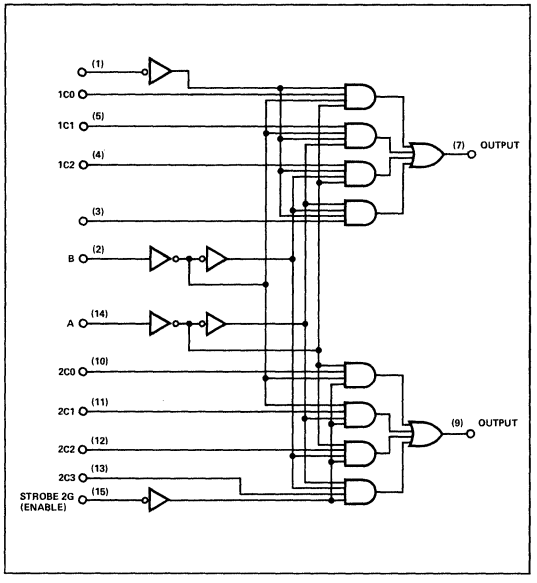
- PERMITS MULTIPLEXING FROM N LINES TO 1 LINE
- PERFORMS PARALLEL-TO-SERIAL CONVERSION
- STROBE (ENABLE) LINE PROVIDED FOR CASCADING (N LINES TO n LINES)
- HIGH-FAN-OUT, LOW-IMPEDANCE, TOTEM-POLE OUTPUTS
- FULLY COMPATIBLE WITH MOST TTL AND DTL CIRCUITS

PIN CONFIGURATION (Top View)



positive logic: see function table

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54LS153			74LS153			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-400			-400	μA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS[1]	54LS153			74LS153			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max, I_{OH} = -400μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max, I_{OL} = 4mA		0.25	0.4				V
		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max, I_{OL} = 8mA					0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-0.36			-0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	-6		-40	-5		-42	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2		6.2	10		6.2	10	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15pF, R_L = 2kΩ		10	15	ns
t_{PHL}	Data	Y			17	26	ns
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select	Y			25	38	ns
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe	Y			21	32	ns

[1] t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

Load circuit and typical waveforms are shown at the front of this section.

signetics

LOW POWER SCHOTTKY HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

S54LS-B,F,W • N74LS-B,F

DIGITAL 54/74 TTL SERIES

S54LS174
N74LS174
S54LS175
N74LS175

TO BE ANNOUNCED

DESCRIPTION

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the S54/N74175 features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

FEATURES

- 40MHz TYPICAL MAXIMUM FREQUENCY
- THREE PERFORMANCE RANGES OFFERED
- BUFFERED CLOCK AND DIRECT CLEAR INPUTS
- INDIVIDUAL DATA INPUT TO EACH FLIP-FLOP
- S54/N74LS174
  HEX D-TYPE FLIP-FLOPS
  CONTAINS 6 FLIP-FLOPS WITH SINGLE-RAIL OUTPUTS
- S54/N74LS175
  QUADRUPLE D-TYPE FLIP-FLOPS
  CONTAINS 4 FLIP-FLOPS WITH SINGLE-RAIL OUTPUTS

FUNCTION TABLE (Each Flip-Flop)

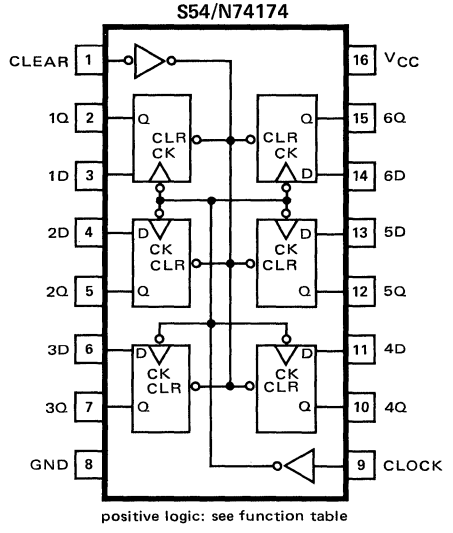
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$[1]
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
[1] = S54/N74175 only

PIN CONFIGURATION (Top View)

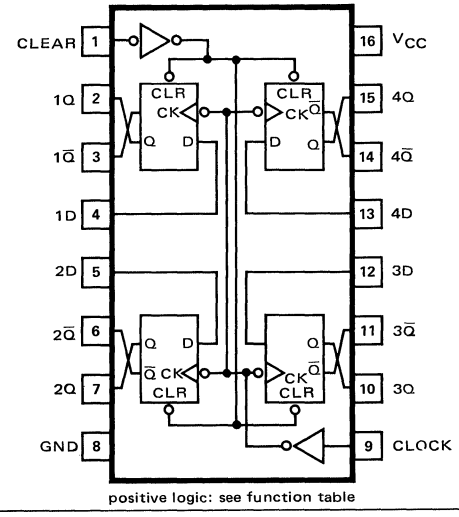
B,F,W PACKAGE

S54/N74174



positive logic: see function table

S54/N74175



positive logic: see function table

APPLICATIONS

BUFFER/STORAGE REGISTERS

SHIFT REGISTERS

PATTERN GENERATORS

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]		54LS174 54LS175			74LS174 74LS175			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{CC} = V_{IL} max,	V_{IH} = 2V, I_{OH} = -400mA	2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V, I_{OL} = 4mA		0.25	0.4				V
			I_{OL} = 8mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_{IL}	Low-level input current: Clock input	V_{CC} = MAX,	V_I = 0.4V			-0.4			-0.4	mA
	Low-level input current: Other inputs					-0.36			-0.36	
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-6		-40	-5		-42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	S54/74		13	22		13	22	mA
			S54/N74175		9	15		9	15	

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54LS174 54LS175			74LS174 74LS175			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				-400			-400	μA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Width of clock or clear pulse		20			20			ns
t_{setup}	Setup time	Data input	20			20			ns
		Clear inactive-state	25			25			ns
t_{hold}	Data hold time		5			5			ns
T_A	Operating free-air temperature		-55		125	0		70	°C

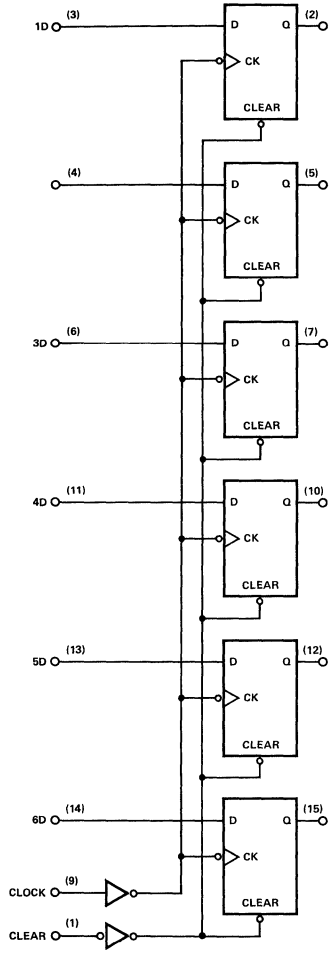
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 2K	30	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear (S54/N74LS175 only)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns

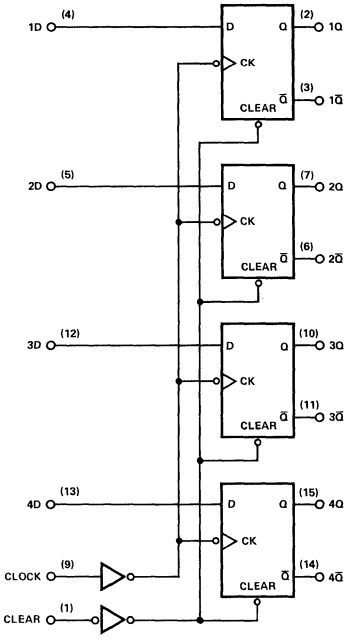
Load circuit and typical waveforms are shown at the front of this section.

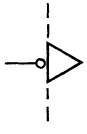
FUNCTIONAL BLOCK DIAGRAMS

S54/N74LS174



S54/N74LS175





. . . dynamic input activated by transition from a high level to a low level.

signetics

LOW POWER SCHOTTKY ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS

S54LS181-N,Q,F • N74LS181-N,F

DIGITAL 54/74 TTL SERIES

S54LS181 N74LS181

DESCRIPTION

The S54/N74LS181 arithmetic logic unit (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182 full carry look-ahead circuit, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

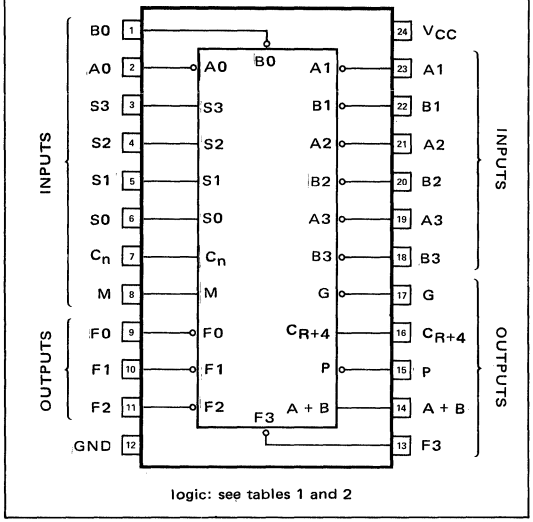
The S54/N74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

FEATURES

- FULL LOOK-AHEAD FOR HIGH-SPEED OPERATIONS ON LONG WORDS
- INPUT CLAMPING DIODES MINIMIZE TRANSMISSION-LINE EFFECTS
- DARLINGTON OUTPUTS REDUCE TURN-OFF TIME
- ARITHMETIC OPERATING MODES:
  - ADDITION
  - SUBTRACTION
  - SHIFT OPERAND A ONE POSITION
  - MAGNITUDE COMPARISON
  - PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- LOGIC FUNCTION MODES:
  - EXCLUSIVE-OR
  - COMPARATOR
  - AND, NAND, OR, NOR
  - PLUS TEN OTHER LOGIC OPERATIONS

PIN CONFIGURATION (Top View)

N,Q,F PACKAGE



PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table II)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

DESCRIPTION Cont'd

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A–B–1 which requires an end-around or forced carry to provide A–B.

The S54/N74LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A ≤ B	A ≥ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≥ B	A ≤ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS devices are characterized for operation from 0°C to 70°C.

ALU SIGNAL DESIGNATIONS

The S54/N74LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

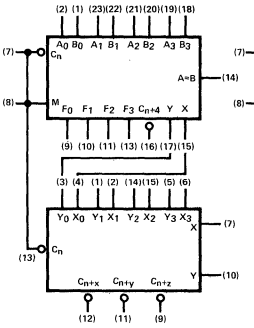


FIGURE 1 (FOR TABLE 1)

FIGURE 2 (FOR TABLE 2)

TABLE 1

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L: ARITHMETIC OPERATIONS	
				LOGIC	C_n = H	C_n = L
S3	S2	S1	S0	FUNCTIONS	(NO CARRY)	(WITH CARRY)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A -B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

FUNCTIONAL BLOCK DIAGRAM

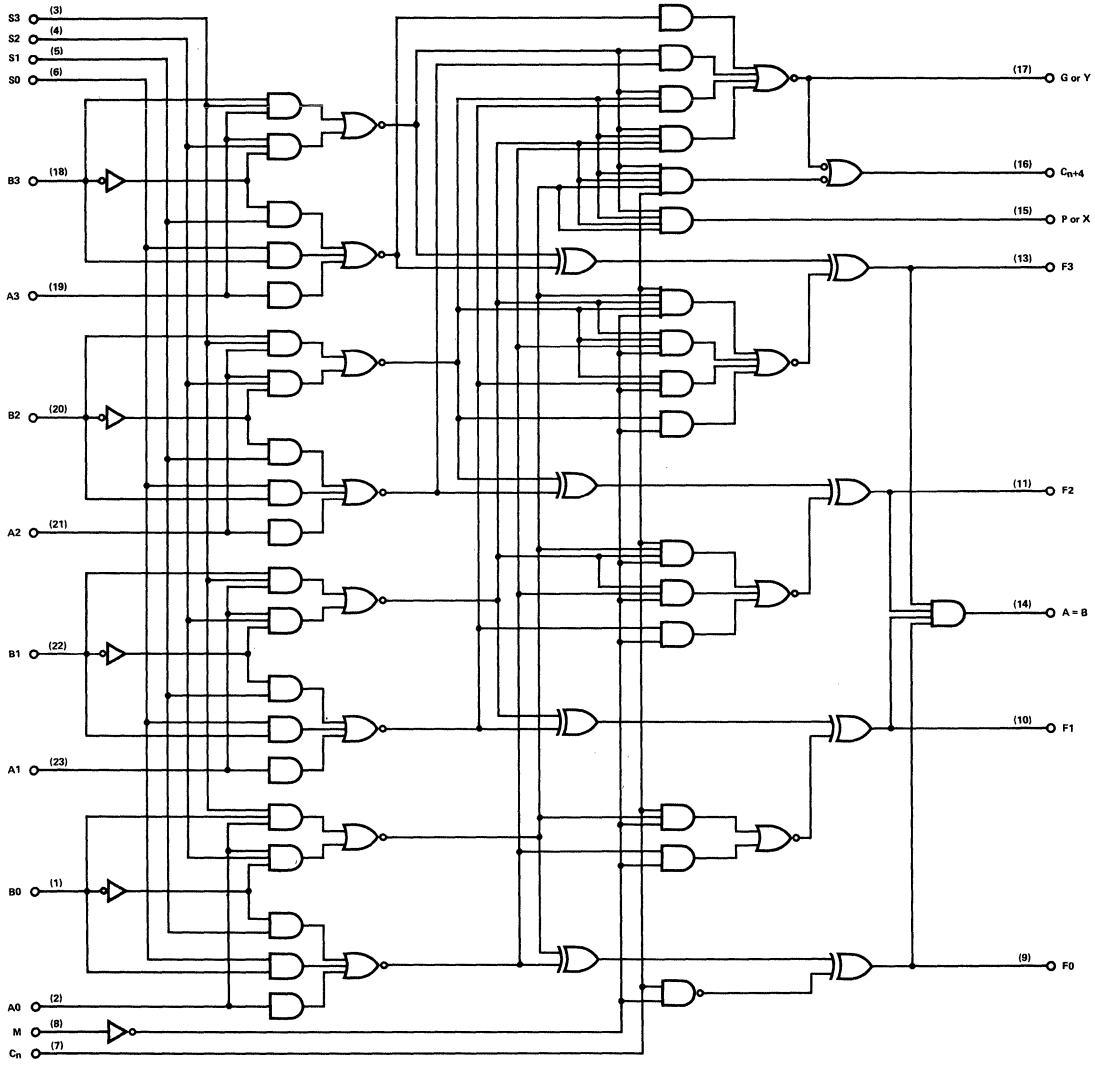


TABLE 2

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L: ARITHMETIC OPERATIONS	
				LOGIC	C_n = L	C_n = H
S3	S2	S1	S0	FUNCTIONS	(NO CARRY)	(WITH CARRY)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = A$\overline{B}$
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

RECOMMENDED OPERATING CONDITIONS

PARAMETER		S54LS181			N74LS181			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current (All outputs except A = B			−400			−400	μA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]		54LS181			74LS181			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400μA	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, V_{OH} = 5.5V			100			100	μA
V_{OL}	Low-level output voltage — All outputs	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V, I_{OL} = 4mA		0.25	0.4				V
			I_{OL} = 8mA					0.35	0.5	
	Output G		I_{OL} = 16mA		0.47	0.7		0.47	0.7	
	Output P		I_{OL} = 8mA		0.35	0.6		0.35	0.5	
	Input — Mode input					0.1			0.1	
I_I	current at max. input voltage — Any A or B input	V_{CC} = MAX,	V_I = 5.5V			0.3			0.3	mA
	Any S input					0.4			0.4	
	Carry input					0.5			0.5	

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]		54LS181			74LS181			UNIT
					MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.7V				20			20	μA
		Any A or B input					60			60	
		Any S input					80			80	
		Carry input					100			100	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4V				−0.36			−0.36	mA
		Any A or B input					−1.08			−1.08	
		Any S input					−1.44			−1.44	
		Carry input					−2			−2	
I_{OS}	Short-circuit output current, any output except A = B[3]		V_{CC} = MAX				−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		20	32		20	34	
				Condition B		21	35		21	37	

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.

NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and A inputs are at 4.5V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5V, all other inputs are grounded.

SWITCHING CHARACTERISTICS [V_{CC} = 5V, T_A = 25°C (C_L = 15pF, R_L = 2kΩ, See Note 4)]

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	C_n	C_{n+4}			18 13	27 20	nS
t_{PLH} t_{PHL}	Any A or B	C_{n+4}	M = 0V, S0 = $\overline{S3}$ = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ mode)		25 25	38 38	nS
t_{PLH} t_{PHL}	Any A or B	C_{n+4}	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		27 27	41 41	nS
t_{PLH} t_{PHL}	C_n	Any F	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		17 13	26 20	nS
t_{PLH} t_{PHL}	Any A or B	G	M = 0V, S0 = $\overline{S3}$ = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ mode)		19 15	29 23	nS
t_{PLH} t_{PHL}	Any A or B	G	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		21 17	32 26	nS
t_{PLH} t_{PHL}	Any A or B	P	M = 0V, S0 = $\overline{S3}$ = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ mode)		20 20	30 30	nS
t_{PLH} t_{PHL}	Any A or B	P	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		20 22	30 33	nS
t_{PLH} t_{PHL}	A_i or B_i	F_i	M = 0V, S0 = $\overline{S3}$ = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ mode)		21 13	32 20	nS
t_{PLH} t_{PHL}	A_i or B_i	F_i	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		21 15	32 23	nS
t_{PLH} t_{PHL}	A_i or B_i	F_i	M = 4.5V (logic mode)		22 19	33 29	nS
t_{PLH} t_{PHL}	Any A or B	A = B	M = 0V, S0 = $\overline{S3}$ = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		33 41	50 62	nS

[1]t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

Load circuit and typical waveforms are shown at front of this section.

LOW POWER SCHOTTKY 50/30 MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

S54LS196
N74LS196
S54LS197
N74LS197

S54LS-A,F,W • N74LS-A,F

DIGITAL 54/74 TTL SERIES

TO BE ANNOUNCED

DESCRIPTION

These high-speed monolithic counters consist of four DC coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter S54/N74LS196 or a divide-by-two and a divide-by-eight counter S54/N74LS197. These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

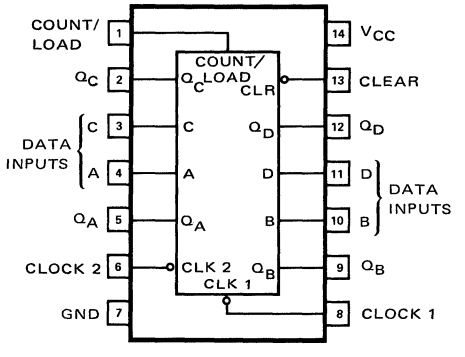
During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 60 milliwatts.

PIN CONFIGURATION (Top View)

A,F,W PACKAGE



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

FEATURES

- PERFORMS BCD, BI-QUINARY, OR BINARY COUNTING
- FULLY PROGRAMMABLE
- FULLY INDEPENDENT CLEAR INPUT
- INPUT CLAMPING DIODES SIMPLIFY SYSTEM DESIGN
- OUTPUT Q_A MAINTAINS FULL FAN-OUT CAPABILITY IN ADDITION TO DRIVING CLOCK-2 INPUT

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS196, S54LS197			N74LS196, N74LS197			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				-400			-400	μA
I_{OL}	Low-level output current				4			8	mA
	Count frequency	Clock-1 input	0		30	0		30	MHz
		Clock-2 input	0		15	0		15	

RECOMMENDED OPERATING CONDITIONS

PARAMETER			S54LS196, S54LS197			N74LS196, N74LS197			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_w	Pulse width	Clock-1 input	10			10			ns
		Clock-2 input	20			20			
		Clear	15			15			
		Load	20			20			
t_{hold}	Input hold time	High-level data	t_w(load)			t_w(load)			ns
		Low-level data	t_w(load)			t_w(load)			
t_{setup}	Input setup time	High-level data	10			10			ns
		Low-level data	15			15			
t_{enable}	Count enable time (See Note 3)		20			20			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]	S54LS196 S54LS197			N74LS196 N74LS197			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max I_{OH} = −400μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 4mA[3]			0.4				V
			V_{IL} = V_{IL} max I_{OL} = 8mA[3]						0.5	
I_I	Input current at maximum input voltage	Data, count/load	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
		Clear, clock 1				0.2			0.2	
		Clock 2 of 'LS196				0.4			0.4	
		Clock 2 of 'LS197				0.2			0.2	
I_{IH}	High-level input current	Data, count/load	V_{CC} = MAX, V_I = 2.7V			20			20	μA
		Clear, clock 1				40			40	
		Clock 2 of 'LS196				80			80	
		Clock 2 of 'LS197				40			40	
		Data, count/load				−0.36			−0.36	
I_{IL}	Low-level output current	Clear	V_{CC} = MAX, V_I = 0.4V			−0.72			−0.72	mA
		Clock 1				−2.4			−2.4	
		Clock 2 of 'LS196				−2.8			−2.8	
		Clock 2 of 'LS197				−1.3			−1.3	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		12	20		12	20	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.
[4] Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.
NOTE4: I_{CC} is measured with all inputs grounded and all outputs open.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	S54/N74LS196			S54/N74LS197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	C_L = 15pF, R_L = 2kΩ	30	40		30	40		MHz
t_{PLH}	Clock 1	Q_A			8	15		8	15	ns
t_{PHL}					13	20		14	21	
t_{PLH}	Clock 2	Q_B			16	24		12	19	ns
t_{PHL}					22	33		23	35	
t_{PLH}	Clock 2	Q_C			38	57		34	51	ns
t_{PHL}					41	62		42	63	
t_{PLH}	Clock 2	Q_D			12	18		55	78	ns
t_{PHL}					30	45		63	95	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D			20	30		18	27	ns
t_{PHL}					29	44		29	44	
t_{PLH}	Load	Any			27	41		26	39	ns
t_{PHL}					30	45		30	45	
t_{PHL}	Clear	Any			34	51		34	51	ns

[1] f_{max} ≡ maximum input count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output.

Load circuit and typical waveforms are shown at the front of this section.

signetics

LOW POWER SCHOTTKY DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

S54LS251-B,F,W • N74LS251-B,F

TO BE ANNOUNCED

DIGITAL 54/74 TTL SERIES

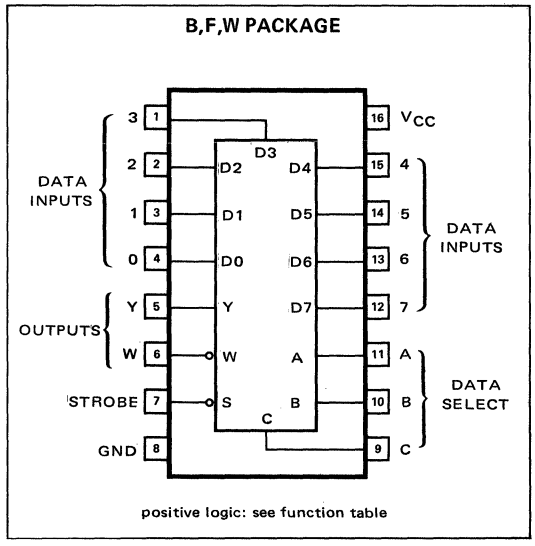
S54LS251 N74LS251

DESCRIPTION

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

PIN CONFIGURATION (Top View)



FEATURES

- THREE-STATE OUTPUTS INTERFACE DIRECTLY WITH SYSTEM BUS
- PERFORM PARALLEL-TO-SERIAL CONVERSION
- PERMIT MULTIPLEXING FRON N-LINES TO ONE LINE
- COMPLEMENTARY OUTPUTS PROVIDE TRUE AND INVERTED DATA
- FULLY COMPATIBLE WITH MOST TTL AND DTL CIRCUITS

FUNCTION TABLE

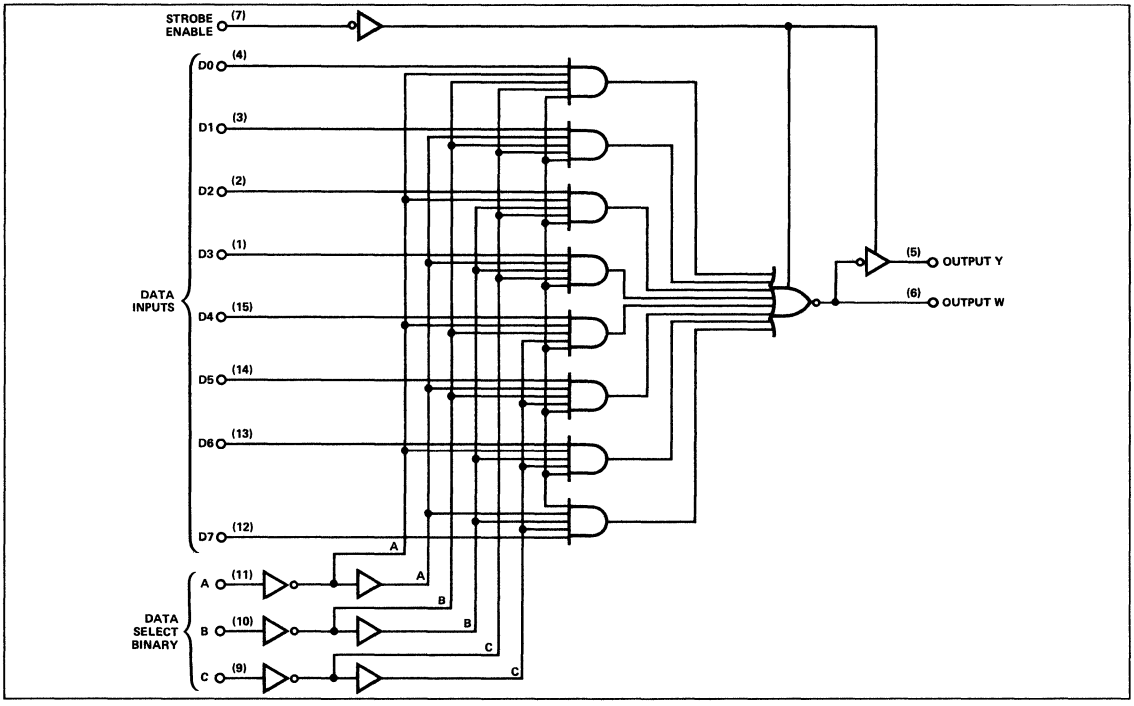
INPUTS		OUTPUTS
SELECT C B A	STROBE S	Y W
X X X	H	Z $\overline{Z}$
L L L	L	D0 $\overline{D0}$
L L H	L	D1 $\overline{D1}$
L H L	L	D2 $\overline{D2}$
L H H	L	D3 $\overline{D3}$
H L L	L	D4 $\overline{D4}$
H L H	L	D5 $\overline{D5}$
H H L	L	D6 $\overline{D6}$
H H H	L	D7 $\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54LS251			74LS251			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]	54LS251			74LS251			UNIT
			MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = MAX	2.5	3.4		2.7	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_O = 2.7V			20			20	μA
		V_{IH} = 2V V_O = 0.4V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, Condition A		6.1	10		6.1	10	mA
		See Note 3 Condition B		7.1	12		7.1	12	

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
A. Strobe grounded.
B. Strobe at 4.5V.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C	Y	C_L = 15pF, R_L = 2kΩ		29	45	ns
t_{PHL}	(4 levels)				28	45	
t_{PLH}	A, B, or C	W			20	33	ns
t_{PHL}	(3 levels)				21	33	
t_{PLH}	Any D	Y			17	28	ns
t_{PHL}					18	28	
t_{PLH}	Any D	W			10	15	ns
t_{PHL}					9	15	
t_{ZH}	Strobe	Y			17	27	ns
t_{ZL}					26	40	
t_{ZH}	Strobe	W			17	27	ns
t_{ZL}					24	40	
t_{HZ}	Strobe	Y	C_L = 5pF, R_L = 2kΩ		30	45	ns
t_{LZ}					15	25	
t_{HZ}	Strobe	W			30	45	ns
t_{LZ}					15	25	

[1] t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level

Load circuit and typical waveforms are shown at the front of this section.

LOW POWER SCHOTTKY DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

S54LS253
N74LS253

S54LS253-B,F,W • N74LS253-B,F

DIGITAL 54/74 TTL SERIES

TO BE ANNOUNCED

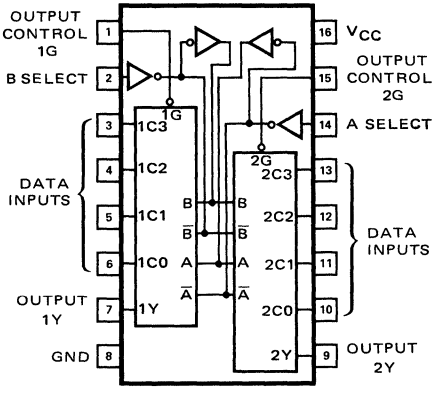
DESCRIPTION

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

PIN CONFIGURATION (Top View)

B,F,W PACKAGE



positive logic: see function table

FEATURES

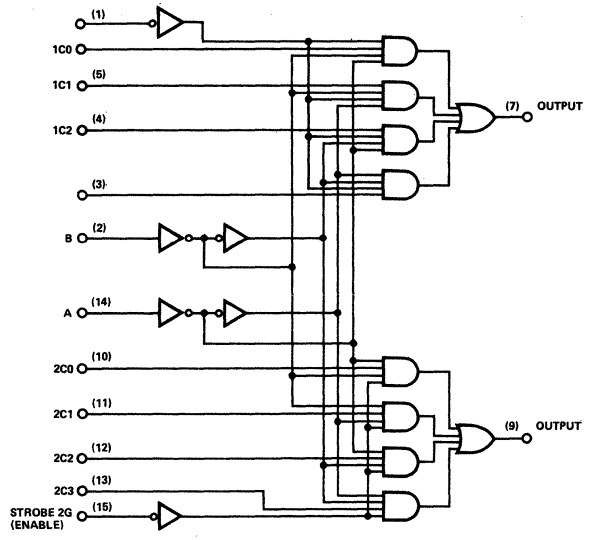
- SCHOTTKY-DIODE-CLAMPED TRANSISTORS
- PERMITS MULTIPLEXING FROM N LINES TO 1 LINE
- PERFORMS PARALLEL-TO-SERIAL CONVERSION
- TYPICAL AVERAGE PROPAGATION DELAY TIMES:
  - DATA INPUT TO OUTPUT – 12ns
  - CONTROL INPUT TO OUTPUT – 16ns
  - SELECT INPUT TO OUTPUT – 21ns
- FULLY COMPATIBLE WITH MOST TTL AND DTL CIRCUITS
- LOW POWER DISSIPATION – 35mW TYPICAL (ENABLED)

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level. L = low level. X = irrelevant. Z = high impedance (off)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]			54LS253			74LS253			UNIT
					MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V,	I_{OL} = 4mA			0.4				V
				I_{OL} = 8mA						0.5	
I_O(off)	Off-State (high-impedance state) output current	V_{CC} = MAX,		V_O = 2.7V			20			20	μA
		V_{IH} = 2V		V_O = 0.4V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				−0.36			−0.36	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	Condition A		7	12		7	12	mA
				Condition B		8.5	14		8.5	14	

[1]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
[2]All typical values are at V_{CC} = 5V, T_A = 25°C.
[3]Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the outputs open under the following conditions:
A. All inputs grounded.
B. Output control at 4.5V, all inputs grounded.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54LS253			74LS253			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

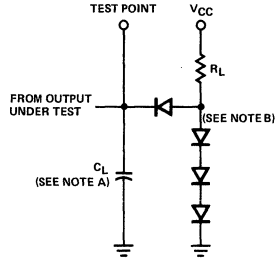
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15pF, R_L = 2kΩ		11	18	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			20	30	ns
t_{PHL}					21	32	
t_{ZH}	Output	Y			11	18	ns
t_{ZL}	Control				15	23	
t_{HZ}	Output	Y	C_L = 5pF, R_L = 2kΩ		27	41	ns
t_{LZ}	Control				12	19	

[1] t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level

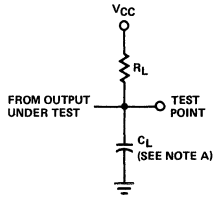
Load circuit and typical waveforms are shown at the front of this section.

TEST CIRCUITS

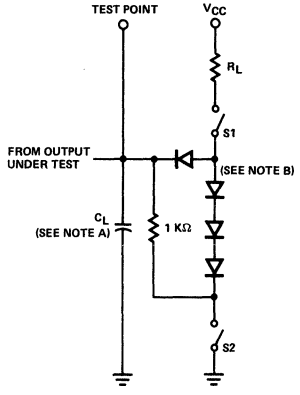
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



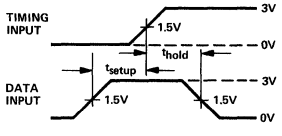
NOTES

A. C_L includes probe and jig capacitance.

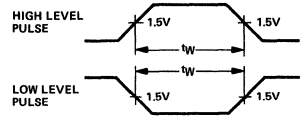
B. All diodes are 1N916 or 1N3064.

WAVEFORMS

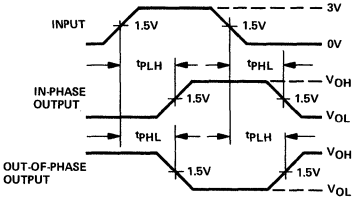
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



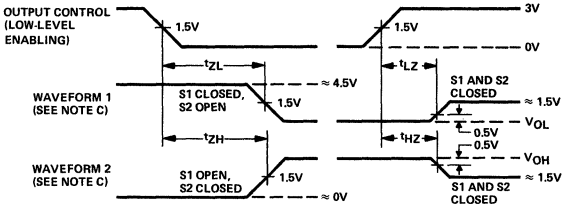
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\Omega$ and:
For Series 54/74, $t_r \leq 7$ ns, $t_f \leq 7$ ns;
For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

DESCRIPTION

The S54S182 and N74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

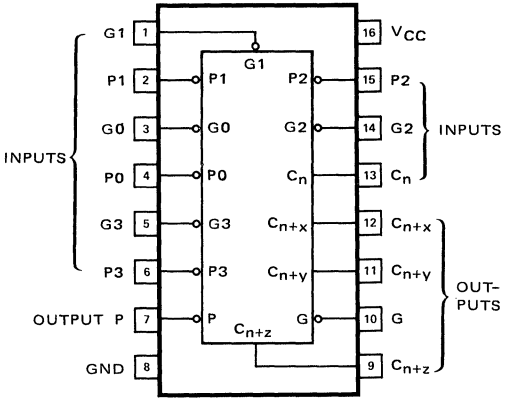
When used in conjunction with the '181, 'LS181, or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '182 or 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '182 or 'S182 circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the '181, 'LS181, and 'S181 ALU's are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the '181, 'LS181, and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 'S182 are:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0 C_n$$
$$C_{n+y} = \overline{G}_1 + \overline{P}_1 \overline{G}_0 + \overline{P}_1 \overline{P}_0 C_n$$
$$C_{n+z} = \overline{G}_2 + \overline{P}_2 \overline{G}_1 + \overline{P}_2 \overline{P}_1 \overline{G}_0 + \overline{P}_2 \overline{P}_1 \overline{P}_0 C_n$$
$$\overline{G} = \overline{G}_3 (\overline{P}_3 + \overline{G}_2)(\overline{P}_3 + \overline{P}_2 + \overline{G}_1)(\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$$
$$\overline{P} = \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{P}_0$$

PIN CONFIGURATION (Top View)

B,F,W, PACKAGE



logic: see description

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54S182			74S182			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER			TEST CONDITIONS[1]	54S182			74S182			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	C_N input	V_{CC} = MAX, V_I = 2.7V			50			50	μA
		P3 input				100			100	
		P2 input				150			150	
		P0, P1, or G3 input				200			200	
		G0 or G2 input				350			350	
		G1 input				400			400	
I_{IL}	Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.5V			−2			−2	mA
		P3 input				−4			−4	
		P2 input				−6			−6	
		P0, P1, or G3 input				−8			−8	
		G0 or G2 input				−14			−14	
		G1 input				−16			−16	
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5V, See Note 3		35			35		mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		69	99		69	109	mA

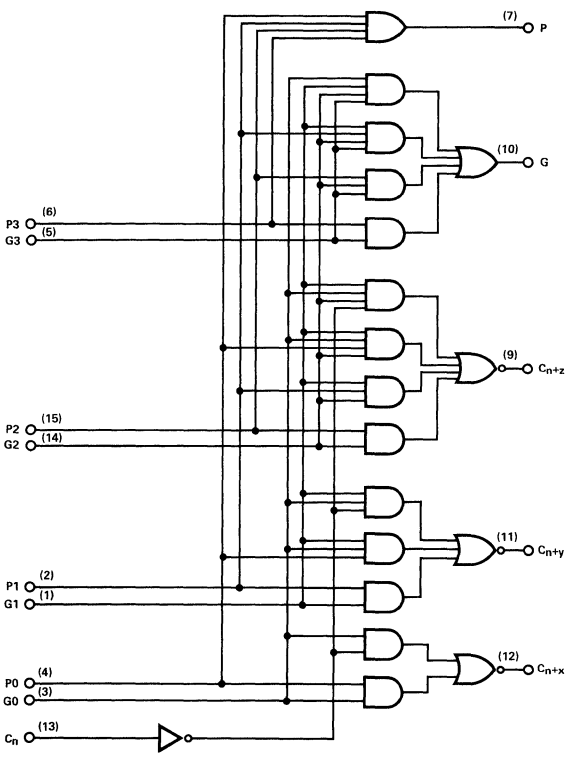
[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
[2] All typical values are at V_{CC} = 5V, T_A = 25°C.
[3] Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

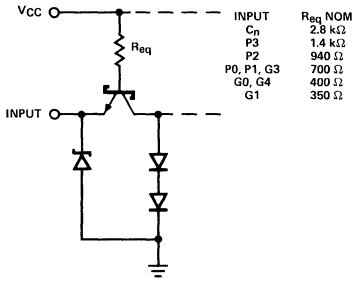
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	C_L = 15pF, R_L = 280Ω		4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	G0, G1, G2, G3, P1, P2, or P3	G			5	7.5	ns
t_{PHL}					7	10.5	
t_{PLH}	P0, P1, P2, or P3	P			4.5	6.5	ns
t_{PHL}					6.5	10	
t_{PLH}	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6.5	10	ns
t_{PHL}					7	10.5	

[1] t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

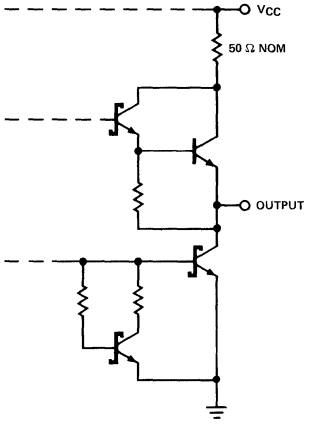
FUNCTIONAL BLOCK DIAGRAM AND SCHEMATICS OF INPUTS AND OUTPUTS



EQUIVALENT OF EACH INPUT

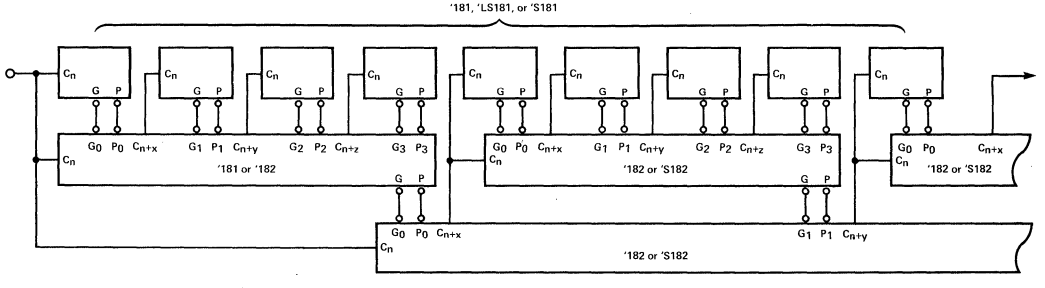


TYPICAL OF ALL OUTPUTS



TYPICAL APPLICATION DATA

64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS



A and B inputs and F outputs of S54/74S181 are not shown.

Load circuit and typical waveforms are shown at the front of this section.

signetics

TTL 256X1 RAM
N74S200 TRI-STATE
N74S206 OPEN COLLECTOR

N74S200–B,I • N74S206–B,I

DIGITAL 54/74 TTL SERIES

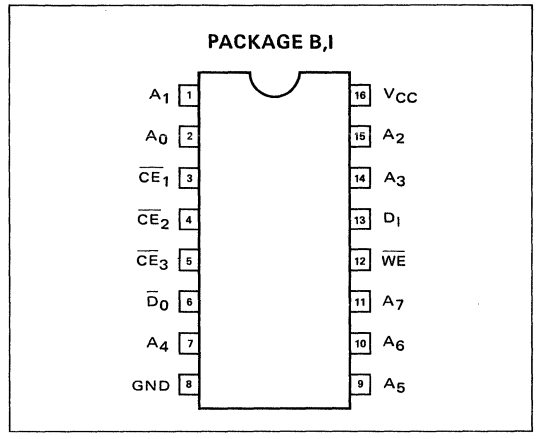
N74S200
N74S206

DESCRIPTION

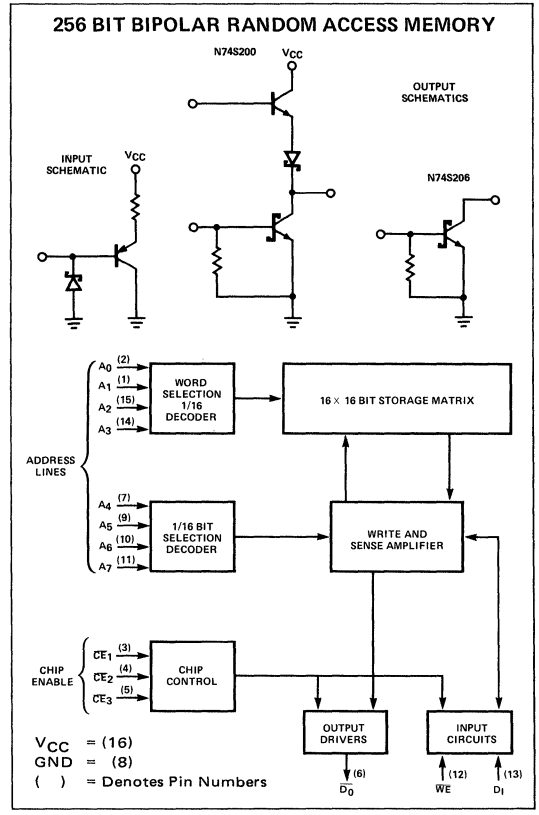
The N74S200 and N74S206 are Schottky clamped TTL, read/write memory arrays organized as 256 words of one bit each. They feature either open collector or tri-state outputs options for optimization of bussed organizations in word expansion. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs, and PNP input transistors which reduce input loading to 25μA for a "1" level, and −100μA for a "0" level.

The additional feature of output blanking during write ($\overline{DO}$ terminal "H" or "Hi-Z" state) permits $\overline{DO}$ and D_I terminals to share a common I/O line to reduce system interconnections. Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as "Cache", buffers, scratch pads, writeable control stores, etc.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



FEATURES

- ORGANIZATION – 256x1
- ADDRESS ACCESS TIME – 30ns, TYPICAL
- WRITE CYCLE TIME – 60ns, MAXIMUM
- POWER DISSIPATION – 1.5mW/BIT, TYPICAL
- INPUT LOADING – –100μA MAXIMUM
- OUTPUT BLANKING DURING WRITE
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTION
  - TRI-STATE (N74S200)
  - OPEN COLLECTOR (N74S206)

APPLICATIONS

BUFFER MEMORY
WRITABLE CONTROL STORE
MEMORY MAPPING
PUSH DOWN STACK
SCRATCH PAD

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power Supply Voltage	7	Vdc
V_{in}	Input Voltage	5.5	Vdc
V_{OH}	High Level Output Voltage (N74S206)	5.5	Vdc
V_O	Off-State Output Voltage (N74S200)	5.5	Vdc
T_A	Operating Temperature Range	0° to 70°	°C
T_{stg}	Storage Temperature Range	-65° to 150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$; $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT	NOTES
V_{IH}	High-level input voltage	V_{CC} = 5.25V		2.0			V	
V_{IL}	Low-level input voltage	V_{CC} = 4.75V				0.85	V	1
V_I	Input clamp voltage	V_{CC} = 4.75V, I_{in} = -18mA			-0.8	-1.2	V	
V_{OH}	High-level output voltage (N74S200)	V_{CC} = 4.75V, V_{IH} = 2.0V, I_{OH} = -10.3mA		2.4			V	1, 5
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.85, I_{OL} = 16mA			0.35	0.45	V	1
I_{OH}	High-level output current (N74S206)	V_{OH} = 2.4V	V_{CC} = 5.25V		1	40	μA	5
		V_{OH} = 5.5V	V_{IH} = 2.0V		1	40	μA	
$I_{O(off)}$	Hi-Z state output current (N74S200)	V_O = 5.5V	V_{CC} = 5.25V		1	40	μA	
		V_O = 0.45V	V_{IH} = 2.0V		-1	-40	μA	
I_I	Input current at V_{in} max	V_{CC} = 5.25V, V_{in} = 5.5V				1	mA	
I_{IH}	High-level input current	V_{CC} = 5.25V, V_{IH} = 2.7V			1	25	μA	
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_{IL} = 0.45V			-10	-100	μA	
I_{OS}	Short-circuit output current (N74S200)	V_{CC} = 5.25V, V_O = 0V		-20		-70	mA	3
I_{CC}	V_{CC} supply current (N74S200)	V_{CC} = 5.25V			80	115	mA	4
	V_{CC} supply current (N74S206)	V_{CC} = 5.25V			80	115	mA	4

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
5. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.

SWITCHING CHARACTERISTICS $0 \leqslant 75°C, 4.75 \leqslant V_{CC} \leqslant 5.25V$

PARAMETER	TEST CONDITIONS		N74S200			N74S206			UNIT	NOTES
	N74S200	N74S206	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} Access time from address	C_L = 15pF			30	50		30	55	ns	B, D, E
t_{PHL} Access time from address	R_L = 400Ω			30	50		30	55	ns	B, D, E
t_{PHL}					–			35		
t_{ZH} Enable time from chip enable					35			–	ns	C, D, E, G
t_{ZL}					35			–		
t_{PLH}					–			25		
t_{HZ} Disable time from chip enable	C_L = 15pF, R_L = 400Ω				20			–	ns	C, D, E, G
t_{LZ}					20			–		
t_{PLH}		C_L = 15pF			–			35		
t_{HZ} Disable time from write enable		R_{L1} = 400Ω			30			–	ns	D, E, G
t_{LZ}		R_{L2} = 1k			30			–		
t_{SR}					–			40		
t_{ZH} Sense-recovery time	C_L = 15pF, R_L = 400Ω				40			–	ns	D, F
t_{ZL}					40			–		
t_w Width of write-enable pulse			40			40			ns	
Setup time:										
Address-to-write-enable			0			0				
t_{setup} Data-to-write enable			0			0			ns	
Chip enable-to-write-enable			0			0				
Hold time:										
Address-from-write-enable			10			10				
t_{hold} Data-from-write-enable			10			10			ns	
Chip enable-from-write-enable			0			0				

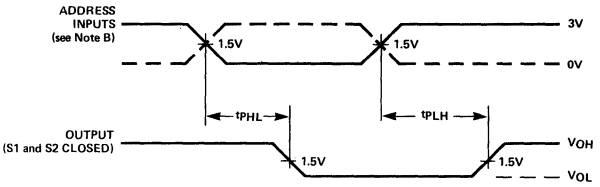
TRUTH TABLE

FUNCTION	$\overline{CE}$*	$\overline{WE}$	OUTPUT
Write (Store D_I Complement)	L	L	Hi-Z (N74S200) H (N74S206)
Read	L	H	Stored Data
Inhibit	H	X	Hi-Z (N74S200) H (N74S206)

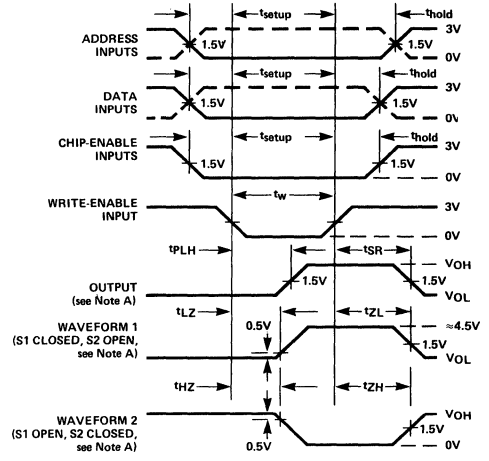
H = high level, L = low level, X = irrelevant
(*)L = all $\overline{CE}$ inputs low; H = one or more $\overline{CE}$ inputs high.

SWITCHING PARAMETER MEASUREMENT INFORMATION

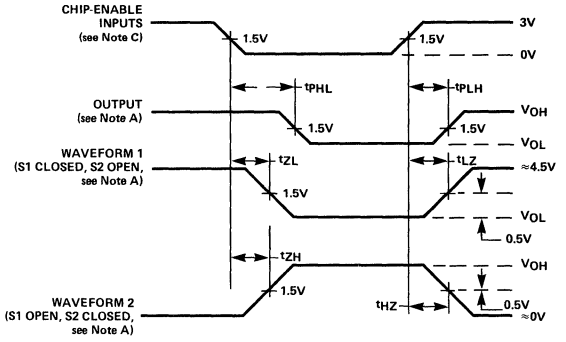
ACCESS TIME FROM ADDRESS



WRITE CYCLE

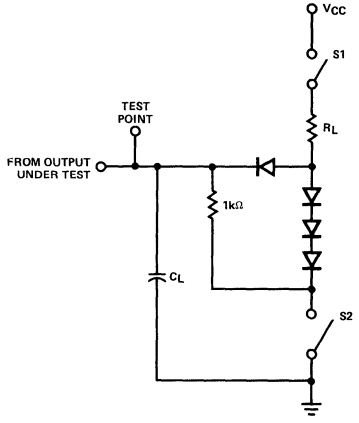


CHIP ENABLE AND DISABLE TIME

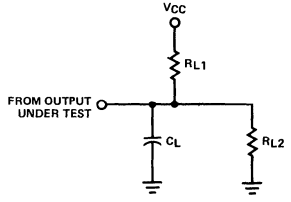


LOAD CIRCUITS

N74S200



N74S206



C_L includes probe and jig capacitance.
All diodes are 1N3064.

NOTES

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write-enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leqslant 2.5$nS, $t_f \leqslant 2.5$nS, PRR $\leqslant$1MHz, and $Z_{out} \approx 50\Omega$.
E. $t_{PLH} \equiv$ propagation delay time, low-to-high-level output; $t_{PHL} \equiv$ propagation delay time, high-to-low-level output.
F. $t_{ZH} \equiv$ propagation delay time, hi-Z to high-level output; $t_{ZL} \equiv$ propagation delay time, hi-Z to low-level output.
G. $t_{HZ} \equiv$ propagation delay time, high-level to hi-Z output; $t_{LZ} \equiv$ propagation delay time, low-level to hi-Z output.

DESCRIPTION

These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped Series 54S/74S TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading as shown under typical application data.

The S54/N74S280 can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although it is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the S54/N74S280 to be substituted for '180 in existing designs to produce an identical function even if 'S280's are mixed with existing '180's.

The S54/N74S280 is fully compatible with most other TTL and DTL circuits. Input buffers are provided so that each input represents only one normalized Series 54S/74S load, and full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normalized Series 54S/74S loads is provided at high logic levels to facilitate connection of unused inputs to used inputs. Typical power dissipation is 335 milliwatts.

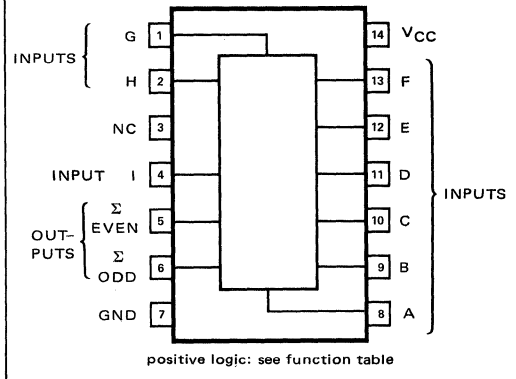
The S54S280 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74S280 is characterized for operation from 0°C to 70°C.

FEATURES

- GENERATES EITHER ODD OR EVEN PARITY FOR NINE DATA LINES
- CASCADABLE FOR n-BITS
- CAN BE USED TO UPGRADE EXISTING SYSTEMS USING MSI PARITY CIRCUITS
- TYPICAL DATA-TO-OUTPUT DELAY OF ONLY 14ns

PIN CONFIGURATION (Top View)

A,F,W, PACKAGE



positive logic: see function table

NC — No internal connection

FUNCTION TABLE

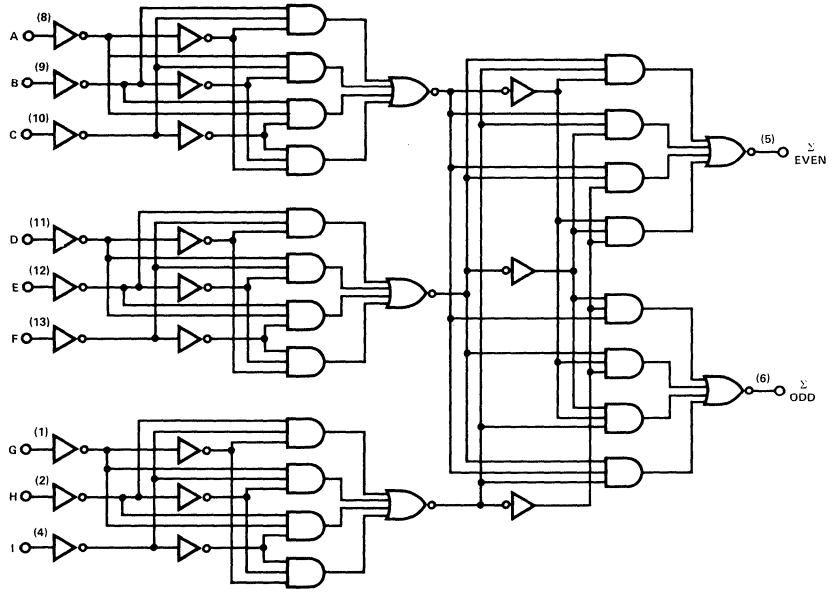
NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

RECOMMENDED OPERATING CONDITIONS

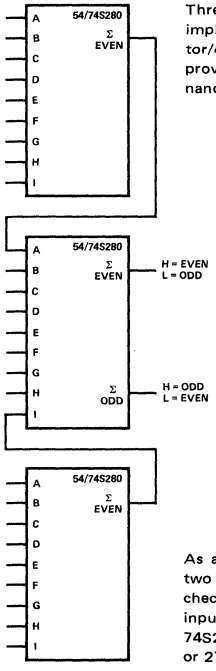
PARAMETER		S54S280			N74S280			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION DATA

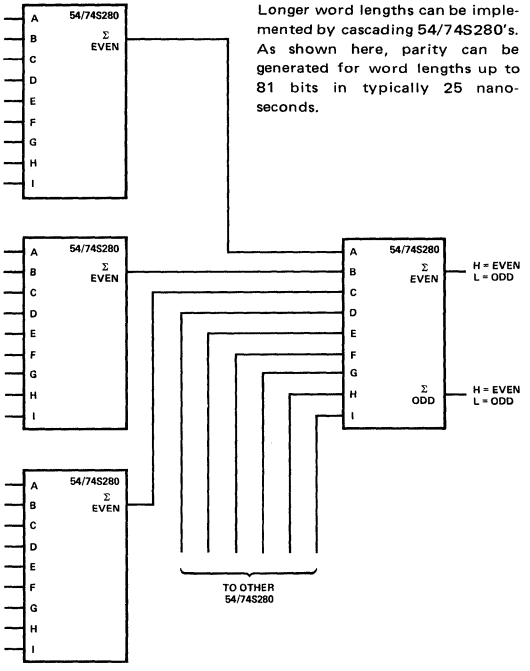
25-LINE PARITY/GENERATOR CHECKER



Three 54/74S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 nanoseconds.

As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (54/74S280) or 3-input (54/74S280) exclusive-OR gate for 18- or 27-line parity applications.

81-LINE PARITY/GENERATOR CHECKER



Longer word lengths can be implemented by cascading 54/74S280's. As shown here, parity can be generated for word lengths up to 81 bits in typically 25 nanoseconds.

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = -18 mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -1 mA	S54S280	2.5	3.4		V
			N74S280	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	S54S280		67	99	mA
			N74S280		67	105	
		V_{CC} = MAX, T_A = 125°C, See Note 2	S54S280W			94	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[2] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[3] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

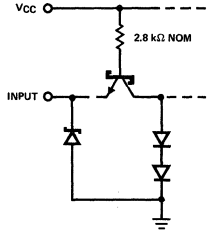
SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15pF, R_L = 180Ω		14	21	ns
t_{PHL}					11.5	18	
t_{PLH}	Data	Σ Odd			14	21	ns
t_{PHL}					11.5	18	

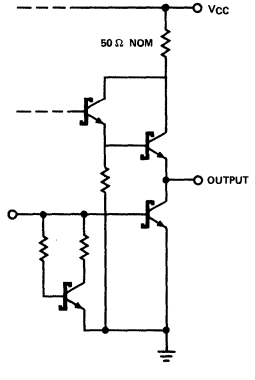
[1] t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output

SCHEMATICS OF INPUTS AND OUTPUTS

EQUIVALENT OF EACH INPUT



TYPICAL OF BOTH OUTPUTS



Load circuit and typical waveforms are shown at the front of this section.

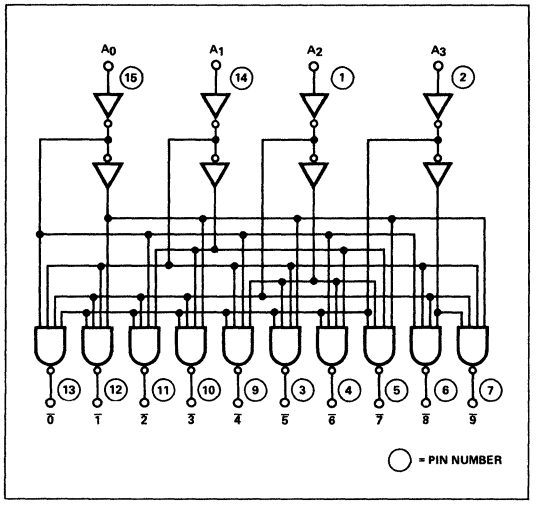
DESCRIPTION

The 9301 is a Multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability.

The 9301 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enables. The logic design of the 9301 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

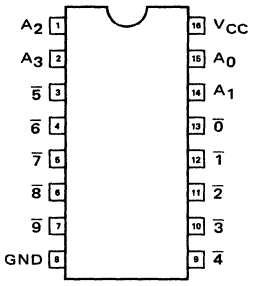
The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 of 8 decoder.

LOGIC DIAGRAM



PIN CONFIGURATION Top View

B,F,W PACKAGE



TRUTH TABLE

A_0	A_1	A_2	A_3	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-Air Temperature Range Unless Otherwise Noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	See 8252 Data Sheet for Pin-for-Pin Replacement				

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

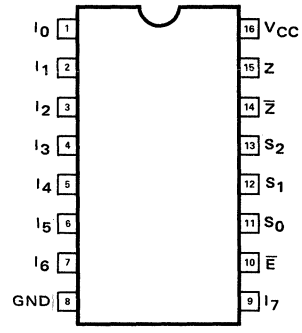
The 9312 is a monolithic, high speed, Eight-Input digital Multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation.

FEATURES

- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMP DIODES

PIN CONFIGURATION Top View

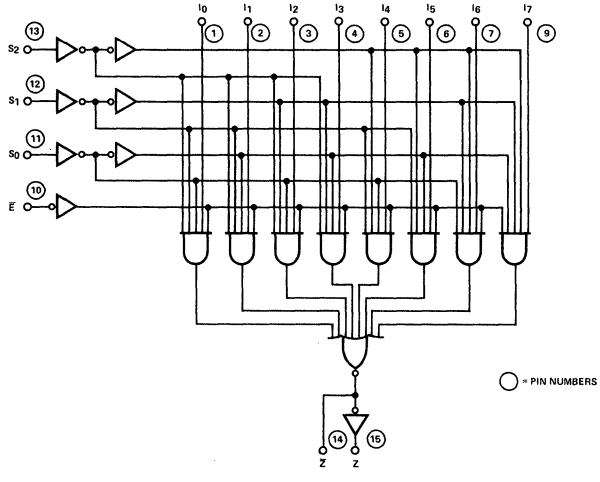
B,F,W PACKAGE



PIN NAMES

S_0, S_1, S_2	Select Inputs
$\overline{E}$	Enable (Active LOW) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Multiplexer Output

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 9312 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select Inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable Input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9312 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one 9312.

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Level does not affect output.

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-Air Temperature Range Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SEE 8230 **Data Sheet for Pin-for-Pin Replacement**				

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

The TTL/MSI 9324 is a High Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than," "greater than" and "equal to." A HIGH level on the enable input forces all three outputs LOW.

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

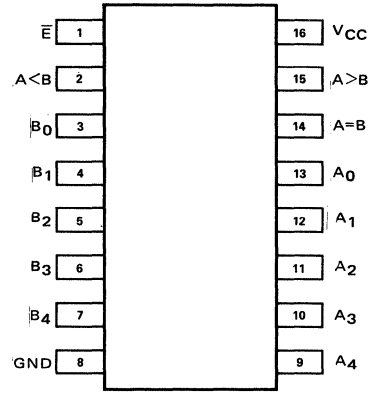
The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

FEATURES

- **THREE SEPARATE OUTPUTS – A < B, A > B, A = B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW LEVEL ENABLE INPUT**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODES**

PIN CONFIGURATION Top View

B,F,W PACKAGE

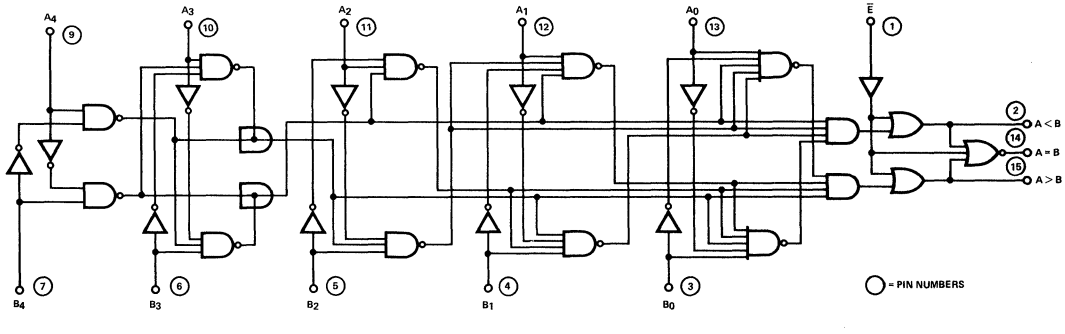


TRUTH TABLE

$\overline{E}$	Ay By	A < B	A > B	A = B
H	X X	L	L	L
L	Word A = Word B	L	L	H
L	Word A > Word B	L	H	L
L	Word B > Word A	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	S9324			N9324			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply Current	4.5	5	5.5	4.75	5	5.25	V
T_A Operating Free-Air Temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS Over Operating Temperature Range Unless Otherwise Noted

PARAMETER	TEST CONDITION	LIMITS			UNIT
		MIN	TYP	MAX	
V_{IH} Input HIGH Voltage	Guaranteed Input HIGH Threshold Voltage for All Inputs	2.0			V
V_{IL} Input LOW Voltage	Guaranteed Input LOW Threshold Voltage for All inputs			0.8	V
V_{CD} Input Clamp Diode Voltage	V_{CC} = MIN, I_{IN} = −12mA, T_A = 25°C			−1.5	V
V_{OH} Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	2.4	3.6		V
V_{OL} Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table		0.2	0.4	V
I_{IH} Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V		20	80	μA
	V_{CC} = MAX, V_{IN} = 5.0V			1.0	mA
I_{IL} Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		−1.92	−3.2	mA
I_{SC} Output Short Circuit Current (I_{OS}) (No More Than 1 Output at a Time)	V_{CC} = MAX, V_{OUT} = 0V	−20	−50	−70	mA
I_{CC} Power Supply Current	V_{CC} = MAX		40	81	mA

SWITCHING CHARACTERISTICS T_A = +25°C, V_{CC} = +5.0V

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	A_2	A > B			19	23	ns
t_{PLH}	A_2	A > B	C_L = 15 pF		23	28	ns
t_{PHL}	A_2	A = B	R_L = 400Ω		35	42	ns
t_{PLH}	A_2	A = B			40	45	ns
t_{PHL}	A_2	A < B			24	29	ns
t_{PLH}	A_2	A < B			29	37	ns
t_{PHL}	$\overline{E}$	A = B			10	16	ns
t_{PLH}	$\overline{E}$	A = B			12	17	ns

DESCRIPTION

The TTL/MSI 9334 is a high speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems.

The TTL/MSI 9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all nonaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the 9334 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

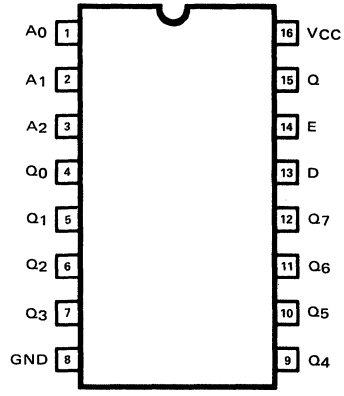
The truth table below summarizes the operations of the 9334.

FEATURES

- **SERIAL TO PARALLEL CAPABILITY**
- **8-BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **INPUT CLAMP DIODES**

PIN CONFIGURATION Top View

B,F,W PACKAGE



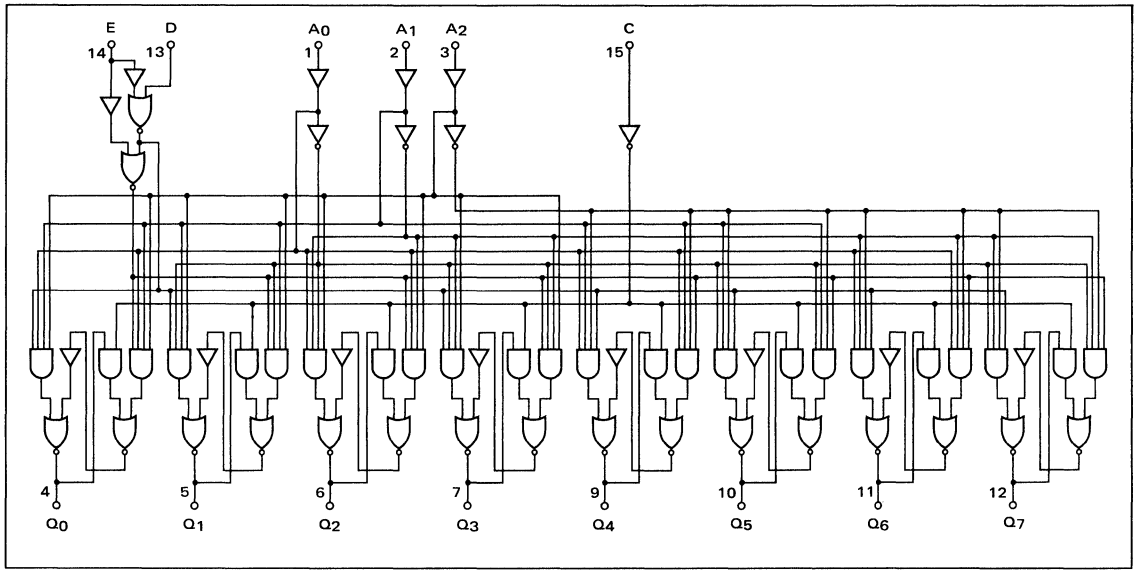
PIN NAMES

A_0, A_1, A_2	Address Inputs
D	Data Input
$\overline{E}$	Enable (Active LOW) Input
$\overline{C}$	Clear (Active LOW) Input
Q_0 to Q_7	Parallel Latch Outputs

RECOMMENDED OPERATING CONDITIONS

PARAMETER		S9334			N9334			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply current	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		70	°C

LOGIC DIAGRAM



TRUTH TABLE

						PRESENT OUTPUT STATES								
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
.	.	.	.	.	.				.					
.	.	.	.	.	.				.					
.	.	.	.	.	.				.					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
.	.	.	.	.	.									
.	.	.	.	.	.									
.	.		.	.	.									
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
O_{N-1} = Previous Output State

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

ELECTRICAL CHARACTERISTICS Over Operating Temperature Range Unless Otherwise Noted

PARAMETER		TEST CONDITIONS	LIMIT			UNIT
			MIN	TYP	MAX	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −720 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	2.4	3.6		V
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 9.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		0.2	0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0			V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs			0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = MIN, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				mA
	A_0, A_1, A_2, D, $\overline{C}$			10	40	
	$\overline{E}$			15	60	
	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current (No more than 1 output at a time)	V_{CC} = MAX, V_{OUT} = 0.0V	−30	−65	−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX		56	86	

SWITCHING CHARACTERISTICS T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMIT			UNIT
			MIN	TYP	MAX	
t_{PLH}	Turn-Off Delay Enable to Output	V_{CC} = 5.0V, C_L = 15pF		19	23	ns
t_{PHL}	Turn-On Delay Enable to Output	Fig. 1 R_L = 680Ω		16	24	ns
t_{PLH}	Turn-Off Delay Data to Output	V_{CC} = 5.0V, C_L = 15pF		28	35	ns
t_{PHL}	Turn-On Delay Data to Output	Fig. 2 R_L = 680Ω		16	24	ns
t_{PLH}	Turn-Off Delay Address to Output	V_{CC} = 5.0V, C_L = 15pF			35	ns
t_{PHL}	Turn-On Delay Address to Output	Fig. 3 R_L = 680Ω			35	ns
t_{PHL}	Turn-On Delay Clear to Output	V_{CC} = 5.0V, C_L = 15pF Fig. 5 R_L = 680Ω		21	25	ns

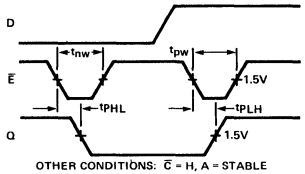
SWITCHING SET-UP REQUIREMENTS T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_s(H)	Set-up Time HIGH Data to Enable			32		ns
t_s(H)	Hold Time HIGH Data to Enable	V_{CC} = 5.0 V, C_L = 15 pF		−18		ns
t_s(L)	Set-up Time LOW Data to Enable	Fig. 4 R_L = 680 Ω		18		ns
t_h(L)	Hold Time LOW Data to Enable			−32		ns
t_s(A-$\overline{E}$)	Set-up Time Address to Enable (See Note 1)	V_{CC} = 5.0 V, C_L = 15 pF Fig. 6 R_L = 680 Ω				ns
t_{pw}($\overline{E}$)	Enable Pulse Width	V_{CC} = 5.0 V, C_L = 15 pF Fig. 1 R_L = 680 Ω		29		ns

NOTES
(1) The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
(2) The shaded areas indicate when the inputs are permitted to change for predictable output performance.

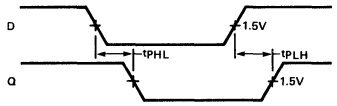
SWITCHING PARAMETER MEASUREMENT INFORMATION

FIGURE 1
TURN-ON & TURN-OFF DELAYS ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



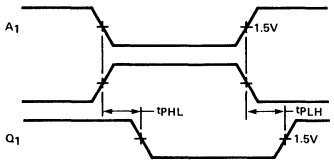
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

FIGURE 2
TURN-ON & TURN-OFF DELAYS DATA TO OUTPUT



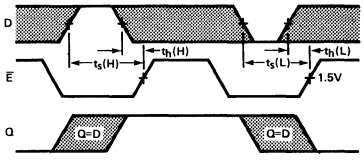
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

FIGURE 3
TURN-ON & TURN-OFF DELAYS ADDRESS TO OUTPUT



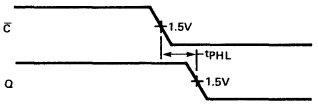
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

FIGURE 4
SET-UP AND HOLD TIME DATA TO ENABLE



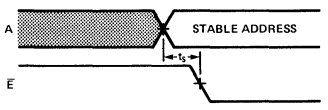
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

FIGURE 5
TURN-ON DELAY CLEAR TO OUTPUT



OTHER CONDITIONS: $\overline{E}$ = H

FIGURE 6
SET-UP TIME ADDRESS TO ENABLE (SEE NOTES 1 & 2)



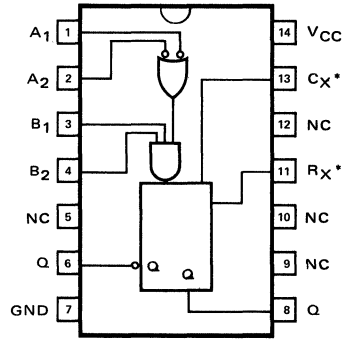
OTHER CONDITIONS: $\overline{C}$ = H

DESCRIPTION

The TTL/Monostable 9601 Retriggerable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9601 has excellent immunity to noise on the V_{CC} and ground lines. The 9601 uses TTL for high speed and high fanout capability.

PIN CONFIGURATION Top View

A,F PACKAGE



*Pins for External Timing
NC — No Internal Connection

ELECTRICAL CHARACTERISTICS Over Recommended Operating Free-Air Temperature Range Unless Otherwise Noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SEE 8T22 Data Sheet for Pin-for-Pin Replacement				

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 82147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All inputs are buffered to represent one normalized 59/79/8200 load. The 82148 encodes eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. The enable input also controls the tri-state outputs, removing the device from the bus when not enabled. For both types, data inputs and outputs are active at the low logic level.

FEATURES (82147)

- ENCODES 10-LINE DECIMAL TO 4-LINE BCD
- TRISTATE OUTPUTS FOR DIRECT BUS INTERFACE
- TYPICAL DATA DELAY — 10ns
- TYPICAL POWER DISSIPATION — 225mW

FEATURES (82148)

- ENCODES 8 DATA LINES TO 3-LINE BINARY (OCTAL)
- TRISTATE OUTPUTS FOR DIRECT BUS INTERFACE
- TYPICAL DATA DELAY — 10ns
- TYPICAL POWER DISSIPATION — 190mW

APPLICATIONS (82147)

KEYBOARD ENCODING

RANGE SELECTION

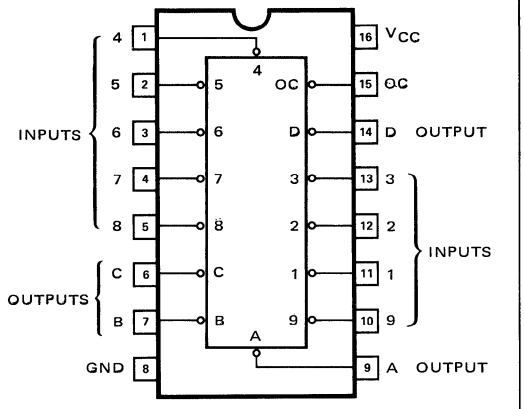
APPLICATIONS (82148)

N-BIT ENCODING

CODE CONVERTERS AND GENERATORS

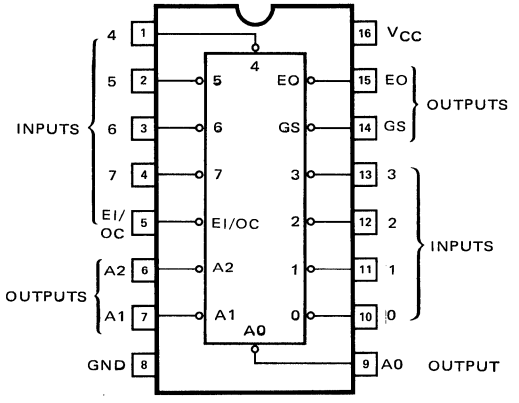
PIN CONFIGURATIONS (Top View)

82147



positive logic: see function table

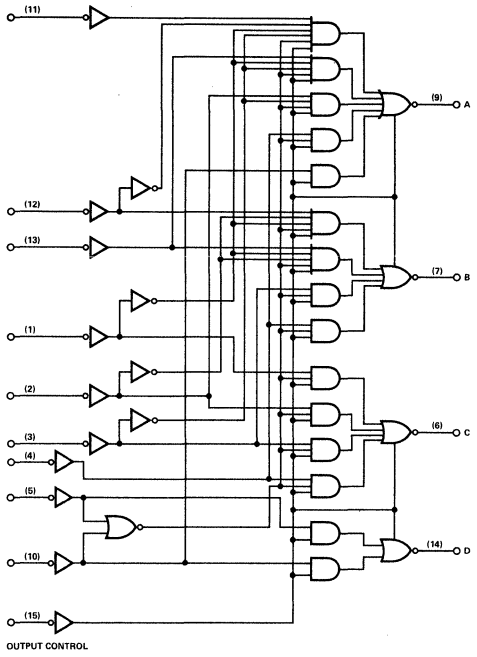
82148



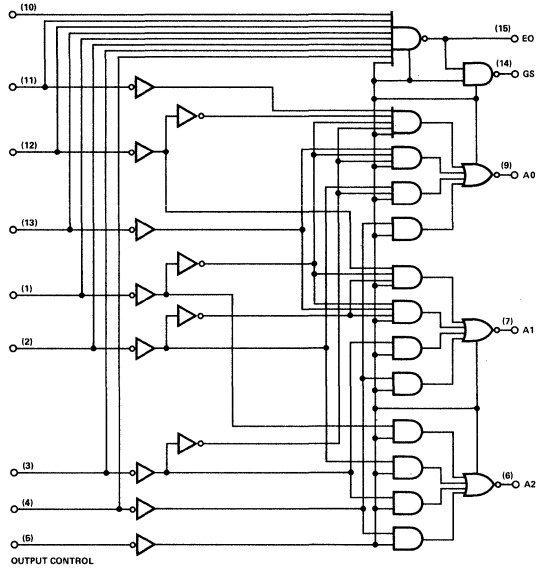
positive logic: see function table

LOGIC DIAGRAMS

82147



82148



FUNCTION TABLE(82147)

INPUTS									OUTPUTS			
O/C	1	2	3	4	5	6	7	8	9	D	C	B	A
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	X	X	X	X	X	X	X	X	L	L	H	H	L
L	X	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	X	L	H	H	H	L	L	L
L	X	X	X	X	X	L	H	H	H	H	L	L	H
L	X	X	X	X	L	H	H	H	H	H	L	H	L
L	X	X	X	L	H	H	H	H	H	H	L	H	H
L	X	X	L	H	H	H	H	H	H	H	H	L	L
L	X	L	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

FUNCTION TABLE(82148)

INPUTS									OUTPUTS				
O/C EI	0	1	2	3	4	5	6	7	A_2	A_1	A_0	G_S	E_O
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER		82147			82148			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−800			−800	μA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Free-air Temperature Range Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS[1]	82147			82148			UNIT
		MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_I Input clamp voltage	V_{CC} = MIN, I_I = -12 mA			-1.5			-1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800μA	2.4	3.3		2.4	3.3		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_O(off) Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IN} = 2V; V_O = 2.7 V			50			50	μA
	V_{CC} = MAX, V_{IN} = 2V; V_O = 0.5 V			-50			-50	μA
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current, 0 input & O/C	V_{CC} = MAX, V_I = 2.4 V			96			40	μA
I_{IH} High-level input current, Any input except 0 & O/C	V_{CC} = MAX, V_I = 2.4 V			40			80	μA
I_{IL} Low-level input current, 0 input & O/C	V_{CC} = MAX, V_I = 0.4 V			-1.6			-1.6	mA
I_{IL} Low-level input current, Any input except 0 & O/C	V_{CC} = MAX, V_I = 0.4 V			-1.6			-3.2	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX	-35		-85	-35		-85	mA
I_{CC} Supply current	V_{CC} = MAX, Condition 1		65	85		53	73	mA
	See Note 3 Condition 2		53	73		42	62	mA

NOTE 3: For 82147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open, I_{CC} (condition 2) is measured with all inputs and outputs open. For 82148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open. I_{CC} (condition 2) is measured with all inputs and outputs open.

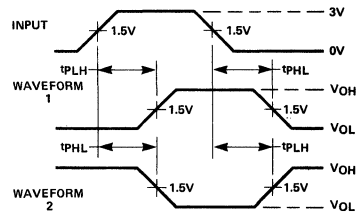
[1] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[2] All typical values are at V_{CC} = 5 V, T_A = 25°C.

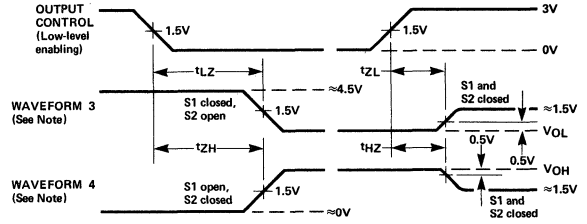
[3] Not more than one output should be shorted at a time.

SWITCHING PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTE
Waveform 3 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 4 is for an output with internal conditions such that the output is high except when disabled by the output control.

82147 SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	Waveform 1	C_L = 15 pF, R_L = 400 Ω		9	14	ns
t_{PHL}						7	11	
t_{PLH}	Any	Any	Waveform 2			13	19	ns
t_{PHL}						10	15	
t_{HZ}	OC	Any	Waveform 4	See Parameter Measurement Information				ns
t_{LZ}	OC	Any	Waveform 3					ns
t_{ZH}	OC	Any	Waveform 4					ns
t_{ZL}	OC	Any	Waveform 3					ns

82148 SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	0 thru 7	A0, A1, or A2	Waveform 1	C_L = 15 pF, R_L = 400 Ω		10	15	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	A0, A1, or A2	Waveform 2			13	19	ns
t_{PHL}						10	15	
t_{PLH}	0 thru 7	CO	Waveform 2			6	10	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	GS	Waveform 1			14	21	ns
t_{PHL}						12	18	
t_{PLH}	EI	A0, A1, or A2	Waveform 1	See Parameter Measurement Information		10	15	ns
t_{PHL}						10	15	
t_{PLH}	EI	GS	Waveform 1			8	12	ns
t_{PHL}						10	15	
t_{PLH}	EI	EO	Waveform 1			8	13	ns
t_{PHL}						13	13	
t_{HZ}	OC	Any	Waveform 4					ns
t_{LZ}	OC	Any	Waveform 3					ns
t_{ZH}	OC	Any	Waveform 4					ns
t_{ZL}	OC	Any	Waveform 3					ns

DESCRIPTION

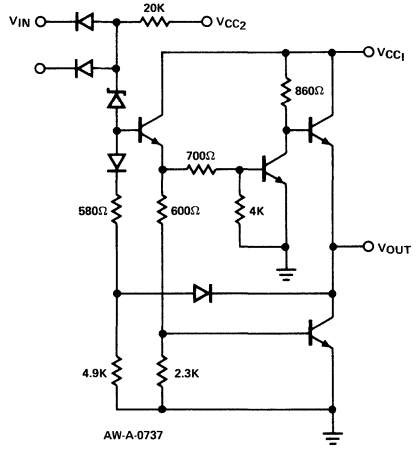
The 8T18 is a Dual 2-Input NAND Interface Gate. It is typically used as a high to low voltage translator which provides translation from up to 30-volt logic levels to standard logic levels of 5 volts.

The basic gate operates from two power supplies. The input structure functions from a high voltage supply V_{CC2}, between 20V and 30V and the second stage transistors and output structure operate from a standard 5V power supply, V_{CC1}.

The high "0" level input threshold (guaranteed at 6.5V) makes the 8T18 very attractive for noisy systems applications such as industrial interfaces.

The output structure features active pull-up and pull-down, providing a low impedance driving source in both "1" and "0" output states. This configuration is particularly suited for driving the high capacitance loads encountered in high fan-out and line driving applications.

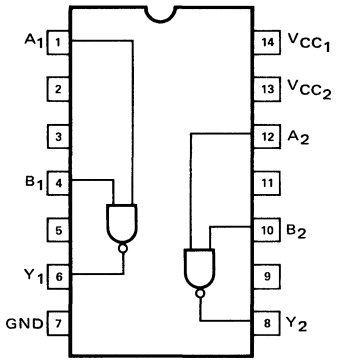
CIRCUIT SCHEMATIC



NOTE: ½ of unit shown. Component values are typical.

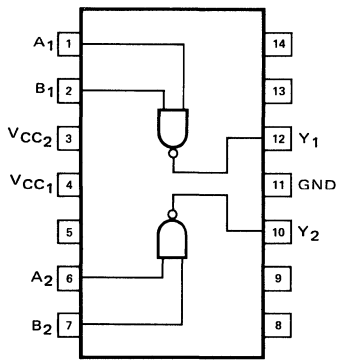
PIN CONFIGURATIONS (Top View)

A, F PACKAGE



AB=$\overline{Y}$

W PACKAGE



AB=$\overline{Y}$

DC ELECTRICAL CHARACTERISTICS Over Recommended Operating Temperature and Voltage

PARAMETER	TEST CONDITIONS					LIMITS			UNIT
	V_{CC1}	V_{CC2}	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	MIN	TYP	MAX	
"1" Output Voltage[7]	4.75V	24.0V	6.5V		-225μA	3.4			V
"0" Output Voltage[8]	4.75V	20.0V	9.0V	9.0V	7.2mA			0.35	V
"0" Input Current	5.25V	24.0V	0.35V	30V					
"1" Input Current	5.0 V	24.0V	30V	0V					
Power Consumption (per gate)									
V_{CC1} Output "0"	5.25V	24.0V						44	mW
V_{CC1} Output "1"	5.25V	24.0V	0V					1	mW
V_{CC2} Output "0"	5.25V	24.0V						39	mW
V_{CC2} Output "1"	5.25V	24.0V	0V					38	mW
Input Voltage Rating			100μA	0V		50			V
Output Short Circuit Current			0V		0V		-75		mA

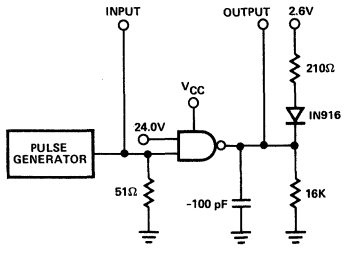
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC1} = 5.0V$, $V_{CC2} = 24.0V$

PARAMETER		TEST CONDITIONS[9]	LIMITS			UNIT
			MIN	TYP	MAX	
t_{on}	Turn-On Delay	$R_L = 210\ \Omega$		27	40	ns
t_{off}	Turn-Off Delay	$C_L = 100$ pF		18	35	ns

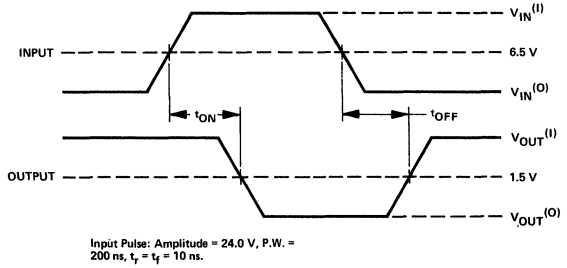
NOTES
1. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" level — "1", "DOWN" level — "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Detailed test conditions for AC testing.

SWITCHING PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT



TYPICAL WAVEFORM

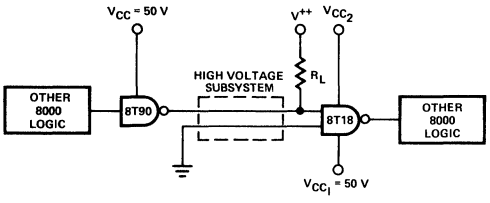


Input Pulse: Amplitude = 24.0 V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

TYPICAL APPLICATION

The 8T18 provides an interface from high level (30-volt) inputs to low level (5-volt) outputs, and thus complements the 8T80 and 8T90. A typical systems application is shown.

The V_{CC2} is returned to a power supply of 20 volts or more. If V^{++} voltage exceeds 30 volts, a series current limiting resistor (to limit current to less than 2 milliamps) or a 20 to 30-volt Zener diode (shunt) must be used. The inputs of the 8T18 are rated at 50 volts reverse breakdown. The threshold voltage of the 8T18 (6.5 volt minimum) is independent of temperature since the various internal junctions are equal in number and opposite in polarity. Thus the 8T18 can be used as an accurate high-level threshold detector.



DESCRIPTION

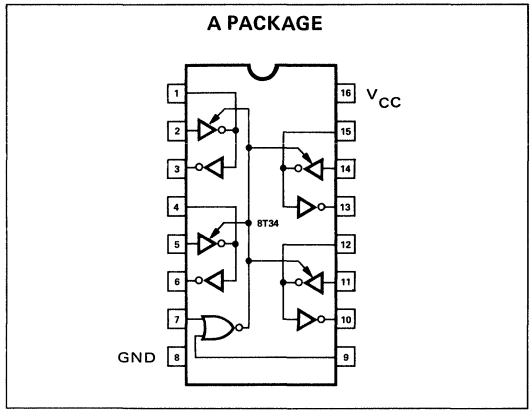
The 8T34 is a quad tri-state transceiver with a common two input disable control for the drivers. Tri-state driver outputs together with low input requirements for the receiver offers extreme versatility in low cost bus organized system.

The tri-state feature of the 8T34 eliminates pull-up resistors but high current bus driving capability allows busses to be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition, the receiver does not load the bus when V_{CC} = 0.

For open collector bus schemes, use the 8T38. In those applications where only a bus receiver is needed, the 8T380 quad bus receiver or the 8T37 hex bus receiver should be considered.

PIN CONFIGURATION (Top View)

A PACKAGE



FEATURES

- RECEIVER HYSTERESIS – 1V TYPICAL
- RECEIVER NOISE IMMUNITY – 2V
- RECEIVER INPUT CURRENT – 20μA TYPICAL (FOR NORMAL V_{CC} AND V_{CC} = 0)
- RECEIVER
  SINK – 16mA AT 0.4V
  SOURCE – 5.2mA AT 2.4V
- DRIVER
  SINK – 50mA AT 0.7V
  SOURCE – 10.4mA AT 2.4V
- DRIVERS HAVE TRI-STATE OUTPUTS
- DRIVES 100Ω TERMINATED BUSSES
- 7400 SERIES COMPATIBLE
- PIN COMPATIBLE WITH DM8834

TRUTH TABLE

MODE	DISABLE A	DISABLE B	DRIVER IN	BUS	RECEIVER OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	0	1
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

ELECTRICAL CHARACTERISTICS (Over Recommended Voltage and Temperature Range)

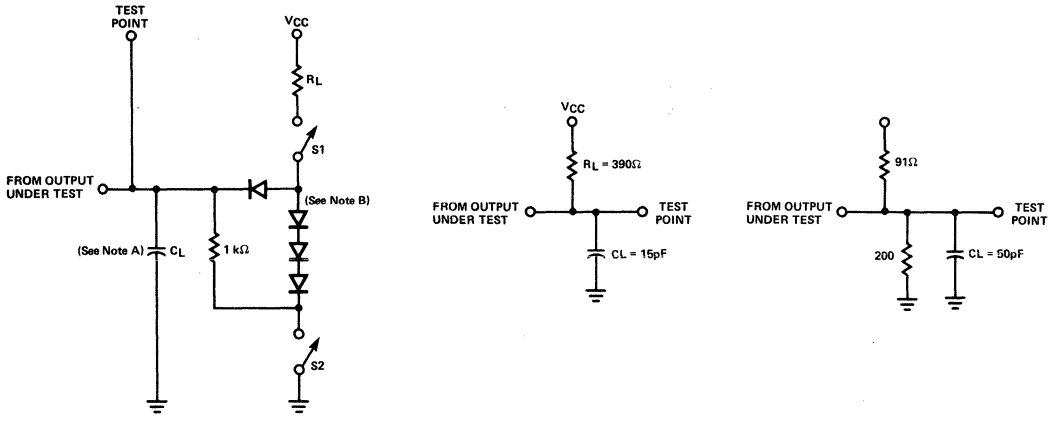
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	"1" Output Voltage						
	Receiver	I_{out} = –5.2mA	V_{CC} = Min.	2.4			V
	Bus	I_{out} = 10.4mA	V_{CC} = Min.	2.4			V
V_{OL}	"0" Output Voltage						
	Receiver	I_{out} = 16mA	V_{CC} = Min.		0.25	0.4	V
	Bus	I_{out} = 50mA	V_{CC} = Min.			0.7	V
V_{IH}	"1" Input Voltage						
	Disable		V_{CC} = Min.	2.0			V
	Driver		V_{CC} = Min.	2.0			V
V_{IL}	"0" Input Voltage						
	Disable		V_{CC} = Min.			0.8	V
	Driver		V_{CC} = Min.			0.8	V
	Bus		V_{CC} = Min.			0.8	V
I_{IH}	"1" Input Current Disable & Driver	V_{out} = 2.4V	V_{CC} = Max.			50	μA
I_{IL}	"0" Input Current Disable & Driver	Disable = V_{out} = 0.4V	V_{CC} = Max.			–1.6	mA
I_{IH}	Max. Bus Current						
	Power On	V_{in} = 4.0V	V_{CC} = Max.		20	100	μA
	Power Off	V_{in} = 4.0V	V_{CC} = 0		20	100	μA
VT+	High Receiver Threshold		V_{CC} = Max.	1.80	2.25	2.50	V
VT–	Low Receiver Threshold		V_{CC} = Min.	1.05	1.30	1.55	V
V_I Max.	Max Input Voltage Disable & Driver	$I_{in} \leqslant$ 1mA				5.5	V
V_{ICL}	Input Clamp Voltage All Inputs	I_{in} = –12mA	V_{CC} = Min.		–1	–1.5	V
I_{OS}	Output Short Circuit Current						
	Receiver	V_{out} = 0V	V_{CC} = Max.	–18	–33	–55	mA
	Driver	V_{out} = 0V	V_{CC} = Max.	–60	–80	–105	mA
I_{CC}	Power Dissipation/ Supply Current	Disable = 0V			210	315	mW
		Driver Input = 2.0V	V_{CC} = Max.		40	60	mA

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{HZ}	Disable to Bus	Load 1, C_L = 15pF Waveform 4	8	15	30	ns
t_{LZ}	Disable to Bus	Load 1, C_L = 15pF Waveform 3	3	9	30	ns
t_{ZH}	Disable to Bus	Load 1, C_L = 50pF Waveform 2	5	10	30	ns
t_{ZL}	Disable to Bus	Load 1, C_L = 50pF Wavefrom 1	8	18	30	ns
t_{PHL}	Driver to Bus	Load 3	4	9	20	ns
t_{PLH}	Driver to Bus	Waveform 5	3	6	15	ns
t_{PHL}	Bus to Receiver	Load 2	5	14	25	ns
t_{PLH}	Bus to Receiver	Waveform 6	12	27	40	ns

SWITCHING PARAMETER MEASUREMENT INFORMATION

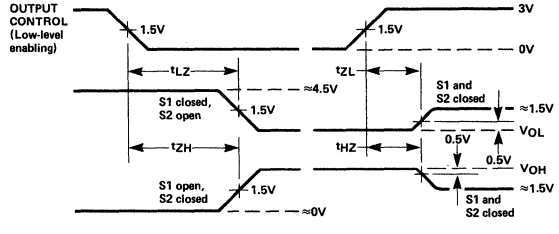
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



LOAD 1 LOAD 2 LOAD 3

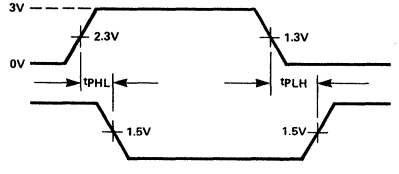
NOTES
A. C_L includes probe and jig capacitance
B. Pin diodes are IN3064

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

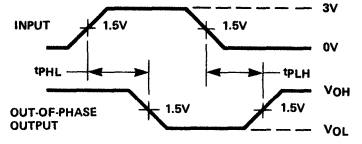


WAVEFORM 3 WAVEFORM 4

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



WAVEFORM 5



WAVEFORM 6

signetics

QUAD BUS TRANSCEIVER (OPEN COLLECTOR) 8T38

8T38-B,F

DIGITAL 8T SERIES INTERFACE TTL/MSI

DESCRIPTION

The 8T38 is a quad bus transceiver with a common two input disable control for the drivers. Open collector driver outputs together with low input requirements for the receivers offer extreme versatility in low cost bus organized systems.

Busses may be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus when $V_{CC} = 0$.

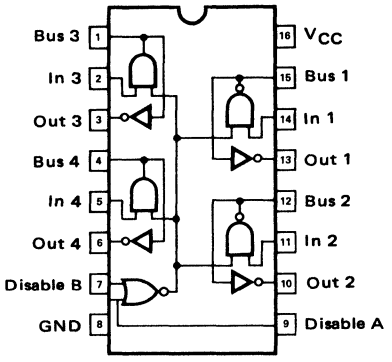
In those applications where only bus receivers are required the 8T380 quad bus receiver or the 8T37 hex bus receiver should be considered.

FEATURES

- **RECEIVER HYSTERESIS – 1V TYPICAL**
- **RECEIVER NOISE IMMUNITY – 2V**
- **RECEIVER INPUT CURRENT – 20μA TYPICAL (FOR NORMAL V_{CC} AND $V_{CC} = 0V$)**
- **RECEIVER**
  SINK – 16mA AT 0.4V
  SOURCE – 5.2mA AT 2.4V
- **DRIVER**
  SINK – 50mA AT 0.7V
- **DRIVERS HAVE OPEN COLLECTOR OUTPUTS**
- **DRIVES 100Ω TERMINATED BUSSES**
- **7400 SERIES COMPATIBLE**
- **PIN COMPATIBLE WITH DM8838**

PIN CONFIGURATION (Top View)

B,F PACKAGE



TRUTH TABLE

MODE	DISABLE A	DISABLE B	DRIVER IN	BUS	RECEIVER OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	0	1
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

AC ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

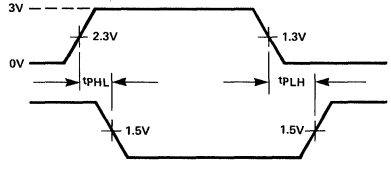
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Disable to Bus	Load 2	11	19	30	ns
t_{PLH}	Disable to Bus	V_{in} = 0V to 3V Measured from V_{in} = 1.5V to Vbus = 1.5V	15	23	35	ns
t_{PHL}	Driver to Bus		5	12	20	ns
t_{PLH}	Driver to Bus		5	12	25	ns
t_{PHL}	Bus to Receiver	Load 1 Waveform 1	5	14	25	ns
t_{PLH}	Bus to Receiver		12	27	40	ns

DC ELECTRICAL CHARACTERISTICS (Over Recommended Voltage and Temperature Range)

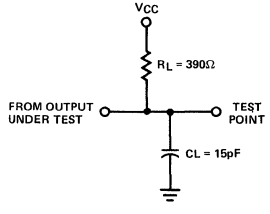
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	"1" Output Voltage						
	Receiver	I_{out} = −400μA	V_{CC} = Min.	2.4			V
V_{OL}	"0" Output Voltage						
	Bus Driver	I_{out} = 50mA	V_{CC} = Min.			0.7	V
	Receiver	I_{out} = 16mA	V_{CC} = Min.		0.25	0.4	V
V_{IH}	"1" Input Voltage						
	Disable		V_{CC} = Min.	2.0			V
	Driver		V_{CC} = Min.	2.0			V
V_{IL}	"0" Input Voltage						
	Disable		V_{CC} = Min.			0.8	V
	Driver		V_{CC} = Min.			0.8	V
I_{IH}	"1" Input Current						
	Disable & Driver	V_{in} = 2.4V	V_{CC} = Max.			50	μA
Bus	Power ON	V_{in} = 4.0V	V_{CC} = Max.		20	100	μA
	Power OFF	V_{in} = 4.0V	V_{CC} = 0		2	100	μA
I_{IL}	"0" Input Current Driver	V_{in} = 0.4V	V_{CC} = Max.			−1.6	mA
VT+	High Receiver Threshold		V_{CC} = Min.	1.80	2.25	2.50	V
VT−	Low Receiver Threshold		V_{CC} = Max.	1.05	1.30	1.55	V
V_{Imax}	Max Input Voltage						
	All Inputs	$I_{in} \leqslant$ 1mA				5.5	V
V_{ICL}	Input Clamp Voltage						
	All Inputs	I_{in} = −12mA	V_{CC} = Min.		−1.0	−1.5	V
I_{OS}	Output Short Circuit						
	Current; Receiver	V_{out} = 0	V_{CC} = Max.	−18	−33	−55	mA
I_{CC}	Power Dissipation/	Disable = 0V,			210	315	mW
	Supply Current	Driver = 2.0V	V_{CC} = Max.		40	60	mA

SWITCHING PARAMETER MEASUREMENT INFORMATION

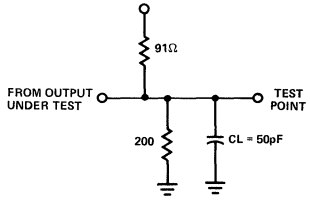
WAVEFORM 1



LOAD CIRCUITS



LOAD 1



LOAD 2

8T363-A

DIGITAL 8T SERIES INTERFACE TTL/MSI

DESCRIPTION

The 8T363 Dual Zero Crossing Detector is an interface circuit incorporating a differential amplifier input and logic gate output. The input amplifier is referenced to zero volts and employs temperature compensation to ensure stable thresholds. The output structure of the 8T363 is compatible with DTL and TTL circuits.

APPLICATIONS

ZERO-CROSSING DETECTOR
HIGH STABILITY ONE-SHOT
BI-DIRECTIONAL ONE-SHOT
FREQUENCY DOUBLER
STABLE-LOW FREQUENCY OSCILLATOR
LINEAR AMPLIFIER
FREQUENCY TO VOLTAGE CONVERTER

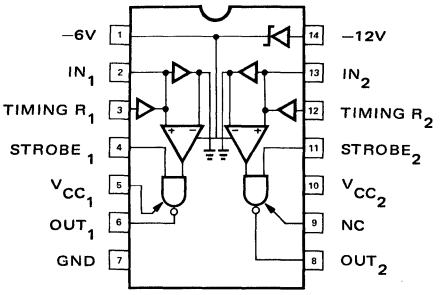
ABSOLUTE MAXIMUM RATINGS

Input Voltage	+7.0V
Output Voltage	+6.0V
V_{CC}	+6.0V
Input Current	±10mA
Output Current	+30, −10mA
Storage Temperature	−65°C to +175°C
Operating Temperature	0°C to +75°C
V−	−7V or −13.5V

Maximum ratings are limiting values above which serviceability may be impaired.

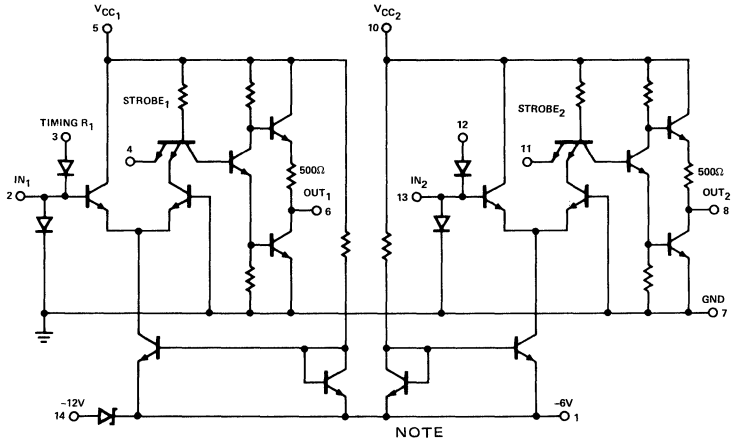
PIN CONFIGURATION (Top View)

A PACKAGE



NC = no connection

CIRCUIT SCHEMATIC



NOTE
Pins 5, 6, 8, and 10 are tied to pin 14 through isolation diodes.

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Temperature — V_{CC} = 5V ±5%, V^- = −6V ±5%, or V^- = −12V ±5%

CHARACTERISTIC	TEST CONDITIONS	MIN	TYP	MAX	UNITS
"1" Output Voltage	V signal = −30mV, I_{out} = −400μA	2.6	3.2		V
"0" Output Voltage	V signal = +30mV, I_{out} = 12.5mA			0.6	V
	I_{out} = 7.5mA			0.4	V
"1" Input Current Strobe	Note 9, V strobe = 2.4V, $V_7 = V_3 = V_{12}$			40	μA
Input High Signal	V signal = 100mV			100	μA
"0" Input Current Strobe	V signal = V_{CC} through 10KΩ resistor, V strobe = 0.6V			−1.4	mA
Input Voltage (Timing R V_F Diode)	$V_7 = V_2 = V_{13}$, I_3 = 1mA, I_{12} = 1mA			1	V
Uncertainty Region-Signal				±30	mV
Icc/Detector	$V_7 = V_3 = V_{12}$, Note 9, T_A = 25°C			6.5	mA
I_{EE}				−13.0	mA

NOTE: Pin 14 must be tied to the most negative voltage used, when V^- = −6V, Pin 14 must be tied to Pin 1.

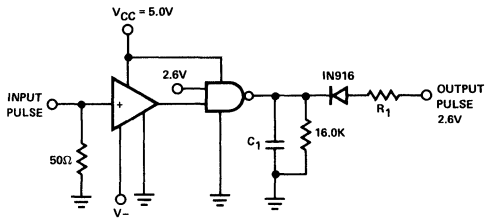
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V, V^- = −6V

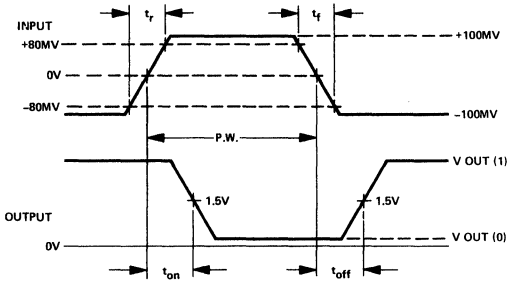
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Turn on Delay	See Test Figure 1, T_A = 25°C			85	ns
Detector Strobe to Output	See Test Figure 2, V signal = V_{CC} through 10KΩ resistor, T_A = 25°C			50	ns
Turn off Delay	See Test Figure 1, T_A = 25°C			65	ns
Detector Strobe to Output	See Test Figure 2, V signal = V_{CC} through 10KΩ resistor, T_A = 25°C			50	ns

NOTES
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition: "UP" level = "1", "DOWN" level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
6. Measurements apply to each gate element independently.

SWITCHING PARAMETER MEASUREMENT INFORMATION

FIGURE 1 – t_{on}, t_{off} DETECTOR INPUTS

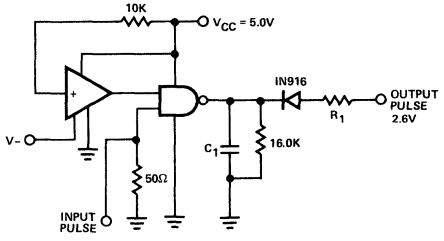


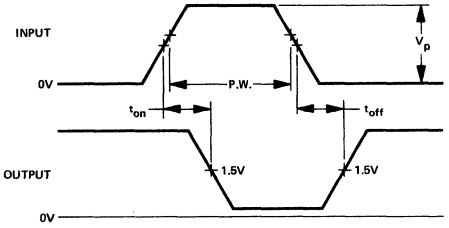


t_{on}	t_{off}
C_1 = 27pF	18pF
R_1 = 210Ω	1.91kΩ

Input Pulse: V_{in}
Pulse Width = 350ns at 50% Points
$t_r = t_f$ = 10ns
Amplitude = ±100mV

FIGURE 2 – t_{on}, t_{off} STROBE TO OUTPUT



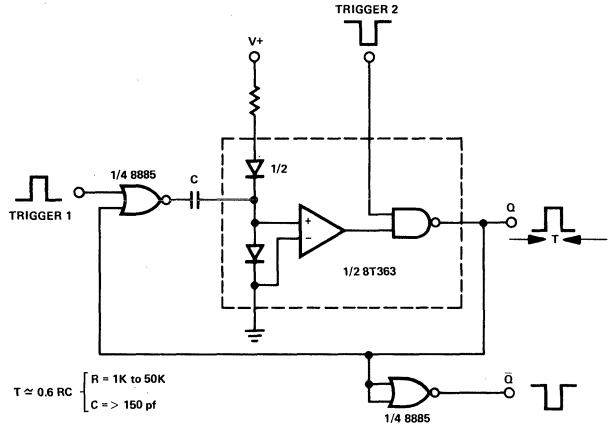


t_{on}	t_{off}
C_1 = 27pF	18pF
R_1 = 210Ω	1.91kΩ

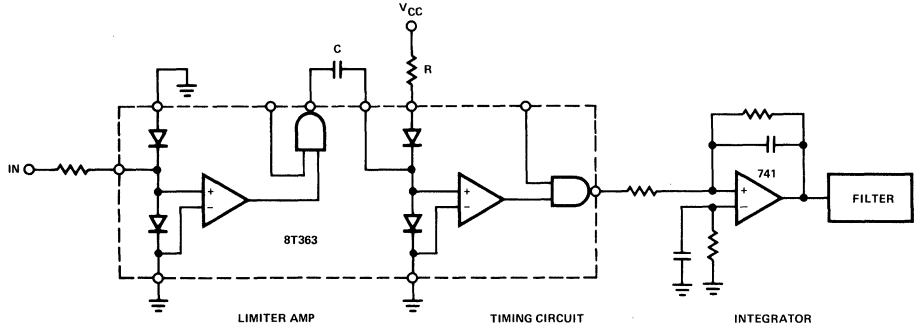
Input Pulse; V_{in}
Pulse Width = 200ns at 50% Points
$t_r = t_f$ (10%–90%) = 10ns
Amplitude V_p = 4.0V

TYPICAL APPLICATIONS

MONOSTABLE MULTIVIBRATOR



FREQUENCY TO VOLTAGE CONVERTER



Sine wave inputs up to approximately 500 kHz are limited, amplified and used to trigger the timing circuit. The timing circuit output is a constant pulse width (pw ≈0.6RC). The constant width pulses are integrated and then filtered to attenuate the remaining high frequency carrier components.

DESCRIPTION

The 82S08 is an ideal device for use in Large Control Stores and MAIN MEMORY. The 82S08 is designed to provide low system power consumption while maintaining fast access times. This has been accomplished by incorporating a "power down" mode. Full-power is applied to all elements of the RAM only when the chip is selected and being addressed. The 82S08 also features low input loading and operates from a single 5.0 V supply.

"ONE LEVEL IN APPEARS AS "ONE" LEVEL OUT"

FEATURES

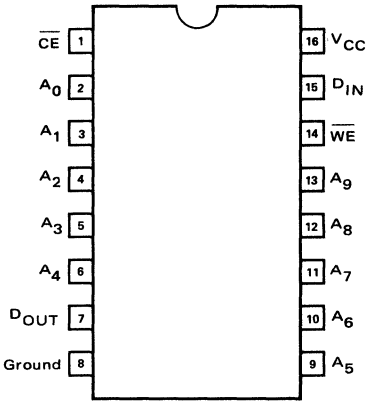
- 1024 X 1 ORGANIZATION
- 55 ns TYPICAL ADDRESS ACCESS TIME
- POWER DOWN MODE FOR MINIMUM POWER
- POWER DISSIPATION – 300 Mw TYPICAL
- 400 uA TYPICAL INPUT LOADING
- OPEN COLLECTOR OUTPUT
- ON-CHIP DECODING
- TTL COMPATIBLE
- 16 PIN DUAL-IN-LINE CERAMIC PACKAGE

APPLICATIONS

BUFFER MEMORY
CONTROL STORE
SCRATCH PAD MEMORY
MAIN MEMORY

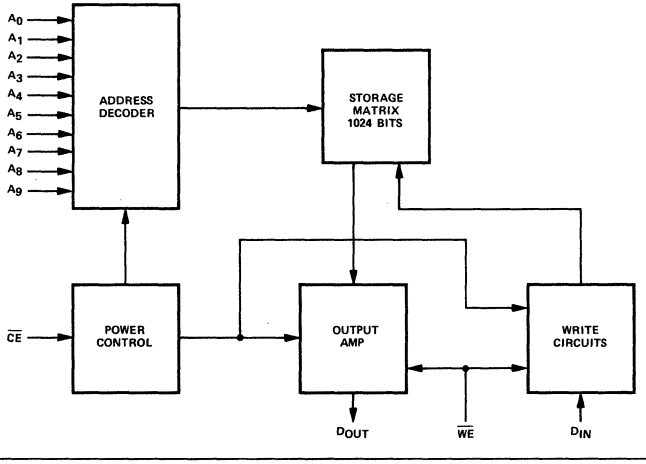
PIN CONFIGURATION

I PACKAGE



THIS PRODUCT AVAILABLE IN 0°C TO 75°C TEMP RANGE ONLY

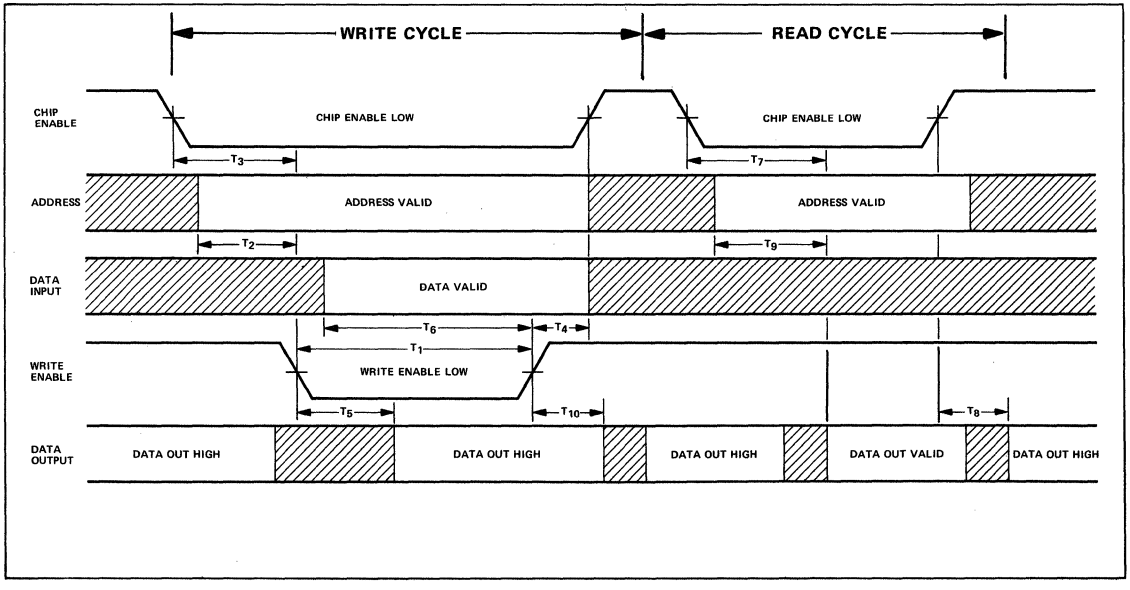
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 0 to 75°C, V_{CC} = 5.0 V ± 5%)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
"O" Input Voltage (V_{IL})				.85	
"I" Input Voltage (V_{IH})		2.0			
"O" Input Current	V_{in} = .45 V, $\overline{CE}$ = "0"			-800	μA
"I" Input Current	V_{in} = 4.5 V, CE = "0"			20	μA
"O" Output Voltage	I_o = 16 MA			.45	V
Output "1" Current	V_{out} = 5.5 V			100	μA
Power Supply Drain "Full Power"	$\overline{CE}$ = "0"		85	120	mA
Power Supply Drain "Powered Down"	$\overline{CE}$ = "1"		50	75	mA
Input Clamp Voltage	I_{in}= -18 mA			-1.2	V
Write Pulse Width	T_1			35	ns
Address Set-Up Time	T_2			40	ns
Chip Enable Set-Up Time	T_3			45	ns
Hold Time ($\overline{CE}$, Address, or Data)	T_4			0	ns
Write Enable to Output Disable Time	T_5			40	ns
Data in Set-Up Time	T_6			40	ns
Chip Enable Access Time	T_7 CL = 30 pf		60	85	ns
Chip Enable Output Disable Time	T_8 CL = 30 pf			40	ns
Address Access Time	T_9 CL = 30 pf		55	80	ns
Write Recovery Time	T_{10} CL = 30 pf			50	ns

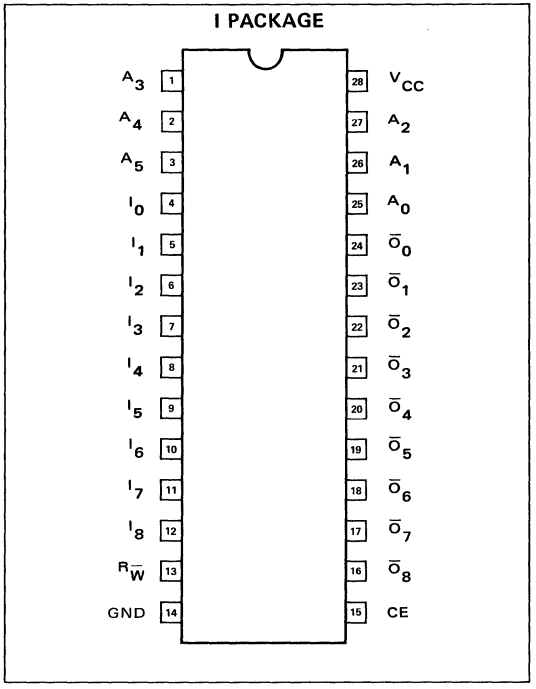
TIMING DIAGRAM



DESCRIPTION

The 82S09 is a 576 bit, TTL compatible, random access memory organized as 64 words by 9 bits per word. It is ideally suited for scratch pad, small buffer, and other applications where the number of words is limited and the number of bits per word is relatively large. The ninth bit provides a parity bit for 8 bits/word systems.

PIN CONFIGURATION



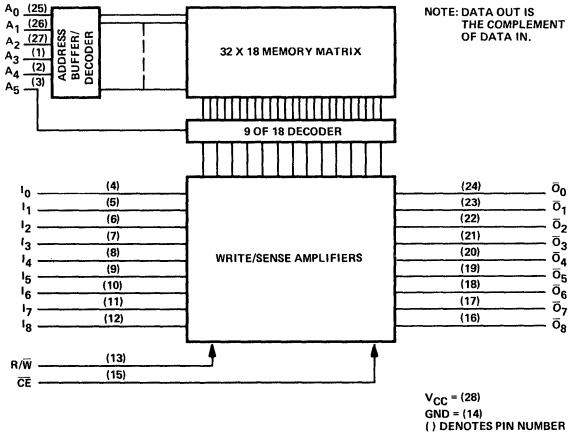
FEATURES

- 64 X 9 ORGANIZATION
- 30 nSEC TYPICAL ACCESS TIME
- 1.5 mW/BIT TYPICAL POWER DISSIPATION
- 100μA INPUT LOAD
- OPEN-COLLECTOR OUTPUT

APPLICATIONS

SCRATCH PAD
BUFFER MEMORIES
CONTROL STORE

BLOCK DIAGRAM



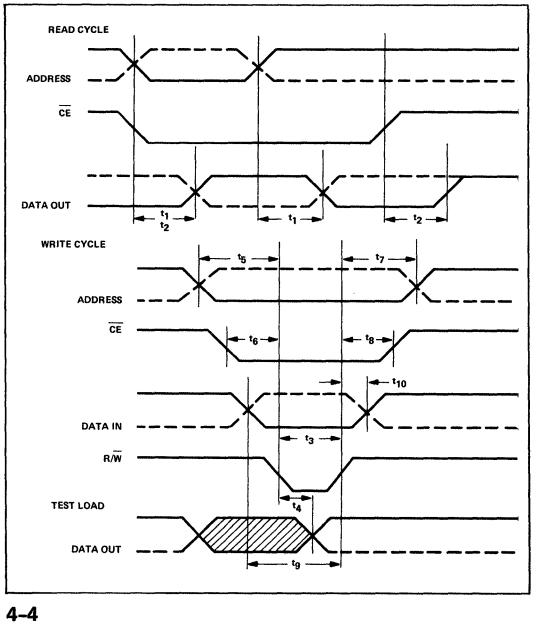
OBJECTIVE ELECTRICAL CHARACTERISTICS $0 \geq T_A \geq 75°C$, $4.75 \geq V_{CC} \geq 5.25$ V

PARAMETER	TEST CONDITION	LIMITS			UNIT
		MIN	TYP	MAX	
"O" Input Current	V_{IN} = 0.45 V			−100	μA
"I" Input Current	V_{IN} = 5.25 V			25	μA
Input Clamp Voltage	I_{IN} = 18 mA			−1.2	V
"O" Input (V_{IL})				0.85	V
"I" Input (V_{IH})		2.0			V
Output Leakage	V_{OUT} = 5.5 V			40	μA
"O" Output Voltage	I_{OUT} = −6.4 mA			0.5	V
Power Supply Current			170	200	mA

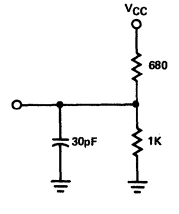
OBJECTIVE SWITCHING CHARACTERISTICS $0 \geq T_A \geq 75°C$, $4.75 \geq V_{CC} \geq 5.25$ V

PARAMETER		TEST CONDITION	LIMITS			UNIT
			MIN	TYP	MAX	
	Access Time					
t_1	Address to Output			35	50	ns
t_2	CE to Output			35	50	ns
t_3	Write Pulse Width		45			ns
t_4	Write Access Time	Data Stable Prior to Write		35	50	ns
t_5/t_6	Address/CE Set-Up		10			ns
t_7/t_8	Address/CE Hold		10			ns
t_9	Data Set-Up		50			ns
t_{10}	Data Hold		5			ns

TIMING DIAGRAM



TEST LOAD



DESCRIPTION

The 82S10/11 is a high speed 1024 bit random access memory organized as 1024 words x 1 bit. With a typical access time of 30 ns, it is ideal for scratch pad applications and for systems requiring very high speed main memory.

Fully TTL compatible, the 82S10/11 requires a single +5 volts power supply and features very low current PNP input structures. This device is available with open collector (82S10) or Tri-State (82S11) outputs and is pin compatible with the Signetics 82S08 "power-down" RAM.

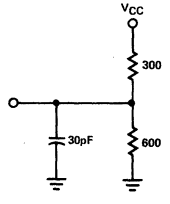
FEATURES

- TTL COMPATIBLE – ALL INPUTS AND OUTPUTS
- 1024 X 1 ORGANIZATION
- 45 ns MAX ACCESS TIME – CHIP ENABLED
- 30 ns MAX CHIP ENABLE ACCESS TIME
- SINGLE +5 VOLT POWER SUPPLY
- LOW INPUT LOADING
- 16 PIN DUAL-IN-LINE PACKAGE

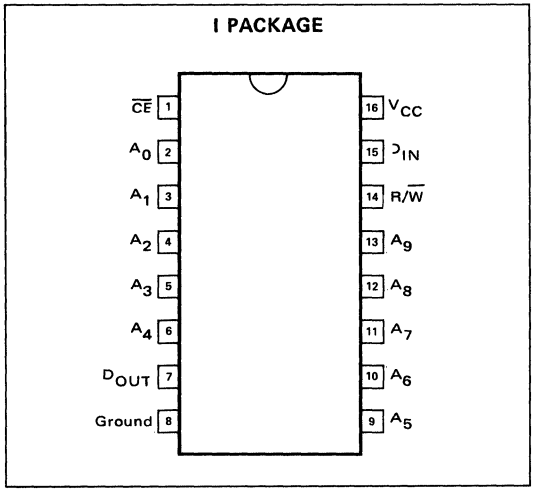
APPLICATIONS

HIGH SPEED MAIN FRAME
CACHE MEMORY
BUFFER STORAGE
WRITEABLE CONTROL STORE

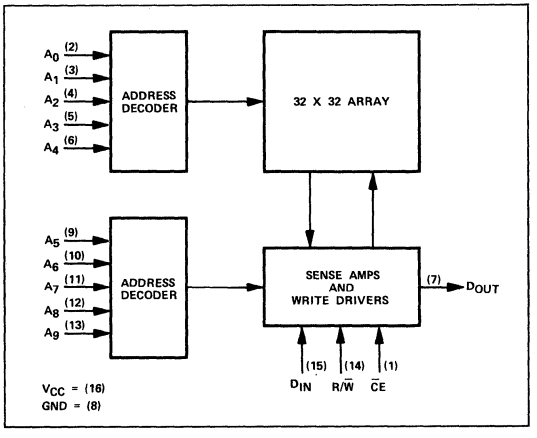
AC TEST LOAD



PIN CONFIGURATION



LOGIC DIAGRAM



TRUTH TABLE

$\overline{CE}$	R/$\overline{W}$	D_I	MODE	OUTPUT	
				82S10	82S11
0	0	0	Write	High	High
0	0	1	Write	High	High
0	1	X	Read	Data	Data
1	X	X	Chip Disabled	1	High "Z"

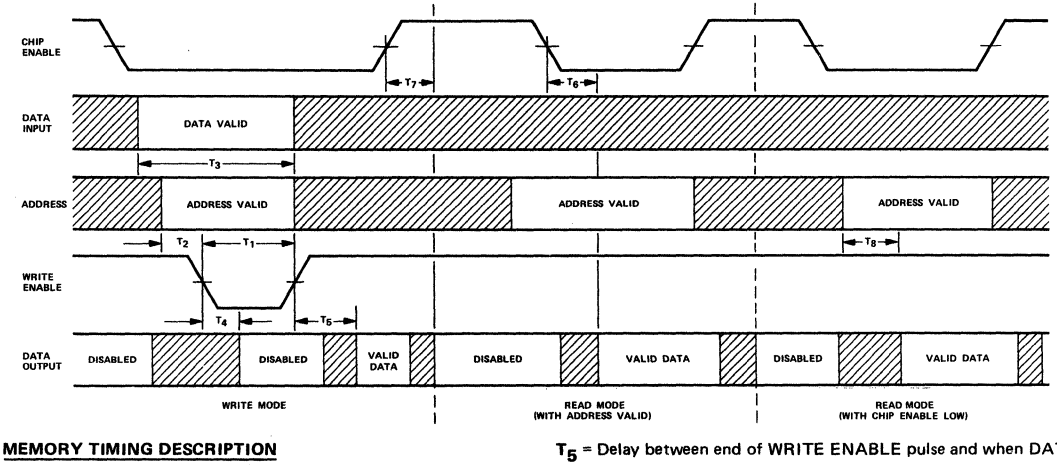
DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$ and $V_{CC} = 5.00V \pm 5\%$)

PARAMETERS	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
"O" Input Current	$V_{in} = 0.45V$		-10	-100	μA
"I" Input Current	$V_{in} = 5.5V$		< 1.0	25	μA
"O" Output Voltage	$I_o = 16$ mA			0.5	V
"I" Output Current (82S11)	$V_{OUT} = 2.4V$			-2	mA
Output Leakage Current (82S10)	$\overline{CE}$ = "1", $V_{OUT} = 5.5V$			40	μA
Output "Off" Current (82S11)	$\overline{CE}$ = "1", $0.45 \leq V_{OUT} \leq 3.5$ V			±60	μA
Power Supply Current	$V_{CC} = 5.25V$		120	160	mA

AC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 75°C$ and $V_{CC} = 5.00V \pm 5\%$)

PARAMETER	SYMBOL (Refer to Timing Diagram)	LIMITS			UNIT
		MIN	TYP	MAX	
Write Enable Pulse Width	T_1		25		ns
Address Set-Up Time	T_2		-15	0	ns
Data In Set-Up Time	T_3		30		ns
Write Enable to Output Disable Time	T_4			30	ns
Write Recovery Time	T_5		17	30	ns
Chip Enable Access Time	T_6		18	30	ns
Chip Enable Output Disable Time	T_7		18	30	ns
Address Access Time	T_8		30	45	ns

TIMING DIAGRAM



MEMORY TIMING DESCRIPTION

T_1 = Width of WRITE ENABLE pulse.

T_2 = Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.

T_3 = Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.

T_4 = Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.

T_5 = Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid - not as shown).

T_6 = Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.

T_7 = Delay between when CHIP ENABLE becomes high and DATA OUTPUT is on off state.

T_8 = Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.

DESCRIPTION

The 82S114 and 82S115 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers. A D-type latch (L) is used to enable the tri-state output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines. In the LATCHED READ mode, after the desired address is applied and both $\overline{CE1}$ and CE2 are enabled, data will enter the output latches following the positive transition of STROBE, and the data out lines will be locked into their last valid state following the negative transition of STROBE. The latches will remain set and the outputs enabled until the chip is disabled and STROBE is brought high.

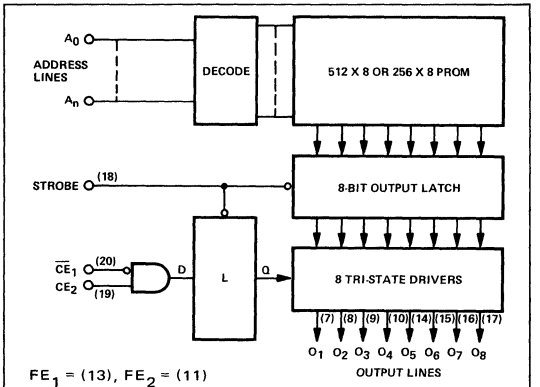
FEATURES

- BUFFERED ADDRESS LINES
- ON-CHIP DECODING
- ON-CHIP STORAGE LATCHES
- TRI-STATE OUTPUTS
- LOW INPUT CURRENT (100μA Max.)
- 35ns TYPICAL ACCESS TIME

APPLICATIONS

MICROPROGRAMMING
HARDWIRE ALGORITHMS
CHARACTER GENERATION
CONTROL STORE
SEQUENTIAL CONTROLLERS

BLOCK DIAGRAM



FE_1 = (13), FE_2 = (11)
V_{CC} = (24), GND = (12), ( ) = Denotes Pin Number

DEVICE	ADDRESS PINS								
	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8
82S114	21	22	23	1	2	4	5	6	–
82S115	21	22	23	1	2	3	4	5	6

PROGRAMMING

Both devices are Field-Programmable, which means that custom patterns are easily incorporated by following the simple fusing procedure in the data sheet. Standard devices are supplied with all outputs at a logical "0". If a programmed unit is required, use the Data Cards or Truth Table input formats given in the back of the Memory Handbook.

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75\ V \leq V_{CC} \leq 5.25\ V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	NOTES
		MIN	TYP	MAX		
Input "0" Current	V_{in} = 0.45 V			−100	μA	
Input "1" Current	V_{in} = 5.5 V			25	μA	
Input (0) Threshold Voltage				.85	V	
Input (1) Threshold Voltage		2			V	1, 3
Input Clamp Voltage	I_{in} = −18 mA	−1.2			V	
Output (0) Voltage	I_{out} = 9.6 mA			0.5	V	
Output (1) Voltage	I_{out} = −2.0 mA	2.7	3.3		V	
Output (1) Short Circuit Current	V_{out} = 0 V, V_{CC} = 5.0 V	−20	−35	−70	mA	1, 2, 3
Input Capacitance	V_{IH} = 2.0 V, V_{CC} = 5.0 V		5		pF	3
Output Capacitance	V_{out} = 2.0 V, V_{CC} = 5.0 V		8		pF	3, 4
Power Supply Current	V_{CC} = 5.0 V		135	170	mA	
Output (1) off Leakage Current (Chip Disabled)	V_{out} = 5.5 V			40	μA	1, 3
Output (0) off Leakage Current (Chip Disabled)	V_{out} = 0.45 V			−40	μA	

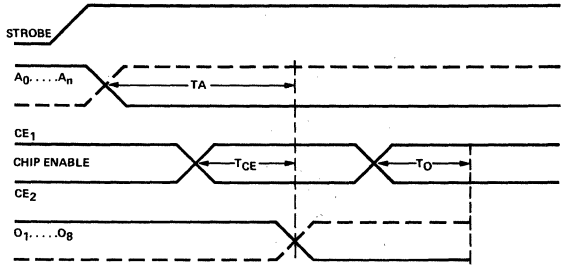
SWITCHING CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75\ V \leq V_{CC} \leq 5.25\ V$

PARAMETER		TEST CONDITIONS	LIMITS			UNITS	NOTES
			MIN	TYP	MAX		
T_A	Address Access Time	LATCHED or TRANSPARENT Read		35		ns	
T_{ADH}	Address Hold Time	LATCHED Read only		−10		ns	
T_{CE}	Chip Enable Access Time	LATCHED or TRANSPARENT Read		20		ns	
T_{CDH}	Chip Enable Hold Time	LATCHED Read only		0		ns	
T_O	Output Disable Time	LATCHED or TRANSPARENT Read		20		ns	3, 5
T_{SW}	Strobe Pulse Width			10		ns	
T_S	Strobe Set-Up Time	LATCHED Read only		20	ns	ns	
T_R	Output Disable Time			15		ns	
T_D	Strobe Access Time			15		ns	

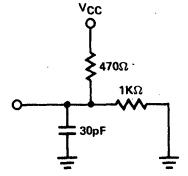
NOTES
1. Positive current is defined as into the terminal referenced.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in "1" state.
3. Applied voltages must not exceed 6.0V. Input currents must not exceed ±30 mA. Output currents must not exceed ±100 mA. Storage temperature must be between −60°C to +150°C.
4. Chip disabled.
5. Rise and fall times for tests must be less than 5ns. Input amplitudes are 3.0V and all measurements are made at 1.5V.

MEMORY TIMING

TRANSPARENT READ
(Output Latches not used)

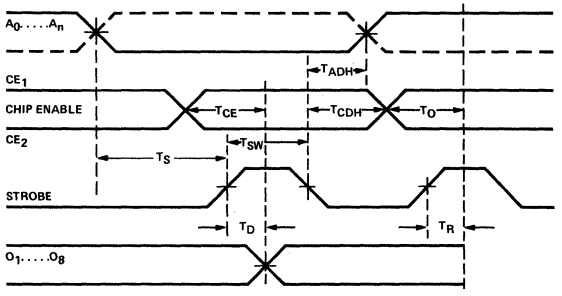


TEST LOAD

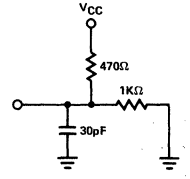


If the strobe is high, the device functions in a manner identical to conventional bipolar ROM's. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_O is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.

LATCHED READ
(Output Latches used)



TEST LOAD



NOTE: Read Cycle = $T_S + T_{ADH} + T_{SW}$

In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transfered and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1"s, proceed as follows:

STEP 1

Ground pin 12, and apply +5.0 ± 0.25V to V_{CC} (pin 24).

STEP 2

Enable the chip by setting CE2 to logic "1" and $\overline{CE1}$ to logic "0" (TTL levels).

STEP 3

Disable "Strobe" by applying a TTL logic "1" to pin 10.

STEP 4

Address the desired programming word by applying TTL "1" and "0" logic levels to the device address inputs.

STEP 5

Apply to FE1 (pin 13) a voltage source of +5.0 ± 0.5V, with 5-10 mA current capability.

STEP 6

Apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit of 150 mA, maximum.

STEP 7

Raise FE2(pin 11) from 0V to +5.0 ± 0.5V for a period of 1 ms, and then return to 0V.

STEP 8

Remove +17.0V supply from programmed output.

STEP 9

Verify programmed output by removing +5.0V supply from FE1 input. Check if output just programmed remains in the "1" state.

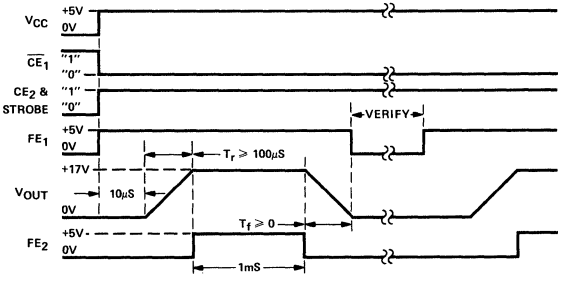
STEP 10

Repeat steps (5) thru (9) to program other bits of the same word.

STEP 11

Change the address, and repeat steps (5) thru (10) until the entire bit pattern is programmed into your custom 82S114/115.

PROGRAMMING TIMING DIAGRAM



DESCRIPTION

The 82S126 (Open Collector Outputs) and the 82S129 (Tri-State Outputs) are Bipolar 1024-Bit Read Only Memories organized as 256 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. Two chip enable lines are provided and the outputs are bussable to allow for memory expansion capability.

The 82S126 and 82S129 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35nS.

The standard 82S126 and 82S129 are supplied with all outputs at a logical "0".

FEATURES

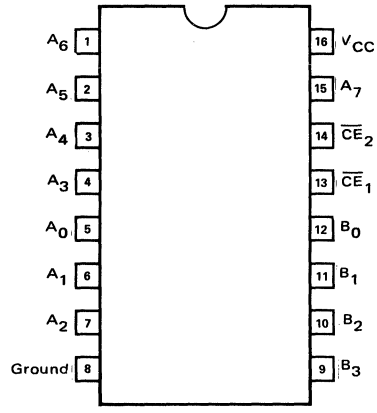
- 50nS MAXIMUM ACCESS TIME
- BUFFERED ADDRESS LINES
- TWO CHIP ENABLE LINES
- OPEN COLLECTOR OR TRI-STATE OUTPUTS
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL

APPLICATIONS

PROTOTYPING
VOLUME PRODUCTION
MICROPROGRAMMING
HARDWIRE ALGORITHMS
CONTROL STORE

PIN CONFIGURATION

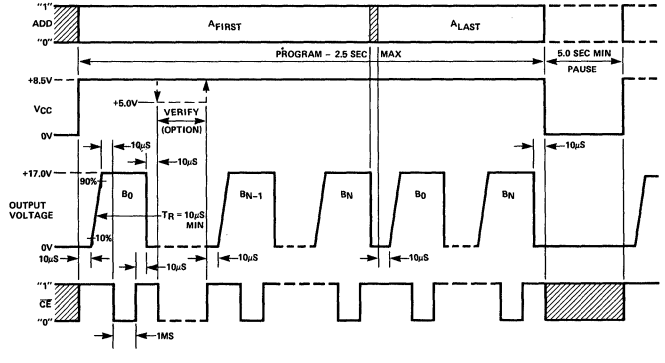
I PACKAGE



PROGRAMMING PROCEDURE

1. Select Address, and raise V_{CC} to 8.5 volts ± 0.5 volts, @ 300 mA minimum.
2. After 10μs delay, apply 17 volts ± 1.0 volts to appropriate output, with 150 mA current limit, and minimum rise time of 10μs.
3. After 10μs delay, pulse $\overline{CE}$ Low (Logic "0") for 1.0 ms (minimum), 2.0 ms (maximum).
4. After 10μs delay, remove 17 volts from output, and select new address.
5. Repeat steps 2–4 until programming is completed.
6. When programming time exceeds 2.5 sec., a 33% ± 10% duty cycle should be imposed.

TYPICAL WAVEFORM During programming



ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25$

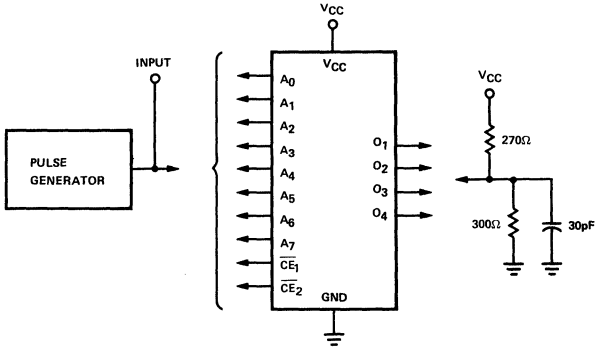
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
"0" Output Voltage	1_{out} = 16mA			0.5	V
"1" Output Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{out} = 5.5V			40	μA
(82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "0", V_{out} = 5.5V			100	μA
(82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = "1", V_{out} = .40 to 5.5V	-40		+40	μA
"1" Output Current (82S129)	$\overline{CE}_1$ = $\overline{CE}_2$ = "0", V_{out} = 2.7V	-2.0			mA
"0" Input Current	V_{in} = 0.4V			100	μA
"1" Input Current	V_{in} = 5.5V			40	μA
Input Voltage					
"0" Level (V_{OL})				.85	V
"1" Level (V_{IH})		2.0			V
Power Consumption			105/525	130/685	mA/mW
Input Clamp Voltage	I_{in} = -18mA				
Output Short Circuit Current	V_{out} = 0 Volts	-20		-70	mA

SWITCHING CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

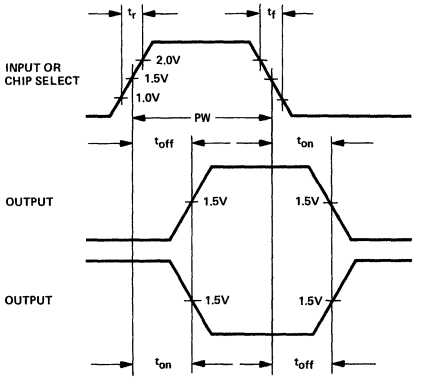
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delay					
Address to Output			35	50	nS
Chip Enable to Output			15	20	nS

NOTES
1. Positive current is defined as into the terminal referenced.
2. Manufacturer reserves the right to make design and process changes and improvements.

AC TEST FIGURE AND WAVEFORM



Ground Pins 13 and 14 when testing address-Output delays.



Input Pulse:
Amplitude = 3.0V
$t_r = t_f$ = 5nS
PW = 200nS (50% Duty Cycle)

DESCRIPTION

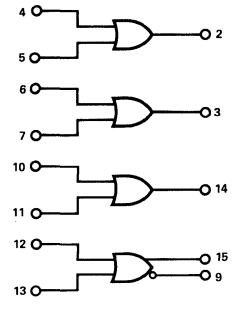
The 10103 package contains three 2 input OR gates and one 2-input OR/NOR gate. In addition to providing the useful OR/NOR function, this 2-input gate can be used as a line driver for driving twisted-pair transmission lines.

The 10103 is a 10,000 series device and, therefore, is completely compatible with other circuits in this family.

FEATURES

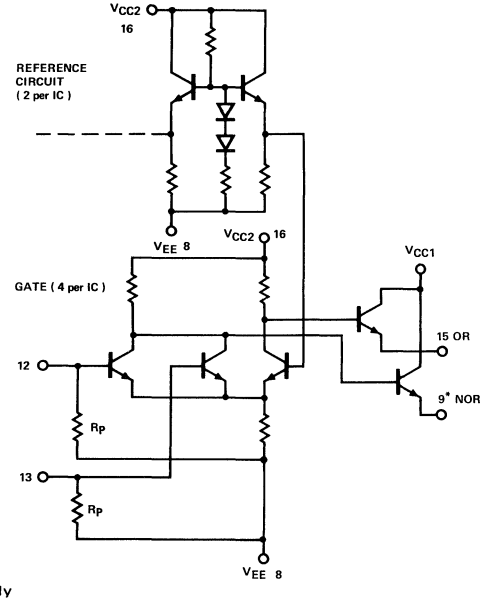
- FAST PROPAGATION DELAY = 2.0 ns TYP
- POWER DISSIPATION = 100mW/PACKAGE TYP
- VERY HIGH FANOUT CAPABILITY – CAN DRIVE 50Ω LINES
- HIGH Z INPUTS WITH 50kΩ PULL-DOWN RESISTORS
- HIGH NOISE IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE}=5.2V ± 5%
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive Logic: High Level = "1"

CIRCUIT SCHEMATIC



All R_P = 50kΩ
*NOR Output Transistor 4th Gate Only

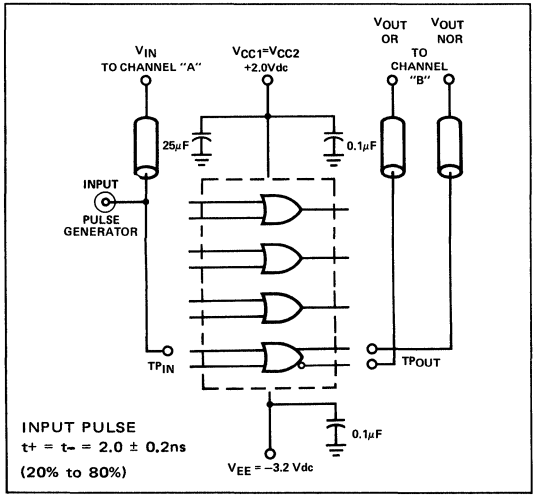
ELECTRICAL CHARACTERISTICS

(At Listed Voltages and Ambient Temperatures)

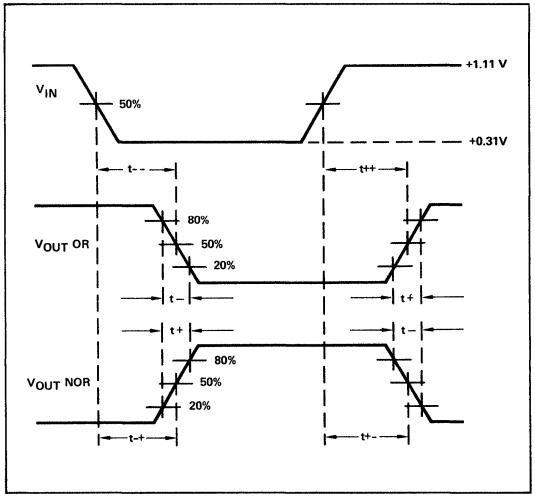
@Test Temperature	Test Voltage Values (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristics	Symbol	Pin Under Test	Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage Applied to Pins Listed Below $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	26	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	–	–	–	–	–	265	–	–	μAdc	12	–	–	–	8	1,16
	I_{inL}	–	–	–	–	0.5	–	–	–	μAdc	–	12	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc		12	–	–	8	1,16
		9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc		13	–	–	8	1,16
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	12		–	–	8	1,16
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	13		–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	12		–	–	8	1,16
		9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	13		–	–	8	1,16
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc		12	–	–	8	1,16
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc		13	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	9	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–		12	8	1,16
		9	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–		13	8	1,16
		15	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	12		8	1,16
		15	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	13		8	1,16
Logic "0" Threshold Voltage	V_{OLA}	9	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	12		8	1,16
		9	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	13		8	1,16
		15	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–		12	8	1,16
		15	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–		13	8	1,16
Switching Times (50-Ohm Load)													Pulse In	Pulse Out	−3.2V	+2.0V
Propagation Delay	t_{12+15+}	15	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	15	8	1,16
	t_{12-15-}	15	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	15	8	1,16
	t_{12+9-}	9	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	9	8	1,16
	t_{12-9+}	9	1.0	3.1	1.0	2.0	2.9	1.0	3.3	ns	–	–	12	9	8	1,16
Rise Time (20% to 80%)	t_{15+}	15	1.1	3.6	1.1	2.0	3.3	1.1	3.7	ns	–	–	12	15	8	1,16
	t_{9+}	9	1.1	3.6	1.1	2.0	3.3	1.1	3.7	ns	–	–	12	9	8	1,16
Fall Time (20% to 80%)	t_{15-}	15	1.1	3.6	1.1	2.0	3.3	1.1	3.7	ns	–	–	12	15	8	1,16
	t_{9-}	9	1.1	3.6	1.1	2.0	3.3	1.1	3.7	ns	–	–	12	9	8	1,16

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DESCRIPTION

The 10104 Quad AND Gate package contains three, 2-input AND gates and one, 2-input AND/NAND. The AND function is formed by series gating, a technique which makes use of the inherent speed of current-mode logic and provides this useful function with minimum propagation delays.

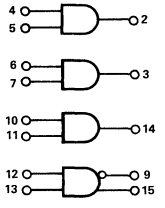
The AND/NAND gate provided in the 10104 package can be used to drive twisted pair, differential transmission lines.

FEATURES

- HIGH SPEED
  PROPAGATION DELAY = 2.7ns TYPICAL
- LOW POWER DISSIPATION = 40mW/GATE TYPICAL
- HIGH FANOUT CAPABILITY, CAN DRIVE 50Ω LINES
- HIGH Z INPUTS, INTERNAL 50KΩ PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS FOR BUSSING APPLICATIONS

LOGIC DIAGRAM

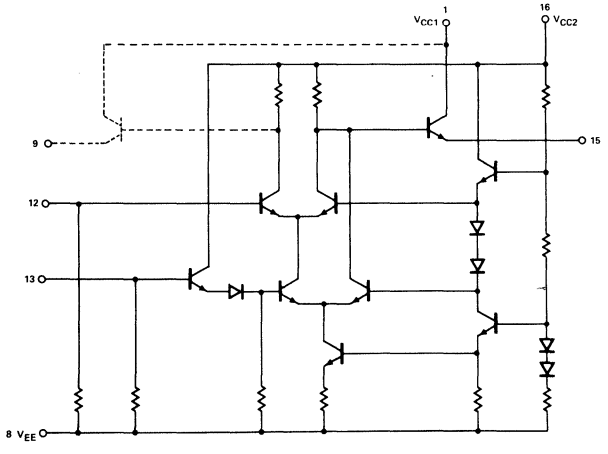
10104 QUAD AND GATE



t_{pd} = 2.7ns TYPICAL

CIRCUIT SCHEMATIC

1/4 OF CIRCUIT SHOWN



ELECTRICAL CHARACTERISTICS

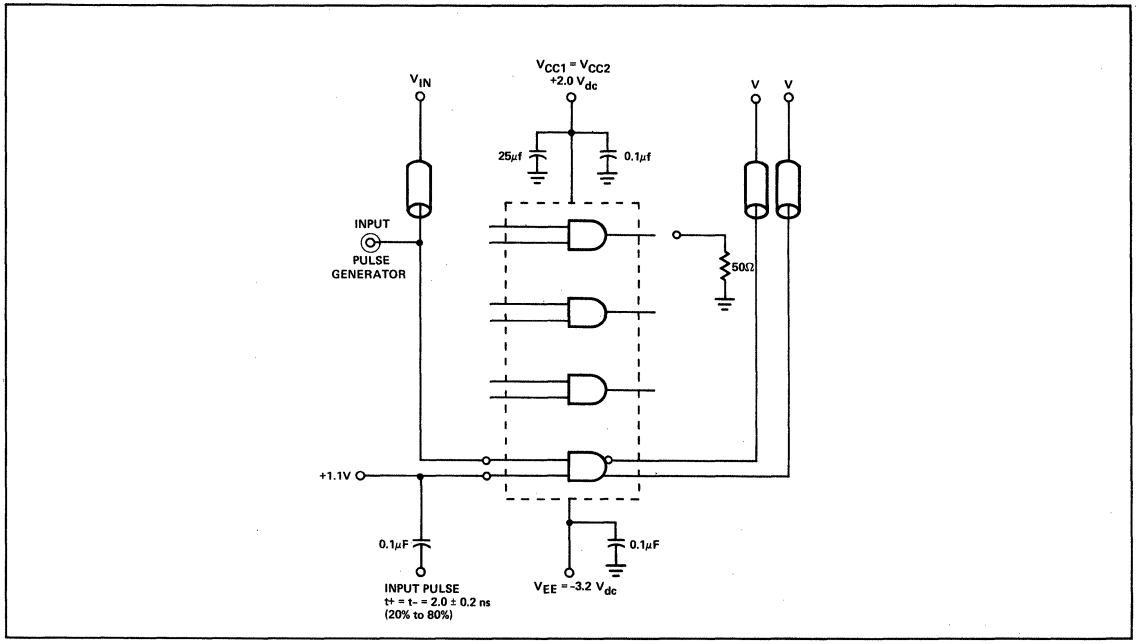
(At listed voltages and ambient temperatures)

Test Temperature	Test Voltage Values (Volts) V_{IH} Max	V_{IL} Min	V_{IHA} Min	V_{ILA} Max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

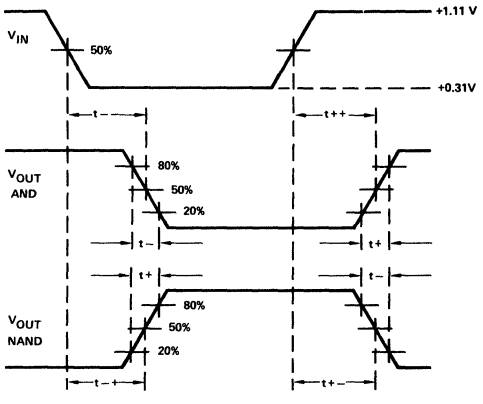
Characteristics	Symbol	Pin Under Test	Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltages Applied to Pins Listed Below V_{IH} Max	V_{IL} Min	V_{IHA} Min	V_{ILA} Max	V_{EE}	(Vcc) Gnd
Power Supply Drain Current	I_E	8				28	35			mAdc					8	1,16
Input Current	I_{InH}	12					220			µAdc	13				8	1,16
		13					265			µAdc	12,13				8	1,16
	I_{InL}	12			0.5					µAdc		12			8	1,16
Logic "1" Output Voltage	V_{OH}	15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	12,13				8	1,16
		9	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	–				8	1,16
Logic "0" Output Voltage	V_{OL}	15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–				8	1,16
		9	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	12,13				8	1,16
Logic "1" Threshold Voltage	V_{OHA}	9	−1.090	–	−0.980	–	–	−0.910	–	Vdc	–			12	8	1,16
		9	−1.090	–	−0.980	–	–	−0.910	–	Vdc	–			13	8	1,16
		15	−1.090	–	−0.980	–	–	−0.910	–	Vdc	12		13		8	1,16
		15	−1.090	–	−0.980	–	–	−0.910	–	Vdc	13		12		8	1,16
Logic "0" Threshold Voltage	V_{OLA}	9	–	−1.655	–	–	−1.630	–	−1.595	Vdc	12		13		8	1,16
		9	–	−1.655	–	–	−1.630	–	−1.595	Vdc	13		12		8	1,16
		15	–	−1.655	–	–	−1.630	–	−1.595	Vdc				12	8	1,16
		15	–	−1.655	–	–	−1.630	–	−1.595	Vdc				13	8	1,16
Switching Times (50 OHM Load)											+1.11V		Pulse In	Pulse Out	−3.2V	+2.0V
Propagation Delay*	t_{12+15+}	15	–	–	–	2.2	–	–	–	ns	13		12	15	8	1,16
	t_{12-15-}	15	–	–	–	2.2	–	–	–	ns	13		12	15	8	1,16
	t_{12+9-}	9	–	–	–	2.2	–	–	–	ns	13		12	9	8	1,16
	t_{12-9+}	9	–	–	–	2.2	–	–	–	ns	13		12	9	8	1,16
	t_{13+15+}	15	–	–	–	2.7	–	–	–	ns	12		13	15	8	1,16
	t_{13+9-}	9	–	–	–	2.7	–	–	–	ns	12		13	9	8	1,16
Rise Time (20% to 80%)	t_{15+}	15	–	–	–	2.0	–	–	–	ns	12		13	15	8	1,16
	t_{9+}	9	–	–	–	2.0	–	–	–	ns	12		13	9	8	1,16
Fall Time (20% to 80%)	t_{15-}	15	–	–	–	2.0	–	–	–	ns	12		13	15	8	1,16
	t_{9-}	9	–	–	–	2.0	–	–	–	ns	12		13	9	8	1,16

*For I_{InH} and AC tests, inputs 4, 7, and 10 are similar to input 13 and inputs 5, 6, and 11 are similar to input 12.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS@ 25°C



V_{OUT} OR-AND-INVERT V_{OUT} OR-AND

NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10108B, F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

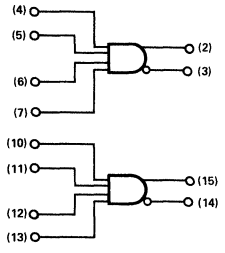
The 10108 Dual AND/NAND gate is a high speed device featuring complementary outputs on each gate. Because of the complementary outputs, this device is ideal for use as a differential line driver.

The 10108 provides the AND/NAND function with little loss in performance from more conventional ECL NOR circuits. This is accomplished by using internal series gating techniques which maintain the inherent speed advantages of CML.

FEATURES

- HIGH SPEED PROPAGATION DELAY
  - 2.3ns TYPICAL FOR AND
  - 2.8ns TYPICAL FOR NAND
- LOW POWER - 145mW/PACKAGE TYPICAL
- HIGH FANOUT - CAN DRIVE 50 LINES
- HIGH Z INPUTS WITH 50kΩ PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS FOR BUSSING APPLICATIONS
- USEFUL AND/NAND FUNCTION

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL "1"

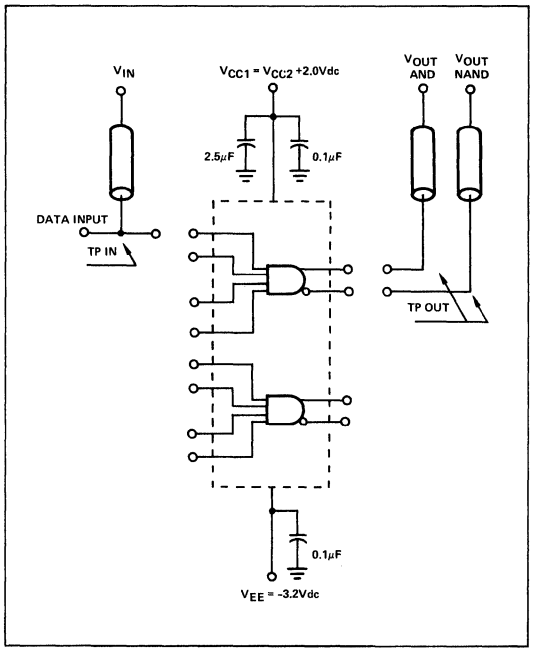
ELECTRICAL CHARACTERISTICS

(Listed Voltages and Ambient Temperatures)

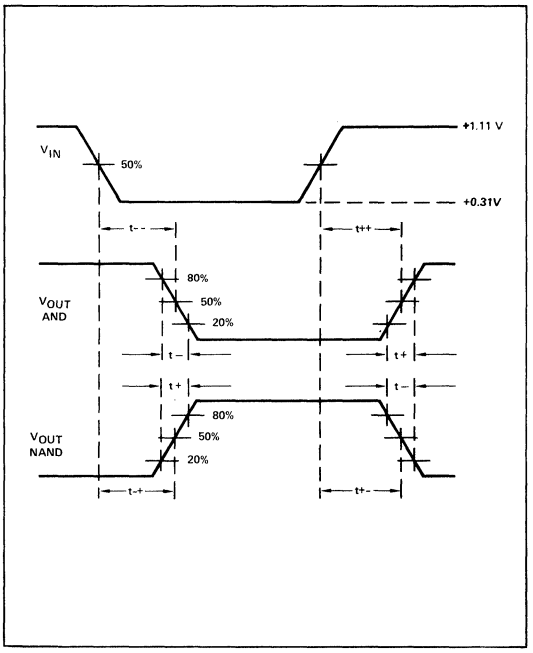
@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
–30°C	–0.890	–1.890	–1.205	–1.500	–5.2
+25°C	–0.810	–1.850	–1.105	–1.475	–5.2
+85°C	–0.700	–1.825	–1.035	–1.440	–5.2

Characteristics	Symbol	Pin Under Test	Test Limits –30°C Min	–30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) gnd
Power Supply Drain Current	I_{EE}	8	–	–	–	28	36	–	–	mA	5, 7, 11, 13	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	265	–	–	μAdc	4	–	–	–	8	1,16
	I_{inL}	4		–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	–1.060	–0.890	–0.960	–	–0.810	–0.890	–0.700	Vdc	4, 5, 6, 7	–	–	–	8	1,16
		3	–1.060	–0.780	–0.960	–	–0.700	–0.890	–0.590	Vdc	–	–	–	–	8	1,16
Logic "0" Output Voltage	VOL	2	–2.000	–1.675	–1.990	–	–1.650	–1.920	–1.615	Vdc	–	–	–	–	8	1,16
		3	–1.890	–1.675	–1.850	–	–1.650	–1.825	–1.615	Vdc	4, 5, 6, 7	–	–	–	8	1,16
Logic "1" Threshold Voltage	VOHA	2	–1.080	–	–0.980	–	–	–0.910	–	Vdc	4, 5, 6, 7	–	–	–	8	1,16
		3	–1.080	–	–0.980	–	–	–0.910	–	Vdc	–	–	–	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	–1.655	–	–	–1.630	–	–1.595	Vdc	–	–	–	–	8	1,16
		3	–	–1.655	–	–	–1.630	–	–1.595	Vdc	4, 5, 6, 7	–	–	–	8	1,16
Switching Times (50Ω Load)											+1.11V		Pulse In	Pulse Out	–3.2V	+2.0V
Propagation Delay	t_{4+2+}	2	–	–	1.4	2.3	3.4	–	–	ns	5, 6, 7	–	4	2	8	1,16
	t_{4-2-}	2	–	–	1.4	2.3	3.4	–	–	ns	5, 6, 7	–	4	2	8	1,16
	t_{4+3-}	3	–	–	1.4	2.3	3.4	–	–	ns	5, 6, 7	–	4	3	8	1,16
	t_{4-3+}	3	–	–	1.4	2.3	3.4	–	–	ns	5, 6, 7	–	4	3	8	1,16
	t_{5+2+}	2	–	–	1.4	2.8	3.7	–	–	ns	4, 6, 7	–	5	2	8	1,16
	t_{5-2-}	2	–	–	1.4	2.8	3.7	–	–	ns	4, 6, 7	–	5	2	8	1,16
	t_{5+3-}	3	–	–	1.4	2.8	3.7	–	–	ns	4, 6, 7	–	5	3	8	1,16
	t_{5-3+}	3	–	–	1.4	2.8	3.7	–	–	ns	4, 6, 7	–	5	3	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.1	2.2	4.0	–	–	ns	4, 6, 7	–	5	2	8	1,16
	t_{3+}	3	–	–	1.1	2.2	4.0	–	–	ns	4, 6, 7	–	5	3	8	1,16
Fall Time (20% to 80)	t_{2-}	2	–	–	1.1	2.2	4.0	–	–	ns	4, 6, 7	–	5	2	8	1,16
	t_{3-}	3	–	–	1.1	2.2	4.0	–	–	ns	4, 6, 7	–	5	3	8	1,16

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

10129F: –30 to +85°C

DIGITAL 10,000 ECL SERIES

DESCRIPTION

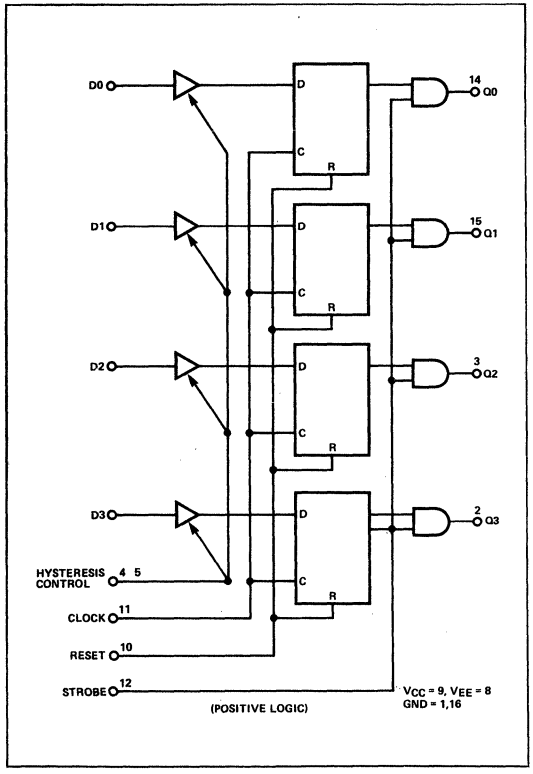
The 10129 is a versatile bus receiver that interfaces directly with both TTL and IBM logic levels on the data bus. The output levels and control inputs are ECL 10K, allowing the 10129 to function as TTL/IBM to ECL translator.

Four on-chip, D-type latches provide a convenient temporary storage medium for bus data awaiting further processing. The latches are controlled by a CLOCK input and a RESET input. Data is entered on the rising edge of the clock and stored as long as the clock remains high. With the clock low, the latches are bypassed, the reset input is disabled and the outputs follow the D inputs.

A STROBE input is provided to "enable" the output buffer gates and thus allow the data from the bus to be synchronized with the rest of the receiving system. With the clock input low, this data comes directly from the D inputs and with the clock high, the data comes from the latches. The HYSTERESIS CONTROL input allows the 10129 to operate with or without hysteresis on the data input lines. Tying this input to V_{EE} fixes the threshold levels while tying this input to grounds inserts 200mV of hysteresis between the positive and negative going directions of the data input swing. (See specification table.)

All control signal inputs are provided with 50kΩ pull-down resistors allowing unused inputs to be left open. Data inputs, however, must be tied to ground or V_{EE}.

LOGIC DIAGRAM



FEATURES

- FAST PROPAGATION DELAY –
  12.0 ns TYPICAL DATA TO OUTPUT
  4.0 ns TYPICAL STROBE TO OUTPUT
- HIGH FANOUT CAPABILITY – CAN DRIVE 50Ω LINES
- ON CHIP LATCHES
- ACCEPTS TTL AND IBM DATA INPUTS; ECL 10K DATA OUTPUTS
- HYSTERESIS CONTROL PIN
- HIGH INPUT Z – 50kΩ PULL-DOWN RESISTORS ON ECL INPUTS (NO PULLDOWNS ON DATA INPUTS)

TRUTH TABLE (Ø = Don't Care)

STROBE	RESET	C	D	Qn + 1
L	Ø	Ø	Ø	L
H	L	H	Ø	Qn
H	Ø	L	L	L
H	Ø	L	H	H
Ø	H	H	Ø	L

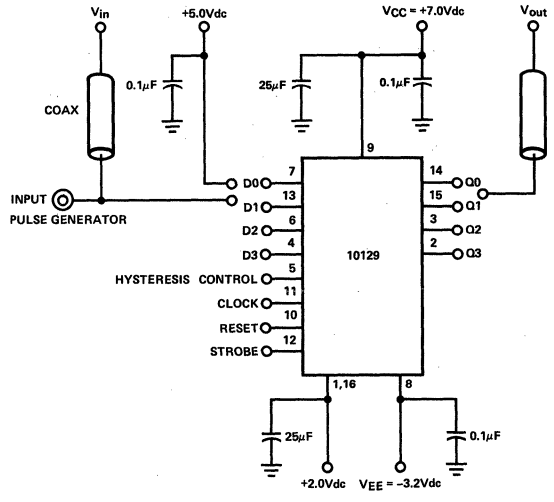
NOTES

1. V_{CC} (Pin 9) = 5.0 volts or 6.0 volts for D.C. tests
   = 7.0 volts for A.C. tests
2. Output latched to logic high state prior to test
3. Hysteresis Mode.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	TEST LIMITS -30°C MIN	-30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNIT	Test Voltage Applied to Pins Listed Below: $V_{IH\ Max}$	$V_{IL\ Min}$	$V_{IHA\ Min}$	$V_{ILA\ Max}$	V_{EE}	Gnd	OTHER TEST CONDITIONS
Negative Power Supply Current	I_E	8					152			mAdc	11	12			8	1, 15, 16	
		8					172			mAdc	11	12			5, 8	1, 16	
Positive Power Supply Current	I_{CC}	9					8			mAdc					8	1, 16	Pins 4, 6, 7, 13= 0.4 (TTL) or 0.15 (IBM) V.
Input current	IinH	4, 6, 7, 13					95			µAdc					8	1, 16	Pins 4, 6, 7, 13= 3.0 (TTL) or 3.11 (IBM) V.
		10					450			µAdc	10, 11				8	1, 16	
		11, 12					245			µAdc	11, 12				8	1, 16	
	IinL	4, 6, 7, 13					-1.0			µAdc					8	1, 16	Pins 4, 6, 7, 13= 0.4 (TTL) or 0.15 (IBM) V.
		10, 11, 12			0.5					µAdc	10, 11, 12				8	1, 16	
Logic "1" Output voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12	10, 11			5, 8	1, 16	Pin 4 = 3.0 (TTL) or
		3	–	–	–	–	–	–	–		–	–			5, 8	1, 16	Pin 6 = 3.0 (TTL) or
		2	–	–	–	–	–	–	–		–	–			8	1, 5, 16	Pin 4 = 3.11 (IBM) V.
		3	–	–	–	–	–	–	–		–	–			8	1, 5, 16	Pin 6 = 3.11 (IBM) V.
Logic "0" Output voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	12	10, 11			5, 8	1, 16	Pin 4 = 0.4 (TTL) or
		3	–	–	–	–	–	–	–		–	–			5, 8	1, 16	Pin 6 = 0.4 (TTL) or
		2	–	–	–	–	–	–	–		–	–			8	1, 5, 16	Pin 4 = 0.15 (IBM) V.
		3	–	–	–	–	–	–	–		–	–			8	1, 5, 16	Pin 6 = 0.15 (IBM) V.
Logic "1" Threshold voltage	V_{OHA}	2 ②	-1.060	–	-0.980	–	–	-0.910	–	Vdc	11, 12	–	–	10	5, 8	1, 16	Pin 4 = 3.0 (TTL) or
		2	–		–			–			–	10, 11	12	–	5, 8	1, 16	Pin 4 = 3.11 (IBM) V
		2 ②	–		–			–			10, 12	–	11	–	5, 8	1, 16	Pin 4 =
		2 ③	–		–			–			12	10, 11	–	–	5, 8	1, 16	Pin 4 = 0.8(TTL) or 0.7(IBM)V.
		2 ③	–		–			–			12	10, 11	–	–	8	1, 16	Pin 4 = +0.4V V_{ILA+}
											12	10, 11	–	–	8	1, 16	Pin 4 = 4.0V V_{ILA-}
Logic "0" Threshold voltage	V_{OLA}	2 ②	–	-1.655	–	–	-1.630	–	-1.595	Vdc	11, 12	–	10	–	5, 8	1, 16	Pin 4 = 3.0 (TTL) or
		2									–	10, 11	–	12	5, 8	1, 16	Pin 4 = 3.11 (IBM) V
		2 ②									10, 12	–	11	–	5, 8	1, 16	Pin 4 =
		2									12	10	–	–	5, 8	1, 16	Pin 4 = 0.8(TTL) or 0.7(IBM)V
		2 ③									12	10	–	–	8	1, 5, 16	Pin 4 = +0.4V V_{ILA+}
		2 ③									12	10	–	–	8	1, 5, 16	Pin 4 = 4.0V V_{ILA-}
Switching times											+1.11V	+0.31V	pulse in	pulse out			
Prop. data input	t_{7+14+}	14	–	–	–	12.0	–	–	–	nS	12	10, 11	7	14	5, 8	1, 16	see Fig 1
	t_{7-14-}	14	–	–	–	10.0	–	–	–	nS	12	10, 11	7	14	5, 8	1, 16	see Fig 1
Clock input	$t_{11-14\pm}$	14	–	–	–	5.0	–	–	–	nS	12	10	7, 11	14	5, 8	1, 16	see Fig 4
strobe input	$t_{12\pm14\pm}$	14	–	–	–	4.0	–	–	–	nS	–	10, 11	12	14	5, 8	1, 16	see Fig 2, Pin 7 = 5.0V
reset input	t_{10+14-}	14	–	–	–	5.0	–	–	–	nS	12	–	10, 11	14	5, 8	1, 16	see Fig 3, Pin 7 = 5.0V
hysteresis mode	t_{7+14+}	14	–	–	–	18.0	–	–	–	nS	12	10, 11	7	14	8	1, 5, 16	see Fig 1
	t_{7-14-}	14	–	–	–	10.0	–	–	–	nS	12	10, 11	7	14	8	1, 5, 16	see Fig 1
Set-up time	t_{setup}	14	–	–	–	15.0	–	–	–	nS	12	10	7, 11	14	5, 8	1, 16	see Fig 5
hold time	t_{hold}	14	–	–	–	15.0	–	–	–	nS	12	10	7, 11	14	5, 8	1, 16	see Fig 5
rise time	t_+	14	–	–	–	2.0	–	–	–	nS	12	10, 11	7	14	5, 8	1, 16	see Fig 1
fall time	t_-	14	–	–	–	2.0	–	–	–	nS	12	10, 11	7	14	5, 8	1, 16	see Fig 1

SWITCHING TIME TEST CIRCUIT



NOTES

1. Unused outputs connected to ground through a 50Ω resistor.
2. 50Ω termination to ground located in each scope channel input.
3. All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

FIGURE 1 – DATA TO OUTPUT
(Clock and Reset are low. Strobe is high)

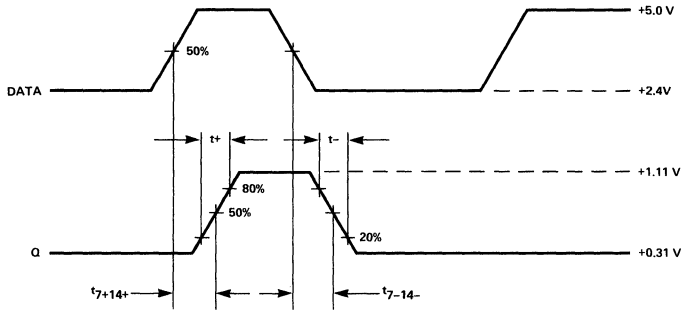


FIGURE 2 – STROBE TO OUTPUT
(Data is high. Clock and Reset are low)

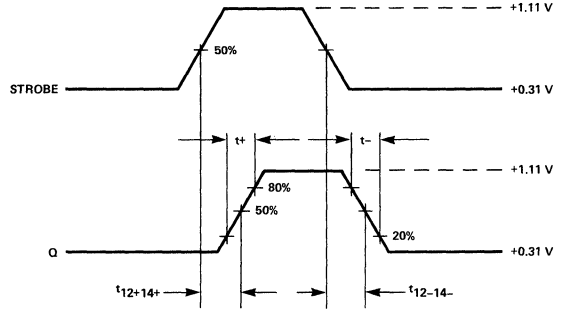


FIGURE 3 – RESET TO OUTPUT
(Data and Strobe are high)

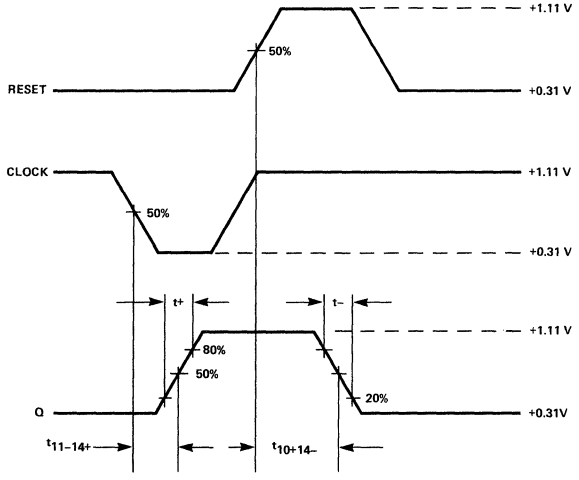


FIGURE 4 – CLOCK TO OUTPUT
(Reset is low. Strobe is high)

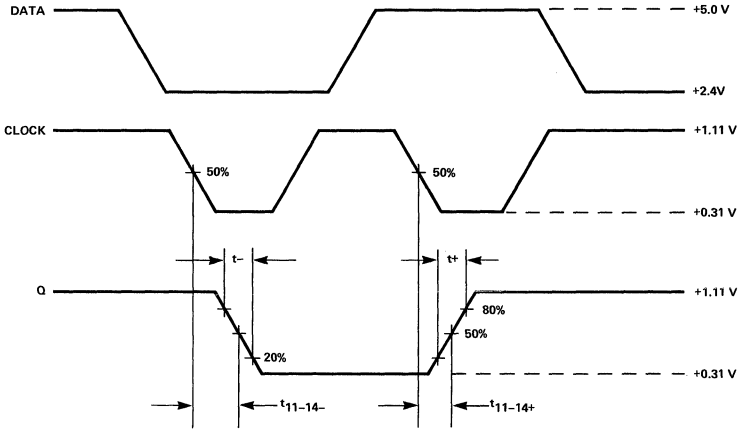
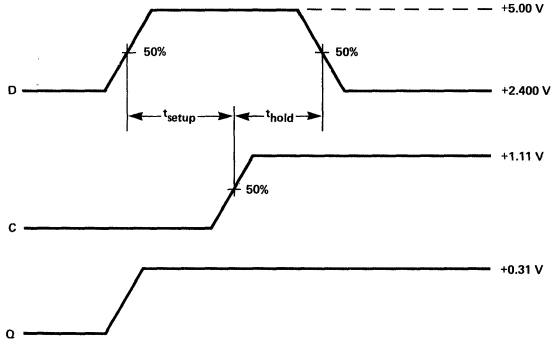


FIGURE 5 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



DESCRIPTION

The 10136 and 10137 are high speed synchronous counters that can count up, count down, preset, or stop count at rates exceeding 100MHz.

The 10136 is a 16-state (Hexadecimal) counter and the 10137 is a 10-state (Decade) counter.

The flexibility of these devices allows the designer to use one basic counter design for all applications. The synchronous count feature makes these MSI parts suitable for either computers or instrumentation.

The carry input enables the counter, and prevents it from changing state when the clock goes high. The inputs S1 and S2 control the state of the counter: stop count, increment (count up), decrement (count down), and preset (program) count. The other inputs are clock, and the four D inputs for presetting the counter.

The counter changes state only on the positive-going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The next state of the counter is determined by the configuration of the inputs only during the positive transition of the clock.

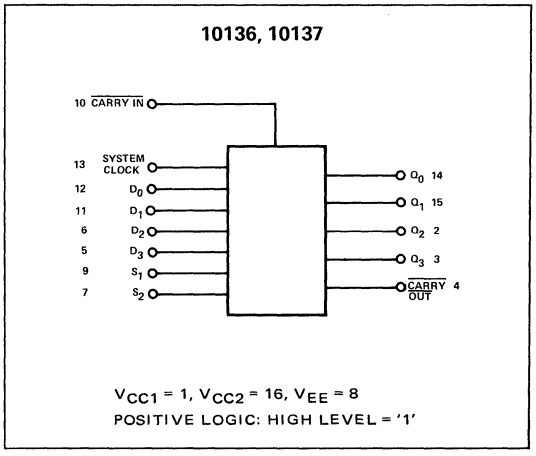
In addition to the four Q's outputs there is a carry out which goes low on the terminal count. In the preset mode the carry out on the 10136 will stay low but the carry out on the 10137 will depend on the condition of Q_1 and/or Q_2.

APPLICATIONS

Either the binary counter (10136) or the decade counter (10137) can be useful in high speed central processors and peripheral controllers, mini-computers, high speed digital communication equipment, and instrumentation.

When used as a prescaler, it is possible to extend the input frequency of the 10136, 37 to over 200MHz with the 10231.

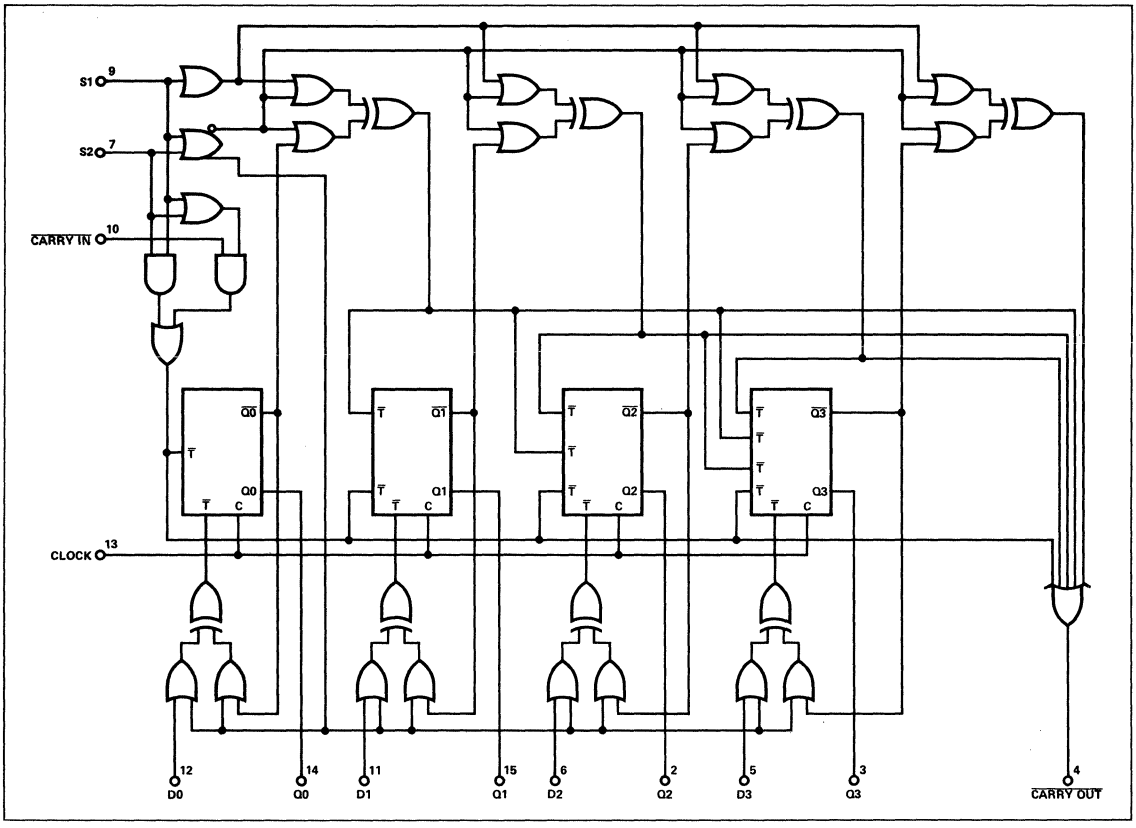
PIN CONFIGURATION (TOP VIEW)



FUNCTION SELECT TABLE

S1	S2	OPERATING MODE
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

UNIVERSAL BINARY UP/DOWN COUNTER – 10136



SEQUENTIAL TRUTH TABLE[1] – 10136

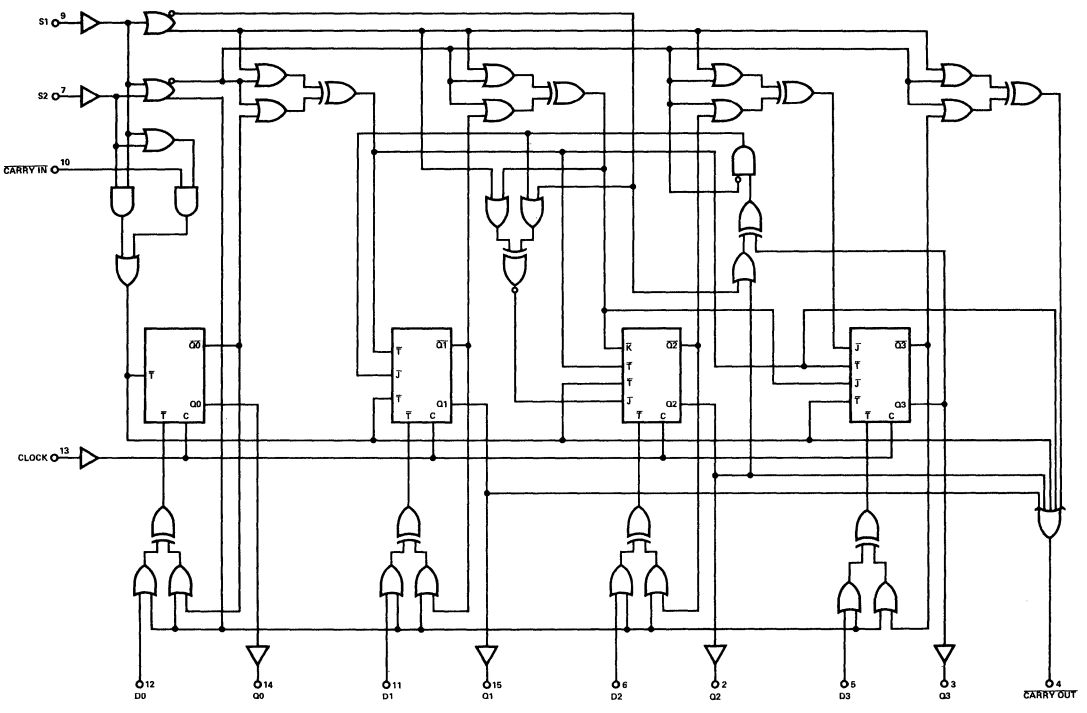
INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock 2	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	Ø	H	L	L	H	H	L
L	H	Ø	Ø	Ø	Ø	L	H	H	L	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	L	H	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	H	H	H	H	L
L	H	Ø	Ø	Ø	Ø	H	L	H	H	H	H	H
L	H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H
H	H	Ø	Ø	Ø	Ø	Ø	H	H	H	H	H	H
L	L	H	H	L	L	Ø	H	H	H	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	L	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	L	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	H	H	H	H	H

Ø = Don't care.

1 = Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

2 = A clock H is defined as a clock input transition from a low to a high logic level.

UNIVERSAL DECADE UP/DOWN COUNTER – 10137



SEQUENTIAL TRUTH TABLE[1] – 10137

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock 2	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	Ø	H	H	H	H	L	H
L	H	Ø	Ø	Ø	Ø	L	H	L	L	L	H	H
L	H	Ø	Ø	Ø	Ø	L	H	H	L	L	H	L
L	H	Ø	Ø	Ø	Ø	L	H	L	L	L	L	H
L	H	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
L	H	Ø	Ø	Ø	Ø	H	H	H	L	L	L	H
L	H	Ø	Ø	Ø	Ø	H	H	H	L	L	L	H
H	H	Ø	Ø	Ø	Ø	Ø	H	H	L	L	L	H
L	L	H	H	L	L	Ø	H	H	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	L	L	L	L

Ø = Don't care.
1 = Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
2 = A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

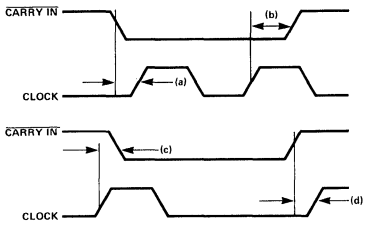
(At Listed Voltages and Ambient Temperatures)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	10136, 10137 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNIT	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	120	150	–	–	mADC	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	5,6,11,12	–	–	–	–	220	–	–	μADC	5,6,11,12	–	–	–	8	1,16
		7	–	–	–	–	265	–	–	μADC	7	–	–	–	8	1,16
		9,10	–	–	–	–	245	–	–	μADC	9,10	–	–	–	8	1,16
		13	–	–	–	–	290	–	–	μADC	13	–	–	–	8	1,16
	$I_{in\ L}$	All	–	–	0.5	–	–	–	–	μADC	–	①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14 ②	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	VDC	12	7,9	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	VDC	–	7,9	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	14 ②	-1.080	–	-0.980	–	–	-0.910	–	VDC	–	7,9	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	14 ②	–	-1.655	–	–	-1.630	–	-1.595	VDC	–	7,9	–	12	8	1,16
Switching Times (50-ohm Load)											+1.11V	+0.31V	Pulse In	Pulse Out	-3.2V	+2.0V
Propagation Delay																
Clock Input	t_{13+14+}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	nS	12	–	13	14	8	1,16
	t_{13+14-}	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	nS	–	–	13	14	8	1,16
	t_{13+4+}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5	nS	7	–	13	4	8	1,16
	t_{13+4-}	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5	nS	7	–	13	4	8	1,16
$\overline{\text{Carry In}}$ To $\overline{\text{Carry Out}}$	t_{10-4-}	4 ③	1.6	7.4	1.6	5.0	6.9	1.9	7.5	nS	9	13	10	4	8	1,16
	t_{10+4+}	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5	nS	9	13	10	4	8	1,16
Set Up Time																
Data Inputs	t_{12+13+}	14	–	–	3.5	2.1	–	–	–	nS	–	7,9	12,13	14	8	1,16
	t_{12-13+}	14	–	–	3.5	2.1	–	–	–	nS	–	7,9	12,13	14	8	1,16
Select Inputs	t_{9+13+}	14	–	–	7.5	5.4	–	–	–	nS	–	–	9,13	14	8	1,16
	t_{7+13+}	14	–	–	7.5	5.4	–	–	–	nS	–	–	7,13	14	8	1,16
$\overline{\text{Carry In}}$ Input	t_{10-13+}	14	–	–	3.7	2.9	–	–	–	nS	7	9	10,13	14	8	1,16
	t_{13+10+}	14	–	–	-1.0	-1.9	–	–	–	nS	7	–	10,13	14	8	1,16
Hold Time																
Data Inputs	t_{13+12+}	14	–	–	-1.0	-1.9	–	–	–	nS	–	7,9	12,13	14	8	1,16
	t_{13+12-}	14	–	–	-1.0	-1.9	–	–	–	nS	–	7,9	12,13	14	8	1,16
Select Inputs	t_{13+9+}	14	–	–	-2.5	-5.4	–	–	–	nS	–	–	9,13	14	8	1,16
	t_{13+7+}	14	–	–	-2.5	-5.4	–	–	–	nS	–	–	7,13	14	8	1,16
$\overline{\text{Carry In}}$ Input	t_{13+10-}	14	–	–	-1.6	-2.4	–	–	–	nS	7	9	10,13	14	8	1,16
	t_{10+13+}	14	–	–	3.1	2.2	–	–	–	nS	7	9	10,13	14	8	1,16
Counting Frequency	$t_{countup}$	14	125	–	125	160	–	125	–	MHz	7	–	13	14	8	1,16
	$t_{countdown}$	14	125	–	125	160	–	125	–	MHz	9	–	13	14	8	1,16
Rise Time (20% to 80%)	t_{4+}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	nS	7	–	13	4	8	1,16
	t_{4+}	14	0.9	3.3	1.1	2.0	3.3	1.1	3.5	nS	7	–	13	14	8	1,16
Fall Time (20% to 80%)	t_{4-}	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	nS	7	–	13	4	8	1,16
	t_{14-}	14	0.9	3.3	1.1	2.0	3.3	1.1	3.5	nS	7	–	13	14	8	1,16

1. Individually apply V_{ILMIN} to pin under test.
2. Measure output after clock pulse V_{IL} ⌐ V_{IH} appears at clock input (Pin 13).
3. Before test set all Q inputs to a logic low.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



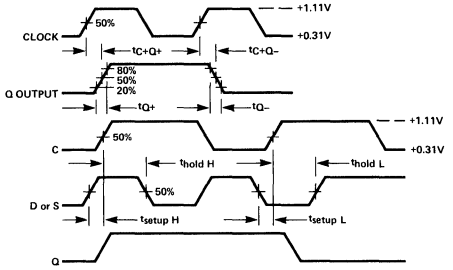
(a) is the minimum time to wait after the counter has been enabled to clock it

(b) is the minimum time before the counter has been disabled that it may be clocked

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter

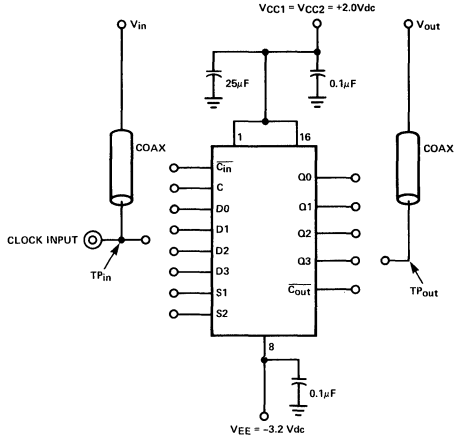
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter

(c) and (d) may be negative numbers.



NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S. t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

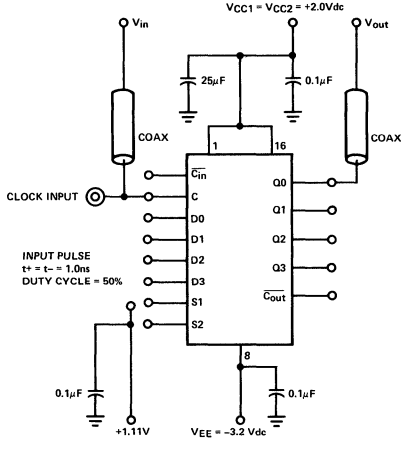


50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

COUNT FREQUENCY TEST CIRCUIT



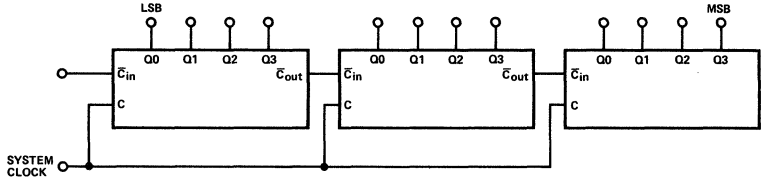
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

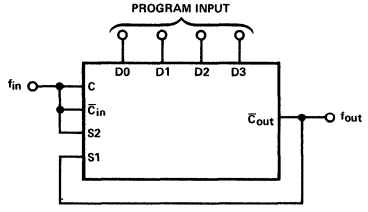
50-ohm termination to ground located in each scope channel input.

UNIVERSAL COUNTER APPLICATIONS

12 BIT SYNCHRONOUS COUNTER



50 MHz PROGRAMMABLE COUNTER



DESCRIPTION

The 10145 is an ECL 64-bit read-write random access memory organized as 16 words of 4 bits each. Words are selected through fully decoded and buffered inputs when the chip enable ($\overline{CE}$) is low. Data is written into the selected word by bringing the READ/$\overline{WRITE}$ input low. Outputs are low during write.

On-chip input pulldown resistors allow any unused inputs to be left open. Open emitter outputs allow corresponding bits of different devices to be tied together to form a "Wire OR" logic connection.

The 10145 utilizes separate internal metal systems and wire bonds for V_{CC1} and V_{CC2}. The exceptionally high speed of the 10145 makes it particularly suited for register file and and scratch pad applications.

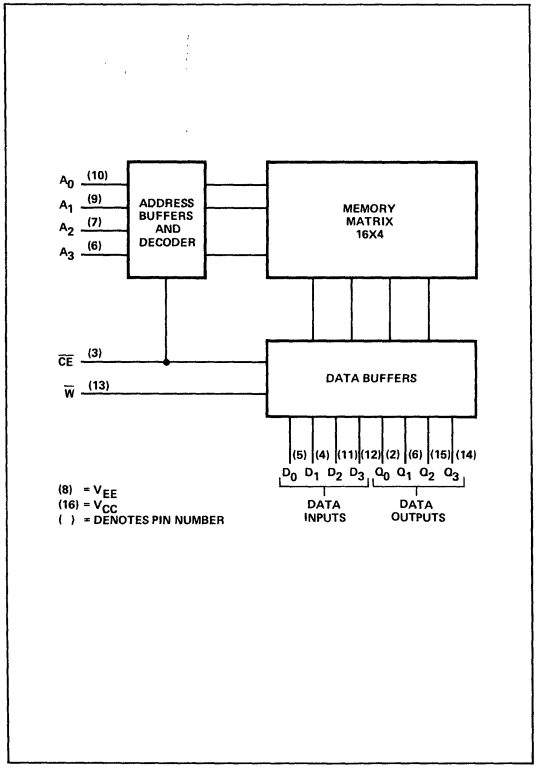
FEATURES

- 8.5ns ADDRESS ACCESS TIME (TYP)
- INPUT PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS AND CHIP ENABLE INPUT FOR MEMORY EXPANSION
- 50 Ohm OUTPUT SPECIFICATION
- SINGLE -5.2V POWER SUPPLY
- FULLY DECODED INPUTS
- FULLY COMPATIBLE WITH SIGNETICS 10,000 SERIES FAMILY OF INTEGRATED CIRCUITS

APPLICATIONS

SCRATCH PAD MEMORIES
BUFFER MEMORIES
REGISTER FILES
CONTROL STORES

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS V_{EE} = -5.2V, V_{CC} = 0V, R_L = 50Ω TO -2.0V

PARAMETER		TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
I_E	Supply Current		25°C		116	145	mA
I_{INH}	Input Current (Pins 3, 6, 7, 9, 10)	$V_{IN} = V_{IH}$ MAX.	25°C			200	μA
I_{INH}	Input Current (Pins 4, 5, 11, 12)	$V_{IN} = V_{IH}$ MAX.	25°C			220	μA
I_{INH}	Input Current (Pin 13)	$V_{IN} = V_{IH}$ MAX.	25°C			455	μA
I_{INL}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ MIN.	25°C	0.5			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
V_{OH}	Output Voltage	$V_{IN} = V_{IH}$ MAX., V_{IL} MIN.	-30°C 25°C 85°C	-1.06 -.96 -.89		-.89 -.81 -.70	Vdc
V_{OL}	Output Voltage	$V_{IN} = V_{IH}$ MAX., V_{IL} MIN.	-30°C 25°C 85°C	-1.89 -1.85 -1.825		-1.675 -1.65 -1.615	Vdc
V_{OHA}	Output Voltage (Threshold)	$V_{IN} = V_{IHA}, V_{ILA}$	-30°C 25°C 85°C	-1.08 -.98 -.91			Vdc
V_{OLA}	Output Voltage (Threshold)	$V_{IN} = V_{IHA}, V_{ILA}$	-30°C 25°C 85°C			-1.655 -1.63 -1.595	Vdc

SWITCHING CHARACTERISTICS V_{EE} = -3.2V, V_{CC} = 2V, R_L = 50Ω TO GND

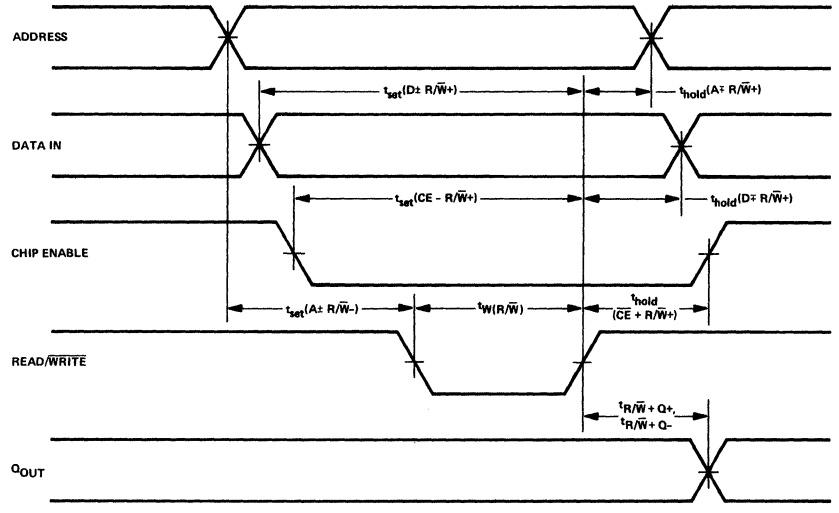
PARAMETER		MIN	TYP	MAX	UNITS
$t_{\overline{CE}-}$ Q+, $t_{\overline{CE}+}$ Q–	Access Time – Chip Enable to Output		5.0	7.5	ns
t_{A+} Q +, t_{A-} Q +	Address to Output		8.5	13.0	ns
t_{A+} Q–, t_{A-} Q –					
	Write Strobe Mode				
$t_{SET(D\pm\ R/\overline{W}+)}$	Data Set-up	11.0	7.5		ns
$t_{SET(CE-\ R/\overline{W}+)}$	Chip Enable Set-up	16.5	11.0		ns
$t_{SET(A\pm\ R/\overline{W}-)}$	Address	5.3	3.5		ns
$t_{HOLD(D\mp\ R/\overline{W}+)}$	Data Hold	4.5	3.0		ns
$t_{HOLD(\overline{CE}+\ R/\overline{W}+)}$	Chip Enable Hold	4.5	3.0		ns
$t_{HOLD(A\mp\ R/\overline{W}+)}$	Address Hold	5.3	3.5		ns
$t_{R/\overline{W}+}$ Q+, $t_{R/\overline{W}+}$ Q–	Recovery Time		7.5	11.0	ns
$t_{W(R/\overline{W})}$	Write Pulse Width	11.0	7.5		ns
	Chip Enable Strobe Mode				
$t_{SET(D\pm\ \overline{CE}+)}$	Data Set-up	11.0	7.5		ns
$t_{SET(R/\overline{W}-\ \overline{CE}+)}$	Read/$\overline{\text{Write}}$ Set-up	16.5	11.0		ns
$t_{SET(A\pm\overline{CE}-)}$	Address Set-up	4.5	3.0		ns
$t_{HOLD(D\mp\overline{CE}+)}$	Data Hold	4.5	3.0		ns
$t_{HOLD(R/\overline{W}+\overline{CE}+)}$	Read/$\overline{\text{Write}}$ Hold	4.5	3.0		ns
$t_{HOLD(A\mp\ CE+)}$	Address Hold	4.5	3.0		ns
$t_{W(\overline{CE})}$	Chip Enable Pulse Width	11.0	7.5		ns
t_+	Rise Time (20%–80%)	1.1	2.5	4.0	ns
t_-	Fall Time (20%–80%)	1.1	2.5	4.0	ns

TEST VOLTAGE VALUES
Vdc ± 1%

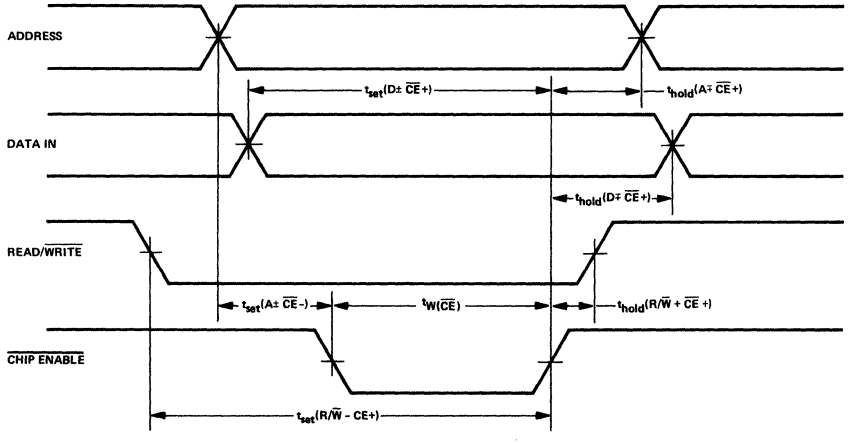
@ Test Temperature	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

TIMING DIAGRAMS

WRITE CYCLE
READ/WRITE STROBE MODE

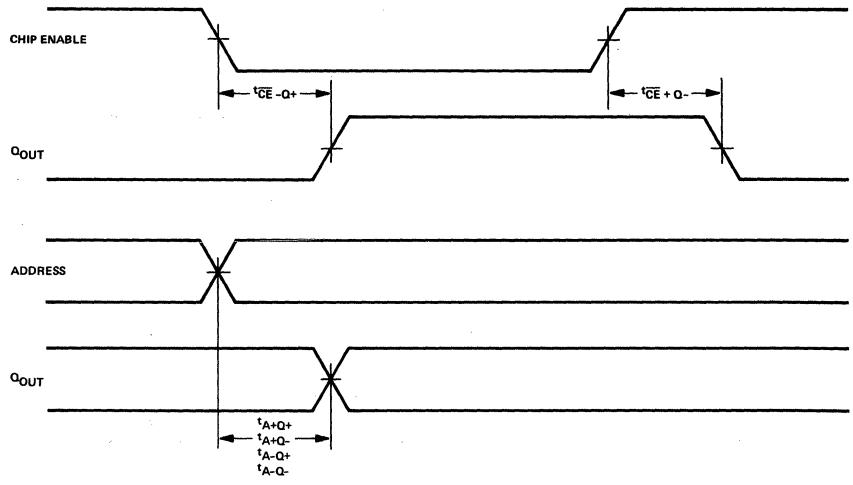


WRITE CYCLE
CHIP ENABLE STROBE MODE

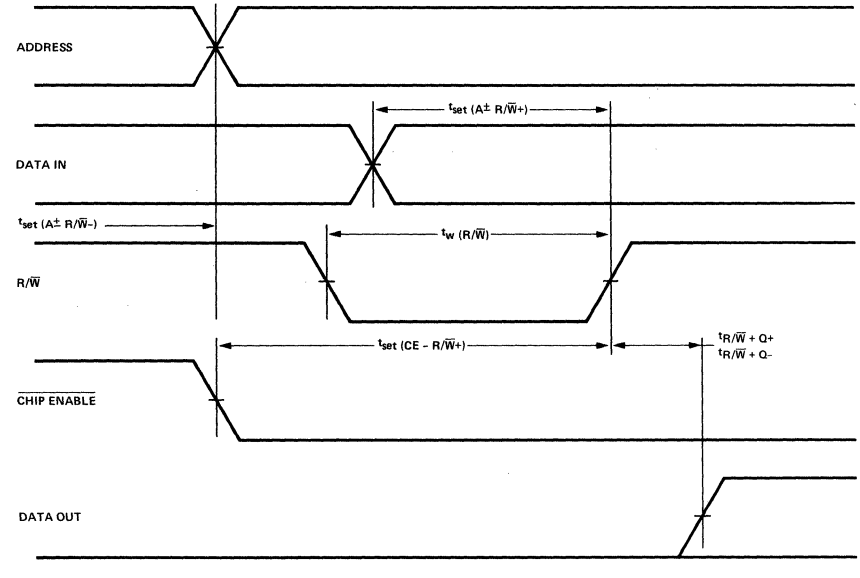


TIMING DIAGRAMS (Cont'd)

READ CYCLE



WRITE/READ CYCLE



DESCRIPTION

The 10165 is a device designed to provide a 3 bit binary coded output for each of 8 input lines. Priority selection circuitry is included so that the output reflects the highest priority input present and ignores lower order inputs. Each of the outputs is stored in a D type latch which allows synchronous sample and store operation. The operation of the latch may be bypassed by holding the C input low. The Q_3 output is high when any of the inputs are high. This allows extension to another device when more than 8 inputs are to be encoded.

FEATURES

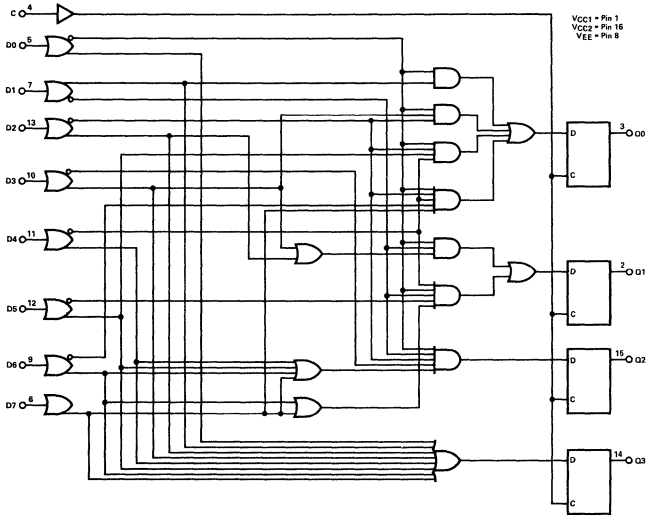
- HIGH FUNCTIONAL DENSITY REDUCES PACKAGE COUNT
- FAST PROPAGATION DELAY = 7.0ns TYPICAL
- LOW POWER DISSIPATION = 545mW/PACKAGE TYPICAL (NO LOAD)
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- HIGH Z INPUTS – INTERNAL 50kΩ RESISTORS
- HIGH FANOUT CAPABILITY – CAN DRIVE 50Ω LINES
- CONTROLLED OUTPUT RISE AND FALL TIMES – –2.0ns TYPICAL (20% TO 80%) (ALL OUTPUTS LOADED)
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS – V_{EE} = –5.2V ±5% RECOMMENDED

TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	Ø	Ø	Ø	Ø	Ø	Ø	Ø	H	L	L	L
L	H	Ø	Ø	Ø	Ø	Ø	Ø	H	L	L	H
L	L	H	Ø	Ø	Ø	Ø	Ø	H	L	H	L
L	L	L	H	Ø	Ø	Ø	Ø	H	L	H	H
L	L	L	L	H	Ø	Ø	Ø	H	H	L	L
L	L	L	L	L	H	Ø	Ø	H	H	L	H
L	L	L	L	L	L	H	Ø	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

Ø = Don't Care
P_D = 545mW typ/pkg (No Load)
t_{pd} = 7.0ns typ (Data to Output)

LOGIC DIAGRAMS



ELECTRICAL CHARACTERISTICS

(At Listed Voltages and Ambient Temperatures)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

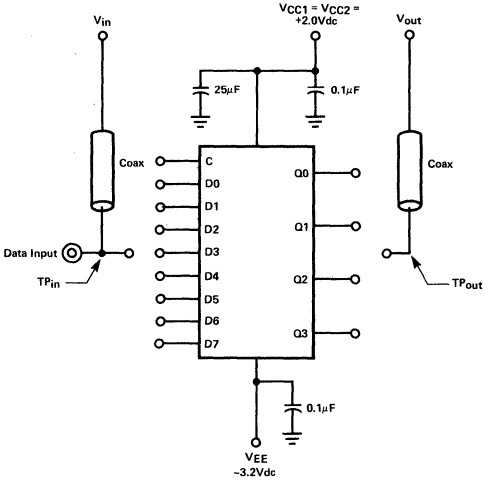
CHARACTERISTIC	SYMBOL	PIN UNDER TEST	10165 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNIT	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	105	131	–	–	mADC	–	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	245	–	–	μADC	4	–	–	–	8	1,16
		5	–	–	–	–	220	–	–	μADC	5 ①	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μADC	–	4	–	–	8	1,16
		5	–	–	0.5	–	–	–	–	μADC	–	5 ①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	VDC	6	4	–	–	8	1,16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	VDC	6	4	–	–	8	1,16
		14	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	VDC	6	4	–	–	8	1,16
		15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	VDC	6	4	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	VDC	–	4	–	–	8	1,16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	VDC	–	4	–	–	8	1,16
		14	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	VDC	–	4	–	–	8	1,16
		15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	VDC	–	4	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	VDC	–	4	6	–	8	1,16
		3	-1.080	–	-0.980	–	–	-0.910	–	VDC	–	4	6	–	8	1,16
		14	-1.080	–	-0.980	–	–	-0.910	–	VDC	–	4	6	–	8	1,16
		15	-1.080	–	-0.980	–	–	-0.910	–	VDC	–	4	6	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	VDC	–	4	–	6	8	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	VDC	–	4	–	6	8	1,16
		14	–	-1.655	–	–	-1.630	–	-1.595	VDC	–	4	–	6	8	1,16
		15	–	-1.655	–	–	-1.630	–	-1.595	VDC	–	4	–	6	8	1,16
Switching Time (50-ohm Load)										UNIT	+1.11V	+0.31V	Pulse In	Pulse Out	-3.2V	+2.0V
Propagation Delay																
Data Input	t_{5+14+}	14	–	–	–	7.0	–	–	–	nS	–	4	5	14	8	1,16
	t_{5-14-}	14	–	–	–	7.0	–	–	–	nS	–	4	5	14	8	1,16
	t_{7+3+}	3	–	–	–	7.0	–	–	–	nS	–	4	7	3	8	1,16
	t_{11+15+}	15	–	–	–	7.0	–	–	–	nS	–	4	11	15	8	1,16
	t_{13+2+}	2	–	–	–	7.0	–	–	–	nS	–	4	13	2	8	1,16
Clock Input	t_{4-3+}	3 ②	–	–	–	7.0	–	–	–	nS	7	–	4	3	8	1,16
	t_{4-3-}	3 ③	–	–	–	7.0	–	–	–	nS	–	–	4	3	8	1,16
	t_{4-14+}	14 ②	–	–	–	7.0	–	–	–	nS	7	–	4	14	8	1,16
	t_{4-14-}	14 ③	–	–	–	7.0	–	–	–	nS	–	–	4	14	8	1,16
Setup Time	t_{setup} H	3	–	–	–	3.4	–	–	–	nS	–	–	4,7	3	8	1,16
	t_{setup} L	3	–	–	–	3.0	–	–	–	nS	–	–	4,7	3	8	1,16
Hold Time	t_{hold} H	3	–	–	–	-2.3	–	–	–	nS	–	–	4,7	3	8	1,16
	t_{hold} L	3	–	–	–	-2.7	–	–	–	nS	–	–	4,7	3	8	1,16
Rise Time (20% to 80%)	t_{3+}	3	–	–	–	2.0	–	–	–	nS	–	4	7	3	8	1,16
Fall Time (20% to 80%)	t_{3-}	3	–	–	–	2.0	–	–	–	nS	–	4	7	3	8	1,16

① The same limit applies for all D type input pins. To test input currents for other D inputs, individually apply proper voltage to pin under test.

② Output latched to low state prior to test.

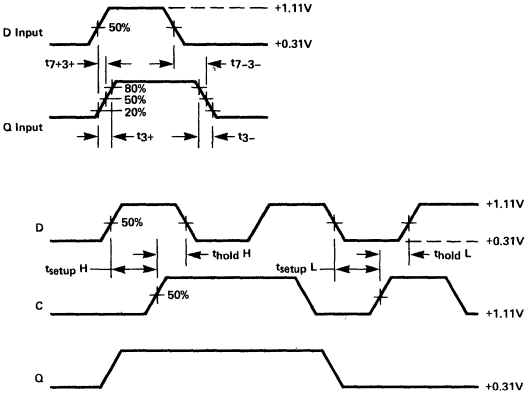
③ Output latched to high state prior to test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

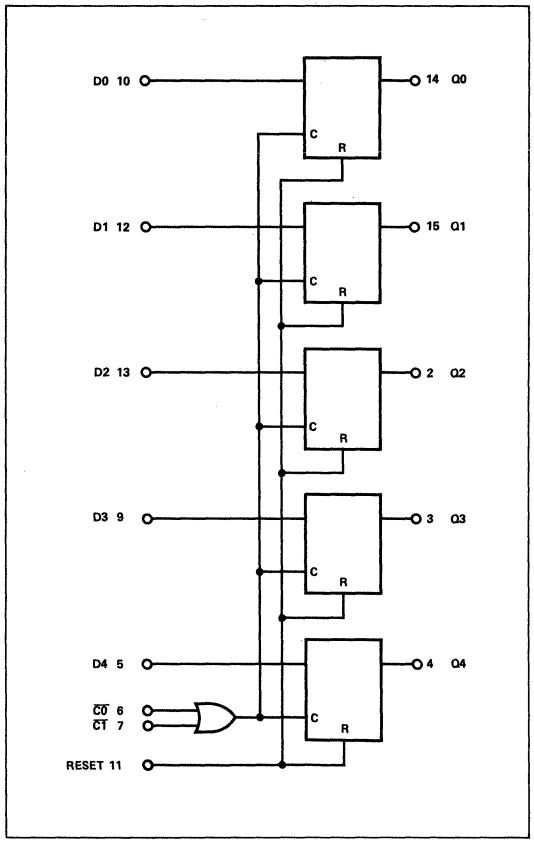
DESCRIPTION

The 10175 is a device which incorporates five D type latches with a common reset and two-input clock. While both of the clock inputs are low the outputs will follow the inputs. The outputs are latched when either of the clocks goes high. The reset is enabled only when the clock is in the high state. Open emitter outputs permit the device to be wire "OR"ed with other open emitter outputs.

FEATURES

- HIGH SPEED – 2.5ns DATA TO OUTPUT DELAY TYPICAL
- COMMON ASYNCHRONOUS RESET FUNCTION
- HIGH Z INPUTS – INTERNAL 50kΩ RESISTORS
- HIGH FANOUT CAPABILITY – DRIVES 50 OHMS
- CONTROLLED OUTPUT RISE AND FALL TIMES – 2ns TYPICAL
- TWO SEPARATE CLOCK PINS – CAN BE USED FOR CLOCK ENABLE FUNCTION

LOGIC DIAGRAM

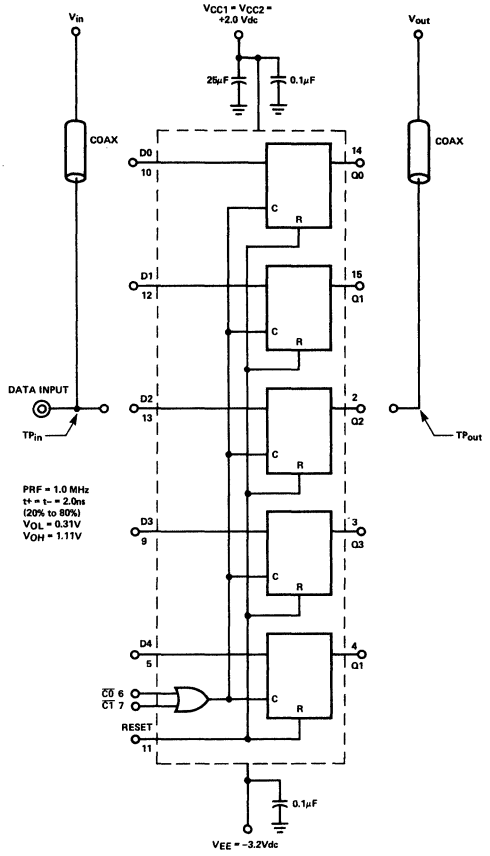


TRUTH TABLE

D	C0	C1	RESET	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Q n
X	X	H	L	Q n
X	H	X	H	L
X	X	H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
P_D = 400mW typ/pkg (No Load)
t_{pd} = 2.5nS typ (Data to Output)

SWITCHING TIME TEST CIRCUIT

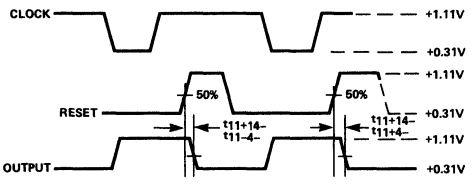


50-ohm termination to ground located in each scope channel input.

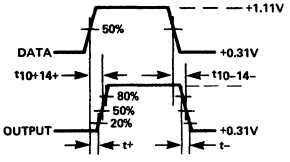
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<$1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

VOLTAGE WAVEFORMS

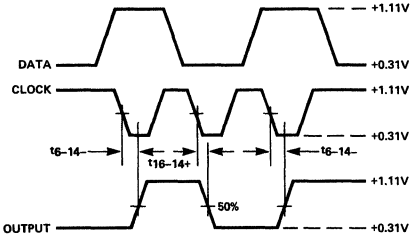
RESET INPUT

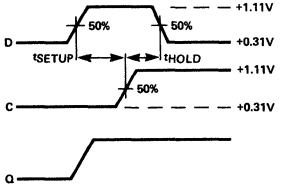


DATA INPUT



CLOCK INPUT





NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (c) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (c) that information must remain unchanged at the data input (D).

ELECTRICAL CHARACTERISTICS

(At Listed Voltages and Ambient Temperatures)

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

CHARACTERISTIC	SYMBOL	PIN UNDER TEST	10175 TEST LIMITS −30°C MIN	−30°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNIT	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	97	–	–	mADC	–	–	–	–	8	1,16
Input Current	I_{inH}	6	–	–	–	–	290	–	–	μADC	6	–	–	–	8	1,16
		7	–	–	–	–	290	–	–	μADC	7	–	–	–	8	1,16
		10	–	–	–	–	290	–	–	μADC	10	–	–	–	8	1,16
		11	–	–	–	–	650	–	–	μADC	11	–	–	–	8	1,16
Input Leakage Current	I_{inL}	All	–	–	0.5	–	–	–	–	μADC	–	①	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	14	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	VDC	10	6	–	–	8	1,16
		15	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	VDC	12	6	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	14	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	VDC	–	6,10	–	–	8	1,16
		15	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	VDC	–	6,12	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	14	−1.080	–	−0.980	–	–	−0.910	–	VDC	–	6	10	–	8	1,16
		15	−1.080	–	−0.980	–	–	−0.910	–	VDC	–	6	12	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	14	–	−1.655	–	–	−1.630	–	−1.595	VDC	–	6	–	10	8	1,16
		15	–	−1.655	–	–	−1.630	–	−1.595	VDC	–	6	–	12	8	1,16
Switching Times											+1.11V	+0.31V	Pulse In	Pulse Out	−3.2V	+2.0V
Data Input	t_{10+14+}	14	–	–	–	2.5	–	–	–	nS	–	6,7	10	14	8	1,16
	t_{10-14-}	14	–	–	–	2.5	–	–	–	nS	–	6,7	10	14	8	1,16
Clock Input	t_{6-14+}	14	–	–	–	3.3	–	–	–	nS	–	7	10,6	14	8	1,16
	t_{6-14-}	14	–	–	–	3.3	–	–	–	nS	–	7	10,6	14	8	1,16
Reset Input	t_{11+4-}	4	–	–	–	2.5	–	–	–	nS	5	6	7,11	4 ②	8	1,16
	t_{11+14-}	14	–	–	–	2.5	–	–	–	nS	10	6	7,11	14 ②	8	1,16
Setup Time	t_{setup}	14	–	–	–	1.5	–	–	–	nS	–	7	6,10	14	8	1,16
Hold Time	t_{hold}	14	–	–	–	0.5	–	–	–	nS	–	7	6,10	14	8	1,16
Rise Time (20% to 80%)	t^+	14	–	–	–	2.0	–	–	–	nS	–	6,7	10	14	8	1,16
Fall Time (20% to 80%)	t^-	14	–	–	–	2.0	–	–	–	nS	–	6,7	10	14	8	1,16

① Individually test each input; apply $V_{IL\ min}$ to pin under test.

② Output latched to high logic state prior to test.

DESCRIPTION

The 10176 contains six D-type master-slave flip flops in a single package. Data present on the "D" inputs are entered into all six master bistables when the common clock input is low. This data is subsequently transferred to the slave bistable when the clock goes from low to high. Thus, outputs change only on a positive-going clock input transition. Data present at the inputs, therefore, will not affect the outputs except on the low to high clock transition.

FEATURES

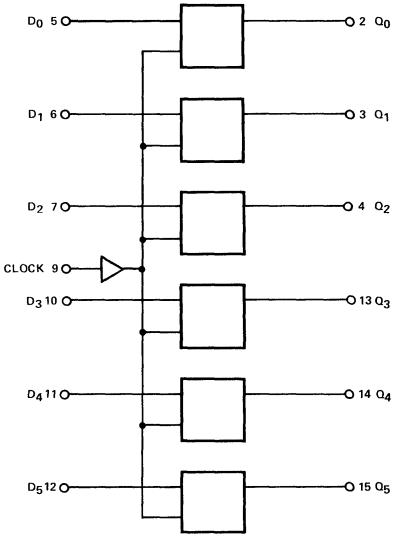
- HIGH SPEED
  - TOGGLE FREQUENCY = 150 MHz TYPICAL
  - PROPAGATION DELAY = 4.0 ns TYPICAL
- LOW POWER
  - 460 mW PER PACKAGE TYPICAL
- HIGH FANOUT
  - 50Ω DRIVE CAPABILITY
- HIGH Z INPUTS WITH 50KΩ PULLDOWN RESISTORS
- OPEN EMITTER OUTPUTS FOR BUSSING APPLICATIONS

TRUTH TABLE

C	D	On+1
L	Ø	Qn
L → H	L	L
L → H	H	H
H → L	Ø	Qn

Ø = Don't Care

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 2
V_{EE} = Pin 8

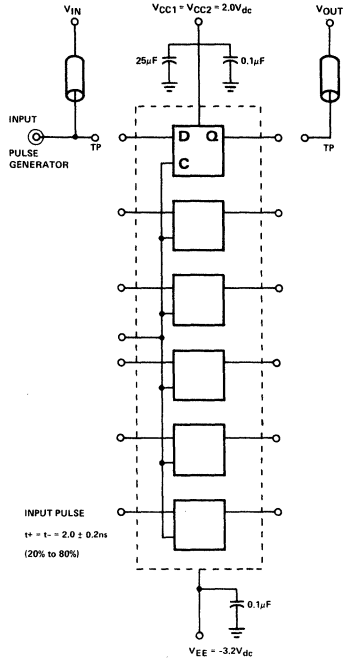
ELECTRICAL CHARACTERISTICS

(At Listed Voltages and Ambient Temperatures)

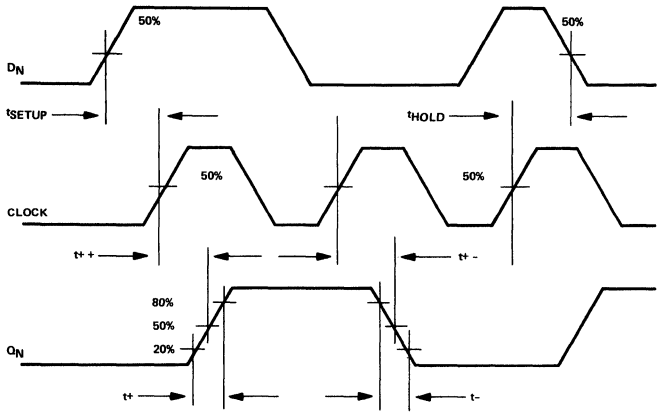
Test Temperature	Test Voltage Values (Volts) $V_{IH\ Max}$	$V_{IL\ Min}$	$V_{IHA\ Min}$	$V_{ILA\ Max}$	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristics	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage Applied to Pins Listed Below $V_{IH\ Max}$	$V_{IL\ Min}$	$V_{IHA\ Min}$	$V_{ILA\ Max}$	V_{EE}	(Vcc) Gnd
Power Supply Current	I_E	8				88	110			mAdc					8	1,16
Input Current	I_{InH}	5					220			μAdc	5				8	1,16
		9					310			μAdc	9				8	1,16
Input Leakage Current	I_{InL}	5			0.5					μAdc		5			8	1,16
		9			0.5					μAdc		9			8	1,16
Logic "1" Output Voltage	V_{OH}	15	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	12				8	1,16
Logic "0" Output Voltage	V_{OL}	15	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc		12			8	1,16
Logic "1" Threshold Voltage	V_{OHA}	15	-1.080	–	-0.980	–	–	-0.910	–	Vdc			12		8	1,16
Logic "0" Threshold Voltage	V_{OLA}	15	–	-1.655	–	–	-1.630	–	-1.595	Vdc				12	8	1,16
Switching Times											+1.11Vdc	+0.31Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Clock Input	t_{9+2+}	2				4.0				ns			5,9	2	8	1,16
Propagation Delay	t_{9+2-}	2				4.0				ns			5,9	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2				2.0				ns			5,9	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2				2.0				ns			5,9	2	8	1,16
Set up Time	t_{setup}	2				1.5				ns			5,9	2	8	1,16
Hold Time	t_{hold}	2				-0.5				ns			5,9	2	8	1,16
Toggle Frequency	f_{tog}	2			125	150				MHz			–	–	8	1,16

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°



NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50—ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50—ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50—ohm termination to ground is located in each scope input. Unused outputs are connected to a 50—ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

DESCRIPTION

The 10179 is a look-ahead carry device that can be used with the 10180 (dual arithmetic unit) or the 10181 (4 bit ALU) to perform high speed arithmetic on long words. The device is capable of examining carry data from four arithmetic units and generating both 2nd and 4th order look-ahead carries to greatly increase system speed over that which can be obtained using ripple-carry techniques.

Additional features of the 10179 include high Z inputs with pull down resistors to allow unused inputs to be left open and open-emitter outputs with 50Ω drive capability.

FEATURES

- **HIGH SPEED: PROPAGATION DELAY = 3.0 ns TYP CARRY, PROPAGATE 4.0 ns TYP GENERATE**
- **LOW POWER: 200mW TYP (NO LOAD)**
- **HIGH FAN OUT: CAN DRIVE 50Ω LINES**
- **HIGH Z INPUTS WITH 50kΩ PULL DOWN RESISTORS.**
- **OPEN EMITTER OUTPUTS**

LOGIC EQUATIONS

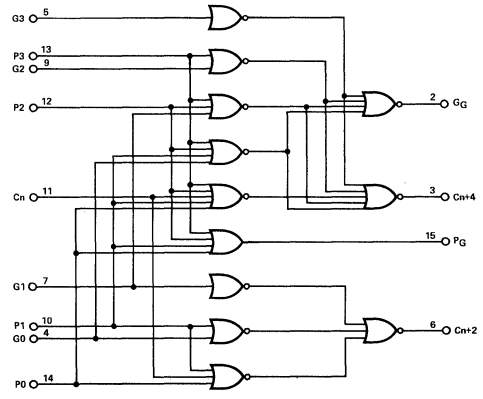
PG = P0 + P1 + P2 + P3

GG= (G0 + P1 + P2 + P3)
(G1 + P2 + P3)
(G2 + P3) G3

Cn+2= (Cn + P0 + P1)(G0 + P1) G1

Cn+4= (Cn + P0 + P1 + P2 + P3)
(G0 + P1 + P2 + P3)
(G1 + P2 + P3)(G2 + P3) G3

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
Positive Logic: High Level "1"

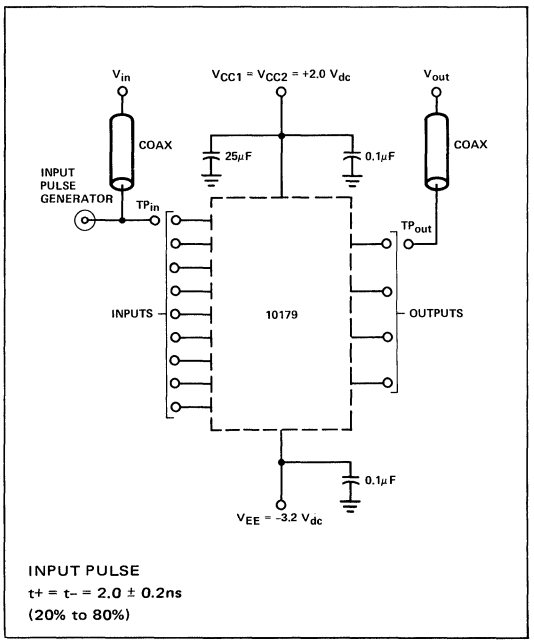
ELECTRICAL CHARACTERISTICS

(At Listed Voltages and Ambient Temperatures)

@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.3
+25°C	-0.810	-1.850	-1.105	-1.475	-5.3
+85°C	-0.700	-1.825	-1.035	-1.440	-5.3

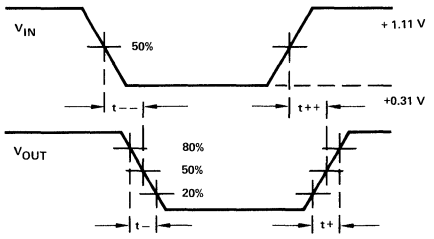
Characteristics	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	8	–	–	–	39	51	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	4, 7, 11	–	–	–	–	270	–	–	μAdc	4, 7, 11	–	–	–	8	1,16
		5, 9	–	–	–	–	225	–	–	μAdc	5, 9	–	–	–	8	1,16
		10, 13	–	–	–	–	440	–	–	μAdc	10, 13	–	–	–	8	1,16
		12	–	–	–	–	395	–	–	μAdc	12	–	–	–	8	1,16
		14	–	–	–	–	355	–	–	μAdc	14	–	–	–	8	1,16
	I_{inL}	4	–	–	0.5	–	–	–	–	μAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	VOE	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	4, 5, 7, 9	–	–	–	8	1,16
Logic "0" Output Voltage	VOL	3	-2.000	-1.675	-1.990	–	-1.650	-1.920	-1.675	Vdc	–	–	–	–	8	1,16
Logic "1" Threshold Voltage	VOHA	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	13	–	5	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	5, 12	–	9	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	5, 9	–	12	–	8	1,16
		2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	5	–	13	–	8	1,16
Logic "0" Threshold Voltage	VOLA	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	13	–	–	5	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	5	–	–	13	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	5	–	–	9	8	1,16
		2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	5, 9	–	–	12	8	1,16
Switching Time (50 Load)											+1.11		Pulse In	Pulse Out	-32V	+2.0V
	t_{11+6+}	6	–	–	1.0	3.0	4.5	–	–	ns	4, 7	–	11	6	8	1,16
	t_{11-6-}	6	–	–	1.0	3.0	4.5	–	–	ns	4, 7	–	11	6	8	1,16
	t_{5+2+}	2	–	–	1.0	4.0	5.5	–	–	ns	4, 7, 9	–	5	2	8	1,16
	t_{5-2-}	2	–	–	1.0	4.0	5.5	–	–	ns	4, 7, 9	–	5	2	8	1,16
Rise time (20% to 80%)	t_{6+}	6	–	–	0.8	3.5	5.5	–	–	ns	4, 7	–	11	6	8	1,16
Fall time (20% to 80%)	t_{6-}	6	–	–	0.8	3.5	5.5	–	–	ns	4, 7	–	11	6	8	1,16

SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t+ = t- = 2.0 ± 0.2ns
(20% to 80%)

PROPAGATION DELAY WAVEFORMS @ 25°C

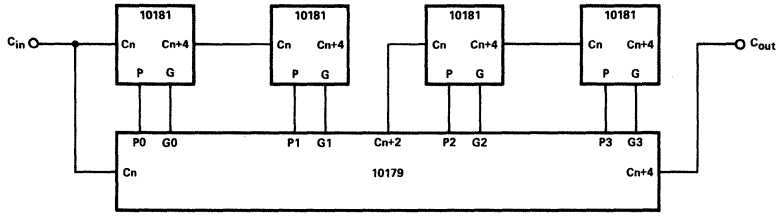


NOTES

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

APPLICATION

16-BIT ALU



DESCRIPTION

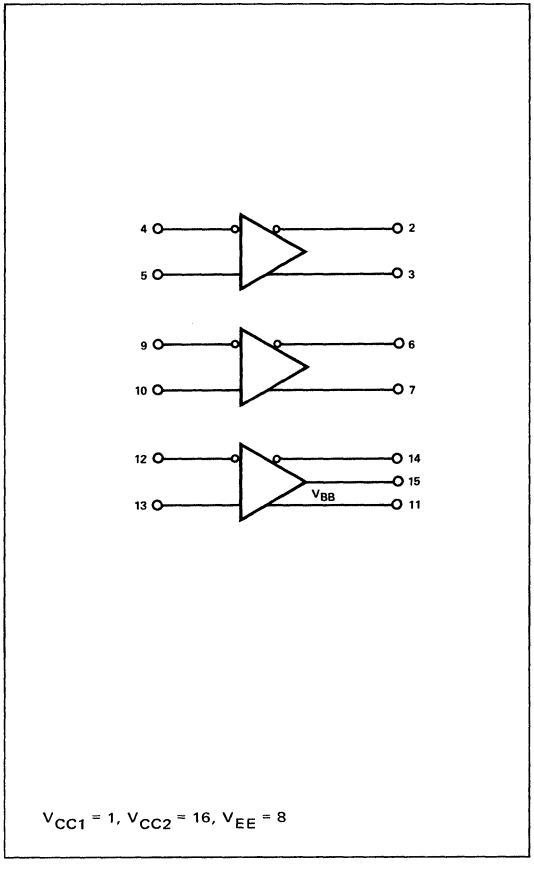
The 10216 is a high speed version of the 10116 triple differential line receiver with complementary outputs. It can be used for sensing either single-ended or differential signals over long transmission lines. To use the device in the single-ended mode, one of the input terminals is connected to the internal bias supply provided on pin 11. This supply can also be used with external resistors to provide hysterisis or for any application requiring a stable V_{BB} voltage level.

The 10216 is provided with active current sources for common mode noise rejection, but this requires that one input of any unused amplifier be connected to V_{BB} to prevent upsetting the current source bias network.

FEATURES

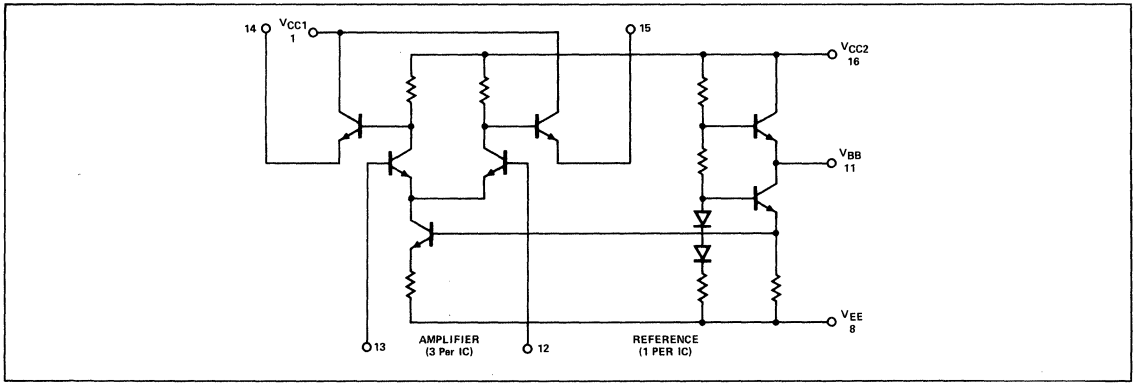
- GOOD COMMON MODE NOISE REJECTION
- FAST PROPAGATION DELAY =
  1.8ns TYP (SINGLE-ENDED)
  1.5ns TYP (DIFFERENTIAL)
- LOW POWER DISSIPATION = 100mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY—CAN DRIVE 50Ω LINES
- VERY HIGH INPUT Z (NO 50k PULLDOWNS)
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS (−5.2V ± 5% RECOMMENDED)
- COMPLEMENTARY OUTPUTS
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- V_{BB} VOLTAGE AVAILABLE ON PIN 11
- PIN COMPATIBLE WITH 10116

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

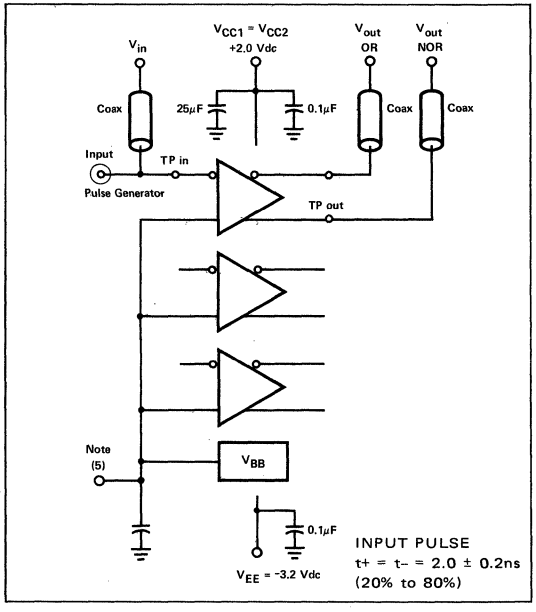
(At Listed Voltages and Ambient Temperatures)

@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	From	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	Pin	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	11	−5.2

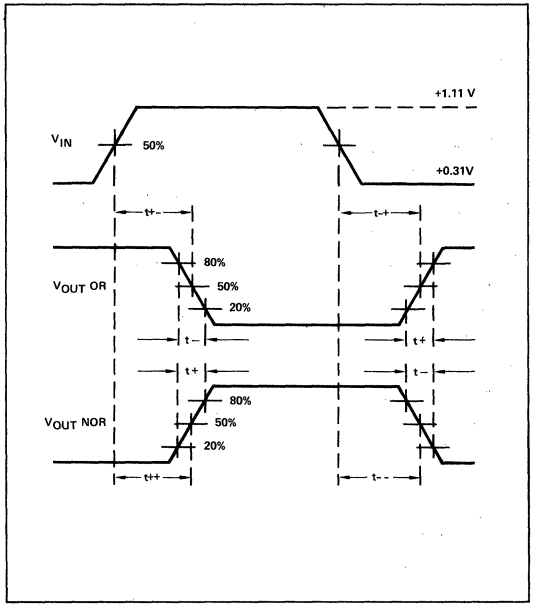
Characteristics	Symbol	Pin Under Test	Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage Applied to Points Below: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	20	25	–	–	mAdc	–	4,9,12	–	–	5,10,13	8	1,16
	I_{inH}	4	–	–	–	–	115	–	–	μAdc	4	9,12	–	–	5,10,13	8	1,16
	I_{CBO}	4	–	–	–	–	1.0	–	–	μAdc	–	9,12	–	–	5,10,13	8,4	1,16
High Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	4	9,12	–	–	5,10,13	8	1,16
		3	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	9,12	4	–	–	5,10,13	8	1,16
Low Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	9,12	4	–	–	5,10,13	8	1,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4	9,12	–	–	5,10,13	8	1,16
High Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	9,12	4	–	5,10,13	8	1,16
		3	−1.080	–	−0.980	–	–	−0.910	–	Vdc	9,12	–	–	4	5,10,13	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	9,12	–	4	5,10,13	8	1,16
		3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	9,12	–	4	–	5,10,13	8	1,16
Reference Voltage	V_{BB}	11	−1.420	−1.280	−1.350	–	−1.230	−1.295	−1.150	Vdc	–	–	–	–	5,10,13	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out		−3.2V	+2.0V
Propagation Delay	t_{4+2+}	2	–	–	1.0	1.8*	2.5	–	–	ns	–	–	4	2	5,10,13	8	1,16
	t_{4-2-}	2	–	–	1.0	1.8*	2.5	–	–	ns	–	–	4	2	5,10,13	8	1,16
	t_{4+3-}	3	–	–	1.0	1.8*	2.5	–	–	ns	–	–	4	3	5,10,13	8	1,16
	t_{4-3+}	3	–	–	1.0	1.8*	2.5	–	–	ns	–	–	4	3	5,10,13	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.0	1.5	2.5	–	–	ns	–	–	4	2	5,10,13	8	1,16
	t_{3+}	3	–	–	1.0	1.5	2.5	–	–	ns	–	–	4	3	5,10,13	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.0	1.5	2.5	–	–	ns	–	–	4	2	5,10,13	8	1,16
	t_{3-}	3	–	–	1.0	1.5	2.5	–	–	ns	–	–	4	3	5,10,13	8	1,16

*1.8 refers to single-ended drive; differential drive results in 1.5 ns delay.

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTES

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 3 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
5. One input from each gate must be tied to V_{BB} (Pin 11) during testing.

DESCRIPTION

The 10231 is a high performance dual master-slave type D flip-flop. Asynchronous set (S) and reset (R) override clock ($\overline{C}$) and clock enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flop-flop, the clock enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the date (D) input will not affect the output information at any other time due to master-slave construction. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

The 10231 is pin compatible with the 10130 dual D-type latch and the 10131 dual master-slave D-type flip-flop.

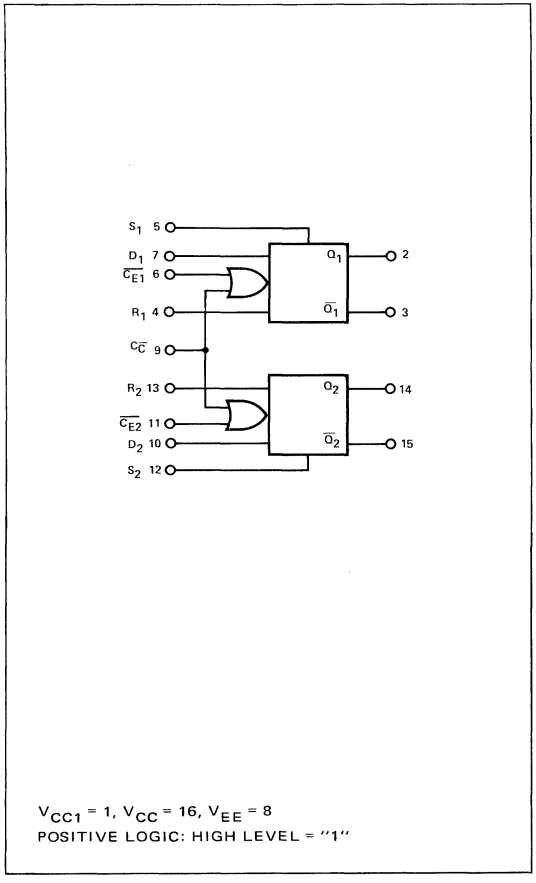
FEATURES

- f_{TOG} = 200 MHz MIN
  = 225 MHz TYP
- FAST PROPAGATION DELAY
  = 2.0 ns TYP (SET, RESET)
  = 2.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 270 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY—CAN DRIVE 50Ω LINES
- HIGH Z INPUTS – INTERNAL 50kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS V_{EE} = −5.2V ± 5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- PIN COMPATIBLE WITH 10130 and 10131

APPLICATIONS

CONTROL LOGIC
STATUS LOGIC
COUNTERS
SHIFT REGISTER
PRESCALERS

LOGIC DIAGRAM



V_{CC1} = 1, V_{CC} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

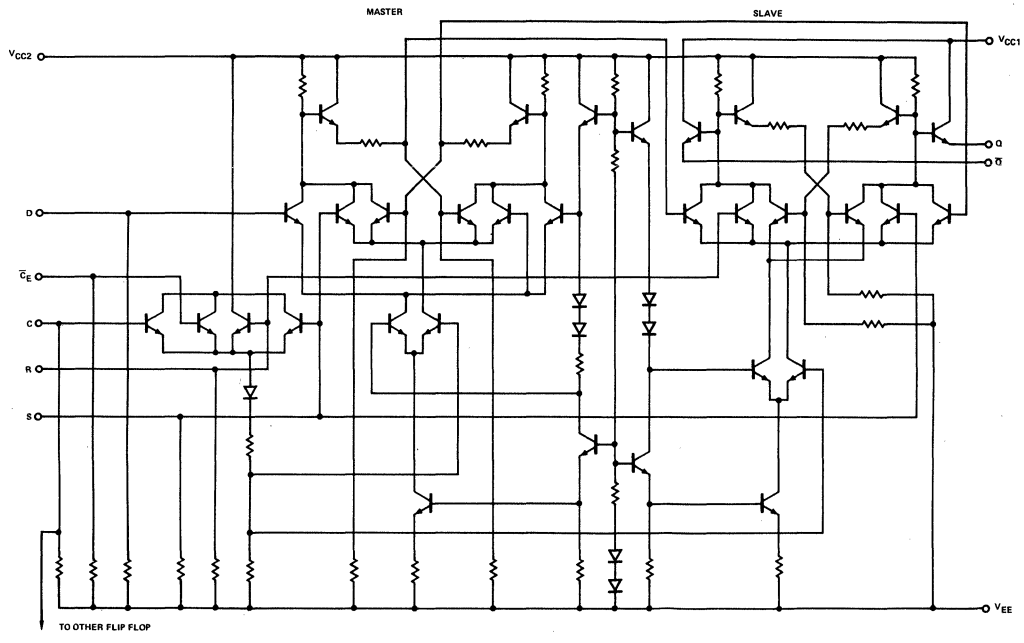
TRUTH TABLE

D	C*	S	R	Qn+1
Ø	L	L	L	Qn
L	H	L	L	L
H	H	L	L	H
Ø	*Ø	H	L	H
Ø	Ø	L	H	L
Ø	Ø	H	H	N.D.

*An H represents a transition from L to H between t=n and t=n + 1
C = C_C + CE
N.D. = not defined

CIRCUIT SCHEMATIC

10231 (1/2 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERICS

(At Listed Voltages and Ambient Temperatures)

@ Test Temperature	Test Voltage Values (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	Test Voltage Applied to Pins Listed Below $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	52	65	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	410	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	–	410	–	–	μAdc	5	–	–	–	8	1,16
		6	–	–	–	–	220	–	–	μAdc	6	–	–	–	8	1,16
		7	–	–	–	–	220	–	–	μAdc	7	–	–	–	8	1,16
		9	–	–	–	–	290	–	–	μAdc	9	–	–	–	8	1,16
Input Lockage Current	I_{inL}	4, 5*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,16
		6, 7, 9*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
		2+	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	5	–	–	–	8	1,16
		3+	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	5	–	8	1,16
		2+	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	–	7	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.665	–	–	-1.630	–	-1.595	Vdc	–	–	5	–	8	1,16
		3+	–	-1.665	–	–	-1.630	–	-1.595	Vdc	–	–	–	7	8	1,16
Switching Time Clock Input**											+1.11Vdc		pulse in	pulse out	-3.2 Vdc	+20 Vdc
Propagation Delay	t_{9-2-}	2	–	–	1.5	2.0	3.3	–	–	ns	–	–	9	2	8	1,16
	t_{9+2+}	2	–	–	1.5	2.0	3.3	–	–	ns	7	–	9	2	8	1,16
	t_{6+2+}	2	–	–	1.5	2.0	3.3	–	–	ns	7	–	6	2	8	1,16
	t_{6+2-}	2	–	–	1.5	2.0	3.3	–	–	ns	–	–	6	2	8	1,16
Rise Time (20% to 80%)	t_{2+}	2	–	–	1.0	1.3	3.1	–	–	ns	7	–	9	2	8	1,16
Fall Time (20% to 80%)	t_{2-}	2	–	–	1.0	1.3	3.1	–	–	ns	–	–	9	2	8	1,16
Set Input	t_{5+2+}	2	–	–	1.1	2.0	3.3	–	–	ns	–	–	5	2	8	1,16
Propagation Delay	t_{12+15+}	15	–	–	1.1	2.0	3.3	–	–	ns	–	–	12	15	8	1,16
	t_{5+3-}	3	–	–	1.1	2.0	3.3	–	–	ns	–	–	5	3	8	1,16
	t_{12+14-}	14	–	–	1.1	2.0	3.3	–	–	ns	–	–	12	14	8	1,16
Reset Input	t_{4+2-}	2	–	–	1.1	2.0	3.3	–	–	ns	–	–	4	2	8	1,16
	t_{13+15-}	15	–	–	1.1	2.0	3.3	–	–	ns	–	–	13	15	8	1,16
	t_{4+3+}	3	–	–	1.1	2.0	3.3	–	–	ns	–	–	4	3	8	1,16
	t_{13+14+}	14	–	–	1.1	2.0	3.3	–	–	ns	–	–	13	14	8	1,16
Setup Time	t_{setup}	7	–	–	1.1	–	–	–	–	ns	–	–	6,7	2	8	1,16
Hold Time	t_{hold}	7	–	–	0.75	–	–	–	–	ns	–	–	6,7	2	8	1,16
Toggle Frequency (max)	f_{Tog}	2	–	–	200	225	–	–	–	MHz	–	–	6	2	8	1,16

* Individually test each input; apply V_{IL} min to pin under test.

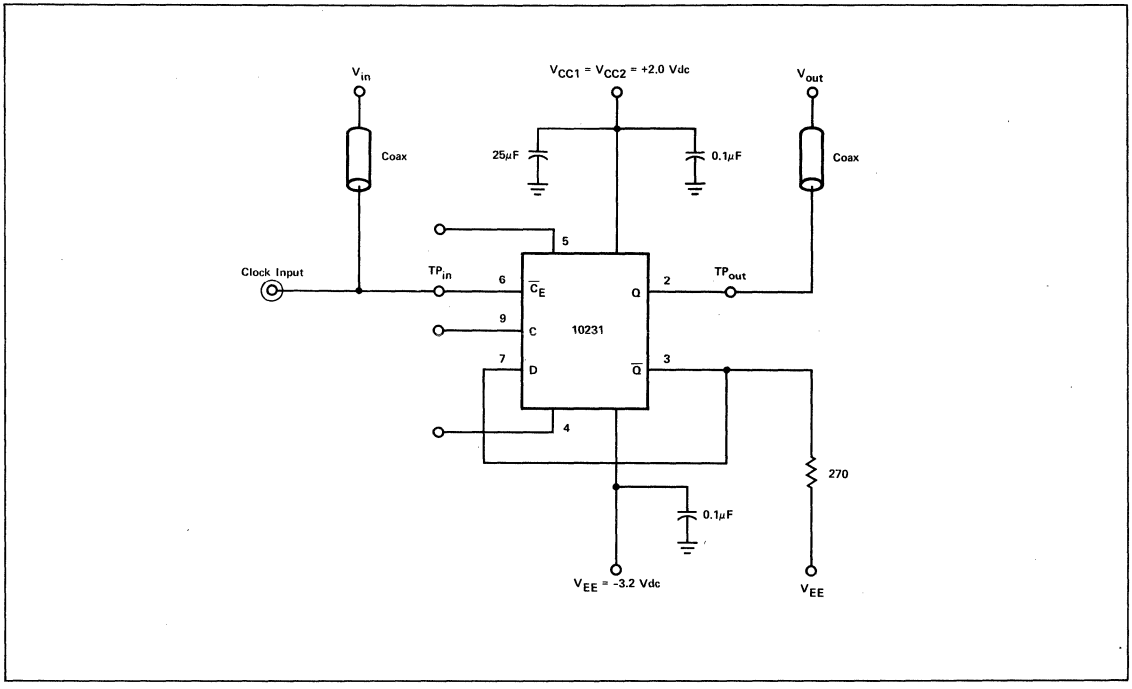
** Pin 3 is tied to pin 7 for these tests.

† Output level to be measured after a clock pulse has been applied to the C_E input (pin 6)

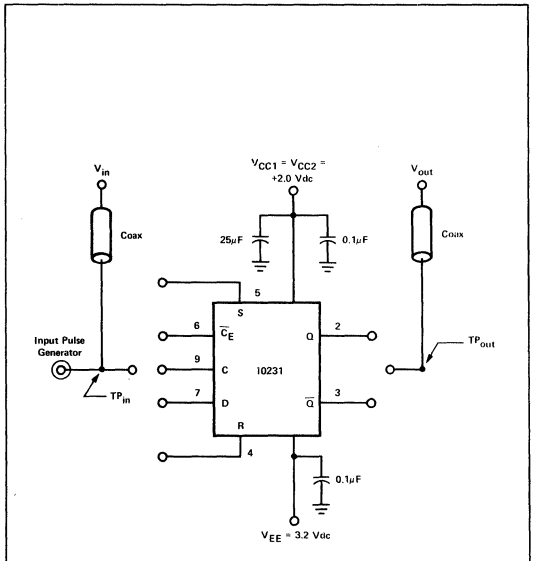
NOTES

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

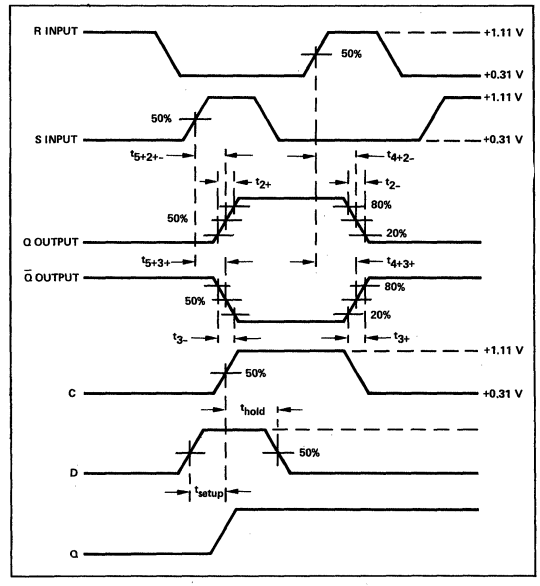
TOGGLE FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTE

Setup is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

Hold is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

DESCRIPTION

The ULN2208 is designed to provide the function of an FM gain block to be used primarily in FM and communications receivers.

The device consists of a three stage limiting amplifier which provides typically 34dB of gain. The device is operated from an internally regulated supply which is also provided at pin 6 for external use.

Input and output terminations of 330Ω and shunt capacitance of 7.0pF are required for use with 10.7MHz ceramic filters.

FEATURES

- **TYPICALLY 34dB GAIN AT 10.7MHz**
- **EXCELLENT TEMPERATURE STABILITY**
- **POWER SUPPLY REJECTION RATIO: 40dB TYPICAL**
- **OPERATING VOLTAGE RANGE: 10V–20V**

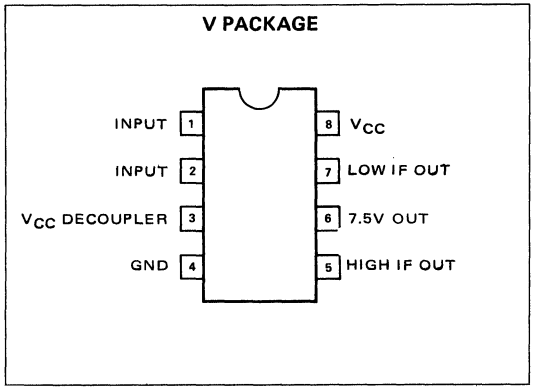
APPLICATIONS

FM STEREO SYSTEMS

COMMUNICATIONS RECEIVERS

FM RADIOS

PIN CONFIGURATION (Top View)

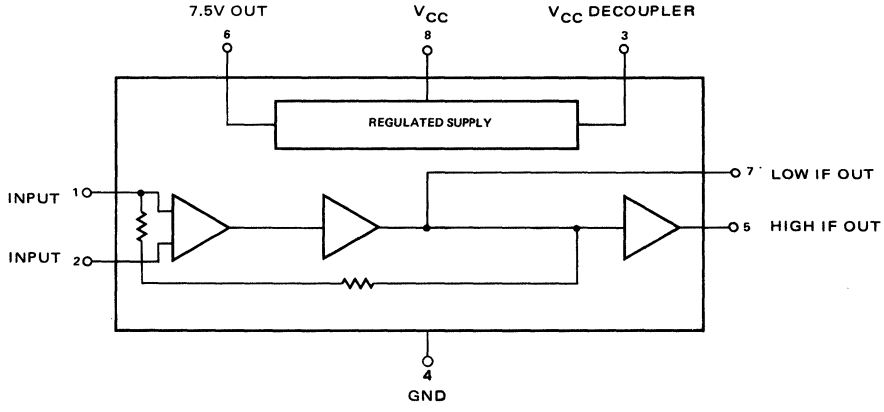


ABSOLUTE MAXIMUM RATINGS

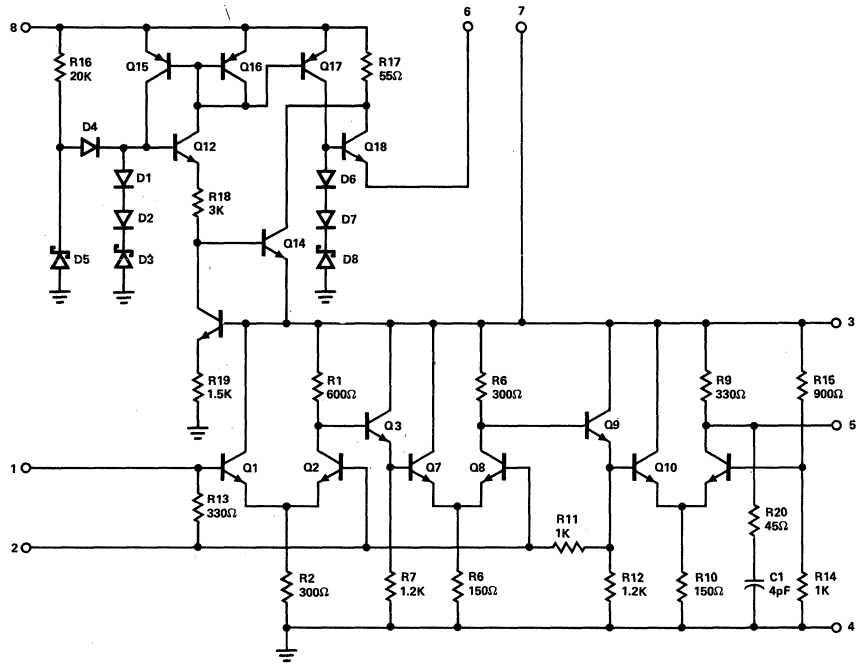
Supply Voltage, V_{CC}	20V
Supply Current, I_{CC}	22mA
Input Voltage (pins 1 and 3)	±3.0V
Power Consumption (Internal)	400mW
Output Current (pin 6)	10mA
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C

*Derate at the rate of 8.3mW/°C at temperatures above +25°C.

BLOCK DIAGRAM



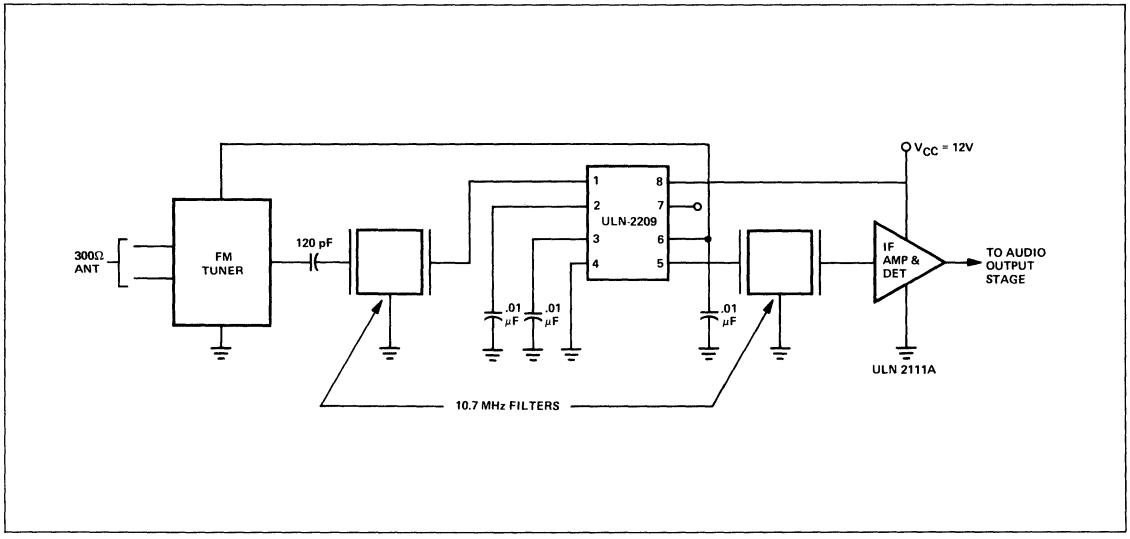
EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +12V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		14	18	22	mA
Total Device Dissipation				400	mW
Terminal Voltage	Pin 1		1.2		V
	Pin 2		1.2		V
	Pin 3		2.4		V
	Pin 5		2.0		V
	Pin 6		7.5		V
Input Limiting Threshold	F = 10.7MHz		400		μV
Output Voltage Swing	F = 10.7MHz		0.4		Vpp
Output Noise Voltage	F = 10.7MHz		1.5		mVrms
Input Impedance					
Parallel Input Resistance	F = 10.7MHz	270	330	390	Ω
Parallel Input Capacitance	F = 10.7MHz	5	7	10	pF
Output Voltage Gain	V_{IN} = 100 mVrms F = 1MHz	30	34	38	dB
Power Supply Rejection	V_{IN} = 250 mVrms F = 100Hz		-40		dB

TYPICAL APPLICATION



TYPE ULN2208 F-M GAIN BLOCK WITH VOLTAGE REGULATOR

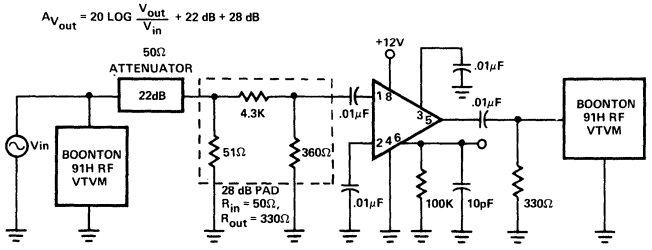


FIGURE 1

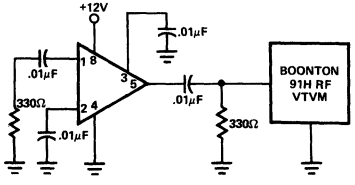


FIGURE 2

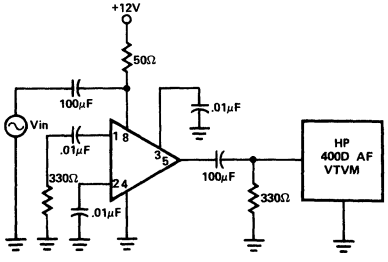


FIGURE 3

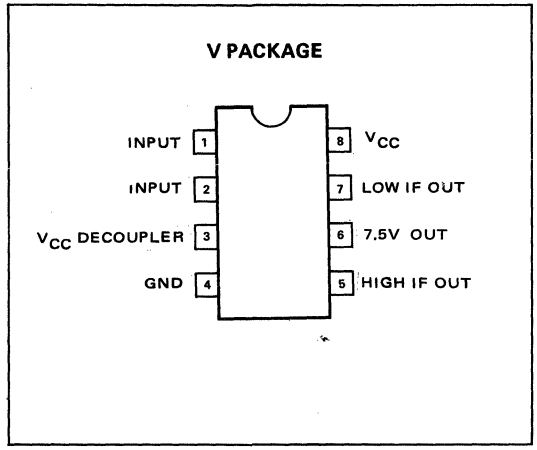
DESCRIPTION

The ULN 2209 is designed to provide the function of an FM gain block to be used primarily in FM and communications receivers.

The device consists of a four stage limiting amplifier which provides typically 48 dB of gain. The device is operated from an internally regulated supply which is also provided at pin 6 for external use.

Input and output terminations of 330Ω and shunt capacitance of 7.0 pF are required for use with 10.7 MHz ceramic filters.

PIN CONFIGURATION (Top View)



FEATURES

- TYPICALLY 50 dB GAIN AT 10.7 MHz
- EXCELLENT TEMPERATURE STABILITY
- POWER SUPPLY REJECTION RATIO: 40 dB TYPICAL
- OPERATING VOLTAGE RANGE: 10V–20V

APPLICATIONS

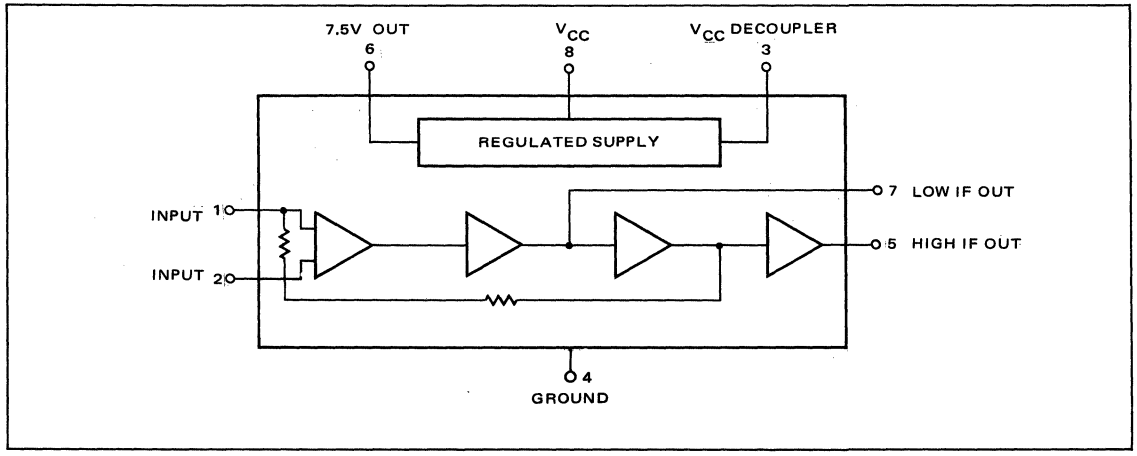
FM STEREO SYSTEMS
COMMUNICATIONS RECEIVERS
FM RADIOS

ABSOLUTE MAXIMUM RATINGS

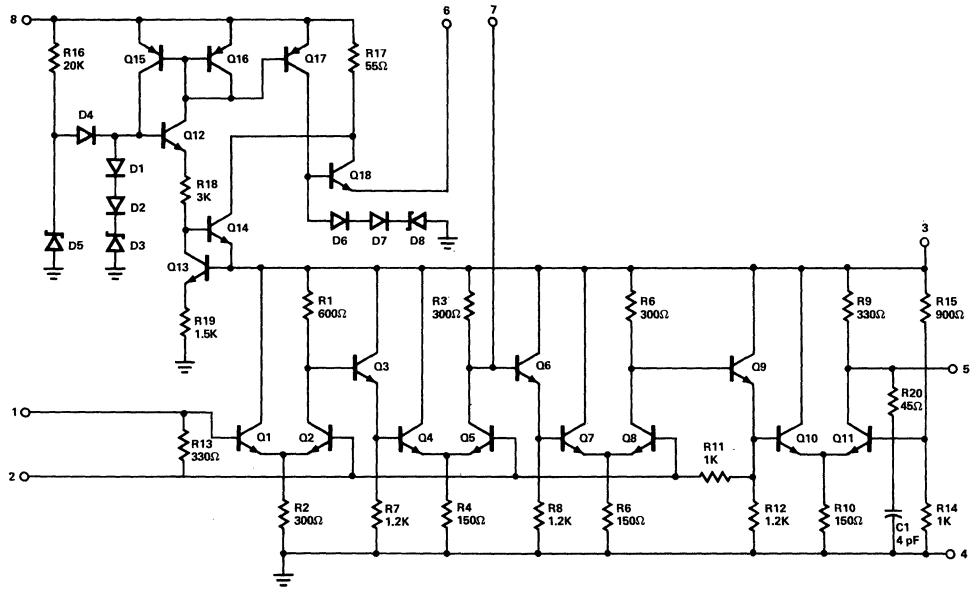
Supply Voltage, V_{CC}	20V
Supply Current, I_{CC}	22 mA
Input Voltage (pins 1 and 3)	±3,0V
Power Consumption (Internal)	400 mW
Output Current (pin 6)	10 mA
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

*Derate at the rate of 8.3 mW/°C at temperatures above +25°C.

BLOCK DIAGRAM



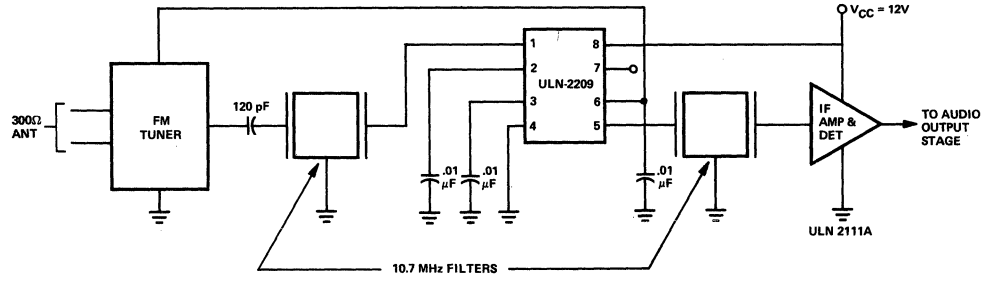
EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +12V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		14	18	22	mA
Total Device Dissipation				400	mW
Terminal Voltage	Pin 1		1.2		V
	Pin 2		1.2		V
	Pin 3		2.4		V
	Pin 5		2.0		V
	Pin 6		7.5		V
Input Limiting Threshold	F = 10.7 MHz		400		μV
Output Voltage Swing	F = 10.7 MHz		0.5		Vpp
Output Noise Voltage	F = 10.7 MHz		4		mVrms
Input Impedance					
Parallel Input Resistance	F = 10.7 MHz	270	330	390	Ω
Parallel Input Capacitance	F = 10.7 MHz	5	7	10	pF
Output Voltage Gain	V_{IN} = 100 mVrms F = 1 MHz	47	50	55	dB
Power Supply Rejection	V_{IN} = 250 mVrms F = 100 Hz		-40		dB

TYPICAL APPLICATION



TYPE ULN-2209 F-M GAIN BLOCK WITH VOLTAGE REGULATOR

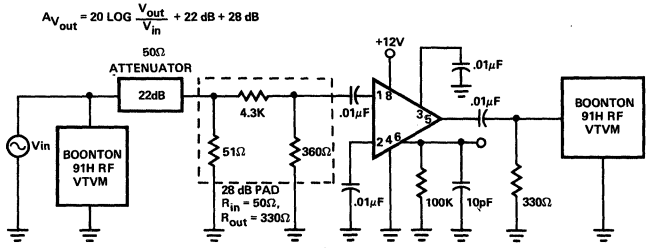


FIGURE 1

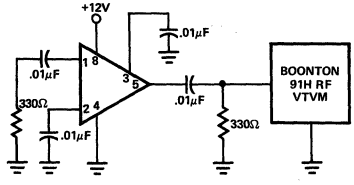


FIGURE 2

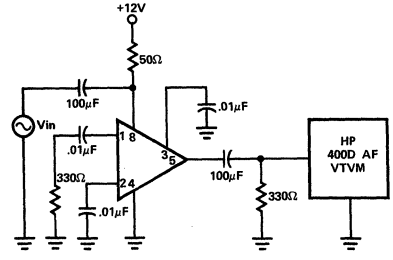


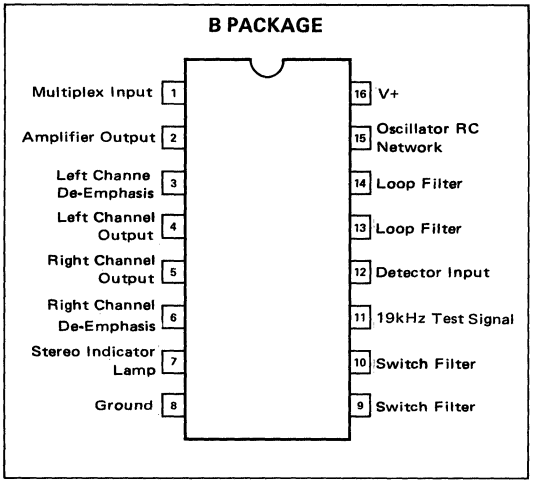
FIGURE 3

DESCRIPTION

The μA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

PIN CONFIGURATION (Top View)



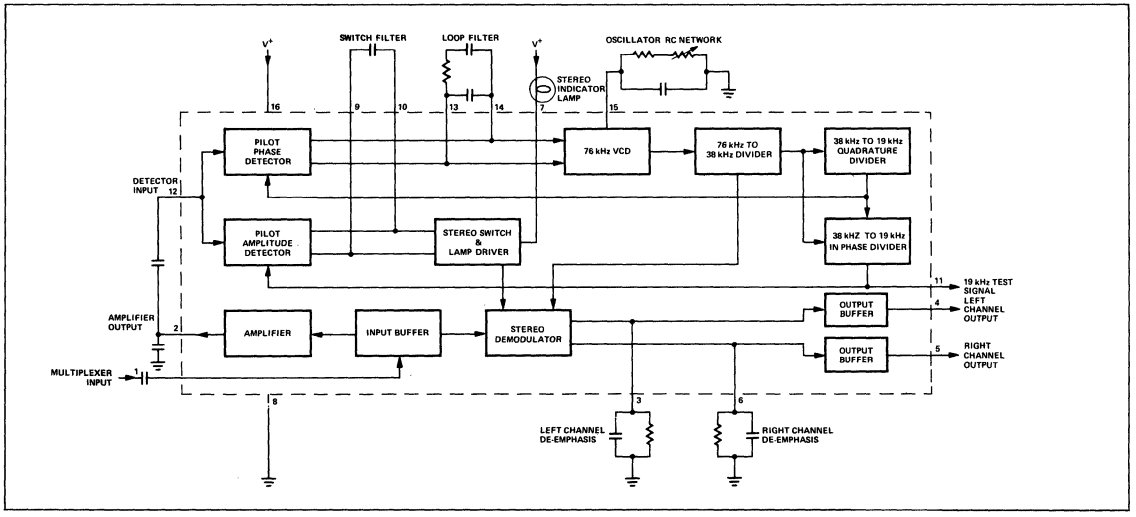
FEATURES

- **45dB CHANNEL SEPARATION**
- **AUTOMATIC STEREO/MONO SWITCHING**
- **70dB SCA REJECTION**
- **10V TO 16V SUPPLY RANGE**
- **HIGH IMPEDANCE INPUT – LOW IMPEDANCE OUTPUT**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Supply Voltage (≤15 Seconds)	+22V
Voltage at Lamp Driver Terminal (LAMP OFF)	+22V
Internal Power Dissipation*	730mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (60 Seconds)	300°C

BLOCK DIAGRAM



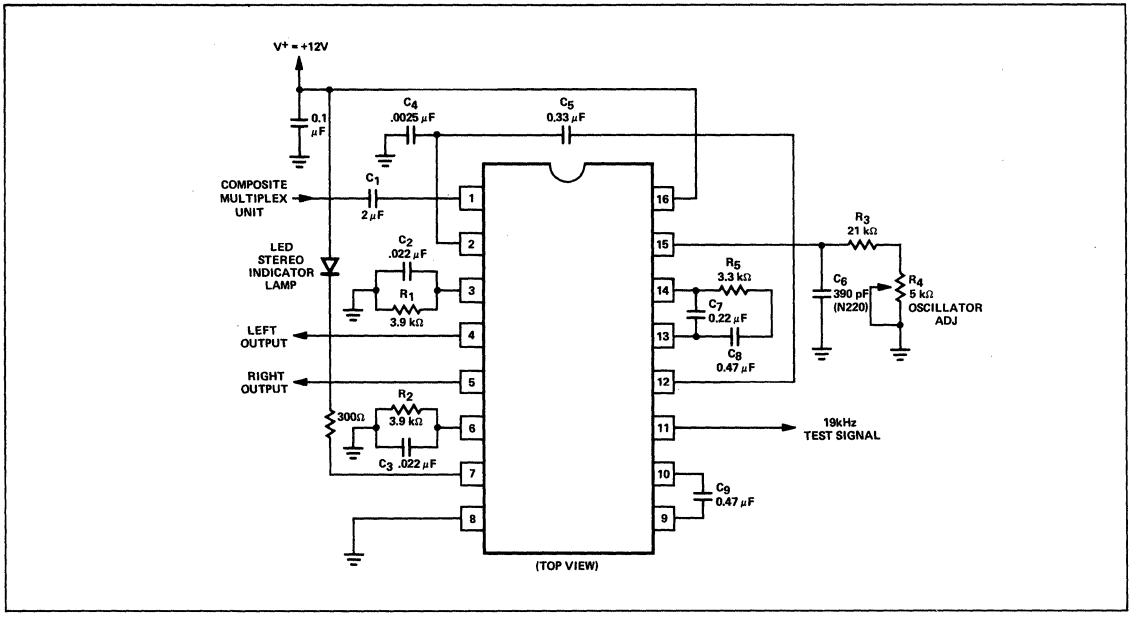
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +12V$, 19 kHz pilot level = 30 mV_{RMS}, Multiplex Signal (L = R, pilot OFF) = 300 mV_{RMS}, Modulation Frequency = 400 Hz or 1 kHz, Test Circuit 1, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Lamp OFF		26	35	mA
Maximum Available Lamp Current		75	150		mA
Voltage at Lamp Driver Terminal	LAMP = 50 mA		1.3	1.8	V
DC Voltage Shift at Either Output Terminal	Stereo to Mono Operation		30	150	mV
Power Supply Ripple Rejection	200 Hz, 200 mV_{RMS}	35			dB
Input Resistance		20	35		kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation	100 Hz		40		dB
	400 Hz	30	45		dB
	10 kHz		45		dB
Channel Balance			0.3	1.5	dB
Voltage Gain	1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level	Lamp Turn-On		15	20	mV_{RMS}
	Lamp Turn-Off	2.0	7.0		mV_{RMS}
Pilot Input Level Hysteresis	Lamp Turn-Off to Turn-On	3.0	7.0		dB
Capture Range		2.0	4.0	6.0	%
Total Harmonic Distortion	Multiplex Level = 600 mV_{RMS} Pilot OFF		0.4	1.0	%
19 kHz Rejection		25	35		dB
38 kHz Rejection		25	45		dB
SCA Rejection (Note 1)			70		dB
VCO Tuning Resistance (Note 2)		21.0	23.3	25.5	kΩ
VCO Frequency Drift	$0°C \leq T_A \leq 25°C$		+0.1	±2	%
	$25°C \leq T_A \leq 70°C$		−0.4	±2	%

NOTES:

1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit 1, required to set reference frequency at pin 11 to 19 kHz ± 10 Hz.

TEST CIRCUIT 1 AND TYPICAL APPLICATION

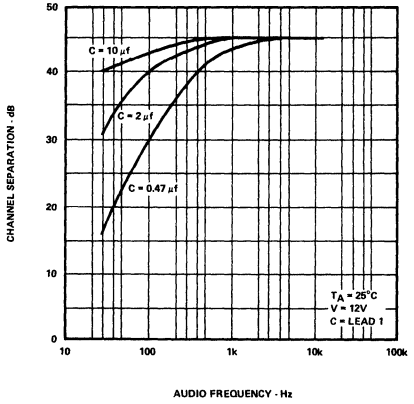


NOTE:

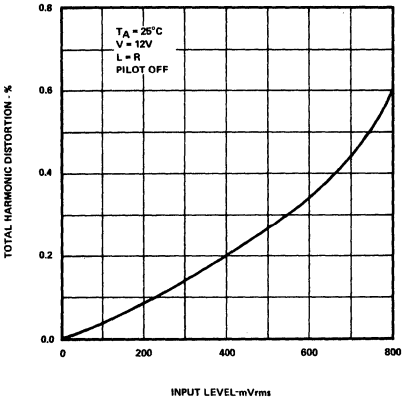
Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified. C_1 Tolerance = +100%, −20%, C_6 Tolerance = ±1% in test circuit and ±5% in typical application, R_3 Tolerance = ±1%, R_4 Tolerance = ±10%, R_1 and R_2 Tolerances = ±1% in test circuit and ±5% in typical application.

TYPICAL CHARACTERISTICS

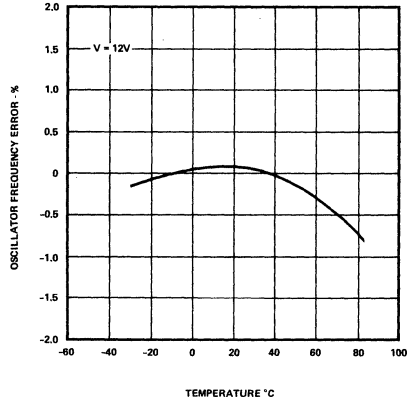
CHANNEL SEPARATION VS AUDIO FREQUENCY



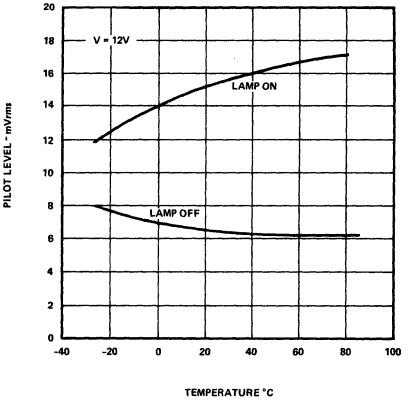
HARMONIC DISTORTION VS INPUT LEVEL



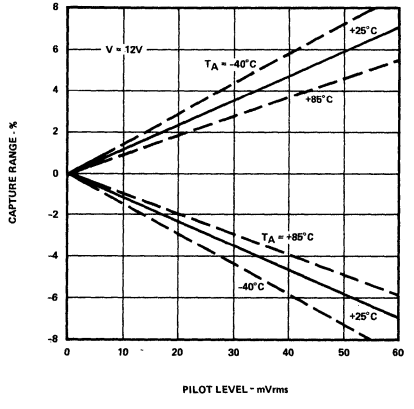
OSCILLATOR FREE RUNNING FREQUENCY ERROR VS AMBIENT TEMPERATURE



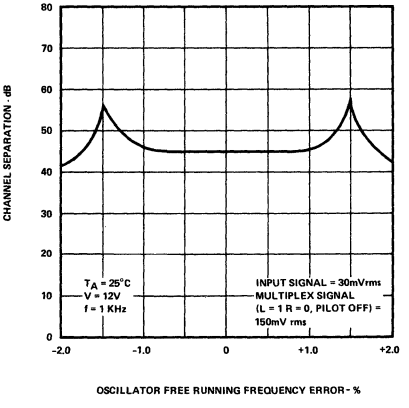
LAMP TURN ON & TURN OFF SENSITIVITY VS AMBIENT TEMPERATURE



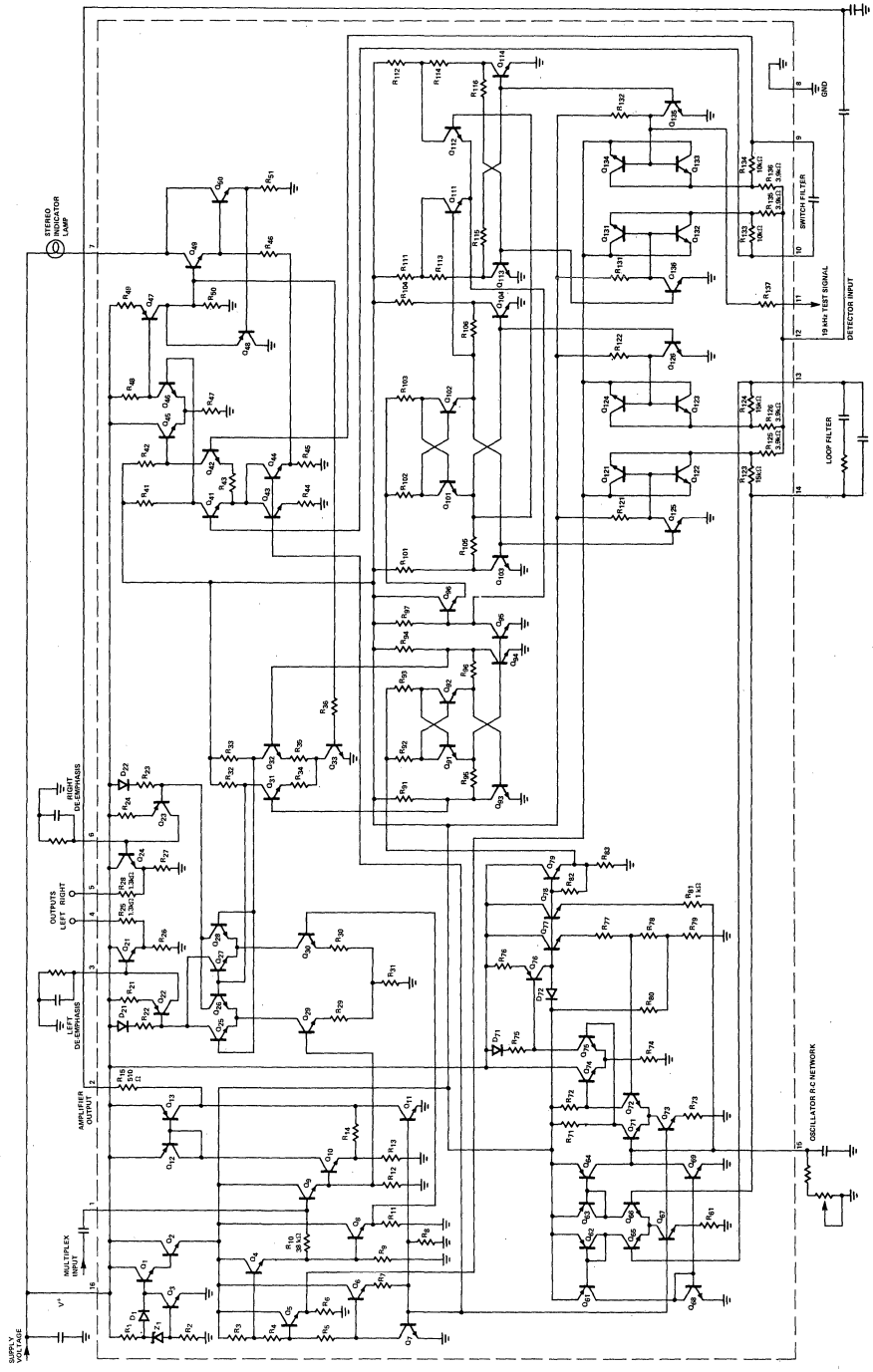
CAPTURE RANGES VS PILOT LEVEL



CHANNEL SEPARATION VS OSCILLATOR FREE RUNNING FREQUENCY ERROR



EQUIVALENT CIRCUIT



DESCRIPTION

The 532 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- INTERNALLY FREQUENCY COMPENSATED FOR UNITY GAIN
- LARGE DC VOLTAGE GAIN – 100dB
- WIDE BANDWIDTH (UNITY GAIN) – 1MHz (TEMPERATURE COMPENSATED)
- WIDE POWER SUPPLY RANGE
  SINGLE SUPPLY – 3V DC TO 30V DC
  OR DUAL SUPPLIES – ±1.5V DC TO ±15V DC
- VERY LOW SUPPLY CURRENT DRAIN (400μA) – ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE (1mW/OP AMP AT +5V DC)
- LOW INPUT BIASING CURRENT – 45nA DC (TEMPERATURE COMPENSATED)
- LOW INPUT OFFSET VOLTAGE – 2mV DC AND OFFSET CURRENT – 5nA DC
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE – 0V DC TO V^+ –1.5V DC SWING

UNIQUE FEATURES

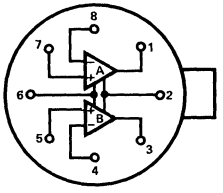
IN THE LINEAR MODE THE INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND AND THE OUTPUT VOLTAGE CAN ALSO SWING TO GROUND, EVEN THOUGH OPERATED FROM ONLY A SINGLE POWER SUPPLY VOLTAGE.

THE UNITY GAIN CROSS FREQUENCY IS TEMPERATURE COMPENSATED.

THE INPUT BIAS CURRENT IS ALSO TEMPERATURE COMPENSATED.

PIN CONFIGURATION (Top View)

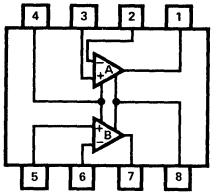
T PACKAGE



1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V^+

ORDER PART NOS. SE532T/SU532T/NE532T

V PACKAGE



1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V^+

ORDER PART NOS. SE532V/SU532V/NE532V

ABSOLUTE MAXIMUM RATINGS

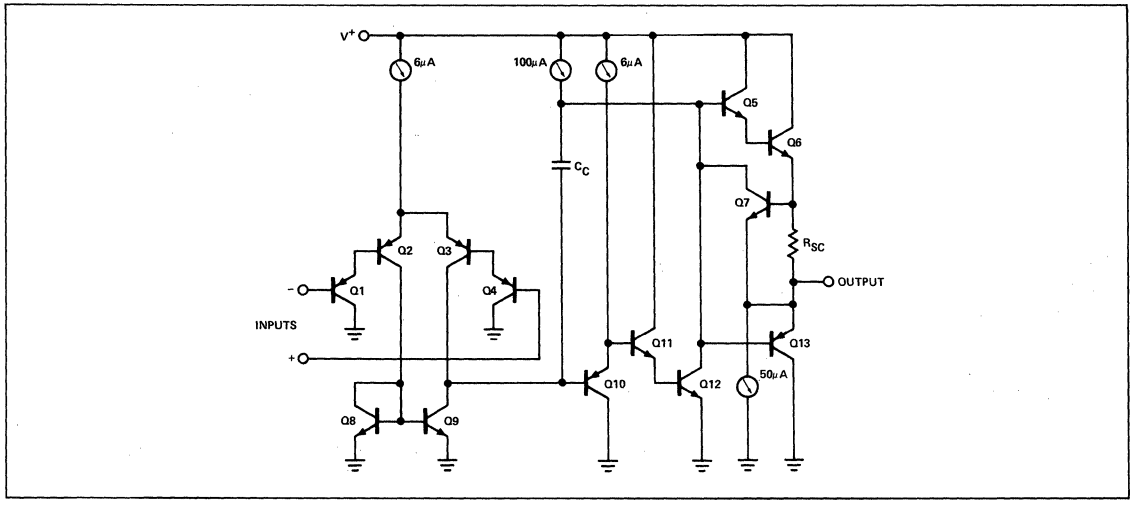
Supply Voltage, V^+	32V DC or ±16V DC
Differential Input Voltage	32V DC
Input Voltage	–0.3V DC to +32V DC
Power Dissipation (Note 1)	
T Package	680mW
V Package	625mW
Output Short-Circuit to GND (Note 2)	
$V^+ \leqslant$ 15V DC and T_A = 25°C	Continuous
Operating Temperature Range	
NE532	0°C to +70°C
SU532	–25°C to +85°C
SE532	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS ($V^+ = +5V_{DC}$ and $T_A = 25°C$ Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	SE532			SU532, NE532			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 0\Omega$		2	5		2	7	mV_{DC}
Input Bias Current (Note 3)	$I_{IN(+)} - I_{IN(-)}$		45	300		45	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$		±3	±30		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 4)		0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ On All Op Amps		0.4	1		0.4	1	mA_{DC}
Large Signal Voltage Gain	$R_L \geqslant 2k\Omega$		100			100		V/mV
Output Voltage Swing	$R_L = 2k\Omega$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common Mode Rejection Ratio	DC		85			85		dB
Power Supply Rejection Ratio	DC		100			100		dB
Amplifier-to-Amplifier Coupling	f = 1kHz to 20kHz (Input Referred)		−120			−120		dB
Output Current Source	$V_{IN}^+ = +1V_{DC}$, $V_{IN}^- = 0V_{DC}$	20	40		20	40		mA_{DC}
Output Current Sink	$V_{IN}^- = +1V_{DC}$, $V_{IN}^+ = 0V_{DC}$	10	20		10	20		mA_{DC}

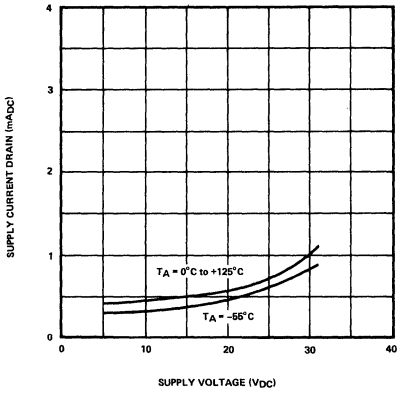
NOTES
1. Derate T package linearly at 4.6mW/°C for ambient temperatures above +25°C. Derate V package at 5mW/°C above 25°C.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
4. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ -1.5V$, but either or both inputs can go to $+30V_{DC}$ without damage.

EQUIVALENT CIRCUIT

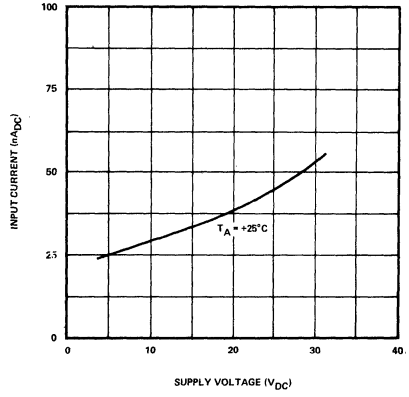


TYPICAL PERFORMANCE CURVES

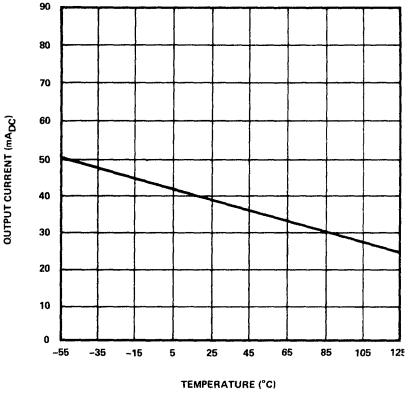
SUPPLY CURRENT



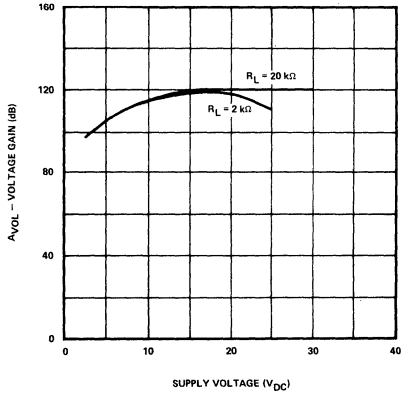
INPUT CURRENT



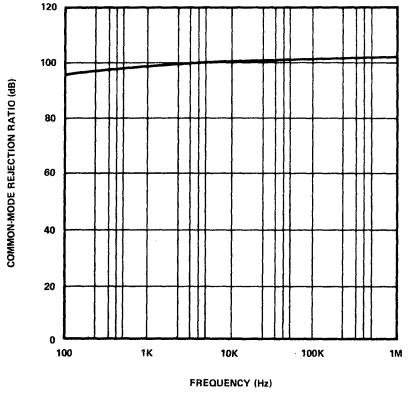
CURRENT LIMITING



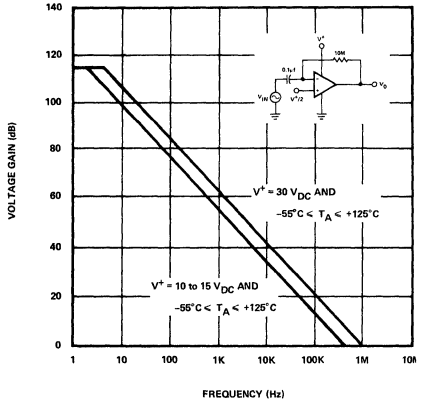
VOLTAGE GAIN



COMMON-MODE REJECTION RATIO

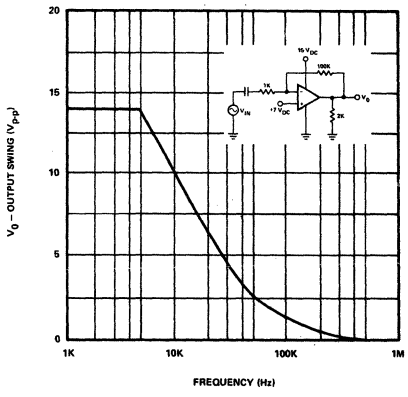


OPEN LOOP FREQUENCY RESPONSE

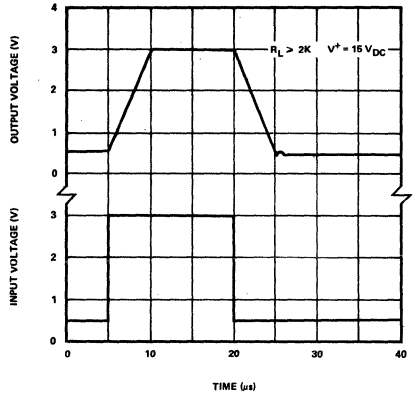


TYPICAL PREFORMANCE CURVES (Cont'd)

LARGE SIGNAL FREQUENCY RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



DESCRIPTION

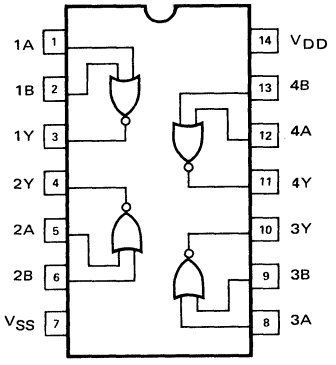
These basic CMOS gates are constructed with MOS P-channel and N-channel enhancement-type devices in a monolithic structure, and find primary use where low power dissipation and/or high noise immunity is desired. The combination of these devices and other CMOS NOR, NAND, and MSI logic functions can account for appreciable package-count savings in various logic configurations.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4001AE
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES . . . 2

PIN CONFIGURATION (Top View)

A PACKAGE

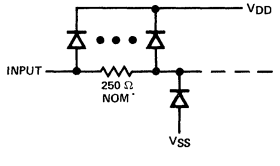


positive logic: $Y = \overline{A+B}$

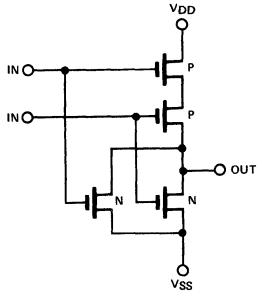
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



SCHEMATIC (Each Gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply Voltage	3		15	V
V_I	Input Voltage	0		V_{DD}	V
T_A	Operating free-air temperature	–40		85	°C

NOTES:

1. Voltage values are with respect to the V_{SS} terminal.
2. Input Current continuous at 25°C may be ±10mA maximum.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 2.5V	MIN 25°C MAX	–0.45 –0.40 –0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_O = 0.4V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			0.5 15	μA
C_{IN}	Input Capacitance		TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			120 80	ns
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			200 200	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			300 200	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			450 450	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 9.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V, V_O = 0.5 V	MIN 25°C MAX	0.60 0.50 0.40			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V	MIN, 25°C MAX			5 30	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

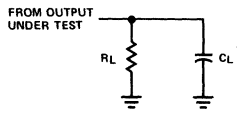
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			65 55	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			130 130	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			125 115	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			300 300	ns

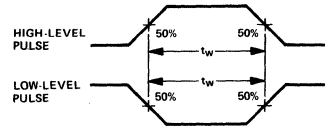
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

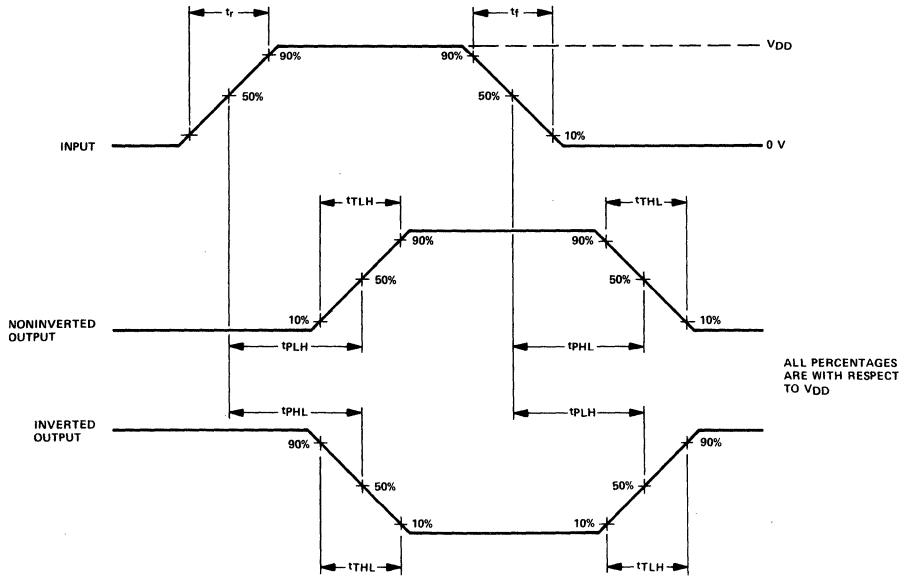


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leqslant 20$ ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, R_{in} = 50 Ω.

DESCRIPTION

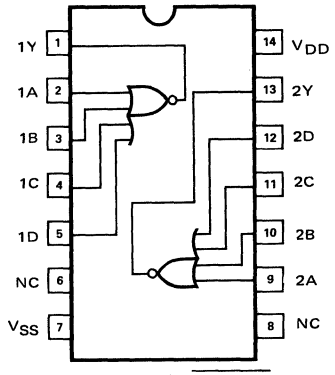
These basic CMOS gates are constructed with MOS P-channel and N-channel enhancement-type devices in a monolithic structure, and find primary use where low power dissipation and/or high noise immunity is desired. The combination of these devices and other CMOS NOR, NAND, and MSI logic functions can account for appreciable package-count savings in various logic configurations.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4002AE
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES . . . 2

PIN CONFIGURATION (Top View)

A PACKAGE



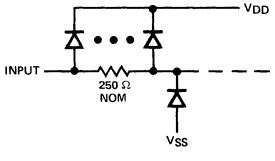
positive logic: $Y = \overline{A+B+C+D}$

NC – No external connection

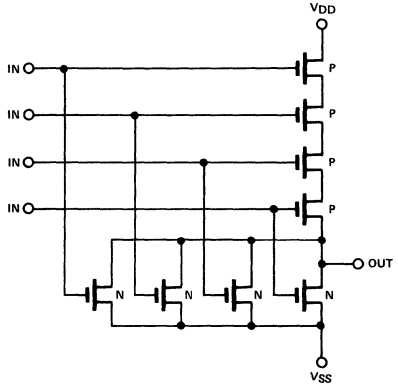
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



SCHEMATIC (Each Gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply voltage	3		15	V
V_I	Input voltage	0		V_{DD}	V
T_A	Operating free-air temperature	–40		85	°C

NOTES:

1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ±10 mA maximum.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 2.5 V	MIN 25°C MAX	–0.45 –0.40 –0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			0.5 15	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			120 80	ns
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			200 200	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			300 200	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			450 450	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 9.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V, V_O = 0.5 V	MIN 25°C MAX	0.60 0.50 0.40			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V	MIN, 25°C MAX			5 30	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

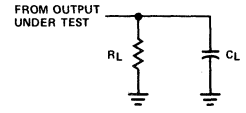
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			65 55	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			130 130	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			125 115	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			300 300	ns

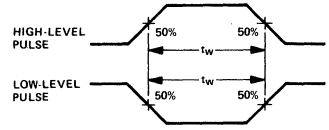
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

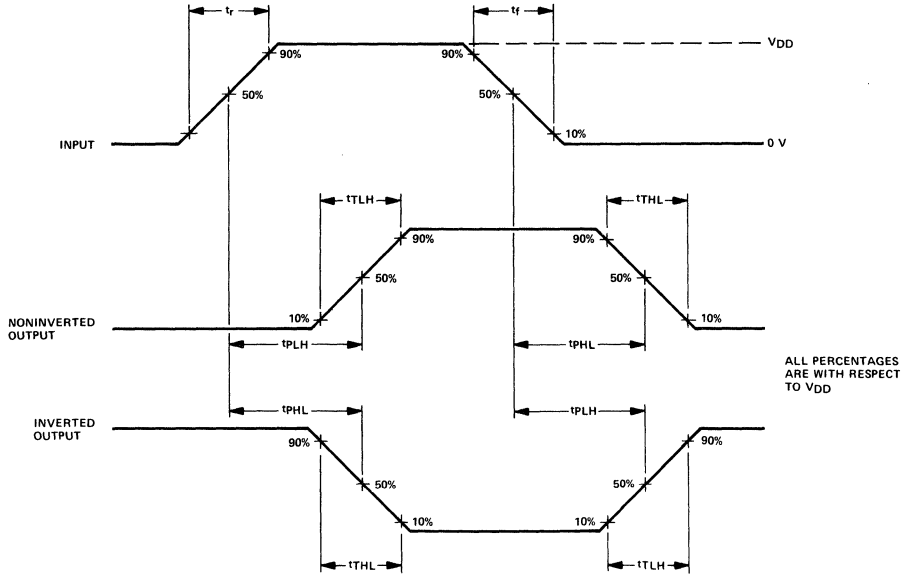


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq$ 20 ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 10 ns, R_{in} = 50 Ω.

DESCRIPTION

The 4007 special purpose device is comprised of three N-channel and three P-channel enhancement-type transistors packaged to provide various degrees of access to each pair of N-channel and P-channel transistors. These versatile devices are useful in inverter circuits, pulse shapers, linear amplifiers, high-input-impedance amplifiers, threshold detectors, transmission gating, and functional gating.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4007AE
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $>10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . <10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES: . . . 2

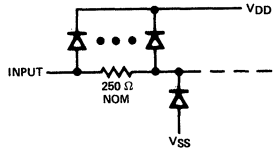
RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS MIN	LIMITS MAX	UNIT
V_{DD}	Supply Voltage	3	15	V
V_I	Input Voltage	0	V_{DD}	V
T_A	Operating Free-air Temperature	-40	85	°C

NOTES

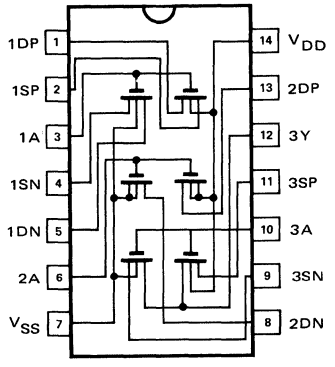
1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ±10 mA maximum.

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



PIN CONFIGURATION (Top View)

A PACKAGE

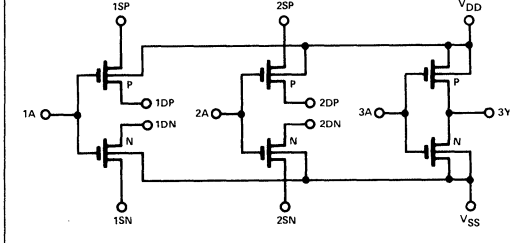


positive logic with SP connected to V_{DD}, DP to DN (designated "Y"), SN to V_{SS}:
$Y = \overline{A}$

ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

SCHEMATIC



ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5V (see Note 2)

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 2.5 V	MIN 25°C MAX	-1.3 -1.1 -0.9			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I - 0 or 5 V	MIN, 25°C MAX			0.5	μA
C_{IN}	Input capacitance		25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C (see Note 2)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			75 75	ns
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			135 135	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			100 100	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			220 220	ns

†t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output

NOTE 2: All measurements are made with each pair of transistors connected to form an inverter as shown in the following table:

PINS CONNECTED TOGETHER	FUNCTION
2, 11 and 14	V_{DD}
4, 7, and 9	V_{SS}
1 and 5	Output of Inverter 1
8 and 13	Output of Inverter 2

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10V (see Note 2)

PARAMETER		TEST CONDITIONS†		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{IH}	High-level input voltage		MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 9.5V	MIN 25°C MAX	-0.65 -0.55 -0.45			mA
I_{OL}	Low-level output current	V_{IH} = 10 V, V_O = 0.5 V	MIN 25°C MAX	1.2 1 0.8			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V	MIN, 25°C MAX			1 30	μA
C_{IN}	Input capacitance		25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C (see Note 2)

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			50 50	ns
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			125 125	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			50 50	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			120 120	

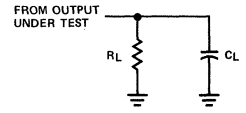
‡t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output

NOTE 2: All measurements are made with each pair of transistors connected to form an inverter as shown in the following table:

PINS CONNECTED TOGETHER	FUNCTION
2, 11 and 14	V_{DD}
4, 7 and 9	V_{SS}
1 and 5	Output of Inverter 1
8 and 13	Output of Inverter 2

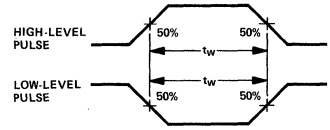
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

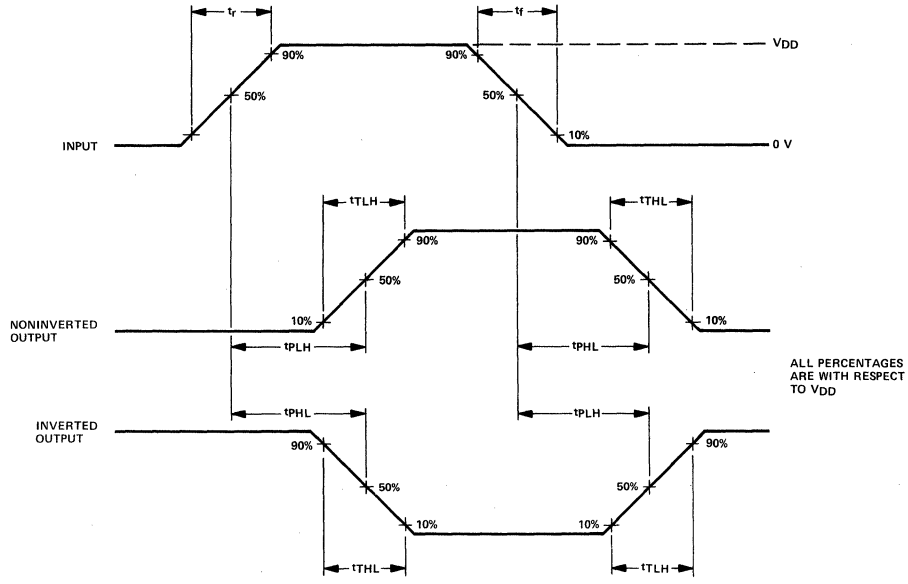


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leqslant 20$ ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, R_{in} = 50 Ω.

DESCRIPTION

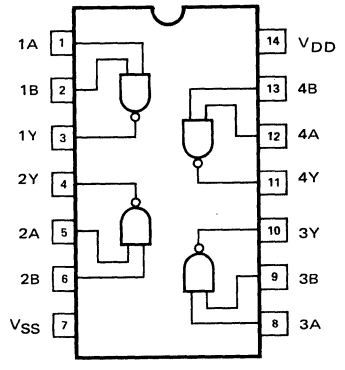
These basic CMOS gates are constructed with MOS P-channel and N-channel enhancement-type devices in a monolithic structure, and find primary use where low power dissipation and/or high noise immunity is desired. The combination of these devices and other CMOS NOR, NAND, and MSI logic functions can account for appreciable package-count savings in various logic configurations.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4011AE
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES . . . 2

PIN CONFIGURATION (Top View)

A PACKAGE

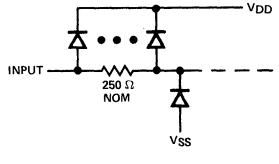


positive logic: $Y = \overline{AB}$

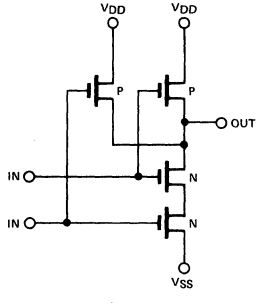
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



SCHEMATIC (Each Gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply voltage	3		15	V
V_I	Input voltage	0		V_{DD}	V
T_A	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 2.5 V	MIN 25°C MAX	–0.45 –0.40 –0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			0.5 15	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			100 100	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			200 200	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			125 150	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			450 450	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†			LIMITS			UNIT
					MIN	TYP	MAX	
V_{IH}	High-level input voltage			MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V		25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0,	V_O = 9.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V,	V_O = 0.5 V	MIN 25°C MAX	0.60 0.50 0.40			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V		MIN, 25°C MAX			5 30	μA
C_{IN}	Input capacitance			TYP. @ 25°C		5		pF

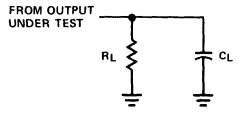
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			50 50	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			130 130	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			75 100	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			300 300	ns

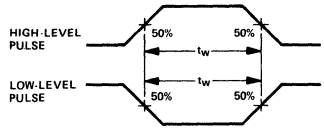
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

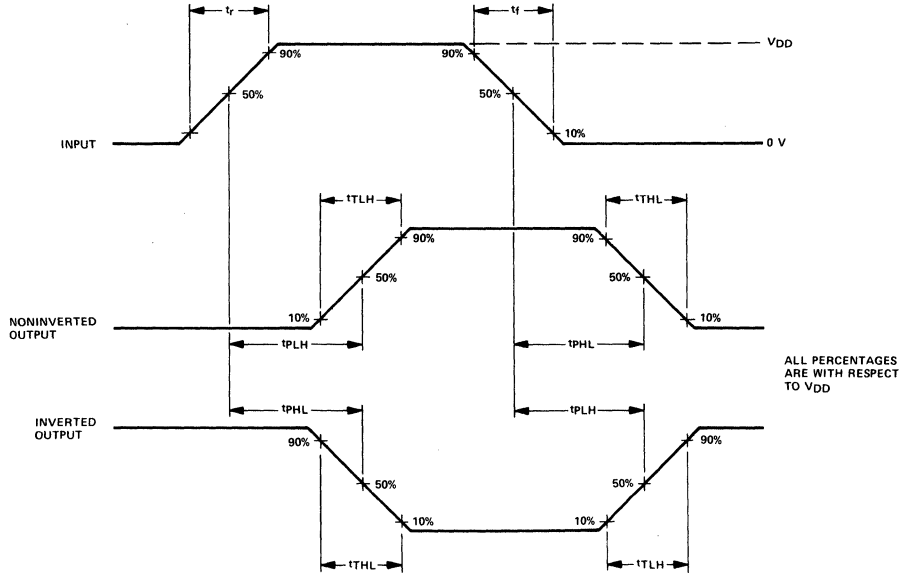


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leqslant 20$ ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, R_{in} = 50 Ω.

DESCRIPTION

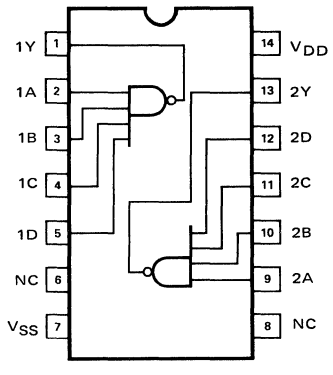
These basic CMOS gates are constructed with MOS P-channel and N-channel enhancement-type devices in a monolithic structure, and find primary use where low power dissipation and/or high noise immunity is desired. The combination of these devices and other CMOS NOR, NAND, and MSI logic functions can account for appreciable package-count savings in various logic configurations.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4012AE
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES . . . 2

PIN CONFIGURATION (Top View)

A PACKAGE



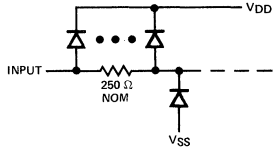
positive logic: $Y = \overline{ABCD}$

NC—No internal connection

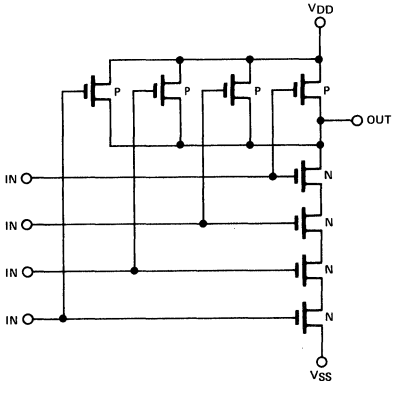
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



SCHEMATIC (Each Gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply voltage	3		15	V
V_I	Input voltage	0		V_{DD}	V
T_A	Operating free-air temperature	−40		85	°C

NOTES:

1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ±10 mA maximum.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†			LIMITS			UNIT
					MIN	TYP	MAX	
V_{IH}	High-level input voltage			MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V		25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0,	V_O = 2.5 V	MIN 25°C MAX	−0.45 −0.40 −0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V,	V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V		MIN, 25°C MAX			0.5 15	μA
C_{IN}	Input capacitance			TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			100 200	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			200 400	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			125 500	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			470 670	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†			LIMITS			UNIT
					MIN	TYP	MAX	
V_{IH}	High-level input voltage			MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V		25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0,	V_O = 9.5 V	MIN 25°C MAX	−0.45 −0.40 −0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V,	V_O = 0.5 V	MIN 25°C MAX	0.60 0.50 0.40			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V		MIN, 25°C MAX			5 30	μA
C_{IN}	Input capacitance			TYP. @ 25°C		5		pF

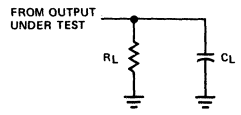
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			50 100	ns
t_{PLH} Propagation delay time, low-to-high-level output t_{PHL} Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			110 200	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			75 250	ns
t_{TLH} Transition time, low-to-high-level output t_{THL} Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			250 400	ns

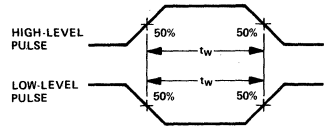
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

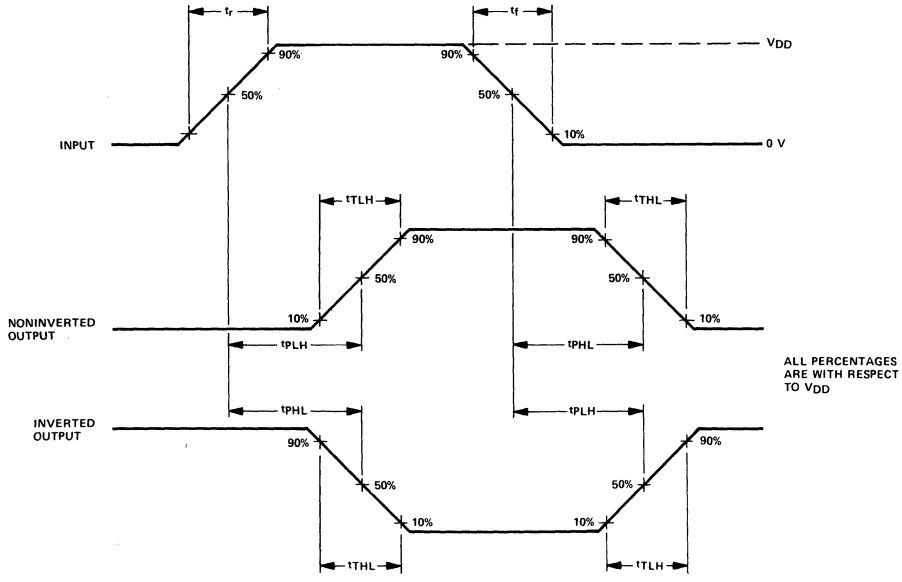


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leqslant 20$ ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, R_{in} = 50 Ω.

DESCRIPTION

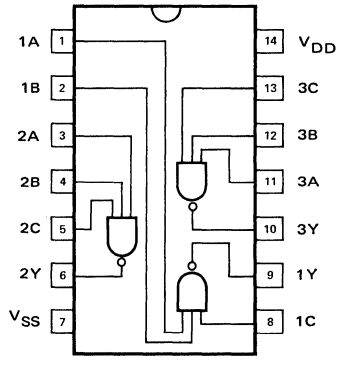
These CMOS gates are constructed with MOS P-channel and N-channel enhancement-type devices in a monolithic structure, and find primary use where low power dissipation and/or high noise immunity is desired. The combination of these devices and other CMOS NOR, NAND, and MSI logic functions can account for appreciable package-count savings in various logic configurations.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4023A
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES . . . 2

PIN CONFIGURATION (Top View)

A PACKAGE

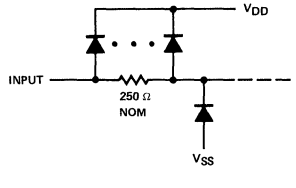


positive logic: $Y = \overline{ABC}$

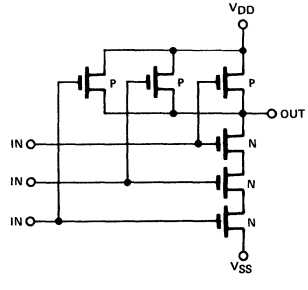
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



SCHEMATIC (each gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply voltage	3		15	V
V_I	Input voltage	0		V_{DD}	V
T_A	Operating free-air temperature	−40		85	°C

NOTES:
1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ± 10 mA maximum.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C MIN	 −0.45		100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 2.5 V	25°C MAX	−0.40 −0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			0.5 15	μA
C_{IN}	Input Capacitance		TYP @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			100 100	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			200 200	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			125 150	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			470 600	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†			LIMITS			UNIT
					MIN	TYP	MAX	
V_{IH}	High-level input voltage			MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C MAX			2.9	
I_I	Input current	V_I = 0 to 10 V		25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0,	V_O = 9.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V,	V_O = 0.5 V	MIN 25°C MAX	0.6 0.5 0.4			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V		MIN, 25°C MAX			5 30	μA
C_{IN}	Input Capacitance			TYP. @ 25°C		5		pF

†MIN and MAX at the right hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			50 50	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			110 110	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			75 100	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			250 275	ns

DESCRIPTION

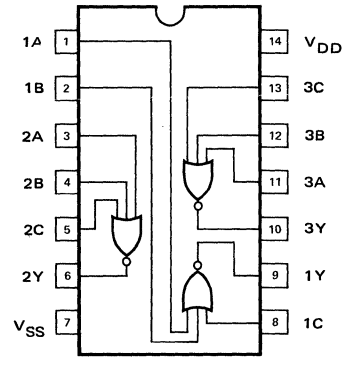
These CMOS gates are constructed with MOS P-channel and N-channel enhancement-type devices in a monolithic structure, and find primary use where low power dissipation and/or high noise immunity is desired. The combination of these devices and other CMOS NOR, NAND, and MSI logic functions can account for appreciable package-count savings in various logic configurations.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4025A
- POWER DISSIPATION . . . 10 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL
- INPUT CURRENT . . . < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- FAN-OUT TO SERIES 54L GATES . . . 2

PIN CONFIGURATION (Top View)

A PACKAGE

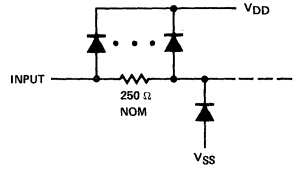


positive logic: $Y = \overline{A+B+C}$

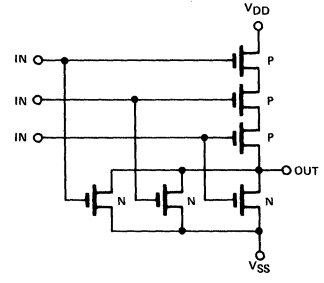
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



SCHEMATIC (each gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply voltage	3		15	V
V_I	Input voltage	0		V_{DD}	V
T_A	Operating free-air temperature	−40		85	°C

NOTES:
1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ± 10 mA maximum.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 2.5 V	MIN 25°C MAX	−0.45 −0.40 −0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			0.5 15	μA
C_{IN}	Input Capacitance		TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			120 80	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			200 200	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			300 200	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			450 450	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C MAX			2.9	
I_I	Input current	V_I = 0 to 10 V	25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0, V_O = 9.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V, V_O = 0.5 V	MIN 25°C MAX	0.6 0.5 0.4			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V	MIN, 25°C MAX			5 30	μA
C_{IN}	Input Capacitance		TYP @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			65 55	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			130 130	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			125 115	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			300 300	ns

DESCRIPTION

The 4027 is a dual J-K-type transition-operated master-slave flip-flop with buffered outputs, independent direct overriding preset and clear inputs, and J, K, and clock inputs. While the clock is low, the data at the J and K inputs is entered into the master section which is isolated from the slave section. On the rising transition of the clock, the J and K inputs are disabled and data previously set up in the master section is transferred to the slave section. Circuit logic for various input configurations is shown in the function table.

Presetting and clearing are independent of the clock and are accomplished by a high-level voltage at the respective input. The $\overline{Q}$ output is complementary to the Q output except for the nonstable situation that exists when both preset and clear inputs are simultaneously high.

FEATURES

- **DESIGNED TO BE INTERCHANGEABLE WITH CD4027AE**
- **POWER DISSIPATION . . . 50 nW TYPICAL**
- **OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES**
- **TOGGLE RATE . . . 8 MHz TYPICAL AT V_{DD} = 10 V**
- **INPUT RESISTANCE . . . $> 10^{12}\ \Omega$ TYPICAL**
- **INPUT OVER-VOLTAGE PROTECTION**
- **FANOUT TO SERIES 54L GATES . . . 2**

FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CK	J	K	Q	$\overline{Q}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H*	H*
L	L	↑	L	L	Q_0	$\overline{Q}_0$
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	TOGGLE	
L	L	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady-state, L = low level (steady-state)

X = irrelevant, ↑ = transition from low to high level

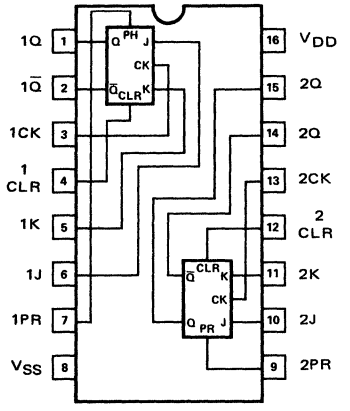
Q_0 = the level of Q before the indicated steady-state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↑ clock transition.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (low) level.

PIN CONFIGURATION (Top View)

B PACKAGE



positive logic: see function table

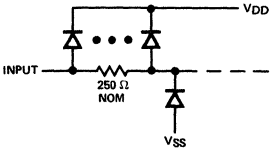
ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	15 V
Input current (see Note 2)	±50 mA
Continuous total dissipation	200 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

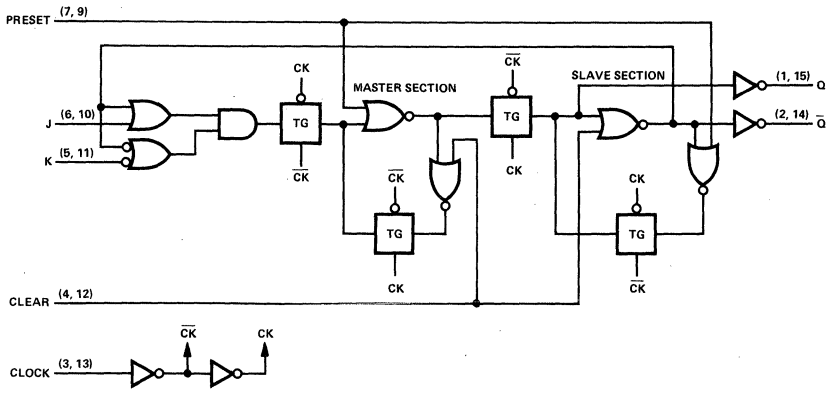
NOTES:

1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ±10 mA maximum.

EQUIVALENT OF EACH INPUT PROTECTIVE NETWORK



FUNCTIONAL BLOCK DIAGRAM (each flip-flop)



TG . . . transmission gate which is a closed switch only when the input shown as ⊥ is high and the input shown as ○ is low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		MIN	TYP	MAX	
V_{DD}	Supply voltage	3		15	V
V_I	Input voltage	0		V_{DD}	V
T_A	Operating free-air temperature	−40		85	°C

RECOMMENDED OPERATING CONDITIONS for V_{DD} = 5V

PARAMETER			LIMITS			UNIT
			MIN	TYP	MAX	
$t_{r(clock)}$	Clock rise time				15	μs
$t_{f(clock)}$	Clock fall time				15	μs
t_w	Pulse width	Clock high	500			ns
		Clock low	500			
		Preset or clear	300			
t_{setup}	Setup time		200			ns

RECOMMENDED OPERATING CONDTIONS for V_{DD} = 10 V

PARAMETER			LIMITS			UNIT
			MIN	TYP	MAX	
$t_{r(clock)}$	Clock rise time				5	μs
$t_{f(clock)}$	Clock fall time				5	μs
t_w	Pulse width	Clock high	165			ns
		Clock low	165			
		Preset or clear	120			
t_{setup}	Setup time		75↑			ns

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IH} = 5 V, V_{IL} = 0, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max I_O = 0	MIN, 25°C, MAX	4.2			
V_{OL}	Low-level output voltage	V_{IH} = 5 V, V_{IL} = 0, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max I_O = 0	MIN, 25°C, MAX			0.8	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IH} = 5 V, V_{IL} = 0 V_O = 2.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 5 V, V_{IL} = 0 V_O = 0.4 V	MIN 25°C MAX	0.45 0.40 0.36			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			10 140	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

†MIN and MAX at the righ-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 5 V, R_L = 200Ω, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			UNIT
					MIN	TYP	MAX	
f_{max}	Maximum clock frequency				1			MHz
t_{PLH}	Propagation delay time, low-to-high-level output	Clock	Q or $\overline{Q}$	C_L = 15 pF C_L = 50 pF			400 550	ns
t_{PHL}	Propagation delay time, high-to-low-level output						400 550	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Preset or Clear	Q or $\overline{Q}$	C_L = 15 pF C_L = 50 pF			350 450	ns
t_{PHL}	Propagation delay time, high-to-low-level output						350 450	ns
t_{TLH}	Transition time, low-to-high-level output		Any	C_L = 15 pF C_L = 50 pF			250 300	ns
t_{THL}	Transition time, high-to-low-level output						250 300	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input voltage		MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IH} = 10 V, V_{IL} = 0, I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max I_O = 0	MIN, 25°C, MAX	9			
V_{OL}	Low-level output voltage	V_{IH} = 10 V, V_{IL} = 0, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max I_O = 0	MIN, 25°C, MAX			1	
I_I	Input current	V_I = 0 to 10 V	25°C			100	nA
I_{OH}	High-level output current	V_{IH} = 10 V, V_{IL} = 0, V_O = 9.5 V	MIN 25°C MAX	-0.45 -0.40 -0.36			mA
I_{OL}	Low-level output current	V_{IH} = 10 V, V_{IL} = 0, V_O = 0.5 V	MIN 25°C MAX	-0.60 -0.50 -0.40			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V	MIN, 25°C, MAX			20 280	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

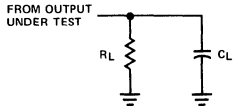
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{DD} = 10 V, R_L = 200kΩ, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			UNIT
					MIN	TYP	MAX	
f_{max}	Maximum clock frequency				3			MHz
t_{PLH}	Propagation delay time, low-to-high-level output	Clock	Q or $\overline{Q}$	C_L = 15pF C_L = 50pF			150 250	ns
t_{PHL}	Propagation delay time, high-to-low-level output						150 250	ns
t_{PLH}	Propagation delay time, low-to-high-level output	Preset or Clear	Q or $\overline{Q}$	C_L = 15pF C_L = 50pF			150 250	ns
t_{PHL}	Propagation delay time, high-to-low-level output						150 250	ns
t_{TLH}	Transition time, low-to-high-level output		Any	C_L = 15pF C_L = 50pF			140 175	ns
t_{THL}	Transition time, high-to-low-level output						140 175	ns

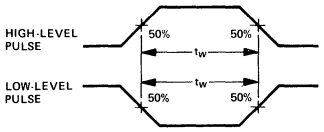
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

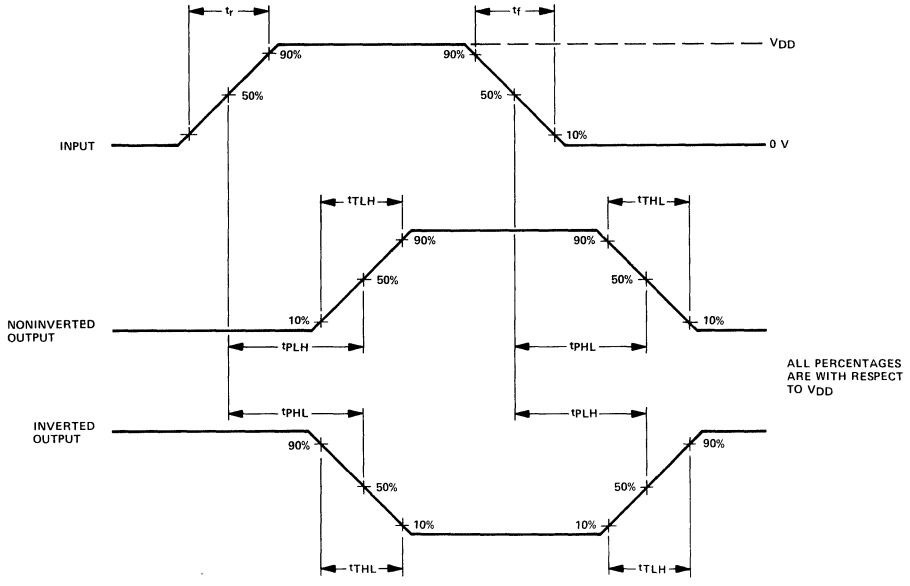


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leqslant 20$ ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, R_{in} = 50 Ω.

DESCRIPTION

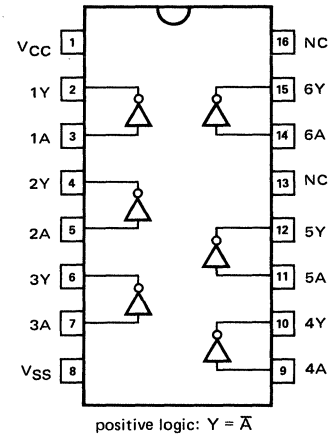
The 4049 CMOS inverting hex buffer may be used as a current sink or source driver, a hex CMOS driver, or a CMOS to DTL or TTL logic-level converter. Conversion ranges are from CMOS logic operating at supply levels of 3 volts to 15 volts to DTL or TTL operating at supply levels of 3 volts to 15 volts. Conversion to logic output levels greater than 6 volts is permitted provided that the V_{CC} supply voltage is $\leqslant V_{IH}$.

FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4049AE AND CD4009AE*(3)
- POWER DISSIPATION . . . 50 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT CURRENT . . . <10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- HIGH CURRENT SINKING CAPABILITY . . . 8 mA MINIMUM AT V_{OL} = 0.5 V, V_{CC} = 10 V, T_A = 25°C
- FAN-OUT TO SERIES 54L GATES . . . 13

PIN CONFIGURATION (Top View)

B PACKAGE



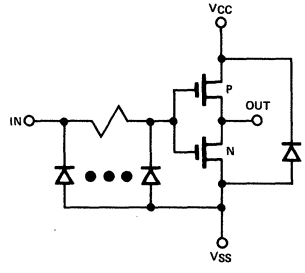
positive logic: $Y = \overline{A}$

NC—No internal connection

ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	15 V
Load capacitance for V_{CC} above 10.5 V	200 pF
Input current (see Note 2)	±50 mA
Continuous total dissipation (pkg)	200 mW
Operating free-air temperature range:	-40°C to 85°C
Storage temperature range	-65°C to 150°C

SCHEMATIC (Each Buffer)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS MIN	LIMITS MAX	UNIT
V_{CC}	Supply voltage	3	15	V
V_I	Input voltage	0	15	V
T_A	Operating free-air temperature	-40	85	°C

NOTES
1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ±10 mA maximum.
3. In most applications, 4049 replaces 4009.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS†			LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{IH}	High-level input voltage			MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			1 0.9	V
V_{OH}	High-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IH} = 5 V,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V		25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0,	V_O = 2.5 V	MIN 25°C MAX	-1.5 -1.25 -1			mA
I_{OL}	Low-level output current	V_{IH} = 5 V,	V_O = 0.4 V	MIN 25°C MAX	3.6 3 2.5			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V		MIN, 25°C MAX			3 42	μA
C_{IN}	Input capacitance			TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			100 70	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			140 125	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			160 60	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			350 80	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{CC} = 10 V

PARAMETER		TEST CONDITIONS†			LIMITS			UNIT
					MIN	TYP	MAX	
V_{IH}	High-level input voltage			MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			2 1.9	V
V_{OH}	High-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IH} = 10 V,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V		25°C			100	nA
I_{OH}	High-level output current	V_{IL} = 0,	V_O = 9.5 V	MIN 25°C MAX	-0.75 -0.6 -0.5			mA
I_{OL}	Low-level output current	V_{IH} = 10 V,	V_O = 0.5 V	MIN 25°C MAX	9.6 8 6.6			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V		MIN, 25°C MAX			5 70	μA
C_{IN}	Input capacitance			TYP. @ 25°C		5		pF

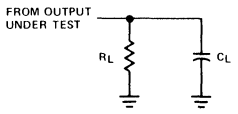
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{CC} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			70 40	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			100 75	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			120 50	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			270 70	ns

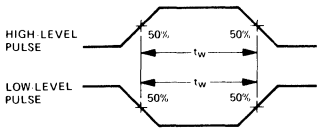
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

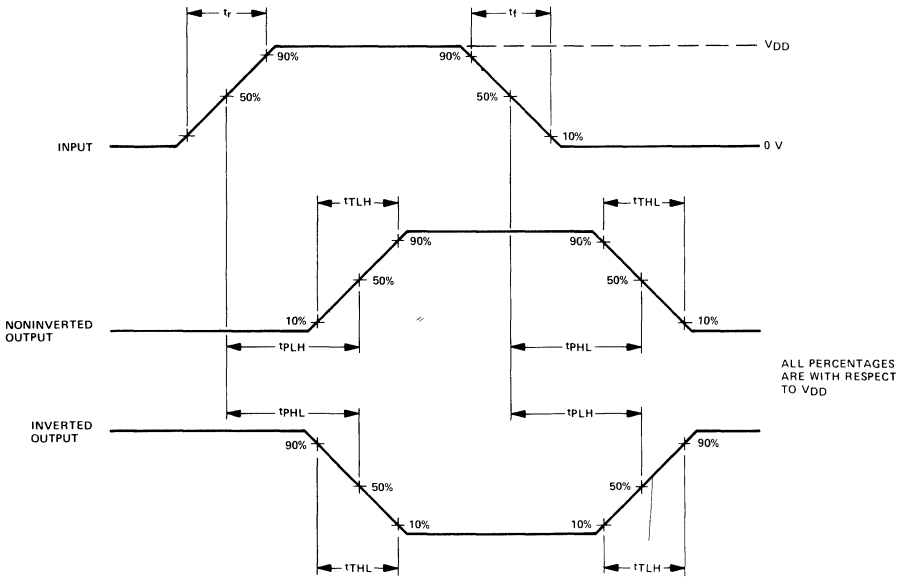


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq 20$ ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, R_{in} = 50 Ω.

DESCRIPTION

The 4050 CMOS noninverting hex buffer may be used as a current sink or source driver, a hex CMOS driver, or a CMOS to DTL or TTL logic-level converter. Conversion ranges are from CMOS logic operating at supply levels of 3 volts to 15 volts to DTL or TTL operating at supply levels of 3 volts to 15 volts. Conversion to logic output levels greater than 6 volts is permitted provided that the V_{CC} supply voltage is $\leqslant V_{IH}$.

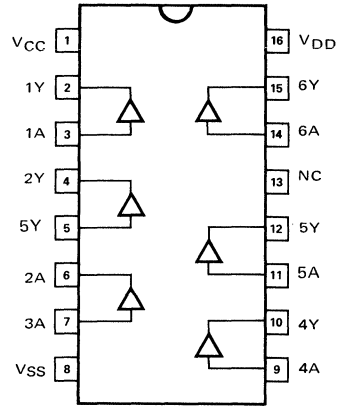
FEATURES

- DESIGNED TO BE INTERCHANGEABLE WITH CD4050AE AND CD4010AE(3)
- POWER DISSIPATION IS 50 nW TYPICAL
- OUTPUT SWING INDEPENDENT OF FAN-OUT TO OTHER CMOS DEVICES
- INPUT CURRENT IS < 10 pA TYPICAL
- INPUT OVER-VOLTAGE PROTECTION
- HIGH CURRENT SINKING CAPABILITY

  8 mA MINIMUM AT V_{OL} = 0.5V, V_{CC} = 10V, T_A = 25°C
- FAN-OUT TO SERIES 54L GATES IS 13

PIN CONFIGURATION (Top View)

B PACKAGE



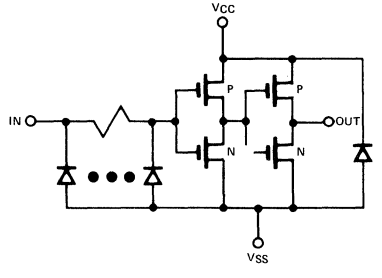
positive logic: Y = A

NC—No internal connection

ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	15 V
Load capacitance for V_{CC} above 10.5 V	200 pF
Input current (see Note 2)	±50 mA
Continuous total dissipation (pkg)	200 mW
Operating free-air temperature range	-40°C to 85°C
Storage temperature range	-65°C to 150°C

SCHEMATIC (Each Buffer)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	3	15	V
V_I	Input voltage	0	15	V
T_A	Operating free-air temperature	-40	85	°C

NOTES
1. Voltage values are with respect to the V_{SS} terminal.
2. Input current continuous at 25°C may be ±10 mA maximum.
3. In most applications, 4050 replaces 4010.

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS†		LIMITS			UNIT
				MIN	TYP	MAX	
V_{IH}	High-level input		MIN 25°C, MAX	3.6 3.5			V
V_{IL}	Low-level input voltage		MIN, 25°C MAX			1.5 1.4	V
V_{OH}	High-level output voltage	V_{IH} = 5 V, I_O = 0	MIN, 25°C MAX	4.99 4.95			V
		V_{IH} = V_{IH} min, I_O = 0	MIN, 25°C, MAX	3.6			
V_{OL}	Low-level output voltage	V_{IL} = 0, I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IL} = V_{IL} max, I_O = 0	MIN, 25°C, MAX			0.95	
I_I	Input current	V_I = 0 to 5 V	25°C			100	nA
I_{OH}	High-level output current	V_{IH} = 5 V, V_O = 2.5 V	MIN 25°C MAX	-1.5 -1.25 -1			mA
I_{OL}	Low-level output current	V_{IL} = 0, V_O = 0.4 V	MIN 25°C MAX	3.6 3 2.5			mA
I_{DD}	Quiescent supply current	V_I = 0 or 5 V	MIN, 25°C MAX			3 42	μA
C_{IN}	Input capacitance		TYP. @ 25°C		5		pF

†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			100 70	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			140 125	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF, R_L = 200 kΩ			160 60	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF, R_L = 200 kΩ			350 80	ns

ELECTRICAL CHARACTERISTICS at specified free-air temperature, V_{CC} = 10 V

PARAMETER		TEST CONDITIONS†			LIMITS			UNIT
					MIN	TYP	MAX	
V_{IH}	High-level input voltage			MIN 25°C, MAX	7.1 7			V
V_{IL}	Low-level input voltage			MIN, 25°C MAX			3 2.9	V
V_{OH}	High-level output voltage	V_{IH} = 10 V,	I_O = 0	MIN, 25°C MAX	9.99 9.95			V
		V_{IH} = V_{IH} min,	I_O = 0	MIN, 25°C, MAX	7.2			
V_{OL}	Low-level output voltage	V_{IL} = 0,	I_O = 0	MIN, 25°C MAX			0.01 0.05	V
		V_{IL} = V_{IL} max,	I_O = 0	MIN, 25°C, MAX			2.9	
I_I	Input current	V_I = 0 to 10 V		25°C			100	nA
I_{OH}	High-level output current	V_{IH} = 10 V,	V_O = 9.5 V	MIN 25°C MAX	−0.75 −0.6 −0.5			mA
I_{OL}	Low-level output current	V_{IL} = 0,	V_O = 0.5 V	MIN 25°C MAX	9.6 8 6.6			mA
I_{DD}	Quiescent supply current	V_I = 0 or 10 V		MIN, 25°C MAX			5 70	μA
C_{IN}	Input capacitance			TYP. @ 25°C		5		pF

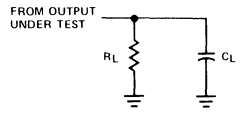
†MIN and MAX at the right-hand side of the test conditions column refer to the respective values of temperature specified under recommended operating conditions.

SWITCHING CHARACTERISTICS, V_{CC} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			70 40	ns
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			100 75	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 15 pF,	R_L = 200 kΩ			120 50	ns
t_{TLH} t_{THL}	Transition time, low-to-high-level output Transition time, high-to-low-level output	C_L = 50 pF,	R_L = 200 kΩ			270 70	ns

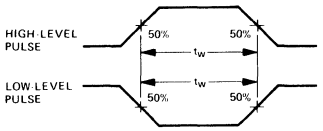
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

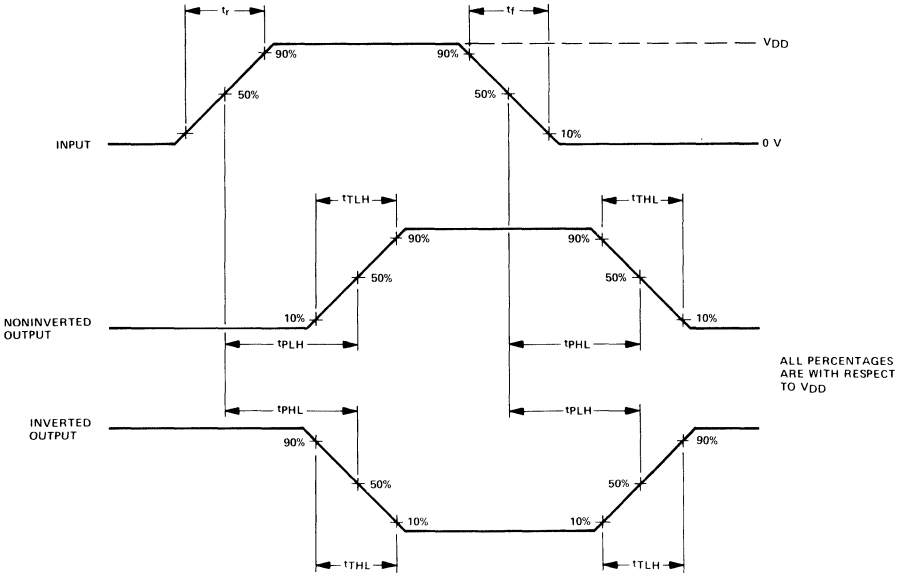


NOTE A: C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS PULSE WIDTHS



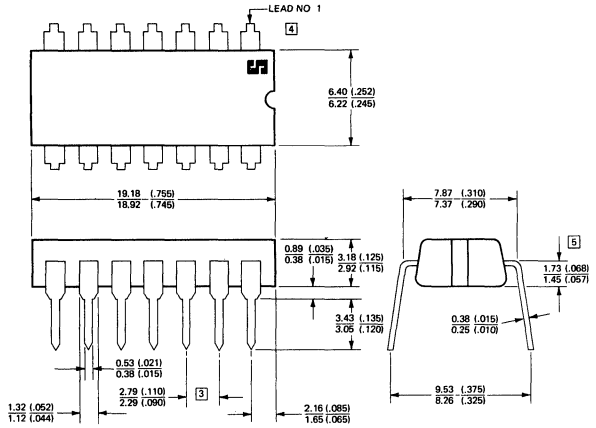
VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



NOTES: B. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq$ 20 ns, t_f = 20 ns.

C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq$ 10 ns, R_{in} = 50 Ω.

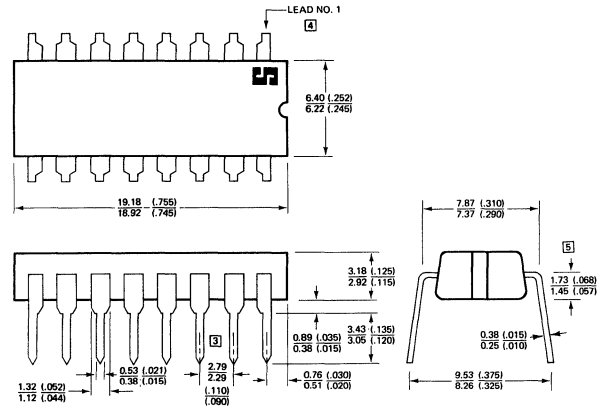
A PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

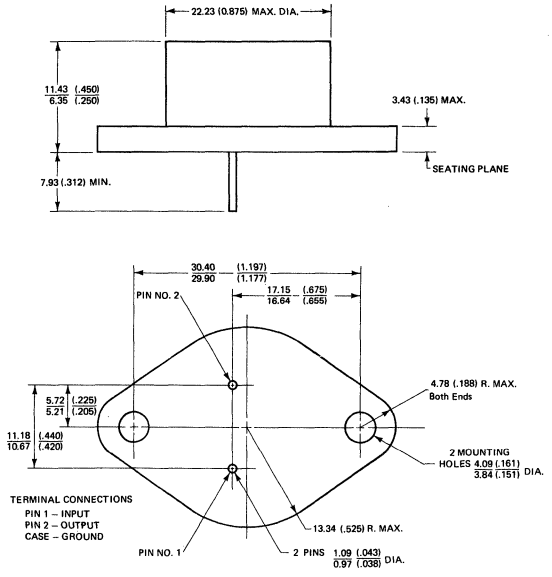
B PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

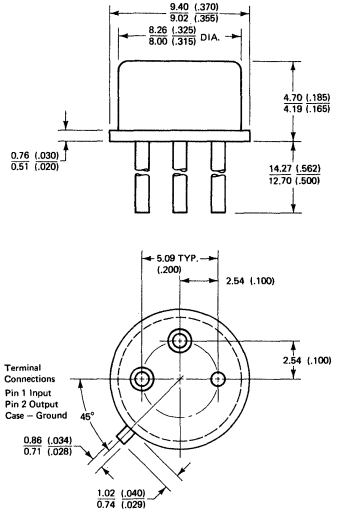
DA PACKAGE



NOTES:

1. Lead Material: No. 52 alloy gold plated.
2. Body Material: 1010 steel gold plated.
3. Lid Material: Steel nickel plated, weld seal.
4. All dimensions shown in parentheses are English. (Inches)

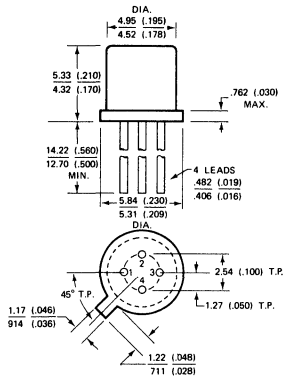
DB PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent – gold plated.
2. Body Material: Eyelet, Kovar or equivalent – gold plated, glass body.
3. Lid Material: Nickel, weld seal.
4. All dimensions shown in parentheses are English. (Inches)

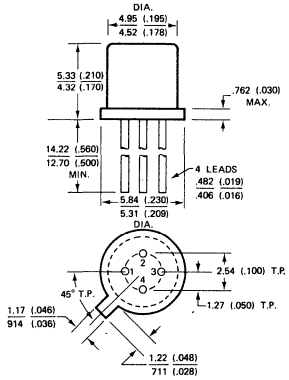
DC PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent – gold plated.
2. Body Material: Eyelet, Kovar or equivalent – gold plated, glass body.
3. Lid Material: Nickel, weld seal.
4. All dimensions shown in parentheses are English. (Inches)

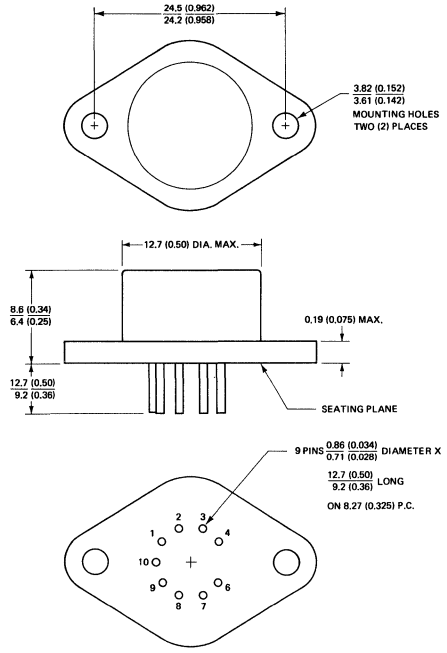
DE PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent – gold plated.
2. Body Material: Eyelet, Kovar or equivalent – gold plated, glass body.
3. Lid Material: Nickel, weld seal.
4. All dimensions shown in parentheses are English. (Inches)

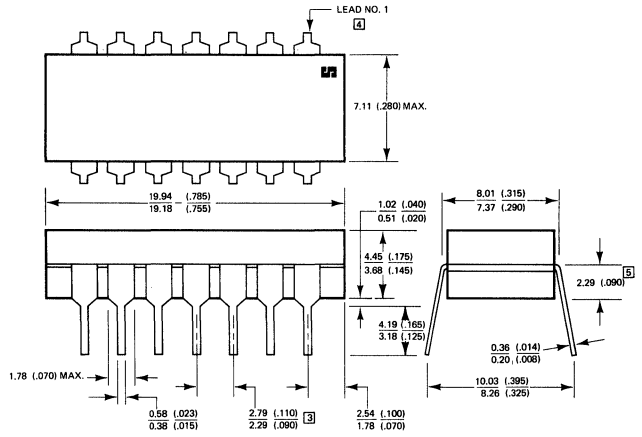
DF PACKAGE



NOTES:

1. Lead Material: Alloy 52, gold plated.
2. All dimensions shown in parentheses are English. (Inches)

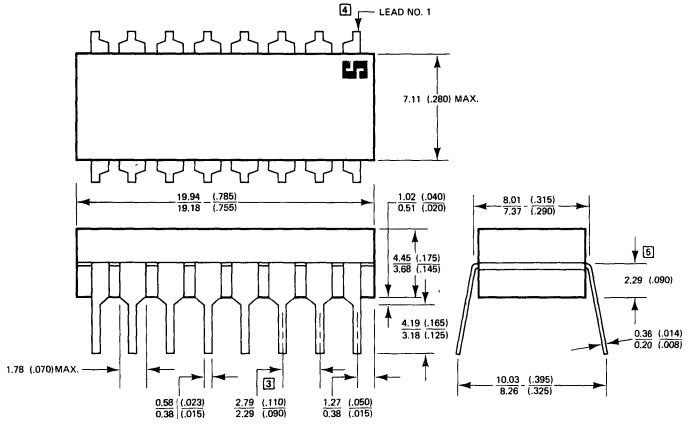
FH PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Thermal resistance: Θ Ja = .095°C/mW, Θ Jc = .027°C/mW.
7. All dimensions shown in parentheses are English. (Inches)

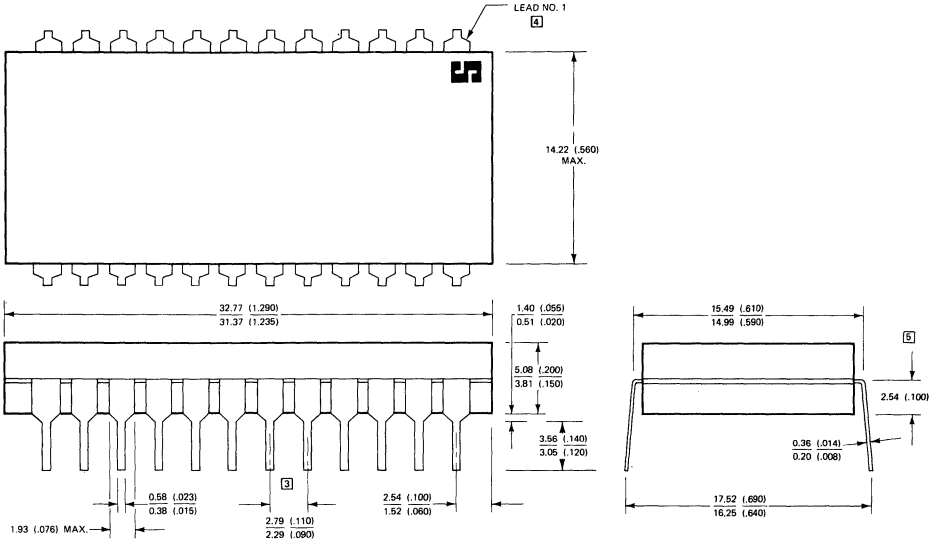
FJ PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Thermal resistance: Θ Ja = .090°C/mW, Θ Jc = .025°C/mW.
7. All dimensions shown in parentheses are English. (Inches)

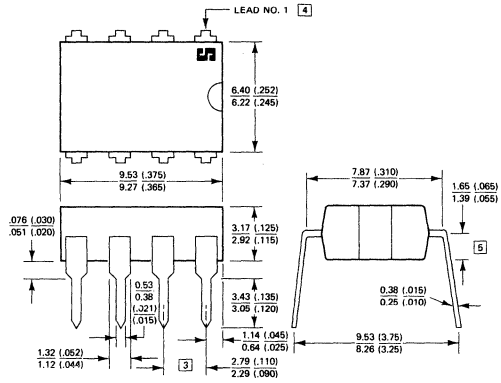
FN PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .012°C/mW.
7. All dimensions shown in parentheses are English. (Inches)

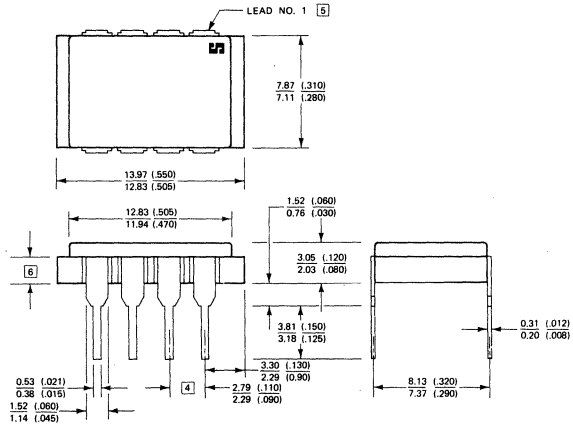
IE PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent, gold plated.
2. Body Material: Ceramic with Kovar or equivalent.
3. Lid Material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal Resistance: Θ Ja = .100°C/mW, Θ Jc = .030°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

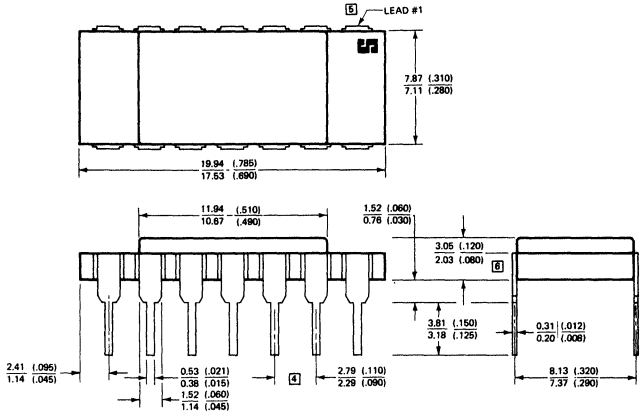
IEA PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent, tin plated.
2. Body Material: Ceramic with Kovar or equivalent.
3. Lid Material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal Resistance: Θ Ja = .100°C/mW, Θ Jc = .030°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

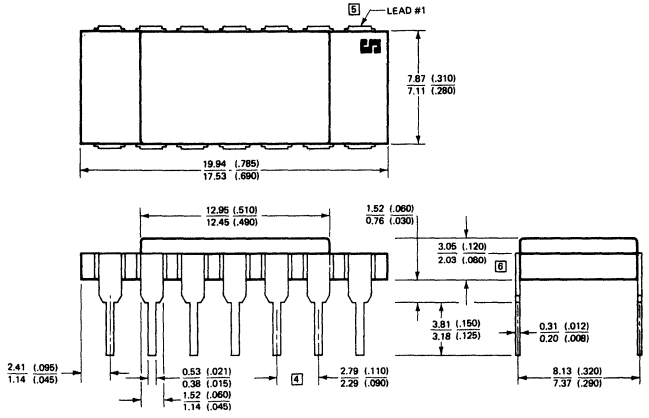
IH PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .085°C/mW, Θ Jc = .022°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

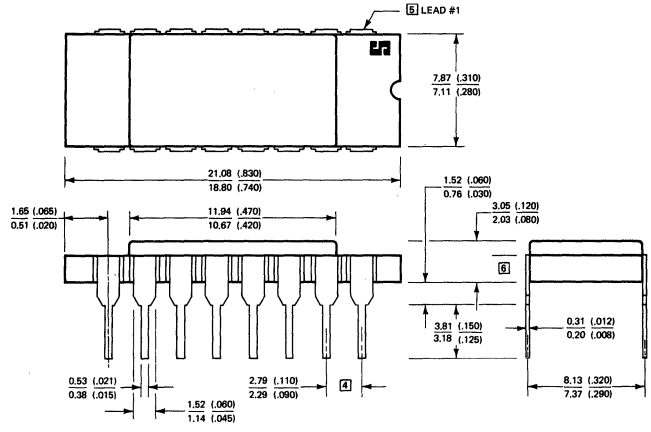
IHA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .085°C/mW, Θ Jc = .022°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

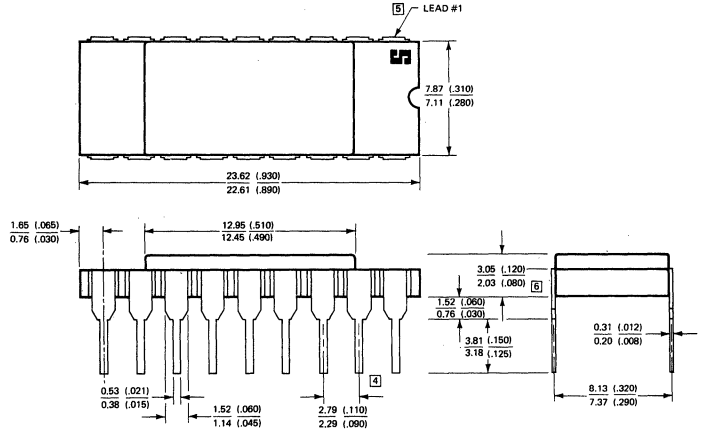
IJ PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .080°C/mW, Θ Jc = .020°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

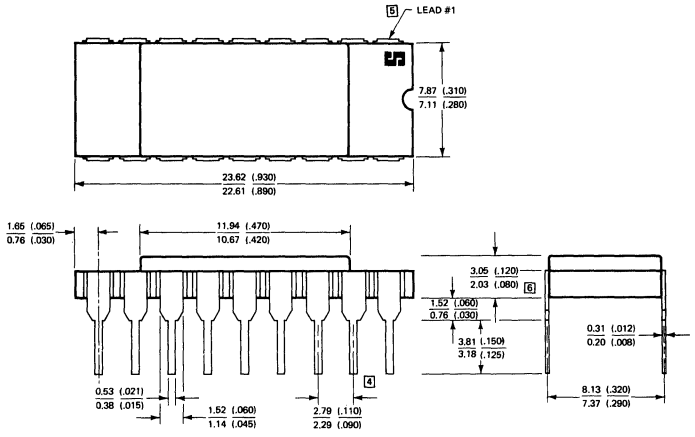
IJA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .080°C/mW, Θ Jc = .020°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

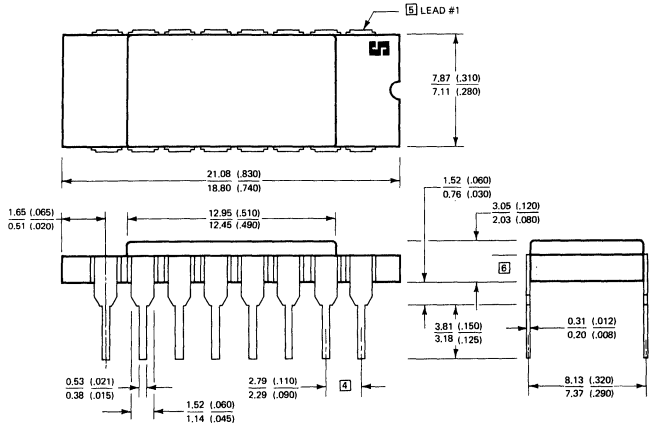
IK PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .075°C/mW, Θ Jc = .018°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

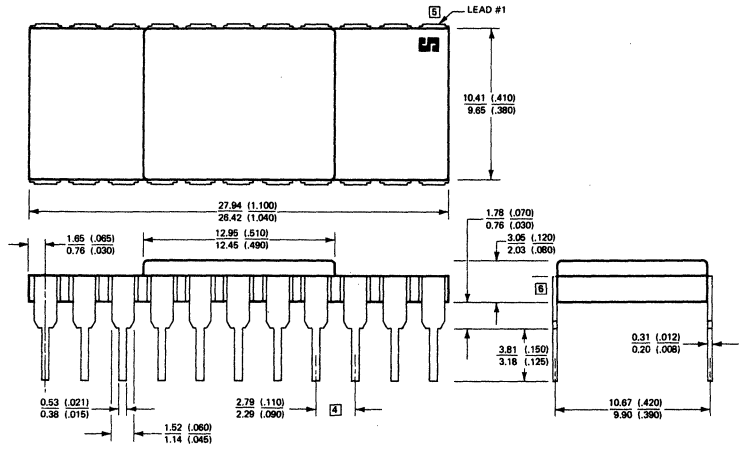
IKA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .075°C/mW, Θ Jc = .018°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

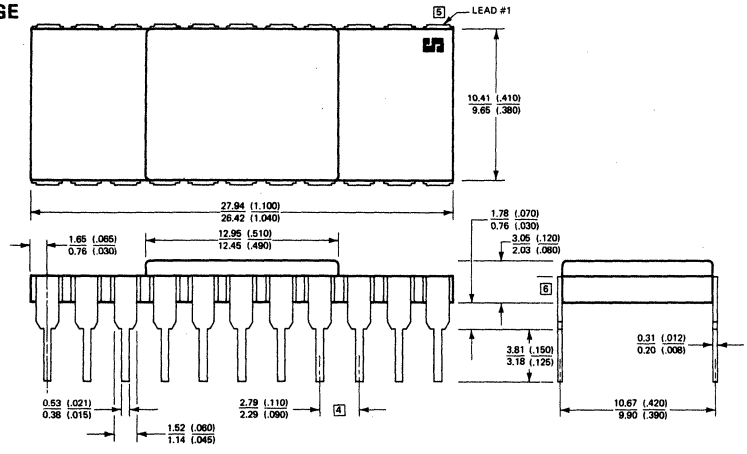
IM PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .055°C/mW, Θ Jc = .012°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

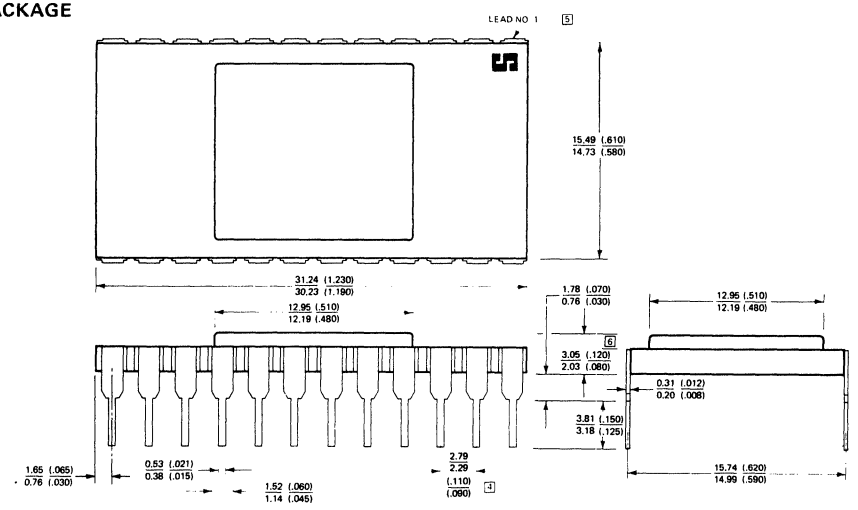
IMA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .055°C/mW, Θ Jc = .012°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

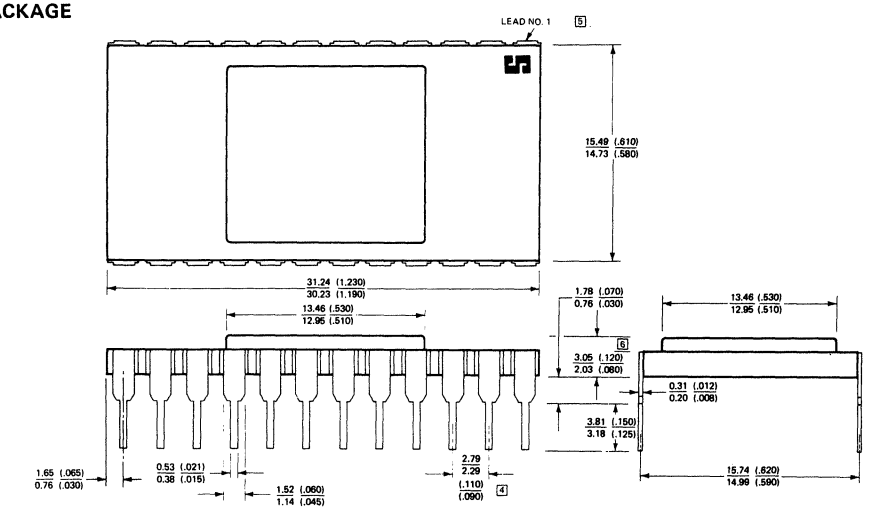
INB PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .015°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

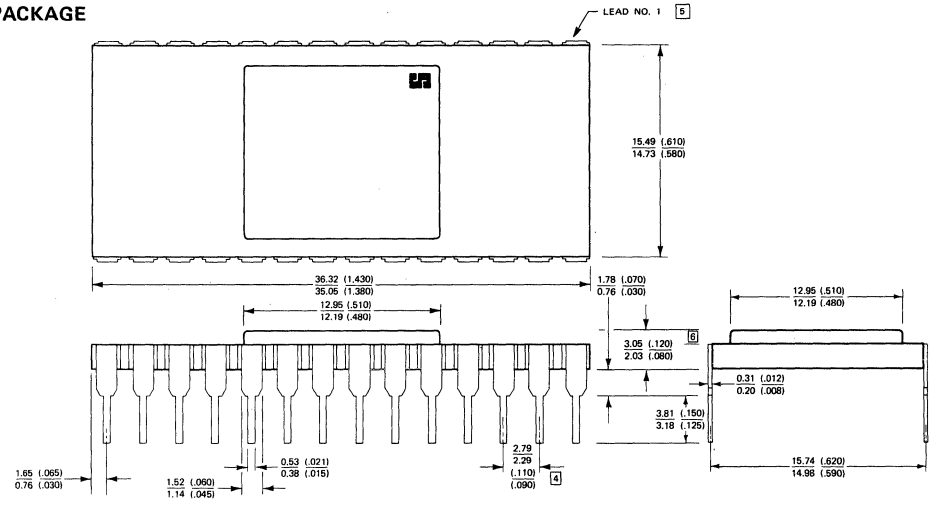
INC PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .015°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

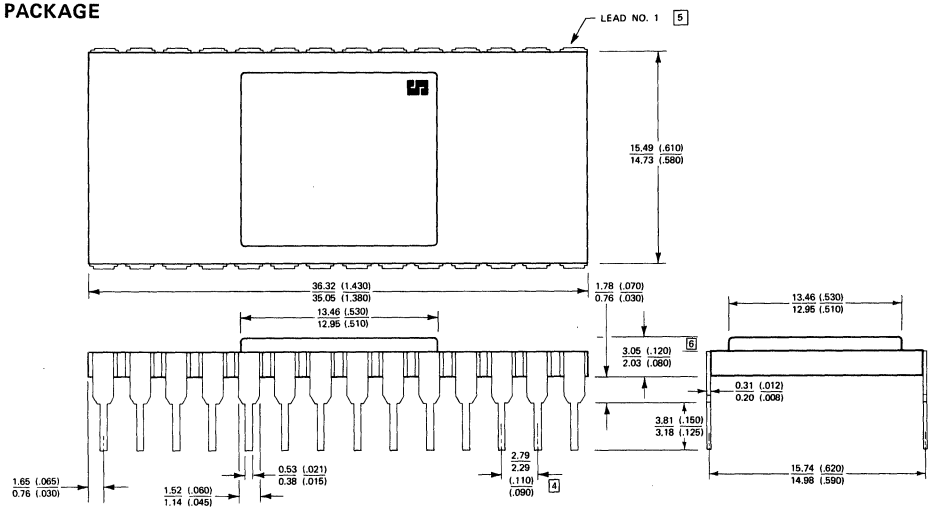
IQ PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

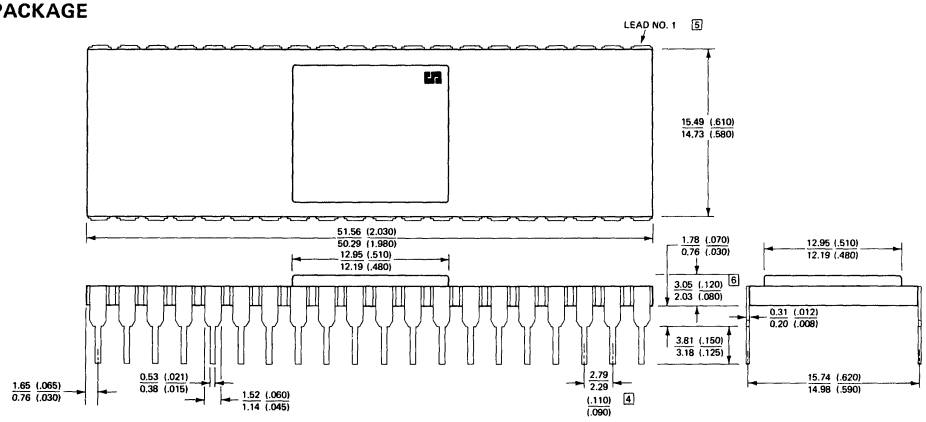
IQA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

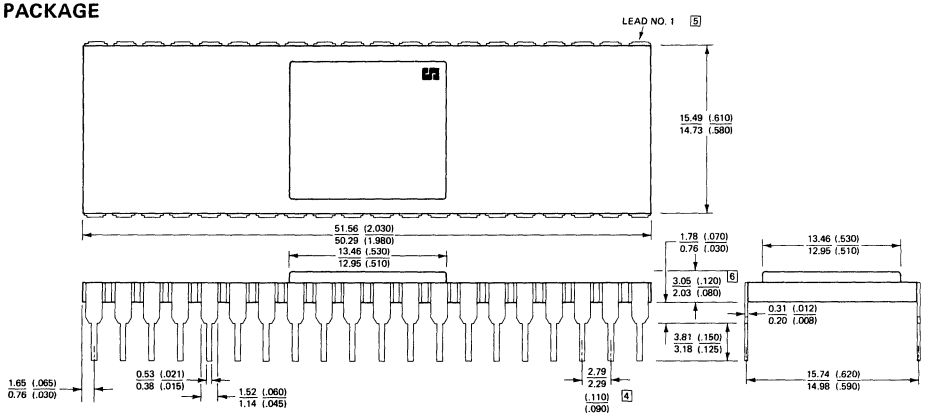
IW PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Kovar or equivalent, gold plated, alloy seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

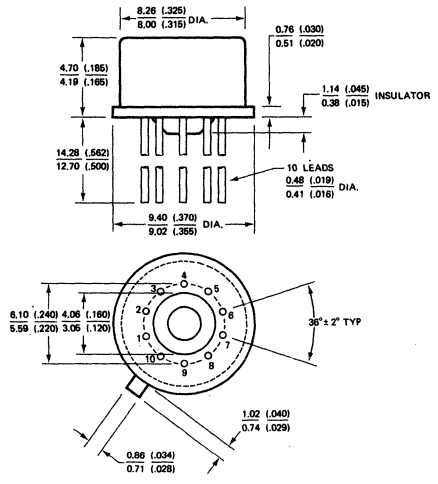
IWA PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, tin plated.
2. Body material: Ceramic with Kovar or equivalent.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Signetics symbol denotes Lead No. 1.
6. Lead spacing shall be measured within this zone.
7. Thermal resistance: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

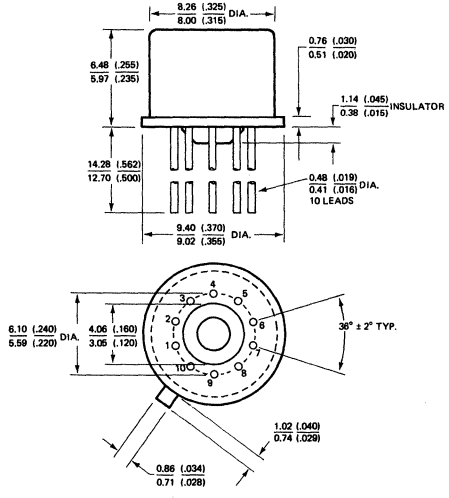
K PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent – gold plated.
2. Body Material: Eyelet, Kovar or equivalent – gold plated, glass body
3. Lid Material: Nickel, weld seal.
4. Thermal Resistance: Θ Ja = .150°C/mW, Θ Jc = .025°C/mW.
5. All dimensions shown in parentheses are English. (Inches)

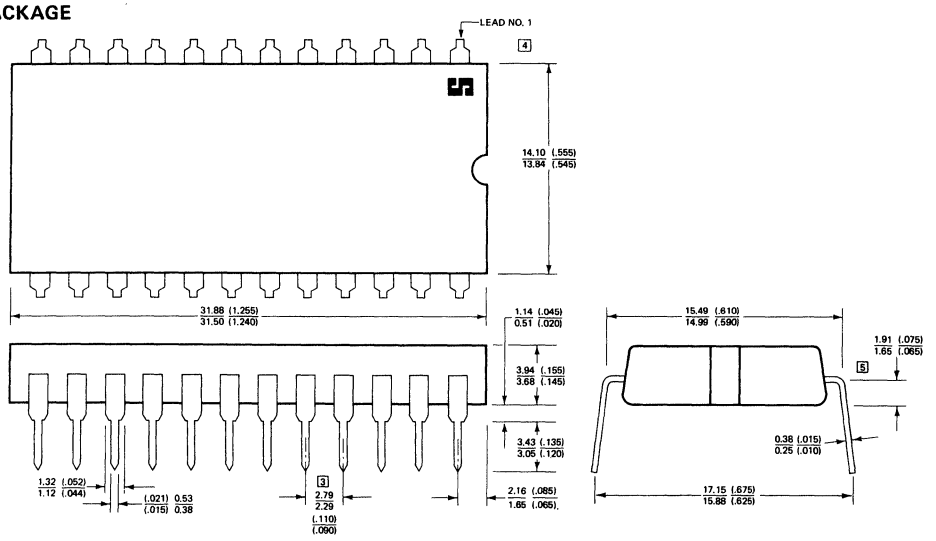
L PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent – gold plated.
2. Body Material: Eyelet, Kovar or equivalent – gold plated, glass body.
3. Lid Material: Nickel, weld seal.
4. Thermal Resistance : Θ Ja = .150°C/mW, Θ Jc = .025°C/mW.
5. All dimensions shown in parentheses are English. (Inches)

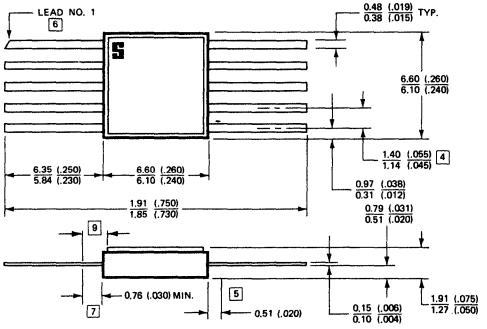
N PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .12°C/mW, Θ Jc = .05°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

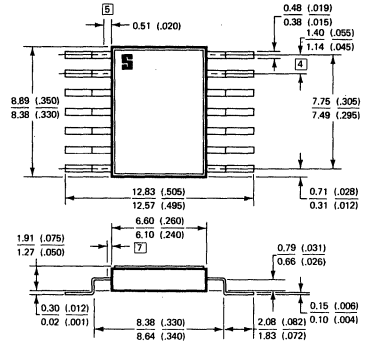
QF PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent, gold plated.
2. Body Material: Ceramic with glass seal at leads.
3. Lid Material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Thermal Resistance: Θ Ja = .175°C/mW, Θ Jc = .060°C/mW.
9. Maximum glass climb, lid skew, or frit squeeze out is .010.
10. All dimensions shown in parentheses are English. (Inches)

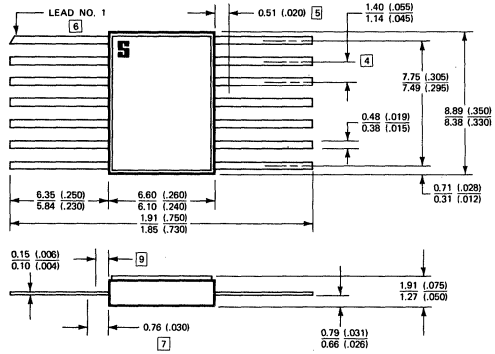
QH PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent, gold plated.
2. Body Material: Ceramic with glass seal at leads.
3. Lid Material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Thermal Resistance: Θ Ja = .170°C/mW, Θ Jc = .050°C/mW.
9. Maximum glass climb, lid skew, or frit squeeze out is .010.
10. All dimensions shown in parentheses are English. (Inches)

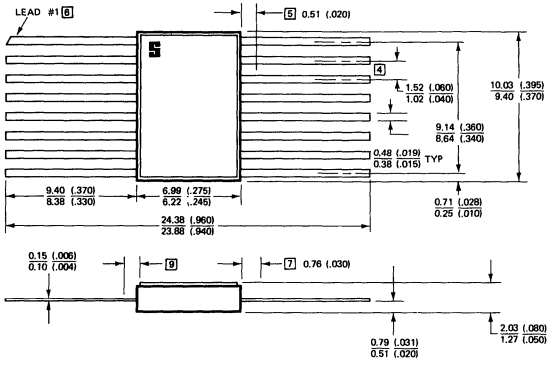
QH PACKAGE



NOTES:

1. Lead Material: Kovar or equivalent, gold plated.
2. Body Material: Ceramic with glass seal at leads.
3. Lid Material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol denotes Lead No. 1.
7. Maximum glass climb, lid skew or frit squeeze out .010.
8. Thermal Resistance; Θ Ja = .170°C/mW, Θ Jc = .050°C/mW.
9. All dimensions shown in parentheses are English. (Inches)

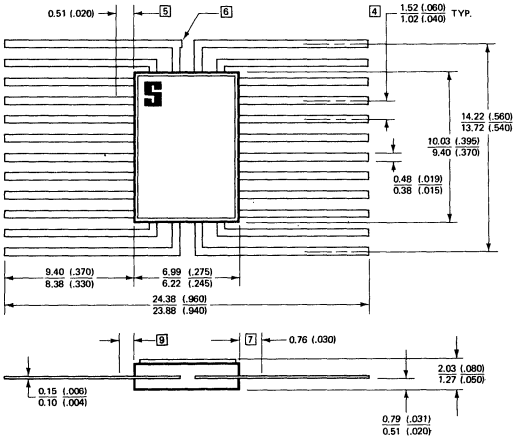
QJ PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with glass seal at leads.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Thermal resistance: Θ Ja = .160°C/mW, Θ Jc = .045°C/mW.
9. Maximum glass climb, lid skew, or frit squeeze out is .010.
10. All dimensions shown in parentheses are English. (Inches)

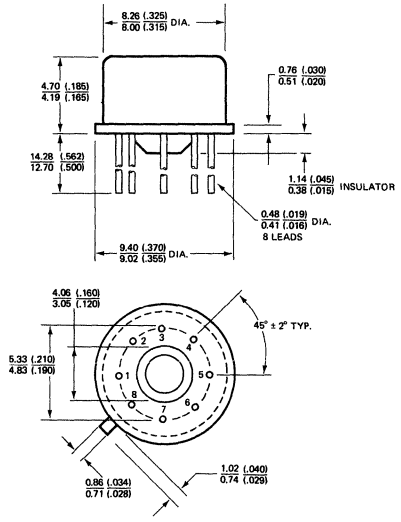
QN PACKAGE



NOTES:

1. Lead material: Kovar or equivalent, gold plated.
2. Body material: Ceramic with glass seal at leads.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Thermal resistance: Θ Ja = .150°C/mW, Θ Jc = .040°C/mW.
9. Maximum glass climb, lid skew, or frit squeeze out is .010.
10. All dimensions shown in parentheses are English. (Inches)

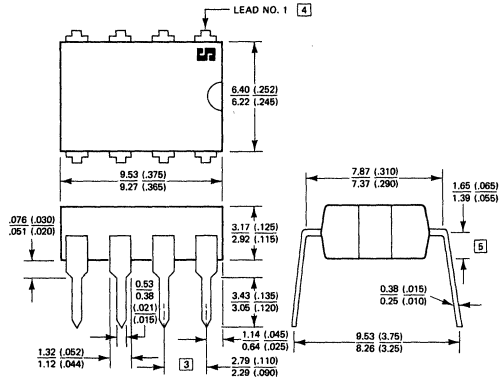
T PACKAGE



NOTES

1. Lead Material: Kovar or equivalent – gold plated.
2. Body Material: Eyelet, Kovar or equivalent – gold plated, glass body.
3. Lid Material: Nickel, weld seal.
4. Thermal Resistance: Θ Ja = .150°C/mW, Θ Jc = .025°C/mW.
5. All dimensions shown in parentheses are English. (Inches)

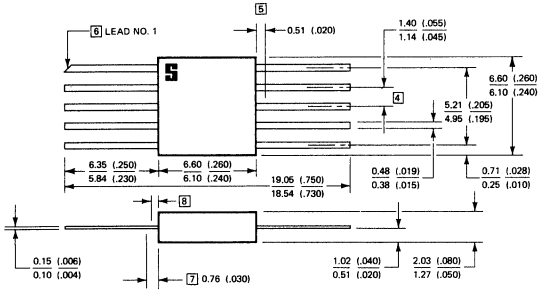
V PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW
8. All dimensions shown in parentheses are English. (Inches)

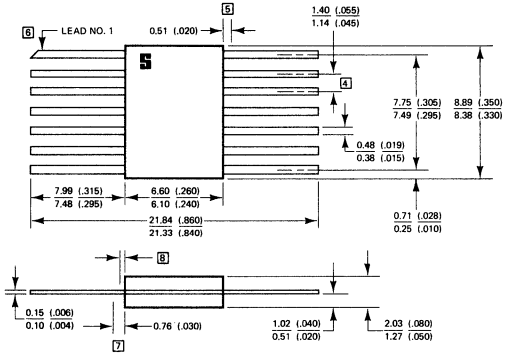
WF PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal at leads.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Maximum glass climb .010.
9. Thermal resistance: Θ Ja = .220°C/mW, Θ Jc = .085°C/mW.
10. All dimensions shown in parentheses are English. (Inches)

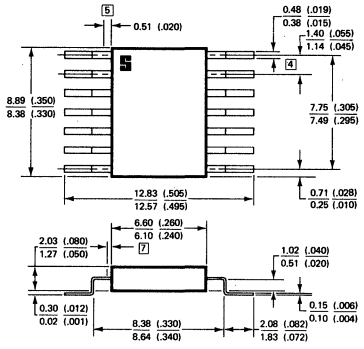
WH PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal at leads.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Maximum glass climb .010.
9. Thermal resistance: Θ Ja = .200°C/mW, Θ Jc = .085°C/mW.
10. All dimensions shown in parentheses are English. (Inches)

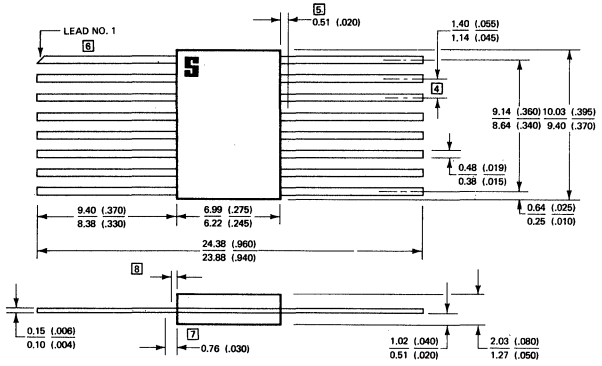
WH PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent, tin plated.
2. Body Material: Ceramic with glass seal at leads.
3. Lid Material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Maximum glass climb .010.
8. Thermal Resistance: Θ Ja = .200°C/mW; Θ Jc = .085°C/mW.
9. All dimensions shown in parentheses are English. (Inches)

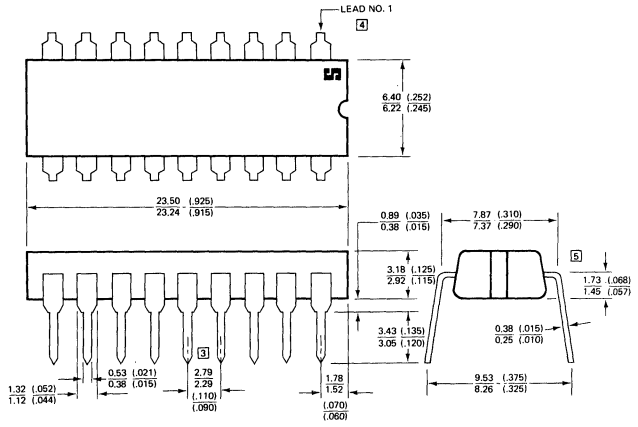
WJ PACKAGE



NOTES:

1. Lead material: Alloy 42 or equivalent, tin plated.
2. Body material: Ceramic with glass seal at leads.
3. Lid material: Ceramic, glass seal.
4. Tolerances non cumulative.
5. Lead spacing shall be measured within this zone.
6. Signetics symbol or angle cut denotes Lead No. 1.
7. Recommended minimum offset before lead bend.
8. Maximum glass climb .010.
9. Thermal resistance: Θ Ja = .195 °C/mW, Θ Jc = .085°C/mW.
10. All dimensions shown in parentheses are English. (Inches)

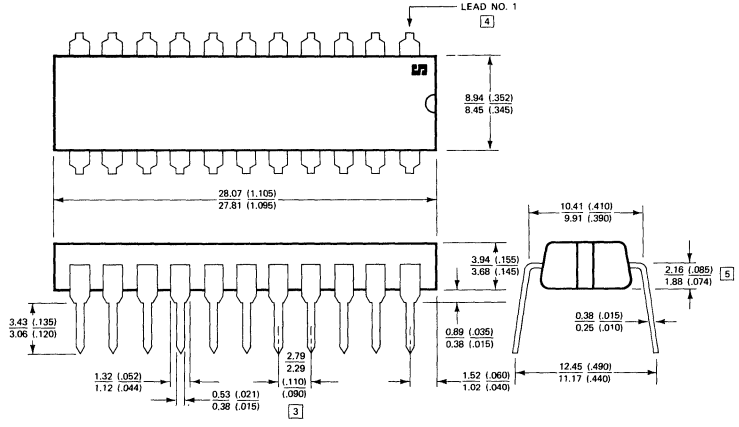
XA PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .16°C/mW, Θ Jc = .08°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

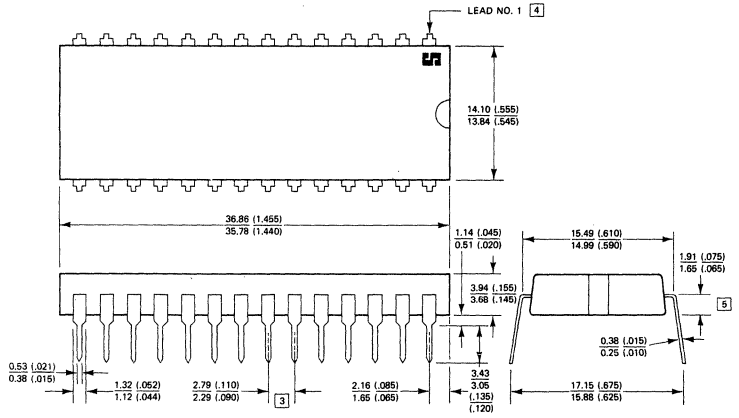
XC PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic.
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .125°C/mW, Θ Jc = .055°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

XF PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent.
2. Body Material: Plastic
3. Tolerances non cumulative.
4. Signetics symbol denotes Lead No. 1.
5. Lead spacing shall be measured within this zone.
6. Body dimensions do not include molding flash.
7. Thermal Resistance: Θ Ja = .12°C/mW, Θ Jc = .05°C/mW.
8. All dimensions shown in parentheses are English. (Inches)

signetics
811 EAST ARQUES AVENUE
SUNNYVALE, CALIF. 94086
TEL: (408) 739-7700
TWX: (910) 339-9283
A Subsidiary of CORNING GLASS WORKS