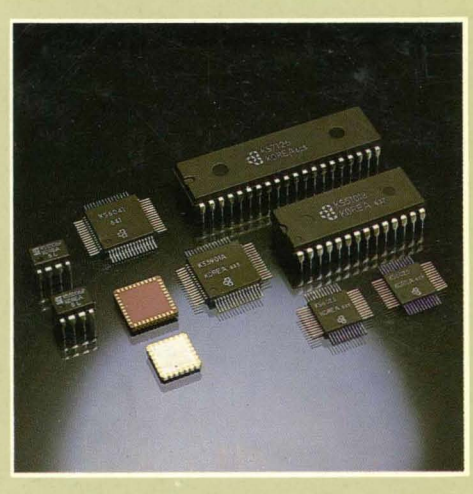
SAMSUNG

MOS Products Data Book



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2.1 RELIABILITY TESTS

Samsung has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the MOS IC family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.

Listed below are details of tests performed to ensure that manufactured product continues to meet Samsung's stringent quality standards. In line quality controls are reviewed extensively in later sections.

The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situtations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of major stresses (and their conditions) run by Samsung on MOS IC products.

HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

($T_j = 125°C$, $V_{CC} = V_{CC}$ max, static)

High temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

($Ta = 85°C$, R.H. = 85%, $V_{CC} = V_{CC}$ opt, static)

Wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/85 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

HIGH TEMPERATURE STORAGE TEST (HTS)

($Ta = 125°C$, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity, and process wearout mechanisms.

PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stess uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)

This stress uses a chamber with alternting temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

Table 1. Reliability Test Items for MOS Product

No.	Test Item	Test Condition	Corrective Test Method	Qualification			Product Rel. Monitor		
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR
1	Visual Inspection Critical Major Minor	Outgoing Visual Spec		 116 116 116	 2 3 5	 0 1 2	 116 116 116	 2 3 5	 0 1 2
2	Electrical Test Critical Major Minor	Outgoing Test Spec		 116 116 116	 2 3 5	 0 1 2	 116 116 116	 2 3 5	 0 1 2
3	Dimension	VIS/MECH Criteria		50	—	0	50	—	0
4	Packing Inspection	Outgoing Packing Criteria		Each Lot			Each Lot		
5	Operating Life Test	$T_a = 25°C$ $V_{CC} = V_{CC}$ (max) 1000 HRS	MIL-STD-883 1005	45	10	1	45	10	1
6	High Temperature OPL	$T_a = 125°C$ Static $V_{CC} = V_{CC}$ (max) 1000 HRS	MIL-STD-883 1005	45	10	1	45	10	1
7	Low Temperature Storage	$T_a = -55°C$ 1000 HRS		45	10	1	45	10	1
8	High Temperature Storage	$T_a = 125°C$ 1000 HRS		45	10	1	45	10	1
9	Pressure Cooker Test	$T_a = 121°C \pm 2°C$ RH = 100% 15 PSIG 168 HRS		45	10	1	45	10	1
10	Liquid Thermal Shock Test	$-55°C \rightleftarrows 150°C$ 5 min, <10 Sec, 5 min 200 Cycles	MIL-STD-883 1011	45	10	1	45	10	1
11	Temperature Cycle	$-65°C \rightleftarrows 25°C \rightleftarrows 150°C$ 10 min, 5 min, 10 min 200 Cycles	MIL-STD-883 1010	45	10	1	45	10	1
12	Solder Heat Resist	$260°C \pm 5°C$ 10 ± 1 Sec Once without Flux		45	10	1	45	10	1
13	Wet High Temp. Storage	$T_a = 85°C$, RH = 85% 1000 HRS		45	10	1	45	10	1
14	Wet High Temperature OPL	$T_a = 85°C$, RH = 85% $V_{CC} = V_{CC}$ (TYP) 1000 HRS		45	10	1	45	10	1

Table 1. Reliability Test Items for MOS Product (Continued)

No.	Test Item	Test Condition	Corrective Test Method	Qualification			Product Rel. Monitor		
				Sample Size	LTPD	Acceptance NBR	Sample Size	LTPD	Acceptance NBR
15	Moisture Resistance	90~98%/65°C 3 HRS 80~98%/25°C 8 HRS 90~98%/65°C 3 HRS	MIL-STD-883 10004	45	10	1	45	10	1
16	Lead Integrity	1) Wire Lead 0.229±0.0144kg for Three 90±5° Arcs on each Leads Bending Cycle: 2 5 Sec 2) Dial-in-lines	MIL-STD-883 2004	32	7	0	32	7	0
17	Solderability	260°C±10°C Preconditioning 1 HRS.	MIL-STD-883 2003	22	10	0	22	10	0
18	Marking Permanancy	Rub Marking with Ten Stokes of a Cotton Cloth Damped with Solvents		22	10	0	22	10	0
19	Mechanical Shock	Pulse Duration: 0.1 1m Sec Shock Pulse: 0.5 3kg	MIL-STD-883 2002	32	7	0	32	7	0
20	Vibration Fatique	20G-3 Axis Orientations f=20 to 2000 CPS for 4 Minute Cycle	MIL-STD-883 3007A	32	7	0	32	7	0
21	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	MIL-STD-883 2001	32	7	0	32	7	0
22	Salt Atmosphere	Nacl T_a=35°C, 24 HRS	MIL-STD-883 1009A	45	10	1	45	10	1
23	Set Aging	—	—	32	7	0	32	7	0
24	ESD	C=200pF R=1.5K	MIL-STD-883 3015 DOD-HDBK-263	5	—	0	5	—	0
25	Sulfide Corrosion Test	T_a=25±2°C Humidity: 75% R/H SO_2: 10±2ppm Velocity: 0.006 0.007m/s	DIN 40046	32	7	0	32	7	0

Table 2. Failure Criteria for MOS Product

Parameter	Symbol	Life End Limit		Unit
		Min	Max	
Output Drive Current (P-CH)	I_{DP}	LSLX0.9	USLX1.1	A
Output Drive Current (N-CH)	I_{DN}	LSLX0.9	USLX1.1	A
Output High Voltage	V_{OH}	LSLX0.9	—	
Output Low Voltage	V_{OL}	—	USLX1.1	V
Input Current	I_{IN}	—	USLX2.0	V
Quiescent Current	I_L	—	USLX2.0	A
Voltage Margin		0.05XUSL + 0.95XLSL	0.95XUSL + 0.05XLSL	V
AC Characteristic Open/Short		LSLX0.9	USLX1.1	Sec
Gross/Fine Leak Visual Color Disturbance Soldering Marking Disturbance		Individual Spec		

Note: LSL: Lower Specification Limit
USL: Upper Specification Limit

2.2 METHODOLOGY OF RELIABILITY TEST

RELIABILITY

Reliability can be loosely characterized as long term product quality.

There are two types of reliability tests: those performed during design and development, and those carried out in production. The first type is usually performed on a limited sample, but for long periods or under very accelerated conditions to investigate wearout mechanisms and determine tolerances and limits in the design process. The second type of tests is performed periodically during production to check, maintain, and improve the assured quality and reliability levels. All reliability tests performed by Samsung are under conditions more severe than those encountered in the field, and although accelerated, are chosen to simulate stresses that devices will be subjected to in actual operation. Care is taken to ensure that the failure modes and mechanisms are unchanged.

FUNDAMENTALS

A semiconductor device is very dependent on its conditions of use (*e.g.,* junction temperature, ambient temperature, voltage, current, *etc.*). Therefore, to predict failure rates, accelerated reliability testing is generally used. In accelerated testing, special stress conditions are considered as parametrically related to actual failure modes. Actual operating life time is predicted using this method. Through accelerated stresses, component failure rates are ascertained in terms of how many devices (in percent) are expected to fail for every 1000 hours of operation. A typical failure rate versus time of activity graph is shown below (the so-called "bath tub curve")

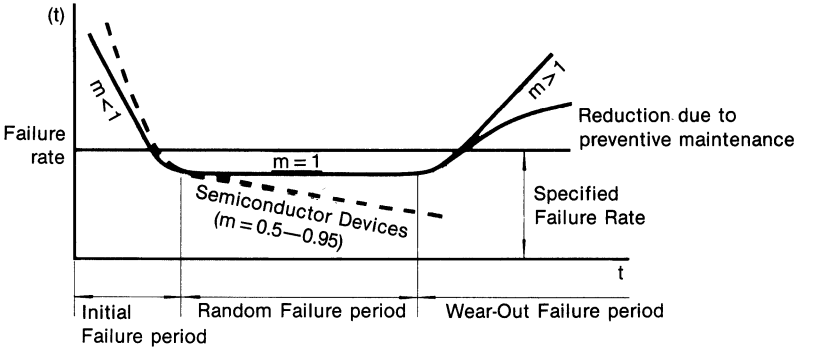


Figure 3. Failure Rate Curve ("Bath Tub Curve")

During their initial time period, products are affected by "infant mortality," intrinsic to all semiconductor technologies. End users are very sensitive to this parameter, which causes early assembly/operation failures in their own system. Periodically, Samsung reviews and publishes life time results. The goal is a steady shift of the limits as shown below.

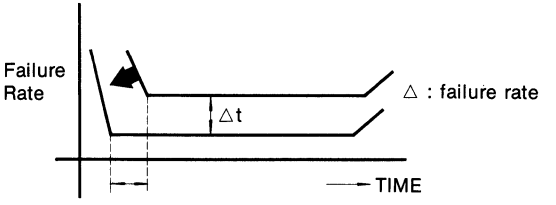


Figure 4. Failure Rate

ACCELERATED HUMIDITY TESTS

To evaluate the reliability of products assembled in plastic packages, Samsung performs accelerated humidity stressing, such as the Pressure Cooker Test (PCT) and Wet High Temperature Operating Life Test (WHOPL).

Figure 5 shows some results obtained with these tests, which illustrate the improvements in recent years. These improvements result mainly from the introduction of purer molding resins, new process methods, and improved cleanliness.

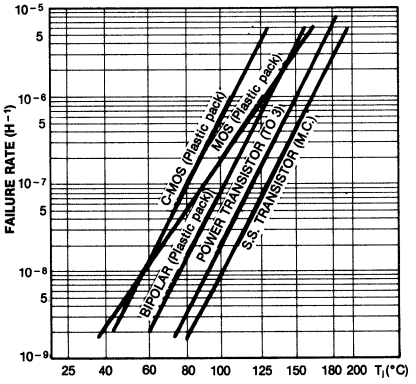


Figure 5. Improvement in Humidity Reliability

ACCELERATED TEMPERATURE TESTS

Accelerated temperature tests are carried out at temperatures ranging from 75°C to 200°C for up to 2000 hours. These tests allow Samsung to evaluate reliability rapidly and economically, as failure rates are strongly dependent on temperature.

The validity of these tests is demonstrated by the good correlation between data collected in the field and laboratory results obtained using the Arrhenius model. Figure 6 shows the relationship between failure rates and temperatures obtained with this model.

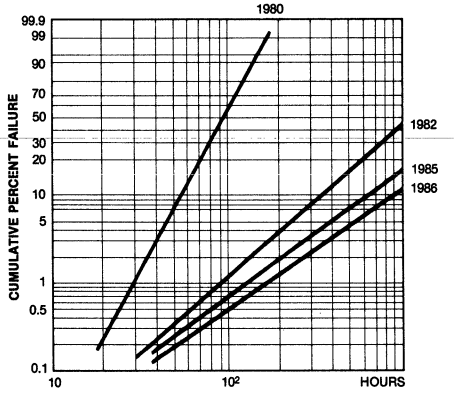


Figure 6. Failure Rate Versus Temperature

2.3 FUNDAMENTAL THEORY FOR ACCELERATED TESTING

Accelerated life testing is powerful because of its strong relation to failure physics. The Arrhenius model, which is generally used for failure modelling, is explained below.

Arrhenius model

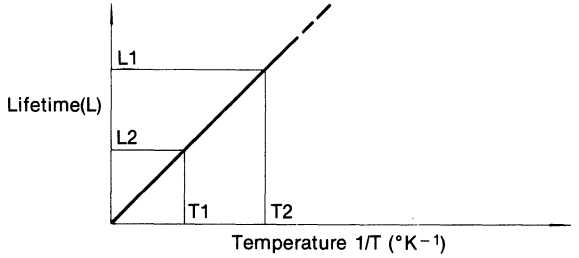
This model can be applied to accelerated Operating Life Tests and uses absolute (Kelvin) temperatures.

$L = A + Ea/K \cdot Tj$

- L : Lifetime
- A : Constant
- Ea : Activation Energy
- K : Boltzman's constant
- Tj : Absolute Junction temperature

If Lifetimes L1 and L2 correspond to Temperatures T1 and T2,

$$L1 = L2 \exp\left[\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right]$$



Actual junction temperature should always be used, and can be computed using the following relationship.

$$Tj = Ta + (P \times \theta ja)$$

Where Tj = Junction temperature
Ta = Ambient temperature
P = Actual power consumption
θ ja = Junction to Ambient thermal resistance (typically 100 degrees celsius/watt for a 16-Pin DIP).

Activation Energy Estimate

Clearly the choice of an appropriate activation energy, Ea, is of paramount importance. The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the literature. The Arrhenius equation describes the rate of many processes responsible for the degradation and failure of electronic components. It follows that the transition of an item from an initially stable condition to a defined degraded state occurs by a thermally activated mechanism. The time for this transition is given by an equation of the form:

$MTBF = B\ EXP\ (Ea/KT)$
MTBF = Mean time between failures
B = Temperature-independent constant

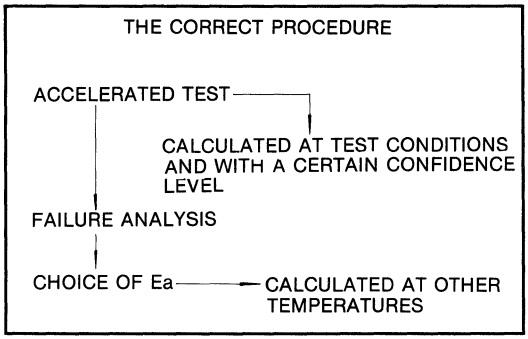
MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting the MTBF equation. The acceleration effect for a 125°C device junction stress with respect to 70°C actual device junction operation is equal to 1000 for Ea = 1eV and 7 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

A. They are often related to high-temp tests where a single Ea (with high value) mechanism has become dominant.
B. They are specifically related to the devices produced by that supplier (and to its technology) for a given period of time
C. They could be modified by the mutual action of other stresses (voltage, mechanical, etc.)
D. Field device-application condition(s) should be considered.

Table 3. Activation energy for each failure mode

Failure Mechanism	Ea
Contamination	1 ~ 1.4 eV
Polarization	1 eV
Aluminum Migration	0.5 ~ 1 eV
Trapping	1 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.3 ~ 0.5 eV



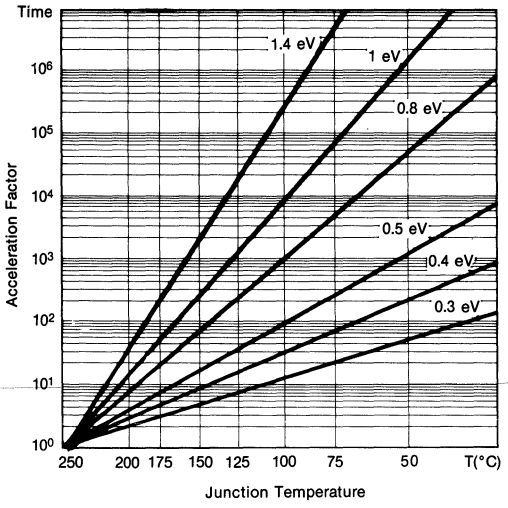


Figure 7. Acceleration Factor vs Activation Energy

2.4 Failure Rate Prediction

Accelerated testing defines the failure rate of products. By derating the data at different conditions, the life expectancy at actual operating conditions can be predicted. In its simplest form the failure rate (at a given temperature) is:

$$FR = \frac{N}{DH}$$

Where FR = Failure Rate
N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the FR at different temperatures, an acceleration factor must be considered. Some failure modes are accelerated via temperature stressing based upon the accelerations of the Arrhenius Law.

For two different temperatures:

$$FR\ (T1) = FR\ (T2)\ \exp\left[\frac{Ea}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

FR (T1) is a point estimate, but to evaluate this data for an interval estimate, we generally use a χ^2 (chi square) distribution. An example follows:

Failure Rate Elaluation

Unit: %/1000HR

Dev. x Hours at 125°C	Fail	Failure Rate at 60% Confidence Level			
1.7×10^6	2	Point Estimate	85°C	70°C	55°C
		0.18	0.0068	0.0018	0.00036

The activation energy, from analysis, was chosen as 1.0 eV based upon test results. The failure rate at the lower operating temperature can be extrapolated by an Arrhenius plot.

Process Monitor (Continued)

Process	Control Item	Spec. Limit	Insp. Frequency
Thin Film	• Cooling Water Temp. • Thickness	• 26 ± 3°C • Individual Spec.	Once/Shift Once/Shift
CVD	• Pin Hole • Thickness	• Individual Spec. • Individual Spec.	Once/Shift Once/Shift
Diffusion	• Tube Temp. • C-V Plot Run Tube • Sheet Resistance • Thickness	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/10days Once/Shift Once/Shift

Raw Material Incoming Inspection

1. Mask Inspection

Defect Detection	• Pinhole & Clear-extension • Opaque Projections & Spots • Scratch/Particle/Stain • Substrate Crack/Glass-chip • Others	All Masks	• Defect Size $\leq$ 1.5μm • Defect Density $\leq$ 0.124EA/cm^2
Registration	• Run-out (X-Y Coordinate) • Orthogonality • Drop-in Accuracy • Die Fit/Rotation	20% • All New Masks	± 0.75μm ± 0.75μm ± 0.50μm ± 0.50μm
Critical Dimension	• Critical Dimension	All Masks	Purchasing Spec.

* Instrument
- Auto mask inspection system for defect-detection (NJS 5MD-44)
- Comparator for registration (MVG 7X7)
- Automatic linewidth measuring system for CD (MPV-CD)

2. Wafer Inspection

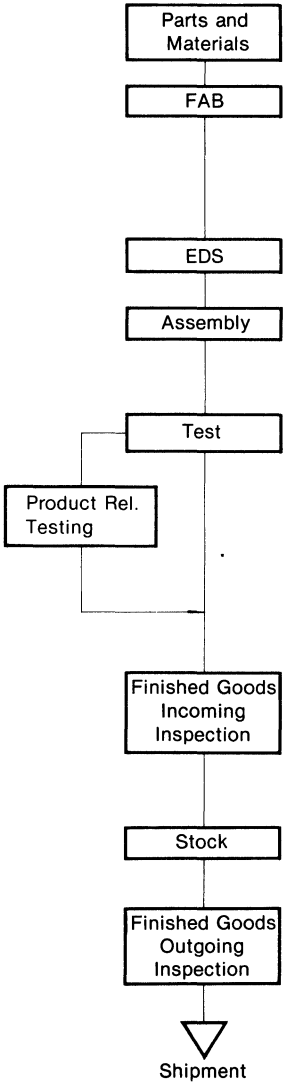
Purpose	Insp. Items	Sample	Remarks
Structural	• Crystallographic Defect	All Lots	• Sirtl Etch
Electrical	• Resistivity • Conductivity	All Lots	• Monitor Water
Dimensional	• Thickness • Diameter • Orientation • Flatness	All Lots	TTV, NTV, Epi-thickness TIR (FPD) Local Slope
Visual	• Surface Quality • Cleanliness	All Lots	Purchasing Spec.

* Instrument
- 4 point probe for resistivity (Kokusai VR-40A, Tencor sonogage, ASM AFPP)
- Flatness measuring system (Siltec)
- Epi. layer thickness gauge (Digilab FTG-12, Qualimatic S-100)
- Automatic Surface Insp. System (Aeronca Wis-150)
- Non-contact thickness gauge (ADE6034)

3. PROCESS CONTROL

GENERAL PROCESS CONTROL

The general process flow in Samsung is shown in Figure 8. This illustration contains the standard process flow from incoming parts and materials to customer shipment.



Acceptance inspection (according to acceptance inspection plan)

Process quality control
- Check of each condition by process quality control procedures
- Process inspection
- Lot control
- Equipment calibration and maintenance

100% Electrical Die Sorting

Process Quality Control and screening of infant mortality defects
- Mechanical screen
- Thermal shock
- Burn-in

100% package sorting of electrical characteristics and marking

Reliability monitoring
1. Product rel. monitor I.
2. Product rel. monitor II.

- High Temperature Operating Life Test
- Environmental test
- Life Test

Sampling Inspection
- Dimensions
- Visual
- Electrical characteristics
- Periodic calibration of measuring equipment

Stock control
- Age control

Sampling Inspection (when applicable)

Figure 8. General Process Flow Chart

3.1 WAFER FABRICATION

Process Controls

The Quality Control program utilizes the following methods of control to achieve its previously stated objectives: process audits, environmental monitors, process monitors, lot acceptance inspections, and process integrity audits.

Definitions

The essential method of the Quality Control Program is defined as follows:

1. Process Audit-Performed on all operations critical to product quality and reliability.
2. Environmental Monitor-Monitors concerning the process environment, *i.e.,* water purity, temperature, humidity, particle counts.
3. Process Monitor-Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variable data.
4. Lot Acceptance-Lot-by-lot sampling. This sampling method is reserved for those operations deemed as critical, and require special attention.

Environmental Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Clean Room	• Temperature • Humidity • Particle • Air Velocity	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	24 Hrs. 24 Hrs. 24 Hrs. 24 Hrs.
D.I. Water	• Particle • Bacteria • Resistivity	• 5 ea/50ml (0.8μ) • 50 colonies/100ml (0.45μ) • Main (Line): More than 16 Mohm-cm • Using point: More than 14 Mohm-cm	24 Hrs. Weekly 24 Hrs. 24 Hrs.

* Instruments
- FMS (Facility Monitoring System) HIAC/ROYCO
- CPM (Central Particle Monitoring System-Dan Scientific)
- Liquid Dust Counter Etch Rate
- Filtration System for Bacterial check
- Air Particle counter
- Air Velocity meter

Process Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Photo	• Aligner N_2 Flow Rate	• Individual Spec.	Once/Shift
	• Aligner Vacuum	• Individual Spec.	Once/Shift
	• Aligner Air	• Individual Spec.	Once/Shift
	• Aligner Pressure	• Individual Spec.	Once/Shift
	• Aligner Intensity	• Individual Spec.	Once/Shift
	• Coater Soft Bake Temperature	• Individual Spec.	Once/Shift
	Vacuum	• Individual Spec.	Once/Shift
		• Individual Spec.	Once/Shift
Etch	• Etchant Temp.	• Individual Spec.	Once/Shift
	• Etch Rate	• Individual Spec.	Once/Shift
	• Spin Dryer N_2 Flow	• Individual Spec.	Once/Shift
	RPM	• Individual Spec.	Once/Shift
	• Hard Bake Temp.	• Individual Spec.	Once/Shift
	N_2 Flow	• Individual Spec.	Once/Shift

In-Process Quality Inspection (FAB)

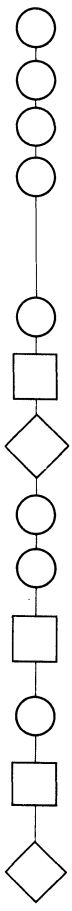
1. Manufacturing Section

Process Step	Process Control Insp.	Frequency
Oxidation	Oxide Thickness	All Lots
Diffusion	Oxide Thickness Sheet Resistance Visual	All Lots All Lots All Lots
Photo	Critical Dimension Visual Mask Clean Inspection	All Lots (MOS) All Lots All Masks with Spot Light (MOS) or Microscope (BIP)
Etch	Critical Dimension Visual	All Lots All Wafers
Thin Film	Metal Thickness Visual	All Lots All Lots
Ion Implant	Sheet Resistance	All Lots (Test Wafer)
Low Temp. Oxide	Thickness	All Lots
	Visual	All Lots
E-Test	Electrical Characteristics	All Lots
Fab. Out	Visual	All Wafers

2. FAB, QC Monitor/Gate

Process Step	FAB, QC Insp.	Frequency
Oxidation	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN Once/Shift
Diffusion	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN Once/Shift
Photo	Critical Dimension Visual Mask CLN Inspection	All Lots (MOS) Once/Shift All Masks After 10 Times Use
Etch	Critical Dimension Visual	All Lots (MOS) All Lots
Thin Film	C-V Test on Tubes on Lots Reflectivity	Once/10 Days and After CLN Once/Shift Once/Shift
Low Temp. Oxide	Refractive Index, Wt% of Phosphorus Visual	1 Test Wafer/Lot 1 Test Wafer/Lot 1 Test Wafer/Lot
E-Test	Measuring Data	All Lots
Calibration	Instrument for Thickness and C.D. Measuring	Once/week

3. Photo/Etch process quality control

Process Flow	Process Step	MFG. Control Item	QC Monitor/Gate
	Prebake	Oven PM, Temperature Time	Oven Particle Temp. N_2 Flow Rate
	Photo Resist (PR) —spin	Thickness Machine PM	
	Soft Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Align/Expose	Light Uniformity Alignment, Focus Test Mask Clean Inspection Mask Clean Exposure Light Intensity	Light Intensity Mask Clean Insp.
	Develop	Equipment PM Solution Control	Vacuum
	Develop Check	PR/C.D.'S Alignment Particles Mask and Resist Defects	
	QC Inspection		Critical Dimension (CD)
	Hard Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Etch	Etch rate, Equipment PM & Settings, Etch Time to Clear	Etchant Temp. Etch Rate
	Inspection	Over/Under	
	PR Strip	Machine-PM	
	Final Check	C.D.'S Over and under Etch, Particles, PR Residue, Defects, Scratches	
	QC Inspection		Same as Final Check, However, More Intense on limited Sample Basis. (AQL 6.5%)

Note: PM represents Preventive Maintenance

4. Reliability-related Interlayer Dielectric, Metallization, and Passivation Process Quality Control Monitor

Item	Frequency
Wt% Phosphorus Content of the Dielectric Glass	1/Shift
Metallization Interconnect	1/Month
Al Step Coverage	1/Month
Metallization Reflectivity	1/Shift
Passivation Thickness and Composition	1/Shift
Thin Film Defect Density	1/Shift

Figure 9. General Wafer Fabrication Flow

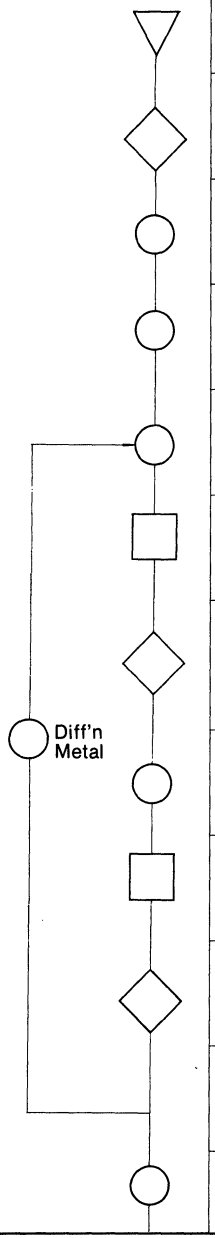
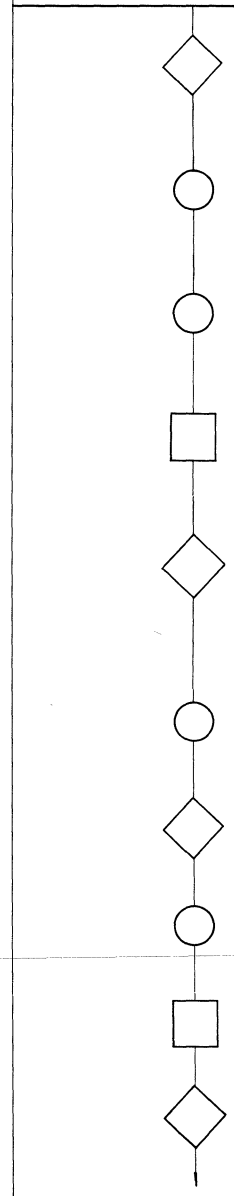
Process Flow	Process Step	Major Control Item
	Wafer and Mask Input	
	Starting Material Incoming Inspection	Mask: (See mask Inspection) Wafer: (See wafer Inspection)
	Wafer Sorting and Labelling	Resistivity
	Initial Oxidation	Oxide Thickness
	Photo	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension
	Etch	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension • Visual/Mech
	Diffusion Metalization	• (See in-process Quality Inspection)
	E-test	• Electrical Characteristics

Figure 9. General Wafer Fabrication Flow (Continued)

Process Flow	Process Step	Major Control Item
	QC Gate	• Electrical Characteristics
	Back-Lap	• Thickness
	Back Side Evaporation	• Thickness, Time Evaporation Rate
	Final Inspection	• All Wafers Screened (Visual/Mech)
	QC Fab. Final Gate	• Visual/Mech. — Major: AQL 1.0% — Minor: AQL 6.5%
	EDS (Electrical Die Sorting)	
	QC Gate	• Function Monitor
	Sawing	
	Inspection	• Chip Screen
	QC Final Inspection	• AQL 1.0% • Fab. Defect • Test Defect • Sawing Defect
Die Attach		

3.2 ASSEMBLY

The process control and inspection points of the assembly operation are explained and listed below:

1. Die Inspection:

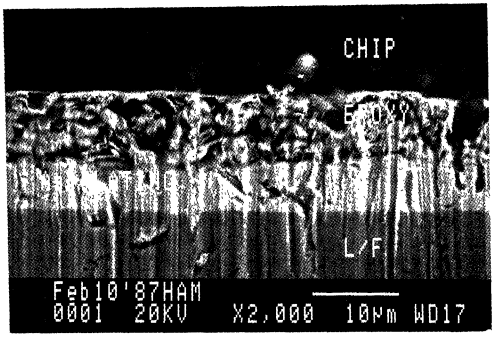
   Following 100% inspection by manufacturing, in-process Quality Control samples each lot according to internal or customer specifications and standards.

2. Die Attach Inspection:

   Visual inspection of samples is done periodically on a machine/operator basis. Die Attach techniques are monitored and temperatures are verified.

3. Die Shear Strength:

   Following Die Attach, Die Shear Strength testing is performed periodically on a machine/operator basis. Either manual or automatic die attach is used.



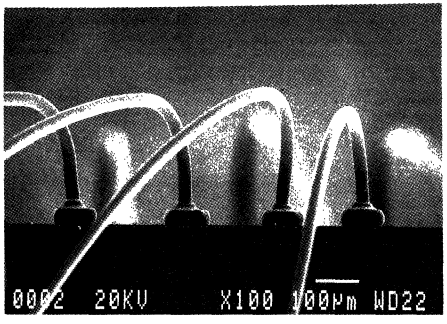
DIE ADHESIVE THICKNESS MONITOR RESULTS. (JEOL SEM, JSM IC845)

4. Wire Bond Inspection:

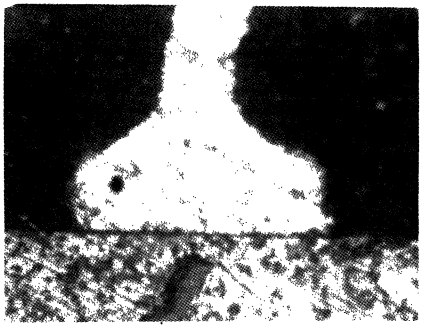
   Visual inspection of samples is complemented by a wire pull test done periodically during each shift. These checks are also done on a machine/operator basis and XR data is maintained.

5. Pre-Seal/Pre-Encapsulation Inspection:

   Following 100% inspection of each lot, samples are taken on a lot acceptance basis and are inspected according to internal or customer criteria.



WIRE LOOP MONITOR RESULTS.



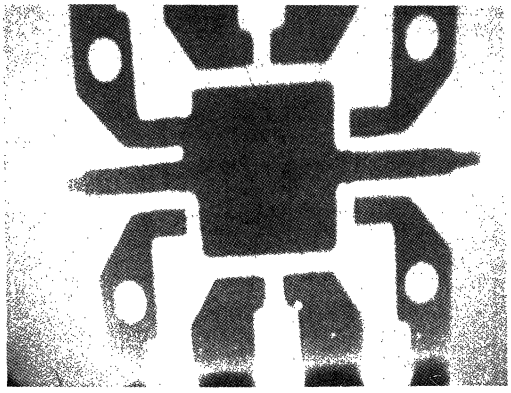
CROSS SECTION INSPECTION FOR BALL BOND.

6. Seal Inspection:

   Periodic monitoring of the sealing operation checks the critical temperature profile of the sealing oven for both glass and metal seals.

7. Post-Seal Inspection:

   Subsequent to a 100% visual inspection, In-Process Quality Control samples each for conformance to visual criteria.



X-RAY MONITOR RESULT. (PHILIPS MG161)

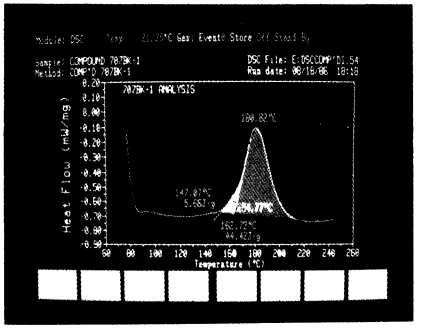
8. General Assembly Flow is shown in Figure 11.

Sampling Plans

1. Sampling plans are based on an AQL (Acceptable Quality Level) concept and are determined by internal or by customer specifications.

2. Raw Material Incoming Inspection. (confined)

Material	Inspection Item	Acceptable Quality Level
Lead Frame	1) Visual Inspection 2) Dimension Inspection 3) Function Test 4) Work Test	LTPD 10%, C=2 LTPD 20%, C=0 LTPD 20%, C=0 LTPD 20%, C=0
Wafer	1) Visual Inspection	AQL 0.65%
Au/Al Wire	1) Visual Inspection 2) Bond Pull Strength Test 3) Bondability Test 4) Chemical Composition Analysis	LTPD 20%, C=0 LTPD 15% C=2 Critical Defect: LTPD 1.5% C=6 Major Defect: LTPD 1.5% C=6 Minor Defect: LTPD 1.5% C=6 n: 4, C=0
Molding Compound	1) Visual Inspection 2) Moldability Test 3) Chemical Composition Analysis	n: 5, C=0 Critical Defect: LTPD 0.15% Major Defect: LTPD 1.0% Minor Defect: LTPD 1.5% n: 5, C=0



MOLDING COMPOUND INCOMING INSPECTION
(THERMAL ANALYSER, DUPONT 9900)

(Continued)

Material	Inspection Item	Acceptable Quality Level
Packing Tube & Pin	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15%, C = 2 n: 10, C = 0 n: 10, C = 0 n: 10, C = 0
Solder	1) Visual Inspection 2) Weight Inspection 3) Chemical Composition Analysis	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 20% C = 0
Flux	1) Acidity Test 2) Specific Gravity Test 3) Chemical Composition Analysis	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 20% C = 0
Solder Preform	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 2.5% AQL 2.5% AQL 2.5%
Coating Resin	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Marking Ink	1) Work Test 2) Mark Permanency Test	Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C = 0
Chip Carrier	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15% C = 2 LTPD 15% C = 0 n: 5, C = 0 n: 5, C = 0
Vinyl Pack	1) Visual Inspection 2) Work Test 3) Electro-Static Inspection	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 15% C = 0
Ag Epoxy	1) Work Test 2) Chemical Composition Analysis	AQL 2.5% AQL 2.5%
Letter Marking	1) Visual Inspection 2) Work Test	100% Inspection C = 0
Spare Parts & Others	1) Dimension Inspection 2) Visual Inspection	AQL 0.65% LTPD 20%

3. In-Process Quality Inspection

A. Assembly Lot Acceptance Inspection

(1) Acceptance quality level for wire bond gate inspection

Defect Class	Inspection Level	Type of Defect	
Critical Defect	AQL 0.65%	— Missing Metal — Chip Crack — No Probe — Epoxy on Die — Mixed Device — Wrong Bond — Missing Bond	— Diffusion Defect — Ink Die — Exposed Contact — Bond Short — Die Lift — Broken Wire
Major Defect	AQL 1.0%	— Metal Missing — Metal Adhesion — Pad Metal Discolored — Tilted Die — Die Orientation — Partial Bond	— Oxide Defect — Probe Damage — Metal Corrosion — Incomplete Wetting — Weakened Wire
Minor Defect	AQL 1.5%	— Adjacent Die — Passivation Glass — Die Attach Defect — Wire Loop Height — Extra Wire	— Contamination — Ball Size — Wire Clearance — Bond Deformation

(2) Acceptance quality level for Mold/Trim gate inspection

Defect Class	Inspection Level	Kind of Defect	
Critical Defect	AQL 0.10%	— Incomplete Mold — Void, Broken Package — Misalignment	— Deformation — No Plating — Broken Lead
Major Defect	AQL 0.4%	— Ejector Pin Defect — Package Burr — Flash on Lead	— Crack, Lead Burr — Rough Surface — Squashed Lead
Minor Defect	AQL 0.65%	— Lead Contamination — Poor Plating — Package Contamination	— Bent Lead

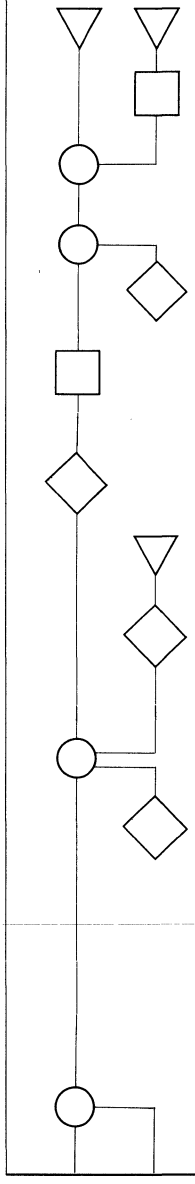
B. In-process monitor inspection

Inspection	Frequency	Reference
•Die Shear Test	Each Lot	MIL-STD-883C, 2019-2
• Bond Strength Test	Each Lot	MIL-STD-883C, 2011-4
• Solderability Test	Weekly	MIL-STD-883C, 2003-3
• Mark Permanency Test	1 Time/Equipment/Day	MIL-STD-883C, 2015-4
• Lead Integrity Test	Weekly	MIL-STD-883C, 2004-4
• In-Process Monitor Inspection for Product	4 Times/Shift/Each Process	Identify for Each Control Limit
• X-Ray Monitor Inspection for Molding	2 Times/Shift/Mold Press	Identify for Each Control Limit
• Monitor Inspection for Production Equipment	2 Times/Shift/Each Unit of Equipment	Identify for Each Control Limit
• Compound Thermal Analysis	3 Equipment/Shift/Day	Identify for Each Control Limit

4. Outgoing quality inspection plan (LTPD)

Defect Class	Discrete	LSI	Kind of Defect
Critical Defect electrical visual	1%	2%	Open, short Wrong configuration, no marking
Major Defect electrical visual	1.5%	3%	Items which affect reliability most strongly
Minor Defect electrical visual	2%	5%	Items which minimally or do not affect reliability at all (cosmetic, appearance, etc.)

Figure 10. General Assembly Flow

<table>
<tr><th>Process Flow</th><th>Process Step</th><th>Major Control Item</th></tr>
<tr><td rowspan="11">  </td><td>Wafer

Wafer Incoming Inspection</td><td>Q.C. Wafer Incoming Inspection AQL 4.0%</td></tr>
<tr><td>Tape Mount</td><td></td></tr>
<tr><td>Sawing Q.C. Monitor</td><td>Q.C. Monitoring:
— Chip-out — Scratch
— Crack — Sawing Discoloration
— Sawing-speed — Cut Count
— D.I. Purity — CO_2 Bubble Purity</td></tr>
<tr><td>Visual Inspection</td><td>100% Screen:
— FAB Defect
— EDS Test Defect
— Sawing & Scratch Defect</td></tr>
<tr><td>Q.C. Gate</td><td>1st AQL 1.0%
Reinspection AQL: 0.65%</td></tr>
<tr><td>Lead Frame (L/F)</td><td></td></tr>
<tr><td>Lead Frame Incoming</td><td>*Q.C.L/F Incoming Inspection
1. Acceptance Quality Level
— Dimension LTPD 20%, C = 0
— Visual & Mechanical: LTPD 10%, C = 2
— Functional Work Test: LTPD 20%, C = 0</td></tr>
<tr><td>Die Attach (D/A)</td><td></td></tr>
<tr><td>Q.C. Monitor</td><td>*Q.C.D/A Monitor Inspection
1. Bond force
2. Frequency: 4 Times/Station/Shift
3. Sample: 24 ea Time
4. Acceptance Criteria
<table><tr><th>Defect</th><th>Acceptance</th><th>Reject</th></tr><tr><td>Critical</td><td>0</td><td>1</td></tr><tr><td>Major</td><td>1</td><td>2</td></tr></table></td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
<tr><td>Cure</td><td></td></tr>
</table>

Figure 10. General Assembly Flow (Continued)

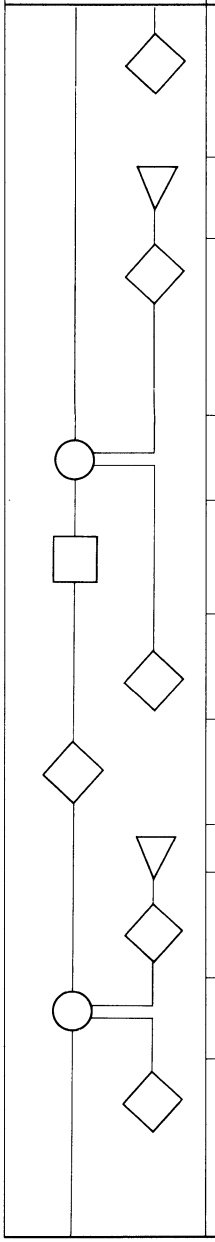
Process Flow	Process Step	Major Control Item
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/out Time 2. Frequency — 1 Time/Shift
	Au Wire	
	Bonding Wire Incoming Inspection	*Q.C Au Wire Incoming Inspection 1. Visual Inspection: N = 5, C = 0 2. Bond Pull Test Strength Test: N = 13, C = 0 3. Bondability Test — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Wire Bonding (W/B)	
	100% Visual Inspection	
	Q.C. Monitor	*Q.C. W/B Monitor Inspection 1. Frequency: 4 Times/Mach/Shift
	Q.C. Gate	1. Q.C. Acceptance Quality Level — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold Compound	
	Incoming Inspection Mold	*Moldability Test — Critical Defect: AQL 0.15% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold	
	Q.C. Monitor	*Q.C. Mold Monitor Inspection 1. In-Process Monitor Inspection — Frequncy: 4 Times/Station/Shift — Sample: 200 Units/Time 2. Acceptance Quality Level — Critical Defect: AQL 0.25% — Major Defect: AQL 0.4%

Figure 10. General Assembly Flow (Continued)

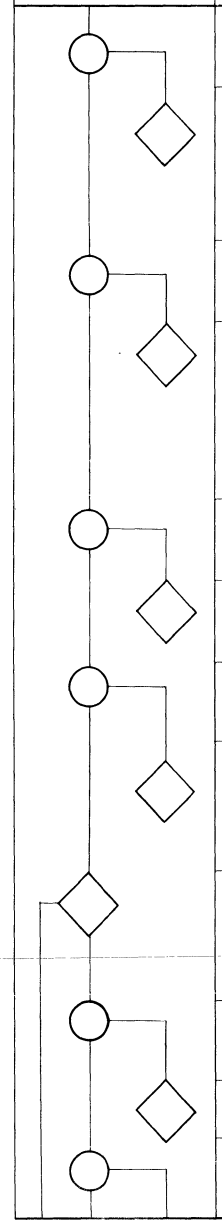
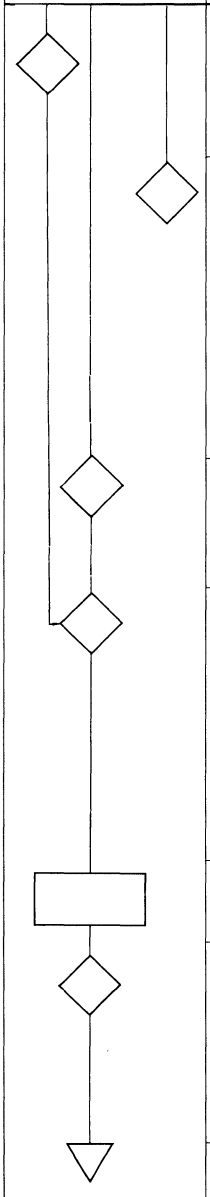
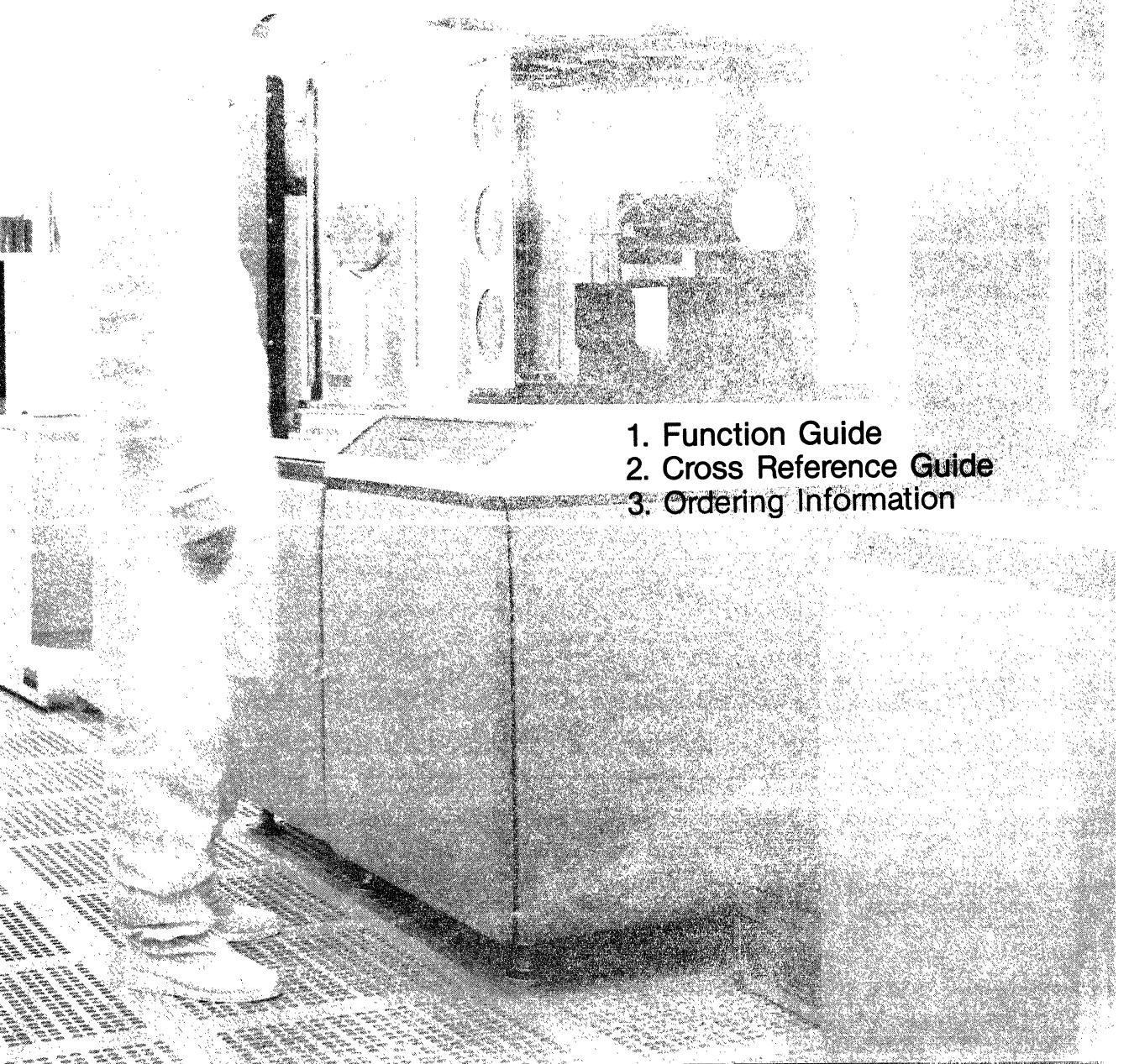
Process Flow	Process Step	Major Control Item
	Cure	
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/out Time 2. Frequency — 1 Time/shift
	Deflash	
	Q.C. Monitor	*Q.C. Deflash Monitor Inspection 1. Control Item — Pressure — Belt Speed — Visual/Mechanical Inspection 2. Frequency: 4 Times/Mach/Shift 3. Identify each Defect Control Limit
	TRIM/BEND	
	Q.C. Monitor	*Q.C. Trim/Bend Monitor Inspection 1. Visual Inspection 2. Frequency: 4 Times/Station/Shift
	Solder	100% Visual Inspection
	Q.C. Monitor	*Q.C. Solder Monitor Inspection 1. Frequency: 4 Times/Mach/Shift 2. Criteria — Critical Defect: AQL 0.25% — Major Defect: AQL 0.4%
	Q.C. Gate	*Q.C. Mold Gate — Acceptance Criteria Critical Defect: AQL 0.10% Major Defect: AQL 0.4% Minor Defect: AQL 0.65%
	Test	100% Electrical Test
	Q.C. Monitor	Correlation Sample Reading for Initial Device Test
	Mark	100% Visual Inspection

Figure 10. General Assembly Flow (Continued)

Process Flow	Process Step	Major Control Item
	PRT Monitoring (Product Reliability Monitor)	1. PRT — HOPL, PCT — Other (when applicable) 2. Acceptance Criteria: LTPD 10%
	Q.C. Monitor	*Q.C. Marking Monitor Inspection — Frequency: 4 Times/Station/Shift — Sample: 24 Units/Time — Identify for Each C.L. — Acceptance Criteria Defect / Acceptance / Reject: Critical 0 / 1; Major 1 / 2
	Q.C. Gate	*Q.C. Final Acceptance Level — Critical Defectg: AQL 0.10% — Major Defect: AQL 0.4% — Minor Defect: AQL 0.65%
	Q.A. Gate	*Q.A. Incoming Inspection 1. Critical Defect: — Electrical Test: LTPD 2% (N = 116, C = 0) — Visual Test: LTPD 2% (N = 116, C = 0) 2. Major Defect: — Electrical Test: LTPD 3% (N = 116, C = 1) — Visual Test: LTPD 3% (N = 116, C = 1) 3. Minor Defect: — Electrical Test: LTPD 5% (N = 116, C = 2) — Visual Test: LTPD 5% (N = 116, C = 2)
	Stock	*Age Control
	Q.A. Gate	*Q.A. Outgoing Inspection 1. Quantity 2. Customer 3. Packing 4. Sampling Inspection (when applicable) — Sampling plan is same as incoming Inspection
	Shipment	

NOTES



1. Function Guide
2. Cross Reference Guide
3. Ordering Information

1. FUNCTION GUIDE

A. CMOS LCD Watch ICs

Device	Display					Function				Additional Features					Electrical Characteristic			Remark
	Digit	Day Flags	Marks	Duplexed LCD	Triplexed LCD	Basic 5 Function	Day Type	Year	Alarm	Snooze	Chronograph	Chime	Timer		V_{DD} (V)	I_{DD} (μA) Typ.	I_{DD} (μA) Max.	
KS5112	6	—	1	—	*	*	—	—	—	—	—	—	—		1.5	0.8	1.5	Internal Capacitor
KS5198	3.5	—	—	*	—	*	—	—	—	—	—	—	—		1.5	0.8	1.5	
KS5199A	3.5	—	—	*	—	*	—	—	—	—	—	—	—		1.5	0.8	1.5	
KS5184	6	7	4	*	—	*	Flag	—	*	*	—	*	—		1.5	1.0	2.0	
KS5190	6	7	4	*	—	*	Flag	—	*	*	*	*	—	Chrono (1/100 sec, 24HR)	1.5	1.0	2.0	
KS5194	4	—	4	*	—	*	—	—	*	—	—	*	—		1.5	1.0	2.0	
†KS5114	3.5	—	—	*	—	*	—	—	—	—	—	—	—		1.5	0.8	1.5	Internal Capacitor

B. CMOS Analog LCD Watch

Device	Display			Function	Electrical Characteristic			Remark
	Hand	Segment	LCD duty		V_{DD} (V)	I_{DD} (μA) Typ	I_{DD} (μA) Max	
KS5113	3	120	1/6	3	1.5	1.5	2.5	Internal Capacitor

C. CMOS Analog Watch

Device	Function	Electrical Characteristic				Remark
		V_{DD} (V)	I_{DD} (nA) Typ	I_{DD} (nA) Max	Osc. (Hz)	
†KS5243	3 Hand Analog Watch	1.5	170	300	32768	External Trimmer Capacitor

D. CMOS Analog Clock ICs

Device	Feature	Electrical Characteristic				Package	Remark
		V_{DD} (V)	I_{DD} (μA) Typ	I_{DD} (μA) Max	Osc. (Hz)		
KS5206	A: 0.5Hz Square Wave Pulse Output E: 0.5Hz 46.9ms Duration Pulse Output F: 0.5Hz 31.2ms Duration Pulse Output	1.5	1.5	2.5	32,768	8 DIP or Chip	2048Hz Alarm
KS5207		1.5	1.5	2.5	32,768	8 DIP or Chip	1 HR Function
KS5209		1.5	1.0	2.0	32,768	8 DIP or Chip	2048Hz Alarm
KS5210		1.5	0.7	2.0	32,768	8 DIP or Chip	2048Hz Alarm
KS5211		1.5	0.7	2.0	32,768	8 DIP or Chip	No Trimmer

E. Calculator ICs

Device		Function	Additional Function	V_{DD}(V)	I_{DD} (μA)		Package	Remark
					Typ	Max		
Calculator	KS6025	Basic	Auto Power Off	1.5	6	9	48 FQP	Solar Cell
	KS6026	Basic	Auto Power Off	1.5	5.6	9	48 FQP	Solar Cell
	KS6027A	Desk Top	—	1.5	7.0	15	Bare Chip	Solar Cell
	†KS6027B	—	—	1.5	7.0	15	60 FQP	Solar Cell
	†KS6027C	Basic	—	3.0	7.0	15	60 FQP	—
	†KS6028	Basic	Auto Power Off	1.5	1.3	3	48 FQP	Solar Cell
	†KS6029	Basic	Auto Power Off	1.5	1.5	3	48 FQP	Solar Cell
	KS6041	Scientific	Auto Power Off	3.0	70	120	48 FQP	—

F. Voice Synthesizer ICs

Device	Synthesis Method	V_{DD}(V)	Maximum Memory	Package	Remark
KS5901A	LPC	5	64K Bytes	60 FQP	
KS5902	LPC	5	48K Bits	24 DIP	Internal ROM
KS5911	ADM	5	256K DRAM × 4	48 FQP	External DRAM
KS5912	ADM	5	64K Bits	16 DIP	Internal ROM
††KS5915	ADM	5	1M DRAM × 4	60 FQP	External DRAM

G. Melody ICs

Device		Title	Time Base (Hz)	V_{DD} (V)	I_{DD}(μA)	Package	Remark
KS5310 Series	KS5310A	Oh! Susanna	32,768	1.5		Bare Chip	1 Melody Bare Chip (At Watch)
KS5313 Series	KS5313N KS5313P KS5313R KS5313Q KS5313S KS5313T	Minuet (BACH) Cuckoo's Waltz Oh! Susanna Home Sweet Home Big Ben For Elise	33,000	1.5	Stand-By 0.1-0.3 Operating 20-30	KS5313: 16 DIP/ 8 DIP	KS5313 Speaker or Piezo Drive
KS5814	KS5814	Sky-Lark's or Cricket's Sound	210,000	1.5	Stand-By 0.1-0.3 Operating 250-400	14 DIP	Speaker
KS5401	††KS5401A	8 Sound effect	125,000	3	Stand-By 0.4-1.5 Operating 300-600	18 DIP	Speaker

H. Miscellaneous

Device	Function	V_{DD} (V)	I_{DD} (μA)		Package	Remark
			Typ	Max		
KS5815	3.5 Digits Clinical Thermometer	1.5	—	100	Bare Chip	
KS5116	6 Digit Up/Down Counter	1.5	9	18	Bare Chip	

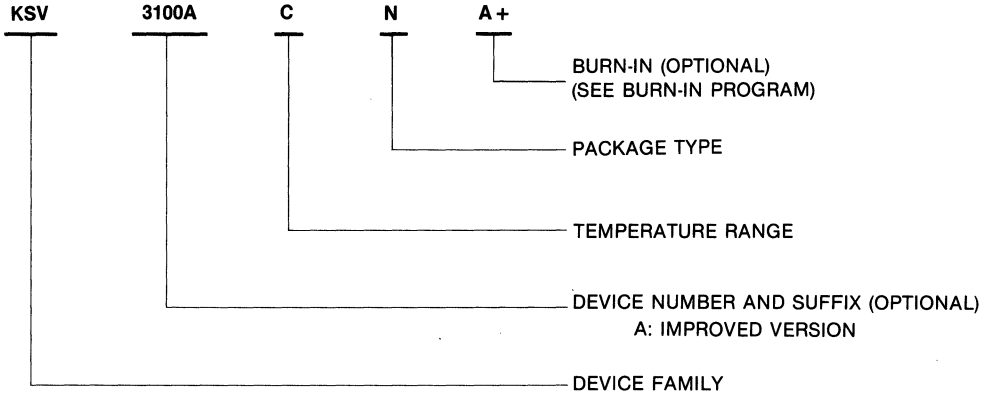
† New Product †† Under Develop

2. CROSS REFERENCE GUIDE

Application	SAMSUNG	OKI	SEIKO	TOSHIBA	Others
LCD Watch	KS5184				LC5641
	KS5198	MSM5001N			
	KS5199A	MSM5001N			
	KS5189	MSM5066			
	KS5190	MSM5066			
	KS5194	MSM5004			
	KS5112			JT6649A-CS	
	†KS5114	MSM5001N			
Analog LCD Watch	KS5113	MSM5008			e1331 STP55721
Analog Watch	†KS5243				e1208
Analog Clock	KS5205				
	KS5206				UM3262
	KS5209				
	KS5210				e1444
	KS5211				RCA92461
Melody	KS5310A		SVM7952		
	KS5313		SVM7920		CIC3821 CIC3822
	KS5814				MN6223
	††KS5401A				HT-88
Calculator	KS6025				LI3128
	KS6026				UM3135
	†KS6027A/B/C			T6899	
	†KS6028				
	†KS6029				LI3135
	KS6041			SC6992	
Voice Synthesizer	KS5901A			T6721	
	KS5902			T6803	SP0255, LC8100
	KS5911			T6668	UM5101
	KS5912			T6667	CIC560
	KS5915			TC8831F	CIC5500
Miscellaneous	KS5815			JT6690-AS	
	KS5116				

† New Product
†† Under Development

3. ORDERING INFORMATION



TEMPERATURE RANGE

BLANK	SEE INDIVIDUAL SPEC
C	COMMERCIAL 0 ~ +70°C
I	INDUSTRIAL −25 ~ +85°C −40 ~ +85°C
M	MILITARY −55 ~ +125°C

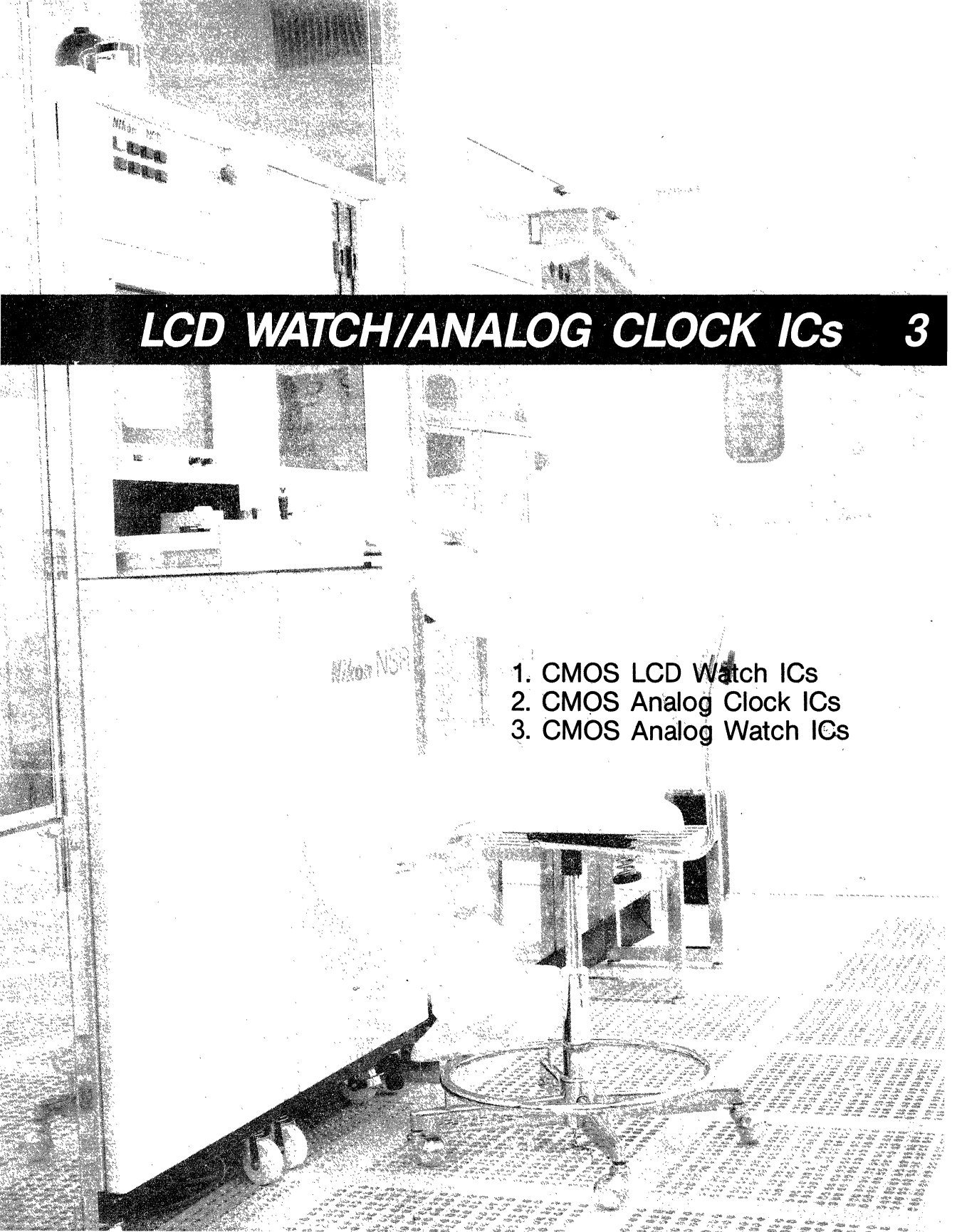
INTEGRATED CIRCUIT

KA	LINEAR IC
KS	CMOS IC
KT	TELECOM IC
LM	NATIONAL
MC	MOTOROLA
NE	SIGNETICS
KSV	A/D-D/A CONVERTER
KAD	A/D CONVERTER
KDA	D/A CONVERTER

PACKAGE TYPE

CODE	PKG. TYPE
D	SOIC
J	CERAMIC DIP
N	PLASTIC DIP (300/600 mil)
S	SIP
Q	FQP
E	SD (400 mil)
B	SSD (Skinny Shrink DIP) (400 mil. Small Pitch)
P	SHD (Shrink DIP) (300 mil. Small Pitch)
W	ZIP
U	PGA
L	LCC
PL	PLCC
M	TO-3
H	TO-3P
Z	TO-92
V	TO-92L
A	TO-126
T	TO-220
X	TO-247
G	BARE CHIP

LCD WATCH/ANALOG CLOCK ICs 3



1. CMOS LCD Watch ICs
2. CMOS Analog Clock ICs
3. CMOS Analog Watch ICs

CMOS LCD Watch ICs

Device	Function	Package	Page
KS5112	5 Functions 6 Digits Watch for Triplexed LCD	Bare Chip	49
KS5113	3 Hands LCD Analog Watch	Bare Chip	56
KS5114	5 Functions 3.5 Digits Watch for Duplexed LCD	Bare Chip	64
KS5184	6 Functions 6 Digits Alarm Watch with Chime for Duplexed LCD	Bare Chip	70
KS5190	6 Functions 6 Digits Alarm Watch with Chronograph and Chime for Duplexed LCD	Bare Chip	74
KS5194	5 Functions 4 Digits Alarm Watch with Chime for Duplexed LCD	Bare Chip	80
KS5199A	5 Functions 3.5 Digits Watch for Duplexed LCD	Bare Chip	84

CMOS Analog Clock ICs

Device	Function	Package	Page
KS5206	Bipolar Stepping Motor Drive Analog Clock	8 DIP or Chip	90
KS5207	Bipolar Stepping Motor Drive Analog Clock	8 DIP or Chip	95
KS5209	Bipolar Stepping Motor Drive Analog Clock	8 DIP or Chip	100
KS5210	Bipolar Stepping Motor Drive Analog Clock	8 DIP or Chip	104
KS5211	Bipolar Stepping Motor Drive Analog Clock	8 DIP or Chip	109

CMOS Analog Watch IC

Device	Function	Package	Page
KS5243	3 Hands Analog Watch	Bare Chip	113

5-FUNCTION 6-DIGIT WATCH CIRCUIT FOR TRIPLEXED LCD.

The KS5112 is a CMOS LSI which contains all logic necessary to implement of a five function six digits liquid crystal display watch. The circuit contains an oscillator amplifier with an internal feedback resistor for the use of 32,768Hz quartz crystals. The circuit operates from a single 1.5 volt battery and contains internal voltage doubler. Only 2 switches are required to control all functions. These switch inputs have pull down resistor and be debounced by internal circuitry.

FUNCTIONS

- 5 functions: Month, Date, Hour, Minute and Second
- 12 hour format.
- Selectable display Hour, Minute, Second / Month, Date.
- One touch correction of time error within ±30 seconds.
- 2 switch sequential operation.
- 4 year calendar.
- LCD test

FEATURES

- **One chip C-MOS construction.**
- **Drives 6 digits triplexed LCD.**
- **Colon and PM display.**
- **Low power consumption.**
- **32,768Hz crystal oscillator.**
- **Single 1.5V battery operation.**
- **Built-in voltage doubler circuit.**
- **Built-in crystal oscillator input capacitor.**
- **Trimmer capacitor included**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage ($V_{DD1} - V_{SS}$)	V_{DS1}	−0.3 ~ +2.0	V
Supply Voltage ($V_{DD2} - V_{SS}$)	V_{DS2}	−0.3 ~ +4.0	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

* Voltage greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 1.5V$, $V_{SS} = 0V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}		1.2	1.5	1.8	V
	V_{DD2}		2.4	3.0	3.6	V
Supply Current	I_{DD}	Without Load		0.8	1.5	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	0.5	3	μA
Oscillator Start Voltage	V_{OSC}	Within 5 Sec			1.45	V
Oscillator Stop Voltage	V_{OSP}				1.15	V
Oscillator Frequency	F_{OSC}			32,768		Hz
DC-DC Conversion Frequency	F_{CON}	$C1 = C2 = 0.1\mu F$		1,024		Hz
LCD Frequency	F_d			43		Hz
Oscillator Capacitor	C_{in}			20		pF
	C_{out}			20		pF
Switch Debouncing Time	T_{deb}				31.25	mSEC

FUNCTIONAL DESCRIPTION

Two switchs (D and S) are required to control all display and setting of function.

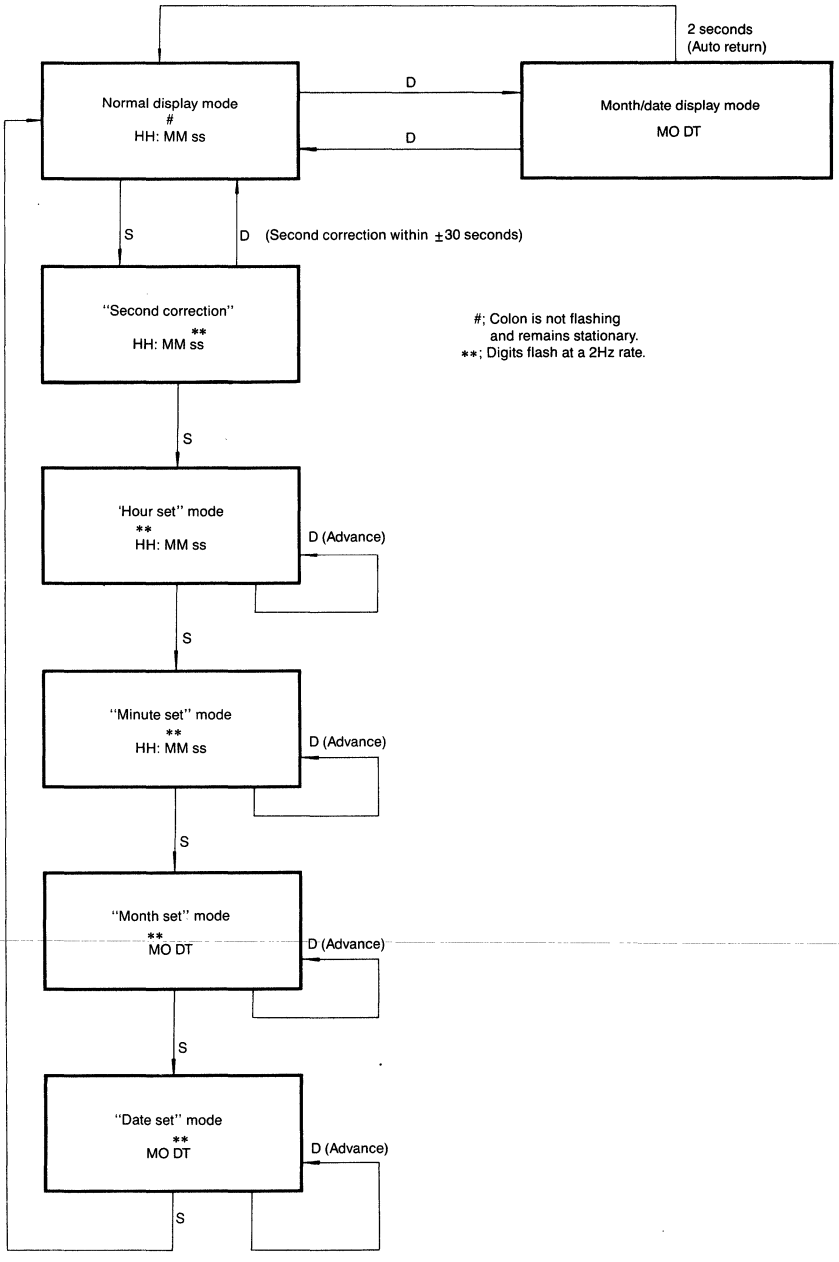
A) Display Control

Hours, minutes and seconds are displayed, colon remains stationary in normal mode.
Month and date are displayed by depressing D-switch.
If D-switch is not depressed continuously, the display will return to normal mode (Hours, minutes and seconds) after 2 seconds.

B) Setting Control

1. Second
   Depressing S-switch in normal mode will cause second correction mode. Second display will flash at a 2Hz rate in this mode. D-switch is used to correct second within ±30 seconds. After seconds correction, the display will return to normal mode (Hours, minutes and seconds).
2. Hour
   Depressing S-switch in second correction mode will cause "Hour set" mode and hour display will flash at a 2Hz rate. D-switch is used to advance contents of selected state. If D-switch is depressed continuously, contents will be advanced at a 4Hz rate.
3. Minute
   The next depressing of S-switch will select "Minute set" mode and minute display will flash at a 2Hz rate. Minute can be advanced as above.
4. Month
   The next depressing of S-switch will select "Month set" mode and month display will flash at a 2Hz rate.
5. Date
   The next depressing of S-switch will select "Date set" mode and date display will flash at a 2Hz rate.
6. Return
   The next depressing of S-switch will return to normal display mode.

OPERATIONAL DIAGRAM



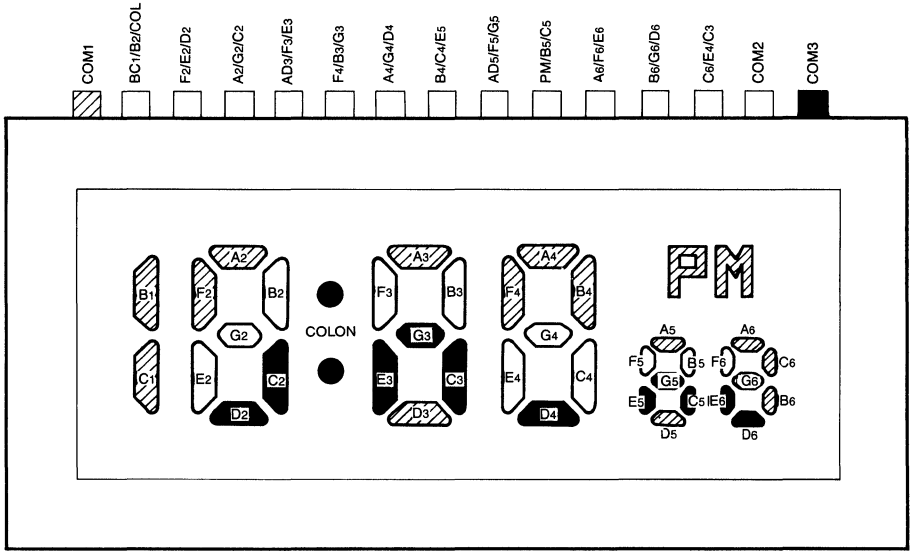
APPLICATION

- The voltage doubler circuit is formed by connecting 0.05μF to 0.1μF capacitor from 'CAP' PAD to '1KO' PAD and from 'VDD2' PAD to 'VSS' PAD.
- Oscillator circuit is formed by connecting crystal from 'OI' PAD to 'OO' PAD.
- The circuit substrate is electrically connected to V_{SS}, the most negative voltage. The preferred assembly method is to connect die area to V_{SS} using a conductive die attach.
- The watch can operate with 1.5V silver oxide battery and user should connect 'VDD' PAD to 1.5V, VSS to 0V.

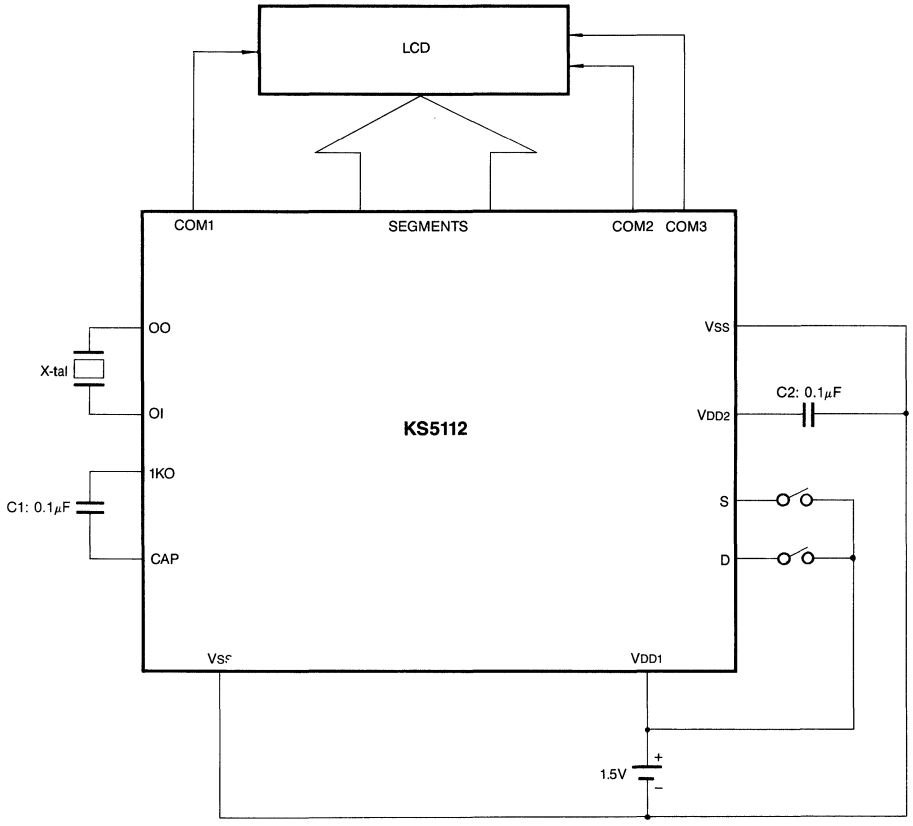
TESTING

- T1, T2 and T3 PAD are provided for testing. In normal operation they should be kept open.
- Three test inputs and two switches are pulled down by internal resistors.

LCD FORMAT

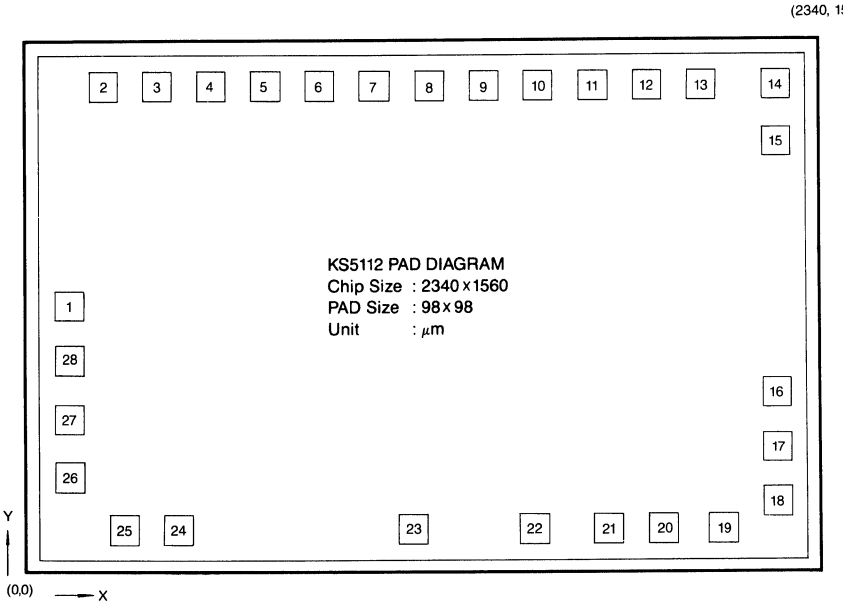


APPLICATION CIRCUIT



* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 10pF
C1 = 4pF
Co = 2.5pF
Rs = 35KΩ
Q = 35,000

PAD DIAGRAM



COORDINATES OF PAD

(Unit: μm)

Pad No.	Name of Pad	Coordinates	
		X	Y
1	COM1	129	789
2	$BC_1/B_2/COL$	230	1431
3	$F_2/E_2/D_2$	390	1431
4	$A_2/G_2/C_2$	550	1431
5	$AD_3/F_3/E_3$	710	1431
6	$F_4/B_3/G_3$	870	1431
7	$A_4/G_4/D_4$	1030	1431
8	$B_4/C_4/E_5$	1190	1431
9	$AD_5/F_5/G_5$	1350	1431
10	$PM/B_5/C_5$	1510	1431
11	$A_6/F_6/E_6$	1670	1431
12	$B_6/G_6/D_6$	1830	1431
13	$C_6/E_4/C_3$	1990	1431
14	COM2	2211	1431

Pad No.	Name of Pad	Coordinates	
		X	Y
15	COM3	2211	1261
16	V_{SS}	2211	526
17	V_{DD2}	2211	366
18	S	2211	206
19	D	2501	129
20	V_{DD1}	1874	129
21	T3	1711	129
22	T2	1494	129
23	T1	1137	129
24	V_{SS}	449	129
25	CAP	289	129
26	1KO	129	285
27	OI	129	457
28	OO	129	629

3 HAND LCD ANALOG WATCH

The KS5113 is a silicon-gate CMOS LSI for 3-HAND analog LCD display watch. It provides three functions (HOUR, MINUTE, SECOND).

It connects the analog LCD panel with 120 segments type.

The KS5113 has 20 segment outputs and 6 common outputs for direct drive of 1/6 duty multiplexing LCD.

It operates on single 1.5V battery and the circuit time base is a 32,768Hz crystal oscillator.

FUNCTIONS

- 3 Function: HOUR, MINUTE, SECOND.
- Time setting: Minute up setting.
- 1 switch operation.

FEATURES

- **One chip CMOS construction.**
- **1/6 duty multiplex LCD drive.**
- **Single 1.5V battery operation.**
- **Voltage doubler, voltage tripler.**
- **Lower power consumption.**
- **32,768Hz Crystal frequency.**
- **Built-in voltage doubler, voltage tripler circuits.**
- **Trimmer capacitor included.**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage ($V_{DD1} - V_{SS}$)	V_{DS1}	−0.3 ~ +2.0	V
Supply Voltage ($V_{DD2} - V_{SS}$)	V_{DS2}	−0.3 ~ +4.0	V
Supply Voltage ($V_{DD3} - V_{SS}$)	V_{DS3}	−0.3 ~ +6.0	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

* Voltage greater than above may damage the circuit

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 1.5V$, $V_{SS} = 0V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}		1.2	1.5	1.8	V
	V_{DD2}		2.4	3.0	3.6	V
	V_{DD3}		3.6	4.5	5.4	V
Supply Current	I_{DD}	Without Load		1.5	2.5	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	0.5	3	μA
Oscillator Start Voltage	V_{OSC}	Within 5 Sec			1.45	V
Oscillator Stop Voltage	V_{OSP}				1.15	V
Oscillator Frequency	F_{OSC}			32,768		Hz
DC-DC Conversion Frequency	F_{CON}	C12 = CD2 = CD3 = 0.1μF		1,024		Hz
LCD Frequency	F_d			43		Hz
Oscillator Capacitor	C_{in}			20		pF
	C_{out}			20		pF
Switch Debouncing Time	T_{deb}				31.25	mSEC

FUNCTIONAL DESCRIPTION

1. Voltage Tripler

The battery voltage (1.5V) can be doubled and tripled by connecting external capacitor CD2, CD3 and C12 to the on-chip voltage doubler and tripler as shown in Fig. 1.

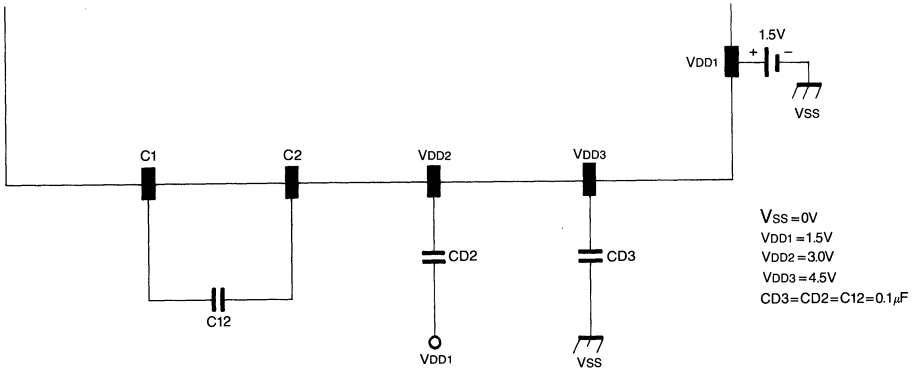
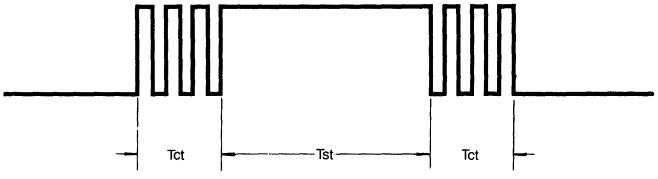


Fig. 1. Voltage Tripler

2. Chattering Prevention

The on chip chatter killer network provided for switch prevent possible error caused by chatter as shown in Fig. 2.



Tct ≤ 33.3 msec (maxmum switch chattering time.)

Tst ≤ 60 msec (minimum stable time)

Fig. 2. Chattering

3. Initial Set

Initial state is shown in Fig. 3.

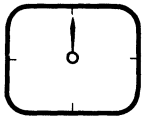
Initial State	Time	Display
Base Watch Mode	(AM) 00:00 00	

Fig. 3.

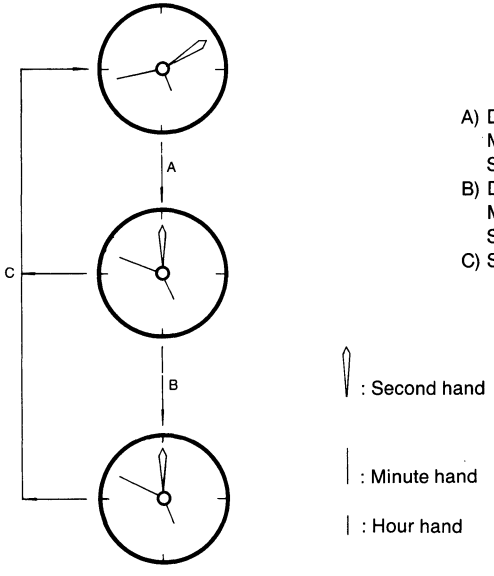
TEST FUNCTIONS

T1	T2	T3	AC	SW	Function
0	0	0	0	—	Normal
Clock	—	—	0	—	Test 256Hz drive
—	Clock	—	0	—	Test 8Hz drive
Clock	0	1	0	Clock	Minute display & TEST
Clock	1	1	0	Clock	Hour display & TEST
—	—	0	1	—	Initial SET
—	—	1	1	—	LAMP TEST

Switch Operation

1) Normal mode.
The normal mode will be displayed with three HANDS (HOUR, MINUTE, SECOND). Second is advanced at 1Hz rate, minute is advanced at 60 second rate, and hour is advanced at 6, 18, 30, 42, 54 minute.

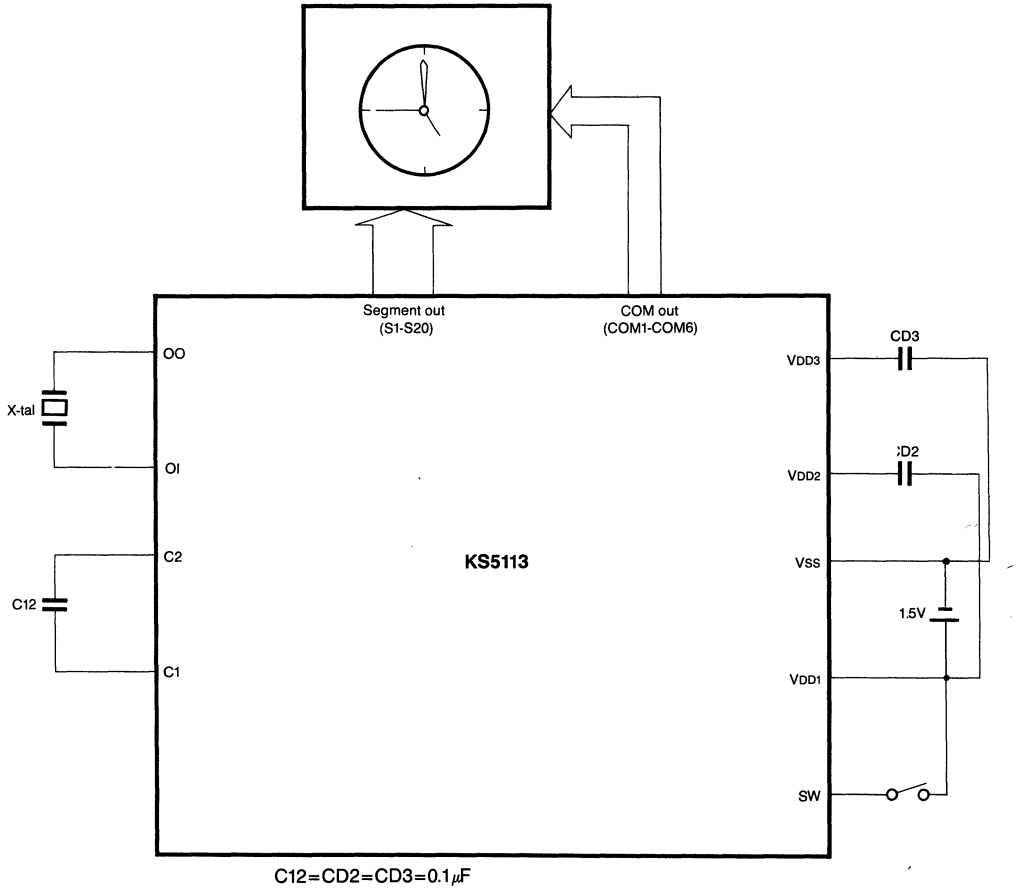
2) Time setting.
When switch SW is depressed less than 1 second, the minute HAND advances + 1 step with the second HAND returning to "O".
If switch SW is depressed over 1-2 second, the minute HAND advances at 8Hz rate with the second HAND remaining "O" and the hour HAND advances according to the minute HAND.



A) Depressing switch SW less than 1 second.
Minute HAND will be advanced + 1.
Second HAND will be returned to "O".
B) Depressing switch SW over 1-2 second.
Minute HAND will be advanced at 8Hz rate.
Second HAND stays "O".
C) Switch SW released.

Fig. 4. Switch operation.

APPLICATION CIRCUIT



C12=CD2=CD3=0.1μF

Fig. 5. Application Circuit

Quartz Crystal Parameter
Fp = 32,768Hz
CL = 10pF
C1 = 4pF
Co = 2.0pF
Rs = 35KΩ
Q = 35,000

LCD FORMAT

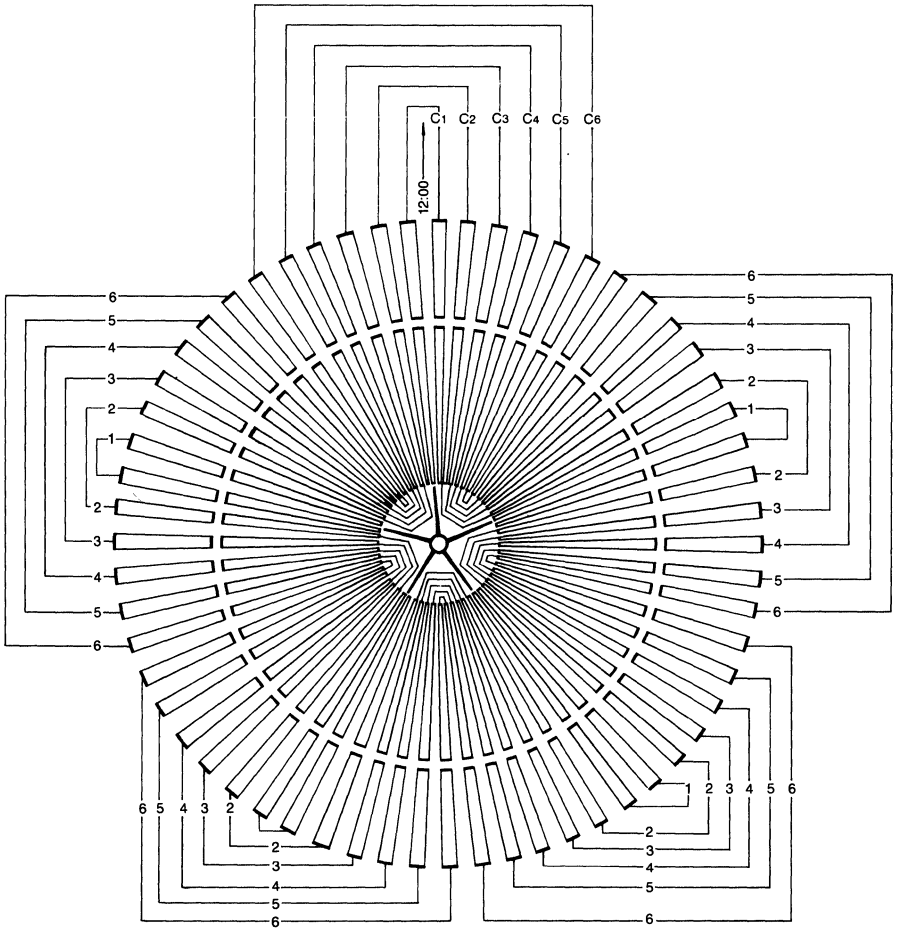


Fig. 6. COMMON SIDE

LCD FORMAT (Continued)

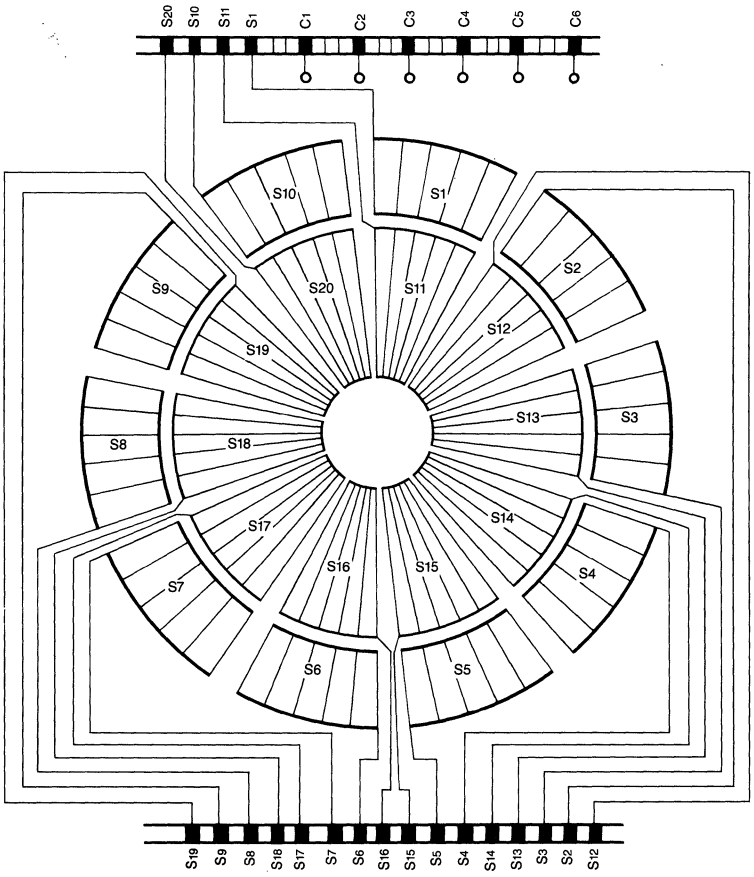
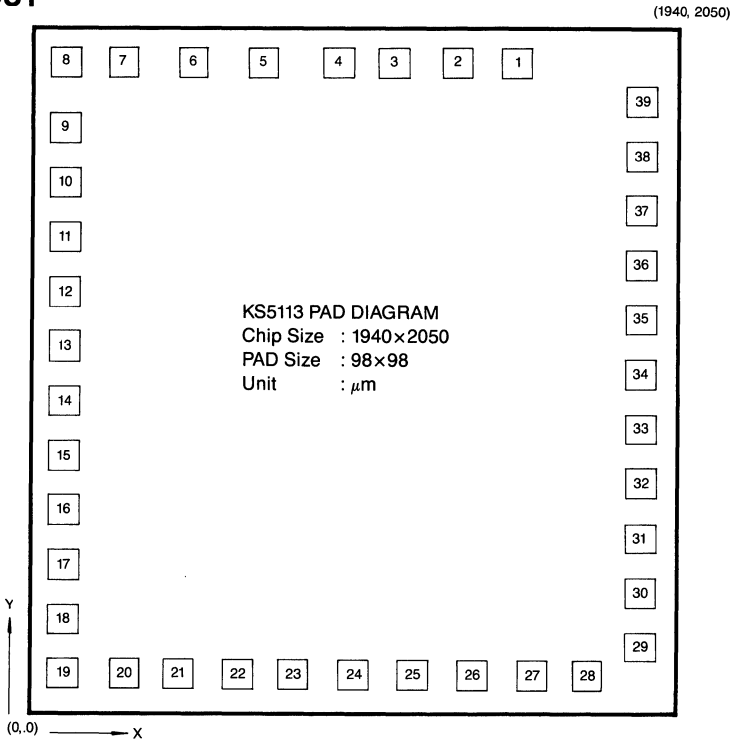


Fig. 7. SEGMENT SIDE

PAD LAYOUT



KS5113 PAD LOCATION

(Unit: μm)

Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y
1	OO	1447	1921	11	S6	129	1409	21	SW	466	129	31	COM5	1811	540
2	OI	1273	1921	12	S16	129	1249	22	V_{DD1}	639	129	32	COM4	1811	700
3	C2	1090	1921	13	S15	129	1089	23	AC	799	129	33	COM3	1811	860
4	C1	930	1921	14	S5	129	929	24	T1	972	129	34	COM2	1811	1020
5	S19	710	1921	15	S4	129	769	25	T2	1145	129	35	COM1	1811	1180
6	S9	504	1921	16	S14	129	609	26	T3	1318	129	36	S1	1811	1340
7	S8	298	1921	17	S13	129	449	27	V_{SS}	1491	129	37	S11	1811	1500
8	S18	129	1921	18	S3	129	289	28	V_{DD2}	1651	129	38	S10	1811	1660
9	S17	129	1729	19	S2	129	129	29	V_{DD3}	1811	220	39	S20	1811	1820
10	S7	129	1569	20	S12	306	129	30	COM6	1811	380	—	—	—	—

FUNCTIONS 3.5 DIGITS WATCH CIRCUIT FOR DUPLEXED LCD.

The KS5114 is low threshold voltage, ion implanted metal gate CMOS integrated circuit which provides all signals to drive a duplexed 3.5 digits liquid crystal display with colon (Fig. 1).
32.768Hz frequency from crystal controlled oscillator is divided to provide SECOND, MINUTE, HOUR, DATE and MONTH information. Phase controlled segment outputs and two Phase controlled back plane outputs are provided for direct drive of the duplexed LCD.
The KS5114 contains inverter/amplifier, output attenuating resistor, capacitor and feed back resistor to drive the crystal.
The frequency of oscillator is divided to provide 512Hz output pulse used as signal for the voltage doubler.

FUNCTIONS

- 5 functions: Month, Date, Hour, Minute and Second.
- Selective alternation of TIME-DATE display mode.
- One touch correction of time error within ±30 seconds.
- 4 years calendar.
- 2 switches sequential operating.
- LCD test.

FEATURES

- **Single chip CMOS construction.**
- **Drives 3.5 digits duplexed LCD.**
- **Low power dissipation (I_{DD}: Typ. 0.8μA, Max. 1.5μA ;1.55V operation).**
- **Colon display.**
- **32.768Hz crystal controlled operation.**
- **Single 1.5V battery operation.**
- **On-chip capacitive voltage doubler.**
- **Debounce circuitly on switch inputs.**
- **Protection against static discharge.**
- **Built-in crystal oscillator π-network input capacitor.**
- **Trimmer capacitor is user selectable. (bonding option)**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_{DS}	−0.3 ~ +2.0	V
Supply Voltage ($V_{DD} - V_{EE}$)	V_{DE}	−0.3 ~ +4.0	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

* Voltage greater than above in damage the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 0V$, $V_{SS} = -1.5V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS}\|$		1.2	1.5	1.8	V
	$\|V_{EE}\|$		2.4	3.0	3.6	V
Supply Current	I_{DD}	Without Load		0.8	1.5	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	0.5	3	μA
Oscillator Start Voltage	$\|V_{OSC}\|$	Within 5 Sec			1.45	V
Oscillator Stop Voltage	$\|V_{OSP}\|$				1.15	V
Oscillator Frequency	F_{OSC}			32,768		Hz
DC-DC Conversion Frequency	F_{CON}	C1 = C2 = 0.1μF		512		Hz
LCD Frequency	F_d			32		Hz
Oscillator Capacitor	C_{in}			25		pF
	C_{out}			25		pF
Time Stability	T_{stb}	$\triangle V_{DD} = 0.5V$ ($C_{out} = 25pF$)			1	ppm
Switch Debouncing Time	T_{deb}				62.5	mSEC

FUNCTIONAL DESCRIPTION

DISPLAY CONTROL

• Standard Display

Normal KS5114 displays HOUR in digit 1, 2 and MINUTE in digit 3 and 4. In this state colon flashes at 1Hz rate.

Depression of D switch on normal display state will cause MONTH to be displayed in digit 1 and 2, DATE in digit 3 and 4 with colon off. MONTH and DATE will continue to be displayed for 2 secnds after the D switch is released. Then HOUR and MINUTE are displayed again.

Two momentary depressions of D switch within 2 seconds on normal display state will cause SECOND to be displayed in digit 3, 4 and the digit 1 and 2 blanked with colon non-flashing continuously. Depressing S in this state resets and holds the SECOND counter until switch S is released and MINUTE counter is either advanced or remained unchanged depending upon whether the SECOND counter is greater or less than 30 seconds.

Depressing D in this state returns the display to HR : MIN display state.

• Alternating display

This mode is selected by activating the set switch (S) in normal display mode. In this mode HR : MIN is automatically displayed alternately with MONTH DATE. Each is displayed for two seconds.

The S input must be activated five times to return to normal display mode and depressing D switch in this alternating mode will cause the SECOND display mode.

3.5 DIGITS LCD FORMAT

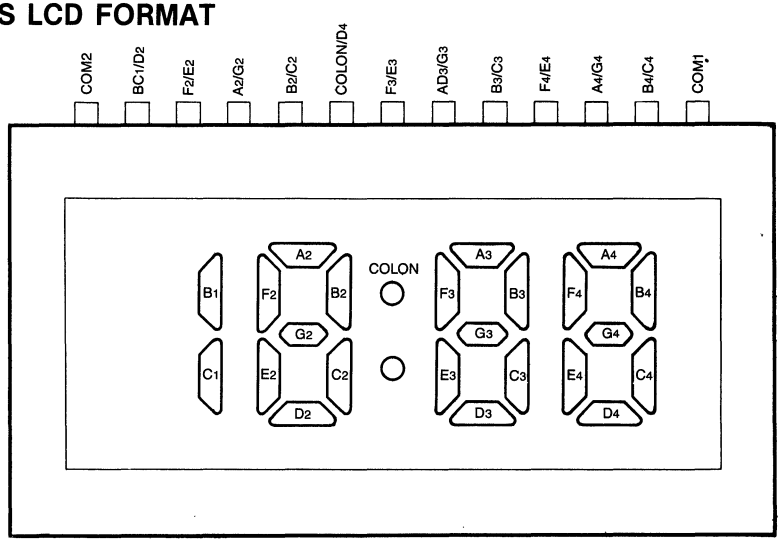


Fig. 1

SETTING PROCEDURE (fig. 2)

Time/calendar setting is accomplished by using S switch to enter and return from setting state. The D switch is used to advance the function at 2Hz rate.

The function to be set is displayed the only one while setting state.

The detailed setting procedure is as follows.

a. Alternating display state

Depressing S switch in normal display state causes the alternating display mode. (Alternating HR : MIN and MONTH DATE)

b. Month

Depressing S switch in normal display state calls MONTH set state and the display shows MONTH in digit 1 and 2. The MONTH counter can be advanced at 2Hz rate by depressing D switch.

c. Date

The next depressin of S switch will select DATE set state and the display shows DATE in digit 3 and 4. The DATE can be advanced as fig. 2.

d. Hour

The next depression of S switch will select HOUR set state and the display shows HOUR in digit 1 and 2 and A (AM)/P (PM) in digit 4.

The colon flashes at 1Hz rate. The HOUR can be advanced as fig. 2.

e. Minute

The next depression of S switch will select MINUTE set state and the display shows MINUTE in digit 3 and 4 and the colon flashes at 1Hz rate. Depressing D switch advance the MINUTE at 2Hz flashing and the watch suspends time-keeping.

f. Hold mode

Then watch enters the HOLD state with the next depression of S switch. In this state the display shows HOUR in digit 1 and 2, MINUTE in digit 3 and 4 and non-flashing colon. (Normal display state)

NOTE

If MINUTE were not changed in MINUTE set state, the watch will not enter the HOLD state but will automatically revert to normal display state.
The carry signal from any preceeding counter during operation is not accepted except for second reset.

SETTING AND DISPLAY SEQUENCE

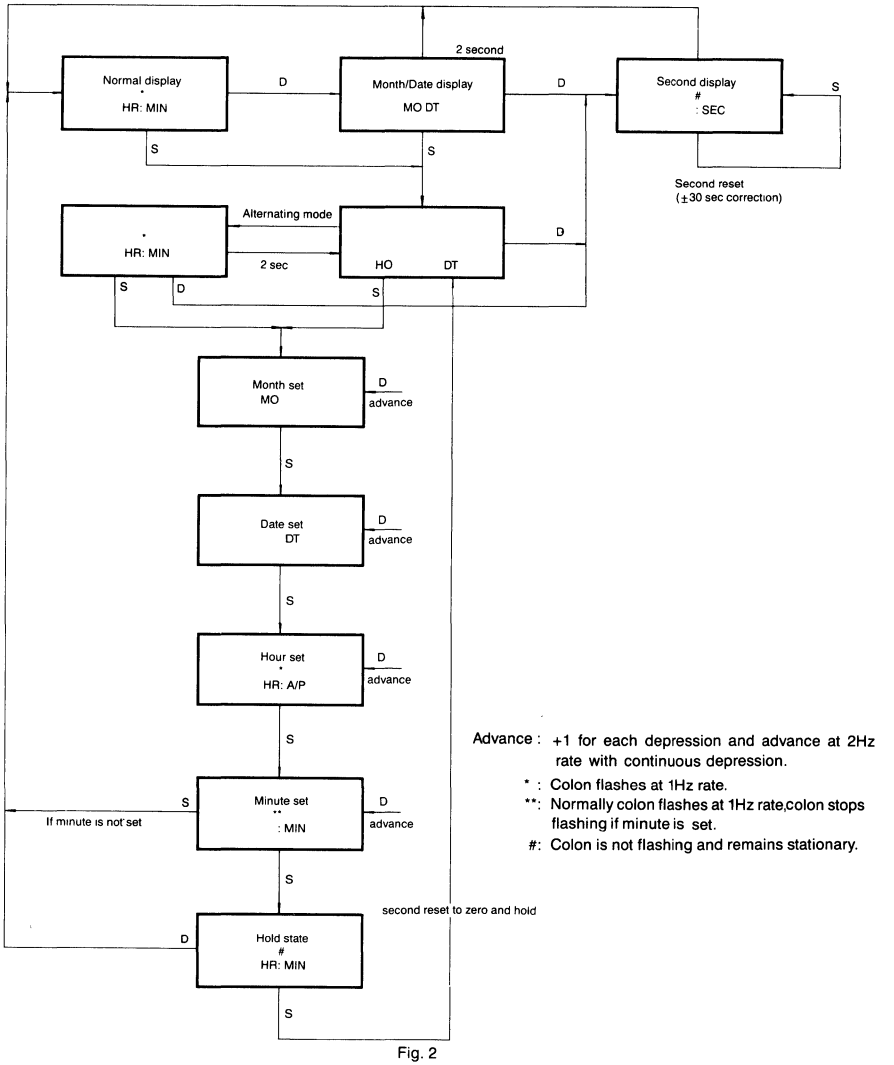
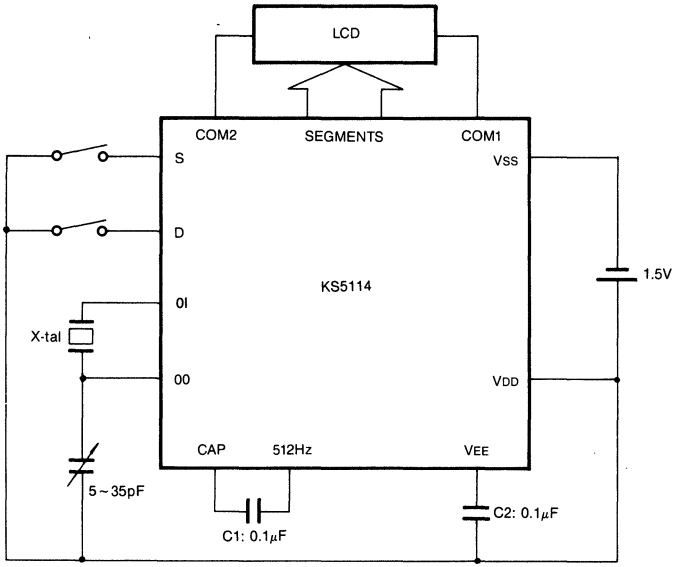


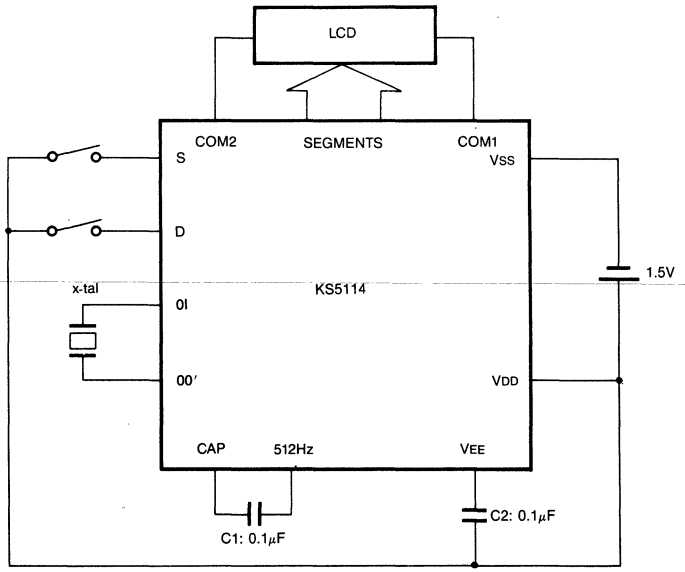
Fig. 2

APPLICATION CIRCUIT

1) External Trimmer Capacitor Type

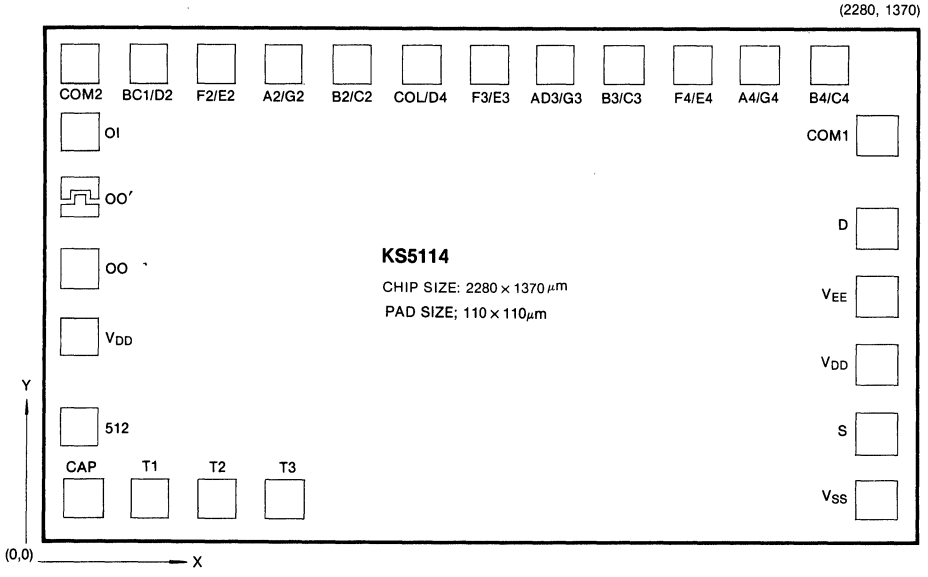


2) Internal Trimmer Capacitor Type



* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 12.5pF
C1 = 4pF
Co = 2.5pF
Rs = 35KΩ
Q = 35,000

PAD DIAGRAM



KS5114 PAD LOCATION

Unit: μm

Pad Name	Coordinates		Pad Name	Coordinates		Pad Name	Coordinates	
	X	Y		X	Y		X	Y
COM2	135	1235	F4/E4	1735	1235	T3	785	135
BC1/D2	315	1235	A4/G4	1935	1235	T2	505	135
F2/E2	495	1235	B4/C4	2115	1235	T1	325	135
A2/G2	675	1235	COM1	2145	1045	CAP	135	135
B2/C2	855	1235	D	2145	865	512	135	315
COL/D4	1035	1235	V_{EE}	2145	685	V_{DD}	135	510
F3/E3	1215	1235	V_{DD}	2145	505	OO'	135	690
AD3/G3	1395	1235	S	2145	325	OO	135	860
B3/C3	1575	1235	V_{SS}	2145	145	OI	135	1050

6 FUNCTION 6 DIGIT ALARM WATCH WITH CHIME FOR DUPLEXED LCD

The KS5184 is a CMOS 6 function watch circuit with alarm function and Chime, which is designed for with 6 Digit duplexed liquid crystal display with 7 day mark, date mark, alarm mark, AM/PM mark and colon.

FUNCTIONS

- 6 Function: Month, Date, Day-of-week, Hour, Minute, Second
- Alarm, Snooze
- Alarm output for melody IC (KS5310 Series)
- User selectable 12 hour/24 hour format
- 4 year calendar
- One touch correction of time error within ±30 seconds.
- Chime on every hour
- 3 Switch sequential operation
- LCD test

FEATURES

- **Single chip CMOS construction**
- **Drives 6 digit duplexed LCD with 7 day mark, AM/PM mark, date mark and alarm mark**
- **Colon display**
- **Direct drive of piezoelectric transducer at 3 volt peak to peak**
- **Fast advance for time and alarm set**
- **32,768Hz crystal frequency**
- **On-chip oscillator and resistors**
- **On-chip voltage doubler**
- **Single 1.5V battery operation**
- **Low power dissipation**
- **Debounce circuitry on switch inputs**
- **Protection against static discharge**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (V_{DD}-V_{SS})	V_{DS}	−0.3 ~ +2.0	V
Supply Voltage (V_{DD}-V_E)	V_{DE}	−0.3 ~ +4.0	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temeprature	T_{stg}	−55 ~ +125	°C

* Voltage greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 0V$, $V_{SS} = -1.5V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS1}\|$		1.2	1.5	1.8	V
	$\|V_{EE1}\|$		2.4	3.0	3.6	V
Supply Current	I_{DD}	Without Load		1.0	2.0	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	0.5	3	μA
Oscillator Start Voltage	$\|V_{OSC}\|$	Within 5 Sec			1.45	V
Oscillator Stop Voltage	$\|V_{OSP}\|$				1.15	V
Alarm Drive Current	I_{ala}	$V_{sat} = 0.5V$ (Both Direction)	0.5	2.0		mA
	I_{alb}	$V_{sat} = 0.5V$	10	20		μA
Oscillator Frequency	F_{OSC}			32,768		Hz
DC-DC Conversion Frequency	F_{CON}	$C1 = C2 = 0.1\mu F$		2,048		Hz
LCD Frequency	F_d			32		Hz
Oscillator Input Capacitor	C_{in}			25		pF
Time Stability	T_{stb}	$\triangle V_{DD} = 0.5V$ ($C_{out} = 25pF$)			1	ppm
Switch Debouncing Time	T_{deb}				62.5	mSEC

LCD FORMAT

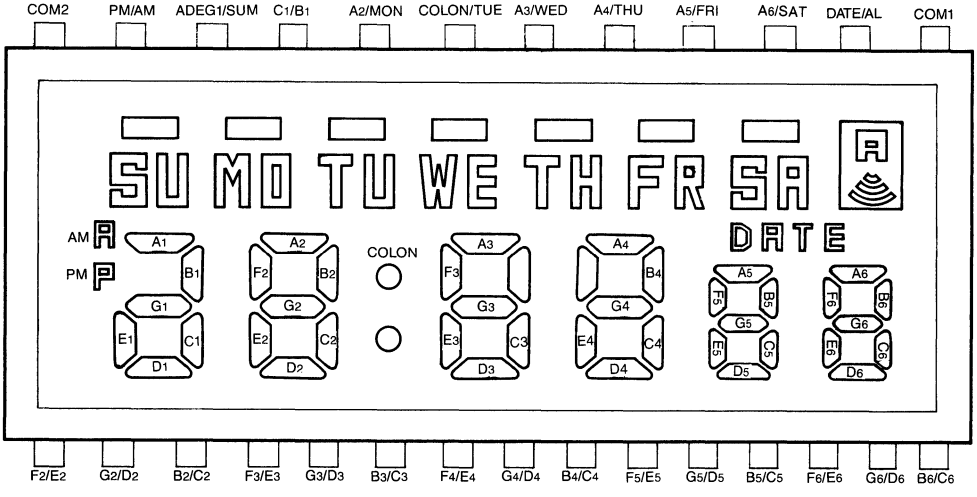


Fig. 1

SETTING SEQUENCE AND SWITCH OPERATION

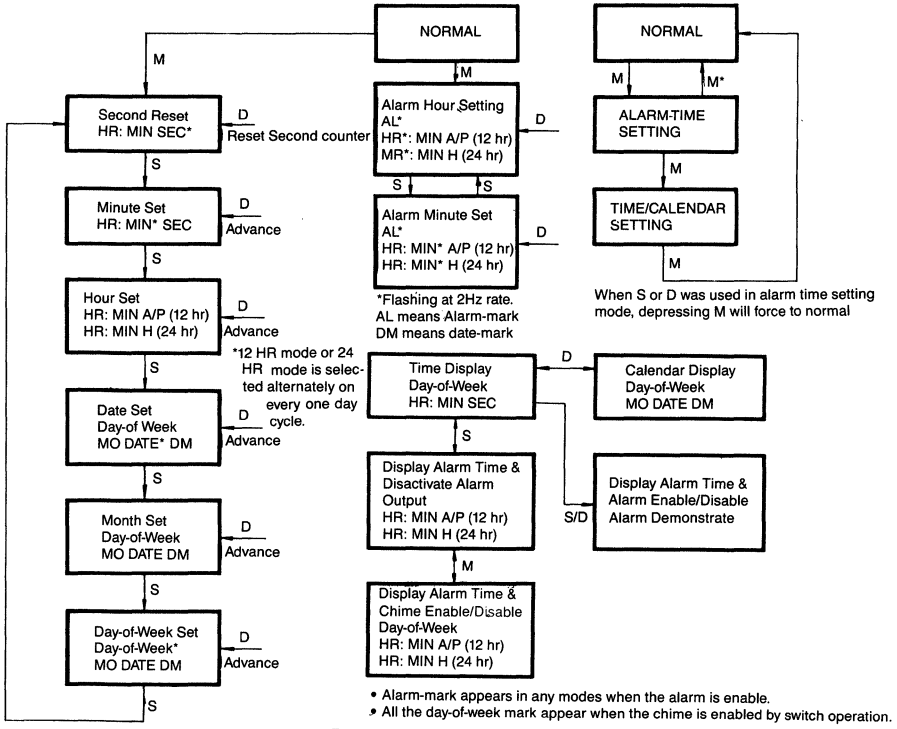


Fig. 2

ALARM OUTPUT WAVEFORMS

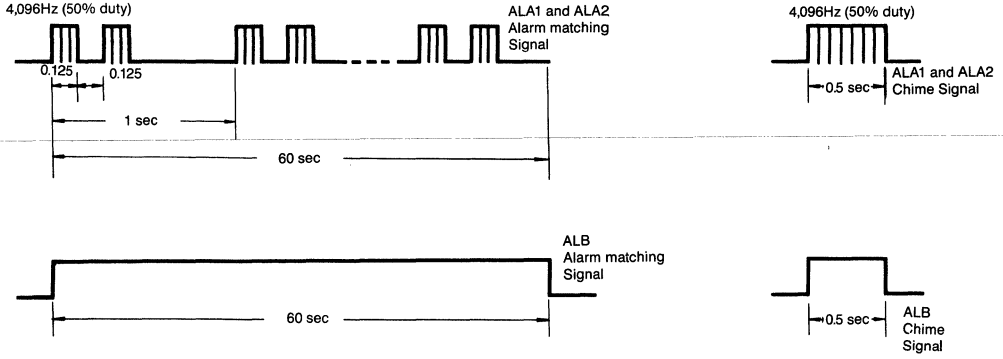
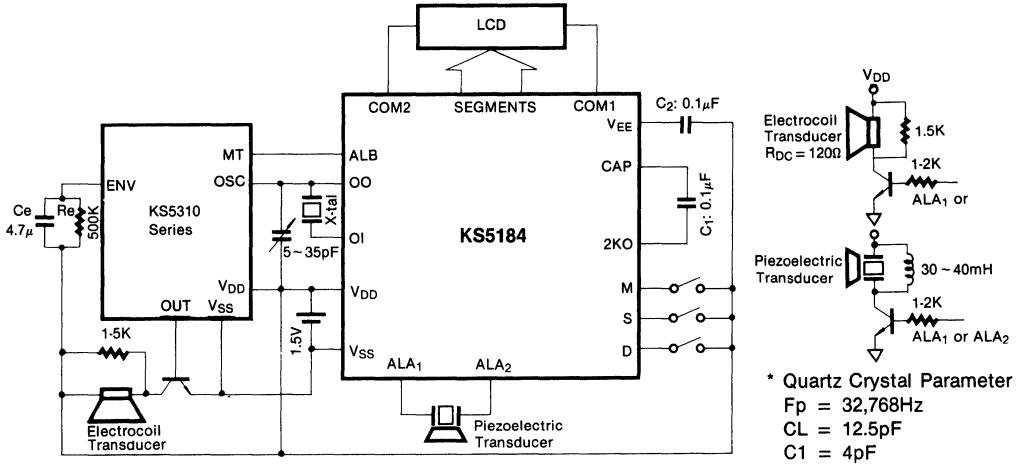


Fig. 3

APPLICATION CIRCUIT

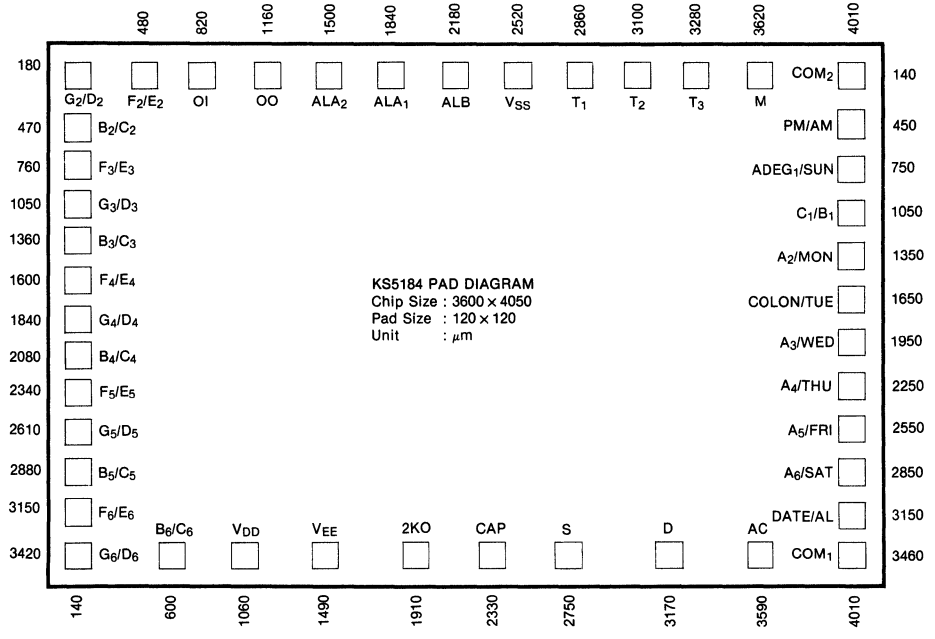


Re and Ce are necessary only when employing envelope circuit with KS5310 Series. Otherwise, ENV pad must be connected to V_{SS}.

* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 12.5pF
C1 = 4pF
CO = 2.5pF
Rs = 35KΩ
Q = 35,000

Fig. 4

PAD DIAGRAM



6 FUNCTION 6 DIGIT ALARM-CHRONOGRAPH DUPLEXED LCD WATCH CIRCUIT

The KS5190 is a CMOS 6 function watch circuit with alarm and autoranging chronograph function; designed to for a 6 digit duplexed liquid crystal display, 7 day mark, date mark, AM/PM mark, and colon.

FUNCTIONS

- 6 Function: Month, Date, Day-of-Week, Hour, Minute, Second
- Alarm function with 4 to 5 minute snooze
- 6 digit Chronograph: Autoranging after 30 minutes to hour, minute; second.
- Use selectable 12 hour/24 hour format
- Alarm output for melody IC (KS5310 Series)
- 4 year calendar
- One touch correction of time error within ±30 seconds.
- Fast advance for time and alarm time set
- Chime on every hour
- 3 Switch sequential operation
- LCD test

FEATURES

- **Single chip CMOS construction**
- **Drives 6 digit duplexed LCD with 7 day mark, AM/PM mark, date mark and alarm mark**
- **Colon display**
- **Direct drive of piezoelectric transducer at 3 volt peak to peak**
- **32,768Hz crystal frequency**
- **On-chip oscillator and resistors**
- **On-chip voltage doubler**
- **Single 1.5V battery operation**
- **Low power dissipation**
- **Debounce circuitry on switch inputs**
- **Protection against static discharge**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_{DS}	$-0.3 \sim +2.0$	V
Supply Voltage ($V_{DD} - V_{EE}$)	V_{DE}	$-0.3 \sim +4.0$	V
Operating Temperature	T_{opr}	$-20 \sim +75$	°C
Storage Temperature	T_{stg}	$-55 \sim +125$	°C

* Voltage greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 0V$, $V_{SS} = -1.5V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS}\|$		1.2	1.5	1.8	V
	$\|V_{EE}\|$		2.4	3.0	3.6	V
Supply Current	I_{DD}	Without Load		1.0	2.0	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	0.5	3	μA
Oscillator Start Voltage	$\|V_{OSC}\|$	Within 5 Sec			1.45	V
Oscillator Stop Voltage	$\|V_{OSP}\|$				1.15	V
Alarm Drive Current	I_{ala}	$V_{sat} = 0.5V$ (Both Direction)	0.5	2.0		mA
	I_{alb}	$V_{sat} = 0.5V$	10	20		μA
Oscillator Frequency	F_{OSC}			32,768		Hz
DC-DC Conversion Frequency	F_{CON}	$C1 = C2 = 0.1\mu F$		1,024		Hz
LCD Frequency	F_d			32		Hz
Oscillator Input Capacitor	C_{in}			25		pF
Time Stability	T_{stb}	$\triangle V_{DD} = 0.5V$ ($C_{out} = 25pF$)			1	ppm
Switch Debouncing Time	T_{deb}				31.25	mSEC

3

LCD FORMAT

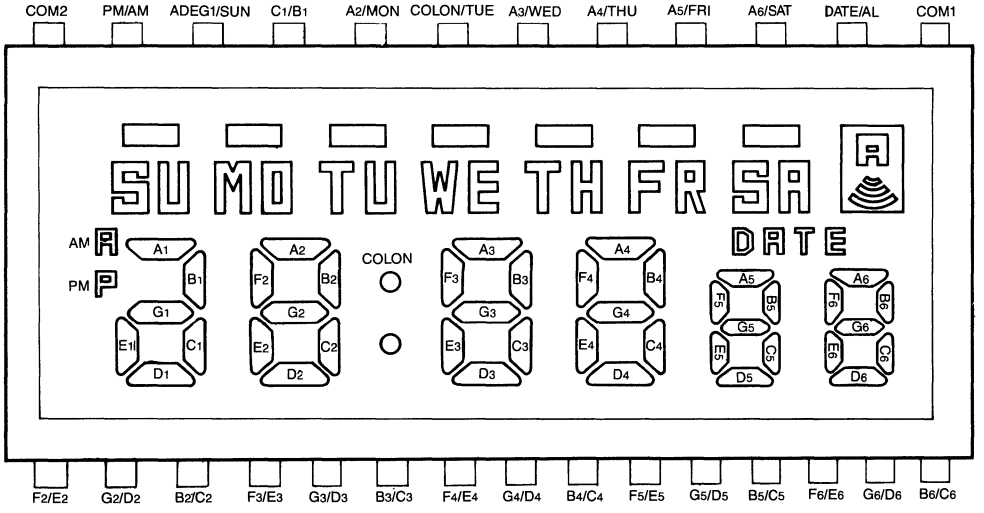


Fig. 1

ALARM OUTPUT WAVEFORMS

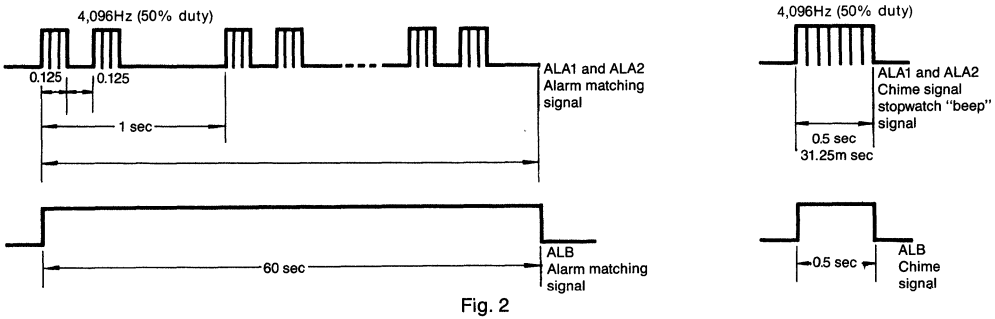


Fig. 2

APPLICATION CIRCUIT

1) Melody Drive Type

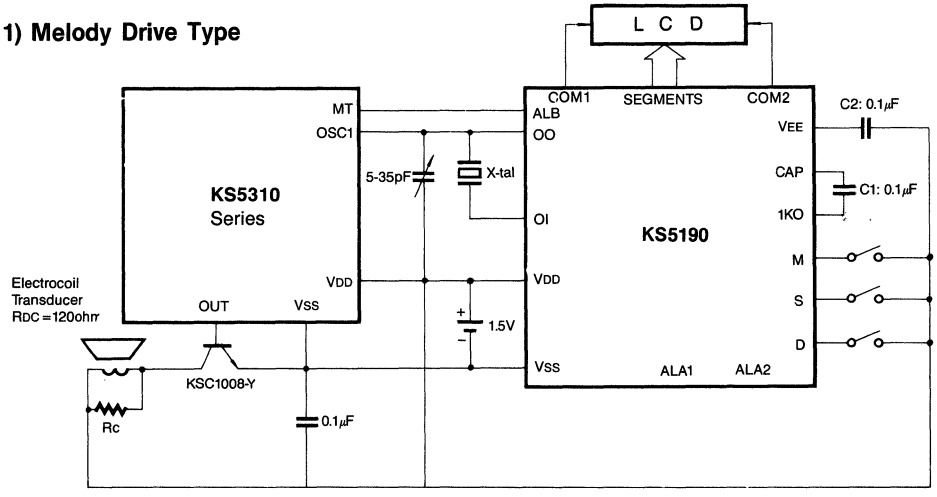


Fig. 3-1. Typical Application Circuit with Melody IC

2) Piezo Drive Type

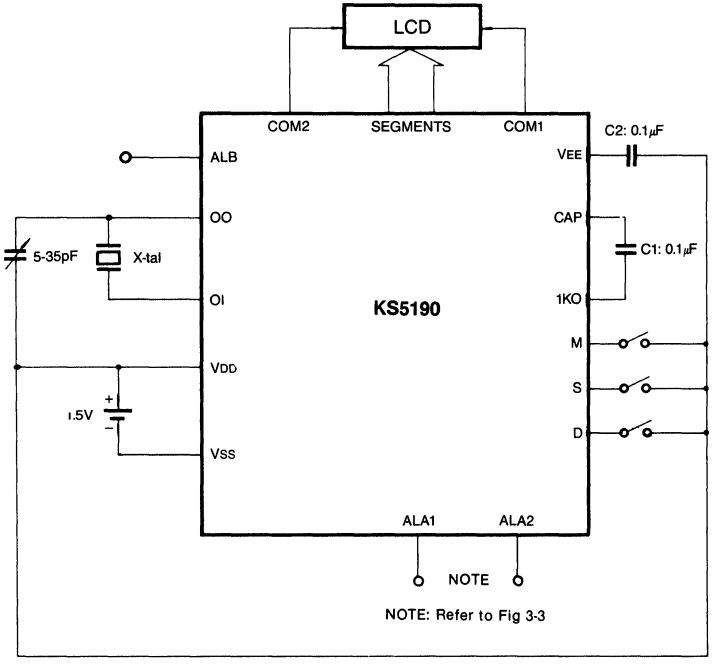
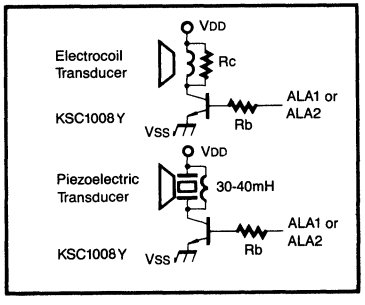


Fig. 3-2. Typical Application Circuit

* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 12.5pF
C1 = 4pF
CO = 2.5pF
Rs = 35KΩ
Q = 35,000



Rb: 2-10 (Kohm)
Rc: 1-5 (Kohm)

Fig. 3-3. Piezo Drive Method

SETTING SEQUENCE AND SWITCH OPERATION

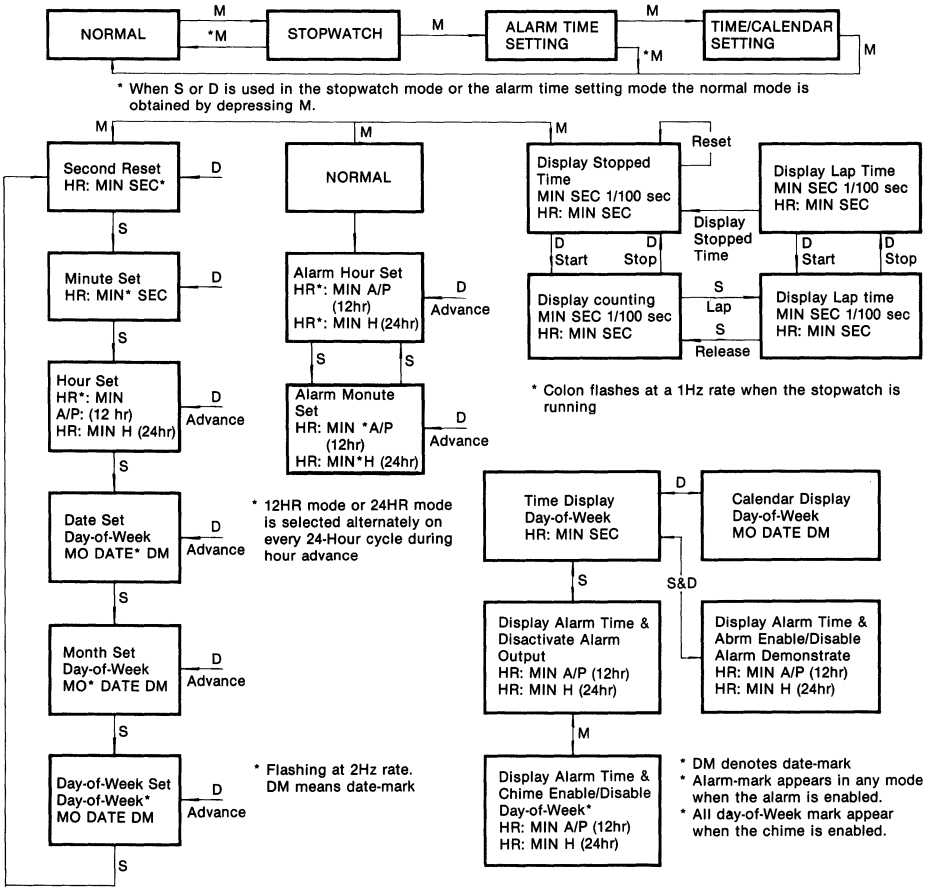
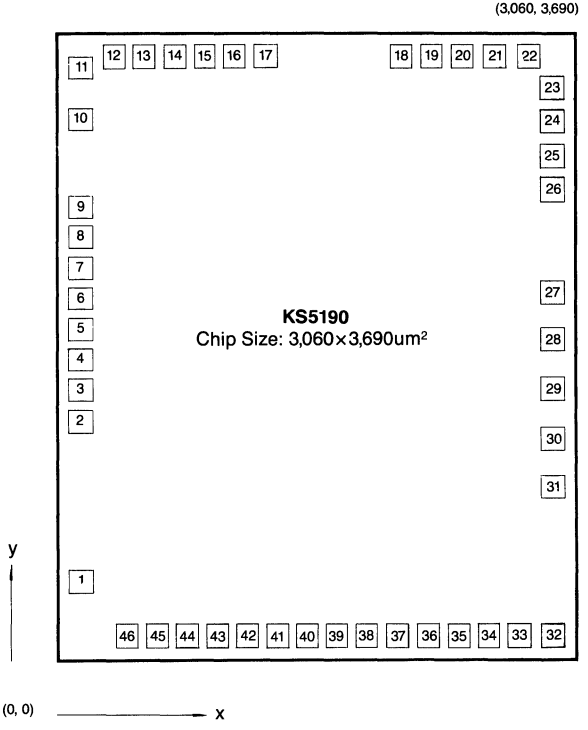


Fig. 4

PAD DIAGRAM



KS5190 PAD LOCATION

Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y	Pad No.	Pad Name	Coordinates X	Coordinates Y
1	OI	135	450	13	A1/SUN	513	3554	25	S	2924	2959	37	F5/E5	1993	134
2	OO	135	1411	14	C1/B1	693	3554	25	CAP	2324	2777	38	B4/C4	1818	134
3	ALA1	135	1600	15	A2/MON	873	3554	27	1KO	2924	2154	39	G4/D4	1538	134
4	ALA2	135	1730	16	CL/TUE	1053	3554	28	V_{EE}	2924	1879	40	F4/E4	1458	134
5	ALB	125	1960	17	A3/WED	1233	3554	29	T2	2924	1591	41	B3/C3	1273	134
6	V_{EE}	135	2140	18	A4/THU	2052	3554	30	T1	2924	1294	42	G3/D3	1098	134
7	V_{SS}	135	2320	19	A5/FRI	2232	3554	31	V_{DD}	2924	1008	43	F3/E3	918	134
8	V_{DD}	135	2500	20	A6/SAT	2412	3554	32	B6/C6	2398	134	44	B2/C2	738	134
9	AC	135	2680	21	DTE/AL	2592	3554	33	C6/D6	2718	134	45	G2/G2	553	134
10	M	135	3202	22	COM1	2739	3554	34	F6/E6	2538	134	46	F2/E2	378	134
11	COM2	135	3507	23	T3	2024	3364	35	B5/C5	2353	134	—	—	—	—
12	PM/AM	333	3554	24	D	2024	3184	35	G5/D5	2173	134	—	—	—	—

5 FUNCTION 4 DIGIT WATCH CIRCUIT WITH ALARM AND CHIME FOR DUPLEXED LCD

The KS5194 is a low threshold voltage, ion implanted metal gate CMOS integrated circuit that provides signals to drive 4 digit duplexed liquid crystal display with colon, PM/AL-TIME mark and AL/CH mark.

FUNCTIONS

- 5 Function: Month, Date, Hour, Minute, Second
- 30 second alarm sound
- Chime on every hour
- User selectable 12 hour/24 hour format
- 4 year calendar
- One touch correction of time error within ±30 seconds.
- Alarm, Chime enable/disable operation
- 2 Switch sequential operation
- LCD test.

FEATURES

- **Single chip CMOS construction**
- **Drives 4 digit duplexed LCD with PM/AL-TIME, alarm mark and chime mark**
- **Colon display**
- **Direct drive of piezoelectric transducer**
- **Low power dissipation**
- **32,768Hz crystal frequency**
- **On-chip oscillator, capacitor and resistors**
- **On-chip voltage doubler**
- **Single 1.5V battery operation**
- **Debounce circuitry on switch inputs**
- **Protection against static discharge**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_{DS}	−0.3 ~ +2.0	V
Supply Voltage ($V_{DD} - V_{EE}$)	V_{DE}	−0.3 ~ +4.0	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

* Voltage greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 0V$, $V_{SS} = -1.5V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS}\|$		1.2	1.5	1.8	V
	$\|V_{EE}\|$		2.4	3.0	3.6	V
Supply Current	I_{DD}	Without Load		1.0	2.0	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	0.5	3	μA
Oscillator Start Voltage	$\|V_{OSC}\|$	Within 5 Sec			1.45	V
Oscillator Stop Voltage	$\|V_{OSP}\|$				1.15	V
Alarm Drive Current	I_{ala}	$V_{sat} = 0.5V$ (Both Direction)	0.5	2.0		mA
Oscillator Frequency	F_{OSC}			32,768		Hz
DC-DC Conversion Frequency	F_{CON}	$C1 = C2 = 0.1\mu F$		1,024		Hz
LCD Frequency	F_d			32		Hz
Oscillator Input Capacitor	C_{in}			10		pF
Time Stability	T_{stb}	$\triangle V_{DD} = 0.5V$ ($C_{out} = 25pF$)			1	ppm
Switch Debouncing Time	T_{deb}				62.5	mSEC

LCD FORMAT

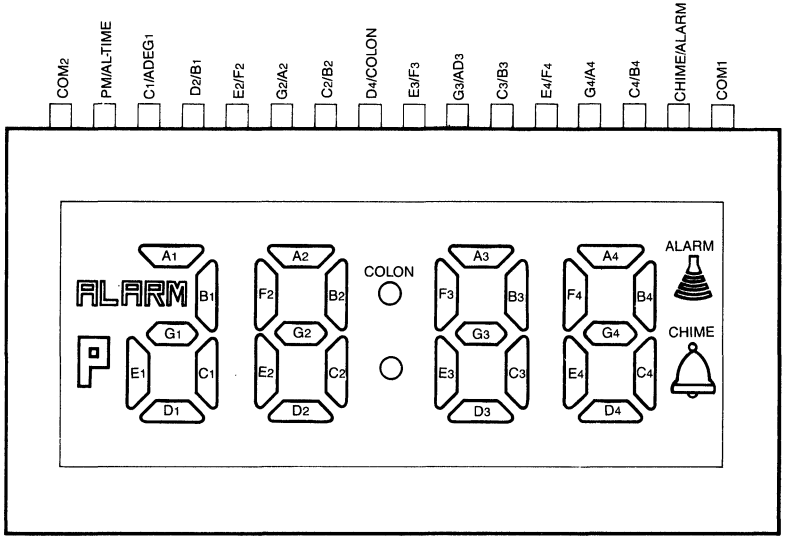
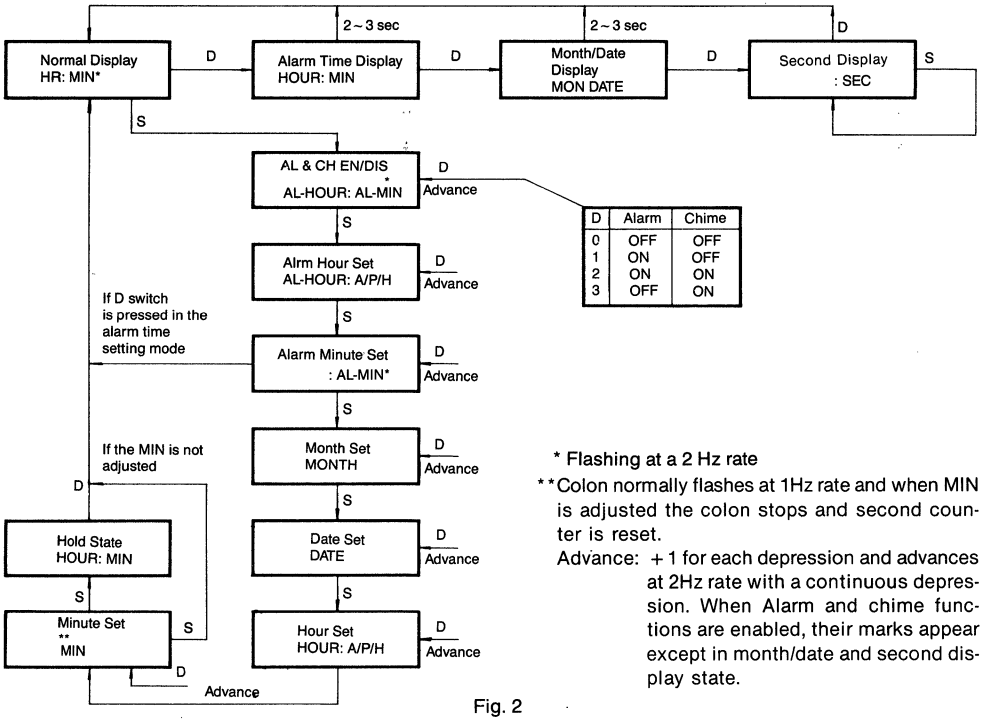


Fig. 1

SETTING SEQUENCE AND SWITCH OPERATION



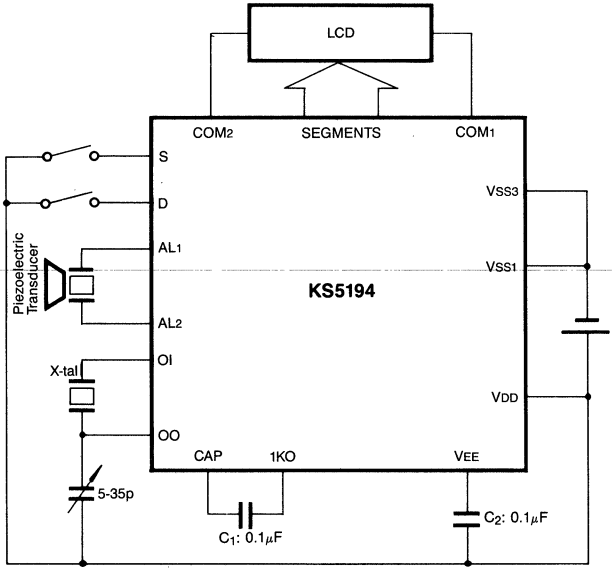
* Flashing at a 2 Hz rate

** Colon normally flashes at 1Hz rate and when MIN is adjusted the colon stops and second counter is reset.

Advance: +1 for each depression and advances at 2Hz rate with a continuous depression. When Alarm and chime functions are enabled, their marks appear except in month/date and second display state.

Fig. 2

APPLICATION CIRCUIT



* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 12.5pF
C1 = 4pF
CO = 2.5pF
Rs = 35KΩ
Q = 35,000

Fig. 3

ALARM OUTPUT WAVEFORM

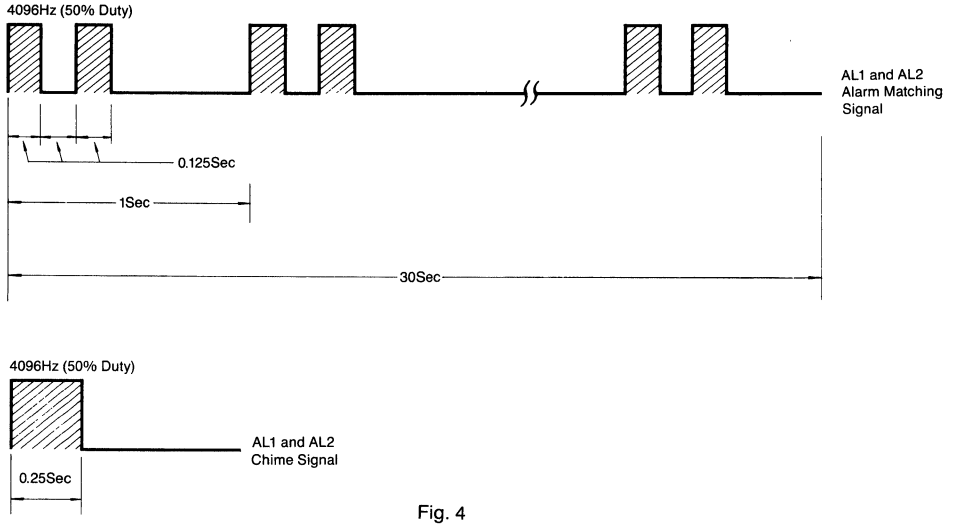


Fig. 4

PAD DIAGRAM

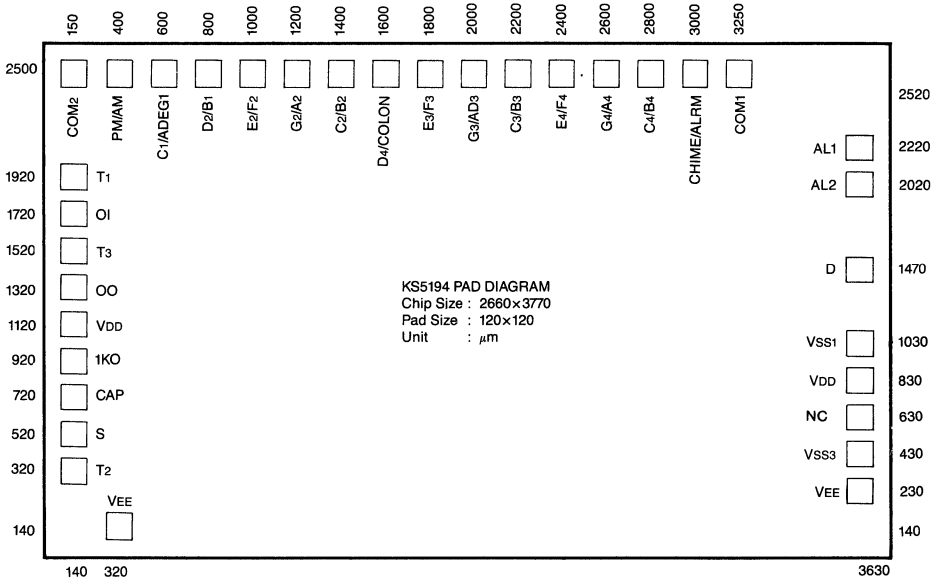


Fig. 5

FUNCTIONS 3.5 DIGITS WATCH CIRCUIT FOR DUPLEXED LCD.

The KS5199A is low threshold voltage, ion implanted metal gate CMOS integrated circuit which provides all signals to drive a duplexed 3.5 digits liquid crystal display with colon (Fig. 1).
32.768Hz frequency from crystal controlled oscillator is divided to provide SECOND, MINUTE, HOUR, DATE and MONTH information.
Phase controlled segment outputs and two Phase controlled back plane outputs are provided for direct drive of the duplexed LCD.
The KS5199A contains inverter/amplifier, output attenuating resistor, capacitor and feed back resistor to drive the crystal.
The frequency of oscillator is divided to provide 512Hz output pulse used as signal for the voltage doubler.

FUNCTIONS

- 5 Function: Month, Date, Hour, Minute and Second.
- Selective alternation of TIME-DATE display mode.
- One touch correction of time error within ±30 seconds.
- 4 year calendar
- 2 switches sequential operating
- LCD test

FEATURES

- **Single chip CMOS construction**
- **Drives 3.5 digits duplexed LCD**
- **Low power dissipation (I_{DD}: Typ. 0.8μA, Max, 1.5μA; 1.55V operation).**
- **Colon display**
- **32,768Hz crystal controlled operation**
- **Single 1.5V battery operation**
- **On-chip capacitive voltage doubler**
- **Debounce circuitly on switch inputs**
- **Protection against static discharge**
- **Built-in crystal oscillator π-network input capacitor**
- **Trimmer capacitor is user selectable (bonding option)**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_{DS}	−0.3 ~ +2.0	V
Supply Voltage ($V_{DD} - V_{EE}$)	V_{DE}	−0.3 ~ +4.0	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

* Voltage greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{SS} = -1.5V$, $V_{DD} = 0V$; unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS}\|$		1.2	1.5	1.7	V
Operating Voltage	$\|V_{EE}\|$		2.4	3.0	3.4	V
Supply Current	I_{DD}	Without load		0.8	1.5	μA
Input Low Voltage	V_{IL}		$V_{SS}+0.3$		V_{SS}	V
Input High Voltage	V_{IH}		−0.3		0	V
Switch Activation Current	I_{SW}	$V_{IN}=V_{DD}$	0.1	1.0	10	μA
Oscillator Start Voltage	$\|V_{OSC}\|$	Within 5 sec			1.45	V
Oscillator Stop Voltage	$\|V_{OSP}\|$				1.15	V
Osc. Input Capacitor	CI			25		pF
Oscillator Frequency	F_{OSC}	CI=25pF, CO=20pF		32,768		Hz
DC-DC Conversion Freq.	V_{CON}	C1=C2=0.1μF		512		Hz
LCD Frequency	FD			32		Hz
SW Debouncing Time	TD				62.5	ms

3

FUNCTIONAL DESCRIPTION

DISPLAY CONTROL

• Standard Display

Normal KS5199A displays HOUR in digit 1, 2 and MINUTE in digit 3 and 4. In this state colon flashes at 1Hz rate.

Depression of D switch on normal display state will cause MONTH to be displayed in digit 1 and 2, DATE in digit 3 and 4 with colon off. MONTH and DATE are continuously displayed for 2 secnds after the D switch is released. Then HOUR and MINUTE are displayed again.

Two momentary depressions of D switch within 2 seconds in normal display state causes SECOND to be displayed in digit 3, 4 and the digit and 2 blanked with colon non-flashing continuously. Depressing S in this state resets and holds the SECOND counter until switch S is released and MINUTE counter either advanced or remains unchanged depending upon whether the SECOND counter is greater or less than 30 seconds.

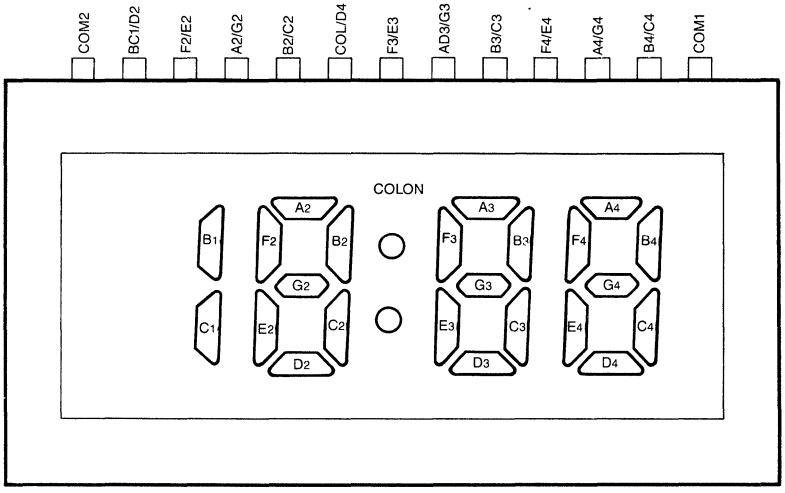
Depressing D in this state returns the display to HR : MIN display state.

• Alternating display

This mode is selected by activating the set switch (S) in normal display mode. In this mode HR : MIN is automatically displayed alternately with MONTH DATE. Each is displayed for two seconds.

The S input must be activated five times to return to normal display mode and depressing D switch in this alternating mode will cause the SECOND display mode.

3.5 DIGITS LCD FORMAT



* BC1/D2 must be connected to B1/C1 pad for 12-hour application.

Fig. 1

4 DIGITS LCD FORMAT

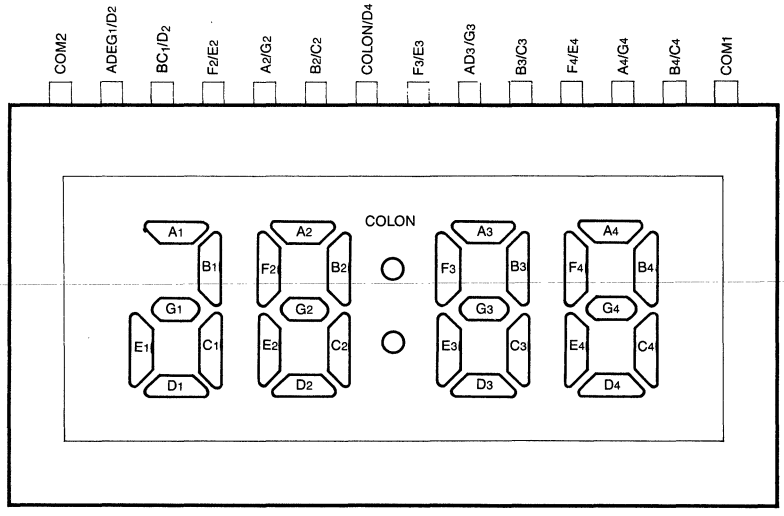


Fig. 2

f. Hold mode

Then watch enters the HOLD state with the next depression of S switch. In this state the display shows HOUR in digit 1 and 2, MINUTE in digit 3 and 4 and non-flashing colon. (Normal display state)

NOTE

It MINUTE is not changed in MINUTE set state, the watch does not enter the HOLD state but automatically reverts to normal display state.
The carry signal from any preceeding counter during operation is not accepted except for second reset.

SETTING AND DISPLAY SEQUENCE

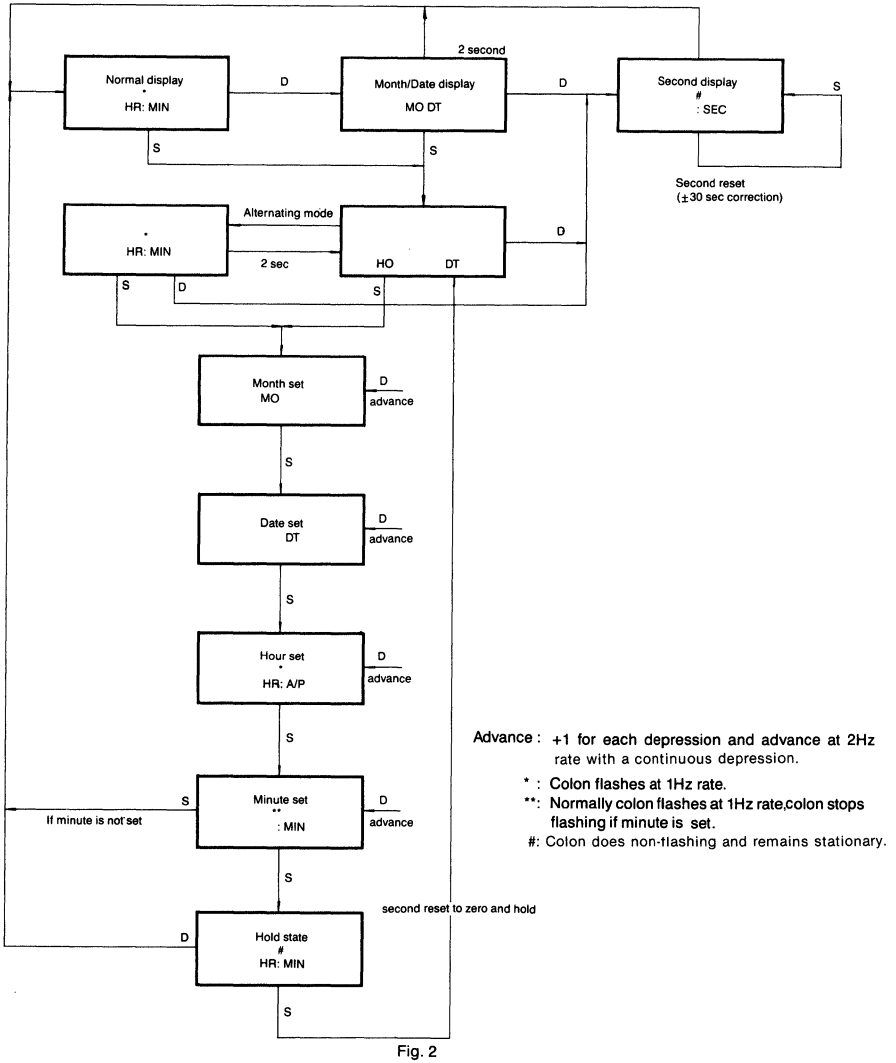
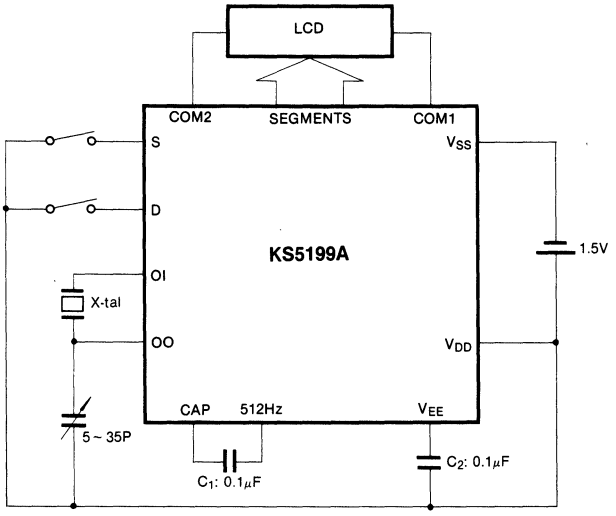


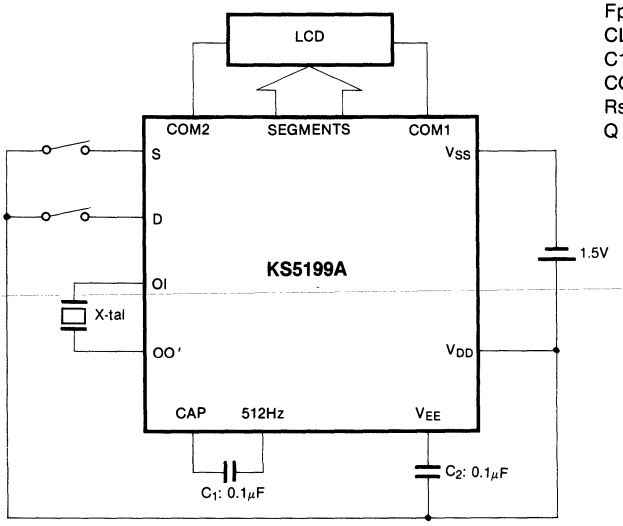
Fig. 2

APPLICATION CIRCUIT

1) External Trimmer Capacitor Type

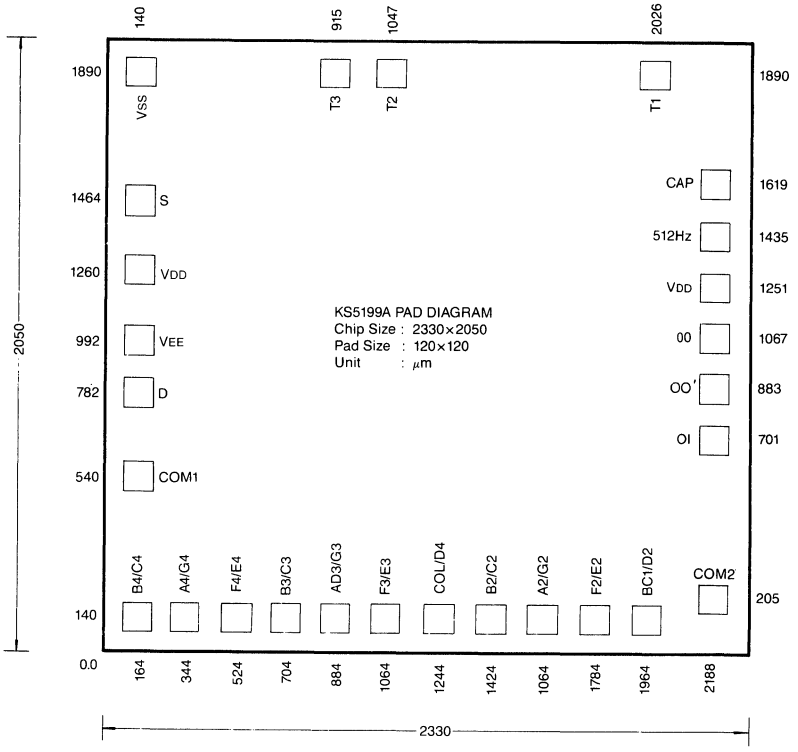


2) Internal Trimmer Capacitor Type



* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 12.5pF
C1 = 4pF
CO = 2.5pF
Rs = 35KΩ
Q = 35,000

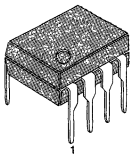
PAD DIAGRAM


KS5199A PAD DIAGRAM
Chip Size : 2330×2050
Pad Size : 120×120
Unit : μm
VSS
T3
T2
T1
S
VDD
VEE
D
COM1
CAP
512Hz
VDD
00
OO'
OI
COM2
B4/C4
A4/G4
F4/E4
B3/C3
AD3/G3
F3/E3
COL/D4
B2/C2
A2/G2
F2/E2
BC1/D2
140
915
1047
2026
1890
1464
1260
992
782
540
1619
1435
1251
1067
883
701
205
0.0
164
344
524
704
884
1064
1244
1424
1064
1784
1964
2188
2330
2050

BIPOLAR STEPPING MOTOR DRIVE ANALOG CLOCK

The KS5206 series, with alarm function, is a C-MOS integrated circuit for use in a clock with bipolar stepping motor.

8 DIP



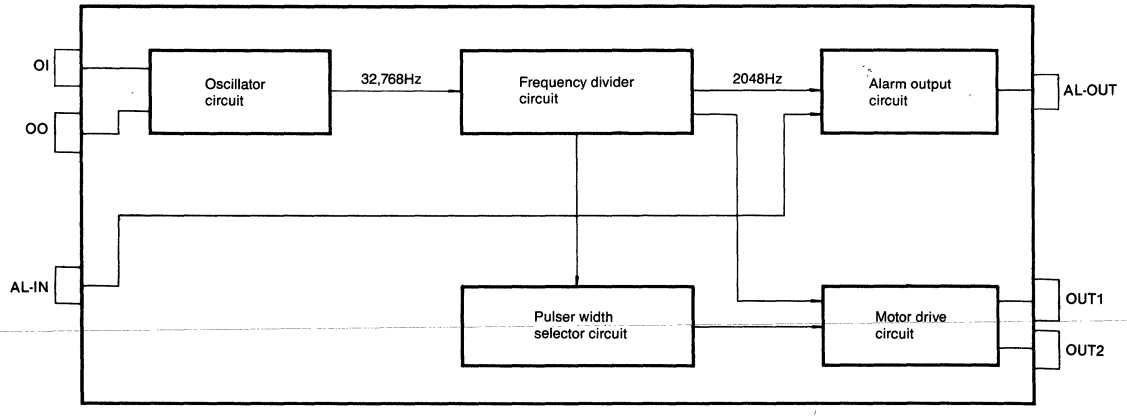
FUNCTIONS

- Output pulse duration KS5206A=0.5Hz, 1 sec.
  KS5206E=0.5Hz, 46.9msec
  KS5206F=0.5Hz, 31.2msec
- Gated 2048Hz alarm output.
- Active-high, AL-IN input for enable alarm output.

FEATURES

- **32.768KHz crystal oscillator**
- **Single 1.5V battery operation**
- **Low power dissipation**
- **8 pin dual-in-line plastic package and bare chip available**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−2.0 ~ 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−10 ~ +60	°C
Storage Temeprature	T_{stg}	−55 ~ +125	°C

• Value greater than this may damage the circuit

ELECTRICAL CHARACTERISTICS

(V_{DD} =0V, V_{SS} = −1.5V, T_a =25°C, F_{OSC} =32.768KHz; Unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	$\|V_{DD}\|$	Rm=∞ V_{SS} =−1.5V	1.2	1.5	1.7	V
Supply Current	I_{DD}			2.0	2.5	μA
Output Drive Current	I_{L1}	Rm=200Ω, V_{SS} =−1.2V	4.0	4.5		mA
	I_{L2}		4.0	4.5		mA
Alarm Output Sink Current	I_S	R=1KΩ, V_{SS} =−1.4V	−0.3	−0.6		mA
AL-IN Switch Current	I_{AL}			55.0	70.0	μA
OSC Start Voltage	$\|V_{OSC}\|$	Within 5 seconds			1.45	V
OSC Stop Voltage	$\|V_{OSP}\|$				1.0	V

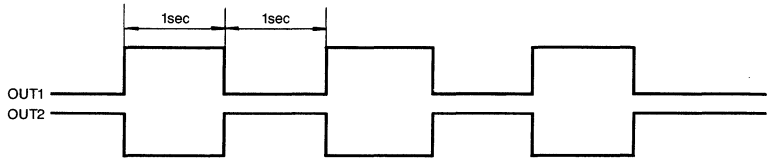
GENERAL DESCRIPTION

The KS5206 series is a C-MOS analog clock IC, driving a stepping motor precisely once in every second. When external 32.768KHz quartz crystal and single 1.5V battery are connected. Basically it consists of oscillator circuit, frequency divider, output pulse former, push-pull motor driver and alarm output. It provides alarm capability which on and off for equal time interval of 500msec. The alarm single is made of 2048Hz, 8Hz and 1Hz.

The alarm output consists of a push-pull stage and is able to drive an external bipolar transistor. Also the KS5206 series has a AL-IN input. As long as AL-IN input is connected with V_{DD}, alarm output is generated. (Fig. 2) To hear alarm sound, Buzzer (or speaker) must be connected to the alarm output. (pin 6) Whenever AL-IN input is connected to V_{DD}, alarm sound can be heard. The two outputs of KS5206A have 0.5Hz, 1 sec-width pulse waves with a 180 degrees phase shift. (Fig. 1-1). The output of KS5206E has 0.5Hz, 46.9msec-width pulse waves and KS5206F has 0.5Hz, 31.2msec-width pulse waves. (Fig. 1-2)

OUT 1 AND OUT 2 WAVEFORMS

1) KS5206A



2) KS5206E/F

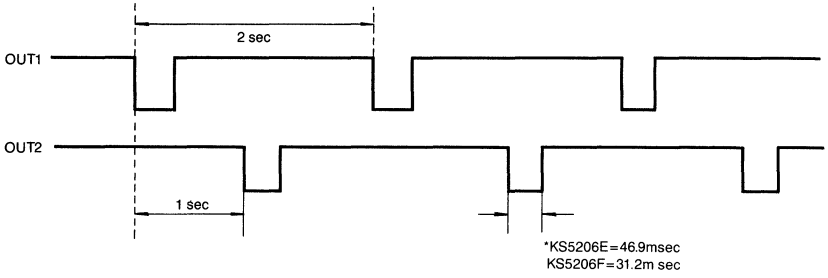


Fig. 1

ALARM OUTPUT WAVEFORM (KS5206A, E, F)

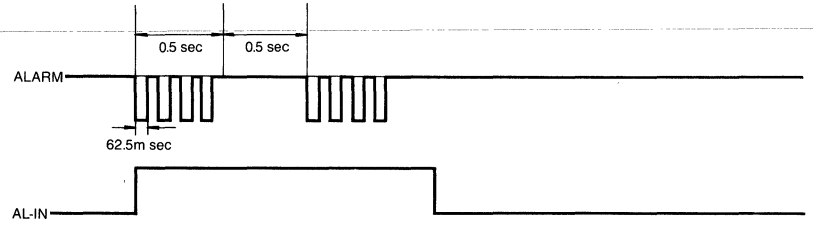
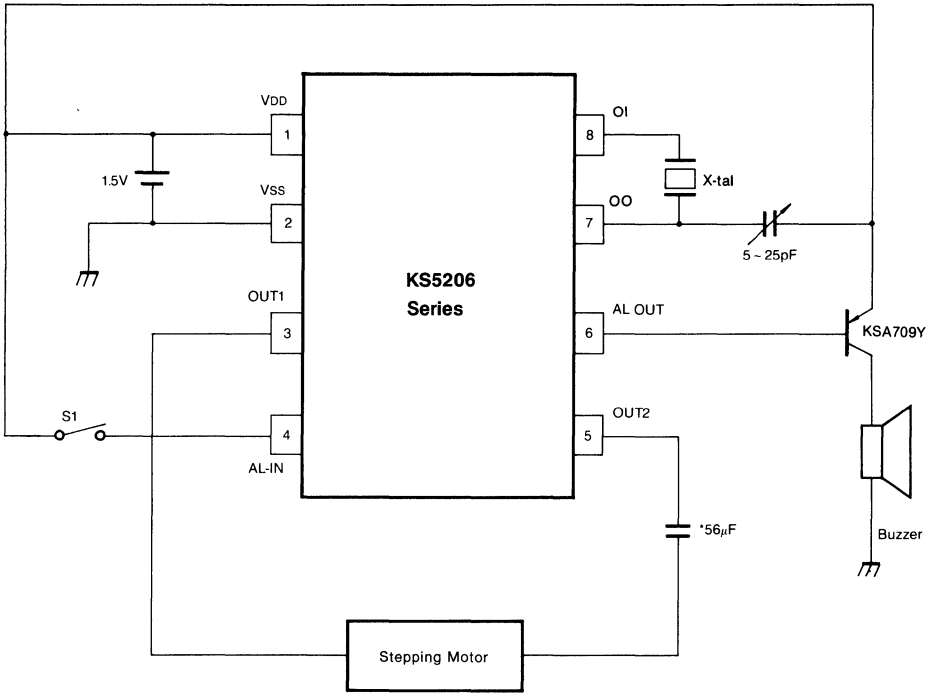


Fig. 2

APPLICATION CIRCUIT

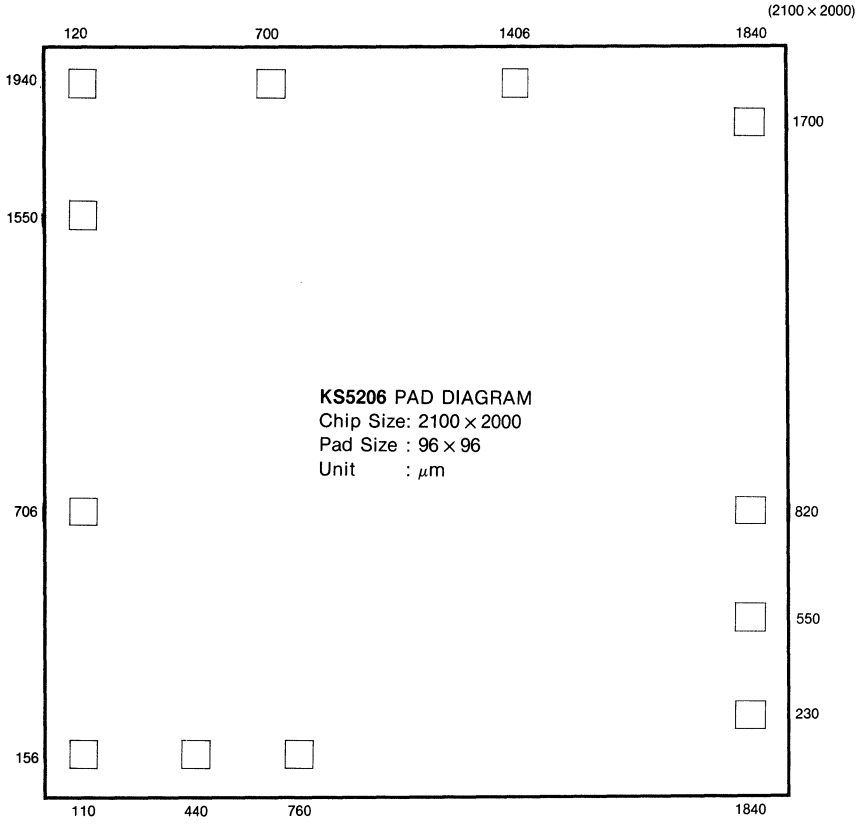


* Quartz crystal parameters
f_P =32,768Hz
C_L =10pF
C1= 4pF
CO=2.5pF
R_S =36K
Q=35,000

* No NEED CAPACITOR in KS5206E, F

Fig. 3.

PAD LOCATION

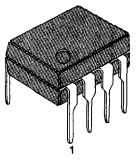


Pad No.	Designation	Pad No.	Designation
1	V_{DD}	8	OUT 2
2	V_{SS}	9	NC
3	T1	10	T2
4	OUT 1	11	AL-OUTPUT
5	RESET	12	1HR
6	AL-IN	13	OO
7	NC	14	OI

BIPOLAR STEPPING MOTOR DRIVE ANALOG CLOCK

The KS5207 series with 1HR function, is a C-MOS integrated circuit in- for use in a clock with bipolar stepping motor.

8 DIP



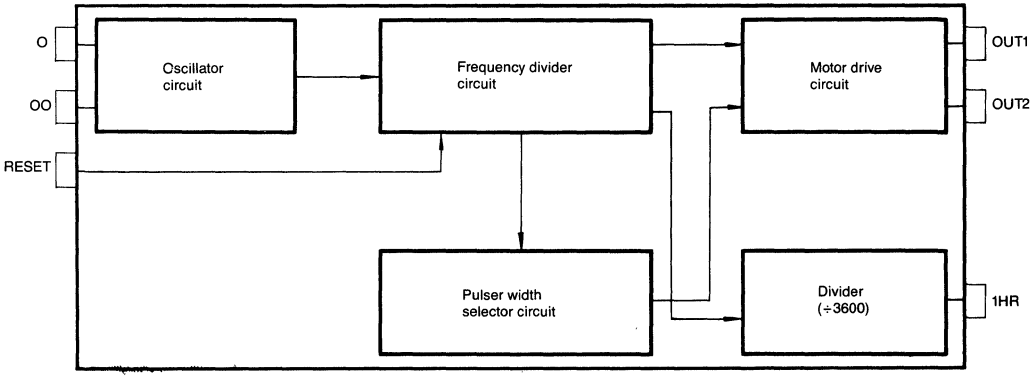
FUNCTIONS

- Output pulse duration KS5207A=0.5Hz, 1sec.
  KS5207E=0.5Hz, 46.9msec
  KS5207F=0.5Hz, 31.2msec
- A 2sec-width pulse output per hour.
- Active-high, RESET input for disable motor output.

FEATURES

- **32.768KHz crystal oscillator.**
- **Single 1.5V battery operation.**
- **Low power dissipation.**
- **8 pin dual-in-line plastic package and bare chip available**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−2.0 ~ 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	Topr	− 10 ~ + 60	°C
Storage Temperature	Tstg	−55 ~ +125	°C

*Value greater than above may damage the circuit

ELECTRICAL CHARACTERISTICS

(V_{DD} =0V, V_{SS} = −1.5V, T_a =25°C, F_{OSC} =32.768KHz; Unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	$\|V_{DD}\|$	Rm=∞, V_{SS} = −1.5V	1.2	1.5	1.7	V
Supply Current	I_{DD}			2.0	2.5	μA
Output Drive Current	I_{L1}	Rm = 200Ω, V_{SS} = −1.2V	4.0			mA
	I_{L2}		4.0			mA
Reset Switch Current	I_{RS}			55	70	μA
OSC Start Voltage	$\|V_{OSC}\|$	Within 5 seconds				V
OSC Stop Voltage	$\|V_{OSP}\|$				1.0	V

GENERAL DESCRIPTION

The KS5207 series is a C-MOS analog clock IC, driving a stepping motor precisely once in every second. When external 32.768KHz quartz crystal and single 1.5V battery are connected. Basically it consists of oscillator circuit, frequency divider, output pulse former, push-pull motor driver and 1HR output. The two outputs of KS5207A have 0.5Hz, 1sec-width pulse waves with a 180 degrees phase shift. (Fig. 1-1)

The output of KS5207E has 0.5Hz, 46.9msec-width pulse waves and KS5207F has 0.5Hz, 31.2msec-width pulse waves. (Fig. 1-2)

Also the KS5207 series has a RESET input. As long as the RESET input is connected to V_{DD}, there is no motor output pulse.

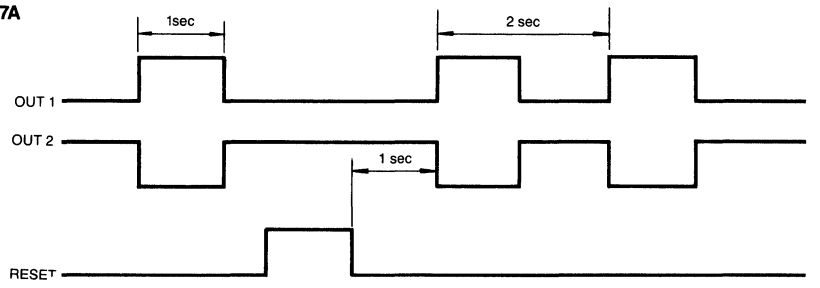
One second after releasing this connection, a relative moter pulse is generated. (Fig. 1)

Particularly, the KS5207 series has a 2sec-width pulse output per hour. (Fig. 2)

To hear melody sound once per hour, melody IC should be connected with the 1HR output. (pin 6)

OUT 1 AND OUT 2 WAVEFORMS

1) KS5207A



2) KS5207E/F

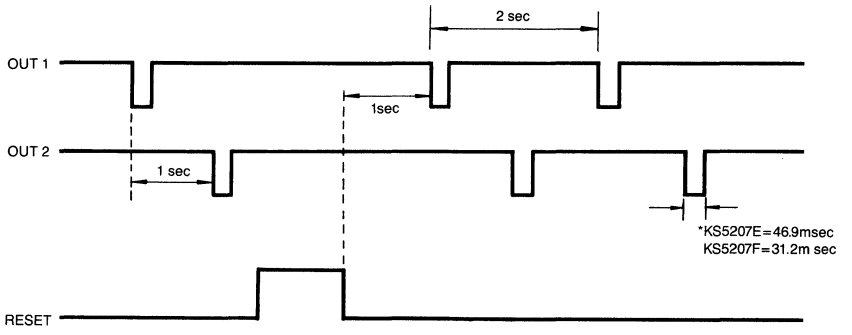


Fig. 1

1 HR OUTPUT WAVEFORM (KS5207A, E, F)

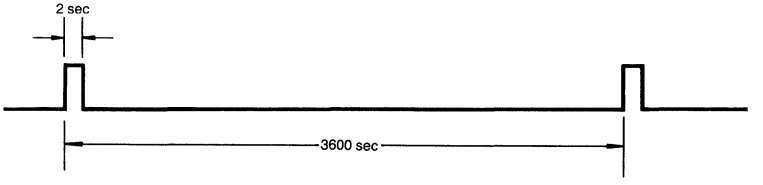
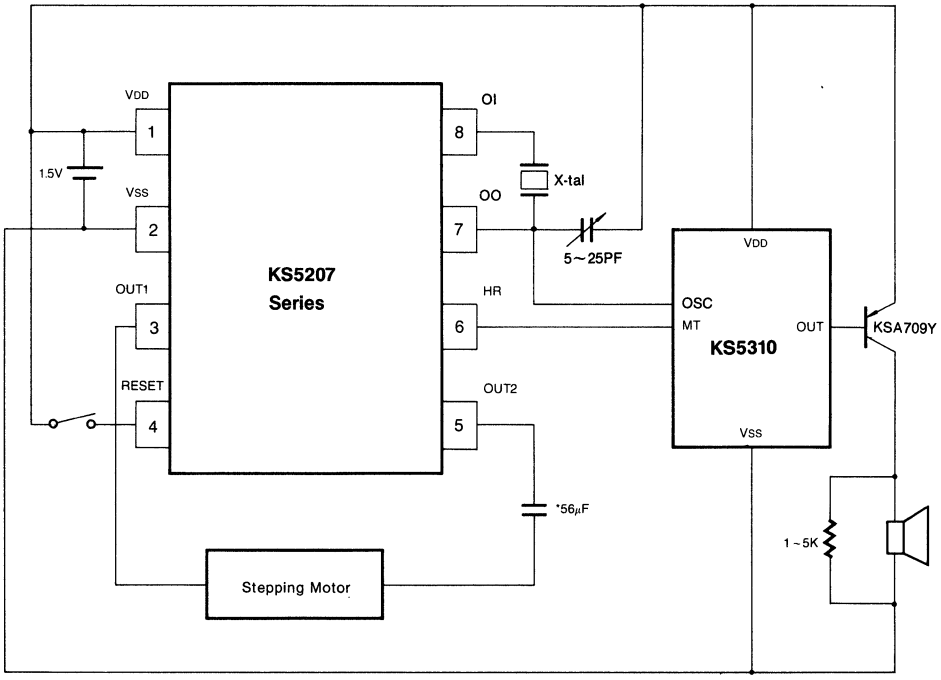


Fig. 2

APPLICATION CIRCUIT

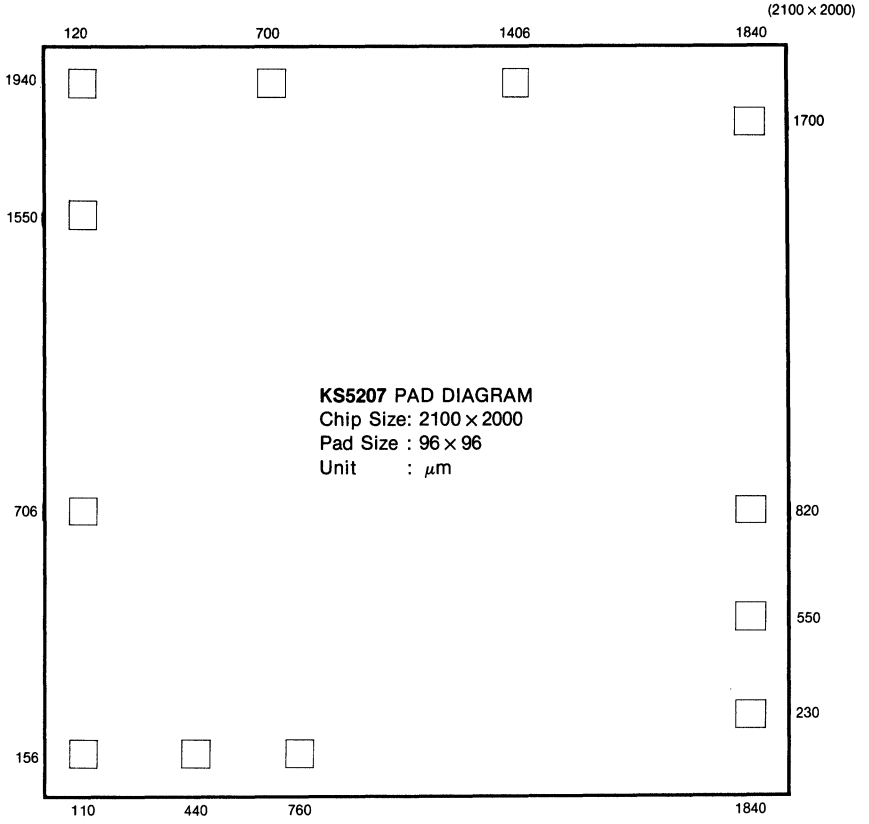


Quartz Crystal Parameters
f_P=32,768Hz
C_L=10pF
C_1=4pF
C0=2.5pF
R_S=36K
Q=35000

* No NEED CAPACITOR in KS5207E, F

Fig. 3

PAD LOCATION

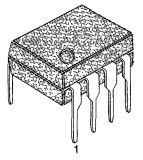


Pad No.	Designation	Pad No.	Designation
1	V_{DD}	8	OUT 2
2	V_{SS}	9	NC
3	T1	10	T2
4	OUT 1	11	AL-OUTPUT
5	RESET	12	1HR
6	AL-IN	13	OO
7	NC	14	OI

BIPOLAR STEPPING MOTOR DRIVE ANALOG CLOCK

The KS5209 series with alarm function is a CMOS integrated circuit for use in a clock with bipolar stepping motor.

8 DIP



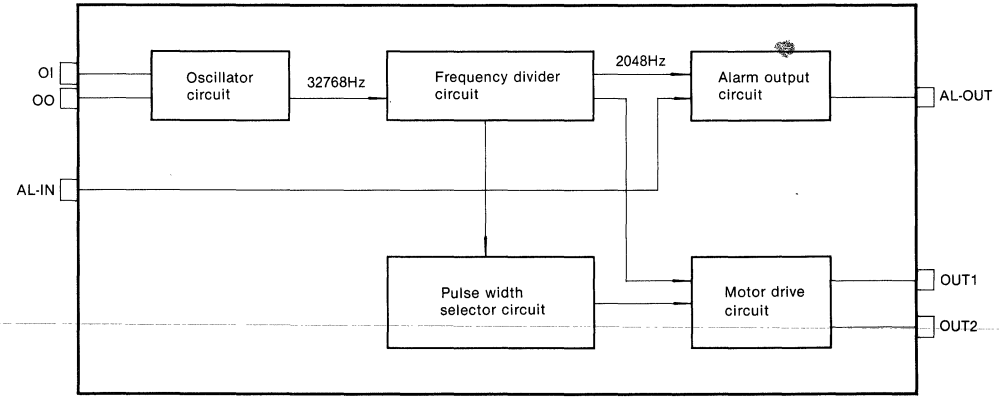
FUNCTIONS

- Output pulse duration: KS5209A = 0.5Hz, 1 sec
  KS5209E = 0.5Hz, 46.9msec
  KS5209F = 0.5Hz, 31.2msec
- Gated 2048Hz alarm output
- Active-high, AL-IN input to enable alarm output

FEATURES

- **32.768KHz crystal oscillator**
- **Single 1.5V battery operation**
- **Low power dissipation**
- **8 pin dual-in-line plastic package and bare chip are available**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	− 0.3 ~ + 1.7	V
Power Dissipation	P_d	300	mW
Operating Temperature	T_{opr}	− 10 ~ + 60	°C
Storage Temperature	T_{stg}	− 55 ~ + 125	°C

• Value greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.5V, V_{SS} = 0V, Ta = 25°C F_{OSC} = 32.768KHz; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	Rm = ∞ , V_{DD} = 1.5V	1.2	1.5	1.7	V
Supply Current	I_{dd}			1.0	2.0	μA
Output Drive Current	IL1	Rm = 200Ω, V_{DD} = 1.2V	4.0			mA
	IL2		4.0			mA
Alarm Output Sink Current	I_S	R_L = 1K, V_{DD} = 1.4V	0.4	0.7		mA
Alarm Output Drive Current	I_d		0.4	0.7		mA
AL-IN Switch Current	I_{al}			2.0	3.0	μA
OSC Start Voltage	V_{OSC}	Specify		0.9	1.1	V
OSC Stop Voltage	V_{stop}			0.9	1.1	V

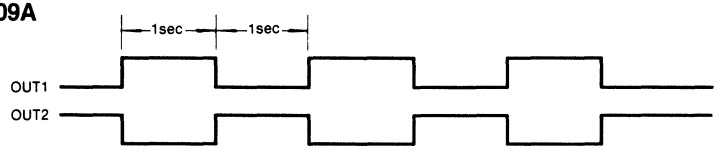
GENERAL DESCRIPTION

The KS5209 series is a CMOS analog clock IC, driving a stepping motor precisely once in every second. When external 32.768KHz quartz crystal and single 1.5V battery are connected. Basically it consists of oscillator circuit, frequency divider, output pulse former, push-pull motor driver and alarm output. It provides alarm capability which on and off for equal time internal of 500msec. The alarm signal is made of 2048Hz, 8Hz, 1Hz.

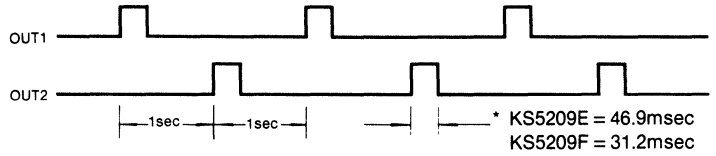
The alarm output consists of a push-pull stage and is able to drive an external-bipolar transister. Also the KS5209 series has a AL-IN input. As long as AL-IN input is connected to V_{DD}, alarm output is generated. (Fig. 2). To hear a alarm sound, buzzer (or speaker) should be connected to the alarm output. Whenever AL-IN input is connected to V_{DD}, alarm sound can be heard. The two outputs of KS5209A have 0.5Hz, 1sec-width pulse waves with a 180 degrees phase shift. (Fig. 1-1). The output of KS5209E has 0.5Hz, 46.9msec-width pulse waves and KS5209F has 0.5Hz, 31.2msec-width pulse waves. (Fig. 1-2).

OUT1 AND OUT2 WAVEFORMS

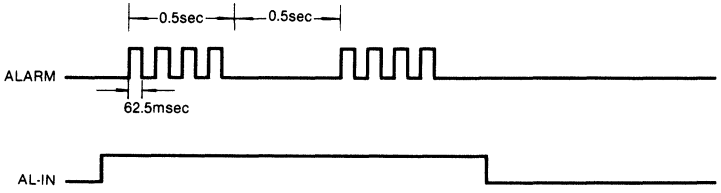
1) KS5209A



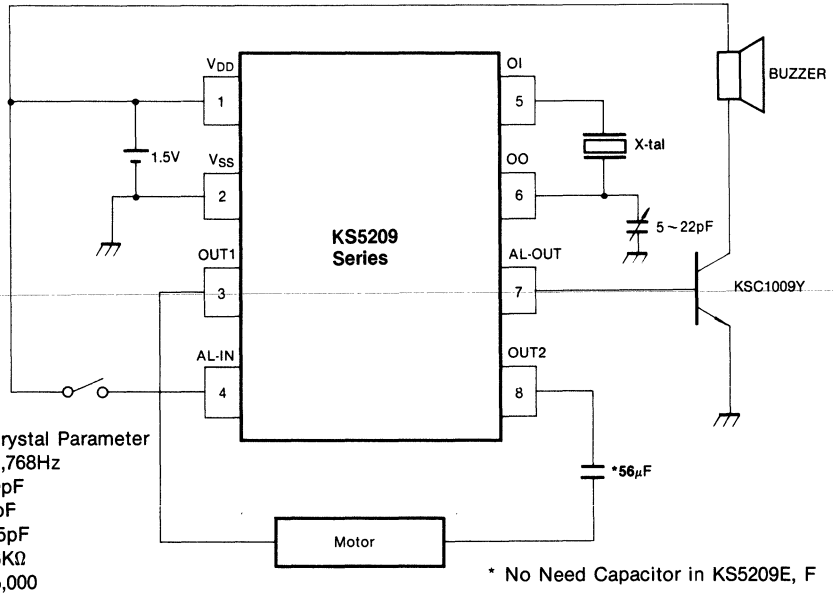
2) KS5209E/F



ALARM OUTPUT WAVEFORM (KS5209A, E, F)



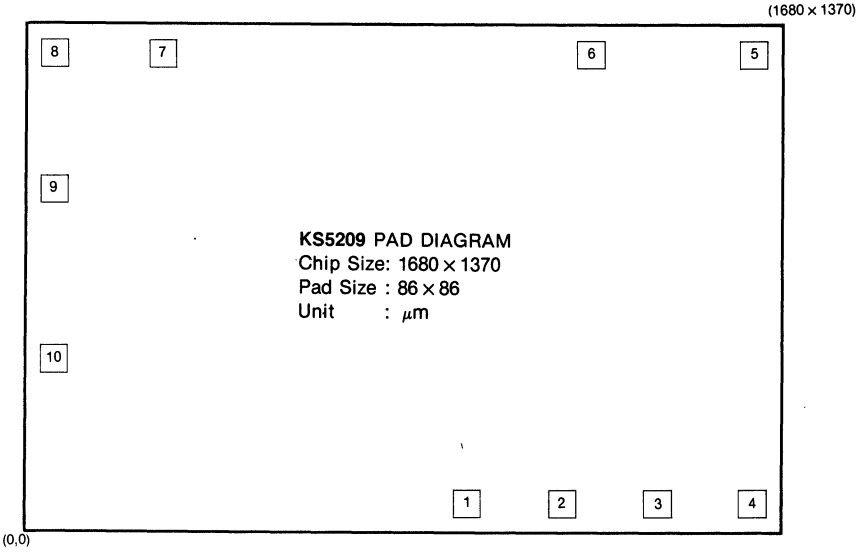
TYPICAL APPLICATION CIRCUIT



* Quartz Crystal Parameter
  Fp = 32,768Hz
  CL = 10pF
  C1 = 4pF
  CO = 2.5pF
  Rs = 36KΩ
  Q = 35,000

* No Need Capacitor in KS5209E, F

PAD LOCATION

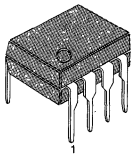


Pad No.	Designation
1	OI
2	SET/TIN
3	V_{DD}
4	V_{SS}
5	M1
6	AL-IN
7	M2
8	T-OUT
9	AL-OUT
10	OO

BIPOLAR STEPPING MOTOR DRIVE ANALOG CLOCK

The KS5210 series, with alarm function, is a C-MOS integrated circuit for use in a clock with bipolar stepping motor.

8 DIP



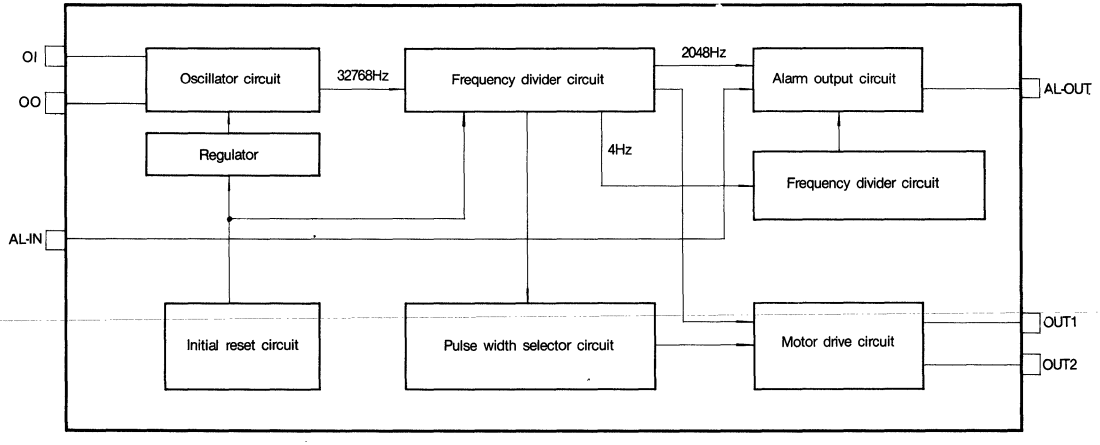
FUNCTIONS

- Output pulse duration: KS5210A = 0.5Hz, 1 sec
  KS5210E = 0.5Hz, 46.9msec
  KS5210F = 0.5Hz, 31.2msec
- Low-active, AL-IN input to enable alarm output

FEATURES

- **32.768KHz crystal oscillator**
- **Single 1.5V battery operation**
- **Low power dissipation**
- **8 pin dual-in-line plastic package and bare chip are available**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +1.8	V
Operating Temperature	T_{opr}	−10 ~ +60	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

• Value greater than above may result damage the circuit

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.4V, V_{SS} = 0V Ta = 25°C F_{OSC} = 32.768KHz: unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	$R_L = \infty$, V_{DD} = 1.4V	1.1		1.8	V
Supply Current	I_{DD}			0.7	2.0	μA
Output Drive Current	I_{L1}	Rm = 200Ω, V_{DD} = 1.2V	4.0			mA
	I_{L2}		4.0			mA
Alarm Output Drive Current	I_D	R_L = 5KΩ, V_{DD} = 1.2V	0.2			mA
Alarm Output Sink Current	I_S		0.5			μA
AL-IN Switch Current	I_{AL}			5.0	10.0	μA
OSC Start Voltage	V_{OSC}	Specify		0.9	1.1	V
OSC Stop Voltage	V_{OSP}			0.9	1.1	V
OSC Stability	V_{ostb}	$\triangle V_{DD}$ = 100mV		0.2	1	ppm

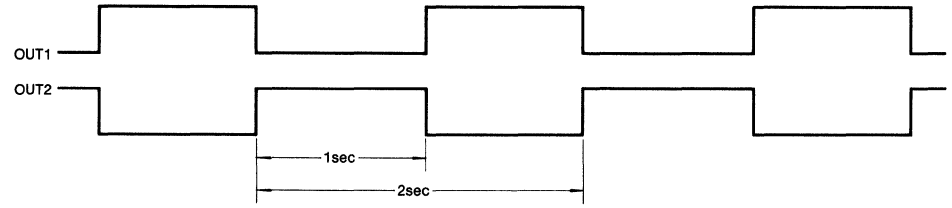
GENERAL DESCRIPTION

The KS5210 series is a C-MOS analog clock IC, driving a stepping motor precisely once in every second. When external 32.768KHz quartz crystal and single 1.5V battery are connected. Basically it consists of oscillator circuit, regulator circuit, frequency divider, output pulse former, push-pull motor driver and alarm output, which makes alarm capability on-time 1sec and then off-time 3 sec. The alarm signal is made of 2048Hz, 8Hz, 0.5Hz and 0.25Hz.

The alarm output consists of a push-pull stage and is able to drive an external bipolar transistor. Also the KS5210 series has a AL-IN input. As long as AL-IN input is connected with V_{SS}, alarm output is generated. (Fig. 2) To hear alarm sound, Buzzer (or speaker) must be connected to the alarm output. (pin 6) Whenever AL-IN input couples with V_{SS}, alarm sound can be heard. The two outputs of KS5210A have 0.5Hz, 1 sec-width pulse waves with a 180 degrees phase shift. (Fig. 1-1) The output of KS5210E has 0.5Hz, 46.9msec-width pulse waves while KS5210F has 0.5Hz, 31.2msec-width pulse waves. (Fig. 1-2)

OUT1 AND OUT2 WAVEFORMS

1) KS5210A



2) KS5210E/F

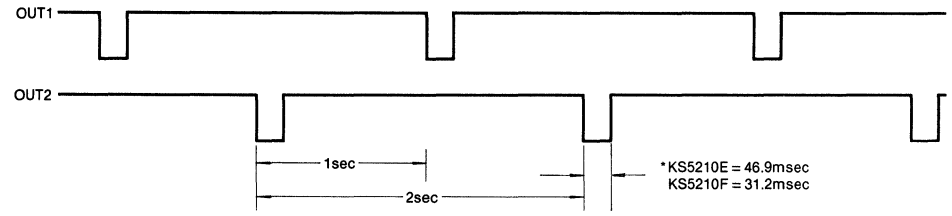


Fig. 1

ALARM OUTPUT WAVEFORM (KS5210A, E, F)

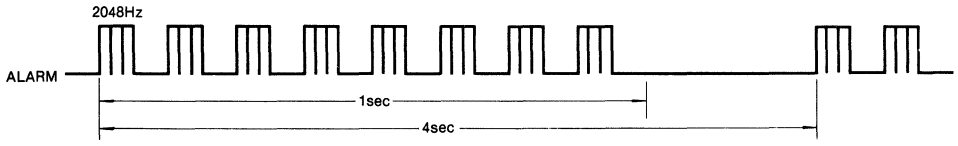
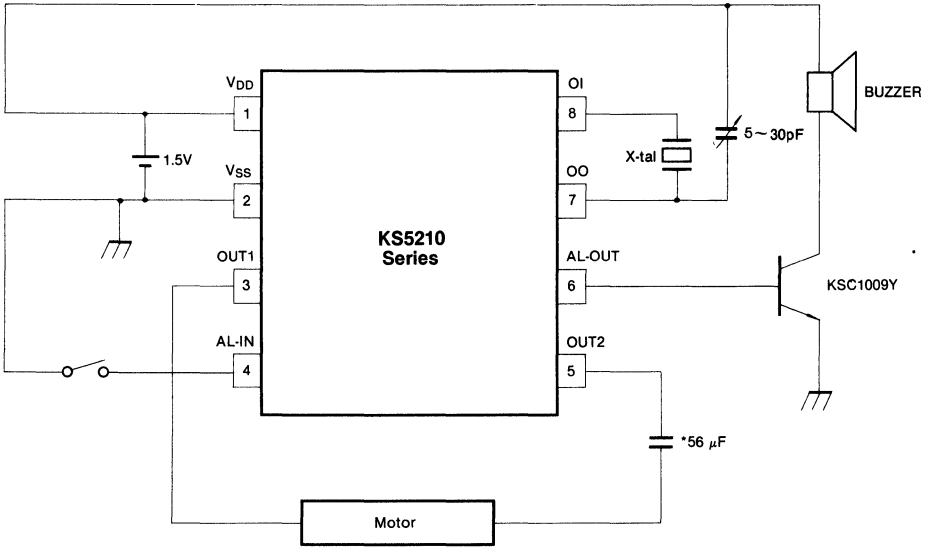


Fig. 2

TYPICAL APPLICATION CIRCUIT

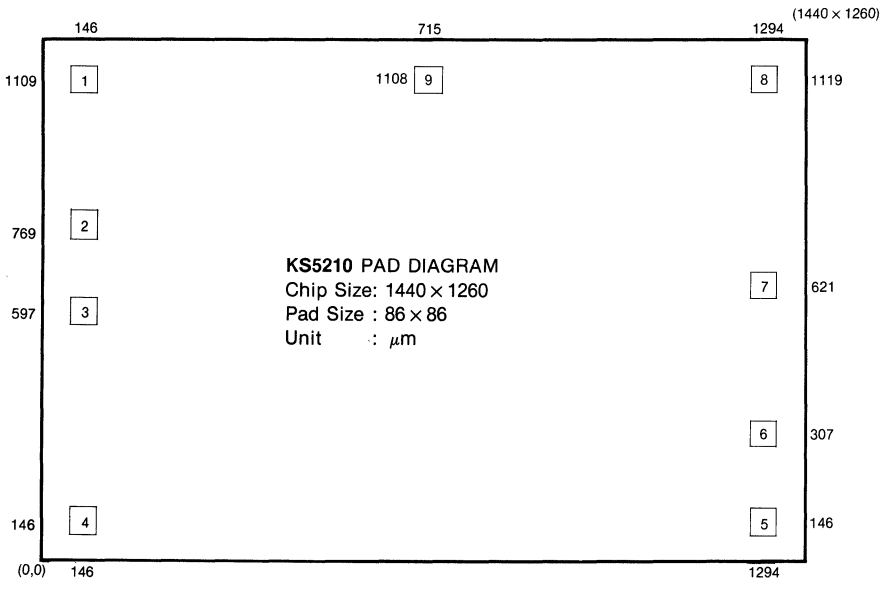


*Quartz crystal parameter
$F_P = 32{,}768Hz$
$C_L = 10pF$
$C_1 = 4pF$
$C_0 = 2.5pF$
$R_S = 36K$
$Q = 35000$

* NO NEED CAPACITOR IN KS5210E, F

Fig. 3

PAD LOCATION

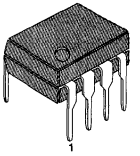


Pad No.	Designation	Pad No.	Designation
1	V_{DD}	6	AL-OUT
2	V_{SS}	7	OO
3	M1	8	OI
4	AL-IN	9	V_{EE}
5	M2	10	

BIPOLAR STEPPING MOTOR DRIVE ANALOG CLOCK

The KS5211 series with alarm function is a CMOS integrated circuit in for use in a with bipolar stepping motor.

8 DIP



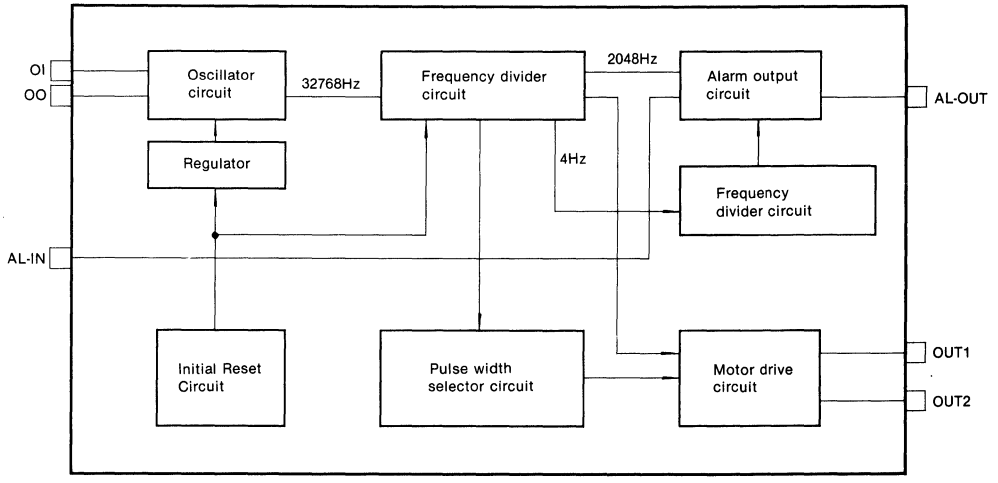
FUNCTIONS

- Output pulse duration: KS5211A = 0.5Hz, 1 sec
  KS5211E = 0.5Hz, 46.9msec
  KS5211F = 0.5Hz, 31.2msec
- Low-active AL-IN input to enable alarm output

FEATURES

- 32.768KHz crystal oscillator
- Single 1.5V battery operation
- Low power dissipation
- 8 pin dual-in-line plastic package and bare chip are available
- No trimmer capacitor

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +1.8	V
Power Dissipation	P_d	300	mW
Operating Temperature	T_{opr}	−10 ~ +60	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

• Value greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.5V, V_{SS} = 0V, Ta = 25°C, F_{OSC} = 32.768KHz; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	Rm = ∞ , V_{DD} = 1.5V	1.2	1.5	1.8	V
Supply Current	I_{dd}			0.7	2.0	μA
Output Drive Current	IL1	Rm = 200Ω, V_{DD} = 1.2V	4.0			mA
	IL2		4.0			mA
Alarm Output Sink Current	I_S	R_L = 1K, V_{DD} = 1.5V	0.3			mA
Alarm Output Drive Current	I_d		0.3			mA
AL-IN Switch Current	I_{al}			2.0	3.0	μA
OSC Start Voltage	V_{OSC}	Specify		0.9	1.1	V
OSC Stop Voltage	V_{stop}			0.9	1.1	V
OSC Stability	O_{stb}	△V_{DD} = 100mV		0.5	1	ppm
OSC Output Capacitance	C_{out}			20		pF
OSC Input Capacitance	C_{in}			20		pF
OSC Accuracy	O_{acr}			0.7	2	sec/day

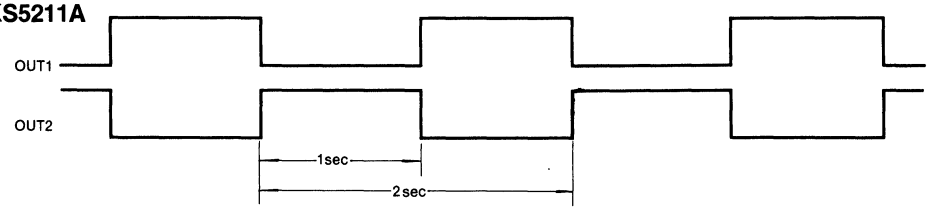
GENERAL DESCRIPTION

The KS5211 series is a CMOS analog clock IC, driving a stepping motor precisely once in every second when external 32.768KHz quartz crystal and single 1.5V battery are connected. Basically it consists of oscillator circuit regulator circuit, frequency divider, output pulse former, push-pull motor driver and alarm output. Which makes alarm capability on-time 1 sec and off-time 3 sec. The alarm signal is made of 2048Hz, 8Hz, 0.5Hz and 0.25Hz.

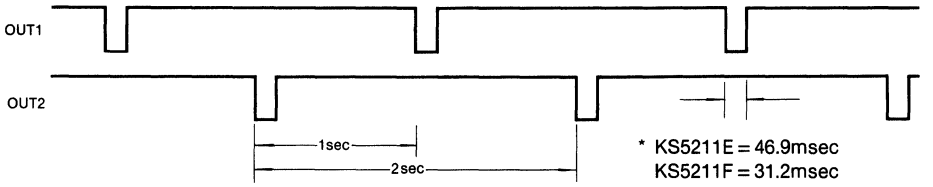
The alarm output consistes of a push-pull stage and is able to drive an external-bipolar transister. And the KS5211 series has a AL-IN input. As long as AL-IN input is connected to V_{SS}, alarm output is generated. (Fig. 2). When buzzer (or speaker) is connected with alarm output, alarm sound can be heard. Also it can be heard if AL-IN input couples with V_{SS}. The two output of KS5211A has 0.5Hz, 1sec-width pulse waves with a 180 degrees phase shift. (Fig. 1-1). The output of KS5211E has 0.5Hz, 46.9msec-width pulse waves and KS5211F has 0.5Hz, 31.2msec-width pulse waves. (Fig. 1-2).

OUT1 AND OUT2 WAVEFORMS

1) KS5211A

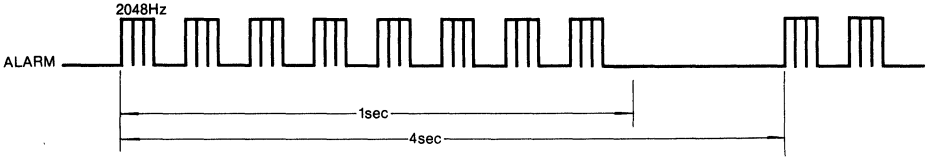


2) KS5211E/F

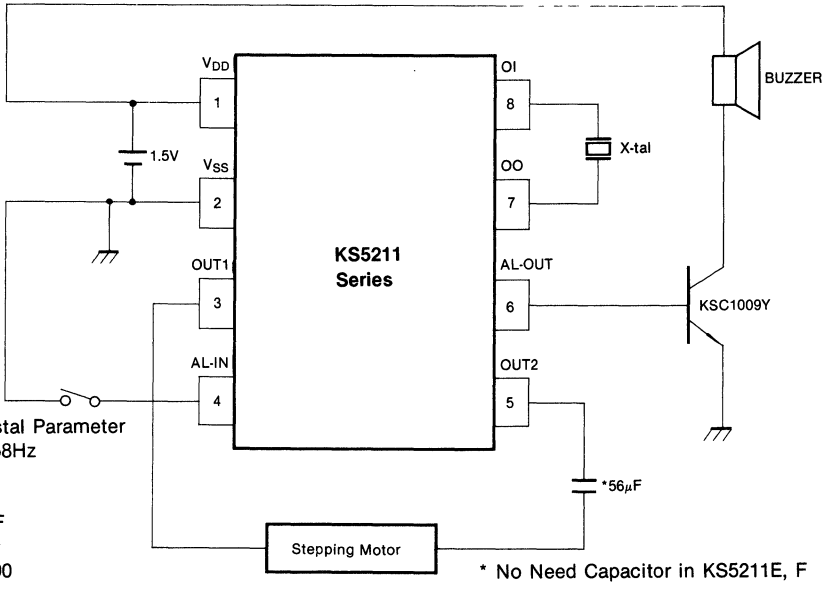


* KS5211E = 46.9msec
KS5211F = 31.2msec

ALARM OUTPUT WAVEFORM (KS5211A, E, F)



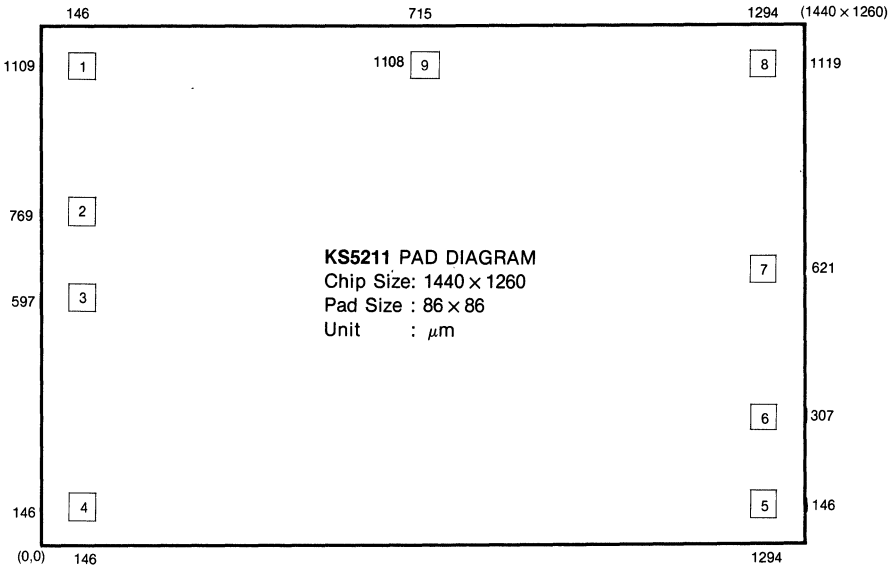
TYPICAL APPLICATION CIRCUIT



* Quartz Crystal Parameter
Fp = 32,768Hz
CL = 10pF
C1 = 4pF
CO = 2.5pF
Rs = 36KΩ
Q = 35,000

* No Need Capacitor in KS5211E, F

PAD LOCATION



Pad No.	Designation	Pad No.	Designation
1	V_{DD}	6	AL-OUT
2	V_{SS}	7	OO
3	M1	8	OI
4	AL-IN	9	V_{EE}
5	M2	10	

GENERAL DESCRIPTION

The KS5243 is an analog watch in CMOS metal gate process. It is designed for 32.768 KHz crystal oscillator analog watch. Pulse width is selected from 0.98 msec to 14.64 msec (by MASK option). Pulse period is selected from 1 sec to 60 sec (by MASK option). It consists of voltage regulator for low power consumption.

FEATURES

- **32.768 KHz oscillator**
- **Voltage regulator**
- **MASK option for PAD location, pulse width, pulse period**
- **Fast test operation by 16 Hz or 32 Hz (metal option)**
- **Stop operation by reset input**
- **Low resistance output for bipolar stepping motor**

OPTION

- **Pulse width**

0.98, 1.95, 2.93, 3.9, 4.88, 5.05, 6.83, 7.8, 8.79, 9.76, 10.74, 11.71, 12.69, 13.66, 14.64 (msec)

- **Pulse period**

1, 2, 3, 4, 5, 6, 10, 12, 15, 20, 30, 60 (sec)
(It is selected by metal option.)

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Test Condition	Unit
Supply Voltage	V_{DD}	$-0.3 \sim +5.0$	V
Input High Voltage	V_{IH}	$V_{DD} \sim +0.3$	V
Input Low Voltage	V_{IL}	$V_{SS} \sim +0.3$	V
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C

* Voltage greater than above may damage the circuit

OPERATING CHARACTERISTICS

(V_{DD} = 0V, V_{SS} = −1.55V, Ta = +25°C; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{SS}		−1.8		−1.2	V
Supply Current	I_{DD}	C_{OUT} = 5 pF C_{TR} = 15 pF		170	300	nA
	I_{DD}	C_{OUT} = 16 pF C_{TR} = 15 pF		280	400	nA
Voltage Between Motor Outputs	V_M	R_L = 2KΩ	±1.4			V
Pulse Period	T_M	Mask Option	2		120	sec
Pulse Width	t_M		0.98		14.64	msec
Test Output Frequency	F_{TE}	TE1		512		Hz
Test Debounce Time	T_{CH}	TE2 = V_{DD}	1		3	msec
Input Current After Debounce Time	I_{TE}	V_{TE} = V_{DD}			1.0	μA
Reset Debounce Delay	T_{RE}	Reset Connected to V_{DD}	7.8		23.4	msec
Input Current After Debounce Time	I_{RE}				100	nA
Oscillator Start Up Vol.	V_{ST}	△V_{SS} = 100mV			−1.2	V
Oscillator Start Up Time	T_{ST}			1	2	sec
Oscillator Stability	△f/f			0.1	0.2	ppm
Oscillator Internal Capacitance	C_{OI}	Mask Option	3		18	pF
	C_{OO}		3		18	pF
ESD	V_{ESD}	100 pF, 1.5KΩ	1,000			V

FUNCTIONAL DESCRIPTION

VOLTAGE REGULATOR

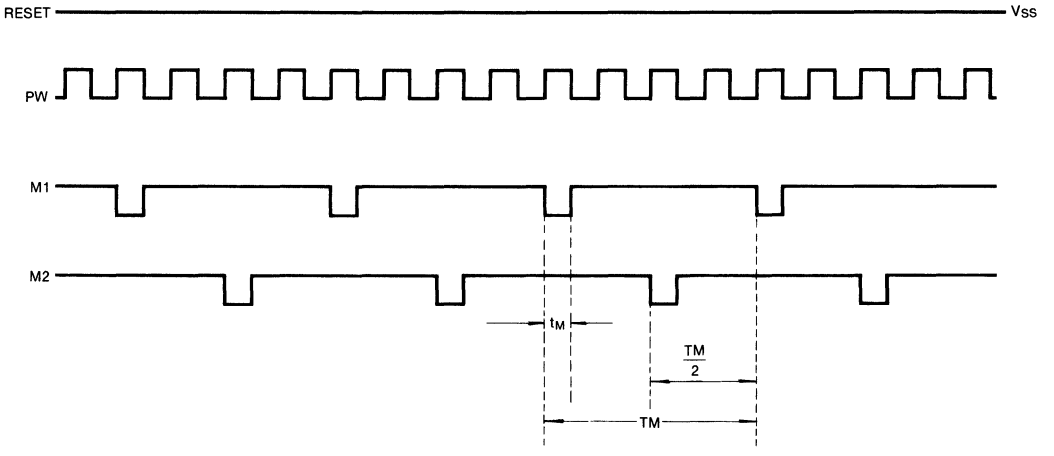
Negative supply voltage V_{EE} contorled by voltage regulator is supplyed to the oscillator output and the leading counter controlled by HIGH frequency. This improves the stability of the oscillator. This makes the total power consumption decrease.

FREQUENCY DIVIDER

The oscillator frequency down to 1/64 Hz by a 21 bit binary counter. V_{DD} and V_{EE} is supplyed to the leading 6 counter while V_{DD} and V_{SS} is supplyed to the remaining 15 counter.

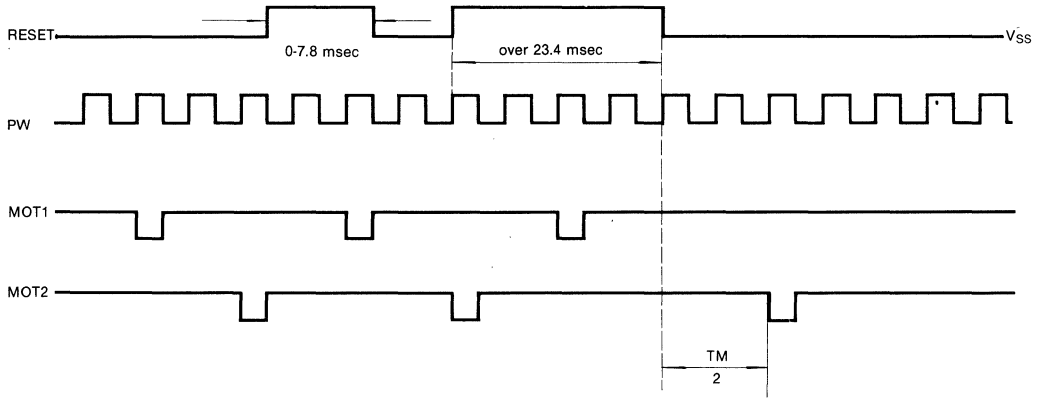
MOTOR DRIVE OUTPUT

The KS5243 contains two push-pull output butters for driving bipolar stepping motors. During a motor pulse width the N channel device of one buffer are active. Between two pulse width the P channel devices of both buffers are active. Pulse period and pulse width is selected by metal option.



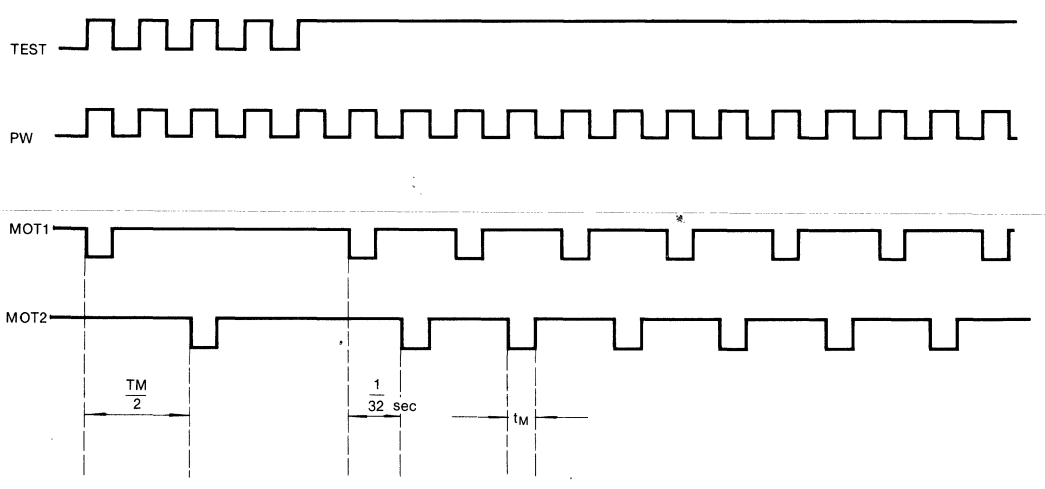
RESET

When the reset input is connected to V_{DD}, all divider counter is reset after debounce delay time. Debounce delay minimum time is 7.8 msec and maximum time is 23.4 msec. When the RESET input is connected to V_{SS}, the next motor pulse appears after the 1/2 pulse period time.

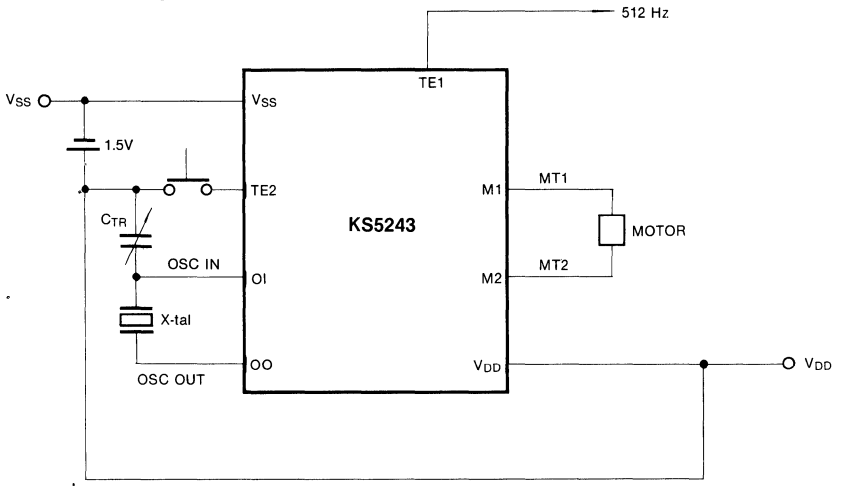


TEST

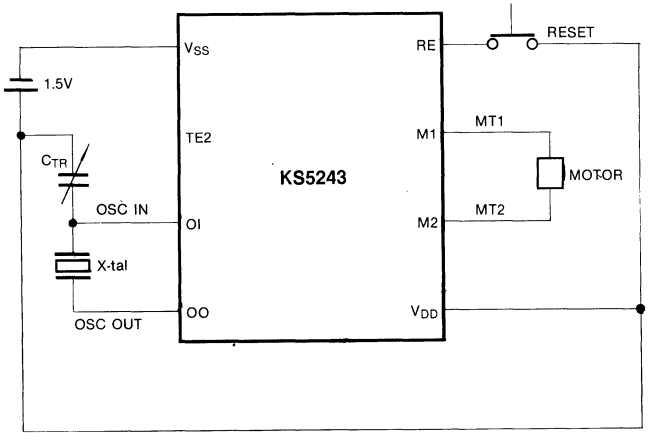
512 Hz of a test frequency is measured on TEST PAD and can be used for testing and tuning the oscillator. When TEST input is connected to V_{DD} for least 3 msec, the pulse period is changed 1/16 sec or 1/32 sec.



TEST CIRCUIT

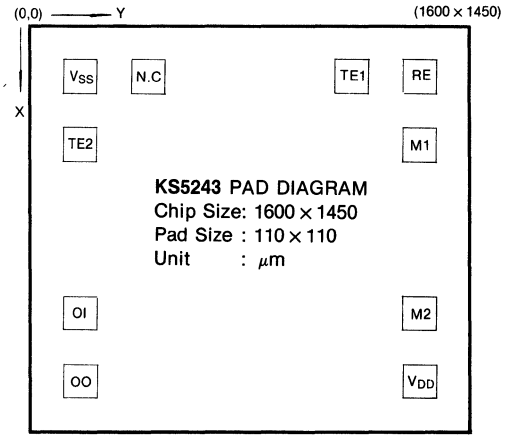


APPLICATION CIRCUIT

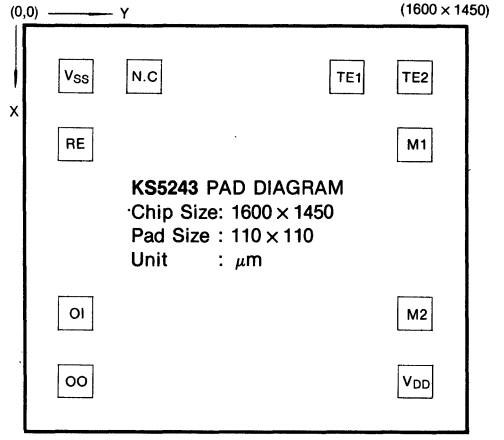


PAD DIAGRAM

TYPE A



TYPE B

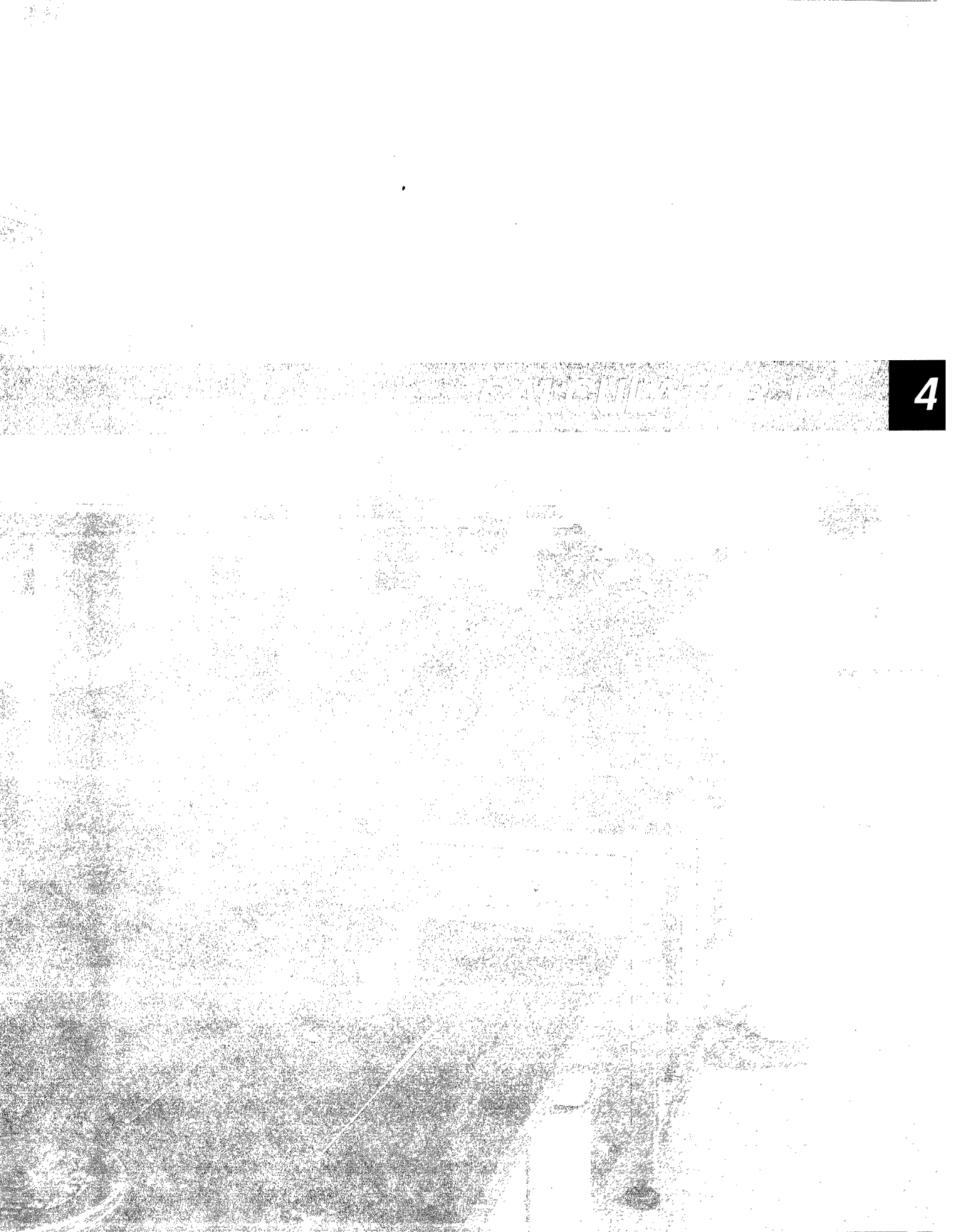


PAD LOCATION

Pad \ Coordination	X	Y
V_{DD}	1465	1265
M2	1245	1265
M1	380	1265
RE (TE2)	135	1265
TE1	135	835
N.C.	135	625
V_{SS}	135	135
TE2 (RE)	315	135
OI	950	135
OO	1155	135

( ): type B

TE1; TEST OUTPUT
TE2; TEST OPERATION INPUT
(It is tested in 'High' state)



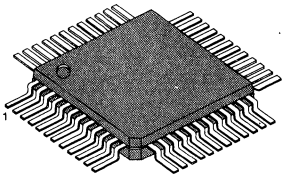
Calculator ICs

Device	Function	Package	Page
KS6025	Basic Function 8 Digits LCD Calculator	48 FQP	121
KS6026	Basic Function 8 Digits LCD Calculator with Internal Voltage Regulator	48 FQP	129
KS6027A	10/12 Digits Selectable Desk Top Calculator	Bare Chip	143
KS6027B	Basic Function 10 Digits LCD Calculator	60 FQP	151
KS6027C	10/12 Digits Basic Selectable Calculator 12 Digits Desk Top Calculator (3V operation)	60 FQP	156
KS6028	Basic Function 8 Digits LCD Calculator with Internal Voltage Regulator	48 FQP	161
KS6029	Basic Function 10 Digits LCD Calculator	48 FQP	171
KS6041	Scientific Function 10 Digits LCD Calculator	48 FQP	181

BASIC FUNCTION 8 DIGITS LCD CALCULATOR

The KS6025 is a single chip CMOS LSI with 8 digits arithmetic operation, single memory extraction-of-square-root, percentage calculation and auto power off functions, designed for FEM LCD operation with 1.5V power supply.

48 FQP



FUNCTIONS

- Four standard functions (+, −, ×, ÷).
- Auto constant calculations (constant: multiplicand, divisor, addend and subtrahend).
- Square and reciprocal calculations.
- Make-up and make-down calculations.
- Extraction of square root.
- Percentage calculations.

FEATURES

- **Single chip CMOS construction.**
- **Chain multiplication and division.**
- **Power calculations.**
- **Rough estimate calculations.**
- **Rollover capability.**
- **Floating decimal.**
- **LCD direct drive.**
- **Overflow indication: E.**
- **Accumulating memory: M+, M−, RM, CM, RM/CM.**
- **48 FQP and bare chip are available**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	Note
Terminal Voltage	V_{GG}	−0.3 ~ +2.1	V	1
	V_{IN}	−0.3 ~ V_{GG} + 0.3	V	
Supply Voltage	V_{GG}	1.1 ~ 1.7	V	
Resistance for CG	Rf	560±5%	KΩ	2
Operating Temperature	T_{opr}	0 ~ +50	°C	
Storage Temperature	T_{stg}	−55 ~ +125	°C	

Note 1. Maximum voltage on any pin is in with respect to GND.
Note 2. Resistor value for CG is varied according to the floating capacitance on a PWB.

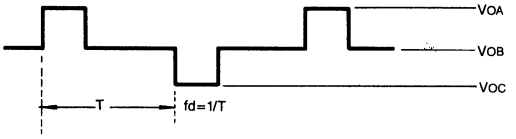
ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{GG} =1.5V unless otherwise specified)

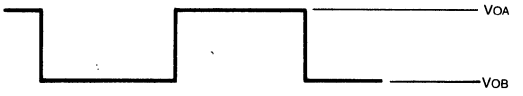
Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit	Note
Input Voltage 1	V_{IH1}			V_{GG}-0.4			V	3
	V_{IL1}				0.4	V		
Input Voltage 2	V_{IH2}			V_{GG}-0.4			V	4
	V_{IL2}					0.2	V	
Input Current 1	I_{IH1}	$V_{IN}=V_{GG}$				1	μA	5
	I_{IL1}	$V_{IN}=0V$		0.3	1	3	μA	
Input Current 2	I_{IH2}	$V_{IN}=V_{GG}$				1	μA	6
	I_{IL2}	$V_{IN}=0V$				1	μA	
Input Current 3	I_{IH3}	$V_{IN}=V_{GG}$	$S2=V_{GG}$			1	μA	4
	I_{IL3}	$V_{IN}=0V$		0.3	1	3	μA	
Input Current 4	I_{IH4}	$V_{IN}=V_{GG}$	$S2=V_{GG}$	3	12	25	μA	4
	I_{IL4}	$V_{IN}=0V$				1	μA	
Output Voltage	V_{OH1}	without load		V_{GG}-0.15			V	7
	V_{OL2}	$I_{out}=15\mu A$				0.15	V	
Output Voltage 2	V_{OA}	without load		2.80	2.95		V	8
	V_{OB}	without load		1.30	1.50	1.70	V	
	V_{OC}	without load			0	0.20	V	
Display Frequency	F_d	V_{GG} =1.3V while display is on, Rf=560K		55	67		Hz	8
Dissipation	I_{OFF}	display is off				0.8	μA	9
	I_{DIS}	V_{GG} =1.3V, while display is on			4.0	5.6	μA	10
	I_{OP}	V_{GG} = 1.2V, while operation			5.0	6.5	μA	11

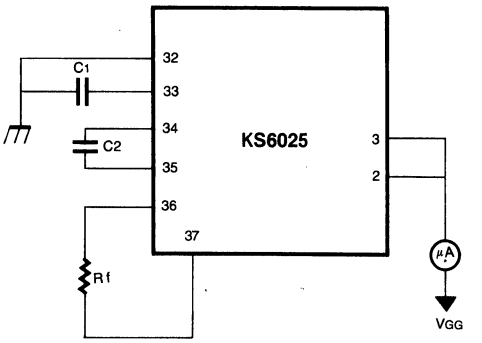
Note: 3. Applies to pin K2, K6 and S2.
4. Applies to pin S1.
5. Applies to pin K2 and K6.
6. Applies to pin S2.
7. Applies to P1, P2, A2 and A5.
8. Applies to H1, H3, a1, a8, b1, b8, c1 and c8.
9. Measured by the below test circuit after power supply automatically turns off.
10. Measured by the below test circuit while "0" is being displayed after auto-clear operation and while key is not being depressed.
11. Measured by the below test circuit while operation is being made by AC key and while key is not being depressed.

OUTPUT WAVEFORM 1



OUTPUT WAVEFORM 2





4

FUNCTIONAL DESCRICTION

- Decimal point system

Complete floating decimal point system.

- Integral number : 8 digits leading zero suppression. Zero shift.
- Symbols : – : negative number display.
  E : error display.
  M : memory display.

• Negative number indication

Antilogarithm : +
Minus : –

Error detections

System errors occur when:
1) The integral part of any calculation result exceeds 8 digits.
2) The integral part of any memory calculation result exceeds 8 digits.
   In addition, the integral part of any addend or subtrahend to memory exceeds 8 digits.
3) The integral part of a make-up and make-down calculation result exceeds 8 digits.
4) The division by zero.
5) The extraction of square root of a negative number.

• Rough estimate calculation error

When the integral part of the result of any standard functions, percentage, square, reciprocal, or power calculations exceeding 8 digits and is equal to 16 digits or less.

Error indication

System error

"0" is indicated in the 1 digit position and "E" in th sign-digit position.

Rough estimate calculation error

The high-order 8 digits calculation result is indicated together with "E."
The decimal point is indicated in the position corresponding to a calculation result of time 10^{-8}, and no zero shift is performed.

Error release

System error

A system error can be release by the AC or ON/CE key.

Rough estimate calculation error

A rough estimate calculation error can be released by the AC or ON/CE key.
A calculation result is not cleared by ON/CE key but is retained.

- **Nember entry**

Numericals can be entered up to 8 digits. Numerical entries equal to 9 digits or more are ignored.

- **Memory protection**

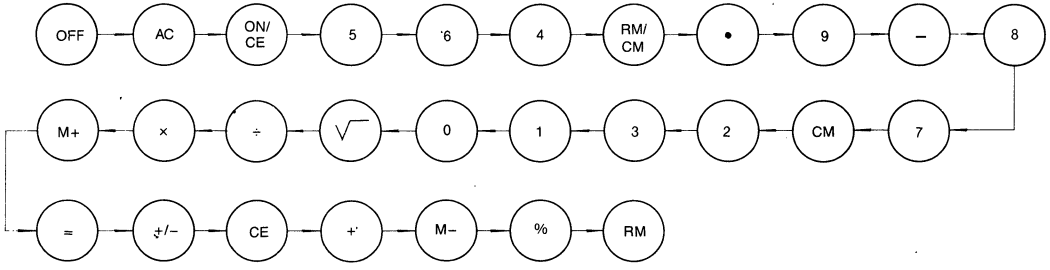
In any error detection, the memory contents present before the detection are protected.

- **Memory indication**

If the memory content is a number other then zero, "M" is indicated in the sign-digit position.

Doubler key depression

The order of the priority when two keys are being depressed simultaneously, is as follows:



When the OFF and AC key are depressed simultaneously, the OFF key is given priority.

- **Key bounce protection**

Front edge
Down to 1 word and up to about 3 words.

Trailling edge
9 words.
1 word is 3.3ms when display frequency is fd = 100Hz.

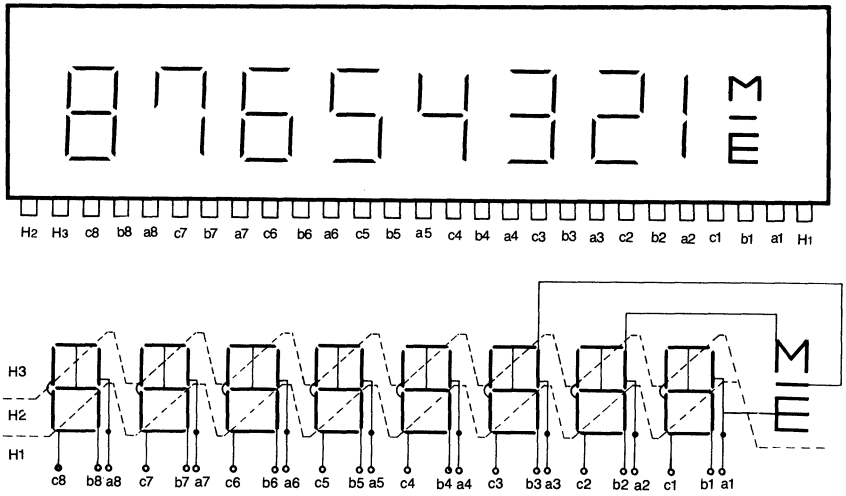
PIN ASSIGMENT

Pin No.	Signal	I/O	Description	Pin No.	Signal	I/O	Description
1	S1	I	TEST/ACL input	25	b7	O	Display output
2	S2	I	APO input	26	c7	O	Display output
3	V_{GG}		Power supply	27	a8	O	Display output
4	H1	O	Display output	28	b8	O	Display output
5	a1	O	Display output	29	c8	O	Display output
6	b1	O	Display output	30	H2	O	Display output
7	GND			31	H3	O	Display output
8	c1	O	Display output	32	GND		
9	a2	O	Display output	33	VC	O	Capacitor terminal for voltage set-up
10	b2	O	Display output	34	VA	O	Capacitor terminal for voltage set-up
11	c2	O	Display output	35	VB	O	Capacitor terminal for voltage set-up
12	a3	O	Display output	36	CG out	O	Resistor terminal for CG
13	b3	O	Display output	37	CG in	I	Capacitor terminal for voltage set-up
14	c3	O	Display output	38	K3	I	Key input
15	a4	O	Display output	39	K2	I	Key input
16	b4	O	Display output	40	A2	O	Strobe output
17	c4	O	Display output	41	A3	O	Strobe output
18	a5	O	Display output	42	A4	O	Strobe output
19	B5	O	Display output	43	A5	O	Strobe output
20	c5	O	Display output	44	P2	0	Strobe output
21	a6	O	Display output	45	P1	O	Strobe output
22	b6	O	Display output	46	K5	I	Key input
23	c6	O	Display output	47	K6	I	Key input
24	a7	O	Display output	48	K4	I	Key input

DISPLAY FONTS

- **Numericals font**

- **Sign font**



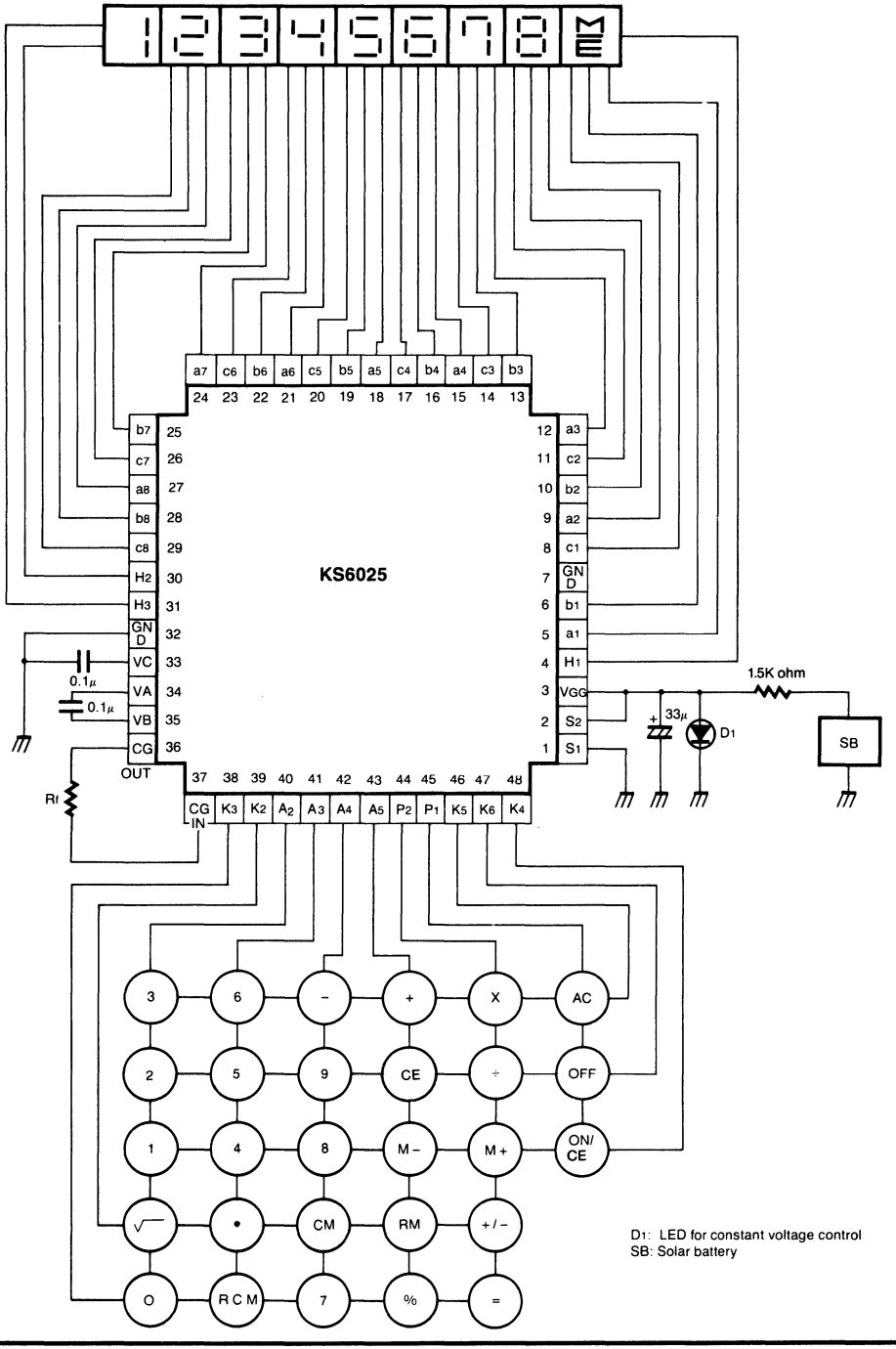
AUTO POWER OFF

Power automatically turns off after 9-11 minutes pass from the last key pressure.

- **AC key**

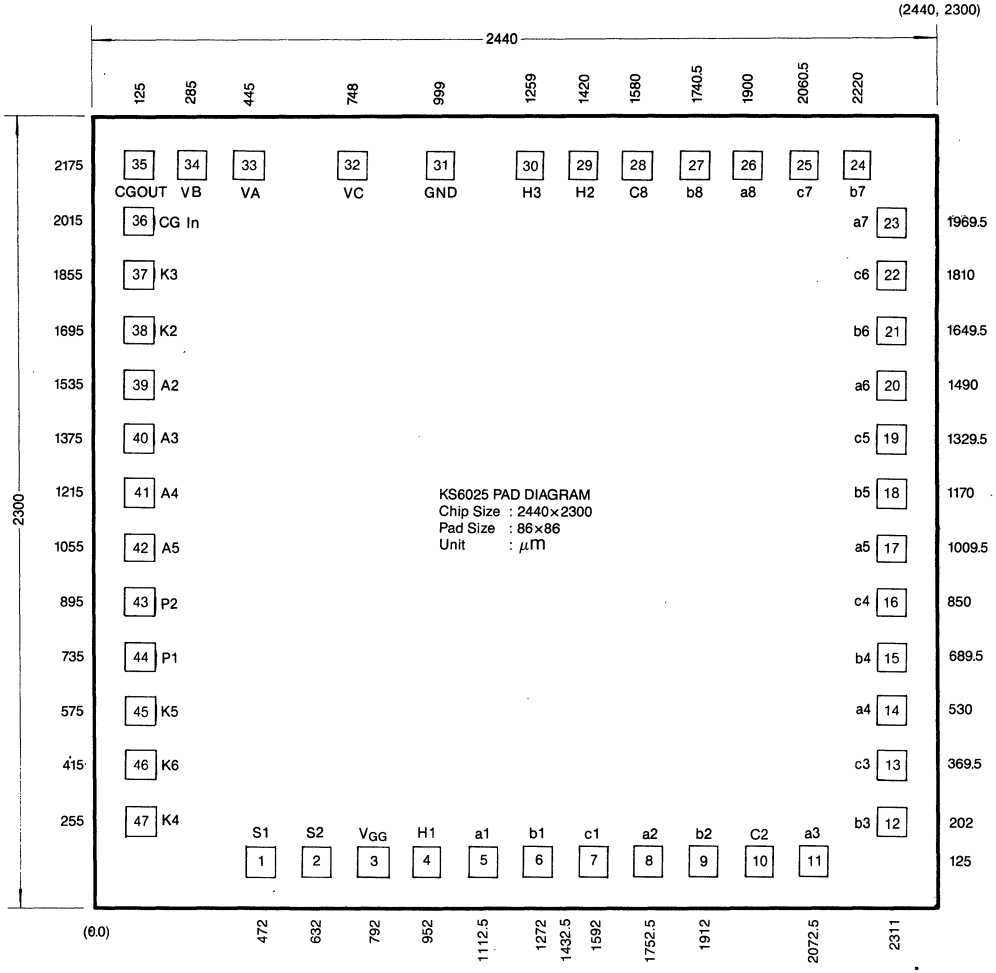
All operations except memory content are cleared by AC key.

APPLICATION CIRCUIT



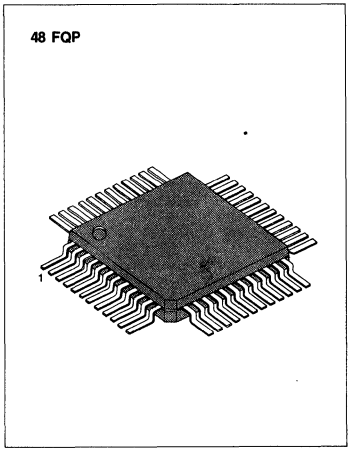
D1: LED for constant voltage control
SB: Solar battery

PAD DIAGRAM


(2440, 2300)
2440
2300
125
285
445
748
999
1259
1420
1580
1740.5
1900
2060.5
2220
2175
2015
1855
1695
1535
1375
1215
1055
895
735
575
415
255
35 CGOUT
34 VB
33 VA
32 VC
31 GND
30 H3
29 H2
28 C8
27 b8
26 a8
25 c7
24 b7
36 CG In
37 K3
38 K2
39 A2
40 A3
41 A4
42 A5
43 P2
44 P1
45 K5
46 K6
47 K4
23 a7
22 c6
21 b6
20 a6
19 c5
18 b5
17 a5
16 c4
15 b4
14 a4
13 c3
12 b3
11 a3
10 C2
9 b2
8 a2
7 c1
6 b1
5 a1
4 H1
3 VGG
2 S2
1 S1
1969.5
1810
1649.5
1490
1329.5
1170
1009.5
850
689.5
530
369.5
202
125
KS6025 PAD DIAGRAM
Chip Size : 2440×2300
Pad Size : 86×86
Unit : μm
(0.0)
472
632
792
952
1112.5
1272
1432.5
1592
1752.5
1912
2072.5
2311

BASIC FUNCTION 8 DIGITS LCD CALCULATOR WITH INTERNAL VOLTAGE REGULATOR

The KS6026 is a single chip CMOS LSI with 8 digits arithmetic operation, single memory, extraction-of-square-root, percentage calculation and auto power off functions, designed for FEM LCD operation with 1.5V power supply.



FUNCTIONS

- Four standard functions (+, −, ×, ÷).
- Auto constant calculations (constant: multiplicand, divisor, addend and subtrahend).
- Square and reciprocal calculations.
- Make-up and make-down calculations.
- Extraction of square root.
- Percentage calculations.

FEATURES

- **Single chip CMOS construction.**
- **Chain multiplication and division.**
- **Power calculations.**
- **Rough estimate calculations.**
- **Rollover capability.**
- **Floating decimal.**
- **LCD direct drive.**
- **Overflow indicacion: "E".**
- **Accumulating memory: M+, M−, RM, CM, RM/CM.**
- **On chip supply voltage limiter by bonding option.**
- **48 FQP and bare chip available.**

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	Note
Terminal Voltage	V_{GG}	−0.3 ~ 2.1	V	1
	V_{IN}	−0.3 ~ V_{GG} + 0.3	V	
Solar Supply Voltage	V_{sb}	1.7 ~ 3	V	2
	V_{GG} (lim)	1.2 ~ 1.8	V	3
Battery Supply Voltage	V_{GG}	1.1 ~ 1.7	V	
Resistance for CG	R_f	560 ± 5%	KΩ	4
Operating Temperature	T_{opr}	0 ~ +50	°C	
Storage Temperature	T_{stg}	−55 ~ +150	°C	

Note 1. Maximum voltage on any pin is in with respect to GND.
2. V_{sb} is solar supply voltage
3. V_{GG} (lim) is limited voltage
4. Resistor value for CG varies according to the floating capacitance on a PWB

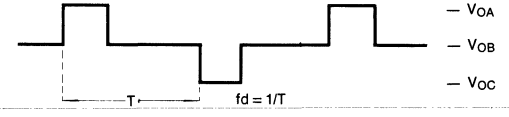
ELECTRICAL CHARACTERISTICS

($Ta = 25°C$, $V_{GG} = 1.5V$, unless otherwise specified)

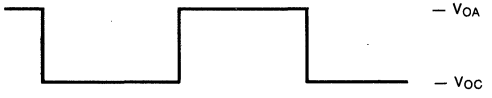
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Input Voltage 1	V_{IH1}		V_{GG}-0.4			V	5
	V_{IL1}				0.4	V	
Input Current 1	I_{IH1}	$V_{IN} = V_{GG}$			1	μA	6
	I_{IL1}	$V_{IN} = 0V$	0.3	1	3	μA	
Output Voltage 1	V_{OH1}	without load	V_{GG}-0.15			V	7
	V_{OL2}	$I_{out} = 15\mu A$			0.15	V	
Output Voltage 2	V_{OA}	without load	2.80	2.95		V	8
	V_{OB}	without load	1.30	1.50	1.70	V	
	V_{OC}	without load		0	0.20	V	
Display Frequency	F_d	$V_{GG} = 1.3V$ while display is on, $R_f = 560Kohm$	55	67		Hz	8
Dissipation	I_{off}	display is off			0.8	μA	9
	I_{dis}	$V_{GG} = 1.3V$, while display is on		4.2	6	μA	10
	I_{op}	$V_{GG} = 1.2V$, while operation		5.6	9	μA	11

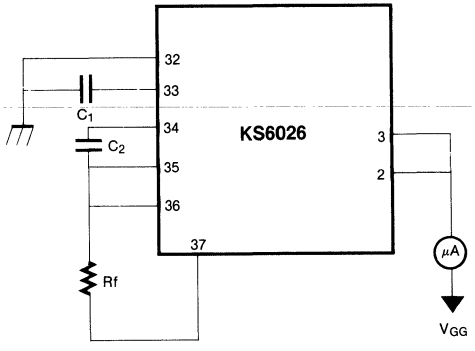
Note 5. Applies to pin K2, K6.
6. Applies to pin K2, and K6.
7. Applies to P1, P2, A2 and A5.
8. Applies to H1, H3, a1, a8, b1, b8, c1 and c8.
9. Measured by the below test circuit after power supply automatically turns off.
10. Measured by the below test circuit while "O" is being displayed after auto-clear operation and while key is not being depressed.
11. Measured by the below test circuit while operation is being made by AC key and while key is free from depression.

OUTPUT WAVEFORM 1



OUTPUT WAVEFORM 2





FUNCTIONAL DESCRIPTION

- Decimal point system

  Complete floating decimal point system.

- Integral number: 8 digits leading zero suppression. Zero shift.

- Symbols: —: negative number display.
  E : error display.
  M : memory display.

• Negative number indication

Antilogarithm: +
Minus : –

Error detections

System errors occur when:
1) The integral part of any calculation result exceeds 8 digits.
2) The integral part of any memory calculation result exceeds 8 digits.
   In addition, the integral part of any addend or subtrahend to memory exceeds 8 digits.
3) The integral part of a make-up and make-down calculation result exceeds 8 digits.
4) The division by zero.
5) The extraction of square root of a negative number.

• Rough estimate calculation error

The integral part of the result of any one of standard for functions, percentage, square, reciprocal, and power calculations exceeds 8 digits and is equal to 16 digits or less.

Error indication

System error

"0" is indicated in the 1 digit position and "E" in the sign-digit position.

Rough estimate calculation error

The high-order 8 digits of a calculation result is indicated together with "E".
The decimal point is indicated in the position corresponding to a calculation result time 10^{-8}, and no zero shift is performed.

Error release

System error

A system error can be release by the AC or ON/C, CE key.

Rough estimate calculation error

A rough estimate calculation error can be released by the AC or ON/C, CE key.
A calculation result is not cleared by ON/C, CE key but is retained.

• Number entry

Numericals can be entered up to 8 digits. Numerical enteries equal to 9 digits or more are ignored.

- **Memory protection**

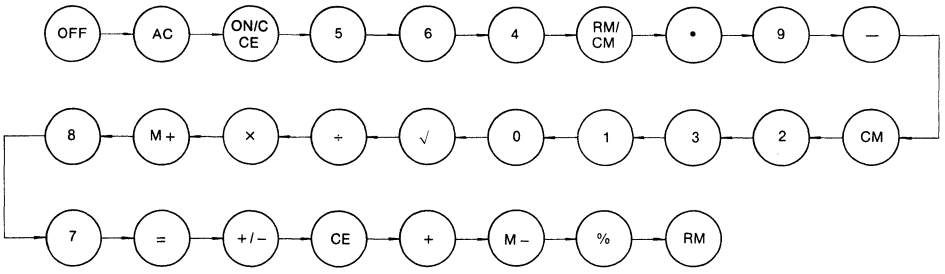
  In any error detection, the memory counters present before the error detection are protected.

- **Memory indication**

  If the memory counters are a number other then zero, "M" is indicated in the sign-digit position.

- **Doubler key depression**

  The order of the priority when two keys are being depressed simultaneously, is regarded as follows:



When the OFF and AC key are depressed simultaneously, the OFF key is given priority.

- **Key bounce protection**

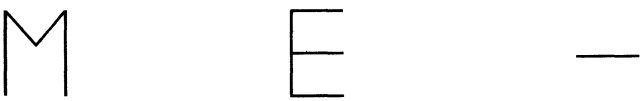
Front edge
Down to 1 word and up to about 3 words.

Trailling edge
9 words.
1 word 3.3ms when display frequency fd = 100Hz.

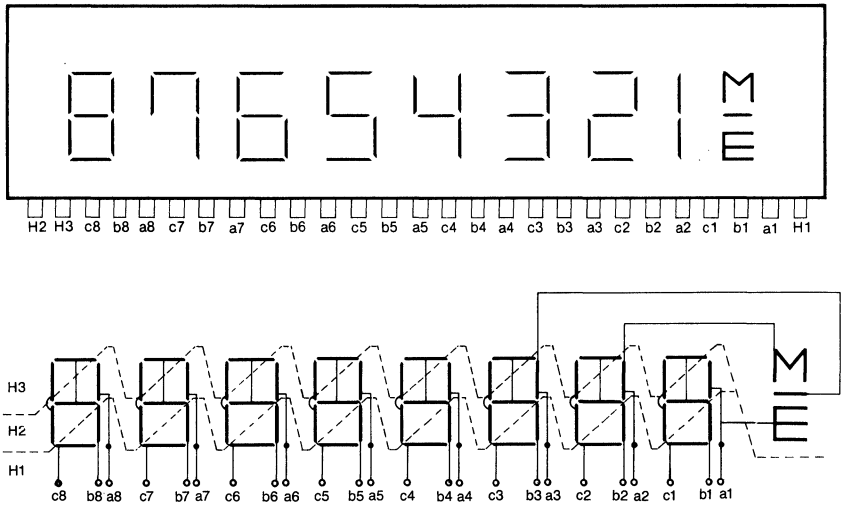
DISPLAY FONTS

- **Numericals font**

- **Sign font**



- **LCD connector**



AUTO POWER OFF

Power automatically turns off a after 9-11 minutes pass from the last key pressure.

- **AC key**

All operation including memory contents are cleared by AC key.

- **Make-up and make-down calculation**

Make-up and make-down calculation are performed as followes.

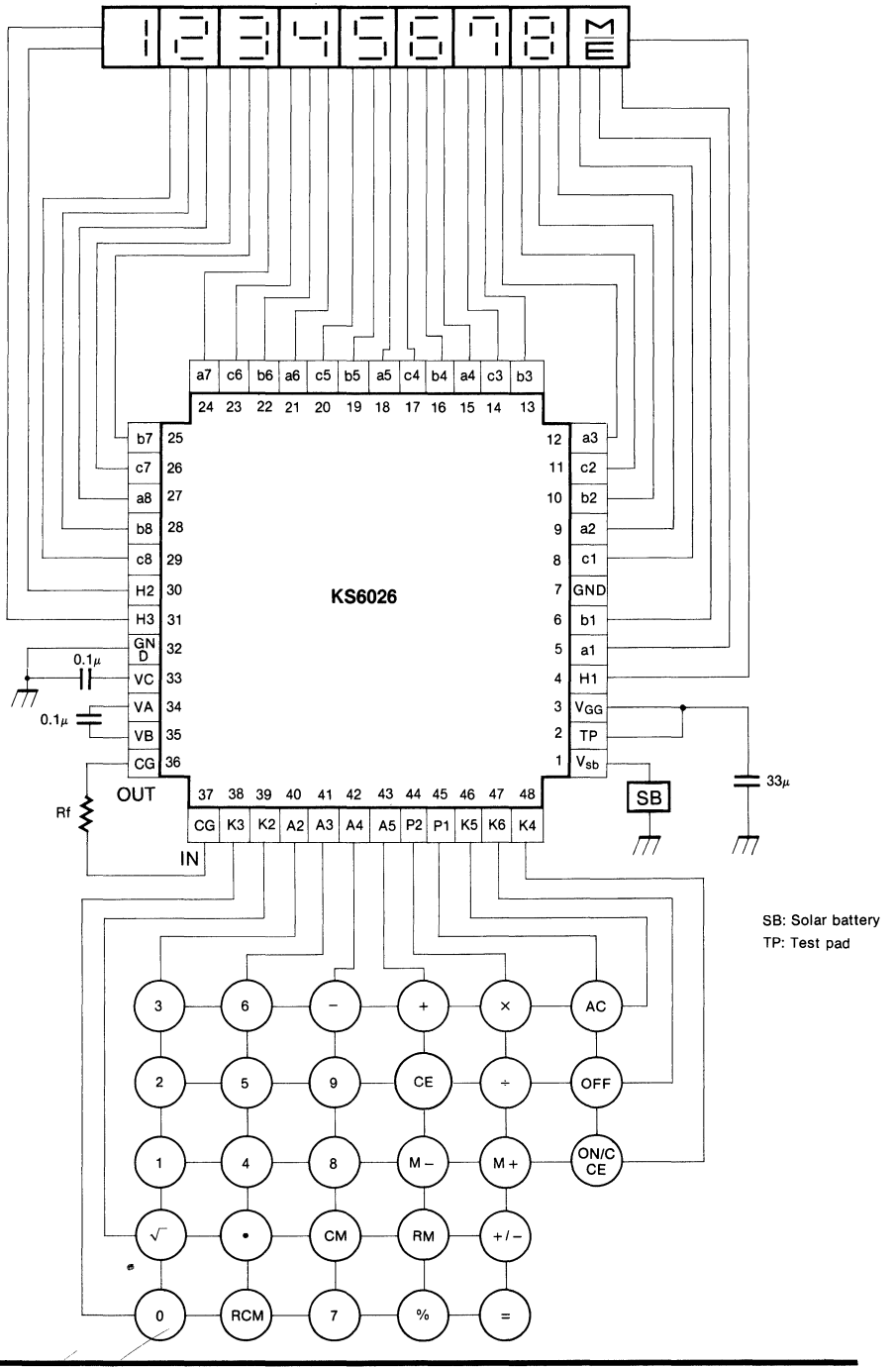
ENTRY		DISPLAY	
A	A	A	A
+	×	A	A
B	B	B	B
%	%	A + AM/100	AM/100
	+ OR −		AM/100
	=		A + AM/100 OR A − AM/100

* AM: AMOUNT

PIN ASSIGNMENT

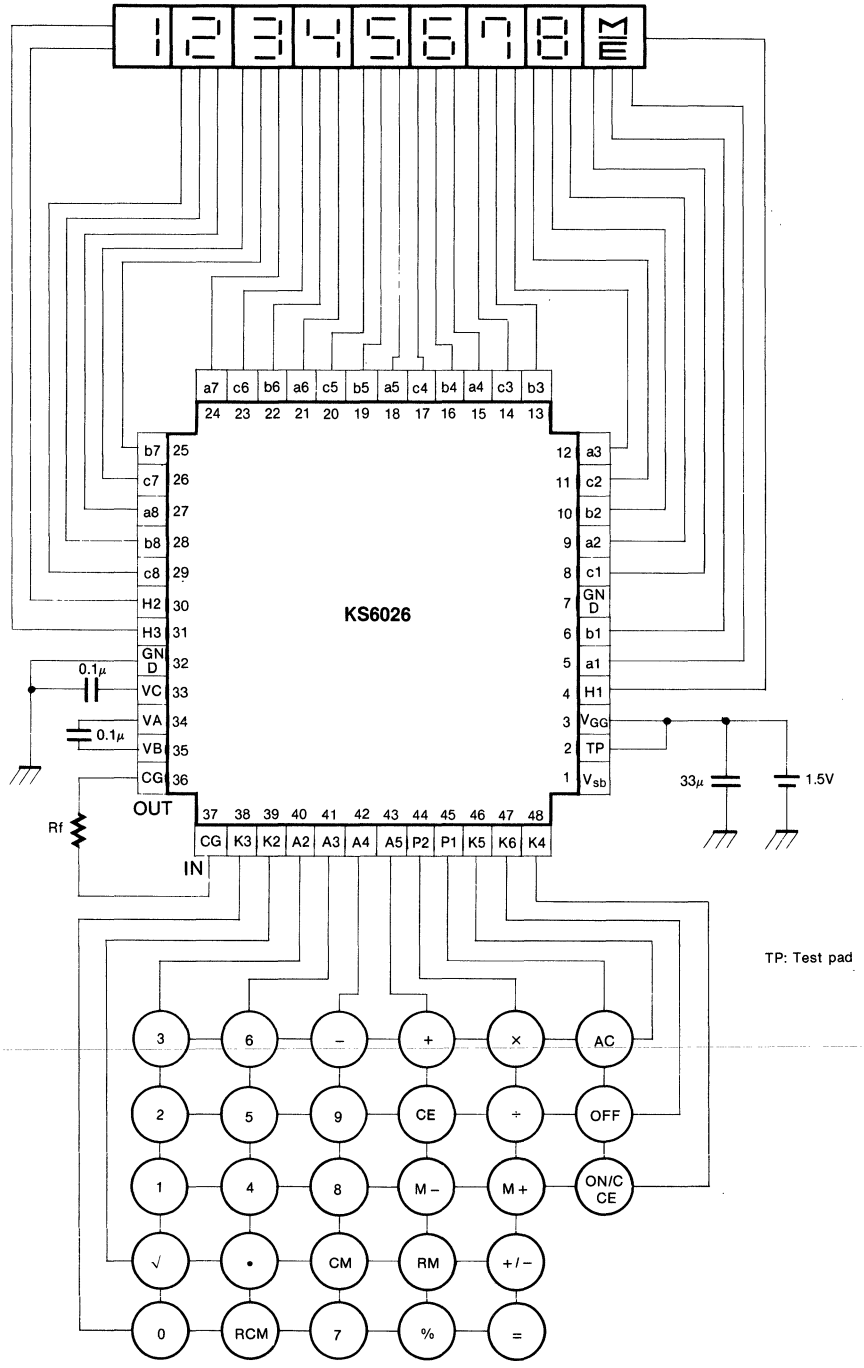
Pin No.	Signal	I/O	Description	Pin No.	Signal	I/O	Description
1	V_{sb}	I	Solar Battery	25	b7	O	Display Output
2	V_{op}	I	Option Pin	26	c7	O	Display Output
3	V_{GG}		Power Supply	27	a8	O	Display Output
4	H1	O	Display Output	28	b8	O	Display Output
5	a1	O	Display Output	29	c8	O	Display Output
6	b1	O	Display Output	30	H2	O	Display Output
7	GND			31	H3	O	Display Output
8	c1	O	Display Output	32	GND		
9	a2	O	Display Output	33	VC	O	Capacitor Terminal for Voltage Set-up
10	b2	O	Display Output	34	VA	O	Capacitor Terminal for Voltage Set-up
11	c2	O	Display Output	35	VB	O	Capacitor Terminal for Voltage Set-up
12	a3	O	Display Output	36	CG Out	O	Resistor Terminal for CG
13	b3	O	Display Output	37	CG In	I	Resistor Terminal for CG
14	c3	O	Display Output	38	K3	I	Key Input
15	a4	O	Display Output	39	K2	I	Key Input
16	b4	O	Display Output	40	A2	O	Strobe Output
17	c4	O	Display Output	41	A3	O	Strobe Output
18	a5	O	Display Output	42	A4	O	Strobe Output
19	b5	O	Display Output	43	A5	O	Strobe Output
20	c5	O	Display Output	44	P2	O	Strobe Output
21	a6	O	Display Output	45	P1	O	Strobe Output
22	b6	O	Display Output	46	K5	I	Key Input
23	c6	O	Display Output	47	K6	I	Key Input
24	a7	O	Display Output	48	K4	I	Key Input

APPLICATION CIRCUIT (for use with a solar cell)



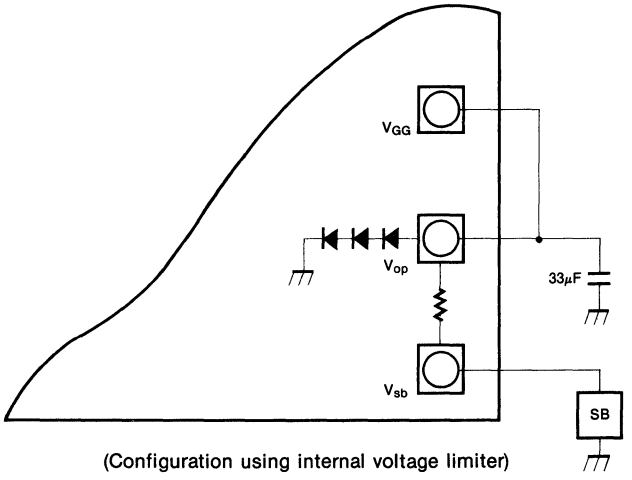
SB: Solar battery
TP: Test pad

APPLICATION CIRCUIT (for use with a battery)



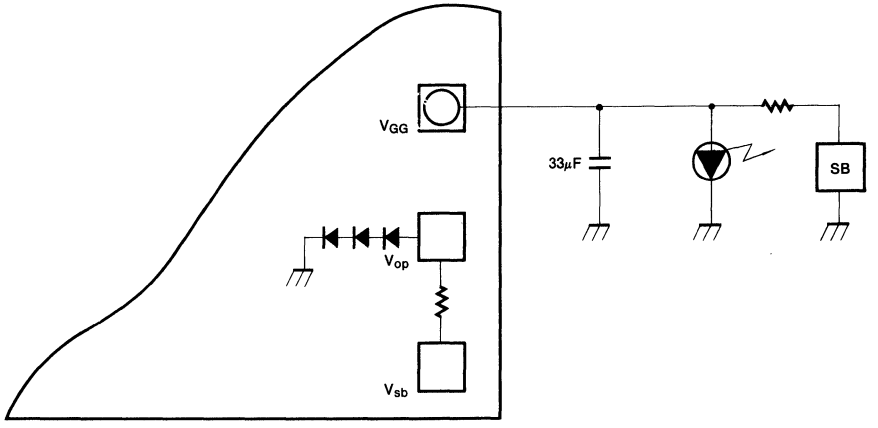
INTERNAL VOLTAGE LIMITER BONDING OPTION METHOD

OPTION 1



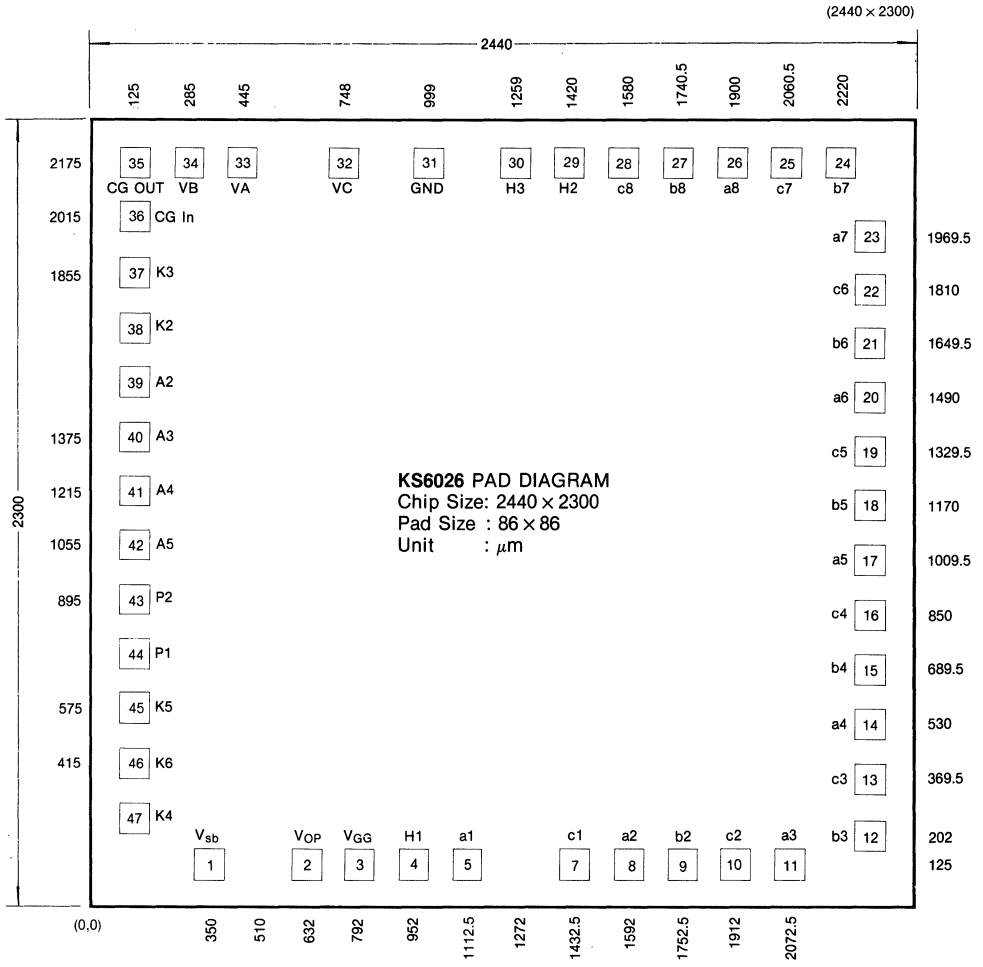
(Configuration using internal voltage limiter)

OPTION 2



(Configuration using external voltage limiter)

PAD DIAGRAM


(2440 × 2300)
2440
2300
(0,0)
KS6026 PAD DIAGRAM
Chip Size: 2440 × 2300
Pad Size : 86 × 86
Unit : μm
35 CG OUT
34 VB
33 VA
32 VC
31 GND
30 H3
29 H2
28 c8
27 b8
26 a8
25 c7
24 b7
36 CG In
37 K3
38 K2
39 A2
40 A3
41 A4
42 A5
43 P2
44 P1
45 K5
46 K6
47 K4
1 Vsb
2 VOP
3 VGG
4 H1
5 a1
7 c1
8 a2
9 b2
10 c2
11 a3
12 b3
13 a3
14 a4
15 b4
16 c4
17 a5
18 b5
19 c5
20 a6
21 b6
22 c6
23 a7

10/12 Digits Multi Type Calculator

KS6027 is distributed to multi type calculator by the user's bonding option. KS6027 can drive the liquid crystal display (LCD) with single power supply. Single power supply operation, wide operating voltage range and low power consumption make it suitable for 1.5V solar battery or 1.5V battery or 3V battery operated calculator.

1. KS6027A—10/12 digits selectable desk top/basic calculator (Bare Chip)
2. KS6027B—10 digits basic calculator (60 FQP)
3. KS6027C—10/12 digits basic selectable calculator (60 FQP)
   12 digits desk top calculator (60 FQP)

FEATURES

- **Complementary output buffer for direct driving of liquid crystal display**
- **Oscillator/clock generator internal to chip**
- **Key board encoding internal to chip**
- **Key board debouncing internal to chip**
- **Wide supply voltage range (1.2V – 2.0V)**
- **Very lower power consumption (7μW TYP)**

ELECTRICAL CHARACTERISTICS

(1) Absolute maximum ratings

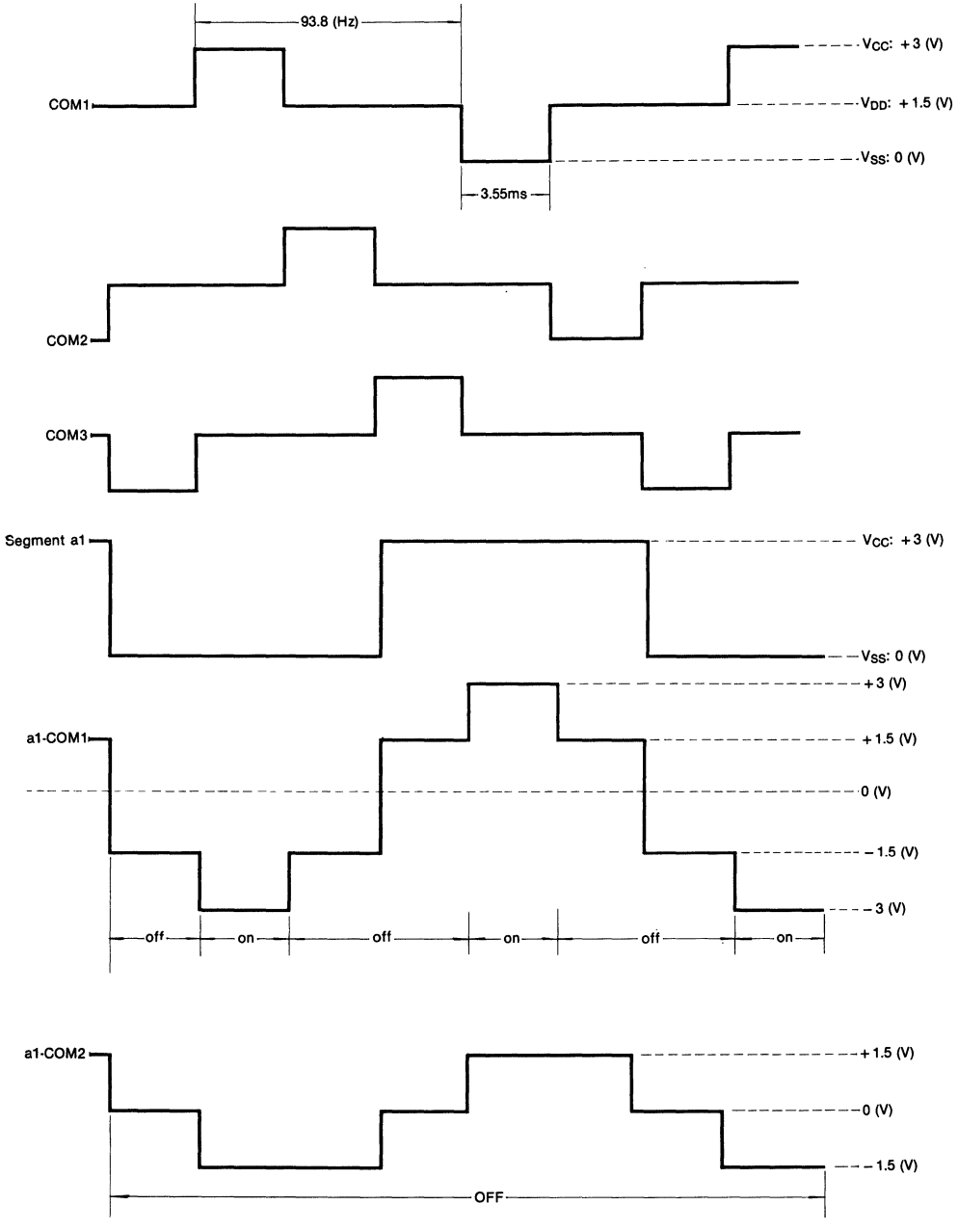
Characteristic	Symbol	Value	Unit
Terminal Voltage	V_{DD}	$-0.3 \sim +2.0$	V
	V_{IN}	$-0.3 \sim V_{DD}-0.3$	V
Operating Temperature	T_{opr}	$0 \sim +40$	°C
Storage Temperature	T_{stg}	$-55 \sim +125$	°C

(2) Electrical characteristics

($V_{DD} = +1.5V$ ($\pm 0.2V$), $V_{CC} = +3V$ ($\pm 0.4V$), $V_{SS} = 0V$, $Ta = 25°C$)

Characteristic	Pin Name	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	—	—		1.2	1.5	2.0	V
Supply Current	—	I_{dis}	$V_{DD} = 1.5V$ Stand-by	—	4.4	6.5	μA
		I_{opr}	$V_{DD} = 1.5V$ Operating	—	7.0	15	
OSC Frequency	—	F_{dis}	$V_{DD} = 1.5V$ Stand-by	5.4	9.0	12.6	KHz
		F_{opr}	$V_{DD} = 1.5V$ Operating	28.8	48	67.2	
Frame Frequency	—	F_f	$V_{DD} = 1.5V$ Stand-by	56.3	93.8	131	Hz
High Input Voltage	K3-K10	V_{IH} (1)	—	$V_{DD}-0.4$	—	V_{DD}	V
	K11-K12	V_{IH} (2)	—	$V_{CC}-0.4$	—	V_{CC}	
Low Input Voltage	KI	V_{IL} (1)	—	V_{SS}	—	0.4	V
	K3-K12	V_{IL} (2)					
High Output Voltage	K1-K8	V_{OH}	—	$V_{DD}-0.2$	—	V_{DD}	V
Low Output Voltage	K1-K8	V_{OL}	—	V_{SS}	—	0.2	V
Key Pull Down Res.	KI	R_{pd1}	$V_{out} = 0.3V$	0.5	1	1.5	KΩ
	K1-K10	R_{pd2}		10	17	28	
Key Pull Up Res.	KI	R_{pu1}	$V_{out} = 1.2V$	145	170	195	KΩ
	K1-K10	R_{pu2}		0.6	1.2	1.9	
	K11-K14	R_{pu3}	$V_{out} = 2.7V$	250	400	550	
High Output Voltage	LCD, COM	V_{OH}	—	$V_{CC}-0.2$	—	V_{CC}	V
"M" Output Voltage	LCD, COM	V_{OM}	—	$V_{DD}-0.2$	—	V_{DD}	V
Low Output Voltage	LCD, COM	V_{OL}	—	V_{SS}	—	0.2	V

WAVE FORMS FOR DISPLAY



PAD DESCRIPTION

PAD No.	Name	I/O	Description	PAD No.	Name	I/O	Description
1	COM1	0	Common Signal 1	36	B10	0	LCD
2	COM2	0	Common Signal 2	37	C10	0	LCD
3	COM3	0	Common Signal 3	38	A11	0	LCD
4	A0 (K)	0	LCD	39	B11	0	LCD
5	BO (K)	0	LCD	40	C11	0	LCD
6	CO	0	LCD	41	A12	0	LCD
7	A1 (K)	0	LCD	42	B12	0	LCD
8	B1 (K)	0	LCD	43	VSS		Solar Cell (−)
9	FDDIS	I	*	44	V_A		**
10	C1 (K)	0	LCD	45	V_B		**
11	A2 (K)	0	LCD	46	V_{CC}		**
12	B2 (K)	0	LCD	47	V_{DD}		+1.5V Power
13	C2	0	LCD	48	V_{DD}		Solar Cell (+)
14	A3	0	LCD	49	EXTNL	I	External Clock
15	B3	0	LCD	50	FODIS	I	Fosc Disable
16	C3	0	LCD	51	KI	I/O	ON Key
17	A4	0	LCD	52	K1	0	Key Input 1
18	B4	0	LCD	53	K2	0	Key Input 2
19	C4	0	LCD	54	K3	I/O	Key Input 3
20	A5	0	LCD	55	K4	I/O	Key Input 4
21	B5	0	LCD	56	K5	I/O	Key Input 5
22	C5	0	LCD	57	K6	I/O	Key Input 6
23	A6	0	LCD	58	K7	I/O	Key Input 7
24	B6	0	LCD	59	K8	I/O	Key Input 8
25	C6	0	LCD	60	K9	I	Key Input 9
26	A7	0	LCD	61	K10	I	Key Input 10
27	B7	0	LCD	62	K11	I	Key Input 11
28	C7	0	LCD	63	K12	I	Key Input 12
29	A8	0	LCD	64	K13		No Connection
30	B8	0	LCD	65	K14		No Connection
31	C8	0	LCD				
32	A9	0	LCD				
33	B9	0	LCD				
34	C9	0	LCD				
35	A10	0	LCD				

* Frequency Doubler Disable
** Capacitor Terminal for Voltage Doubling

1. KS6027A

Desk Top 10 or 12 digits selectable LCD calculator. KS6027A is either 10 digits capacity 2-memory or 12 digits capacity 2-memory electronic calculator on one chip CMOS/LSI.

KS6027A can drive the liquid crystal display (LCD) with single power supply. Single power supply operation, wide operating voltage range and low power consumption make it suitable for 1.5V solar battery operated calculator.

FUNCTION

- Display
  12 digits or 10-digits (selectable with PCB option) of data, 2 digits of sign, error symbol, memory load symbol, constant calculation mode symbol, operation symbol.
- Standard 4 functions
- Memory and grand total (GT) memory calculation
- Automatic percentage operation with add on, discount
- Square root
- Constant calculation
- Chain calculation
- Change sign
- Floating point or momentary mode (selectable with a switch)
- Fixed point ("0", "2", "3", "4")
- Adding point mode
- Registration overflow, indicating that too many digits are entered (the most significant digits are protected).
- Result overflow, indicating during calculation (most function key are locked as it happended).
- Rounding switches (rounding up, down and off)
- Leading zero suppression
- Trailing zero suppression
- Punctuation on display; Commas for thousand.
- Memory and GT memory contents indicator, turn on with non-zero in the memory and GT memory.

BASIC SPECIFICATION

1. Fixed point calculations

1)

Key	Display	Fixed point place
C	0.	DP = 3 (5/4)
3	3.	
÷	3.	
7	7.	
=	0.429	
4	4.	
.	4.	
5	4.5	
1	4.51	
+	4.51	
2	2.	
M+	6.510	
1	1.	
.	1.	
9	1.9	
M+	1.900	
MR	8.410	
MC	8.410	
MR	0.	

2)

Key	Display	Fixed point place
C	0.	DP = 2 (UP)
9	9.	
√	3.	
×	3.	
7	7.	
.	7.	
2	7.2	
3	7.23	
4	7.234	
=	21.71	
5	5.	
+	5.	
1	1.	
.	1.	
6	1.6	
=	6.60	
7	7.	
÷	7.	
4	4.	DP = 0
=	2.	

3)

Key	Display	Fixed point place
C	0.	DP = 0 (CUT)
3	3.	
.	3.	
1	3.1	
×	3.1	
6	6.	
.	6.	
4	6.4	
=	19.	
2	2.	
.	2.	
5	2.5	
+	2.5	
8	8.	DP = 2
=	10.50	
4	4.	
√	2.	
×	2.	
7	7.	
.	7.	
3	7.3	
=	14.6	DP = F

2. Adding point mode calculations

Key	Display	Key	Display
C	0.	1	4.1
4	4	2	4.12
3	43	3	4.123
2	432	M+	4.12
+	4.32	MR	4.18
5	5.	C	0.
=	4.37	9	9.
1	1.	5	95.
2	12.	2	952.
×	12.	−	9.52
3	3.	3	3.
.	3.	.	3.
7	3.7	6	3.6
8	3.78	7	3.67
9	3.789	=	5.85
=	45.46	4	4.
6	6.	+	0.04
M+	0.06	3	3.
4	4.	.	3.
.	4.	=	3.04

3. Constant calculation

1) Multiplication

Key	Display	Constant
k	k	
×	k	
×	k	
a	a	
=	k·a	k ×
b	b	k ×
=	k·b	k ×

2) Division

Key	Display	Constant
k	k	
÷	k	
÷	k	
a	a	
=	a/k	÷ k
b	b	÷ k
=	b/k	÷ k

3) Addition

k	k	
+	k	
+	k	
a	a	
=	a + k	+ k
b	b	+ k
=	b + k	+ k

4) Subtraction

k	k	
−	k	
−	k	
a	a	
=	a − k	− k
b	b	− k
=	b − k	− k

5) Percentage

k	k	
×	k	
×	k	
a	a	
%	k·a/100	k ×
b	b	k ×
%	k·b/100	k ×

6) Percentage

k	k	
÷	k	
÷	k	
a	a	
%	100·a/k	÷ k
b		÷ k
%	100·b/k	÷ k

4. Add-on, discount calculations

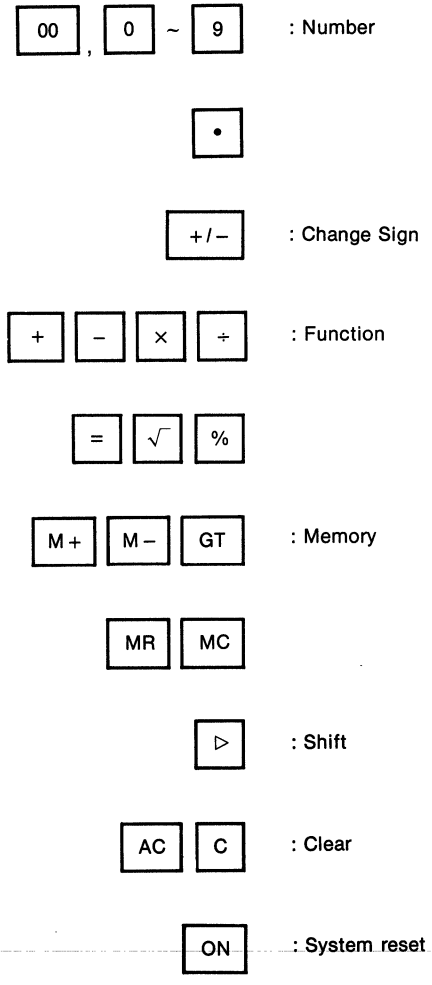
1) Add-on

Key	Display
a	a
×	a
b	b
%	a·b/100
+	a(1 + b/100)

2) Discount

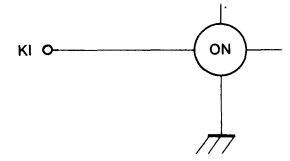
Key	Display
a	a
×	a
b	b
%	a·b/100
−	a(1 − b/100)

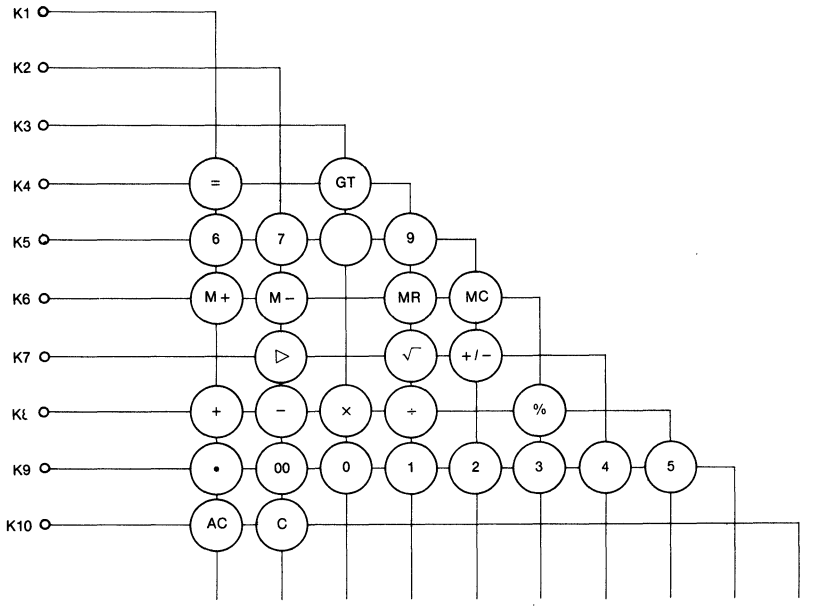
TOUCH KEY CONSTITUTION AND OPERATION



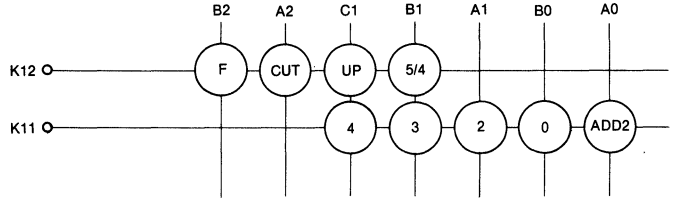
KEY CONSTITUTION AND OPERATION

1. Key Board





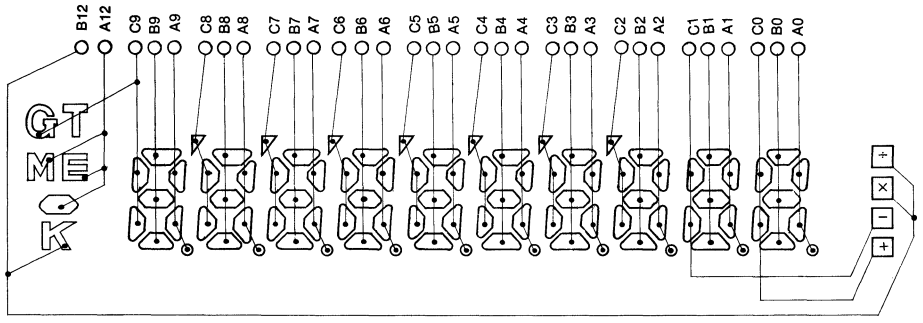
2. Switch



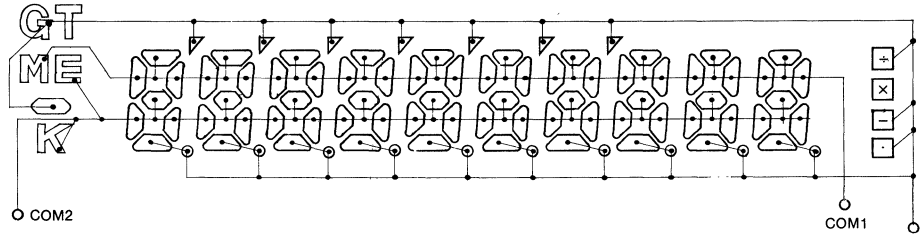
K11: Selectable with fixed point.
* K12: Rounding switches for mode select.

LCD CONNECTION

1. 10 Digits Desk Top

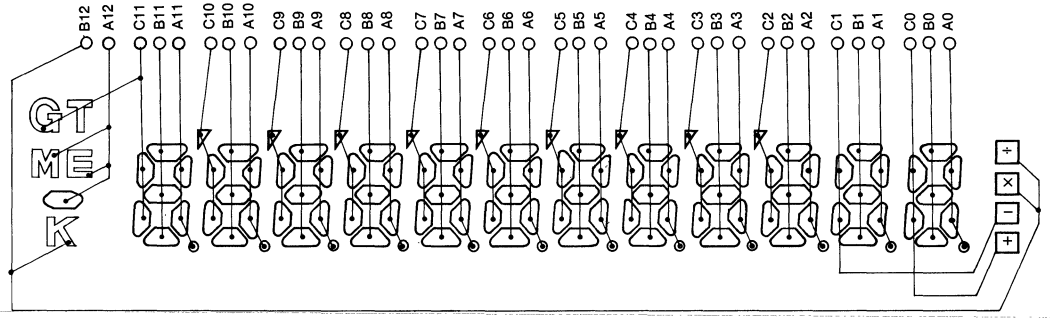


2) Common

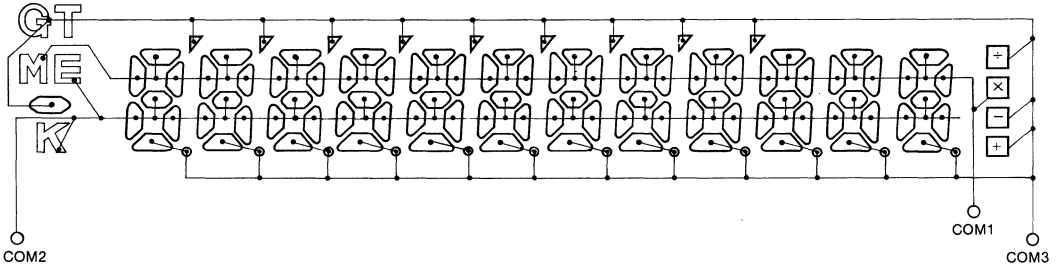


2. 12 Digits Desk Top

1) Segment

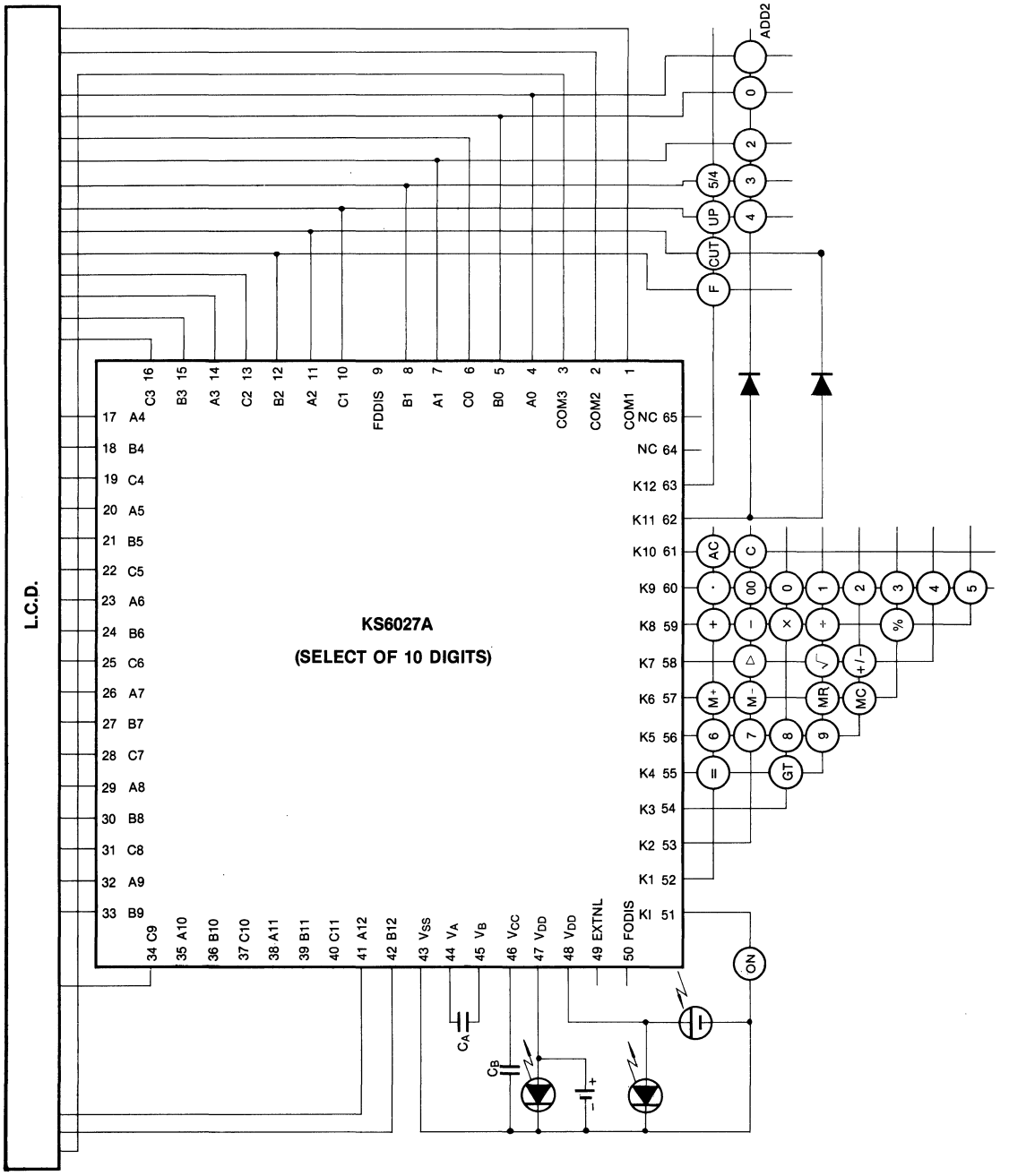


2) Common



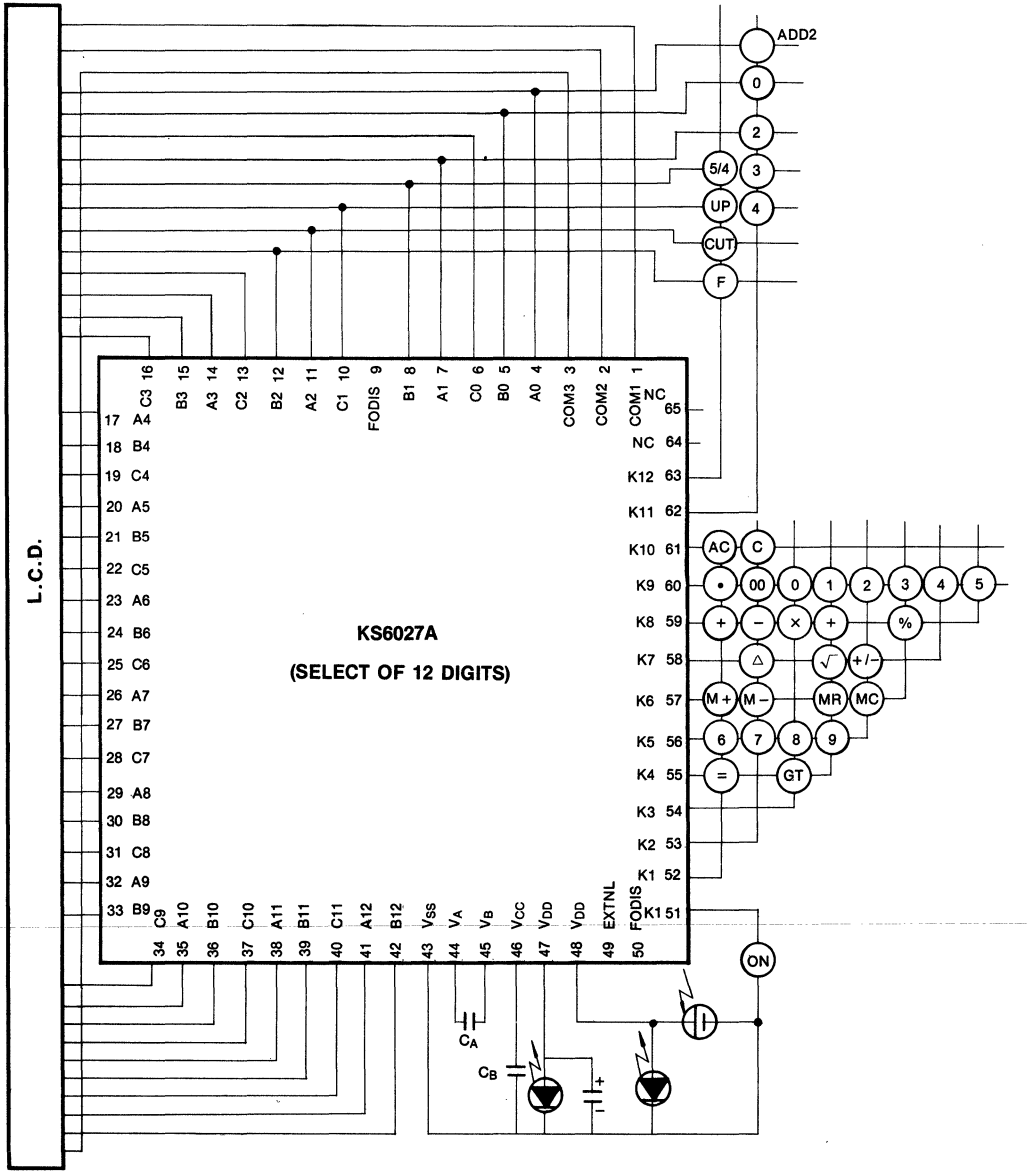
APPLICATION CIRCUIT

1. Select of 10 Digits



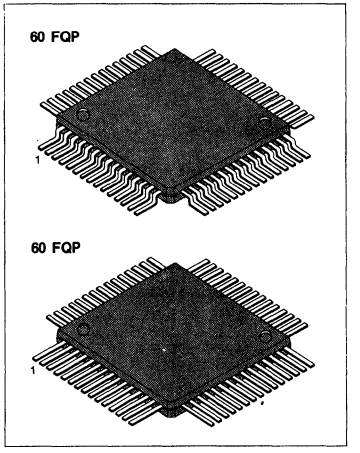
APPLICATION CIRCUIT

2. Select of 12 Digits



2. KS6027B

The KS6027B is a 60 FQP package type of KS6027A, and is used 10 digits basic calculator. It is possible to use 1.5V solar cell as well as battery as shown the application circuit.



FUNCTION

- Display
  10 digits of data, 2 digits of sign, error symbol, memory load symbol, constant calculation mode symbol, operation symbol.
- Standard 4 functions
- Memory and grand total (GT) memory calculation
- Automatic percentage operation with add on, discount
  Square root
- Constant calculation
- Change sign
- Chain calculation
- Registraction overflow, indicating that too many digits are entered (the most significant digits are protected)
- Result overflow, indicating during calculation (most function key are locked as it happended).
- Leading zero suppression
- Trailing zero suppression
- Punctuation on display; Commas for thousand.
- Memory and GT memory contents indicator, turn on with non-zero in the memory and GT memory.

BASIC SPECIFICATION

1. Constant calculation

1) Multiplication

Key	Display	Constant
k	k	
×	k	
×	k·	
a	a	
=	k·a	k ×
b	b	k ×
=	k·b	k ×

2) Division

Key	Display	Constant
k	k	
÷	k	
÷	k	
a	a	
=	a/k	÷ k
b	b	÷ k
=	b/k	÷ k

3) Addition

k	k	
+	k	
+	k	
a	a	
=	a + k	+ k
b	b	+ k
=	b + k	+ k

4) Subtraction

k	k	
−	k	
−	k	
a	a	
=	a − k	− k
b	b	− k
=	b − k	− k

5) Percentage

k	k	
×	k	
×	k	
a	a	
%	k·a/100	k ×
b	b	k ×
%	k·b/100	k ×

6) Percentage

k	k	
÷	k	
÷	k	
a	a	
%	100·a/k	÷ k
b		÷ k
%	100·b/k	÷ k

2. Add-on, discount calculations

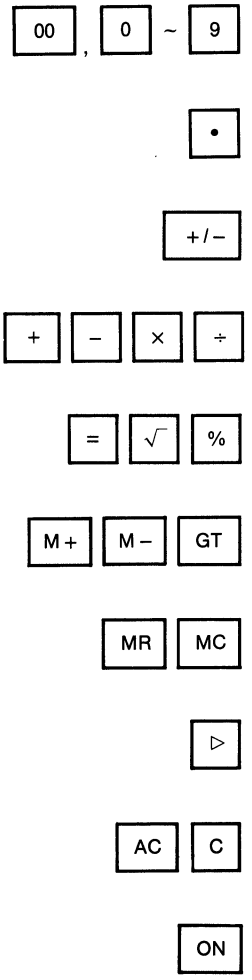
1) Add-on

Key	Display
a	a
×	a
b	b
%	a·b/100
+	a(1 + b/100)

2) Discount

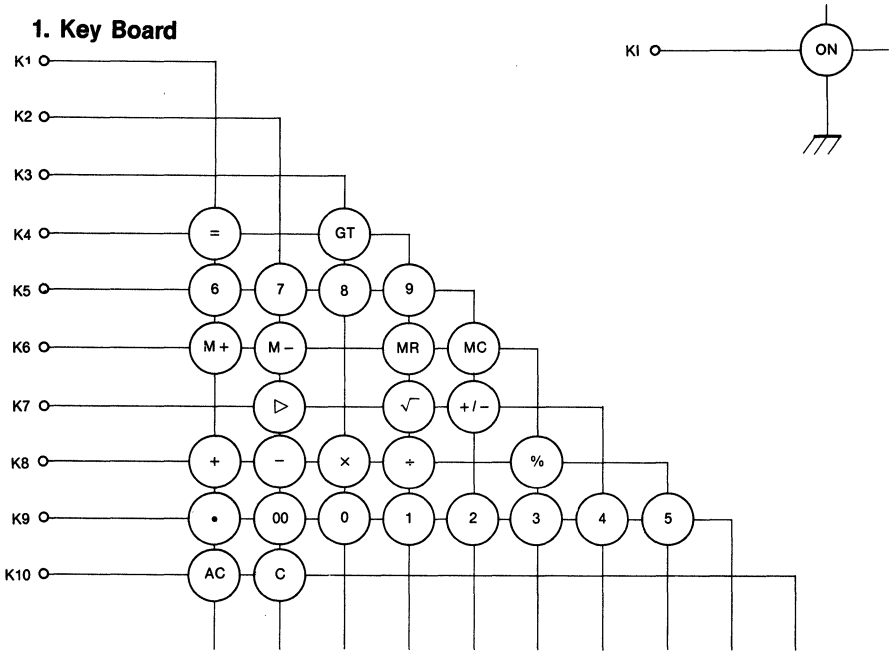
Key	Display
a	a
×	a
b	b
%	a·b/100
−	a(1 − b/100)

TOUCH KEY CONSTITUTION AND OPERATION



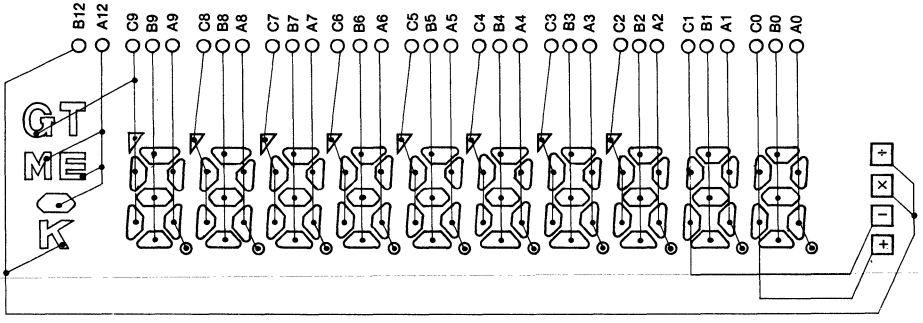
KEY CONSTITUTION AND OPERATION

1. Key Board

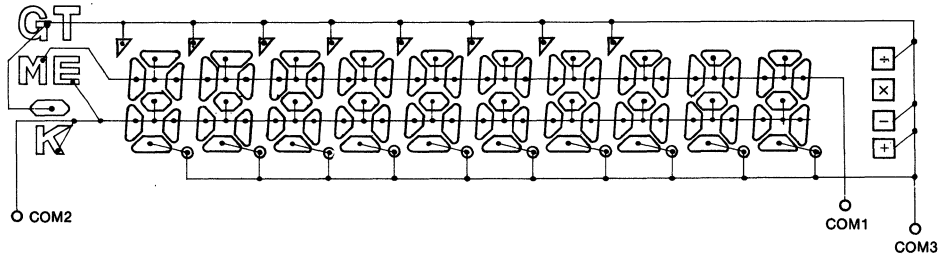


LCD CONNECTION

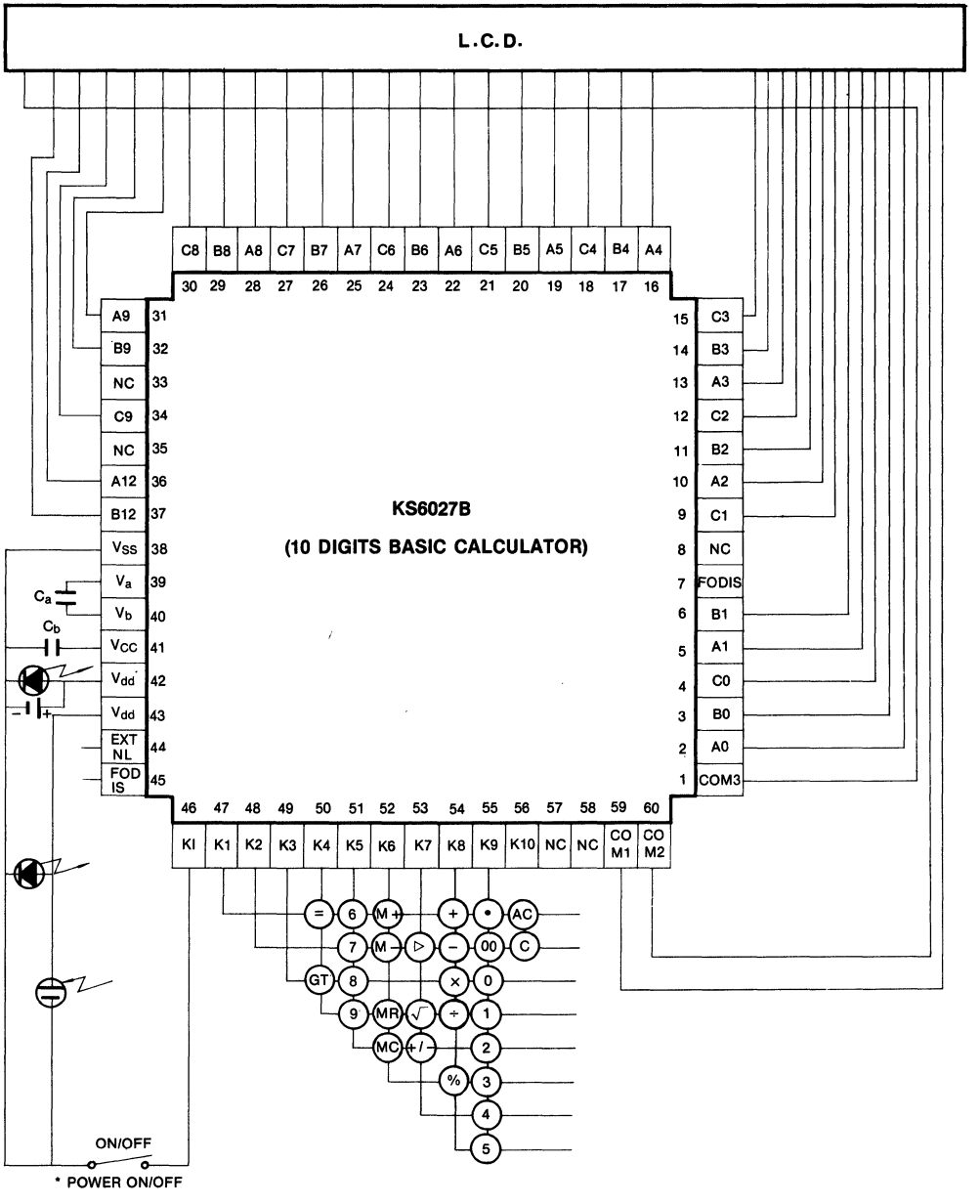
1. Segment



2. Common

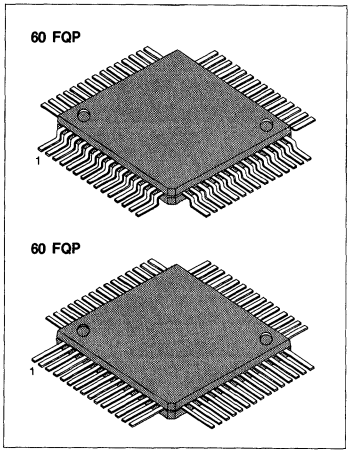


APPLICATION CIRCUIT



3. KS6027C

The KS6027C is 10/12 digits basic or 12 digits desk top (3V operation) calculator which have to use the only 3.0V power supply. However, when you want to use bare chip, you can use 1.5V solar cell as well as 1.5V battery.
Refer to application circuit.



FUNCTION

- Display
  12 digits or 10-digits (selectable with PCB option) of data, 2 digits of sign, error symbol, memory load symbol, constant calculation mode symbol, operation symbol.
- Standard 4 functions
- Memory and grand total (GT) memory calculation
- Automatic percentage operation with add on, discount
- Square root
- Constant calculation
- Chain calculation
- Change sign
- Floating point or momentary mode (selectable with a switch): Desk Top
- Fixed point ("0", "2", "3", "4"): Desk Top
- Adding point mode: Desk Top
- Registraction overflow, indicating that too many digits are entered (the most significant digits are protected).
- Result overflow, indicating during calculation (most function key are locked as it happended).
- Rounding switches (rounding up, down and off)
- Leading zero suppression
- Trailing zero suppression
- Punctuation on display; Commas for thousand.
- Memory and GT memory contents indicator, turn on with non-zero in the memory and GT memory.

BASIC SPECIFICATION

1. Constant calculation

1) Multiplication

Key	Display	Constant
k	k	
×	k	
×	k	
a	a	
=	k·a	k ×
b	b	k ×
=	k·b	k ×

2) Division

Key	Display	Constant
k	k	
÷	k	
÷	k	
a	a	
=	a/k	÷ k
b	b	÷ k
=	b/k	÷ k

3) Addition

k	k	
+	k	
+	k	
a	a	
=	a + k	+ k
b	b	+ k
=	b + k	+ k

4) Subtraction

k	k	
−	k	
−	k	
a	a	
=	a − k	− k
b	b	− k
=	b − k	− k

5) Percentage

k	k	
×	k	
×	k	
a	a	
%	k·a/100	k ×
b	b	k ×
%	k·b/100	k ×

6) Percentage

k	k	
÷	k	
÷	k	
a	a	
%	100·a/k	÷ k
b		÷ k
%	100·b/k	÷ k

2. Add-on, discount calculations

1) Add-on

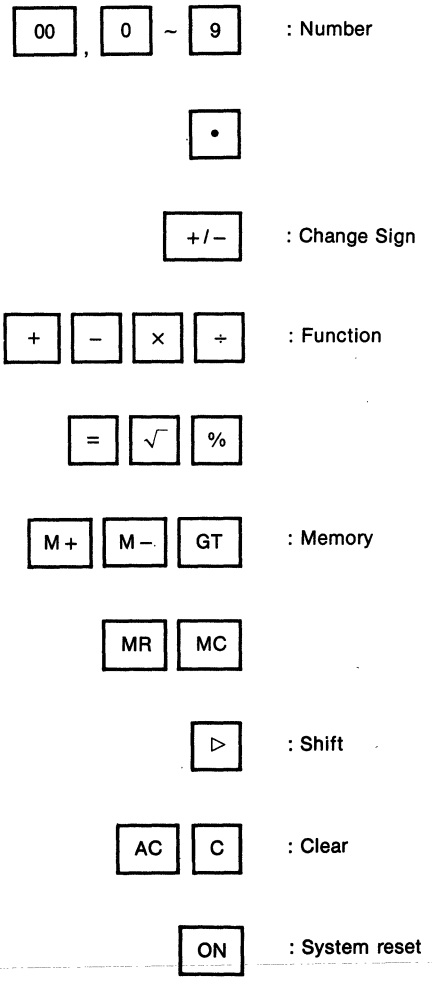
Key	Display
a	a
×	a
b	b
%	a·b/100
+	a(1 + b/100)

2) Discount

Key	Display
a	a
×	a
b	b
%	a·b/100
−	a(1 − b/100)

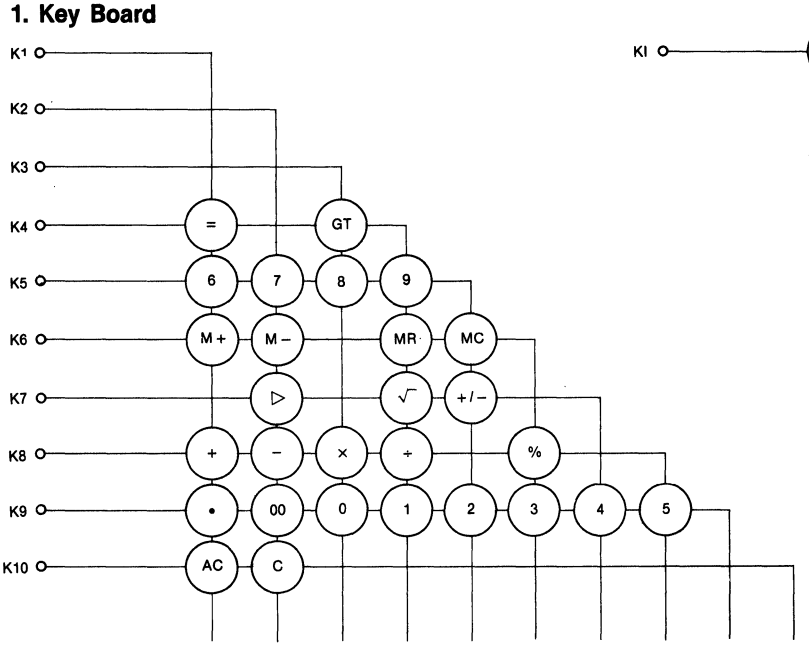
4

TOUCH KEY CONSTITUTION AND OPERATION



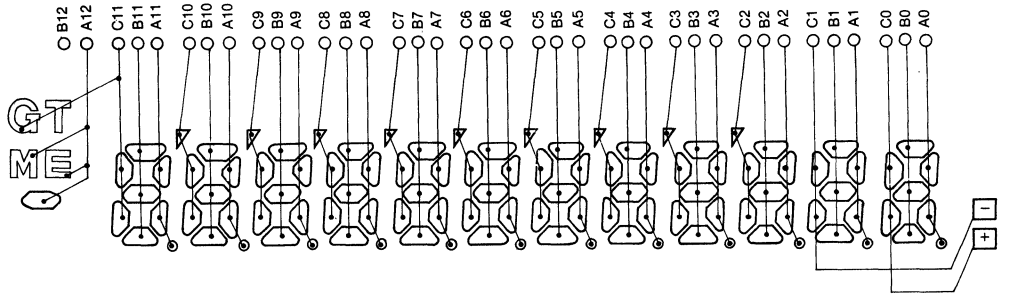
KEY CONSTITUTION AND OPERATION

1. Key Board

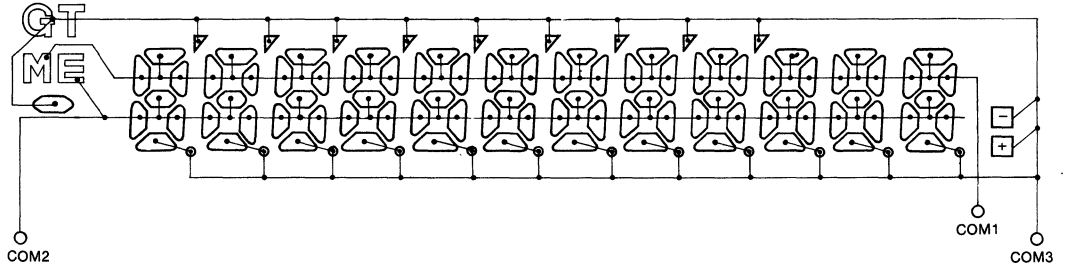


LCD CONNECTION

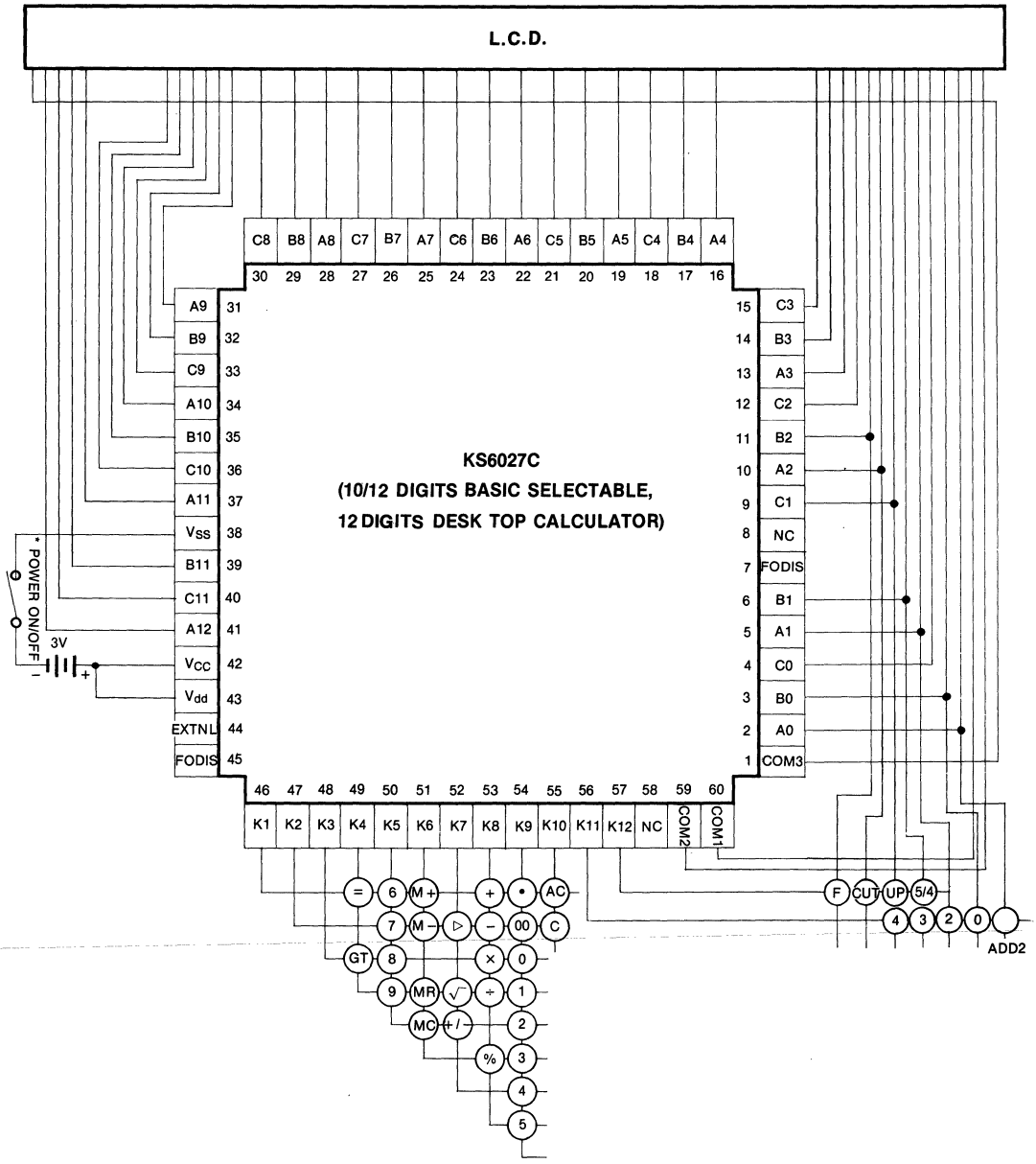
1. Segment



2. Common



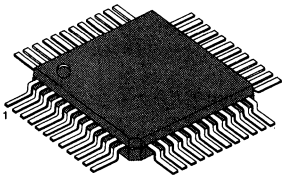
APPLICATION CIRCUIT



BASIC FUNCTION LOW POWER TYPE 8 DIGITS LCD CALCULATOR WITH INTERNAL VOLTAGE REGULATOR

The KS6028 is a single chip CMOS LSI with 8 digits arithmetic operation, single memory, extraction-of-square-root, percentage calculation and auto power off functions, designed for FEM LCD operation with 1.5V power supply.

48 FQP



FUNCTIONS

- Four standard functions (+, −, ×, ÷).
- Auto constant calculations (constant: multiplicand, divisor, addend and subtrabend).
- Square and reciprocal calculations.
- Make-up and make-down calculations.
- Extraction of square root.
- Percentage calculations.

FEATURES

- **Single chip CMOS construction.**
- **Chain multiplication and division.**
- **Power calculations.**
- **Rough estimate calculations.**
- **Rollover capability.**
- **Floating decimal.**
- **LCD direct drive (3, 1/3).**
- **Overflow indication: "E"**
- **Accumulating memory: M−, M−, RM, CM, RM/CM**
- **On-chip oscillator components**
- **On-chip supply voltage limiter by application option.**
- **Very low power consumption.**

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	Note
Terminal Voltage	V_{GG}	−0.3 − 2.1	V	1
	V_{IN}	−0.3 − V_{GG} + 0.3	V	
Solar Supply Voltage	V_{sb}	1.1 ~ 3	V	2
	V_{GG} (lim)	1.1 ~ 1.8	V	3
Battery Supply Voltage	V_B	1.1 ~ 1.8	V	
Operating Temperature	T_{opr}	0 − +50	°C	
Storage Temperature	T_{stg}	−55 − +150	°C	

Note 1. Maximum voltage on any pin with respect to GND.
2. V_{sb} is solar supply voltage.
3. V_{GG} (lim) is limited voltage.

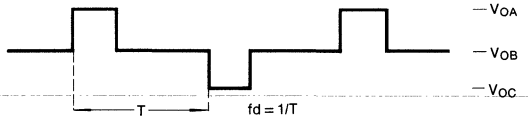
ELECTRICAL CHARACTERISTICS

($Ta = 25°C$, $V_{GG} = 1.5V$, unless otherwise specified)

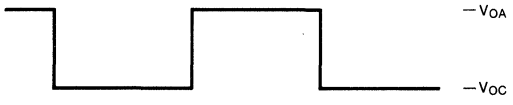
Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Input Voltage 1	V_{IH1}		V_{GG}-0.4			V	4
	V_{IL1}				0.4	V	
Input Current 1	I_{IH1}	$V_{IN} = V_{GG}$			1	μA	5
	I_{IL1}	$V_{IN} = 0V$	0.3	1	3	μA	
Output Voltage 1	V_{OH1}	without load	V_{GG}-0.15			V	6
	V_{OL2}	$I_{out} = 15\mu A$			0.15	V	
Output Voltage 2	V_{OA}	without load	2.80	2.95		V	7
	V_{OB}	without load	1.30	1.50	1.70	V	
	V_{OC}	without load		0	0.20	V	
Display Frequency	F_d	$V_{GG} = 1.3V$ while display is on.	35	50		Hz	7
Dissipation	I_{off}	display is off			0.8	μA	8
	I_{dis}	$V_{GG} = 1.3V$, while display is on		1.3	3	μA	9
	I_{op}	$V_{GG} = 1.1V$, while operation		2.5	5.5	μA	10

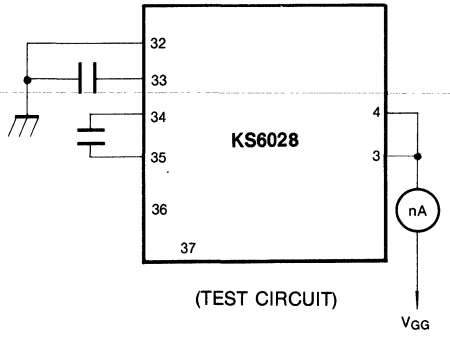
Note 4. Applies to pin K2, K6.
5. Applies to pin K2, and K6.
6. Applies to P1, P2, A2 and A5.
7. Applies to H1, H3, a1, a8, b1, b8, c1 and c8.
8. Measured by the test circuit below after power supply automatically turns off.
9. Measured by the test circuit below while "O" is being displayed after auto-clear operation and while key is not being depressed.
10. Measured by the below test circuit while operated AC key and while key is free from depression.

OUTPUT WAVEFORM 1



OUTPUT WAVEFORM 2





(TEST CIRCUIT)

FUNCTIONAL DESCRIPTION

- Decimal point system

  Complete floating decimal point system.

- Integral number: 8 digits leading zero suppression. Zero shift.

- Symbols: —: negative number display.
  E : error display.
  M : memory display.

• Negative number indication

Antilogarithm: +
Minus : –

Error detections

System errors occur when:
1) The integral part of any calculation result exceeds 8 digits.
2) The integral part of any memory calculation result exceeds 8 digits.
   In addition, the integral part of any addend or subtrahend to memory exceeds 8 digits.
3) The integral part of a make-up and make-down calculation result exceeds 8 digits.
4) The division by zero.
5) The extraction of square root of a negative number.

• Rough estimate calculation error

The integral part of the result of any one of standard for functions, percentage, square, reciprocal, and power calculations exceeds 8 digits and is equal to 16 digits or less.

Error indication

System error

"0" is indicated in the 1 digit position and "E" in the sign-digit position.

Rough estimate calculation error

The high-order 8 digits of a calculation result is indicated together with "E".
The decimal point is indicated in the position corresponding to a calculation result time 10^{-8}, and no zero shift is performed.

Error release

System error

A system error can be release by the AC or ON/CCE key.

Rough estimate calculation error

A rough estimate calculation error can be released by the AC or ON/CCE, CE key.
A calculation result is not cleared by ON/CCE or CE key but is retained.

• Number entry

Numericals can be entered up to 8 digits. Numerical enteries equal to 9 digits or more are ignored.

- **Memory protection**

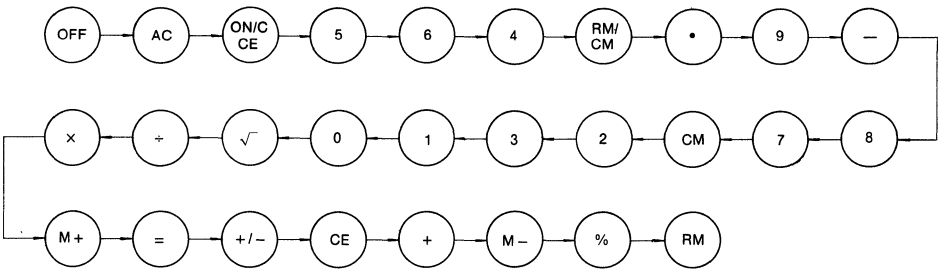
  In any error detection, the memory counters present before the error detection are protected.

- **Memory indication**

  If the memory counter is a number other then zero, "M" is indicated in the sign-digit position.

- **Doubler key depression**

  The order of the priority when two keys are being depressed simultaneously, is as follows:



When the OFF and AC key are depressed simultaneously, the OFF key is given priority.

- **Key bounce protection**

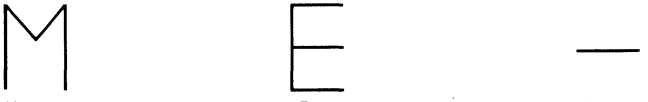
Front edge
Down to 1 word and up to about 3 words.

Trailling edge
9 words.
1 word is 3.3ms when display frequency is fd = 100Hz.

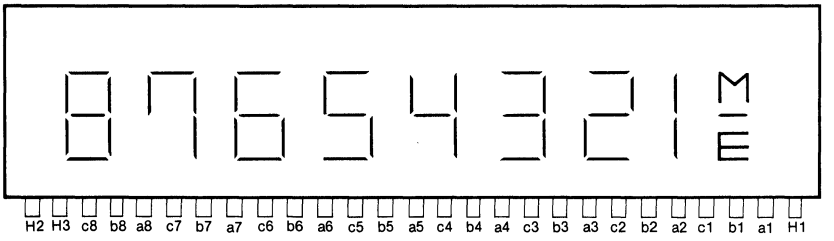
DISPLAY FONTS

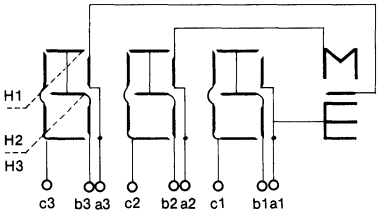
- **Numericals font**

- **Sign font**



- **LCD connector**





AUTO POWER OFF/DISABLE

After 9-11 minute from the last key pressure power is off automatically. By connecting APODIS pin to GND or V_{GG}, whether an auto power off function is available is determined.

APODIS	Auto-power-off state
GND	disable
V_{GG}	enable

AC key

All operation including memory contents are cleared by AC key.

Make-up and make-down calculation

Make-up and make-down calculation are performed as follows.

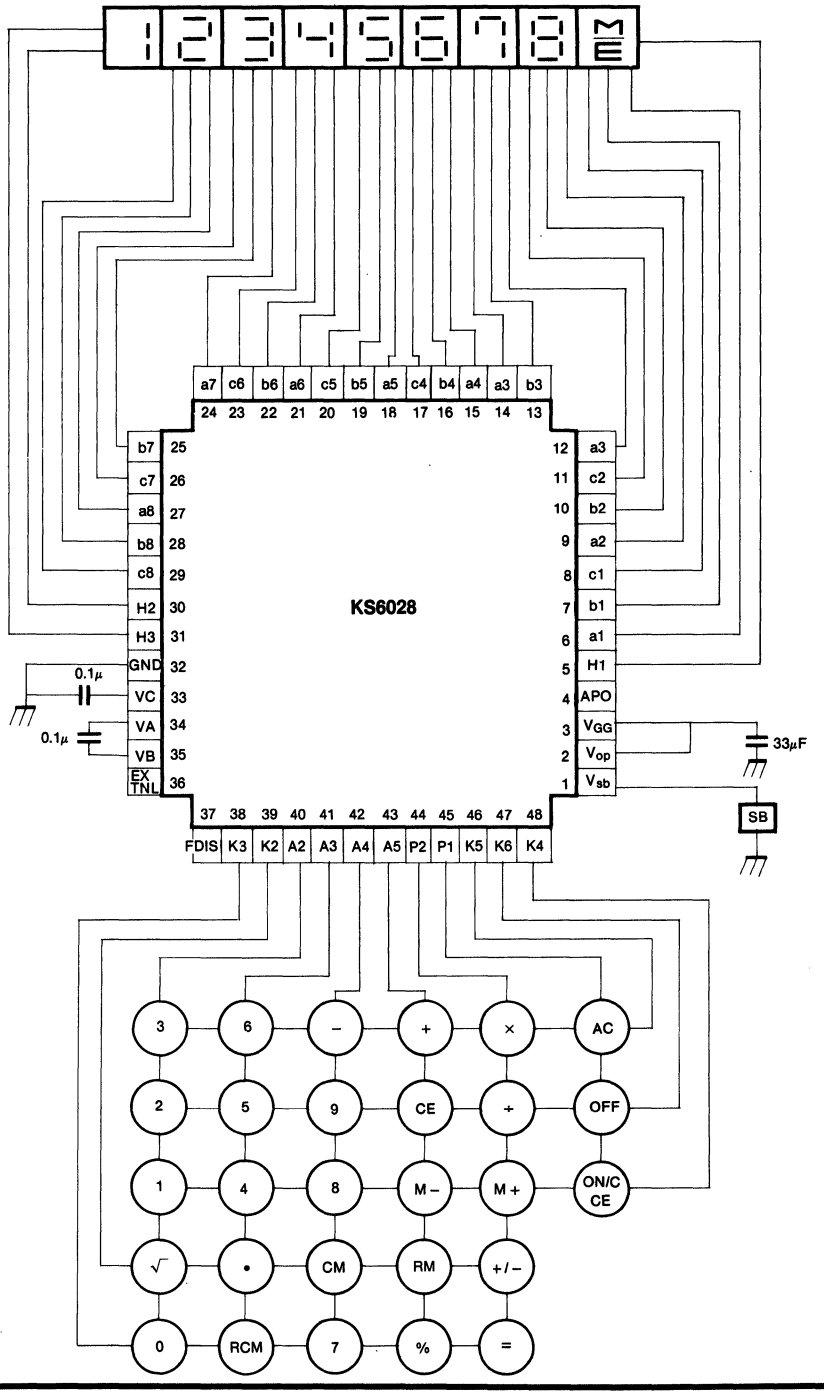
Entry		Display	
A	A	A	A
+	×	A	A
B	B	B	B
%	%	A + AM/100	AM/100
	+ OR −		AM/100
	=		A + AM/100 OR A − AM/100

* AM: Amount

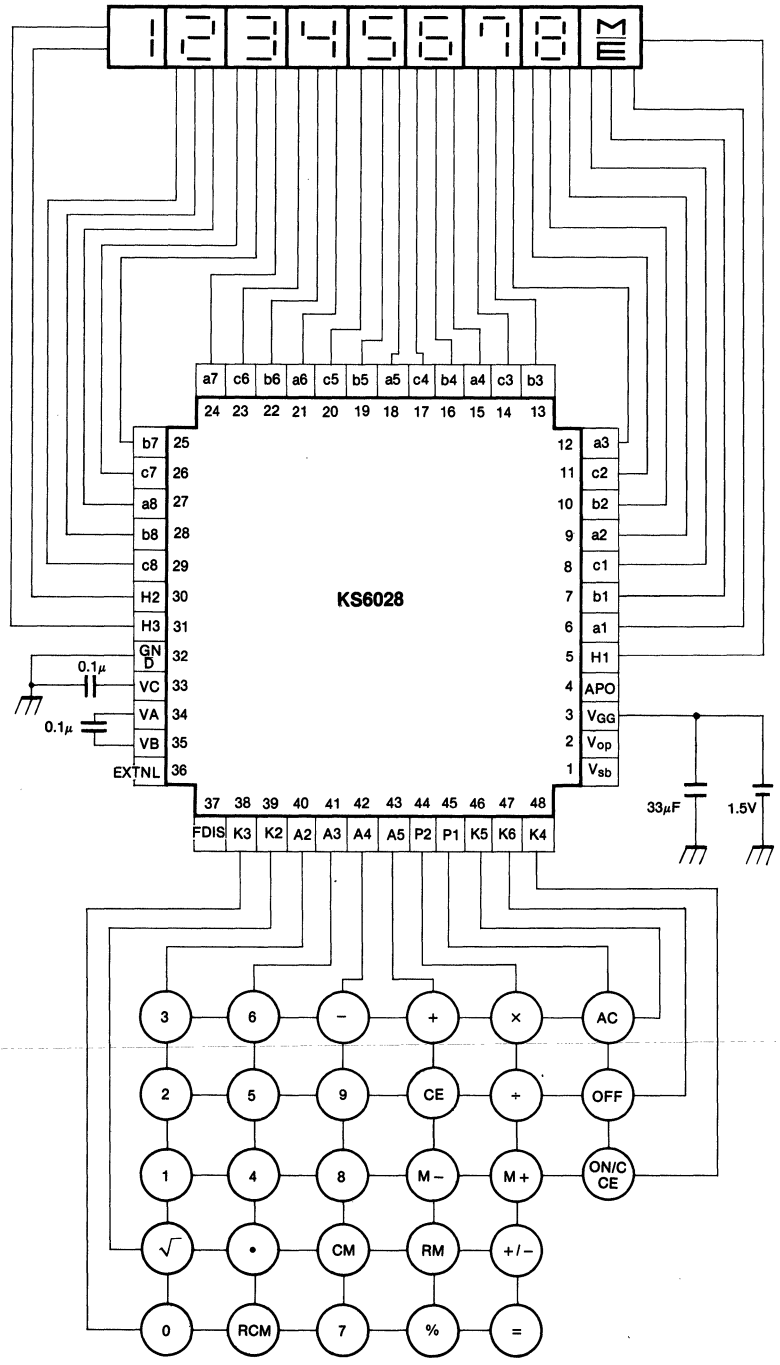
PIN ASSIGNMENT

Pad No.	Pin No.	Signal	I/O	Description	Pad No.	Pin No.	Signal	I/O	Description
1	25	V_{sb}	I	Solar Battery	25	1	b7	O	Display Output
2	26	V_{op}	I	Option Pin	26	2	c7	O	Display Output
3	27	V_{GG}		Power Supply	27	3	a8	O	Display Output
4	28	APODIS	I	APO Disable	28	4	b8	O	Display Output
5	29	H1	O	Display Output	29	5	c8	O	Display Output
6	30	a1	O	Display Output	30	6	H2	O	Display Output
7	31	b1	O	Display Output	31	7	H3	O	Display Output
8	32	c1	O	Display Output	32	8	GND		
9	33	a2	O	Display Output	33	9	VC	O	Capacitor Terminal for Voltage Set-up
10	34	b2	O	Display Output	34	10	VA	O	Capacitor Terminal for Voltage Set-up
11	35	c2	O	Display Output	35	11	WB	O	Capacitor Terminal for Voltage Set-up
12	36	a3	O	Display Output	36	12	EXTNL	I	External Clock
13	37	b3	O	Display Output	37	13	FDIS	I	FOSC and Freq. Doubler Disable
14	38	c3	O	Display Output	38	14	K3	I	Key Input
15	39	a4	O	Display Output	39	15	K2	I	Key Input
16	40	b4	O	Display Output	40	16	A2	O	Strobe Output
17	41	c4	O	Display Output	41	17	A3	O	Strobe Output
18	42	a5	O	Display Output	42	18	A4	O	Strobe Output
19	43	b5	O	Display Output	43	19	A5	O	Strobe Output
20	44	c5	O	Display Output	44	20	P2	O	Strobe Output
21	45	a6	O	Display Output	45	21	P1	O	Strobe Output
22	46	b6	O	Display Output	46	22	K5	I	Key Input
23	47	c6	O	Display Output	47	23	K6	I	Key Input
24	48	a7	O	Display Output	48	24	K4	I	Key Input

APPLICATION CIRCUIT (for use with a solar cell)

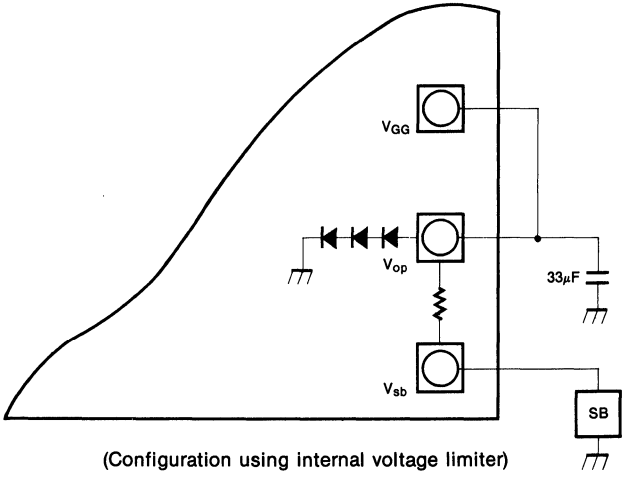


APPLICATION CIRCUIT (for use with a battery)



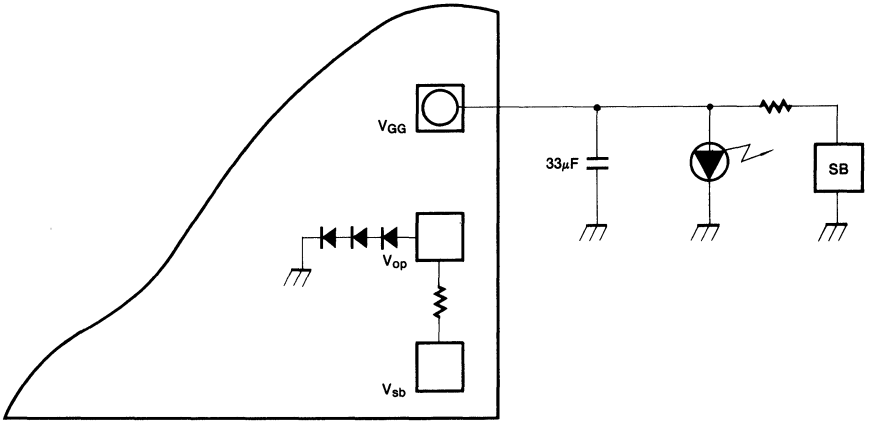
INTERNAL VOLTAGE LIMITER BONDING OPTION METHOD

OPTION 1



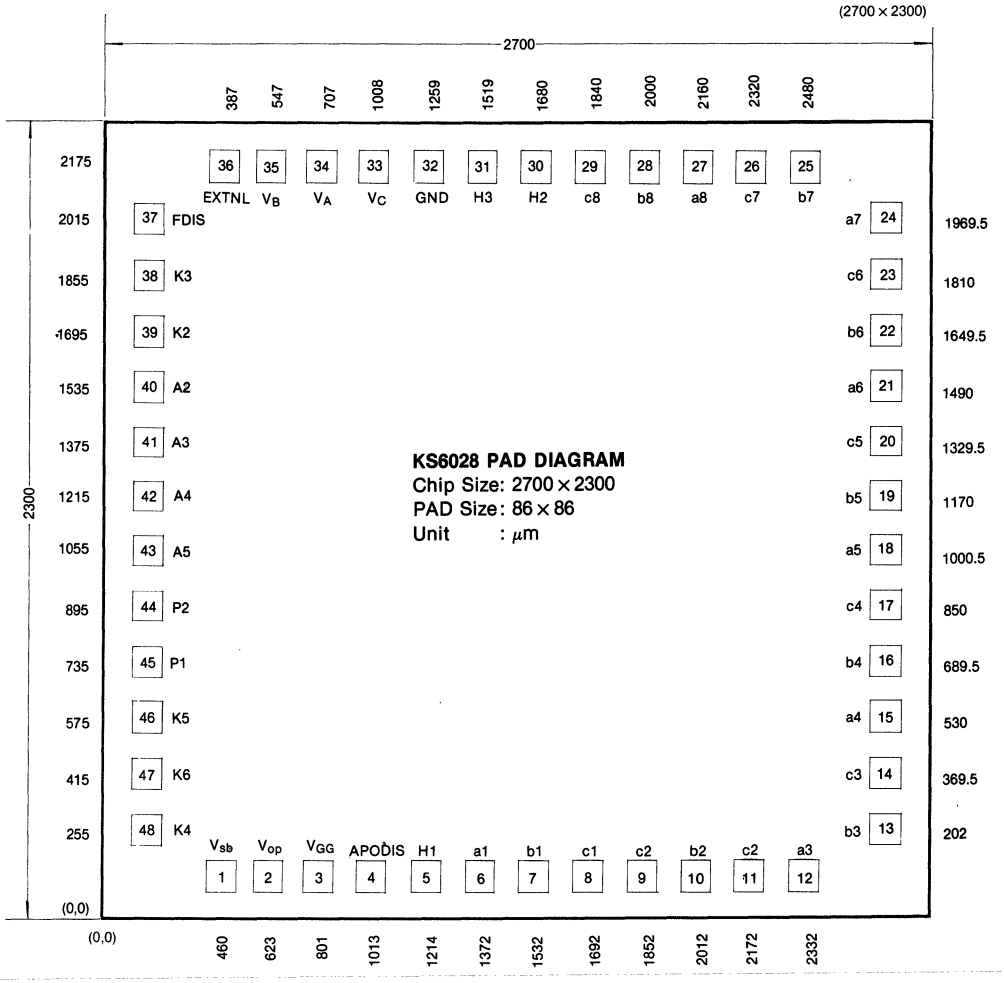
(Configuration using internal voltage limiter)

OPTION 2



(Configuration using external voltage limiter)

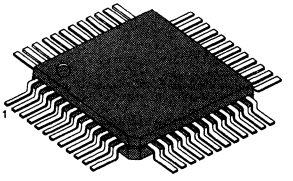
PAD DIAGRAM


(2700 x 2300)
2700
2300
(0,0)
KS6028 PAD DIAGRAM
Chip Size: 2700 x 2300
PAD Size: 86 x 86
Unit : μm
1 Vsb
2 Vop
3 VGG
4 APODIS
5 H1
6 a1
7 b1
8 c1
9 c2
10 b2
11 c2
12 a3
13 b3
14 c3
15 a4
16 b4
17 c4
18 a5
19 b5
20 c5
21 a6
22 b6
23 c6
24 a7
25 b7
26 c7
27 a8
28 b8
29 c8
30 H2
31 H3
32 GND
33 Vc
34 VA
35 VB
36 EXTNL
37 FDIS
38 K3
39 K2
40 A2
41 A3
42 A4
43 A5
44 P2
45 P1
46 K5
47 K6
48 K4
460
623
801
1013
1214
1372
1532
1692
1852
2012
2172
2332
387
547
707
1008
1259
1519
1680
1840
2000
2160
2320
2480
2175
2015
1855
1695
1535
1375
1215
1055
895
735
575
415
255
1969.5
1810
1649.5
1490
1329.5
1170
1000.5
850
689.5
530
369.5
202

BASIC FUNCTION 10 DIGITS LCD CALCULATOR WITH INTERNAL VOLTAGE REGULATOR

The KS6029 is a single chip CMOS LSI with 10 digits arithmetic operation, single memory, extraction-of-square-root, percentage calculation and auto power off functions, designed for FEM LCD operation with 1.5V power supply.

48 FQP



FUNCTIONS

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- Auto constant calculations (constant: multiplicand, divisor, addend and subtrabend).
- Square and reciprocal calculations.
- Make-up and make-down calculations.
- Extraction of square root.
- Percentage calculations.

FEATURES

- **Single chip CMOS construction.**
- **Chain multiplication and division.**
- **Power calculations.**
- **Rough estimate calculations.**
- **Rollover capability.**
- **Floating decimal point.**
- **LCD direct drive (4, 1/4).**
- **Overflow indication: "E"**
- **Accumulating memory: M1, M, RM, CM, RM/CM**
- **On-chip supply voltage limiter by application option.**
- **Very low power consumption.**
- **On-chip oscillator components**

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit	Note
Terminal Voltage	V_{GG}	−0.3 ~ 2.1	V	1
	V_{IN}	−0.3 ~ V_{GG} + 0.3	V	
Solar Supply Voltage	V_{sb}	1.1 ~ 3	V	2
	V_{GG} (lim)	1.1 ~ 1.8	V	3
Battery Supply Voltage	V_B	1.1 ~ 1.8	V	
Operating Temperature	T_{opr}	0 ~ +50	°C	
Storage Temperature	T_{stg}	−55 ~ +150	°C	

Note 1. Maximum voltage on any pin with respect to GND.
2. V_{sb} is solar supply voltage.
3. V_{GG} (lim) is limited voltage.

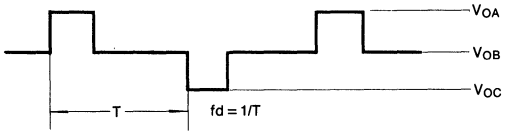
ELECTRICAL CHARACTERISTICS

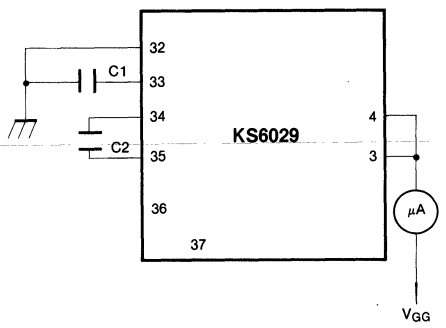
($Ta = 25°C$, $V_{GG} = 1.5V$, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	Note
Input Voltage 1	V_{IH1}		V_{GG}-0.4			V	4
	V_{IL1}				0.4	V	
Input Current 1	I_{IH1}	$V_{IN} = V_{GG}$			1	μA	5
	I_{IL1}	$V_{IN} = 0V$	0.3	1	3	μA	
Output Voltage 1	V_{OH1}	without load	V_{GG}-0.15			V	6
	V_{OL2}	$I_{out} = 15\mu A$			0.15	V	
Output Voltage 2	V_{OA}	without load	2.80	2.95		V	7
	V_{OB}	without load	1.30	1.50	1.70	V	
	V_{OC}	without load		0	0.20	V	
Display Frequency	F_d	$V_{GG} = 1.3V$ while display is on.	35	50		Hz	7
Dissipation	I_{off}	display is off			0.8	μA	8
	I_{dis}	$V_{GG} = 1.3V$, while display is on		1.5	3	μA	9
	I_{op}	$V_{GG} = 1.1V$, while operation		3	5.5	μA	10

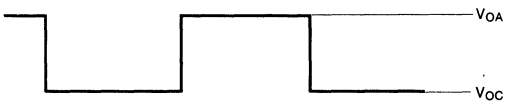
Note 4. Applies to pin K2, K6.
5. Applies to pin K2, and K6.
6. Applies to P1, P2, A2 and A5.
7. Applies to H1, H3, a1, a8, b1, b8, c1 and c8.
8. Measured by the test circuit below after power supply automatically turns off.
9. Measured by the test circuit below while "O" is being displayed after auto-clear operation and while key is not being depressed.
10. Measured by the below test circuit while operated AC key and while key is free of depression.

OUTPUT WAVE FORM 1





OUTPUT WAVE FORM 2



FUNCTIONAL DESCRIPTION

* Decimal point system
  Complete floating decimal point system.

* Integral number: 10 digits leading zero suppression. Zero shift.

* Symbols: —: negative number display.
  E : error display.
  M : memory display.

* Negative number indication

Antilogarithm: +
Minus : –

Error detections

System errors occur when:
1) The integral part of any calculation result exceeds 10 digits.
2) The integral part of any memory calculation result exceeds 10 digits.
   In addition, the integral part of any addend or subtrahend to memory exceeds 10 digits.
3) The integral part of a make-up and make-down calculation result exceeds 10 digits.
4) The division by zero.
5) The extraction of square root of a negative number.

Rough estimate calculation error

The integral part of the result of any one of standard for functions, percentage, square, reciprocal and power calculations exceeds 10 digits and is equal to 20 digits or less.

Error indication

System error

"O" is indicated in the 1 digit position and "E" in the sign-digit position.

Rough estimate calculation error

The high-order 10 digits of a calculation result is indicated together with "E". The decimal point is indicated in the position corresponding to a calculation result time 10^{-10}, and no zero shift is performed.

Error release

System error
A system error can be release by the AC or ON/CCE key.

Rough estimate calculation error
A rough estimate calculation error can be released by the AC or ON/CCE, CE key. A calculation result is not cleared by ON/CCE or CE key but is retained.

*** Number entry**
Numericals can be entered up to 10 digits. Numerical enteries equal to 11 digits or more are ignored.

- **Memory protection**

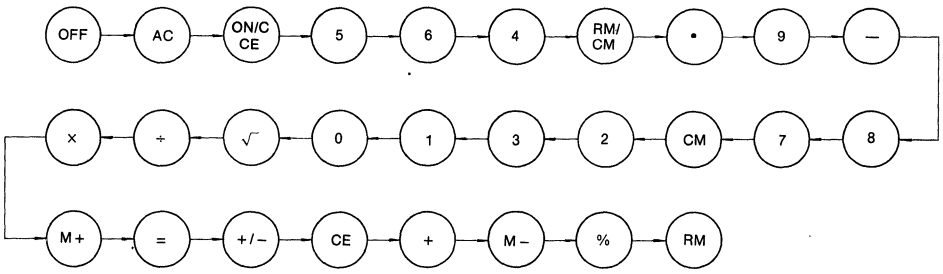
  In any error detection, the memory counters present before the error detection are protected.

- **Memory indication**

  If the memory contents are a number other then zero, "M" is indicated in the sign-digit position.

- **Doubler key depression**

  The order of the priority when two keys are being depressed simultaneously, is regarded as follows:



When the OFF and AC key are depressed simultaneously, the OFF key is given priority.

- **Key bounce protection**

Front edge
Down to 1 word and up to about 3 words.

Trailling edge
9 words.
1 word 3.3ms when display frequency fd = 100Hz.

DISPLAY FONTS

- **Numericals font**

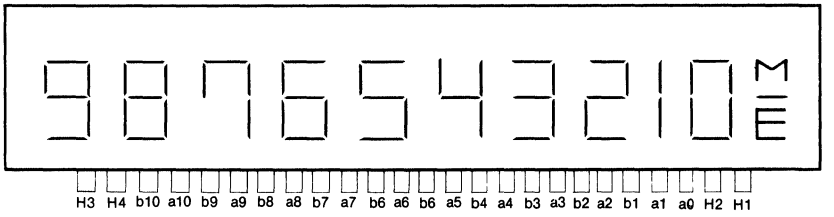
- **Sign font**

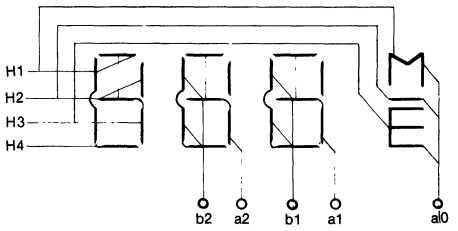

Memory


Error

Minus

LCD connector





AUTO POWER OFF/DISABLE

After 9-11 minute from the last key pressure power is off automatically. By connecting APODIS pin to GND or V_{GG}, whether an auto power off function is available is determined.

APODIS	Auto-power-off state
GND	disable
V_{GG}	enable

AC key

All operation including memory contents are cleared by AC key.

Make-up and make-down calculation

Make-up and make-down calculation are performed as follows.

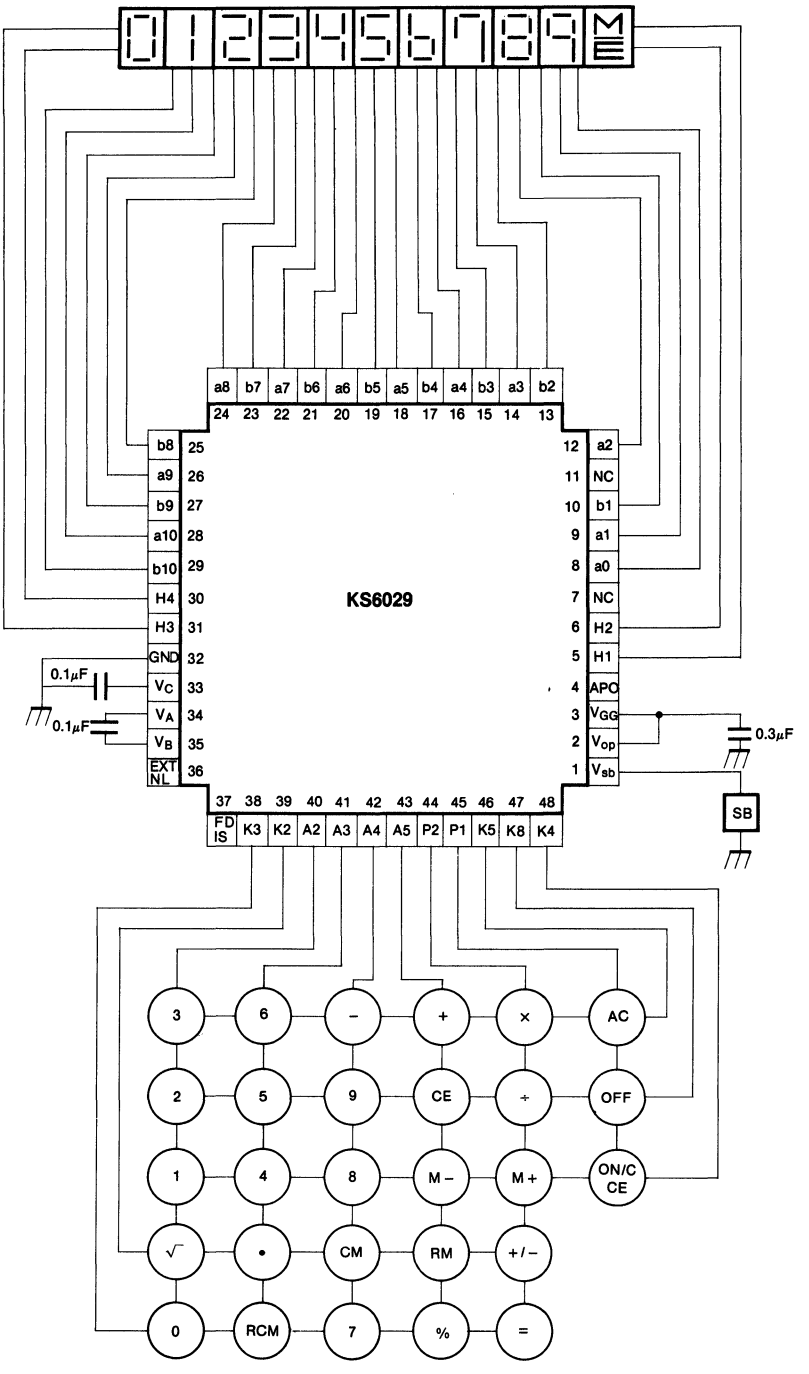
Entry		Display	
A	A	A	A
+	×	A	A
B	B	B	B
%	%	A + AM/100	AM/100
	+ OR −		AM/100
	=		A + AM/100 OR A − AM/100

* AM: Amount

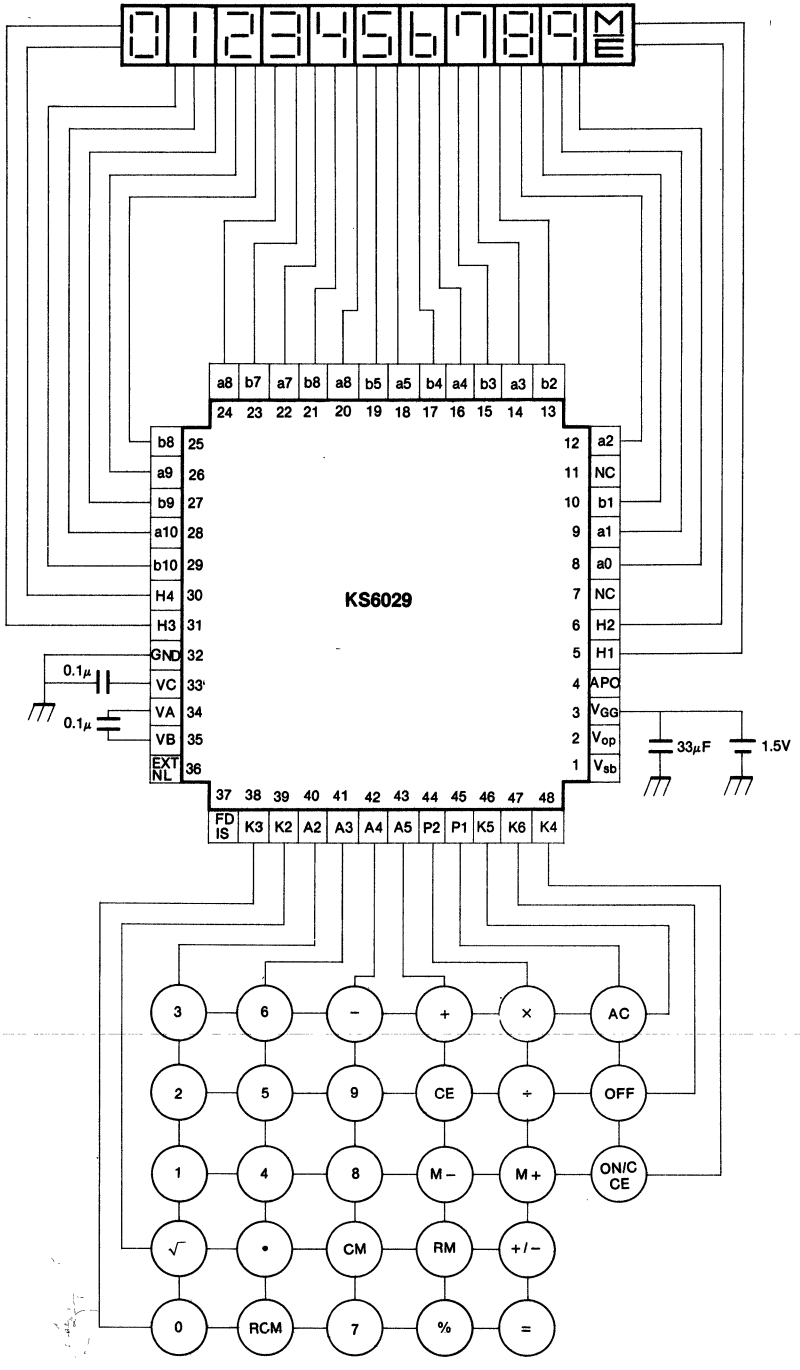
PIN ASSIGNMENT

Pin No.	Signal	I/O	Description	Pin No.	Signal	I/O	Description
1	V_{sb}	I	Solar Battery	25	b8	O	Display Output
2	V_{op}	I	Option Pin	26	a9	O	Display Output
3	V_{GG}		Power Supply	27	b9	O	Display Output
4	APODIS	I	APO Disable	28	a10	O	Display Output
5	H1	O	Display Output	29	b10	O	Display Output
6	H2	O	Display Output	30	H4	O	Display Output
7	NC			31	H3	O	Display Output
8	a0	O	Display Output	32	GND		
9	a1	O	Display Output	33	VC	O	Capacitor Terminal for Voltage Set-up
10	b1	O	Display Output	34	VA	O	Capacitor Terminal for Voltage Set-up
11	NC			35	VB	O	Capacitor Terminal for Voltage Set-up
12	a2	O	Display Output	36	EXTNL	I	External Clock
13	b2	O	Display Output	37	FDIS	I	FOSC and Freq. Doubler Disable
14	a3	O	Display Output	38	K3	I	Key Input
15	b3	O	Display Output	39	K2	I	Key Input
16	a4	O	Display Output	40	A2	O	Strobe Output
17	b4	O	Display Output	41	A3	O	Strobe Output
18	a5	O	Display Output	42	A4	O	Strobe Output
19	b5	O	Display Output	43	A5	O	Strobe Output
20	a6	O	Display Output	44	P2	O	Strobe Output
21	b6	O	Display Output	45	P1	O	Strobe Output
22	a7	O	Display Output	46	K5	I	Key Input
23	b7	O	Display Output	47	K6	I	Key Input
24	a8	O	Display Output	48	K4	I	Key Input

APPLICATION CIRCUIT (for use with a solar cell)

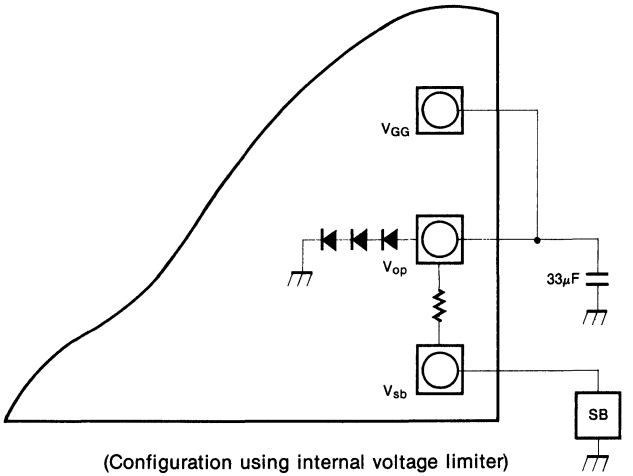


APPLICATION CIRCUIT (for use with a battery)



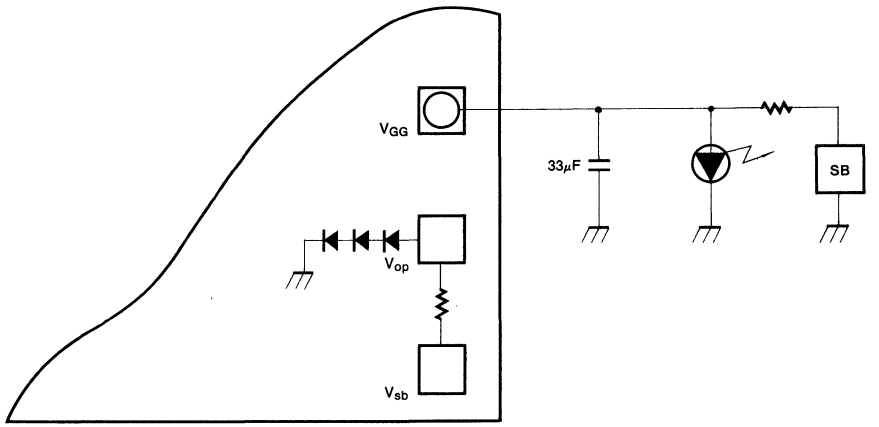
INTERNAL VOLTAGE LIMITER BONDING OPTION METHOD

OPTION 1



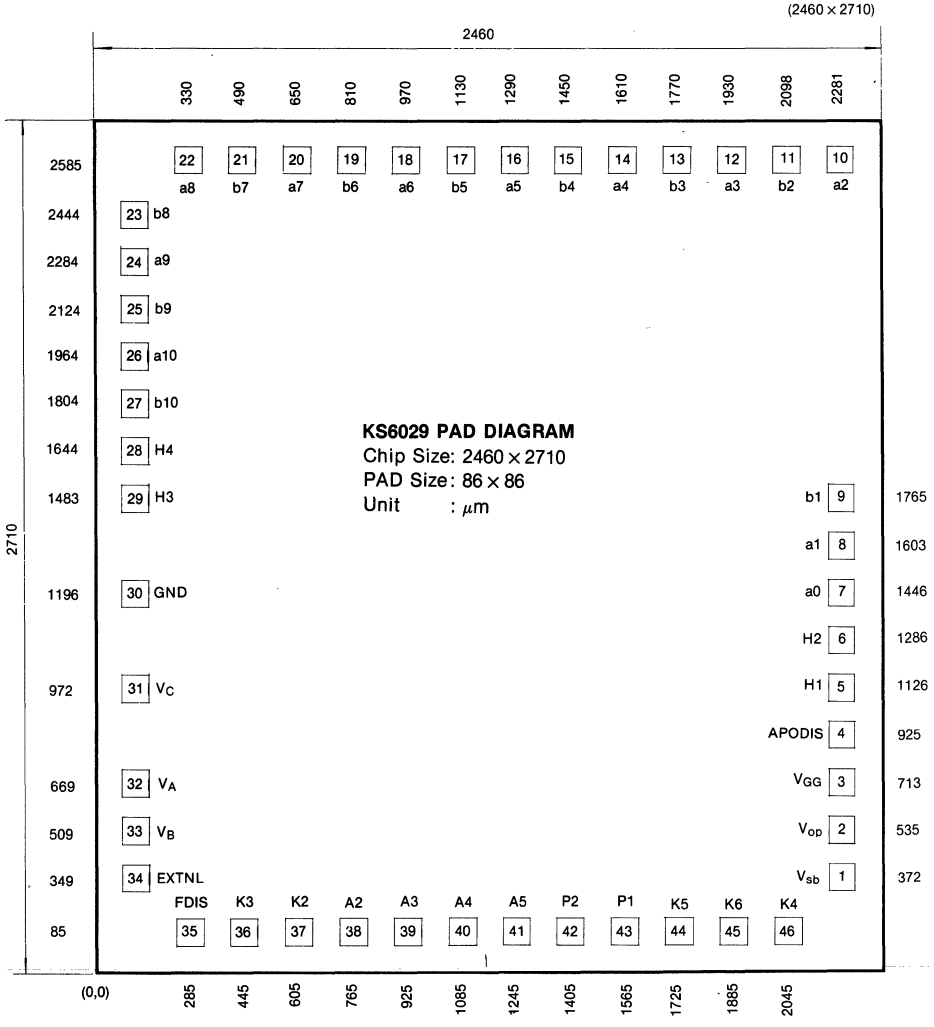
(Configuration using internal voltage limiter)

OPTION 2



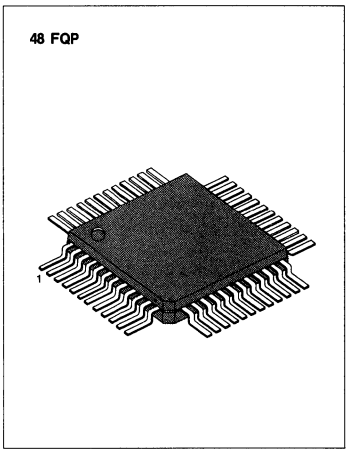
(Configuration using external voltage limiter)

PAD DIAGRAM


(2460 x 2710)
2460
2710
KS6029 PAD DIAGRAM
Chip Size: 2460 x 2710
PAD Size: 86 x 86
Unit : μm
(0,0)
22 a8
21 b7
20 a7
19 b6
18 a6
17 b5
16 a5
15 b4
14 a4
13 b3
12 a3
11 b2
10 a2
23 b8
24 a9
25 b9
26 a10
27 b10
28 H4
29 H3
30 GND
31 VC
32 VA
33 VB
34 EXTNL
35 FDIS
36 K3
37 K2
38 A2
39 A3
40 A4
41 A5
42 P2
43 P1
44 K5
45 K6
46 K4
9 b1
8 a1
7 a0
6 H2
5 H1
4 APODIS
3 VGG
2 Vop
1 Vsb

SCIENTIFIC 10 DIGITS LCD CALCULATOR

KS6041 is the CMOS LSI for 10 digits display and the complete single chip for scientific calculator with 56 programmed function.



FUNCTION

(1) Six operations.
- Four operations (+, −, ×, ÷)
- y^x
- $\sqrt[x]{y}$
- Auto-constant
- Parenthesis
- Percentage

(2) Memory calculation
Independent single memory (x→M, RM, M+)

(3) Four operations complex number calculation.

(4) 1 Variable function.
- Trigonometric and arctrigonometric function.
- Hyperbolic and archyperbolic function
- Square root and cube root
- Factorial
- Time conversions
- Reciprocal and square
- Angular mode conversion

(5) 2 Variables function
- Polar-rectangular coordinate conversion

(6) Statistic calculation
- Number of sample (n)
- Total of square of all data (Σx^2)
- Average (X)
- 2 kinds of the standard deviation (S, σ)
- Total of all data (Σx)

(7) Binary, Octal, Decimal and Hexadcimal number calculation
- Mutual conversion and calculation of binary, Octal, Decimal, and hexadecimal.

(8) Display conversion
Conversion and setting of floating and engineering display.

FEATURES

(1) Display
- **10 display digits plus negative code 1 digit.**
- **Scientific and engineering display.**
- **Mantissa 8 digits plus exponent 2 digits plus negative code 2 digits.**

(2) 14 kinds of special display

M	**Memory**	**GRAD**	**Gradient**
—	**Minus**	**( )**	**Parenthesis**
E	**Error**	**BIN**	**Binary mode**
2ndF	**2nd Function**	**OCT**	**Octal mode**
HYP	**Hyperbolic**	**HEX**	**Hexadecimal mode**
DEG	**Degree**	**CPLX**	**Complex number mode**
RAD	**Radian**	**STAT**	**Statistic calculation mode**

(3) The minus sign of the mantissa is floating minus.

(4) The arithmatic key operation has same sequenc as mathematical equation, 6 pending operations are allowed and ( ) are up to continuous 15 Levels.

(5) Mutual conversion and calculation in arithmetic among binary, octal, decimal, and hexadecimal number.

(6) One independent accumulating memory.

(7) It is possible to convert and fix the display number system by F→E key.

(8) It is possible to specify decimal part digits by TAB key.

(9) Direct drive for LCD (1/3 prebias, 1/4 duty)

(10) Automatic power off (about 7.5 minutes)

(11) Low power consumption
V_{DD} = 3.0V single power supply.

(12) The 48 pin quad flat package is used.

ELECTRICAL CHARACTERISTICS

(1) Absolute maximum ratings.

Item	Symbol	Rating	Unit
Terminal voltage	V_{DD}	−0.3 — +3.3	V
	V_{IN}	−0.3 — V_{DD}-0.3	V
Operating temperature	Topr	0 — +40	°C
Storage temperature	Tstg	−55 — +125	°C

(2) Electrical characteristics.

(V_{DD} = +3.0V ± 0.2V, V_{SS} = 0V, T_a = 25 ± 1.5°C)

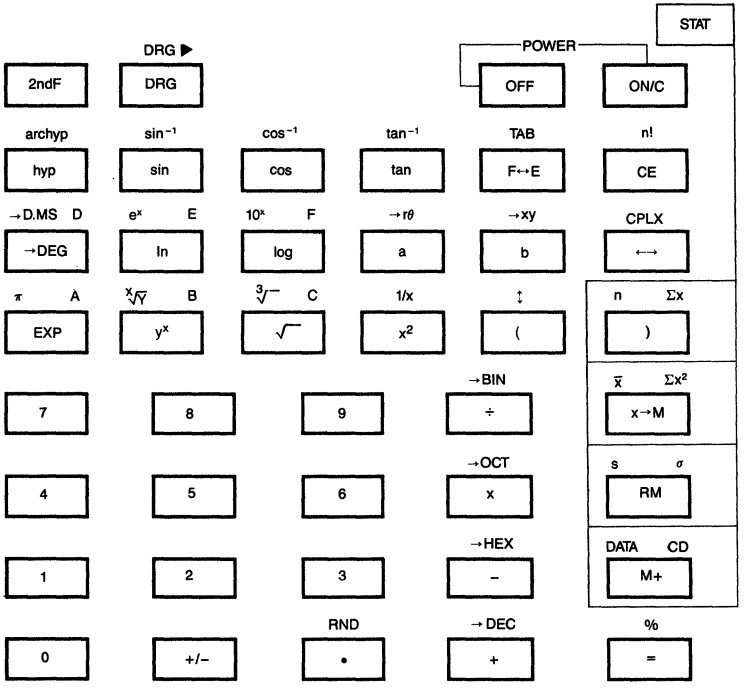
Item	Pin Name	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	—	—	—	2.5	3	3.4	V
Supply current	—	Idis	V_{DD} = 3V, Stand by		20	35	μA
	—	Iopr	V_{DD} = 3V, Operation		70	120	μA
	—	Ioff	V_{DD} = 3V, Off		1	3	μA
Osc frequency	—	Fdis	V_{DD} = 3V, Stand by	30	40	50	KHz
	—	Fopr	V_{DD} = 3V, Operation		200	250	KHz
Frame frequency	—	Ff	V_{DD} = 3V, Stand by	110	145	180	Hz
Auto power off	—	Tapo	V_{DD} = 3V	300	430	600	Sec
High input voltage	KI8-KI1	V_{IH}	—	V_{DD} −0.5		V_{DD}	V
Low input voltage	KI8-KI1	V_{IL}	—	V_{SS}		V_{SS} +0.5	V
High output voltage	KI8, KI4 KI2	V_{OH}	—	V_{DD} −0.2	V_{DD}	V_{DD}	V
Low output voltage	KI1	V_{OL}	—	V_{SS} +0.2	V_{SS}	V_{SS}	V
Key pull down resistance	KI1	Rpd	Vout=0V	27	45	63	kΩ
Key pull up resistance	KI8, KI4 KI2	Rpu	Vout=V_{DD}	27	45	63	kΩ
High output voltage	LCD, COM	V_{OH}	—	V_{DD} −0.2	V_{DD}	V_{DD}	V
"M" output voltage	LCD, COM	V_{OM}	—	2/3 V_{DD} −0.2	2/3 V_{DD}	2/3 V_{DD} +0.2	V
"M" output voltage	LCD, COM	V_{OM}	—	1/3 V_{DD} −0.2	1/3 V_{DD}	1/3 V_{DD} +0.2	V
Low output voltage	LCD, COM	V_{OL}	—	V_{SS}	V_{SS}	V_{SS} +0.2	V

BASIC SPECIFICATION

(1) Number of display digits.
- 10 digits display and 14 kinds of special display.
- Engineering display
  Max mantissa 10 digits plus exponent 2 digits plus each negative code digit.
- Normal display
  Max mantissa 10 digits plus negative code one digit.
  It is possible to specify the number of 0 to 9 digits below the decimal place by assignment of decimal digit.

(2) Classification of operation mode.
Following 6 type of operation mode are set by 2ndF key and below keys.
2ndF STAT : Statistic calculation mode set
2ndF CPLX : Complex number calculation mode set
2ndF −BIN : Binary mode set
2ndF −OCT : Octal mode set
2ndF −HEX : Hexadecimal mode set
2ndF −DEC : Decimal mode set

(3) Kinds of keys and classification of multi-function 42 all touch keys.



(4) The condition during calculation.
No key input is allowed and no data is displayed during calculation.

(5) Display method.

a. Set number and result of operation are displayed in right margin, minus floating.

b. Display of decimal number operation results.
Display is made according to the display format that has been set by F↔E key.

- Floating mode
  $10^{10} \leq |x| \leq 10^{100}$: Exponent display.
  $10^{-99} \leq |x| \leq 10^{-9}$: Exponent display.
  0 and $10^{-9} \leq |x| \leq 10^{10}$: Floating display.
- Engineering mode
  0 and $10^{-99} \leq |x| \leq 10^{100}$ (all ranges); Exponent display.

F↔E key also convert the display format of a displayed numerical value simultaneously with the display format setting.
At the same time, number of digits below the decimal point of the above modes follows the display format assigned by 2ndF and F↔E keys.
Further, in the same manner as F↔E key, the conversion is also taken place simultaneously with the display format setting.
When the number of digits is specified, the displayed last digit is a rounded number, and when there is no specification of the number of digits, the displayed last digit is a cut number.

Example:

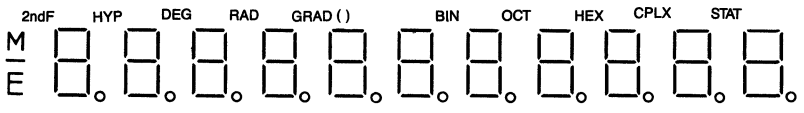
[2]	[÷]	[7]	[=]	0.285714285
TAB [2ndF]	[F↔E]	[3]		0.286
[F↔E]				2.857-01
TAB [2ndF]	[F↔E]	[•]		2.8571428-01

c. Negative numbers are not displayed with the minus symbol "—" but are displayed in hexadecimal, octal, and binary two's complement.

d. Display style and special display

- Display style.

- Special display



e. Examples of display

• Floating of -6000 1/x; TAB=7

• Same as above, engineering display

• Error display

DEG

E

(6) Protection

a. Memory overflow protection
If the overflow occures in the memory calculation, the data before calculation is retained.

b. Statistical overflow protection
If the overflow occures in the statistical calculation, the data before calculation is retained.

(7) The number of digits of the internal retained data.
The number of digits of the mantissa of displayed data is maximum 10 digits, but the available data for successive calculation is the internal retained data.
The number of digits of the mantissa of internal retained data is as follows.

a. Data input	Maximum	10 digits.
b. Arithmetic	Maximum	10 digits.
c. Engineering function		
d. Statistical function		
e. Complex number function		
f. Memory calculation		
g. Number of random	Maximum	3 digits

(8) Auto clear
When the power supply is suddenly turned on, auto clear routine is executed to initialize as DEC mode, no TAB, floating and DEG mode.

(9) Power off function.

a. Auto power off
In about 7.5 minutes, after operation ended or pressing key, the power supply is turned off.

b. OFF
Pressing the key shall stop the oscillator. (Memory safe guard)

c. ON
Pressing this key shall wake the oscillator and initialize.

4

OPERATION MODE

(1) Operation mode

Operation \ Mode		DEC	BIN	OCT	HEX	STAT	CPLX
6 Operation	4 Operation +, −, ×, ÷, =	O	O	O	O	O	O
	Power y^x, $\sqrt[x]{y}$	O	X	X	X	O	X
	Parenthesis ( )	O	O	O	O	X	X
	Constant calculation	O	O	O	O	O	X
	Percentage calculation	O	X	X	X	O	X
STAT	Statistical calculation	X	X	X	X	O	X
CPLX	CPLX calculation	X	X	X	X	X	O
	Input a, b	O	X	X	X	X	O
DATA setting	Numberic input 0, 1	O	O	O	O	O	O
	Numeric input (2-7)	O	X	O	O	O	O
	Numeric input 8, 9	O	X	X	O	O	O
	Hex input A-F	X	X	X	O	X	X
	•, Exp	O	X	X	X	O	O
	+/−	O	O	O	O	O	O
	Shift key	O	O	O	O	O	O
CE		O	O	O	O	O	O
Memory	Memory calculation	O	O	O	O	O	O
Display conversion	P↔E, TAB	O	X	X	X	X	X
P-R conversion	P→R R→P	O	X	X	X	X	O
Random	RND	O	X	X	X	O	O
Function	1 variable function	O	X	X	X	O	O
Augular conversion	DRG DRG▶	O	X	X	X	O	O

(2) The calculation is always shifted to a specified mode by mode keys.
A Mode → B Mode

A / B	DEC	BIN	OCT	HEX	STAT	CPLX
DEC	NOP	DEC Conversion	DEC Conversion	DEC Conversion	DEC Conversion State clear	DEC Conversion State clear
BIN	BIN Conversion	NOP	BIN Conversion	BIN Conversion	BIN Conversion State clear	BIN Conversion State clear
OCT	OCT Conversion	OCT Conversion	NOP	OCT Conversion	OCT Conversion State clear	OCT Conversion State clear
HEX	HEX Conversion	HEX Conversion	HEX Conversion	NOP	HEX Conversion State clear	HEX Conversion State clear
STAT	Display Clear	Display Clear	Display Clear	Display Clear	NOP	Display Clear
CPLX	Display Clear	Display Clear	Display Clear	Display Clear	Display Clear State clear	NOP

NOP: No operation.

KEY DEFINITIONS.

(1) 2ndF
This is the key for specifying the second function.
When this key is pressed, the special display "2ndF" lights. When this key is pressed twice continuously, the second function mode is released.

(2) DRG DRG▶
a. Pressing this key shall change the mode of angle sequencially
┌→ DEG →RAD →GRAD┐ and displayed it.

b. Pressing this key after 2ndF key shall change the mode of angle and shall convert the displayed data
DEG → RAD : $RAD=DEG\times\frac{\pi}{180}$
RAD → GRAD : $GRAD=RAD\times\frac{200}{\pi}$
GRAD → DEG : $DEG=GRAD\times 0.9$

(3) 0 — 9
a. In setting data in the mantissa section, it is set at the right margin, and data in more than 11 digits cannot be input.
b. At the data input against the exponent, last two number are efficient.

(4) • RND
a. The position first pressed has preferenced, and no input is made to data set in the exponent section.
b. When pressed as the first set number, it is regarded as 0 and • keys are pressed.
c. Random as a 2ndF
Pressing this key shall display the random numbers.
The range of random numbers is 0.000-0.999.

(5) +/–
a. In setting data in the mantissa section, this key reverses code in the mantissa section.
Similarly, for exponent section, it reverses code in the exponent section.
b. For the operation result, this key reverses codes in the mantissa section.

(6) + − × ÷ = ( )

a. When the key operations are performed by these keys according to a numerical expression, a result of operation is obtained according to mathematical priorities. Priorities discriminated are;

1) 1 Variable function
2) Expression in ( ); (The most inner expression has priority in case of multiple parentheses)
3) y^x, $\sqrt[x]{y}$
4) ×, ÷
5) +, −

b. Whenever the key is operated, the calculator discrimiuates the above priorities and holds the data and operation keys pending as required.
This pending action is possible up to 6 times and 7 or more pending become error.

c. (Key is accepted only immediately after CE, +, −, ×, ÷, $y3_x$, $\sqrt[x]{y}$, =, (keys and not accepted in all other cases.
When this key is accepted, the displayed data is cleared to 0.
When (key is first accepted, the special display "( )" illuminates.
When a parenthesis expression is completed) and=keys or when it is cleared by ON/C key, etc, or when errors are generated, the special display "( )" goes out.

d. If it is within the allowable range of pending, (can be input into any place in an expression as many times as desired. However, if the key is pressed continuously 16 times or more, it be comes error.

e. From a viewpoint of numerical expression, even when the corresponding C key is not pressed, the operation is not executed if) key is pressed. On the other hand, when (key is pressed and = key is pressed without pressing the corresponding) key, the operation is also completed according to the priority.

(7) Memory calculation (x→M, RM, M+)

a. Memory register "M" used by these keys is the completely independent single memory.
b. Display data is added to "M" (memory register) by M+ key.
If data overflows at this time, the proceeding data is held.
c. Display data is stored in "M" by x→M key.
d. Contents of "M" is displayed by MR key.
e. When data except for 0 is stored in "M", the special display "M" illuminates.

(8) π

a. This key displays a rounded value (3.141592654) of a 12 digit value (3.14159265359) according to the set display format.
b. A value that is used in a subsequent operation is the above 12 digit value.
c. The display is cleared by the following 1st numeric key and a new data is set.

(9) % Calculation

a. When any arithmetic functions or constant mode has not been set, the displayed number is converted from a percentage to a decimal.
Example) 61.5%

	Display
6 1 . 5 %	0.615

b. When = key is pressed after % with any arithmetic function

- Add-on
  $a+b \quad \% \quad = \quad \rightarrow a+\frac{a\times b}{100}$
- Discount
  $a-b \quad \% \quad = \quad \rightarrow a-\frac{a\times b}{100}$
- Percentage
  $a\times b \quad \% \quad = \quad \rightarrow \frac{a\times b}{100}$
  $a\div b \quad \% \quad = \quad \rightarrow \frac{a}{b}\times 100$
- y^x, $\sqrt[x]{y}$
  $a\ y^x\ b \quad \% \quad = \quad \rightarrow a\ \frac{b}{100}$
  $a\ \sqrt[x]{y}\ b \quad \% \quad = \quad \rightarrow \frac{b}{100}$

(10) Trigonometric and arctrigonometric function (1 Variable)
(sin cos tan $\sin^{-1}$ $\cos^{-1}$ $\tan^{-1}$)
These functions are calculated according to respective defined areas and accuracy show in (6), and displayed result of operation can become operators.

(11) Hyperbolic and archyperbolic function.
(hyp → sin cos tan, archyp → sin cos tan)
Same as trigonometric function.

(12) Exponential and logarithmic function.
(e^x 10^x ln log)
Same as tigonometric function.

(13) Reciprocal, square, square root and cube root.
(1/x x^2 $\sqrt{}$ $\sqrt[3]{}$)
Same as trigonometric function.

(14) Factorial function (n!)
n!=nx(n-1)x(n-2)x.....x2x1.
Same as trigonometric function.

(15) →DEG →DMS
a. These keys convert degree, minutes and second into decimal degree and decimal degree into degree minutes and second, respectively.
b. On the DMS format, the integer part of display data is regarded as degree, 2 digits below the decimal point as minute and 3rd digit and below as second.

		1	59	5999
1.999999999	–DMS	degree	minute	second

(16) Coordinate conversion (a b →rθ →xy)
a. These keys convert the rectangular coordinates into the polar coordinates and the polar coordinates into the rectangular coordinates, respectively. The angle unit that have been set by DRG key is followed.
b. Respective defined areas and accruacy are as shown in (6), however, the range of θ obtained by R→P in degree is as follows.

1st	Quadrant	$0° \leq \theta \leq 90°$
2nd	Quadrant	$90° \leq \theta \leq 180°$
3rd	Quadrant	$-180° \leq \theta \leq -90°$
4th	Quadrant	$-90° \leq \theta \leq 0°$

c. Input of 2 variables is performed by setting
x or r by pressing a key and
y or θ by pressing b key.

d. The operation result of x or R is obtained in the display register or by pressing a key and y or θ by pressing b key.

	Input Data		Result	
	a	b	a	b
R→P (Rectangular → Polar)	x	y	r	θ
P→R (Polar → Rectangular)	r	θ	x	y

(→r, θ) $r=\sqrt{x^2+y^2}$, $\theta=\tan^{-1} y/x$
(→x, y) $x=r\cos\theta$, $y=r\sin\theta$

e. (R → P Conversion) ([x, y] → [r, θ])

Key operation	Display
x	x
a	x
y	y
b	y
→rθ	r
b	θ

f. (P → R Conversion) ([r, θ] → [x, y])

θ	θ
b	θ
r	r
a	r
→xy	x
b	y

(17) Binary mode (2ndF, →BIN, 0, 1)

a. Data input and output are both binary integers in maximum 10 digits.
b. A negative number is expressed in binary number of two's complement.
c. The range of internal operation is as shown below and if the result of operation exceed the range, it becomes error (overflow)

	Binary Number	Decimal Number
Outside the operation range	—	512 ≤ DATA
Binary Positive Integer	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 : : 10 1 0	511 510 509 : : 2 1 0
Binary Positive Integer (Complement)	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 0 1 : : 1 0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0	−1 −2 −3 : : −511 −512
Outside the operation range		−512≥DATA

(18) Octal mode (2ndF, →OCT, 0 — 7)

a. Data input and output are both octal integers in maximum 10 digits.
b. A negative number is expressed in octal number display of two's complement.
c. The range of internal operation is as shown below and if the result of operation exceed the range, it becomes error (overflow)

	Octal Number	Decimal Number
Outside the operation range	—	5 3 6 8 7 0 9 1 2 ≤ DATA
Binary Positive Integer	3 7 7 7 7 7 7 7 7 7 3 7 7 7 7 7 7 7 7 6 : : 1 0	5 3 6 8 7 0 9 1 1 5 3 6 8 7 0 9 1 0 : : 1 0
Octal Negative Integer (Complement)	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 6 1 1 1 1 1 1 1 0 1 : : 4 0 0 0 0 0 0 0 0 1 4 0 0 0 0 0 0 0 0 0	−1 −2 : : −5 3 6 8 7 0 9 1 1 −5 3 6 8 7 0 9 1 2
Outside the operation range		−5 3 6 8 7 0 9 1 3 ≥ DATA

(19) Hexadecimal Mode (2ndF, →HEX, 0 — 9, A-F)

a. Data input and output are both hexadecimal integers in maximum 10 digits.
b. A negative number is expressed in hexadecimal number of two's complement.
c. The range of internal operation is as shown below and if the result of operation exceed the range, it becomes error (overflow)

	Hexadecimal Number	Decimal Number
Outside the operation range	—	$1\times10^{10} \leq$ DATA
Hexadecimal Positive Integer	2 5 4 0 B E 3 F F 2 5 4 0 B E 3 F E : : 1 0	9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 8 : : 1 0
Hexadecimal Negative Integer (Complement)	F F F F F F F F F F F F F F F F F F F E : : F D A B F 4 1 C 0 2 F D A B F 4 1 C 0 1	−1 −2 : : −9 9 9 9 9 9 9 9 9 8 −9 9 9 9 9 9 9 9 9 9
Outside the operation range		$-1\times10^{10} \geq$ DATA

(20) Complex number mode (2ndF, CPLX)

a. Pressing these keys shall set the complex number mode.
b. Input of 2 parts is performed by setting the real part (X; pressing a key) and the imaginary part (Y; pressing b key)
c. The operation result of the real part is obtained by pressing = or a key and the imaginary part by pressing b key.

Item	Input Data 1		Function	Input Data 2		Result	
	Real	Imaginary		Real	Imaginary	Real	Imaginary
	a	b		a	b	a	b
Addition	X1	Y1	+	X2	Y2	X1+X2	Y1+Y2
Subtraction	X1	Y1	−	X2	Y2	X1−X2	Y1−Y2
Multiplication	X1	Y1	×	X2	Y2	X1X2−Y1Y2	Y1X2+X1Y2
Division	X1	Y1	÷	X2	Y2	$\frac{X1X2+Y1Y2}{X2^2+Y2^2}$	$\frac{Y1X2-X1Y2}{X2^2+Y2^2}$

(21) Static calculation mode (2ndF, STAT)

a. Pressing these keys shall set the statistic calculation mode.
b. Available number of data is the positive integer, such as $0 \leq n \leq 9999999999$, and when the number of data exceeds this integer, it becomes error.
e. The input range of the data are as follows $0 \leq |\text{ data }| \leq 1\times10^{50}$
This data exceeds the ranges, it becomes error.
d. n Σx Σx²
These keys display the number of data (sample), each sum total of x and sum total of x^2

• Average; $\bar{x} = \frac{\sum_{i=1}^{n} x_i}{n} = \frac{\Sigma x}{n}$

• The standard deviation of the sample

$$s=\sqrt{\frac{\sum_{i=1}^{n}(xi-x)^2}{n^{-1}}}=\sqrt{\frac{\Sigma x^2-(\Sigma x)^2/n}{n^{-1}}}$$

The standard devitation of the population

$$\delta=\sqrt{\frac{\sum_{i=1}^{n}(xi-x)^2}{n}}=\sqrt{\frac{\Sigma x^2-(\Sigma x)^2/n}{n}}$$

ERROR CONDITIONS

(1) The result of operation in exponent parts exceed+99

(2) Entering more than the calculation range (6) of each function.

(3) Dividing by zero.

(4) In statistical calculation.
   a. x, s, σ when n=0
   b. s when n=1

(5) The number of pending operations exceeds 3

(6) The number of the parenthesis in the one level exceed 15

OPERATION RANGE AND ACCURACY.

Function	Angle Unit	Operation Range	Under Flow Area	Normal Accuracy
sin x	DEG	$0\le\|x\|\le4.499999999\times10^{10}$	$0\le\|x\|\le5.729577951\times10^{-98}$	10 digits ±1
	RAD	$0\le\|x\|\le7853981633$	—	
	GRAD	$0\le\|x\|\le4.999999999\times10^{10}$	$0\le\|x\|\le6.366197723\times10^{-98}$	
cos x	DEG	$0\le\|x\|\le4.500000008\times10^{10}$	—	
	RAD	$0\le\|x\|\le7853981649$	—	
	GARD	$0\le\|x\|\le5.000000009\times10^{10}$	—	
tan x	DEG	Same as sin x	Same as sin x	
	RAD	Same as sin x	Same as sin x	
	GARD	Same as sin x	Same as sin x	
$\sin^{-1}$ x	DEG	$0\le\|x\|\le1$	$0\le\|x\|\le1.570796326\times10^{-99}$	
	RAD	$0\le\|x\|\le1$	—	
	GARD	$0\le\|x\|\le1$	$0\le\|x\|\le1.570796326\times10^{-99}$	
$\cos^{-1}$ x	DEG	Same as $\sin^{-1}$x	—	
	RAD	Same as $\sin^{-1}$ x	—	
	GARD	Same as $\sin^{-1}$ x	—	
$\tan^{-1}$ x	DEG	$0\le\|x\|\le9.999999999\times10^{99}$	Same as $\sin^{-1}$ x	
	RAD	$0\le\|x\|\le9.999999999\times10^{99}$	—	
	GARD	$0\le\|x\|\le9.999999999\times10^{99}$	Same as $\sin^{-1}$ x	
ln x		$0\le x$	—	
log x		$0\le x$	—	
e^x		$-9.999999999\times10^{99}\le x\le230.2585092$	$-9.999999999\times10^{99}\le x\le-227.9559243$	

OPERATION RANGE AND ACCURACY. (Continued)

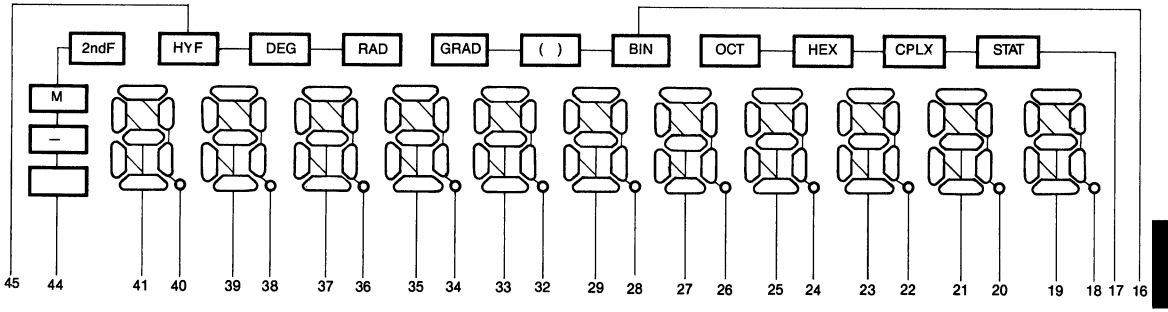
Function	Operation Range	Under Flow Area	Normal Accuracy
10^x	$-9.999999999 \times 10^{99} \le x \le 99.99999999$	$-9.999999999 \times 10^{99} \le x \le -99.00000001$	10 digits ±1
x!	$0 \le x \le 69$ (integer)	—	
$\frac{1}{x}$	$1 \times 10^{-99} \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	$1.000000001 \times 10^{99} \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	
x^2	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{49}$	$0 \le \lvert x \rvert \le 3.162277660 \times 10^{-50}$	
$\sqrt{x}$	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	—	
$\sqrt[3]{x}$	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	—	
DMS→DEG	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{9}$	—	
DEG→DMS	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{9}$	$0 \le \lvert x \rvert \le 2.777777777 \times 10^{-99}$	
sinh x	$0 \le \lvert x \rvert \le 230.2585092$	—	
cosh x	$0 \le \lvert x \rvert \le 230.2585092$	—	
tanh x	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	—	
$\sinh^{-1} x$	$0 \le \lvert x \rvert \le 4.999999999 \times 10^{99}$	—	
$\cosh^{-1} x$	$1 \le x \le 4.999999999 \times 10^{99}$	—	
$\tanh^{-1} x$	$0 \le \lvert x \rvert \le 9.9999999999 \times 10^{-1}$	—	
R→P (x,y) (r, θ)	$\lvert x \rvert, \lvert y \rvert \le 9.999999999 \times 10^{49}$ $(x^2+y^2) \le 9.999999999 \times 10^{99}$	correspond to the under flow area of tan x	
P→R (r, θ) (x,y)	$0 \le r \le 9.999999999 \times 10^{99}$ θ correspond to the operation range of sin x, cos x	θ correspond to the under flow area of sin x, cos x	
DEG→RAD	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	$0 \le \lvert x \rvert \le 5.729577951 \times 10^{98}$	
RAD→GARD	$0 \le \lvert x \rvert \le 1.570796326 \times 10^{98}$	—	
GARD→DEG	$0 \le \lvert x \rvert \le 9.999999999 \times 10^{99}$	$0 \le \lvert x \rvert \le 1.111111111 \times 10^{-99}$	
y^x	$-9.999999999 \times 10^{99} \le x.\ \ln \lvert y \rvert \le 230.2585092$	$-9.999999999 \times 10^{99} \le x.\ \ln \lvert y \rvert \le -227.9559243$	
	i) y>0; The above — mentioned operation range ii) y<0; x (integer) or 1/x (x = odd, x = 0) The above — mentioned operation range iii) y = 0; x>0		
$\sqrt[x]{y}$	$-9.999999999 \times 10 \le \frac{1}{x}.\ \ln \lvert y \rvert \le 230.2585092$	$-9.999999999 \times 10 \le \frac{1}{x}.\ \ln \lvert y \rvert \le -227.9559243$	
	i) y>0; The above — mentioned operation range. ii) y<0; x (odd) or 1/x (integer, x ≒ 0) The above — mentioned operation range. iii) y = 0; x>0		
→DEC	The following operation range after the conversion. $0 \le \lvert x \rvert \le 9999999999$		—
→BIN	The following operation range after the conversion. $1000000000 \le x \le 1111111111,\ 0 \le x \le 1111111111$		—

OPERATION RANGE AND ACCURACY. (Continued)

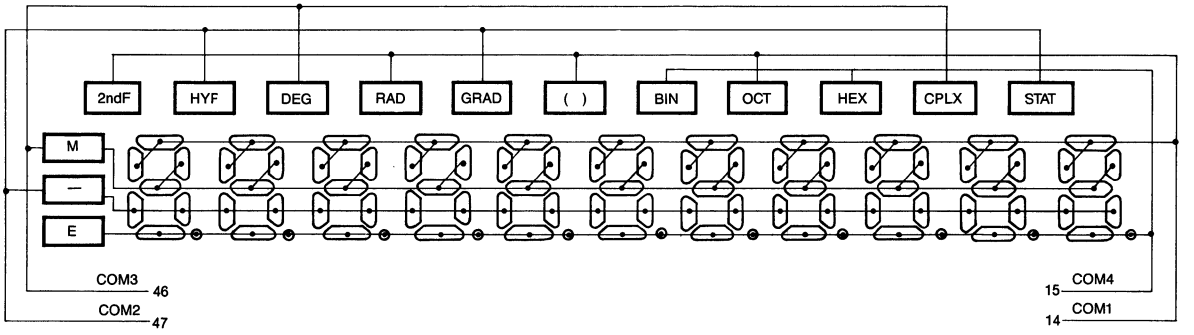
Function	Operation Range Under Flow Area	Normal Accuracy
→OCT	The following operation range after the conversion. $4000000000 \leq x \leq 77777777777, 0 \leq x \leq 37777777777$	—
→HEX	The following operation range after the conversion. $FDABF41C01 \leq x \leq FFFFFFFFFF, 0 \leq x \leq 2540BE3FF$	—
Complex number calculation	(X1+Y1i) +, −, ×, ÷ (X2+Y2i) i) Addition and subtraction $\|X1+X2\| \leq 9.9999999999 \times 10^{99}$ $\|Y1+Y2\| \leq 9.9999999999 \times 10^{99}$ ii) Multiplication $\|X1X2-Y1Y2\| \leq 9.9999999999 \times 10^{99}$ $\|Y1X2-X1Y2\| \leq 9.9999999999 \times 10^{99}$ $\|X1X2\|, \|Y1,Y2\|, \|Y1X2\|, \|X1Y2\| \leq 9.9999999999 \times 10^{99}$ iii) Division $\left\|\frac{X1X2+Y1Y2}{X2^2+Y2^2}\right\|, \left\|\frac{Y1X2-X1Y2}{X2^2+Y2^2}\right\| \leq 9.999999999 \times 10^{99}$ $\|X2^2+Y2^2\|, \|X2^2\|, \|Y2^2\|, \|X1X2+Y1Y2\|, \|Y1X2-X1Y2\|$ $\|X1X2\|, \|Y1Y2\|, \|Y1X2\|, \|X1Y2\| \leq 9.9999999999 \times 10^{99}$	10 digits ± 1
Statistical calculation	i) Data; $\|x\| \leq 9.9999999999 \times 10$ ii) $\|\Sigma x\| \leq 9.9999999999 \times 10$ iii) $\|\Sigma x^2\| \leq 9.9999999999 \times 10$ iv) x; n=0 v) s; n=1 n=0 $0 \leq \frac{\Sigma x^2 - (\Sigma x)^2/n}{n^{-1}} \leq 9.9999999999 \times 10$ vi) σ; n=0 $0 \leq \frac{\Sigma x^2 - (\Sigma x)^2/n}{n} \leq 9.9999999999 \times 10$	10 digits ± 1

LCD CONNECTION

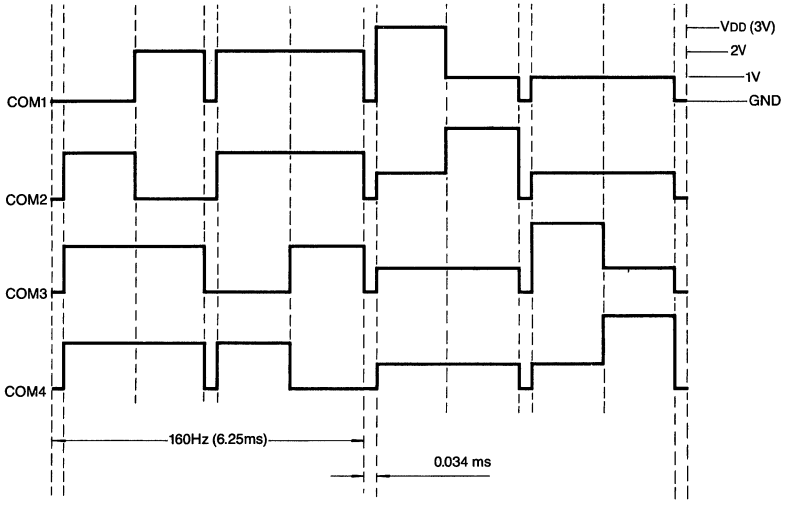
a. Segment



b. Common



WOVEFORM OF COM



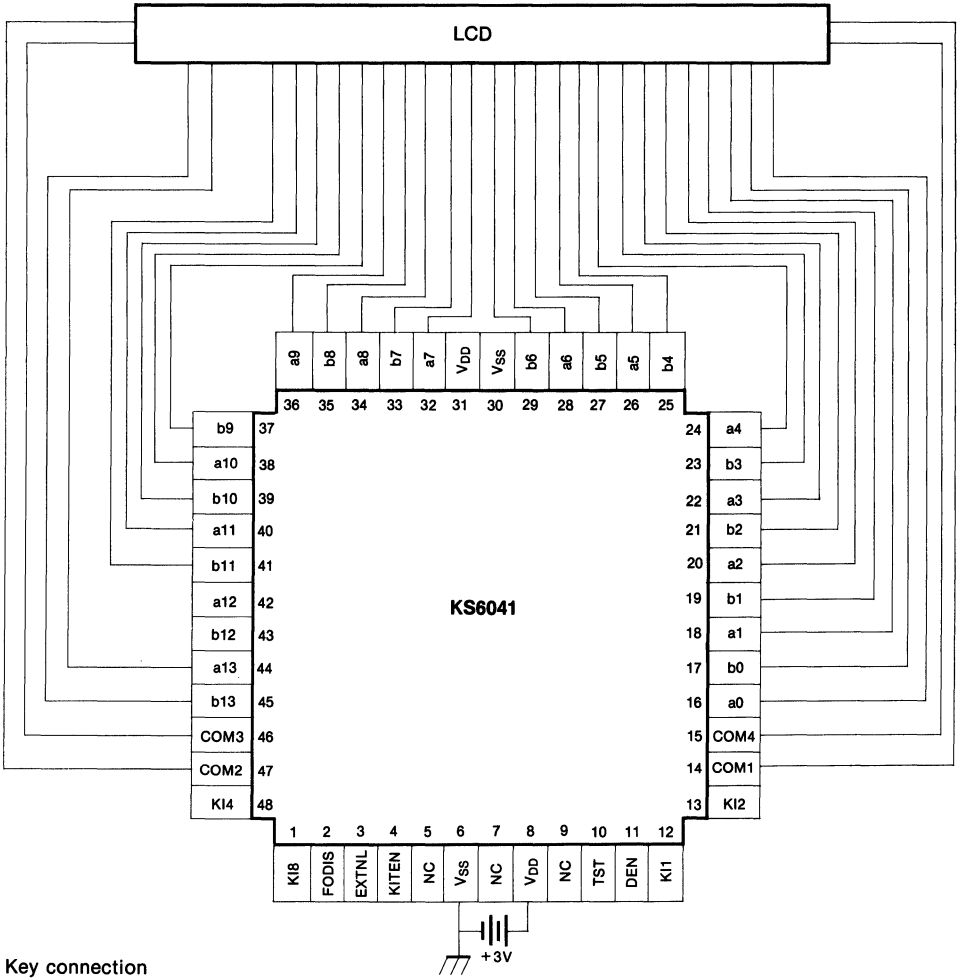
EXTERTAL CONNECTION

(1) Pin description

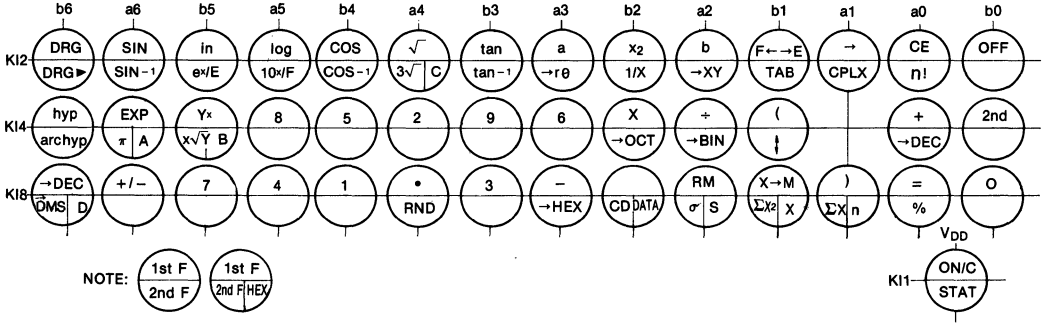
Pin No.	Signal	I/O	Description	Pad No.	Pin No.	Signal	I/O	Description	Pad No.
1	KI8	I	Key input 8	40	25	b4 (KO)	O	LCD (Key output)	16
2	FODIS	I	Fosc disable	41	26	a5 (KO)	O	LCD (Key output)	17
3	EXTNL	I	External clock	42	27	b5 (KO)	O	LCD (Key output)	18
4	KITEN	I	Key in test enable	43	28	a6 (KO)	O	LCD (Key output)	19
5	NC				29	b6 (KO)	O	LCD (Key output)	20
6	V_{SS}		V_{SS} Power (GND)	44	30	V_{SS}		V_{SS} Power (GND)	21
7	NC				31	V_{DD}		V_{DD} Power (+3V)	22
8	V_{DD}		V_{DD} Power (+3V)	45	32	a7	O	LCD	23
9	NC				33	b7	O	LCD	24
10	TST	I/O	Test	1	34	a8	O	LCD	25
11	DEN	I	Dump Enable	2	35	b8	O	LCD	26
12	KI1	I	Key Input 1	3	36	a9	O	LCD	27
13	KI2	I	Key Input 2	4	37	b9	O	LCD	28
14	COM1	O	Common Signal 1	5	38	a10	O	LCD	29
15	COM4	O	Common Signal 4	6	39	b10	O	LCD	30
16	aO (KO)	O	LCD (Key Output)	7	40	a11	O	LCD	31
17	bO (KO)	O	LCD (Key Output)	8	41	b11	O	LCD	32
18	a1 (KO)	O	LCD (Key Output)	9	42	a12	O	No Connection	33
19	b1 (KO)	O	LCD (Key Output)	10	43	b12	O	No Connection	34
20	a2 (KO)	O	LCD (Key Output)	11	44	a13	O	LCD	35
21	b2 (KO)	O	LCD (Key Output)	12	45	b13	O	LCD	36
22	a3 (KO)	O	LCD (Key Output)	13	46	COM3	O	Common Signal 3	37
23	b3 (KO)	O	LCD (Key Output)	14	47	COM2	O	Common Signal 2	38
24	a4 (KO)	O	LCD (Key Output)	15	48	KI4	I	Key Input 4	39

APPLICATION CIRCUIT

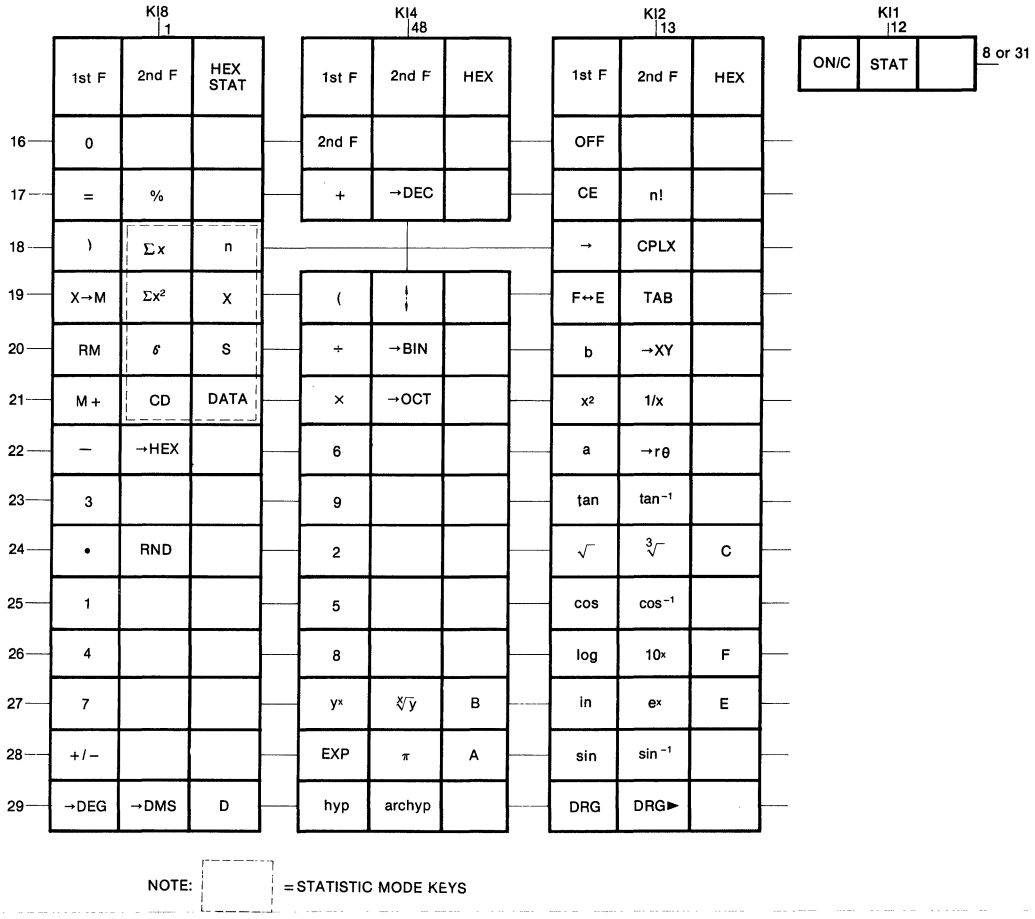
(1) LCD connection



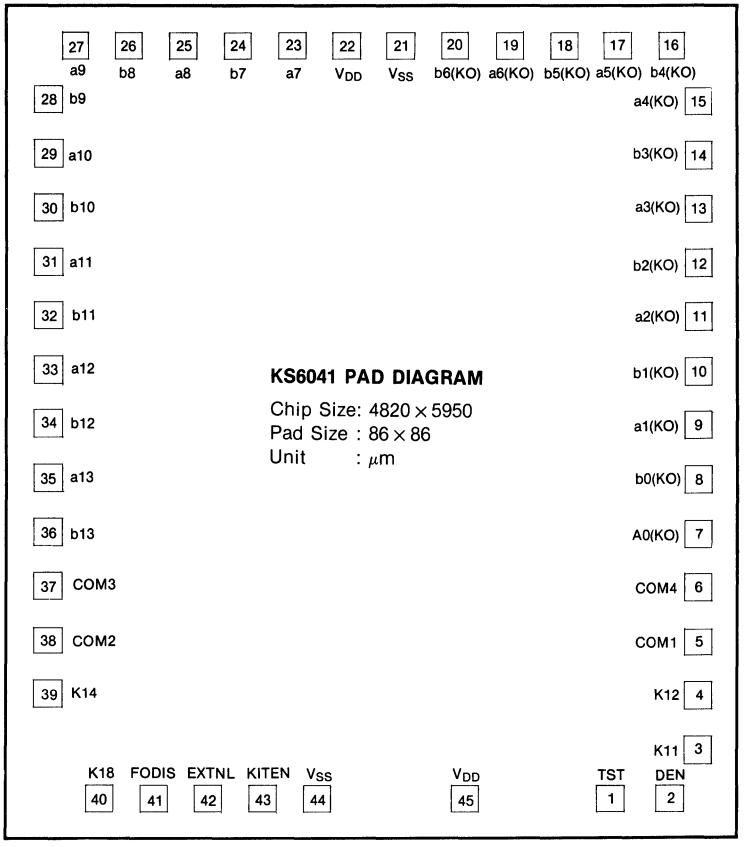
(2) Key connection



KEY CONNECTION



PAD DIAGRAM


27 a9
26 b8
25 a8
24 b7
23 a7
22 VDD
21 VSS
20 b6(KO)
19 a6(KO)
18 b5(KO)
17 a5(KO)
16 b4(KO)
28 b9
29 a10
30 b10
31 a11
32 b11
33 a12
34 b12
35 a13
36 b13
37 COM3
38 COM2
39 K14
a4(KO) 15
b3(KO) 14
a3(KO) 13
b2(KO) 12
a2(KO) 11
b1(KO) 10
a1(KO) 9
b0(KO) 8
A0(KO) 7
COM4 6
COM1 5
K12 4
K11 3
K18 40
FODIS 41
EXTNL 42
KITEN 43
VSS 44
VDD 45
TST 1
DEN 2
KS6041 PAD DIAGRAM
Chip Size: 4820 x 5950
Pad Size : 86 x 86
Unit : μm

NOTES

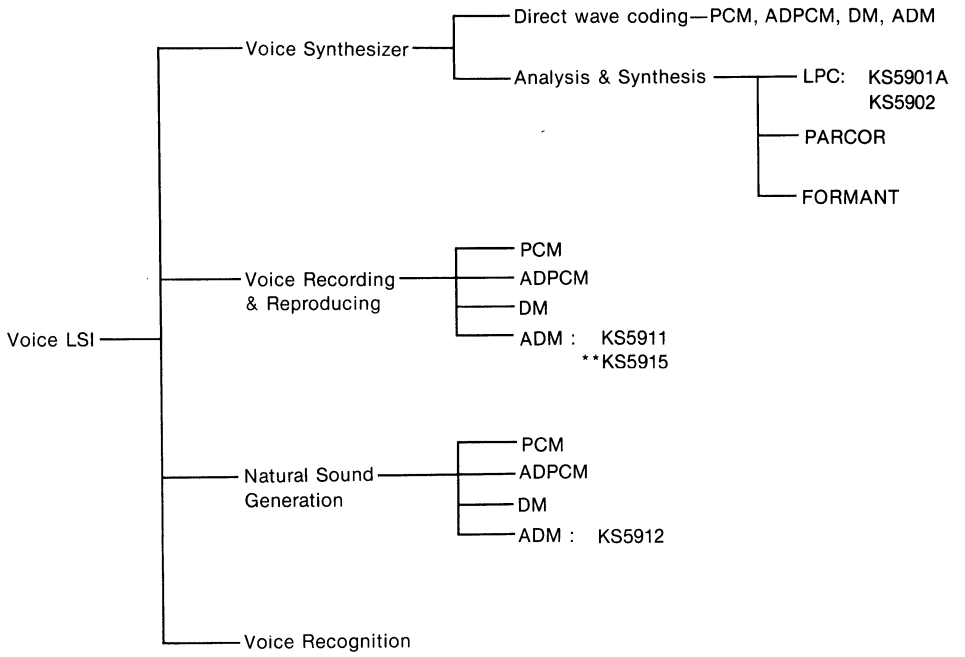
5

Voice Synthesizer ICs

Device	Function	Package	Page
KS5901	CMOS 1 Chip Voice Synthesizer (External EPROM)	64 SDIP	•
KS5901A	CMOS 1 Chip Voice Synthesizer (External EPROM)	60 FQP	213
KS5902XX	CMOS 1 Chip Voice Synthesizer (Internal ROM)	24 DIP	234
KS5911	CMOS 1 Chip Voice Recorder & Reproducer (External DRAM)	48 FQP	248
KS5912XX	CMOS 1 Chip Voice & Sound Generator (Internal ROM)	16 DIP	260
**KS5915	CMOS 1 Chip Voice & Sound Generator (External DRAM)	60 FQP	•

** Under Development

1. CLASSIFICATION OF VOICE LSI



PCM : Pulse Code Modulation.
ADPCM : Adaptive Differential Pulse Code Modulation.
DM : Delta Modulation.
ADM : Adaptive Delta Modulation.
LPC : Linear Predictive Coding.
PARCOR : Partial Auto-Correlation.

NOTE: **Under Development

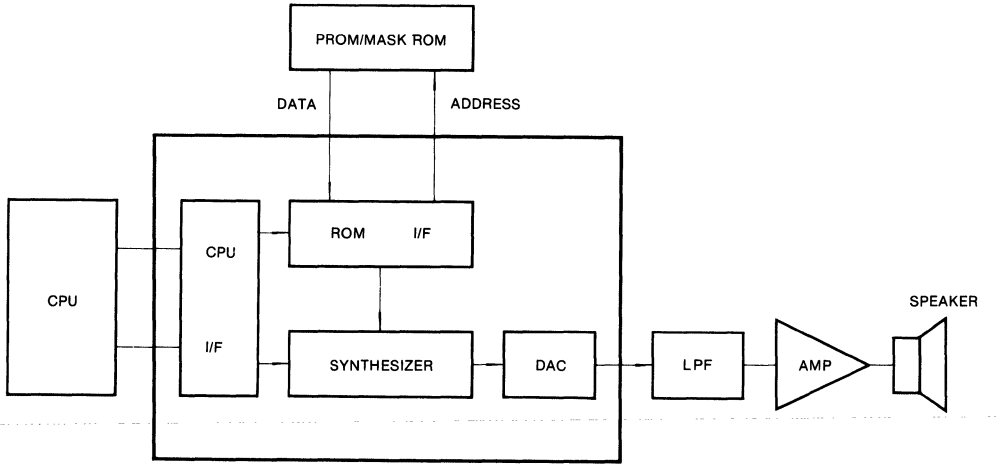
2. VOICE SYNTHESIZER

2-1. External ROM Type: KS5901/KS5901A

A. FEATURES

- Voice synthesis method: LPC
- 640 KHz X-tal oscillation
- 8 KHz sampling frequency
- Control mode: CPU/manual mode
- Various synthesis speed: 0.7 – 1.55 times of normal speed
- Direct access to the external ROM (x 8 Bit)
- Maximum memory size: 64 KBytes (KS5901A), 512KBytes (KS5901)
- Easy interface with CPU
- On chip 9 Bits R-2R D/A converter
- Single 5V power supply
- PKG: KS5901: 64 SDIP
  KS5901A: 60 FQP

B. BLOCK DIAGRAM



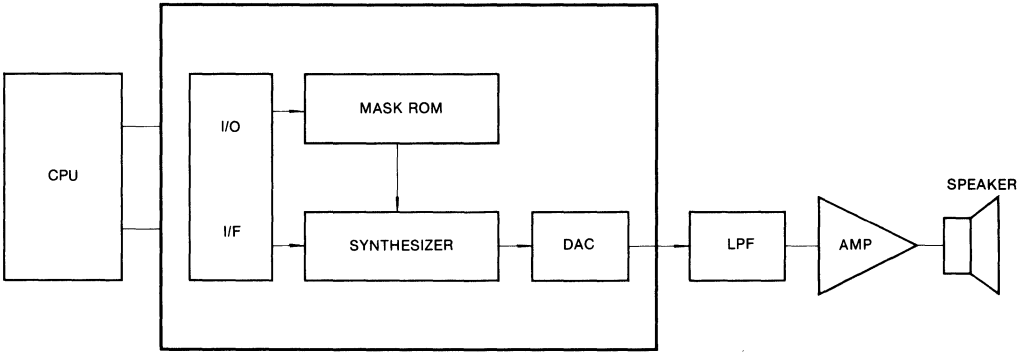
KS52000 KS5901A

2-2. Internal ROM Type: KS5902

A. FEATURES

- Speech synthesis method: LPC
- 2.56 MHz X-tal oscillation
- 8 KHz sampling frequency
- Control mode: CPU/manual mode
- Various synthesis speed: 0.7~1.55 times of normal speed
- Various speech synthesis conditions
- 48 KBits on chip data ROM
- Easy interface with CPU
- On chip 9 Bits R-2R D/A converter
- Single 5V power supply
- Low power consumption by C^2MOS structure
- PKG: 24 Dip

B. BLOCK DIAGRAM

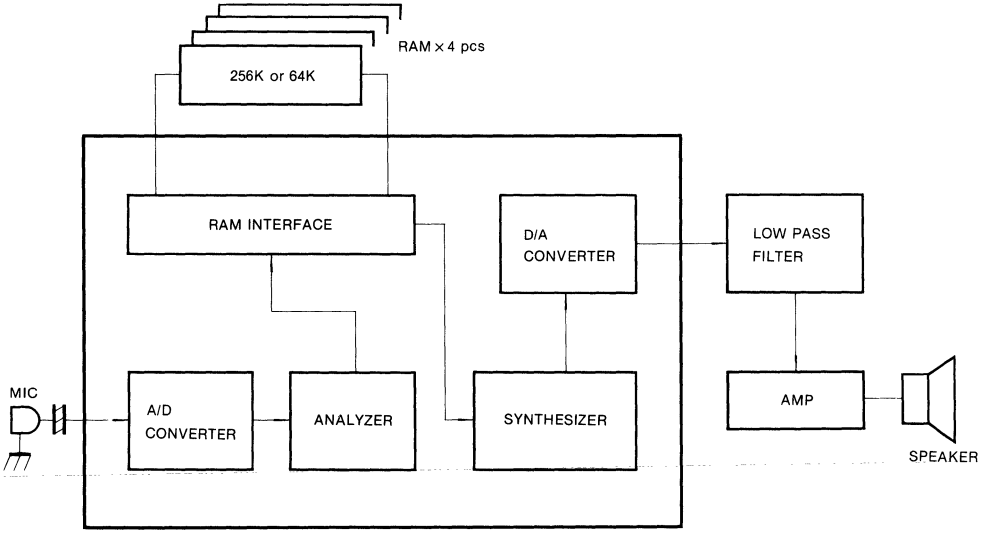


3. VOICE RECORDING & REPRODUCTION LSI: KS5911

A. FEATURES

- Speech analysis & synthesis method: ADM
- RC oscillator: 640 KHz
- Selectable bit rate: 8K, 11K, 16K, 32Kbps
- Control mode: Talking back mode/manual control mode
- Data memory: 64K or 256K DRAM up to 4pcs
- Auto silence detection (Talking back mode)
- Recording/Reproducing of max. 16 phrases (Manual control mode)
- Built-in DRAM refresh counter
- Built-in microphone amplifier & 10 Bits D/A converter
- Single 5V power supply
- Low power consumption by C^2MOS structure
- PKG: 48 FQP

B. BLOCK DIAGRAM



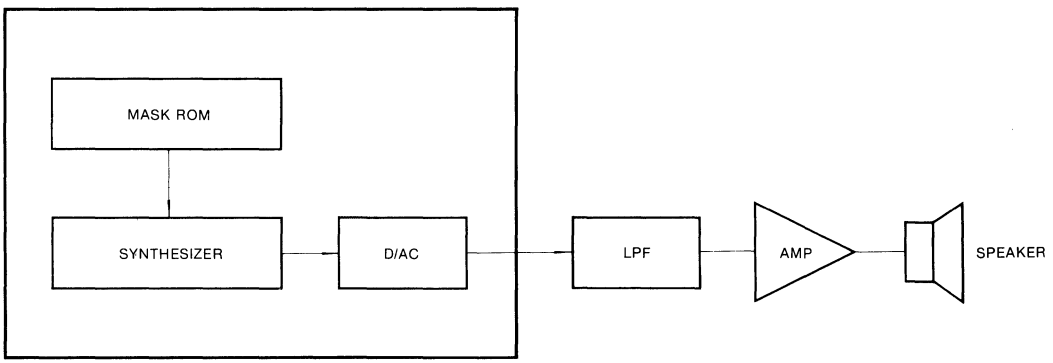
KS5911

4. VOICE & SOUND GENERATOR: KS5912

A. FEATURES

- Sound synthesis method: ADM
- On-chip 64KBits mask ROM
- RC oscillator: 640 KHz
- Control mode: Manual control
- Variable bit rate (Mask option): 32K, 16K, 11K, 8Kbps
- Repeat function: 3 times/8 times
- Phrase selectable: 4 phrase
- Maximum generation time: 8 sec. (8 KHz sampling)
- On-chip 10 Bit D/A converter
- Single 5V power supply
- Low power consumption by C^2MOS logic
- PKG: 16 Dip

B. BLOCK DIAGRAM



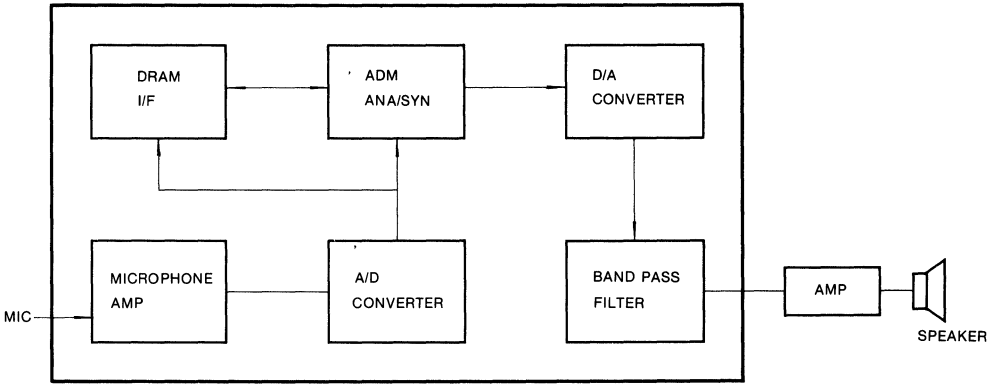
KS5912

5. VOICE RECORDING & REPRODUCING LSI: KS5915

A. FEATURE

- Speech analysis & synthesis method: ADM
- Resonator oscillator: 640 KHz
- Selected bit rate: 11K, 16K, 24K, 32Kbps
- Control mode: CPU/manual
- Data memory: 256K or 1M DRAM up to 4pcs
- Recording/reproducing of max. 16 phrases
- Built-in DRAM refresh counter
- Built-in microphone amplifier & 10 bits D/A converter
- Built-in band pass filter
- Voice trigger in recording (Option)
- Normal mode/256K fixed mode
- PKG: 60 FQP

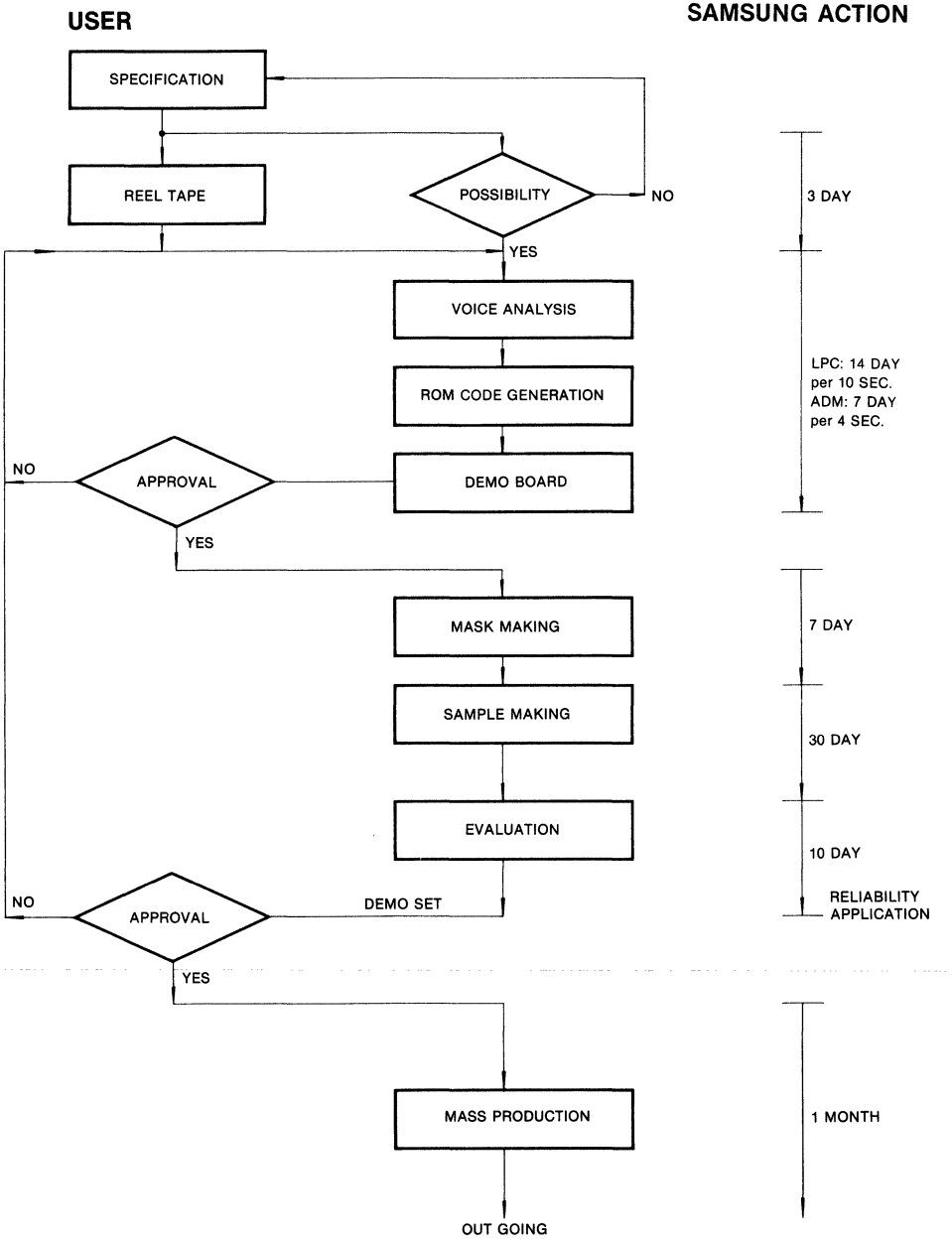
B. BLOCK DIAGRAM



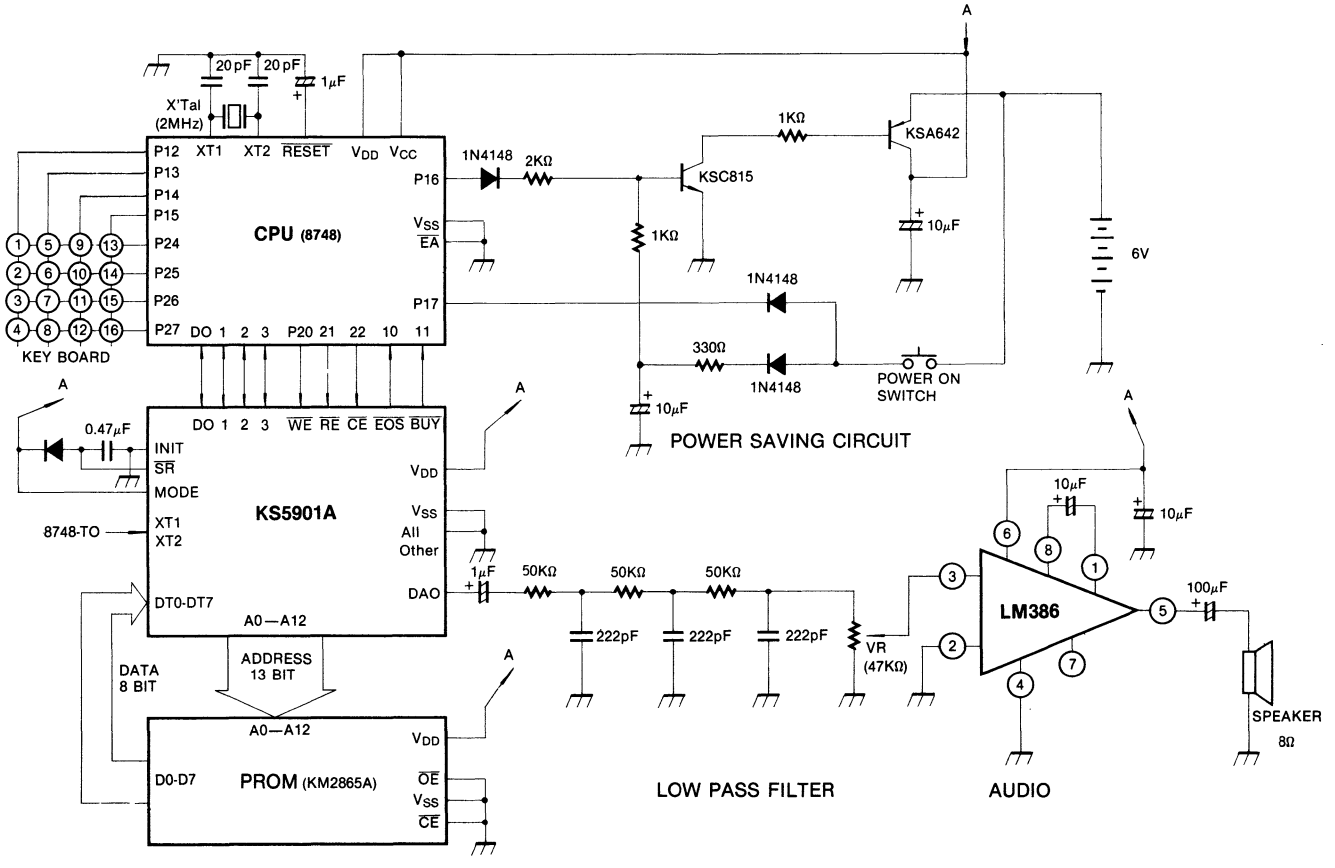
6. SYNTHESIS LSI FUNCTIONS TABLE

Features	KS5901/KS5901A	KS5902XX	KS5911	KS5912XX	KS5915
Synthesis Method	LPC	LPC	ADM	ADM	ADM
Operating Voltage	5V	5V	5V	5V	5V
Oscillation Frequency	640 KHz (X-Tal OSC)	2.56 MHz (X-Tal OSC)	640 KHz (RC OSC)	640 KHz (RC OSC)	640 KHz (X-Tal OSC)
Sampling Frequency	8 KHz	8 KHz	8-32 KHz	8-32 KHz	16-32 KHz
Bit Rate	2.4-9.6 Kbps	2.4-9.6 Kbps	8-32 Kbps	8-32 Kbps	16-32 Kbps
Control Mode	CPU/Manual	CPU/Manual /Auto	Talk-Back/ Manual	Manual	CPU/Manual
Data Memory	External ROM 512KBytes/64KBytes	Internal ROM 48Kbits	External RAM 64K/256K x 4	Internal ROM 64KBits	External RAM 256K/1M x 4
Speech Time	Max. 10 Min./4 Min.	Max. 20 Sec.	Max. 2 Min.	Max. 8 Sec.	Max. 8 Min.
D/A Converter	9 bits	9 bits	10 bits	10 bits	10 bits
PKG	64 SDIP/60 FQP	24 DIP	48 FQP	16 DIP	60 FQP
Applications	HA A/M	Toy Simple Sound Information	Message Phone A/M	Toy	Message Phone A/M

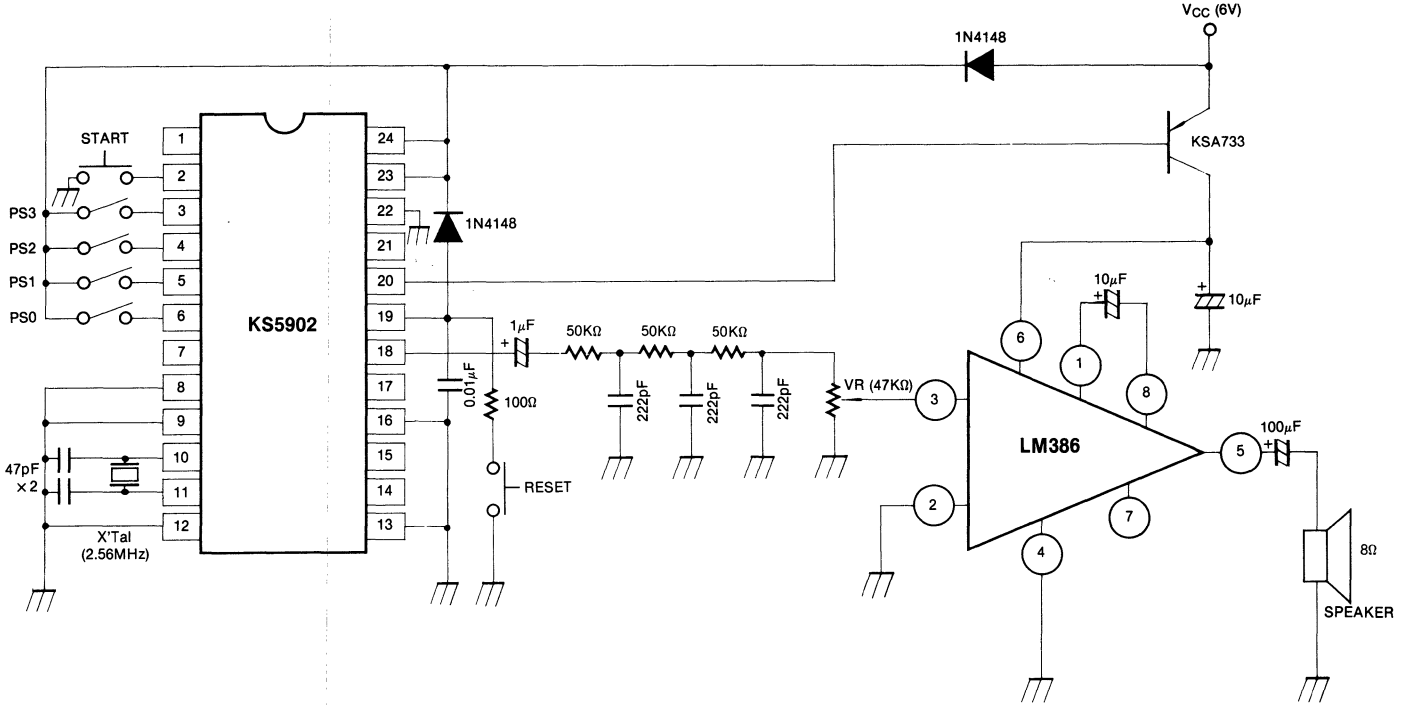
7. VOICE SYNTHESIS LSIs DEVELOPMENT FLOW



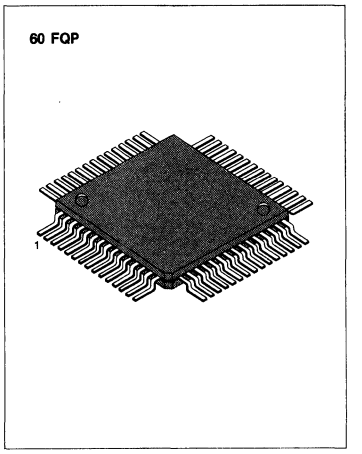
KS5901A APPLICATION CIRCUIT (CPU MODE)



KS5902XX APPLICATION CIRCUIT (KEY MODE)



CMOS 1-CHIP SPEECH SINTHESIZER



The KS5901A is a CMOS speech synthesizer which is developed by Samsung Semiconductor and Telecommunications Co., Ltd. (SST). SST has undertaken a research & development program on an encoded reproduction algorithm called linear predictive coding (LPC). Speech is synthesized by processing an externally provided variable bit stream of LPC encoded speech data, and converting the results to the audible output with an on-chip 9 bits D/A converter.

The speech synthesis system using KS5901A is composed of the following three chips;

KS5901A : CMOS speech synthesizer
PROM : Commercial non-volatile memory (×8 bit)
Micom/μ-processor: 4/8 bits system controller (CPU mode)

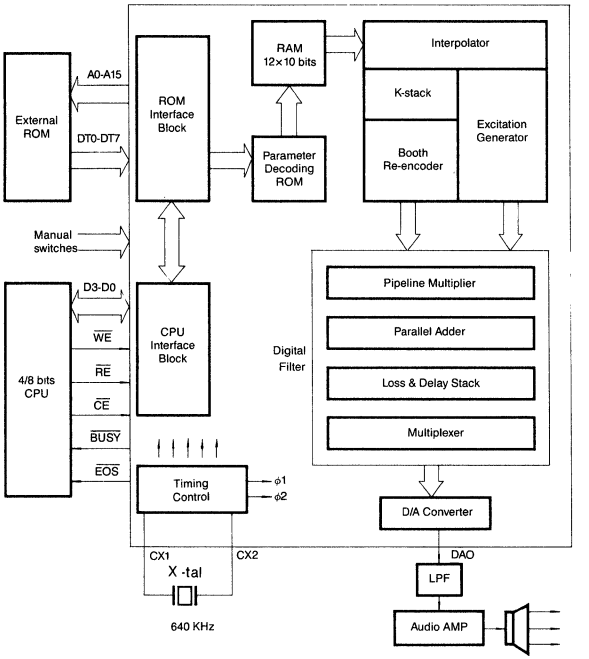
With a considerable memory expansion and controller interfacing capacity, the KS5901A performs speech synthesis operation required for various applications. As the KS5901A is a CMOS LSI, the power consumption is small enough to satisfy the power specification.

5

FEATURES

- **Speech synthesis method; LPC (Linear Predictive Coding)**
- **640 KHz crystal oscillation**
- **8 KHz sampling frequency**
- **Control mode; CPU control/manual control**
- **Various synthesis speed; 0.7-1.55 times of normal speed.**
- **Various speech synthesis conditions;**
  - **. Excitation source**
    Voiced speech; impulse/triangular pulse
    Unvoiced speech; white Gaussian noise
  - **. Bit allocation/frame**
    48 bits/frame; nonlinear transformation
    96 bits/frame; linear transformation
  - **. Frame length; 10/20msec per frame**
  - **. Repetition of the speech parameter set is possible.**
  - **. Loss factor of the synthesis filter is controllable.**
  - **. Variable stage of the digital filter; 8/10 stage.**
- **Direct access to the external ROM (×8 bit)**
- **Maximum memory size; 64K bytes**
- **Easy interface with CPU**
  - **. 4 bits interface bus line**
  - **. 12-kinds of command**
  - **. Monitoring the 4 kinds of status flags**
  - **. $\overline{\text{BUSY}}$, $\overline{\text{EOS}}$ (End of speech) output**
  - **. External ROM data dump mode**
  - **. Less CPU overhead**
- **On chip 9 bits R-2R D/A converter**
- **Low power consumption due to the 2-phase CMOS structure**
- **Single +5V power supply**

BLOCK DIAGRAM



*) LPF: LOW PASS FILTER

Fig. 1 KS5901A functional block diagram

PIN CONFIGURATION

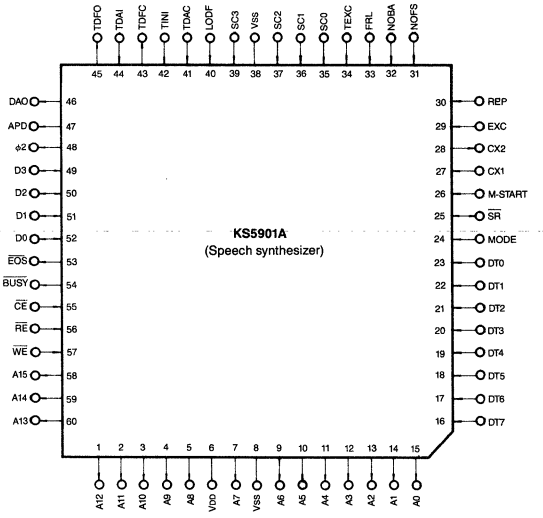


Fig. 2 Pin configuration (60 FQP top view)

PIN DESCRIPTION

Pin (No.)	Name	Input/Output	Function
$A_{15} \sim A_0$ (58-60, 1-5, 7, 9-15)	Address output	Output	Used for external PROM Interface (16 bits address line)
$DT_7 \sim DT_0$ (16-23)	Data input	Input	Used for speech data input from external PROM (8 bit data line)
MODE (24)	Mode switch	Input	Selects CPU or manual control mode H: CPU control L: manual control
$\overline{SR}$ (25)	System reset	Input/Output	System reset. Clears internal registers. (active low)
M-START (26)	Manual start	Input	In the manual control mode, M-START signal initiates reading of external ROM data, starting the synthesis operation.
CX1 (27) CX2 (28)	Oscillator	Input Output	Pins for connecting crystal oscillator
EXC (29)	Excitation source	Input	H: Triangular pulse L: Impulse
REP (30)	Parameter repetition	Input	H: Without repetition L: With repetition
NOFS (31)	Number of filter stages	Input	H: 8-stages L: 10 stages
NOBA (32)	Number of bit allocation	Input	H: 96 bits/frame L: 48 bits/frame
FRL (33)	Frame length	Input	H: 10 msec/frame L: 20 msec/frame
LODF (40)	Loss of digital filter	Input	H: With Loss L: Without Loss
			(In the manual control mode, these pins must be selected to "H" or "L" according to the synthesis conditions.
TEXC (34) TDAC (41) TINI (42) TDAI (44)	Test	Input	Pins for LSI Test (normally ground)
TDFC (43) TDFO (45)	Test	Output	Pins for LSI test (these pins should be open.)
$SC_3 \sim SC_0$ (39, 37-35)	Speed select	Input	In the manual control mode, the synthesis speed follows the "H"/"L" combination of SCO-SC3. Synthesis speed is varied from 0.7 to 1.55.
DAO (46)	D/A output	Output	9 bits R-2R D/A converter output
APD (47)	Audio power down	Output	Controls the power of external audio circuit
$\phi 2$ (48)	System clock	Output	160 KHz system clock output

(continued)

Pin (No.)	Name	Input/Output	Function
$D_3 \sim D_0$ (49-52)	CPU interface bus	Input/Output	Used for CPU interface. When $\overline{WE}$ and $\overline{CE}$ are set to low, these pins are used for command input. When $\overline{RE}$ and $\overline{CE}$ are set to low, these pins are used for monitoring the status flags or reading external ROM data. When $\overline{CE}$ is high, these are in tri-state.
$\overline{EOS}$ (53)	End of speech	Output	When the synthesis operation is terminated by END1 code, $\overline{EOS}$ output is set to low level during one frame. (10/20 msec)
$\overline{BUSY}$ (54)	Busy output	Output	In the CPU control mode, Busy signal is generated by $\overline{WE}/\overline{RE}$ or Osc. enable. (active low)
$\overline{CE}$ (55)	Chip enable	Input	Enables the KS5901A to accept command from CPU during $\overline{WE}$ or to transmit data to CPU during RE pulse. (active low)
$\overline{RE}$ (56)	Read enable	Input	If $\overline{RE}$ is active, CPU can read the LSI, (active low)
$\overline{WE}$ (57)	Write enable	Input	If $\overline{WE}$ is active, CPU can write to the LSI, (active low)
V_{SS} (8, 38)	Power	Input	Ground input
V_{DD} (6)	Power	Input	Supply voltage input (+5V)

(Tab. 1. KS5901A pin description)

*)"H" or high is 5V
"L" or Low is 0V

FUNCTIONAL DESCRIPTION

CPU control mode

When MODE pin is set to "H", the KS5901A switched into the CPU control mode in which the general micom/μ-processor can control the speech synthesizer. The KS5901A supports the 12 commands which make it possible to control the operation and synthesis conditions. It also provides 4 kinds of status flags which represent internal status of KS5901A. Thus, this mode provides the great flexibility for many applications of KS5901A.

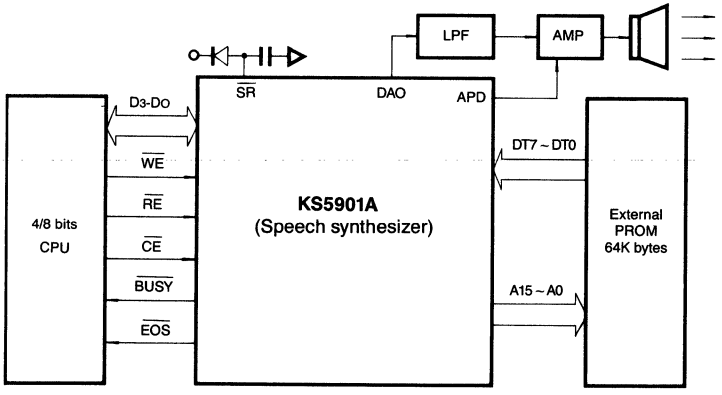


Fig. 3 System configuration in the CPU control mode

1. Commands of KS5901A

A. One nibble commands

(1) ODIS (Oscillator DISable)

This command is used to disable the internal clock oscillation of KS5901A. If the command is given, APD output and status flag of D1 (see 8 page) are set to "H", and the address counter is set to 0000H, and condition values are all cleared, and then KS5901A is turned into the reset state, as $\overline{SR}$ outputs "L" level.

(2) OENA (Oscillator ENAble)

This command releases the ODIS state and resets status flag of D1. After this command, the KS5901A becomes power-on transient state during about 40msec and the $\overline{BUSY}$ outputs the "L" level during that period. As APD output remains "H" level, AENA command should be given so as to enable the external audio circuit.

(3) ADIS (Audio DISable)

If this command is given, APD output is set to "H" level. This command is used to control the power of external audio circuit.

(4) AENA (Audio ENAble)

If this command is given, APD output is set to "L" level. This command is used to control the power of external audio circuit.

(5) STRT (STaRT synthesis operation)

This command is used to start the synthesis operation as reading the external ROM data from where the address counter points.

(6) STOP (STOP synthesis operation)

This command controls KS5901A to stop the synthesis operation. The KS5901A is changed into the stand-by state, while it hold the address counter, the synthesis conditions, speed condition and APD state. This is used to reset "ROM data error" and "command error" status flag.

(7) DDMP (Data DuMP mode)

This command is used to set the data dump mode. In this mode the CPU can read the contents of the external ROM nibble by nibble. When CPU perform its 1st read operation under DDMP mode, 4 bits data ($b_4 \sim b_1$) of the specified address are fetched through data bus ($D_3 \sim D_0$). 2nd read operation enables higher 3 bits ($b_7 \sim b_5$) and LSB 1 bit of the next address (b_0) to be dumped through $D_2 \sim D_0$ and D_3 of data bus respectively. This operation sequence can be continued, and thus the external PROM data can be read into CPU in this mode. It should be noticed that the initial LSB 1 bit (b0) at the specified address is lost because it is treated as the header bit in the KS5901A. Either the speech data or the non-speech data can be stored in the external PROM. By using this mode, the indirect addressing of speech data, i.e., label addressing method, can be carried out. (see 10 page)

(8) NOP (No OPeration)

This command has no effect on the KS5901A except releasing the data dump mode.

(9) Extra command

The KS5901A is not influenced by this command, however the "command error" flag is set to "H" level.

B. Two nibbles commands

(1) LDSPD (LoaD SPeeD code)

This command specifies the synthesis speed with 4 bits data followed by. (refer to Table 6)

(2) LDCON1 (LoaD CONdition 1)

This command specifies the conditions such as the bit allocation per frame, the frame length, the parameter repetition and the stages of digital filter with the successive 4 bits data. (refer to Table 4)

(3) LDCON2 (LoaD CONdition 2)

This command specifies the type of excitation source, the loss factor of the synthesis filter with the successive 4 bits data.

C. Six nibbles command

(1) LDADR (LoaD ADdResses)

The command specifies the start address of the phrase to be synthesized or the PROM data to be read by data dump mode with the successive 5 nibbles data which follow the LDADR command. (refer to page 10)

D. Notice

If any command is given to the KS5901A, the command execution is started between the rising edge of the $\overline{WE}$ signal and internal busy (IBUSY-see page 11) duration. Fig. 4 and 5 illustrate the timing diagrams associated with the command execution and the synthesis operation.

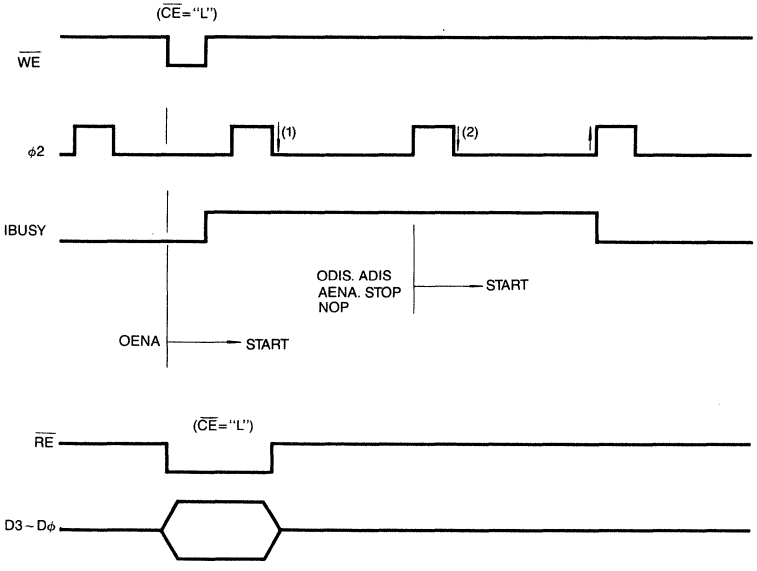


Fig. 4 Timing diagram of the execution of commands

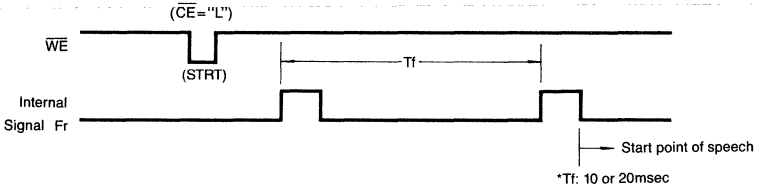


Fig. 5 Timing diagram of the synthesis operation

	Mnemonic	Code Format	Operation	IBUSY Duration
1 nibble Command	ODIS	1001	Oscillator disable, Reset.	3 T max.*
	OENA	1011	Oscillator enable.	3 T max.*
	ADIS	1010	Audio power off. (APD: H)	3 T max.*
	AENA	0100	Audio power on. (APD: L)	3 T max.*
	DDMP	1000	Set data dump mode	10 T max.
	STRT	0001	Start synthesis operation	3 T max.
	STOP	0010	Stop synthesis operation	3 T max.
	NOP	0000	No operation.	3 T max.
	Extra command	11XX	Extra commands	3 T max.
2 nibbles Command	LDSPD	0101, XXXX	Set speed	3 T max.
	LDCON1	0111, XXXX	Set synthesis condition 1	3 T max.
	LDCON2	0110, XX00	Set synthesis condition 2	3 T max.
6 nibbles Command	LDADR	0011 n n n n n**	Set address counter (A15 ~ A0)	3 T max.

*)T: 6.25μsec typ.
**) n: any 1 nibble data.

Tab. 2. KS5901A Commands

	Operation	–BUSY Duration	Caution
$\overline{RE}$	Reading status or ROM data. 2 nibbles, 6 nibbles mode is released.	Status read; 3T ROM data dump; 10T	No execution during IBUSY

Tab. 3 $\overline{RE}$ operation

2. Synthesis conditions and speed code

The synthesis conditions are determined according to the required quality of the synthesized speech and the memory size. The synthesis conditions and speed are specified by LDCON1, LDCON2, and LDSPD commands as previously described.

Condition		Synthesis Condition 1	Synthesis Condition 2
Data bus	Data	LDCON1	LDCON2
D3	L H	48 bits/frame 96 bits/frame	Excitation; Impulse Triangular pulse
D2	L H	20 msec/frame 10 msec/frame	Without loss effect With loss effect
D1	L H	Parameter; repetition no repetition	Not used Always "L"
D0	L H	Filter stages: 10 stages 8 stages	Not used Always "L"

Tab. 4. Synthesis conditions code

Table 5 and 6 illustrate the data bit-rates associated with the synthesis conditions, and the synthesis speed corresponding to each code.

Bit Allocation	Frame Legnth	Parameter Repetition	Bit Rate (Kbps)
48 bits/frame	20msec/frame	Yes	≈2.4
48 bits/frame	20msec/frame	No	
48 bits/frame	10msec/frame	Yes	≈4.8
48 bits/frame	10msec/frame	No	
96 bits/frame	20msec/frame	Yes	≈4.8
96 bits/frame	20msec/frame	No	
96 bits/frame	10msec/frame	Yes	≈9.6
96 bits/frame	10msec/frame	No	

Tab. 5. Synthesis conditions and bit rate

Data bus HEX data	Speed rate	Data bus HEX data	Speed rate
0	1.0*	8	1.4
1	0.7	9	1.5
2	0.8	A	1.55
3	0.9	B	1.0
4	1.0	C	1.0
5	1.1	D	1.0
6	1.2	E	1.0
7	1.3	F	1.0

*Original speed = 1.0

Tab. 6. Speed control code

3. Internal status flags.

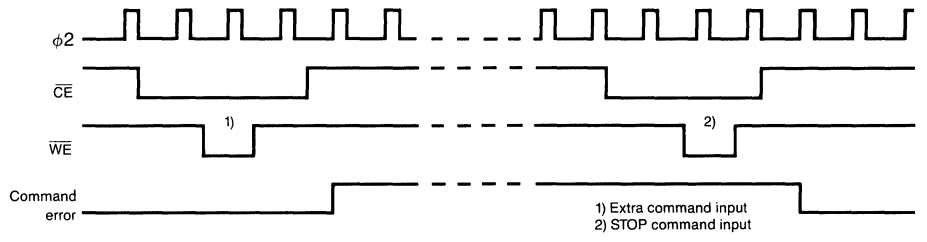
If $\overline{RE}$ signal is given under the normal operation modes except data dump mode, the 4 kinds of internal status 4 bits data bus (D3-D0) of KS5901A. Table 7 shows the summary of the internal status flags. Fig. 6 illustrates the timing associated with it's occurances.

Data Bus	Status Output	Occurance ("H")	Release ("L")
D3	Command error	• Timing error in the interface • Extra command	• Stop command • Power-on reset • Osc. disable
D2	ROM data error	• Nonexistent data • 1st frame data are all high ("I")	• Stop command • Power-on reset • Osc. disable
D1	Osc. disable	• Oscillator disable state	• Osc. enable
D0	End of speech	• Under stand-by state • Stop speech	• Under synthesis operation

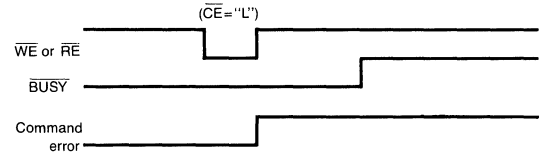
Tab. 7. Summary of the status flags

A. Command error (D3)

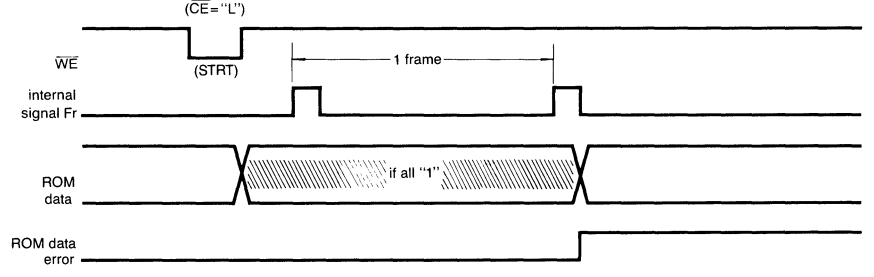
(1) Extra command input



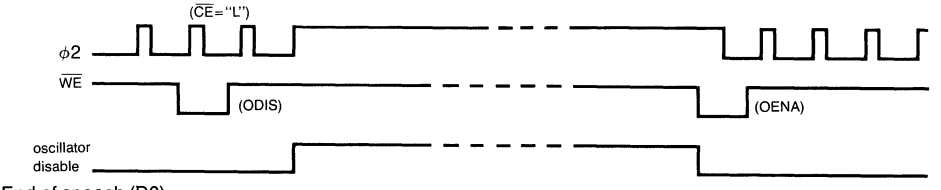
2. When BUSY is activated CE



B. ROM data error (D2)



C. Oscillator disable (D1)



D. End of speech (D0)

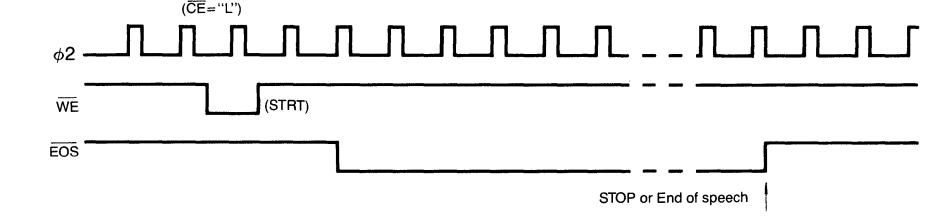


Fig. 6 Timing diagrams of the internal status flags

4. Setting the start address

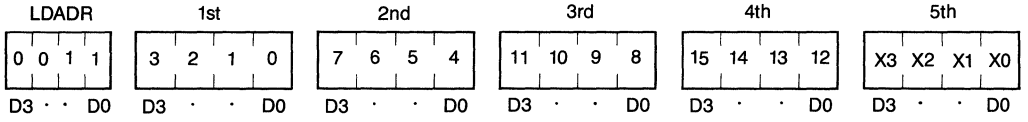
There are two ways of setting the start address of the phrase under CPU control. One is Direct addressing and the another is Indirect addressing.

A. Direct addressing

This addressing is the way to set up the start address of the phrase by directly loading the address data into the KS5901A.

* A start address is given to the 19 bits address counter by LDADR command together with the successive 5 nibbles data, of which the 5th nibble is dummy data. (see appendix)

Input format



Address in address counter

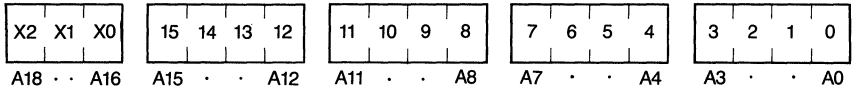


Fig. 7. ROM start address

- After loading the start address, the STRT command initiates the KS5901A to read the external ROM data and start the synthesis operation.
- The address counter continues to increase during synthesis operation until END1 code of the ROM data is detected.
- When END1 code is detected address counting is stopped and the KS5901A returns to the stand-by state.
- In stand-by state, the synthesis operation of the phrase currently addressed can be activated by STRT command
- If END2 code is detected, the start address previously specified by LDADR command is fed to the address counter, and the synthesis operation is repeated. The repetition is continued until the external control, such as STOP/ODIS command or system reset, is given.

B. Indirect addressing

In this mode, some part of speech data ROM is used to the index area. The label must be given to each phrase to be synthesized. The contents stored at the label address are used as the real start address. Address loading sequence of Indirect addressing mode is as follows.

- Using LDADR command, CPU loads the label address of the phrase to be synthesized to the address counter.
- Using DDMP command, CPU reads the start address data (3 bytes), i.e., the contents in the memory location pointed to by the label address and the next two addresses. And save then at the temporary area in the controller.
- Using LDADR command, CPU loads the real start address to the address counter of the KS5901A.
- The real start address must be stored in the format shown in Fig. 8 & 9. The LSB (b0) at the label address should be excluded in storing the start address. As the KS5901A has the addressing range of A0-A15, the last byte only contains one bit address data of A15 at the LSB (b0) and the other bits (b7 ~ b1) become dummy data. (see appendix)
- The control procedures are explained as follows. (refer Fig. 8 & 9)

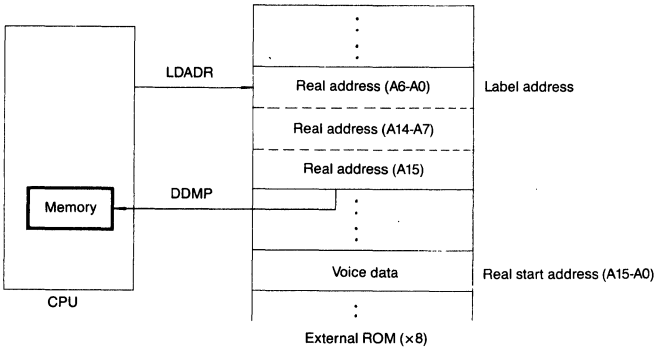


Fig. 8 Setting the label address

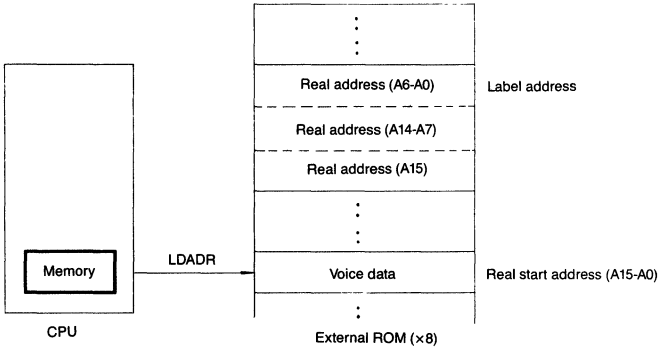


Fig. 9 Setting the real start address.

5. $\overline{\text{BUSY}}$ output

$\overline{\text{BUSY}}$ is generated in the follows:

A. During the execution time of the DDMP command and it's successive $\overline{\text{RE}}$.

$\overline{\text{BUSY}}$ is enabled during from the rising edge of the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ to the rising edge after the 9th falling of $\phi 2$. (10 T max.)

B. During the execution time of the other command or $\overline{\text{RE}}$ for status read.

$\overline{\text{BUSY}}$ is enabled during from the rising edge of the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ to the rising edge after the 2nd falling of $\phi 2$. (3 T max.) See fig. 10.

C. During power-on transient state.

Power switch ON or OENA command causes the KS5901A to be in power-on transient state, of which duration is fixed by the external capacitor connected to $\overline{\text{SR}}$ pin. In transient state, normally 40msec, KS5901A is initialized in it's internal state, and outputs $\overline{\text{BUSY}}$ signal. The $\overline{\text{BUSY}}$ signal due to OENA command become active at the falling edge of $\overline{\text{WE}}$ signal, while it is normally active at the rising edge. See Fig. 11.

* $\overline{\text{BUSY}}$ signal is available only when $\overline{\text{CE}}$ is low (Fig. 10), therefore you must hold $\overline{\text{CE}}$ to low whenever you wish to check it.
* While Internal BUSY (IBUSY) signal is active, KS5901A can not accept the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ signal.
* If the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ signal is given during IBUSY signal, the internal status of the KS5901A may be uncertain. Besides, the "command error" of the status flag is set.

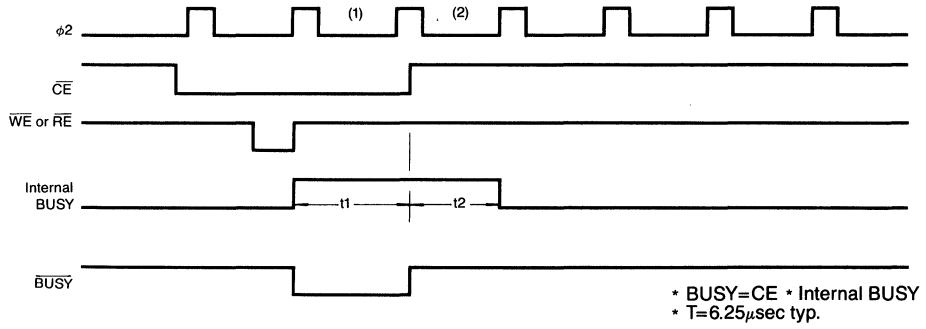


Fig. 10. Timing diagrams of –BUSY signal

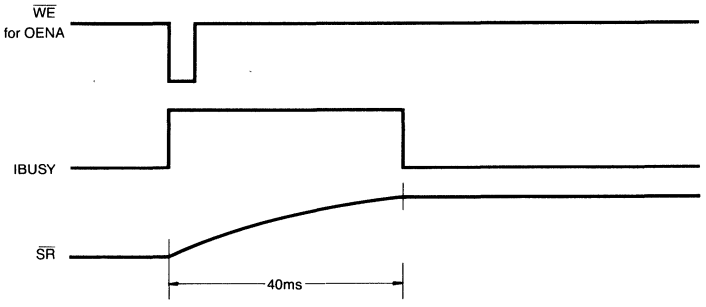


Fig. 11. Timing diagram of power-on transient state

6. Stop and restart operation

Speech synthesizing process is controlled by 2 kinds of code such as END1, END2.

A. Stop operation by END1 code

END1 code inserted at the last part of the speech parameter of a certain phrase controls the KS5901A to halt the increment of address counter, and issues $\overline{EOS}$ signal during 1 frame, remaining all it's internal condition values. At the same time status flag of D0 (End of speech) is set to high level. Figure 12 shows the timing diagram of $\overline{EOS}$ and EOS flag.

B. Restart operation by END2 code

END2 code inserted at the last part of the speech parameter of a certain phrase generates IBUSY during about 2.5ms and resets the address counter to the pre-loaded value by LDADER command, restarting synthesis operation from that address.

You can stop synthesis operation by loading STOP command in, it repeat operation without STRT command.

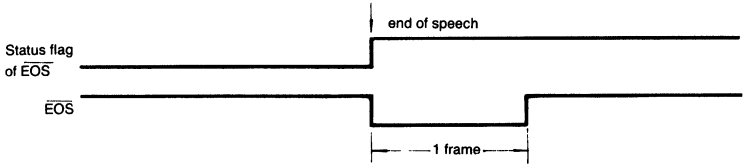


Fig. 12. Timing diagram of −EOS signal

7. Notes on the CPU control mode.

A. MODE pin must be set to "L" level.
B. BUSY pin issues the output of NAND logic of the internal busy and CE signal, therefore BUSY is not issued when CE is high level.
C. RE or WE signal is not detected during internal busy singal.
D. The APD signal set to "H" by the ODIS command is not changed by the OENA command (i.e., remains "H" level). Therefore, if APD is used to control the power of external audio circuit, the AENA command must be beforehand with the START command.
E. In the CPU controlled mode the default values of conditions after reset operation are such as;
   APD : High
   Speed code : ϕH (normal speed)
   COND1 code : ϕH (48 bit, 20msec, with repetition, 10 stages)
   COND2 code : ϕH (impulse, without loss)
F. The internal status of the KS5901A is usually read by RE signal. If you want to dump the speech ROM data, DDMP mode must be set previously.
G. In the DDMP mode the 100μsec of time interval is needed at least between each read operation to dump ROM data.
H. While the synthesis operation is executed by the KS5901A, such commands as DDMP, START, 2 & 6 nibble one are forbidden.
I. After the ODIS command, the time interval of about 40msec is needed so as to execute the OENA command.

5

Manual control mode

When MODE pin is set to "L", the KS5901A is turned into the manual control mode. In this mode, all the synthesis operation and conditions can be controlled by the external switches.

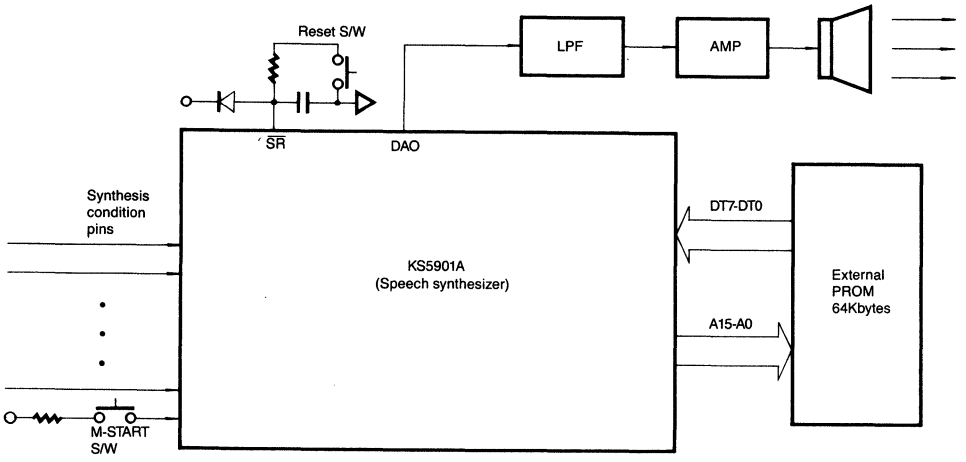


Fig. 13. System configuration the in manual control mode

1. Operation method

A. MODE pin must be set to "L" level.
B. Reset the KS5901A by means of depressing $\overline{SR}$ switch.
C. Through 10 synthesis condition pins, the synthesis conditions of the phrase to be synthesized must be specified.
D. The synthesis operation is started by means of depressing M-START switch.
E. The synthesis operation is halted by END 1 code.
F. The synthesis operation is repeated by END2 code.
G. When speech is halted by END1 code you may do the steps of C & D to perform the synthesis operation of the next phrase.
H. If you want the first phrase, you must operate the steps of B, C, D.

2. RESET operation

When Reset switch connected to $\overline{SR}$ pin is depressed or the power switch is on, the KS5901A remains the initialized state during about 40msec due to the charging time of the external capacitor attached to SR pin. M-START input is not received during that period.

3. START operation

In manual control mode, the chattering-preventing circuit is inserted to debounce the chatterings of the M-START pin. So, M-START input should be continued about min. 20msec (refer to Fig. 14)

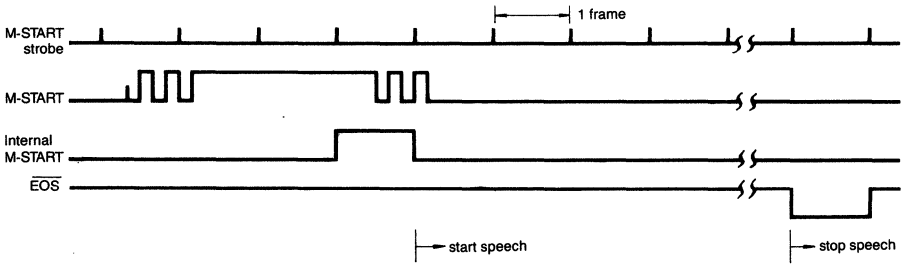


Fig. 14. Timing diagram of debouncing of the M-START signal

4. Synthesis conditions and speed.

In manual control mode, synthesis conditions are determined according to "H/L" combination of synthesis condition pins as shown bellow and synthesis speed follows the "H/L" combination of SC0-SC3 as shown in Tab. 9

Pin No.	Pin Name	Level	Synthesis Condition
29	EXC	L H	Impulse Triangular pulse
40	LODF	L H	With loss effect Without loss effect
31	NCFS	L H	Filter stages: 10 stages 8 stages
32	NOBA	L H	48 bit/frame 96 bit/frame
33	FRL	L H	20 msec/frame 10 msec/frame
30	REP	L H	Parameter: repetition no repetition

Tab. 8 Synthesis conditions in the manual control mode

Pin number				Speed	Pin number				Speed
39	37	36	35		39	37	36	35	
L	L	L	L	1.0*	H	L	L	L	1.4
L	L	L	H	0.7	H	L	L	H	1.5
L	L	H	L	0.8	H	L	H	L	1.55
L	L	H	H	0.9	H	L	H	H	1.0
L	H	L	L	1.0	H	H	L	L	1.0
L	H	L	H	1.1	H	H	L	H	1.0
L	H	H	L	1.2	H	H	H	L	1.0
L	H	H	H	1.3	H	H	H	H	1.0

*Original speed = 1.0

Tab. 9 Speed table in the manual control mode

LPC-PARAMETER EXTRACTION FLOW

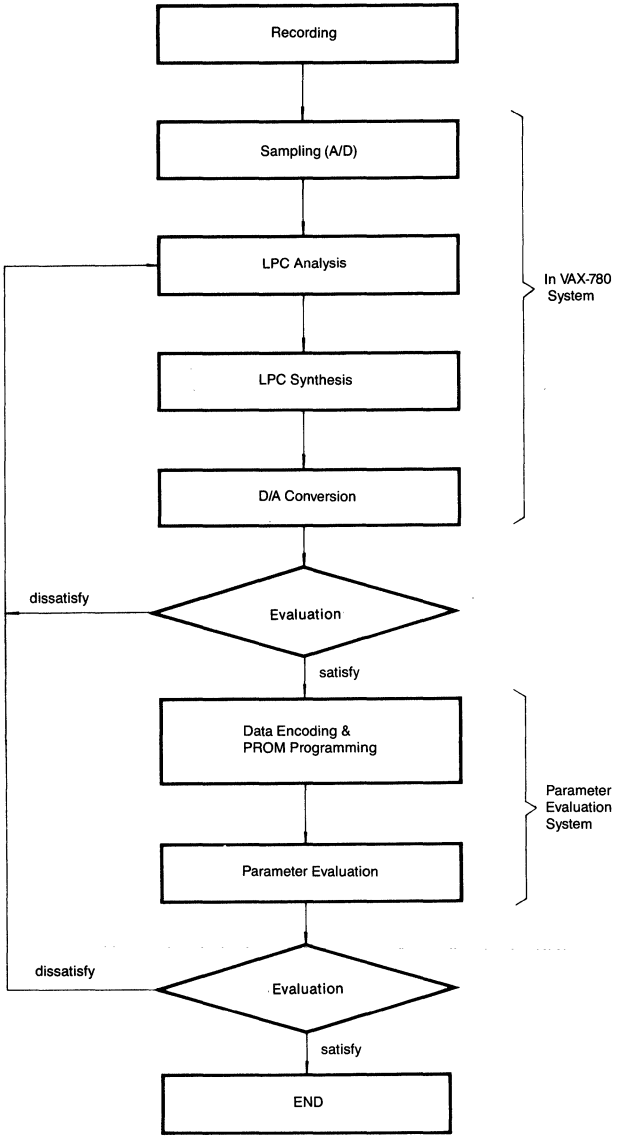


Fig. 15 LPC-parameter extraction flow

SYSTEM CONFIGURATION

1. CPU control mode

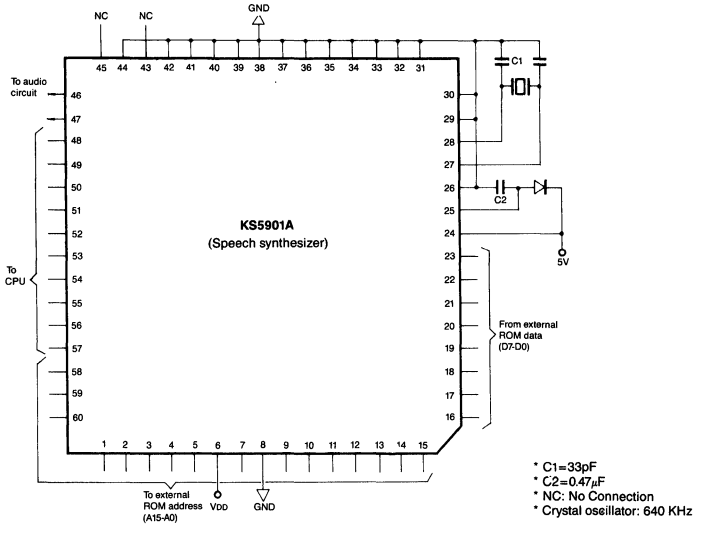
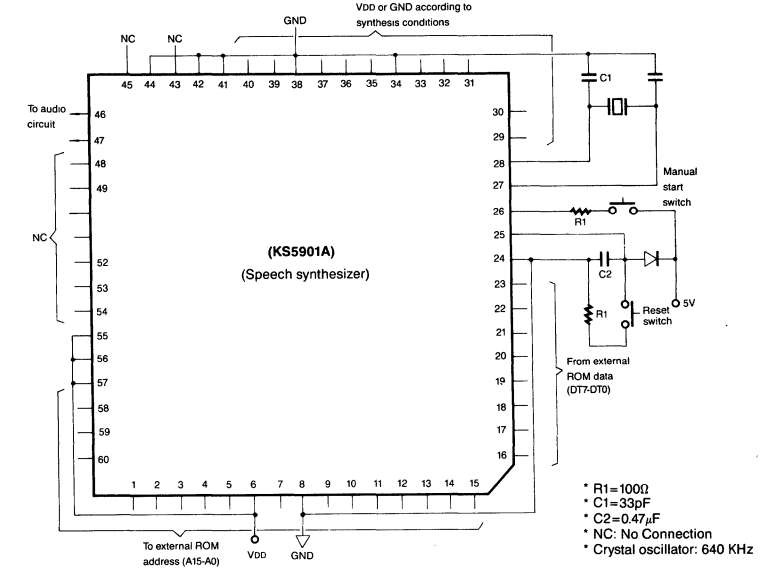


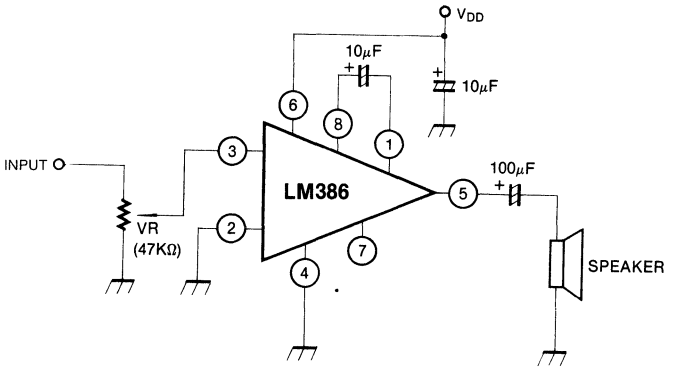
Fig. 16 System configuration in the CPU control mode

2. Manual control mode



Fi.g 17 System configuration in the manual control mode

AUDIO CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

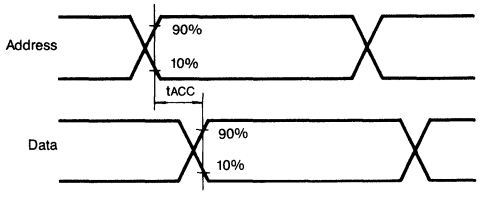
Symbol	Description	Specifications	Unit
V_{DD}	Power supply	−0.3 ~ +6.0	V
V_{IN}	Input voltage	−0.3 ~ V_{DD}+0.3	V
T_{ST}	Storage temperature	−40 ~ +125	°C
T_{OP}	Operation temperature	−10 ~ +55	°C

Tab. 10 Absolute maximum ratings

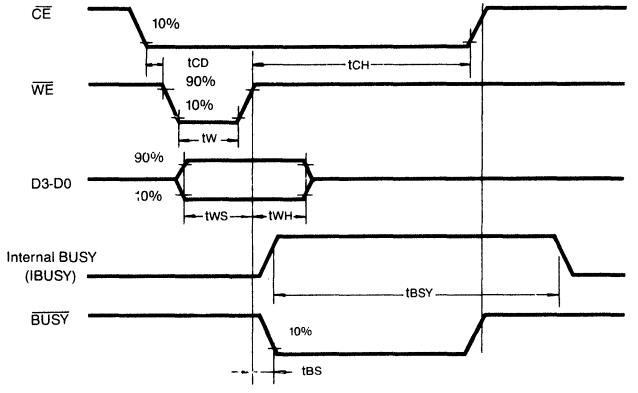
ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Conditions	Min.	Typ.	Max.	Unit
t_{CD}	Chip enable setup time	V_{DD}=5V	200	—	—	nsec
t_W	Write enable pulse width	V_{DD}=5V	500	—	—	nsec
t_{CH}	Chip enable hold time	V_{DD}=5V	200	—	—	nsec
t_{WS}	Data setting time	V_{DD}=5V	500	—	—	nsec
t_{WH}	Data hold time	V_{DD}=5V	300	—	—	nsec
t_{BS}	Busy setting time	V_{DD}=5V	—	—	300	nsec
t_R	Read enable pulse width	V_{DD}=5V	1	—	—	μsec
t_{RS}	Data settling time	V_{DD}=5V	—	—	500	nsec
t_{RH}	Data hold time	V_{DD}=5V	—	—	500	nsec
t_{ACC}	ROM data access time	V_{DD}=5V	—	—	1.5	μsec

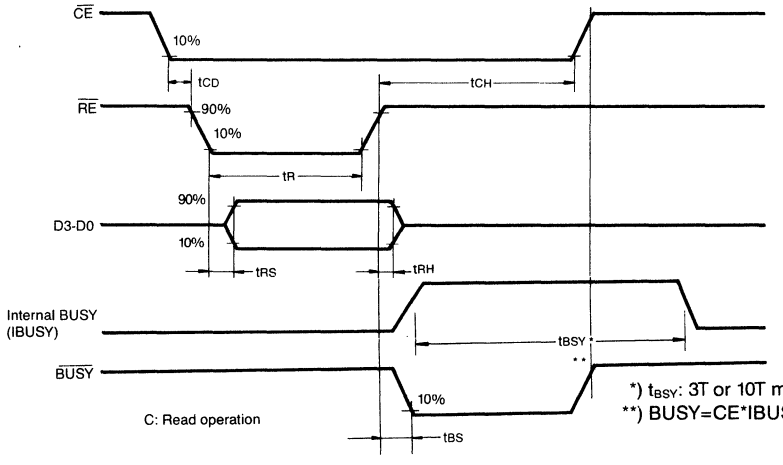
Tab. 11 AC Characteristics



A. External ROM Interface



B. Write operation



C: Read operation

*) t_{BSY}: 3T or 10T max.
**) BUSY=CE*IBUSY (see page 127)

Fig. 18 A.C. Characteristics

Symbol	Characteristics	Specific Pin	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	V_{DD}		3.5	5	6	V
I_{DDA}	Operating current	V_{DD}	V_{DD}=5V	—	1.1	1.5	mA
I_{DDB}	Stand-by current	V_{DD}	V_{DD}=5V	—	0.8	1.0	mA
I_{DDC}	Osc. disable current	V_{DD}	V_{DD}=5V	—	1.0	5.0	μA
$f\phi$	System clock frequency	$\phi 2$	V_{DD}=5V	155	160	165	kHz
f_{OSC}	Oscillator frequency	CX2	V_{DD}=5V	622	640	659	kHz
V_{IH}	"H" input voltage	Except $\overline{SR}$	V_{DD}=5V	V_{DD}-0.8	—	V_{DD}	V
V_{IL}	"L" input voltage	Except $\overline{SR}$	V_{DD}=5V	0	—	0.8	V
V_{OH}	"H" output voltage	Except $\overline{SR}$, DA0, CX2	No load	V_{DD}-0.4	—	V_{DD}	V
V_{OL}	"L" output voltage	Except $\overline{SR}$, DA0, CX2	No load	0	—	0.4	V
V_{OUT}	DAO output voltage	DA0	No load	0	—	V_{DD}	V
R_{INH}	Pull up resistor	$\overline{CE}$, $\overline{WE}$, $\overline{RE}$		190	380	570	kΩ
R_{INL}	Pull down resistor	M-START		70	140	210	kΩ
R_{OUT}	DAO output impedance	DAO		10	15	20	kΩ
I_{OHA}	"H" output current	A0-A15	Vout=V_{DD}-0.4	0.4	—	—	mA
I_{OHB}	"H" output current	D0-D3	Vout=V_{DD}-0.4	0.2	—	—	mA
I_{OHC}	"H" output current	$\overline{EOS}$, $\overline{BUSY}$	Vout=V_{DD}/2	1.0	—	—	mA
I_{OHD}	"H" output current	Others	Vout=V_{DD}-0.4	0.1	—	—	mA
I_{OLA}	"L" output current	A0-A15	Vout=0.4V	0.2	—	—	mA
I_{OLB}	"L" output current	D0-D3	Vout=0.4V	1.3	—	—	mA
I_{OLC}	"L" output current	$\overline{EOS}$, $\overline{BUSY}$	Vout=0.4V	1.0	—	—	mA
I_{OLD}	"L" output current	Others	Vout=0.4V	0.6	—	—	mA
I_{IH}	"H" input current	Except M-START	Vin=V_{DD}	—	—	1	μA
I_{IL}	"L" input current	Except M $\overline{CE}$ $\overline{WE}$, $\overline{RE}$	Vin=GND	—	—	1	μA

Tab. 12 D.C. characteristics

APPENDIX

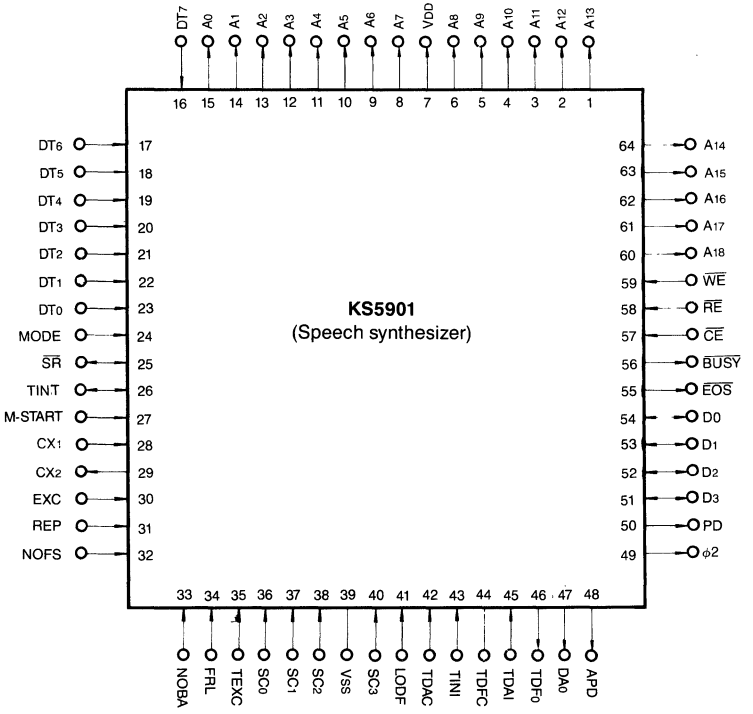
KS5901A is originally designed to have 64 pins. KS5901A is the another version to replace the 64 pin package type, named KS5901. Therefore, the KS5901A is equal to the KS5901 except that it's 5 pins are excluded.

KS5901 has 19 address lines which enable it to access upto 0.5 Mbytes of external PROM/EPROM. It's internal address counter is also 19 bits wide, and you must load 1 dummy nibble to set the start address when using the KS5901A. (see page 10)

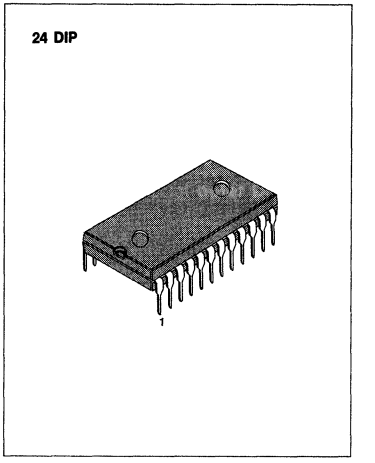
KS5901 has two more signal named PD, TINT. PD represents the status of the internal oscillator which is the same as status flag of D1. TINT is for test only.

The differences between the two chips are summarized as follows.

Item \ Device	KS5901A	KS5901
Pin count	60	64
Package type	QFP	DIP/QFP
No. of address pin	16	19
Addressing range	64 Khytes	0.5 Mbytes
Maximum synthesizing time	4-5 min.	40 min.



CMOS 1-CHIP SPEECH SYNTHESIZER



The KS5902XX is a CMOS one-chip speech synthesizer which produces a good quality of human voice using LPC (Linear Predictive Coding) algorithm. It can be easily used everywhere required to produce synthesized speech with it's simplified I/O design. The KS5902XX has three operating modes. The CPU mode makes it easy to interface with 4/8 bits microprocessor or microcontroller. In the KEY mode it is operated by some keys attached to. In the auto mode, it can synthesize speech automatically according to the simple operation of externally connected switches.

The KS5902XX has 48K bits mask programmable ROM which can produce speech during about 20 sec. continuously. It can be separated to 15 phrases. The KS5902XX also has a built-in 9 bits R-2R D/A converter. (KS5902XX is noted to KS5902 hereinafter, as the 'XX' is 2 character assigned according to the mask option)

FEATURES

1) General Feature

- **Speech synthesis method; LPC**
- **Oscillator frequency; 2.56MHz**
- **Sampling frequency; 8KHz**
- **Operating modes; CPU/KEY/AUTO**
- **On-Chip mask ROM; 48 Kbits**
- **Built-in interpolator**
- **Built-in pipelined multiplier**
- **Easy interface with microprocessor or microcontroller.**
- **Low power consumption due to power-down at the stand-by state**
- **Built-in 9 bits R-2R D/A converter**
- **Clocked CMOS**
- **Single +5V power supply**

2) Synthesizer Feature

- **Synthesizing speed ; variable from 0.7 ~ 1.55 times of normal speech.**
- **Excitation source ; voiced: impulse/triangular pulse unvoiced: white noise**
- **Bit allocation ; 48/96 bits/frame**
- **Frame length ; 10/20 msec/frame**
- **Parameter repetition ; with repeat/without repeat**
- **Loss factor ; with consideration/without consideration**
- **Digital filter stage ; 8/10 stages**
- **Repetition of Phrase ; END1/END2 code.**

BLOCK DIAGRAM

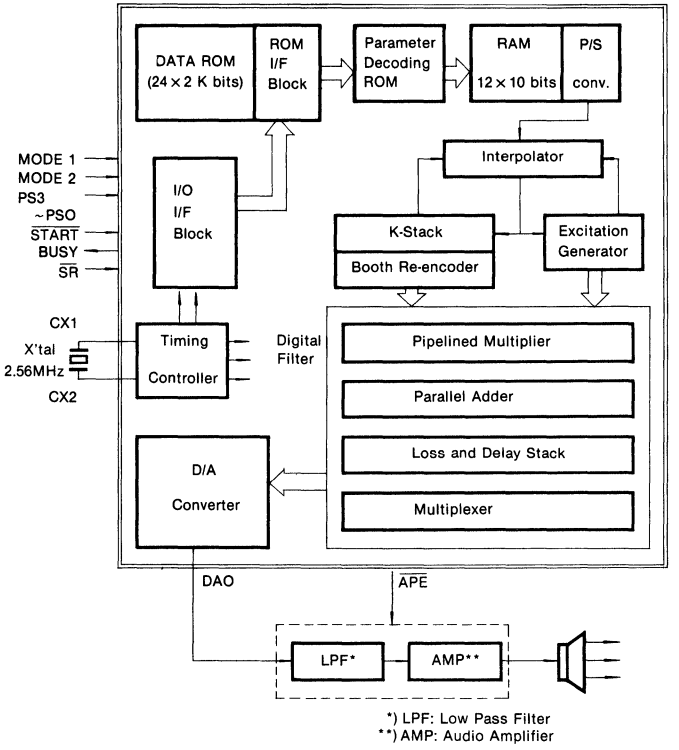


Fig. 1 Functional block diagram

PIN CONFIGURATION

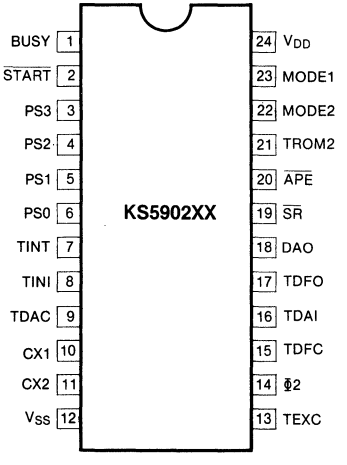


Fig. 2 KS5902 pin assignment

PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	BUSY	O	BUSY Signal Output
2	$\overline{START}$	I	Start Signal Input (internally pull-up)
3	PS3	I	Phrase Select Input (internally pull-down)
4	PS2	I	
5	PS1	I	
6	PS0	I	
7	TINT	I/O	For Test Only
8	TINI	I	For Test Only (normally ground)
9	TDAC	I	For Test Only (normally ground)
10	CX1	I	Crystal Oscillator Input
11	CX2	O	Crystal Oscillator Output
12	V_{SS}	POWER	Ground
13	TEXC	I	For Test Only (normally ground)
14	$\overline{\Phi 2}$	O	System Clock Output (160KHz)
15	TDFC	O	For Test Only
16	TDAI	I	For Test Only (normally ground)
17	TDFO	O	For Test Only
18	DAO	O	D/A Converter Output
19	$\overline{SR}$	I	System Reset (low active)
20	$\overline{APE}$	O	Audio Power Enable (low active)
21	TROM2	O	For Test Only
22	MODE 2	I	Mode Select Input 1
23	MODE 1	I	Mode Select Input 2
24	V_{DD}	POWER	+5 Volt

Tab. 1 KS5902XX pin description

OPERATING PRINCIPLES

Mode Selection

The KS5902XX can be used in three operating modes according to the combinations of MODE 1/MODE 2 pins.

MODE 1	MODE 2	Operating Mode
H*	H	CPU Mode
H	L**	KEY Mode
L	H	AUTO Mode
L	L	Not Used

* H*; +5V, L**; 0V

Tab. 2 Mode selection

CPU Mode

CPU mode makes it easy to interface with microprocessor or microcontroller. It is controlled only by PS3 ~ PS0 & $\overline{START}$, also can be monitored it's status through BUSY and $\overline{APE}$.

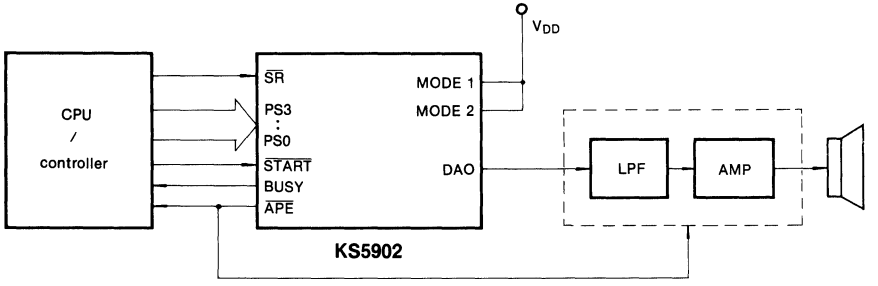


Fig. 3 System configuration in CPU mode

KEY Mode

KEY mode, which is the same as in it's operational principle, is characterized by its manual operation with the switches connected to it. Also, the input debouncing circuit is inserted internally to the $\overline{START}$ pin to prevent malfunction caused by using the KEYs.

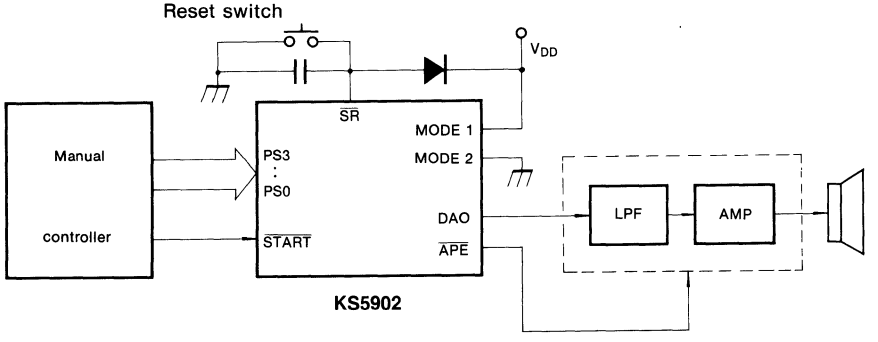


Fig. 4 System configuration in KEY mode

AUTO Model

In this mode, KS5902XX starts its oscillator circuit when anyone of PS3 ~ PS0 is connected to the "H" level, and after 500 msec from that time the KS5902XX fetches phrase selection (PS3 ~ PS0) data to initiate it s synthesis operation. KS5902XX repeats to be selected phrase as long as not all the phrase select (PS3 ~ PS0) lines connected to the "L" level. If it is selected another phrase during one phrase is activated, it completes current phrase and then initiates new phrase.

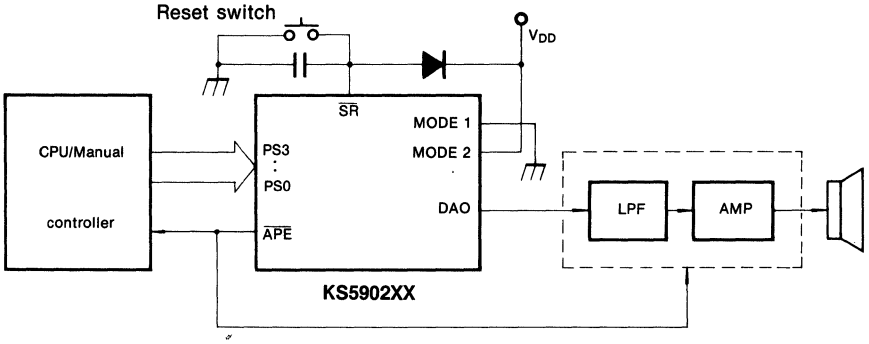


Fig. 5 System configuration in AUTO mode

Phrase Selection

According to the conbinations of 4 phrase selection lines (PS3 – PS0) total 15 phrases of speech are available. Before starting the synthesis operation, phrase selection must be specified in 4 bit code. Possible combinations of phrase selects are as follows, and can be selected at random.

PS3	PS2	PS1	PS0	Selected Phrase
L	L	L	H	#1 Phrase
L	L	H	L	#2 Phrase
L	L	H	H	#3 Phrase
H	H	H	H	#15 Phrase

Tab. 3 Phrase selection by PS3 – PS0

If the KS5902XX receives $\overline{\text{START}}$ signal when all phrase select lines are set to "L" level in CPU, KEY mode, it stops synthesis operation within 1 frame (10/20 msec). In AUTO mode, if all PS3 ~ PS0 are set to "L" level, it stops synthesis operation within 0.5 frame.

Start Operation

48 Kbits on-chip mask ROM is composed of 24 bit x 2K words. Initial 15 addresses are index area which contain synthesis conditions and start address of each phrase, the other addresses are data area which contain speech parameter (refer fig. 6).

The start operation of KS5902XX is as follows. First, phrase is selected by P.S. Second, $\overline{\text{START}}$ signal is given by CPU or manual operation. Third, as its first internal cycle, start address and condition data of the specified phrase in the index area are fed to the address counter and condition latch respectively. Then, after the first internal cycle the desired speech is synthesized with the speech parameter from data area pointed by address counter.

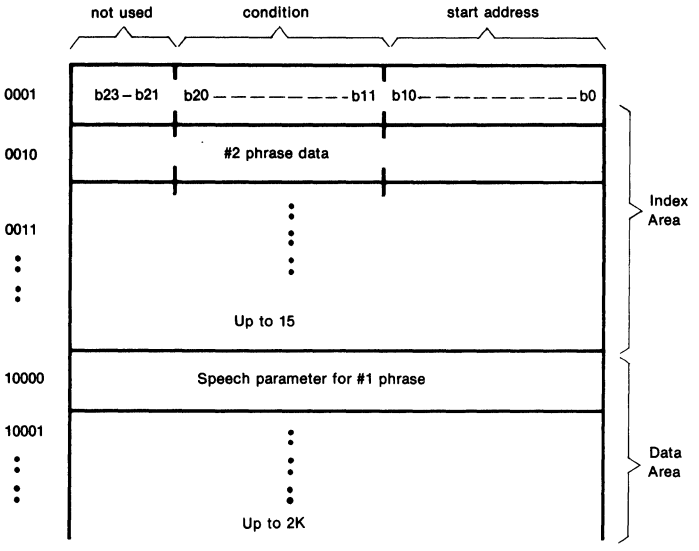


Fig. 6 KS5902XX memory map

Conditions

The 10 bits of b20 ~ b11 of each index address represent condition data. The conditions, described in tab. 4 are determined when original speech is analyzed by LPC algorithm. They can affect the quality of synthesized speech and the total data size, therefore any customer who want to use KS5902XX must determine them through discussions with SST.

The followings are the details of the conditions, but they are not user accessable once mask programed.

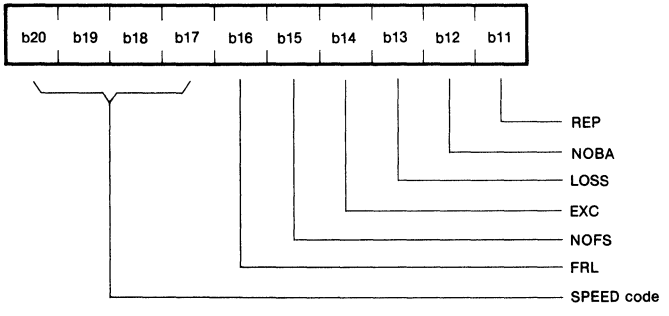


Fig. 7 The descriptions of condition code

Item	Description	Level	Condition
REP	Parameter Repetition	H	Without Repetition
		L	With Repetition
NOBA	Number of Bit Allocation	H	96 Bit/frame
		L	48 Bit/frame
LOSS	Loss Factor of Digital Filter	H	With Consideration
		L	Without Consideration
EXC	Excitation Source	H	Triangular Pulse
		L	Impulse
NOFS	Number of Digital filter Stage	H	8 Stages
		L	10 Stages
FRL	Frame Length	H	10 msec/frame
		L	20 msec/frame
Speed	Speed Rate	LLLH : HLLH HLHL Others	X0.7 : X1.5 X1.55 X1.0 (normal speed)

Tab. 4 The descriptions of condition code

Cautions

(1) The internal status of KS5902XX, after power-on transient time or synthesizing operation is under "system reset," are denoted by "stand-by status" which means the oscillator is disabled.
(2) Any access is prohibitted during BUSY signal is "H".
(3) On the power-on reset, it needs 10 msec of transient time, and during this time any access to KS5902XX is prohibited.
(4) The unused input terminals such as TINI, TDAC, TDAI, TEXC must be connected to "L" level.
(5) The low level of the $\overline{APE}$ terminal represents that KS5902XX is under synthesis operation. This signal may be used to control the audio power so that the low level of the $\overline{APE}$ enables audio power, otherwise disables to save power consumption.

OPERATING METHOD

CPU Mode

(1) Mode selection; Connect the mode select (MODE 1, MODE 2) terminals to "H" level.
(2) Phrase selection; Select any one of the 15 phrases by the combinations of 4 phrase select terminals. (PS3 ~ PS0)
(3) Start; If CPU forces $\overline{START}$ signal under phrase selected, then KS5902 starts the synthesis operation holding low level of $\overline{APE}$. (refer Fig. 8)
(4) Stop; If CPU selects all phrase selects (PS3 ~ PS0) to "L" level and forces $\overline{START}$ signal, synthesizing operation is halted within 1 frame (10/20 msec). (refer Fig. 9)
Otherwise, speech synthesis process is stopped automatically by END 1 code located in the last of each phrase data. In each case KS5902XX outputs the $\overline{APE}$ terminal to it's "H" level then returns to the stand-by state. If END 2 code is contained to the specified phrase, the phrase is repeated until the proces is halted. (refer Fig. 10)
(5) Status signal
a. BUSY; BUSY signal is generated during 60 msec typically from falling edge of the $\overline{START}$ signal. During this time any attempt to access is blocked.

b. $\overline{APE}$; $\overline{APE}$ signal is generated during the system is under synthesis operation. The low level of the $\overline{APE}$ terminal represents this status.

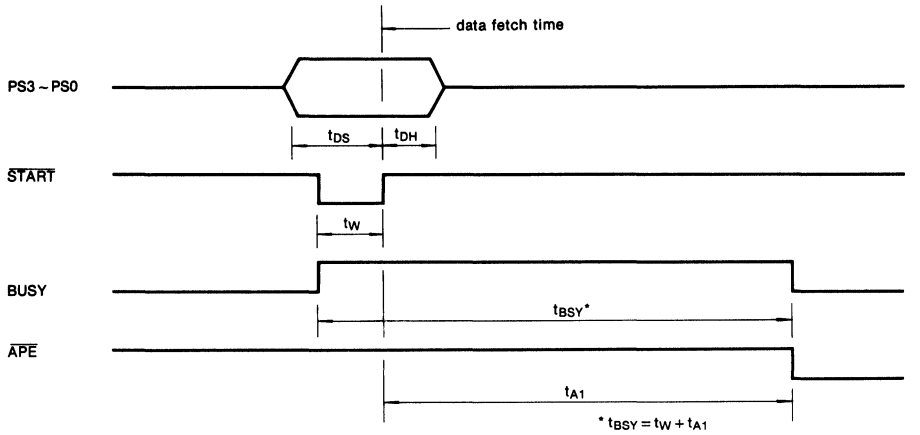
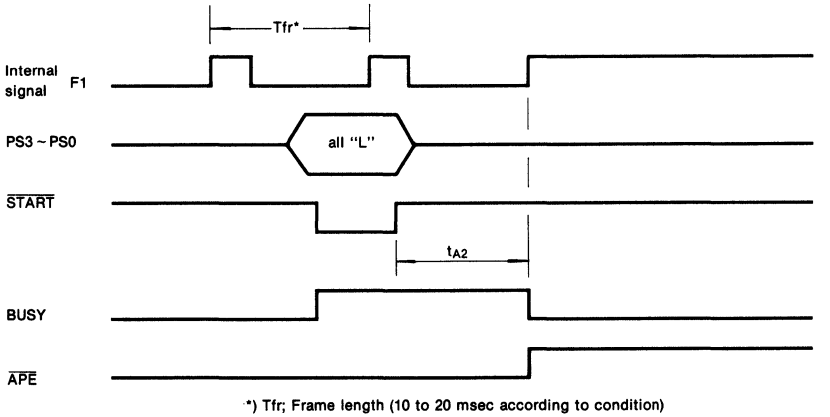


Fig. 8 Timing of start operation in CPU mode

Symbol	Description	Min	Typ	Max	Unit
t_{DS}	Data Settling Time	500	—	—	nsec
t_{DH}	Data Holding Time	300	—	—	nsec
t_W	Start Signal Width	1.0	—	—	μsec
t_{BSY}	Busy Signal Duration	—	60	—	msec
t_{A1}	$\overline{APE}$ Signal Delay 1	—	60	—	msec
t_{A2}	$\overline{APE}$ Signal Delay 2	—	—	20	msec
t_{A3}	$\overline{APE}$ Signal Delay 3	—	40	—	msec

Tab. 5 AC characteristics of CPU mode



*) Tfr; Frame length (10 to 20 msec according to condition)

Fig. 9 Timing of forced stop in CPU mode

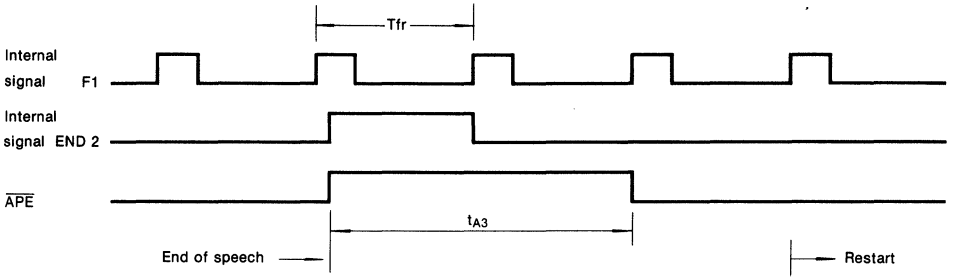


Fig. 10 Repetition of speech by END 2 code

KEY Mode

(1) Mode selection; Connect MODE 1 terminal to "H" level, and MODE 2 terminal to "L" level.
(2) Phrase selection; Select anyone of the 15 phrases by combinations of 4 phrase select terminals (PS3 ~ PS0).
(3) Start; Synthesizing operation is started by pressing start key which is externally connected to $\overline{START}$ terminal. Built-in debouncing circuit requires 40 msec or more to prevent the chatterings of $\overline{START}$ terminal.
(4) Stop; Synthesizing operation can be stopped by one of the three case.
   a. Press $\overline{SR}$ switch connected to $\overline{SR}$ terminal.
   b. Select all phrase selects to "L" level, Then press start switch
   c. Otherwise speech synthesis operation is stopped automatically by END 1 code located on the last of each phrase speech data.

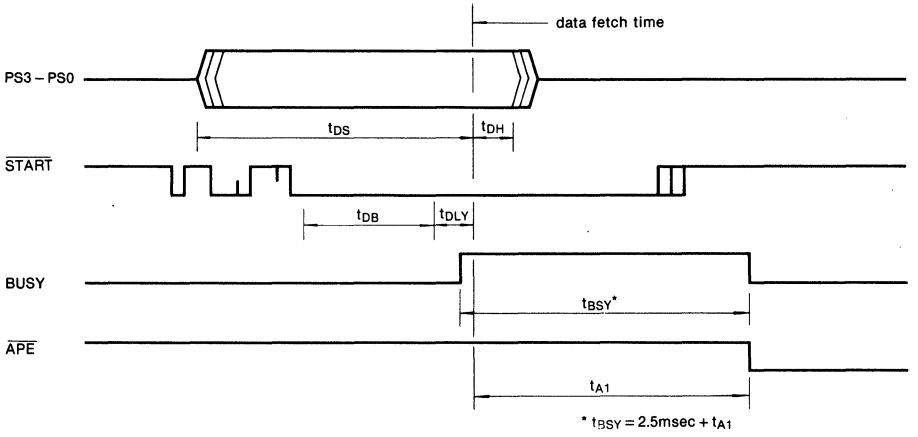


Fig. 11 Timing of start operation in KEY mode

Symbol	Description	Min	Typ	Max	Unit
t_{DS}	Data Settling Time	500	—	—	nsec
t_{DH}	Data Hold Time	300	—	—	nsec
t_{DB}	Input Debounce Time	40	—	—	msec
t_{DLY}	Data Fetch Delay Time	—	20	—	msec
t_{BSY}	Busy Signal Duration	—	42.5	—	msec
t_{A1}	$\overline{APE}$ Signal Delay	—	40	—	msec

Tab. 6 AC characteristics of Key mode

AUTO Mode

(1) Mode selection; Select MODE 1 terminal to "L" and MODE 2 terminal to "H" level.
(2) Phrase select; Select anyone of the 15 phrases by combinations of 4 phrase select terminals. (PS3 ~ PS0)
(3) Start; If anyone of the phrase select is set to "H" level, then internal oscillator circuit starts to oscillate and after 500 msec KS5902XX fetches the phrase select data to begin synthesis operation. Therefore the phrase select terminals must be settled within 500 msec. Synthesis operation is continued unless all phrase selects are set to "L" level. The interval repeated phrases is 560 msec. If the levels of phrase selects are changed under synthesis operation, the new selected phrase is synthesized after the current speech is terminated.
(4) Stop; If all the phrase select lines are set to "L" level, current speech is stopped within 1 fame (10/20 msec).

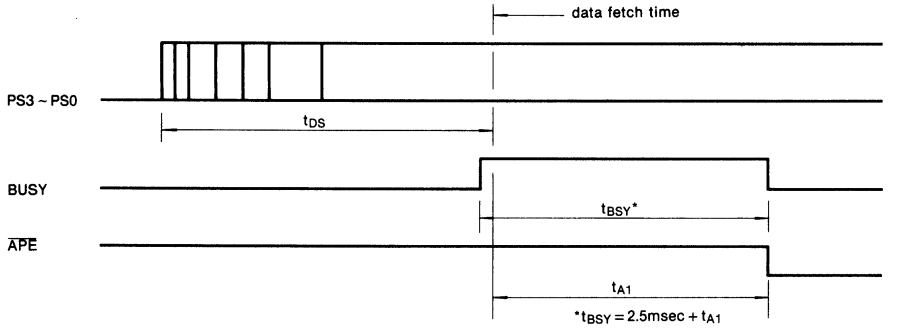


Fig. 12 Timing of start operation in AUTO mode

Symbol	Description	Min	Typ	Max	Unit
t_{DS}	Data Settling Time	—	500	—	msec
t_{BSY}	Busy Signal Duration	—	42.5	—	msec
t_{A1}	$\overline{APE}$ Signal Delay 1	—	40	—	msec
t_{A2}	$\overline{APE}$ Signal Delay 2	—	40	—	msec

Tab. 7 AC characteristics of AUTO mode

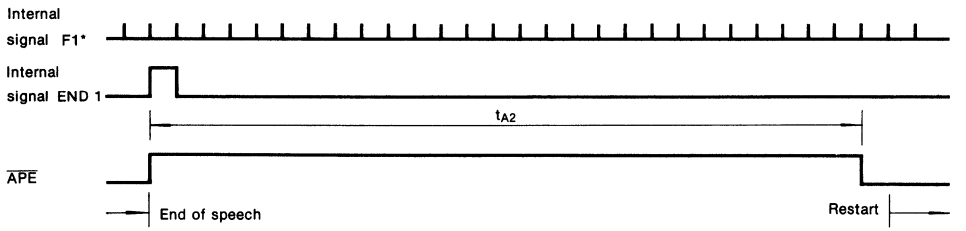


Fig. 13 Repetition of speech in AUTO mode

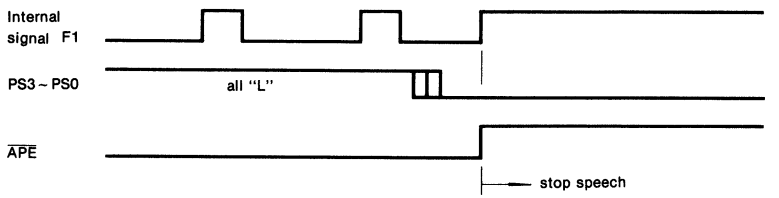
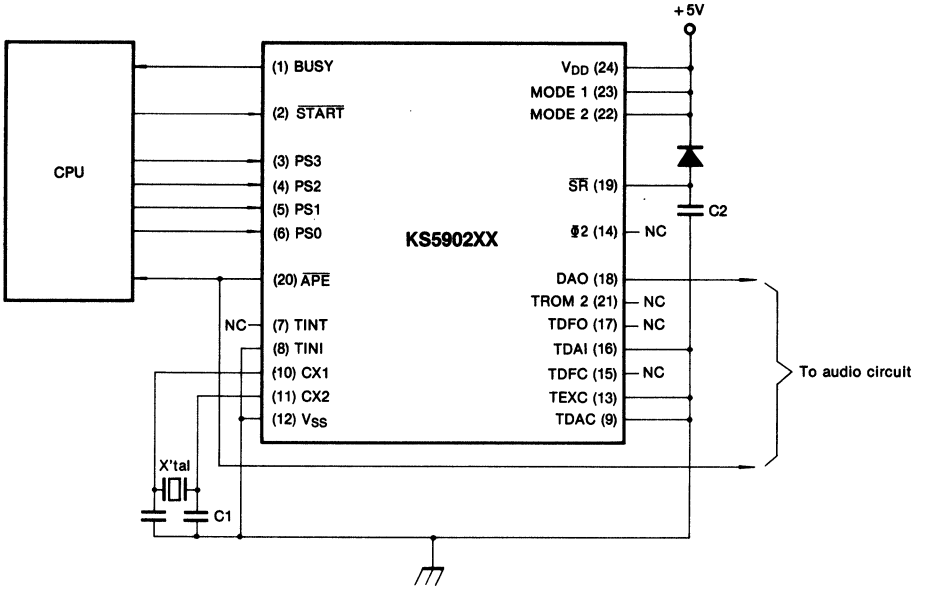
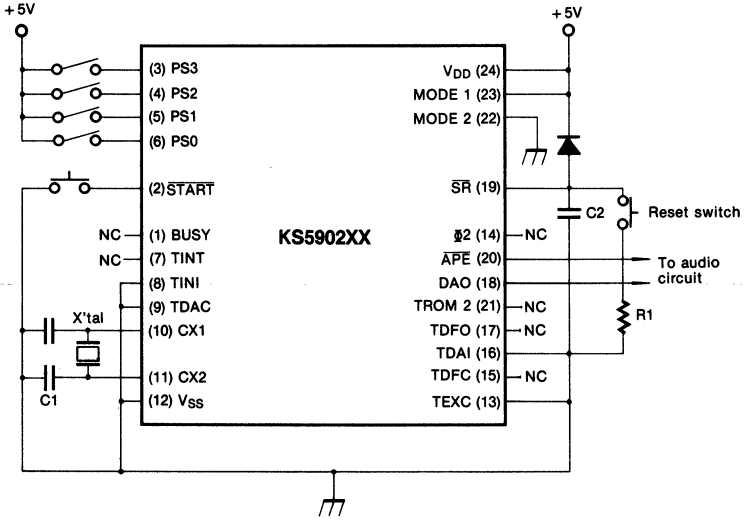


Fig. 14 Stop operation in AUTO mode

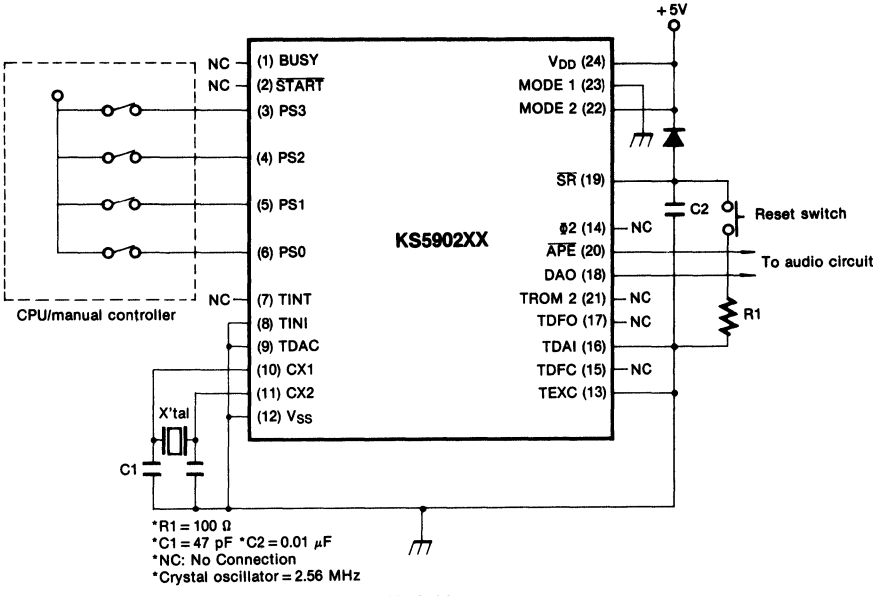
SYSTEM CONFIGURATION



(a) CPU Mode



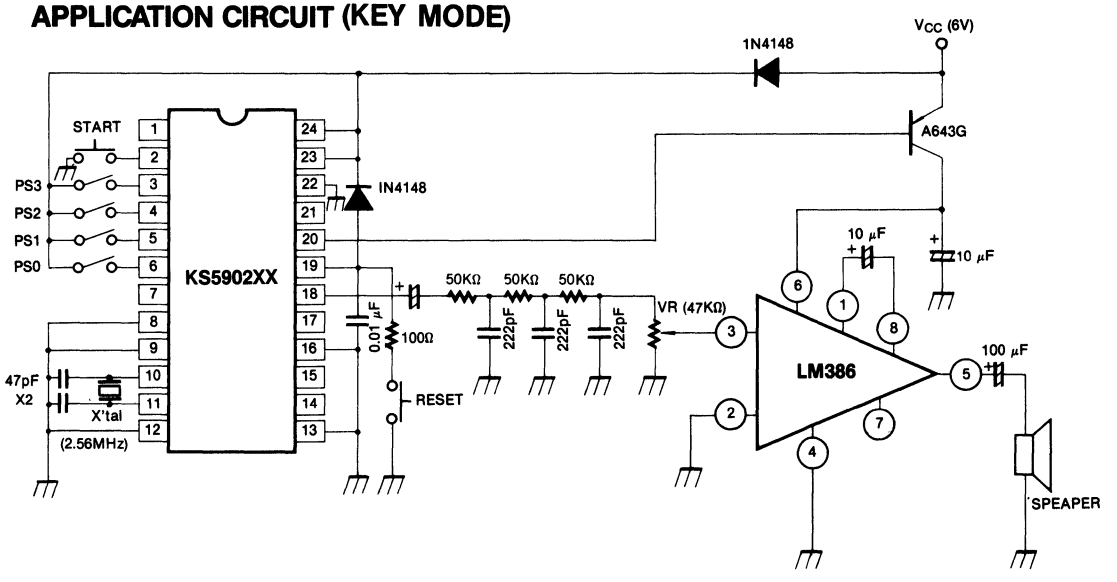
(b) KEY Mode



(c) AUTO Mode

Fig. 15 Application circuit examples

APPLICATION CIRCUIT (KEY MODE)



ELECTRICAL CHARACTERISTICS

(1) Absolute maximum ratings

Description	Symbol	Specifications	Unit
Power Supply	V_{DD}	$-0.3 \sim 7.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Operation Temperature	T_{opr}	$-10 \sim 55$	°C
Storage Temperature	T_{stg}	$-55 \sim 120$	°C

(2) D.C. characteristics ($V_{DD}=5V$, $Ta=25°C$)

Characteristics	Symbol	Specific Pin	Condition	Min	Typ	Max	Unit
Operating Current	I_{DDA}	V_{DD}		—	1.0	1.5	mA
Stand-by Current	I_{DDB}	V_{DD}		—	1.0	5.0	μA
System Clock Frequency	F_o	2		155	160	165	KHz
Oscillator Frequency	F_{OSC}	CX2		2.48	2.56	2.63	MHz
"H" Input Voltage	V_{IH}	Except $\overline{SR}$	$V_{DD}=5V$	$V_{DD}-0.8$	—	V_{DD}	V
"L" Input Voltage	V_{IL}	Except $\overline{SR}$	$V_{DD}=5V$	0	—	0.8	V
"H" Output Voltage	V_{OH}	Except DAO	No Load	$V_{DD}-0.4$	—	V_{DD}	V
"L" Output Voltage	V_{OL}	Except DAO	No Load	0	—	0.4	V
DAO Output Voltage	V_{OUT}	DAO	No Load	0	—	V_{DD}	V
Pull Up Resistor	R_{INH}	$\overline{START}$, MODE 1/2		—	800	—	KΩ
Pull Down Resistor	R_{INL}	PS3 ~ PS0		—	300	—	KΩ
DAO Output Impedance	R_{OUT}	DAO		10	15	20	KΩ
"H" Output Current	I_{OH}	BUSY, $\overline{APE}$, 2	$V_{out}=V_{DD}-0.4$	−0.3	—	—	mA
"L" Output Current	I_{OL}	BUSY, $\overline{APE}$, 2	$V_{out}=0.4V$	0.8	—	—	mA

SPEECH PARAMETER ENCODING

KS5902XX is a speech synthesizer based on LPC (Linear Predictive Coding) algorithm. LPC is a coding technique in which speech signal is converted to frequency domain and, extracting it's characteristic parameters. This method can save memory size over 20 times compared with time domain analysis method, therefore it can store more speech data on limitted memory area. KS5902XX performs speech synthesizing operation with LPC coded speech parameter.

To synthesize speech using KS5902XX, at first it requires the analysis process of recorded voice signal. LPC analysis extracts 12 parameters for each defined interval (frame). The extracted parameters, which represent the characteristics of each frame, have special distribution characteristics. The extracted data can be shrinked more compactly in the quantization process to store them on memory using this distribution characteristics. Several factors are considered to encode them such as frame length, bit allocation, repetition of parameters, etc. Such factors can have influence on the amount of memory size, and on the quality of synthesized speech by causing distortions in extracted parameters. There is a trade-off between memory size and quality of synthesized speech.

To synthesize speech using KS5902XX, as described above, speech parameters must be acquired by analyzing original speech and encoding them. Then SST produces a piece of mask which contains speech parameters of the acquired data. And KS5902XX is fabricated with this new mask plus remaining masks through a series of processes. Thus the customized KS5902XX which contains the desired speech data is aquired. SST have set up the KS5902XX development system for such processes to prepare speech parameters.

Any customer who wants to build speech synthesizing system using KS5902XX must determine the conditions for speech analysis through discussions on the memory size and the quality of the synthesized speech. SST then prepare the speech data using the development system. The speech data are evaluated on the KS5902XX evaluation Kit, and if they are not satisfied to the customer's demand the analysis-evaluation procedure is repeated until they meet the customer's need. The flow of speech parameter encoding is shown below.

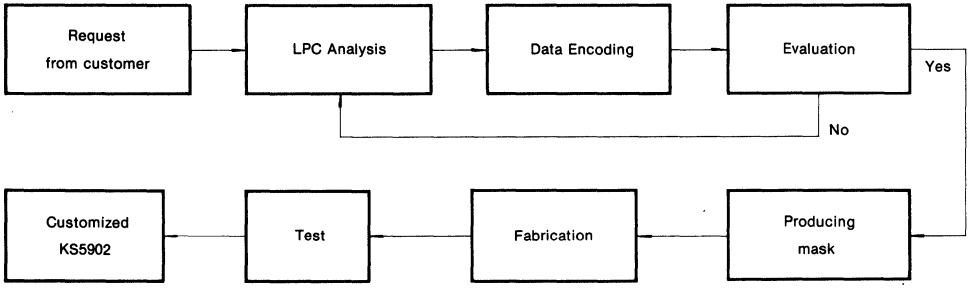


Fig. 16 Speech parameter coding flow

VOICE RECORDING & REPRODUCING LSI

KS5911 is a CMOS LSI for voice (sound) recording & reproducing LSI, using the ADM (Adaptive Delta Modulation) algorithm.

KS5911 cn be used two kinds of modes, that is, manual mode and auto mode with the way of recording/reproducing.

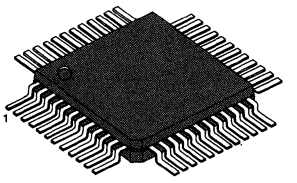
It can be used 64K or 256K DRAM, until maximum 4pcs.

In the manual mode, using 4 input pin, the sound recording/reproducing of maximum 16 phrases can be performed and start/stop input is activated by external key.

In the auto mode, input voice signal is automatically recorded and recording stop with silence detection and recorded voice signal is reproduced automatically.

KS5911 can be used 4 kinds of bits rate (8K, 11K, 16K, 32K BPS).

48 FQP



FEATURES

- **Voice recording & reproducing LSI using ADM algorithm.**
- **Auto-talking back function with auto mode.**
- **64K DRAM or 256K DRAM can be used selectively 1 pcs-4 pcs.**
- **Capable of recording & reproducing of max. 16 phrases.**
- **Selective 4 kinds of bits rate (8K, 11K, 16K, 32K bps).**
- **Built-in in DRAM refresh circuit.**
- **Built-in microphone amplifier.**
- **Built-in 10 bits D/A converter.**
- **Built-in voltage follower for D/A converter buffering.**
- **Built-in RC oscillator (640 KHz-1 MHz).**
- **+5V single power.**
- **Clocked CMOS for low power consumption.**
- **48 pin QFP package.**
- **In case of long time recording/reproducing without phrase selection, using EXT/RIPPLE pin, memory extension is possible.**

FUNCTIONAL BLOCK DIAGRAM

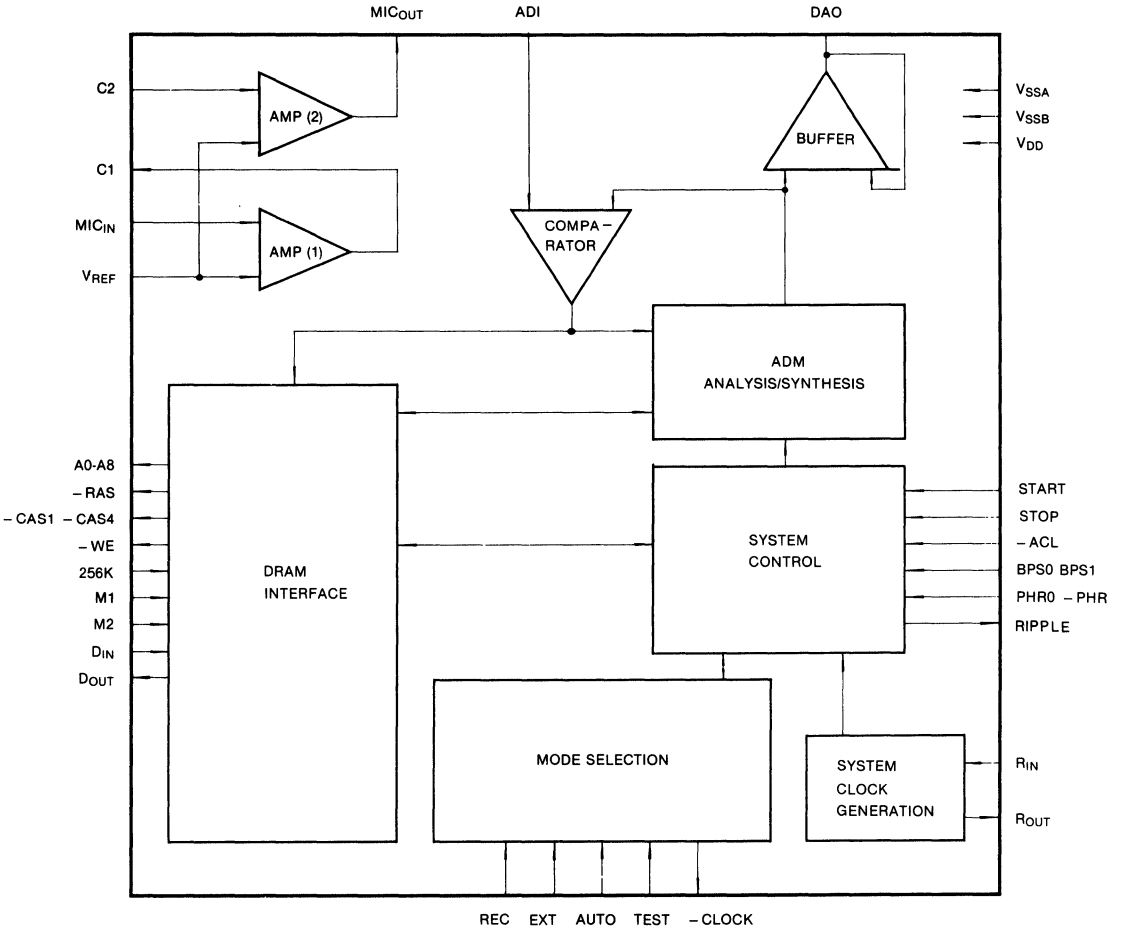


Figure 1. KS5911 Functional Block Diagram

PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Pull Up/Down</th><th>Function</th></tr>
<tr><td>– ACL</td><td>1</td><td>I</td><td>UP</td><td>Reset Input Pin. Use CAP. (1μF)</td></tr>
<tr><td>REC</td><td>2</td><td>I</td><td>DOWN</td><td>At manual mode.
H; Recording mode L; Reproducing mode.</td></tr>
<tr><td>M1
M2</td><td>3
4</td><td>I
I</td><td>—
—</td><td>Programming terminal for the number of outer DRAMs.
<table>
<tr><th>Pin No.</th><th>M1</th><th>M2</th><th>Pin No.</th><th>M1</th><th>M2</th></tr>
<tr><td>1pcs</td><td>L</td><td>L</td><td>3pcs</td><td>H</td><td>L</td></tr>
<tr><td>2pcs</td><td>L</td><td>H</td><td>4pcs</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td></td><td>7</td><td></td><td></td><td>N.C.</td></tr>
<tr><td>PHR0
PHR1
PHR2
PHR3</td><td>5
6
8
9</td><td>I
I
I
I</td><td>DOWN
DOWN
DOWN
DOWN</td><td>Programming terminal for the phrase selection.
<table>
<tr><th>Phrase No.</th><th>PHR0</th><th>PHR1</th><th>PHR2</th><th>PHR3</th></tr>
<tr><td>0</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>1</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>.</td><td>.</td><td>.</td><td>.</td><td>.</td></tr>
<tr><td>15</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>BPS0
BPS1</td><td>10
11</td><td>I
I</td><td>DOWN
DOWN</td><td>Programming terminal for bit rate selection.
<table>
<tr><th>Bit Rate</th><th>BPS0</th><th>BPS1</th><th>Bit Rate</th><th>BPS0</th><th>BPS1</th></tr>
<tr><td>8KBits/sec</td><td>L</td><td>L</td><td>16KBits/sec</td><td>H</td><td>L</td></tr>
<tr><td>11KBits/sec</td><td>L</td><td>H</td><td>32KBits/sec</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>D_{IN}</td><td>12</td><td>I</td><td>UP</td><td>Data input pin. Connect this pin to data output pins of DRAMs.</td></tr>
<tr><td>RIPPLE</td><td>13</td><td>O</td><td>—</td><td>At EXT = H, when maximum address overflow occurs, this pin generates a ripple clock.</td></tr>
<tr><td>– CAS1
– CAS2
– CAS3
– CAS4</td><td>14
15
16
17</td><td>O
O
O
O</td><td>—
—
—
—</td><td>Column address strobe output.
Used from CAS1 to that required corresponding to the number of external DRAMs.</td></tr>
</table>

(to be continued)

PIN DESCRIPTION (Continued)

Pin Name	Pin No.	I/O	Pull Up/Down	Function
– CLOCK	18	O	—	Only test.
D_{OUT}	19	O	—	Data output pin. Connect this to data input pins of external DRAMs.
A8	20	O	—	Address output pin to DRAMs A8 is not needed when 64K bit DRAMs are used.
A7	21	O	—	
A6	22	O	—	
A5	23	O	—	
A4	24	O	—	
A3	25	O	—	
A2	26	O	—	
A1	27	O	—	
A0	28	O	—	
V_{DD}	29	Power	—	+5V (Typ.)
ADI	30	I	—	Voice (or Signal) input pin. The center of input signal level must be 1/2 V_{DD}
DAO	31	O	—	Synthesized voice output pin. The center of output level is 1/2 V_{DD}
V_{SSB}	32	Power	—	System ground.
MIC_{OUT}	33	O	—	Output pin of built-in AMP (1). The center of output level is 1/2 V_{DD}
C2	34	I	—	Input pin of built-in AMP (2).
C1	35	O	—	Output pin of built-in AMP (2). The center of output level is 1/2 V_{DD}
MIC_{IN}	36	I	—	Input pin of built-in AMP (1). Connect to microphone through capacitor.
V_{REF}	37	I/O	—	For connecting capacitor which stabilized the reference voltage for the built-in AMP.
V_{SSA}38	Power	—	Ground OV.	
STOP	39	I	DOWN	Manual stop input pin.
TEST	40	I	DOWN	Only test.
START	41	I	DOWN	Manual start input pin.
EXT	42	I	—	At EXT = H: When address overflow occurs, RIPPLE pin generates a ripple clock. At EXT = L: KS5911 is manual mode.

(to be continued)

5

PIN DESCRIPTION (Continued)

Pin Name	Pin No.	I/O	Pull Up/Down	Function
– RAS	45	O	—	Low address strobe output. Connect this to-RAS pins of outer DRAMs.
256K	46	I	—	Input for the selection of the types of external DRAMs. 256K = H: 256K DRAM type. 256K = L: 64K DRAM type.
R_{OUT}	47	O	—	Pins for RC oscillator Attach variable resistor between R_{OUT} and R_{IN} Generating clock frequency: 640KHz-1MHz.
R_{IN}	48	I	—	

Table 1. KS5911 pin description

'L' = V_{SSB}
'H' = V_{DD}

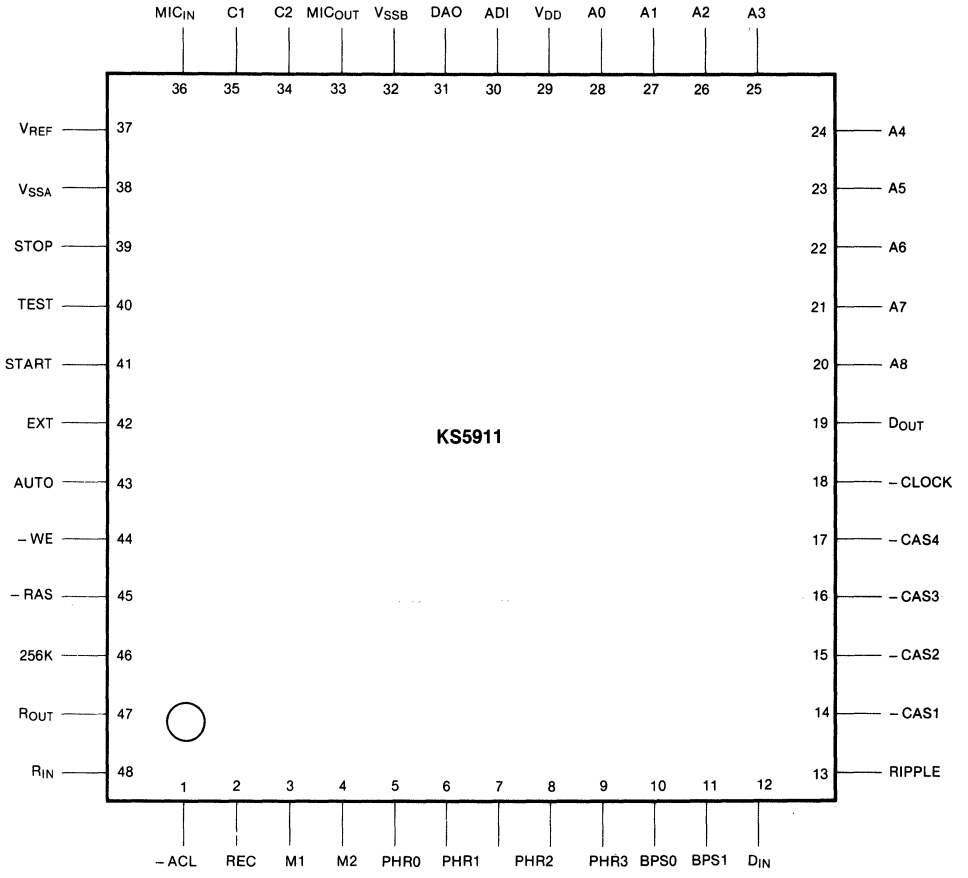


Figure 2. KS5911 Pin configuration (48 QFP, Top view)

FUNCTIONAL DESCRIPTION

Manual Mode (EXT = 'L', TEST = 'L')

Phrase Selection

Using 4 input terminals of PHR0 – PHR3, the sound recording/reproducing of maximum 16 phrases can be performed.

Before starting the sound recording/reproducing, phrases must be specified and can be selected at random.

Pin / Phrase No.	PHR0	PHR1	PHR2	PHR3
No. 0	L	L	L	L
No. 1	L	L	L	H
. . . .				
No. 14	H	H	H	L
No. 15	H	H	H	H

Table 2. Selection of phrases

Selection of bit rate

KS5911 can use 4 kinds of bits rate as shown in Table 4. (8K, 11K, 16K, 32K) which are selected by BPS0 and BPS1 since a bit rate is independently specified for sound recording/reproducing, it is possible to change reproduced voice slow/fast to speak.

Pin / Bit Rate	BPS0	BPS1	Using time (64K)	Using time (256K)
8KBPS	L	L	about 8 sec.	about 32 sec.
11KBPS	L	H	about 6 sec.	about 24 sec.
16KBPS	H	L	about 4 sec.	about 16 sec.
32KBPS	H	H	about 2 sec.	about 8 sec.

*In case of fx = 640 KHz.
*Initial 1Kbits are used index area.

Table 3. Selection of bit rate

Recording procedure

(1) Before recording, KS5911 must be reset by-ACL pin.
(2) REC pin must be H state.
(3) Select bit-rate, phrase number.
(4) When START pin is activated, the contents of address counter are added successively and recording is started.
(5) Then STOP pin is activated or the contents of address counter are reached the maximum address of memory, the recording is stopped.
(6) Repeat from 2), then another phrases are recorded.
(7) Changes of bit-rate and phrase number during recording are ignored.

Reproducing procedure

(1) REC pin must be set to L.
(2) Select bit-rate and phrase number.
(3) If START pin is activated, the start and stop address are readed from index area of memory and reproduced from start address to stop address.
(4) If current address is equal to stop address, reproducing is stopped.
(5) Repeat from 2), then another phrases are reproduced.
(6) Changes of bit-rate and phrase number during reproducing are ignored.

Auto mode

— If AUTO pin is set to "H", KS5911 is auto-tolking back mode.
— Auto mode is independent of REC pin state.
— In the auto mode, KS5911 is automatically recording mode and internal system reset signal is created. Therefore, recording is started.
— In the auto mode, sound information is accumulated to DRAM like manual operation mode.
— When sound stops, namely, silence is detected internally, KS5911 stops automatically recording and reproduces sound stored at the memory.
— If ADI input signal swings within 2.5 ± 0.3125V about 0.5sec, KS5911 set to the reproducing mode automatically.

Reset function

The status during reset operation

Low level to – ACL pin causes the reset to KS5911 and almost internal operations such as recording/reproducing stop, but the refresh counter doesn't stop so that the data stored in DRAM are protected.

The status after reset operation

— Internal address counter is preset to 00400 (H).
— In the recording mode, if recorded address reaches to the maximum address, start input is not given in order to protect DRAM data. The function of RAM-data protection is released by reset so that KS5911 can record newly.

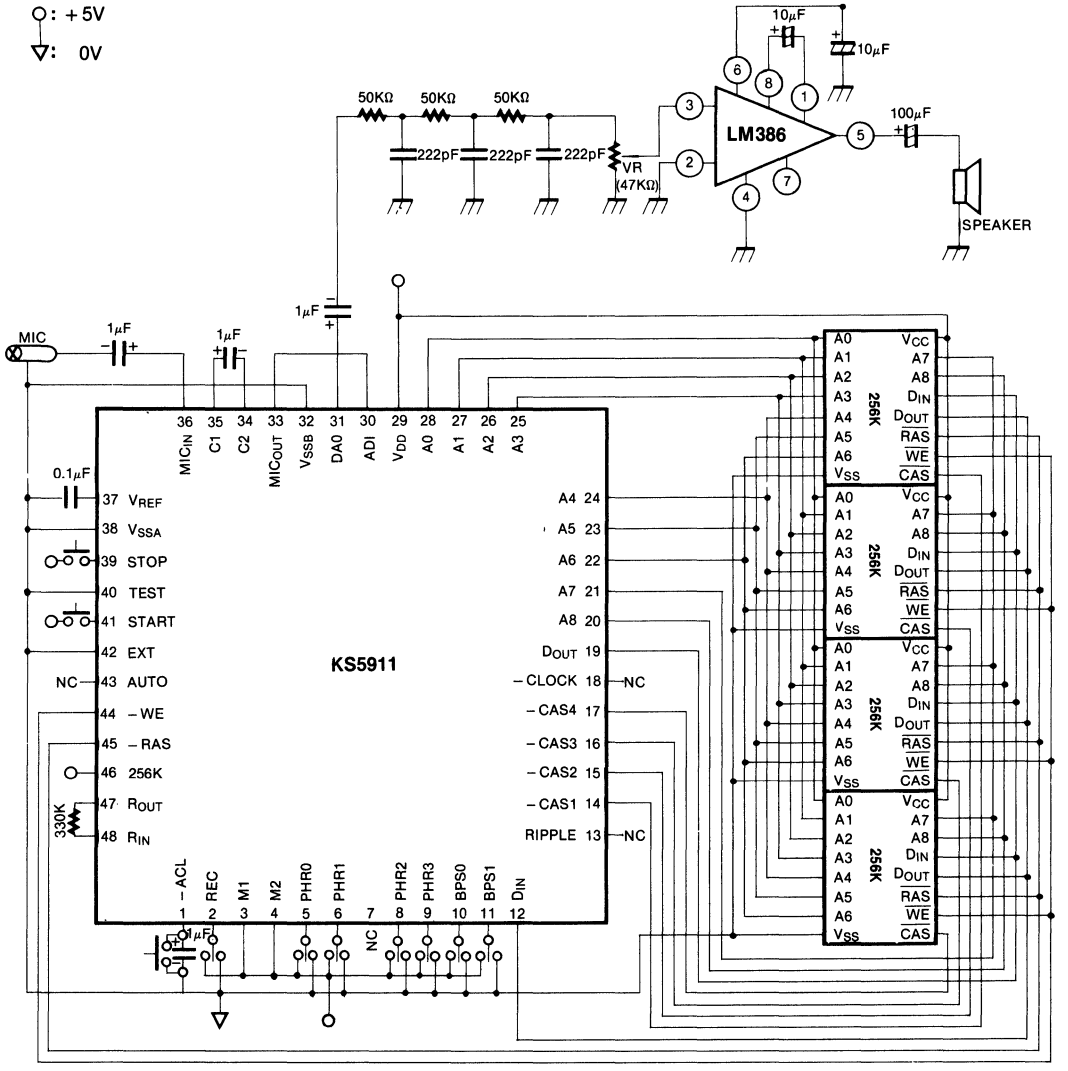
Precautions

— During recording/reproducing operation, pins of M1, M2 and 256K must not be changed.
— System reset doesn't stop the oscillation for the reason of keeping the data in DRAMs.
— The conditions of phrase, bit-rate and recording/reproducing mode settled before start signal is inputed to KS5911 and in the middle of recording/reproducing, conditions of phrase or bit rate must not be changed.
— During recording, start input is not accepted.
— Resistor for RC oscillator must be attached closet to R_{IN}, R_{OUT} pin.
— Output clock (fx) from R_{OUT} is 640 KHz.
If resistor value is small, the frequency is high and resistor value is large the frequency is low.
— If frequency (fx) is high, output voice quality is good because of high bitrate, but frequency is low, output voice quality is bad because of low bitrate.
— At recording mode, built-in mute circuit operates in order to protect bowling effect.

APPLICATION CIRCUIT

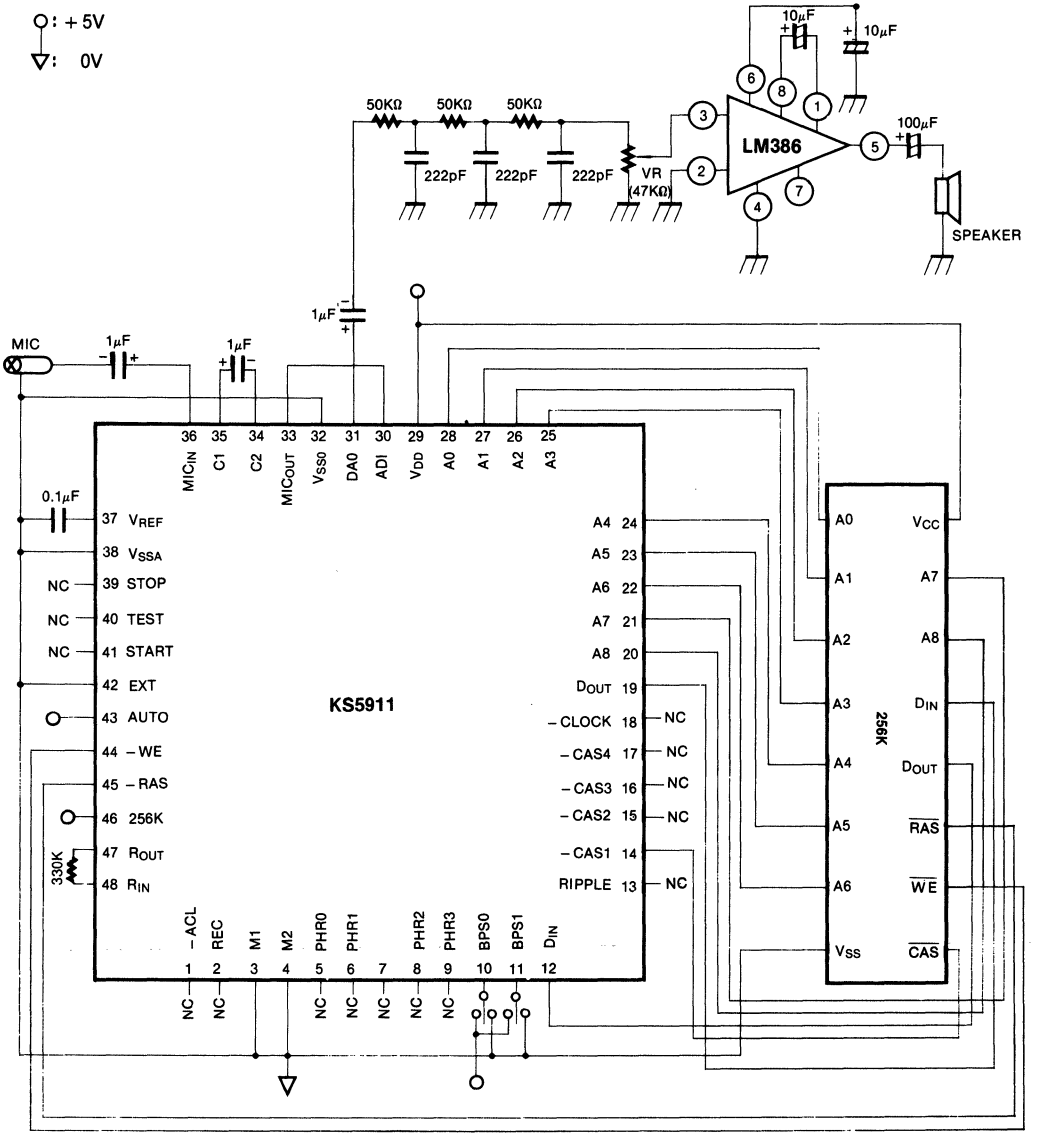
Manual Operation Mode Auto Mode

Auto Mode



*At this diagram, if AUTO (N.C.) set to H, KS5911 is auto-mode.
Figure 3. Application circuit in the manual operation mode

Auto Mode



*The type and number of memory are used 64K DRAM or 256K DRAM and used maximum 4pcs.
Figure 4. Application circuit in the auto mode

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Description	Symbol	Specifications	Unit
Power Supply	V_{DD}	$-0.3 \sim 6.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3$	V
Storage Temperature	T_{ST}	$-30 \sim 90$	C

Table 4. Absolute maximum ratings

Recommended Operation Conditions

Description	Symbol	Specifications	Unit
Power Supply	V_{DD}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{DD}$	V
Operating Temperature	T_{OP}	$-10 \sim 50$	°C
Oscillation Frequency	F_X (fx)	$640 \sim 1000$	KHz

Table 5. Recommended operation conditions

DC Characteristics ($V_{DD} = 5V$, $Ta = 25°C$, $fx = 640$ KHz)

Description	Symbol	Specific Pin	Condition	Min	Typ	Max	Unit
'H' Input Current	I_{IH}	– REC, STOP, START AUTO, TEST, BPS0 BPS1, PHR0—PHR3	$V_{IN} = V_{DD}$		12	18	μA
'L' Input Current 1	I_{IL1}	D_{IN}	$V_{IN} = V_{SSB}$		90	150	μA
'L' Input Current 2	I_{IL2}	– ACL	$V_{IN} = V_{SSB}$		800	1100	μA
'H' Input Voltage 1	V_{IH1}	EXT, D_{IN}	—	3			V
'H' Input Voltage 2	V_{IH2}	All input pin except EXT, D_{IN}	—	4.3			V
'L' Input Voltage 1	V_{IL1}	EXT, D_{IN}	—			0.5	V
'L' Input Voltage 2	V_{IL2}	All input pin except EXT, D_{IN}	—			0.3	V
'H' Output Current	I_{OH}	Output pin	$V_{OUT} = 2.4V$	1.5	3.3		mA
'L' Output Current	I_{OL}	Output pin	$V_{OUT} = 0.8V$	1.0	2.2		mA
Stand-by Current	I_{SS}	V_{SSA}	•Without the external loads at all out pins. •No signal is input		1	1.5	mA

Table 6. DC characteristics

AC CHARACTERISTIC

In the Case of Recording

Description	Symbol	Min	Typ	Max	Unit
Low Address Set-up Time	T_{ASR}	150	—	—	ns
Low Address Holding Time	T_{RAH}	—	—	—	
– RAS Pulse Width	T_{RAS}	—	4.58	—	μs
Column Address Set-up Time	T_{ASC}	150	—	—	ns
Column Address Holding Time	T_{CAH}	500	—	—	
– CAS Pulse Width	T_{CAS}	—	3.05	—	μs
– WE Pulse Width	T_{WEP}	—	3.05	—	μs
Data Output Set-up Time	T_{DWS}	500	—	—	ns
Data Output Holding Time	T_{DWH}	500	—	—	

Table 7. AC characteristics (1)

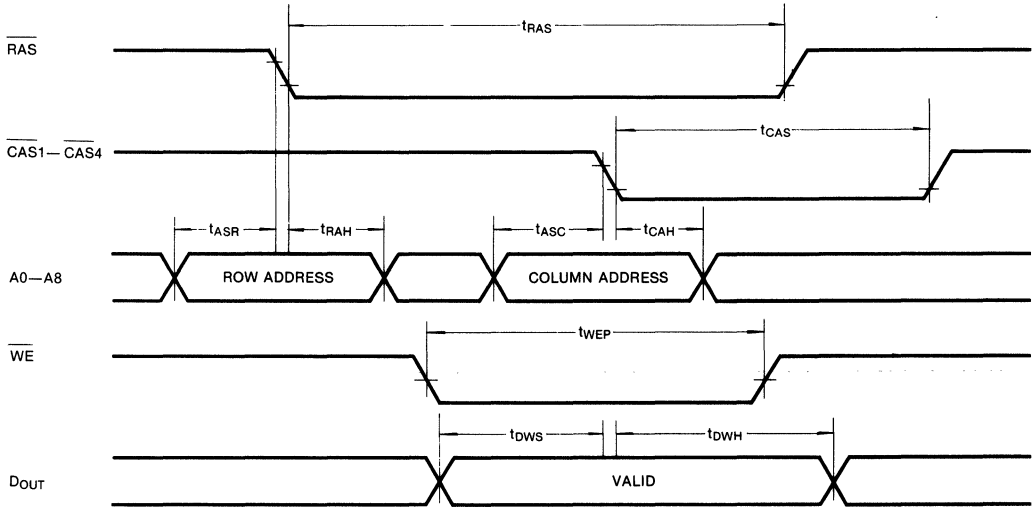


Figure 8. AC Timming Diagrams (1)

In the Case of Reproducing

Description	Symbol	Min	Typ	Max	Unit
Data Input Set-up Time	t_{DCS}	500	—	—	ns
Data Input Holding Time	t_{DCH}	0	—	—	

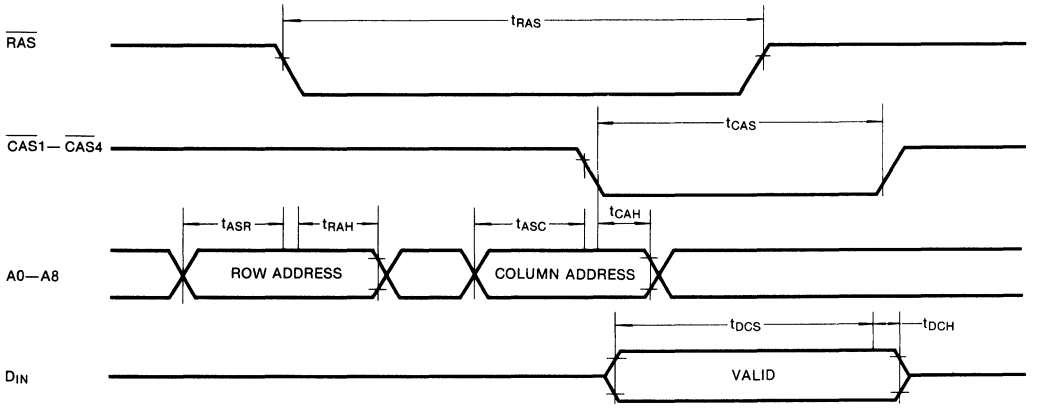


Figure 7. AC Timing Diagrams (2)

Analog Characteristics

Description	Symbol	Specific Pin	Condition	Min	Typ	Max	Unit
Input Voltage Range	V_{IN1}	MIC_{IN}	AMP (1) + AMP (2)			12.5	mV_{p-p}
	V_{IN2}	MIC_{IN}	AMP (1)			125	
	V_{IN3}	C2	AMP (2)			250	
Voltage Gain	V_{G1}	MIC_{IN}-MIC_{OUT}	$V_{IN} = 6mV_{p-p}$ fin = 100 Hz – 10 KHz		46		db
	V_{G2}	MIC_{IN}-C1			26		
	V_{G3}	C2-MIC_{OUT}			20		
Output Resistance	R_{OUT1}	C1	—		1.2		KΩ
	R_{OUT2}	MIC_{OUT}			1.2		
Input Voltage Range	V_{IN4}	ADI	—	1.25		3.75	V
Output Resistance	R_{OUT3}	DAO	—		0.9		KΩ

Table 9. Analog characteristics

CMOS 1-CHIP SPEECH SYNTHESIZER

KS5912XX is a one chip voice/sound reproducing LSI using CVSD (Continuously Variable Slope Delta modulation) algorithm.

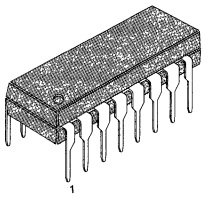
This LSI is capable of reproducing voice/sound up to 8 seconds, seperating 4 phrases.

KS5912XX consists of voice reproducing logic, 64 Kbits ROM to contain encoding data, 10 bits D/A converter, control logic, RC oscillator for cost effect.

This LSI can be used for various applications required for voice and sound reproducing (especially, TOY industry), having simple control method and external circuit.

Voice and sound encoding data that have been edited by ADM tooling system are programmed into internal ROM by changing one mask during the device fabrication.

16 DIP



FEATURES

- **Single chip voice & sound generation LSI by ADM method**
- **On-chip 64 Kbits mask ROM**
- **Simple manual control**
- **Repetition function: 3 times/8 times/infinite**
- **Selectable phrase: 4 phrase**
- **Maximum generation time: 8 sec (8 KHz sampling)**
- **Variable bit rate (make option): 32kbps/16kbps/11kbps/8kbpsss**
- **660 KHz RC Oscillation**
- **On-chip 10 bits D/A converter**
- **Single 5V power supply**
- **Low power consumption by CMOS logic**
- **16 DIP type**

ELECTRICAL CHARACTERISTICS

1) Absolute Rating

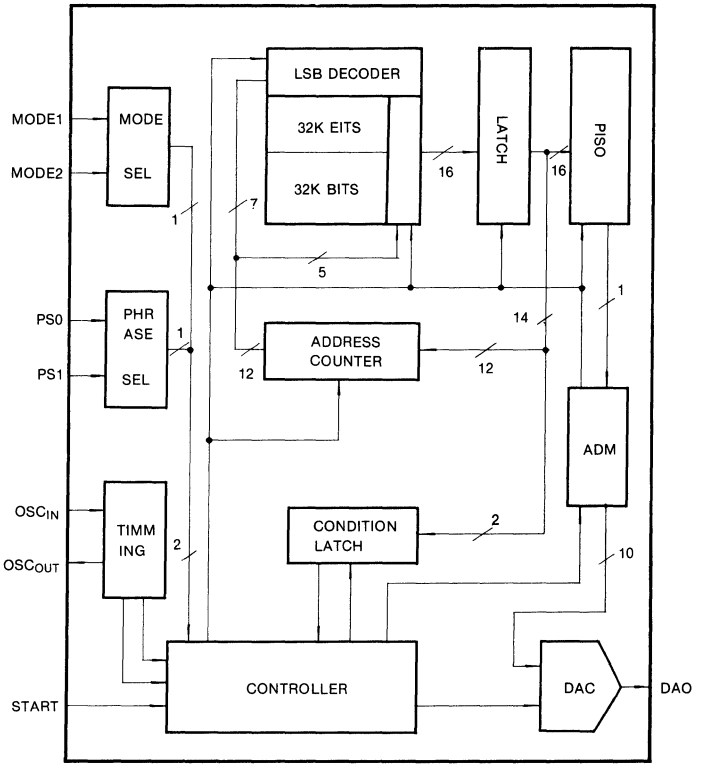
Description	Symbol	Specifications	Unit
Power Supply	V_{DD}	$-0.3 \sim 6.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Storage Temperature	T_{ST}	$-55 \sim 120$	
Operation Temperature	T_{OP}	$-10 \sim 55$	

2) DC Characteristics

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}		3.5	5	5.5	V
Operation Current	I_{DDA}	$V_{DD}=5V$	—	600	900	μA
Stand-by Current	I_{DDB}	$V_{DD}=5V$		100	150	μA
Oscillation Frequency	f_{OSC}	$V_{DD}=5V$ $R=240K\Omega$		660		kHz
DAO Output Voltage	V_{OUT}	NO load	1.25	—	3.75	V
Pull Up Resistor	R_{INH}	MODE1, 2		300		KΩ
Pull Down Resistor	R_{INL}	PS0, 1 START		300		KΩ
		– ACL		17		KΩ

5

INTERNAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

PHRASE SELECTION

Before starting the sound reproducing, phrase must be specified by selection of PS0 and PS1

PS1	PS0	Selected Phrase
L	L	#1 Phrase
L	H	#2 Phrase
H	L	#3 Phrase
H	H	#4 Phrase

Operating Mode Selection

KS5912XX can be performed 3 kinds of mode by using 2 input terminals of mode 1 & mode 2

H: +5V
L: 0V

Mode 2	Mode 1	Operating Mode
H	H	Normal Mode
L	H	REP3 Mode (3 times repetition mode)
H	L	REP8 Mode (8 times repetition mode)
L	L	Not Used

Normal Mode

(1) Normal mode shall be specified by using 2 input terminals of mode 1 and mode 2 (M1:H, M2:H)
(2) The phrase shall be selected by PS0 and PS1 switch.
(3) Sound reproduces by start input ("H" state).
(4) When the ACL terminal becomes "L" level under reproducing, the internal state of KS5912 is initialized and is become stand-by mode.

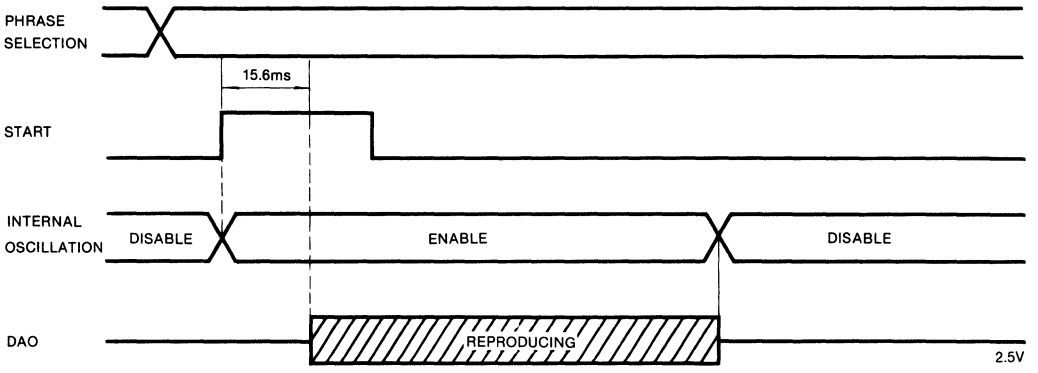


Figure 1. Timming Diagram at Normal Mode

REP3/REP8 Mode

1) REP3/REP8 model shall be specified by using 2 input terminal of mode 1 and mode 2 (M1:H, M2:L/M1:L, M2:H).
2) The phrase shall be selected by PS0 and PS1 switch.
3) The sound of selected phrase repeats 3 times or 8 times by mode selection.
4) Change of phrase or start input is ignored under reproducing.
5) Reproducing can be stopped by ACL input ("L").

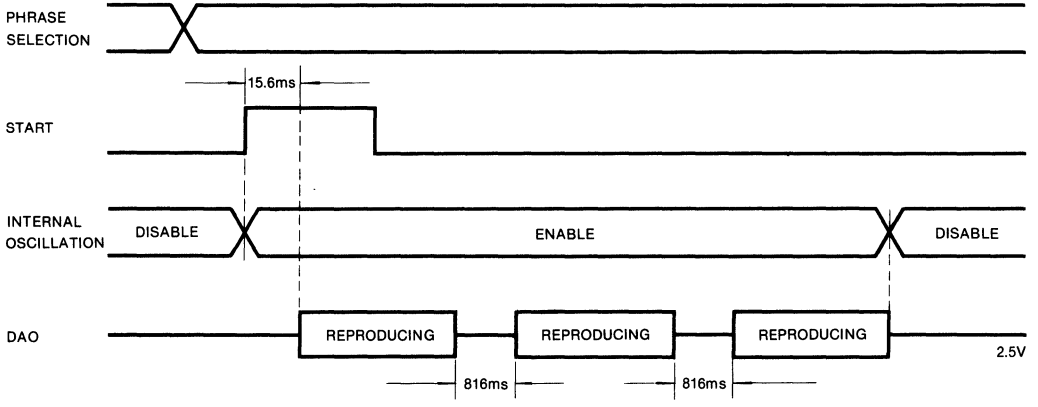


Figure 2. Timming Diagram at REP3 Mode

Infinite Mode

When start signal keeps "H" state continuously, the sound reproduces continuously irrespective of mode (normal, REP3/REP8).

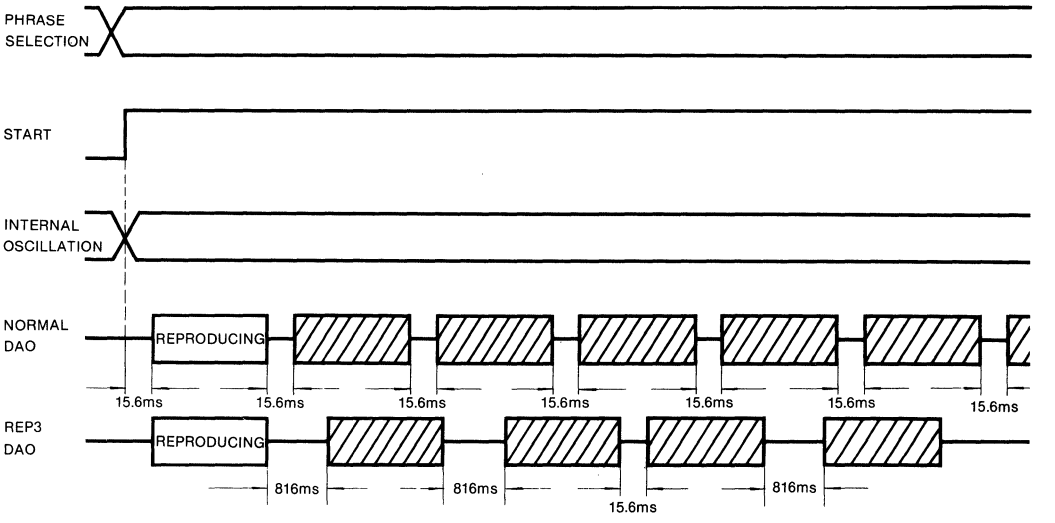


Figure 3. Timming Diagram at Infinite Mode

Start Operation

KS5912XX mask ROM is consist of 16 bits × 4K and index area is stored start address and bit rate for phrase 1, 2, 3 and 4.

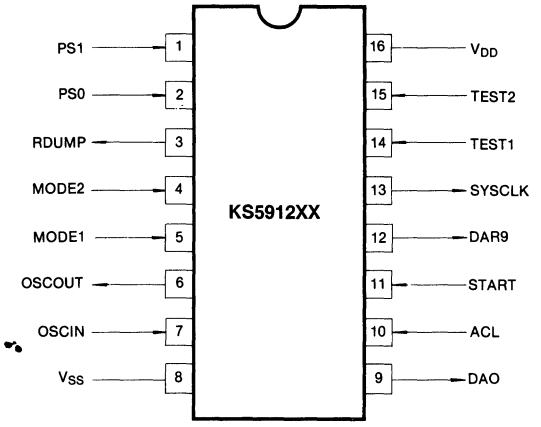
KS5912XX stops internal oscillation for power dissipation at stand-by.

After selection of phrase and start signal, it starts internal oscillation and reproduces sound by information of index area.

Start signal debouncing time for protection of chattering by SW., etc. is 15.6ms. When start signal activates "H", sound reproducing is repeated continuously.

PIN CONFIGURATIONS

1) Pin Assignments



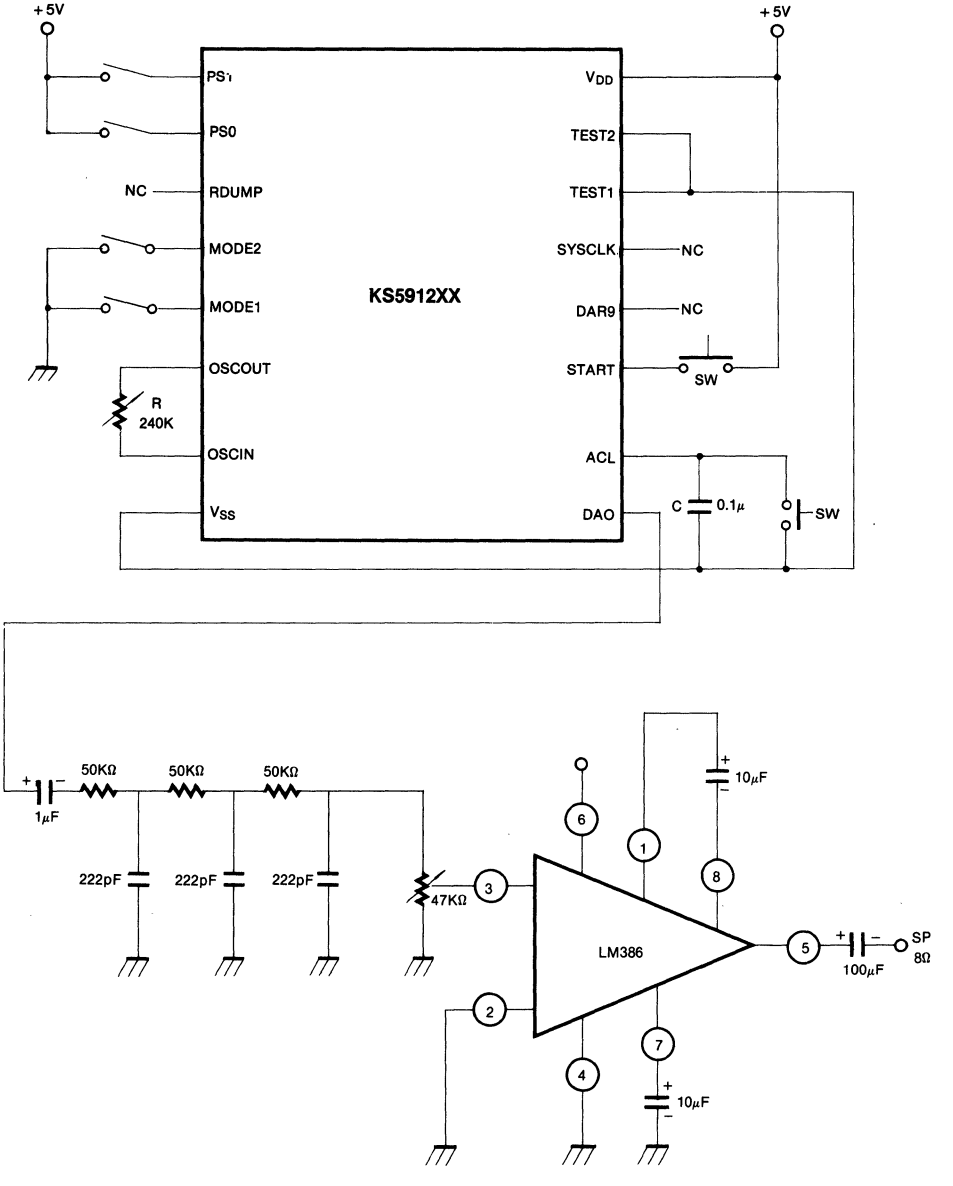
(KS5912XX Pin Assignments)

2) Pin Descriptions

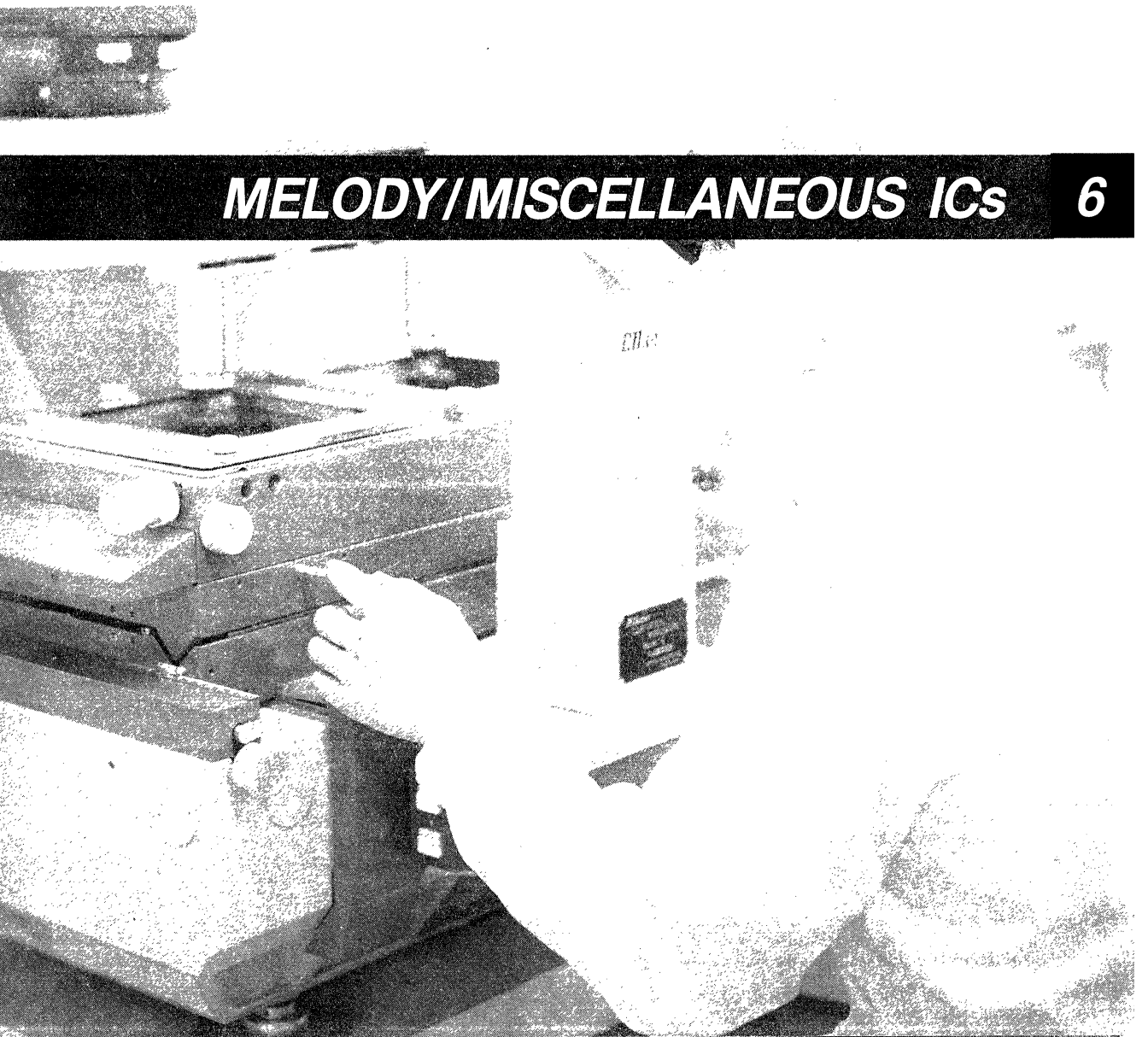
Pin No.	Name	I/O	Descriptions
1	PS1	I	Phrase selection pins (pull-down)
2	PSO	I	
3	RDUMP	O	Internal status output pin for test
4	MODE2	I	MODE selection pin 2 (pull-up)
5	MODE1	I	MODE selection pin 1 (pull-up)
6	OSCOUT	O	660 KHz, RC oscillator OUTPUT pin
7	OSCIN	I	660 KHz, RC oscillator INPUT pin
8	V_{SS}	—	GROUND
9	DAO	O	10 bit D/A converter output
10	– ACL	I	System reset pin (Low Active)
11	START	I	Start signal input pin (pull-down)
12	DAR9	I/O	TEST pin Normally N.C.
13	SYSCLK	O	System clock output pin (128 KHz)
14	TEST1	I/O	TEST pin (Normally Ground)
15	TEST2	I/O	TEST pin (Normally Ground)
16	V_{DD}	—	+5 Volt

TYPICAL APPLICATION CIRCUIT

NORMAL MODE



MELODY/MISCELLANEOUS ICs 6



Melody ICs

Device	Function	Package	Page
KS5310	Simple Melody with Watch	Bare Chip	269
KS5313	Simple Melody IC	8/16 DIP	273
KS5381	Multi Melody IC	16/20 DIP	277
KS5814	Sky-Lark's or Cricker's Sound IC	14 DIP	286

Miscellaneous ICs

Device	Function	Package	Page
KS5116	Functions 6 Digits UP/DOWN Counter Circuit for Triplexed LCD	Bare Chip	289
KS5815	Centigrade/Fatirenhert Clinical Thermometer	60 FQP	295

SIMPLE MELODY WITH WATCH

The KS5310 series is a CMOS LSI chip which electronically plays a prearranged melody.

FUNCTIONS

- Tempo: 16 kinds (presto-largo)
- Sound range: 2.5 octave
- High start input
- Melody stop input
- Selection of automatic stop or repeat of the melody

FEATURES

- **One chip CMOS construction**
- **Plays a melody consisting of 64 notes**
- **Starts from the head of melody**
- **Very low stand-by current**
- **Designed to use with CMOS digital watch circuit**
- **32,768Hz operating frequency**
- **1.5V operation**

BLOCK DIAGRAM

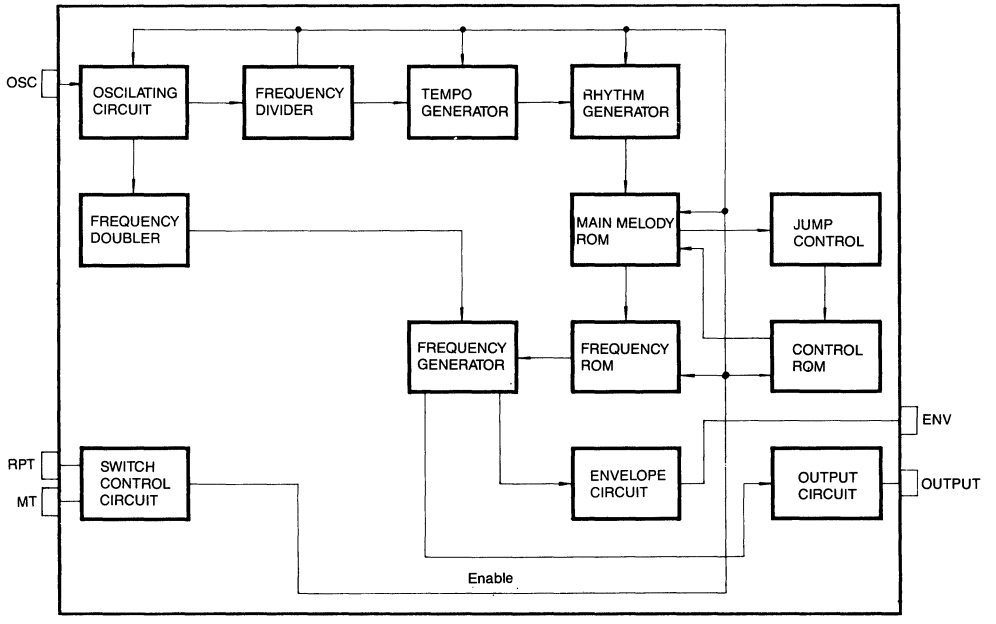


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{SS}	+0.3 ~ −2.0	V
Input Voltage	V_{IN}	V_{SS}+0.3 ~ V_{DD}−0.7	V
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

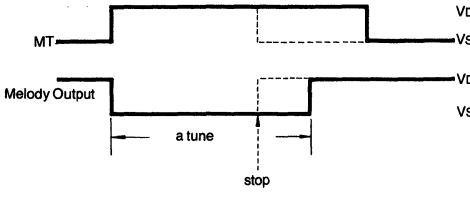
ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{SS}=−1.5V, V_{DD}=0V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS}\|$		1.2	1.5	2	V
Stand-by Current	I_{ST}	Without Load		0.1	0.3	μA
Operating Current	I_{OP}	Without Load		20	30	μA
Input Low Voltage	V_{IL}		V_{SS}	V_{SS}	V_{SS}+0.1	V
Input High Voltage	V_{IH}		V_{DD}−0.1	V_{DD}	V_{DD}	V
Input Low Current	I_{IL}	V_{IL}=V_{SS}			0.05	μA
Input High Current	I_{IH}	V_{IH}=V_{DD}	1.5		15	μA
Output High Current (Output Terminal)	I_{OH}	V_{SS}=−1.2V V_{OH}=−0.7V	30			μA
Output Low Voltage	V_{OL}	Without Load	V_{SS}	V_{SS}	V_{SS}+0.1	V
Output High Voltage	V_{OH}	Without Load	V_{DD}−0.1	V_{DD}	V_{DD}	V

OUTPUT TIMING

1) RPT=V_{SS} (OPEN)



2) RPT=V_{DD}

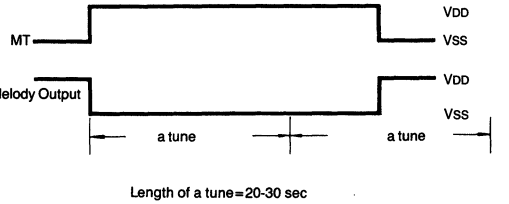
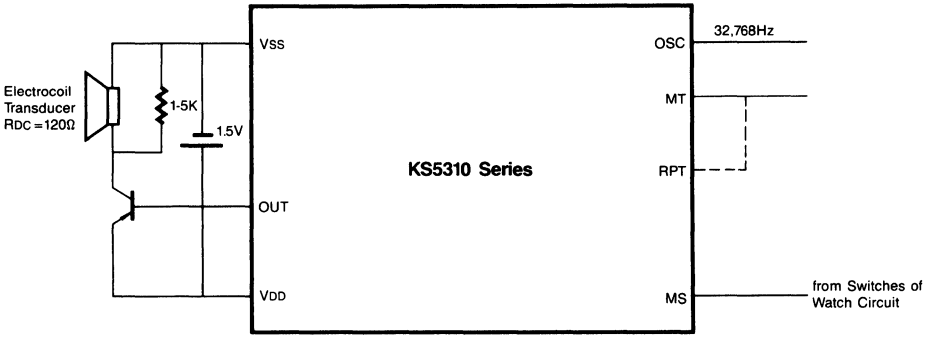


Fig. 2

APPLICATION CIRCUIT



*Currently available types
KS5310A: Oh! Susanna

Fig. 3

PAD DIAGRAM

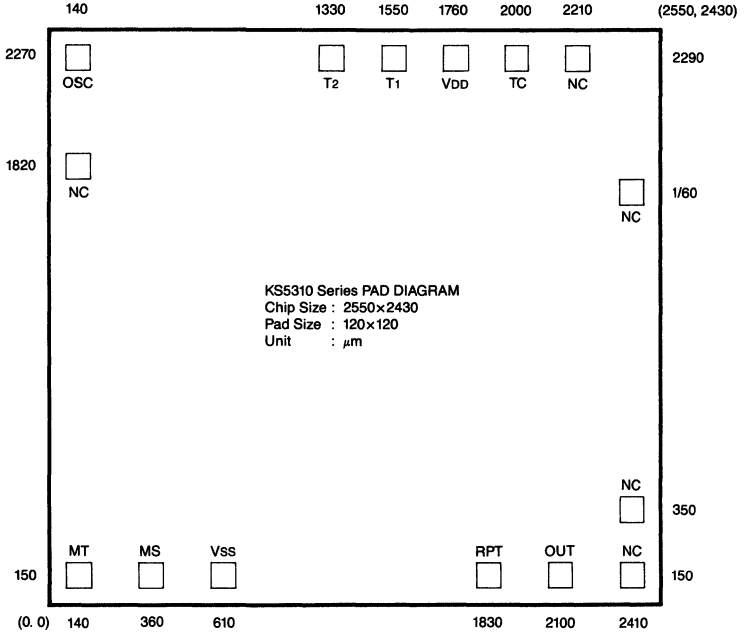


Fig. 4

CUSTOM ORDER

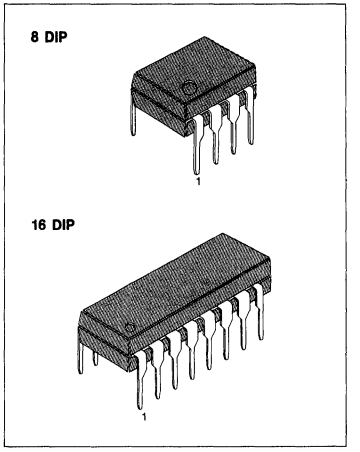
Changing the contents of melody ICs are possible by reprogramming the maskable ROM. Please free to contact us for more information including ORDER spec.

CUSTOM ORDER SPEC

1. Request Date:
2. Development Term:
3. Melody
   a. Song name:
   b. Melody Time:
   c. Tempo:
   d. Octave Range:
   e. Repeated Syllable: (Yes/No)
4. Function
   a. Melody Start Input (Active High/Active Floating)
   b. Melody Start Signal (Level Hold/One Shot)
   c. Repeat Input (RPT)
   d. Repeat Interval
   e. Melody Stop Input:
   f. Output Pad:
   g. Application Set
5. Others.

SIMPLE MELODY IC

The KS5313 series is a CMOS LSI chip which electronically plays a prearranged melody.



FUNCTIONS

- Tempo: 16 kinds
- Sound range: 2.5 octave
- Selection of melody start switch (Active high switch or active floating switch)
- Selection of melody start signal (Level hold or one shot trigger)
- Selection of automatic stop or repeat of the melody
- Melody stop input
- Level Hold mode/one shot mode user option: 16 Dip
- Level Hold mode only: 8 Dip.

FEATURES

- **One chip CMOS construction**
- **Plays a melody consisting of 64 notes**
- **Starts from the head of melody**
- **Very low stand-by current**
- **33KHz operating frequency**
- **1.5V operation**

6

BLOCK DIAGRAM

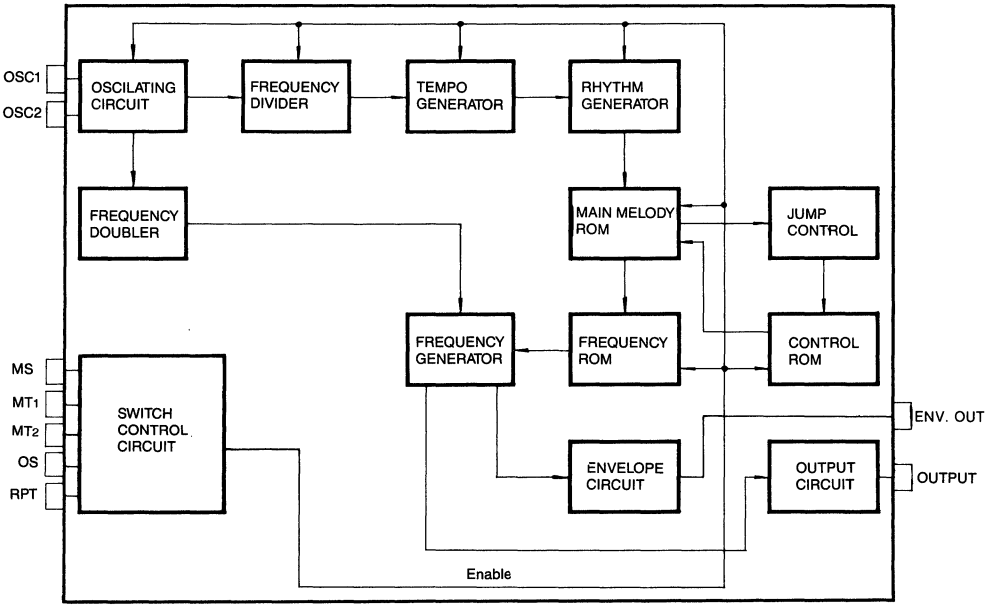


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	0.3 ~ −2.0	V
Input Voltage	V_{IN}	V_{SS} +0.3 ~ V_{DD} −0.7	V
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

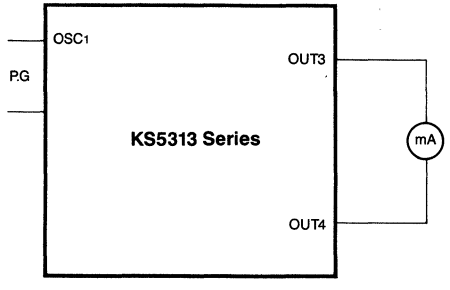
ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{SS} = −1.5V, V_{DD} =0V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	$\|V_{SS}\|$		1.2	1.5	2	V
Input High Voltage	V_{IH}		V_{DD} −0.1		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		V_{SS} +0.1	V
Strand-by Current	I_{ST}	Without Load		0.1	0.3	μA
Operating Current	I_{OP}	Without Load		20	30	μA
Input High Current	I_{IH}	V_{IH} = V_{DD}	1.5		15	μA
Input Low Current	I_{IL}	V_{IL} = V_{SS}			0.05	μA
Output 0 Current	I_{o0}	V_{SS} = −1.2V, V_{OH} = −0.7V, E_{NV} = V_{SS}	15			μA
Output 3, 4 Current	$I_{O(3,4)}$	V_{DD} =I0V, V_{SS} = −1.5V	±1.8			mA
Output Low Voltage	V_{OL}	Without Load	V_{SS}		V_{SS} +0.1	V
Output High Voltage	V_{OH}	Without Load	V_{DD} −0.1		V_{DD}	V
Operating Frequency	F_{OSC}		30	33	36	KHz

TEST CIRCUIT

1) OUT 3 AND OUT 4 DRIVE CURRENT TEST CIRCUIT



P.G: Pulse Generator (1020Hz)

Fig. 2

2) OUT 0 CURRENT TEST CIRCUIT

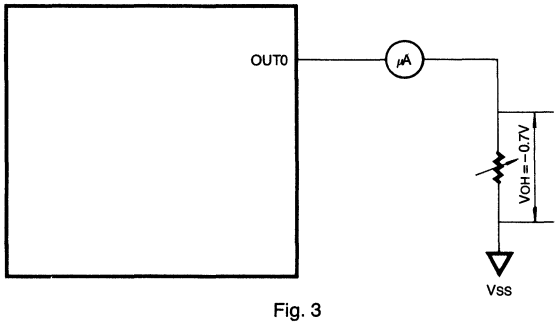
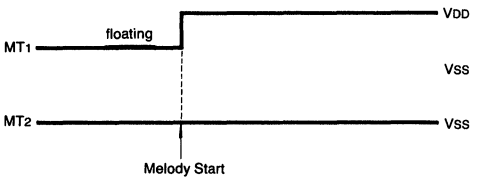


Fig. 3

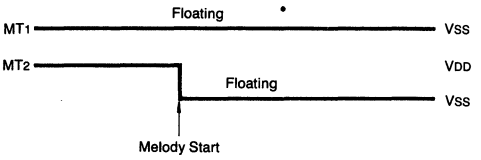
TIMING

1) MELODY START INPUT

a) MT_1 (Active High Input)

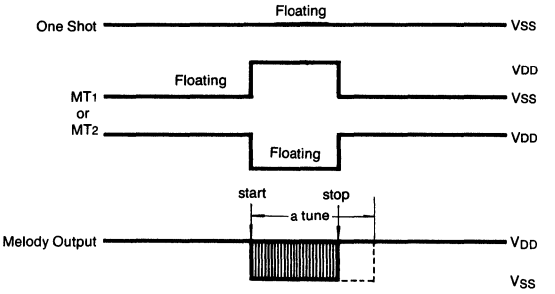


b) MT_2 (Active Floating Input)

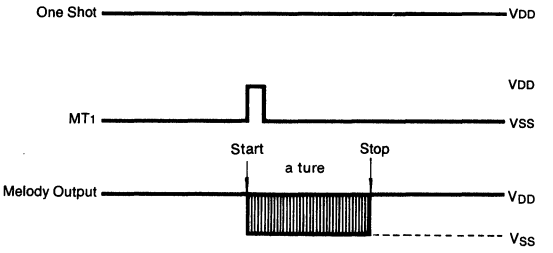


2) MELODY START SIGNAL

a) Level Hold Mode

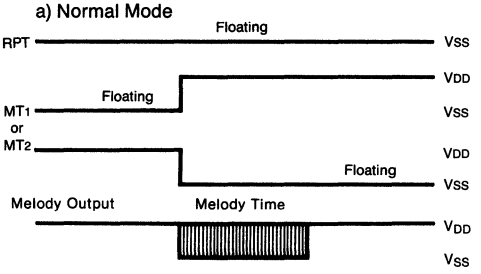


b) One Shot Mode

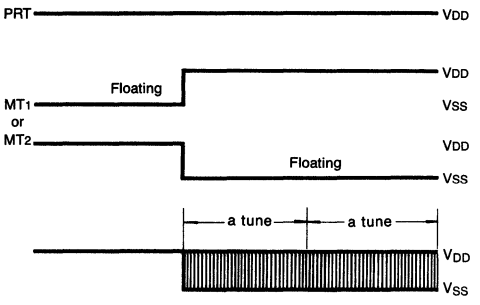


3) REPEAT INPUT

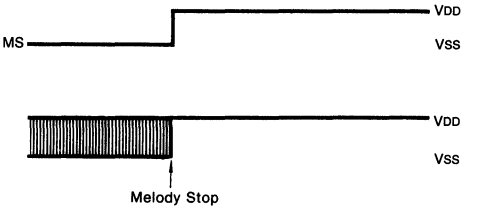
a) Normal Mode



b) Repeat Mode



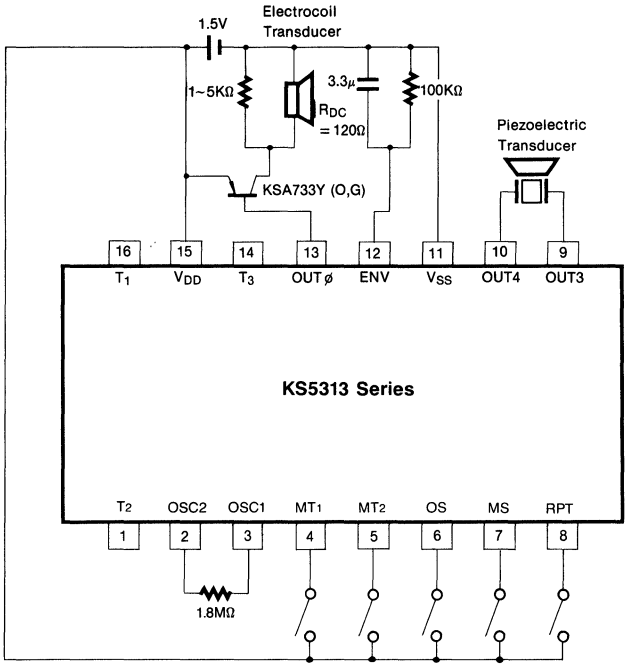
4) MELODY STOP



6

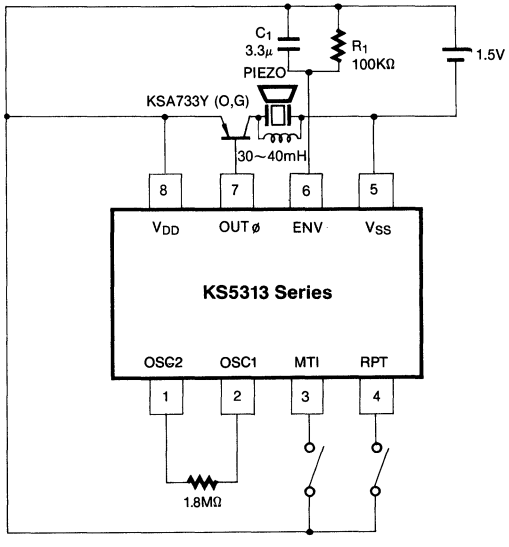
APPLICATION CIRCUIT

1) ONE SHOT & LEVEL HOLD MODE



* Currently available types
KS5313N: MINUET (BACH)
KS5313Q: Home Sweet Home
KS5313S: Big Ben
KS5313T: For Elise
KS5313P: Cuchoo's Waltz
KS5313R: Oh! Susanna

2) LEVEL HOLD MODE



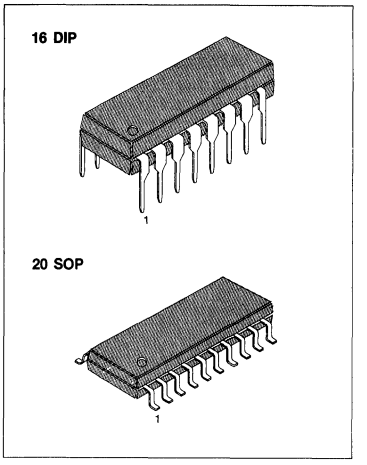
*C_1 and R_1 are necessary only when employ ENVELOPE circuit. Otherwise, ENVELOPE terminal must be connected to V_{SS}.

MULTI MELODY IC

The KS5381 is a CMOS melody IC, the circuit is composed of 512 word ROM, address counter, tempo & rhythm generator, address control circuit, envelope signal generator, switch control circuit, RC oscillator and tone generator. Since the KS5381 includes envelope circuit, it can generate good melody sound without any external component for envelope circuit.

The KS5381 can select 8 melodies in serial select mode and 7 pieces of melody in binary select mode.

The KS5381 can easily connect with the SST standard watch.



FUNCTION

- Tempo: 16 kinds
- Sound Range: 3 octave (G4—G7)
- Play one melody, auto stop
- Play all melodies serially
- Melody stop function
- Serial/binary select mode: bare chip, 20 DIP
- Serial select mode: 16 DIP

FEATURES

- **One chip CMOS construction**
- **Max. 8 melodies, 512 word ROM**
- **Internal envelope circuit**
- **Piezo direct drive**
- **Very low stand-by current**
- **33 KHz operating frequency**
- **1.5V or 3.0V operation**

BLOCK DIAGRAM

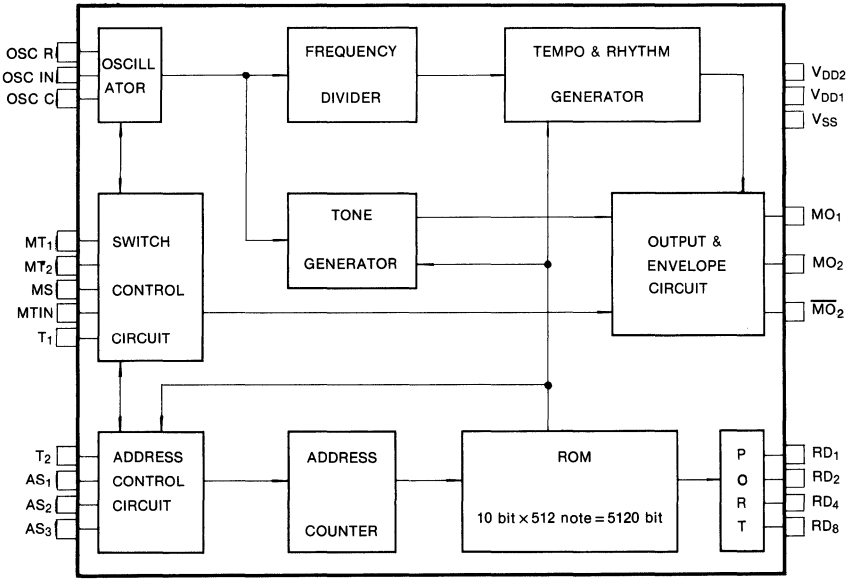


Fig. 1.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage 1	$V_{SS} \sim V_{DD1}$	$-0.3 \sim 4.0$	V
Supply Voltage 1	$V_{SS} \sim V_{DD2}$	$-0.3 \sim 4.0$	
Input Voltage 1	V_{IN1}	$V_{SS}-0.3 \sim V_{DD1}+0.3$	V
Input Voltage 2	V_{IN2}	$V_{SS}-0.3 \sim V_{DD2}+0.3$	
Output Voltage 1	V_{OUT1}	$V_{SS}-0.3 \sim V_{DD1}+0.3$	V
Output Voltage 2	V_{OUT2}	$V_{SS}-0.3 \sim V_{DD2}+0.3$	
Storage Temperature	T_{stg}	$-55 \sim +125$	°C
Operation Temperature	T_{opr}	$-20 \sim +70$	°C

ELECTRICAL CHARACTERISTICS

1.5V Battery Operation ($Ta = 25°C$, $V_{SS} = 0V$, V_{DD1}, $V_{DD2} = 1.55V$)

Characteristics	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Operation Voltage	V_{DD1}		1.25	1.55	3.3	V
	V_{DD2}		1.25	1.55	3.3	
Switch Input Current	I_{IH1}	$V_{IN} = 1.55V$	0.2	1	10	μA
	I_{IL1}	$V_{IN} = 0V$			0.05	
Test Input Current	I_{IH2}	$V_{IN} = 1.55V$	2	10	100	μA
	I_{IL2}	$V_{IN} = 0V$			0.05	
Input Voltage	V_{IH}		1.25			V
	V_{IL}				0.3	
Standby Current	I_{DD}	Without load		0.1	0.5	μA
Output Current MO_2, $\overline{MO_2}$	I_{OH1}	$V_{OH} = 1.0V$	200			μA
	I_{OL1}	$V_{OL} = 0.5V$	200			
*1 Output Resistor of MO_1	RO_1	$V_{OH} = 0.7V$ t1		17		KΩ
	RO_2	$V_{OH} = 0.7V$ t2		30		
	RO_3	$V_{OH} = 0.7V$ t3		50		
	RO_4	$V_{OH} = 0.7V$ t4		75		
	RO_5	$V_{OH} = 0.7V$ t5		110		
	RO_6	$V_{OH} = 0.7V$ t6		170		
	RO_7	$V_{OH} = 0.7V$ t7		260		
	RO_8	$V_{OH} = 0.7V$ t8		450		
	I_{OL2}	$V_{OL} = 0.5V$	2			μA
Switch Chartering Time	T_{CH}	F = 32768 Hz		62.5		mS

†1. See Fig. 4 (t1 ~ t8)

BATTERY OPERATION ($Ta = 25°C$, $V_{SS} = 0V$, $V_{DD1} = 1.5V$, $V_{DD2} = 3.0V$)

Characteristics	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Operation Voltage	V_{DD1}		1.25	1.5	2.4	V
	V_{DD2}		2.4	3.0	3.3	
Switch Input Current	I_{IH1}	$V_{IN} = 3.0V$	1	6	60	μA
	I_{IL1}	$V_{IN} = 0V$			0.1	
Test Input Current	I_{IH2}	$V_{IN} = 3.0V$	5	60	300	μA
	I_{IL2}	$V_{IN} = 0V$			0.1	
Input Voltage	V_{IH}		2.4			V
	V_{IL}				0.3	
Standby Current	I_{DD}	Without load		0.2	1	μA
Output Current MO_2, $\overline{MO_2}$	I_{OH1}	$V_{OH} = 2.5V$	400			μA
	I_{OL1}	$V_{OL} = 0.5V$	400			
Output Resistor of MO_1	RO_1	$V_{OH} = 2.1V$ t1		17		KΩ
	RO_2	$V_{OH} = 2.1V$ t2		30		
	RO_3	$V_{OH} = 2.1V$ t3		50		
	RO_4	$V_{OH} = 2.1V$ t4		75		
	RO_5	$V_{OH} = 2.1V$ t5		110		
	RO_6	$V_{OH} = 2.1V$ t6		170		
	RO_7	$V_{OH} = 2.1V$ t7		260		
	RO_8	$V_{OH} = 2.1V$ t8		450		
	I_{OL2}	$V_{OL} = 0.5V$	2			μA
Switch Chartering Time	T_{CH}	F = 32768 Hz		62.5		mS

6

MELODY SELECT

1. Binary Select Mode
   The KS5381 can repeat a melody which select from 7 melodies.
   (see Table 1 and Fig. 2)

2. Serial Select Mode
   While AS_3, AS_2, AS_1 pins are low level or open, that is, melody select counter is reset, the first melody start by pushing the switches (MT_1, MT_2) at the same time. The next simultaneous pushing of the switches (MT_1, MT_2) will change the melody to the next one. If the switch MT_1 and MT_2 are pushed continuously, the 8 melodies will repeat by itself.
   The total number of melody can be selected at will within 8 by mask option.

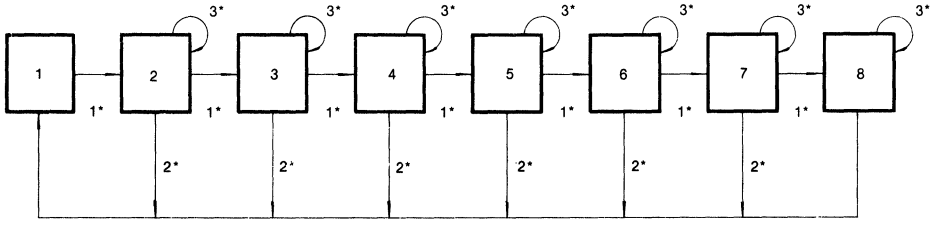


Fig. 2. The Sequence of Melody

1* Advanced by serial select mode
2* Selected by mask option
3* Selected by binary select mode

Usage	Melody	AS_3	AS_2	AS_1
Serial Selection	No. 1-No. 8	L	L	L
Binary Selection	No. 2	L	L	H
	No. 3	L	H	L
	No. 4	L	H	H
	No. 5	H	L	L
	No. 6	H	L	H
	No. 7	H	H	L
	No. 8	H	H	H

Table 1. Serial and Binary Selection (H: V_{DD}, L: V_{SS} (open))

KS5381A SONG LIST

1. Home Sweet Home
2. Oh! Susanna
3. Whispering Hope
4. Dreaming of Home and Mother
5. Oh! My darling Clementine
6. Beautiful Dreamer
7. Red River Valley

MELODY OPERATING

There are two method to start the melody. One is pushing the MT_1 and MT_2 at the same time. The other is to supply DC or watch alarm signal at "MTIN" pin.

1. Switch Operation

When the switch MT_1 and MT_2 are pushed at the same time, the melody start. The switch MT_1, MT_2, MS is used for melody stop. Continuous and simultaneous pushing of switch MT_1 and MT_2 will repeat the same melody in binary select mode and change the 8 melodies serially in serial select mode. Fig. 2 shows operation of these switches.

The melody keep on sounding until the switch MS is on. While MT_1 and MT_2 switches are on, the melody is off as long as MS switch is on. The same melody will restart (binary select opt.) or the next melody will start (serial selection opt.) in 0.75 sec after the MS switch returns to off.

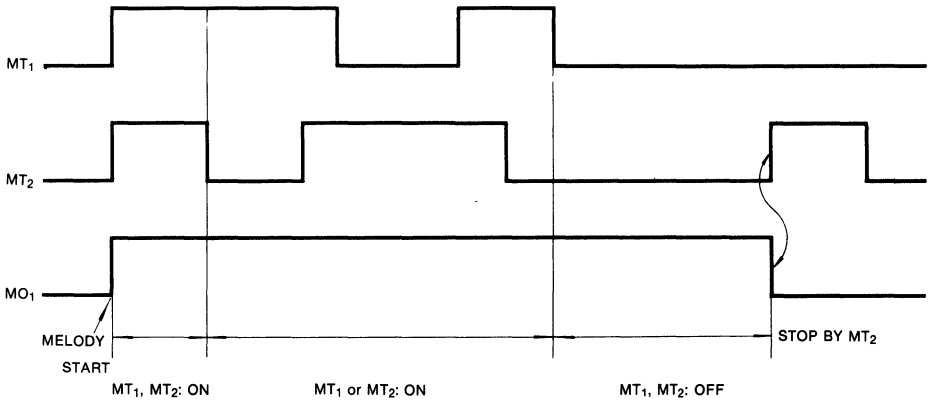


Fig. 3.

2. Alarm Signal Operation

- **On-Hour and Switch Conformation Chime**

The KS5381 has a 0.75 sec timer circuit to prevent the melody from starting by DC or AC signal. The melody does not start by chime sound of the KS5910 or signal below 0.75 sec.

- **Melody Start**

The signals to start melody are the DC or AC signal which is over 0.75 sec. The signals under 0.75 sec will make the KS5381 melody stand-by mode.

- **Melody Stop**

The melody does not stop until it plays the end of the melody even if alarm signal stopped. Though the alarm signal is longer than the melody signal, the melody does not repeat. If the melody is needed to be stopped in the midway, it can be done using either switch MT_1 or MT_2.

- **Melody Sound**

The output frequency of the melody is 400-1500 Hz (musical interval) with signal of 50% duty.

ENVELOPE FUNCTION

The KS5381 has an envelope circuit for high tone quality without any external component. The envelope circuit make the melody output decrease exponencially. (as shown in Fig. 4.) The transistor for amplification would be NPN type and has proper h_{fe} in order to keep this waveform.

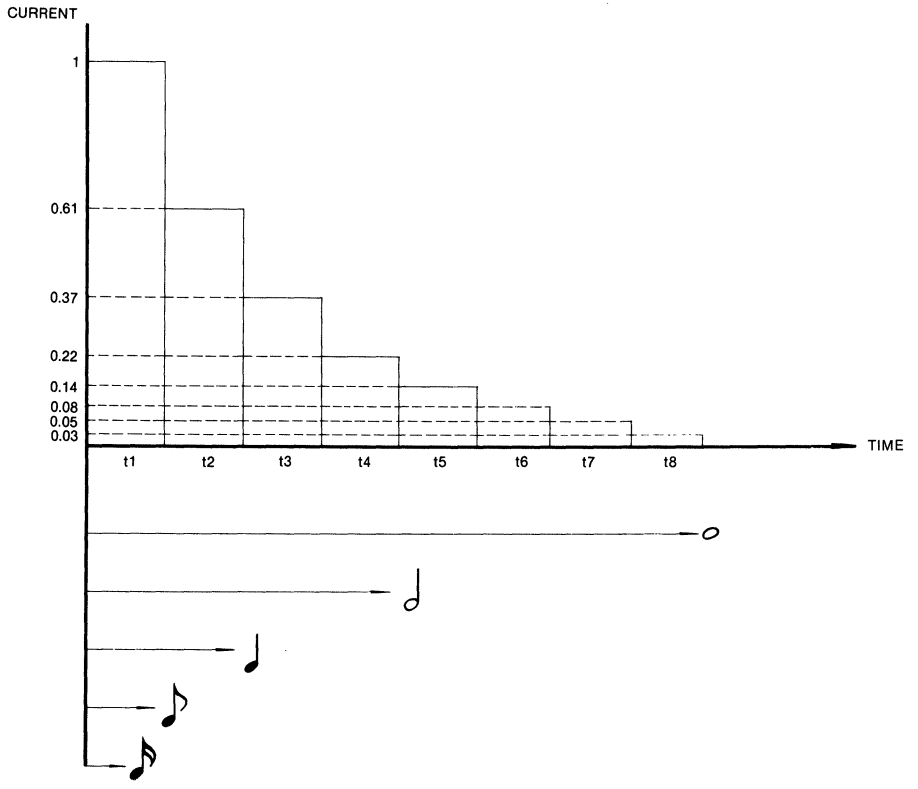


Fig. 4

RC OSCILLATOR

The KS5381 oscillator is composed of 3 inverters, a resistor and a capacitor. The frequency of the oscillator is determined by a external capacitor and a resistor. The frequency of the oscillator vary by applying voltage and temperature, therefore it is right to use trimmer resistor for getting precise 32768 Hz.

PAD DIAGRAM

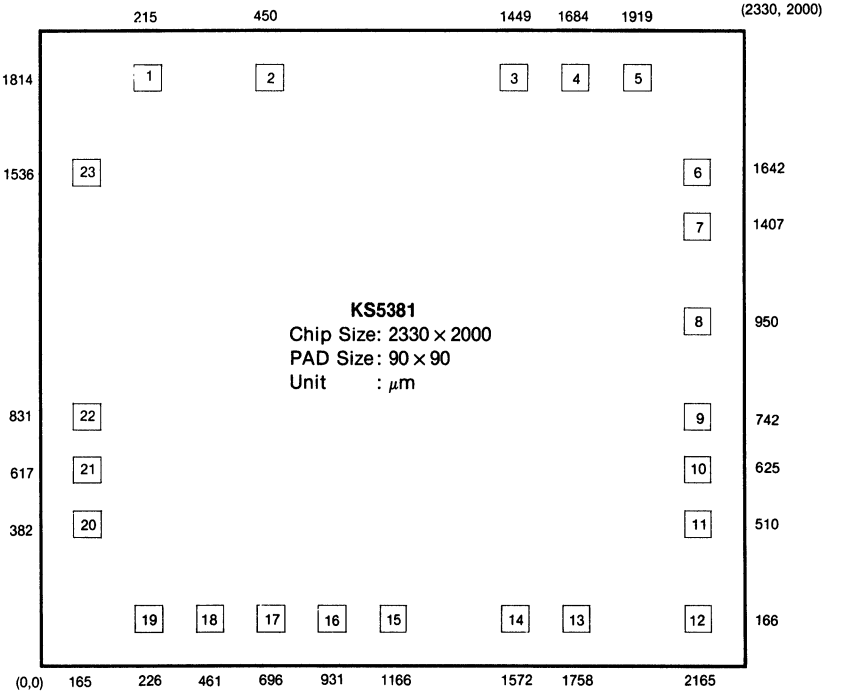


Fig. 5

PAD DESCRIPTION

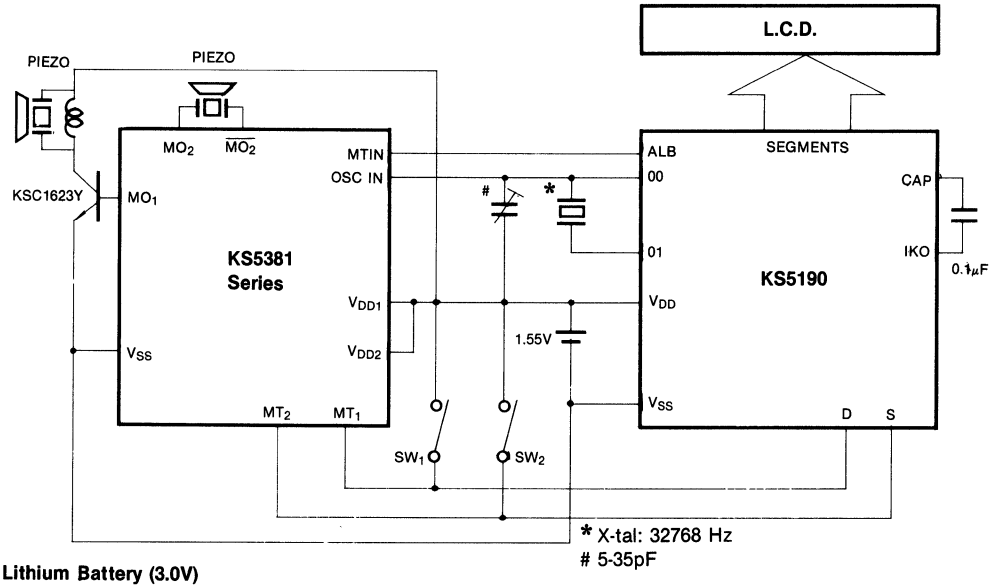
No.	Pin Name	Description	No.	Pin Name	Description
1	MO_2	Direct Piezo Driver	13	MT_2	Start & Stop Input
2	$\overline{MO_2}$	Direct Piezo Driver	14	MS	Melody Stop
3	AS_1	Melody Selection	15	MTIN	Trigger Signal Input
4	AS_2	Melody Selection	16	T_2	Test Input
5	AS_3	Melody Selection	17	T_1	Test Input
6	OSC R	Oscillation	18	RD_8	Test Terminal
7	OSC IN	Oscillation & Ext. Input	19	RD_4	Test Terminal
8	OSC C	Oscillation	20	RD_2	Test Terminal
9	V_{DD1}	1.5V-3.0V Power Supply	21	RD_1	Test Terminal
10	V_{DD1}, V_{DD2}	1.5V-3.0V Power Supply	22	V_{SS}	0V Power Supply
11	V_{DD2}	1.5V-3.0V Power Supply	23	MO_1	ENV. Melody Output
12	MT_1	Start & Stop Input	24		

* Pull-down resistor is incorporated into MT_1, MT_2, MS, MTIN, T_1 and T_2.

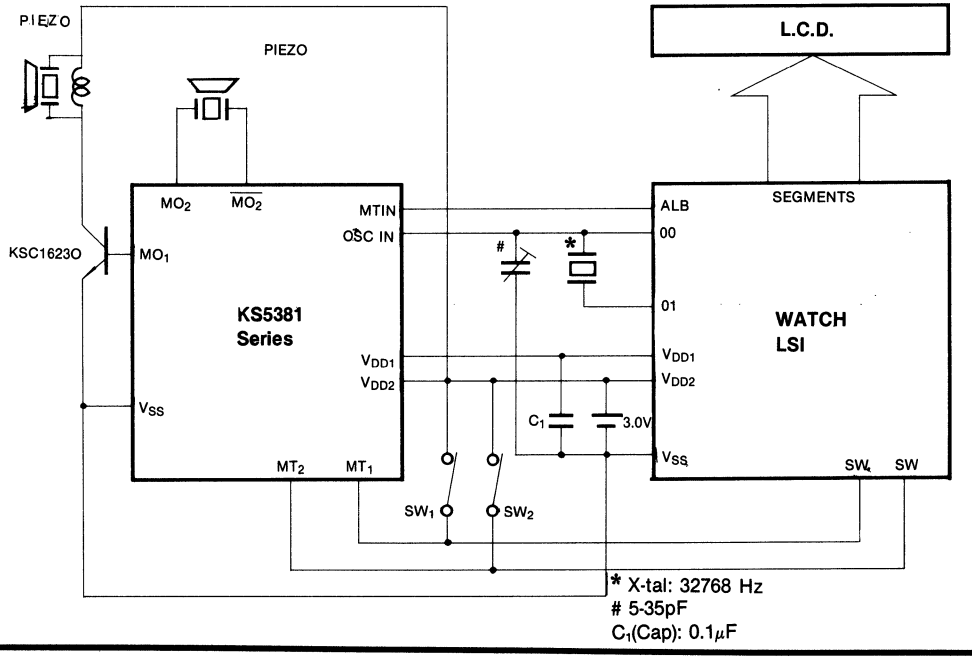
APPLICATION CIRCUIT

1. Combination with Watch

1) Ag0 Battery (1.55V)

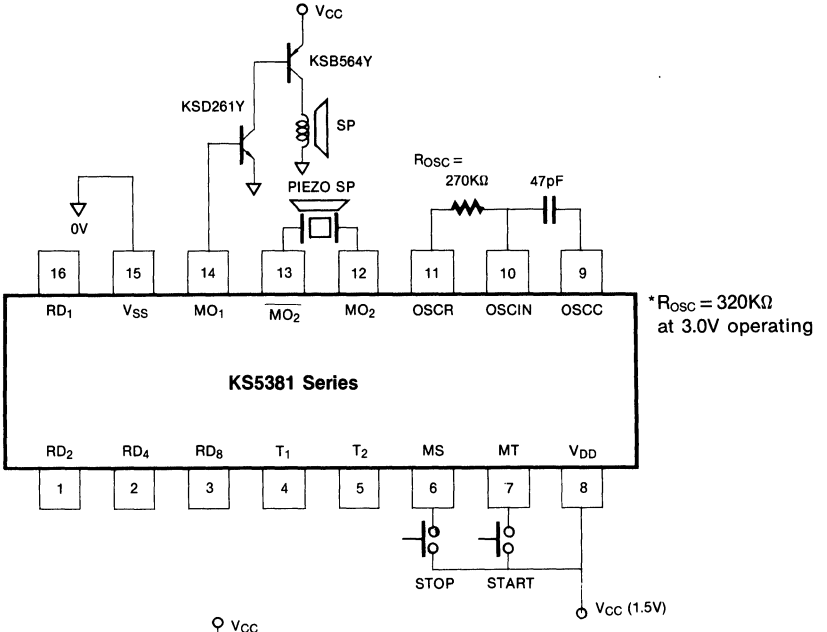


2) Lithium Battery (3.0V)



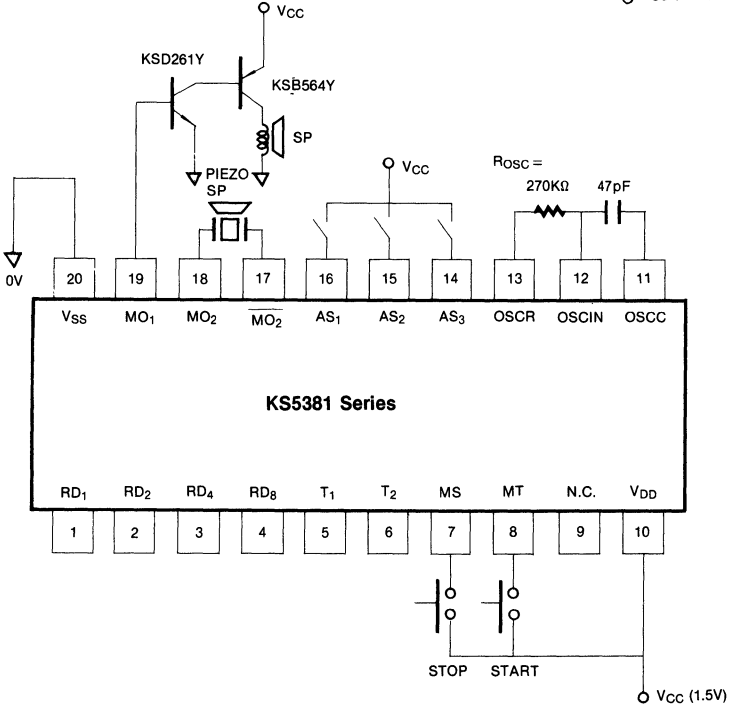
2. PACKAGE APPLICATION CIRCUIT

1) 16 DIP type



*ROSC = 320KΩ at 3.0V operating

2) 20 DIP type



6

SKY-LARK'S OR CRICKET'S SOUND IC

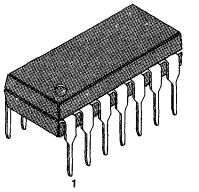
The KS5814 is a CMOS LSI chip which generates either Sky-lark's sound or Cricket's sound.

The RC oscillator frequency is used to generate acoustic pulses for the sounds.

The sound is initiated by $\overline{\text{AL-IN}}$, and continued as long as $\overline{\text{AL-IN}}$ is connected to V_{SS}.

If the $\overline{\text{AL-IN}}$ switch is open, the oscillater will be stopped, thus all operation will be stopped.

14 DIP



FUNCTIONS

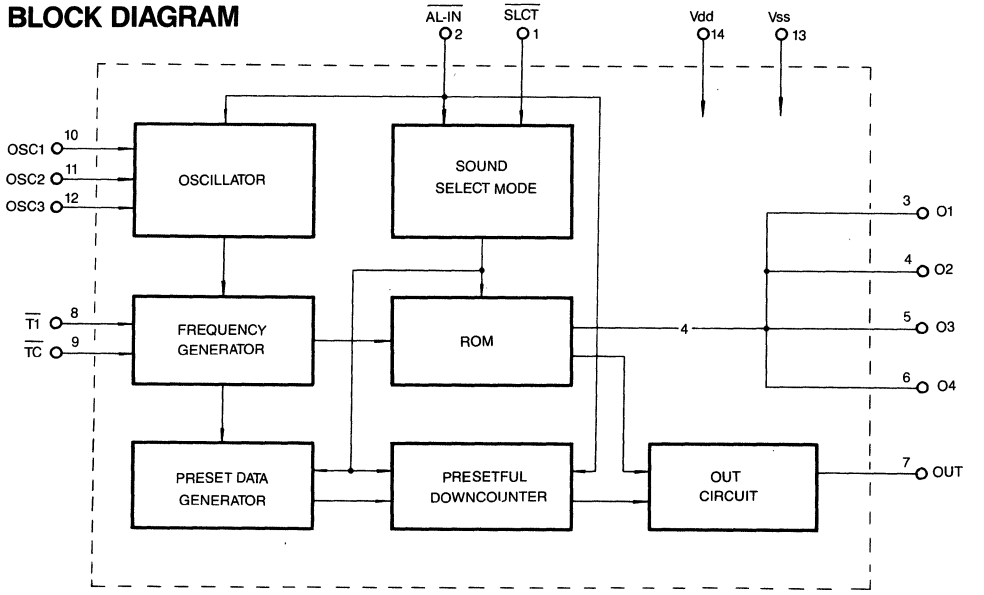
- Selectable either Sky-lark's sound or Cricket's sound by SLCT input

$\overline{\text{AL-IN}}$	$\overline{\text{SLCT}}$	SOUND
L	H	SKY-LARK'S SOUND
L	L	CRICKET'S SOUND
H	—	No operation

FEATURES

- **Single Chip CMOS construction.**
- **RC oscillator.**
- **Speaker drive by using a PNP transistor.**
- **Single battery (1.5V) operation.**
- **Low power dissipation.**
- **14 pins dual-in-line plastic package.**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +3.0	V
Input Voltage	V_{IN}	V_{SS} −0.3 ~ V_{DD} +0.3	V
Operating Temperature	Topr	−10 ~ +55	°C
Storage Temperature	Tstg	−55 ~ +125	°C

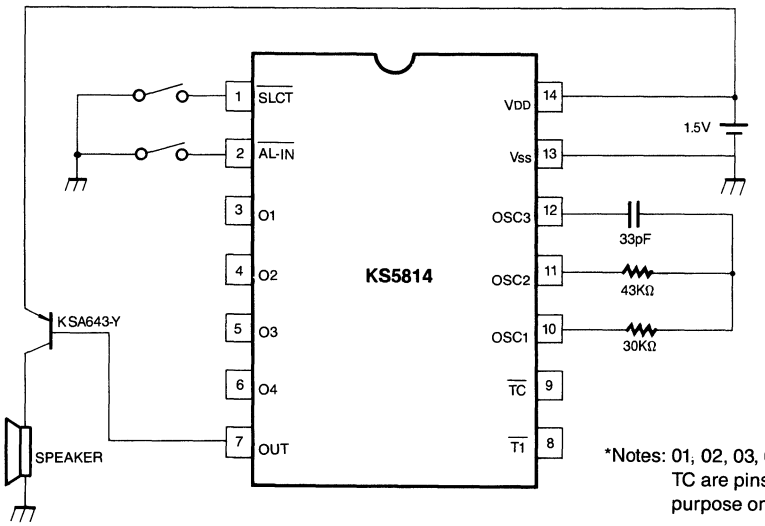
*Value grater than this may result in damage to the circuit.

ELECTRICAL CHARACTERISTICS

(V_{SS} =0V, V_{DD} =1.5V, T_a =25°C; unless otherwise specified)

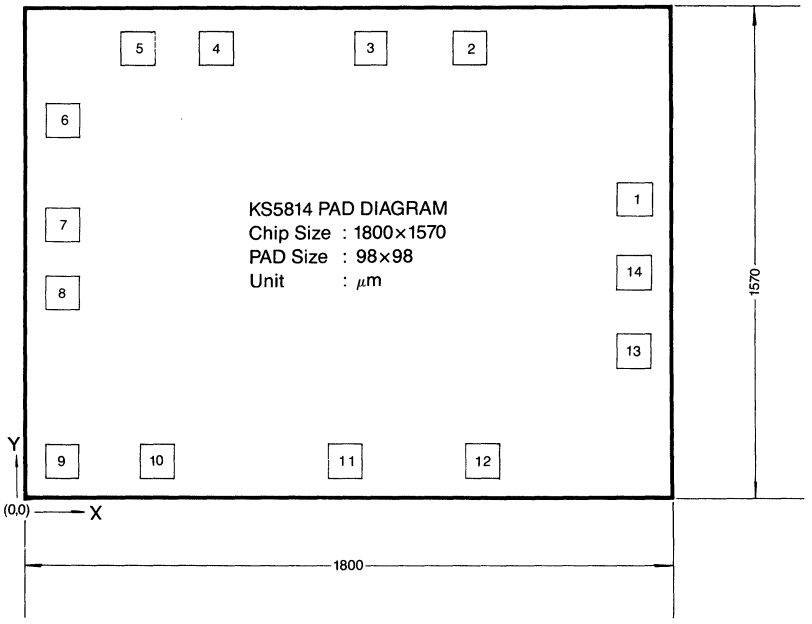
Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.2	1.5	1.8	V
Stanby-by Current	I_{ST}	Without Load		0.1	0.3	μA
Operating Current	I_{OP}		100	250	400	μA
Input Low Voltage	V_{IL}				0.2	V
Input High Voltage	V_{IH}		V_{DD}-0.4			V
Switch Input Current	I_{SW}	Vin=V_{SS}		60	100	μA
Alarm Sink Current	I_{OS}	Rm=1KΩ, V_{DD} =1.2V	0.4	0.7		mA
Oscillation Frequency	F_{OSC}		200	210	220	KHz

APPLICATION CIRCUIT



*Notes: 01, 02, 03, 04, T1 and TC are pins for test purpose only.

PAD DIAGRAM



COORDINATES OF PAD

(Unit: μm)

Pad No.	Name of Pad	Coordinates	
		X	Y
1	$\overline{SLCT}$	1671	800
2	$\overline{AL\text{-}IN}$	1446	1441
3	01	1043	1441
4	02	522	1441
5	03	334	1441
6	04	129	1307
7	OUT	129	830

Pad No.	Name of Pad	Coordinates	
		X	Y
8	$\overline{T_1}$	129	642
9	$\overline{T_C}$	129	129
10	OSC_1	464	129
11	OSC_2	1029	129
12	OSC_3	1379	129
13	V_{SS}	1671	523
14	V_{DD}	1671	720

FUNCTIONS 6 DIGITS UP/DOWN COUNTER CIRCUIT FOR TRIPLEXED LCD

The KS5116 is a silicon-gate CMOS LSI for 6 digits LCD display up/down counter.
It operates on single 1.5V battery and the circuit time base is a 16KHz internal RC oscillator.

FUNCTIONS

- Count up, from zero to any setting number
- Count down, from any setting number to zero
- User selectable up/down mode
- Alarm function
- Output pulse for any external mechanism
- LCD, alarm test

FEATURES

- **Single chip CMOS construction.**
- **Built-in RC oscillator**
- **Built-in voltage doubler**
- **6 digits triplexed LCD drive**
- **4 Switch operation**
- **Low power consumption**
- **Single 1.5V battery operation.**

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage ($V_{DD1} - V_{SS}$)	V_{DS1}	$-0.3 \sim +2.0$	V
Supply Voltage ($V_{DD2} - V_{SS}$)	V_{DS2}	$-0.3 \sim +4.0$	V
Operating Temperature	T_{opr}	$-20 \sim +60$	°C
Storage Temperature	T_{stg}	$-30 \sim +125$	°C

* Voltage greater than above may result in damage to the circuit.

ELECTRICAL CHARACTERISTICS ($T_a = 25°C$, $V_{DD} = 1.5V$, $V_{SS} = 0V$; unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}		1.2	1.5	1.8	V
	V_{DD2}		2.4	3.0	3.6	V
Supply Current	I_{DD}	Without Load		9	18	μA
Input High Voltage	V_{IH}		$V_{DD} - 0.3$		V_{DD}	V
Input Low Voltage	V_{IL}		V_{SS}		$V_{SS} + 0.3$	V
Switch Activation Current	I_{SW}	$V_{in} = V_{DD}$	0.1	1.5	5	μA
Alarm Drive Current	I_{apu}	$V_{sat} = 0.5V$	0.5	2		mA
	I_{aou}	$V_{sat} = 0.5V$	50			μA
Oscillator Frequency	F_{OSC}		25	32	40	KHz
DC-DC Conversion Frequency	F_{CON}	$C1 = C2 = 0.1\mu F$	800	1,024	1,250	Hz
LCD Frequency	F_d		33	43	53	Hz
Switch Debounce Time	t_1		25			mSEC
Switch Periode Time	t_2		35			mSEC

FUNCTIONAL DESCRIPTION

1. LOCK MODE

When power is on or AC switch is depressed, the state is in lock mode. Where D switch is blocked and S switch is enable. The depression of S switch in the lock mode will select setting mode.

2. SETTING MODE

If S switch is depressed in the lock mode, the state becomes setting mode. The D switch is used to advance the function. The flag is off.

- Digit 5,6 flashing mode
  Digit 5,6 will flash at a 1Hz rate when S switch is depressed in the lock mode. If D switch is depressed, the counter of digit 5,6 will advance. Whenever D switch is depressed, the counter of digit 5,6 will advance.
- Digit 3,4 flashing mode
  The next depression of S switch will select digit 3,4 flashing mode. In digit 3,4 flashing mode, digit 3,4 flashes at a 1Hz rate. The operation by using D switch is same as digit 5,6 flashing mode.
- Digit 1,2 flashing mode
  The next depression of S switch will select digit 1,2 flashing mode. In digit 1,2 flashing mode, digit 1,2 flashes at a 1Hz rate. The operation by using D switch is same as digit 5,6 flashing mode.

3. ALL FLASHING MODE

The next depression of S switch will select all flashing mode. All digit flashes at a 1Hz rate with flag up or down. User can select up or down mode

4. NORMAL MODE

The next depression of S switch will select normal mode. If user selects up mode in the all flashing mode, all of digits display 000000. If user selects down mode the digits display setting number in the Setting mode. The next depression of S switch will select digit 5, 6 flashing mode. If D switch is depressed. The counter is counted up or down by state of flag being up or down.

5. COUNTING MODE

The depression of D switch in normal mode will enter counting mode. If counter is matched to setting number in up mode or down mode, alarm sound and outputs pulse output.

6. ALL CLEAR OPERATION

The depression of AC switch will select lock mode in every mode.

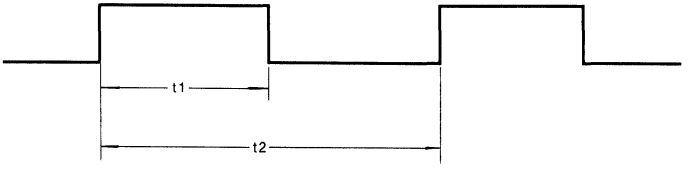
7. LAMP TEST

The depression of S, D and AC switch at a same time will display all digit segment and cause alarm sound with flag (up or down).

8. ALARM MODE

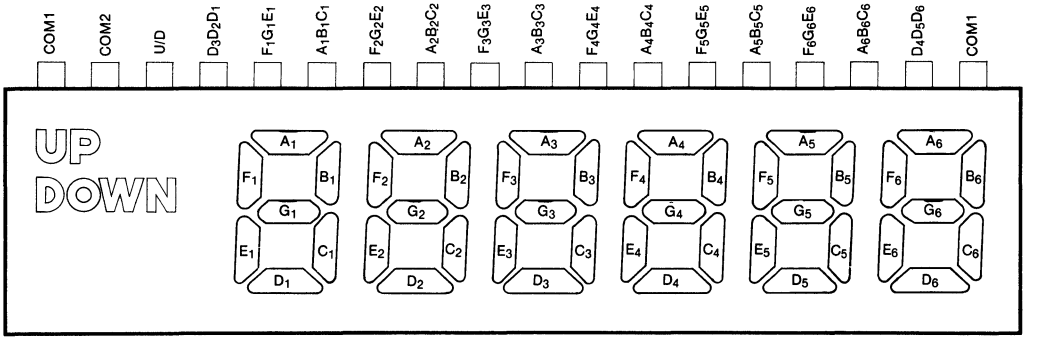
The depression of D and S switch is blocked in alarm mode. After the counter is matched to setting number in up mode or down mode.

* Switch can recognize minimum 30 times per second



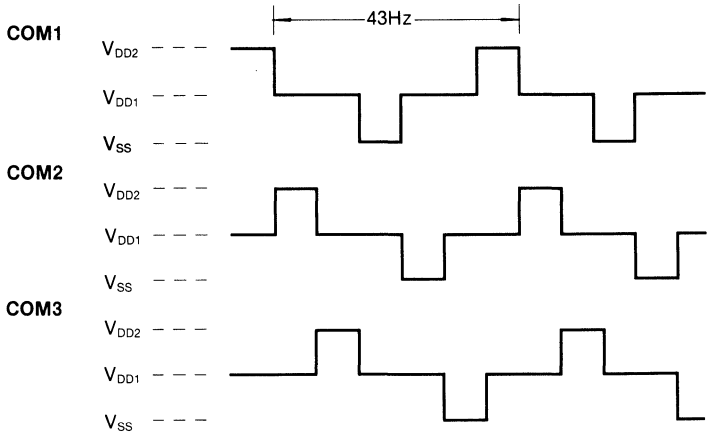
t1 = 25msec
t2 = 35msec

LCD FORMAT

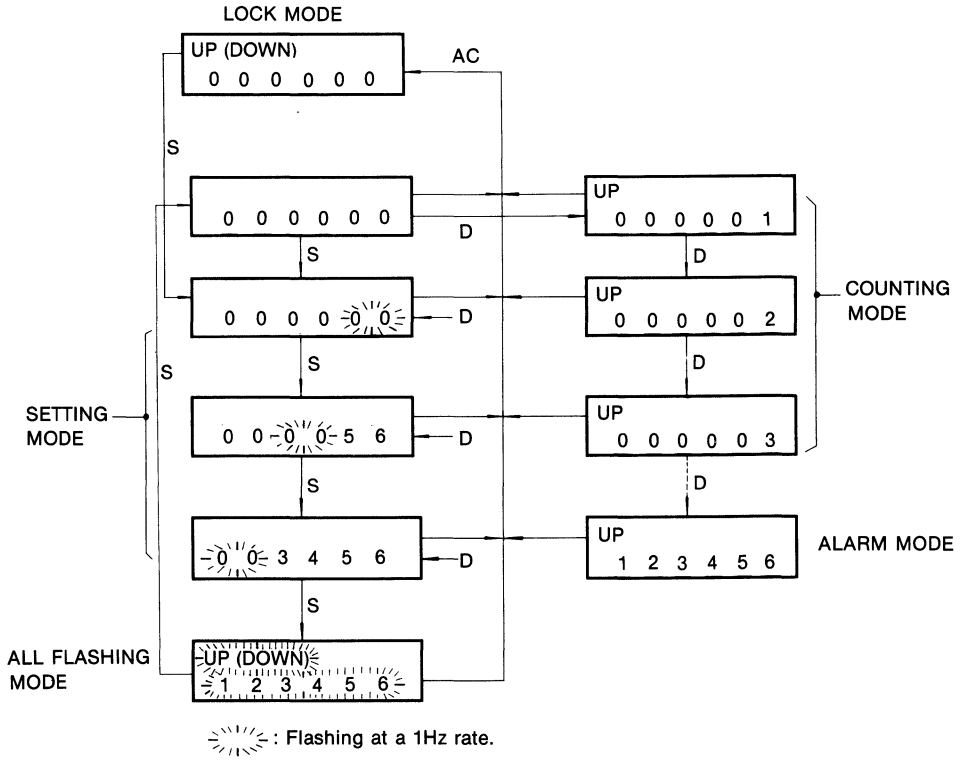


Pad No.	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19
COM1	U	D3	F1	A1	F2	A2	F3	A3	F4	A4	F5	A5	F6	A6	D4
COM2	D	D2	G1	B1	G2	B2	G3	B3	G4	B4	G5	B5	G6	B6	D5
COM3		D1	E1	C1	E2	C2	E3	C3	E4	C4	E5	C5	E6	C6	D6

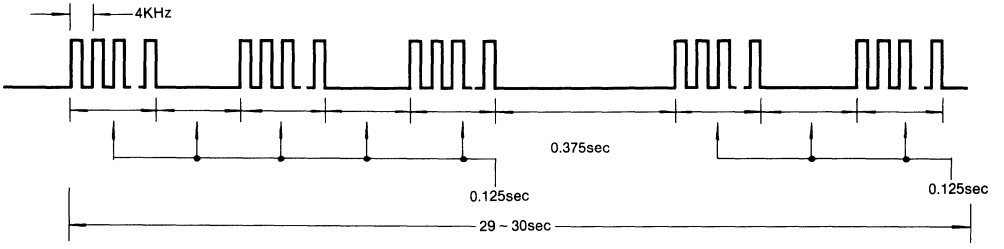
COMMON SIGNAL



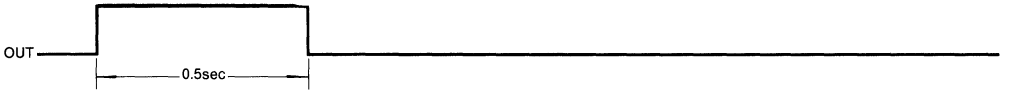
SETTING AND DISPLAY SEQUENCE



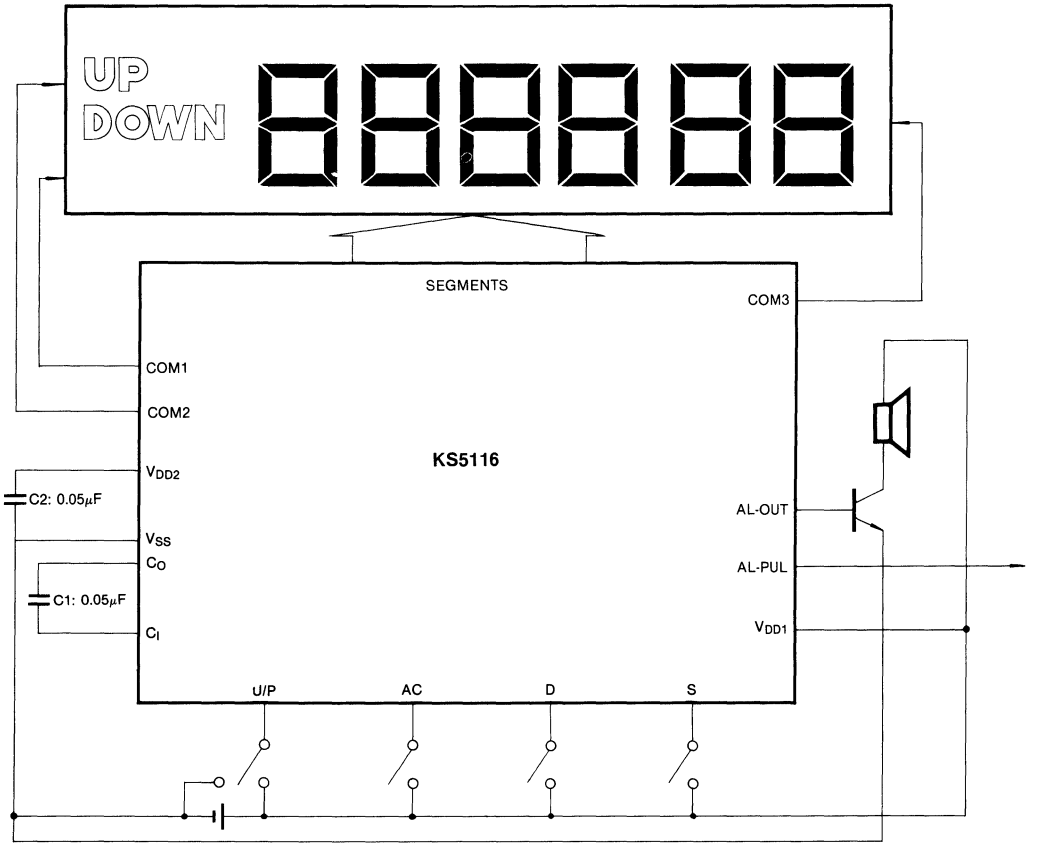
ALARM OUTPUT WAVEFORM



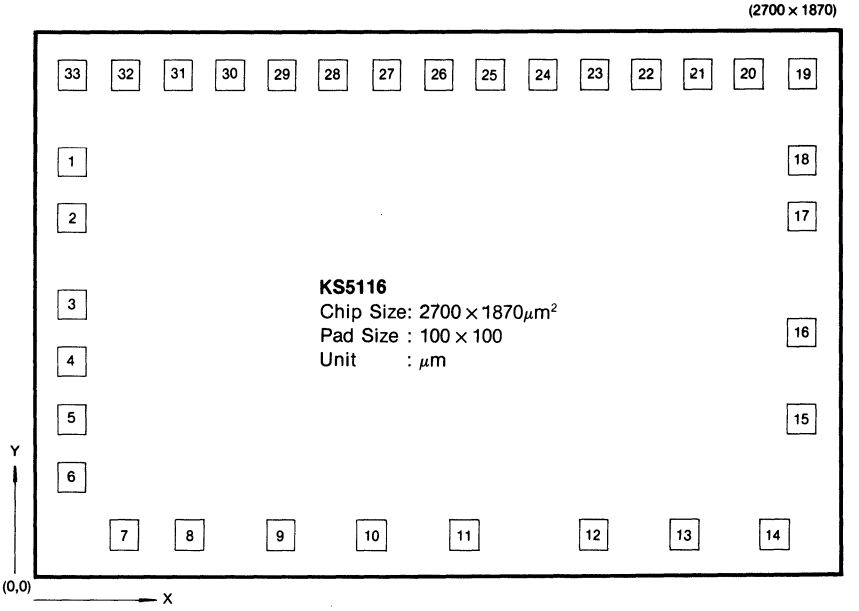
OUTPUT WAVEFORM



APPLICATION CIRCUIT



PAD DIAGRAM



PAD LOCATION

Pad No.	Pad Name	Coordinates		Pad No.	Pad Name	Coordinates		Pad No.	Pad Name	Coordinates	
		X	Y			X	Y			X	Y
1	COM2	184	1412	12	T_3	2007	186	23	$F_5G_5E_5$	1830	1685
2	COM1	184	1252	13	T_2	2189	186	24	$A_4B_4C_4$	1670	1685
3	V_{DD2}	184	1092	14	T_1	2499	186	25	$F_4G_4E_4$	1510	1685
4	V_{SS}	184	932	15	V_{DD1}	2517	468	26	$A_3B_3C_3$	1350	1685
5	CO	184	772	16	AL-PUL	2517	678	27	$F_3G_3E_3$	1190	1685
6	CI	184	612	17	AL-OUT	2517	902	28	$A_2B_2C_2$	1030	1685
7	OSC	364	184	18	COM3	2516	1398	29	$F_2G_2E_2$	870	1685
8	U/D_{SW}	630	185	19	$D_4D_5D_6$	2470	1685	30	$A_1B_1C_1$	710	1685
9	AC	1006	185	20	$A_6B_6C_6$	2310	1685	31	$F_1G_1E_1$	550	1685
10	D	1320	185	21	$F_6G_6E_6$	2150	1685	32	$D_3D_2D_1$	390	1685
11	S	1696	185	22	$A_5B_5C_5$	1990	1685	33	U/D	230	1685

CENTIGRADE/FAHRENHEIT CLINICAL THERMOMETER

The KS5815 is a CMOS digital CLINICAL THERMOMETER IC for measuring body temperature in centigrade of fahrenheit mode by its bonding option. It also provides alarm and automatic power off function. It was designed to interface directly to 3.5 digits and 4 flags.

FUNCTIONS

- Bonding option for centigrade/fahrenheit measurement
- Alarm to indicate temperature measuring time
- Highest temperature hold function
- Automatic power off function (10 minutes)
- 1 switch input operation

FEATURES

- **Single chip CMOS construction**
- **Drives 3.5 digits and 4 flags of duplexed LCD display**
- **On chip capacitive voltage doubler**
- **Single 1.5V battery operation**
- **Measurement accuracy : ±0.1°C (±0.3°F)**
  Measurement range : +32.0 ~ +43.0°C (+90.0 ~ +110.0°F)
  Resolution : 0.1°C (0.1°F)

6

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Supply Voltage ($V_{DD1} - V_{SS}$)	V_{DS1}	−0.1 ~ +3.0	V
Supply Voltage ($V_{DD2} - V_{SS}$)	V_{DS2}	−0.2 ~ +4.0	V
Operating Temperature	Topr	−10 ~ +60	°C
Storage temperature	Tstg	−40 ~ +125	°C

* Voltage greater than above may damage the circuit.

ELECTRICAL CHARACTERISTICS

(V_{SS} =0V, V_{DD1} = 1.5V, V_{DD2} = 3.0V, T_a =25°C, Unless otherwise noticed)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}		1.25	1.50	1.80	V
Operating Voltage	V_{DD2}		—	3.00	—	V
Current Consumption	|Isup1|		—	—	100	μA
Current Consumption	|Isup2|	Power off	—	—	0.1	μA
Output Current (COM1, COM2) V_{DD1}	Ioh1	Voh1=1.3V	—	—	−60.0	μA
	Iol1	Vol1=0.3V	60.0	—	—	
Output current (COM1, COM2) V_{DD2}	Ioh2	Voh2=2.7V	—	—	−40.0	μA
Output Current (Segment, COM3)	Ioh3	Voh3=2.7V	—	—	−20.0	μA
	Iol3	Vol3 = 0.3V	20.0	—	—	
Output Current (Alarm)	Ioh4	Voh4=1.3V	—	—	−80.0	μA
Input Current (SW)	Iih1	Vih1=1.5V	0.1	1.0	10.0	μA
	Iil1	Vil1 = 0.0V	—	—	0.1	

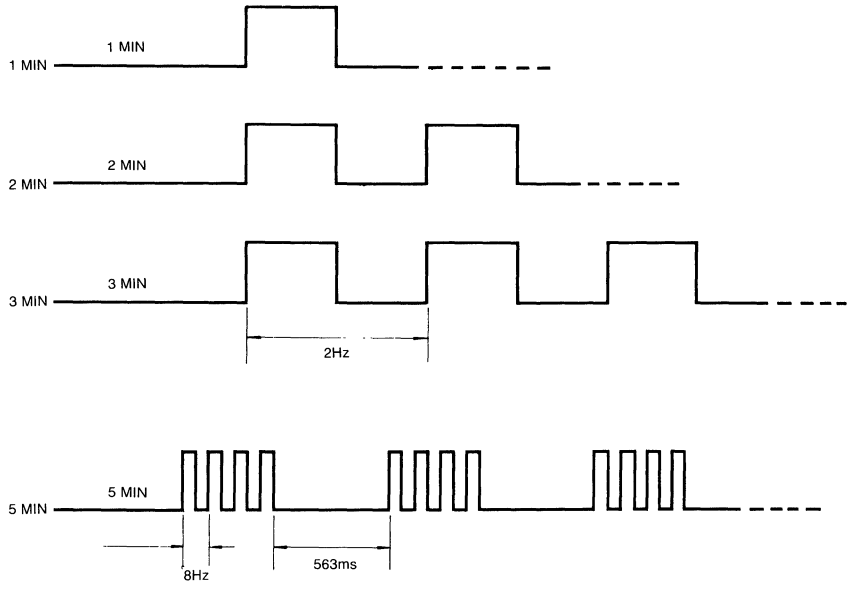
FUNCTIONAL DESCRIPTION

• BONDING OPTION

The centigrade or fahrenheit mode is selected by bonding option. If the pad MS is left open, the all circuits are used as the centigrade mode. On the other hand, to use as the fahrenheit mode, MS should be connected with V_{DD}.

• ALARM FUNCTION

Once the switch is pressed, after 1, 2, 3 and 5 minutes, the corresponding alarm of each minute is generated to notice the end point each measuring time. The output waveforms are shown below at the alarm out terminal. And, at this time, alarm tone of 4094Hz frequency is modulated by frequency corresponding to each minute.



• HIGHEST TEMPERATURE HOLD FUNCTION

To read out the measured temperature value displayed on LCD, the CLINICAL THERMOMETER should be taken out of body. At this time, the displayed value can be changed by this reason. So, once the temperature measured, the LSI has the highest temperature hold function which prevents the change of measured temperature value on LCD. Also, the displayed highest temperature measured value will be kept until power off.

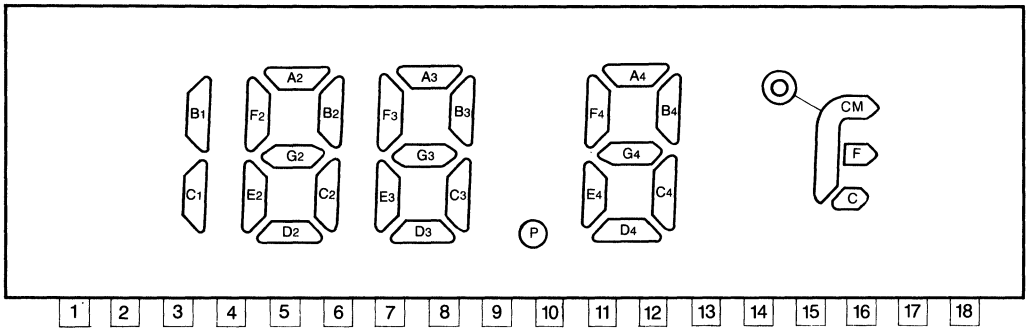
• AUTOMATIC POWER OFF FUNCTION

Automatic power off function is executed after 10 minutes passed from the time of SW pressure to power on, except when the pad, APOD, is connected with V_{DD}.

• SWITCH OPERATION

If the switch SW is depressed during power off condition, then temperature measuring operation is activated to power on state and LCD begins to display the present temperature or LO/HI condition at 1Hz rate. Conversely, if SW is depressed during power on condition, the all operations stops in power off state and the all fonts on LCD are removed.

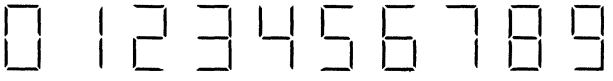
LCD FORMAT



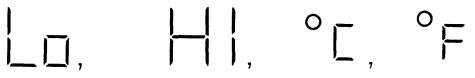
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
COM1		BC1	E2	D2	C2	A3	E3	D3	C3	P	E4	D4	C4				
	COM2	A2	F2	G2	B2	A4	F3	G3	B3		F4	G4	B4				
														CM	C	F	COM3

DISPLAY FONTS

- **NOMERICAL FONTS**

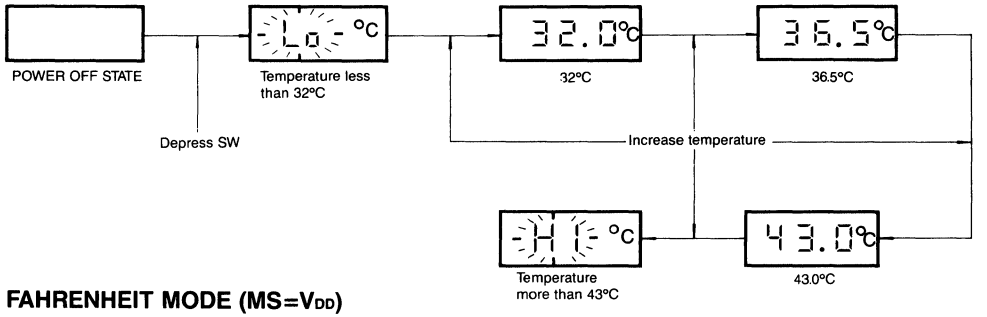


- **CHARACTER FONTS**

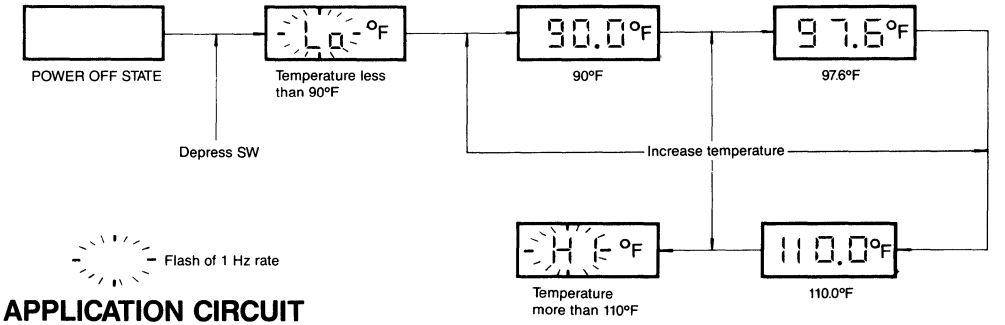


DISPLAY CONDITION

CENTIGRADE MODE (MS=OPEN)



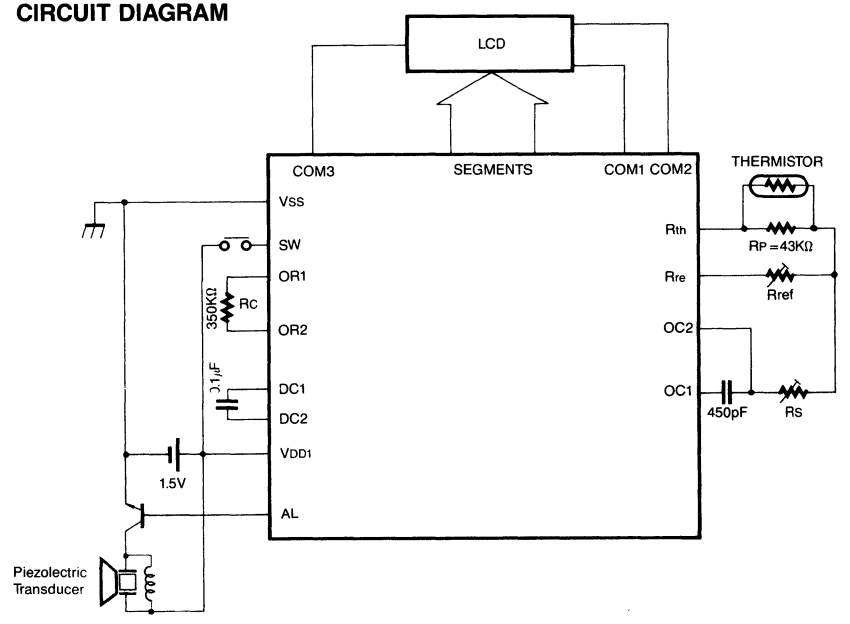
FAHRENHEIT MODE (MS=V_{DD})



Flash of 1 Hz rate

APPLICATION CIRCUIT

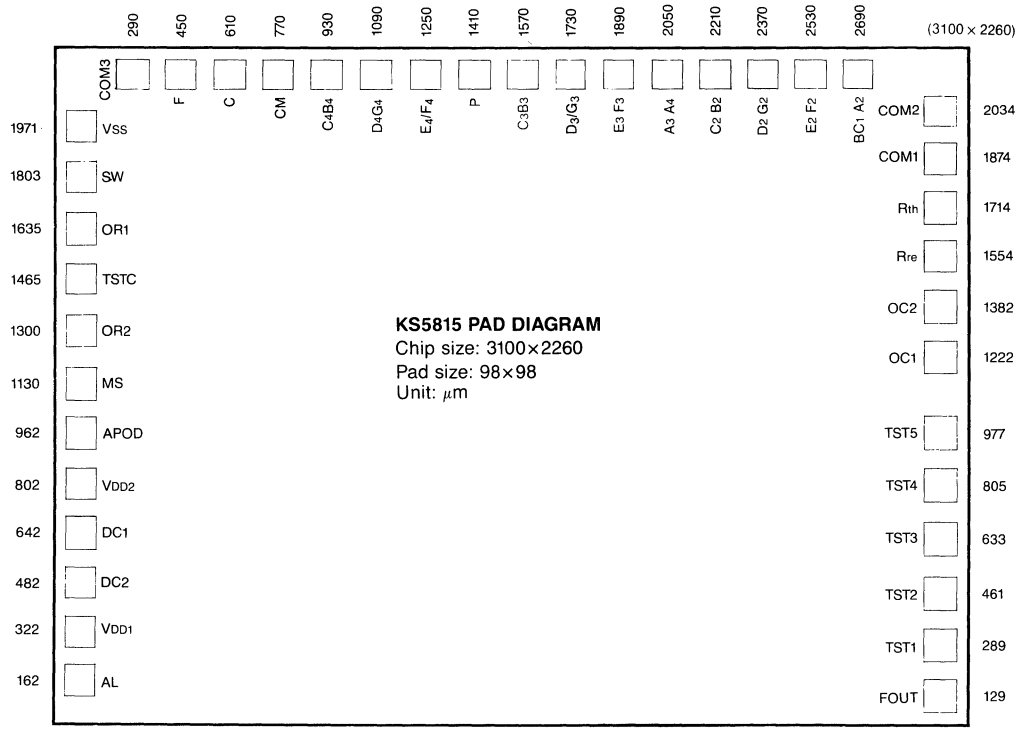
CIRCUIT DIAGRAM



PAD ASSIGNMENT

Pad No.	Signal	I/O	Description	Pad No.	Signal	I/O	Description
1	FOUT	O	OSC. Test Output	21	P	O	Display Output
2	TST1	I	Test Input	22	E4F4	O	Display Output
3	TST2	I	Test Input	23	D4G4	O	Display Output
4	TST3	I	Test Input	24	C4B4	O	Display Output
5	TST4	I	Test Input	25	CM	O	Display Output
6	TST5	I	Test Input	26	C	O	Display Output
7	OC1		Capacitor terminal for oscillator	27	F	O	Display Output
8	OC2		Capacitor terminal for oscillator	28	COM3	O	Display Output
9	Rre		Resistor terminal for oscillator	29	V_{SS}		Power Supply
10	R_{th}		Resistor terminal for oscillator	30	SW	I	Switch terminal for Power ON/OFF
11	COM1	O	Display Output	31	OR1		Resistor terminal for oscillator
12	COM2	O	Display Output	32	TSTC	O	Capacitor test output
13	BC1A2	O	Display Output	33	OR2		Resistor terminal for oscillator
14	E2F2	O	Display Output	34	MS	I	°F/°C Mode select input
15	D2G2	O	Display Output	35	APOD	I	Auto power off disable input
16	C2B2	O	Display Output	36	V_{DD2}		Power Supply
17	A3A4	O	Display Output	37	DC1		Capacitor terminal for doubler
18	E3F3	O	Display Output	38	DC2		Capacitor terminal for doubler
19	D3G3	O	Display Output	39	V_{DD1}		Power Supply
20	C3B3	O	Display Output	40	AL	O	Alarm Output

PAD DIAGRAM



6

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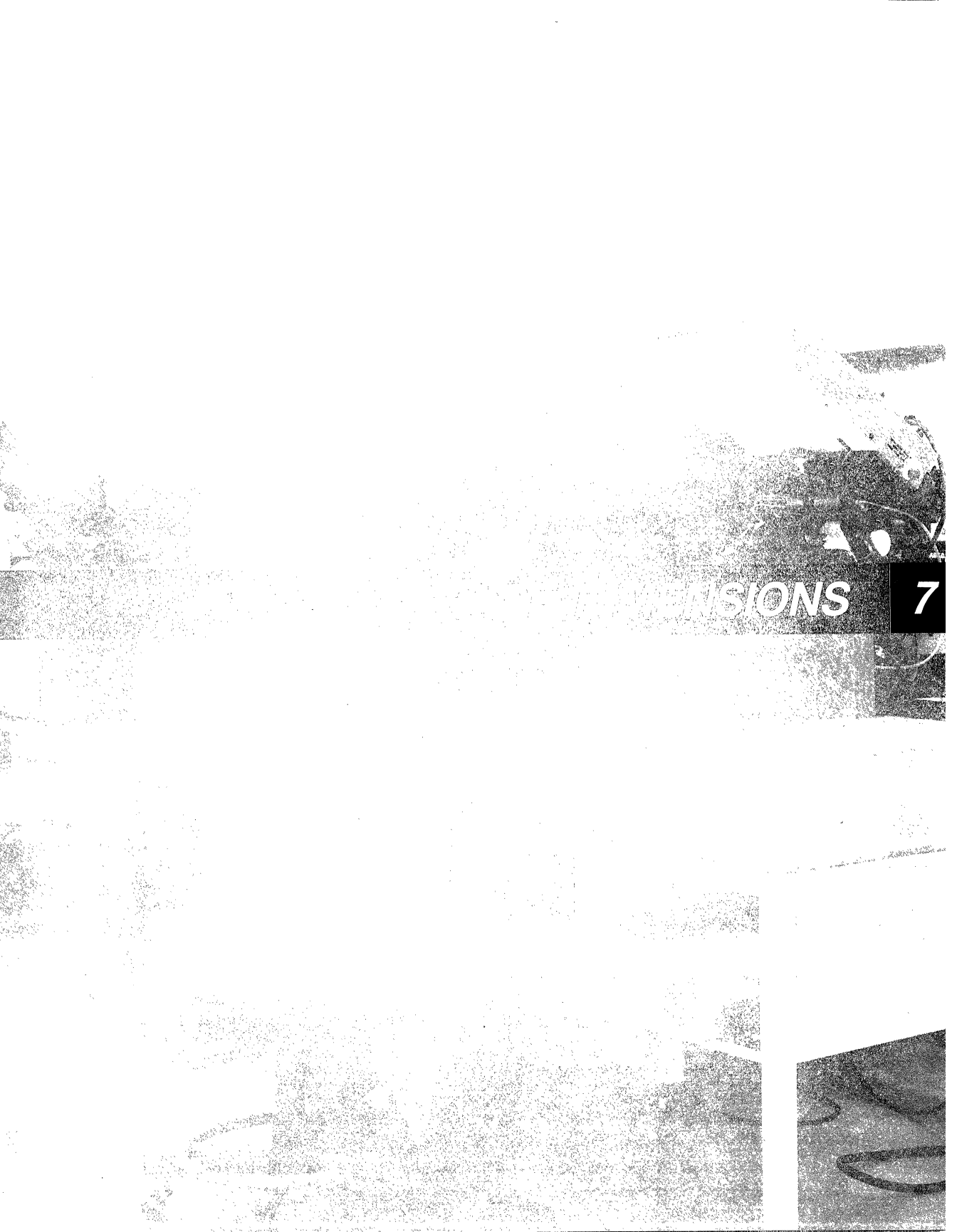
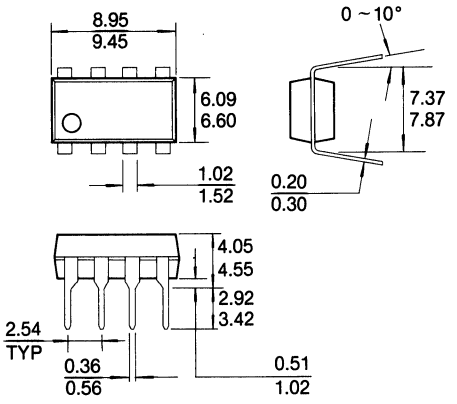

VERSIONS
7

PACKAGE DIMENSIONS

8 DIP

Unit: mm



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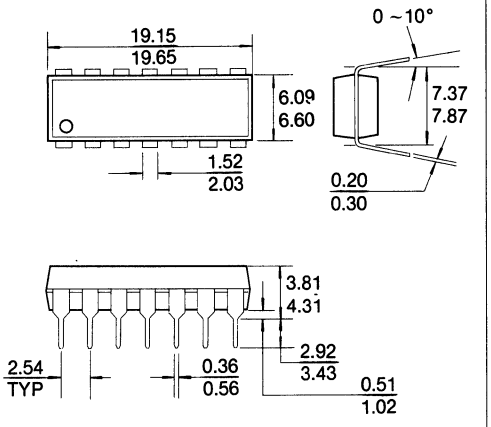

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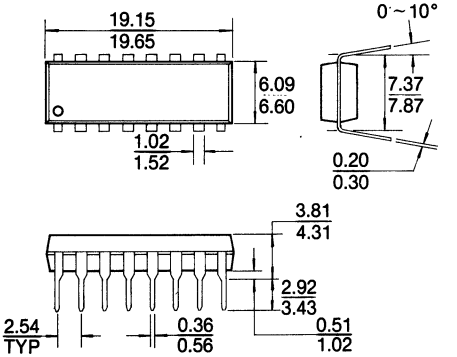

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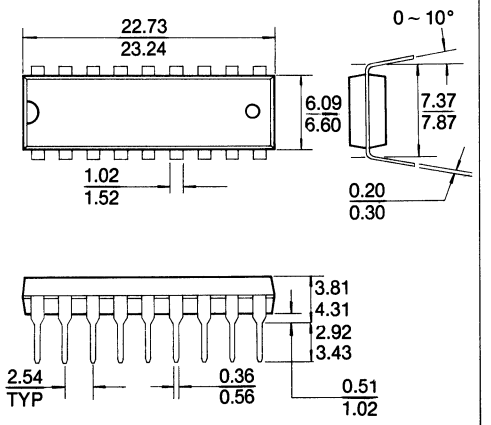

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PACKAGE DIMENSIONS

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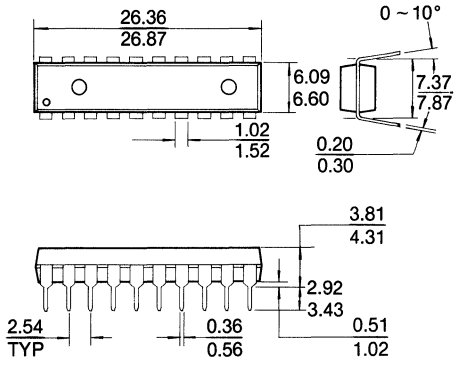
Unit: mm



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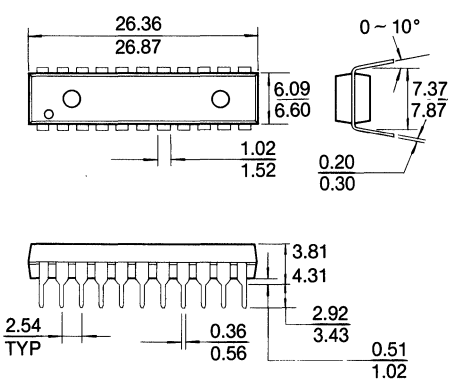

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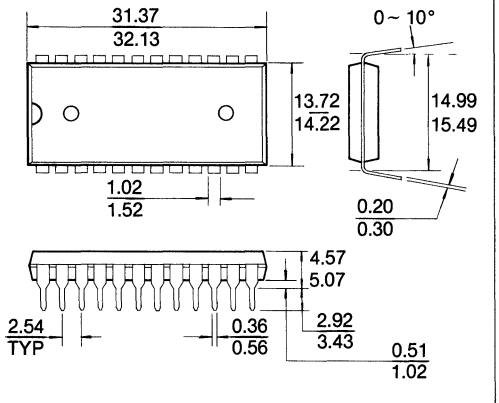

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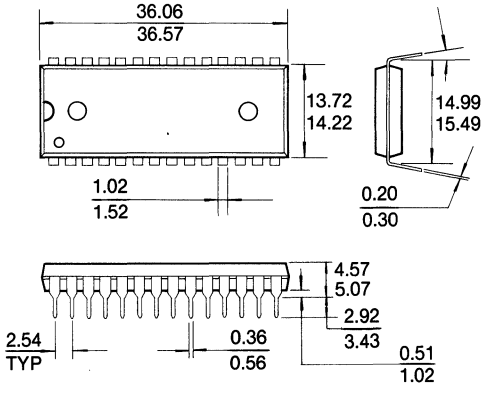

PACKAGE DIMENSIONS

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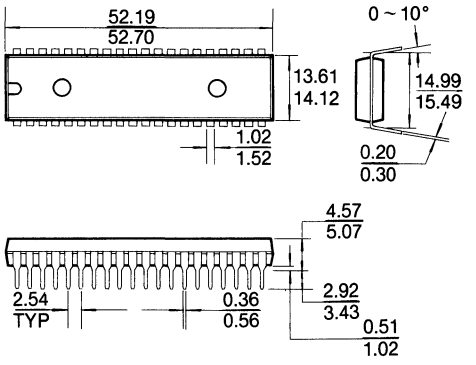

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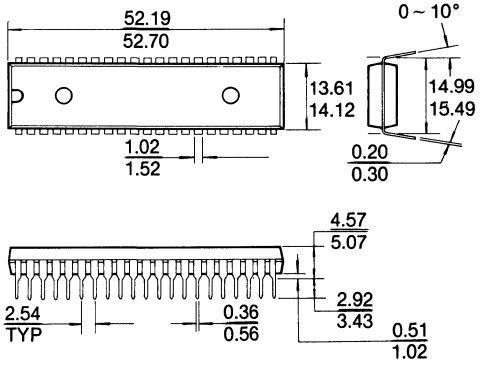
Unit: mm



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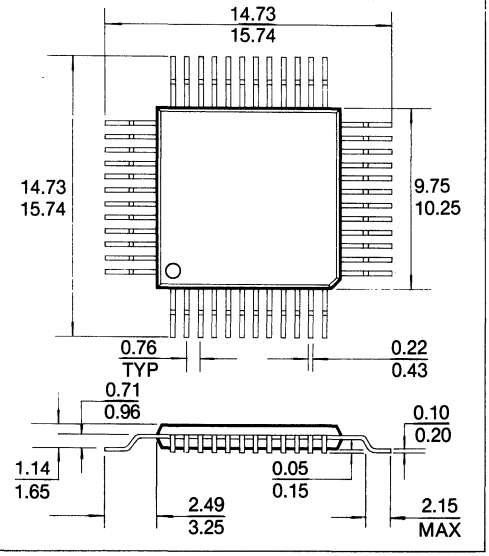
Unit: mm



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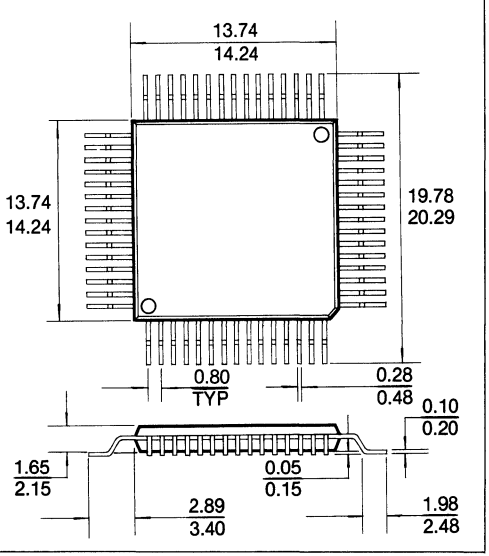
Unit: mm



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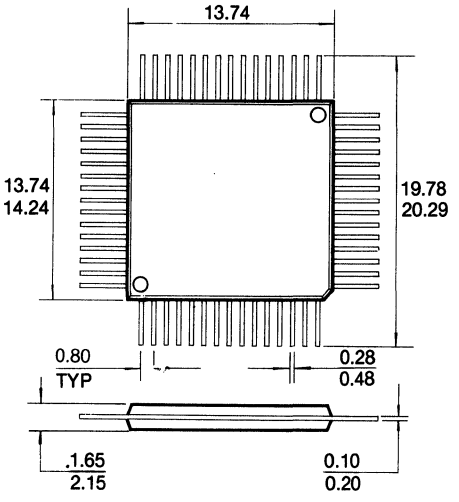
PACKAGE DIMENSIONS

60 FQP **Unit: mm**



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201 East Sandpoint
Suite 220 Santa Ana 92707
714-662-3406

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Suite 198 Santa Clara 95054
408-727-7433

MASSACHUSETTS

20 Burlington Mall Road
Suite 205 Burlington 01803
617-273-4888

ILLINOIS

901 Warrenville Rd.
Suite 120 Lisle, 60532-1359
312-852-2011

TEXAS

15851 Dallas Parkway
Suite 745
Dallas 75248-3307
214-239-0754

NORTH CAROLINA

3200 Nothline Ave
Suite 501G
Forum VI Greensboro, 27408
919-294-5141

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ALABAMA

EMA

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Jordan Center
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205-536-3044

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Scottsdale 85252
602-994-3813

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WESTAR REP COMPANY

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COLORADO

ELECTRODYNE

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PHOENIX SALES

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Palm Harbor, 33563
813-784-8561

ILLINOIS

IRI

8430 Gross Pointe Road
Skokie 60076
312-967-8430

INDIANA

STB & ASSOCIATES
3003 E. 96th Street
Suite 102 Indianapolis 46240
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C.B. JENSEN & ASSOC.
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Troy 48084
313-643-0506

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Lithicum 21090
301-789-9360

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Minneapolis, 55418
612-788-9234

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NECCO
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Ft. Lee 07024
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Contact local sales office

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Contact local sales office

OREGON

EARL & BROWN
7719 S. W. Capitol Highway
Portland 97219
503-245-2283

NEW YORK

NECCO
2460 Lemoine Avenue
Ft. Lee 07024
201-4611-2789

OHIO

J.N. BAILEY & ASSOCIATES
13071 Old Dayton Road
New Lebanon 45345
513-687-1325

1667 Devonshire Drive
Brunswick 44212
216-273-3798

2679 Indianola Avenue
Columbus 43202
614-262-7274

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RIVCO JANUARY, INC.
78 South Trooper Road
Norristown 19403
215-631-1414

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Greenville, 29609
803-233-4637

TEXAS

VIELOCK ASSOCIATES
720 E. Park Boulevard
Suite 102 Plano 75074
214-881-1940

UTAH

ELECTRODYNE
2480 South Main Street
Suite 109 Salt Lake City 84115
801-486-3801

WISCONSIN

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631 Mayfair
Milwaukee 53226
414-259-0965

WASHINGTON

EARL & BROWN
2447-A 152nd Avenue, N.E.
Redmond 98052
206-885-5064

EUROPE

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SATRON HANDELSGES. GmbH
Hoffmeistergasse 8-10/1/15
A-1120 Wien
Tel: 0043-222-87 30 20
Tlx: 047-753 11 85 1
Fax: 0043-222-83 35 83

BELGIUM

C&S ELECTRONICS INTERNATIONAL
Leuvensesteenweg 186
B-1940 Sint-Stevens-Woluwe
Tel: 0032-2-7 25 09 00
Tlx: 046-2 58 20
Fax: 0032-2-7 25 08 13

FINLAND

INSTRUMENTARIUM ELEKTRONIIKKA
P.O. Box 64, Vitikka 1
SF-02631 Espoo
Helsinki
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Tlx: 057-12 44 26
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FRANCE

ASIA MOS (OMNITECH)
Bâtiment Evolic 1
165, Boulevard de Valmy
F-92705 Colombes
Tel: 0033-1-47 60 12 47
Tlx: 042-61 38 90
Fax: 0033-1-47 60 15 82

MICRORAM (SCAIB)
6, Rue le Corbusier
Silic 424
F-94583 Rungis Cedex
Tel: 0033-1-46 86 81 70
Tlx: 042-20 69 52
Fax: 0033-1-45 60 55 49

GERMANY

ASTRONIC GmbH
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D-8024 Deisenhofen
Tel: (49) 0-89-61 30 303
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Tlx: 17 89 84 53
Fax: (49) 0-89-23 03 52 98

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Via Ala di Stura /1/18
I-10148 Torino
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240 Bjs.
E-08006 Barcelona
Tel: 0034-3-2 17 23 40
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SWEDEN
MIKO KOMPONENT AB
Segersbyvägen 3
P.O. Box 2001
S-14502 Norsborg
Tel: 0046-753-89 08 0
Tlx: 054-150 23
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INDIA

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PARRY HOUSE' 3rd floor 43 Moore Street
MADRAS 600 001 India
Tel: 21019/31003
Tlx: 041-8797 HIL IN

PARRRY HOUSE' 3rd floor 43 Moore Street

4. KOREA

NAEWAE ELECTRIC CO., LTD.
Room 403, 22Dong Sumin Bldg,
#16-1, Hangangro-2ka, Yongsanku.
Seoul Korea.
Tel: 701-7341~5
Fax: 717-7246

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Jongroku, Seoul Korea
Tel: 744-2110, 269-6187/8
Fax: 744-4803

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182-2 Jang Sa Dong
Jongroku, Seoul Korea
Tel: 701-6811~6
Fax: 701-6785

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Joongku, Seoul Korea
Tel: 274-3220, 3458

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1131-9 Kurodong, Kuroku,
Seoul Korea
Tel: 868-0277~9
Fax: 868-4604

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CHUNG-KU, SEOUL, KOREA
C.P.O. BOX 8233

TELEX: KORSST K27970
TEL: (SEOUL) 751-2114
FAX: 753-0967

BUCHEON PLANT:
82-3, DODANG-DONG,
BUCHEON, KYUNGKI-DO, KOREA
C.P.O. BOX 5779 SEOUL 100

TELEX: KORSEM K28390
TEL: (SEOUL) 741-0066, 662-0066
FAX: 741-4273

KIHEUNG PLANT:
SAN #24 NONGSUH-RI, KIHEUNG-MYUN
YONGIN-GUN, KYUNGKI-DO, KOREA
C.P.O. BOX 37 SUWON

TELEX: KORSST K23813
TEL: (SEOUL) 741-0620/7
FAX: 741-0628

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KYUNGSANGBUK-DO, KOREA

TELEX: SSTGUMI K54371
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FAX: (GUMI) 52-7942

SAMSUNG SEMICONDUCTOR INC.:
3725 NORTH FIRST STREET
SANJOSE, CA 95134-1708, USA

TEL: (408) 434-5400
TELEX: 339544
FAX: (408) 434-5650

HONG KONG BRANCH:
24/F Tower I Admiralty Centre
18 Harcourt Road
Hong Kong

Tel: 5-8626900
Tlx: 80303 SSTC HX
Fax: 5-8661343

TAIWAN OFFICE:
RM B, 4FL, NO 581
TUN-HWA S, RD, TAIPEI, TAIWAN

TEL: (2) 706-6025/7
FAX: (2) 706-6028

SAMSUNG JAPAN CO.:
SUDACHO VERDE BLDG. 2-3,
KANDASUDACHO CHIYODA-KU,
TOKYO, 101, JAPAN

TEL: (03) 258-9506
TELEX: 2225206 SECJPNJ
FAX: (03) 258-9696

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TEL: 0-6196-90090
FAX: 0-6196-900989
TLX: 4072678 SSED

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